400038

National Semiconductor

Low Voltage Databook

Logic (LVQ)
Interface
Real Time Clocks
Clock Generation and Support (CGS)
Linear
EPROM, EEPROM, and SRAM
ASIC
Embedded Controllers

LOW VOLTAGE
DATABOOK

1992 Edition

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SuperChip™
SuperScript™
SYS32™
TapePak®
TDS™
TeleGate™
The National Anthem®
Time✓Chek™
TINA™
TLC™
Trapezoidal™
TRI-CODE™
TRI-POLY™
TRI-SAFE™
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INTRODUCTION

National Semiconductor is a leading supplier of low voltage semiconductors and offers an extensive breadth of low voltage products targeted for battery-operated and high performance computing systems. This data book, which contains National's initial low voltage portfolio, demonstrates a strong commitment to the future of low voltage semiconductor intensive applications. As National's low voltage portfolio continues to grow so will the data book. Future low voltage devices will be included in subsequent editions of the Low Voltage Data Book.

This data book is a design tool for design, component and system engineers to support low voltage system designs with National components. The products found in this data book are specified for low voltage operation and include Logic, Interface, Clock Circuits, Linear, ASIC, Memory and Embedded Controllers. Also included is technical information relevant to low voltage designs.

The Low Voltage Data Book is consistent with National Semiconductor's mission to excel in serving chosen markets, by delivering semiconductor-intensive products and services of the highest quality and value, thereby providing a competitive advantage to our customers worldwide.

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Section 1

Low Voltage Logic (LVQ)

Section 1 Contents

National Semiconductor

LVQ Descriptions and Family Characteristics

In 1985, a family of high speed advanced CMOS circuits was introduced. FACT™ (Fairchild Advanced CMOS Technology) Logic offered a combination of high speed, low power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability.

The 1.3-micron silicon gate CMOS process utilized in this family was proven in the field of high performance gate arrays, CMOS ASIC, and FACT. It was further enhanced to meet JEDEC standards for 74ACXX logic. In 1989, National Semiconductor introduced the FACT Quiet Series™ product line. This line of mostly octal bus-oriented logic functions is an enhancement of the original FACT line. Manufactured on a sub-micron silicon gate CMOS process, the FACT QS devices offer the lowest noise characteristics of any Advanced CMOS process with AC performance that is faster than FACT.

National's introduction of Low Voltage CMOS products in 1992 incorporates the advantages found in both the FACT and FACT QS product lines. The 'LVQ product line operates at 3.3V ±0.3V and uses the Quiet Series design techniques in the octal functions.

This data book describes the product line with device specification as well as material discussing design considerations and compares the 'LVQ family to predecessor technologies.

Characteristics

- Operating range 3V ±0.3V Guaranteed (operation from 2V–6V V_{DD})
- Industry Standard Functions and Pinouts
- Common Output Specifications for Standard Gates and Buffer/Drivers
- Temperature Range
  - — Commercial −40°C to +85°C
  - — Military −55°C to +125°C
- Improved ESD Protection, typically >4000V
- Improved Latch-Up Immunity
- Guaranteed incident wave switching into 75Ω
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Interfacing

While 'LVQ devices have a wide operating voltage range (V_{DD} = 2 V_{DC} to 6 V_{DC}), the specs herein are guaranteed for 3V ±0.3V operation. 'LVQ has sufficient current drive to interface with most other logic families available today, with CMOS input switching levels and buffered CMOS outputs that can drive ±12 mA of I_{OH} and I_{OL} current. Industry standard nomenclature and pinouts are used. See the section titled Design Considerations, for more details.

Low Voltage/Low Power CMOS Operation

Low power dissipation has always been the hallmark of CMOS devices. Together with a low voltage operating environment, the combination is unbeatable for battery operated computing systems such as laptop computers, notebook PCs, pen-based systems and palmtops.

In the quiescent state, 'LVQ draws 1000 times less power than the equivalent LS or ALS TTL device. This enhances system reliability, because costly regulated high current power supplies, heat sinks and fans are eliminated. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

LVQ =	0.1 mW/Gate
HCMOS =	0.1 mW/Gate
FACT =	0.1 mW/Gate
ALS =	1.2 mW/Gate
LS =	2.0 mW/Gate

Figure 1.1-1 illustrates the effects of I_{DD} versus power supply voltage (V_{DD}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

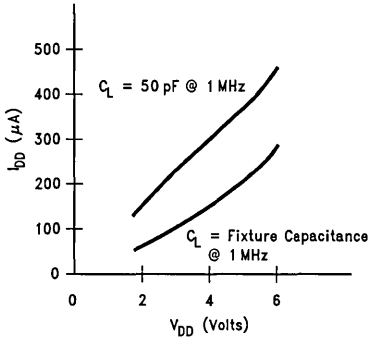

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FIGURE 1.1-1. I_{DD} vs V_{DD}

Product Comparison

Feature	LVQ	FACT AC/ACT	FACT ACQ/ACTQ
Dynamic line driving guaranteed to switch on incident wave into transmission line impedance as low as 50Ω at +85°C; 75Ω at +125°C	Yes* I_{OLD} = 36 mA I_{OHD} = −25 mA	Yes I_{OLD}/I_{OHD}: ±75 mA	Yes I_{OLD}/I_{OHD}: ±75 mA
Guaranteed High Output Drive	I_{OL}/I_{OH}: ±12 mA	I_{OL}/I_{OH}: ±24 mA	I_{OL}/I_{OH}: ±24 mA
Very High Speed Frequency	≤1 ns Internal Gate Delay; up to 100 MHz Toggle Frequency	1 ns Internal Gate Delay; up to 100 MHz Toggle Frequency	≤1 ns Internal Gate Delay; up to 100 MHz Toggle Frequency
CMOS Power	5 μW/Gate	5 μW/Gate	5 μW/Gate
CMOS Input Loading	±1 μA	±1 μA	±1 μA
Extended Operating Voltage Range	2.0V to 6.0V	2.0V to 6.0V	2.0V to 6.0V
DC/AC Characteristics Guaranteed	3.3V ±0.3V	3V and 5V ±10%	3V and 5V ±10%
Excellent Symmetrical Noise Margin (CMOS Inputs)	0.9V High 0.7V Low	1.55V High; 1.55V Low	1.55V High; 1.55V Low
Dynamic Thresholds (TTL-Compatible Inputs)	Maximum 2.0V High (V_{IHD}); Minimum 0.8V Low (V_{ILD})		Maximum 2.2V High (V_{IHD}); Minimum 0.8V Low (V_{ILD})
Guaranteed Latchup Immunity	±300 mA at +125°C	±100 mA at +125°C	±300 mA at +125°C
ESD Immunity	MIL Class 2 (2,000V − 3,999V); Typical 6,000V	MIL Class 2 (2,000V − 3,999V); Typical 6,000V	MIL Class 2 (2,000V − 3,999V); Typical 6,000V
Pin-to-Pin Output Propagation Delay Skew (Maximum)	1.5 ns (t_{OS}); Typical 1.0 ns		1.0 ns (t_{OS}); Typical 0.5 ns
Guaranteed Output Noise Levels (Maximum)	Octals: 0.8V V_{OLP} (Ground Bounce); −0.8V V_{OLV} (Undershoot) Others: See Datasheet Guarantees		2.1V V_{OLP} (Ground Bounce); −1.2V V_{OLV} (Undershoot)
Inherently Radiation Tolerant	Yes	Yes	Yes
Inputs Compatible with: CMOS TTL	LVQ LVQ	AC ACT	ACQ ACTQ
Full Compatibility (Function, Part Number, Pinout) with Standard 54/74 Functions	Yes	Yes	Yes (≥8 Bits)

*Dynamic line driving guaranteed to switch on incident wave into transmission line impedance as low as 75Ω at +85°C.

AC Performance

In comparison to LS, ALS and HC families, 'LVQ devices have faster internal gate delays as well as the basic gate delays. Additionally, as the level of integration increases, 'LVQ logic lends itself to systems operating up to 33 MHz while maintaining low power consumption.

The examples below describe typical values for a 74XX138, 3-to-8 line decoder and a 74xx244 line driver.

'138	
LVQ	= 8.0 ns @ C_L = 50 pF at 3.3V
FACT AC	= 6.0 ns @ C_L = 50 pF at 5.0V
ALS	= 12.0 ns @ C_L = 50 pF at 5.0V
LS	= 22.0 ns @ C_L = 15 pF at 5.0V
HC	= 17.5 ns @ C_L = 50 pF at 5.0V

'244	
LVQ	= 7.0 ns @ C_L = 50 pF at 3.3V
FACT ACQ	= 4.0 ns @ C_L = 50 pF at 5.0V
FACT AC	= 5.0 ns @ C_L = 50 pF at 5.0V
ALS	= 7.0 ns @ C_L = 50 pF at 5.0V
LS	= 12.0 ns @ C_L = 45 pF at 5.0V
HC	= 14.0 ns @ C_L = 50 pF at 5.0V

'LVQ AC performance specifications are guaranteed at 3.3V ±0.3V. For worst case design at 2.0V V_{DD} on all device types, the formula below can be used to determine AC performance.

AC performance at 2.0V V_{DD} = 1.9 × AC specification at 3.3V.

Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 3.3V ±0.3V V_{DD}.

Noise Immunity

The DC noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL} - V_{OL}|/|V_{IH} - V_{OH}|$ at worst case V_{DD}.

LVQ	= 0.7V/0.9V @3.0V V_{DD}
FACT	= 1.25V/1.25V @4.5V V_{DD}
ALS	= 0.4V/0.7V @ 4.5V V_{DD}
LS	= 0.3V/0.7V @ 4.75V V_{DD}
HC	= 0.8V/1.25V @ 4.5V V_{DD}

Output Characteristics

All 'LVQ outputs are buffered to ensure consistent output voltage and current specifications across the family. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system application which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times. In order to minimize device generated noise, the octal devices incorporate Quiet Series technology design and process techniques. All SSI and octal 'LVQ devices are guaranteed to sink and source 12 mA. The 'LVQ devices are capable of driving 75Ω transmission lines.

I_{OL}/I_{OH} Characteristics

LVQ	= 12 mA/−12 mA @3.0V V_{DD}
FACT AC/ACT	= 24 mA/−24 mA @4.5V V_{DD}
FACT ACQ/ACTQ	= 24 mA/−24 mA @4.5V V_{DD}
ALS	= 24 mA/−15 mA @4.5V V_{DD}
LS	= 8 mA/−0.4 mA @4.75V V_{DD}
HC	= 4 mA/−4 mA @4.5V V_{DD}

Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied "typical" output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these "typical" performance values across the operating voltage and temperature limits. Fortunately for the system designers, 'LVQ has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 75Ω for the commercial temperature range.

Figure 1.1-2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ($I_{OUT} > 0$), are the V_{OH} and I_{IH} curves for 'LVQ logic while on the left side ($I_{OUT} < 0$), are the curves for V_{OL} and I_{IL}. Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.

Begin analysis at the V_{OL} (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the V_{IN}/I_{IN} curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a 75Ω load line from this intersection to the V_{OH}/I_{OH} curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 2.85V. Then draw a line with a slope of −75Ω from this first intersection point to the V_{IN}/I_{IN} curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

Dynamic Output Drive (Continued)

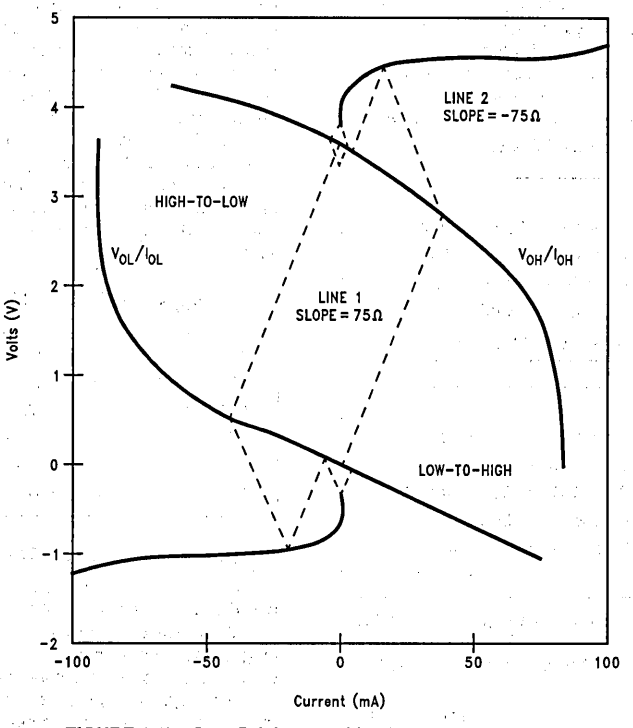

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FIGURE 1.1-2. Gate Driving 75Ω Line Reflection Diagram

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the V_{IN}/I_{IN} curve will be waves travelling from the receiver to the driver.

While this exercise can be done for 'LVQ, it is no longer necessary. 'LVQ is guaranteed to drive an incident wave of enough voltage to switch another 'LVQ input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either at V_{IH} or V_{IL} levels. The formula for calculating the current and voltage required is $|(V_{OQ} - V_I)/Z_O|$ at V_I. For V_{OQ} = 100 mV, V_{IH} = 2.00V, V_{DD} = 3.6V and Z_O = 75Ω, the required I_{OH} at 2.0V is 25.0 mA. For the HIGH-to-LOW transition, V_{OQ} = 3.5V, V_{IL} = 0.8V and Z_O = 75Ω, I_{OL} is 36 mA at 0.8V. 'LVQ's I/O specifications include these limits. For transmission lines with impedances greater than 75Ω, the current requirements are less and switching is still guaranteed.

It is important to note that the typical 12 mA DC drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IN} level.

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of 'LVQ devices with various power supply voltages.

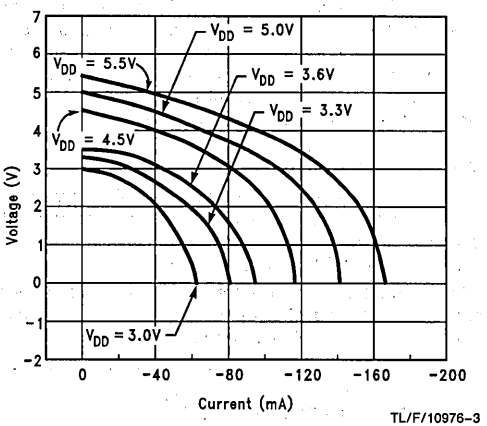

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FIGURE 1.1-3. Output Characteristics V_{OH}/I_{OH}, 'LVQ244

Dynamic Output Drive (Continued)

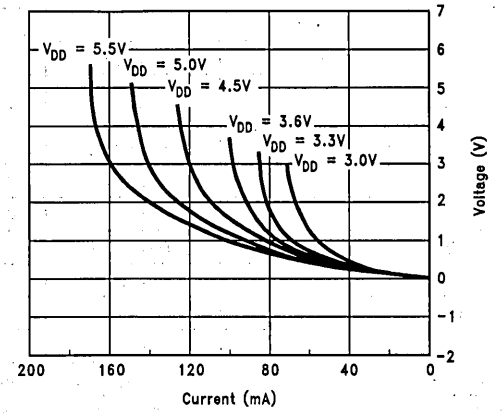

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FIGURE 1.1-4. Output Characteristics V_{OL}/I_{OL}, 'LVQ244

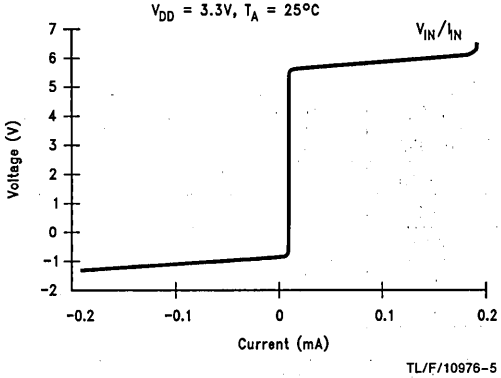

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FIGURE 1.1-5. Input Characteristics V_{IN}/I_{IN}

Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at 3.3V ±0.3V. To this end, National Semiconductor guarantees all of its devices operational at 3.3V ±0.3V.

Operating Voltage Ranges

LVQ	= 3.3V ±0.3V ('LVQ)
FACT	= 2.0V to 6.0V ('AC/'ACQ)
FACT	= 5.0V ±10% ('ACT/'ACTQ)
FACT	= 5.0V ±5% ('FCT/'FCTA)
HC	= 2.0V to 6.0V

Logic Comparisons

Figure 1.1-6 shows the relative position of various logic families in speed/power performance. 'LVQ exhibits 1 ns internal propagation delays while consuming 1 μW of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

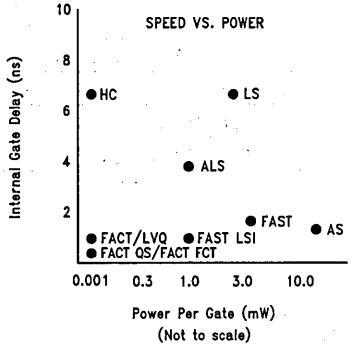

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FIGURE 1.1-6. Internal Gate Delays

General Characteristics (All Max Ratings)

Symbol	Characteristics	LVQ	FACT			Units
			'AC/'ACQ	'ACT/'ACTQ	HCMOS	
$V_{CC/EE/DD}$	Operating Voltage Range	3.3 ±0.3V	5 ±5%	5 ±10%	5 ±10%	V
T_A 74 Series T_A 54 Series	Operating Temperature Range	−40 to +85 −55 to +125	−40 to +85 −55 to +125	−40 to +85 −55 to +125	−40 to +85 −55 to +125	°C
V_{IH} (Min)	Input Voltage (Limits)	2.0	3.15	3.85	2.0	V
V_{IL} (Max)		0.8	0.9	1.65	0.8	V
V_{OH} (Min)	Output Voltage (Limits)	V_{DD} − 0.1	V_{DD} − 0.1	V_{DD} − 0.1	V_{DD} − 0.1	V
V_{OL} (Max)		0.1	0.1	0.1	0.1	V
I_{IH}	Input Current	+1.0	+1.0	+1.0	+1.0	μA
I_{IL}		−1.0	−1.0	−1.0	−1.0	μA
I_{OH}	Output Current at V_0 (Limit)	−12@V_{DD}−0.54	−24 @ V_{DD} − 0.8	−24 @ V_{DD} − 0.8	−4.0 @ V_{DD} − 0.8	mA
I_{OL}		12 @ 0.44V	4.0 @ 0.4V	24 @ 0.44V	4.0 @ 0.4V	mA
DCM	DC Noise Margin LOW/HIGH (V_{DD} = 4.5V)	0.7/0.9 (Note 1)	1.25/1.25	0.7/2.4	0.8/1.25	V

Note: All DC parameters are specified over the commercial temperature range.

Note 1: At V_{DD} = 3.0V

Speed/Power Characteristics (All Typical Ratings)

Symbol	Characteristics		LVQ	FACT AC	HCMOS	Units
I_G	Quiescent Supply Current/Gate		0.0005	0.0005	0.0005	mA
P_G	Power/Gate (Quiescent)		0.0015	0.0025	0.0025	mW
t_{Pd}	Propagation Delay ('244 Typ.)		7.0	5.0	14.0	ns
	Speed Power Product		0.01	0.01	0.04	pJ
f_{max}	Clock Frequency D/FF		125	160	50	MHz
t_{PLH}/t_{PHL}	74XX00	Typ	7.0	5.0	8.0	ns
		Max	10.0	8.5	23.0	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX74	Typ	10.5	8.0	12.0	ns
		Max	13.5	10.5	44.0	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX163	Typ	—	5.0	20.0	ns
		Max	—	10.0	52.0	ns

Conditions: (LVQ) V_{DD} = 3.3V ±0.3V, C_L = 50 pF, Over Temperature: −40°C to +85°C.
(HC/FACT) V_{DD} = 5.0V ±10%, C_L = 50 pF, Over Temp, Max values at −40°C to +85°C for HC/FACT.

FIGURE 1.1-7. Logic Family Comparisons

Circuit Characteristics

POWER DISSIPATION

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, 'LVQ will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Total power dissipation of 'LVQ device under AC conditions is a function of three basic sources, quiescent power, internal dynamic power, and output dynamic power dissipation. Firstly, an 'LVQ device will dissipate power in the quiescent or static condition. This can be calculated by using the formula: (Note: In many datasheets I_{DD}, ΔI_{DD}, I_{DDT}, and V_{DD} are referred to as I_{CC}, ΔI_{CC}, I_{CCT}, and V_{CC}, respectively. There are no differences.)

Eq. 1 $PD_Q = I_{DD} \bullet V_{DD}$

PD_Q = Quiescent Power Dissipation
I_{DD} = Quiescent Power Supply Current Drain
V_{DD} = Power Supply Voltage

Secondly, an 'LVQ device will dissipate power dynamically by charging and discharging internal capacitance. This can be calculated by using one of the following two formulas:

Eq. 2

$$PD_{INT} = (C_{PD} \bullet V_S \bullet f) \bullet V_{DD}$$

PD_{INT} = Internal Dynamic Power Dissipation
C_{PD} = Device Power Dissipation Capacitance
V_S = Output Voltage Swing
f = Internal Frequency of Operation
V_{DD} = Power Supply Voltage

C_{PD} values are specified for each 'LVQ device and are measured per JEDEC standards as described later on in the section titled Ratings, Specifications, and Waveforms. On 'LVQ device data sheets, C_{PD} is a typical value and is given either for the package or for the individual stages with the device (see the section titled Ratings, Specifications, and Waveforms). For 'LVQ devices, V_S and V_{DD} are the same value and can be replaced by V_{DD}^2 in the above formula.

Thirdly, an 'LVQ device will dissipate power dynamically by charging and discharging any load capacitance. This can be calculated by using the following formula:

Eq. 3 $PD_{OUT} = (C_L \bullet V_S \bullet f) \bullet V_{DD}$

PD_{OUT} = Output Power Dissipation
C_L = Load Capacitance
V_S = Output Voltage Swing
f = Output Operating Frequency
V_{DD} = Power Supply Voltage

In many cases the output frequency is the same as the internal operation frequency. Also V_S is similar to V_{DD} and can be replaced by V_{DD}^2. In the case of internal and output frequencies being identical Eq. 2 and Eq. 3 may be combined as follows:

Eq. 4 $PD = (C_L + C_{PD}) \bullet V_{DD}^2 \bullet f$

The total 'LVQ device power dissipation is the sum of the quiescent power and all of the dynamic power dissipation. This is best described as:

Eq. 5 $PD_{TOTAL} = PD_Q + PD_{DYNAMIC}$ or
$PD_{TOTAL} = PD_Q + PD_{INT} + PD_{OUT}$

The following is an exercise in calculating total dynamic I_{DD} for the 'LVQ family. The device used as an example is the 'LVQ374. Static I_{DD}, I_{DDT} and C_{PD} numbers can be found in the 'LVQ374 data sheet. I_{DD} numbers used will be worst-case commercial guarantees. Room temperature power will be less. These are approximate worst-case calculations. The results are compared with 'ACQ374.

The following assumptions have been made:

1. I_{DD} will be calculated per input/output (as per JEDEC C_{PD} calculations). The total for the 'LVQ374 will be the calculated $I_{DD} \times 8$.
2. Worst case conditions and JEDEC would require that the data is being toggled at the clock frequency in order to change the outputs at the maximum rate (½ CP).
3. The data and clock input signals are derived from TTL level drivers (0V to 3.0V swing) at 50% duty cycle.
4. The clock frequency is 16 MHz.
5. I_{DD} will be calculated for C_L = 50 pF, 100 pF and 150 pF.
6. V_{DD} = 3V.
7. Total POWER dissipation can be obtained by multiplying total I_{DD} by V_{DD} (3.0V).
8. Quiescent I_{DD} will be neglected in the total I_{DD} calculation because it is 1000 times less than dynamic I_{DD}.
9. There is no DC load on the outputs, i.e. outputs are either unterminated or terminated with series or AC shunt termination.

The I_{DD} calculations are as follows:

I_{DD} Total = Internal Switching I_{DD} + Output Switching (AC load) I_{DD}

Internal I_{DD} = $(V_{SWING}) \times (C_{PD}) \times$ (CP freq)
= $(3.0) \times (40 \times 10^{-12}) \times (16 \times 10^{+6})$
= 1.92 mA per input being toggled by CP

Output I_{DD} = $(V_{SWING} \times (C_L) \times$ (Q freq)

a) C_L = 50 pF
= $(3.0) \times (50 \times 10^{-12}) \times (8 \times 10^{+6})$
= 1.2 mA per output toggled at ½ CP

b) C_L = 100 pF
= $(3.0) \times (100 \times 10^{-12}) \times (8 \times 10^{+6})$
= 2.4 mA per output toggled at ½ CP

c) C_L = 150 pF
= $(3.0) \times (150 \times 10^{-12}) \times (8 \times 10^{+6})$
= 4.8 mA per output toggled at ½ CP

The combination of lower operating voltage and low CMOS power dissipation can be seen more clearly in this example at various capacitive loads.

Adding Internal and Output I_{DD} together and multiplying by 8 I/O per 'LVQ374, the approximate worst-case I_{DD} calculated results are as follows:

Circuit Characteristics (Continued)

Device	C_L	I_{DD} Total
'LVQ374	50 pF	25 mA or 74.9 mW*
'ACQ374	50 pF	42.9 mA or 214.5 mW*
'LVQ374	100 pF	34.6 mA or 103.7 mW*
'ACQ374	100 pF	58.9 mA or 294.5 mW*
'LVQ374	150 pF	53.8 mA or 161.3 mW*
'ACQ374	150 pF	90.9 mA or 454.5 mW*

*Power is obtained by multiplying I_{DD} by V_{DD}; CP = 16 MHz.

SPECIFICATION DERIVATION

At first glance, the specifications for 'LVQ logic might appear to be widely spread, possibly indicating wide design margins are required. However, several effects are reflected in each specification.

Figures 1.1-10a through *1.1-10e* illustrate how the data from the characterization of actual devices is transformed into the specifications that appear on the data sheet. This data is taken from the 'LVQ244.

Figure 1.1-10a shows the data taken (from one part) on a typical, single path, t_{PHL}, over temperature at 3.3V; there is negligible variation in the value of t_{PHL}. The next graph, *Figure 1.1-10b,* depicts data taken on the same device; this set of curves represents the data on all paths. The data on this plot indicates only a small variation for t_{PHL}.

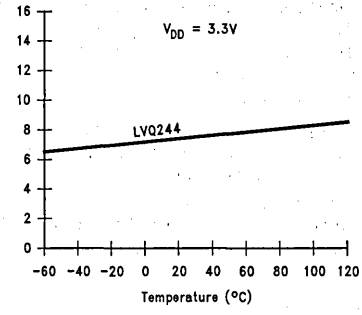
The graphs in *Figures 1.1-10a–b* include data at 3.3V; *Figure 1.1-10c* shows the variation of delay times over the standard 3.3V ±0.3V voltage range. Note there is only a ±6% variation in delay time due to voltage effects.

Now refer to *Figure 1.1-10d* which illustrates the process effects on delay time. This graph indicates that the process effects contribute to the spread in specifications more than any other factor in that the effects of the theoretical process spread can increase or decrease specification times by 30%. Because this 30% spread represents considerably more than ±3 standard deviations, this guarantees an increase in the manufacturability and the quality level of 'LVQ product. To further ensure parts within specification will pass on testers at the limits of calibration, tester guardbands are incorporated.

With voltage and process effects added *(Figure 1.1-10e),* the full range of the specification can be seen. For reference, the data sheet values are shown on the graph.

This linear behavior with temperature and voltage is typical of CMOS. Although the graphs are drawn for a specific device, other part types have very similar graphical representations. Therefore, for performance-critical applications, where not all variables need to be taken into account at once, the user can narrow the specifications. For example, all parts in a critically timed subcircuit are together on a board, so it may be assumed the devices are at the same supply and temperature.

The same reasoning can be applied to setup and hold times. Consider the 'LVQ74. The setup time is 4.0 ns while the hold time is 0.5 ns. Theoretically, if these numbers were violated, the device would malfunction; however, in actuality, the device probably will not malfunction. Looking at the typical setup and hold times gives a better understanding of the device operation.



TL/F/10976–7

FIGURE 1.1-10a. t_{PHL} Single Path

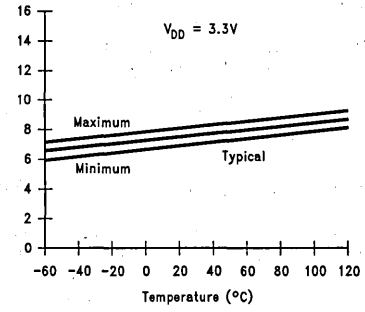


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FIGURE 1.1-10b. t_{PHL}, 'LVQ244, All Paths

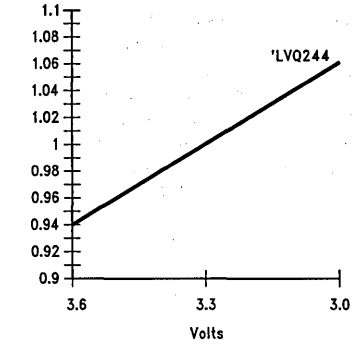

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FIGURE 1.1-10c. Voltage Effects on Delay Times

Circuit Characteristics (Continued)

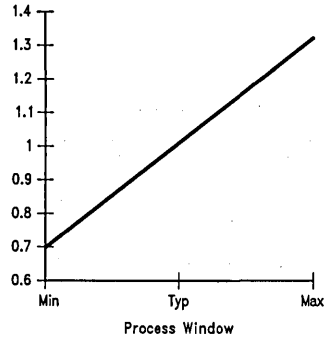

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FIGURE 1.1-10d. LVQ Process Effects on Delay Times

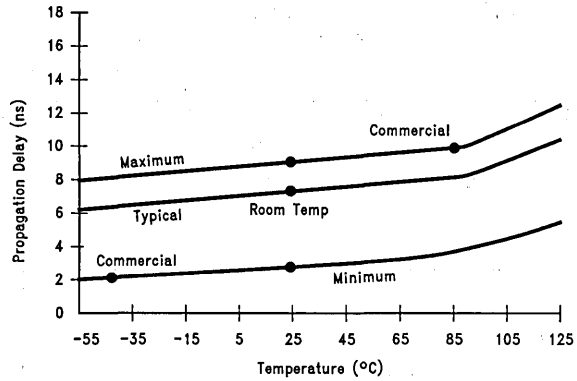

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FIGURE 1.1-10e. t_{PHL}, 'LVQ244, with Voltage and Process Variation

At 25°C and 3.3V, the setup time is 1.5 ns while the hold time is −2.0 ns. They are virtually the same; a positive setup time means the control signal to be valid before the clock edge, a positive hold time indicates the control signal will be held valid after the clock edge for the specified time, and a negative hold time means the control signal can transition before the clock edge. 'LVQ devices were designed to be as immune to metastability as possible. This is reflected in the typical specifications. The true "critical" time where the input is actually sampled is extremely short: less than 50 ps.

By applying the same reasoning as we did to the propagation delays to the setup and hold times, it becomes obvious that the spread from setup to hold time (3.5 ns worst-case) really covers devices across the entire process/temperature/voltage spread. The real difference between the setup and hold times for any single device, at a specified temperature and voltage, is negligible.

CAPACITIVE LOADING EFFECTS

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of 'LVQ devices. Minimum delay numbers may be determined from the table below. Propagation delay are measured to the 50% point of the output waveform.

Parameter		Voltage (V)			Units
		3.0	4.5	5.5	
t_{PLH}	'LVQ Gates	31	22	19	ps/pF
	'LVQ Octals	34	19	19	
t_{PHL}	'LVQ Gates	18	13	13	ps/pF
	'LVQ Octals	32	22	20	

T_A = 25°C

Figures 1.1-11 and *1.1-12* describe propagation delays on 'LVQ devices as affected by variations in power supply voltage (V_{DD}) and lumped load capacitance (C_L). *Figures 1.1-13* and *1.1-14* show the effects of lumped load capacitance on rise and fall times for 'LVQ devices.

Circuit Characteristics (Continued)

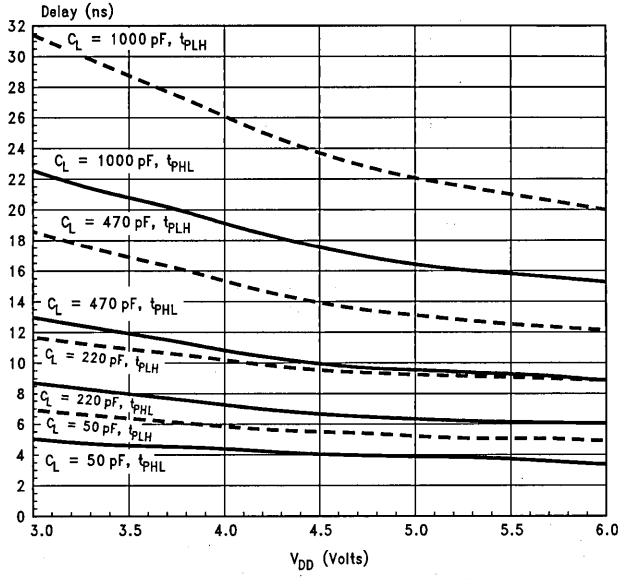

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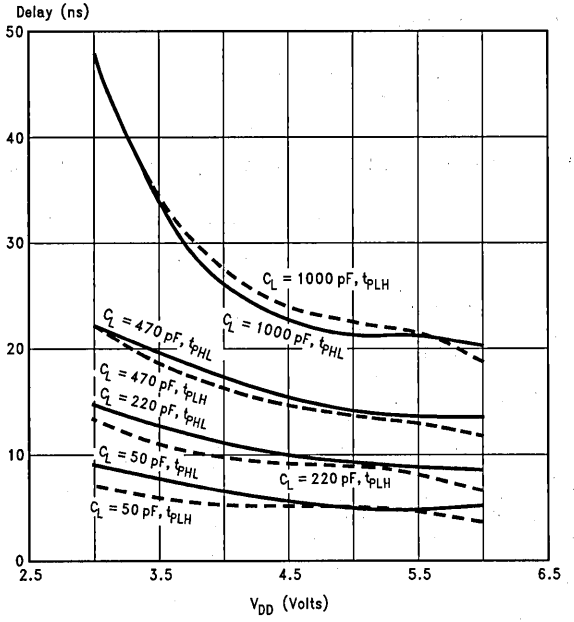
FIGURE 1.1-11. Propagation Delay vs V_{DD} ('LVQ Gates)



TL/F/10976–13

FIGURE 1.1-12. Propagation Delay vs V_{DD} ('LVQ Octal)

Circuit Characteristics (Continued)

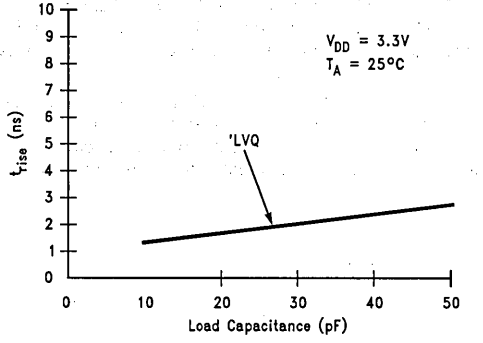


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FIGURE 1.1-13. t_{rise} (V_{IL} − V_{IH}) vs Capacitance

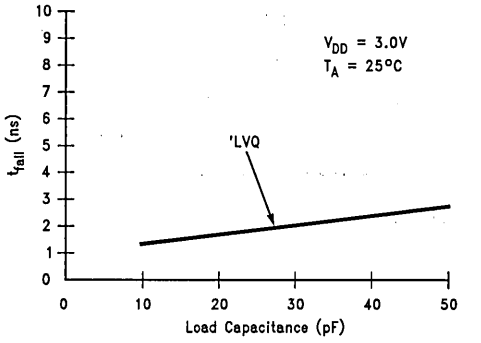

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FIGURE 1.1-14. t_{fall} (V_{IH} − V_{IH}) vs Capacitance

LATCH-UP

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. 'LVQ logic is guaranteed not to latch-up with dynamic currents of 100 mA (300 mA for Octals) forced into or out of the inputs or the outputs under worst case conditions (T_A = 125°C and V_{DD} = 3.6 V_{DC}). At room temperature the parts can typically withstand dynamic currents of close to 1A. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

Devices are designed to reduce the possibility of latch-up occurring; National Semiconductor accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY

'LVQ circuits show excellent resistance to ESD-type damage. These logic devices are classified as category "B" of MIL-STD-883C, test method 3015, and withstand in excess of 4000V typically. 'LVQ logic is guaranteed to have 2000V ESD immunity on all inputs and outputs. 'LVQ parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 1.1-16 shows the ESD test circuit used in the sensitivity analysis for this specification. *Figure 1.1-17* is the pulse waveform required to perform the sensitivity test.

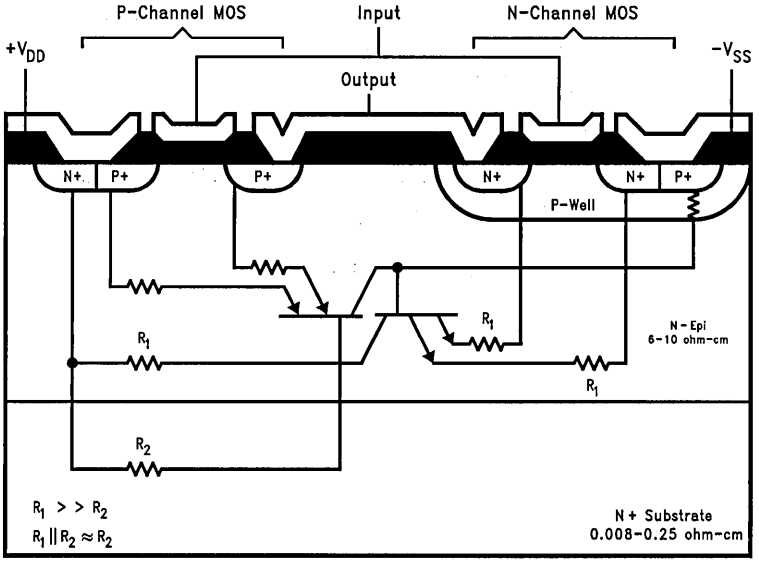

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FIGURE 1.1-15. CMOS EPI Process Cross Section with Latch-up Circuit Model

Circuit Characteristics (Continued)

The test procedure is as follows; five pulses, each of at least 2000V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883C, TM-3015. Devices that result in ESD immunity in the 2000V–3999V range are listed as ESD Class 2. Devices that result in ESD immunity in the 4000+V range are listed as ESD Class 3.

For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.

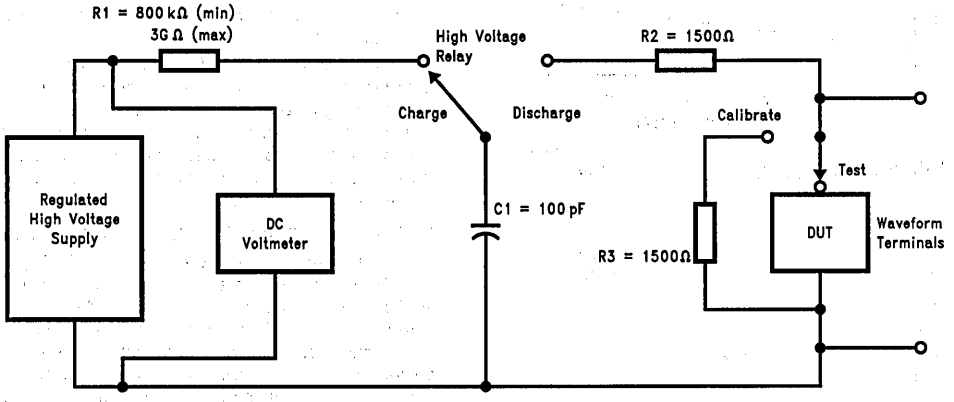

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FIGURE 1.1-16. ESD Test Circuit

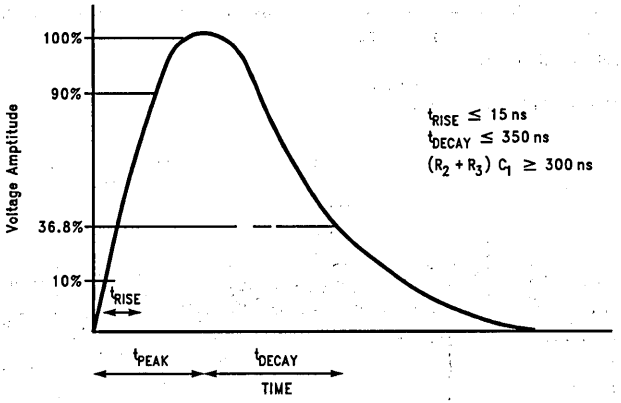

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FIGURE 1.1-17. ESD Pulse Waveform

Circuit Characteristics (Continued)

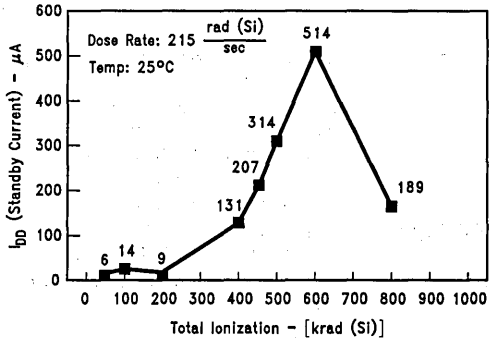
RADIATION TOLERANCE

Information on radiation tolerance is included in this databook but does not imply testing has been performed on 'LVQ devices. Semiconductors subjected to radiation environments undergo degradation in operating life as their exposure to radiation increases. As technology advances, so does the demand for radiation-tolerant devices. National met this challenge by developing the FACT family into a comprehensive radiation tolerant product for present and future rad-hard needs. Such applications include:

- Space (Commercial and Military)
- — Satellites
- — Space Stations
- Airborne and Military (Tactical Arena)
- — Fighters/Bombers
- — Missile Systems
- — Ground Based Systems
- — Navigation & Communications
- Commercial
- — Power Stations
- — Medical
- — Food and Bacterial Control

Radiation tolerant semiconductors increase the useful life of the product in which they are incorporated. Additionally, radiation tolerant devices reduce shielding requirements and improve stabilization of parametric performance, resulting in cost reductions for shielding and weight, reduce power consumption and size.

SUMMARY OF TESTING



TL/F/10976–19

FIGURE 1.1-18. Total Dose Response (54AC245)

Total dose irradiation is presently performed "in-house" using a AECL Gamma Cell 220, Cobalt-60, source (National Bureau of Standards certified). Step-stress radiation testing is performed on each part-type per MIL STD 883 Method 1019.3. After each total dose level, a complete parametric test (DC and AC) is done and the parametric values evaluated.

FACT IS RADIATION TOLERANT

FACT logic employs the use of thin gate oxides, oxidation cycles, and annealing steps that enhance the tolerance of the standard FACT product line.

FACT's epitaxial layer and low-resistivity substrate provide inherent latch-up immunity under dose rate and single event phenomenon (SEP) conditions.

Figure 1.1-18 shows a FACT 'AC245 I_{DD} supply current versus total dose radiation. With the exception of I_{DD} and I_{OZ}, all FACT devices tested to date suffer no parametric degradation or functional failures up to several hundred krads. Due to circuit and layout differences, each function has a unique response to radiation. Relaxed limits for I_{DD} and I_{OZ} are per the applicable /750XX slash sheet, standard military drawing (SMD), or datasheet.

DOSE RATE TEST RESULTS

Analysis of the FACT 54AC299 8-Bit Universal Shift Register upset test data indicates that minimum upset threshold levels occurred under the worst-case conditions of a wide pulse (1 μs), lowest V_{DD} voltage (4.0V DC), and the DUT in the dynamic operating mode.

Measured minimum upset levels were 1.90 to 2.22 $\times$ 10^9 rad(Si)/sec. Narrow pulse (50 ns) data demonstrated radiation upset levels from 4.40 to 5.66 $\times$ 10^9 rad(Si)/sec under dynamic operation.

Upon completion of radiation upset testing, latchup and survivability tests were performed at +25°C, +80°C, +100°C, and +116°C for V_{DD} = 4.5V DC, 5.0V DC, and 5.5V DC. Test results indicated no latchup occurred for either narrow pulse (50 ns) or wide pulse (1 ms) radiation. The radiation test level for narrow pulse was 10^{10} rad(Si)/sec at +25°C. Due to the heating of the circuit, the highest radiation level was limited at +116°C to 7.5 $\times$ 10^9 rad(Si)/sec.

After completion of latchup and survivability tests, verification of latchup windows was performed. Test results indicate no existence of latchup windows under worst case conditions for narrow and wide pulse radiation.

LOW VOLTAGE LOGIC

Employing a low voltage power system not only reduces the magnitude of the radiation-induced leakage current, but also minimizes the threshold voltage shifts and the total dose enhancement of the "hot electron" effect. Dose rate and SEP (Single Event Phenomena) latchup performance is also improved.

Care must be used when using a low-voltage power system in a radiation environment. While improvements are observed as previously mentioned, there are trade-offs to be considered, particularly concerning non-radiation performance. However, one issue of concern in the radiation environment is radiation-induced upset due to dose rate or SEP. As supply voltages are reduced, this function becomes more easily upsettable.

When there is full understanding of the total radiation environment as well as each system's particular design, low-voltage supply is a viable choice.

National Semiconductor

Ratings, Specifications, and Waveforms

Specifying LVQ Devices

Traditionally, when a semiconductor manufacturer completed a new device for introduction, specifications were based on the characterization of just a few parts. While these specifications were appealing to the designer, they were often too tight and, over time, the IC manufacturers had difficulty producing devices to the original specs. This forced the manufacturer to relax circuit specifications to reflect the actual performance of the device.

As a result, designers were required to review system designs to ensure the system would remain reliable with the new specifications. National Semiconductor realized and understood the problems associated with characterizing devices too aggressively.

To provide more realistic and manufacturable specs, National Semiconductor devised a systematic and thorough process to generate specifications. Devices are selected from multiple wafer lots to ensure process variations are taken into account. In addition, the process parameters are measured and compared to the known process limits. With more than five years of experience manufacturing LVQ logic, National Semiconductor can accurately predict how these wafer lots compare with the best and worse case lots that can possibly be expected.

This method of characterizing parts more accurately represents the product across time, voltage, temperature and process rather than portraying the fastest possible device.

These specification guidelines allow designers to design systems more efficiently since the devices used will behave as documented. Unspecified guardbands no longer need to be added by the designer to ensure system reliability.

Power Dissipation—Test Philosophy

In an effort to reduce confusion about measuring power dissipation capacitance, C_{PD}, a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison.

The following is a list of different types of logic functions, along with the input setup conditions under which the C_{PD} was measured for each type of device. By understanding how the device was exercised during C_{PD} measurements, the designer can understand whether the C_{PD} specified for that particular device reflects the total power dissipation capacitance for either the entire device or for just a certain stage of that device. For example, from the following list, it is apparent that the C_{PD} value specified for a counter reflects the internal capacitance for the entire device, since the entire device is being exercised during measurement. On the other hand, the C_{PD} value specified for an octal line driver reflects the internal capacitance for only one of eight stages, since only one input was being switched during test. Therefore the octal's overall power dissipation should be calculated for each of the eight stages, individually.

During the C_{PD} measurements, each output that is being switched should be loaded with the standard 50 pF and 500Ω load. All device measurements are made with V_{DD} = 3.3V at 25°C, with TRI-STATE® outputs enabled.

Gates/Buffers/ Line Drivers:	Switch one input. Bias the remaining inputs such that one output switches.
Latches:	Switch the Enable and D inputs such that the latch toggles.
Flip-Flops:	Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-flop.
Decoders:	Switch one address pin which changes two outputs.
Multiplexers:	Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.
Counters:	Switch the clock pin with other inputs biased such that the device counts.
Shift Registers:	Switch the clock pin with other inputs biased such that the device shifts.
Transceivers:	Switch one data input. For bidirectional devices enable only one direction.
Parity Generator:	Switch one input.
Priority Encoders:	Switch the lowest priority input.

AC Loading and Waveforms

LOADING CIRCUIT

Figure 1.2-1 shows the AC loading circuit used in characterizing and specifying propagation delays of all LVQ devices unless otherwise specified in the data sheet of a specific device.

AC Loading and Waveforms (Continued)

The use of this load, which is equivalent to the FAST® (Fairchild Advanced Schottky TTL) test jig, differs somewhat from previous (HCMOS) practice. This provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance, allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the inloading to be expected in average applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the LVQ product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

The 500Ω resistor to ground can be a high frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high impedance probe. Alternately, the 500Ω resistor to ground can simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See *Figure 1.2-1*.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Shown in *Figure 1.2-1* is a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500Ω resistors and the 2 × V_{DD} supply voltage establish a quiescent HIGH level.

Test Conditions

Figure 1.2-2 describes the input signal voltage levels to be used when testing LVQ circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0V to V_{DD}. The DC parameters are normally tested with V_{IN} at guaranteed input levels, that is V_{IH} to V_{IL} (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 3.3V then dropping to a level corresponding to V_{IH} characteristics, and then raising again to the 3.3V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0V to V_{IL}, then returning to 0V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the LVQ device.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output wave-

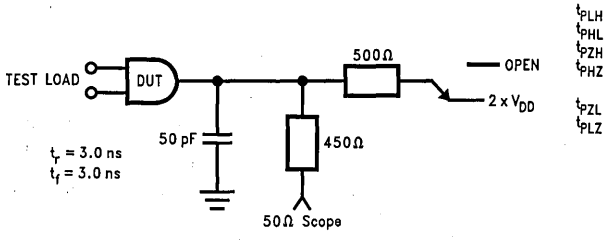


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FIGURE 1.2-1. AC Loading Circuit for LVQ

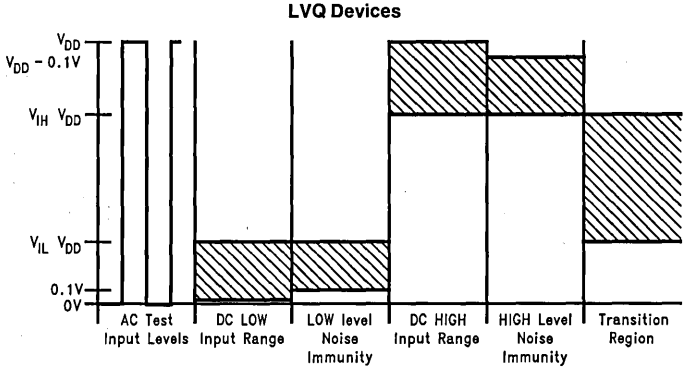

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FIGURE 1.2-2. Test Input Signal Levels

Test Conditions (Continued)

form transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{DD} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

Rise and Fall Times

Input signals should have rise and fall times of 3.0 ns and signal swing of 0V to V_{DD} for 'LVQ devices. Rise and fall times less than or equal to 1 ns should be used for testing f_{max} or pulse widths.

CMOS devices, including 4000 Series CMOS, HC, HCT, FACT™ and LVQ families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, LVQ devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a HIGH level to a LOW level, or from a LOW level to a HIGH level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2–3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the V_{DD} or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world because of this induced voltage.

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it recrosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have V_{DD} and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With LVQ logic having gains as high as 100, it merely takes a 30 mV change in the input to generate a full 3V swing on the output.

Propagation Delays, f_{max}, Set and Hold Times

A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc. See *Figures 1.2-3* and *1.2-4*.

Enable and Disable Times

Figures 1.2-5 and *1.2-6* show that the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from V_{OL} or V_{OH}, respectively. This change enhances the repeatability of measurements, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 0.3V of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 0.3V is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable times and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled. Note that the measurement points have been changed from the previous 10% and 90% points. This better reflects actual test points and does not change specification limits.

Waveforms

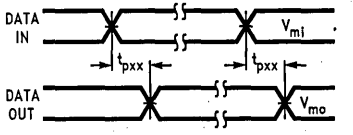

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FIGURE 1.2-3. Waveform for Inverting and Non-Inverting Functions for LVQ

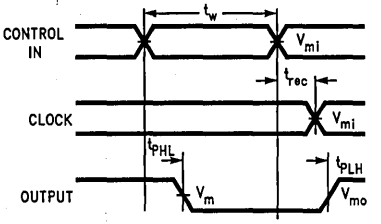

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FIGURE 1.2-4. Propagation Delay, Pulse Width and t_{rec} Waveforms for LVQ

Waveforms (Continued)

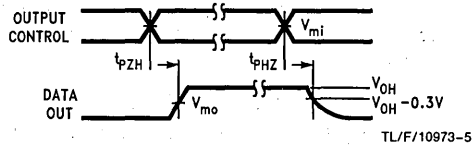

FIGURE 1.2-5. TRI-STATE Output High Enable and Disable Times for LVQ

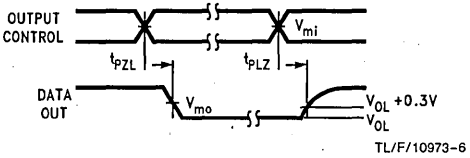

FIGURE 1.2-6. TRI-STATE Output Low Enable and Disable Times for LVQ

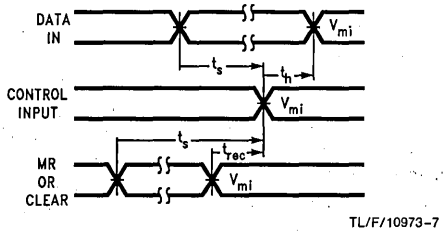

FIGURE 1.2-7. Setup Time, Hold Time and Recovery Time for LVQ

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to LVQ devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, which are near the device, are conductive and connected to ground.

LVQ Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of LVQ.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture or Equivalent
Tektronics Model 7854 Oscilloscope or Equivalent

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{DD} to 3.3V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3.3V HIGH for LVQ devices. Verify levels with a digital volt meter.

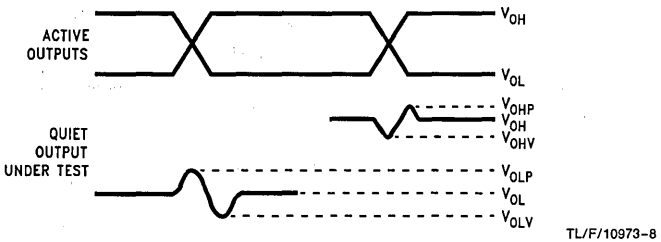

FIGURE 1.2-8. Quiet Output Noise Voltage Waveforms

Note A. V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B. Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

LVQ Noise Characteristics (Continued)

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output LOW during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output HIGH during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

Skew Definitions and Examples

Minimizing output skew is a key design criteria in today's high-speed clocking schemes, and National has incorporated skew specifications into the 'LVQ family of devices.

This section provides general definitions and examples of skew. Common Edge Skew is guaranteed for 'LVQ devices; however other forms of skew are also defined in this section.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s). See *Figure 1.2-10.*

Example:

If signal appears at out #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device, duty cycle and device-to-device delay differences.

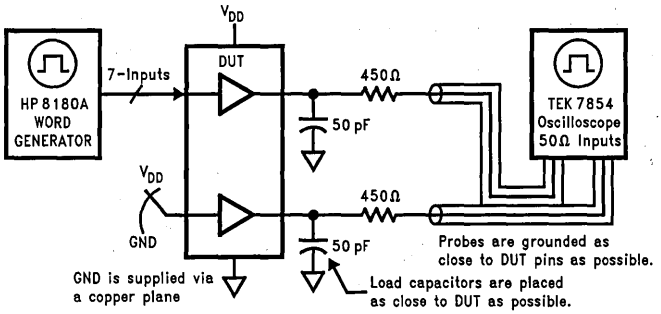

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FIGURE 1.2-9. Simultaneous Switching Test Circuit

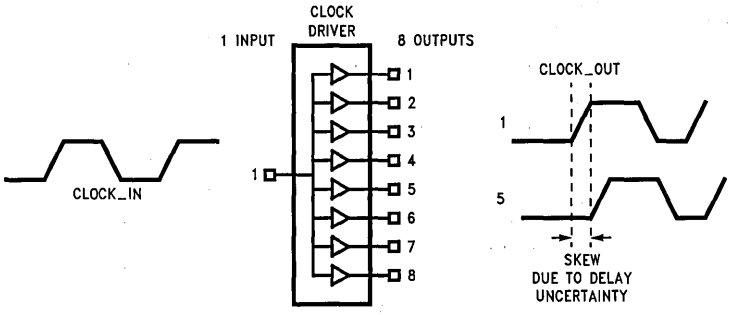

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FIGURE 1.2-10. Clock Output Skew

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

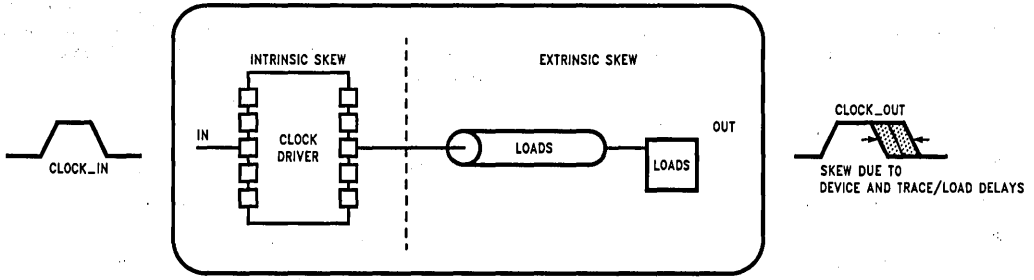

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FIGURE 1.2-11. Sources of Clock Skew

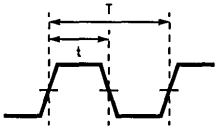
Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles
Total system skew budget = 10% of clock cycle = 2 ns* → 2 ns
If extrinsic skew = 1 ns → − 1 ns
Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design *Rule of thumb.*

CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is *High* or *Low* in a given clock cycle.



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Duty Cycle = t/T * 100%

FIGURE 1.2-12. Duty Cycle Calculation

Clock Signal

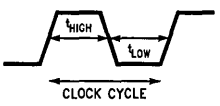

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FIGURE 1.2-13. Clock Cycle

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.

Clock + Skew

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FIGURE 1.2-14. Clock Skew

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE I

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle		
50 MHz	0 ns	10 ns	10 ns	50/50%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%		
50 MHz	1 ns	11 ns	9 ns	55/45%		
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

$t_{OSHL} = |t_{PHL_{MAX}} - t_{PHL_{MIN}}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLH_{MAX}} - t_{PLH_{MIN}}|$

Propagation delays are measured across the outputs of any given device.

Example

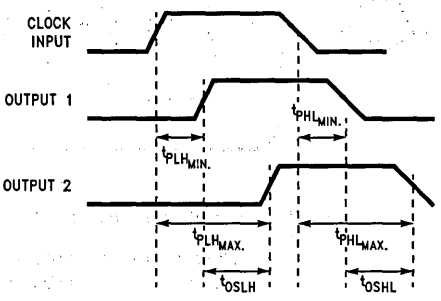

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FIGURE 1.2-15. t_{OSLH}, t_{OSHL}

Definition of Parameters (Continued)

t_{PS} (Pin Skew or Transition Skew)

t_{PS}, describes opposite edge skews, i.e., the difference between the delay of the low-to-high transition and the high-to-low transition on the same pin. This parameter is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. Ideally this number needs to be 0 ns. Effectively, 0 ns means that there is no degradation of the input signal's Duty Cycle.

Many of today's microprocessors require a minimum of a 45:55 percent Duty Cycle. System clock designers typically achieve this in one of two ways. The first method is with an expensive crystal oscillator which meets the 45:55 percent Duty Cycle requirement. An alternative approach is to use a less expensive crystal oscillator and implement a divide by two function. Some microprocessors have addressed this by internally performing the divide by two.

Since Duty Cycle is defined as a percentage, the room for error becomes tighter as the system clock frequency increases. For example in a 25 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 4 ns (t_{PLH} of 18 ns and t_{PLH} of 22 ns) and still meet the Duty Cycle requirement. However for a 50 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 2 ns (t_{PLH} of 9 ns and t_{PHL} of 11 ns) and still meet the Duty Cycle requirement. This analysis assumes a perfect 50:50 percent Duty Cycle input signal.

Definition

t_{PS} (Pin Skew or Transition Skew):

$t_{PS} = |t_{PHL} - t_{PLH}|$

Both high-to-low and low-to-high propagation delays are measured at each output pin across the given device.

Example

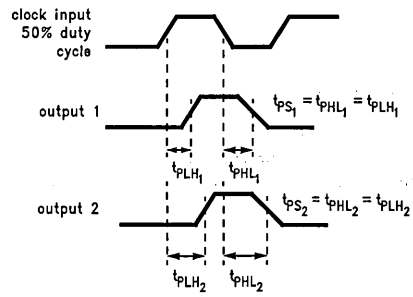

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FIGURE 1.2-16. t_{PS}

Example: A 33 MHz, 50/50% duty cycle input signal would be degraded by 2.6% due to a t_{PS} = 0.8 ns. (See Table and Illustration below.)

Note: Output symmetry degradation also depends on input duty cycle.

TABLE II. Duty Cycle Degradation of 33 MHz

f (MHz)	Input			Device	Output			% Δ DC Input to Output
	DC Input	t_{IN} (ns)	T_{IN} (ns)	t_{PS} (ns)	t_{OUT} (ns)	T_{OUT} (ns)	DC Output	
33	**50%/50%**	15.15/15.15	30.3	**0.8**	14.35/15.95	30.3	47.4%/52.6%	**2.6%**
	45%/55%	13.6/16.6	30.3	**1.5**	12.1/18.1	30.3	39.9%/60.1%	**5.1%**

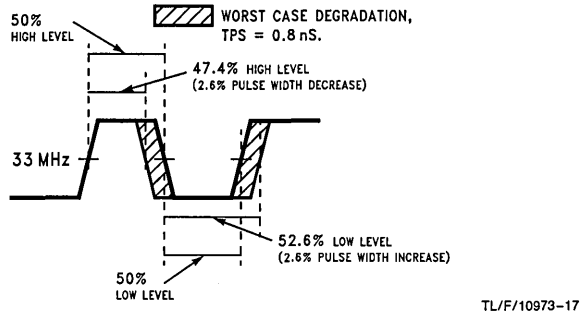

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FIGURE 1.2-17. Pulse Width Degradation

Definition of Parameters (Continued)

t_{OST} (Opposite Edge Skew)

t_{OST} defines the difference between the fastest and the slowest of both transitions within a given chip. Given a specific system with two components, one being positive-edge triggered and one being negative-edge triggered, t_{OST} helps to calculate the required delay elements if synchronization of the positive- and negative-clock edges is required.

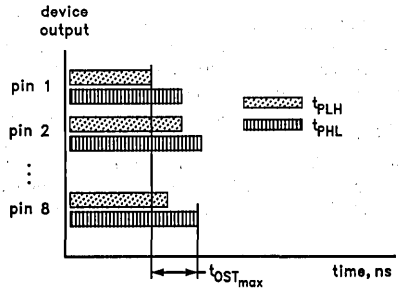

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FIGURE 1.2-18. t_{OST}

Definition

t_{OST} (Opposite Edge Skew):

$$t_{OST} = |t_{P\varphi m} - t_{P\varphi n}|$$

where φ is any edge transition (high-to-low or low-to-high) measured between any two outputs (m or n) within any given device.

Example

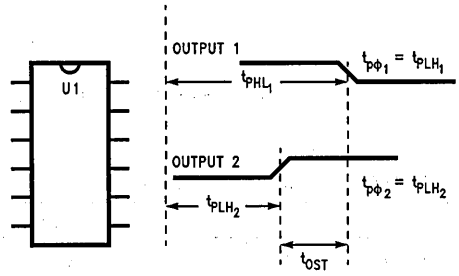

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FIGURE 1.2-19. t_{OST}

Definition of Parameters (Continued)

t_{PV} (Part Variation Skew)

t_{PV} illustrates the distribution of propagation delays between the outputs of any two devices.

Part-to-part skew, t_{PV}, becomes a critical parameter as the driving scheme becomes more complicated. This usually applies to higher-end systems which go from single clock drivers to distributed clock trees to increase fanout (shown below). In a distributed clock tree, part-to-part skew between U2 and U3 must be minimized to optimize system clock frequency. In the case of the clock tree, the total skew becomes a function of $t_{OSLH/HL}$ of U1 plus t_{PV} of U2 and U3.

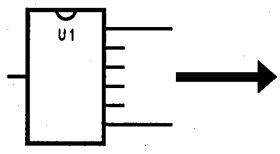

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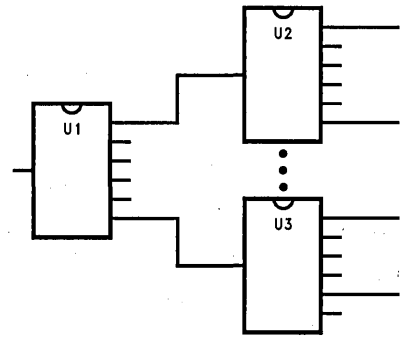
FIGURE 1.2-20. Clock Distribution

Case 1: Single Clock Driver

Total Skew = Pin-to-Pin Skew U1
= t_{OSLH} or t_{OSHL} of U1



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Case 2: Distributed Clock Tree

Total Skew (U2, U3) = Pin-to-Pin Skew (U1) + Part-to-Part Skew (U2, U3)

Definition

t_{PV} (Part Variation Skew):

$t_{PV} = |t_{P\varphi u,v} - t_{P\varphi x,y}|$

where φ is any edge transition (high-to-low or low-to-high) measured from the outputs of any two devices.

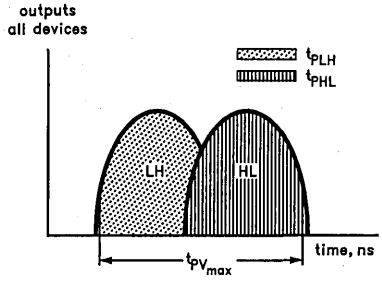

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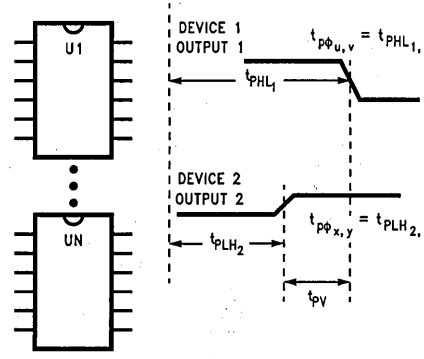
FIGURE 1.2-21. t_{PV}

Example



TL/F/10973–23

FIGURE 1.2-22. t_{PV}

National Semiconductor

Design Considerations

Today's portable and battery-operated system designer is faced with the problem of keeping ahead when addressing system performance, long battery life and reliability. National Semiconductor's advanced CMOS helps designers achieve these goals. Low Voltage CMOS Logic, LVQ, like FACT™ (Fairchild Advanced CMOS Technology) logic, was designed to alleviate many of the drawbacks that are common to present technology logic circuits. LVQ logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a 75Ω transmission line drive capability. Performance features such as advanced Schottky speeds at CMOS power levels, excellent noise suppression, ESD protection, and latch-up immunity are characteristics that designers of state-of-the-art systems require.

To fully utilize the advantages provided by LVQ, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of LVQ. There are six items of interest which need to be evaluated when implementing LVQ devices in new designs:

- Interfacing—Interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving
- Power Supplies and Decoupling—Maximize ground and V_{DD} traces to keep V_{DD}/ground impedance as low as possible; full ground/V_{DD} planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.
- Noise effects—As edge rates increase, the probability of crosstalk and ground bounce problems increases. The noise immunity and high threshold levels improve LVQ's resistance to system-generated problems.
- Board Layout—Prudent board layout will ensure that most noise effects are minimized.
- Electromagnetic Interference

Interfacing Dual Voltage Systems

In order to reliably interface one integrated circuit to another, recommended input and output specifications for voltage and current must be satisfied. Output specifications of the driving IC must meet the input requirements (V_{IL} and V_{IH}) of the receiver IC in order to justify the circuit design. This "noise margin" protects the design against malfunction during system and environmentally generated noise.

For better than two decades, almost all digital signal processing has been designed around a 5V standard power supply. During this period of time countless IC vendors have introduced new product families with higher drive, faster speeds, and lower power. As a result several Input/Output standards exist in the 5V world and interfacing between them can get confusing. Because of the inherent restrictions, pure-TTL technologies cannot operate with a 3.3V power supply. Therefore, the core technology for all 3V ICs will be MOS. In a straight 3V MOS system, all connections can be done directly, both on the outputs and on the inputs.

However, it will be quite some time before ALL components in a portable/desktop PC can operate at 3.3V. This is especially true for peripheral devices such as displays, printers, and faxes. Therefore, at some point in the system, 3V ICs must interface with 5V ICs. If mishandled, this interface will waste power and reduce the reliability of the products at the interface. On the following pages, solutions to possible dual voltage interfaces are outlined.

INTERFACING 5.0V TTL OR "REDUCED SWING" CMOS TO 3.3V LVQ

Bipolar TTL ICs or the newly introduced "reduced swing" (NMOS pull-up) CMOS ICs are the easiest of the 5V technologies to interface with because of their 3V output signal. 3V ICs such as LVQ have input specifications similar to the 5V TTL or TTL-compatible CMOS ICs. In this case, interfacing at this point may be direct. To safeguard this configuration against voltage and temperature fluctuations the designer should regulate BOTH the 3.3V and 5V power supplies together. Another option is to purposely run the 5V power supply on the low side to decrease the 5V-to-3V V_{OH}-to-V_{CC} delta. This optimum configuration reduces any DC power loss from termination at the interface to zero.

However, if the same system is allowed to operate with power supply tolerances that could vary ±10% independently (example: 5.0V +10% and 3.3V −10%), then the input specifications for LVQ products would be violated. In order to remain within the absolute maximum specifications for LVQ products, the V_{OH} of the TTL I/O must be held to within 0.5V of the LVQ V_{CC}. The best way to reduce V_{OH} while retaining signal fidelity and specified propagation delays is to add a parallel resistor termination (to GND) to every signal line at the dual voltage interface.

Interfacing Dual Voltage Systems (Continued)

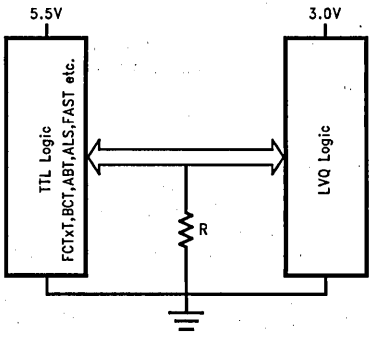


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FIGURE 1.3-1a. Dual Voltage with Parallel Resistor Termination

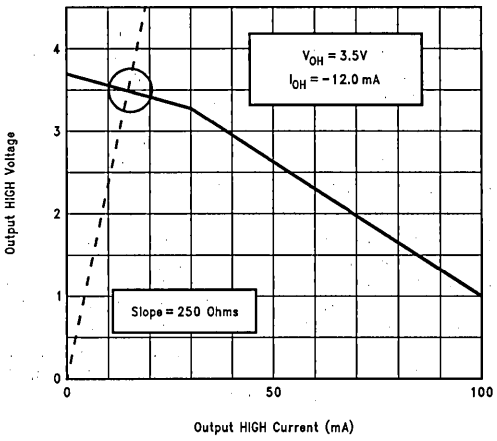

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FIGURE 1.3-1b. 74F244 Output Drive

The "R" value in *Figure 1.3-1a* and *1.3-1b* is derived using manufacturer supplied I_{OH}/V_{OH} curves in conjunction with the formula: R = 3.5V/I_{OH} @ V_{OH} = 3.5V). In this example, the Bipolar I_{OH}/V_{OH} curve is from the FAST Applications Handbook. Although only the 74F244 case is shown, the method also applies to a "reduced swing" CMOS, BICMOS, and other Bipolar devices.

INTERFACING 5.0V CMOS TO 3.3V LVQ

To provide an interface solution between 5V CMOS and LVQ, National Semiconductor has introduced a unidirectional buffer translator product 74LVX244 especially designed to couple 5.0V designs with new 3.3V LVQ designs. These devices, operating with a supply voltage of 3.3V, are designed to interface with CMOS outputs operating from a 5.0V supply.

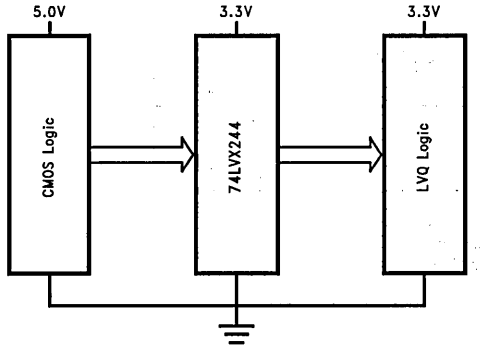

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FIGURE 1.3-2. Dual Voltage with LVQ Translator

When ordinary LVQ inputs are driven beyond V_{CC}, large currents will flow into the silicon substrate raising the internal V_{CC} of the LVQ product to 4.0V or above. Therefore, it is generally not recommended to interface CMOS at 5.0V to non-translator LVQ device at 3.3V. However, such a configuration may become unavoidable in some mixed/dual voltage designs. In order to reduce the V_{OH} level of a CMOS device, a voltage divider must be set up on the output to provide the correct V_{OH} level to the LVQ device. One possible configuration is shown in the *Figure 1.3-3*.

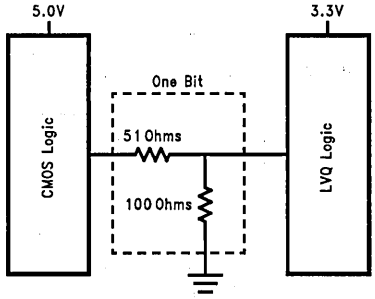

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FIGURE 1.3-3. Dual Voltage with Resistor Divider Network

Although DC power is consumed by the voltage divider, using higher values of resistance for the voltage divider will create an additional propagation delay across the interface. This is due to the RC time constant setup by LVQ device inputs and the Thevenin equivalent resistance of the voltage divider. The resistance values shown exhibit a good compromise between DC power loss and signal fidelity.

INTERFACING 3.3V LVQ TO 5.0V INPUTS

Interfacing a 3V LVQ IC's output to a 5V TTL-compatible CMOS input can be done directly. LVQ 3V output specifications and 5V TTL-compatible CMOS specifications are compatible. Interfacing a 3V LVQ output to a 5V CMOS (V_{IH} = 3.15V @ V_{CC} = 5.0V) input should NEVER be done, be-

Interfacing Dual Voltage Systems

(Continued)

cause the 5V CMOS part will require a low impedance pull up to V_{CC} to satisfy its input requirements. Whenever a LVQ output is pulled up beyond its V_{CC}, an intrinsic diode in the output structure will begin to forward bias causing excessive currents to flow from the interface through the LVQ output and into the 3.3V power supply. This could raise the output level of the 3.3V supply to a level exceeding the maximum rated voltages for some low voltage devices.

Many types of 5V Bipolar inputs can present a similar problem at the dual voltage interface. It is common for a Bipolar device to have 10 kΩ–20 kΩ internal pull-up resistors on every input pin connected directly to the 5V V_{CC} plane. In this case, external pull-down resistors are recommended to create a voltage divider network that would set the logic HIGH voltage to a safe level for the LVQ output as described earlier. *Figure 1.3-4* illustrates such an interface. This type of pull-down is also ideal for any bus with Bipolar or "Reduced Swing" I/O that can be TRI-STATED with high-impedance driver outputs. In the past, busses of this type were pulled up to V_{CC} with 4 kΩ resistors. The same results, pulling the bus away from threshold sensitive areas, are achieved with the pull-down resistor recommended. The value of this resistor is chosen based on the desired voltage divider network.

In summary, to make interfacing easier, reduce the amount of interfacing needed by minimizing the amount of 5V circuitry. Concentrate the 5V circuitry into one area of the system and minimize the number of signals needed to interface with 3V ICs. Wherever possible utilize a direct interface to minimize power consumption and maximize board integration, if necessary use the 74LVX244 translator. For the remaining interface signals, select an external interface solution that best reduces the risk of violating the LVQ absolute maximum voltages while maintaining the best possible noise margins and lowest power dissipation. The table below summarizes all of the interface options that a systems designer may be confronted with in a mixed/dual voltage system design.

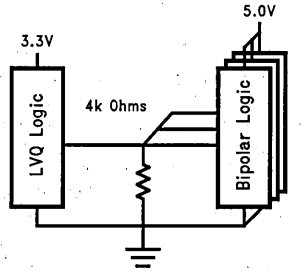

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FIGURE 1.3-4. Dual Voltage System Bus

Driver	Receiver	Direct Interface
LVQ Logic	Bioplar Input BiCMOS Input	OKAY* *See Text on 3.3V LVQ to 5V Bipolar
LVQ Logic	TTL-Compatible CMOS Input	Use ACT or ACTQ
LVQ Logic	CMOS Input	Unacceptible
Bipolar Output BiCMOS Output Reduced Swing CMOS Output	LVQ Logic	OKAY* * See Text on 5V TTL to 3.3V LVQ
CMOS Output	LVQ Logic	Use 74LVX244

Note: In the table above it can be assumed that LVQ is always at a V_{CC} of 3.3V. The outputs driving LVQ and the inputs being driven by LVQ are operating with a V_{CC} of 5.0V.

Line Driving and Termination

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become more significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

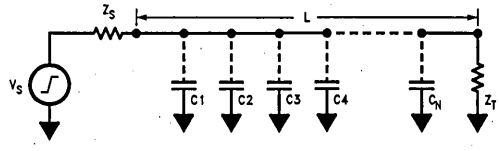
Of the many properties of transmission lines, two are of major interest to the system designer: Z'_o, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z'_o and t_{pde} can be calculated with:

$$Z'_o = \frac{Z_o}{\sqrt{1 + C_D/C_L}}$$

$$t_{pde} = t_{pd}\sqrt{1 + C_D/C_L}$$

where C_L = intrinsic line capacitance and C_D = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.



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Length of Transmission Line = L

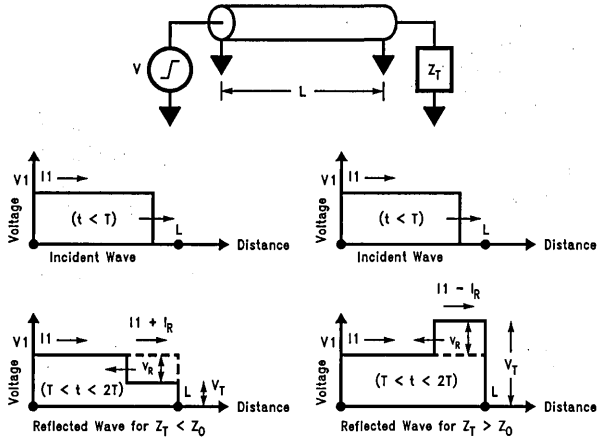
Distributed Load Capacitance per Unit Length = $C_D = \sum_{n=1}^{N} C_L/L$

Characteristic Impedance of a Transmission Line Altered by Distributed Loading

$$= Z'_O = \sqrt{\frac{L_O}{C_O + C_D}} = \frac{Z_O}{\sqrt{1 + \frac{C_D}{C_O}}}$$

Effective Reflection Coefficient at Termination = $\rho = \frac{Z_T - Z'_O}{Z_T + Z'_O}$

FIGURE 1.3-5a. Transmission Line with Distributed Loading



TL/F/10974–2

- Length of Transmission Line = L
- Delay of Transmission Line = T
- Time of Sample = t
- Incident Wave Current = I_1
- Incident Wave Voltage = V_1
- Reflected Wave Current = I_R
- Reflected Wave Voltage = V_R
- Characteristic Impedance of Line = Z_O
- Termination Impedance = Z_T
- Voltage at Termination = V_T

FIGURE 1.3-5b. Reflections Due to Impedance Mismatching

Line Driving and Termination (Continued)

There are several termination schemes which may be used. Included are series, parallel, AC parallel, and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

SERIES TERMINATIONS

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line or especially for single point loads. Loads that are between the driver and the end of the line will receive a two-step waveform. The first step will be the incident wave, V_i. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor, and the impedance of the line according to the formula

$$V_i = V_{DD} \bullet Z'_o/(Z'_o + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. Z_S for 'LVQ is approximately 17Ω. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

PARALLEL TERMINATION

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{DD} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

AC PARALLEL TERMINATION

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The terminating effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin Termination

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{DD} or ground, increasing power consumption.

- Parallel: Resistor = Z_o
- Thevenin: Resistor = $2 \times Z_o$
- Series: Resistor = $Z_o - Z_{out}$
- AC: Resistor = Z_o

  Capacitor = $C \geq \frac{3tr}{Z_o}$

FIGURE 1.3-6b. Suggested Termination Values

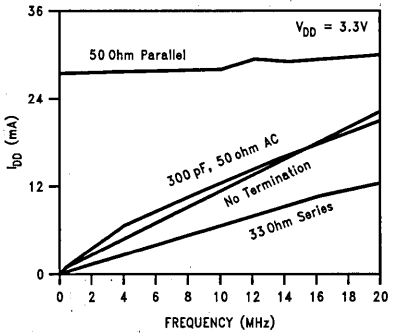


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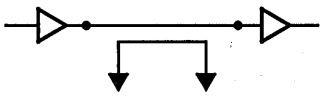
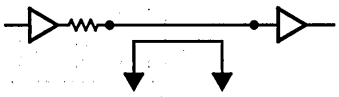
FIGURE 1.3-6c. LVQ I_{DD} vs Termination



TL/F/10974–3

a. No Termination



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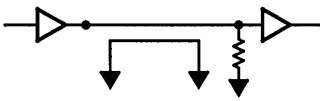
b. Series Termination



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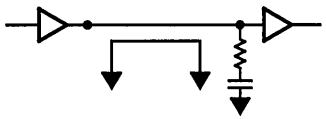
c. Parallel Termination



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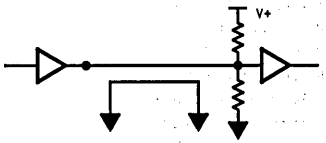
d. AC Parallel Termination



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e. Thevenin Termination

FIGURE 1.3-6a. Termination Schemes

Thevenin Termination (Continued)

LVQ circuits have been designed to drive 75Ω transmission lines over the full commercial temperature range. This is guaranteed by the specified dynamic drive capability of 36 mA source and 25 mA sink current. This ensures incident wave switching on 75Ω transmission lines and is consistent with the 3 ns rated edge transition time.

LVQ product inputs take advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} are specified at 2.0V and 0.8V respectively. The corresponding output levels, V_{OH} and V_{OL}, are specified to be within 0.1V of the rails, of which the output is sourcing or sinking 50 μA or less. These noise margins are outlined in *Figure 1.3-7.*

TL/F/10974–9

FIGURE 1.3-7. LVQ Input Threshold

CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{DD} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 1.3-8 exemplifies the situation when power is removed. Any input driven above the V_{DD} pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{DD} or any output that is HIGH. Depending upon the system, this current, I_{IN}, can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line. Another possible solution would be to ensure that the output enable input is inactive, preventing the outputs from turning on and loading down the bus. This may be accomplished by hardwiring a 4.7 kΩ pull-up resistor to the V_{DD} pin of the LVQ device.

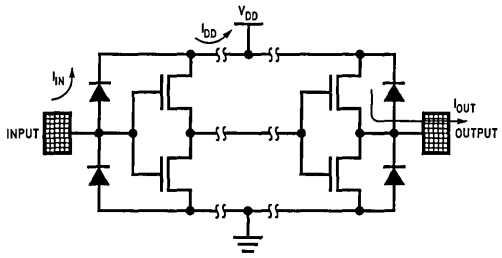

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FIGURE 1.3-8. Noise Effects

Noise Effects

LVQ offers excellent noise immunity. With input thresholds specified at 2.0V and 0.8V and outputs that drive to within 100 mV of the rails, LVQ devices offer noise margins approaching 30% of V_{DD}. At 3.3V V_{DD}, LVQ specified input and output levels give almost 1.0V of noise margin for both ground- and V_{DD}-born noise. With realistic input thresholds closer to 50% of V_{DD}, the actual margins approach 1.5V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the performance of LVQ circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

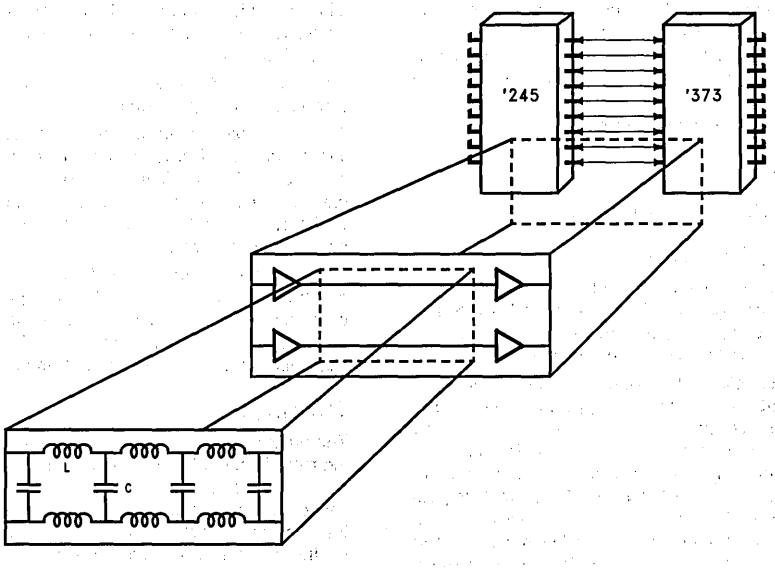
Crosstalk has two basic causes. Forward crosstalk, *Figures 1.3-9b* and *1.3-9d*, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air (ϵ_r = 1.0) and epoxy glass (ϵ_r = 4.7).

Crosstalk (Continued)

As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, *Figures 1.3-9c* and *1.3-9e*, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. LVQ's AC noise margins, shown in *Figure 1.3-10b*, show the immunity to everyday noise which can effect system reliability.



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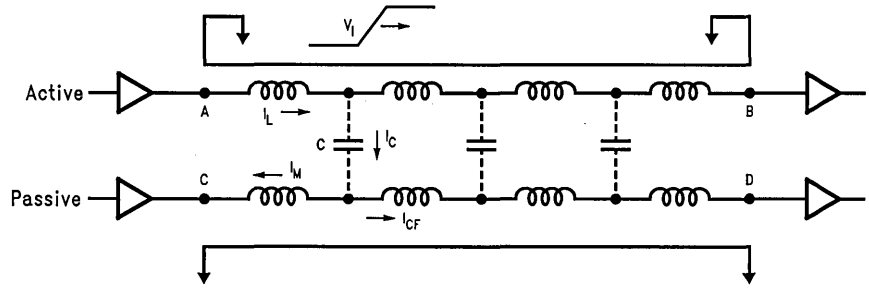
■ Two parallel signal lines provide mutual inductance and shunt capacitance.

FIGURE 1.3-9a. Where Does Crosstalk Take Place?

Crosstalk (Continued)



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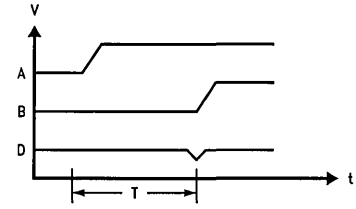
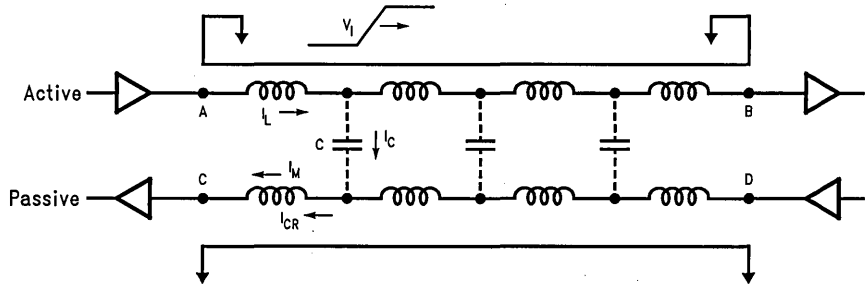
- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = I_C = -C dV_i/dt
- Mutually Induced Current = I_M = mI_L
- Forward Crosstalk Current = I_{CF}
- As the active signal, V_i, propagates from A to B a negative-going spike, V_f, propagates from C to D, coincident with V_i.



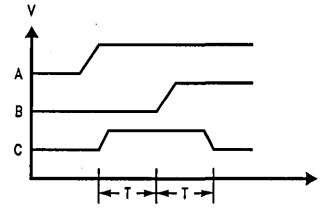
TL/F/10974–13

FIGURE 1.3-9b. Forward Crosstalk—Refresher



TL/F/10974–14

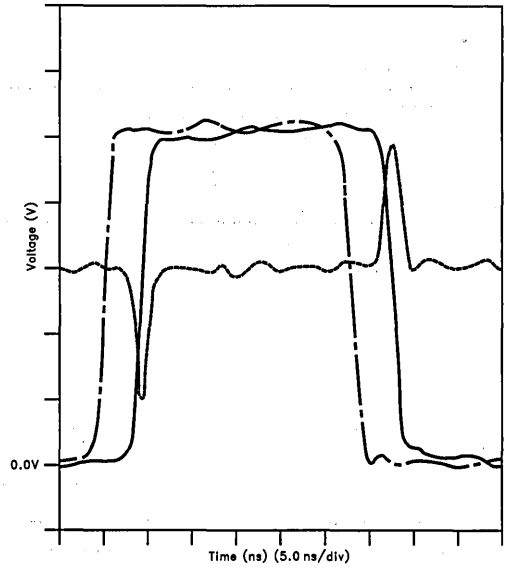
- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = I_C = -C dV_i/dt
- Mutually Induced Current = I_M = mI_L
- Reverse Crosstalk Current = I_{CR}
- As the active signal, V_i, propagates from A to B a positive pulse appears at C for a duration twice the coupled line delay T.



TL/F/10974–15

FIGURE 1.3-9c. Reverse Crosstalk—Refresher

Crosstalk (Continued)

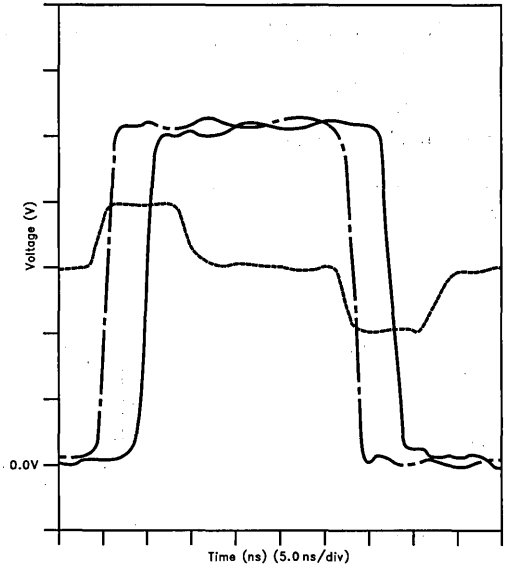


Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Forward Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

TL/F/10974–16

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

FIGURE 1.3-9d. Forward Crosstalk on PCB Traces



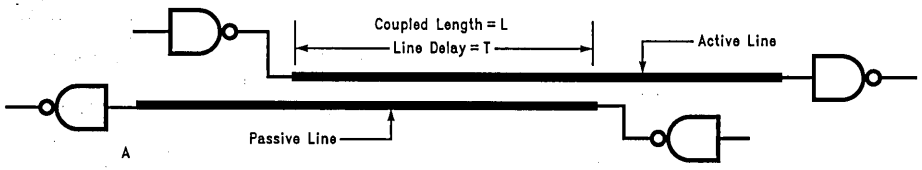
Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Reverse Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

TL/F/10974–17

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

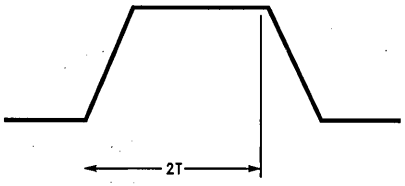
FIGURE 1.3-9e. Reverse Crosstalk on PCB Traces

Crosstalk (Continued)



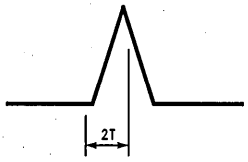
TL/F/10974–18

Noise Pulses at A:



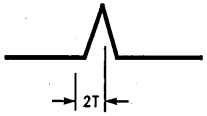
For $T > t_r$ Noise Reaches Max Amplitude

TL/F/10974–19



For $T = 0.5\ t_r$ Noise Just Reaches Max at Peak

TL/F/10974–20



For $T < 0.5\ t_r$ Noise Never Reaches Full Amplitude

TL/F/10974–21

FIGURE 1.3-9f. Partially Coupled Lines

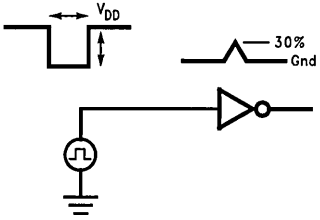


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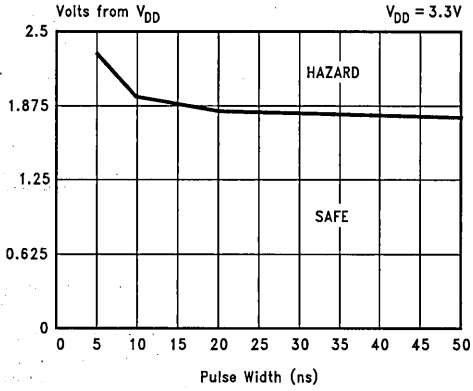
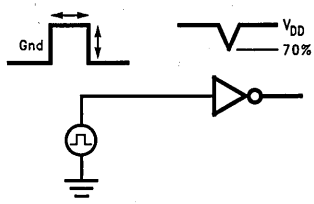
FIGURE 1.3-10a. High Noise Margin



TL/F/10974–23

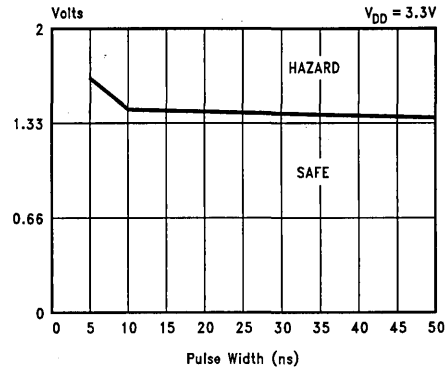
FIGURE 1.3-10b. LVQ High Noise Margin

Crosstalk (Continued)



TL/F/10974–25

FIGURE 1.3-10c. Low Noise Margin



TL/F/10974–24

FIGURE 1.3-10d. FACT AC/ACQ Low Noise Margin

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

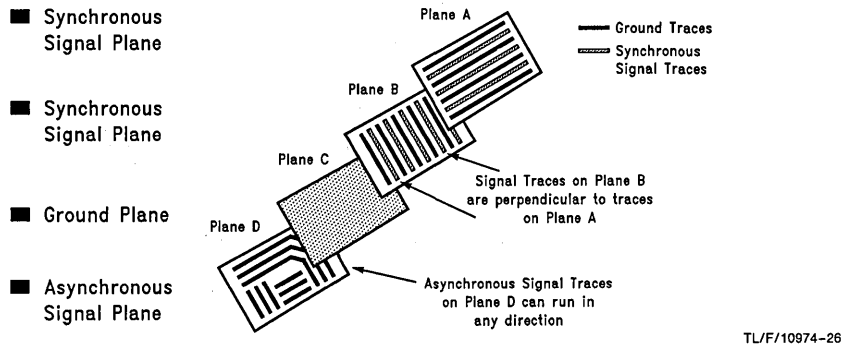


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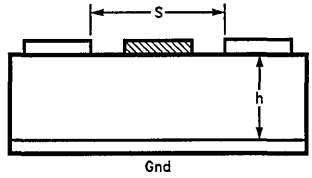
FIGURE 1.3-11a. Recommended Crosstalk—Avoidance Structure



- Minimize parallel trace lengths
- Maximize distance "S" between traces to minimize crosstalk
- Add ground trace between signal traces
- Minimize distance h to keep line impedance low

TL/F/10974–27

FIGURE 1.3-11b. PCB Layout Tips for Crosstalk Avoidance

Decoupling Requirements

National Semiconductor Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with LVQ products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. *Figure 1.3-12* displays various V_{DD} and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 100Ω and 150Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{DD} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in *Figure 1.3-13* to calculate the amount of decoupling necessary. This circuit utilizes an LVQ244 driving a 150Ω bus from a point somewhere in the middle.

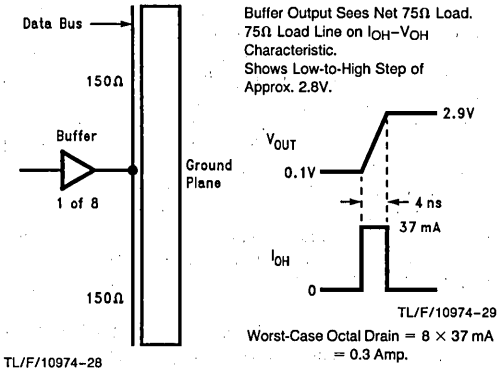


FIGURE 1.3-13. Octal Buffer Driving a 150Ω Bus

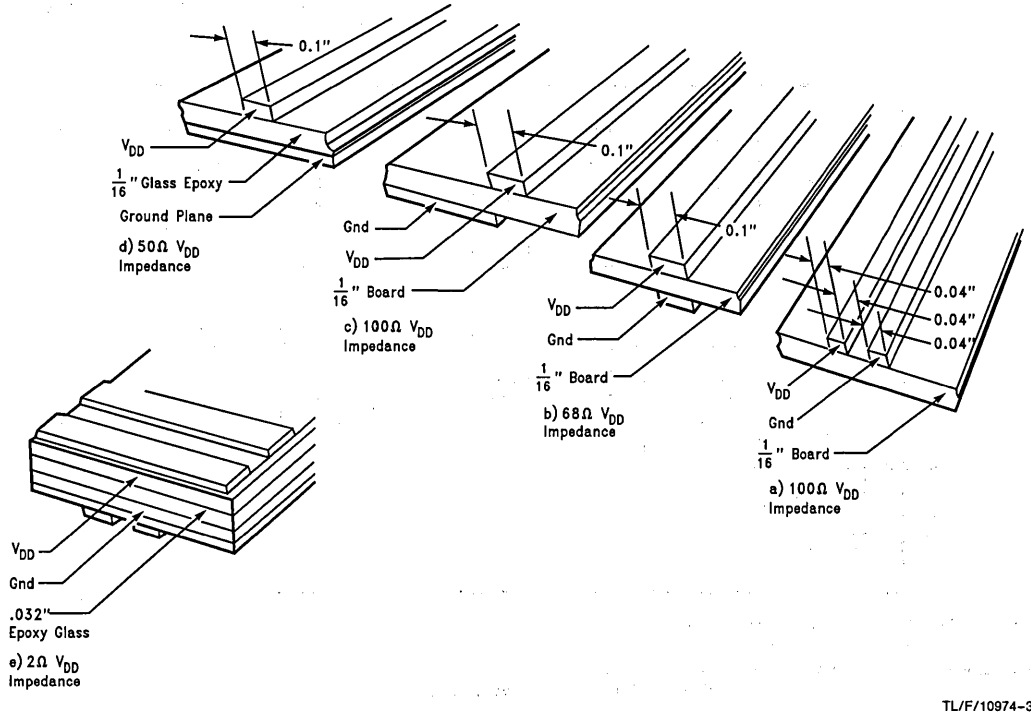


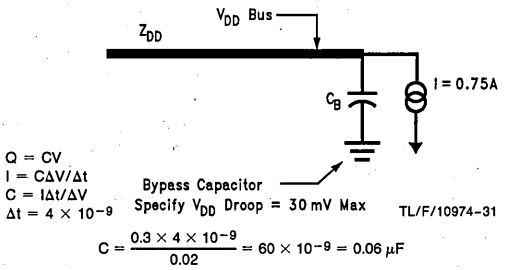
FIGURE 1.3-12. Power Distribution Impedances

Decoupling Requirements (Continued)

Being in the middle of the bus, the driver will see two 150Ω loads in parallel, or an effective impedance of 75Ω. To switch the line from rail to rail, a drive of 37 mA is needed; more than 300 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{DD} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in *Figure 1.3-14.*

In this example, if the V_{DD} droop is to be kept below 20 mV and the edge rate equals 4 ns, a 0.10 μF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.



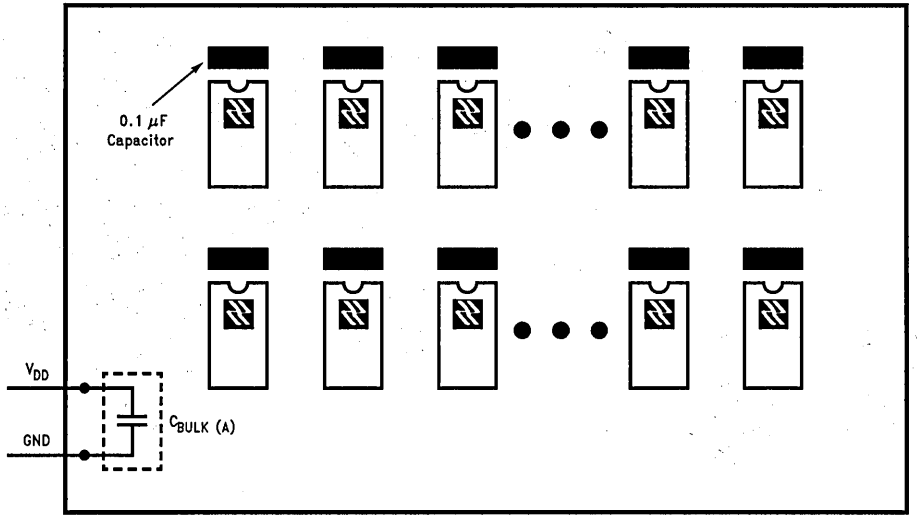
$$C = \frac{0.3 \times 4 \times 10^{-9}}{0.02} = 60 \times 10^{-9} = 0.06\ \mu F$$

Select $C_B \geq 0.10\ \mu F$

FIGURE 1.3-14. Formula for Calculating Decoupling Capacitors

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.



- Need to decouple board at the point of power supply entry
- This capacitor (A) will smooth low frequency bulk switching noise
- A large value electrolytic capacitor is typically used (50 μF–100 μF)

FIGURE 1.3-15. Board-Level Decoupling Capacitor

Electromagnetic Interference

One of the features of advanced CMOS is its fast output edge rates. For the first time a non-ECL logic family is capable of switching outputs at ECL speeds. In fact, advanced CMOS edge rates exceed that of ECL. ECL outputs typically swing 900 mV in 700 ps, translating into an edge rate of 1.3 V/ns. Advanced CMOS outputs, on the other hand, swing 5.0V in approximately 3.0 ns, translating into an edge rate of 1.6 V/ns. Logic families driving at these speeds, however, are more prone to generate higher levels of system noise. Electronic systems using advanced CMOS logic, as with any other high performance logic system, require a higher level of design considerations.

One element of system noise that will be discussed here is referred to as Electromagnetic Interference, or EMI. The level of EMI generated from a system can be greatly reduced with the use of proper Electromagnetic Compatibility (EMC) design techniques. These design considerations begin at the circuit board level and continue through the system level to the enclosures themselves; EMC needs to be a concern at the initial system design stage.

WHAT IS EMI/RFI?

Electromagnetic Interference, or EMI, is an electrical phenomenon where electric field energy and magnetic field energy are transmitted from one source to create interference of transmitted and/or received signals from another source. This may result in the information becoming distorted.

EMI can be an issue of emissions, that is, energy radiated from one system to another or within the same system. It can also be an issue of susceptibility, from high powered microwave signals or nuclear EMP (Electromagnetic Pulse)—an issue more applicable in the military arena than commercial. While this section will specifically address radiated energy, many comments may also apply to susceptibility.

SOURCES OF ELECTROMAGNETIC INTERFERENCE

EMI generation in an electronic system may result from several sources. All mediums of signal transmission—from the signal origin to its destination—are possible sources of radiated EMI. Understanding how each medium—including ICs, coaxial cables, and connectors—can radiate EMI is paramount in effective, high performance system design.

As *Figure 1.3-16* illustrates, EMI in a typical electronic circuit is generated by a current flowing in some current path configured within the circuit. These paths can be either V_{DD}-to-GND loops or output transmission lines. The propagating current pulse creates magnetic field energy, while the voltage drop across the loop area creates electric field energy. The current path material itself acts as an antenna radiating—or receiving—both the electric and magnetic fields.

EMI generation is a function of several factors. Transmitted signal frequency, duty cycle, edge rate, and output voltage swings are the major factors of the resultant EMI levels. *Figure 1.3-17* illustrates a generalized Fourier transformation of the transmitted signal from the time domain to the frequency domain. To think in terms of EMI, one must think in terms of the frequency domain. This illustration helps to realize the role of the time domain signal components in the frequency domain. Notice that as the signal's period decreases, duty cycle decreases, or rise/fall time decreases that the radiated bandwidth increases.

On the circuit level, in addition to the signal component factors mentioned earlier, radiating area, and the resultant antenna's radiating efficiency also play an important role in EMI generation. Also, current spikes, power line noise, and output ringing caused by outputs switching also contribute to the overall EMI. Good design techniques that moderate this noise will play a major role in minimizing radiated EMI.

OVERALL SYSTEM EMI

System EMI is a function of the current loop area. Some of the largest loop areas in a system consist of circuit board signal transmission lines, backplane transmission lines, and I/O cables. The current loop areas of the integrated circuit packages—V_{DD}-to-GND loops—are small in comparison to those of the transmission lines and I/O cables. Differences in IC package pinout schemes are much less noticeable in terms of overall system radiated EMI.

The formula used to model the maximum electric field is listed below. This formula takes into account the antenna dimension and efficiency as well as the basic signal components.

$$|E|_{Max} = \frac{1.32 \times 10^{-3} \bullet I \bullet A \bullet Freq^2}{D}\left[1 + \left(\frac{\lambda}{2}\pi D\right)^2\right]^{1/2} \frac{\mu V}{m}$$

where,

$|E|_{Max}$ is the maximum E-field in the plane of the loop

I is the current amplitude in milliamps

A is the antenna area in square cm

λ is the wavelength at the frequency of interest

D is the observation distance in meters

Freq is the frequency in MHz

and the perimeter of the loop $P \ll \lambda$.

Figure 1.3-18 illustrates lab measurements of radiated emissions from a test board populated with FACT and LVQ logic. The device under test is driving a similar device across 26 cm of printed circuit board trace.

At higher frequencies where, for example, quarter wavelengths approach the lengths of transmission lines common in typical backplanes and plug-in cards, LVQ radiates substantially less EMI than other ACMOS logic.

CIRCUIT BOARD DESIGN CONSIDERATIONS

Original equipment manufacturers cannot afford to fail electromagnetic emissions tests. Since these tests are measured outside of the system, precautions to shield the enclosures, I/O cables, and connections are paramount. However, EMI within a system may also cause errors in data trans-

Electromagnetic Interference (Continued)

mission or unreliable system operation. Therefore, good EMC design techniques at the circuit board level are just as necessary.

Designing a system free of all EMI is an overwhelming task. However, considering the following design recommendations at the circuit board level forms a good foundation on which to design a system with good EMC.

- The use of multilayer printed circuit board is a virtual necessity. Two-sided printed circuit board and wire-wrap boards provide no shielding of EMI. Two-sided boards also do not allow the use of power and ground planes. Instead they require the use of high impedance power and ground traces. Planes provide impedances several orders of magnitude lower than that of traces, reducing transient voltage drops in the power distribution and return loops. As a result of these lower voltage drops, power supply induced EMI can also be reduced.
- In addition to the reduced impedance, these power and ground planes have an inherent EMI shielding effect that the large areas of copper provide. With the use of striplines or signal transmission lines sandwiched between the power and ground planes, the designer can take full advantage of the planes' shielding capabilities. To maximize this shielding effect, keep the power and ground plane areas as homogeneous as possible.
- Since plastic provides no EMI shielding, and sockets of any profile provide plenty of lead length, ICs should be soldered directly to the board. Solder power and ground pins directly to the power and ground planes, respectively. Minimize the IC and associated component lead lengths wherever possible.
- Minimizing the number of simultaneously switching outputs will also help to moderate the current pulse amplitude and output ringing.
- Terminating signal traces longer than 8 inches (typical) will minimize reflections and ringing due to those reflections.
- Avoid capacitively coupling signals from one transmission line to another—crosstalk—by avoiding long parallel signal transmission lines. If parallel transmission lines are unavailable, maximize the distance between the two lines, or insert a ground trace. Minimizing the spacing between the signal plane and ground plane will also help reduce crosstalk. For more details, see section on Crosstalk.

POWER SUPPLY DECOUPLING CONSIDERATIONS

Much of a system's radiated EMI may originate from the power supply itself. Propagation of power supply noise throughout a system is a very undersirable situation in any respect, including EMI. Suppression of this power supply noise is highly recommended. Decoupling the power supply at every level, from the system supply distribution network, down to the individual IC, is also a necessity when designing for low noise—and low EMI.

- On the system level, the use of a tantalum or aluminum electrolytic capacitor in the power supply distribution network is recommended.
- Decoupling the power supply at the point of entry onto the printed circuit board is also highly recommended. The use of a low equivalent series inductance, or ESL, multilayer ceramic capacitor, 50 μF to 100 μF, provides good low to medium frequency filtering and EMI suppression.
- To further suppress power supply noise and associated EMI throughout the circuit board itself, the use of a low ESL chip capacitor for each IC is highly recommended. Because the location of any transient noise on a power or ground plane would be impossible to predict, and the IC density of different circuit boards vary dramatically, every IC on these circuit boards should be adequately decoupled. A 0.10 μF chip capacitor, located as close to each ground pin as possible, will provide good high frequency power supply noise filtering and added EMI suppression.

BACKPLANE CONSIDERATIONS

The above discussion emphasized design techniques for printed circuit boards. However, because the backplane may, and usually does, consist of several long signal transmission lines, the same low noise design techniques should be used.

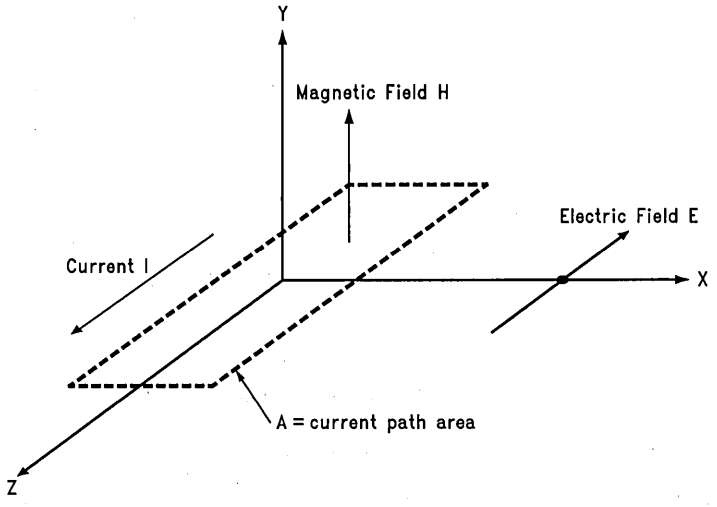
- Multilayer board techniques should also be applied to the backplane. If possible, these transmission lines should be shielded individually. This would allow for a denser parallel layout of transmission lines as well as providing good EMC.
- Use multiple ground and power connections from the backplane to the circuit boards' power and ground planes to minimize the connection impedance. This will help to further suppress any source of power supply generated EMI.

SYSTEM CONSIDERATIONS

One of the major sources of radiated system EMI are the edge connectors, I/O cables, and their associated connectors.

- Use care to ensure that, not only the cables are shielded and the shield properly grounded, but that the shield totally envelopes both the cable and its connectors. The shield should seat firmly into a grounded chassis and touch the chassis a full 360° around the connection. An open ended cable or an improperly grounded connector shield will be a prime suspect for out-of-spec EMI emissions and should be avoided. Use shielded coaxial cables whenever possible. If ribbon cable is preferred, shield all ribbon cables with commercially available ribbon cable shielding. Again, ensure that this shield is properly attached to the connector shield by a full 360°.
- In choosing or designing the enclosure for the system, minimize the number of openings in the enclosure. Since high performance logic now deals with smaller wavelengths than the older technologies, enclosure opening sizes should also be considered. Keep openings as small as possible. If openings are necessary (displays, controls, fans, etc.) there are commercially available accessories that offer good built-in EMI shielding.
- If access panels are necessary, ensure that these panels are properly sealed with some sort of shielding material (gaskets, copper brushes, etc.).
- Of course, the enclosure itself should be of a material that provides good shielding against electric fields.

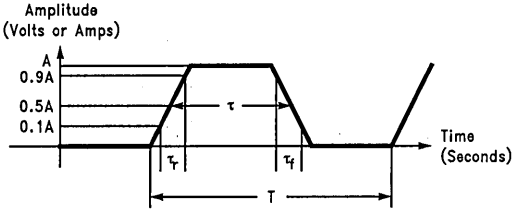
Electromagnetic Interference (Continued)



TL/F/10974–33

FIGURE 1.3-16. EMI is Generated by a Current Flowing along Some Path (Loop)

Time Domain: Trapezoidal Pulse Train



- τ = Pulse Width HIGH
- τ_r = Rise Time
- τ_f = Fall Time
- T = Period
- A = Amplitude

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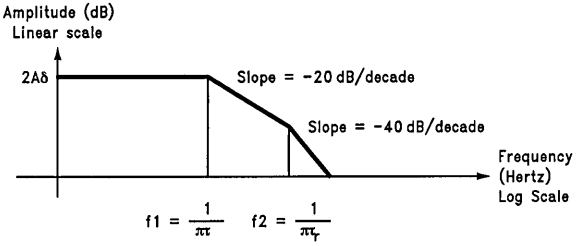
Frequency Domain: Worst-Case Upper Bound Approximation



- f_1 = 1st Breakpoint
- f_2 = 2nd Breakpoint
- δ = Duty Cycle = τ/T

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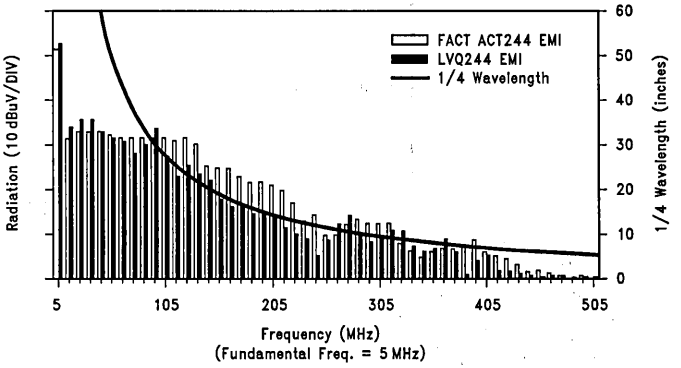
FIGURE 1.3-17. Time Domain to Frequency Domain Conversion

Electromagnetic Interference (Continued)



TL/F/10974–36

FIGURE 1.3-18a. Radiation—LVQ versus ACT244

Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

Such is the case with parts that have a bidirectional pin, exemplified by the '245 Octal Transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for I_{DD} and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static I_{DD} specification orders of magnitude less than standard load currents. Most CMOS I_{DD} specifications are usually less than 100 μA. When conducting an I_{DD} test, greater care must be taken so that other currents will not mask the actual I_{DD} of the device. These currents are usually sourced from the inputs and outputs.

Since the static I_{DD} requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an I_{DD} test. Even a standard 500Ω load resistor will sink 6 mA at 3V, which is more than twice the I_{DD} level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during I_{DD} tests.

Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, I_{DD} can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly ON, and a conduction is created from V_{DD} to ground. This conduction path

Testing Advanced CMOS Devices with I/O Pins (Continued)

leads to the increased I_{DD} current seen in the I_{DD} vs V_{IN} curve. When the input is at either rail, the input structure no longer conducts. Most I_{DD} testing is done with all of the inputs tied to either V_{DD} or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual I_{DD} of the device under test which is being measured by the tester.

When testing the I_{DD} of an LVQ245, problems can arise depending upon how the test is conducted. Note the structure of the '245's I/O pins illustrated below.

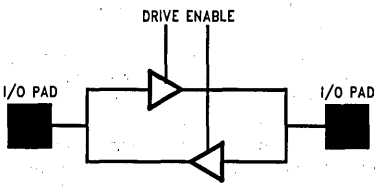


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FIGURE 1.3-22. '245 I/O Structure

Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the I_{DD} of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from V_{DD} to ground. A simple rule to follow is to treat any output which is disabled as an input. This will help insure the integrity of an I_{DD} test.

Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted below.

The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined I_{IN} specification of the input and the I_{OZ} specification of the output. This combined leakage test is defined as IOZ_T. For LVQ devices, I_{IN} is specified at ± 1 μA while I_{OZ} is specified at ± 6 μA. Combining these gives a limit of ± 7 μA for I/O pins. Usually, I/O pins will show leakages that are less than the I_{OZ} specification of the output alone.

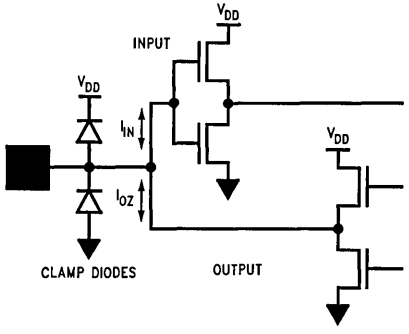

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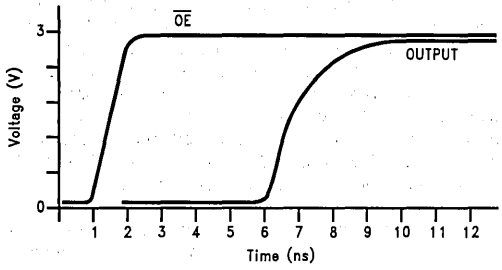
FIGURE 1.3-23. I/O Pin Internal Structure

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

Testing Disable Times of TRI-STATE® Outputs in a Transmission Line Environment

Traditionally, the disable time of a TRI-STATE buffer has been measured from the 50% point on the disable input, to the (V_{OL} + 0.3V) or (V_{OH} − 0.3V) point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown below.



TL/F/10974–39

FIGURE 1.3-24. Typical Bench TRI-STATE Waveform

ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. The following figure illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

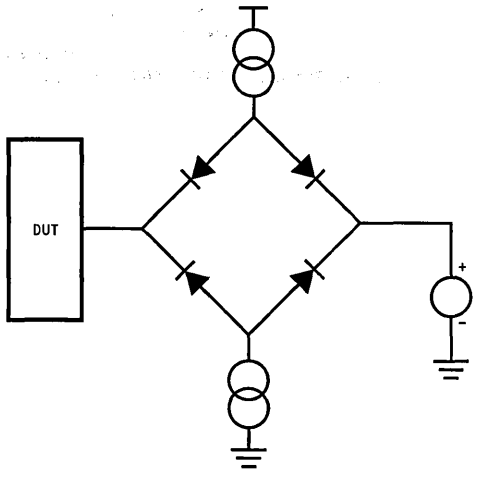


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FIGURE 1.3-25. MCT Wheatstone Bridge Test Load

Testing Disable Times of TRI-STATE Outputs in a Transmission Line Environment (Continued)

The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL}. When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the (V_{OL} + 0.3V) level or fallen to the (V_{OH} − 0.3V) level.

Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in *Figure 1.3-26.*

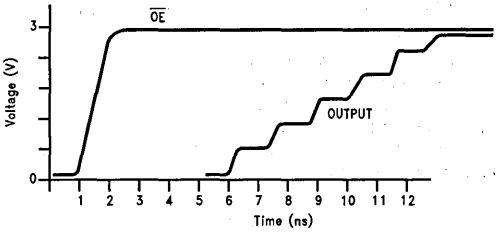

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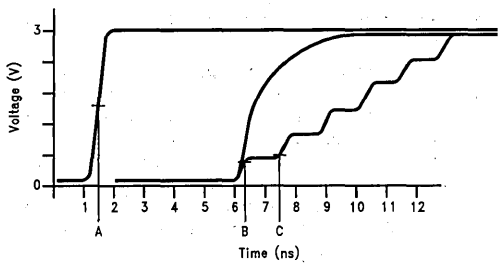
FIGURE 1.3-26. Typical ATE TRI-STATE Waveform

Transmission line theory states the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of 50Ω to 60Ω, this voltage step can be as minimal as 250 mV. If the comparator was programmed to the disable measurement points, it would be looking for a step of approximately 300 mV at 3.0V V_{DD}. Three reflections of the current pulse would be required before the comparator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customer's incoming tests, even though the device meets specifications. The figure below graphically shows this stepout.

Point A represents the typical 50% measurement point on tester driven waveforms. Point B reprsents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become nonrepeatable.



TL/F/10974–42

FIGURE 1.3-27. Measurement Stepout

National Semiconductor

54LVQ/74LVQ00
Low Voltage Quad 2-Input NAND Gate

General Description

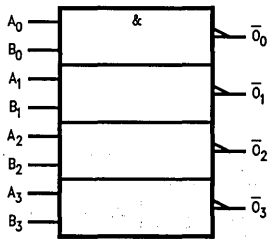
The 'LVQ00 contains four 2-input NAND gates.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

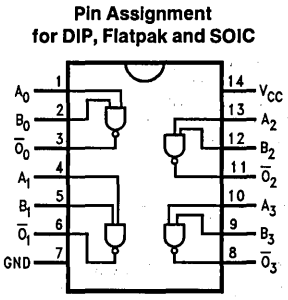
Ordering Code: See Section 8

Logic Symbol

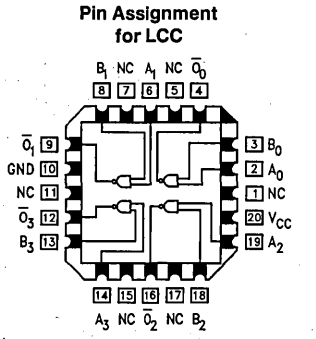


TL/F/11341–1

Connection Diagrams



TL/F/11341–2



TL/F/11341–3

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.5	50	25	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.6	1.0			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−1.0			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.5	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	2.0	7.0	9.5	1.0	11.0	2.0	10.0	ns	1.2-3,4
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.0	1.0	9.0	1.0	8.5	ns	1.2-3,4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	22	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ02
Low Voltage Quad 2-Input NOR Gate

General Description

The 'LVQ02 contains four, 2-input NOR gates.

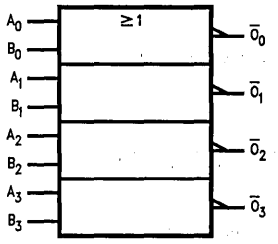
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

Ordering Code: See Section 8

Logic Symbol

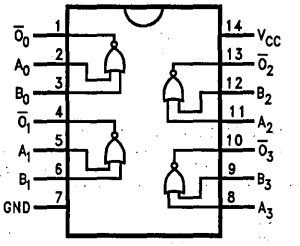
IEEE/IEC



TL/F/11342–1

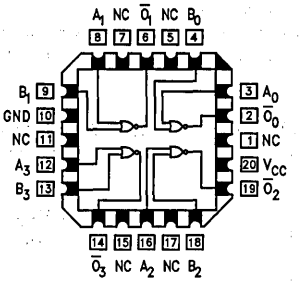
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11342–2

Pin Assignment for LCC



TL/F/11342–3

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C	74LVQ T_A = −55°C to +125°C	54LVQ T_A = −40°C to +85°C	74LVQ	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.5	50	25	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.6	1.0			V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.7	−1.0			V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	5.0	7.5	1.0	9.0	1.0	8.0	ns	1.2-3,4
t_{PHL}	Propagation Delay	3.3	1.5	5.0	7.5	1.0	9.0	1.0	8.0	ns	1.2-3,4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	20	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ04
Low Voltage Hex Inverter

General Description

The 'LVQ04 contains six inverters.

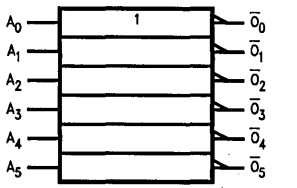
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

Ordering Code: See Section 8

Logic Symbol

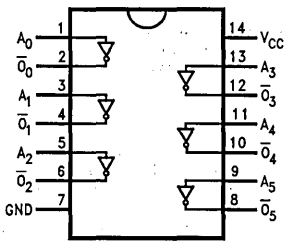
IEEE/IEC



TL/F/11343–1

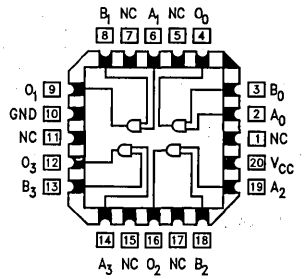
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11343–2

Pin Assignment for LCC



TL/F/11343–3

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.5	50	25	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.8	1.1			V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.8	−1.1			V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}) 0V to threshold (V_{IHD}) f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	4.5	9.0	1.0	11.0	1.0	10.0	ns	1.2-3,4
t_{PHL}	Propagation Delay	3.3	1.5	4.5	8.5	1.0	10.0	1.0	9.5	ns	1.2-3,4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	17	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ08
Low Voltage Quad 2-Input AND Gate

General Description

The 'LVQ08 contains four, 2-input AND gates.

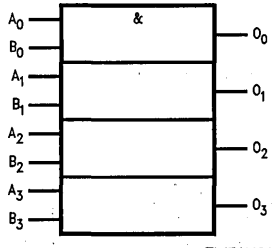
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

Ordering Code: See Section 8

Logic Symbols

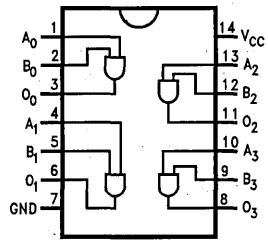
IEEE/IEC



TL/F/11344–1

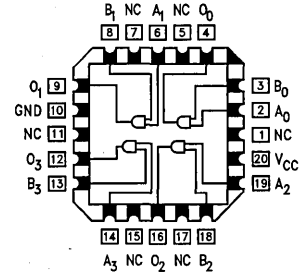
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11344–2

Pin Assignment for LCC



TL/F/11344–3

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.5	50	25	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8			V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8			V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0			V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for waveforms.

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	7.5	9.5	1.0	12.5	1.0	10.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	11.5	1.0	9.0	ns	1.2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	17	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ14
Low Voltage Hex Inverter with Schmitt Trigger Input

General Description

The 'LVQ14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The 'LVQ14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

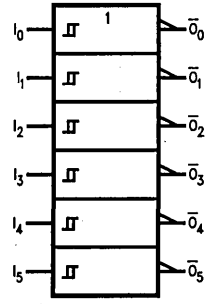
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

Ordering Code: See Section 8

Logic Symbol

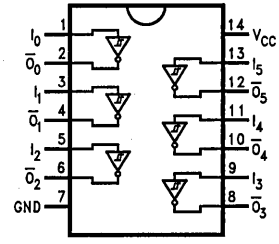
IEEE/IEC



TL/F/11345–1

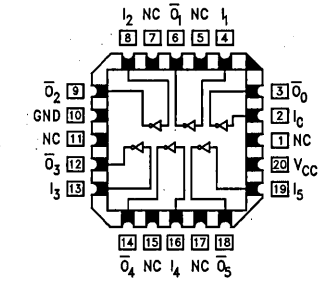
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11345–2

Pin Assignment for LCC



TL/F/11345–3

Function Table

Input	Output
A	$\overline{O}$
L	H
H	L

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46		*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
V_{t+}	Maximum Positive Threshold	3.0		2.2	2.2	2.2	V	T_A = Worst Case
V_{t-}	Minimum Negative Threshold	3.0		0.5	0.5	0.5	V	T_A = Worst Case

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$	54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
$V_{h(max)}$	Maximum Hysteresis	3.0		1.2	1.2	1.2	V	T_A = Worst Case
$V_{h(min)}$	Minimum Hysteresis	3.0		0.3	0.3	0.3	V	T_A = Worst Case
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.5	50	25	μA	V_{IN} = V_{CC} or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.9	1.1			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.8	−1.1			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.9	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.3	2.0			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, C_L = 50 pF			54LVQ $T_A = -55°C$ to $+125°C$, C_L = 50 pF		74LVQ $T_A = -40°C$ to $+85°C$, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	9.5	13.5	1.0	16.0	1.5	15.0	ns	1.2-3,4
t_{PHL}	Propagation Delay	3.3	1.5	7.5	11.5	1.0	14.0	1.5	13.0	ns	1.2-3,4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	20	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ32
Low Voltage Quad 2-Input OR Gate

General Description

The 'LVQ32 contains four, 2-input OR gates.

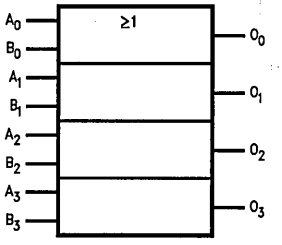
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

Ordering Code: See Section 8

Logic Symbol

IEEE/IEC



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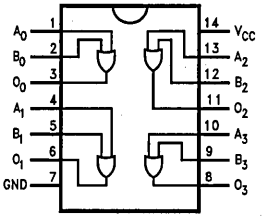
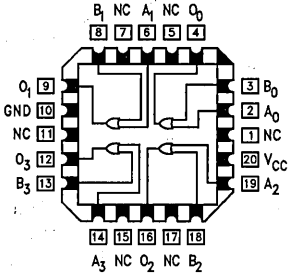
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11346–2

Pin Assignment for LCC



TL/F/11346–3

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ		54LVQ	74LVQ	Units	Conditions
			T_A = +25°C		T_A = −55°C to +125°C	T_A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1		I_{OUT} = 50 μA
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.5	50	25	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8			V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8			V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.9	2.0			V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	7.0	9.0	1.0	12.0	1.5	10.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	11.5	1.0	9.0	ns	1.2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	17	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ74
Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The 'LVQ74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

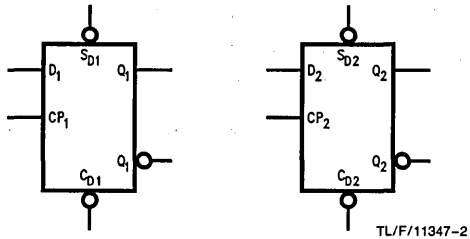
Asynchronous Inputs:
LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

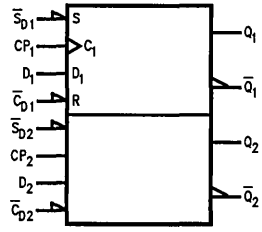
Ordering Code: See Section 8

Logic Symbols



TL/F/11347–1 TL/F/11347–2

IEEE/IEC

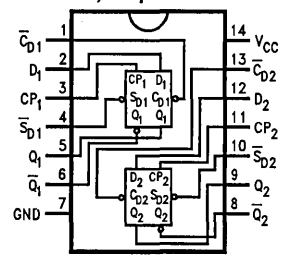


TL/F/11347–3

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs
$Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$	Outputs

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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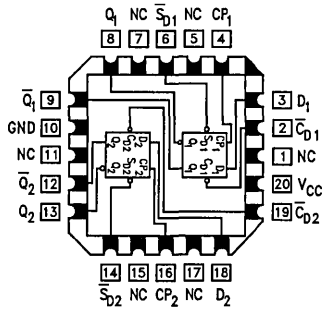
Pin Assignment for LCC



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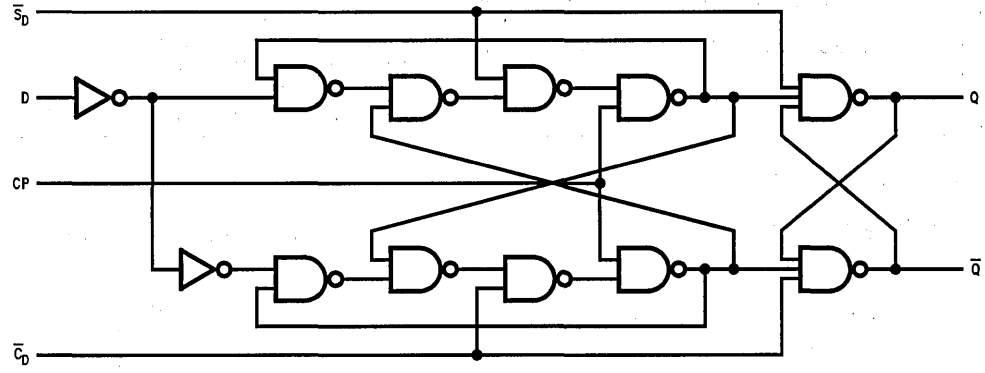
Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous Q($\overline{Q}$) before LOW-to-HIGH Transition of Clock

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.5	0.44		*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$	74LVQ $T_A = -55°C$ to $+125°C$	54LVQ $T_A = -40°C$ to $+85°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.5	50	25	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.2	0.8			V	(Notes 2 and 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.2	−0.8			V	(Notes 2 and 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 and 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2 and 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}, 0V to threshold (V_{IHD}, f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	100	125		70		95		MHz	
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	3.5	8.0	12.0	1.0	13.0	2.5	13.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	4.0	10.5	12.0	1.0	14.0	3.5	13.5	ns	1.2-3, 4
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	4.5	8.0	13.5	1.0	17.5	4.0	16.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	3.5	8.0	14.0	1.0	13.5	3.5	14.5	ns	1.2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$ $C_L = 50$ pF		54LVQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74LVQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Set-up Time, HIGH or LOW D_n to CP_n	3.3	1.5	4.0	5.0	4.5	ns	1.2-7
t_H	Hold Time, HIGH or LOW D_n to CP_n	3.3	−2.0	0.5	0.5	0.5	ns	1.2-7
t_W	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3	3.0	5.5	8.0	7.0	ns	1.2-3
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3	−2.5	0	0.5	0	ns	1.2-3, 7

*Voltage Range is 3.3V ±0.3V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 3.3V$
C_{PD} (Note 1)	Power Dissipation Capacitance	25	pF	$V_{CC} = 3.3V$

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ86
Low Voltage Quad 2-Input Exclusive-OR Gate

General Description

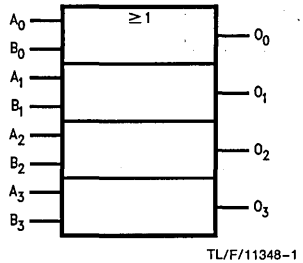
The 'LVQ86 contains four, 2-input exclusive-OR gates.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

Ordering Code: See Section 8

Logic Symbol



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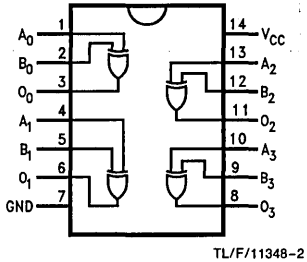
Connection Diagrams



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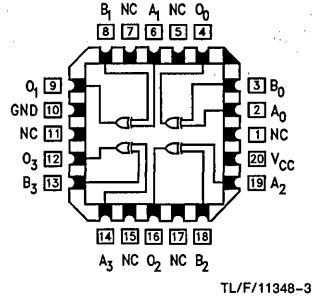


TL/F/11348–3

Pin Names	Description
A_0–A_3	Inputs
B_0–B_3	Inputs
O_0–O_3	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = 25°C	54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44		*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.5	50	25	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8			V	(Notes 2, 4)

†Maximum test duration 20 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay Inputs to Outputs	3.3	2.0	6.0	11.5	1.0	14.0	1.5	12.5	ns	1.2-3, 4
t_{PLH}	Propagation Delay Inputs to Outputs	3.3	2.0	6.5	11.5	1.0	14.0	1.5	12.5	ns	1.2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V

**Skews defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	23	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ138
Low Voltage 1-of-8 Decoder/Demultiplexer

General Description

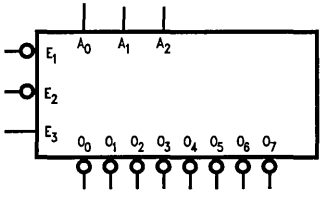
The 'LVQ138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'LVQ138 devices or a 1-of-32 decoder using four 'LVQ138 devices and one inverter.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Demultiplexing capability
- Multiple input enable for each expansion
- Active LOW mutually exclusive outputs

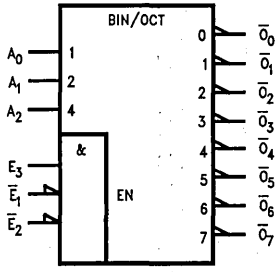
Ordering Code: See Section 8

Logic Symbol



TL/F/11350–1

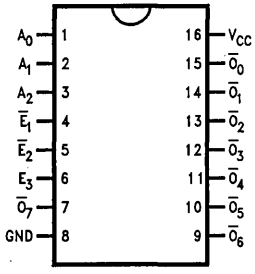
IEEE/IEC



TL/F/11350–4

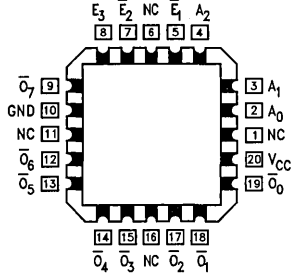
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11350–2

Pin Assignment for LCC



TL/F/11350–3

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

Functional Description

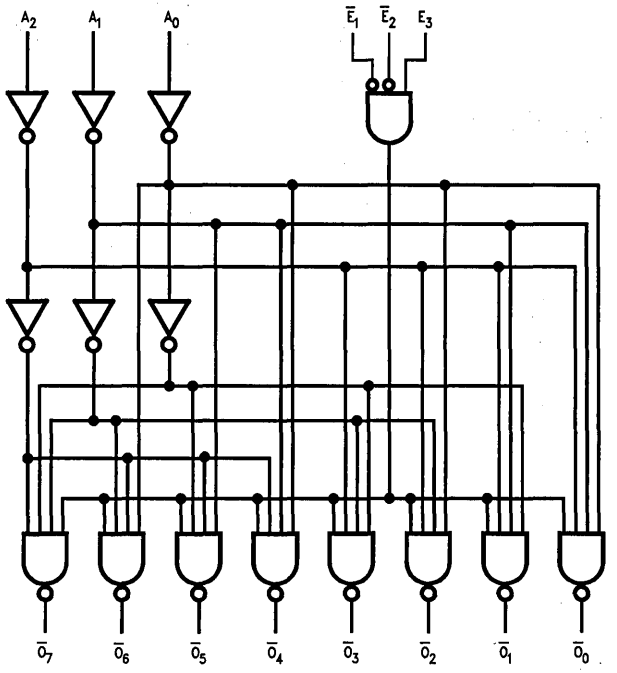
The 'LVQ138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The 'LVQ138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'LVQ138 devices and one inverter (see *Figure 1*). The 'LVQ138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/11350–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

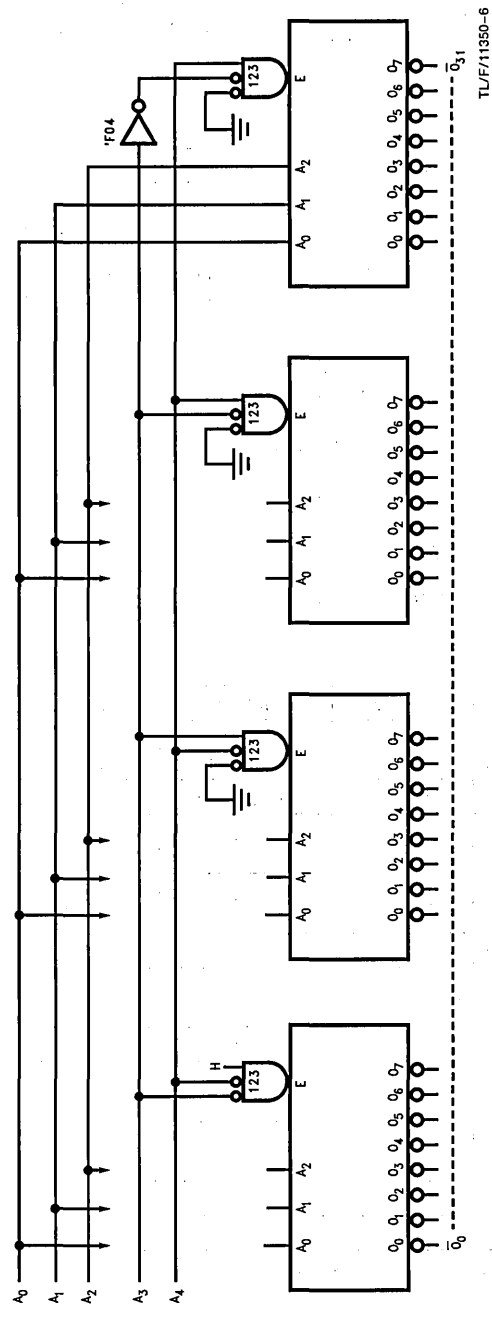


FIGURE 1. Expansion to 1-of-32 Decoding

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Outut Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$	54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8			V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8			V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.5	8.5	13.0	1.0	16.0	1.5	15.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.5	8.0	12.5	1.0	15.0	1.5	14.0	ns	1.2-3, 4
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3	1.5	11.0	15.0	1.0	16.5	1.5	16.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3	1.5	9.5	13.5	1.0	15.5	1.5	15.0	ns	1.2-3, 4
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	3.3	1.5	11.0	15.5	1.0	17.0	1.5	16.5	ns	1.2-3, 4
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	3.3	1.5	8.5	13.0	1.0	15.0	1.5	14.0	ns	1.2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage range is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 3.3V$
C_{PD} (Note 1)	Power Dissipation Capacitance	45	pF	$V_{CC} = 3.3V$

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ151
Low Voltage 8-Input Multiplexer

General Description

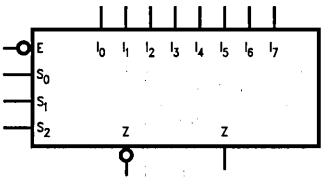
The 'LVQ151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The 'LVQ151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

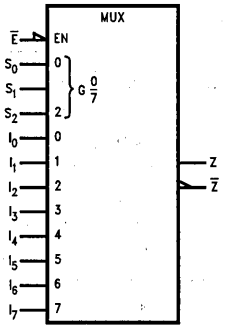
Ordering Code: See Section 8

Logic Symbol



TL/F/11351–1

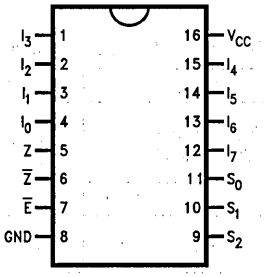
IEEE/IEC



TL/F/11351–4

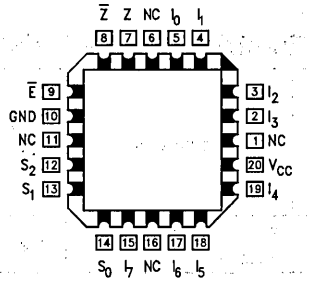
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11351–2

Pin Assignment for LCC



TL/F/11351–3

Truth Table

Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Pin Names	Description
I_0–I_7	Data Inputs
S_0–S_2	Select Inputs
$\overline{E}$	Enable Input
Z	Data Output
$\overline{Z}$	Inverted Data Output

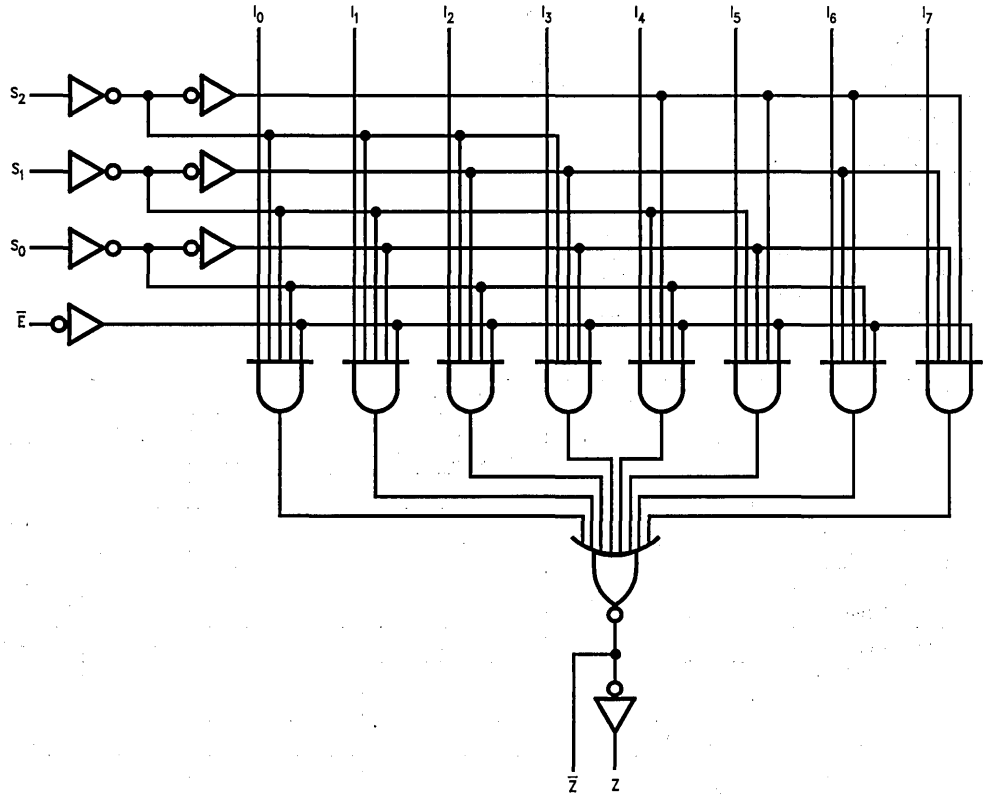
Functional Description

The 'LVQ151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

The 'LVQ151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the 'LVQ151 can provide any logic function of four variables and its complement.

Logic Diagram



TL/F/11351–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8			V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8			V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	3.0	11.5	18.0	1.0	22.0	3.0	20.0	ns	1.2-3,4
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	2.5	12.0	18.0	1.0	22.0	2.5	20.0	ns	1.2-3,4
t_{PLH}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3	2.5	8.0	13.0	1.0	15.5	2.0	14.0	ns	1.2-3,4
t_{PHL}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3	1.5	8.5	13.0	1.0	15.5	1.5	14.0	ns	1.2-3,4
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	2.5	9.5	14.0	1.0	16.0	2.0	15.5	ns	1.2-3,4
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	2.5	9.5	15.0	1.0	18.0	2.0	16.0	ns	1.2-3,4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	45	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ157
Low Voltage Quad 2-Input Multiplexer

General Description

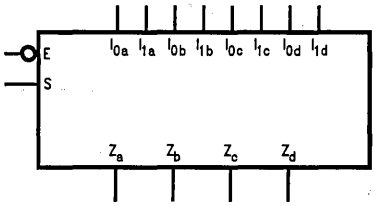
The 'LVQ157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The 'LVQ157 can also be used as a function generator.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω.

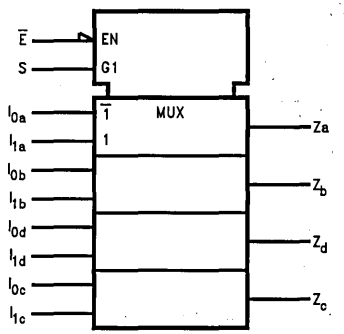
Ordering Code: See Section 8

Logic Symbols



TL/F/11352–1

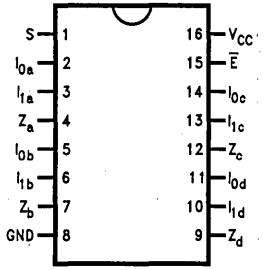
IEEE/IEC



TL/F/11352–3

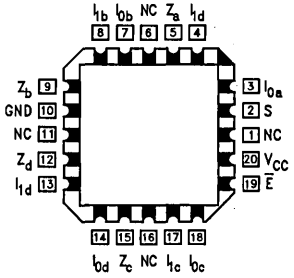
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11352–2

Pin Assignment for LCC



TL/F/11352–4

Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

Functional Description

The 'LVQ157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'LVQ157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

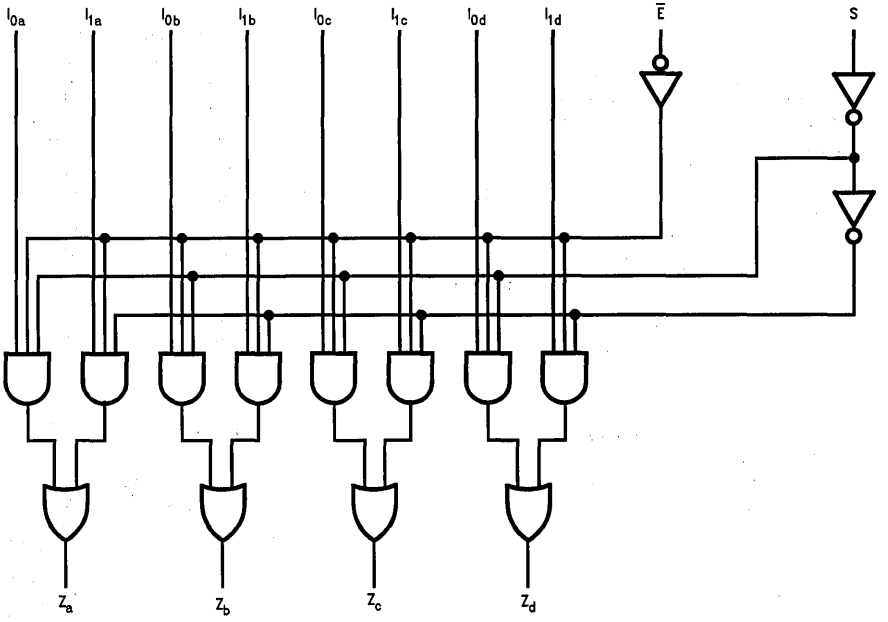
A common use of the 'LVQ157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'LVQ157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/11352–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.7	0.8			V	(Notes 2 & 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8			V	(Notes 2 & 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 & 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for waveforms.

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	3.3	1.5	7.0	11.5	1.0	16.0	1.5	13.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay S to Z_n	3.3	1.5	6.5	11.0	1.0	14.0	1.5	12.0	ns	1.2-3, 4
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	3.3	1.5	7.0	11.5	1.0	16.0	1.5	13.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	3.3	1.5	6.5	11.0	1.0	14.0	1.5	12.0	ns	1.2-3, 4
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.5	1.0	11.0	1.0	9.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.0	1.0	11.0	1.0	9.0	ns	1.2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	34.0	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ174
Low Voltage Hex D Flip-Flop with Master Reset

General Description

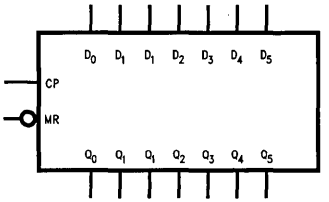
The 'LVQ174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

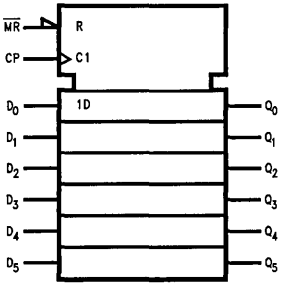
Ordering Code: See Section 8

Logic Symbols



TL/F/11353–1

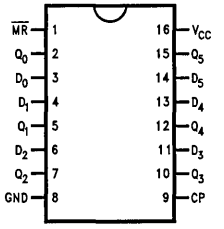
IEEE/IEC



TL/F/11353–2

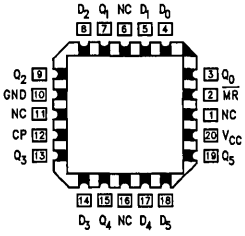
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11353–3

Pin Assignment for LCC



TL/F/11353–4

Pin Names	Description
D_0–D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_5	Outputs

Functional Description

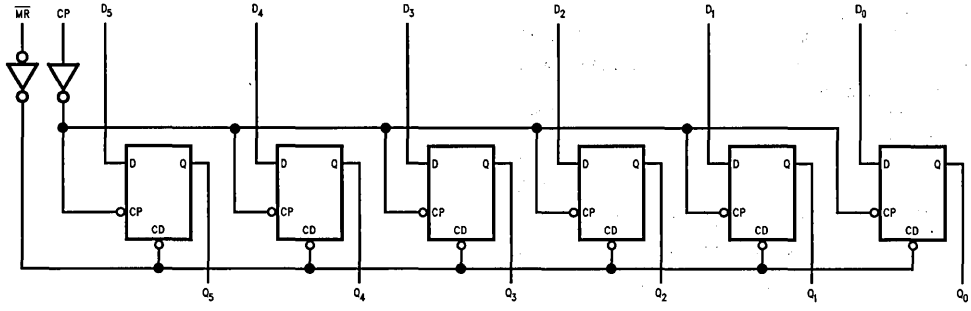
The 'LVQ174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 'LVQ174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	↗	H	H
H	↗	L	L
H	L	X	Q

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Logic Diagram



TL/F/11353–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		3.0		2.56	2.4	2.46	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		3.0		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.7	0.8			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.6	−0.8			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	90	100		65		70		MHz	
t_{PLH}	Propagation Delay CP to Q_n	3.3	2.0	9.0	11.5	1.0	14.0	1.5	12.5	ns	1.2-3,4
t_{PHL}	Propagation Delay CP to Q_n	3.3	2.0	8.5	11.0	1.0	13.0	1.5	12.0	ns	1.2-3,4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3	2.5	9.0	11.5	1.0	13.5	2.0	12.5	ns	1.2-3,4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 1.2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$ $C_L = 50$ pF		54LVQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74LVQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	2.5	6.5	7.5	7.0	ns	1.2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	1.0	3.0	3.0	3.0	ns	1.2-7
t_w	$\overline{MR}$ Pulse Width, LOW	3.3	1.0	5.5	7.0	7.0	ns	1.2-3
t_w	CP Pulse Width	3.3	1.0	5.5	7.0	7.0	ns	1.2-3
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3	0	2.5	3.0	2.5	ns	1.2-3,7

*Voltage Range is 3.3V ±0.3V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	23	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ241
Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'LVQ241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

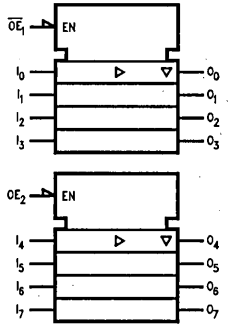
Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbol

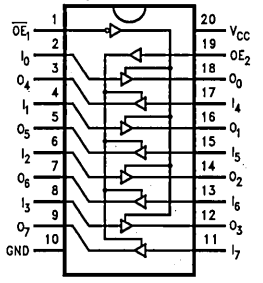
IEE/IEC



TL/F/11355–1

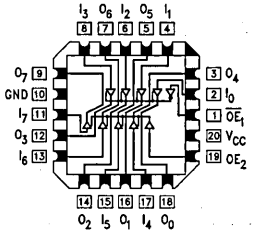
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11355–2

Pin Assignment for LCC



TL/F/11355–3

Pin Names	Description
$\overline{OE}_1$, OE_2	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE_2	I_n	
L	X	Z
H	H	H
H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) $-0.5V$ to $+7.0V$

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ -20 mA
- $V_I = V_{CC} + 0.5V$ $+20$ mA

DC Input Voltage (V_I) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ -20 mA
- $V_O = V_{CC} + 0.5V$ $+20$ mA

DC Output Voltage (V_O) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Source or Sink Current (I_O) ± 50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ± 50 mA

Storage Temperature (T_{STG}) $-65°C$ to $+150°C$

DC Latch-Up Source or Sink Current ± 300 mA

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'LVQ 3.0V to 3.6V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74LVQ $-40°C$ to $+85°C$
- 54LVQ $-55°C$ to $+125°C$

Minimum Input Edge Rate $\Delta V/\Delta t$
- V_{IN} 0.8V to 2.0V
- V_{CC} @ 3.0V 125 mV/ns

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from $-40°C$ to $+125°C$.

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		3.0		2.56	2.4	2.46	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		3.0		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$	54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.5	±10.0	±5.0	μA	V_I(OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n−1 Inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	3.3	2.0	6.5	9.0			2.0	9.5	ns	1.2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.0	13.0			2.5	13.5	ns	1.2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	8.5	14.5			1.0	15.0	ns	1.2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew **Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

Voltage Range is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	70	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ244
Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'LVQ244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

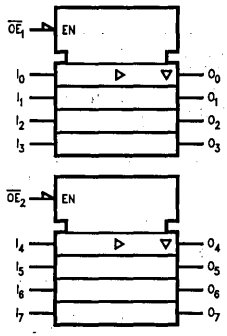
Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbol

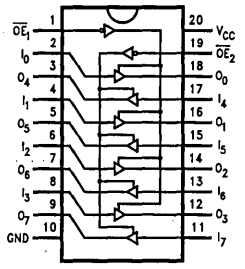
IEE/IEC



TL/F/11356–1

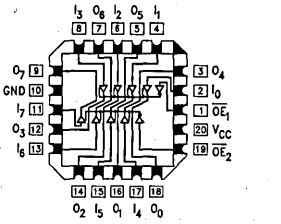
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11356–2

Pin Assignment for LCC



TL/F/11356–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_o)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded thresholds on input associated with output under test.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.5		±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8			V	(Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	3.3	2.0	7.0	9.0			2.0	9.5	ns	1.2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.0	12.0			2.5	12.5	ns	1.2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.0	13.5			1.0	14.0	ns	1.2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD}	Power Dissipation Capacitance	70	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ245
Low Voltage Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

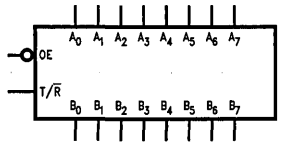
The 'LVQ245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 12 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbols



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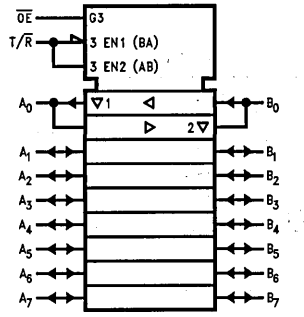
IEEE/IEC



TL/F/11357–2

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A TRI-STATE Inputs or TRI-STATE Outputs
B_0–B_7	Side B TRI-STATE Inputs or TRI-STATE Outputs

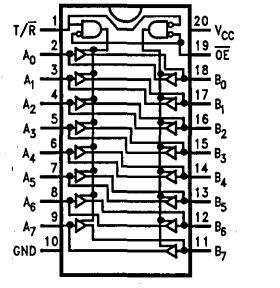
Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

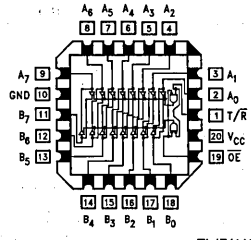
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11357–3

Pin Assignment for LCC



TL/F/11357–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ ns

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = +12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	3.6		±0.6	±11.0	±6.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	3.3	2.0	7.5	10.0			2.0	10.5	ns	1.2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3	3.0	8.5	13.0			3.0	13.5	ns	1.2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	8.5	14.5			1.0	15.0	ns	1.2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
$C_{I/O}$	Input/Output Capacitance	15	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	67	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ273
Low Voltage Octal D Flip-Flop

General Description

The 'LVQ273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

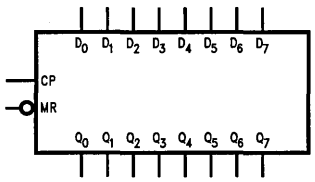
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbols



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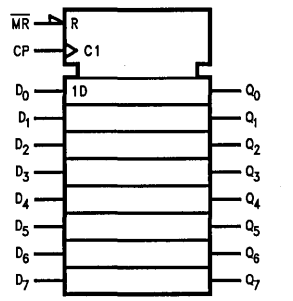
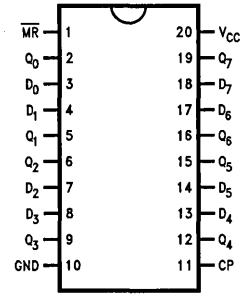
IEEE/IEC



TL/F/11358–2

Connection Diagrams

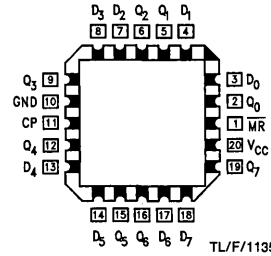
Pin Assignment for DIP, Flatpak and SOIC



TL/F/11358–3

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

Pin Assignment for LCC



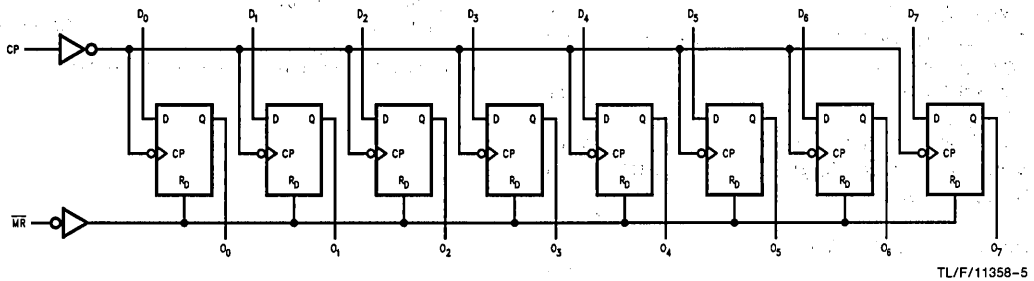
TL/F/11358–4

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/11358–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46		*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44		*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6				−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3			90		75		75	MHz	
t_{PLH}	Propagation Delay CP to Q_n	3.3	4.0	8.0	12.5	1.0	15.0	3.0	14.0	ns	1.2-3, 4
t_{PHL}	Propagation Delay CP to Q_n	3.3	4.0	8.5	13.0	1.0	16.0	3.5	14.5	ns	1.2-3, 4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3	4.0	8.5	13.0	1.0	16.0	3.5	14.0	ns	1.2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew**	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$ $C_L = 50$ pF		54LVQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74LVQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3		5.0	8.0	6.0	ns	1.2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3		0.0	0.0	0.0	ns	1.2-7
t_w	Clock Pulse Width HIGH or LOW	3.3		5.5	6.5	6.0	ns	1.2-7
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	3.3		5.5	10.0	6.0	ns	1.2-7
t_w	Recovery Time $\overline{MR}$ to CP	3.3		4.0	6.0	4.5	ns	1.2-3

*Voltage Range is 3.3V ±0.3V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 3.3V$
C_{PD} (Note 1)	Power Dissipation Capacitance	35	pF	$V_{CC} = 3.3V$

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ373
Low Voltage Octal Transparent Latch with TRI-STATE® Outputs

General Description

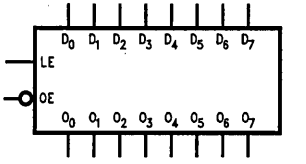
The 'LVQ373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

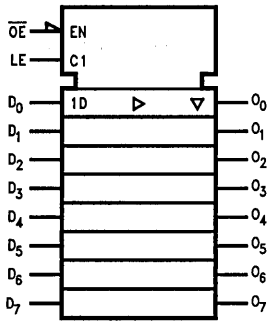
Ordering Code: See Section 8

Logic Symbols



TL/F/11359–1

IEEE/IEC

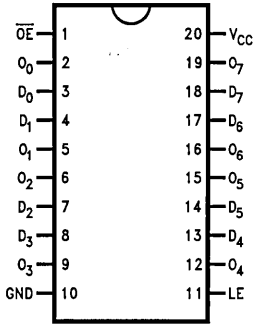


TL/F/11359–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

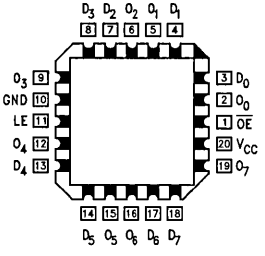
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/11359–3

Pin Assignment for LCC



TL/F/11359–4

Functional Description

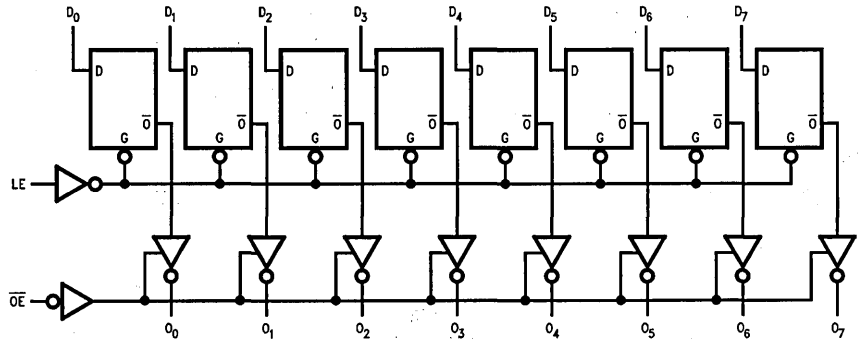
The 'LVQ373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/11359–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C	54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$	54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.5	±10.0	±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	3.3	2.5	8.0	10.5			2.5	11.0	ns	1.2-3, 4
t_{PLH}, t_{PLH}	Propagation Delay LE to O_n	3.3	2.5	8.0	12.0			2.5	12.5	ns	1.2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.5	13.0			2.5	13.5	ns	1.2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.0	14.5			1.0	15.0	ns	1.2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$ $C_L = 50$ pF		54LVQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74LVQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3	0	3.0		3.0	ns	1.2-7
t_h	Hold Time, HIGH or LOW D_n to LE	3.3	0	1.5		1.5	ns	1.2-7
t_w	LE Pulse Width, HIGH	3.3	2.0	4.0		4.0	ns	1.2-3

*Voltage Range is 3.3V ±0.3V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 3.3V$
C_{PD} (Note 1)	Power Dissipation Capacitance	39	pF	$V_{CC} = 3.3V$

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ374
Low Voltage Octal D Flip-Flop with TRI-STATE® Outputs

General Description

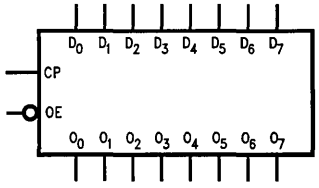
The 'LVQ374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs drive bus lines or buffer memory address registers

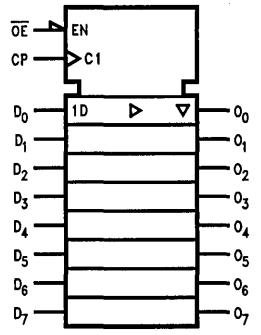
Ordering Code: See Section 8

Logic Symbols



TL/F/11360–1

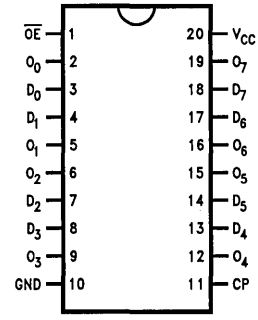
IEEE/IEC



TL/F/11360–2

Connection Diagrams

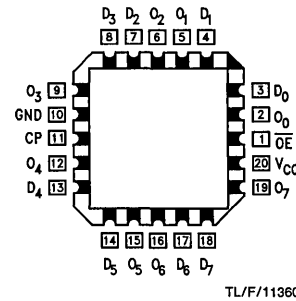
Pin Assignment for DIP, Flatpak and SOIC



TL/F/11360–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Pin Assignment for LCC



TL/F/11360–4

Functional Description

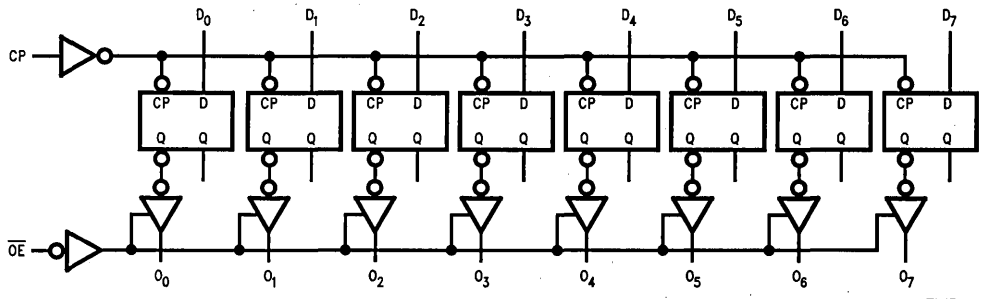
The 'LVQ374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/11360–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$	54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6			−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.5	±10.0	±50	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	75					70		MHz	
t_{PLH}, t_{PHL}	Propagation Delay CP to O_n	3.3	3.0	9.5	13.0			3.0	13.5	ns	1.2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3	3.0	9.5	13.0			3.0	13.5	ns	1.2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.5	14.5			1.0	15.0	ns	1.2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to O_n	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF		54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	0	3.0		3.0	ns	1.2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	0	1.5		1.5	ns	1.2-7
t_w	CP Pulse Width, HIGH or LOW	3.3	2.0	4.0		4.0	ns	1.2-3

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 3.3V$
C_{PD} (Note 1)	Power Dissipation Capacitance	39	pF	$V_{CC} = 3.3V$

Note 1: C_{PD} is measured at 10 MHz.

National Semiconductor

54LVQ/74LVQ573
Low Voltage Octal Latch with TRI-STATE® Outputs

General Description

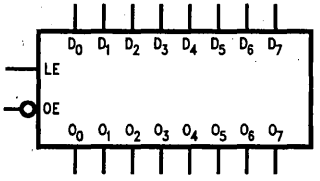
The 'LVQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The 'LVQ573 is functionally identical to the 'LVQ373 but with inputs and outputs on opposite sides of the package.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

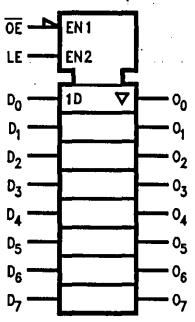
Ordering Code: See Section 8

Logic Symbols



TL/F/11361–1

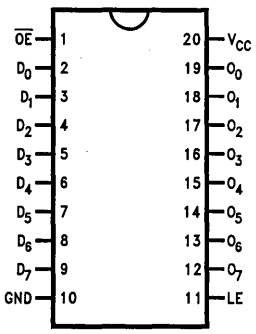
IEEE/IEC



TL/F/11361–2

Connection Diagrams

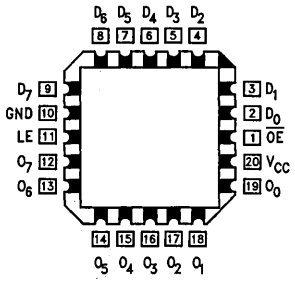
Pin Assignment for DIP, Flatpak and SOIC



TL/F/11361–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

Pin Assignment for LCC



TL/F/11361–4

Functional Description

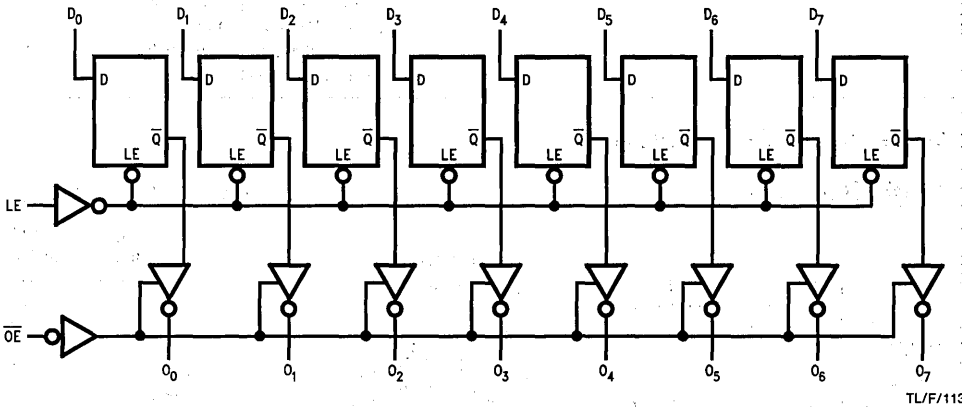
The 'LVQ573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



TL/F/11361–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'LVQ	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
54LVQ	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ T_A = +25°C		54LVQ T_A = −55°C to +125°C	74LVQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ $T_A = +25°C$		54LVQ $T_A = -55°C$ to $+125°C$	74LVQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	3.6				36	mA	$V_{OLD} = 0.8\ V_{Max}$ (Note 1)
I_{OHD}		3.6				−25	mA	$V_{OHD} = 2.0V\ V_{Min}$ (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6		5.0	100	50	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Curent	3.6		±0.5	±11.0	±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8			V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.4	−0.8			V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$, $C_L = 50$ pF			54LVQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74LVQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	3.3	2.5	8.5	10.5			2.5	11.0	ns	1.2-3, 4
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	3.3	2.5	8.5	12.0			2.5	12.5	ns	1.2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.5	13.0			2.5	13.5	ns	1.2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.0	14.5			1.0	15.0	ns	1.2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	3.3		1.0	1.5				1.5	ns	1.2-19

*Voltage Range is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL} or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 1.2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74LVQ $T_A = +25°C$ $C_L = 50$ pF		54LVQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74LVQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to LE	3.3	0	3.0		3.0	ns	1.2-7
t_H	Hold Time, HIGH or LOW D_n to LE	3.3	0	1.5		1.5	ns	1.2-7
t_W	LE Pulse Width, HIGH	3.3	2.0	4.0		4.0	ns	1.2-3

*Voltage Range 3.3 is 3.3V ±0.3V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 3.3V
C_{PD} (Note 1)	Power Dissipation Capacitance	37	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

Section 2
Interface

Section 2 Contents

National Semiconductor

PRELIMINARY

DS14C561
+3.3V-Powered 4 x 5 Driver/Receiver

General Description

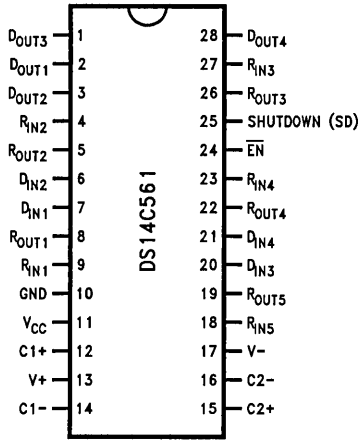
The DS14C561 is a +3.3V-powered device that conforms to the new EIA/TIA-562 standard. This standard provides a faster, lower-power alternative to EIA/TIA-232-E (RS-232) Interfaces, while guaranteeing interoperation with EIA/TIA-232-E Interfaces. The DS14C561 is guaranteed to operate with a minimum supply voltage of +3V, while maintaining the EIA/TIA-562 output signal levels ±3.7V.

The DS14C561 features an internal DC-DC converter, with four external 1.0 μF capacitors to double and invert +3.3V to ±6.6V. The device also offers a shutdown mode that reduces supply current to 10 μA, making the part ideal for use in battery-powered or power-conscious applications.

Features

- Conforms to EIA/TIA-562
- Full AC Specifications
- Internal DC-DC converter
- Operates with a single +3.3V supply
- Low power requirement I_{CC} 6 mA max
- Shutdown mode I_{CX} 10 μA max
- Operates over 64 kbps
- Receiver noise filtering
- TRI-STATE® receiver outputs
- Direct replacement of MAX561

Connection Diagram



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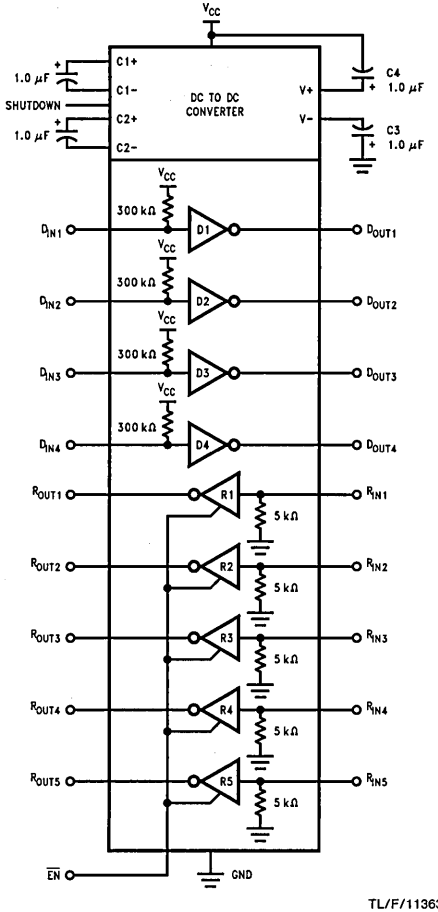
Order Number DS14C561WM
See NS Package Number M28B

Functional Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +14V
V^- Pin	+0.3V to −14V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6) Wide SOIC (WM) Package	1520 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Operating Free Air Temp. (T_A) DS14C561	0	+70	°C

Electrical Characteristics

V_{CC} = +3.3V ±0.3V, C1−C4 = 1 µF, T_A = 0°C to +70°C, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1−C4 = 1.0 µF	D_{IN} = 0.4V		6.0		V
V^-	Negative Power Supply		D_{IN} = 2.4V		−5.0		V
I_{CC}	Supply Current (V_{CC})	No Load			3.5	6.0	mA
I_{CX}	Supply Current Shutdown	R_L = 3 kΩ, SD = V_{CC}			0.1	10	µA
V_{IH}	High Level Enable Voltage		SD	2.0		V_{CC}	V
V_{IL}	Low Level Enable Voltage			GND		0.4	V
I_{IH}	High Level Enable Current			−10		+10	µA
I_{IL}	Low Level Enable Current			−10		+10	µA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage		D_{IN}	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.4	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		+10	µA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.4V$		−10		+10	µA
		V_{IN} = 0V		−10		+10	µA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		3.7	5.0	13.2	V
V_{OL}	Low Level Output Voltage	3 Drivers Loaded		−13.2	−4.0	−3.7	V
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		3.7	4.8	13.2	V
V_{OL}	Low Level Output Voltage	4 Drivers Loaded, V_{CC} = +3.3V		−13.2	−4.2	−3.7	V
I_{OS}^+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.4V		−20	−10	−2	mA
I_{OS}^-	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V		2.0	8.0	20	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V		300			Ω
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage				1.3	2.0	V
V_{TL}	Input Low Threshold Voltage			0.4	1.0		V
V_{HY}	Hysteresis			0.05	0.3		V
R_{IN}	Input Resistance	T_A = 0°C to +70°C		3.0	4.5	7.0	kΩ

Electrical Characteristics (Continued)

V_{CC} = +3.3V ±0.3V, C1–C4 = 1 μF, T_A = 0°C to +70°C, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Continued)							
I_{IN}	Input Current	V_{IN} = +25V		3.57		+8.3	mA
		V_{IN} = +3V		0.43		+1.0	mA
		V_{IN} = −3V		−1.0		−0.43	mA
		V_{IN} = −25V		−8.3		−3.57	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −200 μA		2.6	3.0		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +1.6 mA			0.2	0.4	V
V_{IH}	High Level Input Voltage		$\overline{EN}$	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.4	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.4V$		−10		+10	μA
I_{OZ}	Output Leakage Current	$\overline{EN}$ = V_{CC}, 0V ≤ R_{OUT} ≤ V_{CC}		−10		+10	μA

Switching Characteristics

V_{CC} = +3.3V ±0.3V, C1–C4 = 1 μF, T_A = 0°C to +70°C, unless otherwise specified (Note 4)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS								
t_{PLH}	Propagation Delay LOW to HIGH		R_L = 3 kΩ			1.0	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		C_L = 50 pF			0.8	4.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$		(*Figures 1* and *2*)			0.2	1.0	μs
SR1	Output Slew Rate		R_L = 3 kΩ to 7 kΩ, C_L = 50 pF				30	V/μs
SR2	Output Slew Rate		R_L = 3 kΩ, C_L = 2500 pF, f = 10 kHz				30	V/μs
t_r, t_f	Output Rise, Fall Time (Note 7)	V_{CC} = 3.3V	R_L = 3 kΩ, C_L = 2500 pF, f = 10 kHz		0.2	2.7	3.1	μs
			R_L = 3 kΩ, C_L = 1000 pF, f = 32 kHz		0.2	1.7	2.1	μs
RECEIVER CHARACTERISTICS								
t_{PLH}	Propagation Delay LOW to HIGH		Input Pulse Width > 10 μs			3.7	9.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		C_L = 150 pF			4.7	9.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$		(*Figures 3* and *4*)			1.0	3.0	μs
t_{PLZ}			(*Figures 5* and *7*)			0.2		μs
t_{PZL}						1.2		μs
t_{PHZ}			(*Figures 5* and *6*)			0.4		μs
t_{PZH}						1.2		μs
t_{NW}	Noise Pulse Width Rejected		(*Figures 3* and *4*)			4.0	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: I_{OS}^+ and I_{OS}^- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: t_r = t_f = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 32 kHz (64 kbit/sec). Driver AC input waveform for test purposes: t_r = t_f = ≤ 10 ns, V_{IH} = 3V, V_{IL} = 0V, f = 32 kHz (64 kbit/sec).

Note 5: All typicals are given for V_{CC} = 3.3V and T_A = +25°C.

Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: WM package 14.3 mW/°C..

Note 7: Rise and Fall Times (t_r, t_f) are measured between the ±3.3V levels on the driver output. One output switching.

Parameter Measurement Information

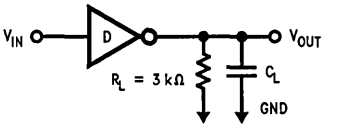

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FIGURE 1. Driver Load Circuit

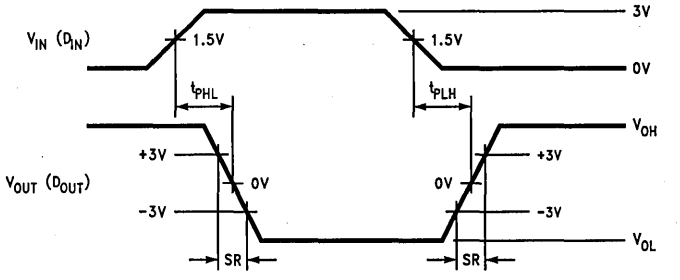

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FIGURE 2. Driver Switching Waveform

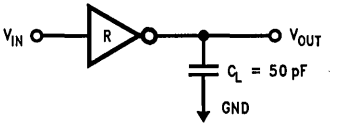

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FIGURE 3. Receiver Load Circuit

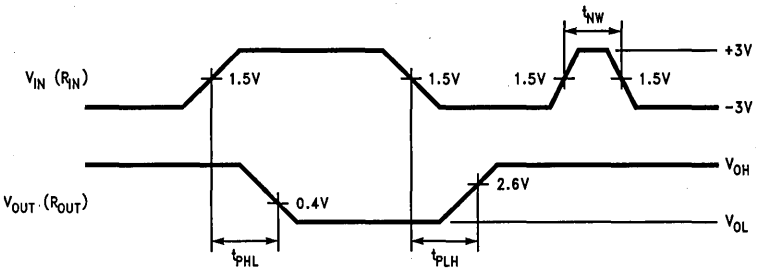

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FIGURE 4. Receiver Propagation Delays and Noise Rejection

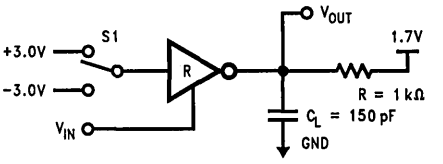

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FIGURE 5. Receiver Disable Load Circuit

Parameter Measurement Information (Continued)

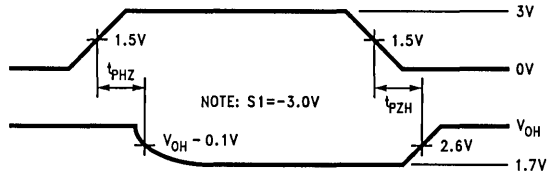

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FIGURE 6. Receiver TRI-STATE® Delay Timing (t_{PHZ}, t_{PZH})

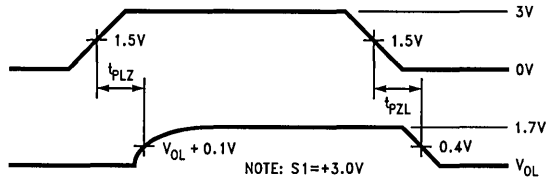

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FIGURE 7. Receiver TRI-STATE® Delay Timing (t_{PLZ}, t_{PZL})

Pin Descriptions

V_{CC} (pin 11)—Power supply pin for the device, +3.3V ±0.3V.

V^+ (pin 13)—Positive supply for drivers. Recommended external capacitor: C4 = 1 μF. This supply is not intended to be loaded externally.

V^- (pin 17)—Negative supply for drivers. Recommended external capacitor: C3 = 1 μF. This supply is not intended to be loaded externally.

C1+, C1− (pins 12 and 14)—External capacitor connection pins. Recommended capacitor: 1μF.

C2+, C2− (pins 15 and 16)—External capacitor connection pins. Recommended capacitor: 1 μF.

$\overline{EN}$ (pin 24)—Controls the Receiver output TRI-STATE® Circuit. A HIGH level on this pin will disable the Receiver Output.

SHUTDOWN (SD) (pin 25)—A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 10 μA. Providing a low power state.

D_{IN} 1–4 (pins 7, 6, 20 and 21)—Inputs of unused drivers may be left open, an internal pull-up resistor pulls input to V_{CC}. Output will be LOW for open inputs. (300 kΩ minimum, typically 3.3 MΩ)

D_{OUT} 1–4 (pins 2, 3, 1 and 28)—Driver output pins conform to EIA/TIA-562 levels.

R_{IN} 1–5 (pins 9, 4, 27, 23 and 18)—Receiver input pins accept EIA/TIA-562 input voltages (±25V). Receivers feature a noise filter and guaranteed hysteresis of 100 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT}1–5 (pins 8, 5, 26, 22 and 19)—Receiver output pins generate a maximum V_{OL} of 0.4V given an I_O of 1.6 mA and a minimum V_{OH} of 2.6V given an I_O of −200 μA.

GND (pin 10)—Ground pin.

Section 3

Real Time Clocks, Clock Generation and Support (CGS)

Section 3 Contents

National Semiconductor

PRELIMINARY

LV8570A Low Voltage Timer Clock Peripheral (TCP)

General Description

The LV8570A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports. The address space is organized as 2 software selectable pages of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, the Timers and their data RAM, and the Time Save RAM. Any of the RAM locations that are not being used for their intended purpose may be used as general purpose CMOS RAM.

Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week, day of month and day of year counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the crystal and two capacitors. The choice of crystal frequency is program selectable.

Two independent multifunction 10 MHz 16-bit timers are provided. These timers operate in four modes. Each has its own prescaler and can select any of 8 possible clock inputs. Thus, by programming the input clocks and the timer counter values a very wide range of timing durations can be achieved. The range is from about 400 ns (4.915 MHz oscillator) to 65,535 seconds (18 hrs., 12 min.).

Power failure logic and control functions have been integrated on chip. This logic is used by the TCP to issue a power fail interrupt, and lock out the μp interface. The time power fails may be logged into RAM automatically when $V_{BB} > V_{CC}$. Additionally, two supply pins are provided. When $V_{BB} > V_{CC}$, internal circuitry will automatically switch from the main supply to the battery supply. Status bits are provided to indicate initial application of battery power, system power, and low battery detect. (Continued)

Features

- 3.3V ±5% Supply
- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week and day of years counters
  - Four selectable oscillator frequencies
  - Parallel Resonant Oscillator
- Two 16-bit timers
  - 10 MHz external clock frequency
  - Programmable multi-function output
  - Flexible re-trigger facilities
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, timer and power fail interrupts
- Up to 44 bytes of CMOS RAM
- INTR/MFO pins programmable High/Low and push-pull or open drain

Block Diagram

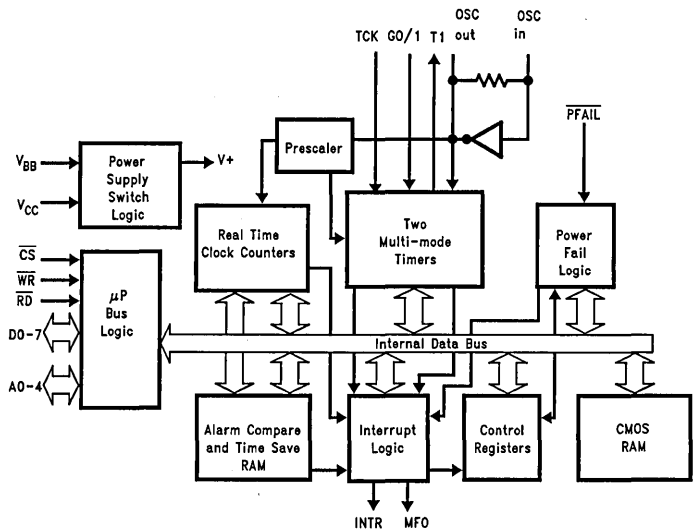

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FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (PD)	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C

Operation Conditions

	Min	Max	Unit
Supply Voltage (V_{CC}) (Note 3)	3.2	3.6	V
Supply Voltage (V_{BB}) (Note 3)	2.2	V_{CC}−0.4	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0.0	V_{CC}	V
Operation Temperature (T_A)	−40	+85	°C
Electr-Static Discharge Rating TBD		1	kV

Typical Values

θ_{JA} DIP: Board = 45°C/W, Socket = 50°C/W

θ_{JA} PLCC: Board = 77°C/W, Socket = 85°C/W

DC Electrical Characteristics

V_{CC} = 3.3V ±5%, V_{BB} = TBD, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage (Note 4)	Any Inputs Except OSC IN, OSC IN with External Clock	2.0 V_{BB} − 0.1	V_{CC} + 0.3	V V
V_{IL}	Low Level Input Voltage	All Inputs Except OSC IN OSC IN with External Clock	−0.3 −0.3	 0.1	V V
V_{OH}	High Level Output Voltage (Excluding OSC OUT)	I_{OUT} = −100 μA I_{OUT} = −2 mA	V_{CC} − 0.2 2.4		V V
V_{OL}	Low Level Output Voltage (Excluding OSC OUT)	I_{OUT} = 100 μA I_{OUT} = 2 mA		0.2 0.3	V V
I_{IN}	Input Current (Except OSC IN)	V_{IN} = V_{CC} or GND		±1.0	μA
I_{OZ}	Output TRI-STATE® Current	V_{OUT} = V_{CC} or GND			μA
I_{LKG}	Output High Leakage Current T1, MFO, INTR Pins	V_{OUT} = V_{CC} or GND Outputs Open Drain			μA
I_{CC}	Quiescent Supply Current (Note 7)	F_{OSC} = 32.768 kHz V_{IN} = V_{CC} or GND (Note 5) V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)			 μA mA mA
		F_{OSC} = 4.194304 MHz or 4.9152 MHz V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)			 mA mA
I_{CC}	Quiescent Supply Current (Single Supply Mode) (Note 7)	V_{BB} = GND V_{IN} = V_{CC} or GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz			 μA mA
I_{BB}	Standby Mode Battery Supply Current (Note 8)	V_{CC} = GND OSC OUT = Open Circuit, Other Pins = GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz			 μA μA
I_{BLK}	Battery Supply Leakage	2.2V ≤ V_{BB} ≤ Other Pins at GND V_{CC} = GND, V_{BB} = V_{CC} = V_{BB} = 2.2V			 μA μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: For F_{OSC} = 4.194304 or 4.9152 MHz, V_{BB} minimum = 2.8V. In battery backed mode, $V_{BB} \leq V_{CC}$ −0.4V.
Single Supply Mode: Data retention voltage is 2.2V min.
In single Supply Mode (Power connected to V_{CC} pin) 3.2V ≤ V_{CC} ≤ 3.6V.

Note 4: This parameter (V_{IH}) is not tested on all pins at the same time.

Note 5: This specification tests I_{CC} with all power fail circuitry disabled, by setting D7 of Interrupt Control Register 1 to 0.

Note 6: This specification tests I_{CC} with all power fail circuitry enabled, by setting D7 of Interrupt Control Register 1 to 1.

Note 7: This specification is tested with both the timers and OSC IN driven by a signal generator. Contents of the Test Register = 00(H), the MFO pin is not configured as buffered oscillator out and MFO, T1, INTR, are configured as open drain.

Note 8: This specification is tested with both the timers off, and only OSC IN is driven by a signal generator. Contents of the Test Register = 00(H) and the MFO pin is not configured as buffered oscillator out.

AC Electrical Characteristics

V_{CC} = 3.3V ±5%, V_{BB} = TBD, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Min	Max	Units
READ TIMING				
t_{AR}	Address Valid Prior to Read Strobe			ns
t_{RW}	Read Strobe Width (Note 9)			ns
t_{CD}	Chip Select to Data Valid Time			ns
t_{RAH}	Address Hold after Read (Note 10)			ns
t_{RD}	Read Strobe to Valid Data			ns
t_{DZ}	Read or Chip Select to TRI-STATE			ns
t_{RCH}	Chip Select Hold after Read Strobe			ns
t_{DS}	Minimum Inactive Time between Read or Write Accesses			ns
WRITE TIMING				
t_{AW}	Address Valid before Write Strobe			ns
t_{WAH}	Address Hold after Write Strobe (Note 10)			ns
t_{CW}	Chip Select to End of Write Strobe			ns
t_{WW}	Write Strobe Width (Note 11)			ns
t_{DW}	Data Valid to End of Write Strobe			ns
t_{WDH}	Data Hold after Write Strobe (Note 10)			ns
t_{WCH}	Chip Select Hold after Write Strobe			ns
TIMER 0/TIMER 1 TIMING				
F_{TCK}	Input Frequency Range	DC		MHz
t_{CK}	Propagation Delay Clock to Output ⎍			ns
t_{GO}	Propagation Delay G0 to G1 to Timer Output (Note 12) ⎍			ns
t_{PGW}	Pulse Width G0 or G1 ⎍ (Note 12)			ns
t_{GS}	Setup Time, G0, G1 to TCK (Note 13)			ns
INTERRUPT TIMING				
t_{ROLL}	Clock Rollover to INTR Out is Typically			

Note 9: Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

Note 10: Hold time is guaranteed by design but not production tested. This limit is not used to calculate outgoing quality levels.

Note 11: Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

Note 12: Timers in Mode 3.

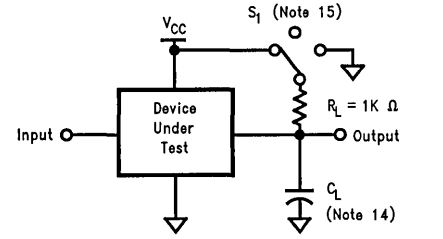
Note 13: Guaranteed by design, not production tested. This limit is not used to calculate outgoing quality levels.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns (10%–90%)
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels (Note 15)	Active High + Active Low −

Note 14: C_L = 100 pF, includes jig and scope capacitance.

Note 15: S1 = V_{CC} for active low to high impedance measurements.
S1 = GND for active high to high impedance measurements.
S1 = open for all other timing measurements.



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Capacitance (T_A = 25°C, f = 1 MHz)

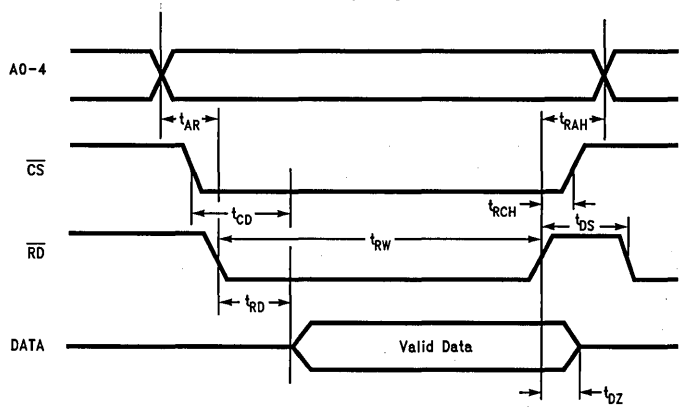
Symbol	Parameter (Note 16)	Typ	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	7	pF

Note 16: This parameter is not 100% tested.

Note 17: Output rise and fall times 25 ns max (10%–90%) with 100 pF load.

Timing Waveforms

Read Timing Diagram



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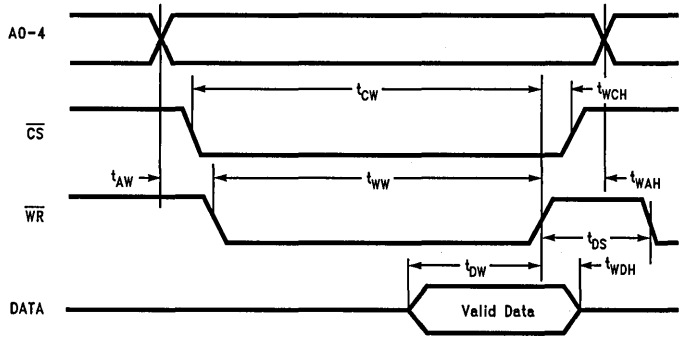
Write Timing Diagram



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General Description (Continued)

The LV8570A's interrupt structure provides four basic types of interrupts: Periodic, Alarm/Compare, Timer, and Power Fail. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

One dedicated general purpose interrupt output is provided. A second interrupt output is available on the Multiple Function Output (MFO) pin. Each of these may be selected to generate an interrupt from any source. Additionally, the MFO pin may be programmed to be either as oscillator output or Timer 0's output.

Pin Description

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (Inputs): These pins interface to μP control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and Write pins are also active low and enable reading or writing to the TCP. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.

A0–A4 (Inputs): These 5 pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.

OSC IN (Input): OSC OUT (Output): These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}, and the correct crystal select bits in the Real Time Mode Register have been set.

MFO (Output): The multi-function output can be used as a second interrupt output for interrupting the μP. This pin can also provide an output for the oscillator or the internal Timer 0. The MFO output can be programmed active high or low, open drain or push-pull. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}. This pin is configured open drain during battery operation ($V_{BB} > V_{CC}$).

INTR (Output): The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The INTR output can be programmed active high or low, push-pull or open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}. This pin is configured open drain during battery operation ($V_{BB} > V_{CC}$).

D0–D7 (Input/Output): These 8 bidirectional pins connect to the host μP's data bus and are used to read from and write to the TCP. When the $\overline{PFAIL}$ pin goes low and a write is not in progress, these pins are at TRI-STATE.

$\overline{PFAIL}$ (Input): In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the TCP goes into a lockout mode, in a minimum of 30 μs or a maximum of 63 μs unless lockout delay is programmed. In the single power supply mode, this pin is not useable as an input and should be tied to V_{CC}. Refer to section on Power Fail Functional Description.

V_{BB} (Battery Power Pin): This pin is connected to a back-up power supply. This power supply is switched to the internal circuitry when the V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the TCP programmed for single power supply only, and power applied to the V_{CC} pin.

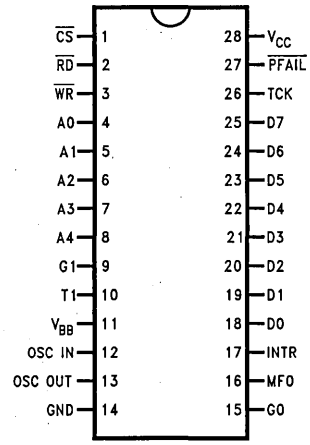
TCK, G1, G0, (Inputs), T1 (Output): TCK is the clock input to both timers when they have an external clock selected. In modes 0, 1, and 2, G0 and G1 are active low enable inputs for timers 0 and 1 respectively. In mode 3, G0 and G1 are positive edge triggers to the timers. T1 is dedicated to the timer 1 output. The T1 output can be programmed active high or low, push-pull or open drain. Timer 0 output is available through MFO pin if desired. If in battery backed mode and a pull-up resistor is attached to T1, it should be connected to a voltage no greater than V_{BB}. The T1 pin is configured open drain during battery operation ($V_{BB} > V_{CC}$).

V_{CC}: This is the main system power pin.

GND: This is the common ground power pin for both V_{BB} and V_{CC}.

Connection Diagrams

Dual-In-Line



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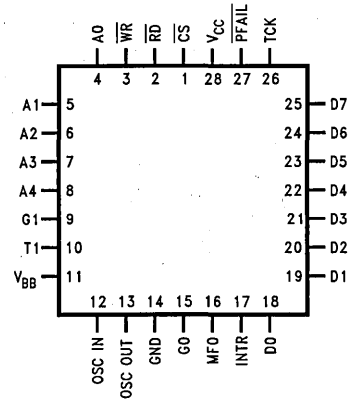
Top View

Order Number LV8570AN
See NS Package Number N28B

Plastic Chip Carrier



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Top View

Order Number LV8570AV
See NS Package Number V28A

Functional Description

The LV8570A contains a fast access real time clock, two 10 MHz 16-bit timers, interrupt control logic, power fail detect logic, and CMOS RAM. All functions of the TCP are controlled by a set of nine registers. A simplified block diagram that shows the major functional blocks is given in *Figure 1.*

The blocks are described in the following sections:

1. Real Time Clock
2. Oscillator Prescaler
3. Interrupt Logic
4. Power Failure Logic
5. Additional Supply Management
6. Timers

The memory map of the TCP is shown in the memory addressing table. The memory map consists of two 31 byte pages with a main status register that is common to both pages. A control bit in the Main Status Register is used to select either page. *Figure 2* shows the basic concept. Page 0 contains all the clock timer functions, while page 1 has scratch pad RAM. The control registers are split into two separate blocks to allow page 1 to be used entirely as scratch pad RAM. Again a control bit in the Main Status Register is used to select either control register block.

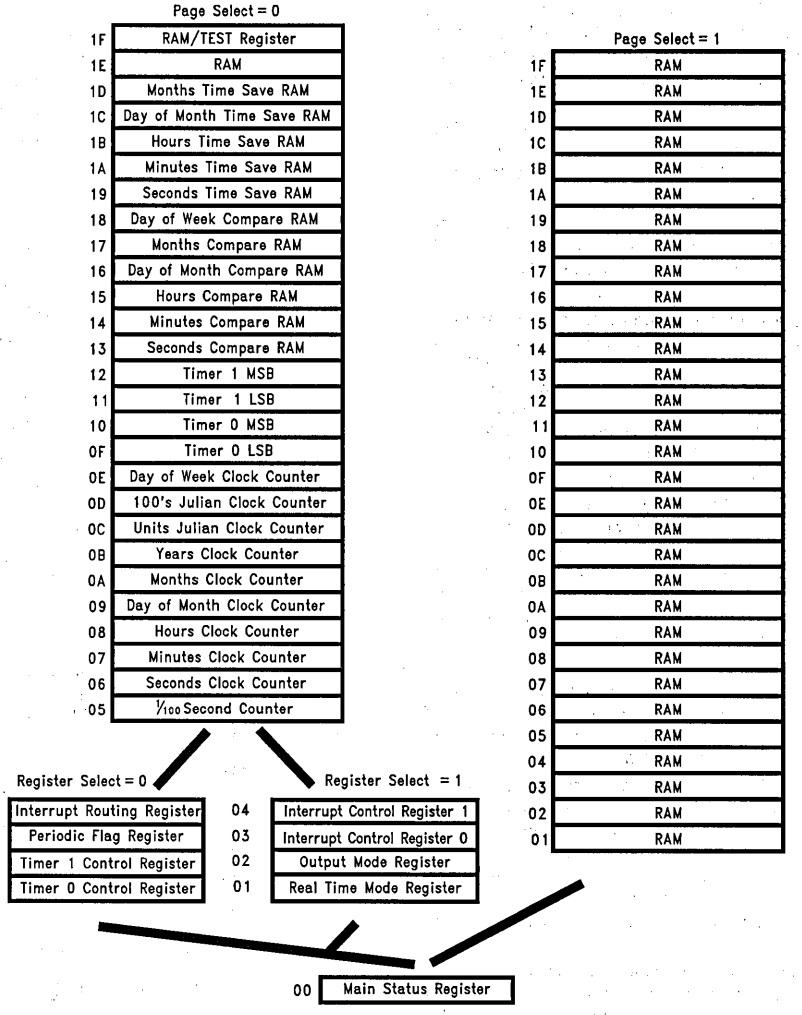

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FIGURE 2. LV8570A Internal Memory Map

Functional Description (Continued)

INITIAL POWER-ON of BOTH V_{BB} and V_{CC}

V_{BB} and V_{CC} may be applied in any sequence. In order for the power fail circuitry to function correctly, whenever power is off, the V_{CC} pin must see a path to ground through a maximum of 1 MΩ. The user should be aware that the control registers will contain random data. The first task to be carried out in an initialization routine is to start the oscillator by writing to the crystal select bits in the Real Time Mode Register. If the LV8570A is configured for single supply mode, an extra 50 μA may be consumed until the crystal select bits are programmed. The user should also ensure that the TCP is not in test mode (see register descriptions).

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

As shown in *Figure 2*, the clock has 10 bytes of counters, which count from 1/100 of a second to years. Each counter counts in BCD and is synchronously clocked. The count sequence of the individual byte counters within the clock is shown later in Table VII. Note that the day of week, day of month, day of year, and month counters all roll over to 1. The hours counter in 12 hour mode rolls over to 1 and the AM/PM bit toggles when the hours rolls over to 12 (AM = 0, PM = 1). The AM/PM bit is bit D7 in the hours counter.

All other counters roll over to 0. Also note that the day of year counter is 12 bits long and occupies two addresses. Upon initial application of power the counters will contain random information.

READING THE CLOCK: VALIDATED READ

Since clocking of the counter occurs asynchronously to reading of the counter, it is possible to read the counter while it is being incremented (rollover). This may result in an incorrect time reading. Thus to ensure a correct reading of the entire contents of the clock (or that part of interest), it must be read without a clock rollover occurring. In general this can be done by checking a rollover bit. On this chip the periodic interrupt status bits can serve this function. The following program steps can be used to accomplish this.

1. Initialize program for reading clock.
2. Dummy read of periodic status bit to clear it.
3. Read counter bytes and store.
4. Read rollover bit, and test it.
5. If rollover occured go to 3.
6. If no rollover, done.

To detect the rollover, individual periodic status bits can be polled. The periodic bit chosen should be equal to the highest frequency counter register to be read. That is if only SECONDS through HOURS counters are read, then the SECONDS periodic bit should be used.

READING THE CLOCK: INTERRUPT DRIVEN

Enabling the periodic interrupt mask bits cause interrupts just as the clock rolls over. Enabling the desired update rate and providing an interrupt service routine that executes in less than 10 ms enables clock reading without checking for a rollover.

READING THE CLOCK: LATCHED READ

Another method to read the clock that does not require checking the rollover bit is to write a one into the Time Save Enable bit (D7) of the Interrupt Routing Register, and then to write a zero. Writing a one into this bit will enable the clock contents to be duplicated in the Time Save RAM. Changing the bit from a one to a zero will freeze and store the contents of the clock in Time Save RAM. The time then can be read without concern for clock rollover, since internal logic takes care of synchronization of the clock. Because only the bits used by the clock counters will be latched, the Time Save RAM should be cleared prior to use to ensure that random data stored in the unused bits do not confuse the host microprocessor. This bit can also provide time save at power failure, see the Additional Supply Management Functions section. With the Time Save Enable bit at a logical 0, the Time Save RAM may be used as RAM if the latched read function is not necessary.

INITIALIZING AND WRITING TO THE CALENDAR-CLOCK

Upon initial application of power to the TCP or when making time corrections, the time must be written into the clock. To correctly write the time to the counters, the clock would normally be stopped by writing the Start/$\overline{\text{Stop}}$ bit in the Real Time Mode Register to a zero. This stops the clock from counting and disables the carry circuitry. When initializing the clock's Real Time Mode Register, it is recommended that first the various mode bits be written while maintaining the Start/$\overline{\text{Stop}}$ bit reset, and then writing to the register a second time with the Start/$\overline{\text{Stop}}$ bit set.

The above method is useful when the entire clock is being corrected. If one location is being updated the clock need not be stopped since this will reset the prescaler, and time will be lost. An ideal example of this is correcting the hours for daylight savings time. To write to the clock "on the fly" the best method is to wait for the 1/100 of a second periodic interrupt. Then wait an additional 16 μs, and then write the data to the clock.

PRESCALER/OSCILLATOR FUNCTIONAL DESCRIPTION

Feeding the counter chain is a programmable prescaler which divides the crystal oscillator frequency to 32 kHz and further to 100 Hz for the counter chain (see *Figure 3*). The crystal frequency that can be selected are: 32 kHz, 32.768 kHz, 4.9152 MHz, and 4.194304 MHz.

Once 32 kHz is generated it feeds both timers and the clock. The clock and timer prescalers can be independently enabled by controlling the timer or clock Start/$\overline{\text{Stop}}$ bits.

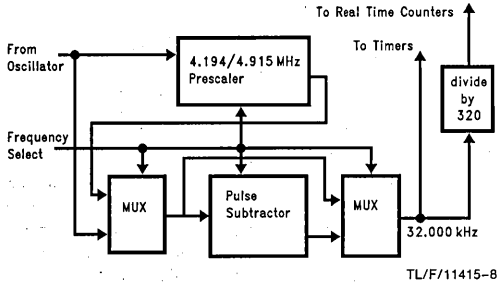

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FIGURE 3. Programmable Clock Prescaler Block

Functional Description (Continued)

The oscillator is programmed via the Real Time Mode Register to operate at various frequencies. The crystal oscillator is designed to offer optimum performance at each frequency. Thus, at 32.768 kHz the oscillator is configured as a low frequency and low power oscillator. At the higher frequencies the oscillator inverter is reconfigured. In addition to the inverter, the oscillator feedback bias resistor is included on chip, as shown in *Figure 4*. The oscillator input may be driven from an external source if desired. Refer to test mode application note for details. The oscillator stability is enhanced through the use of an on chip regulated power supply.

The typical range of trimmer capacitor (as shown in Oscillator Circuit Diagram *Figure 4*, and in the typical application) at the oscillator input pin is suggested only to allow accurate tuning of the oscillator. This range is based on a typical printed circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases, the **load capacitance** specified by the crystal manufacturer (nominal value 11 pF for the 32.768 crystal) is what determines proper oscillation. This load capcitance is the series combination of capacitance on each side of the crystal (with respect to ground).

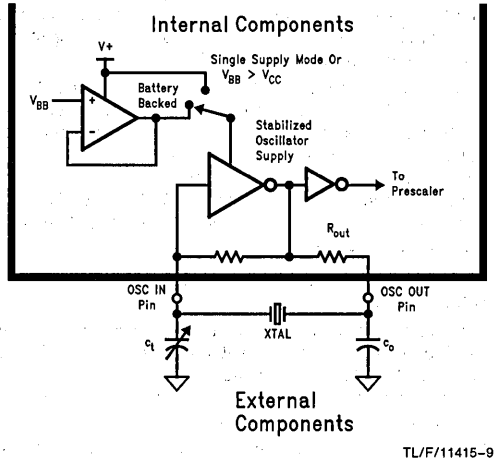

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FIGURE 4. Oscillator Circuit Diagram

XTAL	C_o	C_t	R_{OUT} (Switched Internally)
32/32.768 kHz	47 pF	2 pF–22 pF	150 kΩ to 350 kΩ
4.194304 MHz	68 pF	0 pF–80 pF	500Ω to 900Ω
4.9152 MHz	68 pF	29 pF–49 pF	500Ω to 900Ω

INTERRUPT LOGIC FUNCTIONAL DESCRIPTION

The TCP has the ability to coordinate processor timing activities. To enhance this, an interrupt structure has been implemented which enables several types of events to cause interrupts. Interrupts are controlled via two Control Registers in block 1 and two Status Registers in block 0. (See Register Description for notes on paging and also *Figure 5* and Table I.)

The interrupts are enabled by writing a one to the appropriate bits in Interrupt Control Register 0 and/or 1. Any of the interrupts can be routed to either the INTR pin or the MFO pin, depending on how the Interrupt Routing register is programmed. This, for example, enables the user to dedicate the MFO as a non-maskable interrupt pin to the CPU for power failure detection and enable all other interrupts to appear on the INTR pin. The polarity for the active interrupt can be programmed in the Output Mode Register for either active high or low, and open drain or push pull outputs.

TABLE I. Registers that are Applicable to Interrupt Control

Register Name	Register Select	Page Select	Address
Main Status Register	X	X	00H
Periodic Flag Register	0	0	03H
Interrupt Routing Register	0	0	04H
Interrupt Control Register 0	1	0	03H
Interrupt Control Register 1	1	0	04H
Output Mode Register	1	0	02H

The Interrupt Status Flag D0, in the Main Status Register, indicates the state of INTR and MFO outputs. It is set when either output becomes active and is cleared when all TCP interrupts have been cleared and no further interrupts are pending (i.e., both INTR and MFO are returned to their inactive state). This flag enables the TCP to be rapidly polled by the μP to determine the source of an interrupt in a wired—OR interrupt system.

Note that the Interrupt Status Flag will only monitor the state of the MFO output if it has been configured as an interrupt output (see Output Mode Register description). This is true, regardless of the state of the Interrupt Routing Register. Thus the Interrupt Status Flag provides a true reflection of all conditions routed to the external pins.

Status for the interrupts are provided by the Main Status Register and the Periodic Flag Register. Bits D1–D5 of the Main Status Register are the main interrupt bits.

These register bits will be set when their associated timing events occur. Enabled Alarm or Timer interrupts that occur will set its Main Status Register bit to a one. However, an external interrupt will only be generated if the appropriate Alarm or Timer interrupt enable bits are set (see *Figure 5*).

Disabling the periodic bits will mask the Main Status Register periodic bit, but not the Periodic Flag Register bits. The Power Fail Interrupt bit is set when the interrupt is enabled and a power fail event has occurred, and is not reset until the power is restored. If all interrupt enable bits are 0 no interrupt will be asserted. However, status still can be read from the Main Status Register in a polled fashion (see *Figure 5*).

To clear a flag in bits D2–D5 of the Main Status Register a 1 must be written back into the bit location that is to be cleared. For the Periodic Flag Register reading the status will reset all the periodic flags.

Functional Description (Continued)

Interrupts Fall Into Four Categories:

1. The Timer Interrupts: For description see Timer Section.
2. The Alarm Compare Interrupt: Issued when the value in the time compared RAM equals the counter.
3. The Periodic Interrupts: These are issued at every increment of the specific clock counter signal. Thus, an interrupt is issued every minute, second, etc. Each of these interrupts occurs at the roll-over of the specific counter.
4. The Power Fail Interrupt: Issued upon recognition of a power fail condition by the internal sensing logic. The power failed condition is determined by the signal on the $\overline{\text{PFAIL}}$ pin. The internal power fail signal is gated with the chip select signal to ensure that the power fail interrupt does not lock the chip out during a read or write.

ALARM COMPARE INTERRUPT DESCRIPTON

The alarm/time comparison interrupt is a special interrupt similar to an alarm clock wake up buzzer. This interrupt is generated when the clock time is equal to a value programmed into the alarm compare registers. Up to six bytes can be enabled to perform alarm time comparisons on the counter chain. These six bytes, or some subset thereof, would be loaded with the future time at which the interrupt will occur. Next, the appropriate bits in the Interrupt Control Register 1 are enabled or disabled (refer to detailed description of Interrupt Control Register 1). The TCP then compares these bytes with the clock time. When all the enabled compare registers equal the clock time an alarm interrupt is issued, but only if the alarm compare interrupt is enabled can the interrupt be generated externally. Each alarm compare bit in the Control Register will enable a specific byte for comparison to the clock. Disabling a compare byte is the same as setting its associated counter comparator to an "always equal" state. For example, to generate an interrupt at 3:15 AM of every day, load the hours compare with 0 3 (BCD), the minutes compare with 1 5 (BCD) and the faster counters with 0 0 (BCD), and then disable all other compare registers. So every day when the time rolls over from 3:14:59.99, an interrupt is issued. This bit may be reset by writing a one to bit D3 in the Main Status Register at any time after the alarm has been generated.

If time comparison for an individual byte counter is disabled, that corresponding RAM location can then be used as general purpose storage.

PERIODIC INTERRUPTS DESCRIPTION

The Periodic Flag Register contains six flags which are set by real-time generated "ticks" at various time intervals, see *Figure 5*. These flags constantly sense the periodic signals and may be used whether or not interrupts are enabled. These flags are cleared by any read or write operation performed on this register.

To generate periodic interrupts at the desired rate, the associated Periodic Interrupt Enable bit in Interrupt Control Register 0 must be set. Any combination of periodic interrupts may be enabled to operate simultaneously. Enabled periodic interrupts will now affect the Periodic Interrupt Flag in the Main Status Register. The Periodic Route bit in the Interrupt Routing Register is used to route the periodic interrupt events to either the INTR output or the MFO output.

When a periodic event occurs, the Periodic Interrupt Flag in the Main Status Register is set, causing an interrupt to be generated. The μP clears both flag and interrupt by writing a "1" to the Periodic Interrupt Flag. The individual flags in the periodic Interrupt Flag Register do not require clearing to cancel the interrupt.

If all periodic interrupts are disabled and a periodic interrupt is left pending (i.e., the Periodic Interrupt Flag is still set), the Periodic Interrupt Flag will still be required to be cleared to cancel the pending interrupt.

POWER FAIL INTERRUPTS DESCRIPTION

The Power Fail Status Flag in the Main Status Register monitors the state of the internal power fail signal. This flag may be interrogated by the μP, but it cannot be cleared; it is cleared automatically by the TCP when system power is restored. To generate an interrupt when the power fails, the Power Fail Interrupt Enable bit in Interrupt Control Register 1 is set.

The Power Fail Route bit determines which output the interrupt will appear on. Although this interrupt may not be cleared, it may be masked by clearing the Power Fail Interrupt Enable bit.

POWER FAILURE CIRCUITRY FUNCTIONAL DESCRIPTION

Since the clock must be operated from a battery when the main system supply has been turned off, the LV8570A provides circuitry to simplify design in battery backed systems. This circuitry switches over to the back up supply, and isolates the LV8570A from the host system. *Figure 6* shows a simplified block diagram of this circuitry, which consists of three major sections; 1) power loss logic: 2) battery switch over logic: and 3) isolation logic.

Detection of power loss occurs when $\overline{\text{PFAIL}}$ is low. Debounce logic provides a 30 μs–63 μs debounce time, which will prevent noise on the $\overline{\text{PFAIL}}$ pin from being interpreted as a system failure. After 30 μs–63 μs the debounce logic times out and a signal is generated indicating that system power is marginal and is failing. The Power Fail Interrupt will then be generated.

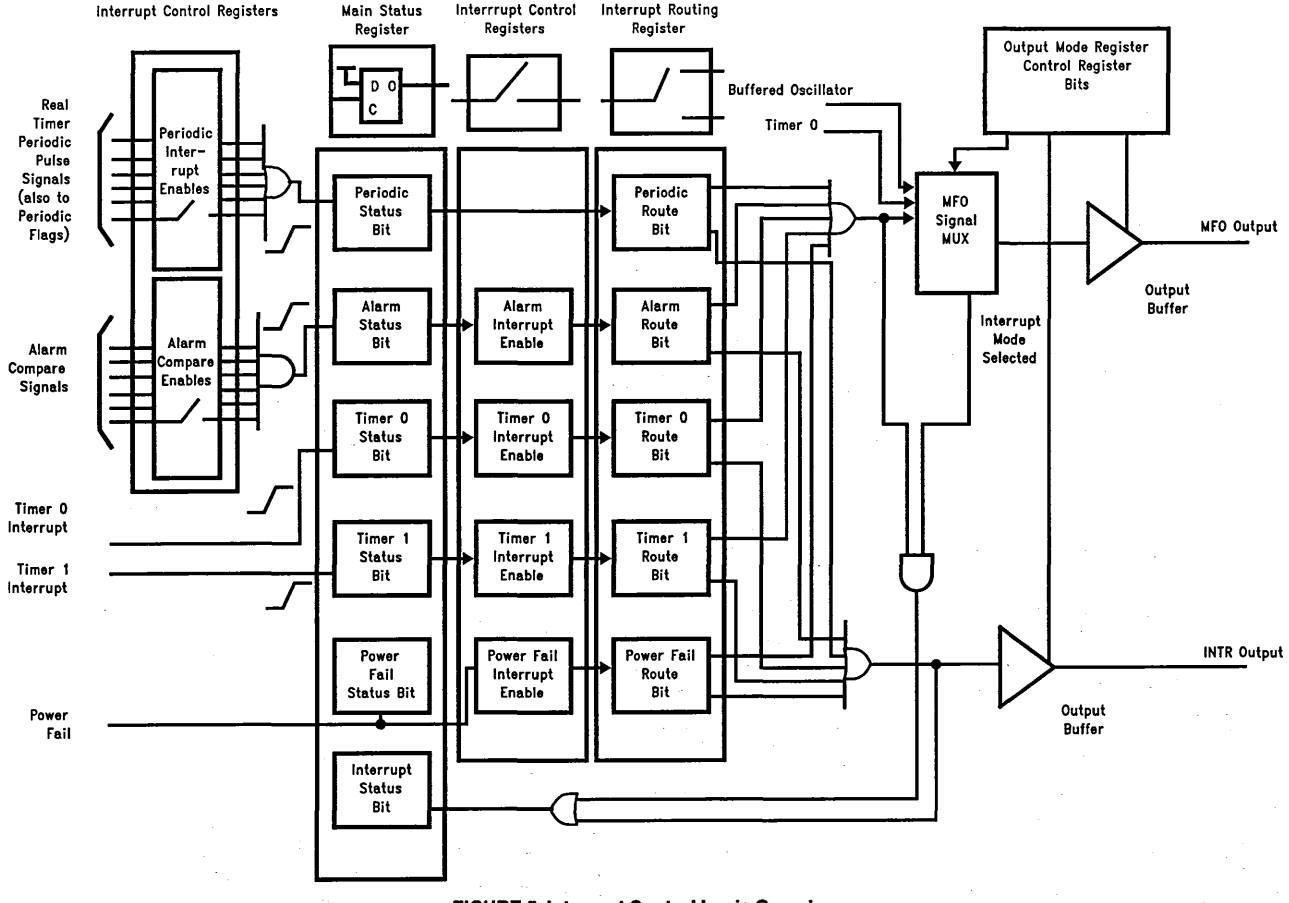

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FIGURE 5. Interrupt Control Logic Overview

Functional Description (Continued)

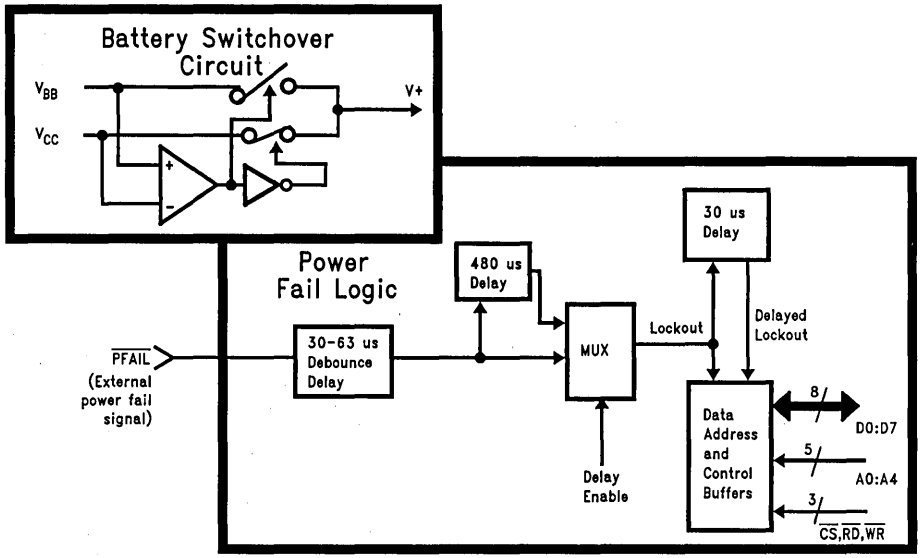

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FIGURE 6. System-Battery Switchover (Upper Left), Power Fail and Lock-Out Circuits (Lower Right)

The user may choose to have this power failed signal lock-out the TCP's data bus within 30 μs min/63 μs max or to delay the lock-out to enable μP access after power failure is detected. This delay is enabled by setting the delay enable bit in the Routing Register. Also, if the lock-out delay was not enabled the TCP will disconnect itself from the bus within 30 μs min → 63 μs max. If chip select is low when a power failure is detected, a safety circuit will ensure that if a read or write is held active continuously for greater than 30 μs after the power fail signal is asserted, the lock-out will be forced. If a lock-out delay is enabled, the LV8570A will remain active for 480 μs after power fail is detected. This will enable the μP to perform last minute bookkeeping before total system collapse. When the host CPU is finished accessing the TCP it may force the bus lock-out before 480 μs has elapsed by resetting the delay enable bit.

The battery switch over circuitry is completely independent of the $\overline{\text{PFAIL}}$ pin. A separate circuit compares V_{CC} to the V_{BB} voltage. As the main supply fails, the TCP will continue to operate from the V_{CC} pin until V_{CC} falls below the V_{BB} voltage. At this time, the battery supply is switched in, V_{CC} is disconnected, and the device is now in the standby mode. If indeterminate operation of the battery switch over circuit is to be avoided, then the voltage at the V_{CC} pin must not be allowed to equal the voltage at the V_{BB} pin.

After the generation of a lock-out signal, and eventual switch in of the battery supply, the pins of the TCP will be configured as shown in Table II. Outputs that have a pull-up resistor should be connected to a voltage no greater than V_{BB}.

TABLE II. Pin Isolation during a Power Failure

Pin	$\overline{\text{PFAIL}}$ = Logic 0	Standby Mode $V_{BB} > V_{CC}$
$\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$	Locked Out	Locked Out
A0–A4	Locked Out	Locked Out
D0–D7	Locked Out	Locked Out
Oscillator	Not Isolated	Not Isolated
TCK, G0, G1	Not Isolated	Locked Out
$\overline{\text{PFAIL}}$	Not Isolated	Not Isolated
INTR, MFO T1	Not Isolated	Open Drain

The Timer and Interrupt Power Fail Operation bits in the Real-Time Mode Register determine whether or not the timers and interrupts will continue to function after a power fail event.

As power returns to the system, the battery switch over circuit will switch back to V_{CC} power as soon as it becomes greater than the battery voltage. The chip will remain in the locked out state as long as $\overline{\text{PFAIL}}$ = 0. When $\overline{\text{PFAIL}}$ = 1

Functional Description (Continued)

the chip is unlocked, but only after another 30 μs min → 63 μs max debounce time. The system designer must ensure that his system is stable when power has returned.

The power fail circuitry contains active linear circuitry that draws supply current from V_{CC}. In some cases this may be undesirable, so this circuit can be disabled by masking the power fail interrupt. The power fail input can perform all lock-out functions previously mentioned, except that no external interrupt will be issued. Note that the linear power fail circuitry is switched off automatically when using V_{BB} in standby mode.

LOW BATTERY, INITIAL POWER ON DETECT, AND POWER FAIL TIME SAVE

There are three other functions provided on the LV8570A to ease power supply control. These are an initial Power On detect circuit, which also can be used as a time keeping failure detect, a low battery detect circuit, and a time save on power failure.

On initial power up the Oscillator Fail Flag will be set to a one and the real time clock start bit reset to a zero. This indicates that an oscillator fail event has occurred, and time keeping has failed.

The Oscillator Fail flag will not be reset until the real-time clock is started. This allows the system to discriminate between an initial power-up and recovery from a power failure. If the battery backed mode is selected, then bit D6 of the Periodic Flag Register must be written low. This will not affect the contents of the Oscillator Fail Flag.

Another status bit is the low battery detect. This bit is set only when the clock is operating under the V_{CC} pin, and when the battery voltage is determined to be less than 2.1V (typical). When the power fail interrupt enable bit is low, it disables the power fail circuit and will also shut off the low battery voltage detection circuit as well.

To relieve CPU overhead for saving time upon power failure, the Time Save Enable bit is provided to do this automatically. (See also Reading the Clock: Latched Read.) The Time Save Enable bit, when set, causes the Time Save RAM to follow the contents of the clock. This bit can be reset by software, but if set before a power failure occurs, it will automatically be reset when the clock switches to the battery supply (not when a power failure is detected by the $\overline{PFAIL}$ pin). Thus, writing a one to the Time Save bit enables both a software write or power fail write.

SINGLE POWER SUPPLY APPLICATIONS

The LV8570A can be used in a single power supply application. To achieve this, the V_{BB} pin must be connected to ground, and the power connected to V_{CC} and $\overline{PFAIL}$ pins. The Oscillator Failed/Single Supply bit in the Periodic Flag Register should be set to a logic 1, which will disable the oscillator battery reference circuit. The power fail interrupt should also be disabled. This will turn off the linear power fail detection circuits, and will eliminate any quiescent power drawn through these circuits. Until the crystal select bits are initialized, the LV8570A may consume about 50 μA due to arbitrary oscillator selection at power on.

(This extra 50 μA is not consumed if the battery backed mode is selected).

TIMER FUNCTIONAL DESCRIPTION

The LV8570A contains 2 independent multi-mode timers. Each timer is composed of a 16-bit negative edge triggered binary down counter and associated control. The operation is similar to existing μP peripheral timers except that several features have been enhanced. The timers can operate in four modes, and in addition, the input clock frequency can be selected from a prescaler over a wide range of frequencies. Furthermore, these timers are capable of generating interrupts as well as hardware output signals, and both the interrupt and timer outputs are fully programmable active high, or low, open drain, or push-pull.

Figure 7 shows the functional block diagram of one of the timers. The timer consists of a 16-bit counter, two 8-bit input registers, two 8-bit output registers, clock prescaler, mode control logic, and output control logic. The timer and the data registers are organized as two bytes for each timer. Under normal operations a read/write to the timer locations will read or write to the data input register. The timer contents can be read by setting the counter Read bit (RD) in the timer control register.

TIMER INITIALIZATION

The timer's operation is controlled by a set of registers, as listed in Table III. These consist of 2 data input registers and one control register per timer. The data input registers contain the timers count down value. The Timer Control Register is used to set up the mode of operation and the input clock rate. The timer related interrupts can be controlled by programming the Interrupt Routing Register and Interrupt Control Register 0. The timer outputs are configured by the Output Mode Register.

TABLE III. Timer Associated Registers

Register Name	Register Select	Page Select	Address
Timer 0 Data MSB	X	0	10H
Timer 0 Data LSB	X	0	0FH
Timer 0 Control Register	0	0	01H
Timer 1 Data MSB	X	0	12H
Timer 1 Data LSB	X	0	11H
Timer 1 Control Register	0	0	02H
Interrupt Routing Register	0	0	04H
Interrupt Control Reg. 0	1	0	03H
Output Mode Register	1	0	02H

All these registers must be initialized prior to starting the timer(s). The Timer Control Register should first be set to select the timer mode with the timer start/$\overline{stop}$ bit reset. Then when the timer is to be started the control register should be rewritten identically but with the start/$\overline{stop}$ bit set.

TIMER OPERATION

Each timer is capable of operation in one of four modes. As mentioned, these modes are programmed in each timer's Control Register which is described later. All four modes operate in a similar manner. They operate on the two 8-bit data words stored into the Data Input Register. At the beginning of a counting cycle the 2 bytes are loaded into the timer and the timer commences counting down towards zero. The exact action taken when zero is reached depends on the mode selected, but in general, the timer output will change state, and an interrupt will be generated if the timer interrupts are unmasked.

Functional Description (Continued)

INPUT CLOCK SELECTION

The input frequency to the timers may be selected. Each timer has a prescaler that gives a wide selection of clocking rates. In addition, the LV8570A has a single external clock input pin that can be selected for either of the timers. Table IV shows the range of programmable clocks available and the corresponding setting in the Timer Control Register.

TABLE IV. Programmable Timer Input Clocks

C2	C1	C0	Selected Clock
0	0	0	External
0	0	1	Crystal Oscillator
0	1	0	(Crystal Oscillator)/4
0	1	1	93.5 μs (10.7 kHz)
1	0	0	1 ms (1 kHz)
1	0	1	10 ms (100 Hz)
1	1	0	1/10 Second (10 Hz)
1	1	1	1 Second (1 Hz)

Note that the second and third selections are not fixed frequencies, but depend on the crystal oscillator frequency chosen.

Since the input clock frequencies are usually running asynchronously to the timer Start/$\overline{\text{Stop}}$ control bit, a 1 clock cycle error may result. This error results when the Start/Stop occurs just after the clock edge (max error). To minimize this error on all clocks an independent prescaler is used for each timer and is designed so that its Start/Stop error is less than 1 clock cycle.

The count hold/gate bit in the Timer Control Register and the external enable pins, G0/G1, can be used to suspend the timer operation in modes 0, 1, and 2 (in mode 3 it is the trigger input). The external pin and the register bit are OR'ed together, so that when either is high the timers are suspended. Suspending the timer causes the same synchronization error that starting the timer does. The range of errors is specified in Table V.

TABLE V. Maximum Synchronization Errors

Clock Selected	Error
External	+Ext. Clock Period
Crystal	+1 Crystal Clock Period
Crystal/4	+1 Crystal Clock Period
10.7 kHz	+32 μs
1 kHz	+32 μs
100 Hz	+32 μs
10 Hz	+32 μs
1 Hz	+32 μs

MODES OF OPERATION

Bits M0 and M1 in the Timer Control Registers are used to specify the modes of operation. The mode selection is described in Table VI.

TABLE VI. Programmable Timer Modes of Operation

M1	M0	Function	Modes
0	0	Single Pulse Generator	Mode 0
0	1	Rate Generator, Pulse Output	Mode 1
1	0	Square Wave Output	Mode 2
1	1	Retriggerable One Shot	Mode 3

MODE 0: SINGLE PULSE GENERATOR

When the timer is in this mode the output will be initially low if the Timer Start/$\overline{\text{Stop}}$ bit is low (stopped). When this mode is initiated the timer output will go high on the next falling edge of the prescaler's input clock, the contents

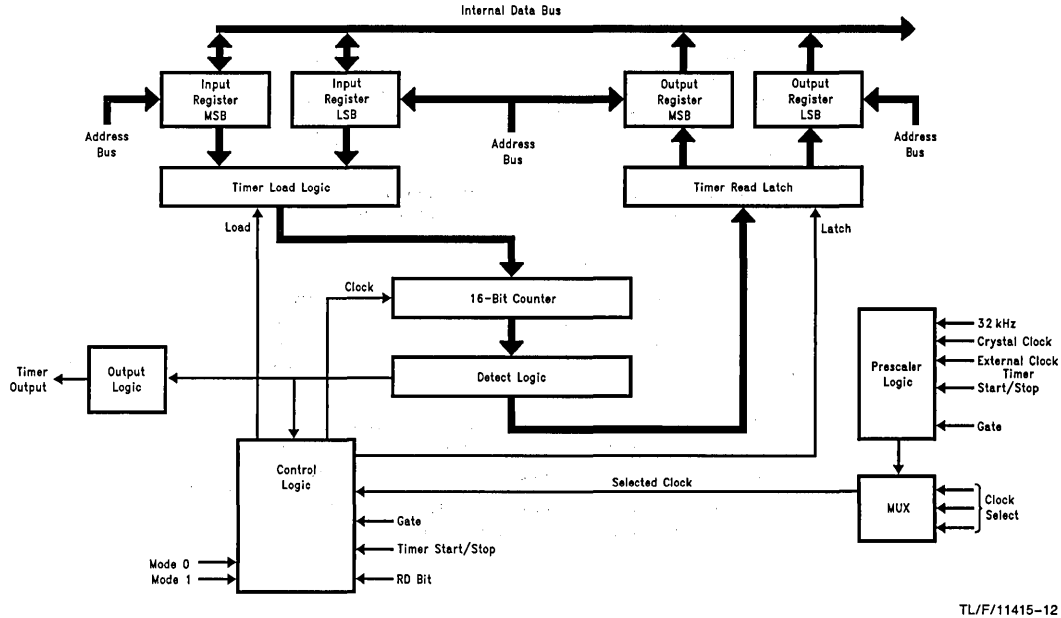

FIGURE 7. LV8570A Timer Block Diagram

Functional Description (Continued)

of the input data registers are loaded into the timer. The output will stay high until the counter reaches zero. At zero the output is reset. The result is an output pulse whose duration is equal to the input clock period times the count value (N) loaded into the input data register. This is shown in *Figure 8*.

Pulse Width = Clock Period × N

An interrupt is generated when the zero count is reached. This can be used for one-time interrupts that are set to occur a certain amount of time in the future. In this mode the Timer Start/$\overline{\text{Stop}}$ bit (TSS) is automatically reset upon zero detection. This removes the need to reset TSS before starting another operation.

The count down operation may be temporarily suspended either under software control by setting the Count Hold/Gate bit in the timer register high, or in hardware by setting the G0 or G1 pin high.

The above discussion assumes that the timer outputs were programmed to be non-inverting outputs (active high). If the polarity of the output waveform is wrong for the application the polarity can be reversed by configuring the Output Mode Register. The drive configuration can also be programmed to be push pull or open drain.

MODE 1: RATE GENERATOR

When operating in this mode the timer will operate continuously. Before the timer is started its output is low. When the timer is started the input data register contents are loaded into the counter on the negative clock edge and the output is set high (again assuming the Output Mode Register is programmed active high). The timer will then count down to zero. Once the zero count is reached the output goes low for one clock period of the timer clock. Then on the next clock the counter is reloaded automatically and the countdown repeats itself. The output, shown in *Figure 9*, is a waveform whose pulse width and period is determined by N, the input register value, and the input clock period:

Period = (N + 1) (Clock Period)

Pulse Width = Clock Period

The G0 or G1 pin and the count hold/gate bit can be used to suspend the appropriate timer countdown when either is high. Again, the output polarity is controllable as in mode 0. If enabled, an interrupt is generated whenever the zero count is reached. This can be used to generate a periodic interrupt.

MODE 2: SQUARE WAVE GENERATOR

This mode is also cyclic but in this case a square wave rather than a pulse is generated. The output square wave period is determined by the value loaded into the timer input register. This period and the duty cycle are:

Period = 2(N + 1) (Clock Period) Duty Cycle = 0.5

When the timer is stopped the output will be low, and when the Start/$\overline{\text{Stop}}$ bit is set high the timer's counter will be loaded on the next clock falling transition and the output will be set high.

The output will be toggled after the zero count is detected and the counter will then be reloaded, and the cycle will continue. Thus, every N + 1 counts the output gets toggled, as shown in *Figure 10*. Like the other modes the timer operation can be suspended either by software setting the count hold/gate bit (CHG) in the Timer Control Register or by using the gate pins. An interrupt will be generated every falling edge of the timer output, if enabled.

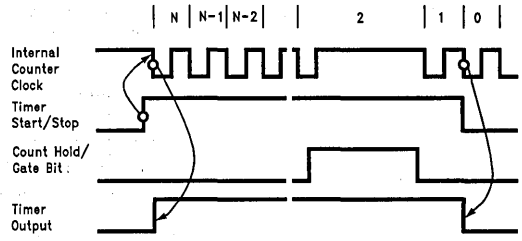

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FIGURE 8. Typical Waveforms for Timer Mode 0 (Timer Output Programmed Active High)

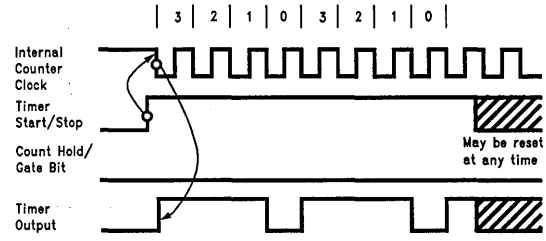

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FIGURE 9. Timing Waveforms for Timer Mode 1 (Timer Output Programmed Active High)

Functional Description (Continued)

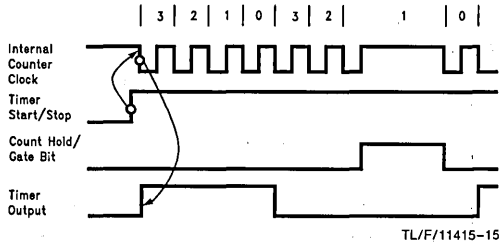


FIGURE 10. Timing Waveforms for Timer Mode 2 (Timer Output Programmed Active High)

MODE 3: RETRIGGERABLE ONE SHOT

This mode is different from the previous three modes in that this is the only mode which uses the external gate to trigger the output. Once the timer Start/$\overline{\text{Stop}}$ bit is set the output stays inactive, and nothing happens until a positive transition is received on the G1 or G0 pins, or the Count Hold/ Gate (CHG) bit is set in the timer control register. When a transition ocurs the one shot output is set active immediately; the counter is loaded with the value in the input register on the next transition of the input clock and the countdown begins. If a retrigger occurs, regardless of the current counter value, the counters will be reloaded with the value in the input register and the counter will be restarted without changing the output state. See *Figure 11*. A trigger count can occur at any time during the count cycle and can be a hardware or software signal (G0, G1 or CHG). In this mode the timer will output a single pulse whose width is determined by the value in the input data register (N) and the input clock period.

Pulse Width = Clock Period × N

Before entering mode 3, if a spurious edge has occurred on G0/G1 or the CHG bit is set to logic 1, then a pulse will appear at MFO or T1 or INTR output pin when the timer is started. To ensure this does not happen, do the following steps before entering mode 3: Configure the timer for mode 0, load a count of zero, then start the timer.

The timer will generate an interrupt only when it reaches a count of zero. This timer mode is useful for continuous "watch dog" timing, line frequency power failure detection, etc.

READING THE TIMERS

Normally reading the timer data register addresses, 0FH and 10H for Timer 0 and 11H and 12H for Timer 1 will result in reading the input data register which contains the preset value for the timers. During timer operation it is often useful to read the contents of the 16-bit down counter. This reading may be an erroneous value of FFFFH.

To read a timer, the μP first sets the timer read bit in the appropriate Timer Control Register high. This will cause the counter's contents to be latched to 2–8 bit output registers, and will enable these registers to be read if the μP reads the timer's input data register addresses. On reading the LSB byte the timer read bit is internally reset and subsequent reads of the timer locations will return the input register values.

DETAILED REGISTER DESCRIPTION

There are 5 external address bits: Thus, the host microprocessor has access to 32 locations at one time. An internal switching scheme provides a total of 67 locations.

This complete address space is organized into two pages. Page 0 contains two blocks of control registers, timers, real time clock counters, and special purpose RAM, while page 1 contains general purpose RAM. Using two blocks enables the 9 control registers to be mapped into 5 locations. The only register that does not get switched is the Main Status Register. It contains the page select bit and the register select bit as well as status information.

A memory map is shown in *Figure 2* and register addressing in Table VII. They show the name, address and page locations for the LV8570A.

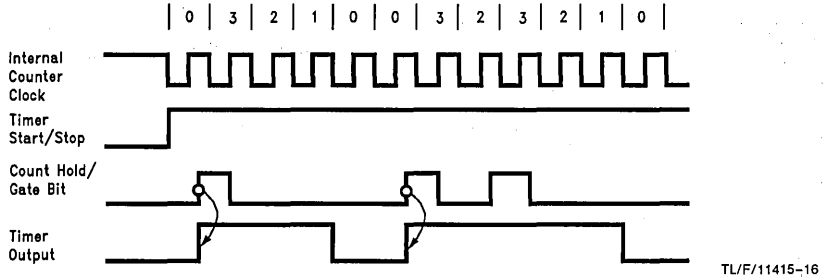


FIGURE 11. Timing Waveforms for Timer Mode 3, Output Programmed Active High

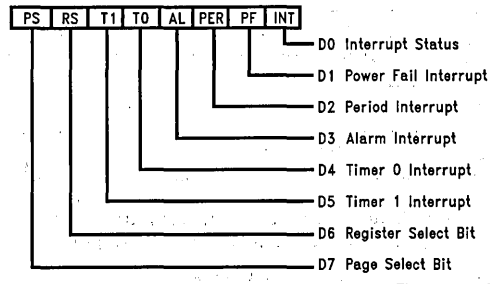
Functional Description (Continued)

TABLE VII. Register/Counter/RAM Addressing for LV8570A

A0-4	PS (Note 1)	RS (Note 2)	Description
CONTROL REGISTERS			
00	X	X	Main Status Register
01	0	0	Timer 0 Control Register
02	0	0	Timer 1 Control Register
03	0	0	Periodic Flag Register
04	0	0	Interrupt Routing Register
01	0	1	Real Time Mode Register
02	0	1	Output Mode Register
03	0	1	Interrupt Control Register 0
04	0	1	Interrupt Control Register 1
COUNTERS (CLOCK CALENDAR)			
05	0	X	1/100, 1/10 Seconds (0-99)
06	0	X	Seconds (0-59)
07	0	X	Minutes (0-59)
08	0	X	Hours (1-12, 0-23)
09	0	X	Days of Month (1-28/29/30/31)
0A	0	X	Months (1-12)
0B	0	X	Years (0-99)
0C	0	X	Julian Date (LSB) (1-99)
0D	0	X	Julian Date (0-3)
0E	0	X	Day of Week (1-7)
TIMER DATA REGISTERS			
0F	0	X	Timer 0 LSB
10	0	X	Timer 0 MSB
11	0	X	Timer 1 LSB
12	0	X	Timer 1 MSB
TIME COMPARE RAM			
13	0	X	Sec Compare RAM (0-59)
14	0	X	Min Compare RAM (0-59)
15	0	X	Hours Compare RAM (1-12, 0-23)
16	0	X	DOM Compare RAM (1-28/29/30/31)
17	0	X	Months Compare RAM (1-12)
18	0	X	DOW Compare RAM (1-7)
TIME SAVE RAM			
19	0	X	Seconds Time Save RAM
1A	0	X	Minutes Time Save RAM
1B	0	X	Hours Time Save RAM
1C	0	X	Day of Month Time Save RAM
1D	0	X	Months Time Save RAM
1E	0	1	RAM
1F	0	X	RAM/Test Mode Register
01-1F	1	X	2nd Page General Purpose RAM

1 PS—Page Select (Bit D7 of Main Status Register)
2 RS—Register Select (Bit D6 of Main Status Register)

MAIN STATUS REGISTER



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The Main Status Register is always located at address 0 regardless of the register block or the page selected.

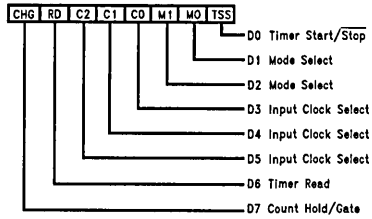
D0: This read only bit is a general interrupt status bit that is taken directly from the interrupt pins. The bit is a one when an interrupt is pending on either the INTR pin or the MFO pin (when configured as an interrupt). This is unlike D3-D5 which can be set by an internal event but may not cause an interrupt. This bit is reset when the interrupt status bits in the Main Status Register are cleared.

D1-D5: These five bits of the Main Status Register are the main interrupt status bits. Any bit may be a one when any of the interrupts are pending. Once an interrupt is asserted the μP will read this register to determine the cause. These interrupt status bits are not reset when read. Except for D1, to reset an interrupt a one is written back to the corresponding bit that is being tested. D1 is reset whenever the $\overline{\text{PFAIL}}$ pin = logic 1. This prevents loss of interrupt status when reading the register in a polled mode. D1, D3-D5 are set regardless of whether these interrupts are masked or not by bits D6 and D7 of Interrupt Control Registers 0 and 1.

D6 and D7: These bits are Read/Write bits that control which register block or RAM page is to be selected. Bit D6 controls the register block to be accessed (see memory map). The memory map of the clock is further divided into two memory pages. One page is the registers, clock and timers, and the second page contains 31 bytes of general purpose RAM. The page selection is determined by bit D7.

Functional Description (Continued)

TIMER 0 AND 1 CONTROL REGISTER



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These registers control the operation of the timers. Each timer has its own register.

D0: This bit will Start (1) or Stop (0) the timer. When the timer is stopped the timer's prescaler and counter are reset, and the timer will restart from the beginning when started again. In mode 0 on time out the TSS bit is internally reset.

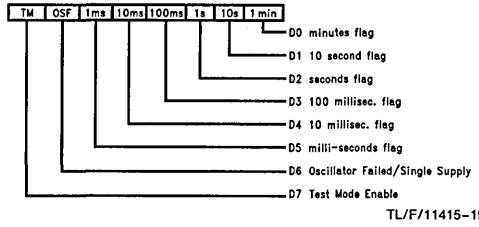
D1 and D2: These control the count mode of the timers. See Table VI.

D3–D5: These bits control which clock signal is applied to the timer's counter input. There is one external clock input pin (TCK) and either (or both) timer(s) can be selected to run off this pin: refer to Table IV for details.

D6: This is the read bit. If a one is written into this location it will cause the contents of the timer to be latched into a holding register, which can be read by the μP at any time. Reading the least significant byte of the timer will reset the RD bit. The timer read cycle can be aborted by writing RD to zero.

D7: The CHG bit has two mode dependent functions. In modes 0 through 2 writing a one to this bit will suspend the timer operation (without resetting the timer prescaler). However, in mode 3 this bit is used to trigger or re-trigger the count sequence as with the gate pins. If retriggering is desired using the CHG bit, it is not necessary to write a zero to this location prior to the re-trigger. The action of further writing a one to this bit will re-trigger the count.

PERIODIC FLAG REGISTER



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The Periodic Flag Register has the same bit for bit correspondence as Interrupt Control Register 0 except for D6 and D7. For normal operation (i.e., not a single supply application) this register must be written to on initial power up or after an oscillator fail event. D0–D5 are read only bits, D6 and D7 are read/write.

D0–D5: These bits are set by the real time rollover events: (Time Change = 1). The bits are reset when the register is read and can be used as selective data change flags.

D6: This bit performs a dual function. When this bit is read, a one indicates that an oscillator failure has occurred and the time information may have been lost. Some of the ways an oscillator failure can be caused are: failure of the crystal; shorting OSC IN or OSC OUT to GND or V_{CC}; removal of crystal; removal of battery when in the battery backed mode (when a '0' is written to D6); lowering the voltage at the V_{BB} pin to a value less than 2.2V when in the battery backed mode. Bit D6 is automatically set to 1 on initial power-up or an oscillator fail event. The oscillator fail flag is reset by writing a one to the clock start/$\overline{\text{stop}}$ bit in the Real Time Mode Register, with the crystal oscillating.

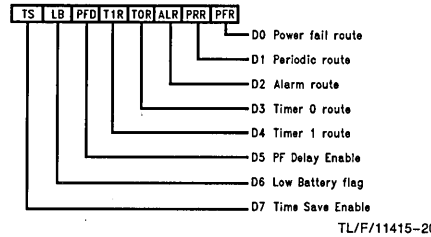
When D6 is written to, it defines whether the TCP is being used in battery backed (normal) or in a single supply mode application. When set to a one this bit configures the TCP for single power supply applications. This bit is automatically set on initial power-up or an oscillator fail event. When set, D6 disables the oscillator reference circuit. The result is that the oscillator is referenced to V_{CC}. When a zero is written to D6 the oscillator reference is enabled, thus the oscillator is referenced to V_{BB}. This allows operation in standard battery standby applications.

At initial power on, if the LV8570A is going to be programmed for battery backed mode, the V_{BB} pin should be connected to a potential in the range of 2.2V to V_{CC} − 0.4V.

For single supply mode operation, the V_{BB} pin should be connected to GND and the $\overline{\text{PFAIL}}$ pin connected to V_{CC}.

D7: Writing a one to this bit enables the test mode register at location 1F (see Table VII). This bit should be forced to zero during initialization for normal operation. If the test mode has been entered, clear the test mode register before leaving test mode. (See separate test mode application note for further details.)

INTERRUPT ROUTING REGISTER



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D0–D4: The lower 5 bits of this register are associated with the main interrupt sources created by this chip. The purpose of this register is to route the interrupts to either the MFO (multi-function pin), or to the main interrupt pin. When any bit is set the associated interrupt signal will be sent to the MFO pin, and when zero it will be sent to the INTR pin.

Functional Description (Continued)

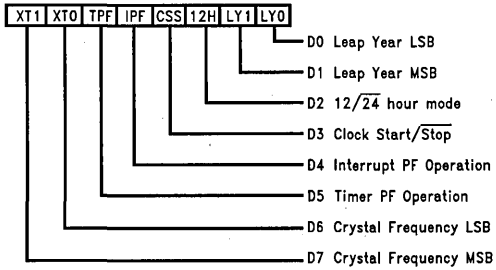
D5: The Delay Enable bit is used when a power fail occurs. If this bit is set, a 480 μs delay is generated internally before the μP interface is locked out. This will enable the μP to access the registers for up to 480 μs after it receives a power fail interrupt. After a power failure is detected but prior to the 480 μs delay timing out, the host μP may force immediate lock out by resetting the Delay Enable bit. Note if this bit is a 0 when power fails then after a delay of 30 μs min/63 μs max the μP cannot read the chip.

D6: This read only bit is set and reset by the voltage at the V_{BB} pin. It can be used by the μP to determine whether the battery voltage at the V_{BB} pin is getting too low. A comparator monitors the battery and when the voltage is lower than 2.1V (typical) this bit is set. The power fail interrupt must be enabled to check for a low battery voltage.

D7: Time Save Enable bit controls the loading of real-time-clock data into the Time Save RAM. When a one is written to this bit the Time Save RAM will follow the corresponding clock registers, and when a zero is written to this bit the time in the Time Save RAM is frozen. This eliminates any synchronization problems when reading the clock, thus negating the need to check for a counter rollover during a read cycle.

This bit must be set to a one prior to power failing to enable the Time Save feature. When the power fails this bit is automatically reset and the time is saved in the Time Save RAM.

REAL TIME MODE REGISTER



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D0–D1: These are the leap year counter bits. These bits are written to set the number of years from the previous leap year. The leap year counter increments on December 31st and it internally enables the February 29th counter state. This method of setting the leap year allows leap year to occur whenever the user wishes to, thus providing flexibility in implementing Japanese leap year function.

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

D2: The count mode for the hours counter can be set to either 24 hour mode or 12 hour mode with AM/PM indicator. A one will place the clock in 12 hour mode.

D3: This bit is the master Start/$\overline{\text{Stop}}$ bit for the clock. When a one is written to this bit the real time counter's prescaler and counter chain are enabled. When this bit is reset to zero the contents of the real time counter is stopped and the prescaler is cleared. When the TCP is initially powered up this bit will be held at a logic 0 until the oscillator starts functioning correctly after which this bit may be modified. If an oscillator fail event occurs, this bit will be reset to logic 0.

D4: This bit controls the operation of the interrupt output in standby mode. If set to a one it allows Alarm, Periodic, and Power Fail interrupts to be functional in standby mode. Timer interrupts will also be functional provided that bit D5 is also set. Note that the MFO and INTR pins are configured as open drain in standby mode.

If bit D4 is set to a zero then interrupt control register 0 and bits D6 and D7 of interrupt control register 1 will be reset when the TCP enters the standby mode. They will have to be re-configured when system (V_{CC}) power is restored.

D5: This bit controls the operation of the timers in standby mode. If set to a one the timers will continue to function when the TCP is in standby mode. The input pins TCK, G0, G1 are locked out in standby mode, and cannot be used.

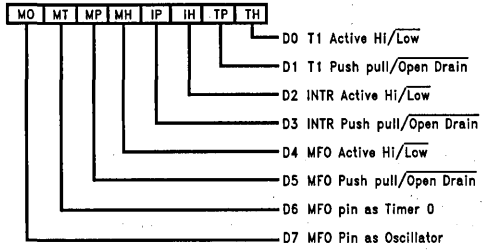
Therefore external control of the timers is not possible in standby mode. Note also that MFO and T1 pins are automatically reconfigured open drain during standby.

D6 and D7: These two bits select the crystal clock frequency as per the following table:

XT1	XT0	Crystal Frequency
0	0	32.768 kHz
0	1	4.194304 MHz
1	0	4.9152 MHz
1	1	32.000 kHz

All bits are Read/Write, and any mode written into this register can be determined by reading the register. On initial power up these bits are random.

OUTPUT MODE REGISTER



TL/F/11415–22

Functional Description (Continued)

D0: This bit, when set to a one makes the T1 (timer 1) output pin active high, and when set to a zero, it makes this pin active low.

D1: This bit controls whether the T1 pin is an open drain or push-pull output. A one indicates push pull.

D2: This bit, when set to a one makes the INTR output pin active high, and when set to a zero, it makes this pin active low.

D3: This bit controls whether the INTR pin is an open drain or push-pull output. A one indicates push-pull.

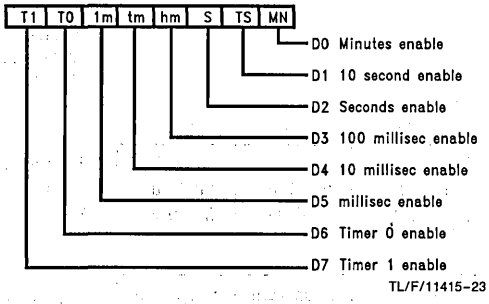
D4: This bit, when set to a one makes the MFO output pin active high, and when set to a zero, it makes this pin active low.

D5: This bit controls whether the MFO pin is an open drain or push-pull output. A one indicates push-pull.

D6 and D7: These bits are used to program the signal appearing at the MFO output, as follows:

D7	D6	MFO Output Signal
0	0	2nd Interrupt
0	1	Timer 0 Waveform
1	X	Buffered Crystal Oscillator

INTERRUPT CONTROL REGISTER 0

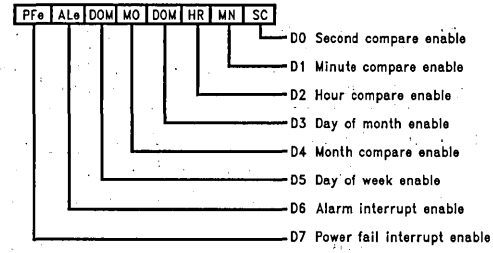


TL/F/11415–23

D0–D5: These bits are used to enable one of the selected periodic interrupts by writing a one into the appropriate bit. These interrupts are issued at the rollover of the clock. For example, the minutes interrupt will be issued whenever the minutes counter increments. In all likelihood the interrupt will be enabled asynchronously with the real time change. Therefore, the very first interrupt will occur in less than the periodic time chosen, but after the first interrupt all subsequent interrupts will be spaced correctly. These interrupts are useful when minute, second, real time reading, or task switching is required. When all six bits are written to a 0 this disables periodic interrupts from the Main Status Register and the interrupt pin.

D6 and D7: These are individual timer enable bits. A one written to these bits enable the timers to generate interrupts to the μP.

INTERRUPT CONTROL REGISTER 1



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D0–D5: Each of these bits are enable bits which will enable a comparison between an individual clock counter and its associated compare RAM. If any bit is a zero then that clock-RAM comparator is set to the "always equal" state and the associated TIME COMPARE RAM byte can be used as general purpose RAM. However, to ensure that an alarm interrupt is not generated at bit D3 of the Main Status Register, all bits must be written to a logic zero.

D6: In order to generate an external alarm compare interrupt to the μP from bit D3 of the Main Status Register, this bit must be written to a logic 1.

D7: The MSB of this register is the enable bit for the Power Fail Interrupt. When this bit is set to a one an interrupt will be generated to the μP when $\overline{\text{PFAIL}} = 0$.

This bit also enables the low battery detection analog circuitry.

If the user wishes to mask the power fail interrupt, but utilize the analog circuitry, this bit should be enabled, and the Routing Register can be used to route the interrupt to the MFO pin. The MFO pin can then be left open or configured as the Timer 0 or buffered oscillator output.

Control and Status Register Address Bit Map

Main Status Register PS = 0 RS = 0 ADDRESS = 00H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W[1]	R/W[1]	R/W[1]	R/W[1]	R[2]	R[3]
Page Select	Register Select	Timer 1 Interrupt	Timer 0 Interrupt	Alarm Interrupt	Periodic Interrupt	Power Fail Interrupt	Interrupt Status

1. Reset by writing 1 to bit.
2. Set/reset by voltage at $\overline{PFAIL}$ pin.
3. Reset when all pending interrupts are removed.

Timer 0 Control Register PS = 0 RS = 0 Address = 01H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Timer 1 Control Register PS = 0 RS = 0 Address = 02H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Periodic Flag Register PS = 0 RS = 0 Address = 03H

R/W	R/W[4]	R[5]	R[5]	R[5]	R[5]	R[5]	R[5]
Test Mode	Osc. Fail/ Single Supply	1 ms Flag	10 ms Flag	100 ms Flag	Seconds Flag	10 Second Flag	Minute Flag

4. Read Osc fail Write 0 Batt-Backed Mode Write 1 Single Supply Mode
5. Reset by positive edge of read.

Interrupt Routing Register PS = 0 RS = 0 Address = 04H

R/W	R[6]	R/W	R/W	R/W	R/W	R/W	R/W
Time Save Enable	Low Battery Flag	Power Fail Delay Enable	Timer 1 Int. Route MFO/$\overline{INT}$	Timer 0 Int. Route MFO/$\overline{INT}$	Alarm Int. Route MFO/$\overline{INT}$	Periodic Int. Route MFO/$\overline{INT}$	Power Fail Int. Route MFO/$\overline{INT}$

6. Set and reset by V_{BB} voltage.

Real Time Mode Register PS = 0 RS = 1 Address = 01H

Crystal Freq. XT1	Crystal Freq. XT0	Timers EN on Back-Up	Interrupt EN on Back-Up	Clock Start/$\overline{Stop}$	12/$\overline{24}$ Hr. Mode	Leap Year MSB	Leap Year LSB

All Bits R/W

Output Mode Register PS = 0 RS = 1 Address = 02H

MFO as Crystal	MFO as Timer 0	MFO PP/$\overline{OD}$	MFO Active HI/$\overline{LO}$	INTR PP/$\overline{OD}$	INTR Active HI/$\overline{LO}$	T1 PP/$\overline{OD}$	T1 Active HI/$\overline{LO}$

All Bits R/W

Interrupt Control Register 0 PS = 0 RS = 1 Address = 03H

Timer 1 Interrupt Enable	Timer 0 Interrupt Enable	1 ms Interrupt Enable	10 ms Interrupt Enable	100 ms Interrupt Enable	Seconds Interrupt Enable	10 Second Interrupt Enable	Minute Interrupt Enable

All Bits R/W

Interrupt Control Register 1 PS = 0 RS = 1 Address = 04H

Power Fail Interrupt Enable	Alarm Interrupt Enable	DOW Interrupt Enable	Month Interrupt Enable	DOM Interrupt Enable	Hours Interrupt Enable	Minute Interrupt Enable	Second Interrupt Enable

All Bits R/W

Application Hints

Suggested Initialization Procedure for LV8570A in battery backed applications that use the V_{BB} pin

1. Enter the test mode by writing a 1 to bit D7 in the Periodic Flag Register.
2. Write zero to the RAM/TEST mode Register located in page 0, address HEX 1F.
3. Leave the test mode by writing a 0 to bit D7 in the Periodic Flag Register. Steps 1, 2, 3 guarantee that if the test mode had been entered during power on (due to random pulses from the system), all test mode conditions are cleared. Most important is that the OSC Fail Disable bit is cleared. Refer to AN-589 for more information on test mode operation.
4. After power on (V_{CC} and V_{BB} powered), select the correct crystal frequency bits (D7, D6 in the Real Time Mode Register) as shown in Table I.

TABLE I

Frequency	D7	D6
32.768 kHz	0	0
4.194304 MHz	0	1
4.9152 MHz	1	0
32.0 kHz	1	1

5. Enter a software loop that does the following:

   Set a 3 second (approx.) software counter. The crystal oscillator may take 1 second to start.

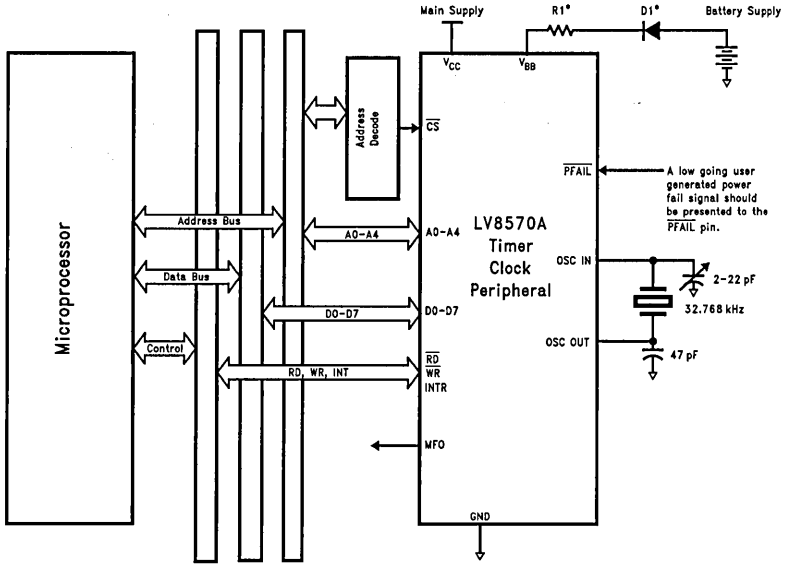
   5.1 Write a 1 to bit D3 in the Real Time Mode Register (try to start the clock). Make sure the crystal select bits remain the same as in step 1. Under normal operation, this bit can be set only if the oscillator is running. During the software loop, RAM, real time counters, output configuration, interrupt control and timer functions may be initialized.
6. Test bit D6 in the Periodic Flag Register:

   IF a 1, go to 5.1. If this bit remains a 1 after 3 seconds, then abort and check hardware. The crystal may be defective or not installed. There may be a short at OSC IN or OSC OUT to V_{CC} or GND, or to some impedance that is less than 10 MΩ.

   IF a 0, then the oscillator is running, go to step 7.
7. Write a 0 to bit D6 in the Periodic Flag Register. This action puts the clock chip in the battery backed mode. This mode can be entered only if the osc fail flag (bit D6 of the Periodic Flag Register) is a 0. Reminder, Bit D6 is a dual function bit. When read, D6 returns oscillator status. When written, D6 causes either the Battery Backed Mode, or the Single Supply Mode of operation.

   The only method to ensure the chip is in the battery backed mode is to measure the waveform at the OSC OUT pin. If the battery backed mode was selected successfully, then the peak to peak waveform at OSC OUT is referenced to the battery voltage. If not in battery backed mode, the waveform is referenced to V_{CC}. The measurement should be made with a high impedance low capacitance probe (10 MΩ, 10 pF oscilloscope probe or better). Typical peak to peak swings are within (TBD on bench) and ground respectively.
8. Write a 1 to bit D7 of Interrupt Control Register 1. This action enables the $\overline{PFAIL}$ pin and associated circuitry.
9. Initialize the rest of the chip as needed.

Typical Application



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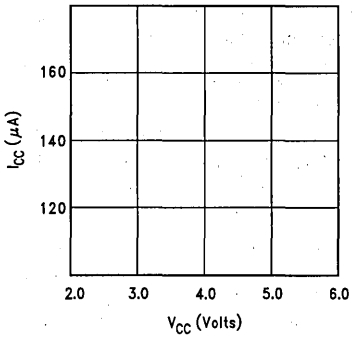
*These components may be necessary to meet UL requirements for lithium batteries. Consult battery manufacturer.

Typical Performance Characteristics

Operating Current vs Supply Voltage (Single Supply Mode F_{OSC} = 32.768 kHz) TBD



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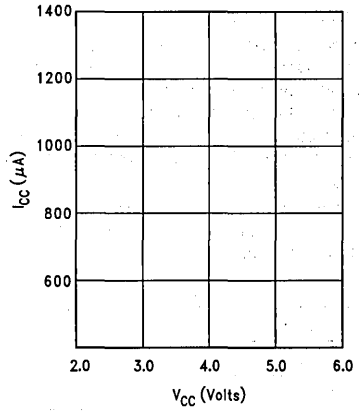
Operating Current vs Supply Voltage (Battery Backed Mode F_{OSC} = 32.768 kHz) TBD



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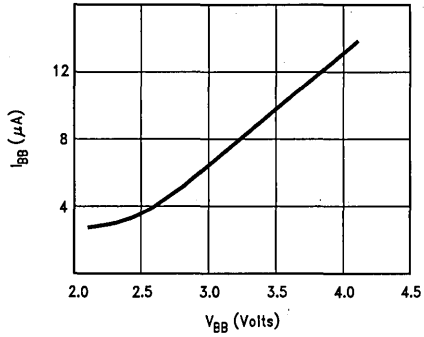
Standby Current vs Power Supply Voltage (F_{OSC} = 32.768 kHz)



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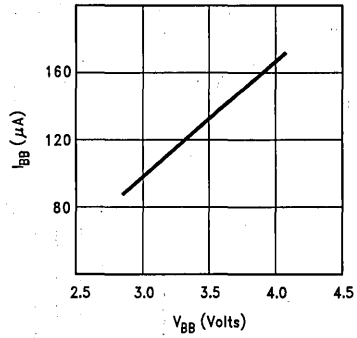
Standby Current vs Power Supply Voltage F_{OSC} = 4.194304 MHz



TL/F/11415–29

National Semiconductor

PRELIMINARY

LV8571A Low Voltage Timer Clock Peripheral (TCP)

General Description

The LV8571A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports. The address space is organized as 2 software selectable pages of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, the Timers and their data RAM, and the Time Save RAM. Any of the RAM locations that are not being used for their intended purpose may be used as general purpose CMOS RAM.

Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week, day of month and day of year counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the crystal and two capacitors. The choice of crystal frequency is program selectable.

Two independent multifunction 10 MHz 16-bit timers are provided. These timers operate in four modes. Each has its own prescaler and can select any of 7 possible clock inputs. Thus, by programming the input clocks and the timer counter values a very wide range of timing durations can be achieved. The range is from about 400 ns (4.915 MHz oscillator) to 65,535 seconds (18 hrs., 12 min.).

Power failure logic and control functions have been integrated on chip. This logic is used by the TCP to issue a power fail interrupt, and lock out the μp interface. The time power fails may be logged into RAM automatically when $V_{BB} > V_{CC}$. Additionally, two supply pins are provided. When $V_{BB} > V_{CC}$, internal circuitry will automatically switch from the main supply to the battery supply. Status bits are provided to indicate initial application of battery power, system power, and low battery detect. (Continued)

Features

- 3.3V ±10% supply
- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week and day of years counters
  - Four selectable oscillator frequencies
  - Parallel resonant oscillator
- Two 16-bit timers
  - 10 MHz external clock frequency
  - Programmable multi-function output
  - Flexible re-trigger facilities
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, timer and power fail interrupts
- Up to 44 bytes of CMOS RAM
- INTR/MFO pins programmable High/Low and push-pull or open drain

Block Diagram

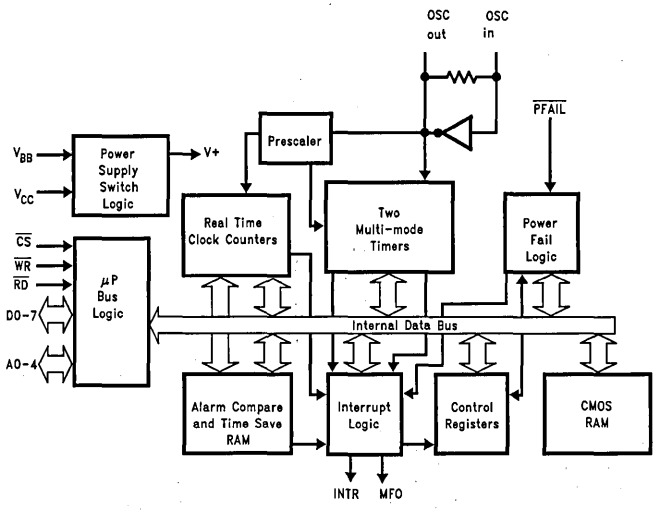


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FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (PD)	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C

Operation Conditions

	Min	Max	Unit
Supply Voltage (V_{CC}) (Note 3)	3.0	3.6	V
Supply Voltage (V_{BB}) (Note 3)	2.2	V_{CC}−0.4	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0.0	V_{CC}	V
Operation Temperature (T_A)	−40	+85	°C
Electr-Static Discharge Rating TBD		1	kV
Typical Values			
θ_{JA} DIP	Board		77°C/W
	Socket		85°C/W
θ_{JA} PLCC	Board		
	Socket		

DC Electrical Characteristics

V_{CC} = 3.3V ±10%, V_{BB} = 2.5V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min (Note 16)	Max (Note 16)	Units
V_{IH}	High Level Input Voltage (Note 4)	Any Inputs Except OSC IN, OSC IN with External Clock	2.0 V_{BB} −0.2	V_{CC} + 0.3	V V
V_{IL}	Low Level Input Voltage	All Inputs Except OSC IN OSC IN with External Clock	−0.3 −0.3	0.8 0.2	V V
V_{OH}	High Level Output Voltage (Excluding OSC OUT)	I_{OUT} = −20 μA I_{OUT} = −2.0 mA	V_{CC} −0.2 2.4		V V
V_{OL}	Low Level Output Voltage (Excluding OSC OUT)	I_{OUT} = 20 μA I_{OUT} = 2.0 mA		0.1 0.3	V V
I_{IN}	Input Current (Except OSC IN)	V_{IN} = V_{CC} or GND		±1.0	μA
I_{OZ}	Output TRI-STATE® Current	V_{OUT} = V_{CC} or GND		±5	μA
I_{LKG}	Output High Leakage Current MFO, INTR Pins	V_{OUT} = V_{CC} or GND Outputs Open Drain		±5	μA
I_{CC}	Quiescent Supply Current (Note 7)	F_{OSC} = 32.768 kHz V_{IN} = V_{CC} or GND (Note 5) V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		 200 700 8	 μA μA mA
		F_{OSC} = 4.194304 MHz or 4.9152 MHz V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		 6 7	 mA mA
I_{CC}	Quiescent Supply Current (Single Supply Mode) (Note 7)	V_{BB} = GND V_{IN} = V_{CC} or GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		 60 6	 μA mA
I_{BB}	Standby Mode Battery Supply Current (Note 8)	V_{CC} = GND OSC OUT = open circuit, other pins = GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		 8 400	 μA μA
I_{BLK}	Battery, Supply Leakage	2.2V ≤ V_{BB} ≤ 2.6V other pins at GND V_{CC} = GND, V_{BB} = 2.6V V_{CC} = 3.6V, V_{BB} = 2.2V	 −5	 1.5 	 μA μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2: Unless otherwise specified all voltages are referenced to ground.
Note 3: For F_{OSC} = 4.194304 or 4.9152 MHz, V_{BB} minimum = 2.8V. In battery backed mode, $V_{BB} \leq V_{CC}$ −0.4V. Single Supply Mode: Data retention voltage is 2.2V min. In single Supply Mode (Power connected to V_{CC} pin) 3.0V ≤ V_{CC} ≤ 3.6V.
Note 4: This parameter (V_{IH}) is not tested on all pins at the same time.
Note 5: This specification tests I_{CC} with all power fail circuitry disabled, by setting D7 of Interrupt Control Register 1 to 0.
Note 6: This specification tests I_{CC} with all power fail circuitry enabled, by setting D7 of Interrupt Control Register 1 to 1.
Note 7: This specification is tested with both the timers and OSC IN driven by a signal generator. Contents of the Test Register = 00(H), the MFO pin is not configured as buffered oscillator out and MFO, INTR, are configured as open drain.
Note 8: This specification is tested with both the timers off, and only OSC IN is driven by a signal generator. Contents of the Test Register = 00(H) and the MFO pin is not configured as buffered oscillator out.

AC Electrical Characteristics

V_{CC} = 3.3V ±10%, V_{BB} = 2.5V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Min (Note 16)	Max (Note 16)	Units
READ TIMING				
t_{AR}	Address Valid Prior to Read Strobe	10		ns
t_{RW}	Read Strobe Width (Note 9)	80		ns
t_{CD}	Chip Select to Data Valid Time		80	ns
t_{RAH}	Address Hold after Read (Note 10)	0		ns
t_{RD}	Read Strobe to Valid Data		70	ns
t_{DZ}	Read or Chip Select to TRI-STATE		70	ns
t_{RCH}	Chip Select Hold after Read Strobe (Note 10)	0		ns
t_{DS}	Minimum Inactive Time between Read or Write Accesses	40		ns
WRITE TIMING				
t_{AW}	Address Valid before Write Strobe	10		ns
t_{WAH}	Address Hold after Write Strobe (Note 10)	0		ns
t_{CW}	Chip Select to End of Write Strobe	60		ns
t_{WW}	Write Strobe Width (Note 11)	50		ns
t_{DW}	Data Valid to End of Write Strobe	40		ns
t_{WDH}	Data Hold after Write Strobe (Note 10)	2		ns
t_{WCH}	Chip Select Hold after Write Strobe (Note 10)	0		ns
INTERRUPT TIMING				
t_{ROLL}	Clock rollover to INTR out is typically 20 μs			

Note 9: Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

Note 10: Hold time is guaranteed by design but not production tested. This limit is not used to calculate outgoing quality levels.

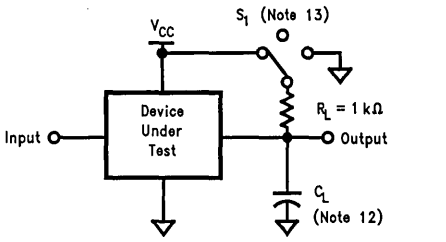
Note 11: Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns (10%–90%)
Input and Output Reference Levels	
TRI-STATE Reference Levels (Note 13)	Active High + Active Low −

Note 12: C_L = 100 pF, includes jig and scope capacitance.

Note 13: S1 = V_{CC} for active low to high impedance measurements.
S1 = GND for active high to high impedance measurements.
S1 = open for all other timing measurements.



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Capacitance (T_A = 25°C, f = 1 MHz)

Symbol	Parameter (Note 14)	Typ	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	7	pF

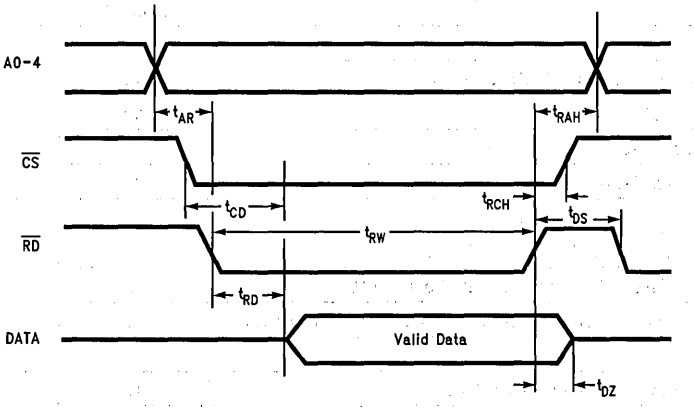
Note 14: This parameter is not 100% tested.

Note 15: Output rise and fall times 25 ns max (10%–90%) with 100 pF load.

Note 16: Room temperature values only.

Timing Waveforms

Read Timing Diagram



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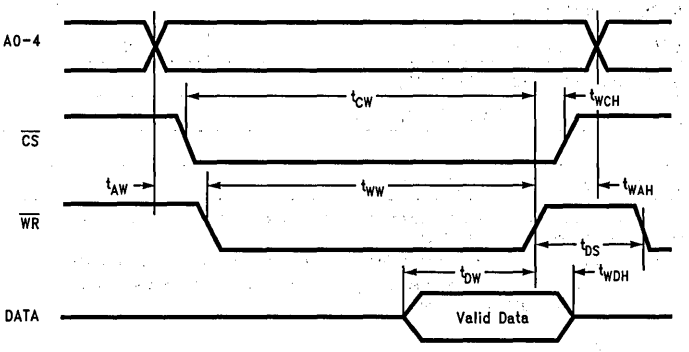
Write Timing Diagram



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General Description (Continued)

The LV8571A's interrupt structure provides four basic types of interrupts: Periodic, Alarm/Compare, Timer, and Power Fail. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

One dedicated general purpose interrupt output is provided. A second interrupt output is available on the Multiple Function Output (MFO) pin. Each of these may be selected to generate an interrupt from any source. Additionally, the MFO pin may be programmed to be either as oscillator output or Timer 0's output.

Pin Description

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (Inputs): These pins interface to μP control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and Write pins are also active low and enable reading or writing to the TCP. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.

A0–A4 (Inputs): These 5 pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.

OSC IN (Input): OSC OUT (Output): These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}, and the correct crystal select bits in the Real Time Mode Register have been set.

MFO (Output): The multi-function output can be used as a second interrupt output for interrupting the μP. This pin can also provide an output for the oscillator or the internal Timer 0. The MFO output can be programmed active high or low, open drain or push-pull. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}. This pin is configured open drain during battery operation ($V_{BB} > V_{CC}$).

INTR (Output): The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The INTR output can be programmed active high or low, push-pull or open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}. This pin is configured open drain during battery operation ($V_{BB} > V_{CC}$).

D0–D7 (Input/Output): These 8 bidirectional pins connect to the host μP's data bus and are used to read from and write to the TCP. When the $\overline{PFAIL}$ pin goes low and a write is not in progress, these pins are at TRI-STATE.

$\overline{PFAIL}$ (Input): In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the TCP goes into a lockout mode, in a minimum of 30 μs or a maximum of 63 μs unless lockout delay is programmed. In the single power supply mode, this pin is not useable as an input and should be tied to V_{CC}. Refer to section on Power Fail Functional Description.

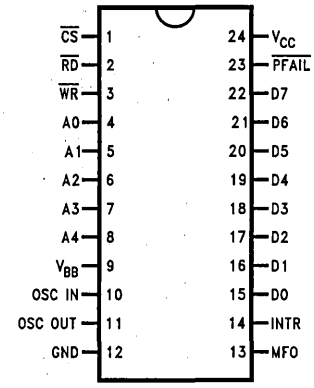
V_{BB} (Battery Power Pin): This pin is connected to a back-up power supply. This power supply is switched to the internal circuitry when the V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the TCP programmed for single power supply only, and power applied to the V_{CC} pin.

V_{CC}: This is the main system power pin.

GND: This is the common ground power pin for both V_{BB} and V_{CC}.

Connection Diagram

Dual-In-Line



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Top View

Order Number LV8571AN
See NS Package Number N24C

3

Functional Description

The LV8571A contains a fast access real time clock, two 10 MHz 16-bit timers, interrupt control logic, power fail detect logic, and CMOS RAM. All functions of the TCP are controlled by a set of nine registers. A simplified block diagram that shows the major functional blocks is given in *Figure 1.*

The blocks are described in the following sections:

1. Real Time Clock
2. Oscillator Prescaler
3. Interrupt Logic
4. Power Failure Logic
5. Additional Supply Management
6. Timers

The memory map of the TCP is shown in the memory addressing table. The memory map consists of two 31 byte pages with a main status register that is common to both pages. A control bit in the Main Status Register is used to select either page. *Figure 2* shows the basic concept. Page 0 contains all the clock timer functions, while page 1 has scratch pad RAM. The control registers are split into two separate blocks to allow page 1 to be used entirely as scratch pad RAM. Again a control bit in the Main Status Register is used to select either control register block.

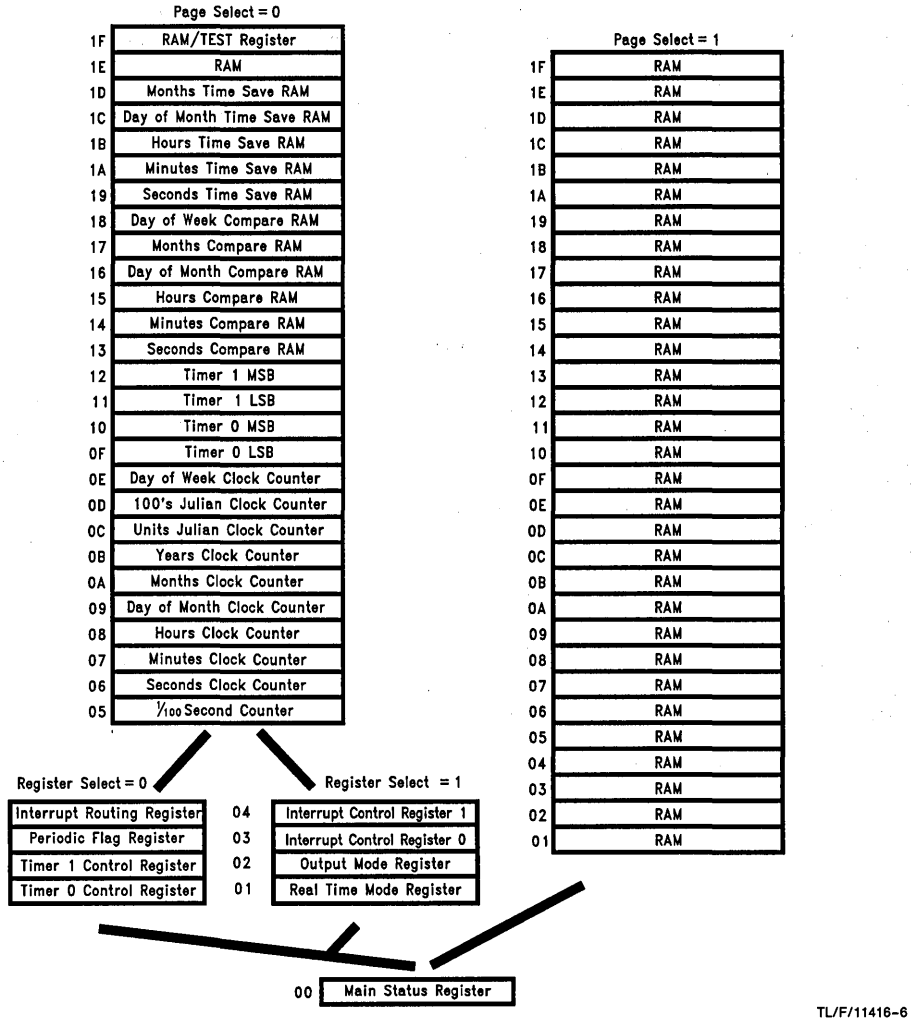

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FIGURE 2. LV8571A Internal Memory Map

Functional Description (Continued)

INITIAL POWER-ON of BOTH V_{BB} and V_{CC}

V_{BB} and V_{CC} may be applied in any sequence. In order for the power fail circuitry to function correctly, whenever power is off, the V_{CC} pin must see a path to ground through a maximum of 1 MΩ. The user should be aware that the control registers will contain random data. The first task to be carried out in an initialization routine is to start the oscillator by writing to the crystal select bits in the Real Time Mode Register. If the LV8571A is configured for single supply mode, an extra 50 μA may be consumed until the crystal select bits are programmed. The user should also ensure that the TCP is not in test mode (see register descriptions).

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

As shown in *Figure 2*, the clock has 10 bytes of counters, which count from 1/100 of a second to years. Each counter counts in BCD and is synchronously clocked. The count sequence of the individual byte counters within the clock is shown later in Table VII. Note that the day of week, day of month, day of year, and month counters all roll over to 1. The hours counter in 12 hour mode rolls over to 1 and the AM/PM bit toggles when the hours rolls over to 12 (AM = 0, PM = 1). The AM/PM bit is bit D7 in the hours counter.

All other counters roll over to 0. Also note that the day of year counter is 12 bits long and occupies two addresses. Upon initial application of power the counters will contain random information.

READING THE CLOCK: VALIDATED READ

Since clocking of the counter occurs asynchronously to reading of the counter, it is possible to read the counter while it is being incremented (rollover). This may result in an incorrect time reading. Thus to ensure a correct reading of the entire contents of the clock (or that part of interest), it must be read without a clock rollover occurring. In general this can be done by checking a rollover bit. On this chip the periodic interrupt status bits can serve this function. The following program steps can be used to accomplish this.

1. Initialize program for reading clock.
2. Dummy read of periodic status bit to clear it.
3. Read counter bytes and store.
4. Read rollover bit, and test it.
5. If rollover occured go to 3.
6. If no rollover, done.

To detect the rollover, individual periodic status bits can be polled. The periodic bit chosen should be equal to the highest frequency counter register to be read. That is if only SECONDS through HOURS counters are read, then the SECONDS periodic bit should be used.

READING THE CLOCK: INTERRUPT DRIVEN

Enabling the periodic interrupt mask bits cause interrupts just as the clock rolls over. Enabling the desired update rate and providing an interrupt service routine that executes in less than 10 ms enables clock reading without checking for a rollover.

READING THE CLOCK: LATCHED READ

Another method to read the clock that does not require checking the rollover bit is to write a one into the Time Save Enable bit (D7) of the Interrupt Routing Register, and then to write a zero. Writing a one into this bit will enable the clock contents to be duplicated in the Time Save RAM. Changing the bit from a one to a zero will freeze and store the contents of the clock in Time Save RAM. The time then can be read without concern for clock rollover, since internal logic takes care of synchronization of the clock. Because only the bits used by the clock counters will be latched, the Time Save RAM should be cleared prior to use to ensure that random data stored in the unused bits do not confuse the host microprocessor. This bit can also provide time save at power failure, see the Additional Supply Management Functions section. With the Time Save Enable bit at a logical 0, the Time Save RAM may be used as RAM if the latched read function is not necessary.

INITIALIZING AND WRITING TO THE CALENDAR-CLOCK

Upon initial application of power to the TCP or when making time corrections, the time must be written into the clock. To correctly write the time to the counters, the clock would normally be stopped by writing the Start/$\overline{\text{Stop}}$ bit in the Real Time Mode Register to a zero. This stops the clock from counting and disables the carry circuitry. When initializing the clock's Real Time Mode Register, it is recommended that first the various mode bits be written while maintaining the Start/$\overline{\text{Stop}}$ bit reset, and then writing to the register a second time with the Start/$\overline{\text{Stop}}$ bit set.

The above method is useful when the entire clock is being corrected. If one location is being updated the clock need not be stopped since this will reset the prescaler, and time will be lost. An ideal example of this is correcting the hours for daylight savings time. To write to the clock "on the fly" the best method is to wait for the 1/100 of a second periodic interrupt. Then wait an additional 16 μs, and then write the data to the clock.

PRESCALER/OSCILLATOR FUNCTIONAL DESCRIPTION

Feeding the counter chain is a programmable prescaler which divides the crystal oscillator frequency to 32 kHz and further to 100 Hz for the counter chain (see *Figure 3*). The crystal frequency that can be selected are: 32 kHz, 32.768 kHz, 4.9152 MHz, and 4.194304 MHz.

Once 32 kHz is generated it feeds both timers and the clock. The clock and timer prescalers can be independently enabled by controlling the timer or clock Start/$\overline{\text{Stop}}$ bits.

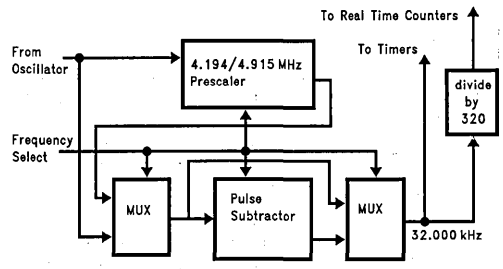

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FIGURE 3. Programmable Clock Prescaler Block

Functional Description (Continued)

The oscillator is programmed via the Real Time Mode Register to operate at various frequencies. The crystal oscillator is designed to offer optimum performance at each frequency. Thus, at 32.768 kHz the oscillator is configured as a low frequency and low power oscillator. At the higher frequencies the oscillator inverter is reconfigured. In addition to the inverter, the oscillator feedback bias resistor is included on chip, as shown in *Figure 4*. The oscillator input may be driven from an external source if desired. Refer to test mode application note for details. The oscillator stability is enhanced through the use of an on chip regulated power supply.

The typical range of trimmer capacitor (as shown in Oscillator Circuit Diagram *Figure 4*, and in the typical application) at the oscillator input pin is suggested only to allow accurate tuning of the oscillator. This range is based on a typical printed circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases, the **load capacitance** specified by the crystal manufacturer (nominal value 11 pF for the 32.768 crystal) is what determines proper oscillation. This load capcitance is the series combination of capacitance on each side of the crystal (with respect to ground).

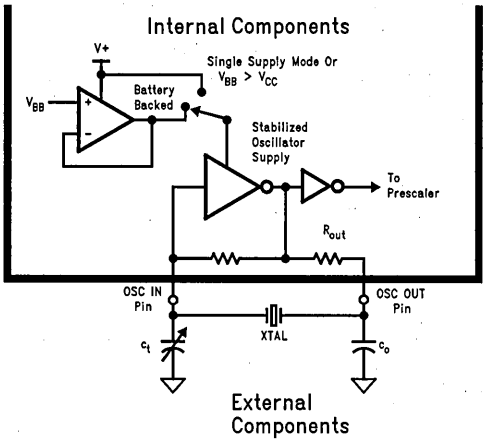

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FIGURE 4. Oscillator Circuit Diagram

XTAL	C_o	C_t	R_{OUT} (Switched Internally)
32/32.768 kHz	47 pF	2 pF–22 pF	150 kΩ to 350 kΩ
4.194304 MHz	68 pF	0 pF–80 pF	500Ω to 900Ω
4.9152 MHz	68 pF	29 pF–49 pF	500Ω to 900Ω

INTERRUPT LOGIC FUNCTIONAL DESCRIPTION

The TCP has the ability to coordinate processor timing activities. To enhance this, an interrupt structure has been implemented which enables several types of events to cause interrupts. Interrupts are controlled via two Control Registers in block 1 and two Status Registers in block 0. (See Register Description for notes on paging and also *Figure 5* and Table I.)

The interrupts are enabled by writing a one to the appropriate bits in Interrupt Control Register 0 and/or 1. Any of the interrupts can be routed to either the INTR pin or the MFO pin, depending on how the Interrupt Routing register is programmed. This, for example, enables the user to dedicate the MFO as a non-maskable interrupt pin to the CPU for power failure detection and enable all other interrupts to appear on the INTR pin. The polarity for the active interrupt can be programmed in the Output Mode Register for either active high or low, and open drain or push pull outputs.

TABLE I. Registers that are Applicable to Interrupt Control

Register Name	Register Select	Page Select	Address
Main Status Register	X	X	00H
Periodic Flag Register	0	0	03H
Interrupt Routing Register	0	0	04H
Interrupt Control Register 0	1	0	03H
Interrupt Control Register 1	1	0	04H
Output Mode Register	1	0	02H

The Interrupt Status Flag D0, in the Main Status Register, indicates the state of INTR and MFO outputs. It is set when either output becomes active and is cleared when all TCP interrupts have been cleared and no further interrupts are pending (i.e., both INTR and MFO are returned to their inactive state). This flag enables the TCP to be rapidly polled by the μP to determine the source of an interrupt in a wired—OR interrupt system.

Note that the Interrupt Status Flag will only monitor the state of the MFO output if it has been configured as an interrupt output (see Output Mode Register description). This is true, regardless of the state of the Interrupt Routing Register. Thus the Interrupt Status Flag provides a true reflection of all conditions routed to the external pins.

Status for the interrupts are provided by the Main Status Register and the Periodic Flag Register. Bits D1–D5 of the Main Status Register are the main interrupt bits.

These register bits will be set when their associated timing events occur. Enabled Alarm or Timer interrupts that occur will set its Main Status Register bit to a one. However, an external interrupt will only be generated if the appropriate Alarm or Timer interrupt enable bits are set (see *Figure 5*).

Disabling the periodic bits will mask the Main Status Register periodic bit, but not the Periodic Flag Register bits. The Power Fail Interrupt bit is set when the interrupt is enabled and a power fail event has occurred, and is not reset until the power is restored. If all interrupt enable bits are 0 no interrupt will be asserted. However, status still can be read from the Main Status Register in a polled fashion (see *Figure 5*).

To clear a flag in bits D2–D5 of the Main Status Register a 1 must be written back into the bit location that is to be cleared. For the Periodic Flag Register reading the status will reset all the periodic flags.

Functional Description (Continued)

Interrupts Fall Into Four Categories:

1. The Timer Interrupts: For description see Timer Section.
2. The Alarm Compare Interrupt: Issued when the value in the time compared RAM equals the counter.
3. The Periodic Interrupts: These are issued at every increment of the specific clock counter signal. Thus, an interrupt is issued every minute, second, etc. Each of these interrupts occurs at the roll-over of the specific counter.
4. The Power Fail Interrupt: Issued upon recognition of a power fail condition by the internal sensing logic. The power failed condition is determined by the signal on the $\overline{\text{PFAIL}}$ pin. The internal power fail signal is gated with the chip select signal to ensure that the power fail interrupt does not lock the chip out during a read or write.

ALARM COMPARE INTERRUPT DESCRIPTON

The alarm/time comparison interrupt is a special interrupt similar to an alarm clock wake up buzzer. This interrupt is generated when the clock time is equal to a value programmed into the alarm compare registers. Up to six bytes can be enabled to perform alarm time comparisons on the counter chain. These six bytes, or some subset thereof, would be loaded with the future time at which the interrupt will occur. Next, the appropriate bits in the Interrupt Control Register 1 are enabled or disabled (refer to detailed description of Interrupt Control Register 1). The TCP then compares these bytes with the clock time. When all the enabled compare registers equal the clock time an alarm interrupt is issued, but only if the alarm compare interrupt is enabled can the interrupt be generated externally. Each alarm compare bit in the Control Register will enable a specific byte for comparison to the clock. Disabling a compare byte is the same as setting its associated counter comparator to an "always equal" state. For example, to generate an interrupt at 3:15 AM of every day, load the hours compare with 0 3 (BCD), the minutes compare with 1 5 (BCD) and the faster counters with 0 0 (BCD), and then disable all other compare registers. So every day when the time rolls over from 3:14:59.99, an interrupt is issued. This bit may be reset by writing a one to bit D3 in the Main Status Register at any time after the alarm has been generated.

If time comparison for an individual byte counter is disabled, that corresponding RAM location can then be used as general purpose storage.

PERIODIC INTERRUPTS DESCRIPTION

The Periodic Flag Register contains six flags which are set by real-time generated "ticks" at various time intervals, see *Figure 5*. These flags constantly sense the periodic signals and may be used whether or not interrupts are enabled. These flags are cleared by any read or write operation performed on this register.

To generate periodic interrupts at the desired rate, the associated Periodic Interrupt Enable bit in Interrupt Control Register 0 must be set. Any combination of periodic interrupts may be enabled to operate simultaneously. Enabled periodic interrupts will now affect the Periodic Interrupt Flag in the Main Status Register. The Periodic Route bit in the Interrupt Routing Register is used to route the periodic interrupt events to either the INTR output or the MFO output.

When a periodic event occurs, the Periodic Interrupt Flag in the Main Status Register is set, causing an interrupt to be generated. The μP clears both flag and interrupt by writing a "1" to the Periodic Interrupt Flag. The individual flags in the periodic Interrupt Flag Register do not require clearing to cancel the interrupt.

If all periodic interrupts are disabled and a periodic interrupt is left pending (i.e., the Periodic Interrupt Flag is still set), the Periodic Interrupt Flag will still be required to be cleared to cancel the pending interrupt.

POWER FAIL INTERRUPTS DESCRIPTION

The Power Fail Status Flag in the Main Status Register monitors the state of the internal power fail signal. This flag may be interrogated by the μP, but it cannot be cleared; it is cleared automatically by the TCP when system power is restored. To generate an interrupt when the power fails, the Power Fail Interrupt Enable bit in Interrupt Control Register 1 is set.

The Power Fail Route bit determines which output the interrupt will appear on. Although this interrupt may not be cleared, it may be masked by clearing the Power Fail Interrupt Enable bit.

POWER FAILURE CIRCUITRY FUNCTIONAL DESCRIPTION

Since the clock must be operated from a battery when the main system supply has been turned off, the LV8571A provides circuitry to simplify design in battery backed systems. This circuitry switches over to the back up supply, and isolates the LV8571A from the host system. *Figure 6* shows a simplified block diagram of this circuitry, which consists of three major sections; 1) power loss logic: 2) battery switch over logic: and 3) isolation logic.

Detection of power loss occurs when $\overline{\text{PFAIL}}$ is low. Debounce logic provides a 30 μs–63 μs debounce time, which will prevent noise on the $\overline{\text{PFAIL}}$ pin from being interpreted as a system failure. After 30 μs–63 μs the debounce logic times out and a signal is generated indicating that system power is marginal and is failing. The Power Fail Interrupt will then be generated.

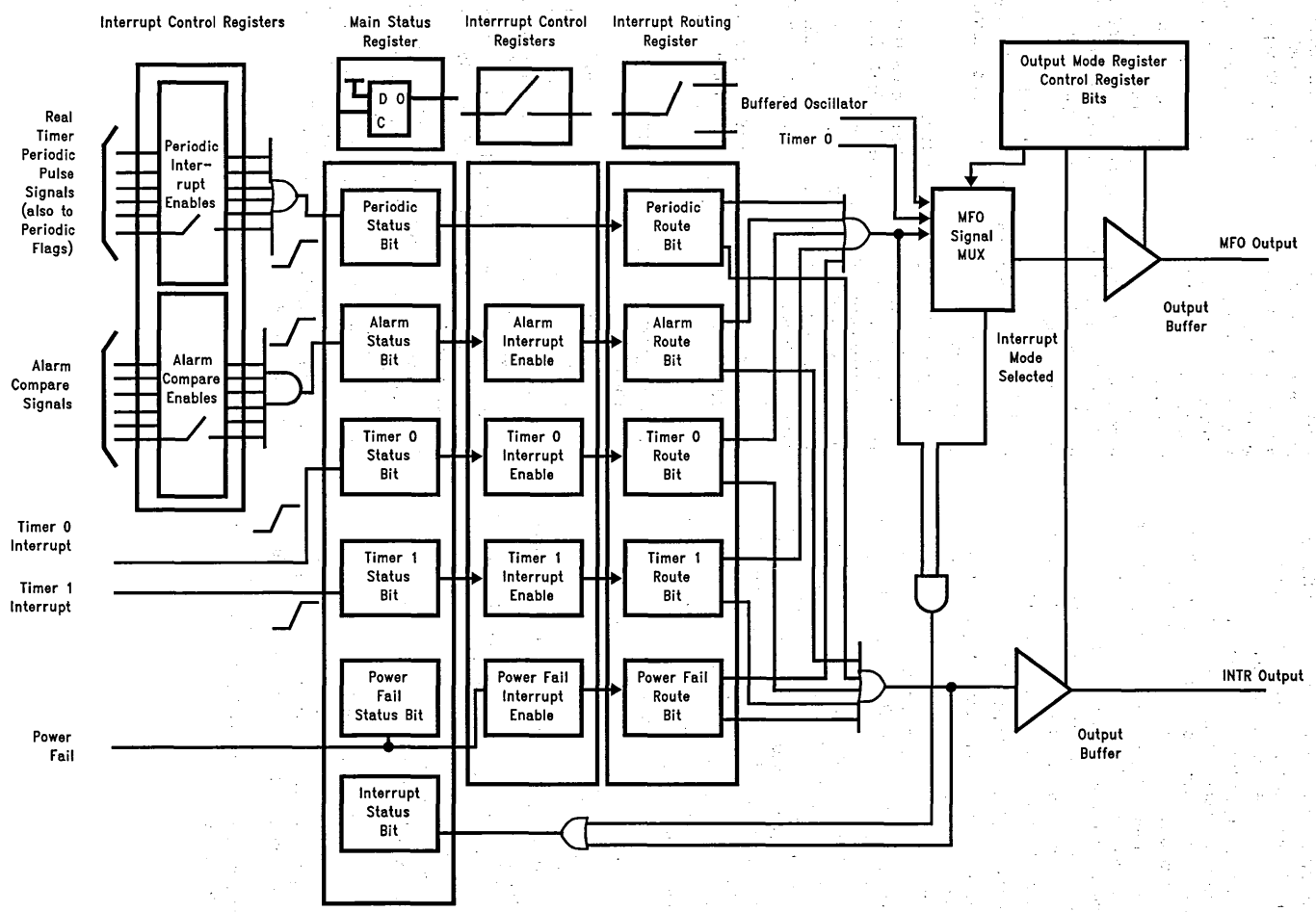

FIGURE 5. Interrupt Control Logic Overview

Functional Description (Continued)

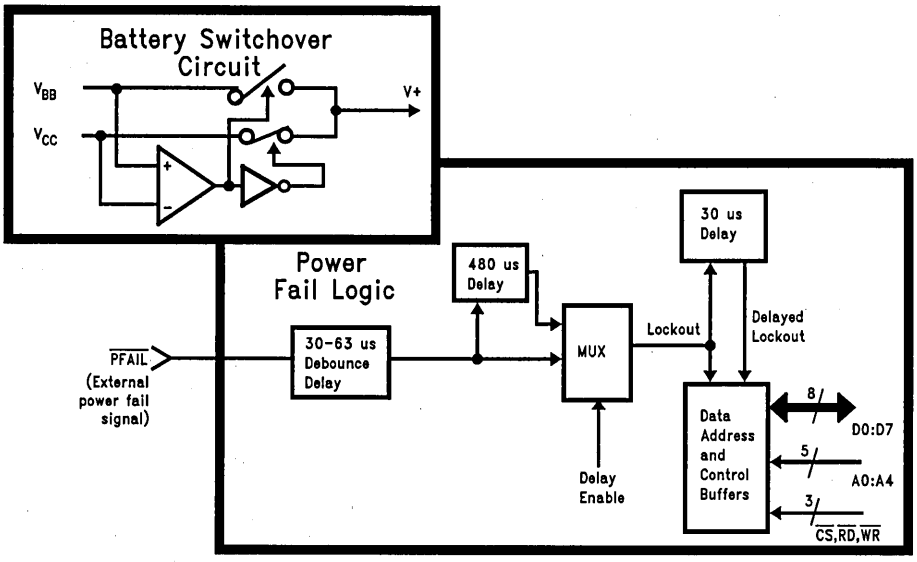

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FIGURE 6. System-Battery Switchover (Upper Left), Power Fail and Lock-Out Circuits (Lower Right)

The user may choose to have this power failed signal lock-out the TCP's data bus within 30 μs min/63 μs max or to delay the lock-out to enable μP access after power failure is detected. This delay is enabled by setting the delay enable bit in the Routing Register. Also, if the lock-out delay was not enabled the TCP will disconnect itself from the bus within 30 μs min → 63 μs max. If chip select is low when a power failure is detected, a safety circuit will ensure that if a read or write is held active continuously for greater than 30 μs after the power fail signal is asserted, the lock-out will be forced. If a lock-out delay is enabled, the LV8571A will remain active for 480 μs after power fail is detected. This will enable the μP to perform last minute bookkeeping before total system collapse. When the host CPU is finished accessing the TCP it may force the bus lock-out before 480 μs has elapsed by resetting the delay enable bit.

The battery switch over circuitry is completely independent of the $\overline{PFAIL}$ pin. A separate circuit compares V_{CC} to the V_{BB} voltage. As the main supply fails, the TCP will continue to operate from the V_{CC} pin until V_{CC} falls below the V_{BB} voltage. At this time, the battery supply is switched in, V_{CC} is disconnected, and the device is now in the standby mode. If indeterminate operation of the battery switch over circuit is to be avoided, then the voltage at the V_{CC} pin must not be allowed to equal the voltage at the V_{BB} pin.

After the generation of a lock-out signal, and eventual switch in of the battery supply, the pins of the TCP will be configured as shown in Table II. Outputs that have a pull-up resistor should be connected to a voltage no greater than V_{BB}.

TABLE II. Pin Isolation during a Power Failure

Pin	$\overline{PFAIL}$ = Logic 0	Standby Mode $V_{BB} > V_{CC}$
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$	Locked Out	Locked Out
A0–A4	Locked Out	Locked Out
D0–D7	Locked Out	Locked Out
Oscillator	Not Isolated	Not Isolated
$\overline{PFAIL}$	Not Isolated	Not Isolated
INTR, MFO	Not Isolated	Open Drain

The Timer and Interrupt Power Fail Operation bits in the Real-Time Mode Register determine whether or not the timers and interrupts will continue to function after a power fail event.

As power returns to the system, the battery switch over circuit will switch back to V_{CC} power as soon as it becomes greater than the battery voltage. The chip will remain in the locked out state as long as $\overline{PFAIL}$ = 0. When $\overline{PFAIL}$ = 1

Functional Description (Continued)

the chip is unlocked, but only after another 30 μs min → 63 μs max debounce time. The system designer must ensure that his system is stable when power has returned.

The power fail circuitry contains active linear circuitry that draws supply current from V_{CC}. In some cases this may be undesirable, so this circuit can be disabled by masking the power fail interrupt. The power fail input can perform all lock-out functions previously mentioned, except that no external interrupt will be issued. Note that the linear power fail circuitry is switched off automatically when using V_{BB} in standby mode.

LOW BATTERY, INITIAL POWER ON DETECT, AND POWER FAIL TIME SAVE

There are three other functions provided on the LV8571A to ease power supply control. These are an initial Power On detect circuit, which also can be used as a time keeping failure detect, a low battery detect circuit, and a time save on power failure.

On initial power up the Oscillator Fail Flag will be set to a one and the real time clock start bit reset to a zero. This indicates that an oscillator fail event has occurred, and time keeping has failed.

The Oscillator Fail flag will not be reset until the real-time clock is started. This allows the system to discriminate between an initial power-up and recovery from a power failure. If the battery backed mode is selected, then bit D6 of the Periodic Flag Register must be written low. This will not affect the contents of the Oscillator Fail Flag.

Another status bit is the low battery detect. This bit is set only when the clock is operating under the V_{CC} pin, and when the battery voltage is determined to be less than 2.1V (typical). When the power fail interrupt enable bit is low, it disables the power fail circuit and will also shut off the low battery voltage detection circuit as well.

To relieve CPU overhead for saving time upon power failure, the Time Save Enable bit is provided to do this automatically. (See also Reading the Clock: Latched Read.) The Time Save Enable bit, when set, causes the Time Save RAM to follow the contents of the clock. This bit can be reset by software, but if set before a power failure occurs, it will automatically be reset when the clock switches to the battery supply (not when a power failure is detected by the $\overline{PFAIL}$ pin). Thus, writing a one to the Time Save bit enables both a software write or power fail write.

SINGLE POWER SUPPLY APPLICATIONS

The LV8571A can be used in a single power supply application. To achieve this, the V_{BB} pin must be connected to ground, and the power connected to V_{CC} and $\overline{PFAIL}$ pins. The Oscillator Failed/Single Supply bit in the Periodic Flag Register should be set to a logic 1, which will disable the oscillator battery reference circuit. The power fail interrupt should also be disabled. This will turn off the linear power fail detection circuits, and will eliminate any quiescent power drawn through these circuits. Until the crystal select bits are initialized, the LV8571A may consume about 50 μA due to arbitrary oscillator selection at power on.

(This extra 50 μA is not consumed if the battery backed mode is selected).

TIMER FUNCTIONAL DESCRIPTION

The LV8571A contains 2 independent multi-mode timers. Each timer is composed of a 16-bit negative edge triggered binary down counter and associated control. The operation is similar to existing μP peripheral timers except that several features have been enhanced. The timers can operate in four modes, and in addition, the input clock frequency can be selected from a prescaler over a wide range of frequencies. Furthermore, these timers are capable of generating interrupts and the Timer 0 output signal is available as a hardware output via the MFO pin. Timer 1 output, however, is not available as a hardware output signal. Both the interrupt and MFO outputs are fully programmable active high, or low, open drain, or push-pull.

Figure 7 shows the functional block diagram of one of the timers. The timer consists of a 16-bit counter, two 8-bit input registers, two 8-bit output registers, clock prescaler, mode control logic, and output control logic. The timer and the data registers are organized as two bytes for each timer. Under normal operations a read/write to the timer locations will read or write to the data input register. The timer contents can be read by setting the counter Read bit (RD) in the timer control register.

TIMER INITIALIZATION

The timer's operation is controlled by a set of registers, as listed in Table III. These consist of 2 data input registers and one control register per timer. The data input registers contain the timers count down value. The Timer Control Register is used to set up the mode of operation and the input clock rate. The timer related interrupts can be controlled by programming the Interrupt Routing Register and Interrupt Control Register 0. The timer outputs are configured by the Output Mode Register.

TABLE III. Timer Associated Registers

Register Name	Register Select	Page Select	Address
Timer 0 Data MSB	X	0	10H
Timer 0 Data LSB	X	0	0FH
Timer 0 Control Register	0	0	01H
Timer 1 Data MSB	X	0	12H
Timer 1 Data LSB	X	0	11H
Timer 1 Control Register	0	0	02H
Interrupt Routing Register	0	0	04H
Interrupt Control Reg. 0	1	0	03H
Output Mode Register	1	0	02H

All these registers must be initialized prior to starting the timer(s). The Timer Control Register should first be set to select the timer mode with the timer start/$\overline{stop}$ bit reset. Then when the timer is to be started the control register should be rewritten identically but with the start/$\overline{stop}$ bit set.

TIMER OPERATION

Each timer is capable of operation in one of four modes. As mentioned, these modes are programmed in each timer's Control Register which is described later. All four modes operate in a similar manner. They operate on the two 8-bit data words stored into the Data Input Register. At the beginning of a counting cycle the 2 bytes are loaded into the timer and the timer commences counting down towards zero. The exact action taken when zero is reached depends on the mode selected, but in general, the timer output will change state, and an interrupt will be generated if the timer interrupts are unmasked.

Functional Description (Continued)

INPUT CLOCK SELECTION

The input frequency to the timers may be selected. Each timer has a prescaler that gives a wide selection of clocking rates. Table IV shows the range of programmable clocks available and the corresponding setting in the Timer Control Register. Note that the output of Timer 1 may be used as the input to Timer 0. This is a cascade option for the timers and allows them to be clocked as a 32-bit down counter.

TABLE IV. Programmable Timer Input Clocks

C2	C1	C0	Selected Clock
0	0	0	Timer 1 Output
0	0	1	Crystal Oscillator
0	1	0	(Crystal Oscillator)/4
0	1	1	93.5 μs (10.7 kHz)
1	0	0	1 ms (1 kHz)
1	0	1	10 ms (100 Hz)
1	1	0	1/10 Second (10 Hz)
1	1	1	1 Second (1 Hz)

Note that the second and third selections are not fixed frequencies, but depend on the crystal oscillator frequency chosen.

Since the input clock frequencies are usually running asynchronously to the timer Start/$\overline{\text{Stop}}$ control bit, a 1 clock cycle error may result. This error results when the Start/Stop occurs just after the clock edge (max error). To minimize this error on all clocks an independent prescaler is used for each timer and is designed so that its Start/Stop error is less than 1 clock cycle.

The count hold/gate bit in the Timer Control Register can be used to suspend the timer operation in modes 0, 1, and 2 (in mode 3 it is the trigger input). Suspending the timer causes the same synchronization error that starting the timer does. The range of errors is specified in Table V.

TABLE V. Maximum Synchronization Errors

Clock Selected	Error
External	+ Ext. Clock Period
Crystal	+ 1 Crystal Clock Period
Crystal/4	+ 1 Crystal Clock Period
10.7 kHz	+ 32 μs
1 kHz	+ 32 μs
100 Hz	+ 32 μs
10 Hz	+ 32 μs
1 Hz	+ 32 μs

MODES OF OPERATION

Bits M0 and M1 in the Timer Control Registers are used to specify the modes of operation. The mode selection is described in Table VI.

TABLE VI. Programmable Timer Modes of Operation

M1	M0	Function	Modes
0	0	Single Pulse Generator	Mode 0
0	1	Rate Generator, Pulse Output	Mode 1
1	0	Square Wave Output	Mode 2
1	1	Retriggerable One Shot	Mode 3

MODE 0: SINGLE PULSE GENERATOR

When the timer is in this mode the output will be initially low if the Timer Start/$\overline{\text{Stop}}$ bit is low (stopped). When this mode is initiated the timer output will go high on the next falling edge of the prescaler's input clock, the contents of the

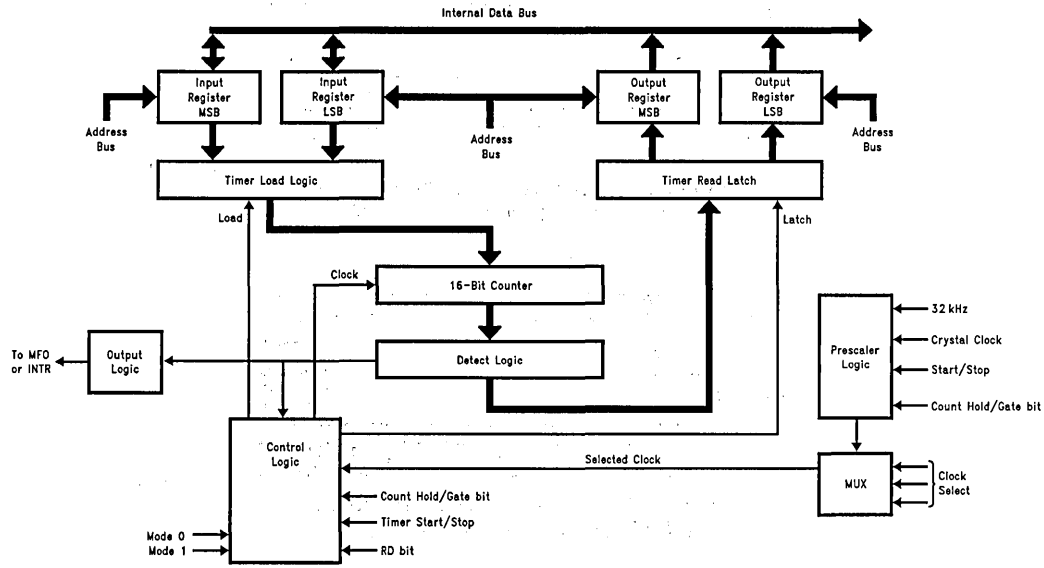

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FIGURE 7. LV8571A Timer Block Diagram

Functional Description (Continued)

input data registers are loaded into the timer. The output will stay high until the counter reaches zero. At zero the output is reset. The result is an output pulse whose duration is equal to the input clock period times the count value (N) loaded into the input data register. This is shown in *Figure 8*.

Pulse Width = Clock Period × N

An interrupt is generated when the zero count is reached. This can be used for one-time interrupts that are set to occur a certain amount of time in the future. In this mode the Timer Start/$\overline{\text{Stop}}$ bit (TSS) is automatically reset upon zero detection. This removes the need to reset TSS before starting another operation.

The count down operation may be temporarily suspended either under software control by setting the Count Hold/Gate bit in the timer register high, or in hardware by setting the G0 or G1 pin high.

The above discussion assumes that the MFO output is programmed to be non-inverting outputs (active high). If the polarity of the output waveform is wrong for the application the polarity can be reversed by configuring the Output Mode Register. The drive configuration can also be programmed to be push pull or open drain.

MODE 1: RATE GENERATOR

When operating in this mode the timer will operate continuously. Before the timer is started its output is low. When the timer is started the input data register contents are loaded into the counter on the negative clock edge and the output is set high (again assuming the Output Mode Register is programmed active high). The timer will then count down to zero. Once the zero count is reached the output goes low for one clock period of the timer clock. Then on the next clock the counter is reloaded automatically and the countdown repeats itself. The output, shown in *Figure 9*, is a waveform whose pulse width and period is determined by N, the input register value, and the input clock period:

Period = (N + 1) (Clock Period)

Pulse Width = Clock Period

Again, the output polarity is controllable as in mode 0. If enabled, an interrupt is generated whenever the zero count is reached. This can be used to generate a periodic interrupt.

MODE 2: SQUARE WAVE GENERATOR

This mode is also cyclic but in this case a square wave rather than a pulse is generated. The output square wave period is determined by the value loaded into the timer input register. This period and the duty cycle are:

Period = 2(N + 1) (Clock Period) Duty Cycle = 0.5

When the timer is stopped the output will be low, and when the Start/$\overline{\text{Stop}}$ bit is set high the timer's counter will be loaded on the next clock falling transition and the output will be set high.

The output will be toggled after the zero count is detected and the counter will then be reloaded, and the cycle will continue. Thus, every N + 1 counts the output gets toggled, as shown in *Figure 10*. Like the other modes the timer operation can be suspended by setting the count hold/gate bit (CHG) in the Timer Control Register. An interrupt will be generated every falling edge of the timer output, if enabled.

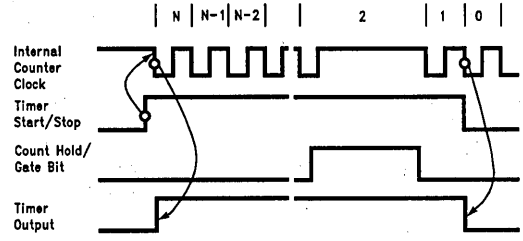

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FIGURE 8. Typical Waveforms for Timer Mode 0 (MFO Output Programmed Active High)

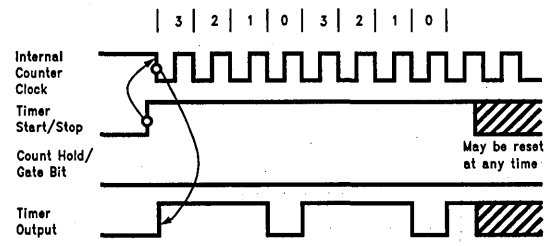

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FIGURE 9. Timing Waveforms for Timer Mode 1 (MFO Output Programmed Active High)

Functional Description (Continued)

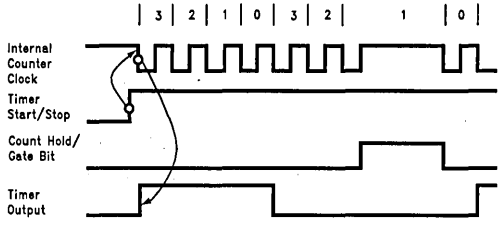

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FIGURE 10. Timing Waveforms for Timer Mode 2 (MFO Output Programmed Active High)

MODE 3: RETRIGGERABLE ONE SHOT

Once the timer Start/$\overline{\text{Stop}}$ bit is set the output stays inactive, and nothing happens until the Count Hold/Gate (CHG) bit is set in the timer control register. When a transition ocurs the one shot output is set active immediately; the counter is loaded with the value in the input register on the next transition of the input clock and the countdown begins. If a retrigger occurs, regardless of the current counter value, the counters will be reloaded with the value in the input register and the counter will be restarted without changing the output state. See *Figure 11*. A trigger count can occur at any time during the count cycle. In this mode the timer will output a single pulse whose width is determined by the value in the input data register (N) and the input clock period.

$$\text{Pulse Width} = \text{Clock Period} \times N$$

The timer will generate an interrupt only when it reaches a count of zero. This timer mode is useful for continuous "watch dog" timing, line frequency power failure detection, etc.

READING THE TIMERS

Normally reading the timer data register addresses, 0FH and 10H for Timer 0 and 11H and 12H for Timer 1 will result in reading the input data register which contains the preset value for the timers. During timer operation it is often useful to read the contents of the 16-bit down counter. This reading may be an erroneous value of FFFFH.

To read a timer, the μP first sets the timer read bit in the appropriate Timer Control Register high. This will cause the counter's contents to be latched to 2–8 bit output registers, and will enable these registers to be read if the μP reads the timer's input data register addresses. On reading the LSB byte the timer read bit is internally reset and subsequent reads of the timer locations will return the input register values.

DETAILED REGISTER DESCRIPTION

There are 5 external address bits: Thus, the host microprocessor has access to 32 locations at one time. An internal switching scheme provides a total of 67 locations.

This complete address space is organized into two pages. Page 0 contains two blocks of control registers, timers, real time clock counters, and special purpose RAM, while page 1 contains general purpose RAM. Using two blocks enables the 9 control registers to be mapped into 5 locations. The only register that does not get switched is the Main Status Register. It contains the page select bit and the register select bit as well as status information.

A memory map is shown in *Figure 2* and register addressing in Table VII. They show the name, address and page locations for the LV8571A.

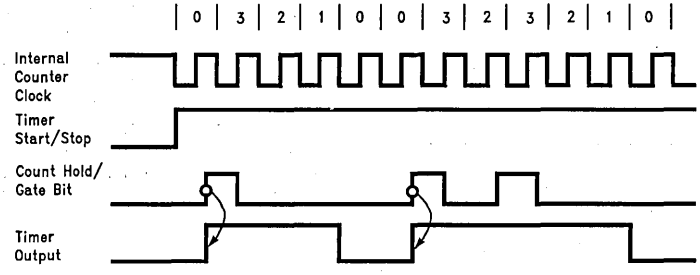

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FIGURE 11. Timing Waveforms for Timer Mode 3, MFO Output Programmed Active High

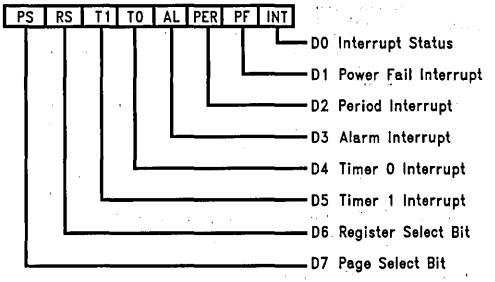
Functional Description (Continued)

TABLE VII. Register/Counter/RAM Addressing for LV8571A

A0-4	PS (Note 1)	RS (Note 2)	Description
CONTROL REGISTERS			
00	X	X	Main Status Register
01	0	0	Timer 0 Control Register
02	0	0	Timer 1 Control Register
03	0	0	Periodic Flag Register
04	0	0	Interrupt Routing Register
01	0	1	Real Time Mode Register
02	0	1	Output Mode Register
03	0	1	Interrupt Control Register 0
04	0	1	Interrupt Control Register 1
COUNTERS (CLOCK CALENDAR)			
05	0	X	1/100, 1/10 Seconds (0-99)
06	0	X	Seconds (0-59)
07	0	X	Minutes (0-59)
08	0	X	Hours (1-12, 0-23)
09	0	X	Days of Month (1-28/29/30/31)
0A	0	X	Months (1-12)
0B	0	X	Years (0-99)
0C	0	X	Julian Date (LSB) (1-99)
0D	0	X	Julian Date (0-3)
0E	0	X	Day of Week (1-7)
TIMER DATA REGISTERS			
0F	0	X	Timer 0 LSB
10	0	X	Timer 0 MSB
11	0	X	Timer 1 LSB
12	0	X	Timer 1 MSB
TIME COMPARE RAM			
13	0	X	Sec Compare RAM (0-59)
14	0	X	Min Compare RAM (0-59)
15	0	X	Hours Compare RAM (1-12, 0-23)
16	0	X	DOM Compare RAM (1-28/29/30/31)
17	0	X	Months Compare RAM (1-12)
18	0	X	DOW Compare RAM (1-7)
TIME SAVE RAM			
19	0	X	Seconds Time Save RAM
1A	0	X	Minutes Time Save RAM
1B	0	X	Hours Time Save RAM
1C	0	X	Day of Month Time Save RAM
1D	0	X	Months Time Save RAM
1E	0	1	RAM
1F	0	X	RAM/Test Mode Register
01-1F	1	X	2nd Page General Purpose RAM

1 PS—Page Select (Bit D7 of Main Status Register)
2 RS—Register Select (Bit D6 of Main Status Register)

MAIN STATUS REGISTER



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The Main Status Register is always located at address 0 regardless of the register block or the page selected.

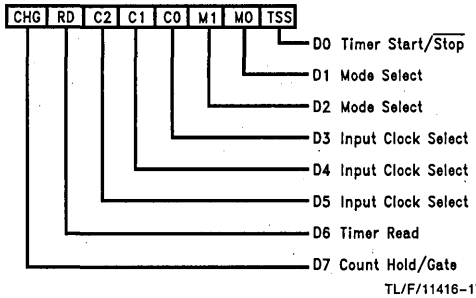
D0: This read only bit is a general interrupt status bit that is taken directly from the interrupt pins. The bit is a one when an interrupt is pending on either the INTR pin or the MFO pin (when configured as an interrupt). This is unlike D3-D5 which can be set by an internal event but may not cause an interrupt. This bit is reset when the interrupt status bits in the Main Status Register are cleared.

D1-D5: These five bits of the Main Status Register are the main interrupt status bits. Any bit may be a one when any of the interrupts are pending. Once an interrupt is asserted the μP will read this register to determine the cause. These interrupt status bits are not reset when read. Except for D1, to reset an interrupt a one is written back to the corresponding bit that is being tested. D1 is reset whenever the $\overline{\text{PFAIL}}$ pin = logic 1. This prevents loss of interrupt status when reading the register in a polled mode. D1, D3-D5 are set regardless of whether these interrupts are masked or not by bits D6 and D7 of Interrupt Control Registers 0 and 1.

D6 and D7: These bits are Read/Write bits that control which register block or RAM page is to be selected. Bit D6 controls the register block to be accessed (see memory map). The memory map of the clock is further divided into two memory pages. One page is the registers, clock and timers, and the second page contains 31 bytes of general purpose RAM. The page selection is determined by bit D7.

Functional Description (Continued)

TIMER 0 AND 1 CONTROL REGISTER



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These registers control the operation of the timers. Each timer has its own register.

D0: This bit will Start (1) or Stop (0) the timer. When the timer is stopped the timer's prescaler and counter are reset, and the timer will restart from the beginning when started again. In mode 0 on time out the TSS bit is internally reset.

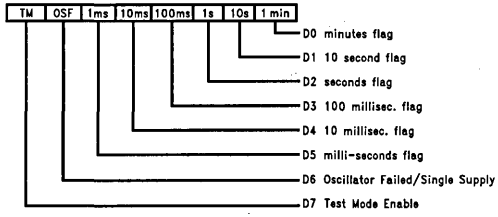
D1 and D2: These control the count mode of the timers. See Table VI.

D3–D5: These bits control which clock signal is applied to the timer's counter input. Refer to Table IV for details.

D6: This is the read bit. If a one is written into this location it will cause the contents of the timer to be latched into a holding register, which can be read by the μP at any time. Reading the least significant byte of the timer will reset the RD bit. The timer read cycle can be aborted by writing RD to zero.

D7: The CHG bit has two mode dependent functions. In modes 0 through 2 writing a one to this bit will suspend the timer operation (without resetting the timer prescaler). However, in mode 3 this bit is used to trigger or re-trigger the count sequence as with the gate pins. If retriggering is desired using the CHG bit, it is not necessary to write a zero to this location prior to the re-trigger. The action of further writing a one to this bit will re-trigger the count.

PERIODIC FLAG REGISTER



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The Periodic Flag Register has the same bit for bit correspondence as Interrupt Control Register 0 except for D6 and D7. For normal operation (i.e., not a single supply application) this register must be written to on initial power up or after an oscillator fail event. D0–D5 are read only bits, D6 and D7 are read/write.

D0–D5: These bits are set by the real time rollover events: (Time Change = 1). The bits are reset when the register is read and can be used as selective data change flags.

D6: This bit performs a dual function. When this bit is read, a one indicates that an oscillator failure has occurred and the time information may have been lost. Some of the ways an oscillator failure can be caused are: failure of the crystal, shorting OSC IN or OSC OUT to GND or V_{CC}, removal of crystal, removal of battery when in the battery backed mode (when a "0" is written to D6), lowering the voltage at the V_{BB} pin to a value less than 2.2V when in the battery backed mode. Bit D6 is automatically set to 1 on initial power-up or an oscillator fail event. The oscillator fail flag is reset by writing a one to the clock start/stop bit in the Real Time Mode Register, with the crystal oscillating.

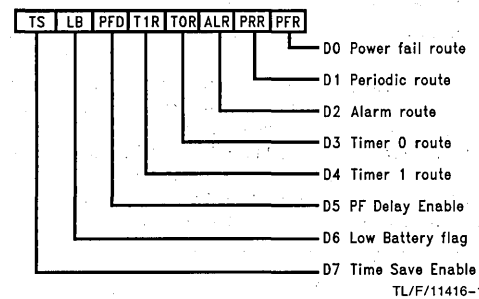
When D6 is written to, it defines whether the TCP is being used in battery backed (normal) or in a single supply mode application. When set to a one this bit configures the TCP for single power supply applications. This bit is automatically set on initial power-up or an oscillator fail event. When set, D6 disables the oscillator reference circuit. The result is that the oscillator is referenced to V_{CC}. When a zero is written to D6 the oscillator reference is enabled, thus the oscillator is referenced to V_{BB}. This allows operation in standard battery standby applications.

At initial power on, if the LV8571A is going to be programmed for battery backed mode, the V_{BB} pin should be connected to a potential in the range of 2.2V to V_{CC}-0.4V.

For single supply mode operation, the V_{BB} pin should be connected to GND and the $\overline{PFAIL}$ pin connected to V_{CC}.

D7: Writing a one to this bit enables the test mode register at location 1F (see Table VII). This bit should be forced to zero during initialization for normal operation. If the test mode has been entered, clear the test mode register before leaving test mode. (See separate test mode application note for further details.)

INTERRUPT ROUTING REGISTER



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D0–D4: The lower 5 bits of this register are associated with the main interrupt sources created by this chip. The purpose of this register is to route the interrupts to either the MFO (multi-function pin), or to the main interrupt pin. When any bit is set the associated interrupt signal will be sent to the MFO pin, and when zero it will be sent to the INTR pin.

Functional Description (Continued)

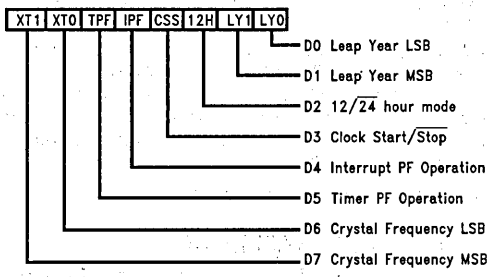
D5: The Delay Enable bit is used when a power fail occurs. If this bit is set, a 480 μs delay is generated internally before the μP interface is locked out. This will enable the μP to access the registers for up to 480 μs after it receives a power fail interrupt. After a power failure is detected but prior to the 480 μs delay timing out, the host μP may force immediate lock out by resetting the Delay Enable bit. Note if this bit is a 0 when power fails then after a delay of 30 μs min/63 μs max the μP cannot read the chip.

D6: This read only bit is set and reset by the voltage at the V_{BB} pin. It can be used by the μP to determine whether the battery voltage at the V_{BB} pin is getting too low. A comparator monitors the battery and when the voltage is lower than 2.1V (typical) this bit is set. The power fail interrupt must be enabled to check for a low battery voltage.

D7: Time Save Enable bit controls the loading of real-time-clock data into the Time Save RAM. When a one is written to this bit the Time Save RAM will follow the corresponding clock registers, and when a zero is written to this bit the time in the Time Save RAM is frozen. This eliminates any synchronization problems when reading the clock, thus negating the need to check for a counter rollover during a read cycle.

This bit must be set to a one prior to power failing to enable the Time Save feature. When the power fails this bit is automatically reset and the time is saved in the Time Save RAM.

REAL TIME MODE REGISTER



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D0–D1: These are the leap year counter bits. These bits are written to set the number of years from the previous leap year. The leap year counter increments on December 31st and it internally enables the February 29th counter state. This method of setting the leap year allows leap year to occur whenever the user wishes to, thus providing flexibility in implementing Japanese leap year function.

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

D2: The count mode for the hours counter can be set to either 24 hour mode or 12 hour mode with AM/PM indicator. A one will place the clock in 12 hour mode.

D3: This bit is the master Start/$\overline{\text{Stop}}$ bit for the clock. When a one is written to this bit the real time counter's prescaler and counter chain are enabled. When this bit is reset to zero the contents of the real time counter is stopped and the prescaler is cleared. When the TCP is initially powered up this bit will be held at a logic 0 until the oscillator starts functioning correctly after which this bit may be modified. If an oscillator fail event occurs, this bit will be reset to logic 0.

D4: This bit controls the operation of the interrupt output in standby mode. If set to a one it allows Alarm, Periodic, and Power Fail interrupts to be functional in standby mode. Timer interrupts will also be functional provided that bit D5 is also set. Note that the MFO and INTR pins are configured as open drain in standby mode.

If bit D4 is set to a zero then interrupt control register 0 and bits D6 and D7 of interrupt control register 1 will be reset when the TCP enters the standby mode. They will have to be re-configured when system (V_{CC}) power is restored.

D5: This bit controls the operation of the timers in standby mode. If set to a one the timers will continue to function when the TCP is in standby mode. The input pins TCK, G0, G1 are locked out in standby mode, and cannot be used.

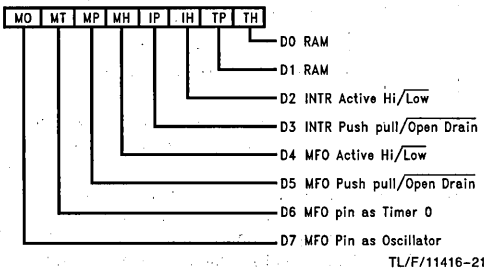
Therefore external control of the timers is not possible in standby mode. Note also that MFO and T1 pins are automatically reconfigured open drain during standby.

D6 and D7: These two bits select the crystal clock frequency as per the following table:

XT1	XT0	Crystal Frequency
0	0	32.768 kHz
0	1	4.194304 MHz
1	0	4.9152 MHz
1	1	32.000 kHz

All bits are Read/Write, and any mode written into this register can be determined by reading the register. On initial power up these bits are random.

OUTPUT MODE REGISTER



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Functional Description (Continued)

D0 and D1: These bits are available as general purpose RAM.

D2: This bit, when set to a one makes the INTR output pin active high, and when set to a zero, it makes this pin active low.

D3: This bit controls whether the INTR pin is an open drain or push-pull output. A one indicates push-pull.

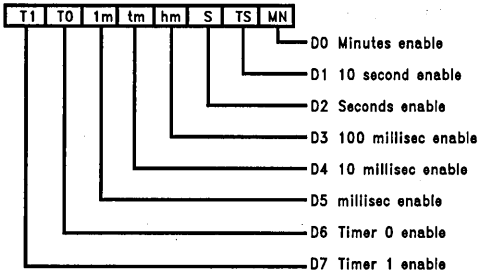
D4: This bit, when set to a one makes the MFO output pin active high, and when set to a zero, it makes this pin active low.

D5: This bit controls whether the MFO pin is an open drain or push-pull output. A one indicates push-pull.

D6 and D7: These bits are used to program the signal appearing at the MFO output, as follows:

D7	D6	MFO Output Signal
0	0	2nd Interrupt
0	1	Timer 0 Waveform
1	X	Buffered Crystal Oscillator

INTERRUPT CONTROL REGISTER 0



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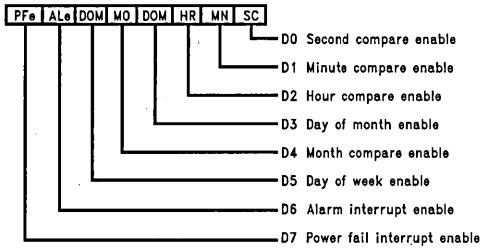
D0–D5: These bits are used to enable one of the selected periodic interrupts by writing a one into the appropriate bit. These interrupts are issued at the rollover of the clock. For example, the minutes interrupt will be issued whenever the minutes counter increments. In all likelihood the interrupt will be enabled asynchronously with the real time change. Therefore, the very first interrupt will occur in less than the periodic time chosen, but after the first interrupt all subsequent interrupts will be spaced correctly. These interrupts are useful when minute, second, real time reading, or task switching is required. When all six bits are written to a 0 this disables periodic interrupts from the Main Status Register and the interrupt pin.

D6 and D7: These are individual timer enable bits. A one written to these bits enable the timers to generate interrupts to the μP.

INTERRUPT CONTROL REGISTER 1



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D0–D5: Each of these bits are enable bits which will enable a comparison between an individual clock counter and its associated compare RAM. If any bit is a zero then that clock-RAM comparator is set to the "always equal" state and the associated TIME COMPARE RAM byte can be used as general purpose RAM. However, to ensure that an alarm interrupt is not generated at bit D3 of the Main Status Register, all bits must be written to a logic zero.

D6: In order to generate an external alarm compare interrupt to the μP from bit D3 of the Main Status Register, this bit must be written to a logic 1.

D7: The MSB of this register is the enable bit for the Power Fail Interrupt. When this bit is set to a one an interrupt will be generated to the μP when $\overline{\text{PFAIL}} = 0$.

This bit also enables the low battery detection analog circuitry.

If the user wishes to mask the power fail interrupt, but utilize the analog circuitry, this bit should be enabled, and the Routing Register can be used to route the interrupt to the MFO pin. The MFO pin can then be left open or configured as the Timer 0 or buffered oscillator output.

Control and Status Register Address Bit Map

Main Status Register PS = 0 RS = 0 ADDRESS = 00H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W[1]	R/W[1]	R/W[1]	R/W[1]	R[2]	R[3]
Page Select	Register Select	Timer 1 Interrupt	Timer 0 Interrupt	Alarm Interrupt	Periodic Interrupt	Power Fail Interrupt	Interrupt Status

1. Reset by writing 1 to bit.
2. Set/reset by voltage at $\overline{PFAIL}$ pin.
3. Reset when all pending interrupts are removed.

Timer 0 Control Register PS = 0 RS = 0 Address = 01H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Timer 1 Control Register PS = 0 RS = 0 Address = 02H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Periodic Flag Register PS = 0 RS = 0 Address = 03H

R/W	R/W[4]	R[5]	R[5]	R[5]	R[5]	R[5]	R[5]
Test Mode	Osc. Fail/ Single Supply	1 ms Flag	10 ms Flag	100 ms Flag	Seconds Flag	10 Second Flag	Minute Flag

4. Read Osc fail Write 0 Batt-Backed Mode Write 1 Single Supply Mode
5. Reset by positive edge of read.

Interrupt Routing Register PS = 0 RS = 0 Address = 04H

R/W	R[6]	R/W	R/W	R/W	R/W	R/W	R/W
Time Save Enable	Low Battery Flag	Power Fail Delay Enable	Timer 1 Int. Route MFO/$\overline{INT}$	Timer 0 Int. Route MFO/$\overline{INT}$	Alarm Int. Route MFO/$\overline{INT}$	Periodic Int. Route MFO/$\overline{INT}$	Power Fail Int. Route MFO/$\overline{INT}$

6. Set and reset by V_{BB} voltage.

Real Time Mode Register PS = 0 RS = 1 Address = 01H

Crystal Freq. XT1	Crystal Freq. XT0	Timers EN on Back-Up	Interrupt EN on Back-Up	Clock Start/$\overline{Stop}$	12/$\overline{24}$ Hr. Mode	Leap Year MSB	Leap Year LSB

All Bits R/W

Output Mode Register PS = 0 RS = 1 Address = 02H

MFO as Crystal	MFO as Timer 0	MFO PP/$\overline{OD}$	MFO Active HI/$\overline{LO}$	INTR PP/$\overline{OD}$	INTR Active HI/$\overline{LO}$	RAM	RAM

All Bits R/W

Interrupt Control Register 0 PS = 0 RS = 1 Address = 03H

Timer 1 Interrupt Enable	Timer 0 Interrupt Enable	1 ms Interrupt Enable	10 ms Interrupt Enable	100 ms Interrupt Enable	Seconds Interrupt Enable	10 Second Interrupt Enable	Minute Interrupt Enable

All Bits R/W

Interrupt Control Register 1 PS = 0 RS = 1 Address = 04H

Power Fail Interrupt Enable	Alarm Interrupt Enable	DOW Interrupt Enable	Month Interrupt Enable	DOM Interrupt Enable	Hours Interrupt Enable	Minute Interrupt Enable	Second Interrupt Enable

All Bits R/W

Application Hints

Suggested initialization procedure for LV8571A in battery backed applications that use the V_{BB} pin.

1. Enter the test mode by writing a 1 to bit D7 in the Periodic Flag Register.
2. Write zero to the RAM/TEST mode Register located in page 0, address HEX 1F.
3. Leave the test mode by writing a 0 to bit D7 in the Periodic Flag Register. Steps 1, 2, 3 guarantee that if the test mode had been entered during power on (due to random pulses from the system), all test mode conditions are cleared. Most important is that the OSC Fail Disable bit is cleared. Refer to AN-589 for more information on test mode operation.
4. After power on (V_{CC} and V_{BB} powered), select the correct crystal frequency bits (D7, D6 in the Real Time Mode Register) as shown in Table 1.

Table 1

Frequency	D7	D6
32.768 KHz	0	0
4.194304 MHz	0	1
4.9152 MHz	1	0
32.0 KHz	1	1

5. Enter a software loop that does the following:

   Set a 3 second(approx) software counter. The crystal oscillator may take 1 second to start.

5.1 Write a 1 to bit D3 in the Real Time Mode Register (try to start the clock). Make sure the crystal select bits remain the same as in step 1. Under normal operation, this bit can be set only if the oscillator is running. During the software loop, RAM, real time counters, output configuration, interrupt control and timer functions may be initialized.

6. Test bit D6 in the Periodic Flag Register:

   IF a 1, go to 5.1 If this bit remains a 1 after 3 seconds, then abort and check hardware. The crystal may be defective or not installed. There may be a short at OSC IN or OSC OUT to V_{CC} or GND, or to some impedance that is less than 10 MΩ.

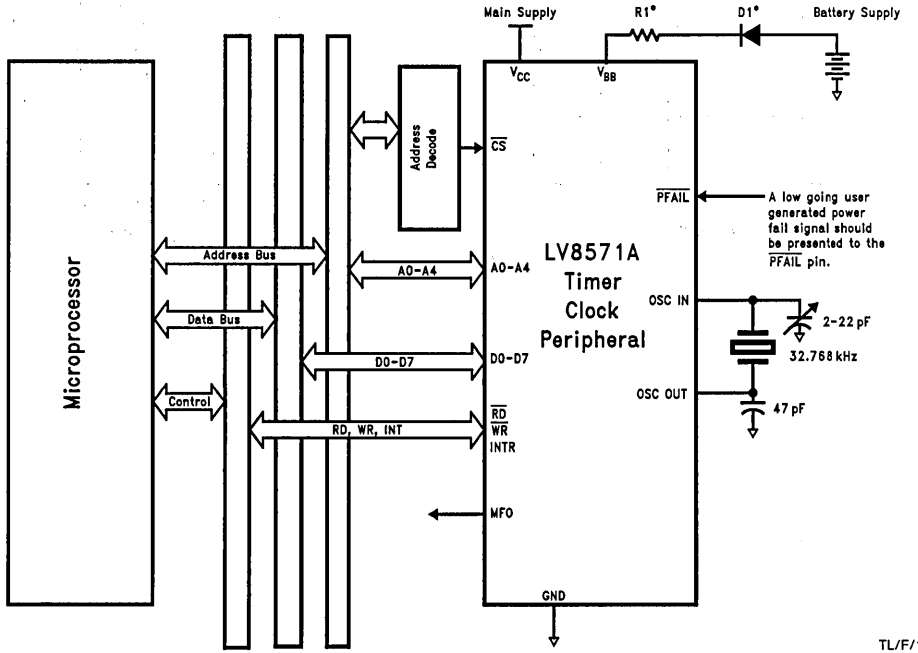
   IF a 0, then the oscillator is running, go to step 7.

7. Write a 0 to bit D6 in the Periodic Flag Register. This action puts the clock chip in the battery backed mode. This mode can be entered only if the OSC fail flag (bit D6 of the Periodic Flag Register) is a 0. Reminder, bit D6 is a dual function bit. When read, D6 returns oscillator status. When written, D6 causes either the Battery Backed Mode, or the Single Supply Mode of operation.

   The only method to ensure the chip is in the battery backed mode is to measure the waveform at the OSC OUT pin. If the battery backed mode was selected successfully, then the peak to peak waveform at OSC OUT is referenced to the battery voltage. If not in battery backed mode, the waveform is referenced to V_{CC}. The measurement should be made with a high impedance low capacitance probe (10 MΩ, 10 pF oscilloscope probe or better). Typical peak to peak swings are within TBD of V_{CC} and ground respectively.

8. Write a 1 to bit D7 of Interrupt Control Register 1. This action enables the PFAIL pin and associated circuitry.
9. Initialize the rest of the chip as needed.

Typical Application



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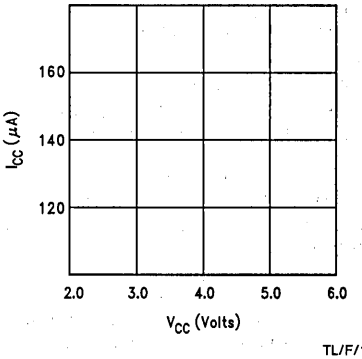
*These components may be necessary to meet UL requirements for lithium batteries. Consult battery manufacturer.

Typical Performance Characteristics

Operating Current vs Supply Voltage (TBD) (Single Supply Mode F_{OSC} = 32.768 kHz)



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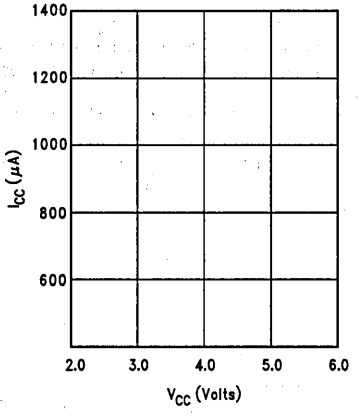
Operating Current vs Supply Voltage (TBD) (Battery Backed Mode F_{OSC} = 32.768 kHz)



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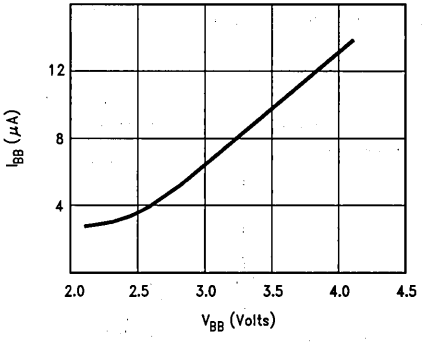
Standby Current vs Power Supply Voltage (F_{OSC} = 32.768 kHz)



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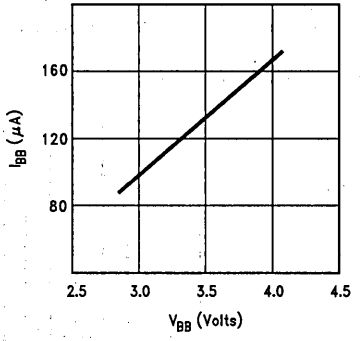
Standby Current vs Power Supply Voltage (F_{OSC} = 4.194304 MHz)



TL/F/11416–28

National Semiconductor

PRELIMINARY

LV8572A Low Voltage Real Time Clock (RTC)

General Description

The LV8572A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports. The address space is organized as 2 software selectable pages of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, and the Time Save RAM. Any of the RAM locations that are not being used for their intended purpose may be used as general purpose CMOS RAM.

Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week, day of month and day of year counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the crystal and two capacitors. The choice of crystal frequency is program selectable.

Power failure logic and control functions have been integrated on chip. This logic is used by the RTC to issue a power fail interrupt, and lock out the µp interface. The time power fails may be logged into RAM automatically when V_{BB} > V_{CC}. Additionally, two supply pins are provided. When V_{BB} > V_{CC}, internal circuitry will automatically switch from the main supply to the battery supply. Status bits are provided to indicate initial application of battery power, system power, and low battery detect. (Continued)

Features

- 3.3V ±10% supply
- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week and day of years counters
  - Four selectable oscillator frequencies
  - Parallel resonant oscillator
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, and power fail interrupts
- Up to 44 bytes of CMOS RAM
- MIL-STD-883C compliant
- SMD #5962-91641-01MJX (future)

Block Diagram

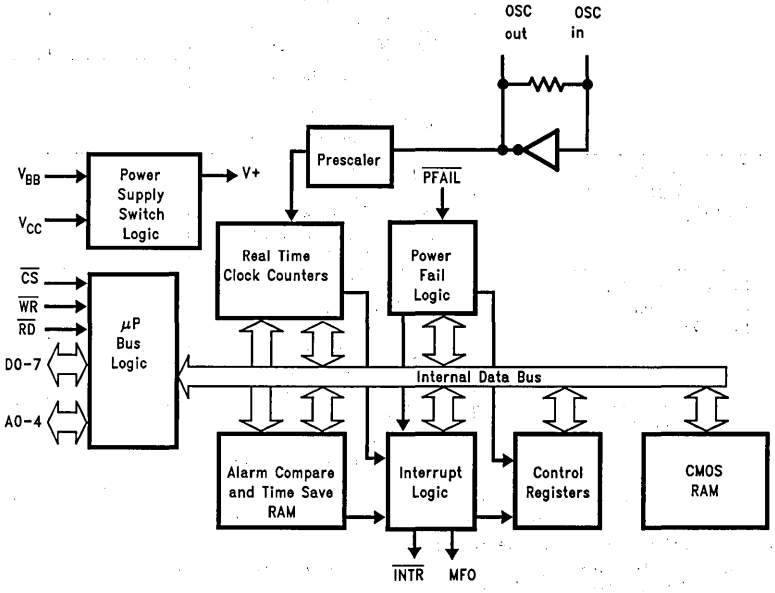


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FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

Specifications for the 883 version of this product are listed separately.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (PD)	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C

Operation Conditions

		Min	Max	Unit
Supply Voltage (V_{CC}) (Note 3)		3.0	3.6	V
Supply Voltage (V_{BB}) (Note 3)		2.2	V_{CC}−0.4	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0.0	V_{CC}	V
Operation Temperature (T_A)		−40	+85	°C
Electr-Static Discharge Rating TBD			1	kV
Typical Values				
θ_{JA} DIP	Board			
	Socket			
θ_{JA} PLCC	Board			80°C/W
	Socket			88°C/W

DC Electrical Characteristics

V_{CC} = 3.3V ±10%, V_{BB} = 2.5V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min (Note 15)	Max (Note 15)	Units
V_{IH}	High Level Input Voltage (Note 4)	Any Inputs Except OSC IN, OSC IN with External Clock	2.0 V_{BB} −0.2	V_{CC} +0.3	V V
V_{IL}	Low Level Input Voltage	All Inputs Except OSC IN OSC IN with External Clock	−0.3 −0.3	0.8 0.2	V V
V_{OH}	High Level Output Voltage (Excluding OSC OUT)	I_{OUT} = −20 μA I_{OUT} = −2.0 mA	V_{CC} −0,2 2.4		V V
V_{OL}	Low Level Output Voltage (Excluding OSC OUT)	I_{OUT} = 20 μA I_{OUT} = 2.0 mA		0.1 0.3	V V
I_{IN}	Input Current (Except OSC IN)	V_{IN} = V_{CC} or GND		±1.0	μA
I_{OZ}	Output TRI-STATE® Current	V_{OUT} = V_{CC} or GND		±5	μA
I_{LKG}	Output High Leakage Current MFO, INTR Pins	V_{OUT} = V_{CC} or GND Outputs Open Drain		±5	μA
I_{CC}	Quiescent Supply Current (Note 7)	F_{OSC} = 32.768 kHz V_{IN} = V_{CC} or GND (Note 5) V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		 200 700 8	 μA μA mA
		F_{OSC} = 4.194304 MHz or 4.9152 MHz V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		 4 6	 mA mA
I_{CC}	Quiescent Supply Current (Single Supply Mode) (Note 7)	V_{BB} = GND V_{IN} = V_{CC} or GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		 20 3	 μA mA
I_{BB}	Standby Mode Battery Supply Current (Note 7)	V_{CC} = GND OSC OUT = open circuit, other pins = GND F_{OSC} = 32.768 kHzμA F_{OSC} = 4.9152 MHz or 4.194304 MHz		 8 400	 μA μA
I_{BLK}	Battery Leakage	2.2V ≤ V_{BB} ≤ 2.6V other pins at GND V_{CC} = GND, V_{BB} = 2.6V V_{CC} = 3.6V, V_{BB} = 2.2V	 −5	 1.5 	 μA μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: For F_{OSC} = 4.194304 or 4.9152 MHz, V_{BB} minimum = 2.8V. In battery backed mode, $V_{BB} \leq V_{CC}$ −0.4V.
Single Supply Mode: Data retention voltage is 2.2V min.
In single Supply Mode (Power connected to V_{CC} pin) 3.0V ≤ V_{CC} ≤ 3.6.

Note 4: This parameter (V_{IH}) is not tested on all pins at the same time.

Note 5: This specification tests I_{CC} with all power fail circuitry disabled, by setting D7 of Interrupt Control Register 1 to 0.

Note 6: This specification tests I_{CC} with all power fail circuitry enabled, by setting D7 of Interrupt Control Register 1 to 1.

Note 7: OSC IN is driven by a signal generator. Contents of the Test Register = 00(H) and the MFO pin is not configured as buffered oscillator out.

AC Electrical Characteristics

V_{CC} = 3.3V ±10%, V_{BB} = 2.5V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Min (Note 15)	Max (Note 15)	Units
READ TIMING				
t_{AR}	Address Valid Prior to Read Strobe	10		ns
t_{RW}	Read Strobe Width (Note 8)	80		ns
t_{CD}	Chip Select to Data Valid Time		80	ns
t_{RAH}	Address Hold after Read (Note 9)	0		ns
t_{RD}	Read Strobe to Valid Data		70	ns
t_{DZ}	Read or Chip Select to TRI-STATE		70	ns
t_{RCH}	Chip Select Hold after Read Strobe (Note 9)	0		ns
t_{DS}	Minimum Inactive Time between Read or Write Accesses	40		ns
WRITE TIMING				
t_{AW}	Address Valid before Write Strobe	10		ns
t_{WAH}	Address Hold after Write Strobe (Note 9)	0		ns
t_{CW}	Chip Select to End of Write Strobe	60		ns
t_{WW}	Write Strobe Width (Note 10)	50		ns
t_{DW}	Data Valid to End of Write Strobe	40		ns
t_{WDH}	Data Hold after Write Strobe (Note 9)	2		ns
t_{WCH}	Chip Select Hold after Write Strobe (Note 9)	0		ns
INTERRUPT TIMING				
t_{ROLL}	Clock Rollover to $\overline{INTR}$ Out is Typically 20 μs			

Note 8: Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

Note 9: Hold time is guaranteed by design but not production tested. This limit is not used to calculate outgoing quality levels.

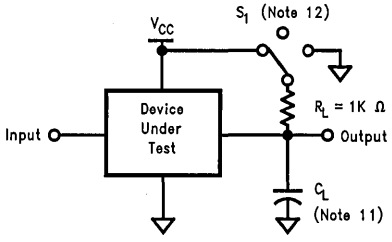
Note 10: Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns (10%–90%)
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels (Note 12)	Active High +0.5V Active Low −0.5V

Note 11: C_L = 100 pF, includes jig and scope capacitance.

Note 12: S1 = V_{CC} for active low to high impedance measurements.
S1 = GND for active high to high impedance measurements.
S1 = open for all other timing measurements.



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Capacitance (T_A = 25°C, f = 1 MHz)

Symbol	Parameter (Note 13)	Typ	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	7	pF

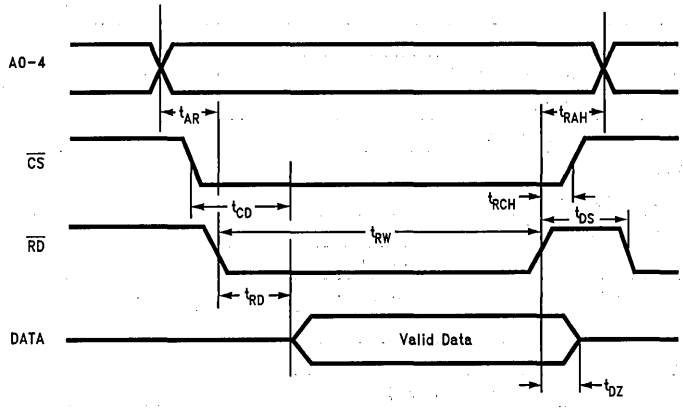
Note 13: This parameter is not 100% tested.

Note 14: Output rise and fall times 25 ns max (10%–90%) with 100 pF load.

Note 15: Room temperature values only.

Timing Waveforms

Read Timing Diagram



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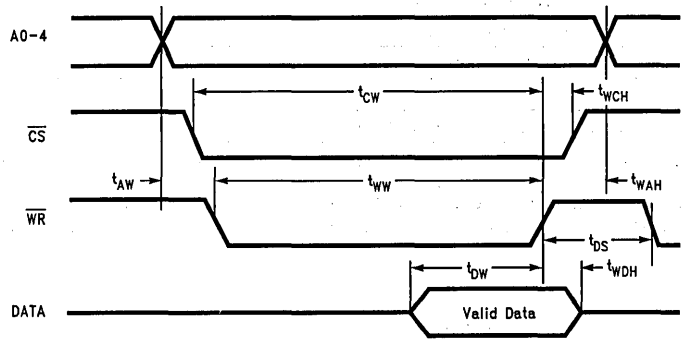
Write Timing Diagram



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General Description (Continued)

The LV8572A's interrupt structure provides three basic types of interrupts: Periodic, Alarm/Compare, and Power Fail. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

Pin Description

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (Inputs): These pins interface to μP control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and Write pins are also active low and enable reading or writing to the RTC. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.

A0–A4 (Inputs): These 5 pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.

OSC IN (Input); OSC OUT (Output): These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}, and the correct crystal select bits in the Real Time Mode Register have been set.

MFO (Output): The multi-function output can be used as a second interrupt output for interrupting the μP. This pin can also provide an output for the oscillator. The MFO output is configured as push-pull, active high for normal or single power supply operation and as an open drain during stand-by mode ($V_{BB} > V_{CC}$). If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

$\overline{INTR}$ (Output): The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The $\overline{INTR}$ output is permanently configured active low, open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

D0–D7 (Input/Output): These 8 bidirectional pins connect to the host μP's data bus and are used to read from and write to the RTC. When the $\overline{PFAIL}$ pin goes low and a write is not in progress, these pins are at TRI-STATE.

$\overline{PFAIL}$ (Input): In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the RTC goes into a lockout mode, in a minimum of 30 μs or a maximum of 63 μs unless lockout delay is programmed. In the single power supply mode, this pin is not useable as an input and should be tied to V_{CC}. Refer to section on Power Fail Functional Description.

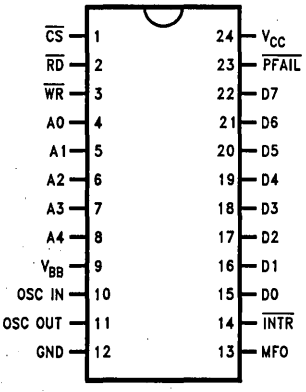
V_{BB} (Battery Power Pin): This pin is connected to a back-up power supply. This power supply is switched to the internal circuitry when the V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the RTC programmed for single power supply only, and power applied to the V_{CC} pin.

V_{CC}: This is the main system power pin.

GND: This is the common ground power pin for both V_{BB} and V_{CC}.

Connection Diagrams

Dual-In-Line



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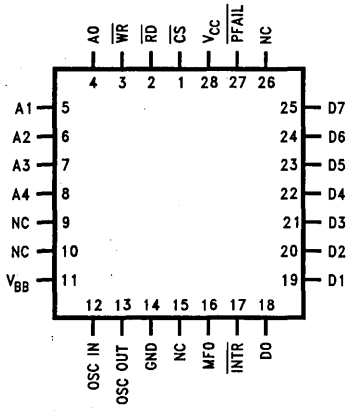
Top View

Order Number LV8572AN
See NS Package Number N24C

Plastic Chip Carrier



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Top View

Order Number LV8572AV
See NS Package Number V28A

Functional Description

The LV8572A contains a fast access real time clock, interrupt control logic, power fail detect logic, and CMOS RAM. All functions of the RTC are controlled by a set of seven registers. A simplified block diagram that shows the major functional blocks is given in *Figure 1*.

The blocks are described in the following sections:

1. Real Time Clock
2. Oscillator Prescaler
3. Interrupt Logic
4. Power Failure Logic
5. Additional Supply Management

The memory map of the RTC is shown in the memory addressing table. The memory map consists of two 31 byte pages with a main status register that is common to both pages. A control bit in the Main Status Register is used to select either page. *Figure 2* shows the basic concept. Page 0 contains all the clock timer functions, while page 1 has scratch pad RAM. The control registers are split into two separate blocks to allow page 1 to be used entirely as scratch pad RAM. Again a control bit in the Main Status Register is used to select either control register block.

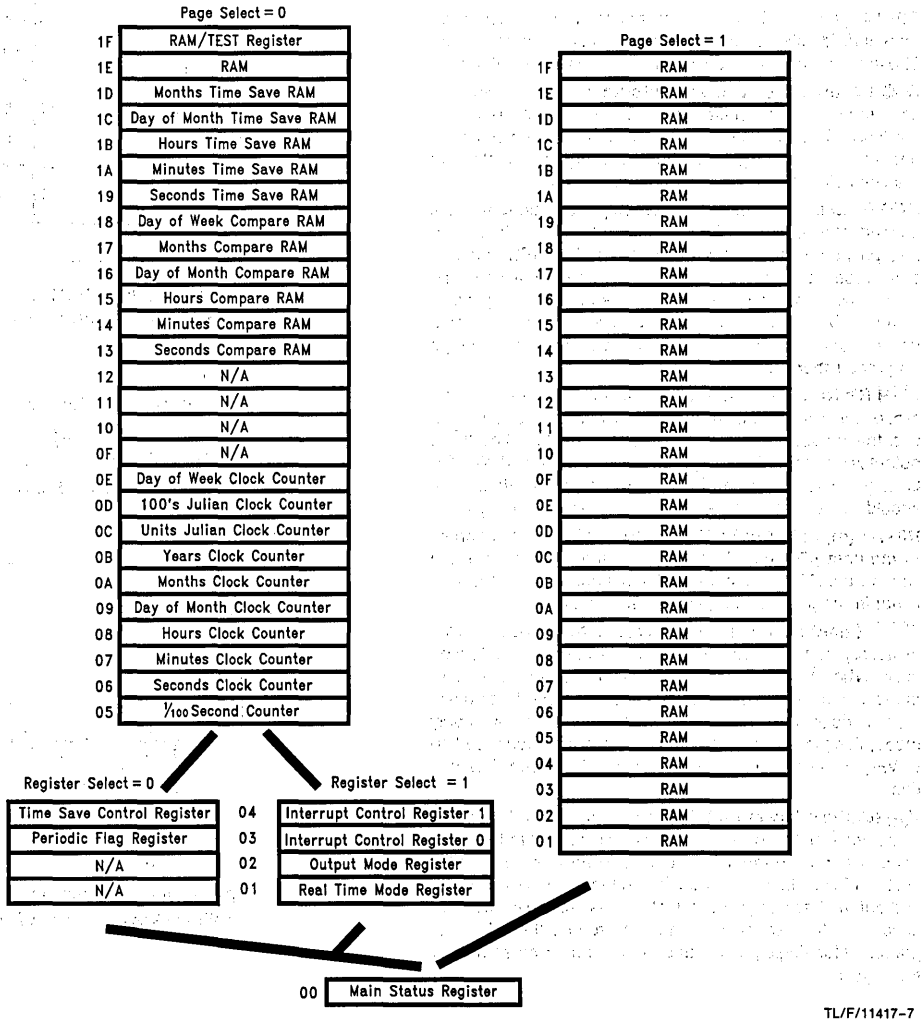

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FIGURE 2. LV8572A Internal Memory Map

Functional Description (Continued)

INITIAL POWER-ON of BOTH V_{BB} and V_{CC}

V_{BB} and V_{CC} may be applied in any sequence. In order for the power fail circuitry to function correctly, whenever power is off, the V_{CC} pin must see a path to ground through a maximum of 1 MΩ. The user should be aware that the control registers will contain random data. The first task to be carried out in an initialization routine is to start the oscillator by writing to the crystal select bits in the Real Time Mode Register. If the LV8572A is configured for single supply mode, an extra 50 μA may be consumed until the crystal select bits are programmed. The user should also ensure that the RTC is not in test mode (see register descriptions).

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

As shown in *Figure 2*, the clock has 10 bytes of counters, which count from 1/100 of a second to years. Each counter counts in BCD and is synchronously clocked. The count sequence of the individual byte counters within the clock is shown later in Table VII. Note that the day of week, day of month, day of year, and month counters all roll over to 1. The hours counter in 12 hour mode rolls over to 1 and the AM/PM bit toggles when the hours rolls over to 12 (AM = 0, PM = 1). The AM/PM bit is bit D7 in the hours counter.

All other counters roll over to 0. Also note that the day of year counter is 12 bits long and occupies two addresses. Upon initial application of power the counters will contain random information.

READING THE CLOCK: VALIDATED READ

Since clocking of the counter occurs asynchronously to reading of the counter, it is possible to read the counter while it is being incremented (rollover). This may result in an incorrect time reading. Thus to ensure a correct reading of the entire contents of the clock (or that part of interest), it must be read without a clock rollover occurring. In general this can be done by checking a rollover bit. On this chip the periodic interrupt status bits can serve this function. The following program steps can be used to accomplish this.

1. Initialize program for reading clock.
2. Dummy read of periodic status bit to clear it.
3. Read counter bytes and store.
4. Read rollover bit, and test it.
5. If rollover occured go to 3.
6. If no rollover, done.

To detect the rollover, individual periodic status bits can be polled. The periodic bit chosen should be equal to the highest frequency counter register to be read. That is if only SECONDS through HOURS counters are read, then the SECONDS periodic bit should be used.

READING THE CLOCK: INTERRUPT DRIVEN

Enabling the periodic interrupt mask bits cause interrupts just as the clock rolls over. Enabling the desired update rate and providing an interrupt service routine that executes in less than 10 ms enables clock reading without checking for a rollover.

READING THE CLOCK: LATCHED READ

Another method to read the clock that does not require checking the rollover bit is to write a one into the Time Save Enable bit (D7) of the Time Save Control Register, and then to write a zero. Writing a one into this bit will enable the clock contents to be duplicated in the Time Save RAM. Changing the bit from a one to a zero will freeze and store the contents of the clock in Time Save RAM. The time then can be read without concern for clock rollover, since internal logic takes care of synchronization of the clock. Because only the bits used by the clock counters will be latched, the Time Save RAM should be cleared prior to use to ensure that random data stored in the unused bits do not confuse the host microprocessor. This bit can also provide time save at power failure, see the Additional Supply Management Functions section. With the Time Save Enable bit at a logical 0, the Time Save RAM may be used as RAM if the latched read function is not necessary.

INITIALIZING AND WRITING TO THE CALENDAR-CLOCK

Upon initial application of power to the RTC or when making time corrections, the time must be written into the clock. To correctly write the time to the counters, the clock would normally be stopped by writing the Start/$\overline{\text{Stop}}$ bit in the Real Time Mode Register to a zero. This stops the clock from counting and disables the carry circuitry. When initializing the clock's Real Time Mode Register, it is recommended that first the various mode bits be written while maintaining the Start/$\overline{\text{Stop}}$ bit reset, and then writing to the register a second time with the Start/$\overline{\text{Stop}}$ bit set.

The above method is useful when the entire clock is being corrected. If one location is being updated the clock need not be stopped since this will reset the prescaler, and time will be lost. An ideal example of this is correcting the hours for daylight savings time. To write to the clock "on the fly" the best method is to wait for the 1/100 of a second periodic interrupt. Then wait an additional 16 μs, and then write the data to the clock.

PRESCALER/OSCILLATOR FUNCTIONAL DESCRIPTION

Feeding the counter chain is a programmable prescaler which divides the crystal oscillator frequency to 32 kHz and further to 100 Hz for the counter chain (see *Figure 3*). The crystal frequency that can be selected are: 32 kHz, 32.768 kHz, 4.9152 MHz, and 4.194304 MHz.

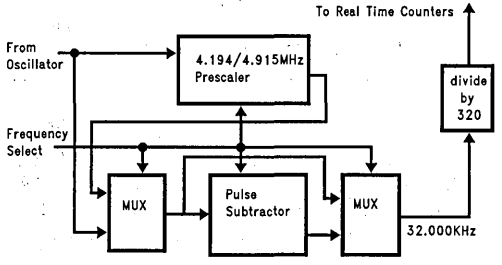

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FIGURE 3. Programmable Clock Prescaler Block

Functional Description (Continued)

The oscillator is programmed via the Real Time Mode Register to operate at various frequencies. The crystal oscillator is designed to offer optimum performance at each frequency. Thus, at 32.768 kHz the oscillator is configured as a low frequency and low power oscillator. At the higher frequencies the oscillator inverter is reconfigured. In addition to the inverter, the oscillator feedback bias resistor is included on chip, as shown in *Figure 4*. The oscillator input may be driven from an external source if desired. Refer to test mode application note for details. The oscillator stability is enhanced through the use of an on chip regulated power supply.

The typical range of trimmer capacitor (as shown in Oscillator Circuit Diagram *Figure 4*, and in the typical application) at the oscillator input pin is suggested only to allow accurate tuning of the oscillator. This range is based on a typical printed circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases, the **load capacitance** specified by the crystal manufacturer (nominal value 11 pF for the 32.768 crystal) is what determines proper oscillation. This load capcitance is the series combination of capacitance on each side of the crystal (with respect to ground).

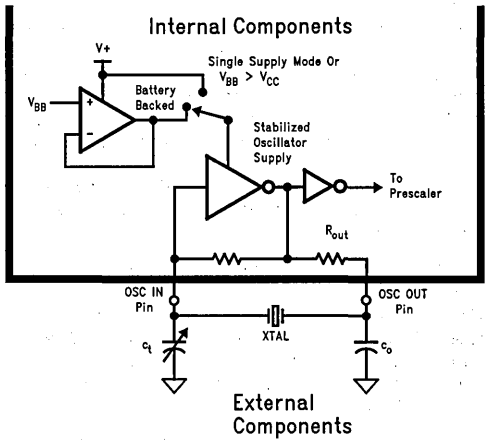

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FIGURE 4. Oscillator Circuit Diagram

XTAL	C_o	C_t	R_{OUT} (Switched Internally)
32/32.768 kHz	47 pF	2 pF–22 pF	150 kΩ to 350 kΩ
4.194304 MHz	68 pF	0 pF–80 pF	500Ω to 900Ω
4.9152 MHz	68 pF	29 pF–49 pF	500Ω to 900Ω

INTERRUPT LOGIC FUNCTIONAL DESCRIPTION

The RTC has the ability to coordinate processor timing activities. To enhance this, an interrupt structure has been implemented which enables several types of events to cause interrupts. Interrupts are controlled via two Control Registers in block 1 and two Status Registers in block 0. (See Register Description for notes on paging and also *Figure 5* and Table I.)

The interrupts are enabled by writing a one to the appropriate bits in Interrupt Control Register 0 and/or 1.

TABLE I. Registers that are Applicable to Interrupt Control

Register Name	Register Select	Page Select	Address
Main Status Register	X	X	00H
Periodic Flag Register	0	0	03H
Interrupt Control Register 0	1	0	03H
Interrupt Control Register 1	1	0	04H
Output Mode Register	1	0	02H

The Interrupt Status Flag D0, in the Main Status Register, indicates the state of INTR and MFO outputs. It is set when either output becomes active and is cleared when all RTC interrupts have been cleared and no further interrupts are pending (i.e., both INTR and MFO are returned to their inactive state). This flag enables the RTC to be rapidly polled by the μP to determine the source of an interrupt in a wired—OR interrupt system. (The Interrupt Status Flag provides a true reflection of all conditions routed to the external pins.)

Status for the interrupts are provided by the Main Status Register and the Periodic Flag Register. Bits D1–D5 of the Main Status Register are the main interrupt bits.

These register bits will be set when their associated timing events occur. Enabled Alarm comparisons that occur will set its Main Status Register bit to a one. However, an external interrupt will only be generated if the Alarm interrupt enable bit is set (see *Figure 5*).

Disabling the periodic interrupts will mask the Main Status Register periodic bit, but not the Periodic Flag Register bits. The Power Fail Interrupt bit is set when the interrupt is enabled and a power fail event has occurred, and is not reset until the power is restored. If all interrupt enable bits are 0 no interrupt will be asserted. However, status still can be read from the Main Status Register in a polled fashion (see *Figure 5*).

To clear a flag in bits D2 and D3 of the Main Status Register a 1 must be written back into the bit location that is to be cleared. For the Periodic Flag Register reading the status will reset all the periodic flags.

Functional Description (Continued)

Interrupts Fall Into Three Categories:

1. The Alarm Compare Interrupt: Issued when the value in the time compared RAM equals the counter.
2. The Periodic Interrupts: These are issued at every increment of the specific clock counter signal. Thus, an interrupt is issued every minute, second, etc. Each of these interrupts occurs at the roll-over of the specific counter.
3. The Power Fail Interrupt: Issued upon recognition of a power fail condition by the internal sensing logic. The power failed condition is determined by the signal on the $\overline{\text{PFAIL}}$ pin. The internal power fail signal is gated with the chip select signal to ensure that the power fail interrupt does not lock the chip out during a read or write.

ALARM COMPARE INTERRUPT DESCRIPTON

The alarm/time comparison interrupt is a special interrupt similar to an alarm clock wake up buzzer. This interrupt is generated when the clock time is equal to a value programmed into the alarm compare registers. Up to six bytes can be enabled to perform alarm time comparisons on the counter chain. These six bytes, or some subset thereof, would be loaded with the future time at which the interrupt will occur. Next, the appropriate bits in the Interrupt Control Register 1 are enabled or disabled (refer to detailed description of Interrupt Control Register 1). The RTC then compares these bytes with the clock time. When all the enabled compare registers equal the clock time an alarm interrupt is issued, but only if the alarm compare interrupt is enabled can the interrupt be generated externally. Each alarm compare bit in the Control Register will enable a specific byte for comparison to the clock. Disabling a compare byte is the same as setting its associated counter comparator to an "always equal" state. For example, to generate an interrupt at 3:15 AM of every day, load the hours compare with 0 3 (BCD), the minutes compare with 1 5 (BCD) and the faster counters with 0 0 (BCD), and then disable all other compare registers. So every day when the time rolls over from 3:14:59.99, an interrupt is issued. This bit may be reset by writing a one to bit D3 in the Main Status Register at any time after the alarm has been generated.

If time comparison for an individual byte counter is disabled, that corresponding RAM location can then be used as general purpose storage.

PERIODIC INTERRUPTS DESCRIPTION

The Periodic Flag Register contains six flags which are set by real-time generated "ticks" at various time intervals, see *Figure 5*. These flags constantly sense the periodic signals and may be used whether or not interrupts are enabled. These flags are cleared by any read or write operation performed on this register.

To generate periodic interrupts at the desired rate, the associated Periodic Interrupt Enable bit in Interrupt Control Register 0 must be set. Any combination of periodic interrupts may be enabled to operate simultaneously. Enabled periodic interrupts will now affect the Periodic Interrupt Flag in the Main Status Register.

When a periodic event occurs, the Periodic Interrupt Flag in the Main Status Register is set, causing an interrupt to be generated. The μP clears both flag and interrupt by writing a "1" to the Periodic Interrupt Flag. The individual flags in the periodic Interrupt Flag Register do not require clearing to cancel the interrupt.

If all periodic interrupts are disabled and a periodic interrupt is left pending (i.e., the Periodic Interrupt Flag is still set), the Periodic Interrupt Flag will still be required to be cleared to cancel the pending interrupt.

POWER FAIL INTERRUPTS DESCRIPTION

The Power Fail Status Flag in the Main Status Register monitors the state of the internal power fail signal. This flag may be interrogated by the μP, but it cannot be cleared; it is cleared automatically by the RTC when system power is restored. To generate an interrupt when the power fails, the Power Fail Interrupt Enable bit in Interrupt Control Register 1 is set. Although this interrupt may not be cleared, it may be masked by clearing the Power Fail Interrupt Enable bit.

POWER FAILURE CIRCUITRY FUNCTIONAL DESCRIPTION

Since the clock must be operated from a battery when the main system supply has been turned off, the LV8572A provides circuitry to simplify design in battery backed systems. This switches over to the back up supply, and isolates itself from the host system. *Figure 6* shows a simplified block diagram of this circuitry, which consists of three major sections; 1) power loss logic: 2) battery switch over logic: and 3) isolation logic.

Detection of power loss occurs when $\overline{\text{PFAIL}}$ is low. Debounce logic provides a 30 μs–63 μs debounce time, which will prevent noise on the $\overline{\text{PFAIL}}$ pin from being interpreted as a system failure. After 30 μs–63 μs the debounce logic times out and a signal is generated indicating that system power is marginal and is failing. The Power Fail Interrupt will then be generated.

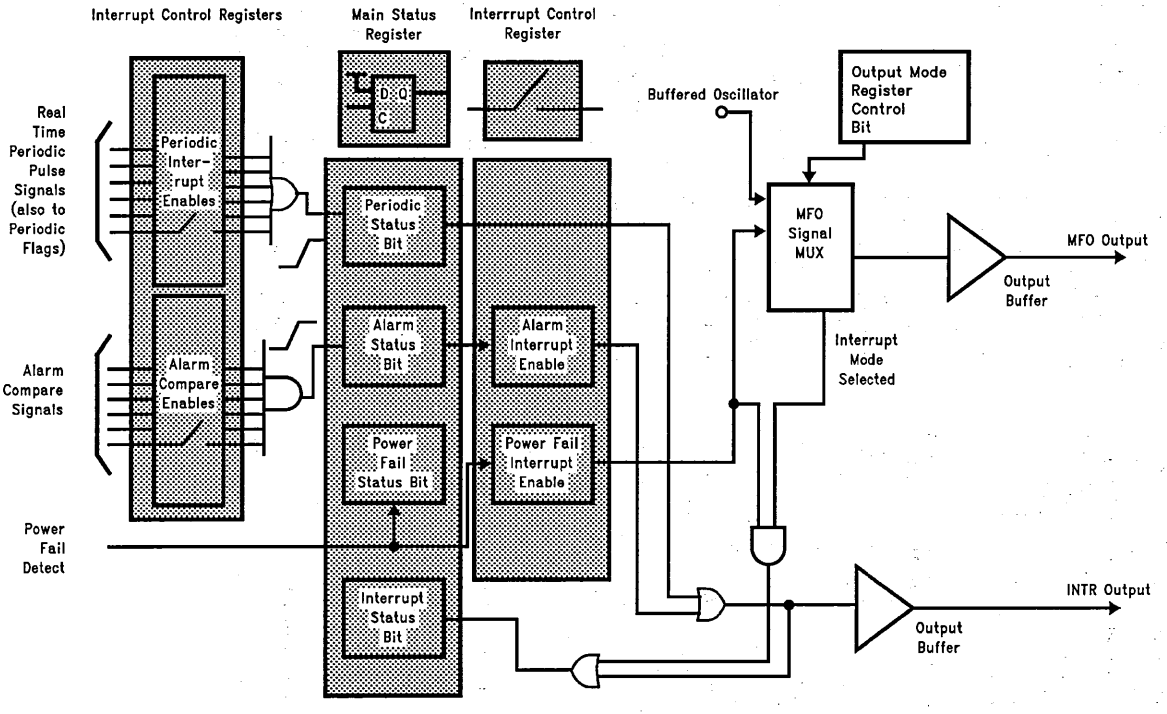

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FIGURE 5. Interrupt Control Logic Overview

Functional Description (Continued)

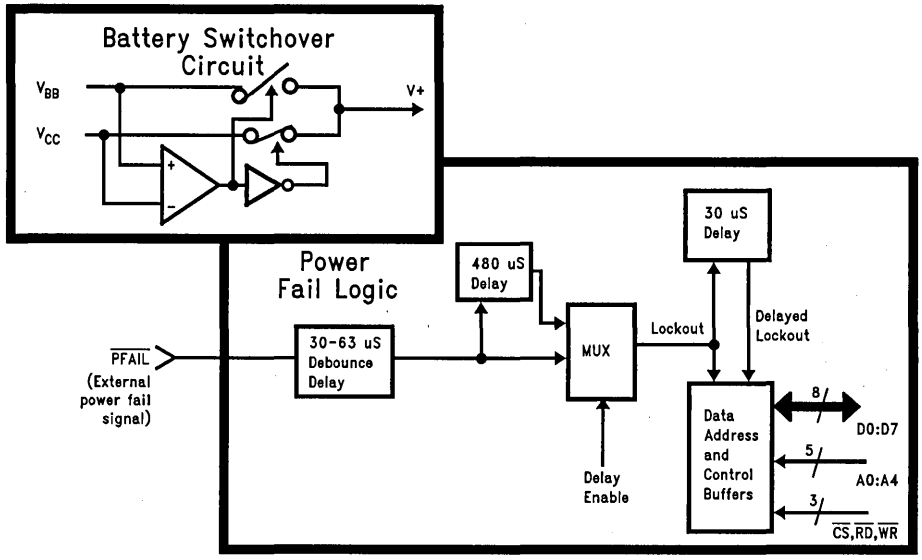

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FIGURE 6. System-Battery Switchover (Upper Left), Power Fail and Lock-Out Circuits (Lower Right)

If chip select is low when a power failure is detected, a safety circuit will ensure that if a read or write is held active continuously for greater than 30 μs after the power fail signal is asserted, the lock-out will be forced. If a lock-out delay is enabled, the LV8572A will remain active for 480 μs after power fail is detected. This will enable the μP to perform last minute bookkeeping before total system collapse. When the host CPU is finished accessing the RTC it may force the bus lock-out before 480 μs has elapsed by resetting the delay enable bit.

The battery switch over circuitry is completely independent of the $\overline{\text{PFAIL}}$ pin. A separate circuit compares V_{CC} to the V_{BB} voltage. As the main supply fails, the RTC will continue to operate from the V_{CC} pin until V_{CC} falls below the V_{BB} voltage. At this time, the battery supply is switched in, V_{CC} is disconnected, and the device is now in the standby mode. If indeterminate operation of the battery switch over circuit is to be avoided, then the voltage at the V_{CC} pin must not be allowed to equal the voltage at the V_{BB} pin.

After the generation of a lock-out signal, and eventual switch in of the battery supply, the pins of the RTC will be configured as shown in Table II. Outputs that have a pull-up resistor should be connected to a voltage no greater than V_{BB}.

TABLE II. Pin Isolation during a Power Failure

Pin	$\overline{\text{PFAIL}}$ = Logic 0	Standby Mode $V_{BB} > V_{CC}$
$\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$	Locked Out	Locked Out
A0–A4	Locked Out	Locked Out
D0–D7	Locked Out	Locked Out
Oscillator	Not Isolated	Not Isolated
$\overline{\text{PFAIL}}$	Not Isolated	Not Isolated
INTR, MFO	Not Isolated	Open Drain

The Interrupt Power Fail Operation bit in the Real-Time Mode Register determine whether or not the interrupts will continue to function after a power fail event.

As power returns to the system, the battery switch over circuit will switch back to V_{CC} power as soon as it becomes greater than the battery voltage. The chip will remain in the locked out state as long as $\overline{\text{PFAIL}}$ = 0. When $\overline{\text{PFAIL}}$ = 1

3

Functional Description (Continued)

the chip is unlocked, but only after another 30 μs min → 63 μs max debounce time. The system designer must ensure that his system is stable when power has returned.

The power fail circuitry contains active linear circuitry that draws supply current from V_{CC}. In some cases this may be undesirable, so this circuit can be disabled by masking the power fail interrupt. The power fail input can perform all lock-out functions previously mentioned, except that no external interrupt will be issued. Note that the linear power fail circuitry is switched off automatically when using V_{BB} in standby mode.

LOW BATTERY, INITIAL POWER ON DETECT, AND POWER FAIL TIME SAVE

There are three other functions provided on the LV8572A to ease power supply control. These are an initial Power On detect circuit, which also can be used as a time keeping failure detect, a low battery detect circuit, and a time save on power failure.

On initial power up the Oscillator Fail Flag will be set to a one and the real time clock start bit reset to a zero. This indicates that an oscillator fail event has occurred, and time keeping has failed.

The Oscillator Fail flag will not be reset until the real-time clock is started. This allows the system to discriminate between an initial power-up and recovery from a power failure. If the battery backed mode is selected, then bit D6 of the Periodic Flag Register must be written low. This will not affect the contents of the Oscillator Fail Flag.

Another status bit is the low battery detect. This bit is set only when the clock is operating under the V_{CC} pin, and when the battery voltage is determined to be less than 2.1V (typical). When the power fail interrupt enable bit is low, it disables the power fail circuit and will also shut off the low battery voltage detection circuit as well.

To relieve CPU overhead for saving time upon power failure, the Time Save Enable bit is provided to do this automatically. (See also Reading the Clock: Latched Read.) The Time Save Enable bit, when set, causes the Time Save RAM to follow the contents of the clock. This bit can be reset by software, but if set before a power failure occurs, it will automatically be reset when the clock switches to the battery supply (not when a power failure is detected by the $\overline{PFAIL}$ pin). Thus, writing a one to the Time Save bit enables both a software write or power fail write.

SINGLE POWER SUPPLY APPLICATIONS

The LV8572A can be used in a single power supply application. To achieve this, the V_{BB} pin must be connected to ground, and the power connected to V_{CC} and $\overline{PFAIL}$ pins. The Oscillator Failed/Single Supply bit in the Periodic Flag Register should be set to a logic 1, which will disable the oscillator battery reference circuit. The power fail interrupt should also be disabled. This will turn off the linear power fail detection circuits, and will eliminate any quiescent power drawn through these circuits. Until the crystal select bits are initialized, the LV8572A may consume about 50 μA due to arbitrary oscillator selection at power on.

(This extra 50 μA is not consumed if the battery backed mode is selected).

DETAILED REGISTER DESCRIPTION

There are 5 external address bits: Thus, the host microprocessor has access to 28 locations at one time. An internal switching scheme provides a total of 61 locations.

This complete address space is organized into two pages. Page 0 contains two blocks of control registers, timers, real time clock counters, and special purpose RAM, while page 1 contains general purpose RAM. Using two blocks enables the 9 control registers to be mapped into 5 locations. The only register that does not get switched is the Main Status Register. It contains the page select bit and the register select bit as well as status information.

A memory map is shown in *Figure 2* and register addressing in Table III. They show the name, address and page locations for the LV8572A.

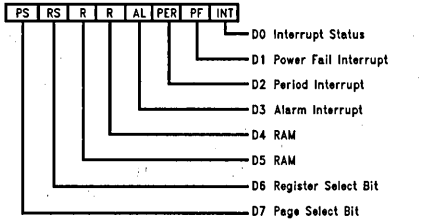
TABLE III. Register/Counter/RAM Addressing for LV8572A

A0-4	PS (Note 1)	RS (Note 2)	Description
CONTROL REGISTERS			
00	X	X	Main Status Register
03	0	0	Periodic Flag Register
04	0	0	Time Save Control Register
01	0	1	Real Time Mode Register
02	0	1	Output Mode Register
03	0	1	Interrupt Control Register 0
04	0	1	Interrupt Control Register 1
COUNTERS (CLOCK CALENDAR)			
05	0	X	1/100, 1/10 Seconds (0-99)
06	0	X	Seconds (0-59)
07	0	X	Minutes (0-59)
08	0	X	Hours (1-12, 0-23)
09	0	X	Days of Month (1-28/29/30/31)
0A	0	X	Months (1-12)
0B	0	X	Years (0-99)
0C	0	X	Julian Date (LSB) (1-99)
0D	0	X	Julian Date (0-3)
0E	0	X	Day of Week (1-7)
TIME COMPARE RAM			
13	0	X	Sec Compare RAM (0-59)
14	0	X	Min Compare RAM (0-59)
15	0	X	Hours Compare RAM (1-12, 0-23)
16	0	X	DOM Compare RAM (1-28/29/30/31)
17	0	X	Months Compare RAM (1-12)
18	0	X	DOW Compare RAM (1-7)
TIME SAVE RAM			
19	0	X	Seconds Time Save RAM
1A	0	X	Minutes Time Save RAM
1B	0	X	Hours Time Save RAM
1C	0	X	Day of Month Time Save RAM
1D	0	X	Months Time Save RAM
1E	0	1	RAM
1F	0	X	RAM/Test Mode Register
01-1F	1	X	2nd Page General Purpose RAM

1 PS—Page Select (Bit D7 of Main Status Register)
2 RS—Register Select (Bit D6 of Main Status Register)

Functional Description (Continued)

MAIN STATUS REGISTER



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The Main Status Register is always located at address 0 regardless of the register block or the page selected.

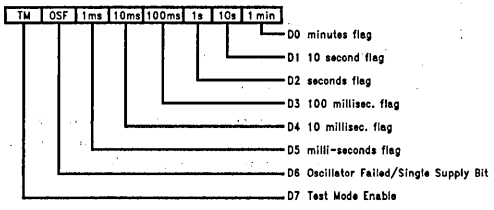
D0: This read only bit is a general interrupt status bit that is taken directly from the interrupt pins. The bit is a one when an interrupt is pending on either the INTR pin or the MFO pin (when configured as an interrupt). This is unlike D3 which can be set by an internal event but may not cause an interrupt. This bit is reset when the interrupt status bits in the Main Status Register are cleared.

D1–D3: These three bits of the Main Status Register are the main interrupt status bits. Any bit may be a one when any of the interrupts are pending. Once an interrupt is asserted the μP will read this register to determine the cause. These interrupt status bits are not reset when read. Except for D1, to reset an interrupt a one is written back to the corresponding bit that is being tested. D1 is reset whenever the $\overline{\text{PFAIL}}$ pin = logic 1. This prevents loss of interrupt status when reading the register in a polled mode. D1 and D3 are set regardless of whether these interrupts are masked or not by bits D6 and D7 of Interrupt Control Registers 0 and 1.

D4–D5: General purpose RAM bits.

D6 and D7: These bits are Read/Write bits that control which register block or RAM page is to be selected. Bit D6 controls the register block to be accessed (see memory map). The memory map of the clock is further divided into two memory pages. One page is the registers, clock and timers, and the second page contains 31 bytes of general purpose RAM. The page selection is determined by bit D7.

PERIODIC FLAG REGISTER



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The Periodic Flag Register has the same bit for bit correspondence as Interrupt Control Register 0 except for D6 and D7. For normal operation (i.e., not a single supply application) this register must be written to on initial power up or after an oscillator fail event. D0–D5 are read only bits, D6 and D7 are read/write.

D0–D5: These bits are set by the real time rollover events: (Time Change = 1). The bits are reset when the register is read and can be used as selective data change flags.

D6: This bit performs a dual function. When this bit is read, a one indicates that an oscillator failure has occurred and the time information may have been lost. Some of the ways an oscillator failure can be caused are: failure of the crystal, shorting OSC IN or OSC OUT to GND or V_{CC}, removal of crystal, removal of battery when in the battery backed mode (when a "0" is written to D6), lowering the voltage at the V_{BB} pin to a value less than 2.2V when in the battery backed mode. Bit D6 is automatically set to 1 on initial power-up or an oscillator fail event. The oscillator fail flag is reset by writing a one to the clock start/stop bit in the Real Time Mode Register, with the crystal oscillating.

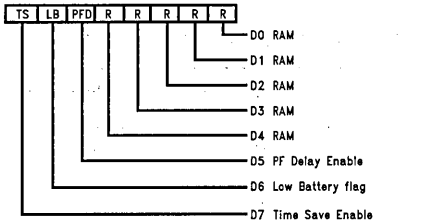
When D6 is written to, it defines whether the TCP is being used in battery backed (normal) or in a single supply mode application. When set to a one this bit configures the TCP for single power supply applications. This bit is automatically set on initial power-up or an oscillator fail event. When set, D6 disables the oscillator reference circuit. The result is that the oscillator is referenced to V_{CC}. When a zero is written to D6 the oscillator reference is enabled, thus the oscillator is referenced to V_{BB}. This allows operation in standard battery standby applications.

At initial power on, if the LV8572A is going to be programmed for battery backed mode, the V_{BB} pin should be connected to a potential in the range of 2.2V to V_{CC} − 0.4V.

For single supply mode operation, the V_{BB} pin should be connected to GND and the $\overline{\text{PFAIL}}$ pin connected to V_{CC}.

D7: Writing a one to this bit enables the test mode register at location 1F (see Table III). This bit should be forced to zero during initialization for normal operation. If the test mode has been entered, clear the test mode register before leaving test mode. (See separate test mode application note for further details.)

TIME SAVE CONTROL REGISTER



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D0–D4: General purpose RAM bits.

Functional Description (Continued)

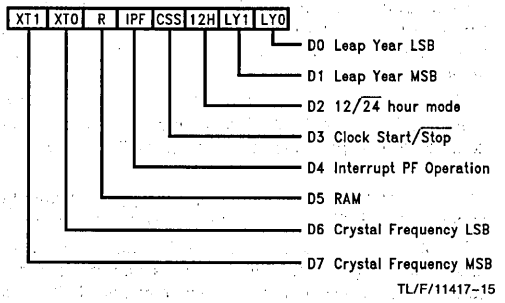
D5: The Delay Enable bit is used when a power fail occurs. If this bit is set, a 480 μs delay is generated internally before the μP interface is locked out. This will enable the μP to access the registers for up to 480 μs after it receives a power fail interrupt. After a power failure is detected but prior to the 480 μs delay timing out, the host μP may force immediate lock out by resetting the Delay Enable bit. Note if this bit is a 0 when power fails then after a delay of 30 μs min/63 μs max the μP cannot read the chip.

D6: This read only bit is set and reset by the voltage at the V_{BB} pin. It can be used by the μP to determine whether the battery voltage at the V_{BB} pin is getting too low. A comparator monitors the battery and when the voltage is lower than 2.1V (typical) this bit is set. The power fail interrupt must be enabled to check for a low battery voltage.

D7: Time Save Enable bit controls the loading of real-time-clock data into the Time Save RAM. When a one is written to this bit the Time Save RAM will follow the corresponding clock registers, and when a zero is written to this bit the time in the Time Save RAM is frozen. This eliminates any synchronization problems when reading the clock, thus negating the need to check for a counter rollover during a read cycle.

This bit must be set to a one prior to power failing to enable the Time Save feature. When the power fails this bit is automatically reset and the time is saved in the Time Save RAM.

REAL TIME MODE REGISTER



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D0–D1: These are the leap year counter bits. These bits are written to set the number of years from the previous leap year. The leap year counter increments on December 31st and it internally enables the February 29th counter state. This method of setting the leap year allows leap year to occur whenever the user wishes to, thus providing flexibility in implementing Japanese leap year function.

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

D2: The count mode for the hours counter can be set to either 24 hour mode or 12 hour mode with AM/PM indicator. A one will place the clock in 12 hour mode.

D3: This bit is the master Start/$\overline{\text{Stop}}$ bit for the clock. When a one is written to this bit the real time counter's prescaler and counter chain are enabled. When this bit is reset to zero the contents of the real time counter is stopped and the prescaler is cleared. When the RTC is initially powered up this bit will be held at a logic 0 until the oscillator starts functioning correctly after which this bit may be modified. If an oscillator fail event occurs, this bit will be reset to logic 0.

D4: This bit controls the operation of the interrupt output in standby mode. If set to a one it allows Alarm, Periodic, and Power Fail interrupts to be functional in standby mode. Note that the MFO pin is configured as open drain in standby mode.

If bit D4 is set to a zero then interrupt control register and the periodic interrupt flag will be reset when the RTC enters the standby mode. They will have to be re-configured when system (V_{CC}) power is restored.

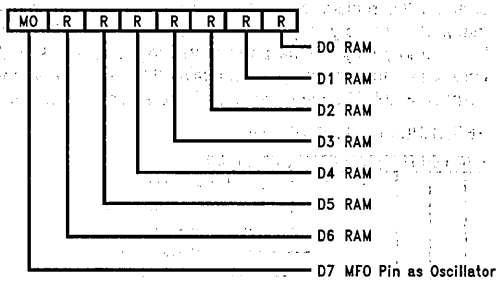
D5: General purpose RAM.

D6 and D7: These two bits select the crystal clock frequency as per the following table:

XT1	XT0	Crystal Frequency
0	0	32.768 kHz
0	1	4.194304 MHz
1	0	4.9152 MHz
1	1	32.000 kHz

All bits are Read/Write, and any mode written into this register can be determined by reading the register. On initial power up these bits are random.

OUTPUT MODE REGISTER



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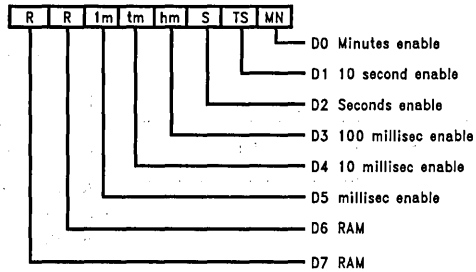
D0–D6: General Purpose RAM

Functional Description (Continued)

D7: This bit is used to program the signal appearing at the MFO output, as follows:

D7	MFO Output Signal
0	Power Fail Interrupt
1	Buffered Crystal Oscillator

INTERRUPT CONTROL REGISTER 0



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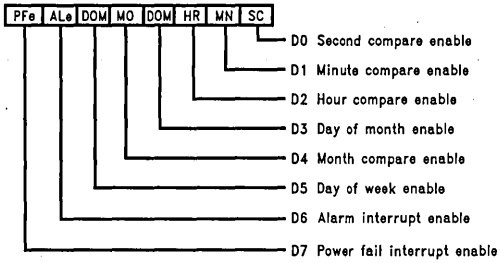
D0–D5: These bits are used to enable one of the selected periodic interrupts by writing a one into the appropriate bit. These interrupts are issued at the rollover of the clock. For example, the minutes interrupt will be issued whenever the minutes counter increments. In all likelihood the interrupt will be enabled asynchronously with the real time change. Therefore, the very first interrupt will occur in less than the periodic time chosen, but after the first interrupt all subsequent interrupts will be spaced correctly. These interrupts are useful when minute, second, real time reading, or task switching is required. When all six bits are written to a 0 this disables periodic interrupts from the Main Status Register and the interrupt pin.

D6 and D7: General Purpose RAM.

INTERRUPT CONTROL REGISTER 1



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D0–D5: Each of these bits are enable bits which will enable a comparison between an individual clock counter and its associated compare RAM. If any bit is a zero then that clock-RAM comparator is set to the "always equal" state and the associated TIME COMPARE RAM byte can be used as general purpose RAM. However, to ensure that an alarm interrupt is not generated at bit D3 of the Main Status Register, all bits must be written to a logic zero.

D6: In order to generate an external alarm compare interrupt to the μP from bit D3 of the Main Status Register, this bit must be written to a logic 1.

D7: The MSB of this register is the enable bit for the Power Fail Interrupt. When this bit is set to a one an interrupt will be generated to the μP when $V_{BB} > V_{CC}$.

This bit also enables the low battery detection analog circuitry.

Control and Status Register Address Bit Map

Main Status Register PS = X RS = X ADDRESS = 00H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W[1]	R/W[1]	R[2]	R[3]
Page Select	Register Select	RAM	RAM	Alarm Interrupt	Periodic Interrupt	Power Fail Interrupt	Interrupt Status

Periodic Flag Register PS = 0 RS = 0 Address = 03H

R/W	R/W[4]	R[5]	R[5]	R[5]	R[5]	R[5]	R[5]
Test Mode	Osc. Fail/ Single Supply	1 ms Flag	10 ms Flag	100 ms Flag	Seconds Flag	10 Second Flag	Minute Flag

Time Save Control Register PS = 0 RS = 0 Address = 04H

R/W	R[6]	R/W	R/W	R/W	R/W	R/W	R/W
Time Save Enable	Low Battery Flag	Power Fail Delay Enable	RAM	RAM	RAM	RAM	RAM

Real Time Mode Register PS = 0 RS = 1 Address = 01H

Crystal Freq. XT1	Crystal Freq. XT0	RAM	Interrupt EN on Back-Up	Clock Start/$\overline{\text{Stop}}$	12/$\overline{24}$ Hr. Mode	Leap Year MSB	Leap Year LSB

All Bits R/W

Output Mode Register PS = 0 RS = 1 Address = 02H

MFO as Crystal	RAM	RAM	RAM	RAM	RAM	RAM	RAM

All Bits R/W

Interrupt Control Register 0 PS = 0 RS = 1 Address = 03H

RAM	RAM	1 ms Interrupt Enable	10 ms Interrupt Enable	100 ms Interrupt Enable	Seconds Interrupt Enable	10 Second Interrupt Enable	Minute Interrupt Enable

All Bits R/W

Interrupt Control Register 1 PS = 0 RS = 1 Address = 04H

Power Fail Interrupt Enable	Alarm Interrupt Enable	DOW Interrupt Enable	Month Interrupt Enable	DOM Interrupt Enable	Hours Interrupt Enable	Minute Interrupt Enable	Second Interrupt Enable

All Bits R/W

1. Reset by writing 1 to bit.
2. Set/reset by voltage at $\overline{\text{PFAIL}}$ pin.
3. Reset when all pending interrupts are removed.
4. Read Osc fail Write 0 Batt-Backed Mode Write 1 Single Supply Mode
5. Reset by positive edge of read.
6. Set and reset by V_{BB} voltage.

Application Hints

Suggested Initialization Procedure for LV8572A in Battery Backed Applications that use the V_{BB} Pin.

1. Enter the test mode by writing a 1 to bit D7 in the Periodic Flag Register.
2. Write zero to the RAM/TEST mode Register located in page 0, address HEX 1F.
3. Leave the test mode by writing a 0 to bit D7 in the Periodic Flag Register. Steps 1,2,3 guarantee that if the test mode had been entered during power on (due to random pulses from the system), all test mode conditions are cleared. Most important is that the OSC Fail Disable bit is cleared. Refer to AN-589 for more information on test mode operation.
4. After power on (V_{CC} and V_{BB} powered), select the correct crystal frequency bits (D7, D6 in the Real Time Mode Register) as shown in Table IV.

TABLE IV

Frequency	D7	D6
32.768 kHz	0	0
4.194304 MHz	0	1
4.9152 MHz	1	0
32.0 kHz	1	1

5. Enter a software loop that does the following:

   Set a 3 second(approx) software counter. The crystal oscillator may take 1 second to start.

5.1 Write a 1 to bit D3 in the Real Time Mode Register (try to start the clock). Make sure the crystal select bits remain the same as in step 1. Under normal operation, this bit can be set only if the oscillator is running. During the software loop, RAM, real time counters, output configuration, interrupt control and timer functions may be initialized.

6. Test bit D6 in the Periodic Flag Register:

   IF a 1, go to 5.1. If this bit remains a 1 after 3 seconds, then abort and check hardware. The crystal may be defective or not installed. There may be a short at OSC IN or OSC OUT to V_{CC} or GND, or to some impedance that is less than 10 MΩ.

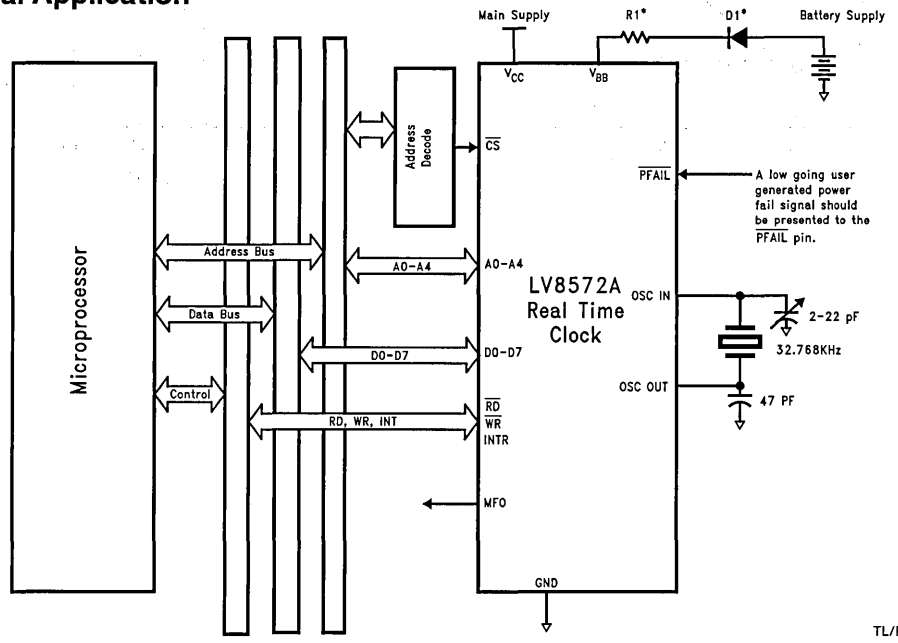
   IF a 0, then the oscillator is running, go to step 7.

7. Write a 0 to bit D6 in the Periodic Flag Register. This action puts the clock chip in the battery backed mode. This mode can be entered only if the OSC fail flag (bit D6 of the Periodic Flag Register) is a 0. Reminder, Bit D6 is a dual function bit. When read, D6 returns oscillator status. When written, D6 causes either the Battery Backed Mode, or the Single Supply Mode of operation.

   The only method to ensure the chip is in the battery backed mode is to measure the waveform at the OSC OUT pin. If the battery backed mode was selected successfully, then the peak to peak waveform at OSC OUT is referenced to the battery voltage. If not in battery backed mode, the waveform is referenced to V_{CC}. The measurement should be made with a high impedance low capacitance probe (10 MΩ, 10 pF oscilloscope probe or better). Typical peak to peak swings are within 0.6V of V_{CC} and ground respectively.

8. Write a 1 to bit D7 of Interrupt Control Register 1. This action enables the PFAIL pin and associated circuitry.
9. Initialize the rest of the chip as needed.

Typical Application



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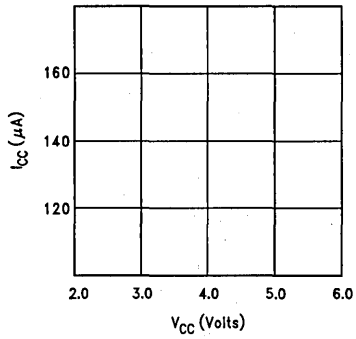
*These components may be necessary to meet UL requirements for lithium batteries. Consult battery manufacturer.

Typical Performance Characteristics

Operating Current vs Supply Voltage (TBD) (Single Supply Mode F_{OSC} = 32.768 kHz)



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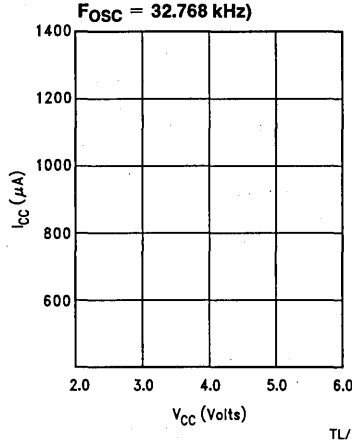
Operating Current vs Supply Voltage (TBD) (Battery Backed Mode F_{OSC} = 32.768 kHz)



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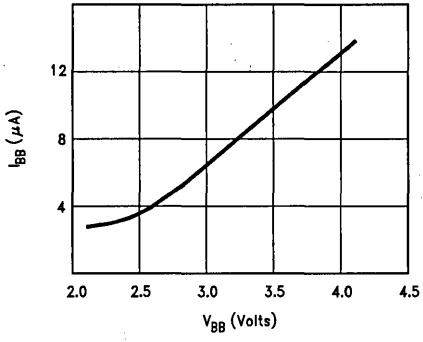
Standby Current vs Power Supply Voltage (F_{OSC} = 32.768 kHz)



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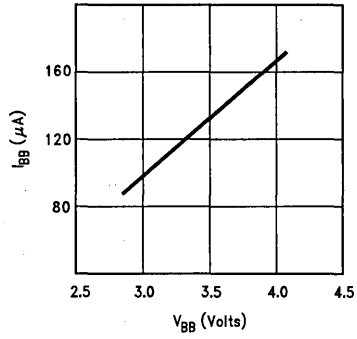
Standby Current vs Power Supply Voltage F_{OSC} = 4.194304 MHz



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National Semiconductor

PRELIMINARY

LV8573A Low Voltage Real Time Clock (RTC)

General Description

The LV8573A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports organized as one block of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, and the Time Save RAM.

Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week and day of month counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the 32.768 kHz crystal and two capacitors.

Power failure logic and control functions have been integrated on chip. This logic is used by the RTC to issue a power fail interrupt, and lock out the μP interface. The time power fails may be logged into RAM automatically when $V_{BB} > V_{CC}$. Additionally, two supply pins are provided. When $V_{BB} > V_{CC}$, internal circuitry will automatically switch from the main supply to the battery supply.

The LV8573A's interrupt structure provides three basic types of interrupts: Periodic, Alarm/Compare, and Power Fail. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

Features

- 3.3V ±10% supply
- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week counter
  - Parallel resonant oscillator
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, and power fail interrupts

Block Diagram

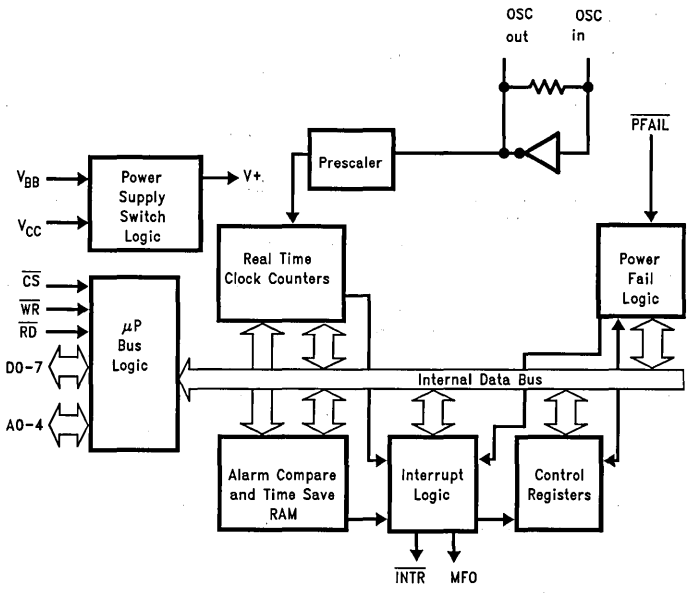

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FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (PD)	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C

Operation Conditions

	Min	Max	Unit
Supply Voltage (V_{CC}) (Note 3)	3.0	3.6	V
Supply Voltage (V_{BB}) (Note 3)	2.2	V_{CC}−0.4	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0.0	V_{CC}	V
Operation Temperature (T_A)	−40	+85	°C
Electr-Static Discharge Rating TBD		1	kV

Typical Values

θ_{JA} DIP	Board	
	Socket	
θ_{JA} PLCC	Board	80°C/W
	Socket	88°C/W

DC Electrical Characteristics

V_{CC} = 3.3V ±10%, V_{BB} = 2.5V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF unless otherwise specified

Symbol	Parameter	Conditions	Min (Note 15)	Max (Note 15)	Units
V_{IH}	High Level Input Voltage (Note 4)	Any Inputs Except OSC IN, OSC IN with External Clock	2.0 V_{BB} − 0.2	V_{CC} +0.3	V V
V_{IL}	Low Level Input Voltage	All Inputs Except OSC IN OSC IN with External Clock	−0.3 −0.3	0.8 0.2	V V
V_{OH}	High Level Output Voltage (Excluding OSC OUT)	I_{OUT} = −20 μA I_{OUT} = −2.0 mA	V_{CC} −0.2 2.4		V V
V_{OL}	Low Level Output Voltage (Excluding OSC OUT)	I_{OUT} = 20 μA I_{OUT} = 2.0 mA		0.2 0.3	V V
I_{IN}	Input Current (Except OSC IN)	V_{IN} = V_{CC} or GND		±1	μA
I_{OZ}	Output TRI-STATE® Current	V_{OUT} = V_{CC} or GND		±5	μA
I_{LKG}	Output High Leakage Current MFO, INTR Pins	V_{OUT} = V_{CC} or GND Outputs Open Drain		±5	μA
I_{CC}	Quiescent Supply Current (Note 6)	F_{OSC} = 32.768 kHz V_{IN} = V_{CC} or GND (Note 5) V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		 200 700 8	 μA μA mA
I_{CC}	Quiescent Supply Current (Single Supply Mode) (Note 7)	V_{BB} = GND V_{IN} = V_{CC} or GND F_{OSC} = 32.768 kHz		20	μA
I_{BB}	Standby Mode Battery Supply Current (Note 7)	V_{CC} = GND OSC OUT = open circuit, other pins = GND F_{OSC} = 32.768 kHz		8	μA
I_{BLK}	Battery Leakage	2.2V ≤ V_{BB} ≤ 2.6V other pins at GND V_{CC} = GND, V_{BB} = 2.6V V_{CC} = 3.6V	 −5	 1.5 	 μA μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: In battery backed mode, $V_{BB} \leq V_{CC} - 0.4V$.
Single Supply Mode: Data retention voltage is 2.2V min.
In single Supply Mode (Power connected to V_{CC} pin) 3.0V ≤ V_{CC} ≤ 3.6V.

Note 4: This parameter (V_{IH}) is not tested on all pins at the same time.

Note 5: This specification tests I_{CC} with all power fail circuitry disabled, by setting D7 of Interrupt Control Register 1 to 0.

Note 6: This specification tests I_{CC} with all power fail circuitry enabled, by setting D7 of Interrupt Control Register 1 to 1.

Note 7: OSC IN is driven by a signal generator. Contents of the Test Register = 00(H) and the MFO pin is not configured as buffered oscillator out.

AC Electrical Characteristics

V_{CC} = 3.3V ±10%, V_{BB} = 2.5V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF unless otherwise specified

Symbol	Parameter	Min (Note 15)	Max (Note 15)	Units
READ TIMING				
t_{AR}	Address Valid Prior to Read Strobe	10		ns
t_{RW}	Read Strobe Width (Note 8)	80		ns
t_{CD}	Chip Select to Data Valid Time		80	ns
t_{RAH}	Address Hold after Read (Note 9)	0		ns
t_{RD}	Read Strobe to Valid Data		70	ns
t_{DZ}	Read or Chip Select to TRI-STATE		70	ns
t_{RCH}	Chip Select Hold after Read Strobe (Note 9)	0		ns
t_{DS}	Minimum Inactive Time between Read or Write Accesses	40		ns
WRITE TIMING				
t_{AW}	Address Valid before Write Strobe	10		ns
t_{WAH}	Address Hold after Write Strobe (Note 9)	0		ns
t_{CW}	Chip Select to End of Write Strobe	60		ns
t_{WW}	Write Strobe Width (Note 10)	50		ns
t_{DW}	Data Valid to End of Write Strobe	40		ns
t_{WDH}	Data Hold after Write Strobe (Note 9)	2		ns
t_{WCH}	Chip Select Hold after Write Strobe (Note 9)	0		ns
INTERRUPT TIMING				
t_{ROLL}	Clock rollover to $\overline{INTR}$ out typically 20 μs			

Note 8: Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

Note 9: Hold time is guaranteed by design but not production tested. This limit is not used to calculate outgoing quality levels.

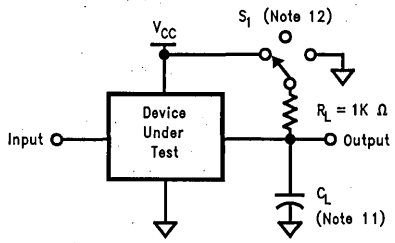
Note 10: Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns (10%–90%)
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels (Note 12)	Active High +0.5V Active Low −0.5V

Note 11: C_L = 100 pF, includes jig and scope capacitance.

Note 12: S1 = V_{CC} for active low to high impedance measurements.
S1 = GND for active high to high impedance measurements.
S1 = open for all other timing measurements.



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Capacitance (T_A = 25°C, f = 1 MHz)

Symbol	Parameter (Note 14)	Typ	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	7	pF

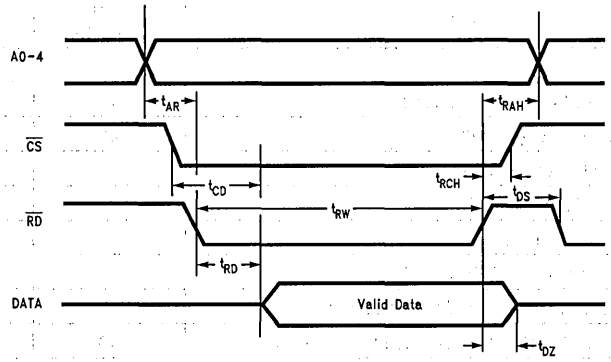
Note 13: This parameter is not 100% tested.

Note 14: Output rise and fall times 25 ns max (10%–90%) with 100 pF load.

Note 15: Room temperature values only.

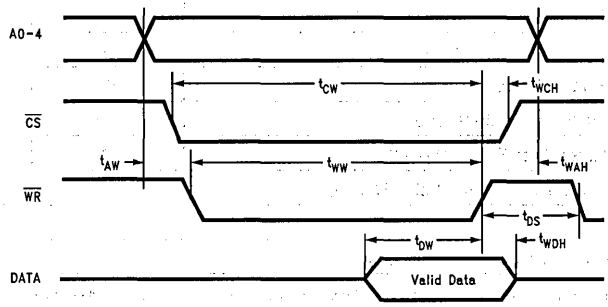
Timing Waveforms

Read Timing Diagram



TL/F/11418–3

Write Timing Diagram



TL/F/11418–4

Pin Description

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (Inputs): These pins interface to μP control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and Write pins are also active low and enable reading or writing to the RTC. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.

A0–A4 (Inputs): These 5 pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.

OSC IN (Input); OSC OUT (Output): These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}.

MFO (Output): The multi-function output can be used as a second interrupt (Power fail) output for interrupting the μP. This pin can also provide an output for the oscillator. The MFO output is configured as push-pull, active high for normal or single power supply operation and as an open drain during standby mode ($V_{BB} > V_{CC}$). If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

$\overline{INTR}$ (Output): The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The $\overline{INTR}$ output is permanently configured active low, open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

D0–D7 (Input/Output): These 8 bidirectional pins connect to the host μP's data bus and are used to read from and write to the RTC. When the $\overline{PFAIL}$ pin goes low and a write is not in progress, these pins are at TRI-STATE.

$\overline{PFAIL}$ (Input): In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the RTC goes into a lockout mode, in a minimum of 30 μs or a maximum of 63 μs unless lockout delay is programmed. In the single power supply mode, this pin is not useable as an input and should be tied to V_{CC}. Refer to section on Power Fail Functional Description.

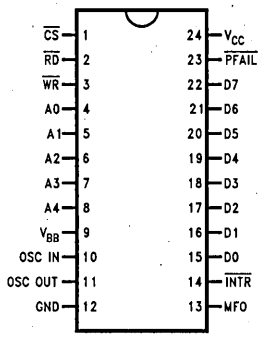
V_{BB} (Battery Power Pin): This pin is connected to a back-up power supply. This power supply is switched to the internal circuitry when the V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the RTC programmed for single power supply only, and power applied to the V_{CC} pin.

V_{CC}: This is the main system power pin.

GND: This is the common ground power pin for both V_{BB} and V_{CC}.

Connection Diagrams

Dual-In-Line

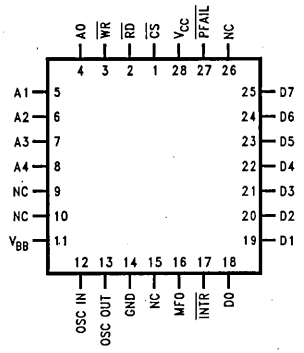


TL/F/11418–5

Top View

Order Number LV8573AN
See NS Package Number N24C

Plastic Chip Carrier



TL/F/11418–6

Top View

Order Number LV8573AV
See NS Package Number V28A

Functional Description

The LV8573A contains a fast access real time clock, interrupt control logic, and power fail detect logic. All functions of the RTC are controlled by a set of seven registers. A simplified block diagram that shows the major functional blocks is given in *Figure 1*.

The blocks are described in the following sections:

1. Real Time Clock
2. Oscillator Prescaler
3. Interrupt Logic
4. Power Failure Logic
5. Additional Supply Management

The memory map of the RTC is shown in the memory addressing table *(Figure 2)*. A control bit in the Main Status Register is used to select either control register block.

INITIAL POWER-ON of BOTH V_{BB} and V_{CC}

V_{BB} and V_{CC} may be applied in any sequence. In order for the power fail circuitry to function correctly, whenever power is off, the V_{CC} pin must see a path to ground through a maximum of 1 MΩ. The user should be aware that the control registers will contain random data. The user should ensure that the RTC is not in test mode (see register descriptions).

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

As shown in *Figure 2*, the clock has 8 bytes of counters, which count from 1/100 of a second to years. Each counter counts in BCD and is synchronously clocked. The count sequence of the individual byte counters within the clock is shown later in Table VII. Note that the day of week, day of month, and month counters all roll over to 1. The hours counter in 12 hour mode rolls over to 1 and the AM/PM bit toggles when the hours rolls over to 12 (AM = 0, PM = 1). The AM/PM bit is bit D7 in the hours counter.

All other counters roll over to 0. Upon initial application of power the counters will contain random information.

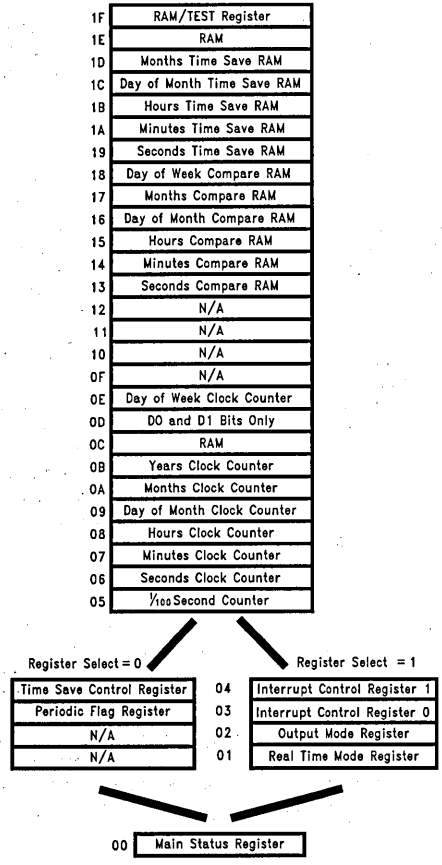


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FIGURE 2. LV8573A Internal Memory Map

Functional Description (Continued)

READING THE CLOCK: VALIDATED READ

Since clocking of the counter occurs asynchronously to reading of the counter, it is possible to read the counter while it is being incremented (rollover). This may result in an incorrect time reading. Thus to ensure a correct reading of the entire contents of the clock (or that part of interest), it must be read without a clock rollover occurring. In general this can be done by checking a rollover bit. On this chip the periodic interrupt status bits can serve this function. The following program steps can be used to accomplish this.

1. Initialize program for reading clock.
2. Dummy read of periodic status bit to clear it.
3. Read counter bytes and store.
4. Read rollover bit, and test it.
5. If rollover occured go to 3.
6. If no rollover, done.

To detect the rollover, individual periodic status bits can be polled. The periodic bit chosen should be equal to the highest frequency counter register to be read. That is if only SECONDS through HOURS counters are read, then the SECONDS periodic bit should be used.

READING THE CLOCK: INTERRUPT DRIVEN

Enabling the periodic interrupt mask bits cause interrupts just as the clock rolls over. Enabling the desired update rate and providing an interrupt service routine that executes in less than 10 ms enables clock reading without checking for a rollover.

READING THE CLOCK: LATCHED READ

Another method to read the clock that does not require checking the rollover bit is to write a one into the Time Save Enable bit (D7) of the Time Save Control Register, and then to write a zero. Writing a one into this bit will enable the clock contents to be duplicated in the Time Save RAM. Changing the bit from a one to a zero will freeze and store the contents of the clock in Time Save RAM. The time then can be read without concern for clock rollover, since internal logic takes care of synchronization of the clock. Because only the bits used by the clock counters will be latched, the Time Save RAM should be cleared prior to use to ensure that random data stored in the unused bits do not confuse the host microprocessor. This bit can also provide time save at power failure, see the Additional Supply Management Functions section. With the Time Save Enable bit at a logical 0, the Time Save RAM may be used as RAM if the latched read function is not necessary.

INITIALIZING AND WRITING TO THE CALENDAR-CLOCK

Upon initial application of power to the TCP or when making time corrections, the time must be written into the clock. To correctly write the time to the counters, the clock would normally be stopped by writing the Start/$\overline{\text{Stop}}$ bit in the Real Time Mode Register to a zero. This stops the clock from counting and disables the carry circuitry. When initializing the clock's Real Time Mode Register, it is recommended that first the various mode bits be written while maintaining the Start/$\overline{\text{Stop}}$ bit reset, and then writing to the register a second time with the Start/$\overline{\text{Stop}}$ bit set.

The above method is useful when the entire clock is being corrected. If one location is being updated the clock need not be stopped since this will reset the prescaler, and time will be lost. An ideal example of this is correcting the hours for daylight savings time. To write to the clock "on the fly" the best method is to wait for the 1/100 of a second periodic interrupt. Then wait an additional 16 μs, and then write the data to the clock.

PRESCALER/OSCILLATOR FUNCTIONAL DESCRIPTION

Feeding the counter chain is a programmable prescaler which divides the crystal oscillator frequency to 32 kHz and further to 100 Hz for the counter chain (see *Figure 3*).

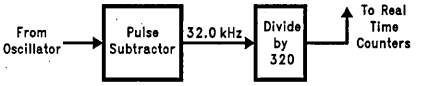

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FIGURE 3. Programmable Clock Prescaler Block

In addition to the inverter, the oscillator feedback bias resistor is included on chip, as shown in *Figure 4*. The oscillator input may be driven from an external source if desired. Refer to test mode application note for details. The oscillator stability is enhanced through the use of an on chip regulated power supply.

The typical range of trimmer capacitor (as shown in Oscillator Circuit Diagram *Figure 4*, and in the typical application) at the oscillator input pin is suggested only to allow accurate tuning of the oscillator. This range is based on a typical printed circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases, the **load capacitance** specified by the crystal manufacturer (nominal value 11 pF for the 32.768 crystal) is what determines proper oscillation. This load capcitance is the series combination of capacitance on each side of the crystal (with respect to ground).

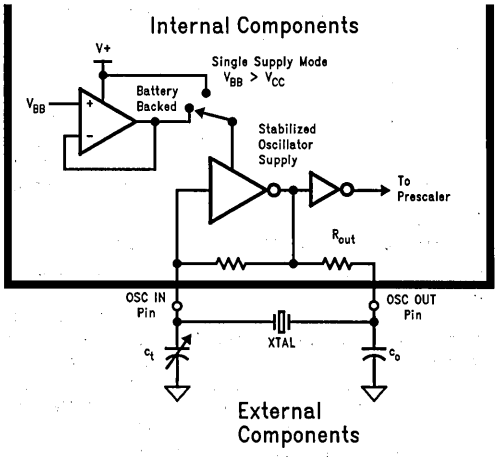

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FIGURE 4. Oscillator Circuit Diagram

Functional Description (Continued)

XTAL	C_o	C_t	R_{OUT}
32.768 kHz	47 pF	2 pF–22 pF	150 kΩ to 350 kΩ

INTERRUPT LOGIC FUNCTIONAL DESCRIPTION

The RTC has the ability to coordinate processor timing activities. To enhance this, an interrupt structure has been implemented which enables several types of events to cause interrupts. Interrupts are controlled via two Control Registers in block 1 and two Status Registers in block 0. (See Register Description for notes on paging and Table I.)

The interrupts are enabled by writing a one to the appropriate bits in Interrupt Control Register 0 and/or 1.

TABLE I. Registers that are Applicable to Interrupt Control

Register Name	Register Select	Address
Main Status Register	X	00H
Periodic Flag Register	0	03H
Interrupt Control Register 0	1	03H
Interrupt Control Register 1	1	04H
Output Mode Register	1	02H

The Interrupt Status Flag D0, in the Main Status Register, indicates the state of $\overline{INTR}$ and MFO outputs. It is set when either output becomes active and is cleared when all RTC interrupts have been cleared and no further interrupts are pending (i.e., both $\overline{INTR}$ and MFO are returned to their inactive state). This flag enables the RTC to be rapidly polled by the μP to determine the source of an interrupt in a wired—OR interrupt system. (The Interrupt Status Flag provides a true reflection of all conditions routed to the external pins.)

Status for the interrupts are provided by the Main Status Register and the Periodic Flag Register. Bits D1–D5 of the Main Status Register are the main interrupt bits.

These register bits will be set when their associated timing events occur. Enabled Alarm comparisons that occur will set its Main Status Register bit to a one. However, an external interrupt will only be generated if the Alarm interrupt enable bit is set (see *Figure 5*).

Disabling the periodic interrupts will mask the Main Status Register periodic bit, but not the Periodic Flag Register bits. The Power Fail Interrupt bit is set when the interrupt is enabled and a power fail event has occurred, and is not reset until the power is restored. If all interrupt enable bits are 0 no interrupt will be asserted. However, status still can be read from the Main Status Register in a polled fashion (see *Figure 5*).

To clear a flag in bits D2 and D3 of the Main Status Register a 1 must be written back into the bit location that is to be cleared. For the Periodic Flag Register reading the status will reset all the periodic flags.

Interrupts Fall Into Three Categories:

1. The Alarm Compare Interrupt: Issued when the value in the time compared RAM equals the counter.
2. The Periodic Interrupts: These are issued at every increment of the specific clock counter signal. Thus, an interrupt is issued every minute, second, etc. Each of these interrupts occurs at the roll-over of the specific counter.
3. The Power Fail Interrupt: Issued upon recognition of a power fail condition by the internal sensing logic. The power failed condition is determined by the signal on the $\overline{PFAIL}$ pin. The internal power fail signal is gated with the chip select signal to ensure that the power fail interrupt does not lock the chip out during a read or write.

ALARM COMPARE INTERRUPT DESCRIPTON

The alarm/time comparison interrupt is a special interrupt similar to an alarm clock wake up buzzer. This interrupt is generated when the clock time is equal to a value programmed into the alarm compare registers. Up to six bytes can be enabled to perform alarm time comparisons on the counter chain. These six bytes, or some subset thereof, would be loaded with the future time at which the interrupt will occur. Next, the appropriate bits in the Interrupt Control Register 1 are enabled or disabled (refer to detailed description of Interrupt Control Register 1). The RTC then compares these bytes with the clock time. When all the enabled compare registers equal the clock time an alarm interrupt is issued, but only if the alarm compare interrupt is enabled can the interrupt be generated externally. Each alarm compare bit in the Control Register will enable a specific byte for comparison to the clock. Disabling a compare byte is the same as setting its associated counter comparator to an "always equal" state. For example, to generate an interrupt at 3:15 AM of every day, load the hours compare with 0 3 (BCD), the minutes compare with 1 5 (BCD) and the faster counters with 0 0 (BCD), and then disable all other compare registers. So every day when the time rolls over from 3:14:59.99, an interrupt is issued. This bit may be reset by writing a one to bit D3 in the Main Status Register at any time after the alarm has been generated.

If time comparison for an individual byte counter is disabled, that corresponding RAM location can then be used as general purpose storage.

PERIODIC INTERRUPTS DESCRIPTION

The Periodic Flag Register contains six flags which are set by real-time generated "ticks" at various time intervals, see *Figure 5*. These flags constantly sense the periodic signals and may be used whether or not interrupts are enabled. These flags are cleared by any read or write operation performed on this register.

To generate periodic interrupts at the desired rate, the associated Periodic Interrupt Enable bit in Interrupt Control Register 0 must be set. Any combination of periodic interrupts may be enabled to operate simultaneously. Enabled periodic interrupts will now affect the Periodic Interrupt Flag in the Main Status Register.

When a periodic event occurs, the Periodic Interrupt Flag in the Main Status Register is set, causing an interrupt to be generated. The μP clears both flag and interrupt by writing a "1" to the Periodic Interrupt Flag. The individual flags in the periodic Interrupt Flag Register do not require clearing to cancel the interrupt.

If all periodic interrupts are disabled and a periodic interrupt is left pending (i.e., the Periodic Interrupt Flag is still set), the Periodic Interrupt Flag will still be required to be cleared to cancel the pending interrupt.

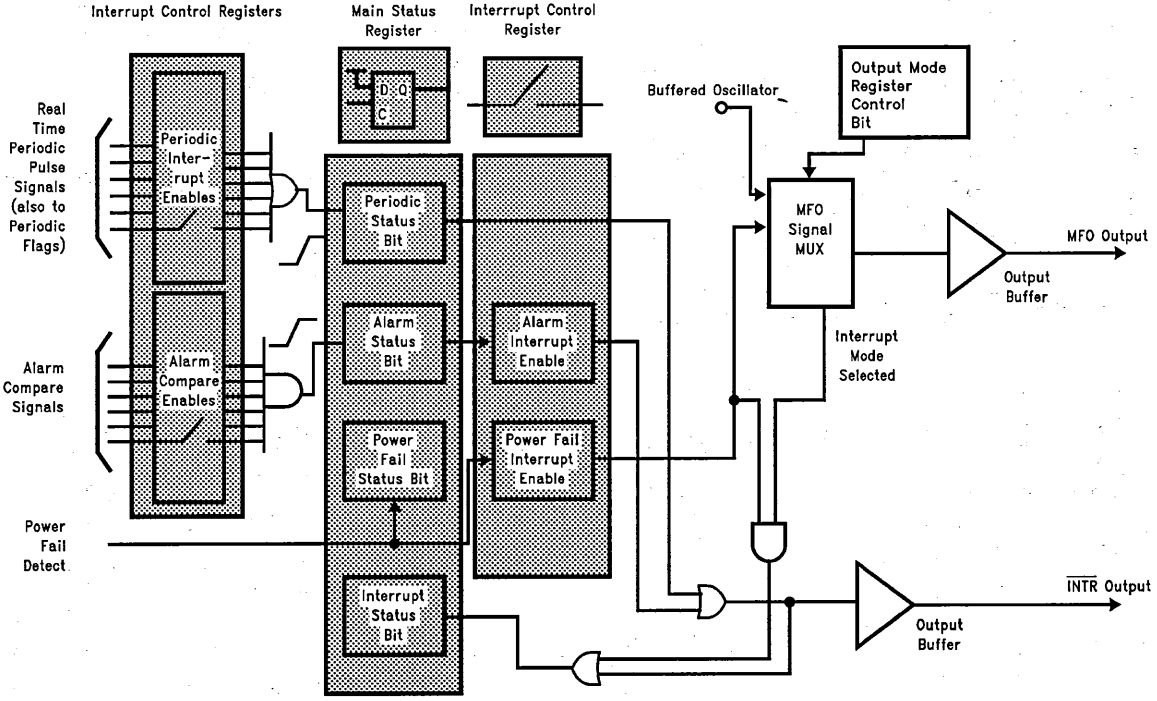

FIGURE 5. Interrupt Control Logic Overview

Functional Description (Continued)

POWER FAIL INTERRUPTS DESCRIPTION

The Power Fail Status Flag in the Main Status Register monitors the state of the internal power fail signal. This flag may be interrogated by the μP, but it cannot be cleared; it is cleared automatically by the RTC when system power is restored. To generate an interrupt when the power fails, the Power Fail Interrupt Enable bit in Interrupt Control Register 1 is set. Although this interrupt may not be cleared, it may be masked by clearing the Power Fail Interrupt Enable bit.

POWER FAILURE CIRCUITRY FUNCTIONAL DESCRIPTION

Since the clock must be operated from a battery when the main system supply has been turned off, the LV8573A provides circuitry to simplify design in battery backed systems. This switches over to the back up supply, and isolates itself from the host system. *Figure 6* shows a simplified block diagram of this circuitry, which consists of three major sections; 1) power loss logic: 2) battery switch over logic: and 3) isolation logic.

Detection of power loss occurs when $\overline{PFAIL}$ is low. Debounce logic provides a 30 μs–63 μs debounce time, which will prevent noise on the $\overline{PFAIL}$ pin from being interpreted as a system failure. After 30 μs–63 μs the debounce logic times out and a signal is generated indicating that system power is marginal and is failing. The Power Fail Interrupt will then be generated.

If chip select is low when a power failure is detected, a safety circuit will ensure that if a read or write is held active continuously for greater than 30 μs after the power fail signal is asserted, the lock-out will be forced.

The battery switch over circuitry is completely independent of the $\overline{PFAIL}$ pin. A separate circuit compares V_{CC} to the V_{BB} voltage. As the main supply fails, the RTC will continue to operate from the V_{CC} pin until V_{CC} falls below the V_{BB} voltage. At this time, the battery supply is switched in, V_{CC} is disconnected, and the device is now in the standby mode. If indeterminate operation of the battery switch over circuit is to be avoided, then the voltage at the V_{CC} pin must not be allowed to equal the voltage at the V_{BB} pin.

After the generation of a lock-out signal, and eventual switch in of the battery supply, the pins of the RTC will be configured as shown in Table II. Outputs that have a pull-up resistor should be connected to a voltage no greater than V_{BB}.

TABLE II. Pin Isolation during a Power Failure

Pin	$\overline{PFAIL}$ = Logic 0	Standby Mode $V_{BB} > V_{CC}$
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$	Locked Out	Locked Out
A0–A4	Locked Out	Locked Out
D0–D7	Locked Out	Locked Out
Oscillator	Not Isolated	Not Isolated
$\overline{PFAIL}$	Not Isolated	Not Isolated
INTR, MFO	Not Isolated	Open Drain

The Interrupt Power Fail Operation bit in the Real-Time Mode Register determines whether or not the interrupts will continue to function after a power fail event.

As power returns to the system, the battery switch over circuit will switch back to V_{CC} power as soon as it becomes greater than the battery voltage. The chip will remain in the locked out state as long as $\overline{PFAIL}$ = 0. When $\overline{PFAIL}$ = 1 the chip is unlocked, but only after another 30 μs min → 63 μs max debounce time. The system designer must ensure that his system is stable when power has returned.

The power fail circuitry contains active linear circuitry that draws supply current from V_{CC}. In some cases this may be undesirable, so this circuit can be disabled by masking the power fail interrupt. The power fail input can perform all lock-out functions previously mentioned, except that no ex-

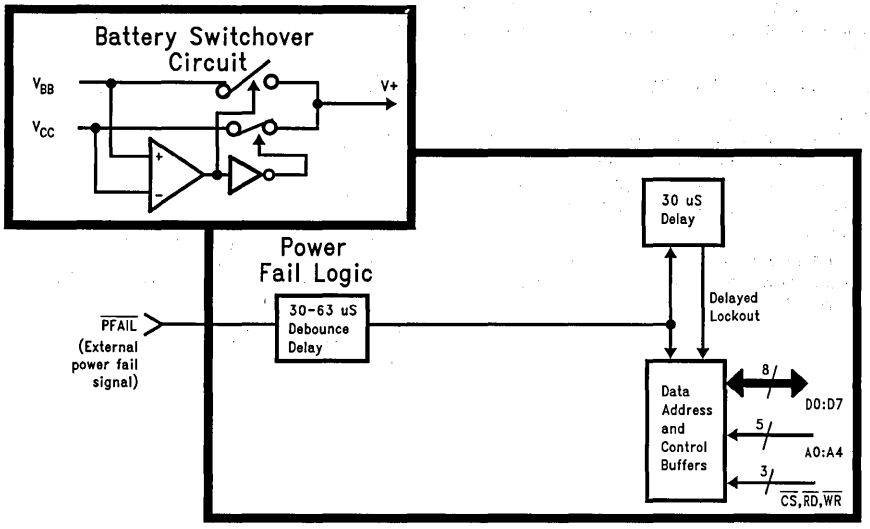

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FIGURE 6. System-Battery Switchover (Upper Left), Power Fail and Lock-Out Circuits (Lower Right)

Functional Description (Continued)

ternal interrupt will be issued. Note that the linear power fail circuitry is switched off automatically when using V_{BB} in standby mode.

INITIAL POWER ON DETECT AND POWER FAIL TIME SAVE

There are two other functions provided on the LV8573A to ease power supply control. These are an initial Power On detect circuit, which also can be used as a time keeping failure detect, and a time save on power failure.

On initial power up the Oscillator Fail Flag will be set to a one and the real time clock start bit reset to a zero. This indicates that an oscillator fail event has occurred, and time keeping has failed.

The Oscillator Fail flag will not be reset until the real-time clock is started. This allows the system to discriminate between an initial power-up and recovery from a power failure. If the battery backed mode is selected, then bit D6 of the Periodic Flag Register must be written low. This will not affect the contents of the Oscillator Fail Flag.

To relieve CPU overhead for saving time upon power failure, the Time Save Enable bit is provided to do this automatically. (See also Reading the Clock: Latched Read.) The Time Save Enable bit, when set, causes the Time Save RAM to follow the contents of the clock. This bit can be reset by software, but if set before a power failure occurs, it will automatically be reset when the clock switches to the battery supply (not when a power failure is detected by the $\overline{PFAIL}$ pin). Thus, writing a one to the Time Save bit enables both a software write or power fail write.

SINGLE POWER SUPPLY APPLICATIONS

The LV8573A can be used in a single power supply application. To achieve this, the V_{BB} pin must be connected to ground, and the power connected to V_{CC}. The Oscillator Failed/Single Supply bit in the Periodic Flag Register should be set to a logic 1, which will disable the oscillator battery reference circuit. The power fail interrupt should also be disabled. This will turn off the linear power fail detection circuits, and will eliminate any quiescent power drawn through these circuits.

DETAILED REGISTER DESCRIPTION

There are 5 external address bits: Thus, the host microprocessor has access to 28 locations at one time. An internal switching scheme provides a total of 30 locations.

The only register that does not get switched is the Main Status Register. It contains the register select bit as well as status information.

A memory map is shown in *Figure 2* and register addressing in Table III. They show the name, address and page locations for the LV8573A.

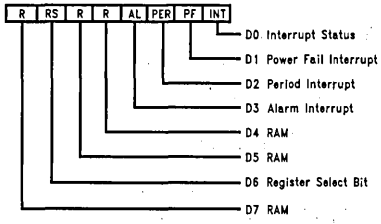
TABLE III. Register/Counter/RAM Addressing for LV8573A

A0-4	RS (Note 1)	Description	
CONTROL REGISTERS			
00	X	Main Status Register	
01	0	N/A	
02	0	N/A	
03	0	Periodic Flag Register	
04	0	Time Save Control Register	
01	1	Real Time Mode Register	
02	1	Output Mode Register	
03	1	Interrupt Control Register 0	
04	1	Interrupt Control Register 1	
COUNTERS (CLOCK CALENDAR)			
05	X	1/100, 1/10 Seconds	(0–99)
06	X	Seconds	(0–59)
07	X	Minutes	(0–59)
08	X	Hours	(1–12, 0–23)
09	X	Days of Month	(1–28/29/30/31)
0A	X	Months	(1–12)
0B	X	Years	(0–99)
0C	X	RAM	
0D	X	D0, D1 bits only	
0E	X	Day of Week	(1–7)
0F	X	N/A	
10	X	N/A	
11	X	N/A	
12	X	N/A	
TIME COMPARE RAM			
13	X	Sec Compare RAM	(0–59)
14	X	Min Compare RAM	(0–59)
15	X	Hours Compare RAM	(1–12, 0–23)
16	X	DOM Compare RAM	(1–28/29/30/31)
17	X	Months Compare RAM	(1–12)
18	X	DOW Compare RAM	(1–7)
TIME SAVE RAM			
19	X	Seconds Time Save RAM	
1A	X	Minutes Time Save RAM	
1B	X	Hours Time Save RAM	
1C	X	Day of Month Time Save RAM	
1D	X	Months Time Save RAM	
1E	1	RAM	
1F	X	RAM/Test Mode Register	

Note 1: RS—Register Select (Bit D6 of Main Status Register)

Functional Description (Continued)

MAIN STATUS REGISTER



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The Main Status Register is always located at address 0 regardless of the register block selected.

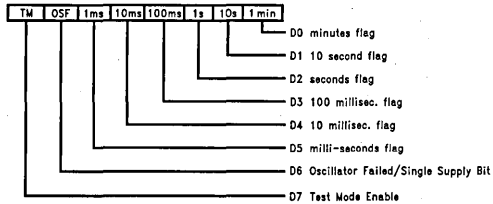
D0: This read only bit is a general interrupt status bit that is taken directly from the interrupt pins. The bit is a one when an interrupt is pending on either the $\overline{INTR}$ pin or the MFO pin (when configured as an interrupt). This is unlike D3 which can be set by an internal event but may not cause an interrupt. This bit is reset when the interrupt status bits in the Main Status Register are cleared.

D1–D3: These three bits of the Main Status Register are the main interrupt status bits. Any bit may be a one when any of the interrupts are pending. Once an interrupt is asserted the μP will read this register to determine the cause. These interrupt status bits are not reset when read. Except for D1, to reset an interrupt a one is written back to the corresponding bit that is being tested. D1 is reset whenever the $\overline{PFAIL}$ pin = logic 1. This prevents loss of interrupt status when reading the register in a polled mode. D1 and D3 are set regardless of whether these interrupts are masked or not by bits D6 and D7 of Interrupt Control Registers 0 and 1.

D4, D5 and D7: General purpose RAM bits.

D6: Bit D6 controls the register block to be accessed (see memory map).

PERIODIC FLAG REGISTER



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The Periodic Flag Register has the same bit for bit correspondence as Interrupt Control Register 0 except for D6 and D7. For normal operation (i.e., not a single supply application) this register must be written to on initial power up or after an oscillator fail event. D0–D5 are read only bits, D6 and D7 are read/write.

D0–D5: These bits are set by the real time rollover events: (Time Change = 1). The bits are reset when the register is read and can be used as selective data change flags.

D6: This bit performs a dual function. When this bit is read, a one indicates that an oscillator failure has occurred and the time information may have been lost. Some of the ways an oscillator failure can be caused are: failure of the crystal, shorting OSC IN or OSC OUT to GND or V_{CC}, removal of crystal, removal of battery when in the battery backed mode (when a "0" is written to D6), lowering the voltage at the V_{BB} pin to a value less than 2.2V when in the battery backed mode. Bit D6 is automatically set to 1 on initial power-up or an oscillator fail event. The oscillator fail flag is reset by writing a one to the clock start/stop bit in the Real Time Mode Register, with the crystal oscillating.

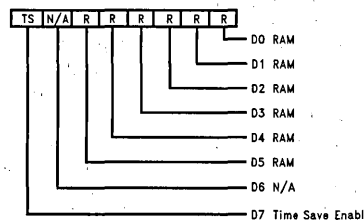
When D6 is written to, it defines whether the TCP is being used in battery backed (normal) or in a single supply mode application. When set to a one this bit configures the TCP for single power supply applications. This bit is automatically set on initial power-up or an oscillator fail event. When set, D6 disables the oscillator reference circuit. The result is that the oscillator is referenced to V_{CC}. When a zero is written to D6 the oscillator reference is enabled, thus the oscillator is referenced to V_{BB}. This allows operation in standard battery standby applications.

At initial power on, if the LV8573A is going to be programmed for battery backed mode, the V_{BB} pin should be connected to a potential in the range of 2.2V to V_{CC} − 0.4V.

For single supply mode operation, the V_{BB} pin should be connected to GND and the $\overline{PFAIL}$ pin connected to V_{CC}.

D7: Writing a one to this bit enables the test mode register at location 1F (see Table III). This bit should be forced to zero during initialization for normal operation. If the test mode has been entered, clear the test mode register before leaving test mode. (See separate test mode application note for further details.)

TIME SAVE CONTROL REGISTER



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D0–D5: General purpose RAM bits.

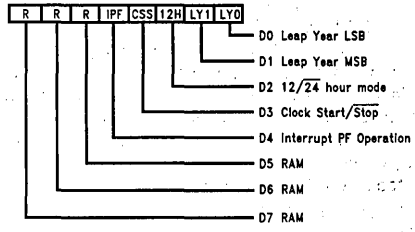
D6: Not Available, appears as logic 0 when read.

D7: Time Save Enable bit controls the loading of real-time-clock data into the Time Save RAM. When a one is written to this bit the Time Save RAM will follow the corresponding clock registers, and when a zero is written to this bit the time in the Time Save RAM is frozen. This eliminates any synchronization problems when reading the clock, thus negating the need to check for a counter rollover during a read cycle.

This bit must be set to a one prior to power failing to enable the Time Save feature. When the power fails this bit is automatically reset and the time is saved in the Time Save RAM.

Functional Description (Continued)

REAL TIME MODE REGISTER



TL/F/11418–15

D0–D1: These are the leap year counter bits. These bits are written to set the number of years from the previous leap year. The leap year counter increments on December 31st and it internally enables the February 29th counter state. This method of setting the leap year allows leap year to occur whenever the user wishes to, thus providing flexibility in implementing Japanese leap year function.

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

D2: The count mode for the hours counter can be set to either 24 hour mode or 12 hour mode with AM/PM indicator. A one will place the clock in 12 hour mode.

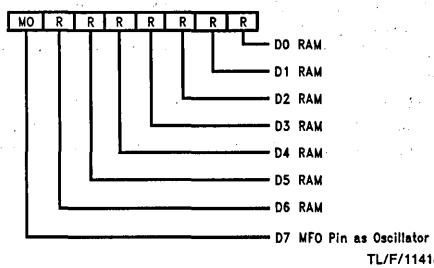
D3: This bit is the master Start/$\overline{\text{Stop}}$ bit for the clock. When a one is written to this bit the real time counter's prescaler and counter chain are enabled. When this bit is reset to zero the contents of the real time counter is stopped. When the RTC is initially powered up this bit will be held at a logic 0 until the oscillator starts functioning correctly after which this bit may be modified. If an oscillator fail event occurs, this bit will be reset to logic 0.

D4: This bit controls the operation of the interrupt output in standby mode. If set to a one it allows Alarm, Periodic, and Power Fail interrupts to be functional in standby mode. Note that the MFO pin is configured as open drain in standby mode.

If bit D4 is set to a zero then the interrupt control register and the periodic interrupt flag will be reset when the RTC enters the standby mode. They will have to be re-configured when system (V_{CC}) power is restored.

D5–D7: General purpose RAM bits.

OUTPUT MODE REGISTER



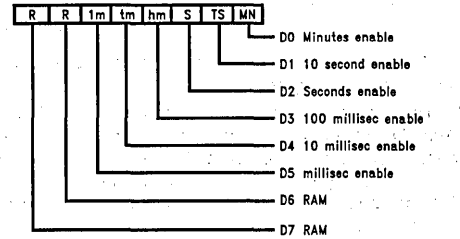
TL/F/11418–16

D0–D6: General purpose RAM bits.

D7: This bit is used to program the signal appearing at the MFO output, as follows:

D7	MFO Output Signal
0	Power Fail Interrupt
1	Buffered Crystal Oscillator

INTERRUPT CONTROL REGISTER 0

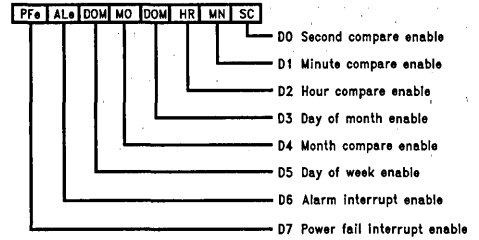


TL/F/11418–17

D0–D5: These bits are used to enable one of the selected periodic interrupts by writing a one into the appropriate bit. These interrupts are issued at the rollover of the clock. For example, the minutes interrupt will be issued whenever the minutes counter increments. In all likelihood the interrupt will be enabled asynchronously with the real time change. Therefore, the very first interrupt will occur in less than the periodic time chosen, but after the first interrupt all subsequent interrupts will be spaced correctly. These interrupts are useful when minute, second, real time reading, or task switching is required. When all six bits are written to a 0 this disables periodic interrupts from the Main Status Register and the interrupt pin.

D6 and D7: General purpose RAM.

INTERRUPT CONTROL REGISTER 1



TL/F/11418–18

D0–D5: Each of these bits are enable bits which will enable a comparison between an individual clock counter and its associated compare RAM. If any bit is a zero then that clock-RAM comparator is set to the "always equal" state and the associated TIME COMPARE RAM byte can be used as general purpose RAM. However, to ensure that an alarm interrupt is not generated at bit D3 of the Main Status Register, all bits must be written to a logic zero.

D6: In order to generate an external alarm compare interrupt to the μP from bit D3 of the Main Status Register, this bit must be written to a logic 1.

D7: The MSB of this register is the enable bit for the Power Fail Interrupt. When this bit is set to a one an interrupt will be generated to the μP when a $V_{BB} > V_{CC}$.

Control and Status Register Address Bit Map

Main Status Register PS = X RS = X ADDRESS = 00H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W[1]	R/W[1]	R[2]	R[3]
RAM	Register Select	RAM	RAM	Alarm Interrupt	Periodic Interrupt	Power Fail Interrupt	Interrupt Status

Periodic Flag Register PS = 0 RS = 0 Address = 03H

R/W	R/W[4]	R[5]	R[5]	R[5]	R[5]	R[5]	R[5]
Test Mode	Osc. Fail/ Single Supply	1 ms Flag	10 ms Flag	100 ms Flag	Seconds Flag	10 Second Flag	Minute Flag

1. Reset by writing 1 to bit.
2. Set/reset by voltage at $\overline{\text{PFAIL}}$ pin.
3. Reset when all pending interrupts are removed.
4. Read Osc fail Write 0 Batt-Backed Mode Write 1 Single Supply Mode
5. Reset by positive edge of read.

Time Save Control Register PS = 0 RS = 0 Address = 04H

Time Save Enable	N/A	RAM	RAM	RAM	RAM	RAM	RAM	All Bits R/W

Real Time Mode Register PS = 0 RS = 1 Address = 01H

RAM	RAM	RAM	Interrupt EN on Back-Up	Clock Start/$\overline{\text{Stop}}$	12/$\overline{24}$ Hr. Mode	Leap Year MSB	Leap Year LSB	All Bits R/W

Output Mode Register PS = 0 RS = 1 Address = 02H

MFO as Crystal	RAM	RAM	RAM	RAM	RAM	RAM	RAM	All Bits R/W

Interrupt Control Register 0 PS = 0 RS = 1 Address = 03H

RAM	RAM	1 ms Interrupt Enable	10 ms Interrupt Enable	100 ms Interrupt Enable	Seconds Interrupt Enable	10 Second Interrupt Enable	Minute Interrupt Enable	All Bits R/W

Interrupt Control Register 1 PS = 0 RS = 1 Address = 04H

Power Fail Interrupt Enable	Alarm Interrupt Enable	DOW Interrupt Enable	Month Interrupt Enable	DOM Interrupt Enable	Hours Interrupt Enable	Minute Interrupt Enable	Second Interrupt Enable	All Bits R/W

Application Hints

Suggested Initialization Procedure for LV8573A in Battery Backed Applications that use the V_{BB} Pin

1. Enter the test mode by writing a 1 to bit D7 in the Periodic Flag Register.
2. Write zero to the RAM/TEST mode Register located in page 0, address HEX 1F.
3. Leave the test mode by writing a 0 to bit D7 in the Periodic Flag Register. Steps 1, 2, 3 guarantee that if the test mode had been entered during power on (due to random pulses from the system), all test mode conditions are cleared. Most important is that the OSC Fail Disable bit is cleared. Refer to AN-589 for more information on test mode operation.
4. Enter a software loop that does the following:
   Set a 3 second(approx) software counter. The crystal oscillator may take 1 second to start.

4.1 Write a 1 to bit D3 in the Real Time Mode Register (try to start the clock). Under normal operation, this bit can be set only if the oscillator is running. During the software loop, RAM, real time counters, output configuration, interrupt control and timer functions may be initialized.

Application Hints (Continued)

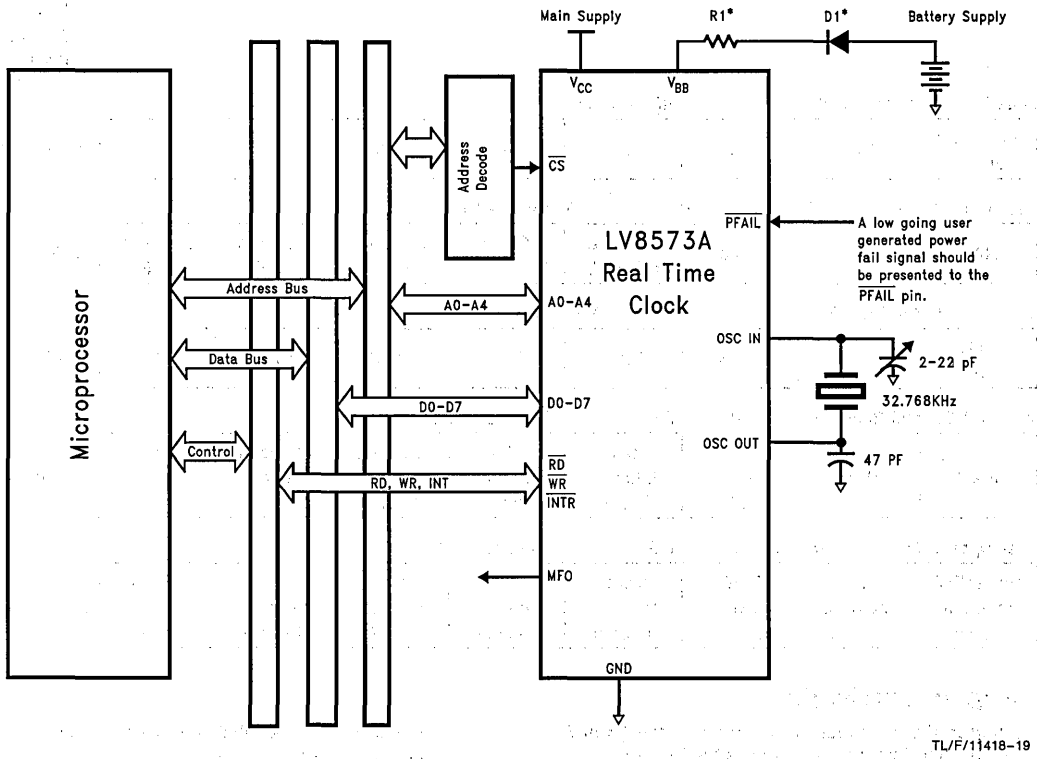
5. Test bit D6 in the Periodic Flag Register:

   IF a 1, go to 4.1. If this bit remains a 1 after 3 seconds, then abort and check hardware. The crystal may be defective or not installed. There may be a short at OSC IN or OSC OUT to V_{CC} or GND, or to some impedance that is less than 10 MΩ.

   IF a 0, then the oscillator is running, go to step 7.

6. Write a 0 to bit D6 in the Periodic Flag Register. This action puts the clock chip in the battery backed mode. This mode can be entered only if the OSC fail flag (bit D6 of the Periodic Flag Register) is a 0. Reminder, bit D6 is a dual function bit. When read, D6 returns oscillator status. When written, D6 causes either the Battery Backed Mode, or the Single Supply Mode of operation. The only method to ensure the chip is in the battery backed mode is to measure the waveform at the OSC OUT pin. If the battery backed mode was selected successfully, then the peak to peak waveform at OSC OUT is referenced to the battery voltage. If not in battery backed mode, the waveform is referenced to V_{CC}. The measurement should be made with a high impedance low capacitance probe (10 MΩ, 10 pF oscilloscope probe or better). Typical peak to peak swings are within 0.6V of V_{CC} and ground respectively.
7. Write a 1 to bit D7 of Interrupt Control Register 1. This action enables the PFAIL pin and associated circuitry.
8. Initialize the rest of the chip as needed.

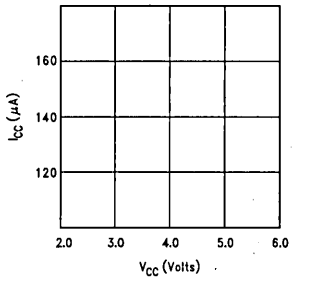
Typical Application



*These components may be necessary to meet UL requirements for lithium batteries. Consult battery manufacturer.

Typical Performance Characteristics

Operating Current vs Supply Voltage (Single Supply Mode F_{OSC} = 32.768 kHz) TBD



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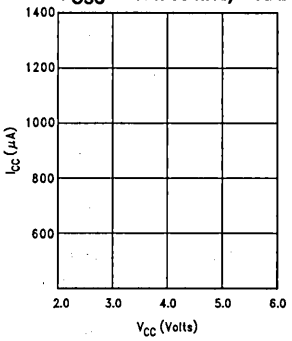
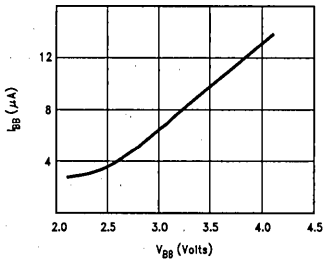
Operating Current vs Supply Voltage (Battery Backed Mode F_{OSC} = 32.768 kHz) TBD



TL/F/11418–21

Standby Current vs Power Supply Voltage (F_{OSC} = 32.768 kHz)



TL/F/11418–22

National Semiconductor

CGS54C/74C2525 • CGS54CT/74CT2525
CGS54C/74C2526 • CGS54CT/74CT2526
1-to-8 Minimum Skew Clock Driver

The CGS 'C/CT2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications. The '2525 is designed to distribute a single clock to eight separate receivers with low skew across all outputs during both the t_{PLH} and t_{PHL} transitions. The '2526 is similar to the '2525 but contains a multiplexed clock input to allow for systems with dual clock speeds or systems where a separate test clock has been implemented.

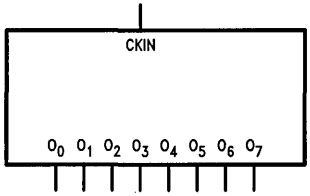
Features

- These CGS devices implement National's FACT™ family
- Ideal for signal generation and clock distribution
- Guaranteed pin to pin and part to part skew
- Multiplexed clock input ('2526)
- Guaranteed 2000V minimum ESD protection
- Symmetric output current drive of 24 mA for I_{OL}/I_{OH}
- 'CT has TTL-compatible inputs
- These products identical to 74AC/ACT2525 and 2526

Ordering Code: See Section 8

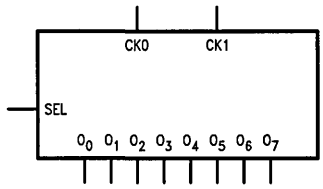
Logic Symbols

'2525



TL/F/10684–1

'2526

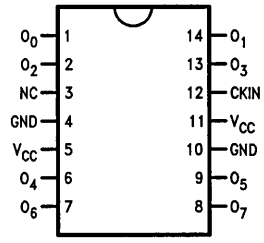


TL/F/10684–2

Connection Diagrams

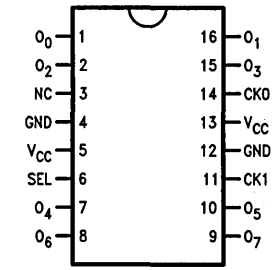
Pin Assignment for DIP, Flatpak and SOIC

'2525



TL/F/10684–3

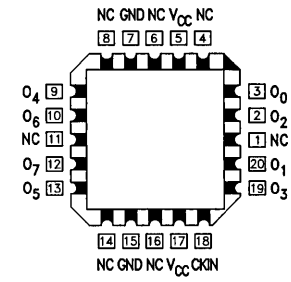
'2526



TL/F/10684–4

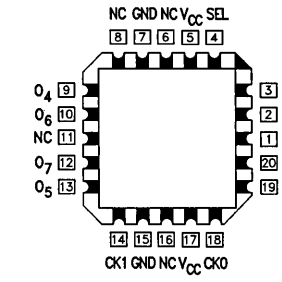
Pin Assignment for LCC

'2525



TL/F/10684–5

'2526



TL/F/10684–6

Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CK_n input will have an active effect on the outputs of the circuit. When SEL = 1, the CK_1 input is selected and when SEL = 0, the CK_0 input is selected. The non-selected CK_n input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK_{IN} or CK_1/CK_0 pins when either the multiplexed ('2526) or the straight ('2525) clock distribution chip is selected.

Pin Description

Pin Names	Description
CK_{IN}	Clock Input ('2525)
CK_0, CK_1	Clock Inputs ('2526)
O_0–O_7	Outputs
SEL	Clock Select ('2526)

Truth Tables

'2525

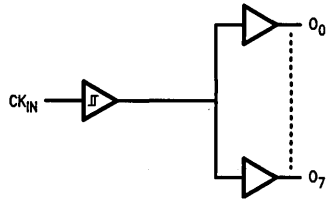
Inputs	Outputs
CK_{IN}	O_1–O_7
L	L
H	H

'2526

Inputs			Outputs
CK_0	CK_1	SEL	O_1–O_7
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

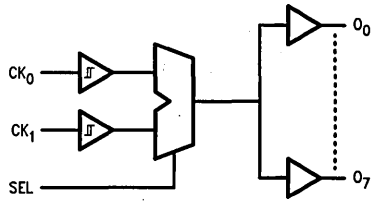
L = Low Voltage Level
H = High Voltage Level
X = Immaterial

'2525



TL/F/10684–7

'2526



TL/F/10684–8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+0.2 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = 0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 MA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of CGS circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'C	2.0V to 6.0V
'CT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
CGS74C/CT	−40°C to +85°C
CGS54C/CT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'C Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'CT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for CGS54C/74C Family Devices

Symbol	Parameter	V_{CC} (V)	CGS74C T_A = +25°C	CGS54C T_A = −55°C to +125°C	CGS74C T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		I_{OH} −24 mA
		5.5		4.86	4.7		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.40	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50		24 mA
		5.5		0.36	0.50		I_{OL} 24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for CGS54C/74C Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	CGS74C $T_A = +25°C$	CGS54C $T_A = -55°C$ to $+125°C$	CGS74C $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for CGS54C @ 25°C is identical to CGS74C @ 25°C.

DC Electrical Characteristics for CGS54CT/74CT Family Devices

Symbol	Parameter	V_{CC} (V)	CGS74CT $T_A = +25°C$		CGS54CT $T_A = -55°C$ to $+125°C$	CGS74CT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for CGS54CT @ 25°C is identical to CGS74CT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter		V_{CC}* (V)	CGS74C $T_A = +25°C$ $C_L = 50$ pF			CGS54C $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74C $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
				Min	Typ	Max	Min	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay CK to O_n ('2525)		3.3	3.0	6.5	11.0	3.0	11.0	3.0		12.5	ns
			5.0	3.2	5.0	7.8	2.5	8.2	2.9		8.1	
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n ('2526)		3.3	3.0	7.0	13.0			3.0		14.0	ns
			5.0	3.6	5.5	7.8			3.3		8.6	
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2526)		3.3	3.0	8.0	14.0			3.0		15.0	ns
			5.0	4.0	6.5	8.5			3.5		9.5	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		3.3		0.3	1.0		1.5			1.0	ns
			5.0		0.2	0.7		1.0			0.7	
t_{OSLH}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		3.3		0.3	1.0		1.5			1.0	ns
			5.0		0.2	0.7		1.0			0.7	
t_{OST}	Maximum Skew Opposite Edge Output-to-Output (Note 1) Variation		5.0		0.4	1.0		1.5			1.0	ns
								1.0				
t_{PV}	Maximum Skew Part-to-Part Variation (Note 2)	'C2525 'CT2525 'C2526	5.0			3.5		4.0				ns
		'CT2526	5.0			5.0						ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (20% to 80% V_{CC})		5.0			3.0		4.0			3.75	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (0.8V/2.0V and 2.0V/0.8V)				0.9					1.1		ns

*Voltage Range 3.3 is 3.3V ±0.3V

Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the CLK to Q propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	CGS74CT $T_A = +25°C$ $C_L = 50$ pF			CGS54CT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74CT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay CK to O_n ('2525)	5.0	4.6	6.5	9.0			4.0	10.1	ns
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n ('2526)	5.0	5.8	8.5	11.1			5.1	12.4	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC}* (V)	CGS74CT $T_A = +25°C$ $C_L = 50$ pF			CGS54CT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74CT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
				Min	Typ	Max	Min	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2526)		5.0	5.1	8.5	12.4			4.4		14.1	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		5.0		0.2	0.7					0.7	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		5.0		0.2	0.7					0.7	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output (Note 1) Variation		5.0		0.4	1.0					1.0	ns
t_{PV}	Maximum Skew Part-to-Part Variation (Note 2)	AC2525 ACT2525 AC2526	5.0			3.5						ns
		ACT2526	5.0			5.0						ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (20% to 80% V_{CC})		5.0			3.0					3.75	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (0.8V/2.0V and 2.0V/0.8V)				0.9					1.1		ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance ('2525)	820 pF−1.2 x 10^{-18} (f)*	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance ('2526)	820 pF−1.2 x 10^{-18} (f)*	pF	$V_{CC} = 5.0V$

*f = frequency

Recommended Maximum Power Dissipation (W)

LFPM	$T_A = 25°C$		$T_A = 85°C$	
	PDIP	SOIC	PDIP	SOIC
0	1.105	0.858	0.528	0.41
225	1.493	1.055	0.714	0.504
500	1.71	1.210	0.820	0.578

Section 4

Linear

Section 4 Contents

National Semiconductor

LM10/LM10B(L)/LM10C(L) Operational Amplifier and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV. Some other characteristics of the LM10 are

- input-offset voltage 2.0 mV (max)
- input-offset current 0.7 nA (max)
- input-bias current 20 nA (max)
- reference regulation 0.1% (max)
- offset-voltage drift 2μV/°C
- reference drift 0.002%/°C

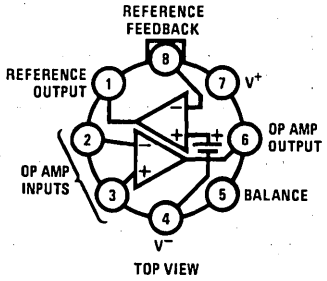
The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Connection and Functional Diagrams

Metal Can Package (H)

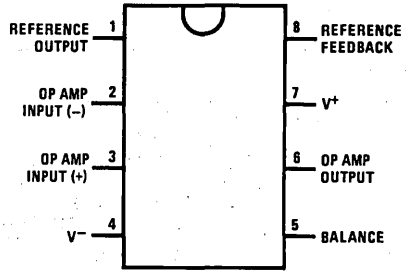


TOP VIEW

TL/H/5652-1

Order Number LM10H, LM10BH, LM10CH, LM10BLH or LM10CLH
See NS Package Number H08A

Dual-In-Line Package (N)

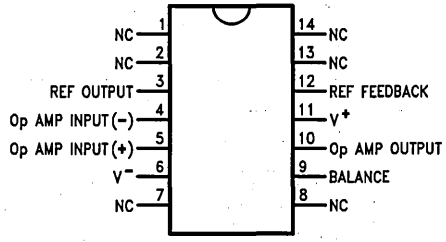


TOP VIEW

TL/H/5652-15

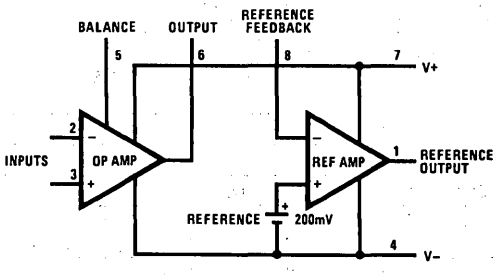
Order Number LM10CN or LM10CLN
See NS Package Number N08E

Small Outline Package (M)



TL/H/5652-17

Order Number LM10CWM or LM10CLWM
See NS Package Number M14B



TL/H/5652-16

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

	LM10/LM10B/LM10C	LM10BL/LM10CL
Total Supply Voltage	45V	7V
Differential Input Voltage (note 1)	±40V	±7V
Power Dissipation (note 2)	internally limited	
Output Short-circuit Duration (note 3)	continuous	
Storage-Temp. Range	−55°C to +150°C	
Lead Temp. (Soldering, 10 seconds) Metal Can	300°C	
Lead Temp. (Soldering, 10 seconds) DIP	260°C	
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

Electrical Characteristics

$T_J = 25°C$, $T_{MIN} \leq T_J \leq T_{MAX}$ (note 4) **(Boldface type refers to limits over temperature range)**

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0 **3.0**		0.5	4.0 **5.0**	mV mV
Input offset current (note 5)			0.25	0.7 **1.5**		0.4	2.0 **3.0**	nA nA
Input bias current			10	20 **30**		12	30 **40**	nA nA
Input resistance		250 **150**	500		150 **115**	400		kΩ kΩ
Large signal voltage gain	$V_S = \pm 20V$, $I_{OUT} = 0$ $V_{OUT} = \pm 19.95V$ $V_S = \pm 20V$, $V_{OUT} = \pm 19.4V$ $I_{OUT} = \pm 20$ mA **(± 15 mA)** $V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA $V_{OUT} = \pm 0.4V$ **(±0.3V)**, $V_{CM} = -0.4V$	120 **80** 50 **20** 1.5 **0.5**	400 130 3.0 		80 **50** 25 **15** 1.0 **0.75**	400 130 3.0 		V/mV V/mV V/mV V/mV V/mV V/mV
Shunt gain (note 6)	1.2V **(1.3V)** ≤ V_{OUT} ≤ 40V, $R_L = 1.1$ kΩ 0.1 mA ≤ I_{OUT} ≤ 5 mA 1.5V ≤ V^+ ≤ 40V, $R_L = 250\Omega$ 0.1 mA ≤ I_{OUT} ≤ 20 mA	14 **6** 8 **4**	33 25 		10 **6** 6 **4**	33 25 		V/mV V/mV V/mV V/mV
Common-mode rejection	−20V ≤ V_{CM} ≤ 19.15V **(19V)** $V_S = \pm 20V$	93 **87**	102		90 **87**	102		dB dB
Supply-voltage rejection	−0.2V ≥ V^- ≥ −39V $V^+ = 1.0V$ **(1.1V)** 1.0V **(1.1V)** ≤ V^+ ≤ 39.8V $V^- = -0.2V$	90 **84** 96 **90**	96 106 		87 **84** 93 **90**	96 106 		dB dB dB dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift	$T_C < 100°C$		60			90		pA/°C
Line regulation	1.2V **(1.3V)** ≤ V_S ≤ 40V 0 ≤ I_{REF} ≤ 1.0 mA, $V_{REF} = 200$ mV		0.001	0.003 **0.006**		0.001	0.008 **0.01**	%/V %/V
Load regulation	0 ≤ I_{REF} ≤ 1.0 mA $V^+ - V_{REF} \geq 1.0V$ **(1.1V)**		0.01	0.1 **0.15**		0.01	0.15 **0.2**	% %

Electrical Characteristics

$T_J = 25°C$, $T_{MIN} \le T_J \le T_{MAX}$, (note 4) **(Boldface type refers to limits over temperature range)** (Continued)

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Amplifier gain	$0.2V \le V_{REF} \le 35V$	50 **23**	75		25 **15**	70		V/mV V/mV
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			270	400 **500**		300	500 **570**	μA μA
Supply current change	1.2V **(1.3V)** $\le V_S \le$ 40V		15	**75**		15	**75**	μA

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0 **3.0**		0.5	4.0 **5.0**	mV mV
Input offset current (note 5)			0.1	0.7 **1.5**		0.2	2.0 **3.0**	nA nA
Input bias current			10	20 **30**		12	30 **40**	nA nA
Input resistance		250 **150**	500		150 **115**	400		kΩ kΩ
Large signal voltage gain	$V_S = \pm 3.25V$, $I_{OUT} = 0$ $V_{OUT} = \pm 3.2V$ $V_S = \pm 3.25V$, $I_{OUT} = 10$ mA $V_{OUT} = \pm 2.75$ V $V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA $V_{OUT} = \pm 0.4V$ **($\pm$0.3V)**, $V_{CM} = -0.4V$	60 **40** 10 **4** 1.5 **0.5**	300 25 3.0 		40 **25** 5 **3** 1.0 **0.75**	300 25 3.0 		V/mV V/mV V/mV V/mV V/mV V/mV
Shunt gain (note 6)	$1.5V \le V^+ \le 6.5V$, $R_L = 500\Omega$ 0.1 mA $\le I_{OUT} \le$ 10 mA	8 **4**	30		6 **4**	30		V/mV V/mV
Common-mode rejection	$-3.25V \le V_{CM} \le 2.4V$ **(2.25V)** $V_S = \pm 3.25V$	89 **83**	102		80 **74**	102		dB dB
Supply-voltage rejection	$-0.2V \ge V^- \ge -5.4V$ $V^+ = 1.0V$ **(1.2V)** 1.0V **(1.1V)** $\le V^+ \le 6.3V$ $V^- = 0.2V$	86 **80** 94 **88**	96 106 		80 **74** 80 **74**	96 106 		dB dB dB dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift			60			90		pA/°C
Line regulation	1.2V **(1.3V)** $\le V_S \le$ 6.5V $0 \le I_{REF} \le$ 0.5 mA, $V_{REF} = 200$ mV		0.001	0.01 **0.02**		0.001	0.02 **0.03**	%/V %/V
Load regulation	$0 \le I_{REF} \le$ 0.5 mA $V^+ - V_{REF} \ge$ 1.0V **(1.1V)**		0.01	0.1 **0.15**		0.01	0.15 **0.2**	% %
Amplifier gain	$0.2V \le V_{REF} \le 5.5V$	30 **20**	70		20 **15**	70		V/mV V/mV

Electrical Characteristics

$T_J = 25°C$, $T_{MIN} \leq T_J \leq T_{MAX}$, (note 4) **(Boldface type refers to limits over temperature range)** (Continued)

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			260	400 **500**		280	500 **570**	μA μA

Note 1: The Input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.

Note 2: The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

Note 3: Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

Note 4: These specifications apply for $V^- \leq V_{CM} \leq V^+ - 0.85V$ **(1.0V)**, 1.2V **(1.3V)** $< V_S \leq V_{MAX}$, $V_{REF} = 0.2V$ and $0 \leq I_{REF} \leq 1.0$ mA, unless otherwise specified: $V_{MAX} = 40V$ for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation;** this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \cong 20$ ms), die heating ($\tau_2 \cong 0.2$s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

Note 5: For $T_J > 90°C$, I_{OS} may exceed 1.5 nA for $V_{CM} = V^-$. With $T_J = 125°C$ and $V^- \leq V_{CM} \leq V^- + 0.1V$, $I_{OS} \leq 5$ nA.

Note 6: This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Note 7: Refer to RETS10X for LM10H military specifications.

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the unloaded output is in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

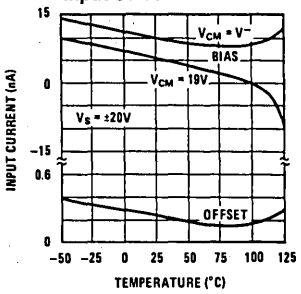
Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

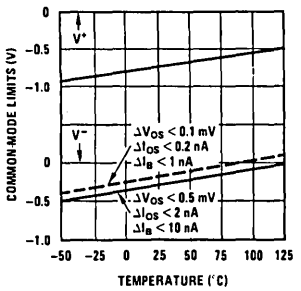
Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

Typical Performance Characteristics (Op Amp)

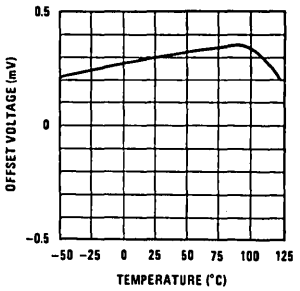
Input Current



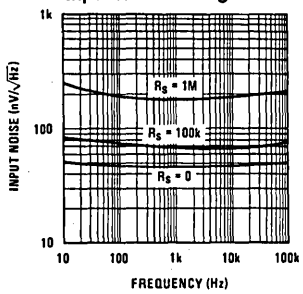
Common Mode Limits



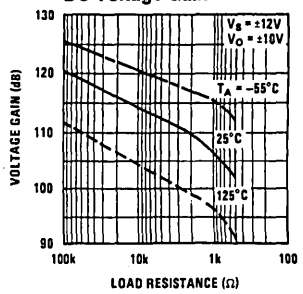
Offset Voltage Drift



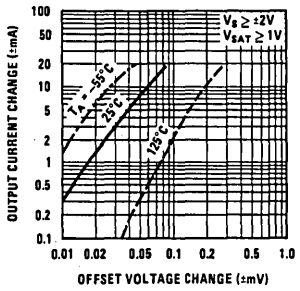
Input Noise Voltage



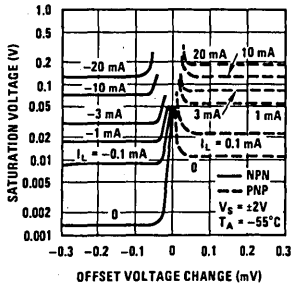
DC Voltage Gain



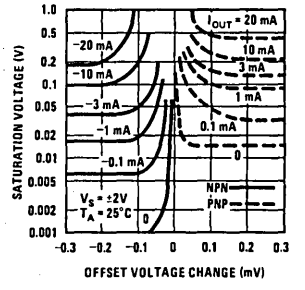
Transconductance



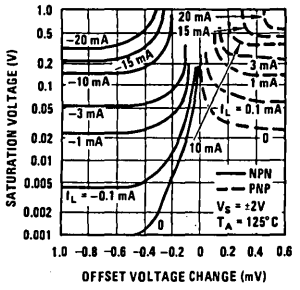
Output Saturation Characteristics



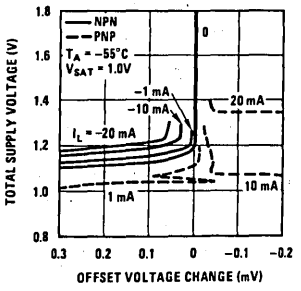
Output Saturation Characteristics



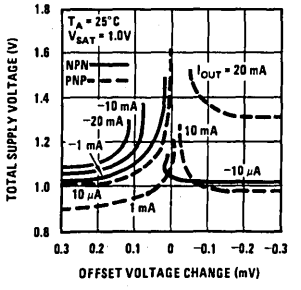
Output Saturation Characteristics



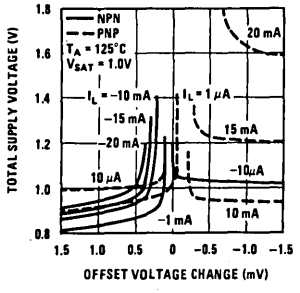
Minimum Supply Voltage



Minimum Supply Voltage



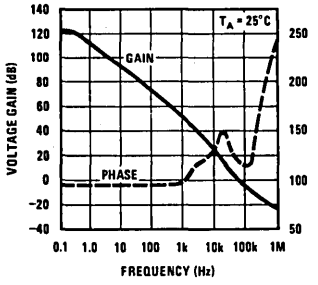
Minimum Supply Voltage



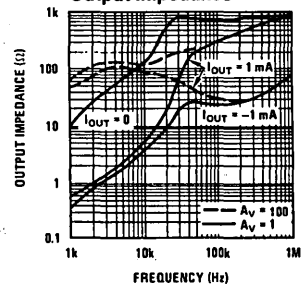
TL/H/5652–2

Typical Performance Characteristics (Op Amp) (Continued)

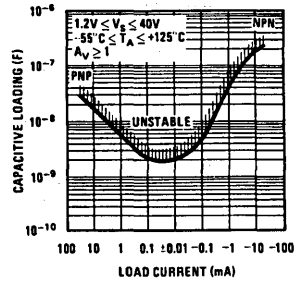
Frequency Response



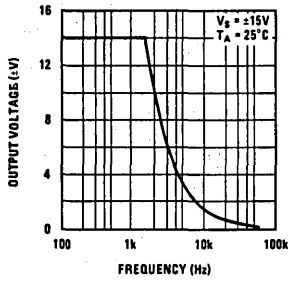
Output Impedance



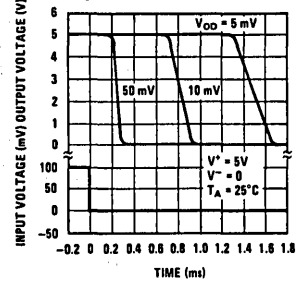
Typical Stability Range



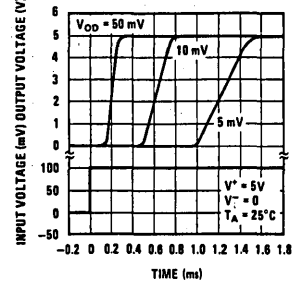
Large Signal Response



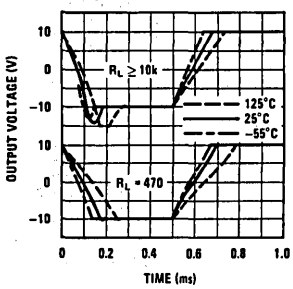
Comparator Response Time For Various Input Overdrives



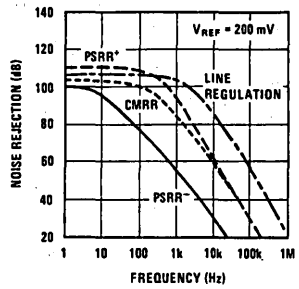
Comparator Response Time For Various Input Overdrives



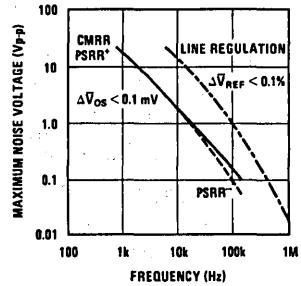
Follower Pulse Response



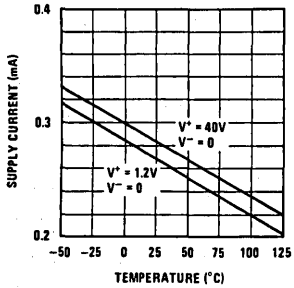
Noise Rejection



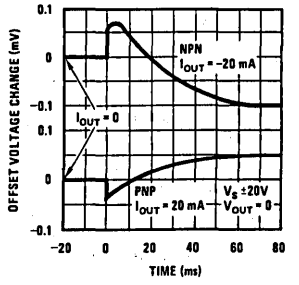
Rejection Slew Limiting



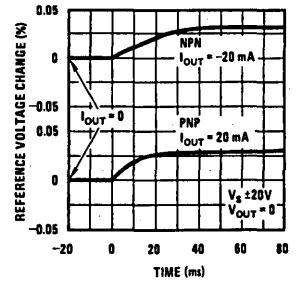
Supply Current



Thermal Gradient Feedback

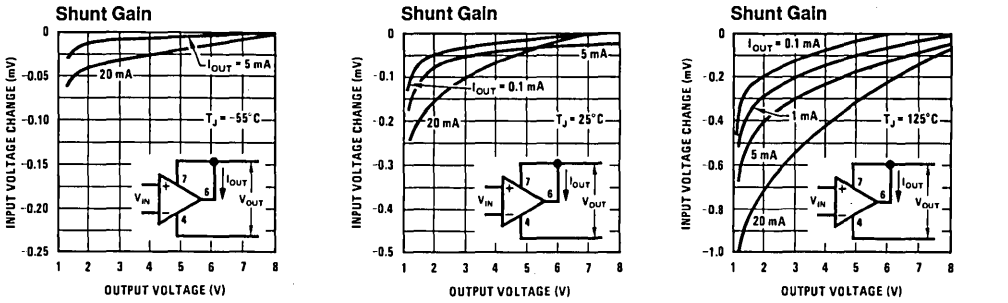


Thermal Gradient Cross-coupling



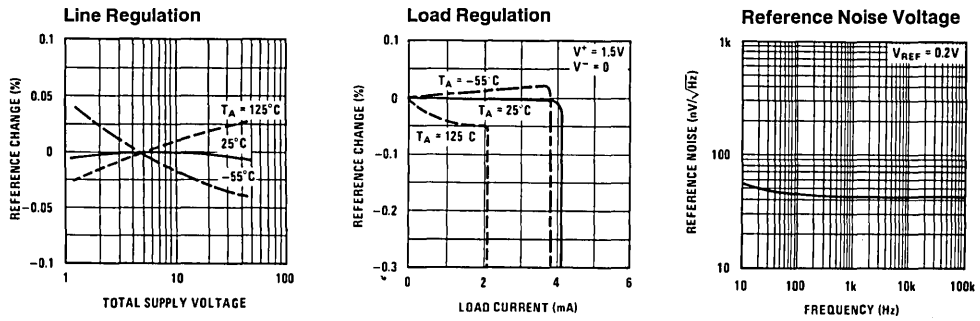
TL/H/5652–3

Typical Performance Characteristics (Op Amp) (Continued)



TL/H/5652–4

Typical Performance Characteristics (Reference)

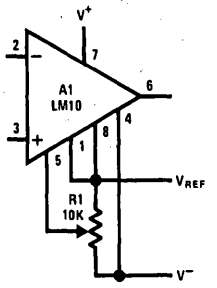


TL/H/5652–5

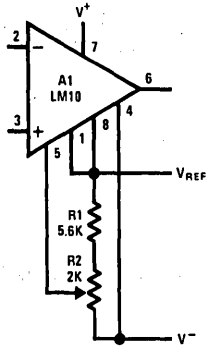
Typical Applications†† (Pin numbers are for devices in 8-pin packages)

Op Amp Offset Adjustment

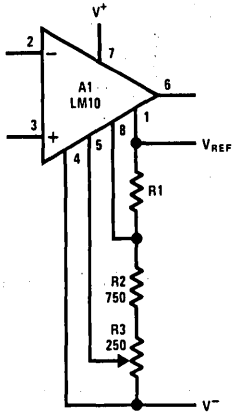
Standard



Limited Range

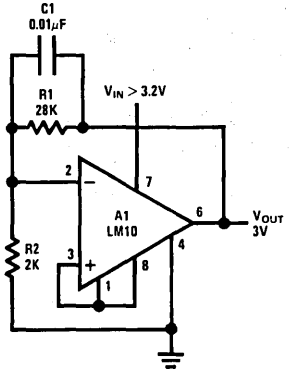


Limited Range With Boosted Reference

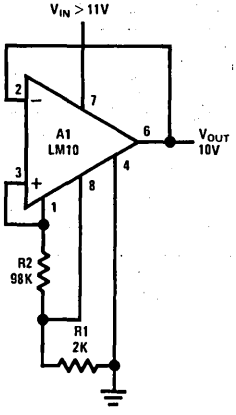


Positive Regulators†

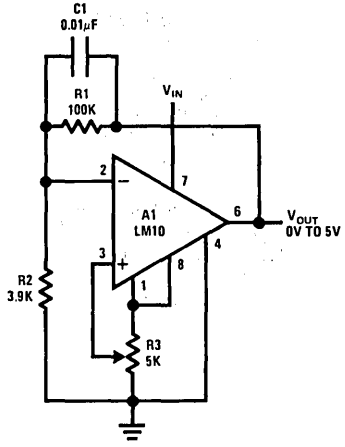
Low Voltage



Best Regulation



Zero Output



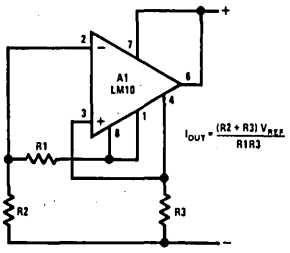
TL/H/5652–6

†Use only electrolytic output capacitors.

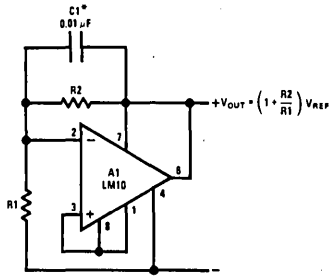
††Circuit descriptions available in application note AN-211.

Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

Current Regulator

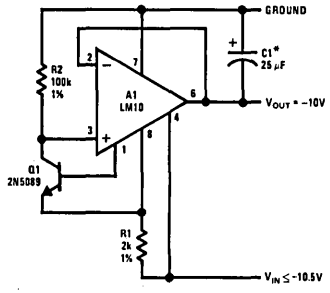


Shunt Regulator



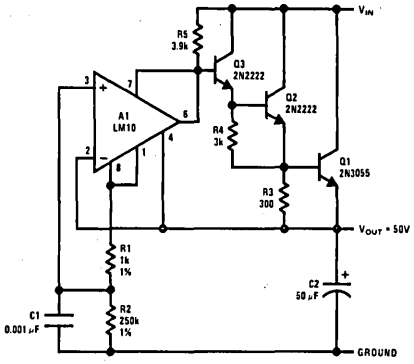
*Required For Capacitive Loading

Negative Regulator

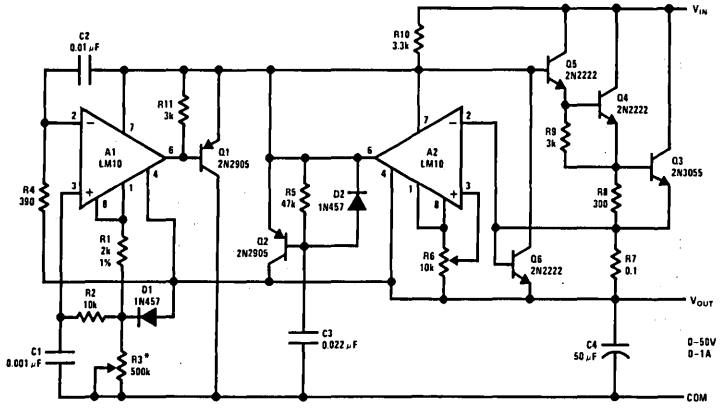


*Electrolytic

Precision Regulator



Laboratory Power Supply



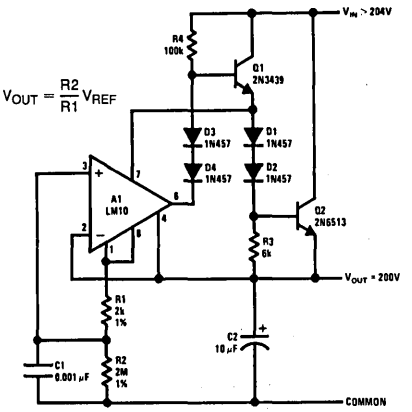
TL/H/5652-7

*$V_{OUT} = 10^{-4}$ R3

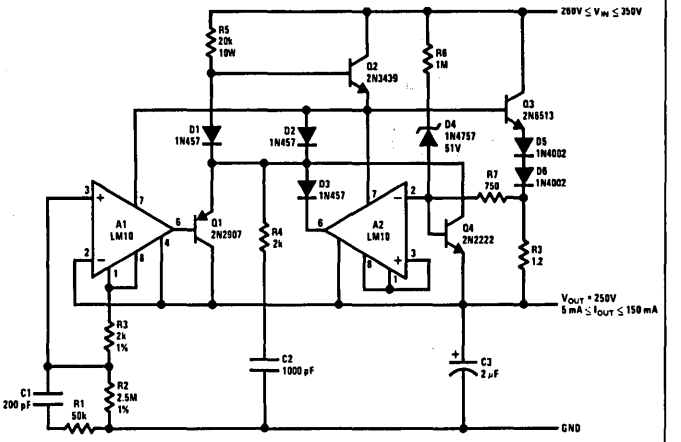
††Circuit descriptions available in application note AN-211.

Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

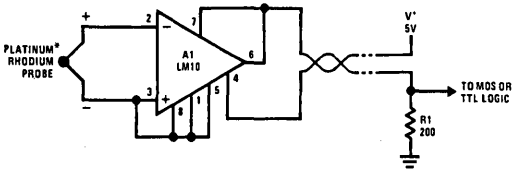
HV Regulator



Protected HV Regulator

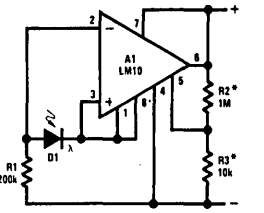


Flame Detector



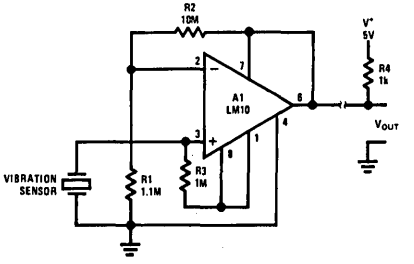
*800°C Threshold Is Established By Connecting Balance To V_{REF}.

Light Level Sensor

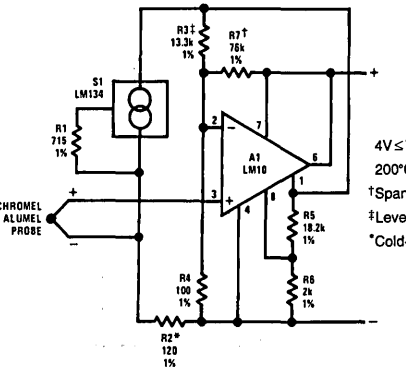


*Provides Hysteresis

Remote Amplifier



Remote Thermocouple Amplifier



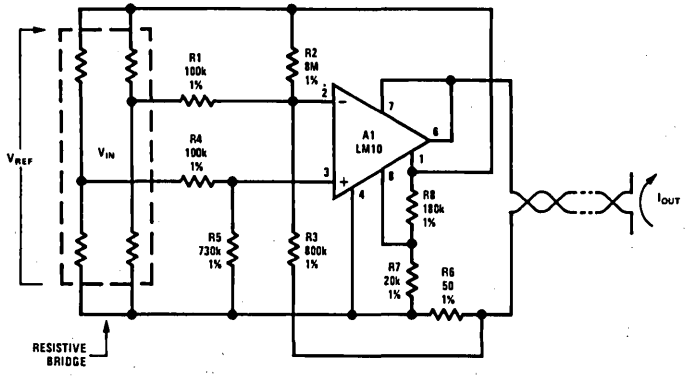
$4V \leq V_{OUT} \leq 20V$
$200°C \leq T_P \leq 700°C$
†Span Trim
‡Level-shift Trim
*Cold-junction Trim

TL/H/5652–8

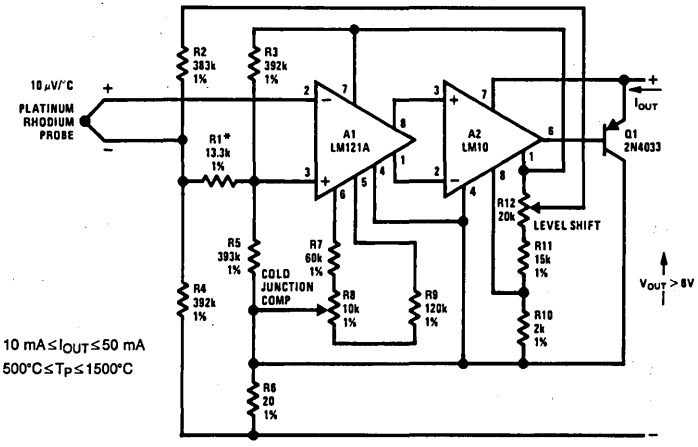
††Circuit descriptions available in application note AN-211.

Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Transmitter for Bridge Sensor

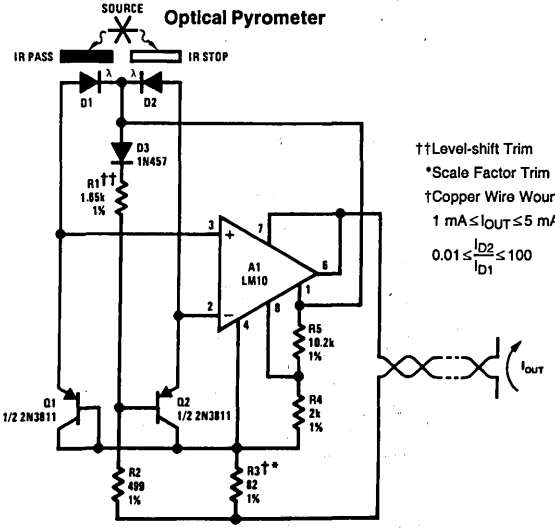


Precision Thermocouple Transmitter



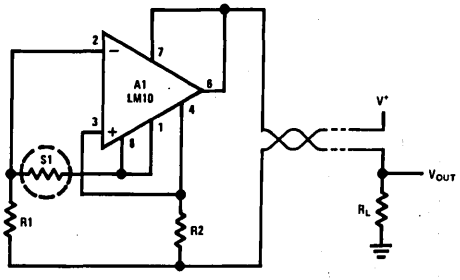
*Gain Trim

Optical Pyrometer



††Level-shift Trim
*Scale Factor Trim
†Copper Wire Wound
1 mA ≤ I_{OUT} ≤ 5 mA
$0.01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$

Resistance Thermometer Transmitter



††Circuit descriptions available in application note AN-211.

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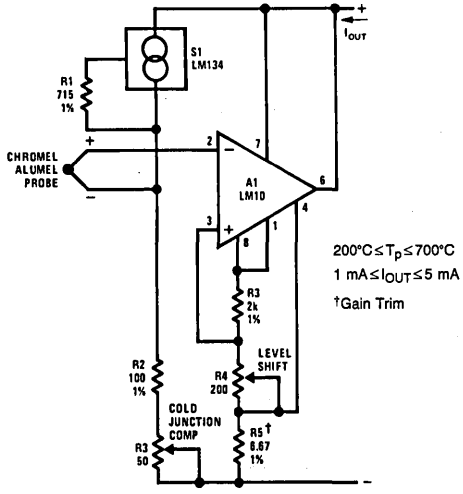
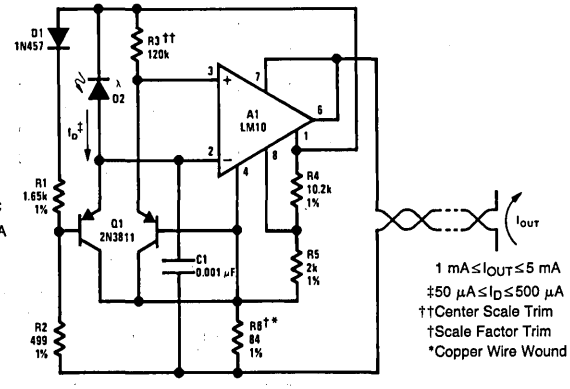
Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Thermocouple Transmitter



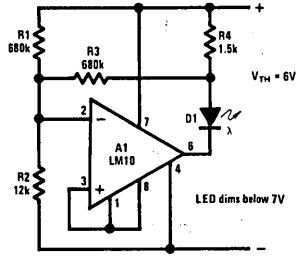
200°C≤T_p≤700°C
1 mA≤I_{OUT}≤5 mA
†Gain Trim

Logarithmic Light Sensor

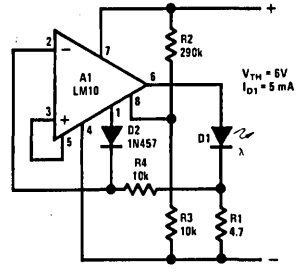


1 mA≤I_{OUT}≤5 mA
‡50 μA≤I_D≤500 μA
††Center Scale Trim
†Scale Factor Trim
*Copper Wire Wound

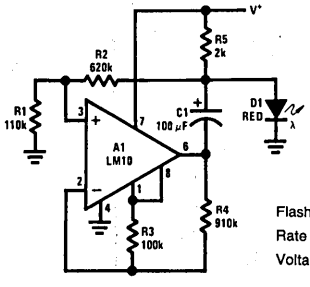
Battery-level Indicator



Battery-threshold Indicator

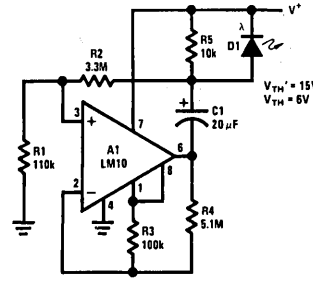


Single-cell Voltage Monitor



Flashes Above 1.2V
Rate Increases With
Voltage

Double-ended Voltage Monitor



Flash Rate Increases
Above 6V and Below 15V

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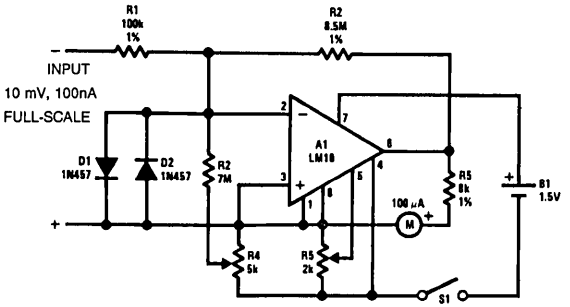
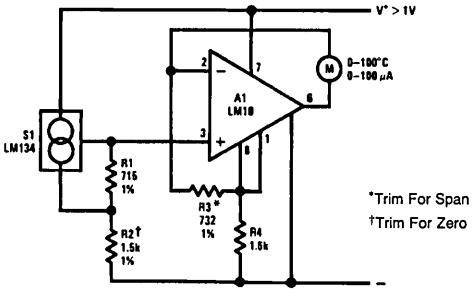
††Circuit descriptions available in application note AN-211.

Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

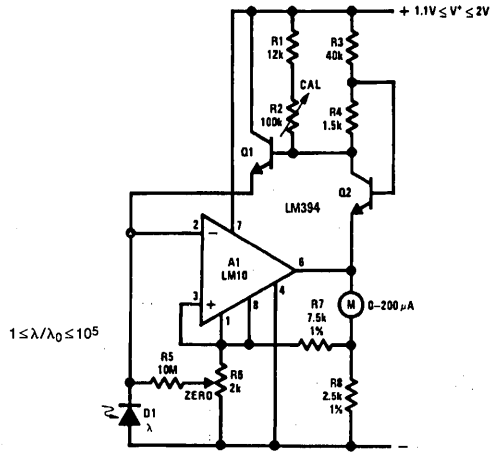
Meter Amplifier



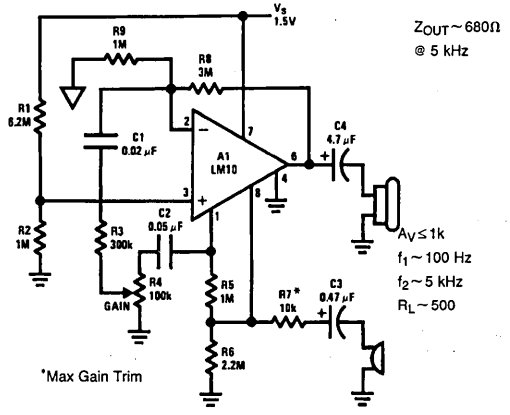
Thermometer



Light Meter



Microphone Amplifier



††Circuit descriptions available in application note AN-211.

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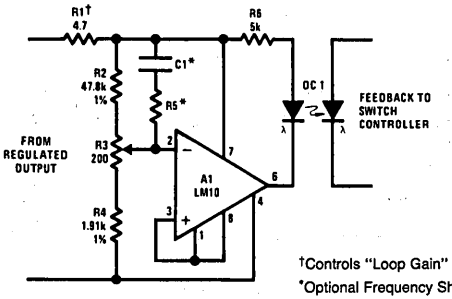
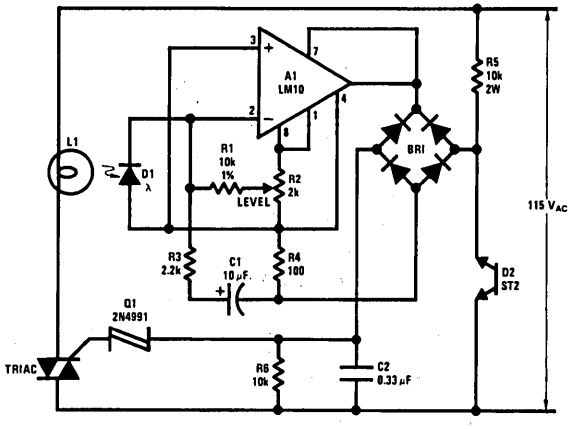
Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Isolated Voltage Sensor



†Controls "Loop Gain"
*Optional Frequency Shaping

Light-level Controller



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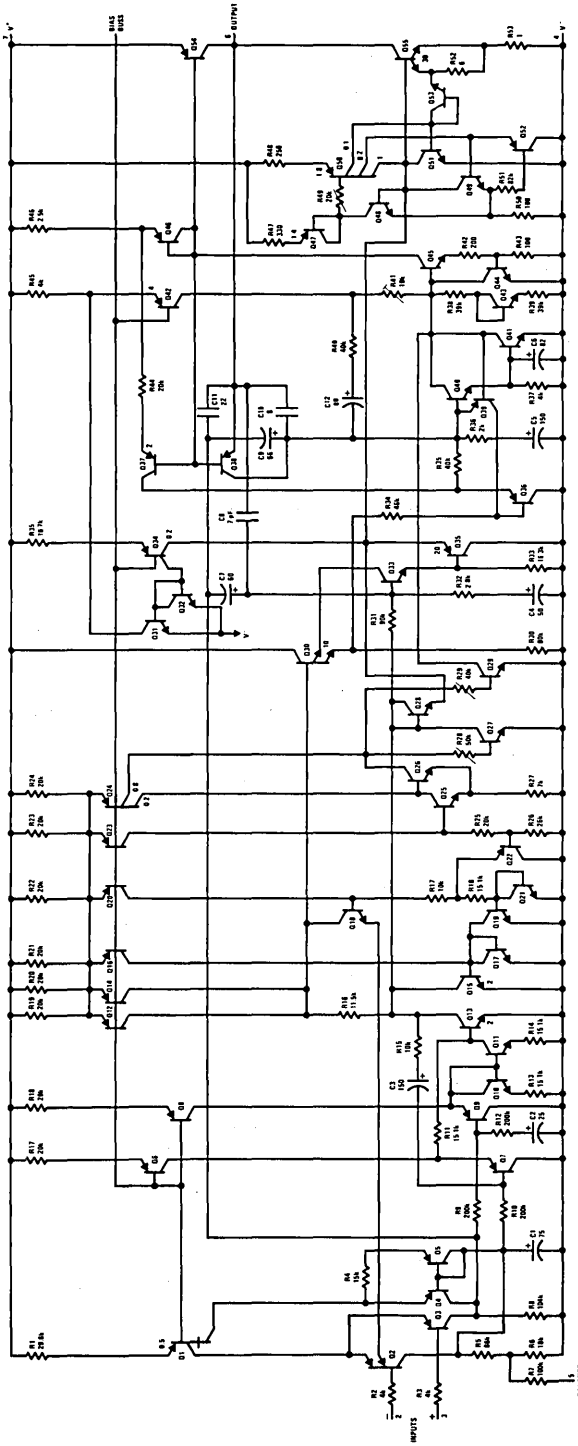
††Circuit descriptions available in application note AN-211.

Application Hints

With heavy amplifier loading to V−, resistance drops in the V− lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

Operational Amplifier Schematic (Pin numbers are for 8-pin packages)



TL/H/5652–13

Reference and Internal Regulator (Pin numbers are for 8-pin packages)

National Semiconductor

LM4250/LM4250C Programmable Operational Amplifier

General Description

The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

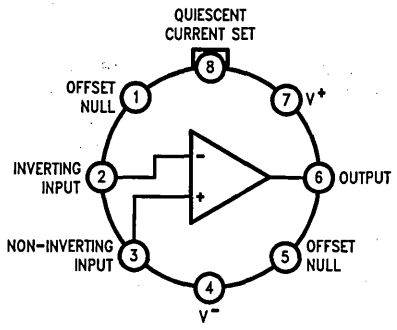
The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to +70°C temperature range instead of the −55°C to +125°C temperature range of the LM4250.

Features

- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

Connection Diagrams

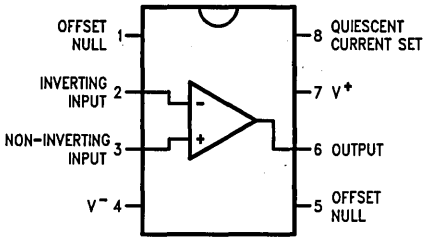
Metal Can Package



TL/H/9300-2

Top View

Dual-In-Line Package



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Top View

Ordering Information

Temperature Range		Package	NSC Package Number
Military $-55°C \leq T_A \leq +125°C$	Commercial $0°C \leq T_A \leq +70°C$		
	LM4250CN	8-Pin Molded DIP	N08E
	LM4250CM	8-Pin Surface Mount	M08E
LM4250J LM4250J-MIL	LM4250CJ	8-Pin Ceramic DIP	J08E
LM4250H LM4250H-MIL	LM4250CH	8-Pin Metal Can	H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 2)

	LM4250	LM4250C
Supply Voltage	±18V	±18V
Operating Temp. Range	$-55°C \le T_A \le +125°C$	$0°C \le T_A \le +70°C$
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
I_{SET} Current	150 nA	150 nA
Output Short Circuit Duration	Continuous	Continuous
T_{JMAX}		
H-Package	150°C	100°C
N-Package		100°C
J-Package	150°C	100°C
M-Package		100°C
Power Dissipation at $T_A = 25°C$		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	1200 mW
N-Package		500 mW
J-Package	1000 mW	600 mW
M-Package		350 mW
Thermal Resistance (Typical) θ_{JA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	65°C/W	65°C/W
N-Package		130°C/W
J-Package	108°C/W	108°C/W
M-Package		190°C/W
(Typical) θ_{JC}		
H-Package	21°C/W	21°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 3) 800V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Refer to RETS4250X for military specifications.

Note 3: Human body model, 1.5 kΩ in series with 100 pF.

Resistor Biasing

Set Current Setting Resistor to V⁻

	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

Electrical Characteristics LM4250 ($-55°C \le T_A \le +125°C$ unless otherwise specified.) $T_A = T_J$

Parameter	Conditions	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 0.6V$, $R_L = 10\ k\Omega$	40k		50k	
Supply Current	$T_A = 25°C$		7.5 μA		80 μA
Power Consumption	$T_A = 25°C$		23 μW		240 μW
V_{OS}	$R_S \le 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = +125°C$ $T_A = -55°C$		5 nA 3 nA		10 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		$\pm 0.6V$		$\pm 0.6V$	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	30k		30k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	$\pm 0.6V$		$\pm 0.6V$	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	76 dB		76 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

Parameter	Conditions	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 10\ k\Omega$	100k		100k	
Supply Current	$T_A = 25°C$		10 μA		90 μA
Power Consumption	$T_A = 25°C$		300 μW		2.7 mW
V_{OS}	$R_S \le 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = +125°C$ $T_A = -55°C$		25 nA 3 nA		25 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		$\pm 13.5V$		$\pm 13.5V$	
Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	$\pm 12V$		$\pm 12V$	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	76 dB		76 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

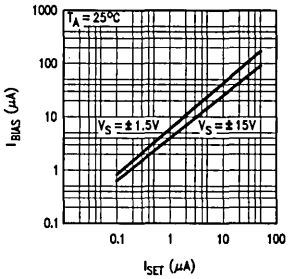
Electrical Characteristics LM4250C ($0°C \le T_A \le +70°C$ unless otherwise specified.) $T_A = T_J$

Parameter	Conditions	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 0.6V$, $R_L = 10\ k\Omega$	25k		25k	
Supply Current	$T_A = 25°C$		8 μA		90 μA
Power Consumption	$T_A = 25°C$		24 μW		270 μW
V_{OS}	$R_S \le 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		$\pm 0.6V$		$\pm 0.6V$	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	25k		25k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	$\pm 0.6V$		$\pm 0.6V$	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	74 dB		74 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

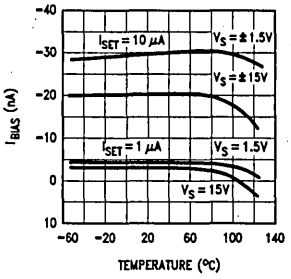
Parameter	Conditions	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 10\ k\Omega$	60k		60k	
Supply Current	$T_A = 25°C$		11 μA		100 μA
Power Consumption	$T_A = 25°C$		330 μW		3 mW
V_{OS}	$R_S \le 100\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		$\pm 13.5V$		$\pm 13.5V$	
Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	$\pm 12V$		$\pm 12V$	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	74 dB		74 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

Typical Performance Characteristics

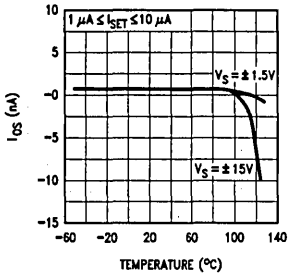
Input Bias Current vs I_{SET}



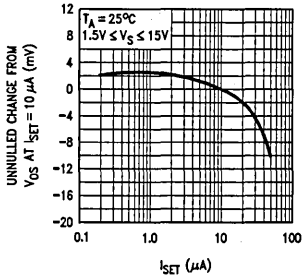
Input Bias Current vs Temperature



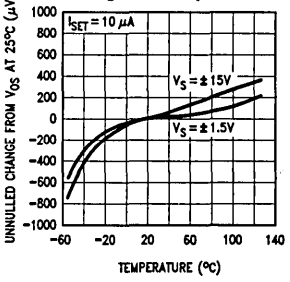
Input Offset Current vs Temperature



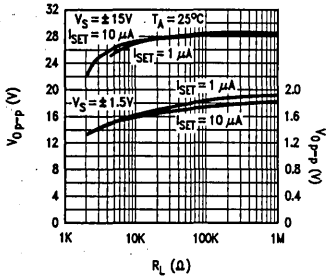
Unnulled Input Offset Voltage Change vs I_{SET}



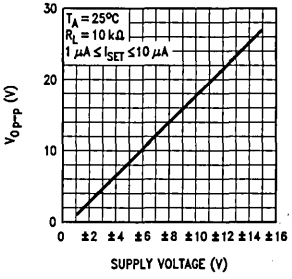
Unnulled Input Offset Voltage Change vs Temperature



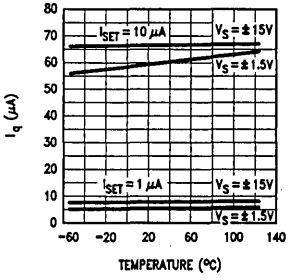
Peak to Peak Output Voltage Swing vs Load Resistance



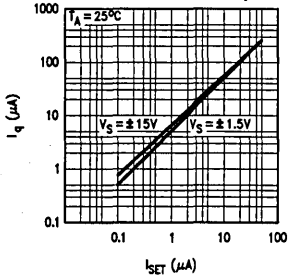
Peak to Peak Output Voltage Swing vs Supply Voltage



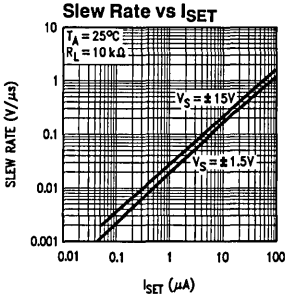
Quiescent Current (I_Q) vs Temperature



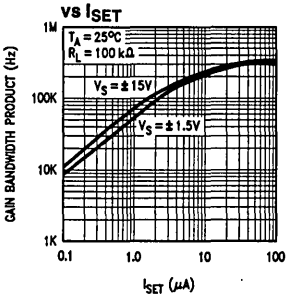
Quiescent Current (I_Q) vs I_{SET}



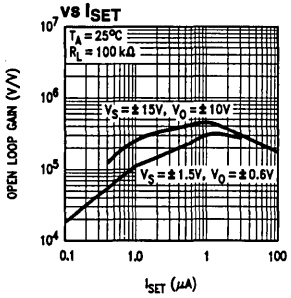
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}



Open Loop Voltage Gain vs I_{SET}



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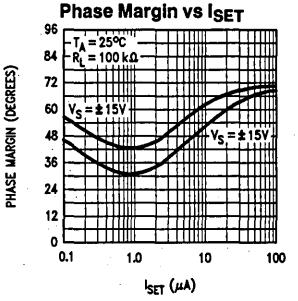
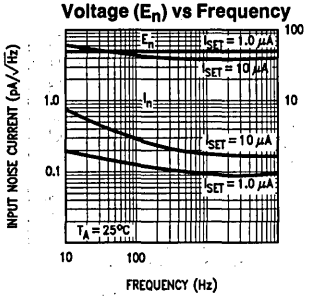
4

Typical Performance Characteristics (Continued)

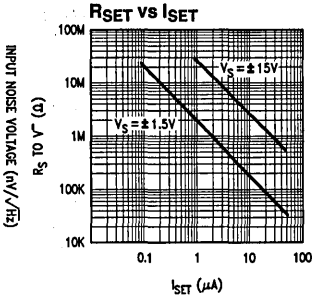
Phase Margin vs I_{SET}



Input Noise Current (I_n) and Voltage (E_n) vs Frequency



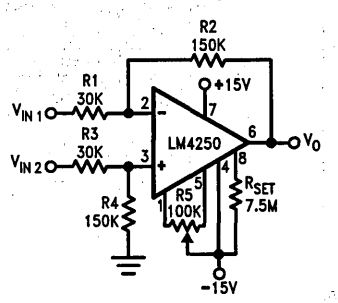
R_{SET} vs I_{SET}



TL/H/9300-7

Typical Applications

X5 Difference Amplifier



Quiescent P_D = 0.6 mW

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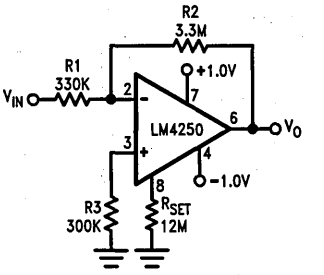
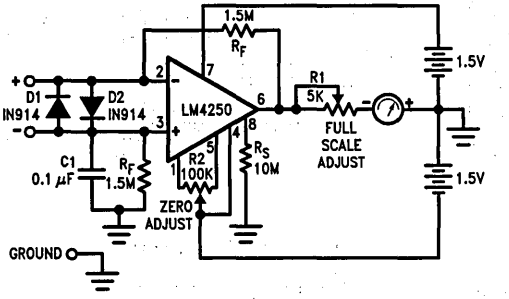
500 Nano-Watt X10 Amplifier



TL/H/9300-4

Quiescent P_D = 500 nW

Floating Input Meter Amplifier
100 nA Full Scale



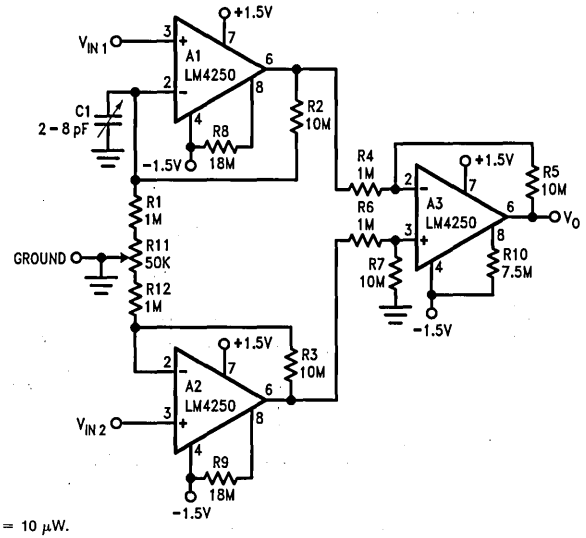
Quiescent P_D = 1.8 μW

*Meter movement (0–100 μA, 2 kΩ) marked for 0–100 nA full scale.

TL/H/9300-8

Typical Applications (Continued)

X100 Instrumentation Amplifier 10 μW



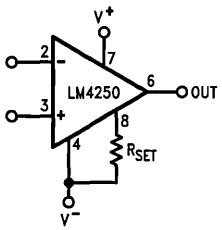
TL/H/9300–9

Note 1: Quiescent P_D = 10 μW.

Note 2: R2, R3, R4, R5, R6 and R7 are 1% resistors.

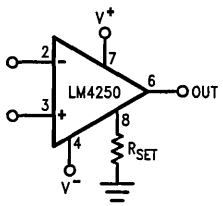
Note 3: R11 and C1 are for DC and AC common mode rejection adjustments.

R_{SET} Connected to V^-



TL/H/9300–10

R_{SET} Connected to Ground



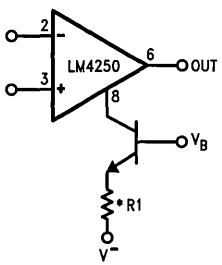
TL/H/9300–11

I_{SET} Equations:

$$I_{SET} \approx \frac{V^+ + |V^-| - 0.5}{R_{SET}}$$ where R_{SET} is connected to V^-.

$$I_{SET} \approx \frac{V^+ - 0.5}{R_{SET}}$$ where R_{SET} is connected to ground.

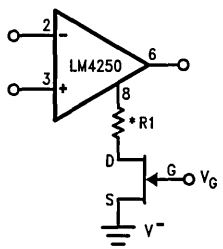
Transistor Current Sourcing Biasing



*R1 limits I_{SET} maximum

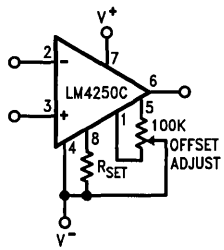
TL/H/9300–12

FET Current Sourcing Biasing



TL/H/9300–13

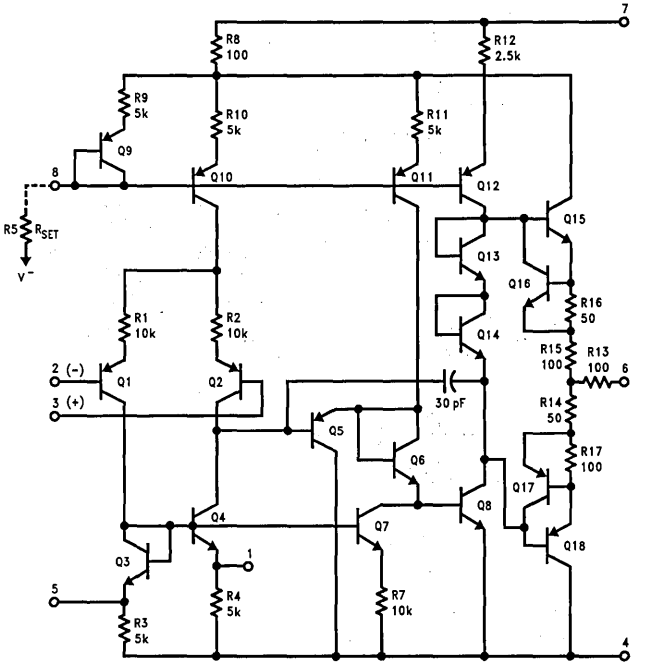
Offset Null Circuit



TL/H/9300–14

4

Schematic Diagram



TL/H/9300–1

National Semiconductor

ADVANCE INFORMATION

LMC6484/LMC6484A CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6484 low power amplifier offers the advantage of both rail-to-rail input common-mode voltage range and rail-to-rail output swing. This performance is important when designing systems with a single-supply voltage range from 3V to 15V. Special design techniques provide an excellent common-mode rejection ratio of 85 dB. CMRR is an often overlooked parameter for amplifiers in this class. For an example of where this performance is critical, consider single-supply data acquisition systems. The LMC6484 will maintain the linearity performance of single-supply data acquisition systems because of its high CMRR that extends across the full input common-mode range.

Applications of the LMC6484 include signal conditioning circuits, peak detectors, low-droop sample and holds, pH detectors, wide dynamic-range current sources and low supply voltage transducer applications.

See the LMC6482 data sheet for a Dual CMOS operational amplifier with these same features.

Features (Typical unless otherwise noted)

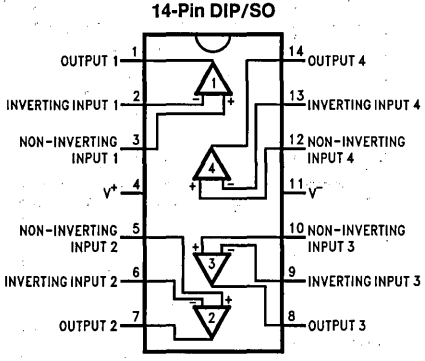
- Rail-to-Rail input common-mode voltage range
- Rail-to-Rail output swing
- Operates from 3V to 15V Supply
- Large capacitive load capability up to 500 pF
- Excellent Rail-to-Rail CMRR 85 dB
- Low input offset voltage 3 mV Max
- Low offset voltage drift 1.5 μV/°C
- Ultra low input current 20 fA
- High voltage gain (R_L = 100 kΩ) 120 dB
- Low current consumption 500 μA/Amplifier
- Specified for loads to 600Ω

Applications

- Transducer and sensor amplifier
- Portable analytic equipment (medical & military)
- Signal conditioning circuits

Connection Diagram

14-Pin DIP/SO



TL/H/11395–1

Ordering Information

Package	Temperature Range		
	Military −55°C to +125°C	Industrial −40°C to +85°C	NSC Drawing
14-Pin Molded DIP	LMC6484MN	LMC6484AIN LMC6484IN	N14A
14-Pin Small Outline		LMC6484AIM LMC6484IM	M14A

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office or Distributors for availability and specifications.

National Semiconductor

LM831 Low Voltage Audio Power Amplifier

General Description

The LM831 is a dual audio power amplifier optimized for very low voltage operation. The LM831 has two independent amplifiers, giving stereo or higher power bridge (BTL) operation from two- or three-cell power supplies.

The LM831 uses a patented compensation technique to reduce high-frequency radiation for optimum performance in AM radio applications. This compensation also results in lower distortion and less wide-band noise.

The input is direct-coupled to the LM831, eliminating the usual coupling capacitor. Voltage gain is adjustable with a single resistor.

Features

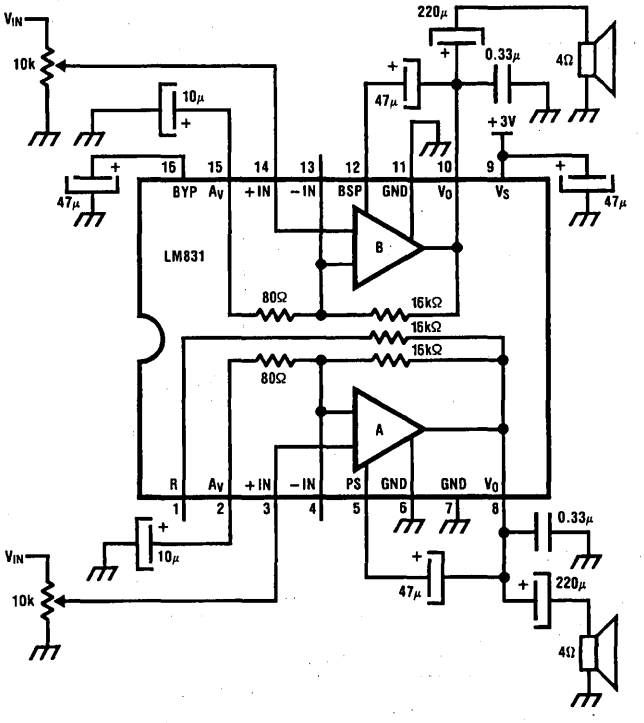
- Low voltage operation, 1.8V to 6.0V
- High power, 440 mW, 8Ω, BTL, 3V
- Low AM radiation
- Low noise
- Low THD

Applications

- Portable tape recorders
- Portable radios
- Headphone stereo
- Portable speakers

Typical Application

Dual Amplifier with Minimum Parts



TL/H/6754–1

A_V = 46 dB, BW = 250 Hz to 35 kHz

P_{OUT} = 220 mW/Ch, R_L = 4Ω

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	7.5V
Input Voltage, V_{IN}	±0.4V
Power Dissipation (Note 1), P_D	1.4W
Operating Temperature (Note 1), T_{opr}	−40°C to +85°C
Storage Temperature, T_{stg}	−65°C to +150°C
Junction Temperature, T_j	+150°C
Lead Temp. (Soldering, 10 sec.), T_L	+260°C

Electrical Characteristics

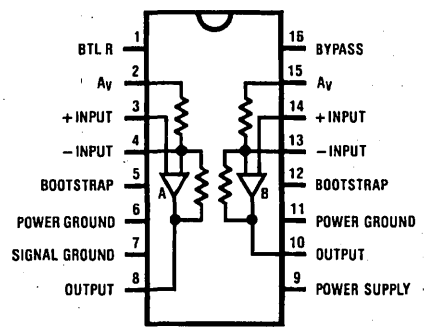
Unless otherwise specified, T_A = 25°C, V_S = 3V, f = 1 kHz, test circuit is dual or BTL amplifier with minimum parts.

Symbol	Parameter	Conditions	Typ	Tested Limit	Unit (Limit)
V_S	Operating Voltage		3 3	1.8 6	V(Min) V(Max)
I_Q	Supply Current	V_{IN} = 0, Dual Mode V_{IN} = 0, BTL Mode	5 6	10 15	mA (Max) mA (Max)
V_{OS}	Output DC Offset	V_{IN} = 0, BTL Mode	10	50	mV (Max)
R_{IN}	Input Resistance		25	15 35	k (Min) k (Max)
A_V	Voltage Gain	V_{IN} = 2.25 mV_{rms}, f = 1 kHz, Dual Mode	46	44 48	dB (Min) dB (Max)
PSRR	Supply Rejection	V_S = 3V + 200 mV_{rms} @ f = 1 kHz	46	30	dB (Min)
P_{OD}	Power Out	V_S = 3V, R_L = 4Ω, 10% THD, Dual Mode	220	150	mW (Min)
P_{ODL}	Power Out Low, V_S	V_S = 1.8V, R_L = 4Ω, 10% THD, Dual Mode	45	10	mW (Min)
P_{OB}	Power Out	V_S = 3V, R_L = 8Ω, 10% THD, BTL Mode	440	300	mW (Min)
P_{OBL}	Power Out Low, V_S	V_S = 1.8V, R_L = 8Ω, 10% THD, BTL Mode	90	20	mW (Min)
Sep	Channel Separation	Referenced to V_O = 200 mV_{rms}	52	40	dB (Min)
I_B	Input Bias Current		1	2	μA (Max)
E_{n0}	Output Noise	Wide Band (250 ~ 35 kHz)	250	500	μV (Max)
THD	Distortion	V_S = 3V, P_O = 50 mW, f = 1 kHz, Dual	0.25	1	% (Max)

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Connection Diagram

Dual-In-Line Package



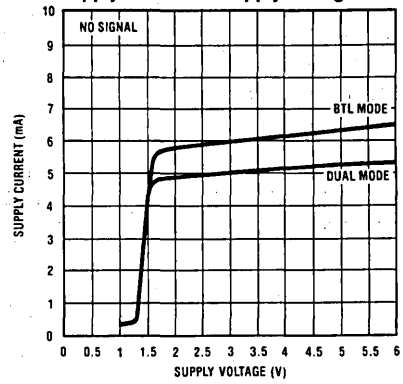
TL/H/6754–2

Top View

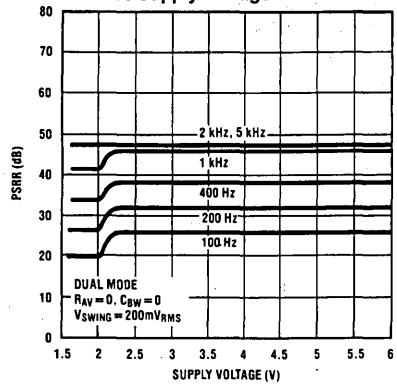
Order Number LM831N
See NS Package Number N16E

Typical Performance Characteristics

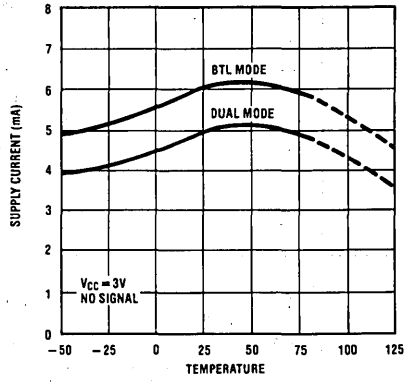
Supply Current vs Supply Voltage



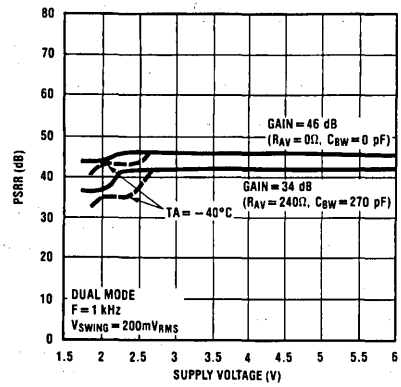
PSRR vs Supply Voltage



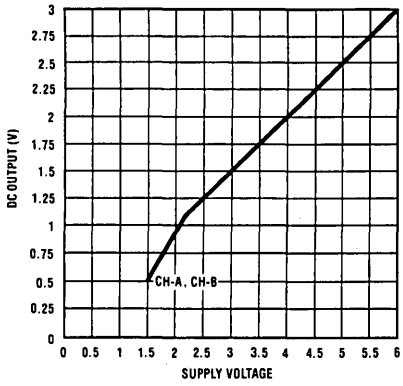
Supply Current vs Temperature



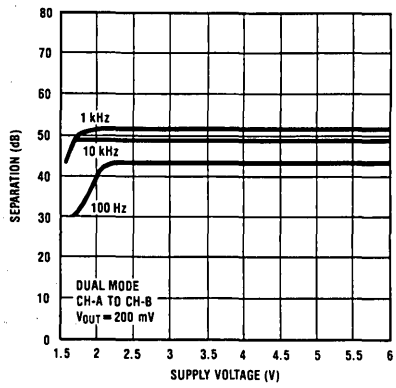
PSRR vs Supply Voltage



DC Output vs Supply Voltage



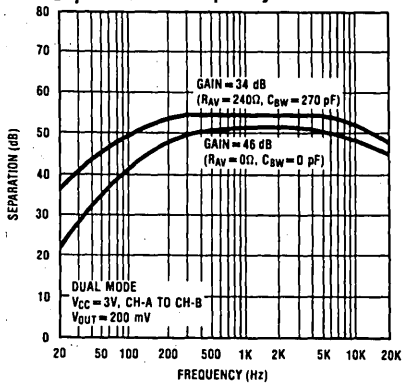
Separation vs Supply Voltage



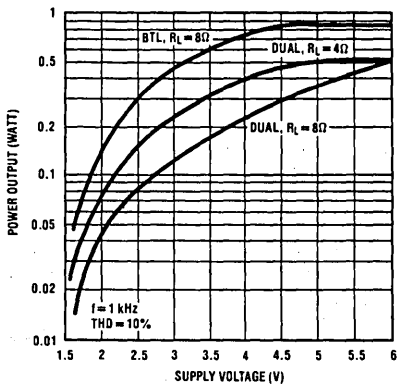
TL/H/6754–4

Typical Performance Characteristics (Continued)

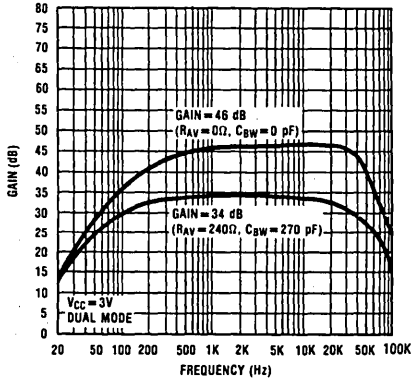
Separation vs Frequency



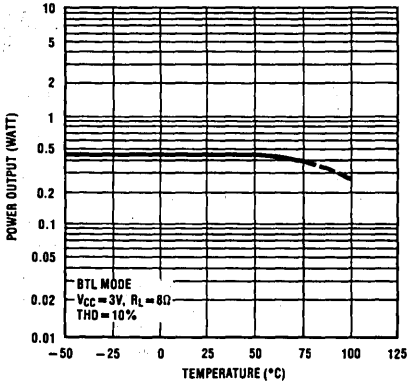
Power Output vs Supply Voltage



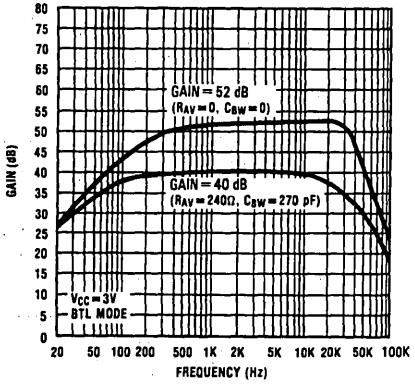
Gain vs Frequency



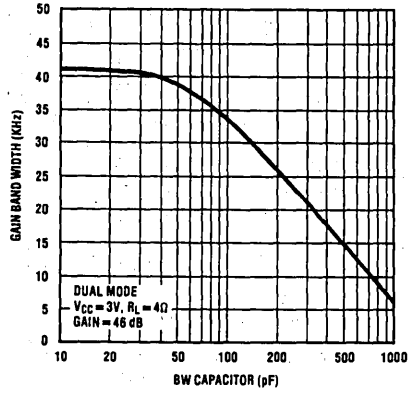
Power Output vs Temperature



Gain vs Frequency



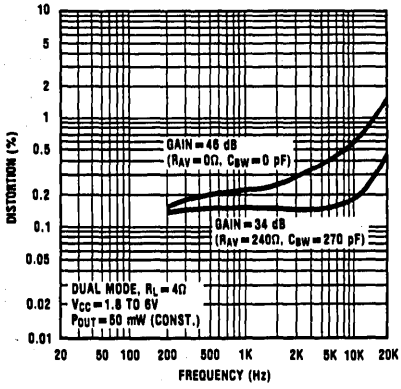
Bandwidth vs BW Capacitance



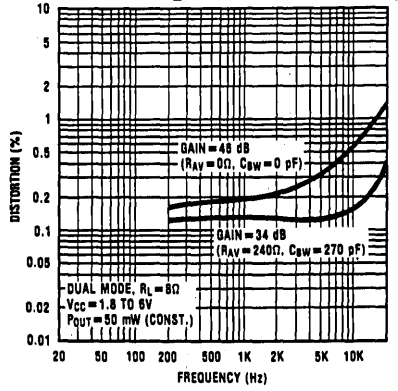
TL/H/6754–5

Typical Performance Characteristics (Continued)

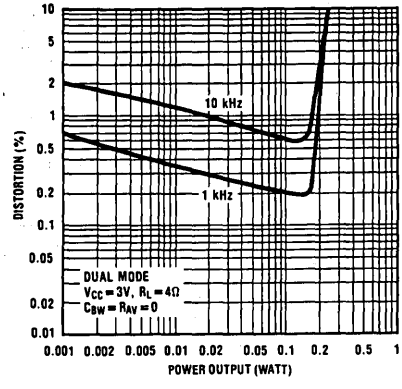
Dual Mode, R_L = 4Ω Distortion vs Frequency



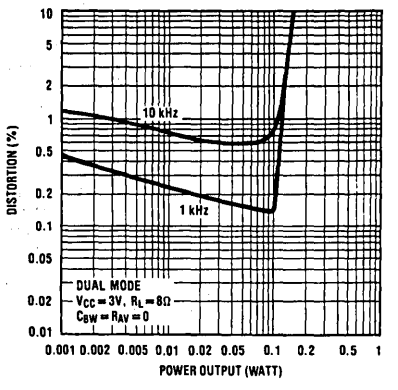
Dual Mode, R_L = 8Ω Distortion vs Frequency



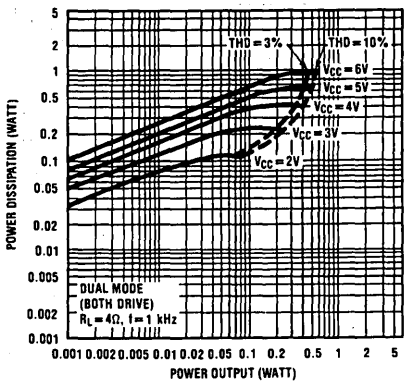
Distortion vs Power Output (Note 2)



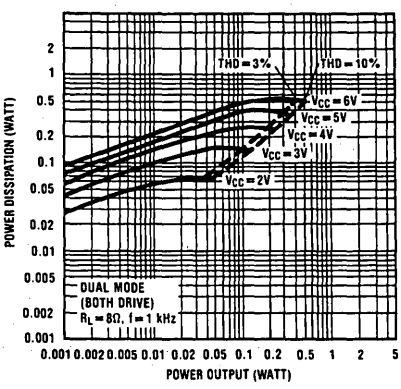
Distortion vs Power Output (Note 2)



Power Dissipation vs Power Output



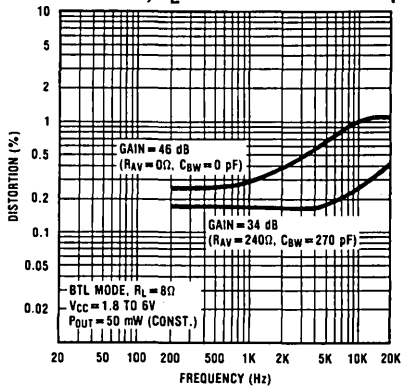
Power Dissipation vs Power Output



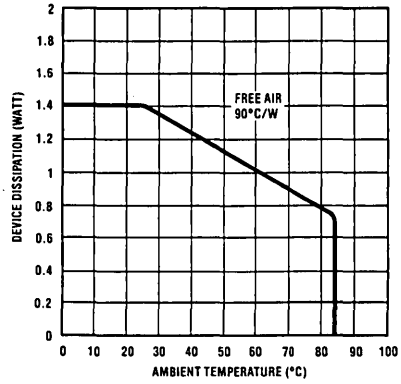
TL/H/6754–6

Typical Performance Characteristics (Continued)

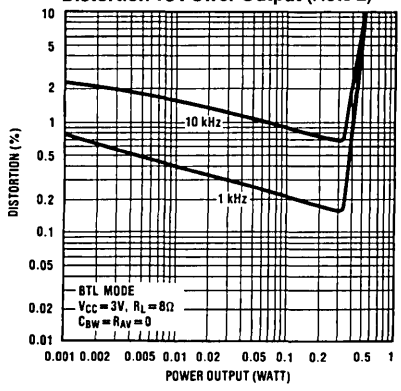
BTL Mode, R_L = 8Ω Distortion vs Frequency



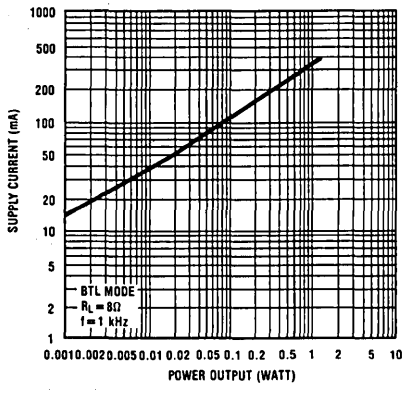
Device Dissipation vs Ambient Temperature



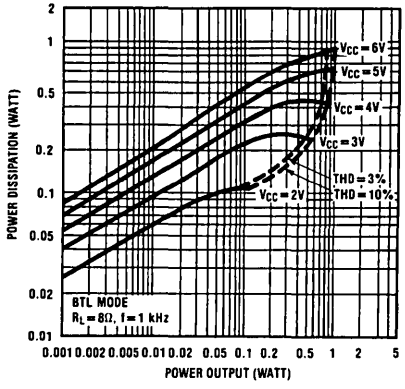
Distortion vs Power Output (Note 2)



Supply Current vs Power Output



Power Dissipation vs Power Output

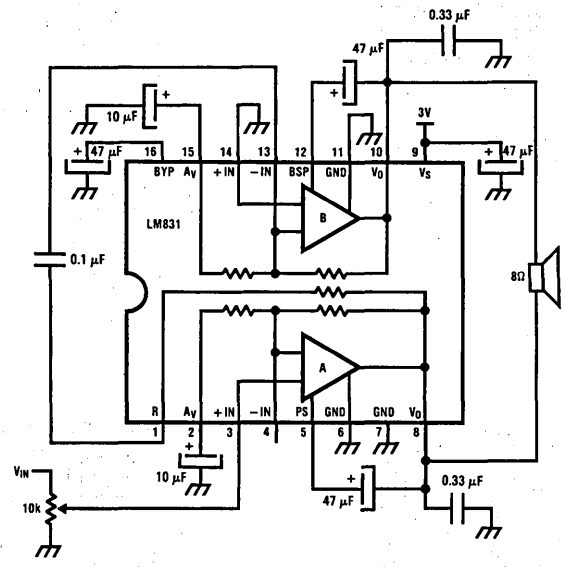


Note 2: 1 kHz curve is measured with 400 Hz–30 kHz Filter.

TL/H/6754–7

Typical Applications

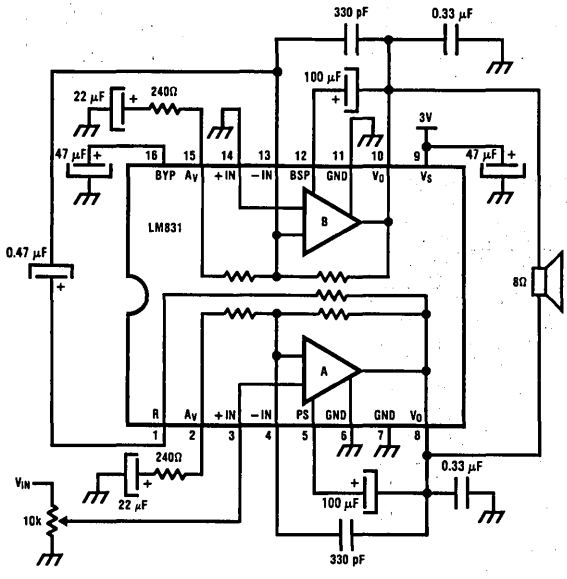
BTL Amplifier with Minimum Parts



TL/H/6754–8

A_V = 52 dB, BW = 250 Hz to 25 kHz
P_{OUT} = 440 mW, R_L = 8Ω

BTL Amplifier for HI-FI Quality

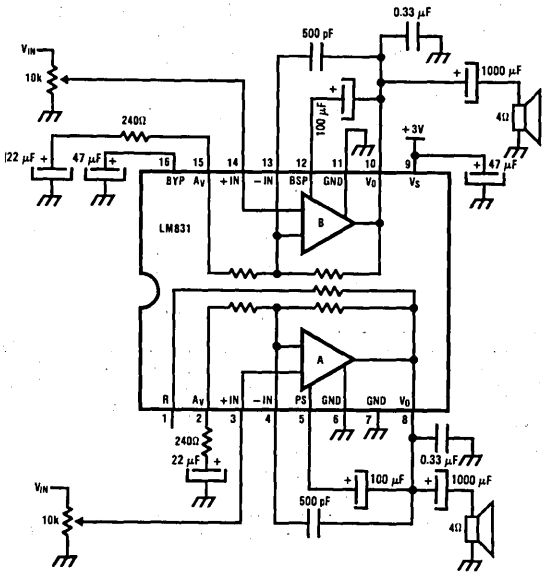


TL/H/6754–9

A_V = 40 dB, BW = 20 Hz to 20 kHz
P_{OUT} = 440 mW, R_L = 8Ω
(Dynamic Range Over 80 dB)

Typical Applications (Continued)

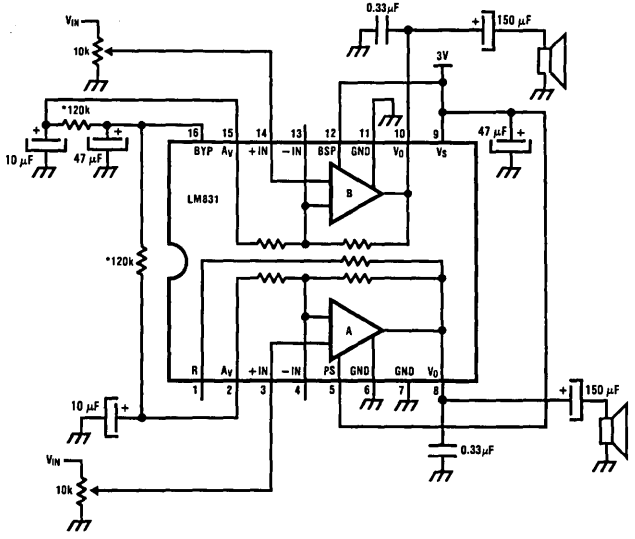
Dual Amplifier for Hi-Fi Quality



TL/H/6754–10

A_V = 34 dB, BW = 50 Hz to 20 kHz
P_{OUT} = 220 mW/Ch, R_L = 4Ω
(Dynamic Range Over 80 dB)

Low-Cost Power Amplifier (No Bootstrap)



TL/H/6754–11

P_{OUT} = 150 mW/Ch, BW = 300 Hz to 35 kHz
BTL Mode is also possible
*For 3-cell applications, the 120k resistor should be changed to 20K.

LM831 Circuit Description Refer to the external component diagram and equivalent schematic.

The power supply is applied to Pin 9 and is filtered by resistor R_1 and capacitor C_{BY} on Pin 16. This filtered voltage at Pin 16 is used to bias all of the LM831 circuits except the power output stage. Resistor R_0 generates a biasing current that sets the output DC voltage for optimum output power for any given supply voltage.

Feedback is provided to the input transistor Q_1 emitter by R_6 and R_7.

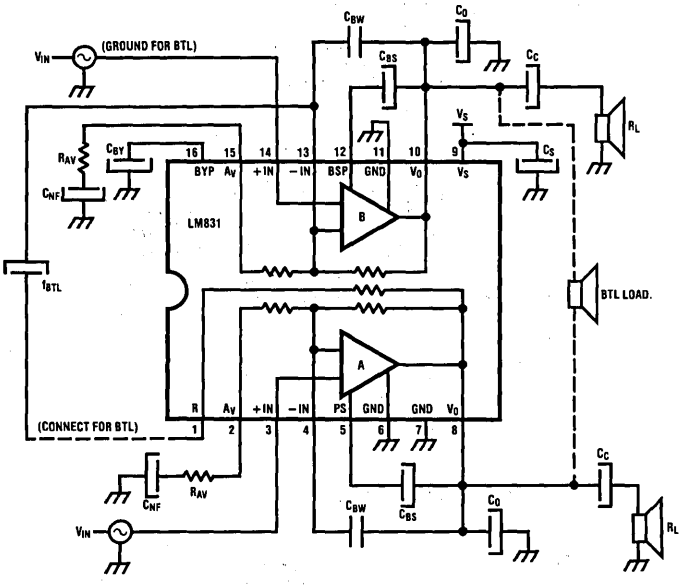
The capacitor C_{NF} on Pin 2 provides unity DC gain for maximum DC accuracy.

Q_2 provides voltage gain and the rest of the devices buffer the output load from Q_2's collector.

Bootstrapping of Pin 5 by C_{BS} allows maximum output swing and improved supply rejection.

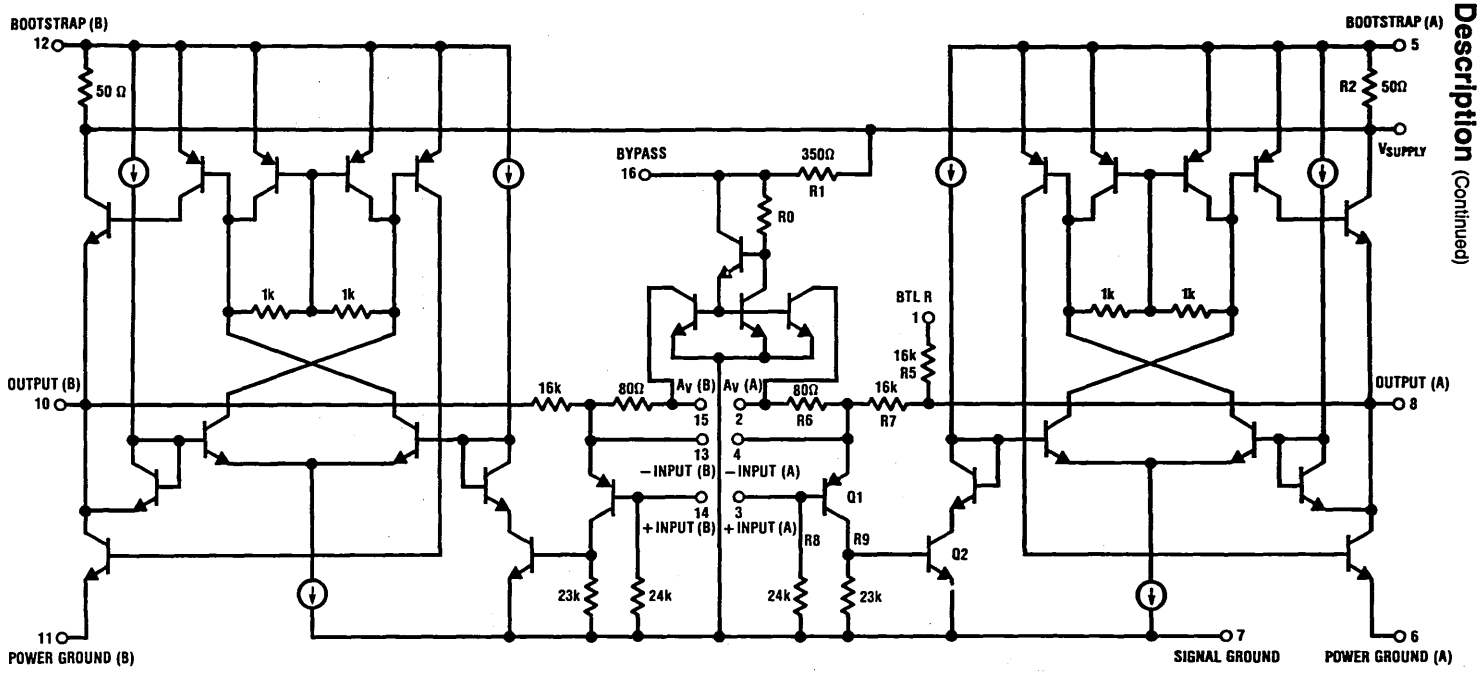
R_5 is provided for bridge (BTL) operation.

External Component Diagram



TL/H/6754–12

LM831 Equivalent Schematic



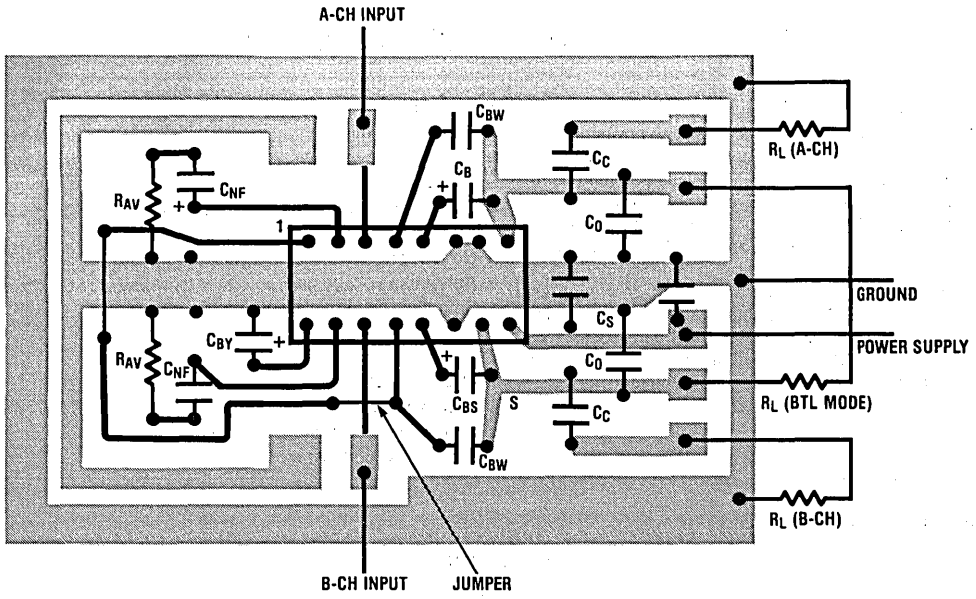
TL/H/6754–13

External Components (Refer to External Component Diagram)

Component	Comments	Min	Max
C_O	Required to stabilize output stage.	0.33 μF	1 μF
C_c	Output coupling capacitors for Dual Mode. Sets a low-frequency pole in the frequency response. $f_L = \frac{1}{2\pi C_c R_L}$	100 μF	10,000 μF
C_{BS}	Bootstrap capacitors. Sets a low-frequency pole in the power BW. Recommended value is $C_{BS} = \frac{1}{10 \bullet 2\pi \bullet f_L \bullet R_L}$	22 μF or (short Pins 4 & 12 to 9)	470 μF
C_S	Supply bypass. Larger values improve low-battery performance by reducing supply ripple.	47 μF	10,000 μF
C_{BY}	Filters the supply for improved low-voltage operation. Also sets turn-on delay.	47 μF	470 μF
C_{NF}	Sets a low-frequency response. Also affects turn-on delay. $f_L = \frac{1}{2\pi \bullet C_{NF} \bullet (R_{AV} + 80)}$ In BTL Mode, C_{NF} on Pin 15 can be reduced without affecting the frequency response. However, the turn-on "POP" will be worsened.	10 μF	100 μF
C_{BTL}	Used only in the Bridge Mode. Connects the output of the first amplifier to the inverting input of the other through an internal resistor. Sets a low-frequency pole in one-half the frequency response. $f_L = \frac{1}{2\pi \bullet C_{BTL} \bullet 16k}$	0.1 μF	1 μF
C_{BW}	Improves clipping waveform and sets the high-frequency bandwidth. Works with an internal 16k resistor. (This equation applies for $R_{AV} \neq 0$. For 46 dB application, see BW–C_{BW} curve.) $f_H = \frac{1}{2\pi \bullet C_{BW} \bullet 16k}$	See table below	
R_{AV}	Used to reduce the gain and improve the distortion and signal to noise. If this is desired, C_{BW} must also be used.	See table below	

Typical A_V	R_{AV}	C_{BW}	
		Min	Max
46 dB	Short	Open	4700 pF
40 dB	82	100 pF	4700 pF
34 dB	240	270 pF	4700 pF
28 dB	560	500 pF	4700 pF

Printed Circuit Layout for LM831N (Foil Side View) Refer to External Component Diagram



TL/H/6754–14

Note: Power ground pattern should be as wide as possible. Supply bypass capacitor should be as close to the IC as possible. Output compensation capacitors should also be close to the IC.

National Semiconductor

LM1896/LM2896 Dual Power Audio Amplifier

General Description

The LM1896 is a high performance 6V stereo power amplifier designed to deliver 1 watt/channel into 4Ω or 2 watts bridged monaural into 8Ω. Utilizing a unique patented compensation scheme, the LM1896 is ideal for sensitive AM radio applications. This new circuit technique exhibits lower wideband noise, lower distortion, and less AM radiation than conventional designs. The amplifier's wide supply range (3V–9V) is ideal for battery operation. For higher supplies (V_S > 9V) the LM2896 is available in an 11-lead single-in-line package. The LM2896 package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

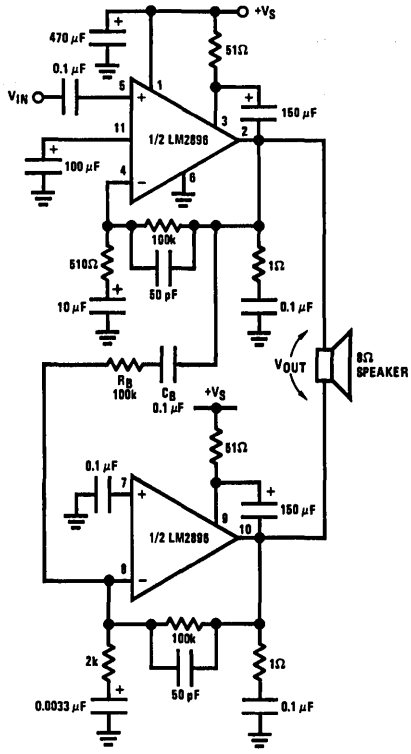
Features

- Low AM radiation
- Low noise
- 3V, 4Ω, stereo P_O = 250 mW
- Wide supply operation 3V–15V (LM2896)
- Low distortion
- No turn on "pop"
- Adjustable voltage gain and bandwidth
- Smooth waveform clipping
- P_O = 9W bridged, LM2896

Applications

- Compact AM-FM radios
- Stereo tape recorders and players
- High power portable stereos

Typical Applications



TL/H/7920–1

FIGURE 1. LM2896 In Bridge Configuration (A_V = 400, BW = 20 kHz)

Order Number LM1896N **Order Number LM2896P**
See NS Package Number N14A **See NS Package Number P11A**

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
- LM1896 V_S = 12V
- LM2896 V_S = 18V

Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

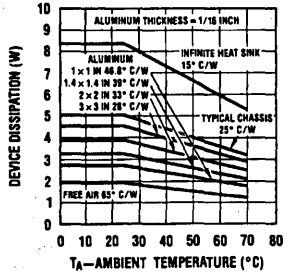
Unless otherwise specified, T_A = 25°C, A_V = 200 (46 dB). For the LM1896; V_S = 6V and R_L = 4Ω. For LM2896, T_{TAB} = 25°C, V_S = 12V and R_L = 8Ω. Test circuit shown in *Figure 2.*

Parameter	Conditions	LM1896			LM2896			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Current	P_O = 0W, Dual Mode		15	25		25	40	mA
Operating Supply Voltage		3		10	3		15	V
Output Power	THD = 10%, f = 1 kHz							
LM1896N-1	V_S = 6V, R_L = 4Ω Dual Mode } T_A = 25°C	0.9	1.1					W/ch
LM1896N-2	V_S = 6V, R_L = 8Ω Bridge Mode } T_A = 25°C		1.8	2.1				W
	V_S = 9V, R_L = 8Ω Dual Mode } T_A = 25°C		1.3					W/ch
LM2896P-1	V_S = 12V, R_L = 8Ω Dual Mode } T_{TAB} = 25°C				2.0	2.5		W/ch
LM2896P-2	V_S = 12V, R_L = 8Ω Bridge Mode } T_{TAB} = 25°C				7.2	9.0		W
	V_S = 9V, R_L = 4Ω Bridge Mode } T_{TAB} = 25°C					7.8		W
	V_S = 9V, R_L = 4Ω Dual Mode } T_{TAB} = 25°C					2.5		W/ch
Distortion	f = 1 kHz							
	P_O = 50 mW		0.09			0.09		%
	P_O = 0.5W		0.11			0.11		%
	P_O = 1W					0.14		%
Power Supply Rejection Ratio (PSRR)	C_{BY} = 100 μF, f = 1 kHz, C_{IN} = 0.1 μF Output Referred, V_{RIPPLE} = 250 mV	−40	−54		−40	−54		dB
Channel Separation	C_{BY} = 100 μF, f = 1 kHz, C_{IN} = 0.1 μF Output Referred	−50	−64		−50	−64		dB
Noise	Equivalent Input Noise R_S = 0, C_{IN} = 0.1 μF, BW = 20 − 20 kHz		1.4			1.4		μV
	CCIR/ARM		1.4			1.4		μV
	Wideband		2.0			2.0		μV
DC Output Level		2.8	3	3.2	5.6	6	6.4	V
Input Impedance		50	100	350	50	100	350	kΩ
Input Offset Voltage			5			5		mV
Voltage Difference between Outputs	LM1896N-2, LM2896P-2		10	20		10	20	mV
Input Bias Current			120			120		nA

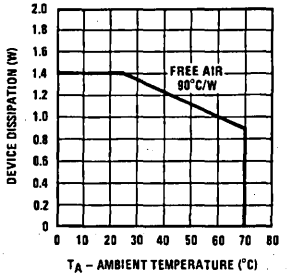
Note 1: For operation at ambient temperature greater than 25°C, the LM1896/LM2896 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon mounting techniques.

Typical Performance Curves

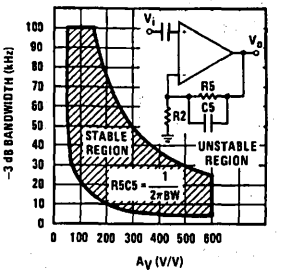
LM2896 Device Dissipation vs Ambient Temperature



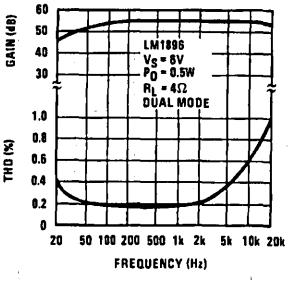
LM1896 Maximum Device Dissipation vs Ambient Temperature



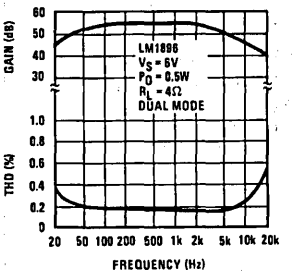
−3 dB Bandwidth vs Voltage Gain for Stable Operation



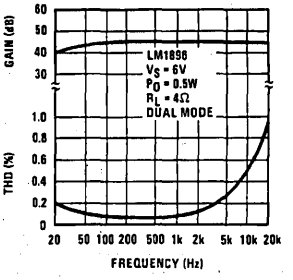
THD and Gain vs Frequency
A_V = 54 dB, BW = 30 kHz



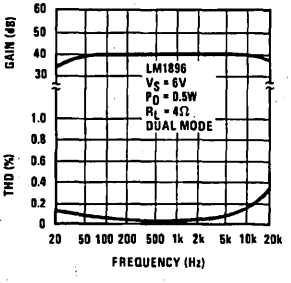
THD and Gain vs Frequency
A_V = 54 dB, BW = 5 kHz



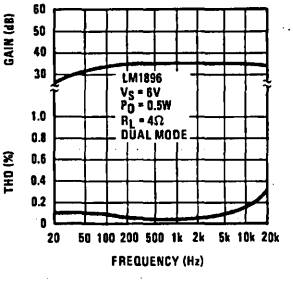
THD and Gain vs Frequency
A_V = 46 dB, BW = 50 kHz



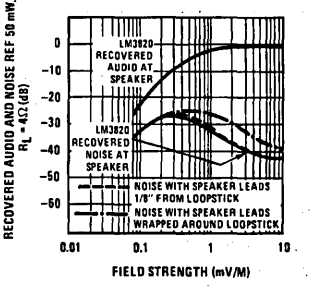
THD and Gain vs Frequency
A_V = 40 dB, BW = 20 kHz



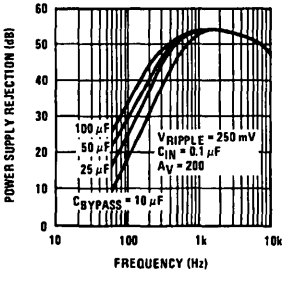
THD and Gain vs Frequency
A_V = 34 dB, BW = 50 kHz



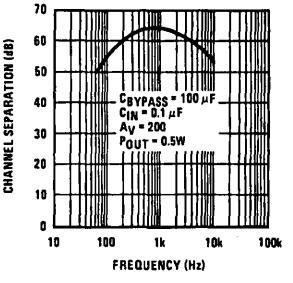
AM Recovered Audio and Noise vs Field Strength for Different Speaker Lead Placement



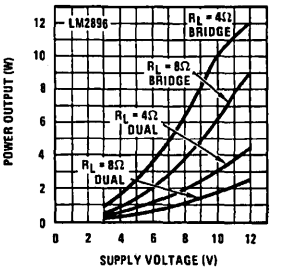
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



Channel Separation (Referred to the Output) vs Frequency



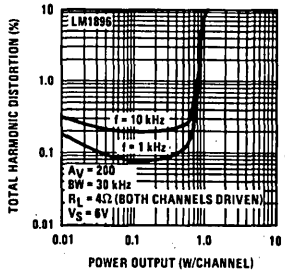
Power Output vs Supply Voltage



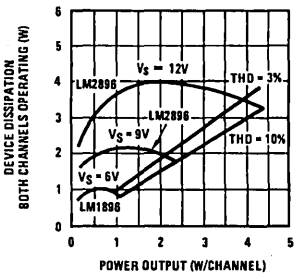
TL/H/7920–2

Typical Performance Curves (Continued)

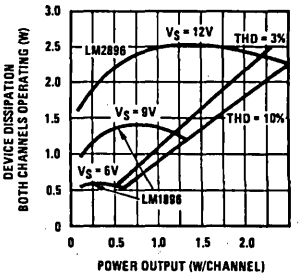
Total Harmonic Distortion vs Power Output



Power Dissipation vs Power Output $R_L = 4\Omega$

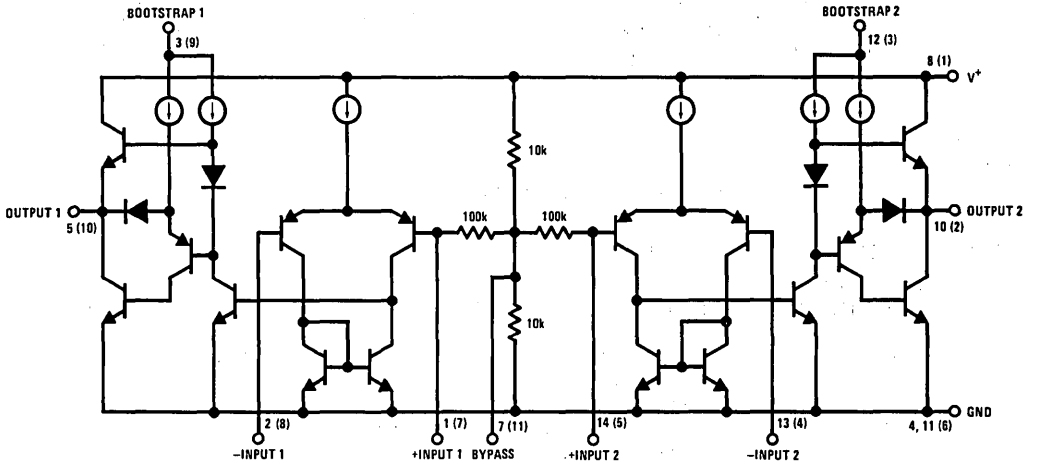


Power Dissipation vs Power Output $R_L = 8\Omega$



TL/H/7920–3

Equivalent Schematic



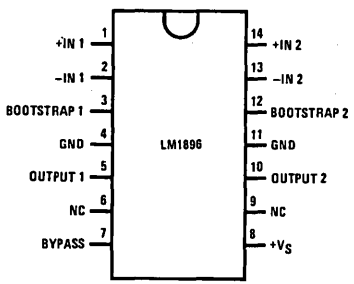
6, 9 No connection on LM1896

( ) indicates pin number for LM2896

TL/H/7920–4

Connection Diagrams

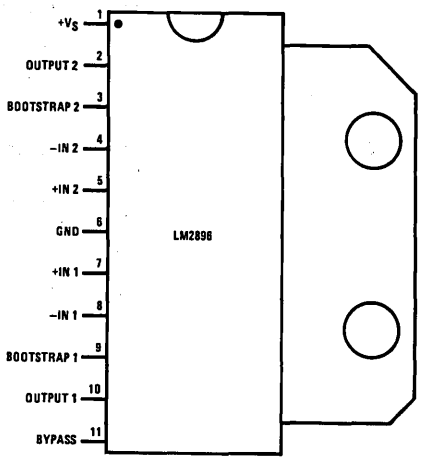
Dual-In-Line Package



TL/H/7920–5

Top View

Single-In-Line Package

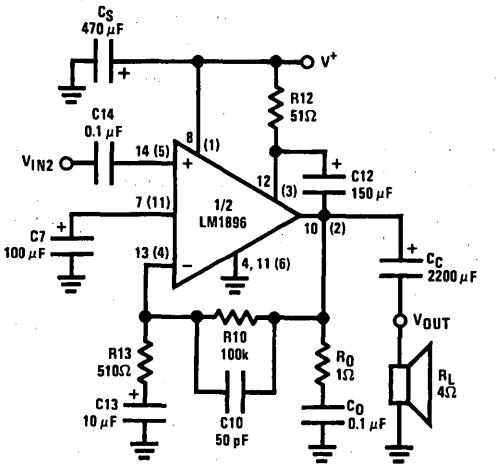


TL/H/7920–6

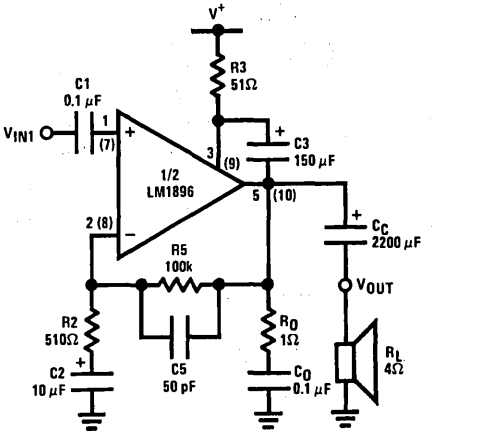
Top View

4

Typical Applications (Continued)



TL/H/7920–7



TL/H/7920–8

6, 9 No connection on LM1896

( ) Indicates pin number for LM2896

FIGURE 2. Stereo Amplifier with A_V = 200, BW = 30 kHz

External Components *(Figure 2)*

Components	Comments
1. R2, R5, R10, R13	Sets voltage gain, $A_V = 1 + R5/R2$ for one channel and $A_V = 1 + R10/R13$ for the other channel.
2. R3, R12	Bootstrap resistor sets drive current for output stage and allows pins 3 and 12 to go above V_S.
3. R_O	Works with C_O to stabilize output stage.
4. C1, C14	Input coupling capacitor. Pins 1 and 14 are at a DC potential of $V_S/2$. Low frequency pole set by: $f_L = \frac{1}{2\pi R_{IN} C1}$
5. C2, C13	Feedback capacitors. Ensure unity gain at DC. Also a low frequency pole at: $f_L = \frac{1}{2\pi R2C2}$
6. C3, C12	Bootstrap capacitors, used to increase drive to output stage. A low frequency pole is set by: $f_L = \frac{1}{2\pi R3C3}$
7. C5, C10	Compensation capacitor. These stabilize the amplifiers and adjust their bandwidth. See curve of bandwidth vs allowable gain.
8. C7	Improves power supply rejection (See Typical Performance Curves). Increasing C7 increases turn-on delay.
9. C_C	Output coupling capacitor. Isolates pins 5 and 10 from the load. Low frequency pole set by: $f_L = \frac{1}{2\pi C_C R_L}$
10. C_O	Works with R_O to stabilize output stage.
11. C_S	Provides power supply filtering.

Application Hints

AM Radios

The LM1896/LM2896 has been designed fo fill a wide range of audio power applications. A common problem with IC audio power amplifiers has been poor signal-to-noise performance when used in AM radio applications. In a typical radio application, the loopstick antenna is in close proximity to the audio amplifer. Current flowing in the speaker and power supply leads can cause electromagnetic coupling to the loopstick, resulting in system oscillation. In addition, most audio power amplifiers are not optimized for lowest noise because of compensation requirements. If noise from the audio amplifier radiates into the AM section, the sensitivity and signal-to-noise ratio will be degraded.

The LM1896 exhibits extremely low wideband noise due in part to an external capacitor C5 which is used to tailor the bandwidth. The circuit shown in *Figure 2* is capable of a signal-to-noise ratio in excess of 60 dB referred to 50 mW. Capacitor C5 not only limits the closed loop bandwidth, it also provides overall loop compensation. Neglecting C2 in *Figure 2*, the gain is:

$$A_V(S) = \frac{S + A_V \omega_o}{S + \omega_o}$$

$$\text{where } A_V = \frac{R2 + R5}{R2}, \quad \omega_o = \frac{1}{R5C5}$$

A curve of −3 dB BW (ω_o) vs A_V is shown in the Typical Performance Curves.

Figure 3 shows a plot of recovered audio as a function of field strength in μV/M. The receiver section in this example is an LM3820. The power amplifier is located about two inches from the loopstick antenna. Speaker leads run parallel to the loopstick and are 1/8 inch from it. Referenced to a 20 dB S/N ratio, the improvement in noise performance over conventional designs is about 10 dB. This corresponds to an increase in usable sensitivity of about 8.5 dB.

Bridge Amplifiers

The LM1896/LM2896 can be used in the bridge mode as a monaural power amplifier. In addition to much higher power output, the bridge configuration does not require output coupling capacitors. The load is connected directly between the amplifier outputs as shown in *Figure 4*.

Amp 1 has a voltage gain set by 1 + R5/R2. The output of amp 1 drives amp 2 which is configured as an inverting amplifier with unity gain. Because of this phase inversion in amp 2, there is a 6 dB increase in voltage gain referenced to V_i. The voltage gain in bridge is:

$$\frac{V_o}{V_i} = 2\left(1 + \frac{R5}{R2}\right)$$

C_B is used to prevent DC voltage on the output of amp 1 from causing offset in amp 2. Low frequency response is influenced by:

$$f_L = \frac{1}{2\pi R_B C_B}$$

Several precautions should be observed when using the LM1896/LM2896 in bridge configuration. Because the amplifiers are driving the load out of phase, an 8Ω speaker will appear as a 4Ω load, and a 4Ω speaker will appear as a 2Ω load. Power dissipation is twice as severe in this situation. For example, if V_S = 6V and R_L = 8Ω bridged, then the maximum dissipation is:

$$P_D = \frac{V_S^2}{20\,R_L} \times 2 = \frac{6^2}{20 \times 4} \times 2$$

$$P_D = 0.9 \text{ Watts}$$

This amount of dissipation is equivalent to driving two 4Ω loads in the stereo configuration.

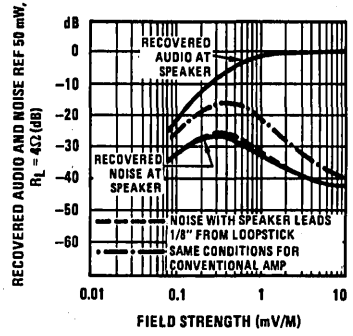
When adjusting the frequency response in the bridge configuration, R5C5 and R10C10 form a 2 pole cascade and the −3 dB bandwidth is actually shifted to a lower frequency:

$$BW = \frac{0.707}{2\pi RC}$$

where R = feedback resistor

C = feedback capacitor

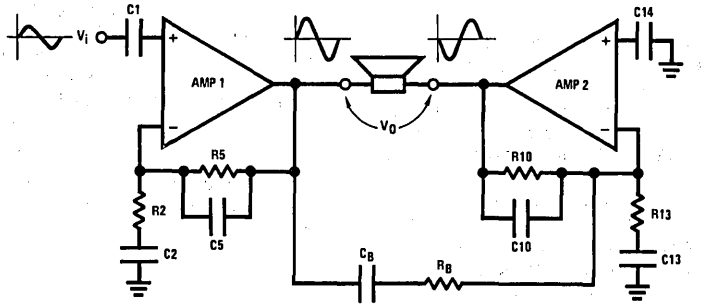
To measure the output voltage, a floating or differential meter should be used because a prolonged output short will over dissipate the package. *Figure 1* shows the complete bridge amplifier.



TL/H/7920–9

FIGURE 3. Improved AM Sensitivity over Conventional Design

Application Hints (Continued)



TL/H/7920–10

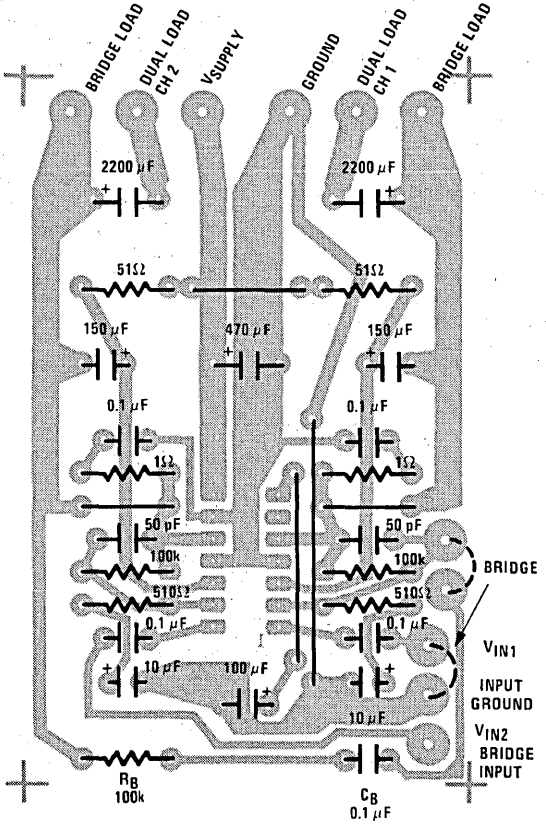
Figure 4. Bridge Amplifier Connection

Printed Circuit Layout

Printed Circuit Board Layout

Figure 5 and *Figure 6* show printed circuit board layouts for the LM1896 and LM2896. The circuits are wired as stereo amplifiers. The signal source ground should return to the input ground shown on the boards. Returning the loads to power supply ground through a separate wire will keep the THD at its lowest value. The inputs should be terminated in less than 50 kΩ to prevent an input-output oscillation. This oscillation is dependent on the gain and the proximity of the bridge elements R_B and C_B to the (+) input. If the bridge mode is not used, do not insert R_B, C_B into the PCB.

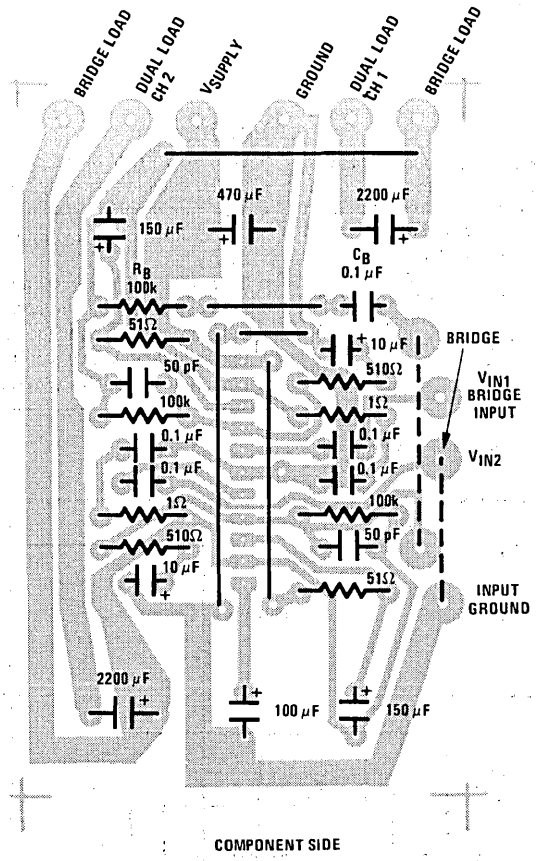
To wire the amplifer into the bridge configuration, short the capacitor on pin 7 (pin 1 of the LM1896) to ground. Connect together the nodes labeled BRIDGE and drive the capacitor connected to pin 5 (pin 14 of the LM1896).



TL/H/7920–11

FIGURE 5. Printed Circuit Board Layout for the LM1896

Printed Circuit Layout (Continued)



TL/H/7920–12

FIGURE 6. Printed Circuit Board Layout for the LM2896

National Semiconductor

PRELIMINARY

LMC555 CMOS Timer

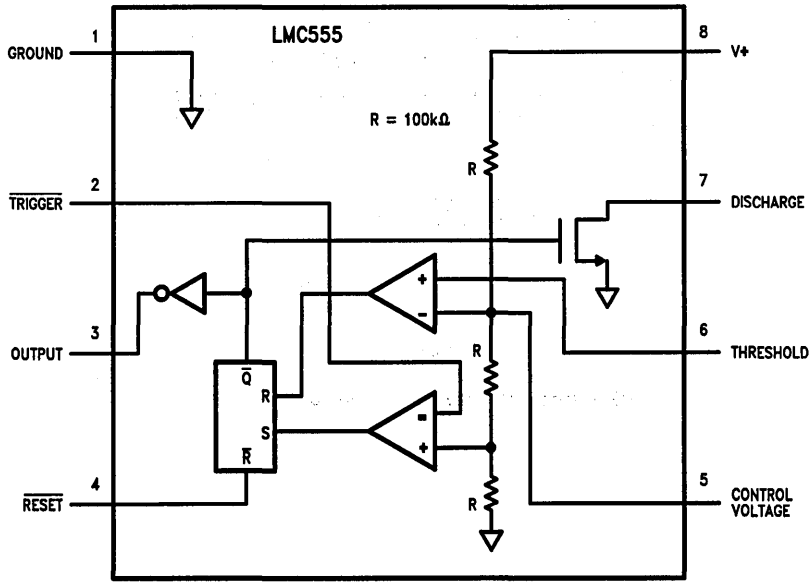
General Description

The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. It offers the same capability of generating accurate time delays and frequencies but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the astable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of National Semiconductor's LMCMOS™ process extends both the frequency range and low supply capability.

Features

- Less than 1 mW typical power dissipation at 5V supply
- 3 MHz astable frequency capability
- 1.5V supply operating voltage guaranteed
- Output fully compatible with TTL and CMOS logic at 5V supply
- Tested to −10 mA, +50 mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers

Block and Connection Diagrams



TL/H/8669–1

(Pinouts for Molded and Metal Can Packages are identical)

Order Number LMC555CH, LMC555CM or LMC555CN
See NS Package Number H08C, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V8	15V
Input Voltages, V2, V4, V5, V6	−0.3V to V_S + 0.3V
Output Voltages, V3, V7	15V
Output Current I3, I7	100 mA
Operating Temperature Range (Note 1)	−40°C to +85°C*
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted

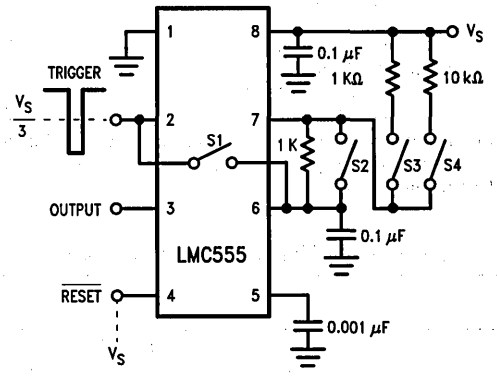
Symbol	Parameter	Conditions	Min	Typ	Max	Units (Limits)
I8	Supply Current	V_S = 1.5V V_S = 5V V_S = 12V		50 100 150	150 250 400	μA
V5	Control Voltage	V_S = 1.5V V_S = 5V V_S = 12V	0.8 2.9 7.4	1.0 3.3 8.0	1.2 3.8 8.6	V
V7	Discharge Saturation Voltage	V_S = 1.5V, I_7 = 1 mA V_S = 5V, I_7 = 10 mA		75 150	150 300	mV
$V3_L$	Output Voltage (Low)	V_S = 1.5V, I_3 = 1 mA V_S = 5V, I_3 = 8 mA V_S = 12V, I_3 = 50 mA		0.2 0.3 1.0	0.4 0.6 2.0	V
$V3_H$	Output Voltage (High)	V_S = 1.5V, I_3 = −0.25 mA V_S = 5V, I_3 = −2 mA V_S = 12V, I_3 = −10 mA	1.0 4.4 10.5	1.25 4.7 11.3		V
V2	Trigger Voltage	V_S = 1.5V V_S = 12V	0.4 3.7	0.5 4.0	0.6 4.3	V
I2	Trigger Current	V_S = 5V		10		pA
V4	Reset Voltage	V_S = 1.5V (Note 2) V_S = 12V	0.4 0.4	0.7 0.75	1.0 1.1	V
I4	Reset Current	V_S = 5V		10		pA
I6	Threshold Current	V_S = 5V		10		pA
I7	Discharge Leakage	V_S = 12V		1.0	100	nA
t	Timing Accuracy	SW 2, 4 Closed V_S = 1.5V V_S = 5V V_S = 12V	 0.9 1.0 1.0	 1.1 1.1 1.1	 1.25 1.20 1.25	ms
Δt/ΔVs	Timing Shift with Supply	V_S = 5V ±1V		0.3		%/V
Δt/ΔT	Timing Shift with Temperature	V_S = 5V −40°C ≤ T ≤ +85°C		75		ppm/°C
f_A	Astable Frequency	SW 1, 3 Closed V_S = 12V	4.0	4.8	5.6	kHz
f_{MAX}	Maximum Frequency	Max. Freq. Test Circuit, V_S = 5V		3.0		MHz
t_R, t_F	Output Rise and Fall Times	Max. Freq. Test Circuit V_S = 5V, C_L = 10 pF		15		ns
t_{PD}	Trigger Propagation Delay	V_S = 5V, Measure Delay from Trigger to Output		100		ns

* Refer to RETSC555X drawing for specifications of military LMC555H version.

Note 1: For operation at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 111°C/W for the LMC555CN, 167°C/W for the LMC555CH, and 169°C/W for the LMC555CM. Maximum allowable dissipation at 25°C is 1126 mW for the LMC555CN, 755 mW for the LMC555CH, and 740 mW for the LMC555CM.

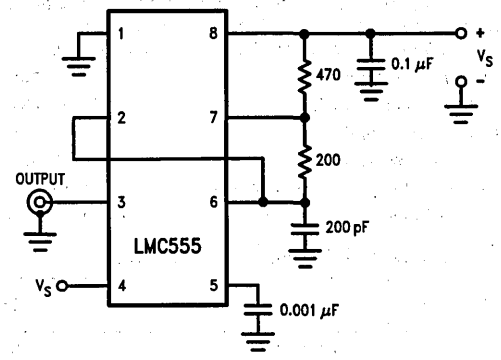
Note 2: If the $\overline{\text{RESET}}$ pin is to be used at temperatures of −20°C and below V_S is required to be 2.0V or greater.

Test Circuit



TL/H/8669-2

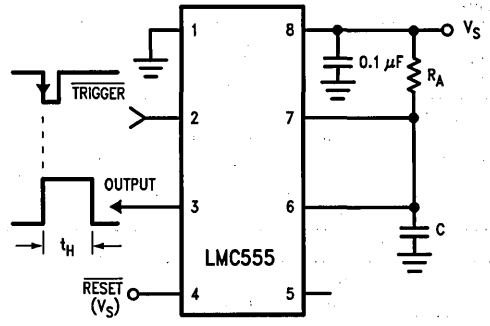
Maximum Frequency Test Circuit



TL/H/8669-3

Typical Applications

Monostable (One-Shot)



TL/H/8669-4

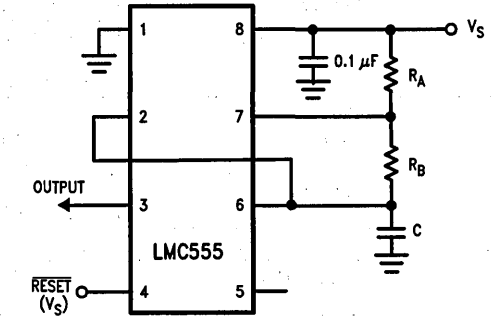
t_H = 1.1 R_AC (Gives time that output is high following trigger)

RESET overrides TRIGGER, which can override THRESHOLD. Therefore, the trigger pulse must be shorter than the desired t_H.

The minimum trigger pulse width is 20 ns.

The minimum reset pulse width is 400 ns.

Variable Duty Cycle Oscillator

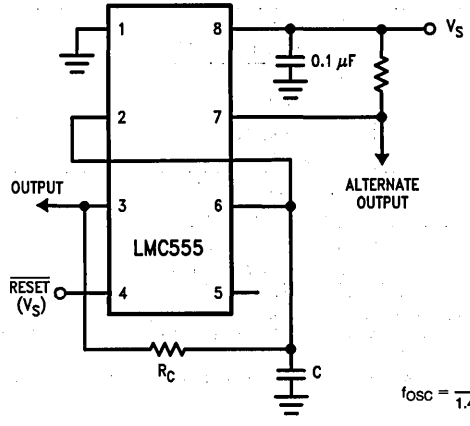


TL/H/8669-5

$$f_{OSC.} = \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{Duty Cycle} = \frac{R_B}{R_A + 2R_B}$$ (Gives fraction of total period that output is low)

50% Duty Cycle Oscillator



$$f_{OSC} = \frac{1}{1.4R_CC}$$

TL/H/8669-6

National Semiconductor

LMC568 Low Power Phase-Locked Loop

General Description

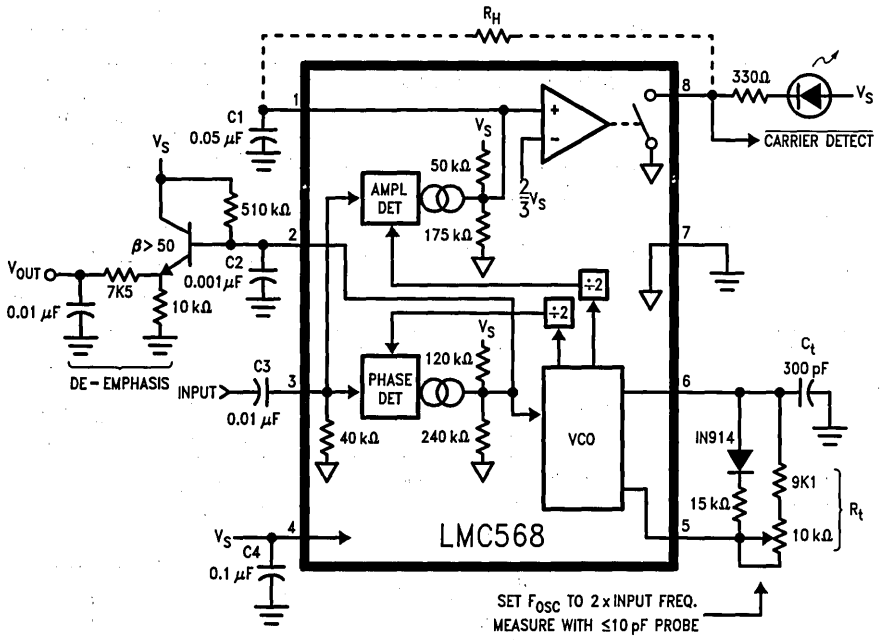
The LMC568 is an amplitude-linear phase-locked loop consisting of a linear VCO, fully balanced phase detectors, and a carrier detect output. LMCMOS™ technology is employed for high performance with low power consumption.

The VCO has a linearized control range of ±30% to allow demodulation of FM and FSK signals. Carrier detect is indicated when the PLL is locked to an input signal greater than 26 mVrms. LMC568 applications include FM SCA and TV second audio program decoders, FSK data demodulators, and voice pagers.

Features

- Demodulates ±15% deviation FM/FSK signals
- Carrier Detect Output with hysteresis
- Operation to 500 kHz input frequency
- Low THD—0.5% typ. for ±10% deviation
- 2V to 9V supply voltage range
- Low supply current drain

Typical Application (100 kHz input frequency, refer to notes pg. 3)



TL/H/9135–1

Order Number LMC568CM or LMC568CN
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage, Pin 3	$2\ V_{p-p}$
Supply Voltage, Pin 4	10V
Output Voltage, Pin 8	13V
Voltage at All Other Pins	V_S to Gnd
Output Current, Pin 8	30 mA
Package Dissipation	500 mW

Operating Temperature Range (T_A)	−25°C to +125°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

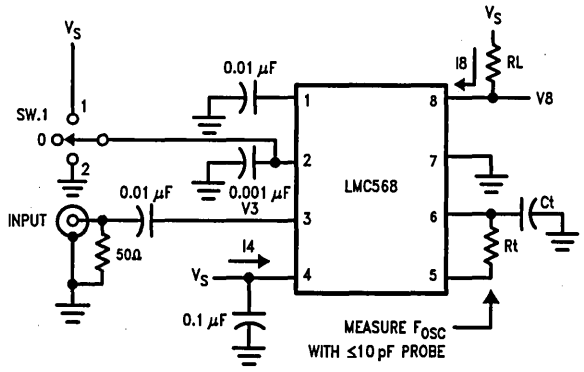
See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, $T_A = 25°C$, $V_S = 5V$, RtCt #2, Sw. 1 Pos. 0; and no input unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I4	Power Supply Current	RtCt #1, Quiescent or Activated	$V_S = 2V$		0.35		mAdc
			$V_S = 5V$		0.75	1.5	
			$V_S = 9V$		1.2	2.4	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	$V_S = 2V$		98		kHz
			$V_S = 5V$	90	103	115	
			$V_S = 9V$		105		
Δf_0	Center Frequency Shift with Supply	$\frac{f_0\|_{9V} - f_0\|_{2V}}{7\ f_0\|_{5V}} \times 100$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level until Pin 8 Goes Low.	$V_S = 2V$	8	16	25	mVrms
			$V_S = 5V$	15	26	42	
			$V_S = 9V$		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level until Pin 8 Goes High.			1.5		mVrms
V8	Output 'Sat' Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; L.D.B.W. $= \frac{F_{osc}\|_{P2} - F_{osc}\|_{P1}}{F_{osc}\|_{P0}} \times 100$	$V_S = 2V$		30		%
			$V_S = 5V$	40	55		
			$V_S = 9V$		60		
ΔBW	Bandwidth Skew	Skew $= \left(\frac{F_{osc}\|_{P2} + F_{osc}\|_{P1}}{2\ F_{osc}\|_{P0}} - 1\right) \times 100$			1	±5	%
V_{out}	Recovered Audio	Typical Application Circuit Input = 100 mVrms, F = 100 kHz F_{mod} = 400 Hz, ±10 kHz Dev.	$V_S = 2V$		170		mVrms
			$V_S = 5V$		270		
			$V_S = 9V$		400		
THD	Total Harmonic Distortion	Typical Application Circuit as Above, Measure V_{out} Distortion.			0.5		%
$\frac{S+N}{N}$	Signal to Noise Ratio	Typical Application Circuit Remove Modulation, Measure V_n $(S + N)/N = 20 \log (V_{out}/V_n)$.			65		dB
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2			700		kHz

Test Circuit



RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

TL/H/9135–3

Notes to Typical Application

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close to possible to pin 4. Also, due to pin voltages tracking supply, a large C4 is necessary for low frequency PSRR.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC568 must be set up to run at twice the frequency of the input signal. The components shown in the typical application are for F_{osc} = 200 kHz (100 kHz input frequency). For operation at lower frequencies, increase the capacitor value; for higher frequencies proportionally reduce the resistor values.

If low distortion is not a requirement, the series diode/resistor between pins 6 and 5 may be omitted. This will reduce VCO supply dependence and increase V_{out} by approximately 2 dB with THD = 2% typical. The center frequency as a function of Rt and Ct is given by:

$$F_{osc} \cong \frac{1}{1.4\ Rt\ Ct}\ Hz$$

To allow for I.C. and component value tolerences, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC568 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals that are centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via C3.

OUTPUT TAKEOFF

The output signal is taken off the loop filter at pin 2. Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). The nominal pin 2 source resistance is 80 kΩ, requiring the use of an external buffer transistor to drive nominal loads.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built-in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will become narrower than the LDBW. However, the maximum hold-in range will always equal the LDBW. The 2 kHz de-emphasis pole shown may be modified or omitted as required by the application.

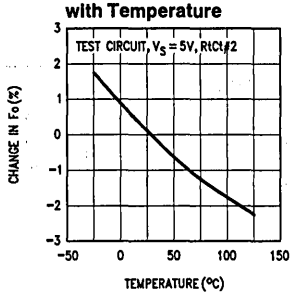
CARRIER DETECT

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_S. The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input is of sufficient amplitude to cause pin 1 to fall below 2/3 V_S. The carrier detect threshold is internally set to 26 mVrms typical on a 5V supply.

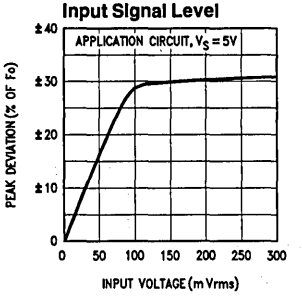
Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Optional resistor R_H increases the hysteresis in the pin 8 output for applications such as audio mute control. The minimum allowable value for R_H is 330 kΩ.

LMC568 Typical Performance Characteristics

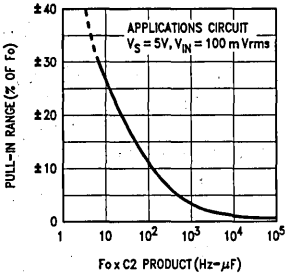
Frequency Drift with Temperature



Peak Deviation vs Input Signal Level



Pull-In Range as a Function of C2



TL/H/9135–2

National Semiconductor

LM4040
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4040 precision voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SOT-23 surface-mount package. The LM4040's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4040 easy to use. Further reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V. The minimum operating current increases from 60 μA for the LM4040-2.5 to 100 μA for the LM4040-10.0. All versions have a maximum operating current of 15 mA.

The LM4040 utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Also available is the LM4041 with two reverse breakdown voltage versions: adjustable and 1.2V. Please see the LM4041 data sheet.

Features

- Small packages: SOT-23, TO-92, and SO-8
- No output capacitor required
- Tolerates capacitive loads
- Fixed reverse breakdown voltages of 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V
- Contact National Semiconductor Analog Marketing for parts with extended temperature range

Key Specifications (LM4040-2.5)

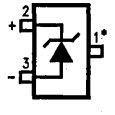
- Output voltage tolerance (A grade, 25°C) ±0.1% (max)
- Low output noise (10 Hz to 100 kHz) 35 μV_{rms} (typ)
- Wide operating current range 60 μA to 15 mA
- Industrial temperature range −40°C to +85°C
- Low temperature coefficient 100 ppm/°C (max)
- Contact National Semiconductor Analog Marketing for parts with lower temperature coefficient

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Automotive
- Precision Audio Components

Connection Diagrams

SOT-23



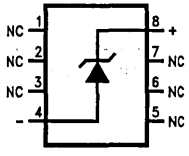
TL/H/11323-1

*This pin must be left floating or connected to pin 3.

Top View

See NS Package Number TO-236AB

SO-8

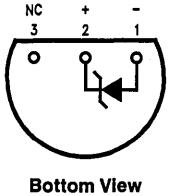


TL/H/11323-2

Top View

See NS Package Number M08A

TO-92



TL/H/11323-3

Bottom View

See NS Package Number Z03A

Ordering Information

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	Package		
	M3 (SOT-23)	Z (TO-92)	M (SO-8)
0.1%, 100 ppm/°C max (A grade)	LM4040AIM3-2.5, LM4040AIM3-4.1, LM4040AIM3-5.0, LM4040AIM3-8.2, LM4040AIM3-10.0 **See NS Package Number TO-236AB**	LM4040AIZ-2.5, LM4040AIZ-4.1, LM4040AIZ-5.0, LM4040AIZ-8.2, LM4040AIZ-10.0 **See NS Package Number Z03A**	LM4040AIM-2.5, LM4040AIM-4.1, LM4040AIM-5.0, LM4040AIM-8.2, LM4040AIM-10.0 **See NS Package Number M08A**
0.2%, 100 ppm/°C max (B grade)	LM4040BIM3-2.5, LM4040BIM3-4.1, LM4040BIM3-5.0, LM4040BIM3-8.2, LM4040BIM3-10.0 **See NS Package Number TO-236AB**	LM4040BIZ-2.5, LM4040BIZ-4.1, LM4040BIZ-5.0, LM4040BIZ-8.2, LM4040BIZ-10.0 **See NS Package Number Z03A**	LM4040BIM-2.5, LM4040BIM-4.1, LM4040BIM-5.0, LM4040BIM-8.2, LM4040BIM-10.0 **See NS Package Number M08A**
0.5%, 100 ppm/°C max (C grade)	LM4040CIM3-2.5, LM4040CIM3-4.1, LM4040CIM3-5.0, LM4040CIM3-8.2, LM4040CIM3-10.0 **See NS Package Number TO-236AB**	LM4040CIZ-2.5, LM4040CIZ-4.1, LM4040CIZ-5.0, LM4040CIZ-8.2, LM4040CIZ-10.0 **See NS Package Number Z03A**	LM4040CIM-2.5, LM4040CIM-4.1, LM4040CIM-5.0, LM4040CIM-8.2, LM4040CIM-10.0 **See NS Package Number M08A**
1.0%, 150 ppm/°C max (D grade)	LM4040DIM3-2.5, LM4040DIM3-4.1, LM4040DIM3-5.0, LM4040DIM3-8.2, LM4040DIM3-10.0 **See NS Package Number TO-236AB**	LM4040DIZ-2.5, LM4040DIZ-4.1, LM4040DIZ-5.0, LM4040DIZ-8.2, LM4040DIZ-10.0, **See NS Package Number Z03A**	LM4040DIM-2.5, LM4040DIM-4.1, LM4040DIM-5.0, LM4040DIM-8.2, LM4040DIM-10.0 **See NS Package Number M08A**
2.0%, 150 ppm/°C max (E grade)	LM4040EIM3-2.5 **See NS Package Number TO-236AB**	LM4040EIZ-2.5 **See NS Package Number Z03A**	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	20 mA
Forward Current	10 mA
Power Dissipation (T_A = 25°C) (Note 2)	
M Package	540 mW
M3 Package	306 mW
Z Package	550 mW
Storage Temperature	−65°C to +150°C
Lead Temperature	
M and M3 Packages	
Vapor phase (60 seconds)	+215°C
Infrared (15 seconds)	+220°C
Z Package	
Soldering (10 seconds)	+260°C
ESD Susceptibility	
Human Body Model (Note 3)	2 kV
Machine Model (Note 3)	200V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1 & 2)

Temperature Range	
($T_{min} \le T_A \le T_{max}$)	$-40°C \le T_A \le +85°C$
Reverse Current	
LM4040-2.5	60 μA to 15 mA
LM4040-4.1	68 μA to 15 mA
LM4040-5.0	74 μA to 15 mA
LM4040-8.2	91 μA to 15 mA
LM4040-10.0	100 μA to 15 mA

LM4040-2.5

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	2.500			V
	Reverse Breakdown Voltage Tolerance	I_R = 100 μA		±2.5 **±19**	±5.0 **±21**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 60 **65**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	20 15 15	**100**	**100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.3	 0.8 **1.0**	 0.8 **1.0**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	2.5	 6.0 **8.0**	 6.0 **8.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.3	 0.8	 0.8	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	35			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-2.5 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C, D and E designate initial Reverse Breakdown Voltage tolerances of ±0.5%, ±1.0% and ±2.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	LM4040EIM3 LM4040EIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	2.500				V
	Reverse Breakdown Voltage Tolerance	I_R = 100 μA		±12 **±29**	±25 **±49**	±50 **±74**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 65 **70**	 65 **70**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	20 15 15	 **100**	 **150**	 **150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.4	 0.8 **1.0**	 1.0 **1.2**	 1.0 **1.2**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	2.5	 6.0 **8.0**	 8.0 **10.0**	 8.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz $I_{AC} = 0.1\ I_R$	0.3	 0.9	 1.1	 1.1	Ω Ω(max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	35				μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120				ppm

LM4040-4.1

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	4.096			V
	Reverse Breakdown Voltage Tolerance	I_R = 100 μA		±4.1 **±31**	±8.2 **±35**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		50	 68 **73**	 68 **73**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	30 20 20	 **100**	 **100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.5	 0.9 **1.2**	 0.9 **1.2**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	3.0	 7.0 **10.0**	 7.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.0	 1.0	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-4.1 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	4.096			V
	Reverse Breakdown Voltage Tolerance	I_R = 100 μA		±20 **±47**	±41 **±81**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		50	 68 **73**	 73 **78**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	30 20 20	 **100**	 **150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.5	 0.9 **1.2**	 1.2 **1.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	3.0	 7.0 **10.0**	 9.0 **13.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.0	 1.3	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-5.0

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	5.000			V
	Reverse Breakdown Voltage Tolerance	I_R = 100 μA		±5.0 **±38**	±10 **±43**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		54	 74 **80**	 74 **80**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	30 20 20	 **100**	 **100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.5	 1.0 **1.4**	 1.0 **1.4**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	3.5	 8.0 **12.0**	 8.0 **12.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	1.1	1.1	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	40			ppm

LM4040-5.0 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	5.000			V
	Reverse Breakdown Voltage Tolerance	I_R = 100 μA		±25 **±58**	±50 **±99**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		54	 74 **80**	 79 **85**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	30 20 20	 **100**	 **150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.5	 1.0 **1.3**	 1.3 **1.8**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	3.5	 8.0 **12.0**	 10.0 **15.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.1	 1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-8.2

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	8.192			V
	Reverse Breakdown Voltage Tolerance	I_R = 150 μA		±8.2 **±61**	±16 **±70**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		67	 91 **95**	 91 **95**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	40 20 20	 **100**	 **100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.6	 1.3 **2.5**	 1.3 **2.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	7.0	 10.0 **18.0**	 10.0 **18.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.6	 1.5	 1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	130			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

LM4040-8.2 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	8.192			V
	Reverse Breakdown Voltage Tolerance	I_R = 150 μA		±41 **±94**	±82 **±162**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		67	 91 **95**	 96 **100**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	40 20 20	 **100**	 **150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA	0.6	 1.3 **2.5**	 1.7 **3.0**	mV mV (max) mV (max)
		1 mA ≤ I_R ≤ 15 mA	7.0	 10.0 **18.0**	 15.0 **24.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.6	 1.5	 1.9	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	130			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

LM4040-10.0

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	10.00			V
	Reverse Breakdown Voltage Tolerance	I_R = 150 μA		±10 **±75**	±20 **±85**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		75	 100 **103**	 100 **103**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	40 20 20	 **100**	 **100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.8	 1.5 **3.5**	 1.6 **3.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	8.0	 12.0 **23.0**	 12.0 **23.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.7	 1.7	 1.7	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	180			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

LM4040-10.0 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	10.00			V
	Reverse Breakdown Voltage Tolerance	I_R = 150 μA		±50 **±115**	±100 **±198**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		75	 100 **103**	 110 **113**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	40 20 20	 **100**	 **150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA	0.8	 1.5 **3.5**	 2.0 **4.0**	mV mV (max) mV (max)
		1 mA ≤ I_R ≤ 15 mA	8.0	 12.0 **23.0**	 18.0 **29.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, I_{AC} = 0.1 I_R	0.7	 1.7	 2.3	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	180			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4040, T_{Jmax} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 185°C/W for the M package, 326°C/W for the SOT-23 package, and 180°C/W with 0.4" lead length and 170°C/W with 0.125" lead length for the TO-92 package.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: Typicals are at T_J = 25°C and represent most likely parametric norm.

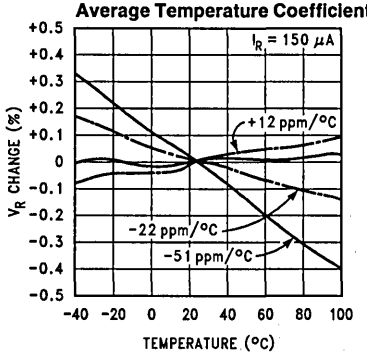
Note 5: Limits are 100% production tested at 25°C. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

Note 6: The boldface (over-temperature) limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance ±[($\Delta V_R/\Delta T$)(65°C)(V_R)]. $\Delta V_R/\Delta T$ is the V_R temperature coefficient, 65°C is the temperature range from −40°C to the reference point of 25°C, and V_R is the reverse breakdown voltage. The total over-temperature tolerance for the different grades is shown below:

A-grade: ±0.75% = ±0.1% ±100 ppm/°C × 65°C
B-grade: ±0.85% = ±0.2% ±100 ppm/°C × 65°C
C-grade: ±1.15% = ±0.5% ±100 ppm/°C × 65°C
D-grade: ±1.98% = ±1.0% ±150 ppm/°C × 65°C
E-grade: ±2.98% = ±1.0% ±150 ppm/°C × 65°C
Therefore, as an example, the A-grade LM4040-2.5 has an over-temperature Reverse Breakdown Voltage tolerance of ±2.5V × 0.75% = ±19 mV.

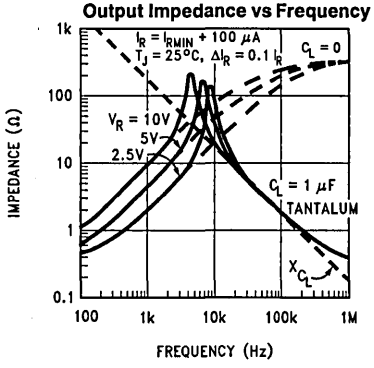
Typical Performance Characteristics

Temperature Drift for Different Average Temperature Coefficient



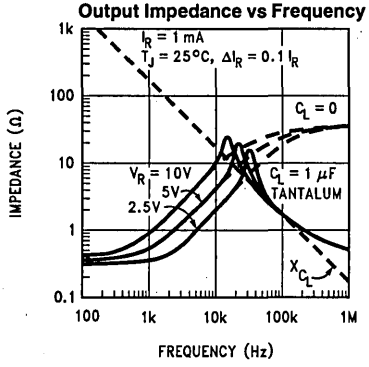
TL/H/11323-4

Output Impedance vs Frequency



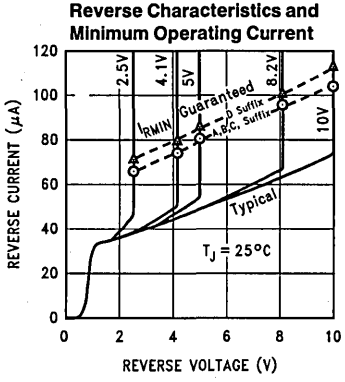
TL/H/11323-10

Output Impedance vs Frequency



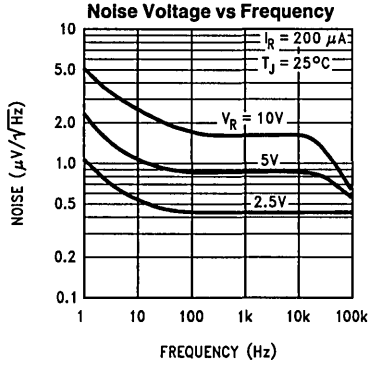
TL/H/11323-11

Reverse Characteristics and Minimum Operating Current



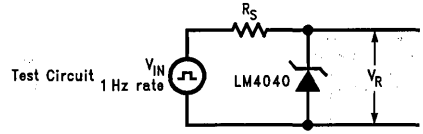
TL/H/11323-12

Noise Voltage vs Frequency

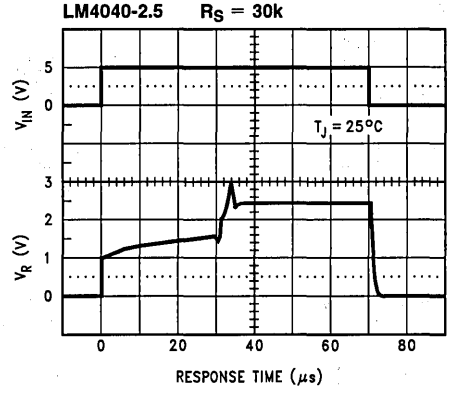


TL/H/11323-13

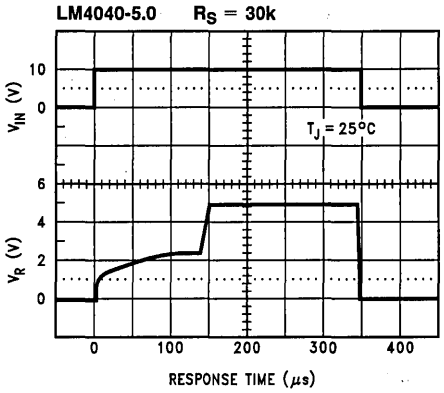
Start-Up Characteristics



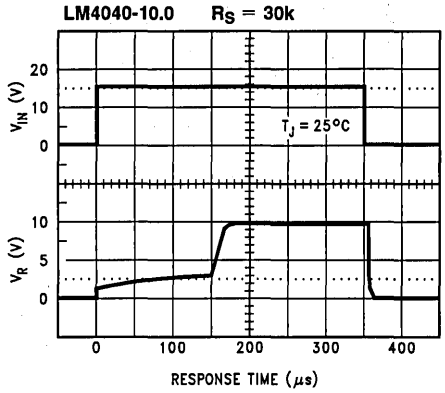
TL/H/11323-5



TL/H/11323-7

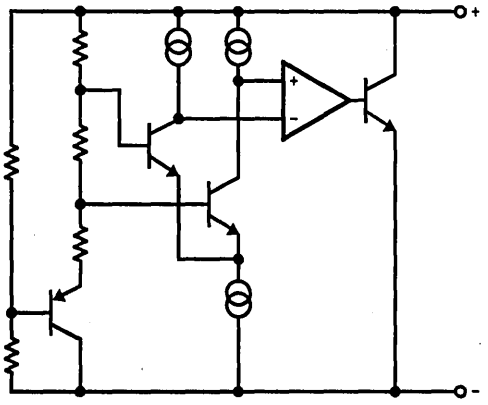


TL/H/11323-8



TL/H/11323-9

Functional Block Diagram



TL/H/11323–14

Applications Information

The LM4040 is a precision micro-power curvature-corrected bandgap shunt voltage reference. For space critical applications, the LM4040 is available in the sub-miniature SOT-23 surface-mount package. The LM4040 has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "−" pin. If, however, a bypass capacitor is used, the LM4040 remains stable. Reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V. The minimum operating current increases from 60 μA for the LM4040-2.5 to 100 μA for the LM4040-10.0. All versions have a maximum operating current of 15 mA.

LM4040s in the SOT-23 packages have a parasitic Schottky diode between pin 3 (−) and pin 1 (Die attach interface contact). Therefore, pin 1 of the SOT-23 package must be left floating or connected to pin 3.

The 4.096V version allows single +5V 12-bit ADCs or DACs to operate with an LSB equal to 1 mV. For 12-bit ADCs or DACs that operate on supplies of 10V or greater, the 8.192V version gives 2 mV per LSB.

In a conventional shunt regulator application *(Figure 1)*, an external series resistor (R_S) is connected between the supply voltage and the LM4040. R_S determines the current that flows through the load (I_L) and the LM4040 (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the LM4040 even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4040 is less than 15 mA.

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_Q), and the LM4040's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q}$$

Typical Applications

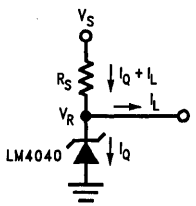


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FIGURE 1. Shunt Regulator

Typical Applications (Continued)

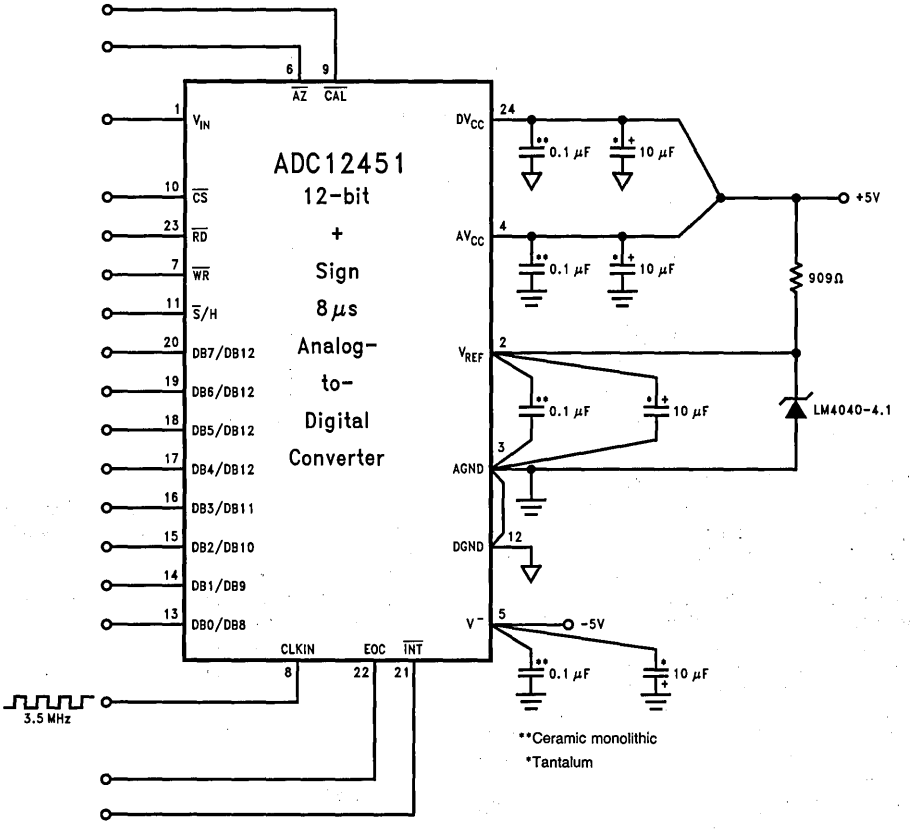
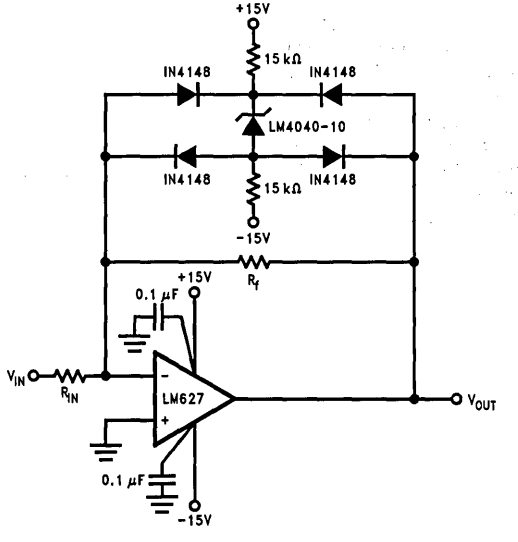


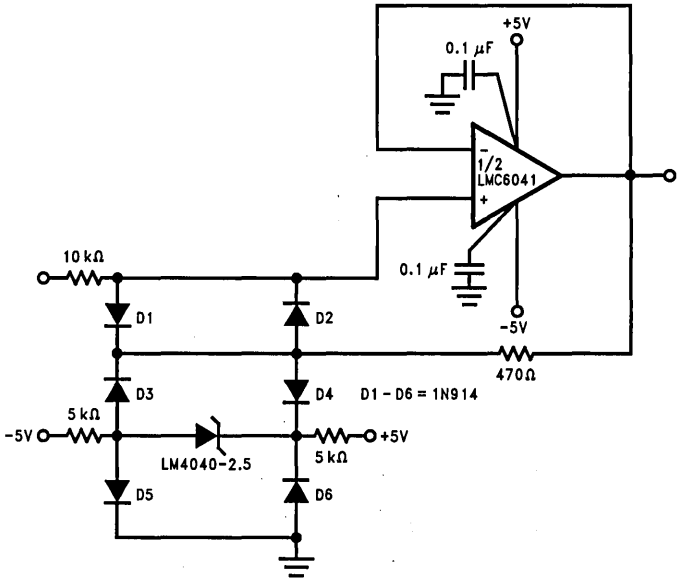
FIGURE 2. LM4040-4.1's Nominal 4.096 breakdown voltage gives ADC12451 1 mV/LSB TL/H/11323-16



TL/H/11323-17

FIGURE 3. Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage. Nominal clamping voltage is ±11.5V (LM4040's reverse breakdown voltage + 2 diode V_F).

Typical Applications (Continued)



TL/H/11323-18

FIGURE 4. Protecting Op Amp Input. The bounding voltage is ±4V with the LM4040-2.5 (LM4040's reverse breakdown voltage + 3 diode V_F).

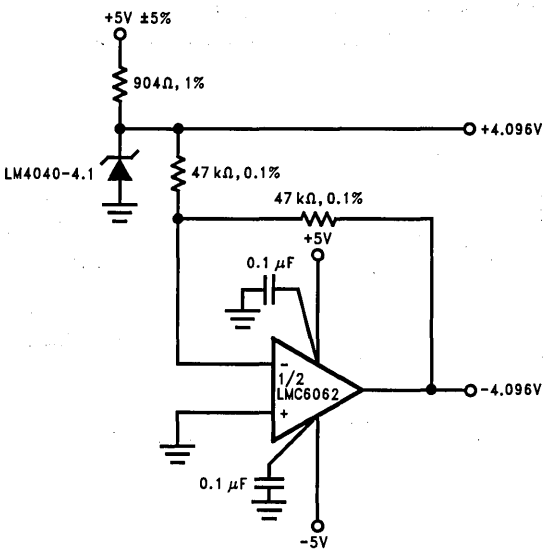


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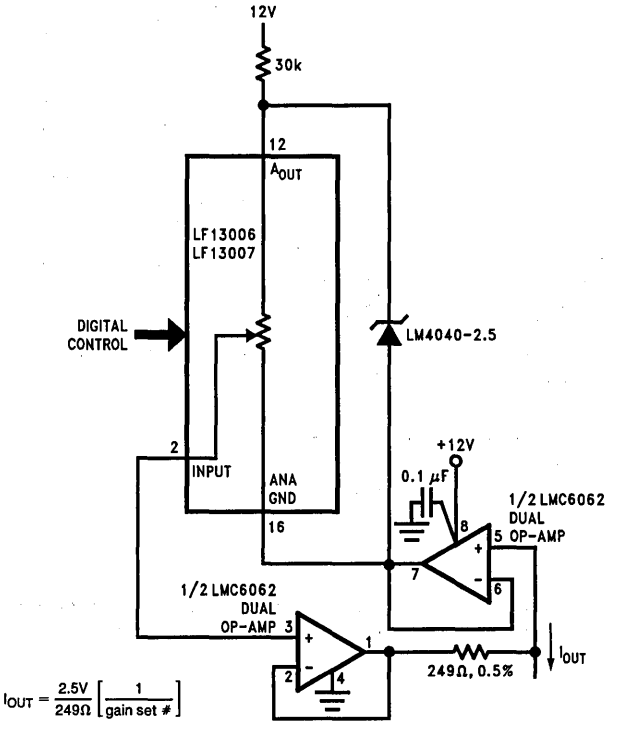
FIGURE 5. Precision ±4.096V Reference

Typical Applications (Continued)



TL/H/11323-20

FIGURE 6. Programmable Current Source

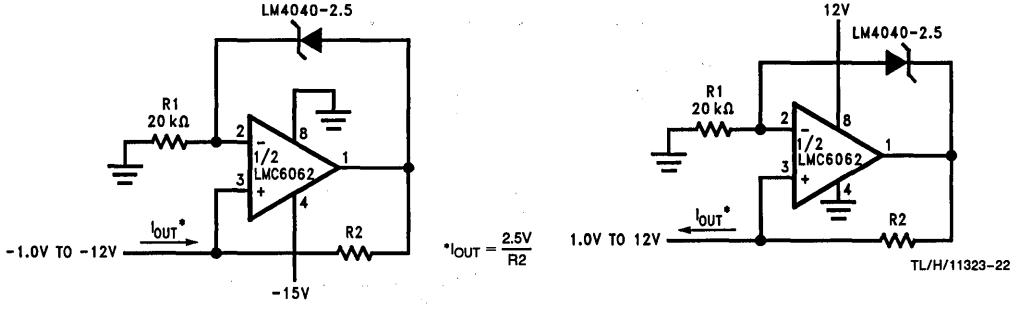


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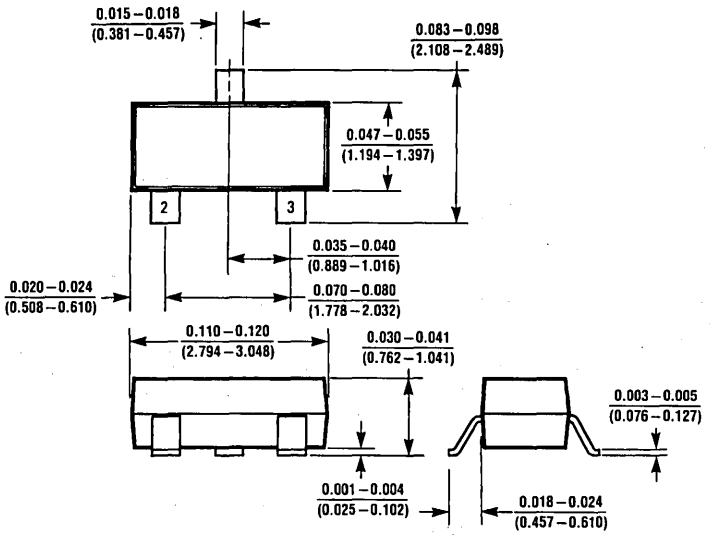
FIGURE 7. Precision 1 μA to 1 mA Current Sources

Packaging Information



TL/H/11323–24

Plastic Surface Mount Package (M3)
NS Package Number TO-236AB

National Semiconductor

LM113/LM313 Reference Diode

General Description

The LM113/LM313 are temperature compensated, low voltage reference diodes. They feature extremely-tight regulation over a wide range of operating currents in addition to an unusually-low breakdown voltage and good temperature stability.

The diodes are synthesized using transistors and resistors in a monolithic integrated circuit. As such, they have the same low noise and long term stability as modern IC op amps. Further, output voltage of the reference depends only on highly-predictable properties of components in the IC; so they can be manufactured and supplied to tight tolerances.

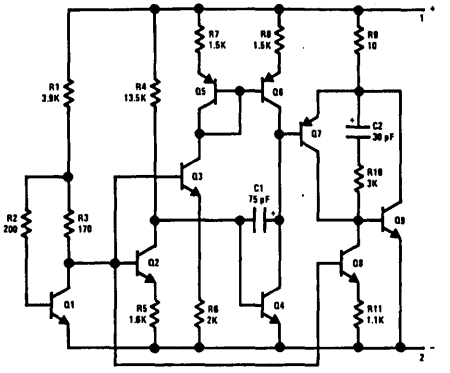
- Dynamic impedance of 0.3Ω from 500 μA to 20 mA
- Temperature stability typically 1% over −55°C to 125°C range (LM113), 0°C to 70°C (LM313)
- Tight tolerance: ±5%, ±2% or ±1%

The characteristics of this reference recommend it for use in bias-regulation circuitry, in low-voltage power supplies or in battery powered equipment. The fact that the breakdown voltage is equal to a physical property of silicon—the energy-band gap voltage—makes it useful for many temperature-compensation and temperature-measurement functions.

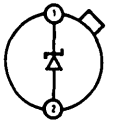
Features

- Low breakdown voltage: 1.220V

Schematic and Connection Diagrams



Metal Can Package



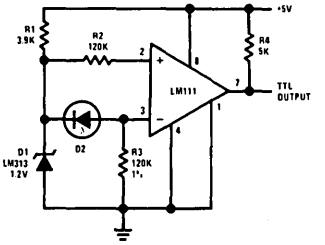
Note: Pin 2 connected to case.
TOP VIEW

Order Number LM113H or LM113-1H or LM113-2H or LM313H
See NS Package Number H02A

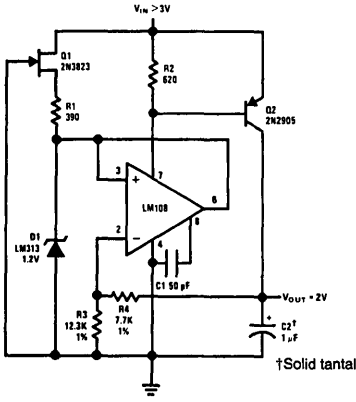
TL/H/5713-1

Typical Applications

Level Detector for Photodiode



Low Voltage Regulator



†Solid tantalum.

TL/H/5713-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 3)

Power Dissipation (Note 1)	100 mW
Reverse Current	50 mA
Forward Current	50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature Range	
LM113	−55°C to +125°C
LM313	0°C to +70°C

Electrical Characteristics (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
Reverse Breakdown Voltage					
LM113/LM313	I_R = 1 mA	1.160	1.220	1.280	V
LM113-1		1.210	1.22	1.232	V
LM113-2		1.195	1.22	1.245	V
Reverse Breakdown Voltage Change	0.5 mA ≤ I_R ≤ 20 mA		6.0	15	mV
Reverse Dynamic Impedance	I_R = 1 mA		0.2	1.0	Ω
	I_R = 10 mA		0.25	0.8	Ω
Forward Voltage Drop	I_F = 1.0 mA		0.67	1.0	V
RMS Noise Voltage	10 Hz ≤ f ≤ 10 kHz, I_R = 1 mA		5		μV
Reverse Breakdown Voltage Change with Current	0.5 mA ≤ I_R ≤ 10 mA, T_{MIN} ≤ T_A ≤ T_{MAX}			15	mV
Breakdown Voltage Temperature Coefficient	1.0 mA ≤ I_R ≤ 10 mA, T_{MIN} ≤ T_A ≤ T_{MAX}		0.01		%/°C

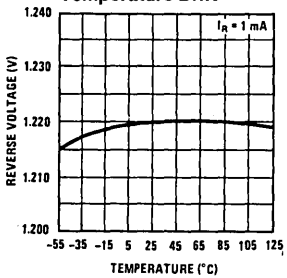
Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction and a thermal resistance of 80°C/W junction to case or 440°C/W junction to ambient.

Note 2: These specifications apply for T_A = 25°C, unless stated otherwise. At high currents, breakdown voltage should be measured with lead lengths less than ¼ inch. Kelvin contact sockets are also recommended. The diode should not be operated with shunt capacitances between 200 pF and 0.1 μF, unless isolated by at least a 100Ω resistor, as it may oscillate at some currents.

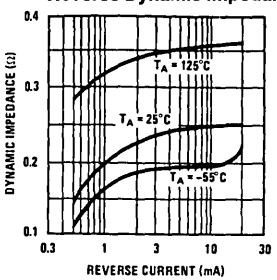
Note 3: Refer to the following RETS drawings for military specifications: RETS113-1X for LM113-1, RETS113-2X for LM113-2 or RETS113X for LM113.

Typical Performance Characteristics

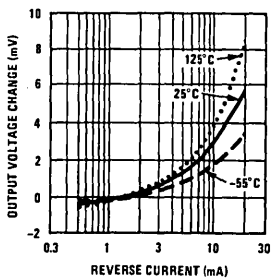
Temperature Drift



Reverse Dynamic Impedance



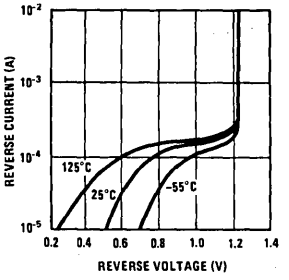
Reverse Characteristics



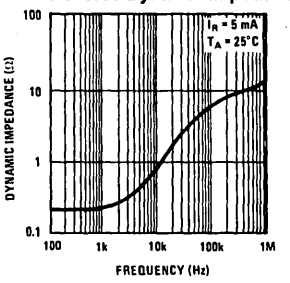
TL/H/5713–3

Typical Performance Characteristics (Continued)

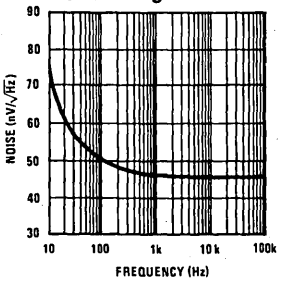
Reverse Characteristics



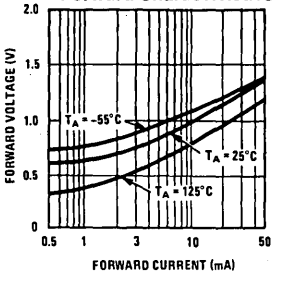
Reverse Dynamic Impedance



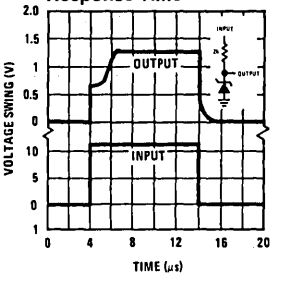
Noise Voltage



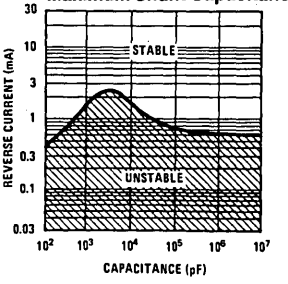
Forward Characteristics



Response Time



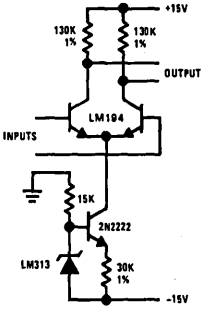
Maximum Shunt Capacitance



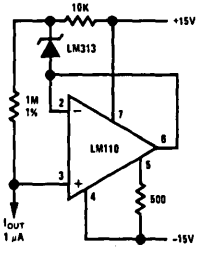
TL/H/5713–4

Typical Applications (Continued)

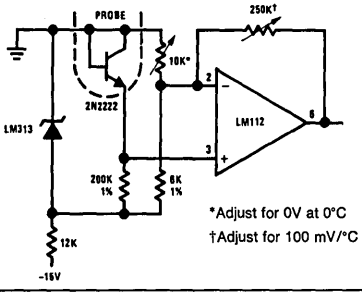
Amplifier Biasing for Constant Gain with Temperature



Constant Current Source



Thermometer



*Adjust for 0V at 0°C
†Adjust for 100 mV/°C

TL/H/5713–5

National Semiconductor

LM136-2.5/LM236-2.5/LM336-2.5V Reference Diode

General Description

The LM136-2.5/LM236-2.5 and LM336-2.5 integrated circuits are precision 2.5V shunt regulator diodes. These monolithic IC voltage references operate as a low-temperature-coefficient 2.5V zener with 0.2Ω dynamic impedance. A third terminal on the LM136-2.5 allows the reference voltage and temperature coefficient to be trimmed easily.

The LM136-2.5 series is useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from 5V logic supplies. Further, since the LM136-2.5 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

The LM136-2.5 is rated for operation over −55°C to +125°C while the LM236-2.5 is rated over a −25°C to +85°C temperature range.

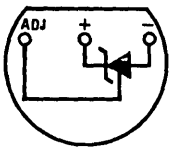
The LM336-2.5 is rated for operation over a 0°C to +70°C temperature range. See the connection diagrams for available packages.

Features

- Low temperature coefficient
- Wide operating current of 400 μA to 10 mA
- 0.2Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

Connection Diagrams

TO-92
Plastic Package

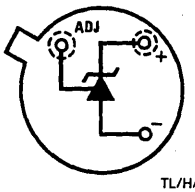


TL/H/5715–8

Bottom View

Order Number LM236Z-2.5, LM236AZ-2.5, LM336Z-2.5 or LM336BZ-2.5
See NS Package Number Z03A

TO-46
Metal Can Package

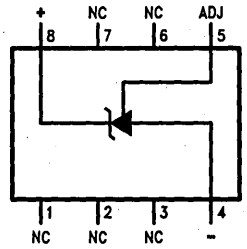


TL/H/5715–20

Bottom View

Order Number LM136H-2.5, LM136H-2.5/883, LM236H-2.5, LM336H-2.5, LM136AH-2.5 or LM236AH-2.5
See NS Package Number H03H

SO Package



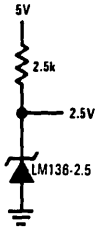
TL/H/5715–12

Top View

Order Number LM236M-2.5, LM336M-2.5 or LM336BM-2.5
See NS Package Number M08A

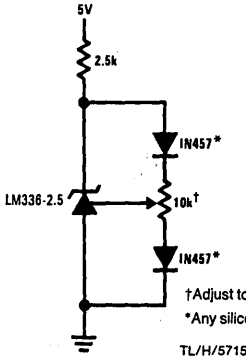
Typical Applications

2.5V Reference



TL/H/5715–9

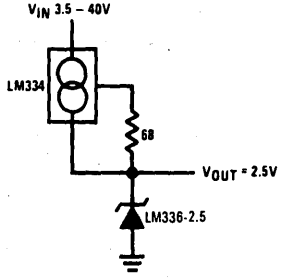
2.5V Reference with Minimum Temperature Coefficient



†Adjust to 2.490V
*Any silicon signal diode

TL/H/5715–10

Wide Input Range Reference



TL/H/5715–11

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	−60°C to +150°C
Operating Temperature Range (Note 2)	
LM136	−55°C to +150°C
LM236	−25°C to +85°C
LM336	0°C to +70°C

Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM136A-2.5/LM236A-2.5 LM136-2.5/LM236-2.5			LM336B-2.5 LM336-2.5			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1$ mA							
	LM136/LM236/LM336	2.440	2.490	2.540	2.390	2.490	2.590	V
	LM136A/LM236A, LM336B	2.465	2.490	2.515	2.440	2.490	2.540	V
Reverse Breakdown Change With Current	$T_A = 25°C$, 400 μA ≤ I_R ≤ 10 mA		2.6	6		2.6	10	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1$ mA, f = 100 Hz		0.2	0.6		0.2	1	Ω
Temperature Stability (Note 4)	V_R Adjusted to 2.490V, $I_R = 1$ mA, *(Figure 2)*							
	0°C ≤ T_A ≤ 70°C (LM336)					1.8	6	mV
	−25°C ≤ T_A ≤ +85°C (LM236H, LM236Z)		3.5	9				mV
	−25°C ≤ T_A ≤ +85°C (LM236M)		7.5	18				mV
	−55°C ≤ T_A ≤ +125°C (LM136)		12	18				mV
Reverse Breakdown Change With Current	400 μA ≤ I_R ≤ 10 mA		3	10		3	12	mV
Reverse Dynamic Impedance	$I_R = 1$ mA		0.4	1		0.4	1.4	Ω
Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1$ mA, t = 1000 hrs		20			20		ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: For elevated temperature operation, T_j max is:

LM136	150°C
LM236	125°C
LM336	100°C

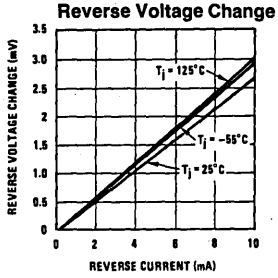
Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4" leads) 170°C/W (0.125" lead)	440°C/W	165°C/W
θ_{ja} (Junction to Case)	n/a	80°C/W	n/a

Note 3: Unless otherwise specified, the LM136-2.5 is specified from −55°C ≤ T_A ≤ +125°C, the LM236-2.5 from −25°C ≤ T_A ≤ +85°C and the LM336-2.5 from 0°C ≤ T_A ≤ +70°C.

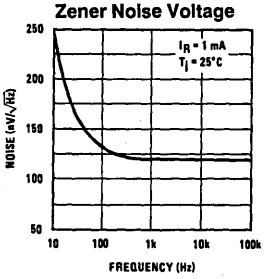
Note 4: Temperature stability for the LM336 and LM236 family is guaranteed by design. Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels. Stability is defined as the maximum change in V_{ref} from 25°C to T_A (min) or T_A (max).

Typical Performance Characteristics

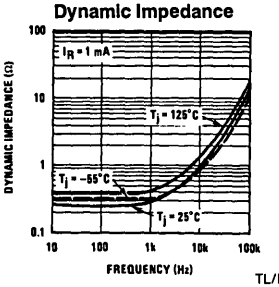
Reverse Voltage Change



Zener Noise Voltage



Dynamic Impedance



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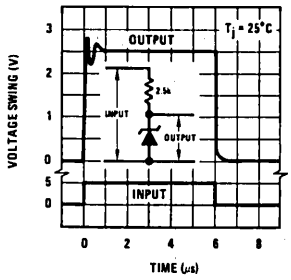
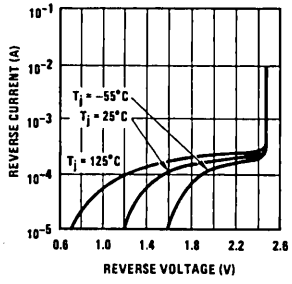
Typical Performance Characteristics (Continued)

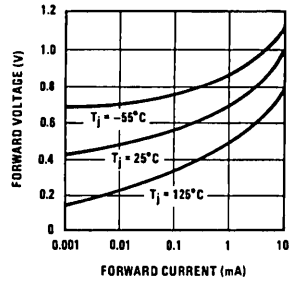
Response Time



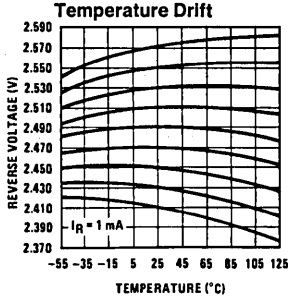
Reverse Characteristics



Forward Characteristics



Temperature Drift



TL/H/5715–3

Application Hints

The LM136 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

If minimum temperature coefficient is desired, two diodes can be added in series with the adjustment potentiometer as shown in *Figure 2*. When the device is adjusted to 2.490V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136. It is usually sufficient to mount the diodes near the LM136 on the printed circuit board. The absolute resistance of R1 is not critical and any value from 2k to 20k will work.

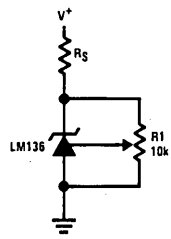


FIGURE 1. LM136 With Pot for Adjustment of Breakdown Voltage (Trim Range = ±120 mV typical)

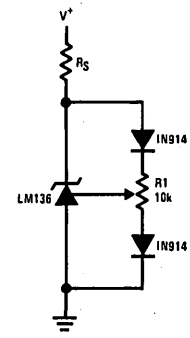


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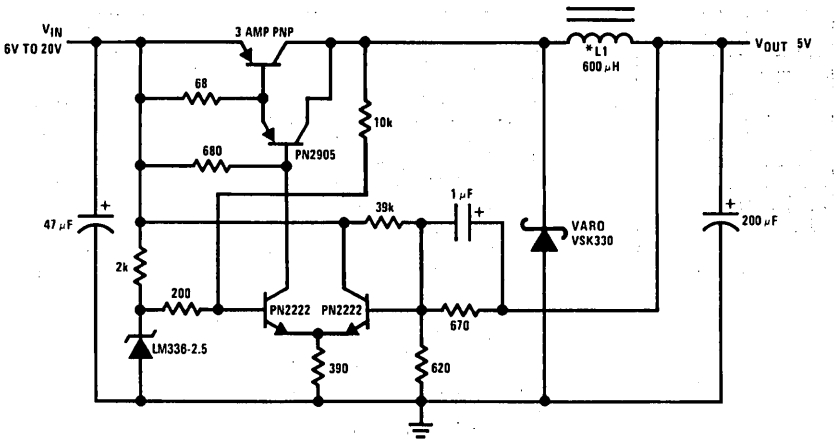
FIGURE 2. Temperature Coefficient Adjustment (Trim Range = ±70 mV typical)

Typical Applications (Continued)

Low Cost 2 Amp Switching Regulator†



*L1 60 turns #16 wire on Arnold Core A-254168-2

†Efficiency ≈ 80%

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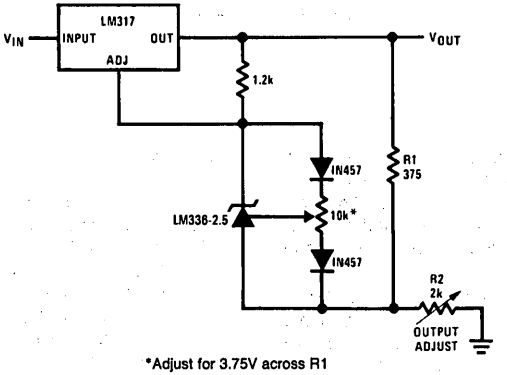
Precision Power Regulator with Low Temperature Coefficient



*Adjust for 3.75V across R1

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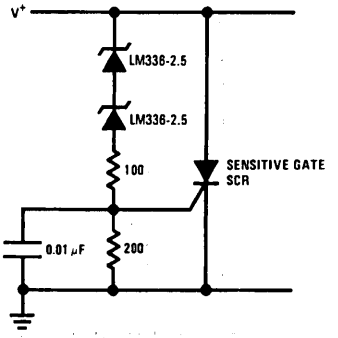
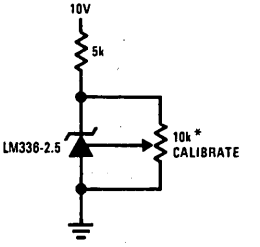
5V Crowbar



TL/H/5715–14

Trimmed 2.5V Reference with Temperature Coefficient Independent of Breakdown Voltage

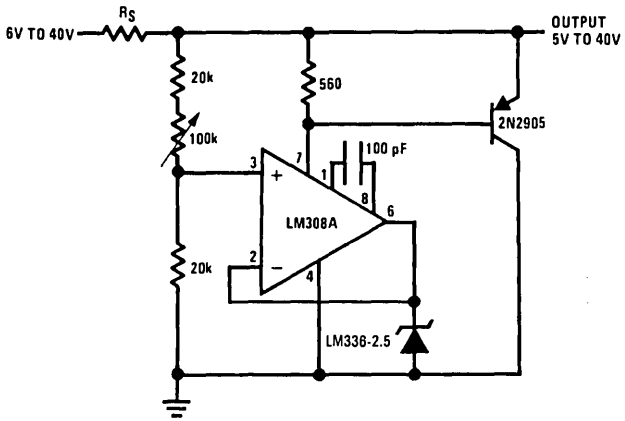


*Does not affect temperature coefficient

TL/H/5715–15

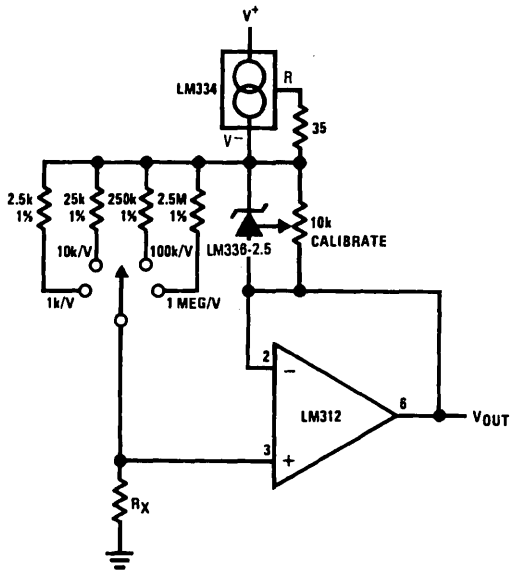
Typical Applications (Continued)

Adjustable Shunt Regulator



TL/H/5715–6

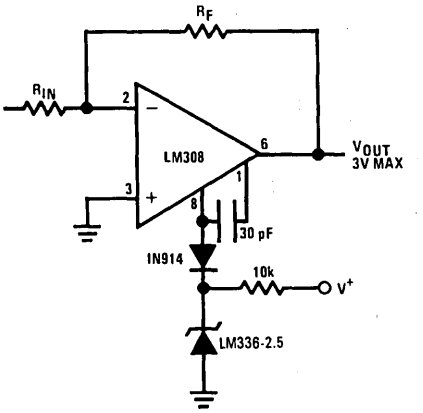
Linear Ohmmeter



TL/H/5715–16

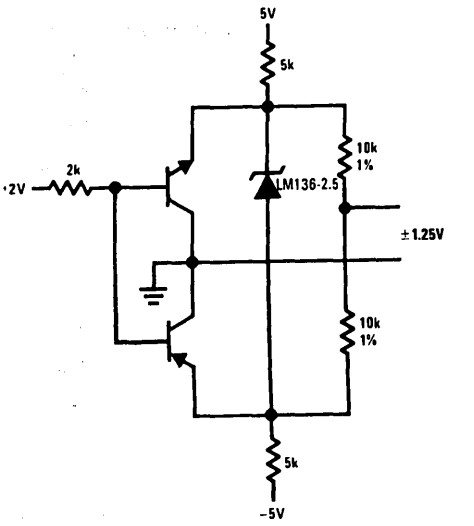
Typical Applications (Continued)

Op Amp with Output Clamped



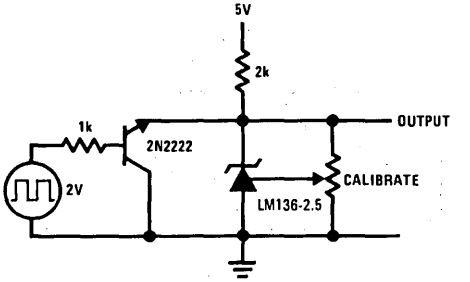
TL/H/5715–17

Bipolar Output Reference



TL/H/5715–18

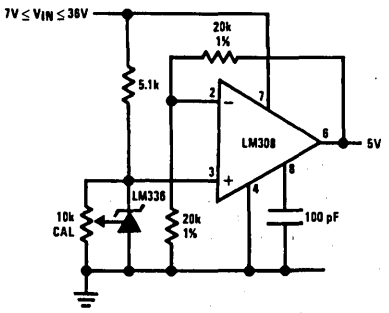
2.5V Square Wave Calibrator



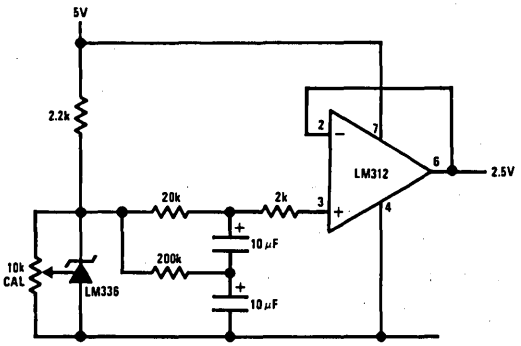
TL/H/5715–19

Typical Applications (Continued)

5V Buffered Reference

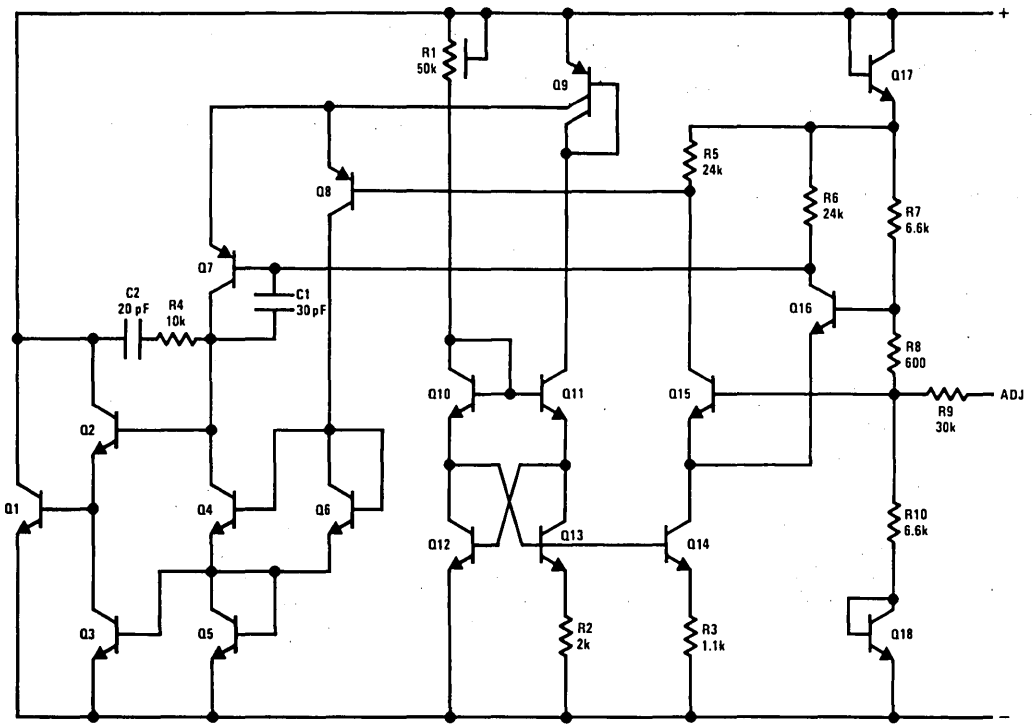


Low Noise Buffered Reference



TL/H/5715–7

Schematic Diagram



TL/H/5715–1

National Semiconductor

LM185-1.2/LM285-1.2/LM385-1.2 Micropower Voltage Reference Diode

General Description

The LM185-1.2/LM285-1.2/LM385-1.2 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185-1.2 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-1.2 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185-1.2 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

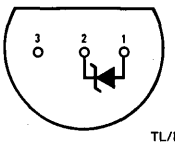
The LM185-1.2 is rated for operation over a −55°C to 125°C temperature range while the LM285-1.2 is rated −40°C to 85°C and the LM385-1.2 0°C to 70°C. The LM185-1.2/LM285-1.2 are available in a hermetic TO-46 package and the LM285-1.2/LM385-1.2 are also available in a low-cost TO-92 molded package, as well as S.O.

Features

- ±4 mV (±0.3%) max. initial tolerance (A grade)
- Operating current of 10 μA to 20 mA
- 0.6Ω max dynamic impedance (A grade)
- Low temperature coefficient
- Low voltage reference—1.235V
- 2.5V device and adjustable device also available — LM185-2.5 series and LM185 series, respectively

Connection Diagrams

TO-92
Plastic Package (Z)

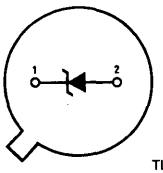


TL/H/5518–10

Bottom View

Order Number LM285Z-1.2, LM285AZ-1.2, LM285AXZ-1.2, LM285AYZ-1.2, LM285BXZ-1.2, LM285BYZ-1.2, LM385Z-1.2, LM385AZ-1.2, LM385AXZ-1.2, LM385AYZ-1.2, LM385BZ-1.2, LM385BXZ-1.2 or LM385BYZ-1.2
See NS Package Number Z03A

TO-46
Metal Can Package (H)

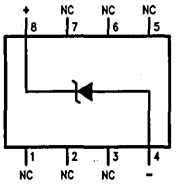


TL/H/5518–6

Bottom View

Order Number LM185H-1.2, LM185H-1.2/883, LM185AH-1.2, LM185AXH-1.2, LM185AYH-1.2, LM185BXH-1.2, LM185BYH-1.2, LM285H-1.2, LM285AH-1.2, LM285AXH-1.2, LM285AYH-1.2, LM285BXH-1.2, LM285BYH-1.2 or LM385H-1.2
See NS Package Number H02A

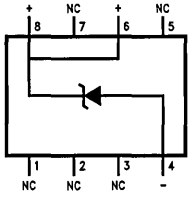
SO Package



TL/H/5518–9

Order Number LM285M-1.2, LM285AM-1.2, LM285AXM-1.2, LM285AYM-1.2, LM285BXM-1.2, LM285BYM-1.2, LM385M-1.2, LM385AM-1.2, LM385AXM-1.2, LM385AYM-1.2, LM385BM-1.2, LM385BXM-1.2 or LM385BYM-1.2
See NS Package Number M08A

SO Package
Alternate Pinout

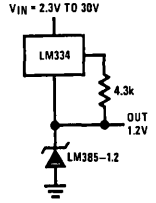


TL/H/5518–11

Order Number LM385SM-1.2, LM385ASM-1.2
See NS Package Number M08A

Typical Application

Wide Input Range Reference



TL/H/5518–8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range (Note 3)	
LM185-1.2	−55°C to +125°C
LM285-1.2	−40°C to +85°C
LM385-1.2	0°C to 70°C
Storage Temperature	−55°C to +150°C
Soldering Information	
TO-92 package: 10 sec.	260°C
TO-46 package: 10 sec.	300°C
SO package: Vapor phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM185A-1.2 LM185AX-1.2 LM185AY-1.2 LM285A-1.2 LM285AX-1.2 LM285AY-1.2			LM385A-1.2 LM385AX-1.2 LM385AY-1.2			Units (Limit)
		Typ	Tested Limit (Notes 5, 8)	Design Limit (Note 6)	Typ	Tested Limit (Note 5)	Design Limit (Note 6)	
Reverse Breakdown Voltage	I_R = 100 μA	1.235 **1.230**	1.231 1.239	 **1.220** **1.245**	1.235 **1.235**	1.231 1.239	 **1.225** **1.245**	V(Min) V(Max) V(Min) V(Max)
Minimum Operating Current		7	8	**10**	7	8	**10**	μA (Max)
Reverse Breakdown Voltage Change with Current	$I_{MIN} \le I_R \le$ 1 mA		1	**1.5**		1	**1.5**	mV (Max)
	1 mA ≤ $I_R \le$ 20 mA		10	**20**		10	**20**	mV (Max)
Reverse Dynamic Impedance	I_R = 100 μA, f = 20 Hz	0.2		0.6 **1.5**	0.2		0.6 **1.5**	Ω (Max)
Wideband Noise (rms)	I_R = 100 μA, 10 Hz ≤ f ≤ 10 kHz	60			60			μV
Long Term Stability	I_R = 100 μA, T = 1000 Hr, T_A = 25°C ±0.1°C	20			20			ppm
Average Temperature Coefficient (Note 7)	$I_{MIN} \le I_R \le$ 20 mA X Suffix Y Suffix All Others		 **30** **50**	 **150**		 **30** **50**	 **150**	ppm/°C (Max)

Electrical Characteristics (Continued) (Note 4)

Parameter	Conditions	Typ	LM185-1.2 LM185BX-1.2 LM185BY-1.2 LM285-1.2 LM285BX-1.2 LM285BY-1.2		LM385B-1.2 LM385BX-1.2 LM385BY-1.2		LM385-1.2		Units (Limit)
			Tested Limit (Notes 5, 8)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Reverse Breakdown Voltage	$T_A = 25°C$, $10\ \mu A \le I_R \le 20\ mA$	1.235	1.223 1.247		1.223 1.247		1.205 1.260		V(Min) V(Max)
Minimum Operating Current		8	10	**20**	15	**20**	15	**20**	μA (Max)
Reverse Breakdown Voltage Change with Current	$10\ \mu A \le I_R \le 1\ mA$		1	**1.5**	1	**1.5**	1	**1.5**	mV (Max)
	$1\ mA \le I_R \le 20\ mA$		10	**20**	20	**25**	20	**25**	mV (Max)
Reverse Dynamic Impedance	$I_R = 100\ \mu A$, f = 20 Hz	1							Ω
Wideband Noise (rms)	$I_R = 100\ \mu A$, 10 Hz ≤ f ≤ 10 kHz	60							μV
Long Term Stability	$I_R = 100\ \mu A$, T = 1000 Hr, $T_A = 25°C \pm 0.1°C$	20							ppm
Average Temperature Coefficient (Note 7)	$I_R = 100\ \mu A$ X Suffix Y Suffix All Others		**30** **50**	 **150**	**30** **50**	 **150**		 **150**	 ppm/°C ppm/°C ppm/°C (Max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Refer to RETS185H-1.2 for military specifications.

Note 3: For elevated temperature operation, T_j max is:

LM185 150°C
LM285 125°C
LM385 100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{JA} (junction to ambient)	180°C/W (0.4" leads) 170°C/W (0.125" leads)	440°C/W	165°C/W
θ_{JC} (junction to case)	N/A	80°C/W	N/A

Note 4: Parameters identified with **boldface type** apply at temperature extremes. All other numbers apply at $T_A = T_J = 25°C$.

Note 5: Guaranteed and 100% production tested.

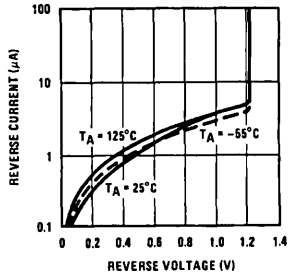
Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate average outgoing quality levels.

Note 7: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures between the operating T_{MAX} and T_{MIN}, divided by $T_{MAX} - T_{MIN}$. The measured temperatures are −55°C, −40°C, 0°C, 25°C, 70°C, 85°C, 125°C.

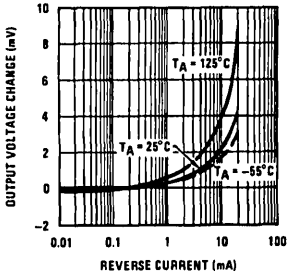
Note 8: A military RETS electrical specification is available on request.

Typical Performance Characteristics

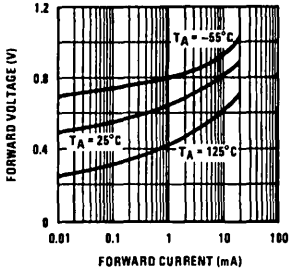
Reverse Characteristics



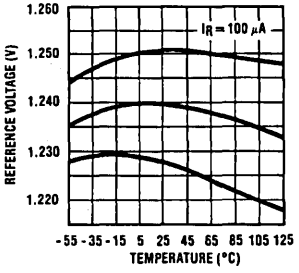
Reverse Characteristics



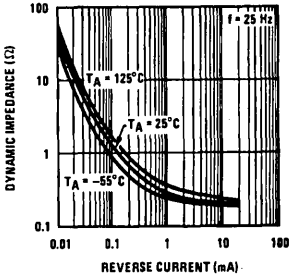
Forward Characteristics



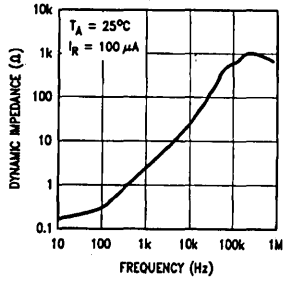
Temperature Drift of 3 Representative Units



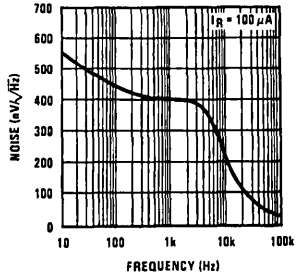
Reverse Dynamic Impedance



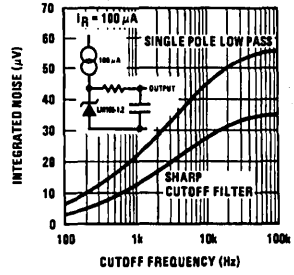
Reverse Dynamic Impedance



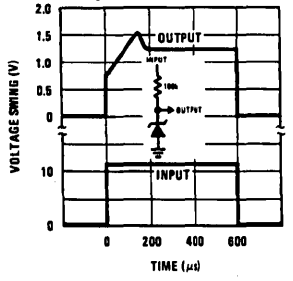
Noise Voltage



Filtered Output Noise



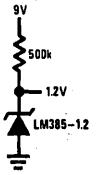
Response Time



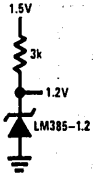
TL/H/5518–3

Typical Applications (Continued)

Micropower Reference from 9V Battery

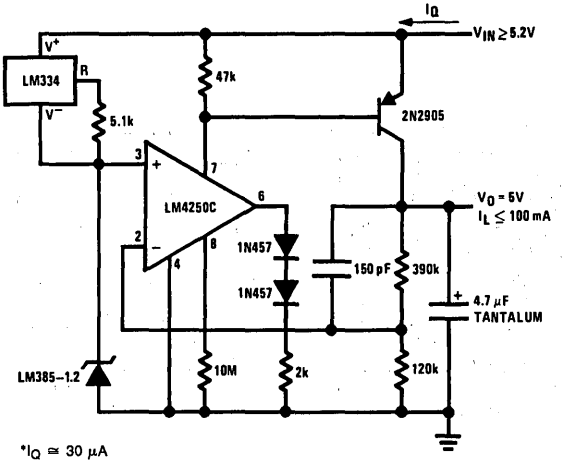


Reference from 1.5V Battery



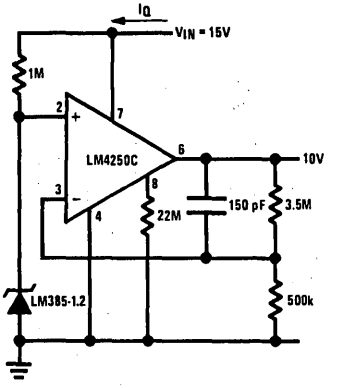
TL/H/5518-2

Micropower* 5V Regulator



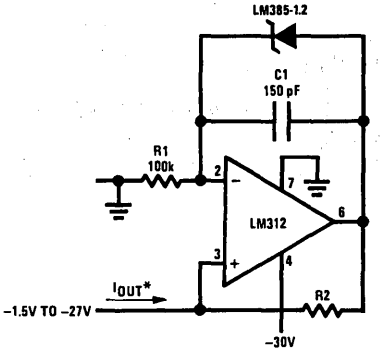
*$I_Q \cong 30\ \mu A$

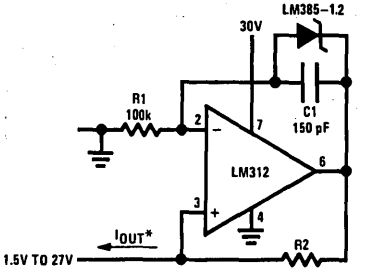
Micropower* 10V Reference



*$I_Q \cong 20\ \mu A$ standby current

Precision 1 μA to 1 mA Current Sources





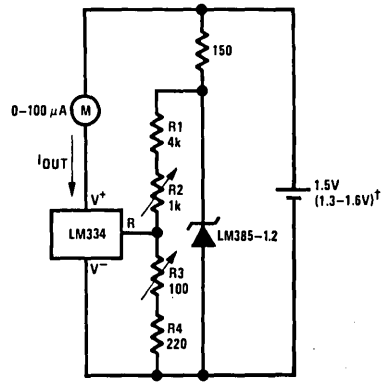
$$*I_{OUT} = \frac{1.23V}{R2}$$

TL/H/5518-4

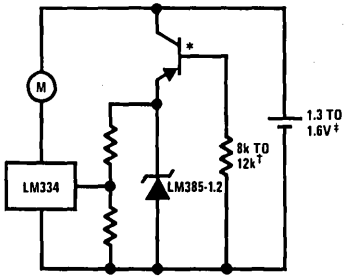
Typical Applications (Continued)

METER THERMOMETERS

0°C – 100°C Thermometer



Lower Power Thermometer



* 2N3638 or 2N2907 select for inverse $H_{FE} \cong 5$

† Select for operation at 1.3V

‡ $I_Q \cong 600\ \mu A$ to $900\ \mu A$

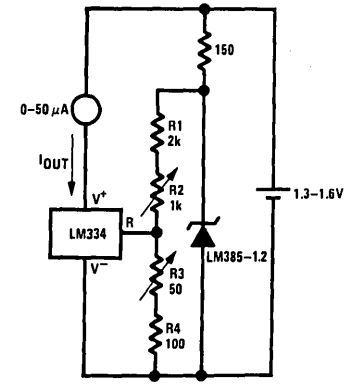
Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1 μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

†I_Q at 1.3V ≅ 500 μA

I_Q at 1.6V ≅ 2.4 mA

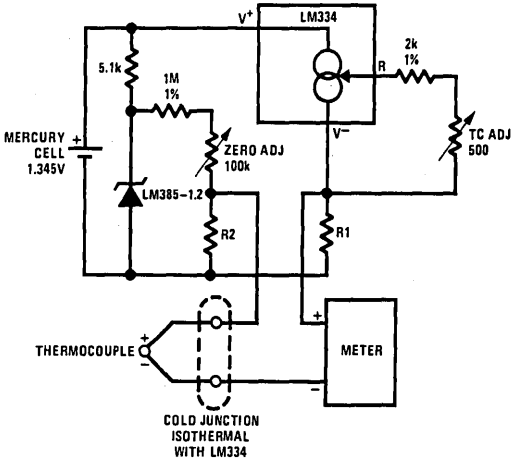
0°F – 50°F Thermometer



Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

Micropower Thermocouple Cold Junction Compensator



TL/H/5518–5

Adjustment Procedure

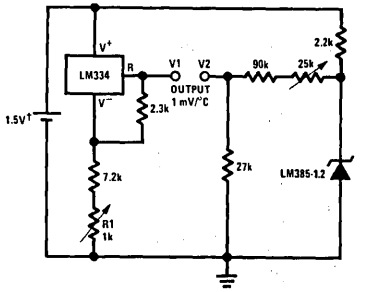
1. Adjust TC ADJ pot until voltage across R1 equals Kelvin temperature multiplied by the thermocouple Seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple Seebeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Coefficient (μV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @ 25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

Typical supply current 50 μA

Typical Applications (Continued)

Centigrade Thermometer



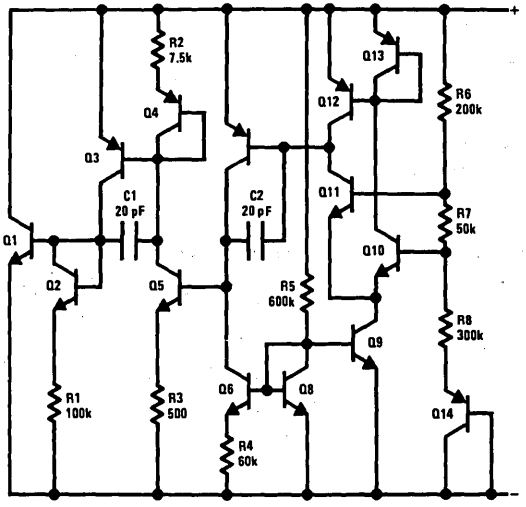
Calibration

1. Adjust R1 so that V1 = temp at 1 mV/°K
2. Adjust V2 to 273.2 mV

†I_Q for 1.3V to 1.6V battery voltage = 50 μA to 150 μA

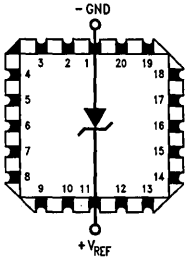
TL/H/5518–1

Schematic Diagram



TL/H/5518–7

Connection Diagrams (Continued)



TL/H/5518–12

Order Number LM185-1.2/883 or LM185-2.5/883
See NS Package Number E20A

National Semiconductor

LM185-2.5/LM285-2.5/LM385-2.5 Micropower Voltage Reference Diode

General Description

The LM185-2.5/LM285-2.5/LM385-2.5 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 20 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM-185-2.5 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-2.5 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185-2.5 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life.

Further, the wide operating current allows it to replace older references with a tighter tolerance part. For applications requiring 1.2V see LM185-1.2.

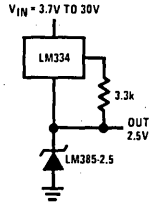
The LM185-2.5 is rated for operation over a −55°C to 125°C temperature range while the LM285-2.5 is rated −40°C to 85°C and the LM385-2.5 0°C to 70°C. The LM185-2.5/LM285-2.5 are available in a hermetic TO-46 package and the LM285-2.5/LM385-2.5 are also available in a low-cost TO-92 molded package, as well as S.O.

Features

- ±20 mV (±0.8%) max. initial tolerance (A grade)
- Operating current of 20 μA to 20 mA
- 0.6Ω dynamic impedance (A grade)
- Low temperature coefficient
- Low voltage reference—2.5V
- 1.2V device and adjustable device also available—LM185-1.2 series and LM185 series, respectively

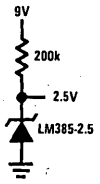
Applications

Wide Input Range Reference



TL/H/5519–12

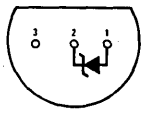
Micropower Reference from 9V Battery



TL/H/5519–2

Connection Diagrams

TO-92
Plastic Package

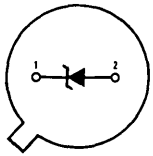


TL/H/5519–8

Bottom View

Order Number LM285Z-2.5, LM285AZ-2.5, LM285AXZ-2.5, LM285AYZ-2.5, LM285BXZ-2.5, LM285BYZ-2.5, LM385Z-2.5, LM385AZ-2.5, LM385AXZ-2.5, LM385AYZ-2.5, LM385BZ-2.5, LM385BXZ-2.5 or LM385BYZ-2.5
See NS Package Number Z03A

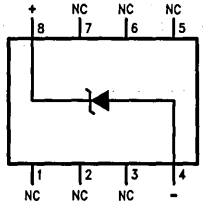
TO-46
Metal Can Package



TL/H/5519–13

Bottom View
Order Number LM185H-2.5, LM185H-2.5/883 LM185AH-2.5, LM185AXH-2.5, LM185AYH-2.5, LM185BXH-2.5, LM185BYH-2.5, LM285H-2.5, LM285AH-2.5, LM285AXH-2.5, LM285AYH-2.5, LM285BXH-2.5 or LM285BYH-2.5
See NS Package Number H02A

SO Package



TL/H/5519–11

Order Number LM285M-2.5, LM285AM-2.5, LM285AXM-2.5, LM285AYM-2.5, LM285BXM-2.5, LM285BYM-2.5, LM385M-2.5, LM385AM-2.5, LM385AXM-2.5, LM385AYM-2.5, LM385BM-2.5, LM385BXM-2.5 or LM385BYM-2.5
See NS Package Number M08A

4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range (Note 3)	
LM185-2.5	−55°C to + 125°C
LM285-2.5	−40°C to + 85°C
LM385-2.5	0°C to 70°C
Storage Temperature	−55°C to + 150°C
Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	Typ	LM185A-2.5 LM185AX-2.5 LM185AY-2.5 LM285A-2.5 LM285AX-2.5 LM285AY-2.5		LM385A-2.5 LM385AX-2.5 LM385AY-2.5		Units (Limits)
			Tested Limit (Notes 5, 8)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Reverse Breakdown Voltage	I_R = 100 μA	2.500	2.480		2.480		V(Min)
			2.520		2.520		V(Max)
		2.500		**2.460**		**2.470**	V(Min)
				2.535		**2.530**	V(Max)
Minimum Operating Current		12	18	**20**	18	**20**	μA (Max)
Reverse Breakdown Voltage Change with Current	$I_{MIN} \le I_R \le$ 1mA		1	**1.5**	1	**1.5**	mV (Max)
	1 mA ≤ $I_R \le$ 20 mA		10	**20**	10	**20**	mV (Max)
Reverse Dynamic Impedance	I_R = 100 μA, f = 20 Hz	0.2		0.6		0.6	Ω
				1.5		**1.5**	
Wideband Noise (rms)	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	120					μV
Long Term Stability	I_R = 100 μA, T = 1000 Hr, T_A = 25°C ±0.1°C	20					ppm
Average Temperature Coefficient (Note 7)	$I_{MIN} \le I_R \le$ 20 mA						
	X Suffix		**30**		**30**		ppm/°C (Max)
	Y Suffix		**50**		**50**		
	All Others			**150**		**150**	

Electrical Characteristics (Continued) (Note 4)

Parameter	Conditions	Typ	LM185-2.5 LM185BX-2.5 LM185BY-2.5 LM285-2.5 LM285BX-2.5 LM285BY-2.5		LM385B-2.5 LM385BX-2.5 LM385BY-2.5		LM385-2.5		Units (Limit)
			Tested Limit (Notes 5, 8)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Reverse Breakdown Voltage	$T_A = 25°C$, $20\ \mu A \le I_R \le 20\ mA$	2.5	2.462 2.538		2.462 2.538		2.425 2.575		V(Min) V(Max)
Minimum Operating Current		13	20	**30**	20	**30**	20	**30**	μA (Max)
Reverse Breakdown Voltage Change with Current	$20\ \mu A \le I_R \le 1\ mA$		1	**1.5**	2.0	**2.5**	2.0	**2.5**	mV (Max)
	$1\ mA \le I_R \le 20\ mA$		10	**20**	20	**25**	20	**25**	mV (Max)
Reverse Dynamic Impedance	$I_R = 100\ \mu A$, $f = 20\ Hz$	1							Ω
Wideband Noise (rms)	$I_R = 100\ \mu A$, $10\ Hz \le f \le 10\ kHz$	120							μV
Long Term Stability	$I_R = 100\ \mu A$, $T = 1000\ Hr$, $T_A = 25°C \pm 0.1°C$	20							ppm
Average Temperature Coefficient (Note 7)	$I_R = 100\ \mu A$ X Suffix Y Suffix All Others		 **30** **50**	 **150**	 **30** **50**	 **150**	 	 **150**	 ppm/°C ppm/°C ppm/°C (Max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Refer to RETS185H-2.5 for military specifications.

Note 3: For elevated temperature operation, $T_{J\ MAX}$ is:

LM185 150°C
LM285 125°C
LM385 100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4" Leads) 170°C/W (0.125" Leads)	440°C/W	165°C/W
θ_{ja} (Junction to Case)	N/A	80°C/W	N/A

Note 4: Parameters identified with **boldface type** apply at temperature extremes. All other numbers apply at $T_A = T_J = 25°C$.

Note 5: Guaranteed and 100% production tested.

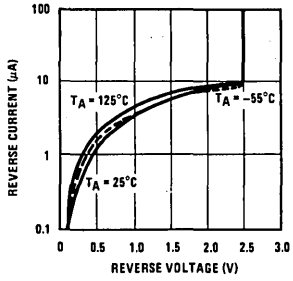
Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate average outgoing quality levels.

Note 7: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures between the operating T_{MAX} and T_{MIN}, divided by $T_{MAX}-T_{MIN}$. The measured temperatures are −55°C, −40°C, 0°C, 25°C, 70°C, 85°C, 125°C.

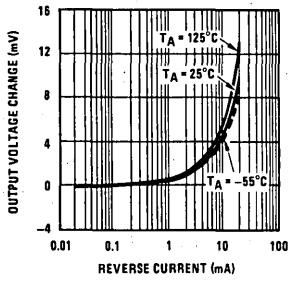
Note 8: A military RETS electrical specification available on request.

Typical Performance Characteristics

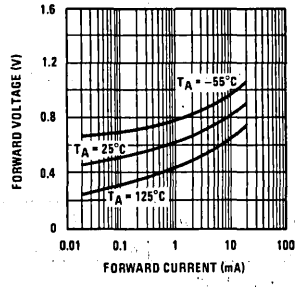
Reverse Characteristics



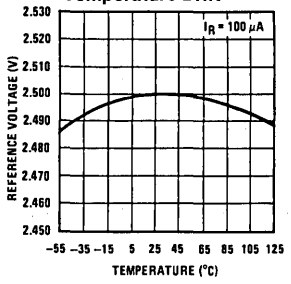
Reverse Characteristics



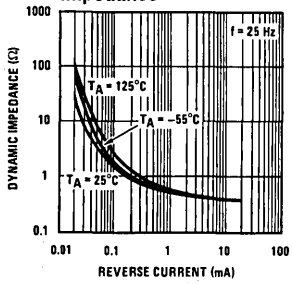
Forward Characteristics



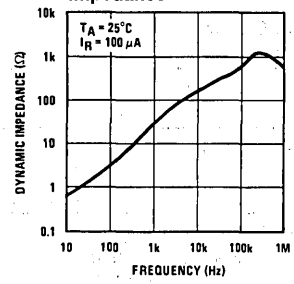
Temperature Drift



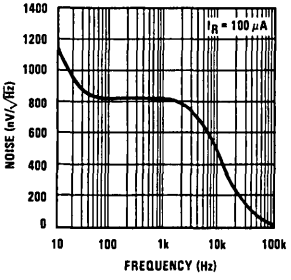
Reverse Dynamic Impedance



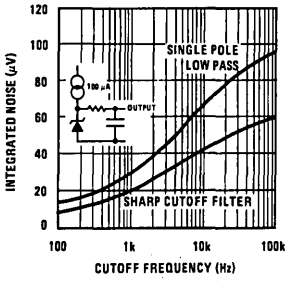
Reverse Dynamic Impedance



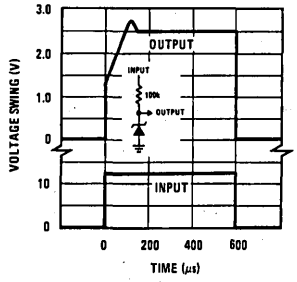
Noise Voltage



Filtered Output Noise



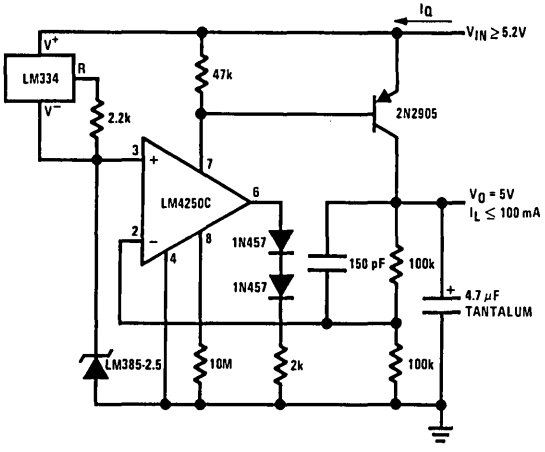
Response Time



TL/H/5519–3

LM385-2.5 Applications

Micropower* 5V Regulator



*$I_Q \cong 40\ \mu A$

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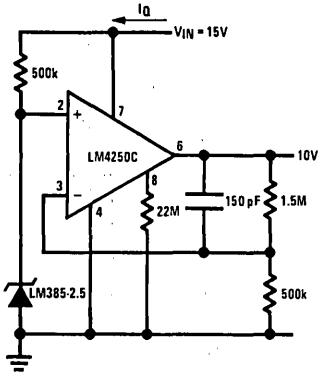
Micropower* 10V Reference



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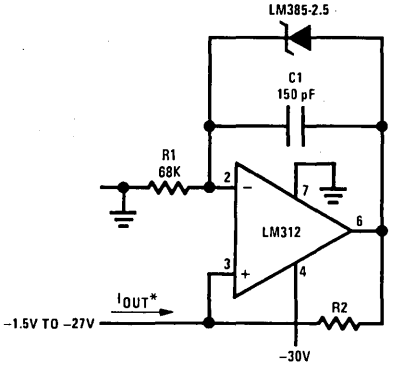
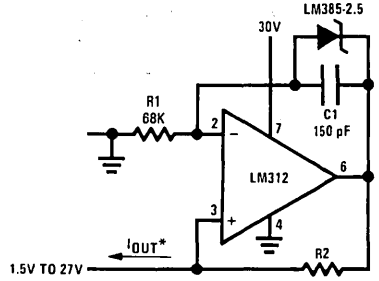
*$I_Q \cong 30\ \mu A$ standby current

Precision 1 μA to 1 mA Current Sources





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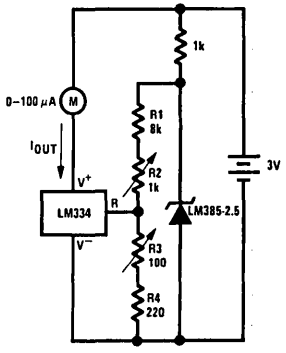
$$*I_{OUT} = \frac{2.5V}{R2}$$

METER THERMOMETERS

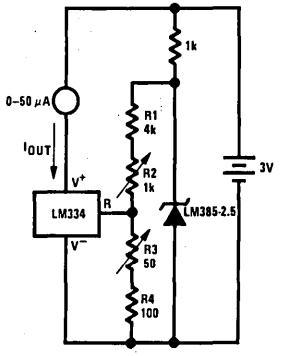
0°C–100°C Thermometer



Calibration

1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1 μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

0°F–50°F Thermometer



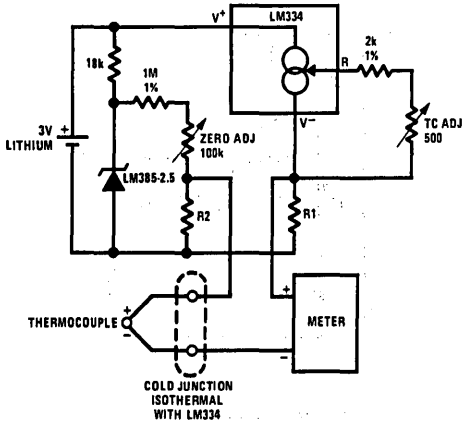
TL/H/5519-5

Calibration

1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

LM385-2.5 Applications (Continued)

Micropower Thermocouple Cold Junction Compensator



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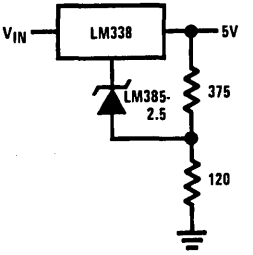
Adjustment Procedure

1. Adjust TC ADJ pot until voltage across R1 equals Kelvin temperature multiplied by the thermocouple Seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple Seebeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Co-efficient (μV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

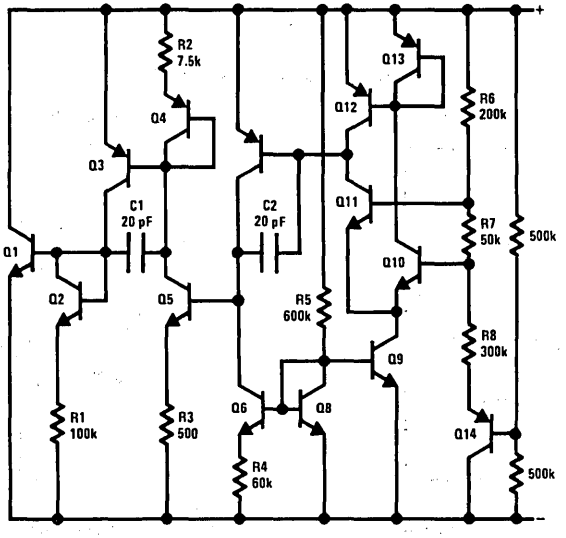
Typical supply current 50 μA

Improving Regulation of Adjustable Regulators



TL/H/5519–7

Schematic Diagram



TL/H/5519–1

National Semiconductor

LM1575/LM2575-ADJ, LM2575HV-ADJ Simple Switcher™ 1 Amp Step-Down Voltage Regulator

General Description

The LM1575-ADJ series are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator. These devices feature an output voltage which is adjustable from 1.23V to 37V (57V for the HV version) and is capable of driving a 1A load with excellent line and load regulation.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation and a fixed-frequency oscillator.

The LM1575-ADJ series offers a high efficiency replacement for popular three-terminal adjustable linear regulators. It substantially reduces the size of the heat sink, and in many cases no heat sink is required.

A standard series of inductors are available from several different manufacturers optimized for use with the LM1575-ADJ series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±2% tolerance on feedback voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring less than 200 μA standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

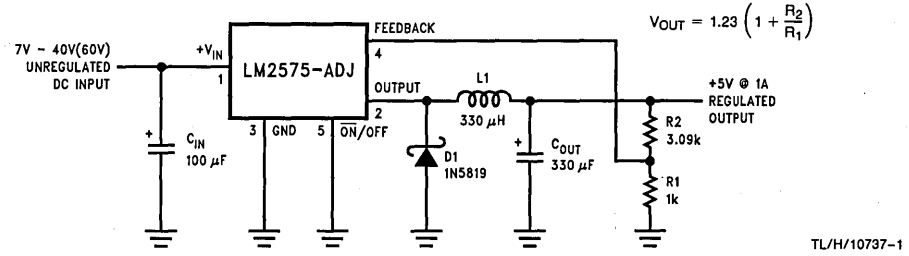
Features

- Adjustable output, reference voltage ±2% max over line and load conditions
- Guaranteed 1A output current
- Wide input voltage range, 4V to 40V (60V for HV)
- Wide output voltage range, 1.23V to 37V (57V for HV)
- Requires only 6 external components
- 52 kHz fixed frequency internal oscillator
- Low power standby mode, I_Q typically < 200 μA
- Efficiency typically over 80%
- Uses readily available standard inductors
- Thermal shutdown and current limit protection
- 100% electrical thermal limit burn-in

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter (Inverting Buck-Boost)
- Isolated Flyback Converter using minimum number of external components
- Negative Boost Converter

Typical Application and Ordering Information



Note: Pin numbers are for TO-220 Package.

Package Type	NSC Package Drawing	Order Number For: Standard Voltage Rating (40V)	Order Number For: High Voltage Rating (60V)	Temperature Range
5-Lead TO-220 Straight Leads	T05A	LM2575T-ADJ	LM2575HVT-ADJ	−40°C ≤ T_J ≤ +125°C
5-Lead TO-220 Bent, Staggered Leads	T05D	LM2575T-ADJ Flow LB03	LM2575HVT-ADJ Flow LB03	
16-Pin Molded DIP	N16A	LM2575N-ADJ	LM2575HVN-ADJ	
24-Pin Surface Mount	M24B	LM2575M-ADJ	LM2575HVM-ADJ	
4-Pin TO-3	K04A	LM1575K-ADJ/883		−55°C ≤ T_J ≤ +150°C

Refer to Connection Diagrams at end of datasheet

Patent Pending

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Maximum Supply Voltage	
LM1575/LM2575	45V
LM2575HV	63V
$\overline{ON}$/OFF Pin Input Voltage	$-0.3V \le V \le +40V$
Output Voltage to Ground (Steady State)	−1V
Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Minimum ESD Rating	
(C = 100 pF, R = 1.5 kΩ)	2 kV
FB Pin (Pin 4)	1 kV
Lead Temperature	
(Soldering, 10 sec.)	260°C

Operating Ratings

Maximum Junction Temperature	150°C
Temperature Range	
LM1575	$-55°C \le T_J \le +150°C$
LM2575/LM2575HV	$-40°C \le T_J \le +125°C$
Supply Voltage	
LM1575/LM2575	40V
LM2575HV	60V

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V, and I_{LOAD} = 200 mA.

Symbol	Parameter	Conditions	Typ	LM1575-ADJ Limit (Note 2)	LM2575-ADJ LM2575HV-ADJ Limit (Note 3)	Units (Limits)
SYSTEM PARAMETERS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Feedback Voltage	V_{IN} = 12V, I_{LOAD} = 0.2A V_{OUT} = 5V, Circuit of *Figure 1*	1.230	 1.217 1.243	 1.217 1.243	V V(min) V(max)
V_{OUT}	Feedback Voltage LM1575/LM2575	0.2A ≤ I_{LOAD} ≤ 1A, 8V ≤ V_{IN} ≤ 40V V_{OUT} = 5V, Circuit of *Figure 1*	1.230	 1.205/**1.193** 1.255/**1.267**	 1.193/**1.180** 1.267/**1.280**	V V(min) V(max)
V_{OUT}	Feedback Voltage LM2575HV	0.2A ≤ I_{LOAD} ≤ 1A, 8V ≤ V_{IN} ≤ 60V V_{OUT} = 5V, Circuit of *Figure 1*	1.230		 1.193/**1.180** 1.273/**1.286**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 1A, V_{OUT} = 5V	82			%
DEVICE PARAMETERS						
I_b	Feedback Bias Current	V_{OUT} = 5V	50	100/**500**	100/**500**	nA
f_O	Oscillator Frequency	(Note 11)	52	 47/**43** 58/**62**	 47/**42** 58/**63**	kHz kHz(min) kHz(max)
V_{SAT}	Saturation Voltage	I_{OUT} = 1A (Note 5)	0.9	 1.2/**1.4**	 1.2/**1.4**	V V(max)
DC	Max Duty Cycle (ON)	(Note 6)	98	 93	 93	% %(min)
I_{CL}	Current Limit	Peak Current, $t_{ON} \le 3\ \mu s$ (Note 5)	2.2	 1.7/**1.3** 3.0/**3.2**	 1.7/**1.3** 3.0/**3.2**	A A(min) A(max)
I_L	Output Leakage Current	V_{IN} = 40V (Note 7) Output = 0V V_{IN} = 60V for HV Output = −1V (Note 7) Output = −1V	 7.5	2 30	2 30	mA(max) mA mA(max)
I_Q	Quiescent Current	(Note 7)	5	 10/**12**	 10	mA mA(max)
I_{STBY}	Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF)	50	 200/**500**	 200	μA μA(max)
θ_{JA} θ_{JC} θ_{JA} θ_{JA} θ_{JC} θ_{JA} θ_{JA}	Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T Package, Junction to Ambient (Note 8) T Package, Junction to Ambient (Note 9) T Package, Junction to Case N Package, Junction to Ambient (Note 10) M Package, Junction to Ambient (Note 10)	35 1.5 65 45 2 85 100			 °C/W

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, V_{IN} = 12V, and I_{LOAD} = 200 mA. (Continued)

Symbol	Parameter	Conditions	Typ	LM1575-ADJ Limit (Note 2)	LM2575-ADJ LM2575HV-ADJ Limit (Note 3)	Units (Limits)
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 1*						
V_{IH}	$\overline{ON}$/OFF Pin Logic Input Level	V_{OUT} = 0V	1.4	2.2/**2.4**	2.2/**2.4**	V(min)
V_{IL}		V_{OUT} = 5V	1.2	1.0/**0.8**	1.0/**0.8**	V(max)
I_{IH}	$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF)	12	30	30	μA μA(max)
I_{IL}		$\overline{ON}$/OFF Pin = 0V (ON)	0	10	10	μA μA(max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face).** All limits are used to calculate Average Outgoing Quality Level, and all are 100% production tested.

Note 3: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face).** All room temperature limits are 100% production tested. All limits at **temperature extremes** are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Note 4: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM1575/LM2575 is used as shown in the *Figure 1* test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.

Note 5: Output (pin 2) sourcing current. No diode, inductor or capacitor connected to output.

Note 6: Feedback (pin 4) removed from output and connected to 0V.

Note 7: Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.

Note 8: Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with ½" leads in a socket, or on a PC board with minimum copper area.

Note 9: Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with ¼" leads soldered to a PC board containing approximately 4 square inches of copper area surrounding the leads.

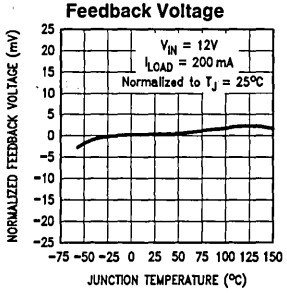
Note 10: Junction to ambient thermal resistance with approximately 1 square inch of pc board copper surrounding the leads. Additional copper area will lower thermal resistance further. See thermal model in Switchers made Simple software.

Note 11: The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which pulls the feedback voltage lower than 0.7V. This self-protection feature lowers the average power dissipation of the IC by reducing the minimum duty cycle from 5% to approximately 2%.

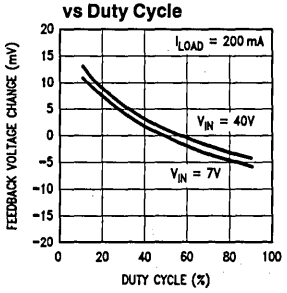
Note 12: Refer to RETS LM1575K-ADJ for current revision of military RETS/SMD.

Typical Performance Characteristics (Circuit of *Figure 1*)

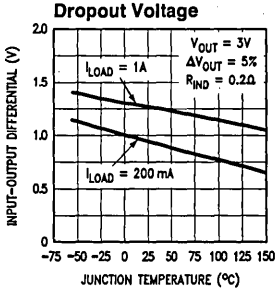
Normalized Feedback Voltage



Feedback Voltage vs Duty Cycle



Dropout Voltage



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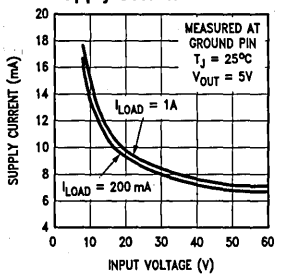
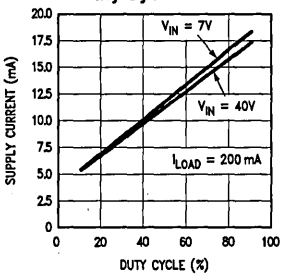
Typical Performance Characteristics (Circuit of *Figure 1*) (Continued)

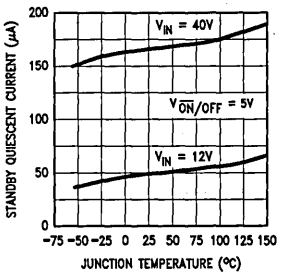
Supply Current



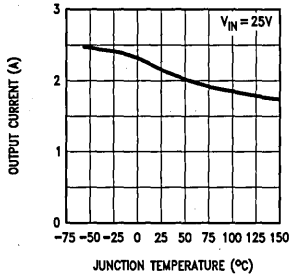
Supply Current vs Duty Cycle



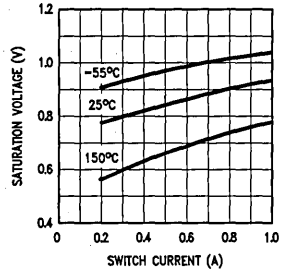
Standby Quiescent Current



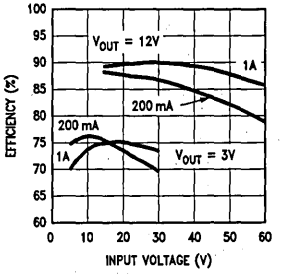
Current Limit



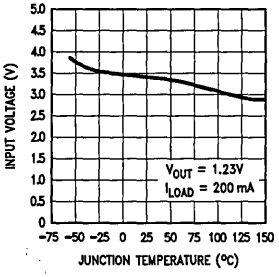
Switch Saturation Voltage



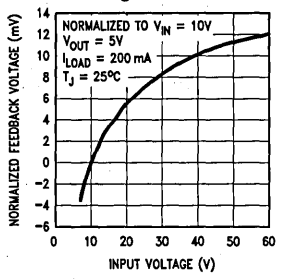
Efficiency



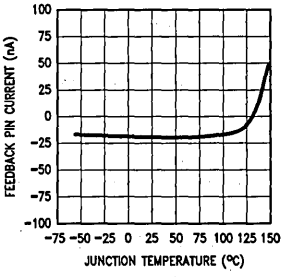
Minimum Operating Voltage



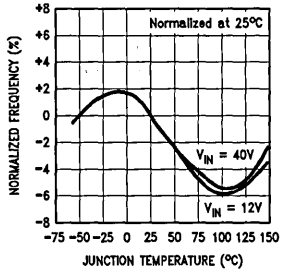
Line Regulation



Feedback Pin Current



Oscillator Frequency



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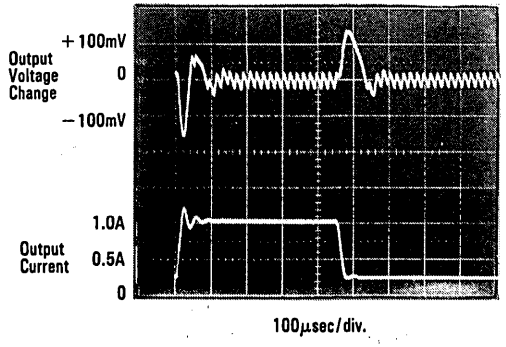
Typical Performance Characteristics (Circuit of *Figure 1*) (Continued)

Load Transient Response



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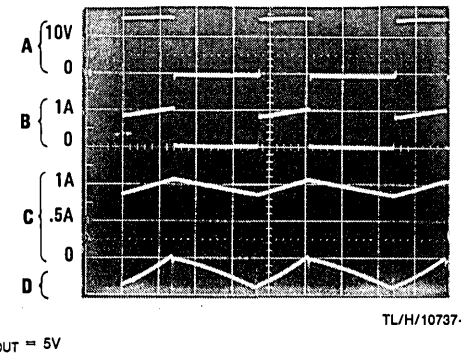
V_{OUT} = 5V

Switching Waveforms



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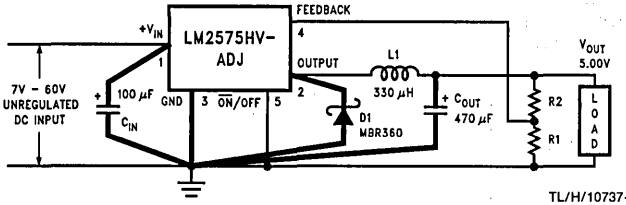
V_{OUT} = 5V

A: Output pin voltage, 10V/div
B: Output pin current, 1A/div
C: Inductor current, 0.5A/div
D: Output ripple voltage, 20 mV/div, AC-coupled
Horizontal Time Base: 5 μs/div

Test Circuit and Layout Guidelines



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C_{IN} — 100 μF, 75V, Aluminum Electrolytic
C_{OUT} — 470 μF, 15V, Aluminum Electrolytic
D1 — Schottky, MBR360
L1 — 330 μH, 415-0926 (AIE)
R1 — 1k, 0.01%
R2 — 3.065k, 0.01%
5-pin TO-220 socket—2936 (Loranger Mfg. Co.)
4-pin TO-3 socket—8112-AG7 (Augat Inc.)

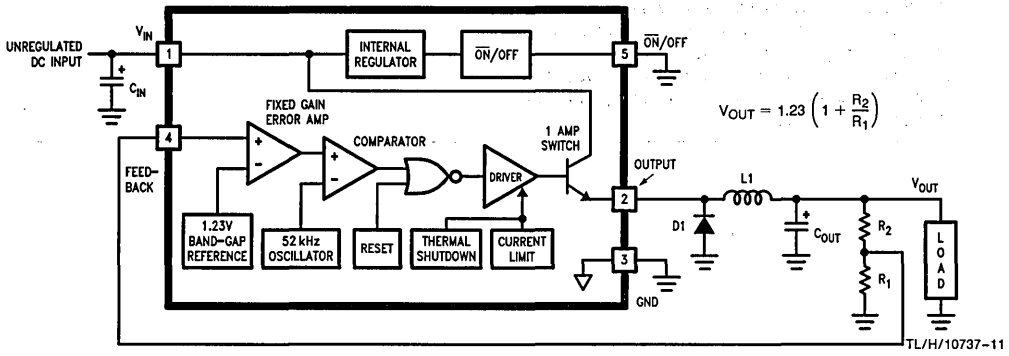
*HV Version

Note: Pin numbers are for the TO-220 package.

FIGURE 1

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal stray inductance and ground loops, the length of the leads indicated by heavy lines should be **kept** as **short** as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results.

Block Diagram and Typical Application



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Note: Pin numbers are for the TO-220 package.

FIGURE 2

LM1575-ADJ Series Buck Regulator Design Procedure

Procedure	Example
Given: V_{OUT} = Regulated Output Voltage V_{IN}(max) = Maximum input voltage I_{LOAD}(max) = Maximum load current F = Switching frequency *(fixed at 52 kHz)*	**Given:** V_{OUT} = 10V V_{IN}(max) = 25V I_{LOAD}(max) = 1A F = 52 kHz
1. Programming Output Voltage *(selecting R_1 and R_2)* Use the following formula to select the appropriate resistor values. $V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right)$ where V_{REF} = 1.23V R1 can be between 1k and 10k. *(for best temperature coefficient and stability with time, use 1% metal film resistors)* $R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$	**1. Programming Output Voltage** *(selecting R_1 and R_2)* $V_{OUT} = 1.23\left(1 + \frac{R_2}{R_1}\right)$ select R_1 = 1k $R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 1k\left(\frac{10V}{1.23V} - 1\right)$ R_2 = 1k (8.13 −1) = 7.13k, use closest 1% value 7.15k
2. Inductor Selection (L1) A. Calculate E • T (V • μs), from the following formula; $E \bullet T = (V_{IN} - V_{OUT})\frac{V_{OUT}}{V_{IN}} \bullet \frac{1000}{F(in\ kHz)}$ (V • μs) B. Use the E • T value from the previous formula and match it with the E • T number on the vertical axis of the **inductor value selection guide** shown in *Figure 4.* C. On the horizontal axis, select the maximum load current. D. Identify the region intersected by the E • T value and the maximum load current value, and note the inductor code for that region. E. Match Inductor code to the inductor value as shown in *Figure 5. (and manufacturer's part number)*	**2. Inductor Selection (L1)** A. Calculate E • T (V • μs) $E \bullet T = (25 - 10) \bullet \frac{10}{25} \bullet \frac{1000}{52} = 115\ V \bullet \mu s$ B. E • T = 115 V • μs C. I_{LOAD}(max) = 1A D. Inductor code = H470 E. Inductor value = 470 μH *Choose from **AIE** part #430-0634, **Pulse Engineering** part #PE-53118, or **Renco** part #RL1961.*
3. Output Capacitor Selection (C_{OUT}) The value of the output capacitor together with the inductor defines the dominant pole-pair of the switching regulator loop. For stable operation, the capacitor must satisfy the following requirement: A. $C_{OUT} \geq 7{,}785\frac{V_{IN}(max)}{V_{OUT} \bullet L(\mu H)}$ (μF) The above formula yields capacitor values between 10 μF and 2200 μF that will satisfy the loop requirements for stable operation. But to achieve an acceptable output ripple voltage (approximately 1% of the output voltage) and transient response, the output capacitor may need to be several times larger than the above formula yields.	**3. Output Capacitor Selection (C_{OUT})** A. $C_{OUT} > 7{,}785\frac{25}{10 \bullet 150} = 130\ \mu F$ However, for acceptable output ripple voltage select $C_{OUT} \geq 220\ \mu F$ C_{OUT} = 220 μF electrolytic Capacitor

LM1575-ADJ Series Buck Regulator Design Procedure (Continued)

Procedure	Example

The amount of output ripple voltage is primarily a function of the ESR (Equivalent Series Resistance) of the output capacitor. The value and the type of capacitor used will determine the amount of ESR it contains. Selecting a capacitor with a low ESR will result in a low output ripple voltage. In general, the lower capacitor values have the higher ESR ratings.

The lower capacitor values (220 μF–680 μF) will allow typically 50 mV to 150 mV of output ripple voltage, while larger-value capacitors will reduce the ripple to approximately 35 mV to 50 mV.

$$V_{RIPPLE\ p\text{-}p} \geq 0.3 \times I_{LOAD}(max) \times ESR$$

To further reduce the output ripple voltage, several standard electrolytic capacitors may be paralleled, or a higher-grade capacitor may be used. Such capacitors are often called "high-frequency", "low-inductance", or "low-ESR". These will reduce the output ripple to 10 mV to 20 mV. However, reducing the ESR below 0.05Ω can cause instability. For this reason, the use of a tantalum capacitor as the sole capacitor is not recommended. Tantalum capacitors (because of their good low temperature characteristics) can be used in parallel with aluminum electrolytics, with the tantalum making up 10% or 20% of the total capacitance.

The capacitor's ripple current rating at 52 kHz should be at least 50% higher than the ripple component of the inductor current.

$$I_{RIPPLE}(max) \geq 1.5 \times 0.3 \times I_{LOAD}(max)$$

B. The capacitor's voltage rating should be at least 1.25 times greater than the output voltage. For a 10V output, a rating of at least 15V is appropriate, and a 20V rating is recommended.

4. Catch Diode Selection (D1)

The catch-diode current rating must be at least 1.2 times greater than the maximum load current. Also, if the power supply design must withstand continuous shorted output conditions, the diode current rating should be greater than 1A. The most stressful condition for this diode is an overload or short circuit condition.

A. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.

B. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best efficiency, especially in low output voltage switching regulators (less than 5V). Fast-Recovery, High-Efficiency, or Ultra-Fast Recovery diodes are also suitable, but some types with an abrupt turn-off characteristic may cause instability and EMI problems. A fast-recovery diode with soft recovery characteristics is a better choice. Standard 60 Hz diodes (e.g., 1N4001, or IN5400, etc.) are also **not suitable**. See *Figure 3* for Schottky and "soft" fast-recovery diode selection guide.

V_{IN} (max)	Schottky		Fast Recovery	
	1A	3A	1A	3A
20V	1N5817 MBR120P SR102	1N5820 MBR320P SR302	The following diodes are all rated to 100V 11DF1 MUR110 HER102	The following diodes are all rated to 100V 31DF1 MUR310 HER302
30V	1N5818 MBR130P 11DQ03 SR103	1N5821 MBR330 31DQ03 SR303		
40V	1N5819 MBR140P 11DQ04 SR104	1N5822 MBR340 31DQ04 SR304		
50V	MBR150 11DQ05 SR105	MBR350 31DQ05 SR305		
60V	MBR1601 11DQ06 SR106	MBR3603 31DQ06 SR306		

FIGURE 3. Diode Selection Guide

To further simplify the buck regulator design procedure, National Semiconductor is making available computer design software to be used with the Simple Switcher™ line of switching regulators. ***Switchers Made Simple*** *is available on a (5¼") diskette for IBM compatible computers from a National Semiconductor sales office in your area.*

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LM1575-ADJ Series Buck Regulator Design Procedure (Continued)

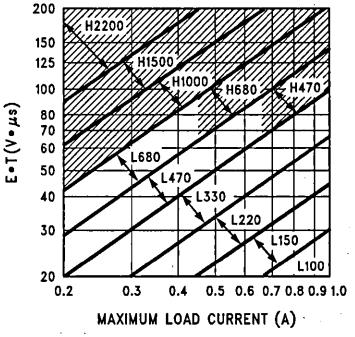

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FIGURE 4. Inductor Value Selection Guide (for Continuous Mode Operation)

Inductor Code	Inductor Value	AIE[1]	Pulse Eng.[2]	Renco[3]
L47	47 μH	415-0932	PE-53112	RL2442
L68	68 μH	415-0931	PE-92114	RL2443
L100	100 μH	415-0930	PE-92108	RL2444
L150	150 μH	415-0953	PE-53113	RL1954
L220	220 μH	415-0922	PE-52626	RL1953
L330	330 μH	415-0926	PE-52627	RL1952
L470	470 μH	415-0927	PE-53114	RL1951
L680	680 μH	415-0928	PE-52629	RL1950
H150	150 μH	415-0936	PE-53115	RL2445
H220	220 μH	430-0636	PE-53116	RL2446
H330	330 μH	430-0635	PE-53117	RL2447
H470	470 μH	430-0634	PE-53118	RL1961
H680	680 μH	415-0935	PE-53119	RL1960
H1000	1000 μH	415-0934	PE-53120	RL1959
H1500	1500 μH	415-0933	PE-53121	RL1958
H2200	2200 μH	415-0945	PE-53122	RL2448

FIGURE 5. Inductor Selection by Manufacturer's Part Number

Note 1: AIE Magnetics, div. Vernatron Corp. Passive Components Group, (813) 347-2181
2801 72nd Street North, St. Petersburg, FL 33710

Note 2: Pulse Engineering, (619) 268-2400
P.O. Box 12235, San Diego, CA 92112

Note 3: Renco Electronics Inc., (516) 586-5566
60 Jeffryn Blvd. East, Deer Park, NY 11729

Typical Applications

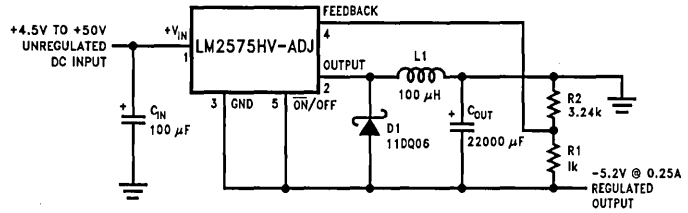

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FIGURE 6. Inverting Buck-Boost

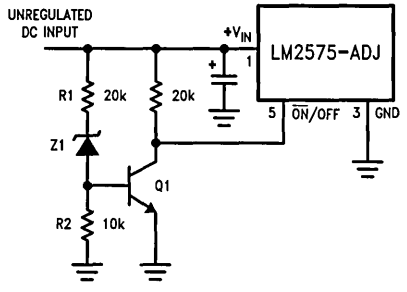

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FIGURE 7. Undervoltage Lockout

Figure 6 shows an LM2575-ADJ in a very simple buck-boost configuration to generate a negative 5.2V output, from a positive input voltage. This circuit bootstraps the regulator's ground pin to the negative output voltage, then by grounding the feedback pin, the regulator senses the inverted output voltage and regulates it to −5.2V.

The maximum available output current in this configuration is approximately 0.25A. Higher currents (up to 0.4A) are possible with input voltages greater than 8V, or by increasing the value of the output capacitor.

The pulsed switch currents in this buck-boost configuration are higher than in the standard buck-mode design. To avoid exceeding the maximum switch current rating, the available output current is less than the standard buck configuration. Also, the Start-up input current is higher than the standard buck-mode regulator, and this could overload the input power source. Using a delayed turn-on or an undervoltage lockout circuit would allow the input voltage to rise to a high enough level before the switcher would be allowed to turn on. The circuit in *Figure 7* can be modified for the buck-boost under-voltage lockout by wiring the emitter of Q1 and the low side of R1, to the ground pin of the LM2575, which is the negative output of the inverting buck-boost circuit.

The buck regulator design procedure section can not be used to select the inductor, because of the structural differences between the buck and the buck-boost regulator topologies. The recommended range of inductor values for the buck-boost designs is between 47 µH and 200 µH. The peak inductor current, which is the same as the peak switch current, can be calculated from the following formula:

$$I_p \approx \frac{I_{LOAD}\,(V_{IN} + V_O)}{V_{IN}} + \frac{V_{IN}\,V_O}{V_{IN} + V_O} \times \frac{1}{2L_1\,f_{OSC}}$$

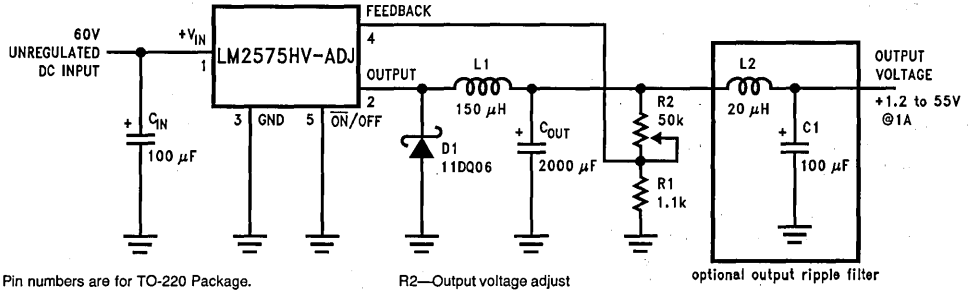
Where f_{OSC} = 52 kHz. Under normal continuous inductor current operating conditions, the minimum V_{IN} represents the worst case. Select an inductor that is rated for the peak current anticipated.

The ***Switchers Made Simple*** design software can be used to determine the feasibility of regulator designs using different topologies, different input-output parameters, different components, etc.

In some applications it is desirable to keep the regulator off until the input voltage reaches a certain threshold. An undervoltage lockout circuit which accomplishes this task is shown in *Figure 7*. This circuit keeps the regulator off until the input voltage reaches a predetermined level.

$$V_{TH} \approx V_{Z1} + V_{BE}\,(Q1)$$

A 1A power supply that features an adjustable output voltage is shown in *Figure 8*. An additional L-C filter that reduces the output ripple by a factor of 10 or more, to about 5 mV, is included in this circuit.



Note: Pin numbers are for TO-220 Package.

R2—Output voltage adjust

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FIGURE 8. 1.2V to 55V Adjustable 1A Power Supply with Low Output Ripple

Application Hints

INPUT CAPACITOR (C_{IN})

To maintain stability, the regulator input pin must be bypassed with at least a 47 µF low-ESR electrolytic capacitor. Capacitors with high voltage ratings, or capacitors which are physically larger, generally have a lower ESR. The capacitor's leads must be kept short, and located as close as possible to the regulator.

If the operating temperature range includes temperatures below −25°C, the input capacitor value may need to be larger. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures and age. Adding a ceramic or solid tantalum capacitor near the input pin will increase the regulator stability at cold temperatures. For maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be greater than $1.2 \times (t_{ON}/T) \times I_{LOAD}$.

INDUCTOR SELECTION

The inductor value selection guide of *Figure 4* was designed for buck regulator designs of the continuous inductor current type. When using inductor values shown in the inductor selection guide, the peak-to-peak inductor ripple current will be approximately 20% to 30% of the maximum DC current. With relatively heavy load currents, the circuit operates in the continuous mode (inductor current always flowing), but under light load conditions, the circuit will be forced to the discontinuous mode (inductor current falls to zero for a period of time). This discontinuous mode of operation is perfectly acceptable. For light loads (less than approximately 200 mA) it may be desirable to operate the regulator in the discontinuous mode, primarily because of the lower inductor values required for the discontinuous mode.

The LM2575 can be used for both continuous and discontinuous modes of operation. The selection guide chooses inductor values suitable for continuous mode operation, but if the inductor value chosen is prohibitively high, the designer should investigate the possibility of discontinuous operation. The computer design software ***Switchers Made Simple*** will provide all component values for discontinuous (as well as continuous) mode of operation.

Inductors are available in different styles such as pot core, toroid, E-frame, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin core type, consists of wire wrapped on a ferrite rod core. This type of construction makes for an inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more electromagnetic interference (EMI). This EMI can cause problems in sensitive circuits, or can give incorrect scope readings becauseof induced voltages in the scope probe.

The inductors listed in the selection chart include ferrite pot core construction for AIE, powdered iron toroid for Pulse Engineering, and ferrite bobbin core for Renco.

An inductor should not be operated beyond its maximum rated current because it may saturate. When an inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This will cause the switch current to rise very rapidly. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

The inductor manufacturers' data sheets include current and energy limits to avoid inductor saturation.

OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.

The output ripple voltage is due mainly to the inductor sawtooth ripple current multiplied by the ESR of the output capacitor (see Section 3A of design procedure).

The voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. To minimize these voltage spikes, special low inductance capacitors must be used, and their lead lengths must be kept short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.

An additional small LC filter can be added to the output to further reduce the amount of output ripple and transients, as in *Figure 8*.

FEEDBACK CONNECTION

The LM2575-ADJ feedback circuitry is designed so that, when the output voltage is connected directly to the Feedback pin, the output voltage is 1.230V.

$\overline{ON}$/OFF INPUT

For normal operation, the $\overline{ON}$/OFF pin should be grounded or driven with a low-level TTL voltage (typically below 1.6V). To put the regulator into standby mode, drive this pin with a high-level TTL or CMOS signal.

GROUNDING

To maintain output voltage stability, the power ground connections must be low-impedance (see *Figure 1*). For the TO-3 style package, the case is ground. For the 5-lead TO-220 style package, both the tab and pin 3 are ground and either connection may be used, as they are both part of the same copper lead frame.

With the N or M packages, all the pins labeled ground, power ground, or signal ground should be soldered directly to wide printed circuit board copper traces. This assures both low inductance connections and good thermal properties.

HEAT SINK/THERMAL CONSIDERATIONS

In many cases, no heat sink is required to keep the LM2575 junction temperature within the allowed operating range. For each application, to determine whether or not a heat sink will be required, the following must be identified:

1. Maximum ambient temperature (in the application).
2. Maximum regulator power dissipation (in application).
3. Maximum allowed junction temperature (150°C for LM1575 or 125°C for the LM2575). For a safe, conservative design, a temperature approximately 15°C cooler than the maximum temperatures should be selected.
4. LM2575 package thermal resistances θ_{JA} and θ_{JC}.

Total power dissipated by the LM2575 can be estimated as follows:

$$P_D = (V_{IN})(I_Q) + (V_O/V_{IN})(I_{LOAD})(V_{SAT})$$

where I_Q (quiescent current) and V_{SAT} can be found in the Characteristic Curves shown previously, V_{IN} is the applied minimum input voltage, V_O is the regulated output voltage, and I_{LOAD} is the load current. The dynamic losses during turn-on and turn-off are negligible if a Schottky type catch diode is used.

Application Hints (Continued)

When no heat sink is used, the junction temperature rise can be determined by the following:

$$\Delta T_J = (P_D)(\theta_{JA})$$

To arrive at the actual operating junction temperature, add the junction temperature rise to the maximum ambient temperature.

$$T_J = \Delta T_J + T_A$$

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, then a heat sink is required.

When using a heat sink, the junction temperature rise can be determined by the following:

$$\Delta T_J = (P_D)(\theta_{JC} + \theta_{interface} + \theta_{Heat\ sink})$$

The operating junction temperature will be:

$$T_J = T_A + \Delta T_J$$

As above, if the actual operating junction temperature is greater than the selected safe operating junction temperature, then a larger heat sink is required (one that has a lower thermal resistance).

When using the LM2575 in the plastic DIP (N) or surface mount (M) packages, several items about the thermal properties of the packages should be understood. The majority of the heat is conducted out of the package through the leads, with a minor portion through the plastic parts of the package. Since the lead frame is solid copper, heat from the die is readily conducted through the leads to the printed circuit board copper, which is acting as a heat sink.

For best thermal performance, the ground pins and all the unconnected pins should be soldered to generous amounts of printed circuit board copper, such as a ground plane. Large areas of copper provide the best transfer of heat to the surrounding air. Copper on both sides of the board is also helpful in getting the heat away from the package, even if there is no direct copper contact between the two sides. Thermal resistance numbers as low as 40 °C/W for the SO package, and 30 °C/W for the N package can be realized with a carefully engineered pc board.

Included on the ***Switcher Made Simple*** design software is a more precise (non-linear) thermal model that can be used to determine junction temperature with different input-output parameters or different component values. It can also calculate the heat sink thermal resistance required to maintain the regulators junction temperature below the maximum operating temperature.

Definition of Terms

BUCK REGULATOR

A switching regulator topology in which a higher voltage is converted to a lower voltage. Also known as a step-down switching regulator.

BUCK-BOOST REGULATOR

A switching regular topology in which a positive voltage is converted to a negative voltage without a transformer.

DUTY CYCLE (D)

Ratio of the output switch's on-time to the oscillator period.

for buck regulator $$D = \frac{t_{ON}}{T} = \frac{V_{OUT}}{V_{IN}}$$

for buck-boost regulator $$D = \frac{t_{ON}}{T} = \frac{|V_O|}{|V_O| + V_{IN}}$$

where T is the oscillator period, typically 1/52 kHz or 19 μs.

CATCH DIODE OR CURRENT STEERING DIODE

The diode which provides a return path for the load current when the LM2575 switch is OFF.

EFFICIENCY (η)

The proportion of input power actually delivered to the load.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

EQUIVALENT SERIES INDUCTANCE (ESL)

The pure inductance component of a capacitor (see *Figure 9*). The amount of inductance is determined to a large extent on the capacitor's construction. In a buck regulator, this unwanted inductance causes voltage spikes to appear on the output.

EQUIVALENT SERIES RESISTANCE (ESR)

The purely resistive component of a real capacitor's impedance (see *Figure 9*). It causes power loss resulting in capacitor heating, which directly affects the capacitor's operating lifetime. When used as a switching regulator output filter, higher ESR values result in higher output ripple voltages.

Most standard aluminum electrolytic capacitors in the 470 μF–2000 μF range have 0.05Ω to 0.3Ω ESR. Higher-grade capacitors ("low-ESR", "high-frequency", or "low-inductance") in the 220 μF–1000 μF range generally have ESR of less than 0.15Ω.

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FIGURE 9. Simple Model of a Real Capacitor

OUTPUT RIPPLE VOLTAGE

The AC component of the switching regulator's output voltage. It is usually dominated by the output capacitor's ESR multiplied by the inductor's ripple current. The peak-to-peak value of this sawtooth ripple current will be typically 30% of the maximum load current (when the Design Procedure in the datasheet is followed).

CAPACITOR RIPPLE CURRENT

RMS value of the maximum allowable alternating current at which a capacitor can be operated continuously at a specified temperature.

STANDBY QUIESCENT CURRENT (I_{STBY})

Supply current required by the LM2575 when in the standby mode ($\overline{ON}$/OFF pin is driven to TTL-high voltage), thus turning the output switch OFF.

INDUCTOR RIPPLE CURRENT

The peak-to-peak value of the inductor current waveform, typically a sawtooth waveform when the regulator is operating continuous (vs. discontinuous)

CONTINUOUS/DISCONTINUOUS MODE OF OPERATION

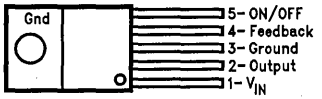
Relates to the inductor current. In the continuous mode, the inductor current is always flowing and never drops to zero, vs. the discontinuous mode, where the inductor current drops to zero for a period of time.

INDUCTOR SATURATION

The condition which exists when an inductor cannot hold any more magnetic flux. When an inductor saturates, the inductor appears less inductive and the resistive component dominates. Inductor current is then limited only by the DC resistance of the wire and the available source current.

Connection Diagrams

Straight Leads
5-Lead TO-220 (T)

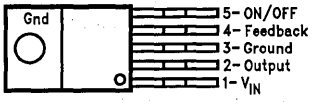


TL/H/10737-17

Top View

Order Number LM2575T-ADJ
or LM2575HVT-ADJ
See NS Package Number T05A

Bent, Staggered Leads
5-Lead TO-220 (T)

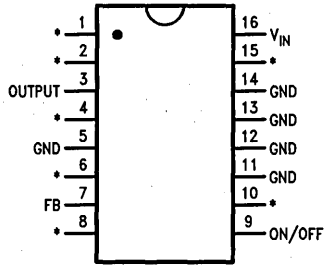


TL/H/10737-18

Top View

Order Number LM2575T-ADJ Flow LB03
or LM2575HVT-ADJ Flow LB03
See NS Package Number T05D

16-Lead DIP (N)



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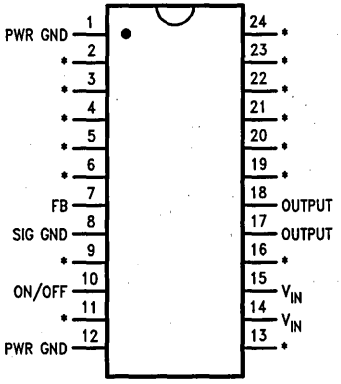
*No Internal Connection

Top View

Order Number LM2575N-ADJ
or LM2575HVN-ADJ
See NS Package Number N16A

24-Lead Surface Mount (M)



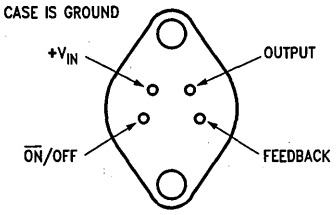
TL/H/10737-3

*No Internal Connection

Top View

Order Number LM2575M-ADJ
or LM2575HVM-ADJ
See NS Package Number M24B

4-Lead TO-3 (K)



TL/H/10737-9

Bottom View

Order Number LM1575K-ADJ/883
See NS Package Number K04A

National Semiconductor

LM2576-ADJ/LM2576HV-ADJ
Simple Switcher™ 3 Amp Step-Down Voltage Regulator

General Description

The LM2576-ADJ series are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator. These devices feature an output voltage which is adjustable from 1.23V to 37V and is capable of driving a 3A load with excellent line and load regulation.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation and a fixed-frequency oscillator.

The LM2576-ADJ series offers a high efficiency replacement for popular three-terminal adjustable linear regulators. It substantially reduces the size of the heat sink, and in some cases no heat sink is required.

A standard series of inductors are available from several different manufacturers optimized for use with the LM2576-ADJ series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±3% tolerance on feedback voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring less than 200 μA standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

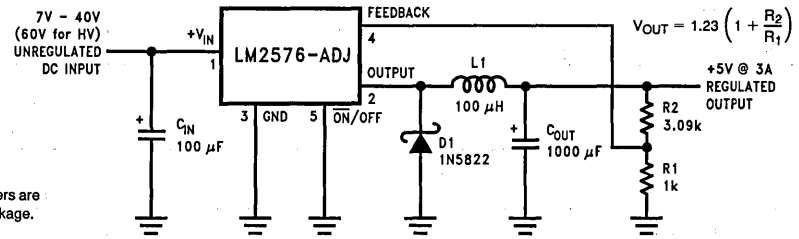
Features

- Adjustable output, reference voltage ±3% max over line and load conditions
- Guaranteed 3A output current
- Wide input voltage range, 4V to 40V (60V for HV)
- Wide output voltage range, 1.23V to 37V
- Requires only 6 external components
- 52 kHz fixed frequency internal oscillator
- Low power standby mode, I_Q typically < 200 μA
- Efficiency typically over 80%
- Uses readily available standard inductors
- Thermal shutdown and current limit protection
- 100% electrical thermal limit burn-in

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter (Inverting Buck-Boost)
- Negative Boost Converter

Typical Application



Note: Pin numbers are for TO-220 Package.

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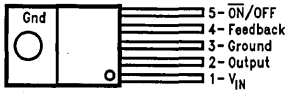
Connection Diagrams

Straight Leads
5-Lead TO-220 (T)

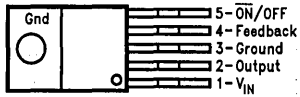


TL/H/11052–2

Top View

Order Number LM2576T-ADJ
or LM2576HVT-ADJ
See NS Package Number T05A

Bent, Staggered Leads
5-Lead TO-220 (T)



TL/H/11052–3

Top View

Order Number LM2576T-ADJ Flow LB03
or LM2576HVT-ADJ Flow LB03
See NS Package Number T05D

4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Maximum Supply Voltage	
LM2576	45V
LM2576HV	63V
$\overline{ON}$/OFF Pin Input Voltage	$-0.3 \le V \le +40V$
Output Voltage to Ground (Steady State)	$-1V$
Power Dissipation	Internally Limited
Storage Temperature Range	$-65°C$ to $+150°C$
Minimum ESD Rating	
(C = 100 pF, R = 1.5 kΩ)	2 kV
FB Pin (Pin 4)	1 kV
Lead Temperature	
(Soldering, 10 sec.)	260°C

Operating Ratings

Maximum Junction Temperature	150°C
Temperature Range	
LM2576/LM2576HV	$-40°C \le T_J \le +125°C$
Supply Voltage	
LM2576	40V
LM2576HV	60V

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, V_{IN} = 12V, and I_{LOAD} = 500 mA.

Symbol	Parameter	Conditions	Typ	LM2576-ADJ LM2576HV-ADJ Limit (Note 2)	Units (Limits)
SYSTEM PARAMETERS (Note 3) Test Circuit *Figure 1*					
V_{OUT}	Feedback Voltage	V_{IN} = 12V, I_{LOAD} = 0.5A V_{OUT} = 5V, Circuit of *Figure 1*	1.230	 1.217 1.243	V V(min) V(max)
V_{OUT}	Feedback Voltage LM2576	0.5A ≤ I_{LOAD} ≤ 3A, 8V ≤ V_{IN} ≤ 40V V_{OUT} = 5V, Circuit of *Figure 1*	1.230	 1.193/**1.180** 1.267/**1.280**	V V(min) V(max)
V_{OUT}	Feedback Voltage LM2576HV	0.5A ≤ I_{LOAD} ≤ 3A, 8V ≤ V_{IN} ≤ 60V V_{OUT} = 5V, Circuit of *Figure 1*	1.230	 1.193/**1.180** 1.273/**1.286**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 3A, V_{OUT} = 5V	82		%
DEVICE PARAMETERS					
I_b	Feedback Bias Current	V_{OUT} = 5V	50	100/**500**	nA
f_O	Oscillator Frequency	(Note 9)	52	 47/**42** 58/**63**	kHz kHz(min) kHz(max)
V_{SAT}	Saturation Voltage	I_{OUT} = 3A (Note 4)	1.4	 1.8/**2.0**	V V(max)
DC	Max Duty Cycle (ON)	(Note 5)	98	 93	% %(min)
I_{CL}	Current Limit	(Notes 4 and 9)	5.8	 4.2/**3.5** 6.9/**7.5**	A A(min) A(max)
I_L	Output Leakage Current	V_{IN} = 40V, (Note 6), Output = 0V Output = −1V Output = −1V	 7.5	2 30	mA(max) mA mA(max)
I_Q	Quiescent Current	(Note 6)	5	 10	mA mA(max)
I_{STBY}	Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF)	50	 200	μA μA(max)
θ_{JA} θ_{JA} θ_{JC}	Thermal Resistance	T Package, Junction to Ambient (Note 7) T Package, Junction to Ambient (Note 8) T Package, Junction to Case	65 45 2		°C/W

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V, and I_{LOAD} = 500 mA. (Continued)

Symbol	Parameter	Conditions	Typ	LM2576-ADJ LM2576HV-ADJ Limit (Note 2)	Units (Limits)
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 1*					
V_{IH} V_{IL}	$\overline{ON}$/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 5V	1.4 1.2	2.2/**2.4** 1.0/**0.8**	V(min) V(max)
I_{IH}	$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF)	12	 30	μA μA(max)
I_{IL}		$\overline{ON}$/OFF Pin = 0V (ON)	0	 10	μA μA(max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face).** All room temperature limits are 100% production tested. All limits at **temperature extremes** are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Note 3: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2576 is used as shown in the *Figure 1* test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.

Note 4: Output (pin 2) sourcing current. No diode, inductor or capacitor connected to output.

Note 5: Feedback (pin 4) removed from output and connected to 0V.

Note 6: Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.

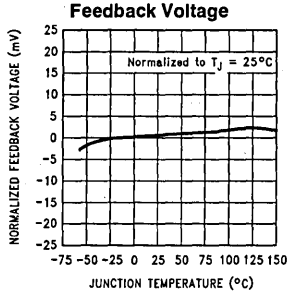
Note 7: Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with ½" leads in a socket, or on a PC board with minimum copper area.

Note 8: Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with ¼" leads soldered to a PC board containing approximately 4 square inches of copper area surrounding the leads.

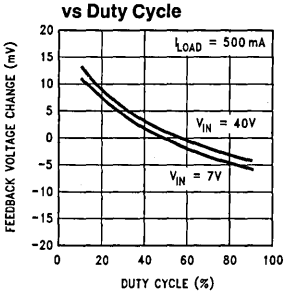
Note 9: The oscillator frequency reduces to approximately 11 kHz in the event of an output short or an overload which pulls the feedback voltage lower than 0.7V. This self-protection feature lowers the average power dissipation of the IC by reducing the minimum duty cycle from 5% to approximately 2%.

Typical Performance Characteristics (Circuit of *Figure 1*)

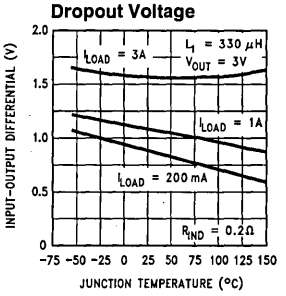
Normalized Feedback Voltage



Feedback Voltage vs Duty Cycle



Dropout Voltage



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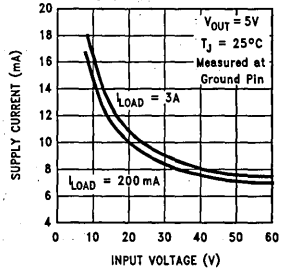
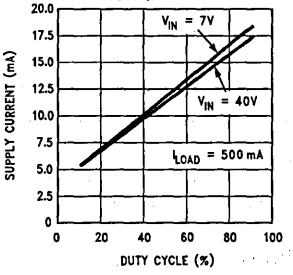
Typical Performance Characteristics (Circuit of *Figure 1*) (Continued)

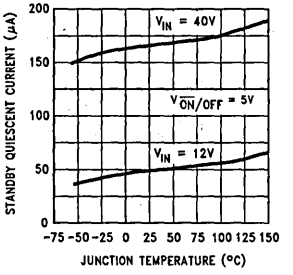
Supply Current



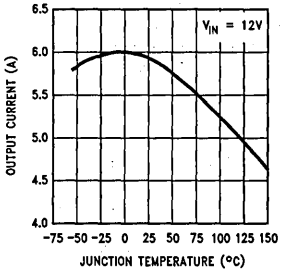
Supply Current vs Duty Cycle



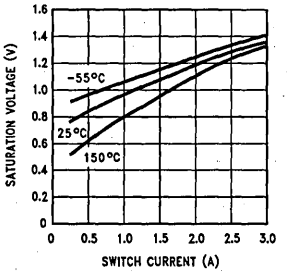
Standby Quiescent Current



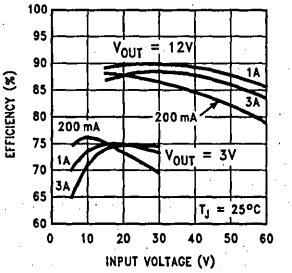
Current Limit



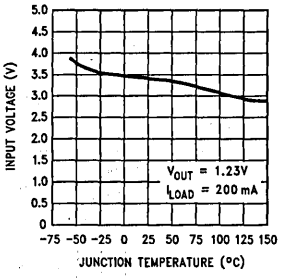
Switch Saturation Voltage



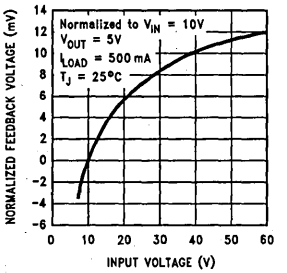
Efficiency



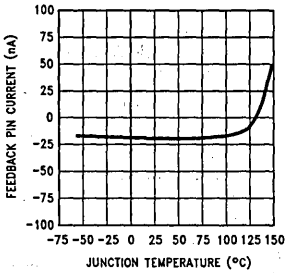
Minimum Operating Voltage



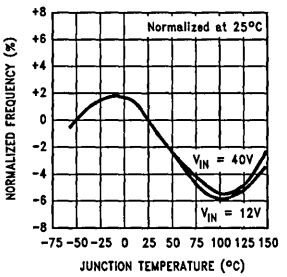
Line Regulation



Feedback Pin Current



Oscillator Frequency



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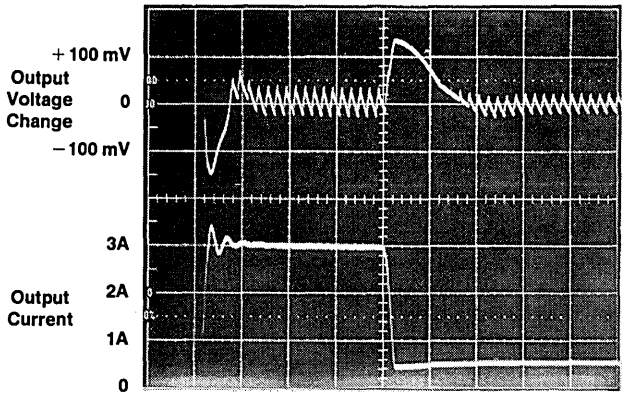
Typical Performance Characteristics (Circuit of *Figure 1*) (Continued)

Load Transient Response



100 μs/div.

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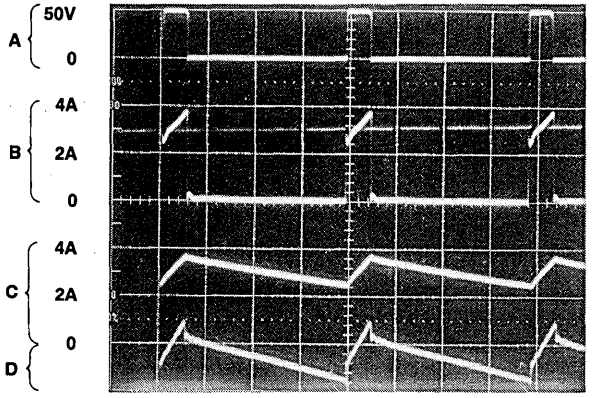
Switching Waveforms



5 μs/div.

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A: Output pin voltage, 50V/div
B: Output pin current, 2A/div
C: Inductor current, 2A/div
D: Output ripple voltage, 50 mV/div, AC-coupled
Horizontal Time Base: 5 μs/div.

Test Circuit and Layout Guidelines

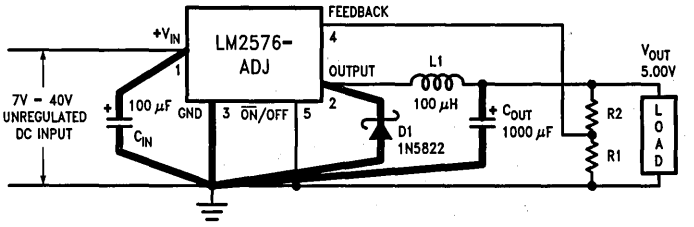

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FIGURE 1

C_{IN} — 100 µF, 50V, Aluminum Electrolytic
C_{OUT} — 1000 µF, 15V, Aluminum Electrolytic
D1 — Schottky, 1N5822
L1 — 100 µH, Pulse Eng. PE-92108
R1 — 1k, 0.01%
R2 — 3.065k, 0.01%
5-pin TO-220 socket—2936 (Loranger Mfg. Co.)

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal stray inductance and ground loops, the length of the leads indicated by heavy lines should be **kept** as **short** as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results.

Block Diagram and Typical Application

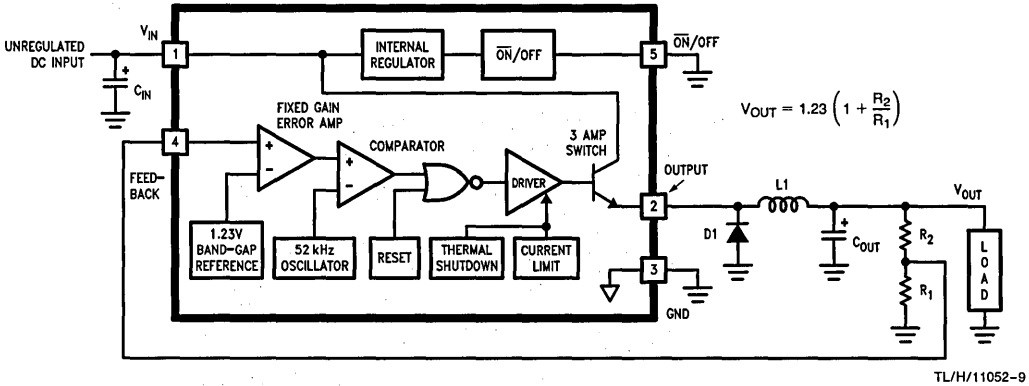

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FIGURE 2

LM2576-ADJ Series Buck Regulator Design Procedure

Procedure	Example
Given: V_{OUT} = Regulated Output Voltage V_{IN}(max) = Maximum input voltage I_{LOAD}(max) = Maximum load current F = Switching frequency *(fixed at 52 kHz)*	**Given:** V_{OUT} = 10V V_{IN}(max) = 25V I_{LOAD}(max) = 3A F = 52 kHz
1. Programming Output Voltage *(selecting R_1 and R_2)* Use the following formula to select the appropriate resistor values. $V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right)$ where V_{REF} = 1.23V R1 can be between 1k and 10k. *(for best temperature coefficient and stability with time, use 1% metal film resistors)* $R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$	**1. Programming Output Voltage** *(selecting R_1 and R_2)* $V_{OUT} = 1.23\left(1 + \frac{R_2}{R_1}\right)$ select R_1 = 1k $R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 1k\left(\frac{10V}{1.23V} - 1\right)$ R_2 = 1k (8.13 −1) = 7.13k, use closest 1% value 7.15k
2. Inductor Selection (L1) A. Calculate E • T (V • μs), from the following formula; $E \bullet T = (V_{IN} - V_{OUT})\frac{V_{OUT}}{V_{IN}} \bullet \frac{1000}{F(\text{in kHz})}$ (V • μs) B. Use the E • T value from the previous formula and match it with the E • T number on the vertical axis of the **inductor value selection guide** shown in *Figure 4.* C. On the horizontal axis, select the maximum load current. D. Identify the region intersected by the E • T value and the maximum load current value, and note the inductor code for that region. E. Match Inductor code to the inductor value as shown in *Figure 5. (and manufacturer's part number)*	**2. Inductor Selection (L1)** A. Calculate E • T (V • μs) $E \bullet T = (25 - 10) \bullet \frac{10}{25} \bullet \frac{1000}{52} = 115\ V \bullet \mu s$ B. E • T = 115 V • μs C. I_{LOAD}(max) = 3A D. Inductor code = H150 E. Inductor value = 150 μH *Choose from **AIE** part #415-0936, **Pulse Engineering** part #PE-53115, or **Renco** part #RL2445.*
3. Output Capacitor Selection (C_{OUT}) The value of the output capacitor together with the inductor defines the dominant pole-pair of the switching regulator loop. For stable operation, the capacitor must satisfy the following requirement: **A.** $C_{OUT} \geq 13{,}300\frac{V_{IN}(max)}{V_{OUT} \bullet L(\mu H)}$ (μF) The above formula yields capacitor values between 10 μF and 2200 μF that will satisfy the loop requirements for stable operation. But to achieve an acceptable output ripple voltage (approximately 1% of the output voltage) and transient response, the output capacitor may need to be several times larger than the above formula yields.	**3. Output Capacitor Selection (C_{OUT})** **A.** $C_{OUT} > 13{,}300\frac{25}{10 \bullet 150} = 221\ \mu F$ However, for acceptable output ripple voltage select $C_{OUT} \geq 680\ \mu F$ C_{OUT} = 680 μF electrolytic Capacitor **B.** Capacitor voltage rating = 20V Higher voltage electrolytic capacitors generally have lower ESR numbers, and for this reason it may be necessary to select a capacitor rated for a higher voltage that would normally be needed. If instability occurs, (especially at the higher input voltages) the ESR of the output capacitor may be at fault, and a higher voltage capacitor or a low ESR switching capacitor should be used.

LM2576-ADJ Series Buck Regulator Design Procedure (Continued)

Procedure

The amount of output ripple voltage is primarily a function of the ESR (Equivalent Series Resistance) of the output capacitor. The value and the type of capacitor used will determine the amount of ESR it contains. Selecting a capacitor with a low ESR will result in a low output ripple voltage. In general, the lower capacitor values have the higher ESR ratings.

The lower capacitor values (220 μF–1000 μF) will allow typically 50 mV to 150 mV of output ripple voltage, while larger-value capacitors will reduce the ripple to approximately 35 mV to 50 mV.

$$V_{RIPPLE\ p\text{-}p} \geq 0.3 \times I_{LOAD}(max) \times ESR$$

To further reduce the output ripple voltage, several standard electrolytic capacitors may be paralleled, or a higher-grade capacitor may be used. Such capacitors are often called "high-frequency", "low-inductance", or "low-ESR". These will reduce the output ripple to 10 mV to 20 mV. However, reducing the ESR below 0.05Ω can cause instability. For this reason, the use of a tantalum capacitor as the sole capacitor is not recommended. Tantalum capacitors (because of their good low temperature characteristics) can be used in parallel with aluminum electrolytics, with the tantalum making up 10% or 20% of the total capacitance.

The capacitor's ripple current rating at 52 kHz should be at least 50% higher than the ripple component of the inductor current.

$$I_{RIPPLE}(max) \geq 1.5 \times 0.3 \times I_{LOAD}(max)$$

B. The capacitor's voltage rating should be at least 1.25 times greater than the output voltage. For a 10V output, a rating of at least 15V is appropriate, and a 20V or 25V rating is recommended.

4. Catch Diode Selection (D1)

The catch-diode current rating must be at least 1.2 times greater than the maximum load current. Also, if the power supply design must withstand continuous shorted output conditions, the diode current rating should be greater than 3A. The most stressful condition for this diode is an overload or short circuit condition.

A. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.

B. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best efficiency, especially in low output voltage switching regulators (less than 5V). Fast-Recovery, High-Efficiency, or Ultra-Fast Recovery diodes are also suitable, but some types with an abrupt turn-off characteristic may cause instability and EMI problems. A fast-recovery diode with soft recovery characteristics is a better choice. Standard 60 Hz diodes (e.g., 1N4001, or IN5400, etc.) are also **not suitable**. See *Figure 3* for Schottky and "soft" fast-recovery diode selection guide.

Example

V_{IN} (max)	Schottky		Fast Recovery	
	3A	4A–6A	3A	4A–6A
20V	1N5820 MBR320P SR302	1N5823	The following diodes are all rated to 100V 31DF1 HER302	The following diodes are all rated to 100V 50WF10 MUR410 HER602
30V	1N5821 MBR330 31DQ03 SR303	50WQ03 31DQ03 1N5824		
40V	1N5822 MBR340 31DQ04 SR304	MBR340 31DQ04 50WQ04 1N5825		
50V	MBR350 31DQ05 SR305	50WQ05		
60V	MBR360 DQ06 SR306	50WQ06 50SQ060		

FIGURE 3. Diode Selection Guide

To further simplify the buck regulator design procedure, National Semiconductor is making available computer design software to be used with the Simple Switcher™ line of switching regulators. ***Switchers Made Simple*** *is available on a (5¼") diskette for IBM compatible computers from a National Semiconductor sales office in your area.*

LM2576-ADJ Series Buck Regulator Design Procedure (Continued)

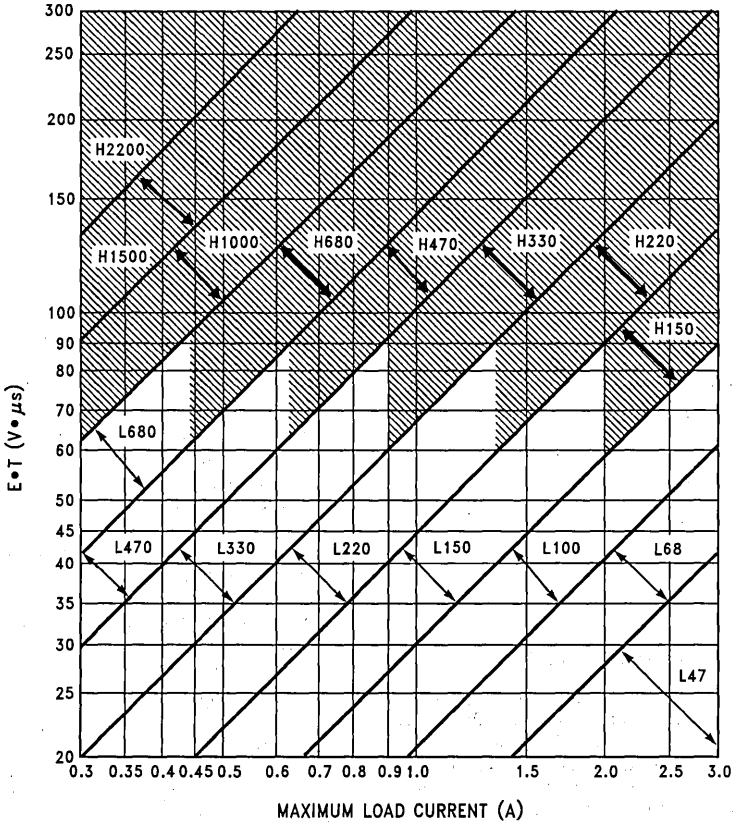

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FIGURE 4. Inductor Value Selection Guide (for Continuous Mode Operation)

Inductor Code	Inductor Value	AIE[1]	Pulse Eng.[2]	Renco[3]
L47	47 μH	415-0932	PE-53112	RL2442
L68	68 μH	415-0931	PE-92114	RL2443
L100	100 μH	415-0930	PE-92108	RL2444
L150	150 μH	415-0953	PE-53113	RL1954
L220	220 μH	415-0922	PE-52626	RL1953
L330	330 μH	415-0926	PE-52627	RL1952
L470	470 μH	415-0927	PE-53114	RL1951
L680	680 μH	415-0928	PE-52629	RL1950
H150	150 μH	415-0936	PE-53115	RL2445
H220	220 μH	430-0636	PE-53116	RL2446
H330	330 μH	430-0635	PE-53117	RL2447
H470	470 μH	430-0634	PE-53118	RL1961
H680	680 μH	415-0935	PE-53119	RL1960
H1000	1000 μH	415-0934	PE-53120	RL1959
H1500	1500 μH	415-0933	PE-53121	RL1958
H2200	2200 μH	415-0945	PE-53122	RL2448

FIGURE 5. Inductor Selection by Manufacturer's Part Number

Note 1: AIE Magnetics, div. Vernatron Corp. Passive Components Group, (813) 347-2181 2801 72nd Street North, St. Petersburg, FL 33710

Note 2: Pulse Engineering, (619) 268-2400 P.O. Box 12235, San Diego, CA 92112

Note 3: Renco Electronics Inc., (516) 586-5566 60 Jeffryn Blvd. East, Deer Park, NY 11729

4

Typical Applications

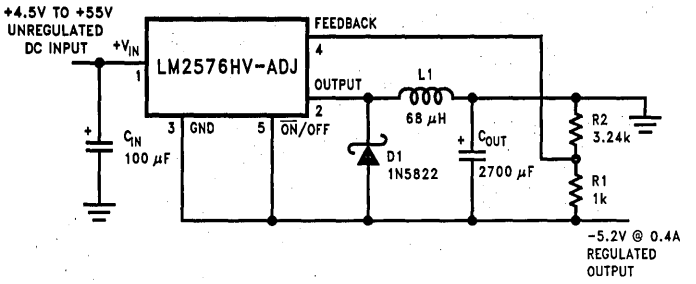

FIGURE 6. Inverting Buck-Boost

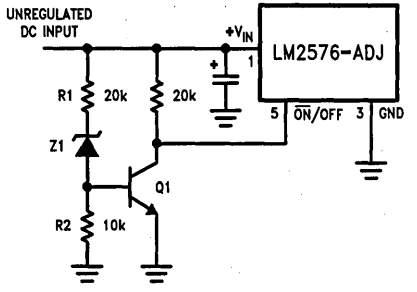

FIGURE 7. Undervoltage Lockout

Figure 6 shows an LM2576HV-ADJ in a very simple buck-boost configuration to generate a negative 5.2V output, from a positive input voltage. This circuit bootstraps the regulator's ground pin to the negative output voltage, then by grounding the feedback pin, the regulator senses the inverted output voltage and regulates it to −5.2V.

The maximum available output current in this configuration is approximately 0.4A. Higher currents (up to 0.7A) are possible with input voltages greater than 8V, or by increasing the value of the output capacitor.

The pulsed switch currents in this buck-boost configuration are higher than in the standard buck-mode design. To avoid exceeding the maximum switch current rating, the available output current is less than the standard buck configuration. Also, the Start-up input current is higher than the standard buck-mode regulator, and this could overload the input power source. Using a delayed turn-on or an undervoltage lockout circuit would allow the input voltage to rise to a high enough level before the switcher would be allowed to turn on. The circuit in *Figure 7* can be modified for the buck-boost under-voltage lockout by wiring the emitter of Q1 and the low side of R1, to the ground pin of the LM2576, which is the negative output of the inverting buck-boost circuit.

The maximum voltage appearing across the inverting regulator is the absolute sum of the input and output voltage. For a −5V output, the maximum input voltage for the LM2576 is +35V, or +55V for the LM2576HV.

The buck regulator design procedure section can not be used to select the inductor, because of the structural differences between the buck and the buck-boost regulator topologies. The recommended range of inductor values for the buck-boost designs is between 47 µH and 200 µH. The peak inductor current, which is the same as the peak switch current, can be calculated from the following formula:

$$I_p \approx \frac{I_{LOAD}\,(V_{IN} + V_O)}{V_{IN}} + \frac{V_{IN}\,V_O}{V_{IN} + V_O} \times \frac{1}{2L1\,f_{OSC}}$$

Where f_{OSC} = 52 kHz. Under normal continuous inductor current operating conditions, the minimum V_{IN} represents the worst case. Select an inductor that is rated for the peak current anticipated.

The ***Switchers Made Simple*** design software can be used to determine the feasibility of regulator designs using different topologies, different input-output parameters, different components, etc.

In some applications it is desirable to keep the regulator off until the input voltage reaches a certain threshold. An undervoltage lockout circuit which accomplishes this task is shown in *Figure 7*. This circuit keeps the regulator off until the input voltage reaches a predetermined level.

$$V_{TH} \approx V_{Z1} + 2V_{BE}\,(Q1)$$

A 3A power supply that features an adjustable output voltage is shown in *Figure 8*. An additional L-C filter that reduces the output ripple by a factor of 10 or more, to about 5 mV, is included in this circuit.

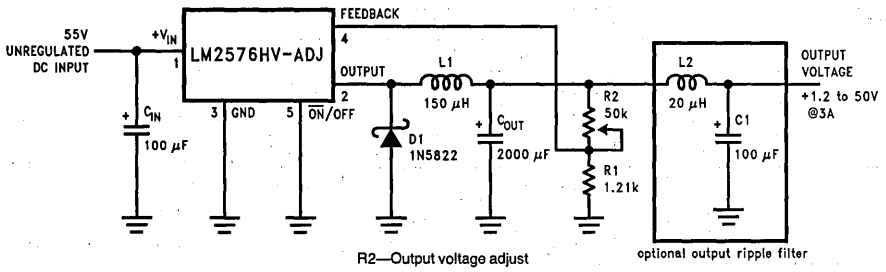

FIGURE 8. 1.2V to 50V Adjustable 3A Power Supply with Low Output Ripple

Application Hints

INPUT CAPACITOR (C_{IN})

Because of higher switching currents, input supply bypassing is more important in the LM2576 than in the LM2575. To maintain stability, the regulator input pin must be bypassed with at least a 47 μF low-ESR electrolytic capacitor. Capacitors with high voltage ratings, or capacitors which are physically larger, generally have a lower ESR. The capacitor's leads must be kept short, and located as close as possible to the regulator.

If the operating temperature range includes temperatures below $-25°C$, the input capacitor value may need to be larger. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures and age. Adding a ceramic or solid tantalum capacitor near the input pin will increase the regulator stability at cold temperatures. For maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be greater than $1.2 \times (t_{ON}/T) \times I_{LOAD}$.

INDUCTOR SELECTION

The inductor value selection guide of *Figure 4* was designed for buck regulator designs of the continuous inductor current type. When using inductor values shown in the inductor selection guide, the peak-to-peak inductor ripple current will be approximately 20% to 30% of the maximum DC current. With relatively heavy load currents, the circuit operates in the continuous mode (inductor current always flowing), but under light load conditions, the circuit will be forced to the discontinuous mode (inductor current falls to zero for a period of time). This discontinuous mode of operation is perfectly acceptable. For light loads (less than approximately 300 mA) it may be desirable to operate the regulator in the discontinuous mode, primarily because of the lower inductor values required for the discontinuous mode.

The LM2576 can be used for both continuous and discontinuous modes of operation. The selection guide chooses inductor values suitable for continuous mode operation, but if the inductor value chosen is prohibitively high, the designer should investigate the possibility of discontinuous operation. The computer design software ***Switchers Made Simple*** will provide all component values for discontinuous (as well as continuous) mode of operation.

Inductors are available in different styles such as pot core, toroid, E-frame, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin core type, consists of wire wrapped on a ferrite rod core. This type of construction makes for an inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more electromagnetic interference (EMI). This EMI can cause problems in sensitive circuits, or can give incorrect scope readings becauseof induced voltages in the scope probe.

The inductors listed in the selection chart include ferrite pot core construction for AIE, powdered iron toroid for Pulse Engineering, and ferrite bobbin core for Renco.

An inductor should not be operated beyond its maximum rated current because it may saturate. When an inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the switch current to rise very rapidly and may cause problems. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

The inductor manufacturers' data sheets include current and energy limits to avoid inductor saturation.

OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.

The output ripple voltage is due mainly to the inductor sawtooth ripple current multiplied by the ESR of the output capacitor (see Section 3A of design procedure).

The voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. To minimize these voltage spikes, special low inductance capacitors must be used, and their lead lengths must be kept short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.

An additional small LC filter can be added to the output to further reduce the amount of output ripple and transients, as in *Figure 8*.

FEEDBACK CONNECTION

The LM2576-ADJ feedback circuitry is designed so that, when the output voltage is connected directly to the Feedback pin, the output voltage is 1.230V.

$\overline{ON}$/OFF INPUT

For normal operation, the $\overline{ON}$/OFF pin should be grounded or driven with a low-level TTL voltage (typically below 1.6V). To put the regulator into standby mode, drive this pin with a high-level TTL or CMOS signal.

GROUNDING

To maintain output voltage stability, the power ground connections must be low-impedance (see *Figure 1*). For the 5-lead TO-220 style package, both the tab and pin 3 are ground and either connection may be used, as they are both part of the same copper lead frame.

HEAT SINK/THERMAL CONSIDERATIONS

In many cases, only a small heat sink is required to keep the LM2576 junction temperature within the allowed operating range. For each application, to determine whether or not a heat sink will be required, the following must be identified:

1. Maximum ambient temperature (in the application).
2. Maximum regulator power dissipation (in application).
3. Maximum allowed junction temperature (125°C for the LM2576). For a safe, conservative design, a temperature approximately 15°C cooler than the maximum temperatures should be selected.
4. LM2576 package thermal resistances θ_{JA} and θ_{JC}.

Total power dissipated by the LM2576 can be estimated as follows:

$$P_D = (V_{IN})(I_Q) + (V_O/V_{IN})(I_{LOAD})(V_{SAT})$$

Application Hints (Continued)

where I_Q (quiescent current) and V_{SAT} can be found in the Characteristic Curves shown previously, V_{IN} is the applied minimum input voltage, V_O is the regulated output voltage, and I_{LOAD} is the load current. The dynamic losses during turn-on and turn-off are negligible if a Schottky type catch diode is used.

When no heat sink is used, the junction temperature rise can be determined by the following:

$$\Delta T_J = (P_D)(\theta_{JA})$$

To arrive at the actual operating junction temperature, add the junction temperature rise to the maximum ambient temperature.

$$T_J = \Delta T_J + T_A$$

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, then a heat sink is required.

When using a heat sink, the junction temperature rise can be determined by the following:

$$\Delta T_J = (P_D)(\theta_{JC} + \theta_{interface} + \theta_{Heat\ sink})$$

The operating junction temperature will be:

$$T_J = T_A + \Delta T_J$$

As above, if the actual operating junction temperature is greater than the selected safe operating junction temperature, then a larger heat sink is required (one that has a lower thermal resistance).

Included on the ***Switcher Made Simple*** design software is a more precise (non-linear) thermal model that can be used to determine junction temperature with different input-output parameters or different component values. It can also calculate the heat sink thermal resistance required to maintain the regulators junction temperature below the maximum operating temperature.

Definition of Terms

BUCK REGULATOR

A switching regulator topology in which a higher voltage is converted to a lower voltage. Also known as a step-down switching regulator.

BUCK-BOOST REGULATOR

A switching regular topology in which a positive voltage is converted to a negative voltage without a transformer.

DUTY CYCLE (D)

Ratio of the output switch's on-time to the oscillator period.

for buck regulator $$D = \frac{t_{ON}}{T} = \frac{V_{OUT}}{V_{IN}}$$

for buck-boost regulator $$D = \frac{t_{ON}}{T} = \frac{|V_O|}{|V_O| + V_{IN}}$$

where T is the oscillator period, typically 1/52 kHz or 19 μs.

CATCH DIODE OR CURRENT STEERING DIODE

The diode which provides a return path for the load current when the LM2576 switch is OFF.

EFFICIENCY (η)

The proportion of input power actually delivered to the load.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

EQUIVALENT SERIES INDUCTANCE (ESL)

The pure inductance component of a capacitor (see *Figure 9*). The amount of inductance is determined to a large extent on the capacitor's construction. In a buck regulator, this unwanted inductance causes voltage spikes to appear on the output.

EQUIVALENT SERIES RESISTANCE (ESR)

The purely resistive component of a real capacitor's impedance (see *Figure 9*). It causes power loss resulting in capacitor heating, which directly affects the capacitor's operating lifetime. When used as a switching regulator output filter, higher ESR values result in higher output ripple voltages.

Most standard aluminum electrolytic capacitors in the 470 μF–2000 μF range have 0.05Ω to 0.3Ω ESR. Higher-grade capacitors ("low-ESR", "high-frequency", or "low-inductance") in the 220 μF–1000 μF range generally have ESR of less than 0.15Ω.

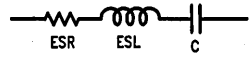

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FIGURE 9. Simple Model of a Real Capacitor

OUTPUT RIPPLE VOLTAGE

The AC component of the switching regulator's output voltage. It is usually dominated by the output capacitor's ESR multiplied by the inductor's ripple current. The peak-to-peak value of this sawtooth ripple current will be typically 20% to 30% of the maximum load current (when the Design Procedure in the datasheet is followed).

CAPACITOR RIPPLE CURRENT

RMS value of the maximum allowable alternating current at which a capacitor can be operated continuously at a specified temperature.

STANDBY QUIESCENT CURRENT (I_{STBY})

Supply current required by the LM2576 when in the standby mode ($\overline{ON}$/OFF pin is driven to TTL-high voltage), thus turning the output switch OFF.

INDUCTOR RIPPLE CURRENT

The peak-to-peak value of the inductor current waveform, typically a sawtooth waveform when the regulator is operating continuous (vs. discontinuous)

CONTINUOUS/DISCONTINUOUS MODE OF OPERATION

Relates to the inductor current. In the continuous mode, the inductor current is always flowing and never drops to zero, vs. the discontinuous mode, where the inductor current drops to zero for a period of time.

INDUCTOR SATURATION

The condition which exists when an inductor cannot hold any more magnetic flux. When an inductor saturates, the inductor appears less inductive and the resistive component dominates. Inductor current is then limited only by the DC resistance of the wire and the available source current.

OPERATING VOLT-MICROSECOND CONSTANT ($E \cdot T_{op}$)

The product (in Volt•μseconds) of the voltage applied to the inductor and the time the voltage is applied. This $E \cdot T_{op}$ constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle.

National Semiconductor

LM1577-ADJ/LM2577-ADJ
Simple Switcher™ Step-Up Voltage Regulator

General Description

The LM1577-ADJ/LM2577-ADJ are monolithic integrated circuits that provide all of the power and control functions for step-up (boost), flyback, and forward converter switching regulators. The output voltage is adjustable, providing up to 60V as a step-up regulator, and even higher voltages as a flyback or forward converter regulator.

Requiring a minimum number of external components, these regulators are cost effective, and simple to use. Listed in this data sheet are a family of standard inductors and flyback transformers designed to work with these switching regulators.

Included on the chip is a 3.0A NPN switch and its associated protection circuitry, consisting of current and thermal limiting, and undervoltage lockout. Other features include a 52 kHz fixed-frequency oscillator that requires no external components, a soft start mode to reduce in-rush current during start-up, and current mode control for improved rejection of input voltage and output load transients.

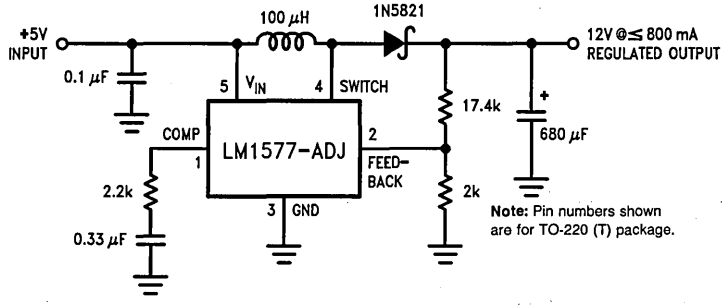
Features

- Requires few external components
- NPN output switches 3.0A, can stand off 65V
- Wide input voltage range: 3.5V to 40V
- Current-mode operation for improved transient response, line regulation, and current limit
- 52 kHz internal oscillator
- Soft-start function reduces in-rush current during start-up
- Output switch protected by current limit, under-voltage lockout, and thermal shutdown

Typical Applications

- Simple boost regulator
- Flyback and forward regulators
- Multiple-output regulator

Typical Application



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Ordering Information

Package Type	NSC Package Drawing	Order Number	Temperature Range
5-Lead TO-220, Straight Leads	T05A	LM2577T-ADJ	−40°C ≤ T_J ≤ +125°C
5-Lead TO-220 Bent, Staggered Leads	T05D	LM2577T-ADJ Flow LB03	
16-Pin Molded DIP	N16A	LM2577N-ADJ	
24-Pin Surface Mount	M24B	LM2577M-ADJ	
4-Pin TO-3	K04A	LM1577K-ADJ/883	−55°C ≤ T_J ≤ +150°C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	45V
Output Switch Voltage	65V
Output Switch Current (Note 2)	6.0A
Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Maximum Junction Temperature	150°C
Minimum ESD Rating (C = 100 pF, R = 1.5 kΩ)	2 kV

Operating Ratings

Supply Voltage	$3.5V \le V_{IN} \le 40V$
Output Switch Voltage	$0V \le V_{SWITCH} \le 60V$
Output Switch Current	$I_{SWITCH} \le 3.0A$
Junction Temperature Range	
LM1577	$-55°C \le T_J \le +150°C$
LM2577	$-40°C \le T_J \le +125°C$

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 5V, $V_{FEEDBACK} = V_{REF}$, and I_{SWITCH} = 0.

Symbol	Parameter	Conditions	Typical	LM1577-ADJ Limit (Notes 3, 8)	LM2577-ADJ Limit (Note 4)	Units (Limits)
SYSTEM PARAMETERS Circuit of *Figure 1* (Note 5)						
V_{OUT}	Output Voltage	V_{IN} = 5V to 10V I_{LOAD} = 100 mA to 800 mA (Note 3)	12.0	 11.60/**11.40** 12.40/**12.60**	 11.60/**11.40** 12.40/**12.60**	V V(min) V(max)
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 3.5V to 10V I_{LOAD} = 300 mA	20	 50/**100**	 50/**100**	mV mV(max)
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load Regulation	V_{IN} = 5V I_{LOAD} = 100 mA to 800 mA	20	 50/**100**	 50/**100**	mV mV(max)
η	Efficiency	V_{IN} = 5V, I_{LOAD} = 800 mA	80			%
DEVICE PARAMETERS						
I_S	Input Supply Current	$V_{FEEDBACK}$ = 1.5V (Switch Off)	7.5	 10.0/**14.0**	 10.0/**14.0**	mA mA(max)
		I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle)	25	 50/**85**	 50/**85**	mA mA(max)
V_{UV}	Input Supply Undervoltage Lockout	I_{SWITCH} = 100 mA	2.90	 2.70/**2.65** 3.10/**3.15**	 2.70/**2.65** 3.10/**3.15**	V V(min) V(max)
f_O	Oscillator Frequency	Measured at Switch Pin I_{SWITCH} = 100 mA	52	 48/**42** 56/**62**	 48/**42** 56/**62**	kHz kHz(min) kHz(max)
V_{REF}	Reference Voltage	Measured at Feedback Pin V_{IN} = 3.5V to 40V V_{COMP} = 1.0V	1.230	1.214/**1.206** 1.246/**1.254**	1.214/**1.206** 1.246/**1.254**	V V(min) V(max)
$\Delta V_{REF}/\Delta V_{IN}$	Reference Voltage Line Regulation	V_{IN} = 3.5V to 40V	0.5			mV
I_B	Error Amp Input Bias Current	V_{COMP} = 1.0V	100	 300/**800**	 300/**800**	nA nA(max)
G_M	Error Amp Transconductance	I_{COMP} = −30 μA to +30 μA V_{COMP} = 1.0V	3700	 2400/**1600** 4800/**5800**	 2400/**1600** 4800/**5800**	μmho μmho(min) μmho(max)
A_{VOL}	Error Amp Voltage Gain	V_{COMP} = 1.1V to 1.9V R_{COMP} = 1.0 MΩ (Note 6)	800	 500/**250**	 500/**250**	V/V V/V(min)

Electrical Characteristics (Continued)

Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 5V, $V_{FEEDBACK}$ = V_{REF}, and I_{SWITCH} = 0.

Symbol	Parameter	Conditions	Typical	LM1577-ADJ Limit (Notes 3, 8)	LM2577-ADJ Limit (Note 4)	Units (Limits)
DEVICE PARAMETERS (Continued)						
	Error Amplifier Output Swing	Upper Limit $V_{FEEDBACK}$ = 1.0V	2.4	2.2/**2.0**	2.2/**2.0**	V V(min)
		Lower Limit $V_{FEEDBACK}$ = 1.5V	0.3	0.40/**0.55**	0.40/**0.55**	V V(max)
	Error Amp Output Current	$V_{FEEDBACK}$ = 1.0V to 1.5V V_{COMP} = 1.0V	±200	±130/±**90** ±300/±**400**	±130/±**90** ±300/±**400**	µA µA(min) µA(max)
I_{SS}	Soft Start Current	$V_{FEEDBACK}$ = 1.0V V_{COMP} = 0V	5.0	2.5/**1.5** 7.5/**9.5**	2.5/**1.5** 7.5/**9.5**	µA µA(min) µA(max)
D	Maximum Duty Cycle	V_{COMP} = 1.5V I_{SWITCH} = 100 mA	95	93/**90**	93/**90**	% %(min)
$\Delta I_{SWITCH}/\Delta V_{COMP}$	Switch Transconductance		12.5			A/V
I_L	Switch Leakage Current	V_{SWITCH} = 65V $V_{FEEDBACK}$ = 1.5V (Switch Off)	10	300/**600**	300/**600**	µA µA(max)
V_{SAT}	Switch Saturation Voltage	I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle)	0.5	0.7/**0.9**	0.7/**0.9**	V V(max)
	NPN Switch Current Limit	V_{COMP} = 2.0V	4.3	3.7/**3.0** 5.3/**6.0**	3.7/**3.0** 5.3/**6.0**	A A(min) A(max)
θ_{JA} θ_{JC}	Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case	35 1.5			°C/W
θ_{JA} θ_{JC}		T Package, Junction to Ambient T Package, Junction to Case	65 2			
θ_{JA}		N Package, Junction to Ambient (Note 7)	85			
θ_{JA}		M Package, Junction to Ambient (Note 7)	100			

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Output current cannot be internally limited when the LM1577/LM2577 is used as a step-up regulator. To prevent damage to the switch, its current must be externally limited to 6.0A. However, output current is internally limited when the LM1577/LM2577 is used as a flyback or forward converter regulator in accordance to the Application Hints.

Note 3: All limits guaranteed at room temperature (standard type face) and at temperature extremes (**boldface type**). All limits are used to calculate Outgoing Quality Level, and are 100% production tested.

Note 4: All limits guaranteed at room temperature (standard type face) and at temperature extremes (**boldface type**). All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Note 5: External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the LM1577/LM2577 is used as shown in the Test Circuit, system performance will be as specified by the system parameters.

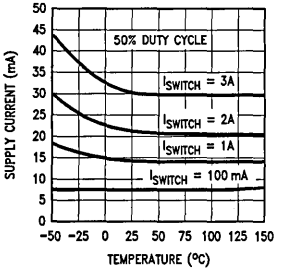
Note 6: A 1.0 MΩ resistor is connected to the compensation pin (which is the error amplifier's output) to ensure accuracy in measuring A_{VOL}. In actual applications, this pin's load resistance should be ≥10 MΩ, resulting in A_{VOL} that is typically twice the guaranteed minimum limit.

Note 7: Junction to ambient thermal resistance with approximately 1 square inch of pc board copper surrounding the leads. Additional copper area will lower thermal resistance further. See thermal model in "Switchers Made Simple" software.

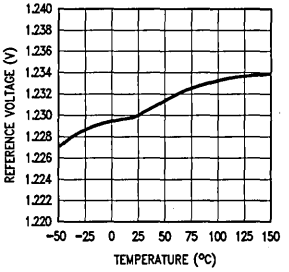
Note 8: A military RETS electrical test specification is available on request. At the time of printing, the LM1577K-ADJ/883 RETS specification complied fully with the **boldface** limits in this column. The LM1577K-ADJ/883 may also be procured to a Standard Military Drawing specification.

Typical Performance Characteristics

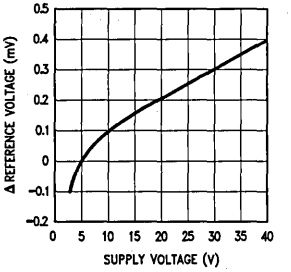
Supply Current vs Temperature



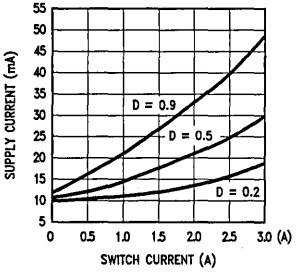
Reference Voltage vs Temperature



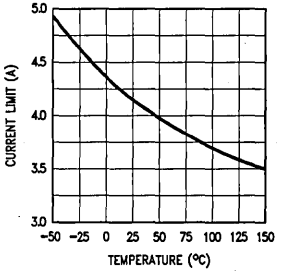
Δ Reference Voltage vs Supply Voltage



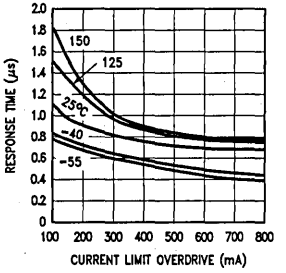
Supply Current vs Switch Current



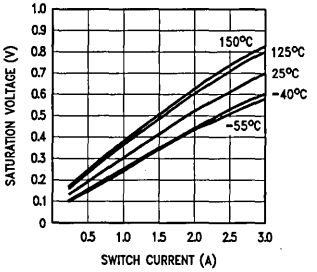
Current Limit vs Temperature



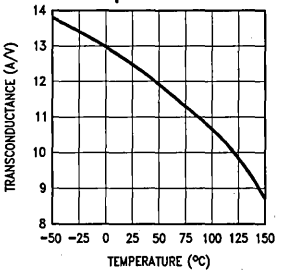
Current Limit Response Time vs Overdrive



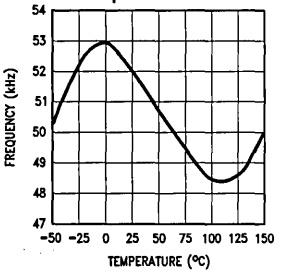
Switch Saturation Voltage vs Switch Current



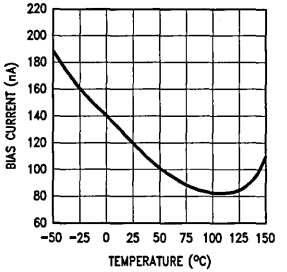
Switch Transconductance vs Temperature



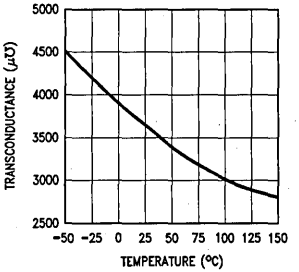
Oscillator Frequency vs Temperature



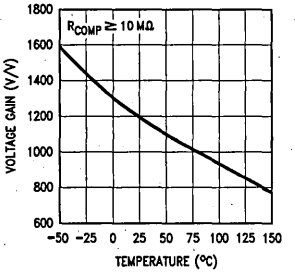
Feedback Pin Bias Current vs Temperature



Error Amp Transconductance vs Temperature



Error Amp Voltage Gain vs Temperature



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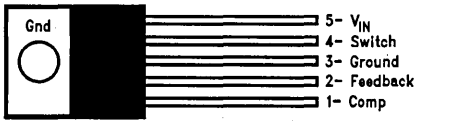
Connection Diagrams

Straight Leads
5-Lead TO-220 (T)



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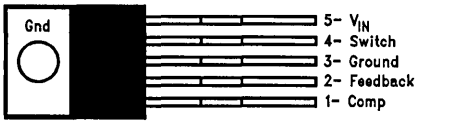
Top View

Order Number LM2577T-ADJ
See NS Package Number T05A

Bent, Staggered Leads
5-Lead TO-220 (T)



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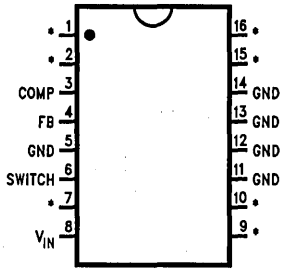
Top View

Order Number LM2577T-ADJ Flow LB03
See NS Package Number T05D

16-Lead DIP (N)



*No internal Connection

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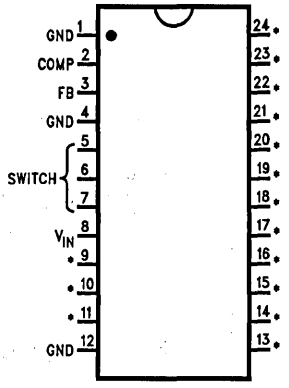
Top View

Order Number LM2577N-ADJ
See NS Package Number N16A

24-Lead Surface Mount (M)



*No internal Connection

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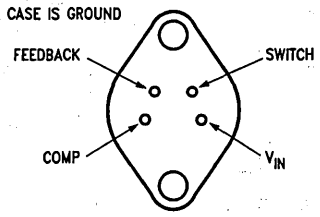
Top View

Order Number LM2577M-ADJ
See NS Package Number M24B

4-Lead TO-3 (K)

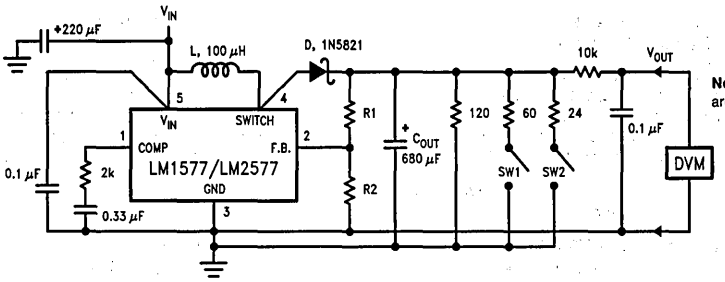


TL/H/10743-3

Bottom View

Order Number LM1577K-ADJ/883
See NS Package Number K04A

Application Hints



L = 415-0930 (AIE)
D = any manufacturer

C_{OUT} = Sprague Type 673D Electrolytic 680 μF, 20V

R1 = 48.7k in series with 511Ω (1%)
R2 = 5.62k (1%)

FIGURE 1. Circuit Used to Specify System Parameters

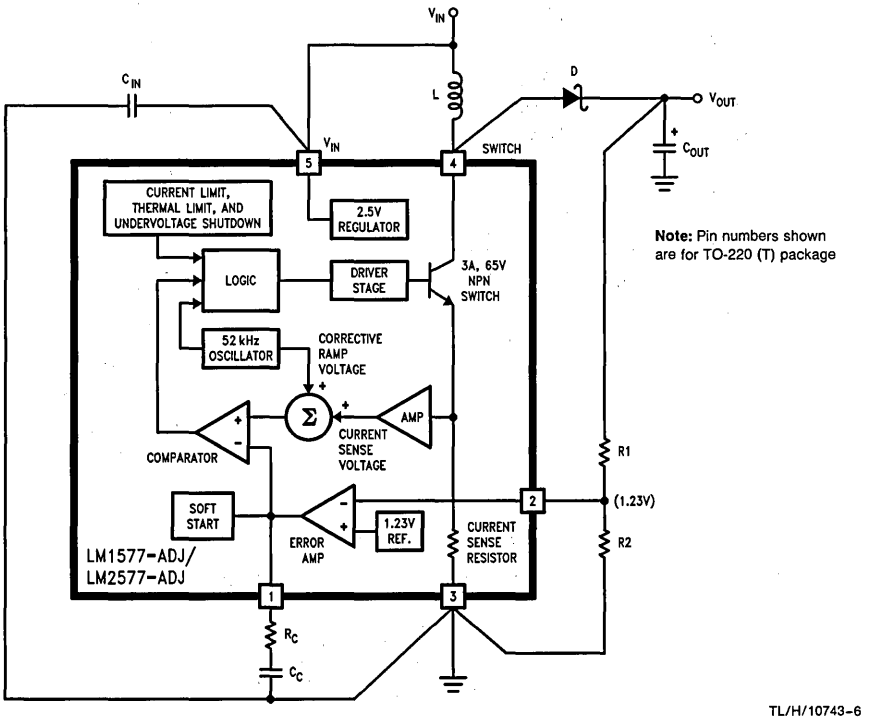


FIGURE 2. LM1577/LM2577 Block Diagram and Boost Regulator Application

STEP-UP (BOOST) REGULATOR

Figure 2 shows the LM1577/LM2577 used as a Step-Up Regulator. This is a switching regulator used for producing an output voltage greater than the input supply voltage.

A basic explanation of how it works is as follows. The LM1577/LM2577 turns its output switch on and off at a frequency of 52 kHz, and this creates energy in the inductor (L). When the NPN switch turns on, the inductor current charges up at a rate of V_{IN}/L, storing current in the inductor. When the switch turns off, the lower end of the inductor flies above V_{IN}, discharging its current through diode (D) into the output capacitor (C_{OUT}) at a rate of $(V_{OUT} - V_{IN})/L$. Thus, energy stored in the inductor during the switch on time is transferred to the output during the switch off time. The output voltage is controlled by the amount of energy transferred which, in turn, is controlled by modulating the peak inductor current. This is done by feeding back a portion of the output voltage to the error amp, which amplifies the difference between the feedback voltage and a 1.230V reference. The error amp output voltage is compared to a voltage proportional to the switch current (i.e., inductor current during the switch on time).

Application Hints (Continued)

The comparator terminates the switch on time when the two voltages are equal, thereby controlling the peak switch current to maintain a constant output voltage.

Voltage and current waveforms for this circuit are shown in *Figure 3*, and formulas for calculating them are given in *Figure 4*.

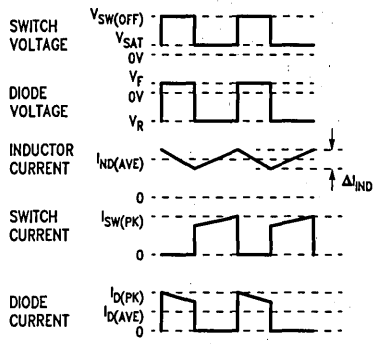


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FIGURE 3. Step-Up Regulator Waveforms

Duty Cycle	D	$\frac{V_{OUT} + V_F - V_{IN}}{V_{OUT} + V_F - V_{SAT}} \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}}$
Average Inductor Current	$I_{IND(AVE)}$	$\frac{I_{LOAD}}{1 - D}$
Inductor Current Ripple	ΔI_{IND}	$\frac{V_{IN} - V_{SAT}}{L} \frac{D}{52{,}000}$
Peak Inductor Current	$I_{IND(PK)}$	$\frac{I_{LOAD}}{1 - D} + \frac{\Delta I_{IND}}{2}$
Peak Switch Current	$I_{SW(PK)}$	$\frac{I_{LOAD}}{1 - D} + \frac{\Delta I_{IND}}{2}$
Switch Voltage When Off	$V_{SW(OFF)}$	$V_{OUT} + V_F$
Diode Reverse Voltage	V_R	$V_{OUT} - V_{SAT}$
Average Diode Current	$I_{D(AVE)}$	I_{LOAD}
Peak Diode Current	$I_{D(PK)}$	$\frac{I_{LOAD}}{1 - D} + \frac{\Delta I_{IND}}{2}$
Power Dissipation of LM1577/2577	P_D	$0.25\Omega \left(\frac{I_{LOAD}}{1 - D}\right)^2 D + \frac{I_{LOAD}\, D\, V_{IN}}{50\,(1 - D)}$

V_F = Forward Biased Diode Voltage
I_{LOAD} = Output Load Current

FIGURE 4. Step-Up Regulator Formulas

STEP-UP REGULATOR DESIGN PROCEDURE

The following design procedure can be used to select the appropriate external components for the circuit in *Figure 2*, based on these system requirements.

Given:

$V_{IN\ (min)}$ = Minimum input supply voltage
V_{OUT} = Regulated output voltage
$I_{LOAD(max)}$ = Maximum output load current

Before proceeding any further, determine if the LM1577/LM2577 can provide these values of V_{OUT} and $I_{LOAD(max)}$ when operating with the minimum value of V_{IN}. The upper limits for V_{OUT} and $I_{LOAD(max)}$ are given by the following equations.

$$V_{OUT} \leq 60V$$

and $V_{OUT} \leq 10 \times V_{IN(min)}$

$$I_{LOAD(max)} \leq \frac{2.1A \times V_{IN(min)}}{V_{OUT}}$$

These limits must be greater than or equal to the values specified in this application.

1. Inductor Selection (L)

A. *Preliminary Calculations:*

The inductor section is based on the calculation of the following three parameters:

$D_{(max)}$, the maximum switch duty cycle ($0 \leq D \leq 0.9$):

$$D_{(max)} = \frac{V_{OUT} + V_F - V_{IN(min)}}{V_{OUT} + V_F - 0.6V}$$

where V_F = 0.5V for Schottky diodes and 0.8V for fast recovery diodes (typically);

E•T, the product of volts × time that charges the inductor:

$$E \bullet T = \frac{D_{(max)}\,(V_{IN(min)} - 0.6V)10^6}{52{,}000\ Hz} \quad (V \bullet \mu s)$$

$I_{IND,DC}$, the average inductor current under full load;

$$I_{IND,DC} = \frac{1.05 \times I_{LOAD(max)}}{1 - D_{(max)}}$$

B. *Identify Inductor Value:*

1. From *Figure 5*, identify the inductor code for the region indicated by the intersection of E•T and $I_{IND,DC}$. This code gives the inductor value in microhenries. The L or H prefix signifies whether the inductor is rated for a maximum E•T of 90 V•μs (L) or 250 V•μs (H).

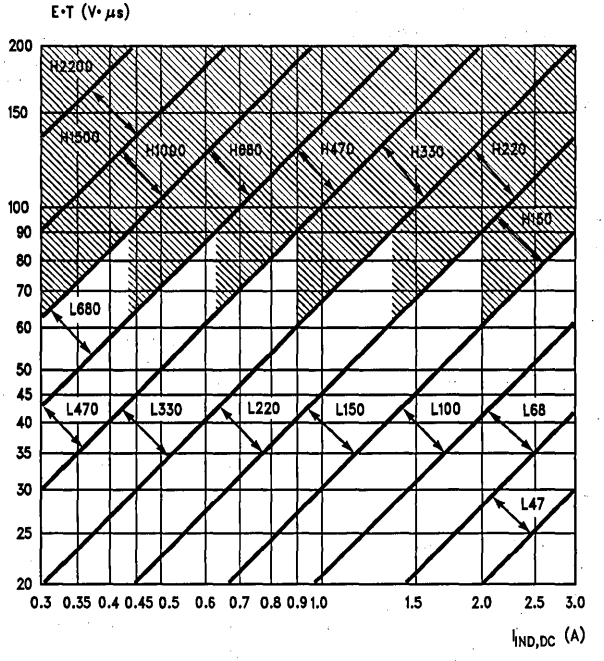
2. If $D < 0.85$, go on to step C. If $D \geq 0.85$, then calculate the minimum inductance needed to ensure the switching regulator's stability:

$$L_{MIN} = \frac{6.4\,(V_{IN(min)} - 0.6V)\,(2D_{(max)} - 1)}{1 - D_{(max)}} \quad (\mu H)$$

If L_{MIN} is smaller than the inductor value found in step B1, go on to step C. Otherwise, the inductor value found in step B1 is too low; an appropriate inductor code should be obtained from the graph as follows:

1. Find the lowest value inductor that is greater than L_{MIN}.
2. Find where E•T intersects this inductor value to determine if it has an L or H prefix. If E•T intersects both the L and H regions, select the inductor with an H prefix.

Application Hints (Continued)



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Note:

This chart assumes that the inductor ripple current inductor is approximately 20% to 30% of the average inductor current (when the regulator is under full load). Greater ripple current causes higher peak switch currents and greater output ripple voltage; lower ripple current is achieved with larger-value inductors. The factor of 20 to 30% is chosen as a convenient balance between the two extremes.

FIGURE 5. Inductor Selection Graph

C. *Select an inductor* from the table of *Figure 6* which cross-references the inductor codes to the part numbers of three different manufacturers. Complete specifications for these inductors are available from the respective manufacturers. The inductors listed in this table have the following characteristics:

AIE: ferrite, pot-core inductors; Benefits of this type are low electro-magnetic interference (EMI), small physical size, and very low power dissipation (core loss). Be careful not to operate these inductors too far beyond their maximum ratings for E•T and peak current, as this will saturate the core.

Pulse: powdered iron, toroid core inductors; Benefits are low EMI and ability to withstand E•T and peak current above rated value better than ferrite cores.

Renco: ferrite, bobbin-core inductors; Benefits are low cost and best ability to withstand E•T and peak current above rated value. Be aware that these inductors generate more EMI than the other types, and this may interfere with signals sensitive to noise.

Inductor Code	Manufacturer's Part Number		
	AIE	Pulse	Renco
L47	415 - 0932	PE - 53112	RL2442
L68	415 - 0931	PE - 92114	RL2443
L100	415 - 0930	PE - 92108	RL2444
L150	415 - 0953	PE - 53113	RL1954
L220	415 - 0922	PE - 52626	RL1953
L330	415 - 0926	PE - 52627	RL1952
L470	415 - 0927	PE - 53114	RL1951
L680	415 - 0928	PE - 52629	RL1950
H150	415 - 0936	PE - 53115	RL2445
H220	430 - 0636	PE - 53116	RL2446
H330	430 - 0635	PE - 53117	RL2447
H470	430 - 0634	PE - 53118	RL1961
H680	415 - 0935	PE - 53119	RL1960
H1000	415 - 0934	PE - 53120	RL1959
H1500	415 - 0933	PE - 53121	RL1958
H2200	415 - 0945	PE - 53122	RL2448

AIE Magnetics, div. Vernitron Corp., (813) 347-2181
2801 72nd Street North, St. Petersburg, FL 33710
Pulse Engineering, (619) 268-2400
P.O. Box 12235, San Diego, CA 92112
Renco Electronics Inc., (516) 586-5566
60 Jeffryn Blvd. East, Deer Park, NY 11729

FIGURE 6. Table of Standardized Inductors and Manufacture's Part Numbers

Application Hints (Continued)

2. Compensation Network (R_C, C_C) and Output Capacitor (C_{OUT}) Selection

R_C and C_C form a pole-zero compensation network that stabilizes the regulator. The values of R_C and C_C are mainly dependant on the regulator voltage gain, $I_{LOAD(max)}$, L and C_{OUT}. The following procedure calculates values for R_C, C_C, and C_{OUT} that ensure regulator stability. Be aware that this procedure doesn't necessarily result in R_C and C_C that provide optimum compensation. In order to guarantee optimum compensation, one of the standard procedures for testing loop stability must be used, such as measuring V_{OUT} transient response when pulsing I_{LOAD}. (See *Figure 11*.)

A. *First, calculate the maximum value for* R_C

$$R_C \leq \frac{750 \times I_{LOAD(max)} \times V_{OUT}^2}{V_{IN(min)}^2}$$

Select a resistor less than or equal to this value, and it should also be no greater than 3 kΩ.

B. *Calculate the minimum value for* C_{OUT} using the following two equations.

$$C_{OUT} \geq \frac{0.19 \times L \times R_C \times I_{LOAD(max)}}{V_{IN(min)} \times V_{OUT}}$$

and

$$C_{OUT} \geq \frac{V_{IN(min)} \times R_C \times (V_{IN(min)} + (3.74 \times 10^5 \times L))}{487{,}800 \times V_{OUT}^3}$$

The larger of these two values is the minmum value that ensures stability.

C. *Calculate the minimum value of* C_C.

$$C_C \geq \frac{58.5 \times V_{OUT}^2 \times C_{OUT}}{R_C^2 \times V_{IN(min)}}$$

The compensation capacitor is also part of the soft start circuitry. When power to the regulator is turned on, the switch duty cycle is allowed to rise at a rate controlled by this capacitor (with no control on the duty cycle, it would immediately rise to 90%, drawing huge currents from the input power supply). In order to operate properly, the soft start circuit requires $C_C \geq 0.22\ \mu F$.

The value of the output filter capacitor is normally large enough to require the use of aluminum electrolytic capacitors. *Figure 7* lists several different types that are recommended for switching regulators, and the following parameters are used to select the proper capacitor.

Working Voltage (WVDC): Choose a capacitor with a working voltage at least 20% higher than the regulator output voltage.

Ripple Current: This is the maximum RMS value of current that charges the capacitor during each switching cycle. For step-up and flyback regulators, the formula for ripple current is

$$I_{RIPPLE(RMS)} = \frac{I_{LOAD(max)} \times D_{(max)}}{1 - D_{(max)}}$$

Choose a capacitor that is rated at least 50% higher than this value at 52 kHz.

Equivalent Series Resistance (ESR): This is the primary cause of output ripple voltage, and it also affects the values of R_C and C_C needed to stabilize the regulator. As a result, the preceding calculations for C_C and R_C are only valid if ESR doesn't exceed the maximum value specified by the following equations.

$$ESR \leq \frac{0.01 \times 15V}{I_{RIPPLE(P\text{-}P)}} \text{ and } \leq \frac{8.7 \times (10) - 3 \times V_{IN}}{I_{LOAD(max)}}$$

where

$$I_{RIPPLE(P\text{-}P)} = \frac{1.15 \times I_{LOAD(max)}}{1 - D_{(max)}}$$

Select a capacitor with ESR, at 52 kHz, that is less than or equal to the lower value calculated. Most electrolytic capacitors specify ESR at 120 Hz which is 15% to 30% higher than at 52 kHz. Also, be aware that ESR increases by a factor of 2 when operating at −20°C.

Application Hints (Continued)

In general, low values of ESR are achieved by using large value capacitors (C ≥ 470 μF), and capacitors with high WVDC, or by paralleling smaller-value capacitors.

3. Output Voltage Selection (R1 and R2)

Resistors R1 and R2 divide the output down so it can be compared with the LM1577/LM2577 internal 1.23V reference. For a given desired output voltage V_{OUT}, select R1 and R2 so that

$$\frac{R1}{R2} = \frac{V_{OUT}}{1.23V} - 1$$

4. Input Capacitor Selection (C_{IN})

The switching action in the step-up regulator causes a triangular ripple current to be drawn from the supply source. This in turn causes noise to appear on the supply voltage. For proper operation of the LM1577, the input voltage should be decoupled. Bypassing the Input Voltage pin directly to ground with a good quality, low ESR, 0.1 μF capacitor (leads as short as possible) is normally sufficient.

If the LM1577 is located far from the supply source filter capacitors, an additional large electrolytic capacitor (e.g. 47 μF) is often required.

5. Diode Selection (D)

The switching diode used in the boost regulator must withstand a reverse voltage equal to the circuit output voltage, and must conduct the peak output current of the LM2577. A suitable diode must have a minimum reverse breakdown voltage greater than the circuit output voltage, and should be rated for average and peak current greater than $I_{LOAD(max)}$ and $I_{D(PK)}$. Schottky barrier diodes are often favored for use in switching regulators. Their low forward voltage drop allows higher regulator efficiency than if a (less expensive) fast recovery diode was used. See *Figure 8* for recommended part numbers and voltage ratings of 1A and 3A diodes.

Cornell Dubilier—Types 239, 250, 251, UFT, 300, or 350
P.O. Box 128, Pickens, SC 29671
(803) 878-6311

Nichicon—Types PF, PX, or PZ
927 East Parkway, Schaumburg, IL 60173
(708) 843-7500

Sprague—Types 672D, 673D, or 674D
Box 1, Sprague Road, Lansing, NC 28643
(919) 384-2551

United Chemi-Con—Types LX, SXF, or SXJ
9801 West Higgins Road, Rosemont, IL 60018
(708) 696-2000

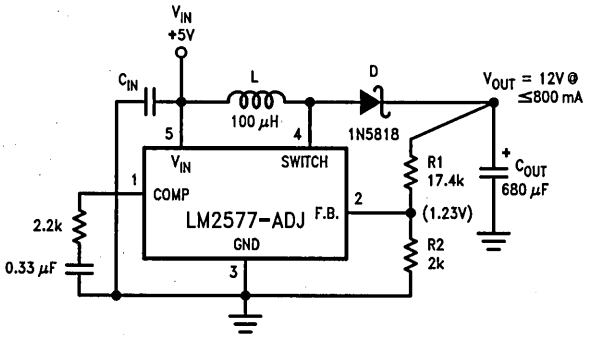
FIGURE 7. Aluminum Electrolytic Capacitors Recommended for Switching Regulators

V_{OUT} (max)	Schottky		Fast Recovery	
	1A	3A	1A	3A
20V	1N5817 MBR120P	1N5820 MBR320P		
30V	1N5818 MBR130P 11DQ03	1N5821 MBR330P 31DQ03		
40V	1N5819 MBR140P 11DQ04	1N5822 MBR340P 31DQ04		
50V	MBR150 11DQ05	MBR350 31DQ05	1N4933 MUR105	
100V			1N4934 HER102 MUR110 10DL1	MR851 30DL1 MR831 HER302

FIGURE 8. Diode Selection Chart

Application Hints (Continued)

By adding a few external components (as shown in *Figure 9*), the LM2577 can be used to produce a regulated output voltage that is greater than the applied input voltage. Typical performance of this regulator is shown in *Figures 10* and *11*. The switching waveforms observed during the operation of this circuit are shown in *Figure 12*.



TL/H/10743-9

Note: Pin numbers shown are for TO-220 (T) package.

FIGURE 9. Step-up Regulator Delivers 12V from a 5V Input

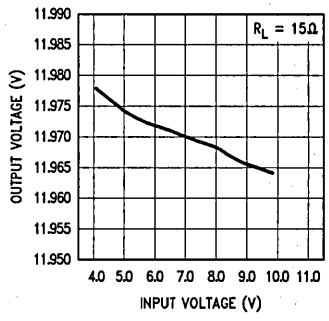


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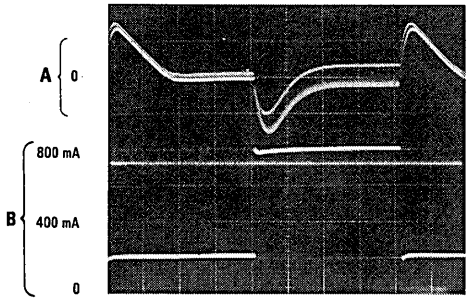
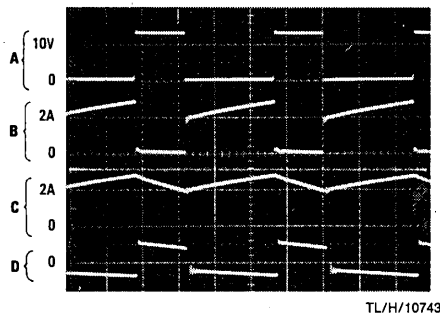
FIGURE 10. Line Regulation (Typical) of Step-Up Regulator of *Figure 9*



TL/H/10743-11

FIGURE 11. Load Transient Response of Step-Up Regulator of *Figure 9*

A: Output Voltage Change, 100 mV/div. (AC-coupled)
B: Load current, 0.2 A/div
Horizontal: 5 ms/div



TL/H/10743-12

FIGURE 12. Switching Waveforms of Step-Up Regulator of *Figure 9*

A: Switch pin voltage, 10 V/div
B: Switch pin current, 2 A/div
C: Inductor current, 2 A/div
D: Output ripple voltage, 100 mV/div (AC-coupled)
Horizontal: 5 μs/div

Application Hints (Continued)

FLYBACK REGULATOR

A Flyback regulator can produce single or multiple output voltages that are lower or greater than the input supply voltage. *Figure 13* shows the LM1577/LM2577 used as a flyback regulator with positive and negative regulated outputs. Its operation is similar to a step-up regulator, except the output switch controls the primary current of a flyback transformer. Note that the primary and secondary windings are out of phase, so no current flows through secondary when current flows through the primary. This allows the primary to charge up the transformer core when the switch is on. When the switch turns off, the core discharges by sending current through the secondary, and this produces voltage at the outputs. The output voltages are controlled by adjusting the peak primary current, as described in the step-up regulator section.

Voltage and current waveforms for this circuit are shown in *Figure 14*, and formulas for calculating them are given in *Figure 15*.

FLYBACK REGULATOR DESIGN PROCEDURE

1. Transformer Selection

A family of standardized flyback transformers are available for creating flyback regulators that produce ± dual output voltages, as shown in *Figure 13*. *Figure 16* lists these transformers with the input voltage, output voltages and maximum load current they are designed for.

2. Compensation Network (C_C, R_C) and Output Capacitor (C_{OUT}) Selection

As explained in the Step-Up Regulator Design Procedure, C_C, R_C and C_{OUT} must be selected as a group. The following procedure is for a dual output flyback regulator with equal turns ratios for each secondary (i.e. both output voltages have the same magnitude). The equations can be used for a single output regulator by changing $\Sigma I_{LOAD(max)}$ to $I_{LOAD(max)}$ in the following equations.

A. *First, calculate the maximum value for R_C.*

$$R_C \leq \frac{750 \times \Sigma I_{LOAD(max)} \times (V_{OUT} + V_{IN(min)}N)^2}{V_{IN(min)}^2}$$

Where $\Sigma I_{LOAD(max)}$ is the sum of the load current (magnitude) required from both outputs. Select a resistor less than or equal to this value, and no greater than 3 kΩ.

B. *Calculate the minimum value for ΣC_{OUT}* (sum of C_{OUT} at both outputs) using the following two equations.

$$C_{OUT} \geq \frac{0.19 \times R_C \times L_P \times \Sigma I_{LOAD(max)}}{V_{OUT} \times V_{IN(min)}}$$

and

$$C_{OUT} \geq \frac{V_{IN(min)} \times R_C \times N^2 \times (V_{IN(min)} + (3.74 \times 10^5 \times L_P))}{487{,}800 \times V_{OUT}^2 \times (V_{OUT} + V_{IN(min)} \times N)}$$

The larger of these two values must be used to ensure regulator stability.

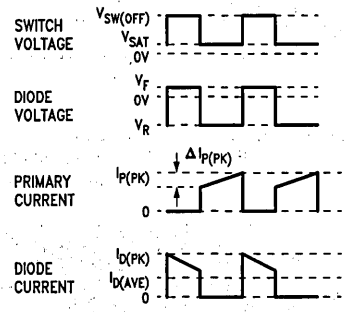


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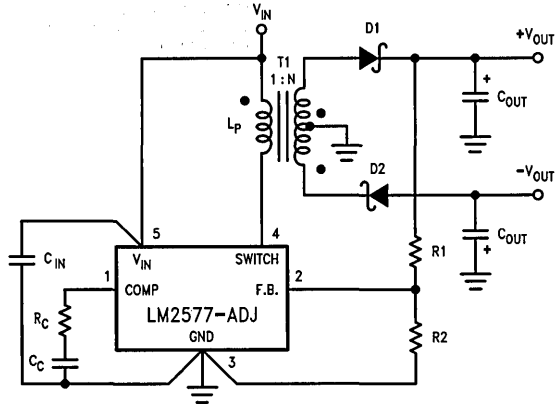
FIGURE 14. Flyback Regulator Waveforms



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Note: Pin numbers shown are for the TO-220 (T) package.

FIGURE 13. LM1577/LM2577 Flyback Regulator with ± Outputs

Application Hints (Continued)

Duty Cycle	D	$\frac{V_{OUT} + V_F}{N(V_{IN} - V_{SAT}) + V_{OUT} + V_F} \approx \frac{V_{OUT}}{N(V_{IN}) + V_{OUT}}$
Primary Current Variation	ΔI_P	$\frac{D(V_{IN} - V_{SAT})}{L_P \times 52{,}000}$
Peak Primary Current	$I_{P(PK)}$	$\frac{N}{\eta} \times \frac{\Sigma I_{LOAD}}{1 - D} + \frac{\Delta I_{PK}}{2}$
Switch Voltage when Off	$V_{SW(OFF)}$	$V_{IN} + \frac{V_{OUT} + V_F}{N}$
Diode Reverse Voltage	V_R	$V_{OUT} + N(V_{IN} - V_{SAT})$
Average Diode Current	$I_{D(AVE)}$	I_{LOAD}
Peak Diode Current	$I_{D(PK)}$	$\frac{I_{LOAD}}{1 - D} + \frac{\Delta I_{IND}}{2}$
Short Circuit Diode Current		$\approx \frac{6A}{N}$
Power Dissipation of LM1577/LM2577	P_D	$0.25\Omega \left(\frac{N \Sigma I_{LOAD}}{1 - D}\right)^2 + \frac{N I_{LOAD} D}{50(1 - D)} V_{IN}$

N = Transformer Turns Ratio = $\frac{\text{number of secondary turns}}{\text{number of primary turns}}$

η = Transformer Efficiency *(typically 0.95)*

$\Sigma I_{LOAD} = |+I_{LOAD}| + |-I_{LOAD}|$

FIGURE 15. Flyback Regulator Formulas

C. *Calculate the minimum value of* C_C

$$C_C \geq \frac{58.5 \times C_{OUT} \times V_{OUT} \times (V_{OUT} + (V_{IN(min)} \times N))}{R_C^2 \times V_{IN(min)} \times N}$$

D. *Calculate the maximum ESR* of the $+V_{OUT}$ and $-V_{OUT}$ output capacitors in parallel.

$$ESR+ \| ESR- \leq \frac{8.7 \times 10^{-3} \times V_{IN(min)} \times V_{OUT} \times N}{\Sigma I_{LOAD(max)} \times (V_{OUT} + (V_{IN(min)} \times N))}$$

This formula can also be used to calculate the maximum ESR of a single output regulator.

At this point, refer to this same section in the **Step-Up Regulator Design Procedure** for more information regarding the selection of C_{OUT}.

4

3. Output Voltage Selection

Resistors R1 and R2 divide the output down so that it can be compared to the LM1577/LM2577 internal reference. For a desired output voltage, select R1 and R2 so that

$$\frac{R1}{R2} = \frac{V_{OUT}}{1.23V} - 1$$

4. Diode Selection

The switching diode in a flyback converter must withstand the reverse voltage specified by the following equation.

$$V_R = V_{OUT} + \frac{V_{IN}}{N}$$

A suitable diode must have a reverse voltage rating greater than this. In addition it must be rated for more than the average and peak diode currents listed in *Figure 15*.

5. Input Capacitor Selection

The primary of a flyback transformer draws discontinuous pulses of current from the input supply. As a result, a flyback regulator generates more noise at the input supply than a step-up regulator, and this requires a larger bypass capacitor to decouple the LM1577/LM2577 V_{IN} pin from this noise. For most applications, a low ESR, 1.0 μF cap will be sufficient, if it is connected very close to the V_{IN} and Ground pins.

In addition to this bypass cap, a larger capacitor (≥ 47 μF) should be used where the flyback transformer connects to the input supply. This will attenuate noise which may interfere with other circuits connected to the same input supply voltage.

Transformer Type		Input Voltage	Dual Output Voltage	Maximum Output Current
1	L_P = 100 μH N = 1	5V	±10V	325 mA
		5V	±12V	275 mA
		5V	±15V	225 mA
2	L_P = 200 μH N = 0.5	10V	±10V	700 mA
		10V	±12V	575 mA
		10V	±15V	500 mA
		12V	±10V	800 mA
		12V	±12V	700 mA
		12V	±15V	575 mA
3	L_P = 250 μH N = 0.5	15V	±10V	900 mA
		15V	±12V	825 mA
		15V	±15V	700 mA

Transformer Type	Manufacturers' Part Numbers		
	AIE	Pulse	Renco
1	326-0637	PE-65300	RL-2580
2	330-0202	PE-65301	RL-2581
3	330-0203	PE-65302	RL-2582

FIGURE 16. Flyback Transformer Selection Guide

6. Snubber Circuit

A "snubber" circuit is required when operating from input voltages greater than 10V, or when using a transformer with $L_P \geq 200$ μH. This circuit clamps a voltage spike from the transformer primary that occurs immediately after the output switch turns off. Without it, the switch voltage may exceed the 65V maximum rating. As shown in *Figure 17*, the snubber consists of a fast recovery diode, and a parallel RC. The RC values are selected for switch clamp voltage (V_{CLAMP}) that is 5V to 10V greater than $V_{SW(OFF)}$. Use the following equations to calculate R and C;

$$C \geq \frac{0.02 \times L_P \times I_{P(PK)}^2}{(V_{CLAMP})^2 - (VSW_{(OFF)})^2}$$

$$R \leq \left(\frac{V_{CLAMP} + V_{SW(OFF)} - V_{IN}}{2}\right)^2 \times \left(\frac{19.2 \times 10^{-4}}{L_P \times I_{P(PK)}^2}\right)$$

Power dissipation (and power rating) of the resistor is;

$$P = \left(\frac{V_{CLAMP} + V_{SW(OFF)} - V_{IN}}{2}\right)^2 / R$$

The fast recovery diode must have a reverse voltage rating greater than V_{CLAMP}.

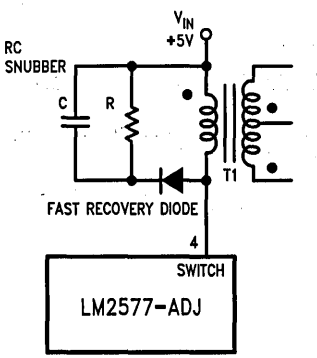

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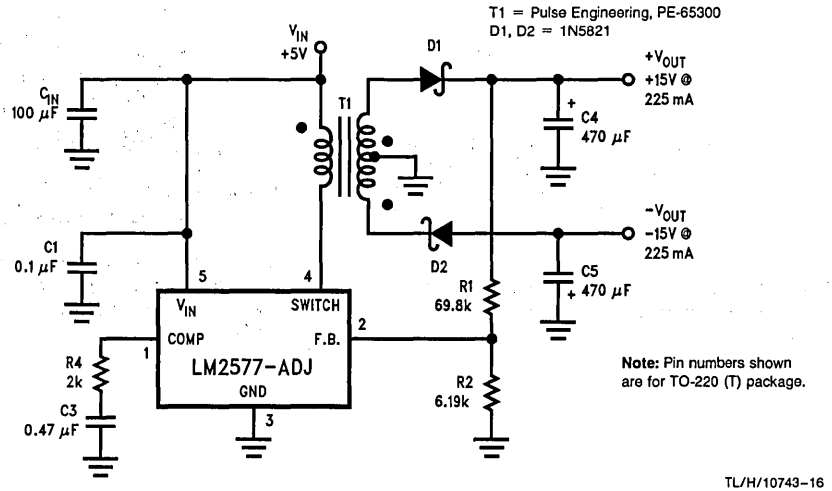
FIGURE 17. Snubber Circuit

Application Hints (Continued)

The circuit of *Figure 18* produces ±15V (at 225 mA each) from a single 5V input. The output regulation of this circuit is shown in *Figures 19* and *20*, while the load transient response is shown in *Figures 21* and *22*. Switching waveforms seen in this circuit are shown in *Figure 15*.



TL/H/10743–16

FIGURE 18. Flyback Regulator Easily Provides Additional Outputs

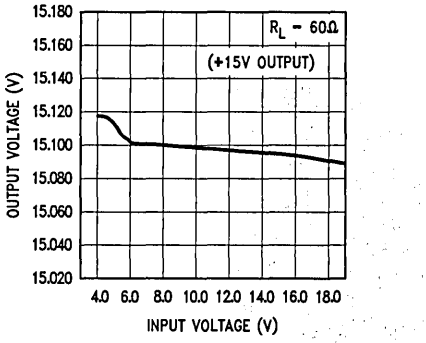


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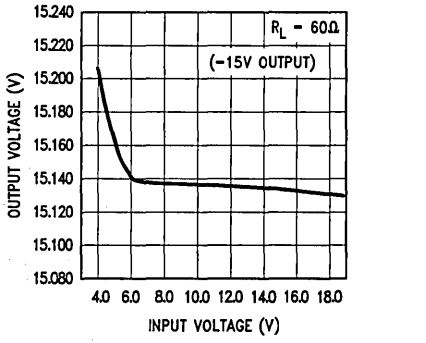
FIGURE 19. Line Regulation (Typical) of Flyback Regulator of *Figure 13*, +15V Output



TL/H/10743–18

FIGURE 20. Line Regulation (Typical) of Flyback Regulator of *Figure 13*, −15V Output

Application Hints (Continued)

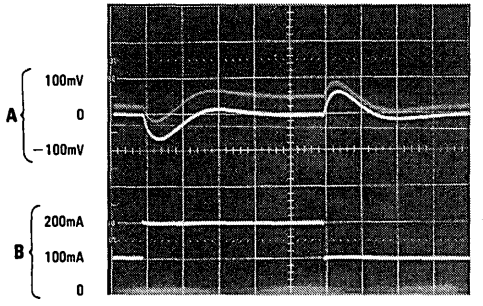


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FIGURE 21. Load Transient Response of Flyback Regulator of *Figure 13*, +15V Output

A: Output Voltage Change, 100 mV/div
B: Output Current, 100 mA/div
Horizontal: 10 ms/div

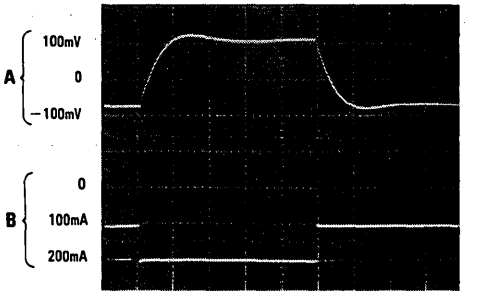

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FIGURE 22. Load Transient Response of Flyback Regulator of *Figure 13*, −15V Output

A: Output Voltage Change, 100 mV/div
B: Output Current, 100 mA/div
Horizontal: 10 ms/div

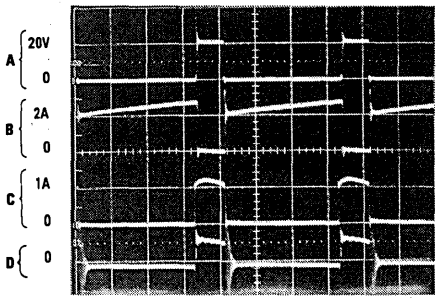

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FIGURE 23. Switching Waveforms of Flyback Regulator of *Figure 13*, Each Output Loaded with 60Ω

A: Switch pin voltage, 20 V/div
B: Primary current, 2 A/div
C: +15V Secondary current, 1 A/div
D: +15V Output ripple voltage, 100 mV/div
Horizontal: 5 μs/div

National Semiconductor

LM1578A/LM2578A/LM3578A Switching Regulator

General Description

The LM1578A is a switching regulator which can easily be set up for such DC-to-DC voltage conversion circuits as the buck, boost, and inverting configurations. The LM1578A features a unique comparator input stage which not only has separate pins for both the inverting and non-inverting inputs, but also provides an internal 1.0V reference to each input, thereby simplifying circuit design and p.c. board layout. The output can switch up to 750 mA and has output pins for its collector and emitter to promote design flexibility. An external current limit terminal may be referenced to either the ground or the V_{in} terminal, depending upon the application. In addition, the LM1578A has an on board oscillator, which sets the switching frequency with a single external capacitor from <1 Hz to 100 kHz (typical).

The LM1578A is an improved version of the LM1578, offering higher maximum ratings for the total supply voltage and output transistor emitter and collector voltages.

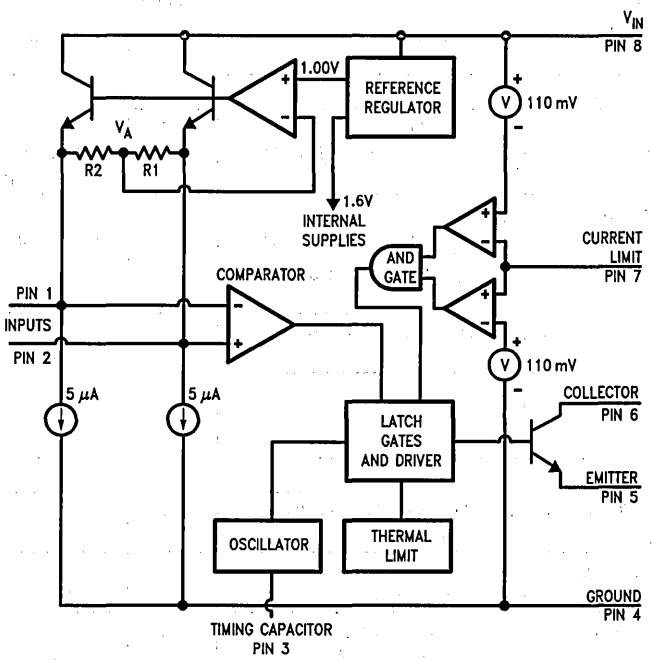
Features

- Inverting and non-inverting feedback inputs
- 1.0V reference at inputs
- Operates from supply voltages of 2V to 40V
- Output current up to 750 mA, saturation less than 0.9V
- Current limit and thermal shut down
- Duty cycle up to 90%

Applications

- Switching regulators in buck, boost, inverting, and single-ended transformer configurations
- Motor speed control
- Lamp flasher

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	50V
Collector Output to Ground	−0.3V to +50V
Emitter Output to Ground (Note 2)	−1V to +50V
Power Dissipation (Note 3)	Internally limited
Output Current	750 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	260°C
Maximum Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV

Operating Ratings

Ambient Temperature Range	
LM1578A	$-55°C \le T_A \le +125°C$
LM2578A	$-40°C \le T_A \le +85°C$
LM3578A	$0°C \le T_A \le +70°C$
Junction Temperature Range	
LM1578A	$-55°C \le T_J \le +150°C$
LM2578A	$-40°C \le T_J \le +125°C$
LM3578A	$0°C \le T_J \le +125°C$

Electrical Characteristics

These specifications apply for $2V \le V_{IN} \le 40V$ ($2.2V \le V_{IN} \le 40V$ for $T_J \le -25°C$), timing capacitor C_T = 3900 pF, and 25% ≤ duty cycle ≤ 75%, unless otherwise specified. Values in standard typeface are for T_J = 25°C; values in **boldface type** apply for operation over the specified operating junction temperature range.

Symbol	Parameter	Conditions	Typical (Note 5)	LM1578A Limit (Note 6)	LM2578A/ LM3578A Limit (Note 7)	Units
OSCILLATOR						
f_{OSC}	Frequency		20	 22.4 17.6	 24 16	kHz kHz (max) kHz (min)
$\Delta f_{OSC}/\Delta T$	Frequency Drift with Temperature		**−0.13**			%/°C
	Amplitude		550			mV_{p-p}
REFERENCE/COMPARATOR (Note 8)						
V_R	Input Reference Voltage	$I_1 = I_2$ = 0 mA and $I_1 = I_2$ = 1 mA ±1% (Note 9)	1.0	 1.035/**1.050** 0.965/**0.950**	 1.050/**1.070** 0.950/**0.930**	V V (max) V (min)
$\Delta V_R/\Delta V_{IN}$	Input Reference Voltage Line Regulation	$I_1 = I_2$ = 0 mA and $I_1 = I_2$ = 1 mA ±1% (Note 9)	0.003	 0.01/**0.02**	 0.01/**0.02**	%/V %/V (max)
I_{INV}	Inverting Input Current	$I_1 = I_2$ = 0 mA, duty cycle = 25%	0.5			μA
	Level Shift Accuracy	Level Shift Current = 1 mA	1.0	 5/**8**	 10/**13**	% % (max)
$\Delta V_R/\Delta t$	Input Reference Voltage Long Term Stability		100			ppm/1000h
OUTPUT						
V_C (sat)	Collector Saturation Voltage	I_C = 750 mA pulsed, Emitter grounded	0.7	 0.85/**1.2**	 0.90/**1.0**	V V (max)
V_E (sat)	Emitter Saturation Voltage	I_O = 80 mA pulsed, $V_{IN} = V_C$ = 40V	1.4	 1.6/**2.1**	 1.7/**2.0**	V V (max)
I_{CES}	Collector Leakage Current	$V_{IN} = V_{CE}$ = 40V, Emitter grounded, Output OFF	0.1	 50/**100**	 200/**250**	μA μA (max)
$BV_{CEO(SUS)}$	Collector-Emitter Sustaining Voltage	I_{SUST} = 0.2A (pulsed), V_{IN} = 0	60	 50	 50	V V (min)

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Typical (Note 5)	LM1578A Limit (Note 6)	LM2578A/ LM3578A Limit (Note 7)	Units
CURRENT LIMIT						
V_{CL}	Sense Voltage Shutdown Level	Referred to V_{IN} or Ground (Note 10)	110	95 140	80 160	mV mV (min) mV (max)
$\Delta V_{CL}/\Delta T$	Sense Voltage Temperature Drift		**0.3**			%/°C
I_{CL}	Sense Bias Current	Referred to V_{IN} Referred to ground	4.0 0.4			μA μA
DEVICE POWER CONSUMPTION						
I_S	Supply Current	Output OFF, V_E = 0V	2.0	3.0/**3.3**	3.5/**4.0**	mA mA (max)
		Output ON, I_C = 750 mA pulsed, V_E = 0V	14			mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: For $T_J \geq 100°C$, the Emitter pin voltage should not be driven more than 0.6V below ground (see Application Information).

Note 3: At elevated temperatures, devices must be derated based on package thermal resistance. The device in the TO-99 package must be derated at 150°C/W, junction to ambient, or 45°C/W, junction to case. The device in the 8-pin DIP must be derated at 95°C/W, junction to ambient. The device in the surface-mount package must be derated at 150°C/W, junction-to-ambient.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values are for T_J = 25°C and represent the most likely parametric norm.

Note 6: All limits guaranteed and 100% production tested at room temperature (standard type face) and at **temperature extremes (bold type face).** All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 7: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face).** Room temperature limits are 100% production tested. Limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate AOQL.

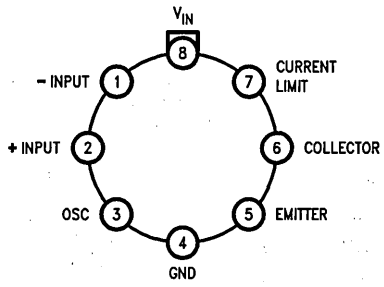
Note 8: Input terminals are protected from accidental shorts to ground but if external voltages higher than the reference voltage are applied, excessive current will flow and should be limited to less than 5 mA.

Note 9: I_1 and I_2 are the external sink currents at the inputs (refer to Test Circuit).

Note 10: Connection of a 10 kΩ resistor from pin 1 to pin 4 will drive the duty cycle to its maximum, typically 90%. Applying the minimum Current Limit Sense Voltage to pin 7 will not reduce the duty cycle to less than 50%. Applying the maximum Current Limit Sense Voltage to pin 7 is certain to reduce the duty cycle below 50%. Increasing this voltage by 15 mV may be required to reduce the duty cycle to 0%, when the Collector output swing is 40V or greater (see Ground-Referred Current Limit Sense Voltage typical curve).

Connection Diagram and Ordering Information

Metal Can



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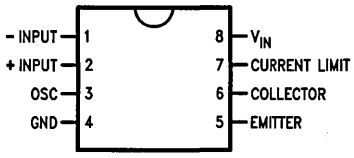
Top View
Order Number LM1578AH, LM2578AH, or LM3578AH
See NS Package Number H08C

Dual-In-Line Package

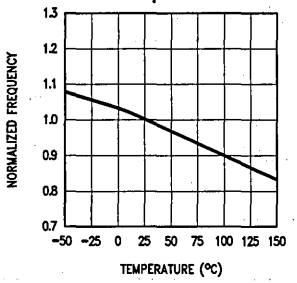


TL/H/8711–29

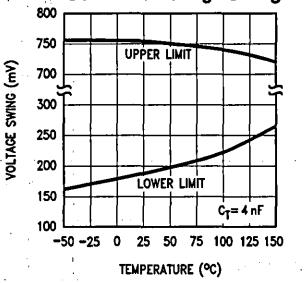
Order Number LM3578AM, LM2578AN or LM3578AN
See NS Package Number M08A or N08E

Typical Performance Characteristics

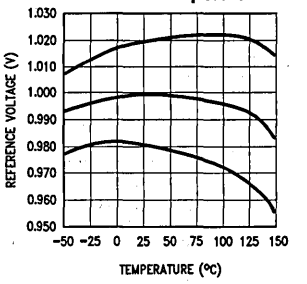
Oscillator Frequency Change with Temperature



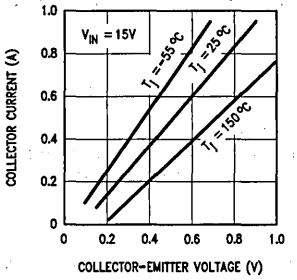
Oscillator Voltage Swing



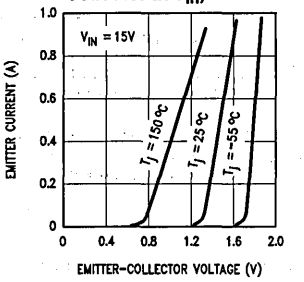
Input Reference Voltage Drift with Temperature



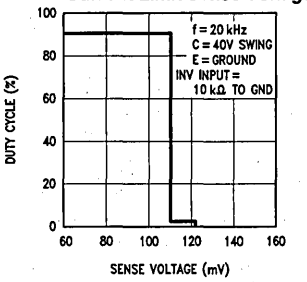
Collector Saturation Voltage (Sinking Current, Emitter Grounded)



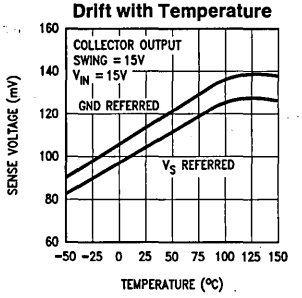
Emitter Saturation Voltage (Sourcing Current, Collector at V_{IN})



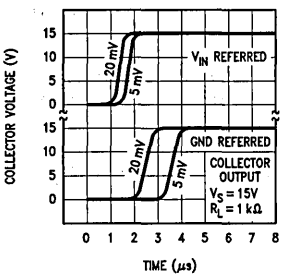
Ground Referred Current Limit Sense Voltage



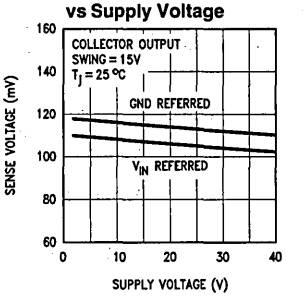
Current Limit Sense Voltage Drift with Temperature



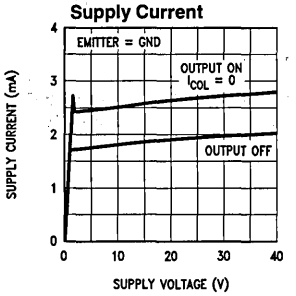
Current Limit Response Time for Various Over Drives



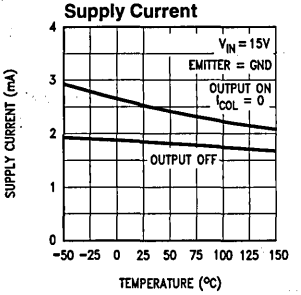
Current Limit Sense Voltage vs Supply Voltage



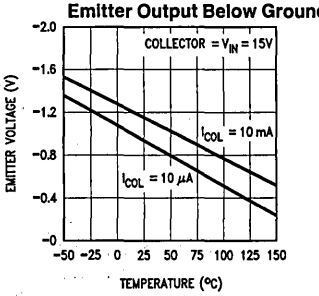
Supply Current



Supply Current



Collector Current with Emitter Output Below Ground



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Test Circuit*

Parameter tests can be made using the test circuit shown. Select the desired V_{in}, collector voltage and duty cycle with adjustable power supplies. A digital volt meter with an input resistance greater than 100 MΩ should be used to measure the following:

Input Reference Voltage to Ground; S1 in either position.

Level Shift Accuracy (%) = $(T_{P3}(V)/1V) \times 100\%$; S1 at $I_1 = I_2 = 1$ mA

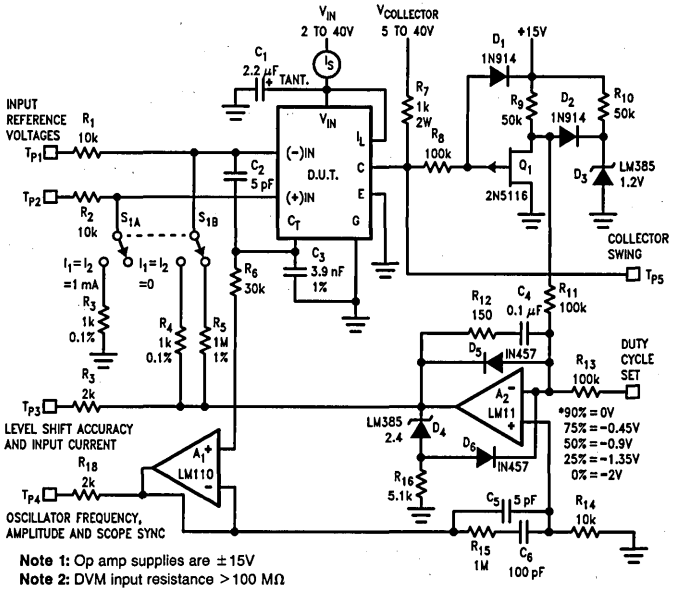
Input Current (mA) = $(1V - T_{p3}(V))/1$ MΩ: S1 at $I_1 = I_2 = 0$ mA.

Oscillator parameters can be measured at T_{p4} using a frequency counter or an oscilloscope.

The Current Limit Sense Voltage is measured by connecting an adjustable 0-to-1V floating power supply in series with the current limit terminal and referring it to either the ground or the V_{in} terminal. Set the duty cycle to 90% and monitor test point T_{P5} while adjusting the floating power supply voltage until the LM1578A's duty cycle just reaches 0%. This voltage is the Current Limit Sense Voltage.

The Supply Current should be measured with the duty cycle at 0% and S1 in the $I_1 = I_2 = 0$ mA position.

*LM1578A specifications are measured using automated test equipment. This circuit is provided for the customer's convenience when checking parameters. Due to possible variations in testing conditions, the measured values from these testing procedures may not match those of the factory.



Note 1: Op amp supplies are ±15V
Note 2: DVM input resistance >100 MΩ
Note 3: *LM1578 max duty cycle is 90%

TL/H/8711–3

Definition of Terms

Input Reference Voltage: The reference voltage referred to ground, applied to either the inverting or non-inverting inputs, which will cause the output to switch ON or OFF.

Input Reference Current: The current applied to either the inverting or the non-inverting input which will cause the output to switch ON or OFF.

Input Level Shift Accuracy: If there are two equal resistors sinking current from the inverting and non-inverting input terminals, the Input Level Shift Accuracy is the ratio of the voltage across the resistors to produce a given duty cycle at the output.

Collector Saturation Voltage: With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's emitter connected to ground, the Collector Saturation Voltage is the collector-to-emitter voltage for a given collector current.

Emitter Saturation Voltage: With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's collector connected to V_{in}, the Emitter Saturation Voltage is the collector-to-emitter voltage for a given emitter current.

Collector Emitter Sustaining Voltage: The collector-emitter breakdown voltage of the output transistor, measured at a specified current.

Current Limit Sense Voltage: The voltage at the Current Limit pin, referred to either the supply or the ground terminal, which (via logic circuitry) will cause the output transistor to turn OFF and resets cycle-by-cycle at the oscillator frequency.

Current Limit Sense Current: The bias current for the Current Limit terminal with the applied voltage equal to the Current Limit Sense Voltage.

Supply Current: The IC power supply current, excluding the current drawn through the output transistor, with the oscillator operating.

Functional Description

The LM1578A is a pulse-width modulator designed for use as a switching regulator controller. It may also be used in other applications which require controlled pulse-width voltage drive.

A control signal, usually representing output voltage, fed into the LM1578A's comparator is compared with an internally-generated reference. The resulting error signal and the oscillator's output are fed to a logic network which determines when the output transistor will be turned ON or OFF. The following is a brief description of the subsections of the LM1578A.

COMPARATOR INPUT STAGE

The LM1578A's comparator input stage is unique in that both the inverting and non-inverting inputs are available to the user, and both contain a 1.0V reference. This is accomplished as follows: A 1.0V reference is fed into a modified voltage follower circuit (see FUNCTIONAL DIAGRAM). When both input pins are open, no current flows through R1 and R2. Thus, both inputs to the comparator will have the potential of the 1.0V reference, V_A. When one input, for example the non-inverting input, is pulled ΔV away from V_A, a current of $\Delta V/R1$ will flow through R1. This same current flows through R2, and the comparator sees a total voltage of $2\Delta V$ between its inputs. The high gain of the system, through feedback, will correct for this imbalance and return both inputs to the 1.0V level.

This unusual comparator input stage increases circuit flexibility, while minimizing the total number of external components required for a voltage regulator system. The inverting switching regulator configuration, for example, can be set up without having to use an external op amp for feedback polarity reversal (see TYPICAL APPLICATIONS).

OSCILLATOR

The LM1578A provides an on-board oscillator which can be adjusted up to 100 kHz. Its frequency is set by a single external capacitor, C_1, as shown in *Figure 1*, and follows the equation

$$f_{OSC} = 8 \times 10^{-5}/C_1$$

The oscillator provides a blanking pulse to limit maximum duty cycle to 90%, and a reset pulse to the internal circuitry.

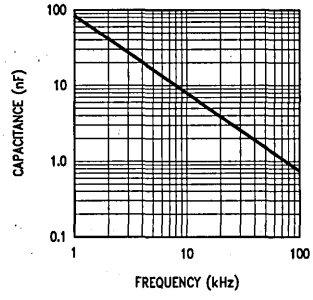


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FIGURE 1. Value of Timing Capacitor vs Oscillator Frequency

OUTPUT TRANSISTOR

The output transistor is capable of delivering up to 750 mA with a saturation voltage of less than 0.9V. (see *Collector Saturation Voltage* and *Emitter Saturation Voltage* curves).

The emitter must not be pulled more than 1V below ground (this limit is 0.6V for $T_J \geq 100°C$). Because of this limit, an external transistor must be used to develop negative output voltages (see the Inverting Regulator Typical Application). Other configurations may need protection against violation of this limit (see the Emitter Output section of the Applications Information).

CURRENT LIMIT

The LM1578A's current limit may be referenced to either the ground or the V_{in} pins, and operates on a cycle-by-cycle basis.

The current limit section consists of two comparators: one with its non-inverting input referenced to a voltage 110 mV below V_{in}, the other with its inverting input referenced 110 mV above ground (see FUNCTIONAL DIAGRAM). The current limit is activated whenever the current limit terminal is pulled 110 mV away from either V_{in} or ground.

Applications Information

CURRENT LIMIT

As mentioned in the functional description, the current limit terminal may be referenced to either the V_{in} or the ground terminal. Resistor R3 converts the current to be sensed into a voltage for current limit detection.

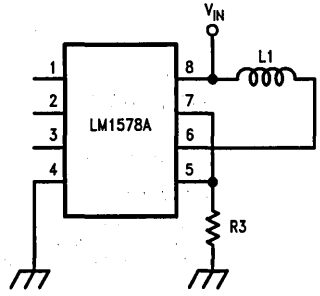

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FIGURE 2. Current Limit, Ground Referred

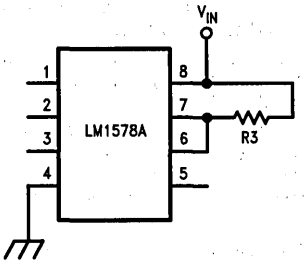

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FIGURE 3. Current Limit, V_{in} Referred

Applications Information (Continued)

CURRENT LIMIT TRANSIENT SUPPRESSION

When noise spikes and switching transients interfere with proper current limit operation, R1 and C1 act together as a low pass filter to control the current limit circuitry's response time.

Because the sense current of the current limit terminal varies according to where it is referenced, R1 should be less than 2 kΩ when referenced to ground, and less than 100Ω when referenced to V_{in}.

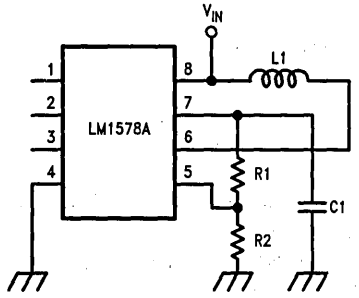

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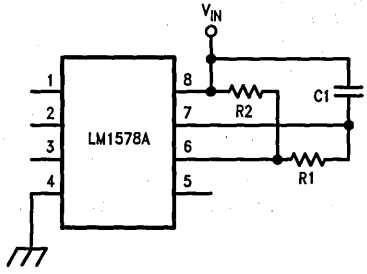
FIGURE 4. Current Limit Transient Suppressor, Ground Referred

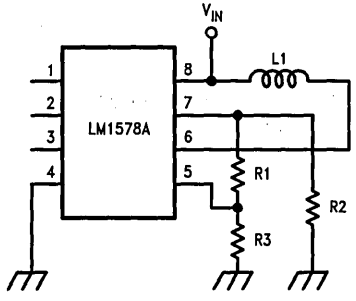


TL/H/8711–18

FIGURE 5. Current Limit Transient Suppressor, V_{in} Referred

C.L. SENSE VOLTAGE MULTIPLICATION

When a larger sense resistor value is desired, the voltage divider network, consisting of R1 and R2, may be used. This effectively multiplies the sense voltage by (1 + R1/R2). Also, R1 can be replaced by a diode to increase current limit sense voltage to about 800 mV (diode V_f + 110 mV).



TL/H/8711–19

FIGURE 6. Current Limit Sense Voltage Multiplication, Ground Referred

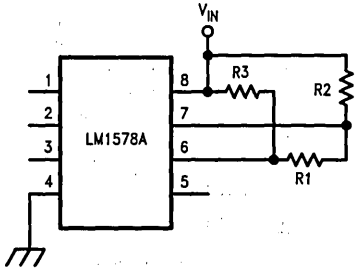


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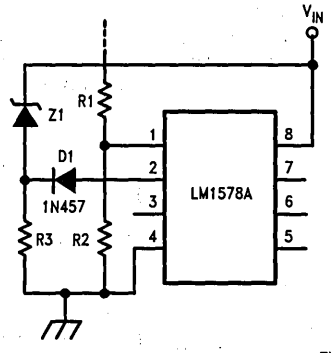
FIGURE 7. Current Limit Sense Voltage Multiplication, V_{in} Referred

UNDER-VOLTAGE LOCKOUT

Under-voltage lockout is accomplished with few external components. When V_{in} becomes lower than the zener breakdown voltage, the output transistor is turned off. This occurs because diode D1 will then become forward biased, allowing resistor R3 to sink a greater current from the non-inverting input than is sunk by the parallel combination of R1 and R2 at the inverting terminal. R3 should be one-fifth of the value of R1 and R2 in parallel.



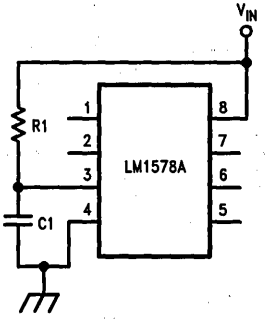
TL/H/8711–22

FIGURE 8. Under-Voltage Lockout

MAXIMUM DUTY CYCLE LIMITING

The maximum duty cycle can be externally limited by adjusting the charge to discharge ratio of the oscillator capacitor with a single external resistor. Typical values are 50 μA for the charge current, 450 μA for the discharge current, and a voltage swing from 200 mV to 750 mV. Therefore, R1 is selected for the desired charging and discharging slopes and C1 is readjusted to set the oscillator frequency.

Applications Information (Continued)



TL/H/8711–21

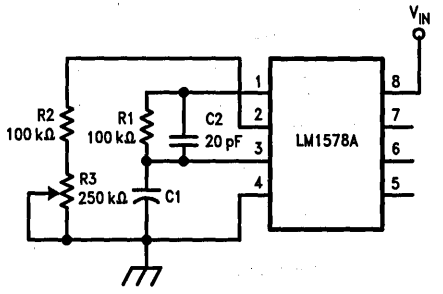
FIGURE 9. Maximum Duty Cycle Limiting

DUTY CYCLE ADJUSTMENT

When manual or mechanical selection of the output transistor's duty cycle is needed, the cirucit shown below may be used. The output will turn on with the beginning of each oscillator cycle and turn off when the current sunk by R2 and R3 from the non-inverting terminal becomes greater than the current sunk from the inverting terminal.

With the resistor values as shown, R3 can be used to adjust the duty cycle from 0% to 90%.

When the sum of R2 and R3 is twice the value of R1, the duty cycle will be about 50%. C1 may be a large electrolytic capacitor to lower the oscillator frequency below 1 Hz.

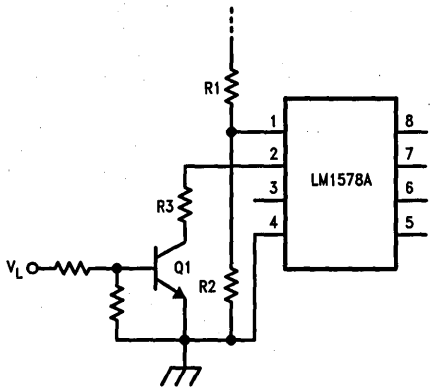


TL/H/8711–23

FIGURE 10. Duty Cycle Adjustment

REMOTE SHUTDOWN

The LM1578A may be remotely shutdown by sinking a greater current from the non-inverting input than from the inverting input. This may be accomplished by selecting resistor R3 to be approximately one-half the value of R1 and R2 in parallel.



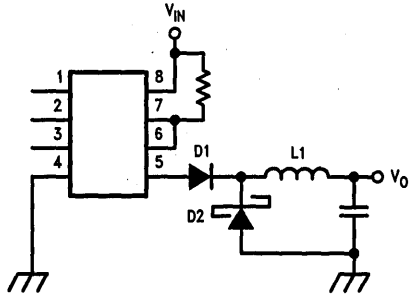
TL/H/8711–24

FIGURE 11. Shutdown Occurs when V_L is High

EMITTER OUTPUT

When the LM1578A output transistor is in the OFF state, if the Emitter output swings below the ground pin voltage, the output transistor will turn ON because its base is clamped near ground. The *Collector Current with Emitter Output Below Ground* curve shows the amount of Collector current drawn in this mode, vs temperature and Emitter voltage. When the Collector-Emitter voltage is high, this current will cause high power dissipation in the output transistor and should be avoided.

This situation can occur in the high-current high-voltage buck application if the Emitter output is used and the catch diode's forward voltage drop is greater than 0.6V. A fast-recovery diode can be added in series with the Emitter output to counter the forward voltage drop of the catch diode (see *Figure 2*). For better efficiency of a high output current buck regulator, an external PNP transistor should be used as shown in *Figure 16.*



TL/H/8711–30

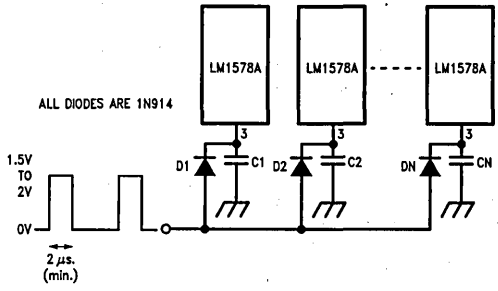
FIGURE 12. D1 Prevents Output Transistor from Improperly Turning ON due to D2's Forward Voltage

Applications Information (Continued)

SYNCHRONIZING DEVICES

When several devices are to be operated at once, their oscillators may be synchronized by the application of an external signal. This drive signal should be a pulse waveform with a minimum pulse width of 2 μs. and an amplitude from 1.5V to 2.0V. The signal source must be capable of 1.) driving capacitive loads and 2.) delivering up to 500 μA for each LM1578A.

Capacitors C1 thru CN are to be selected for a 20% slower frequency than the synchronization frequency.



TL/H/8711–25

FIGURE 13. Synchronizing Devices

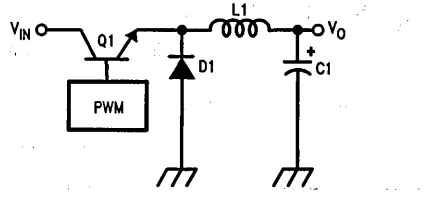
Typical Applications

The LM1578A may be operated in either the continuous or the discontinuous conduction mode. The following applications (except for the Buck-Boost Regulator) are designed for continuous conduction operation. That is, the inductor current is not allowed to fall to zero. This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

BUCK REGULATOR

The buck configuration is used to step an input voltage down to a lower level. Transistor Q1 in *Figure 14* chops the input DC voltage into a squarewave. This squarewave is then converted back into a DC voltage of lower magnitude by the low pass filter consisting of L1 and C1. The duty cycle, D, of the squarewave relates the output voltage to the input voltage by the following equation:

$$V_{out} = D \times V_{in} = V_{in} \times (t_{on})/(t_{on} + t_{off}).$$



TL/H/8711–5

FIGURE 14. Basic Buck Regulator

Figure 15 is a 15V to 5V buck regulator with an output current, I_o, of 350 mA. The circuit becomes discontinuous at 20% of $I_{o(max)}$, has 10 mV of output voltage ripple, an efficiency of 75%, a load regulation of 30 mV (70 mA to 350 mA) and a line regulation of 10 mV ($12 \leq V_{in} \leq 18V$).

Component values are selected as follows:

$R1 = (V_o - 1) \times R2$ where $R2 = 10\ k\Omega$

$R3 = V/I_{sw(max)}$

$R3 = 0.15\Omega$

where:

V is the current limit sense voltage, 0.11V

$I_{sw(max)}$ is the maximum allowable current thru the output transistor.

L1 is the inductor and may be found from the inductance calculation chart (*Figure 16*) as follows:

Given $V_{in} = 15V$ $V_o = 5V$

$I_{o(max)} = 350\ mA$ $f_{OSC} = 50\ kHz$

Discontinuous at 20% of $I_{o(max)}$.

Note that since the circuit will become discontinuous at 20% of $I_{o(max)}$, the load current must not be allowed to fall below 70 mA.

Step 1: Calculate the maximum DC current through the inductor, $I_{L(max)}$. The necessary equations are indicated at the top of the chart and show that $I_{L(max)} = I_{o(max)}$ for the buck configuration. Thus, $I_{L(max)} = 350\ mA$.

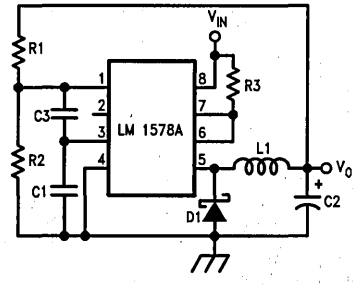
Step 2: Calculate the inductor Volts-sec product, E-T_{op}, according to the equations given from the chart. For the Buck:

$E\text{-}T_{op} = (V_{in} - V_o)(V_o/V_{in})(1000/f_{osc})$

$= (15 - 5)(5/15)(1000/50)$

$= 66V\text{-}\mu s.$

with the oscillator frequency, f_{osc}, expressed in kHz.



$V_{in} = 15V$
$V_o = 5V$
$V_{ripple} = 10\ mV$
$I_o = 350\ mA$
$f_{osc} = 50\ kHz$
$R1 = 40\ k\Omega$
$R2 = 10\ k\Omega$
$R3 = 0.15\Omega$
$C1 = 1820\ pF$
$C2 = 220\ \mu F$
$C3 = 20\ pF$
$L1 = 470\ \mu H$
$D1 = 1N5818$

TL/H/8711–6

FIGURE 15. Buck or Step-Down Regulator

Step 3: Using the graph with axis labeled "Discontinuous At % I_{OUT}" and "$I_{L(max,\ DC)}$" find the point where the desired maximum inductor current, $I_{L(max,\ DC)}$ intercepts the desired discontinuity percentage.

In this example, the point of interest is where the 0.35A line intersects with the 20% line. This is nearly the midpoint of the horizontal axis.

Step 4: This last step is merely the translation of the point found in Step 3 to the graph directly below it. This is accomplished by moving straight down the page to the point which intercepts the desired E-T_{op}. For this example, E-T_{op} is 66V-μs and the desired inductor value is 470 μH. Since this example was for 20% discontinuity, the bottom chart could have been used directly, as noted in step 3 of the chart instructions.

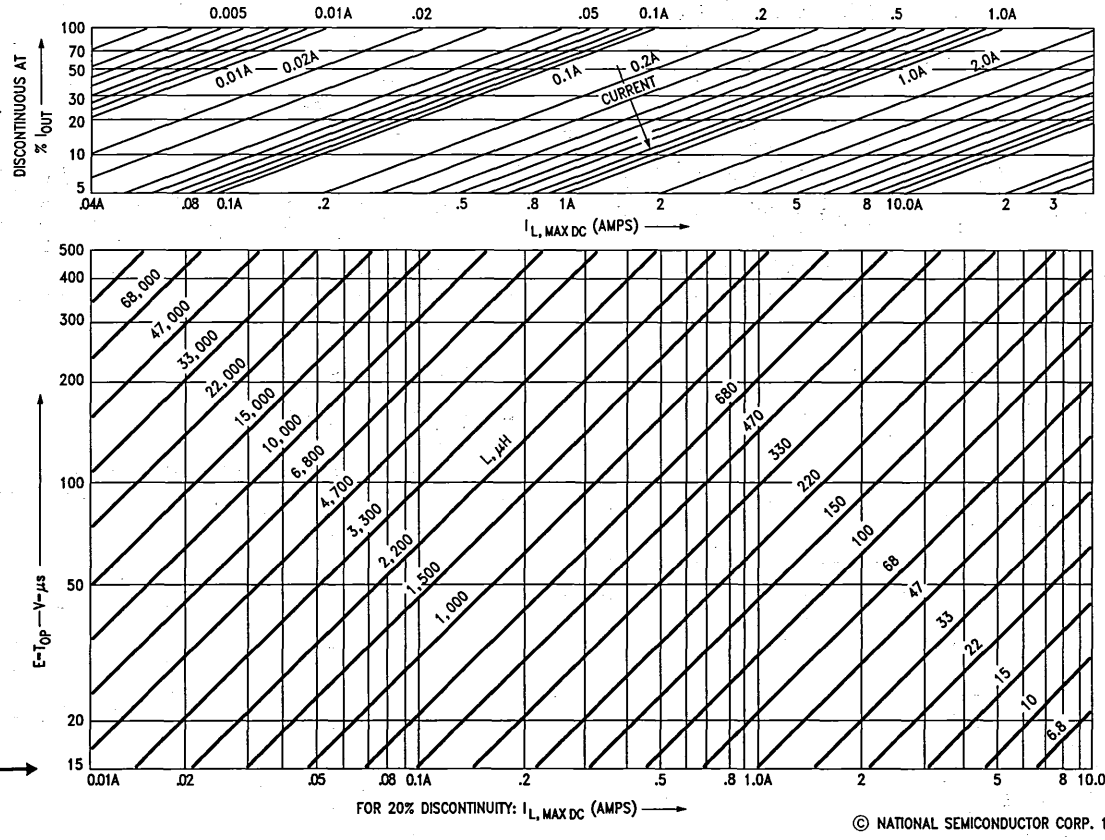
4

Typical Applications (Continued)

HOW TO USE THIS CHART

1. CALCULATE $I_{L,\,MAX\ DC}$ HERE
2. CALCULATE E-T_{OP} HERE
3. ENTER REQUIRED % DISCONTINUITY $= \frac{\Delta I_L \cdot 100\%}{2I_{L,\,MAX\ DC}}$ HERE IF "20%" PROCEED TO (7)
4. PROCEED HORIZONTALLY TO $I_{L,\,MAX\ DC}$ FROM (1)
5. FROM $I_{L,\,MAX\ DC}$ PROCEED VERTICALLY TO E-T_{OP} FROM (2)
6. READ INDUCTANCE VALUE AT E-T_{OP} FOR $I_{L,\,MAX\ DC}$
7. READ $I_{L,\,MAX\ DC}$ FROM (1) HERE
8. READ INDUCTANCE VALUE AT E-T_{OP} FOR $I_{L,\,MAX\ DC}$

BUCK	BOOST	INVERT	
$I_L = I_{LOAD}$	$I_L = I_{LOAD} \frac{V_O}{V_{IN}}$	$I_L = I_{LOAD} \cdot \frac{V_{IN} + \lvert V_O \rvert}{V_{IN}}$	I_L
$(V_{IN} - V_O) \cdot \frac{V_O}{V_{IN}} \cdot \frac{1000}{F, kHz}$	$(V_O - V_{IN}) \cdot \frac{V_{IN}}{V_O} \cdot \frac{1000}{F, kHz}$	$V_{IN} \cdot \frac{\lvert V_O \rvert}{V_{IN} + \lvert V_O \rvert} \cdot \frac{1000}{F, kHz}$	E-T_{OP}



TL/H/8711–31

FIGURE 16. DC/DC Inductance Calculator

Typical Applications (Continued)

For a full line of standard inductor values, contact Pulse Engineering (San Diego, Calif.) regarding their PE526XX series, or A. I. E. Magnetics (Nashville, Tenn.).

A more precise inductance value may be calculated for the Buck, Boost and Inverting Regulators as follows:

BUCK

$L = V_o (V_{in} - V_o)/(\Delta I_L V_{in} f_{osc})$

BOOST

$L = V_{in}^2 (V_o - V_{in})/(\Delta I_L f_{osc} V_o^2)$

INVERT

$L = V_{in}^2 |V_o|/[\Delta I_L (V_{in} + |V_o|)^2 f_{osc}]$

where ΔI_L is the current ripple through the inductor. ΔI_L is usually chosen based on the minimum load current expected of the circuit. For the buck regulator, since the inductor current I_L equals the load current I_O,

$$\Delta I_L = 2 \bullet I_{O(min)}$$

ΔI_L = 140 mA for this circuit. ΔI_L can also be interpreted as

$$\Delta I_L = 2 \bullet (\text{Discontinuity Factor}) \bullet I_L$$

where the Discontinuity Factor is the ratio of the minimum load current to the maximum load current. For this example, the Discontinuity Factor is 0.2.

The remainder of the components of *Figure 15* are chosen as follows:

C1 is the timing capacitor found in *Figure 1*.

$C2 \geq V_o (V_{in} - V_o)/(8 f_{osc}^2 V_{in} V_{ripple} L1)$

where V_{ripple} is the peak-to-peak output voltage ripple.

C3 is necessary for continuous operation and is generally in the 10 pF to 30 pF range.

D1 should be a Schottky type diode, such as the 1N5818 or 1N5819.

BUCK WITH BOOSTED OUTPUT CURRENT

For applications requiring a large output current, an external transistor may be used as shown in *Figure 17*. This circuit steps a 15V supply down to 5V with 1.5A of output current. The output ripple is 50 mV, with an efficiency of 80%, a load regulation of 40 mV (150 mA to 1.5A), and a line regulation of 20 mV ($12V \leq V_{in} \leq 18V$).

Component values are selected as outlined for the buck regulator with a discontinuity factor of 10%, with the addition of R4 and R5:

$R4 = 10 V_{BE1} B_f / I_p$

$R5 = (V_{in} - V - V_{BE1} - V_{sat}) B_f / (I_{L(max, DC)} + I_{R4})$

where:

V_{BE1} is the V_{BE} of transistor Q1.

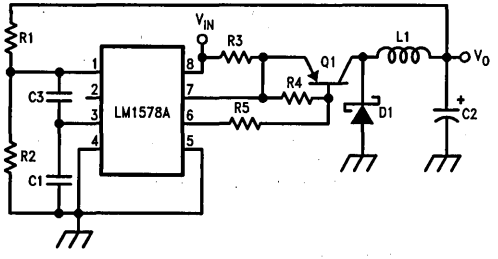
V_{sat} is the saturation voltage of the LM1578A output transistor.

V is the current limit sense voltage.

B_f is the forced current gain of transistor Q1 (B_f = 30 for *Figure 17*).

$I_{R4} = V_{BE1}/R4$

$I_p = I_{L(max, DC)} + 0.5 \Delta I_L$



V_{in} = 15V	R4 = 200Ω
V_o = 5V	R5 = 330Ω
V_{ripple} = 50 mV	C1 = 1820 pF
I_o = 1.5A	C2 = 330 μF
f_{osc} = 50 kHz	C3 = 20 pF
R1 = 40 kΩ	L1 = 220 μH
R2 = 10 kΩ	D1 = 1N5819
R3 = 0.05Ω	Q1 = D45

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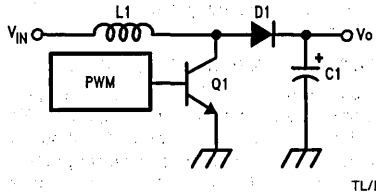
FIGURE 17. Buck Converter with Boosted Output Current

Typical Applications (Continued)

BOOST REGULATOR

The boost regulator converts a low input voltage into a higher output voltage. The basic configuration is shown in *Figure 18*. Energy is stored in the inductor while the transistor is on and then transferred with the input voltage to the output capacitor for filtering when the transistor is off. Thus,

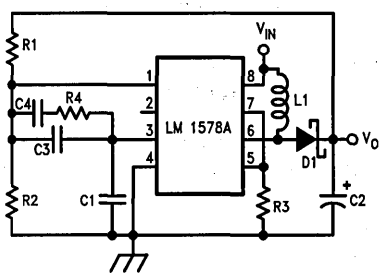
$$V_o = V_{in} + V_{in}(t_{on}/t_{off}).$$



TL/H/8711–9

FIGURE 18. Basic Boost Regulator

The circuit of *Figure 19* converts a 5V supply into a 15V supply with 150 mA of output current, a load regulation of 14 mV (30 mA to 150 mA), and a line regulation of 35 mV ($4.5V \leq V_{in} \leq 8.5V$).



V_{in} = 5V
V_o = 15V
V_{ripple} = 10 mV
I_o = 150 mA
f_{osc} = 50 kHz
R1 = 140 kΩ
R2 = 10 kΩ
R3 = 0.1Ω
R4 = 220 kΩ
C1 = 1820 pF
C2 = 470 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 330 μH
D1 = 1N5818

TL/H/8711–11

FIGURE 19. Boost or Step-Up Regulator

$R1 = (V_o - 1)\,R2$ where $R2 = 10\,k\Omega$.

$R3 = V/(I_{L(max,\,DC)} + 0.5\,\Delta I_L)$

where:

$\Delta I_L = 2(I_{LOAD(min)})(V_o/V_{in})$

R4, C3 and C4 are necessary for continuous operation and are typically 220 kΩ, 20 pF, and 0.0022 μF respectively.

C1 is the timing capacitor found in *Figure 1*.

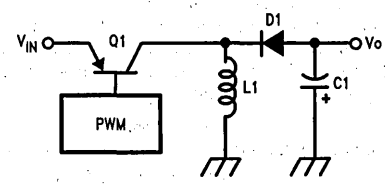
$C2 \geq I_o\,(V_o - V_{in})/(f_{osc}\,V_o\,V_{ripple})$.

D1 is a Schottky type diode such as a IN5818 or IN5819.

L1 is found as described in the buck converter section.

INVERTING REGULATOR

Figure 20 shows the basic configuration for an inverting regulator. The input voltage is of a positive polarity, but the output is negative. The output may be less than, equal to, or greater in magnitude than the input. The relationship between the magnitude of the input voltage and the output voltage is $V_o = V_{in} \times (t_{on}/t_{off})$.



TL/H/8711–10

FIGURE 20. Basic Inverting Regulator

Figure 21 shows an LM1578A configured as a 5V to −15V polarity inverter with an output current of 300 mA, a load regulation of 44 mV (60 mA to 300 mA) and a line regulation of 50 mV ($4.5V \leq V_{in} \leq 8.5V$).

$R1 = (|V_o| + 1)\,R2$ where $R2 = 10\,k\Omega$.

$R3 = V/(I_{L(max,\,DC)} + 0.5\,\Delta I_L)$.

$R4 = 10V_{BE1}B_f/(I_{L\,(max,\,DC)} + 0.5\,\Delta I_L)$

where:

V, V_{BE1}, V_{sat}, and B_f are defined in the "Buck Converter with Boosted Output Current" section.

$\Delta I_L = 2(I_{LOAD(min)})(V_{in} + |V_o|)/V_{IN}$

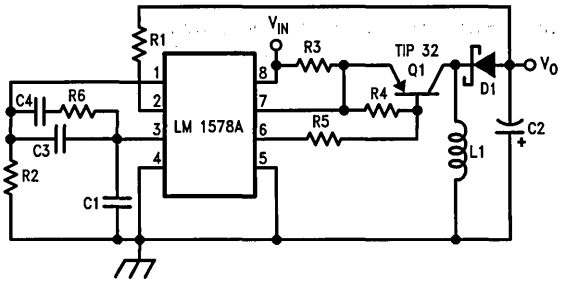
R5 is defined in the "Buck with Boosted Output Current" section.

R6 serves the same purpose as R4 in the Boost Regulator circuit and is typically 220 kΩ.

C1, C3 and C4 are defined in the "Boost Regulator" section.

$C2 \geq I_o\,|V_o|/[f_{osc}(|V_o| + V_{in})\,V_{ripple}]$

L1 is found as outlined in the section on buck converters, using the inductance chart for the invert configuration and 20% discontinuity.



V_{in} = 5V
V_o = −15V
V_{ripple} = 5 mV
I_o = 300 mA, I_{min} = 60 mA
f_{osc} = 50 kHz
R1 = 160 kΩ R2 = 10 kΩ
R3 = 0.01 Ω R4 = 190Ω
R5 = 82Ω R6 = 220 kΩ
C1 = 1820 pF
C2 = 1000 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 150 μH
D1 = 1N5818

TL/H/8711–12

FIGURE 21. Inverting Regulator

Typical Applications (Continued)

BUCK-BOOST REGULATOR

The Buck-Boost Regulator, shown in *Figure 22*, may step a voltage up or down, depending upon whether or not the desired output voltage is greater or less than the input voltage. In this case, the output voltage is 12V with an input voltage from 9V to 15V. The circuit exhibits an efficiency of 75%, with a load regulation of 60 mV (10 mA to 100 mA) and a line regulation of 52 mV.

$R1 = (V_o - 1)\,R2$ where $R2 = 10\,k\Omega$

$R3 = V/0.75A$

R4, C1, C3 and C4 are defined in the "Boost Regulator" section.

D1 and D2 are Schottky type diodes such as the 1N5818 or 1N5819.

$$C2 \geq \frac{(I_o/V_{ripple})(V_o + 2V_d)}{[f_{osc}(V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})]}$$

where:

V_d is the forward voltage drop of the diodes.

V_{sat} is the saturation voltage of the LM1578A output transistor.

V_{sat1} is the saturation voltage of transistor Q1.

$$L1 \geq (V_{in} - V_{sat} - V_{sat1})(t_{on}/I_p)$$

where:

$$t_{on} = \frac{(1/f_{osc})(V_o + 2V_d)}{(V_o + V_{in} + 2V_d - V_{sat} - V_{sat1})}$$

$$I_p = \frac{2I_o(V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})}{(V_{in} - V_{sat} - V_{sat1})}$$

RS-232 LINE DRIVER POWER SUPPLY

The power supply, shown in *Figure 23*, operates from an input voltage as low as 4.2V (5V nominal), and delivers an output of ±12V at ±40 mA with better than 70% efficiency. The circuit provides a load regulation of ±150 mV (from 10% to 100% of full load) and a line regulation of ±10 mV. Other notable features include a cycle-by-cycle current limit and an output voltage ripple of less than 40 mVp-p.

A unique feature of this circuit is its use of feedback from both outputs. This dual feedback configuration results in a sharing of the output voltage regulation by each output so that neither side becomes unbalanced as in single feedback systems. In addition, since both sides are regulated, it is not necessary to use a linear regulator for output regulation.

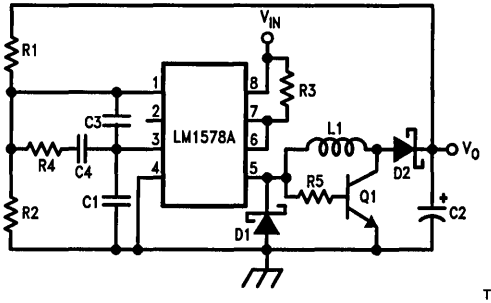
The feedback resistors, R2 and R3, may be selected as follows by assuming a value of 10 kΩ for R1;

$R2 = (V_o - 1V)/45.8\,\mu A = 240\,k\Omega$

$R3 = (|V_o| + 1V)/54.2\,\mu A = 240\,k\Omega$

Actually, the currents used to program the values for the feedback resistors may vary from 40 μA to 60 μA, as long as their sum is equal to the 100 μA necessary to establish the 1V threshold across R1. Ideally, these currents should be equal (50 μA each) for optimal control. However, as was done here, they may be mismatched in order to use standard resistor values. This results in a slight mismatch of regulation between the two outputs.

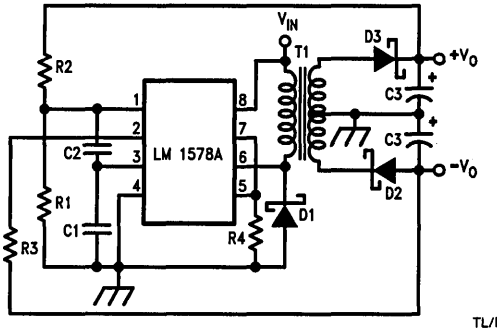
The current limit resistor, R4, is selected by dividing the current limit threshold voltage by the maximum peak current level in the output switch. For our purposes R4 = 90 mV/750 mA = 0.12Ω. A value of 0.1Ω was used.



$9V \leq V_{in} \leq 15V$
$V_o = 12V$
$I_o = 100\,mA$
$V_{ripple} = 50\,mV$
$f_{osc} = 50\,kHz$
R1 = 110 k
R2 = 10 k
R3 = 0.1
R4 = 220 k
R5 = 270
C1 = 1820 pF
C2 = 220 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 220 μH
D1, D2 = 1N5819
Q1 = D44

TL/H/8711–13

FIGURE 22. Buck-Boost Regulator



$V_{in} = 5V$
$V_o = \pm 12V$
$I_o = \pm 40\,mA$
$f_{osc} = 80\,kHz$
R1 = 10 kΩ
R2 = 240 kΩ
R3 = 240 kΩ
R4 = 0.1 Ω
C1 = 820 pF
C2 = 10 pF
C3 = 220 μF
D1, D2, D3 = 1N5819
T1 = PE-64287

TL/H/8711–14

FIGURE 23. RS-232 Line Driver Power Supply

Typical Applications (Continued)

Capacitor C1 sets the oscillator frequency and is selected from *Figure 1*.

Capacitor C2 serves as a compensation capacitor for synchronous operation and a value of 10 to 50 pF should be sufficient for most applications.

A minimum value for an ideal output capacitor C3, could be calculated as $C = I_o \times t/\Delta V$ where I_o is the load current, t is the transistor on time (typically $0.4/f_{osc}$), and ΔV is the peak-to-peak output voltage ripple. A larger output capacitor than this theoretical value should be used since electrolytics have poor high frequency performance. Experience has shown that a value from 5 to 10 times the calculated value should be used.

For good efficiency, the diodes must have a low forward voltage drop and be fast switching. 1N5819 Schottky diodes work well.

Transformer selection should be picked for an output transistor "on" time of $0.4/f_{osc}$, and a primary inductance high enough to prevent the output transistor switch from ramping higher than the transistor's rating of 750 mA. Pulse Engineering (San Diego, Calif.) and Renco Electronics, Inc. (Deer Park, N.Y.) can provide further assistance in selecting the proper transformer for a specific application need. The transformer used in *Figure 23* was a Pulse Engineering PE-64287.

National Semiconductor

LP2950/LP2950AC/LP2950C 5V and LP2951/LP2951AC/LP2951C Adjustable Micropower Voltage Regulators

General Description

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75 μA typ.) and very low dropout voltage (typ. 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950 in the popular 3-pin TO-92 package is pin-compatible with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V output or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

Features

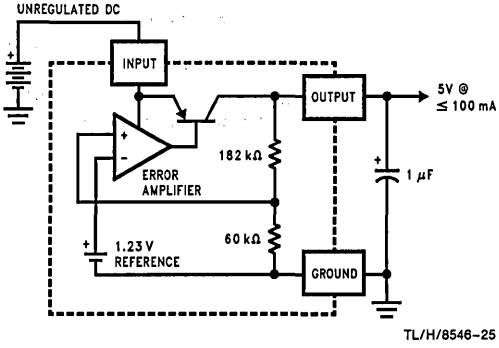
- High accuracy 5V, guaranteed 100 mA output
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs only 1 μF for stability
- Current and Thermal Limiting

LP2951 versions only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

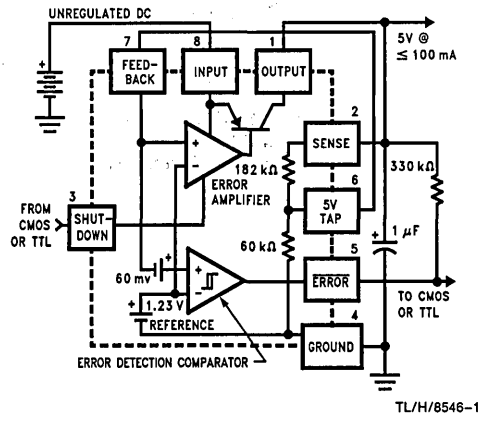
Block Diagram and Typical Applications

LP2950



TL/H/8546-25

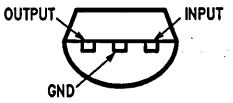
LP2951



TL/H/8546-1

Connection Diagrams and Ordering Information

TO-92 Plastic Package (Z)

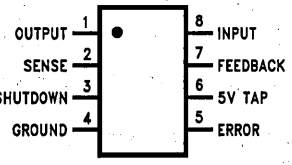


TL/H/8546-2

Bottom View

Order Number LP2950ACZ-5.0 or LP2950CZ-5.0
See NS Package Number Z03A

Dual-In-Line Packages (N, J)
Surface-Mount Package (M)



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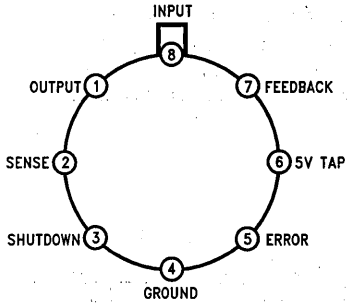
Top View

Order Number LP2951CJ, LP2951ACJ, LP2951J, LP2951J/883 or 5962-3870501MPA
See NS Package Number J08A

Order Number LP2951ACN or LP2951CN
See NS Package Number N08E

Order Number LP2951ACM or LP2951CM
See NS Package Number M08A

Metal Can Package (H)

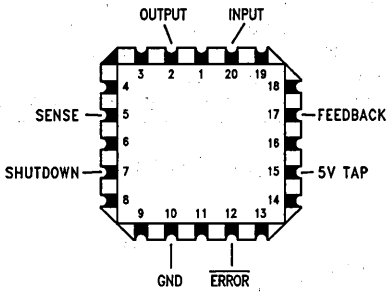


TL/H/8546-19

Top View

Order Number LP2951H, LP2951H/883 or 5962-3870501MGA
See NS Package Number H08C

Leadless Chip Carrier (E)



TL/H/8546-24

Top View

Order Number LP2951E/883 or 5962-3870501M2A
See NS Package Number E20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Lead Temp. (Soldering, 5 seconds)	260°C
Storage Temperature Range	−65° to +150°C
Operating Junction Temperature Range (Note 8)	
LP2951	−55° to +150°C
LP2950AC/LP2950C, LP2951AC/LP2951C	−40° to +125°C
Input Supply Voltage	−0.3 to +30V
Feedback Input Voltage (Notes 9 and 10)	−1.5 to +30V
Shutdown Input Voltage (Note 9)	−0.3 to +30V
Error Comparator Output Voltage (Note 9)	−0.3 to +30V

ESD Rating is to be determined.

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 2)	LP2951		LP2950AC LP2951AC			LP2950C LP2951C			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
Output Voltage	T_J = 25°C	5.0	5.025 4.975	5.0	5.025 4.975		5.0	5.05 4.95		V max V min
	−25°C ≤ T_J ≤ 85°C					5.05 4.95			5.075 4.925	V max V min
	Full Operating Temperature Range		**5.06** **4.94**			**5.06** **4.94**			**5.1** **4.9**	V max V min
Output Voltage	100 μA ≤ I_L ≤ 100 mA T_J ≤ $T_{J_{MAX}}$		**5.075** **4.925**			**5.07** **4.93**			**5.12** **4.88**	V max V min
Output Voltage Temperature Coefficient	(Note 12)	**20**	**120**	**20**		**100**	**50**		**150**	ppm/°C
Line Regulation (Note 14)	6V ≤ V_{in} ≤ 30V (Note 15)	0.03	0.1 **0.5**	0.03	0.1	**0.2**	0.04	0.2	**0.4**	% max % max
Load Regulation (Note 14)	100 μA ≤ I_L ≤ 100 mA	0.04	0.1 **0.3**	0.04	0.1	**0.2**	0.1	0.2	**0.3**	% max % max
Dropout Voltage (Note 5)	I_L = 100 μA	50	80 **150**	50	80	**150**	50	80	**150**	mV max mV max
	I_L = 100 mA	380	450 **600**	380	450	**600**	380	450	**600**	mV max mV max
Ground Current	I_L = 100 μA	75	120 **140**	75	120	**140**	75	120	**140**	μA max μA max
	I_L = 100 mA	8	12 **14**	8	12	**14**	8	12	**14**	mA max mA max
Dropout Ground Current	V_{in} = 4.5V I_L = 100 μA	110	170 **200**	110	170	**200**	110	170	**200**	μA max μA max
Current Limit	V_{out} = 0	160	200 **220**	160	200	**220**	160	200	**220**	mA max mA max
Thermal Regulation	(Note 13)	0.05	0.2	0.05	0.2		0.05	0.2		%/W max
Output Noise, 10 Hz to 100 KHz	C_L = 1 μF	430		430			430			μV rms
	C_L = 200 μF	160		160			160			μV rms
	C_L = 3.3 μF (Bypass = 0.01 μF Pins 7 to 1 (LP2951))	100		100			100			μV rms
8-Pin Versions only		**LP2951**		**LP2951AC**			**LP2951C**			
Reference Voltage		1.235	1.25 **1.26** 1.22 **1.2**	1.235	1.25 1.22	**1.26** **1.2**	1.235	1.26 1.21	**1.27** **1.2**	V max V max V min V min
Reference Voltage	(Note 7)		**1.27** **1.19**			**1.27** **1.19**			**1.285** **1.185**	V max V min

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 2)	LP2951		LP2951AC			LP2951C			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
8-Pin Versions only (Continued)										
Feedback Pin Bias Current		20	40 **60**	20	40	**60**	20	40	**60**	nA max nA max
Reference Voltage Temperature Coefficient	(Note 12)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C
Error Comparator										
Output Leakage Current	V_{OH} = 30V	0.01	1 **2**	0.01	1	**2**	0.01	1	**2**	μA max μA max
Output Low Voltage	V_{in} = 4.5V I_{OL} = 400 μA	150	250 **400**	150	250	**400**	150	250	**400**	mV max mV max
Upper Threshold Voltage	(Note 6)	60	40 **25**	60	40	**25**	60	40	**25**	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 **140**	75	95	**140**	75	95	**140**	mV max mV max
Hysteresis	(Note 6)	15		15			15			mV
Shutdown Input										
Input Logic Voltage	Low (Regulator ON) High (Regulator OFF)	1.3	**0.6** **2.0**	1.3		**0.7** **2.0**	1.3		**0.7** **2.0**	V V max V min
Shutdown Pin Input Current	$V_{shutdown}$ = 2.4V	30	50 **100**	30	50	**100**	30	50	**100**	μA max μA max
	$V_{shutdown}$ = 30V	450	600 **750**	450	600	**750**	450	600	**750**	μA max μA max
Regulator Output Current in Shutdown	(Note 11)	3	10 **20**	3	10	**20**	3	10	**20**	μA max μA max

Note 1: Boldface limits apply at temperature extremes.

Note 2: Unless otherwise specified all limits guaranteed for T_J = 25°C, V_{in} = 6V, I_L = 100 μA and C_L = 1 μF. Additional conditions for the 8-pin versions are Feedback tied to 5V Tap and Output tied to Output Sense (V_{out} = 5V) and $V_{shutdown} \leq 0.8V$.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V **(2.3V over temperature)** must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{out}/V_{ref} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV × 5V/1.235V = 384 mV. Thresholds remain constant as a percent of V_{out} as V_{out} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: $V_{ref} \leq V_{out} \leq (V_{in} - 1V)$, $2.3V \leq V_{in} \leq 30V$, $100\ \mu A \leq I_L \leq 100$ mA, $T_J \leq T_{JMAX}$.

Note 8: The junction-to-ambient thermal resistance of the TO-92 package is 180°C/W with 0.4" leads and 160°C/W with 0.25" leads to a PC board. The thermal resistance of the 8-pin DIP packages is 105°C/W for the molded plastic (N) and 130°C/W for the cerdip (J) junction to ambient when soldered directly to a PC board. Thermal resistance for the metal can (H) is 160°C/W junction to ambient and 20°C/W junction to case. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W. Thermal resistance for the leadless chip carrier (E) package is 95°C/W junction to ambient and 24°C/W junction to case.

Note 9: May exceed input supply voltage.

Note 10: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 11: $V_{shutdown} \geq 2V$, $V_{in} \leq 30V$, V_{out} = 0, Feedback pin tied to 5V Tap.

Note 12: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 13: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10 ms.

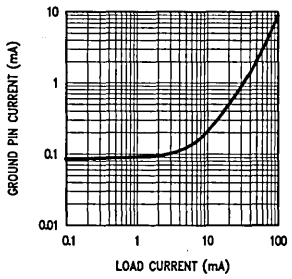
Note 14: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 15: Line regulation for the LP2951 is tested at 150°C for I_L = 1 mA. For I_L = 100 μA and T_J = 125°C, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

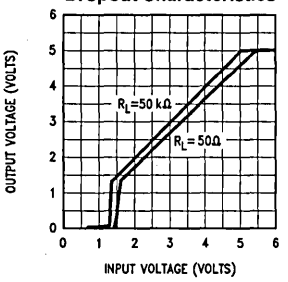
Note 16: A Military RETS spec is available on request. At time of printing, the LP2951 RETS spec complied with the boldface limits in this column. The LP2951H, E, or J may also be procured as Standard Military Drawing Spec #5962-3870501MGA, M2A, or MPA.

Typical Performance Characteristics

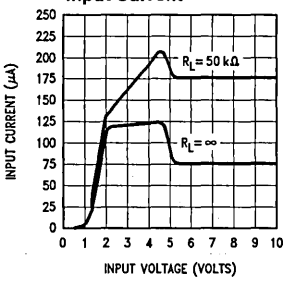
Quiescent Current



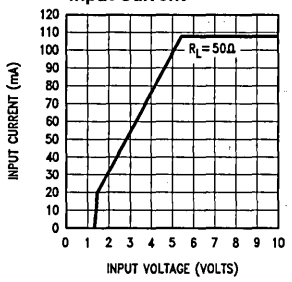
Dropout Characteristics



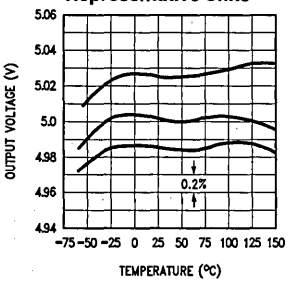
Input Current



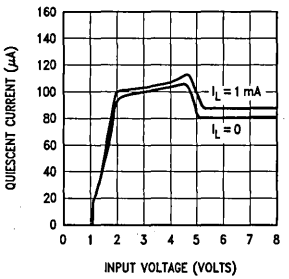
Input Current



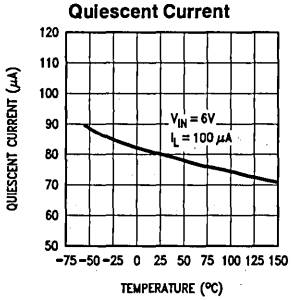
Output Voltage vs. Temperature of 3 Representative Units



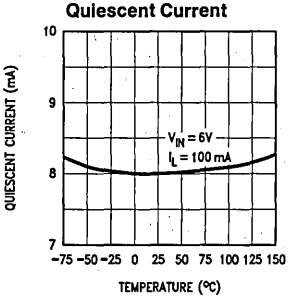
Quiescent Current



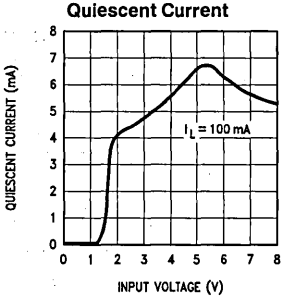
Quiescent Current



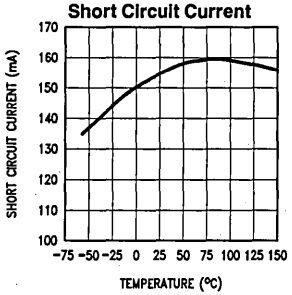
Quiescent Current



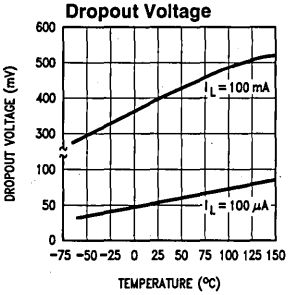
Quiescent Current



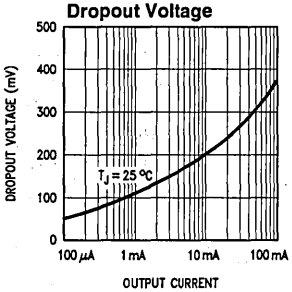
Short Circuit Current



Dropout Voltage



Dropout Voltage



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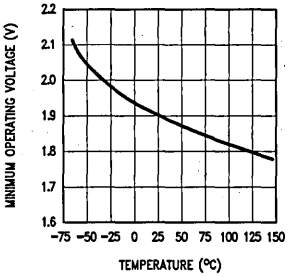
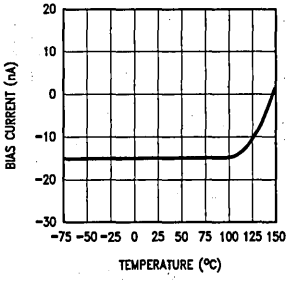
Typical Performance Characteristics (Continued)

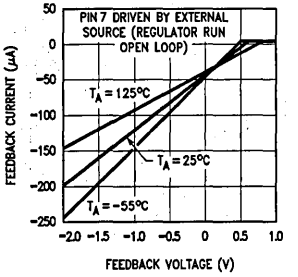
LP2951
Minimum Operating Voltage



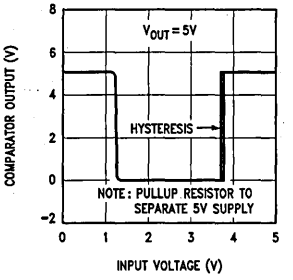
LP2951
Feedback Bias Current



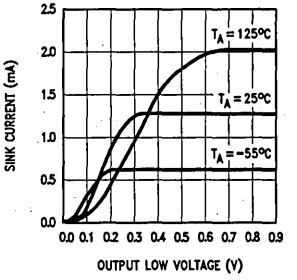
LP2951
Feedback Pin Current



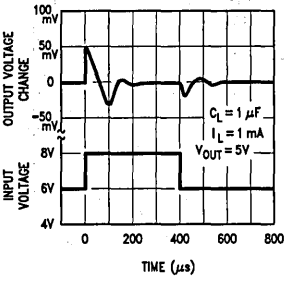
LP2951
Error Comparator Output



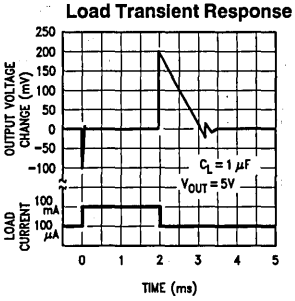
LP2951
Comparator Sink Current



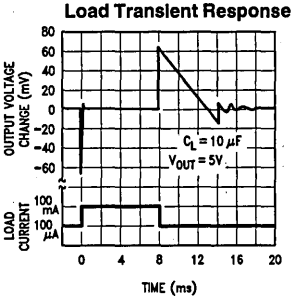
Line Transient Response



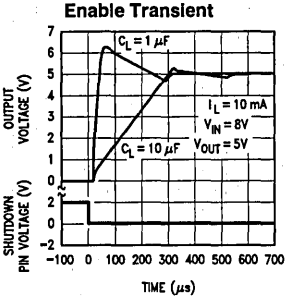
Load Transient Response



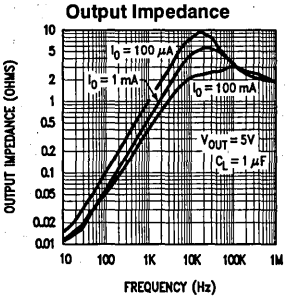
Load Transient Response



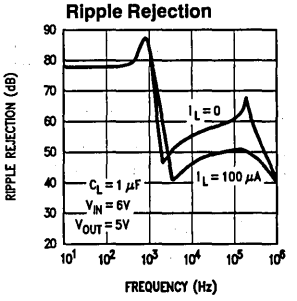
LP2951
Enable Transient



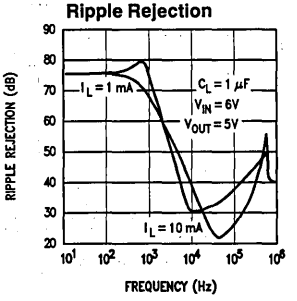
Output Impedance



Ripple Rejection



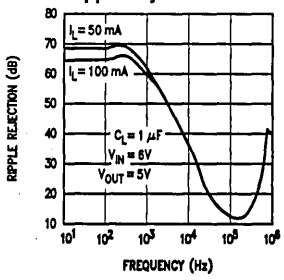
Ripple Rejection



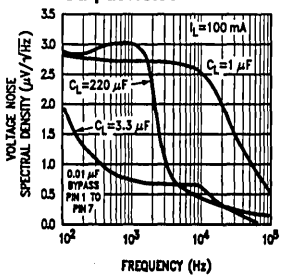
TL/H/8546–4

Typical Performance Characteristics (Continued)

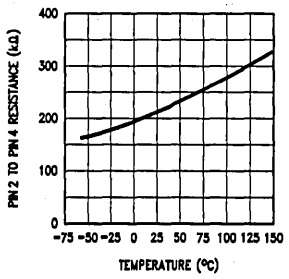
Ripple Rejection



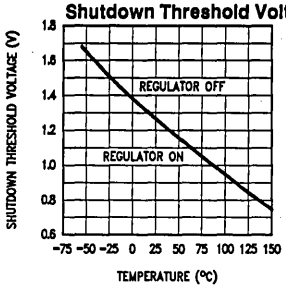
Output Noise



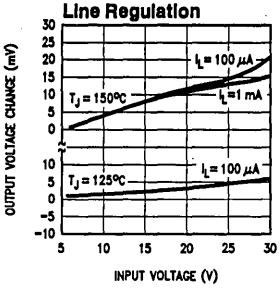
LP2951 Divider Resistance



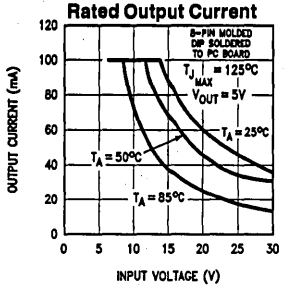
Shutdown Threshold Voltage



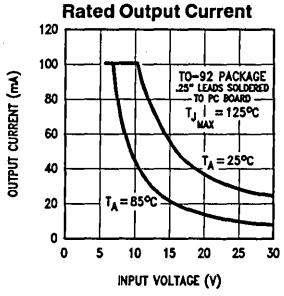
Line Regulation



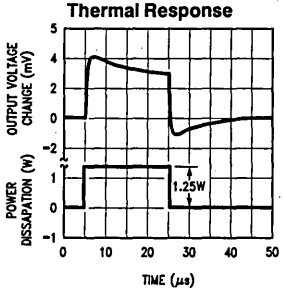
LP2951 Maximum Rated Output Current



LP2950 Maximum Rated Output Current



Thermal Response



TL/H/8546–5

Application Hints

EXTERNAL CAPACITORS

A 1.0 µF (or greater) capacitor is required between the LP2950/LP2951 output and ground for stability. Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 µF for currents below 10 mA or 0.1 µF for currents below 1 mA. Using the 8-Pin versions at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a 3.3 µF (or greater) capacitor should be used.

Unlike many other regulators, the LP2950 will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951 version with external resistors, a minimum load of 1 µA is recommended.

A 1 µF tantalum or aluminum electrolytic capacitor should be placed from the LP2950/LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the LP2951 Feedback terminal (pin 7) can cause instability. This may especially be a problem

Application Hints (Continued)

when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3 μF will fix this problem.

ERROR DETECTION COMPARATOR OUTPUT

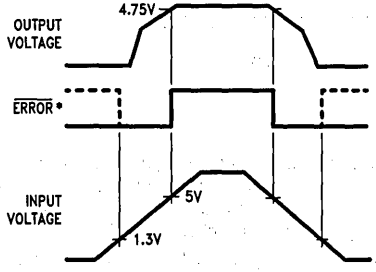
The comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60 mV divided by the 1.235 reference voltage. (Refer to the block diagram in the front of the datasheet.) This trip level remains "5% below normal" regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the LP2951's dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the 5V output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 μA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 MΩ. The resistor is not required if this output is unused.

PROGRAMMING THE OUTPUT VOLTAGE (LP2951)

The LP2951 may be pin-strapped for 5V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5V Tap). Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in *Figure 2,* an external pair of resistors is required.



TL/H/8546-20

*When $V_{IN} \leq$ 1.3V, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see *Figure 2*), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

FIGURE 1. $\overline{\text{ERROR}}$ Output Timing

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally −20 nA. The minimum recommended load current of 1 μA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 μA. Since the LP2951 typically draws 60 μA at no load with Pin 2 open-circuited, this is a small price to pay.

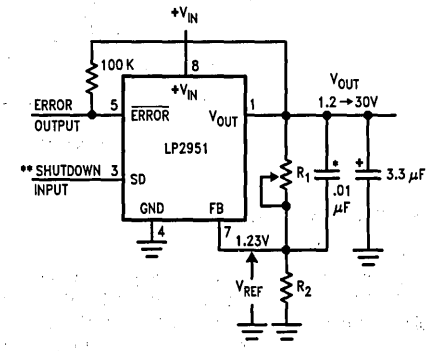
REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP2950 but is relatively inefficient, as increasing the capacitor from 1 μF to 220 μF only decreases the noise from 430 μV to 160 μV rms for a 100 kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ \text{Hz}}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 100 μV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.



TL/H/8546-7

FIGURE 2. Adjustable Regulator

*See Application Hints

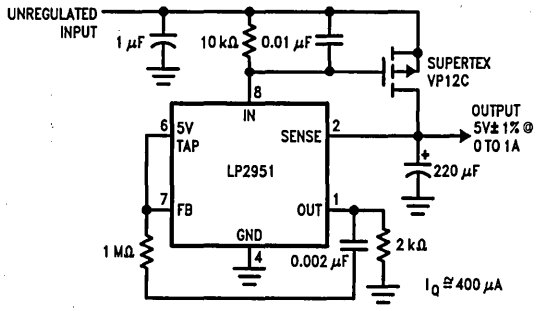
$$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

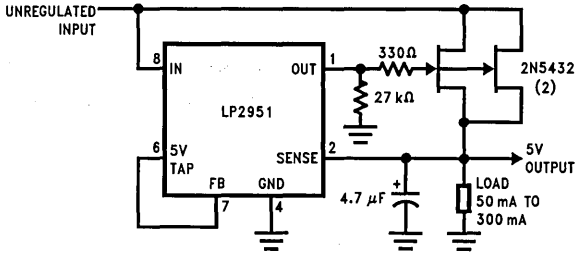
Typical Applications

1A Regulator with 1.2V Dropout



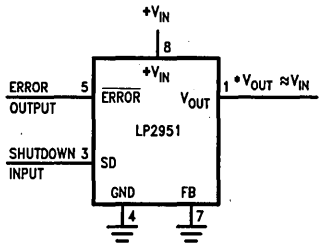
TL/H/8546-22

300 mA Regulator with 0.75V Dropout



TL/H/8546-21

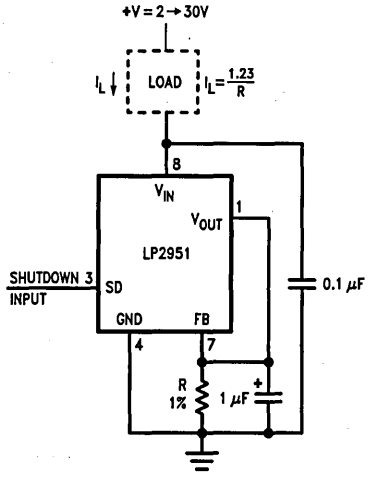
Wide Input Voltage Range Current Limiter



TL/H/8546-9

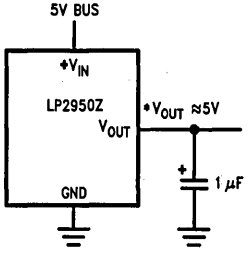
*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Low Drift Current Source



TL/H/8546-8

5 Volt Current Limiter

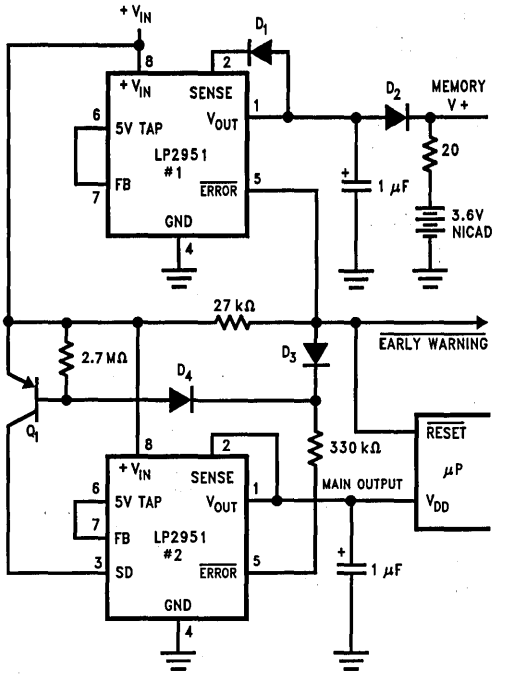


TL/H/8546-10

*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Typical Applications (Continued)

Regulator with Early Warning and Auxiliary Output

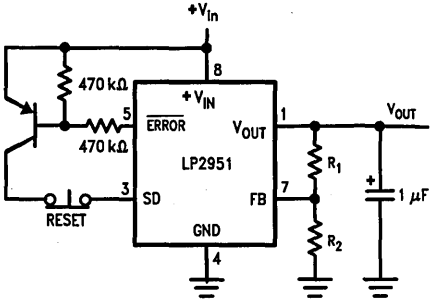


TL/H/8546–11

- Early warning flag on low input voltage
- Main output latches off at lower input voltages
- Battery backup on auxiliary output

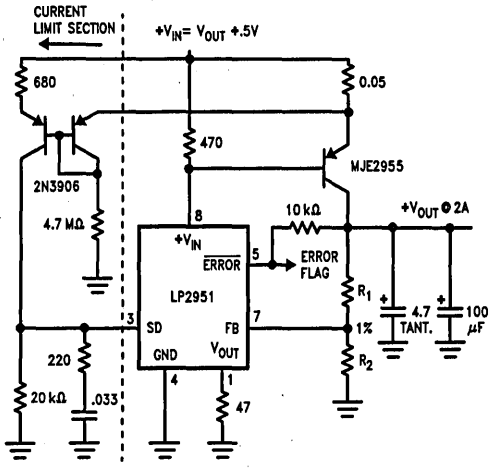
Operation: Reg. #1's V_{out} is programmed one diode drop above 5V. Its error flag becomes active when $V_{in} \leq 5.7V$. When V_{in} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When V_{in} again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

Latch Off When Error Flag Occurs



TL/H/8546–12

2 Ampere Low Dropout Regulator

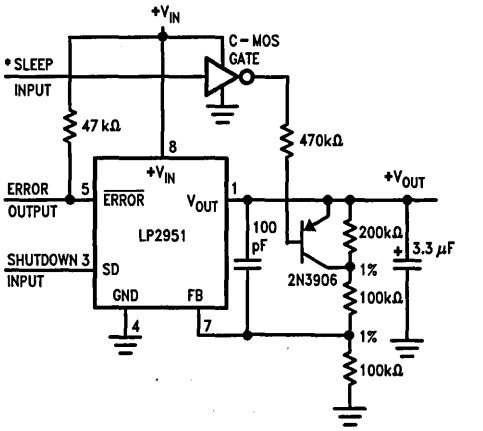


$V_{out} = 1.23V \left(1 + \frac{R_1}{R_2}\right)$

TL/H/8546–13

For 5V_{out}, use internal resistors. Wire pin 6 to 7, & wire pin 2 to +V_{out} Buss.

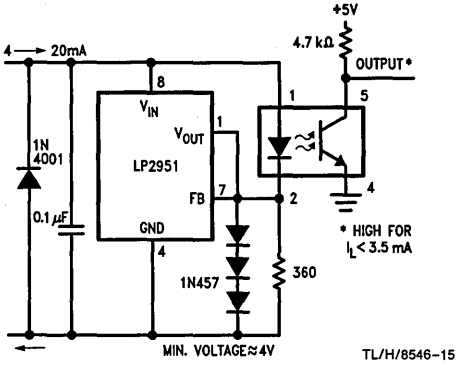
5V Regulator with 2.5V Sleep Function



*High input lowers V_{out} to 2.5V

TL/H/8546–14

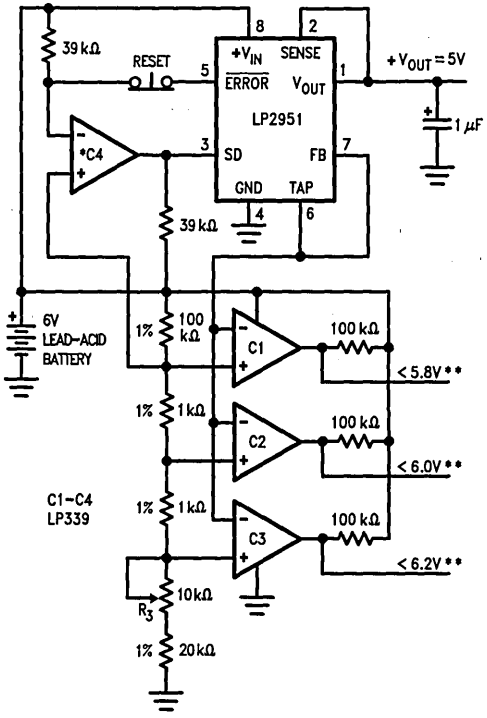
Open Circuit Detector for 4 → 20 mA Current Loop



TL/H/8546–15

Typical Applications (Continued)

Regulator with State-of-Charge Indicator



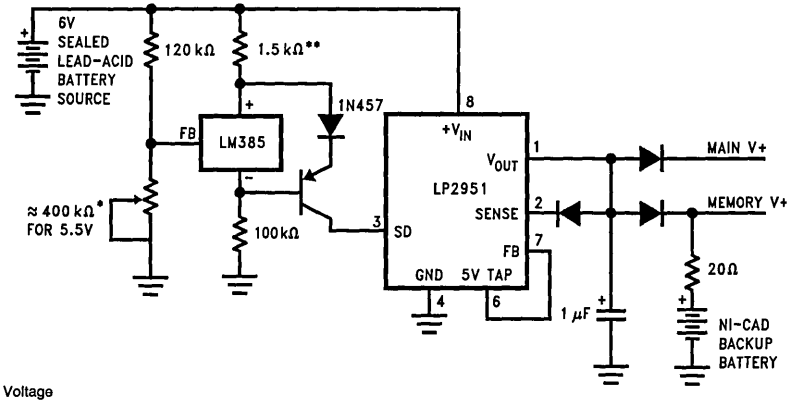
TL/H/8546–16

*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V.

**Outputs go low when V_{in} drops below designated thresholds.

Low Battery Disconnect

For values shown, Regulator shuts down when V_{in} < 5.5V and turns on again at 6.0V. Current drain in disconnected mode is ≈ 150 µA.



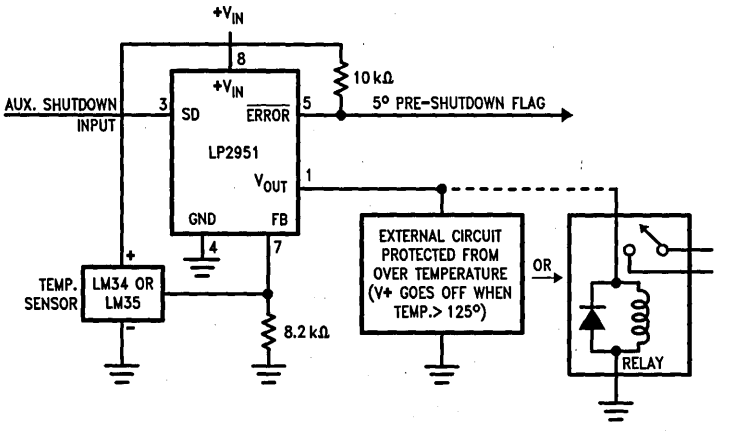
TL/H/8546–17

*Sets disconnect Voltage

**Sets disconnect Hysteresis

Typical Applications (Continued)

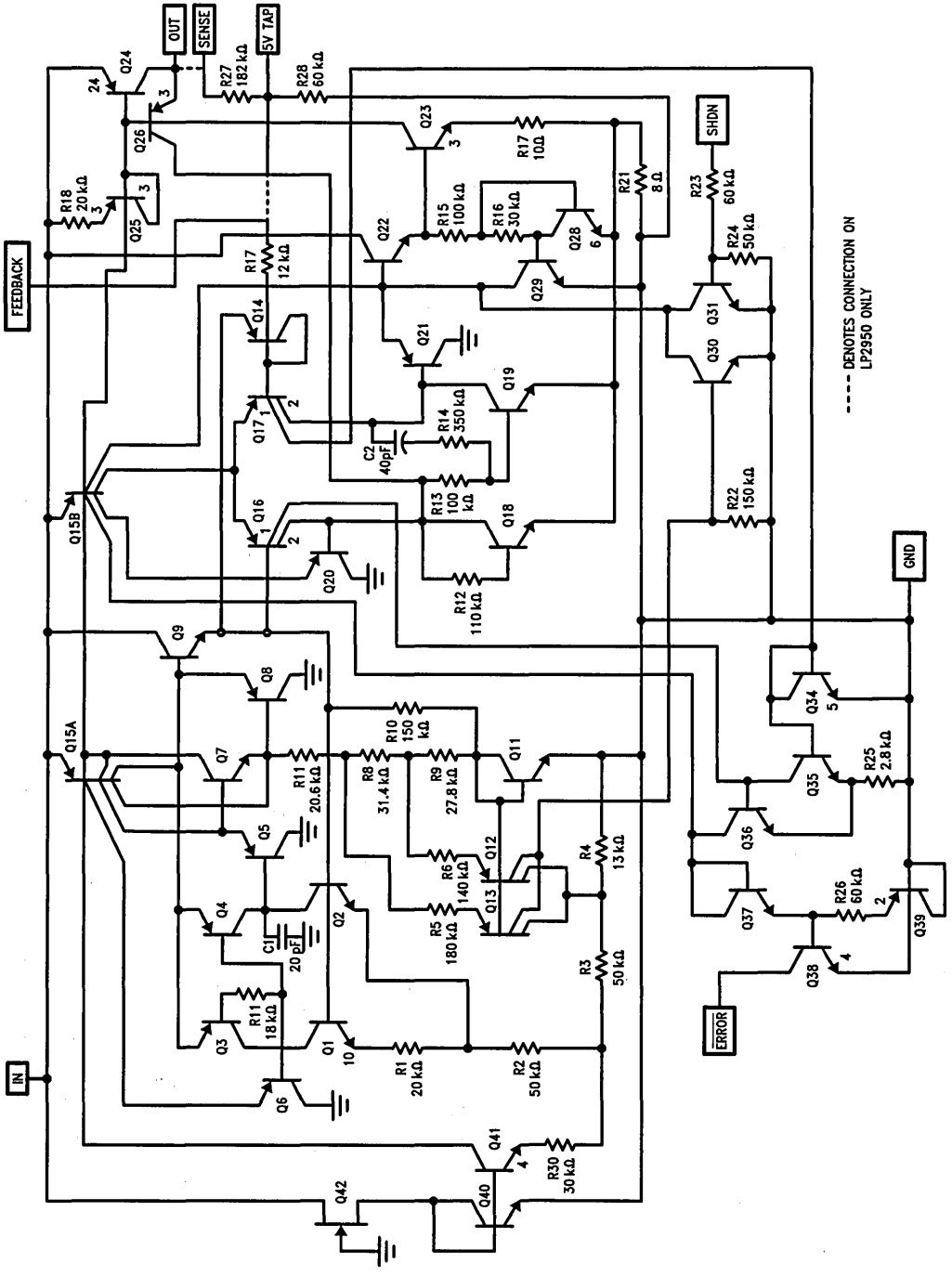
System Overtemperature Protection Circuit



TL/H/8546–18

LM34 for 125°F Shutdown
LM35 for 125°C Shutdown

Schematic Diagram



TL/H/8546–23

4

National Semiconductor

LP2952/LP2952A/LP2953/LP2953A
Adjustable Micropower Low-Dropout Voltage Regulators

General Description

The LP2952 and LP2953 are micropower voltage regulators with very low quiescent current (130 μA typical at 1 mA load) and very low dropout voltage (typ. 60 mV at light load and 470 mV at 250 mA load current). They are ideally suited for battery-powered systems. Furthermore, the quiescent current increases only slightly at dropout, which prolongs battery life.

The LP2952 and LP2953 retain all the desirable characteristics of the LP2951, but offer increased output current, additional features, and an improved shutdown function.

The internal crowbar pulls the output down quickly when the shutdown is activated.

The error flag goes low if the output voltage drops out of regulation.

Reverse battery protection is provided.

The internal voltage reference is made available for external use, providing a low-T.C. reference with very good line and load regulation.

The parts are available in plastic DIP and surface mount packages.

Features

- Output voltage adjusts from 1.23V to 29V
- Guaranteed 250 mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight line and load regulation
- Very low temperature coefficient
- Current and thermal limiting
- Reverse battery protection
- 50 mA (typical) output pulldown crowbar

LP2953 Versions Only

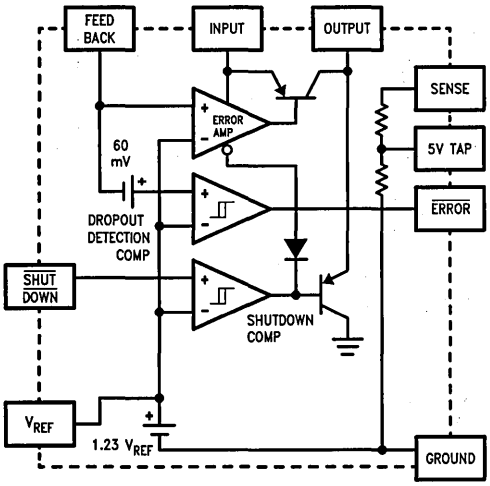
- Auxiliary comparator included with CMOS/TTL compatible output levels. Can be used for fault detection, low input line detection, etc.

Applications

- High-efficiency linear regulator
- Regulator with under-voltage shutdown
- Low dropout battery-powered regulator
- Snap-ON/Snap-OFF regulator

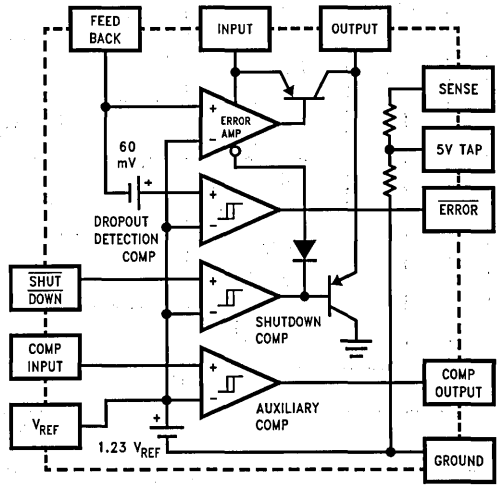
Block Diagrams

LP2952



TL/H/11127–1

LP2953



TL/H/11127–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	
LP2952AI/LP2952I	−40°C to +125°C
LP2953AI/LP2953I	−40°C to +125°C
Lead Temp. (Soldering, 5 seconds)	260°C
Power Dissipation (Note 2)	Internally Limited
Input Supply Voltage	−20V to +30V
Feedback Input Voltage (Note 3)	−0.3V to +5V
Comparator Input Voltage (Note 4)	−0.3V to +30V
Shutdown Input Voltage (Note 4)	−0.3V to +30V
Comparator Output Voltage (Note 4)	−0.3V to +30V
ESD Rating (Note 15)	2 kV

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the −40°C to +125°C junction temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQL) methods. Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, Feedback pin is tied to 5V Tap pin, Output pin is tied to Output Sense pin, V_{OUT} = 5V.

Symbol	Parameter	Conditions	Typical	2952AI 2953AI		2952I 2953I		Units
				Min	Max	Min	Max	
V_O	Output Voltage		5.0	4.975 **4.940**	5.025 **5.060**	4.950 **4.900**	5.050 **5.100**	V
		1 mA ≤ I_L ≤ 250 mA	5.0	**4.930**	**5.070**	**4.880**	**5.120**	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temp. Coefficient	(Note 5)	**20**		**100**		**150**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Output Voltage Line Regulation	V_{IN} = 6V to 30V	0.03		0.1 **0.2**		0.2 **0.4**	%
$\frac{\Delta V_O}{V_O}$	Output Voltage Load Regulation (Note 6)	I_L = 1 mA to 250 mA I_L = 0.1 mA to 1 mA	0.04		0.16 **0.20**		0.20 **0.30**	%
$V_{IN}-V_O$	Dropout Voltage (Note 7)	I_L = 1 mA	60		100 **150**		100 **150**	mV
		I_L = 50 mA	240		300 **420**		300 **420**	
		I_L = 100 mA	310		400 **520**		400 **520**	
		I_L = 250 mA	470		600 **800**		600 **800**	
I_{GND}	Ground Pin Current (Note 8)	I_L = 1 mA	130		170 **200**		170 **200**	µA
		I_L = 50 mA	1.1		2 **2.5**		2 **2.5**	mA
		I_L = 100 mA	4.5		6 **8**		6 **8**	
		I_L = 250 mA	21		28 **33**		28 **33**	
I_{GND}	Ground Pin Current at Dropout (Note 8)	V_{IN} = 4.5V I_L = 100 µA	165		210 **240**		210 **240**	µA
I_{GND}	Ground Pin Current at Shutdown (Note 8)	(Note 9)	105		140		140	µA

Electrical Characteristics Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the −40°C to +125°C junction temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQL) methods. Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, Feedback pin is tied to 5V Tap pin, Output pin is tied to Output Sense pin, V_{OUT} = 5V. (Continued)

Symbol	Parameter	Conditions	Typical	2952AI 2953AI		2952I 2953I		Units
				Min	Max	Min	Max	
I_{LIMIT}	Current Limit	V_{OUT} = 0	380		500 **530**		500 **530**	mA
$\frac{\Delta V_O}{\Delta Pd}$	Thermal Regulation	(Note 10)	0.05		0.2		0.2	%/W
e_n	Output Noise Voltage (10 Hz to 100 kHz) I_L = 100 mA	C_L = 2.2 µF	400					µV RMS
		C_L = 33 µF	260					
		C_L = 33 µF (Note 11)	80					
V_{REF}	Reference Voltage	(Note 12)	1.230	1.215 **1.205**	1.245 **1.255**	1.205 **1.190**	1.255 **1.270**	V
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Line Regulation	V_{IN} = 2.5V to 6V V_{IN} = 6V to 30V (Note 13)	0.03		0.1 **0.2**		0.2 **0.4**	%
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Load Regulation	I_{REF} = 0 to 200 µA	0.25		0.4 **0.6**		0.8 **1.0**	%
$\frac{\Delta V_{REF}}{\Delta T}$	Reference Voltage Temp. Coefficient	(Note 5)	**20**					ppm/°C
I_B(FB)	Feedback Pin Bias Current		20		40 **60**		40 **60**	nA
I_O (SINK)	Output "OFF" Pulldown Current	(Note 9)	50	30 **20**		30 **20**		mA
DROPOUT DETECTION COMPARATOR								
I_{OH}	Output "HIGH" Leakage	V_{OH} = 30V	0.01		1 **2**		1 **2**	µA
V_{OL}	Output "LOW" Voltage	V_{IN} = 4V I_O(COMP) = 400 µA	150		250 **400**		250 **400**	mV
V_{THR} (MAX)	Upper Threshold Voltage	(Note 14)	−240	−320 **−380**	−150 **−130**	−320 **−380**	−150 **−130**	mV
V_{THR} (MIN)	Lower Threshold Voltage	(Note 14)	−350	−450 **−640**	−280 **−180**	−450 **−640**	−280 **−180**	mV
HYST	Hysteresis	(Note 14)	60					mV
SHUTDOWN INPUT (Note 16)								
V_{OS}	Input Offset Voltage	(Referred to V_{REF})	±3	−7.5 **−10**	7.5 **10**	−7.5 **−10**	7.5 **10**	mV
HYST	Hysteresis		6					mV
I_B	Input Bias Current	V_{IN}(S/D) = 0 to 5V	10	−30 **−50**	30 **50**	−30 **−50**	30 **50**	nA

Electrical Characteristics Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the −40°C to +125°C junction temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQL) methods. Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, Feedback pin is tied to 5V Tap pin, Output pin is tied to Output Sense pin, V_{OUT} = 5V. (Continued)

Symbol	Parameter	Conditions	Typical	2952AI 2953AI		2952I 2953I		Units
				Min	Max	Min	Max	
AUXILIARY COMPARATOR (LP2953 Only)								
V_{OS}	Input Offset Voltage	(Referred to V_{REF})	±3	−7.5 **−10**	7.5 **10**	−7.5 **−10**	7.5 **10**	mV
HYST	Hysteresis		6					mV
I_B	Input Bias Current	V_{IN}(COMP) = 0 to 5V	10	−30 **−50**	30 **50**	−30 **−50**	30 **50**	nA
I_{OH}	Output "HIGH" Leakage	V_{OH} = 30V V_{IN}(COMP) = 1.3V	0.01		1 **2**		1 **2**	µA
V_{OL}	Output "LOW" Voltage	V_{IN}(COMP) = 1.1V I_O(COMP) = 400 µA	150		250 **400**		250 **400**	mV

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$.

Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. See APPLICATION HINTS for additional information on heatsinking and thermal resistance.

Note 3: When used in dual-supply systems where the regulator load is returned to a negative supply, the output voltage must be diode-clamped to ground.

Note 4: May exceed the input supply voltage.

Note 5: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 6: Load regulation is measured at constant junction temperature using low duty cycle pulse testing. Two separate tests are performed, one for the range of 100 µA to 1 mA and one for the 1 mA to 250 mA range. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 7: Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1 volt differential. At very low values of programmed output voltage, the input voltage minimum of 2V **(2.3V over temperature)** must be observed.

Note 8: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the ground pin current, output load current, and current through the external resistive divider (if used).

Note 9: $V_{SHUTDOWN} \leq 1.1V$, V_{OUT} = 5V.

Note 10: Thermal regulation is the change in output voltage at a time T after a change in power dissipation, excluding load or line regulation effects. Specifications are for a 200 mA load pulse at V_{IN} = 20V (3W pulse) for T = 10 ms.

Note 11: Connect a 0.1 µF capacitor from the output to the feedback pin.

Note 12: $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1V)$, $2.3V \leq V_{IN} \leq 30V$, $100\ \mu A \leq I_L \leq 250$ mA.

Note 13: Two separate tests are performed, one covering $2.5V \leq V_{IN} \leq 6V$ and the other test for $6V \leq V_{IN} \leq 30V$.

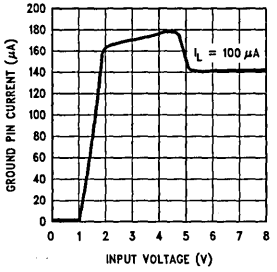
Note 14: Comparator thresholds are referred to a 5V output. To express the threshold voltages in terms of a differential at the Feedback terminal, divide by the error amplifier gain = V_{OUT}/V_{REF}.

Note 15: Human body model, 200 pF discharged through 1.5 kΩ.

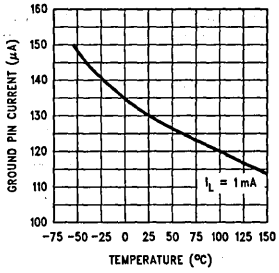
Note 16: Drive $\overline{\text{Shutdown}}$ pin with TTL or CMOS-low level to shut regulator OFF, high level to turn regulator ON.

Typical Performance Characteristics

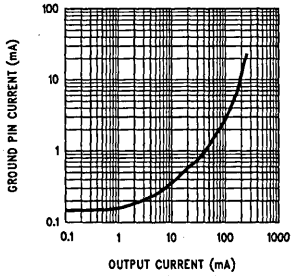
Quiescent Current



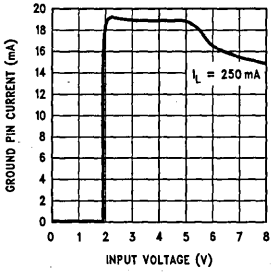
Quiescent Current



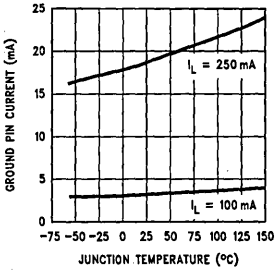
Ground Pin Current vs Load



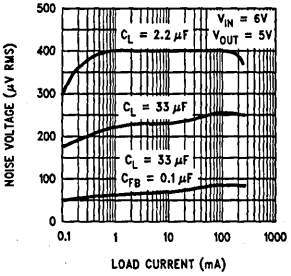
Ground Pin Current



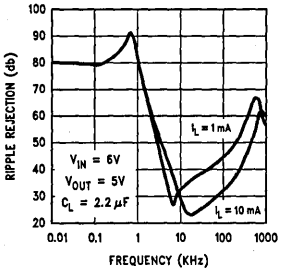
Ground Pin Current



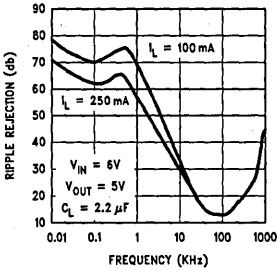
Output Noise Voltage



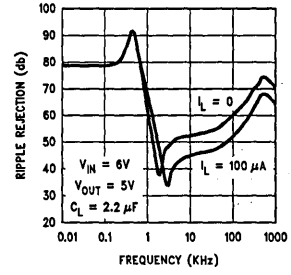
Ripple Rejection



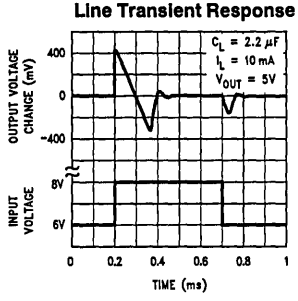
Ripple Rejection



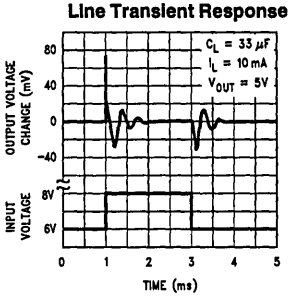
Ripple Rejection



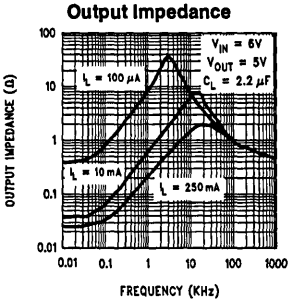
Line Transient Response



Line Transient Response



Output Impedance



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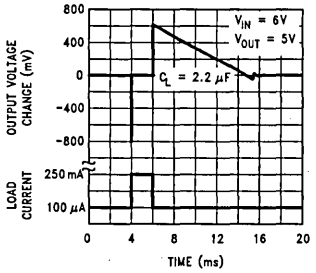
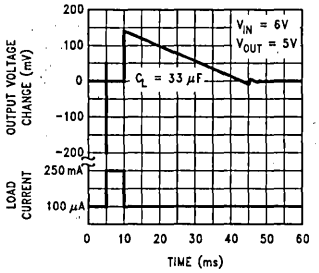
Typical Performance Characteristics (Continued)

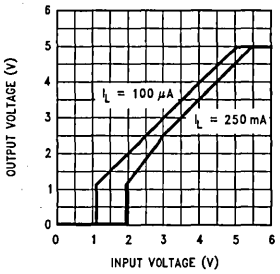
Load Transient Response



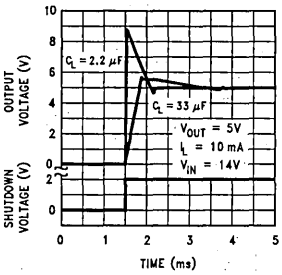
Load Transient Response



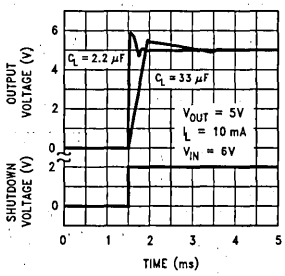
Dropout Characteristics



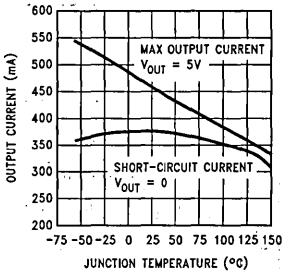
Enable Transient



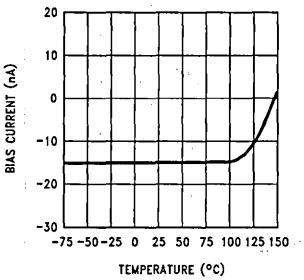
Enable Transient



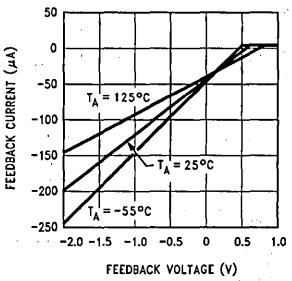
Short-Circuit Output Current and Maximum Output Current



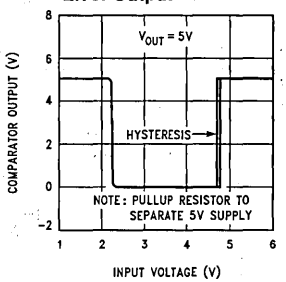
Feedback Bias Current



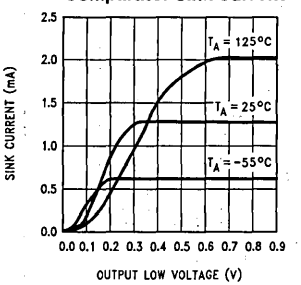
Feedback Pin Current



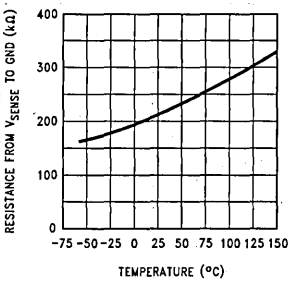
Error Output



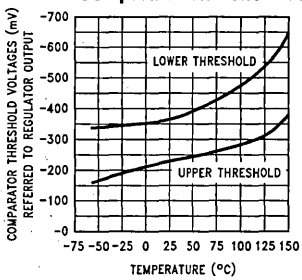
Comparator Sink Current



Divider Resistance



Dropout Detection Comparator Threshold Voltages



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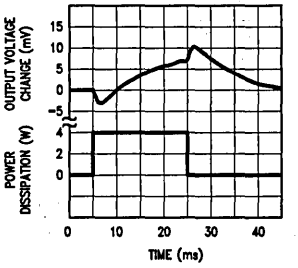
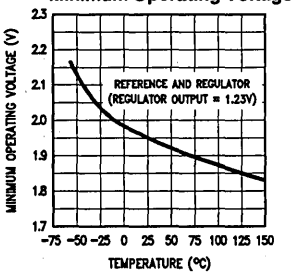
Typical Performance Characteristics (Continued)

Thermal Regulation



Minimum Operating Voltage



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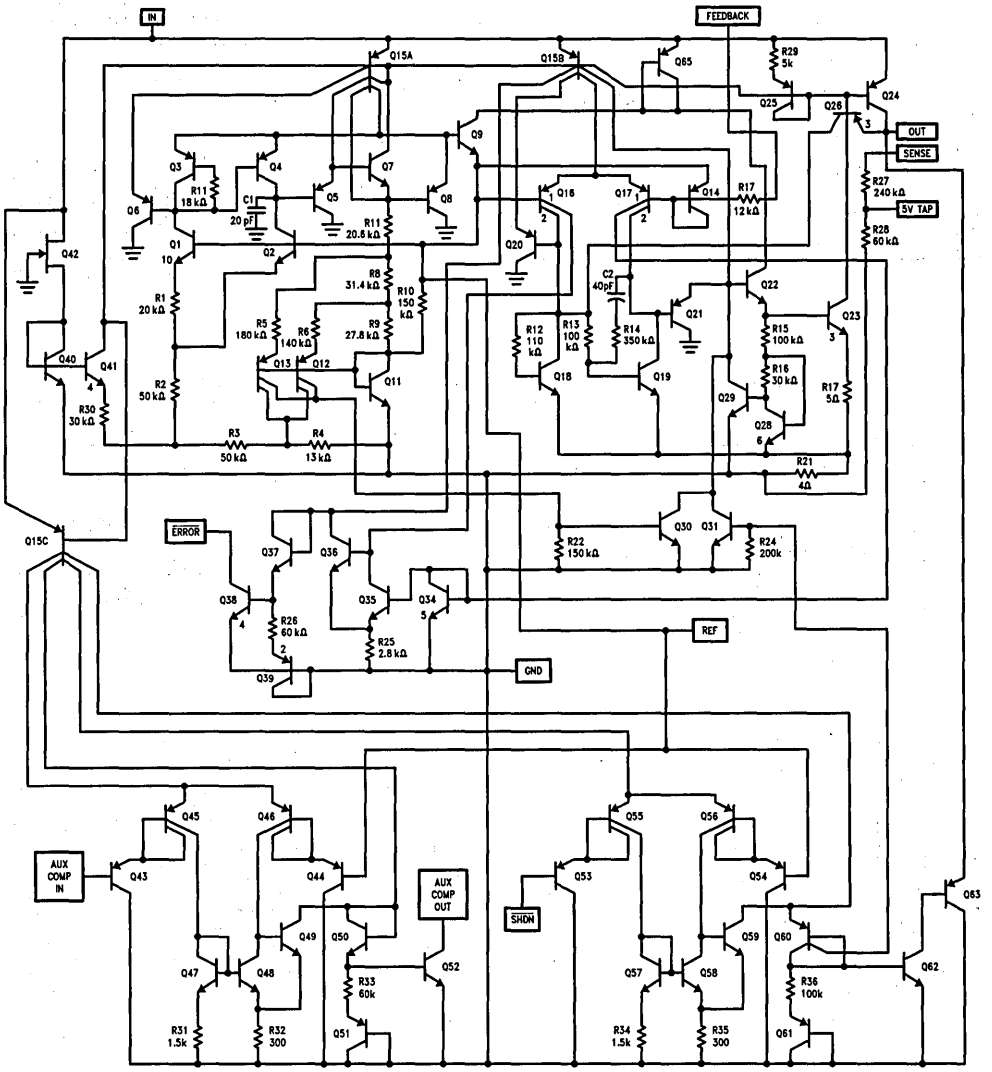
Schematic Diagram



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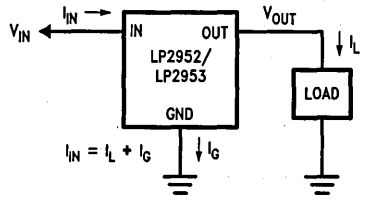
Application Hints

HEATSINK REQUIREMENTS

A heatsink may be required with the LP2952/LP2953 depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the maximum power dissipated by the regulator, P(max), must be calculated. It is important to remember that if the regulator is powered from a transformer connected to the AC line, the **maximum specified AC input voltage** must be used (since this produces the maximum DC input voltage to the regulator). *Figure 1* shows the voltages and currents which are present in the circuit. The formula for calculating the power dissipated in the regulator is also shown in *Figure 1*:



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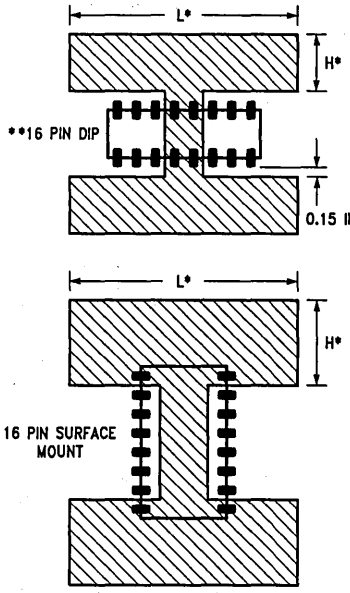
$$P_{TOTAL} = (V_{IN} - V_{OUT})\, I_L + (V_{IN})\, I_G$$

FIGURE 1. Current/Voltage Diagram

Figure 2 shows copper patterns which may be used to dissipate heat from the LP2952 and LP2953:



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*For best results, use L = 2H

**14-Pin DIP is similar, refer to Table I for pins designated for heatsinking.

FIGURE 2. Copper Heatsink Patterns

The next parameter which must be calculated is the maximum allowable temperature rise, T_R(max). This is calculated by using the formula:

$$T_R(max) = T_J(max) - T_A(max)$$

where: T_J(max) is the maximum allowable junction temperature

T_A(max) is the maximum ambient temperature

Using the calculated values for T_R(max) and P(max), the required value for junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

$$\theta_{(J-A)} = T_R(max)/P(max)$$

The heatsink for the LP2952 and LP2953 is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are:

TABLE I

Part	Package	Pins
LP2952N	14-Pin DIP	3, 4, 5, 10, 11, 12
LP2953N	16-Pin DIP	4, 5, 12, 13
LP2952M	16-Pin Surface Mt.	1, 8, 9, 16
LP2953M	16-Pin Surface Mt.	1, 8, 9, 16

Table II shows some values of junction-to-ambient thermal resistance (θ_{J-A}) for values of L and W for 1 oz. copper:

TABLE II

Package	L (in.)	H (in.)	θ_{J-A} (°C/W)
16-Pin DIP	1	0.5	70
	2	1	60
	3	1.5	58
	4	0.19	66
	6	0.19	66
14-Pin DIP	1	0.5	65
	2	1	51
	3	1.5	49
Surface Mount	1	0.5	83
	2	1	70
	3	1.5	67
	6	0.19	69
	4	0.19	71
	2	0.19	73

Application Hints (Continued)

EXTERNAL CAPACITORS

A 2.2 μF (or greater) capacitor is required between the output pin and ground to assure stability. Without this capacitor, the part may oscillate. Most type of tantalum or aluminum electrolytics will work here. Film types will work, but are more expensive. Many aluminum electrolytics contain electrolytes which freeze at −30°C, which requires the use of solid tantalums below −25°C. The important parameters of the capacitor are an ESR of about 5Ω or less and a resonant frequency above 500 kHz (the ESR may increase by a factor of **20** or **30** as the temperature is reduced from 25°C to −30°C). The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.68 μF for currents below 10 mA or 0.22 μF for currents below 1 mA.

Programming the output for voltages below 5V runs the error amplifier at lower gains requiring *more* output capacitance for stability. For the worst-case condition of 1.23V output and 250 mA of load current, a 6.8 μF (or larger) capacitor should be used.

A 1 μF capacitor should be placed from the input pin to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery input is used.

Stray capacitance to the Feedback terminal can cause instability. This problem is most likely to appear when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between the Output and Feedback pins and increasing the output capacitance to 6.8 μF (or greater) will cure the problem.

MINIMUM LOAD

When setting the output voltage using an external resistive divider, a minimum current of 1 μA is recommended through the resistors to provide a minimum load.

It should be noted that a minimum load current is specified in several of the electrical characteristic test conditions, so this value must be used to obtain correlation on these tested limits.

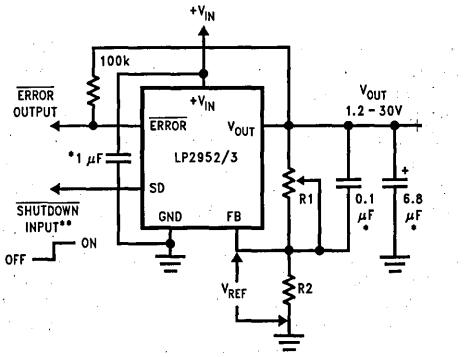
PROGRAMMING THE OUTPUT VOLTAGE

The regulator may be pin-strapped for 5V operation using its internal resistive divider by tying the Output and Sense pins together and also tying the Feedback and 5V Tap pins together.

Alternatively, it may be programmed for any voltage between the 1.23V reference and the 30V maximum rating using an external pair of resistors (see *Figure 3*). The complete equation for the output voltage is:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) + (I_{FB} \times R1)$$

where V_{REF} is the 1.23V reference and I_{FB} is the Feedback pin bias current (−20 nA typical). The minimum recommended load current of 1 μA sets an upper limit of 1.2 MΩ on the value of R2 in cases where the regulator must work with no load (see **MINIMUM LOAD**). I_{FB} will produce a typical 2% error in V_{OUT} which can be eliminated at room temperature by trimming R1. For better accuracy, choosing R2 = 100 kΩ will reduce this error to 0.17% while increasing the resistor program current to 12 μA. Since the typical quiescent current is 120 μA, this added current is negligible.



TL/H/11127–9

FIGURE 3. Adjustable Regulator

*See Application Hints

**Drive with TTL-low to shut down

DROPOUT VOLTAGE

The dropout voltage of the regulator is defined as the minimum input-to-output voltage differential required for the output voltage to stay within 100 mV of the output voltage measured with a 1V differential. The dropout voltage is independent of the programmed output voltage.

DROPOUT DETECTION COMPARATOR

This comparator produces a logic "LOW" whenever the output falls out of regulation by more than about 5%. This figure results from the comparator's built-in offset of 60 mV divided by the 1.23V reference (refer to block diagrams on page 1). The 5% low trip level remains constant regardless of the programmed output voltage. An out-of-regulation condition can result from low input voltage, current limiting, or thermal limiting.

Figure 4 gives a timing diagram showing the relationship between the output voltage, the $\overline{\text{ERROR}}$ output, and input voltage as the input voltage is ramped up and down to a regulator programmed for 5V output. The $\overline{\text{ERROR}}$ signal becomes low at about 1.3V input. It goes high at about 5V input, where the output equals 4.75V. Since the dropout voltage is load dependent, the **input** voltage trip points will vary with load current. The **output** voltage trip point does not vary.

The comparator has an open-collector output which requires an external pull-up resistor. This resistor may be connected to the regulator output or some other supply voltage. Using the regulator output prevents an invalid "HIGH" on the comparator output which occurs if it is pulled up to an external voltage while the regulator input voltage is reduced below 1.3V. In selecting a value for the pull-up resistor, note that while the output can sink 400 μA, this current adds to battery drain. Suggested values range from 100 kΩ to 1 MΩ. This resistor is not required if the output is unused.

When $V_{IN} \leq 1.3V$, the error flag pin becomes a high impedance, allowing the error flag voltage to rise to its pull-up voltage. Using V_{OUT} as the pull-up voltage (rather than an external 5V source) will keep the error flag voltage below 1.2V (typical) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested) to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

Application Hints (Continued)

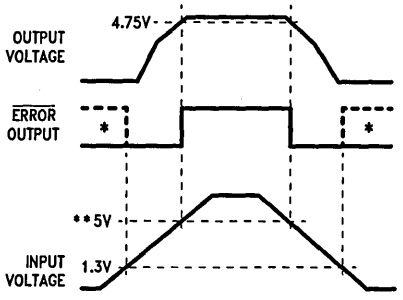


FIGURE 4. ERROR Output Timing

*In shutdown mode, ERROR will go high if it has been pulled up to an external supply. To avoid this invalid response, pull up to regulator output.

**Exact value depends on dropout voltage. (See Application Hints)

OUTPUT ISOLATION

The regulator output can be left connected to an active voltage source (such as a battery) with the regulator input power shut off, **as long as the regulator ground pin is connected to ground.** If the ground pin is left floating, **damage to the regulator can occur** if the output is pulled up by an external voltage source.

REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present on the output. One method is to reduce regulator bandwidth by increasing output capacitance. This is relatively inefficient, since large increases in capacitance are required to get significant improvement.

Noise can be reduced more effectively by a bypass capacitor placed across R1 (refer to *Figure 3*). The formula for selecting the capacitor to be used is:

$$C_B = \frac{1}{2\pi\ R1 \times 20\ Hz}$$

This gives a value of about 0.1 μF. When this is used, the output capacitor must be 6.8 μF (or greater) to maintain stability. The 0.1 μF capacitor reduces the high frequency gain of the circuit to unity, lowering the output noise from 260 μV to 80 μV using a 10 Hz to 100 kHz bandwidth. Also, noise is no longer proportional to the output voltage, so improvements are more pronounced at high output voltages.

AUXILIARY COMPARATOR (LP2953 only)

The LP2953 contains an auxiliary comparator whose inverting input is connected to the 1.23V reference. The auxiliary comparator has an open-collector output whose electrical characteristics are similar to the dropout detection comparator. The non-inverting input and output are brought out for external connections.

SHUTDOWN INPUT

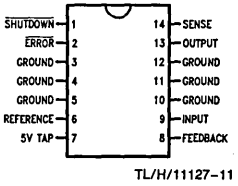
When the operating junction temperature is between −40°C and +125°C, the shutdown input may be left open (floating) for normal regulator operation (regulator output ON).

Operation at junction temperatures above the 125°C maximum (which is **not recommended**) has shown that leaving the shutdown pin open may cause the part to turn ON and OFF. This occurs when internal leakage current activates the shutdown pin, causing the output to go OFF. This reduces power dissipation, which results in die cooling. This allows the part to turn back ON, and the cycle starts over.

If the part is operated above 125°C, the shutdown pin must be connected to the regulator input voltage through a pull-up resistor to assure that the regulator remains ON. This resistor is not required for operation between −40°C and +125°C, but can be used without affecting performance.

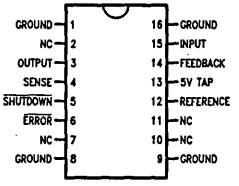
Pinout Drawings

LP2952 14-Pin DIP



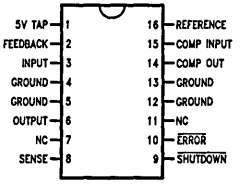
TL/H/11127–11

LP2952 16-Pin SO



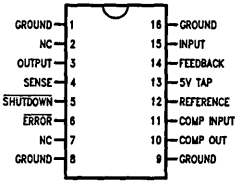
TL/H/11127–12

LP2953 16-Pin DIP



TL/H/11127–13

LP2953 16-Pin SO



TL/H/11127–14

Ordering Information

LP2952

Order Number	Temp. Range (T_J) °C	Package	NSC Drawing Number
LP2952IN	−40 to +125	14-Pin Molded DIP	N14A
LP2952AIN			
LP2952IM	−40 to +125	16-Pin Surface Mt.	M16A
LP2952AIM			

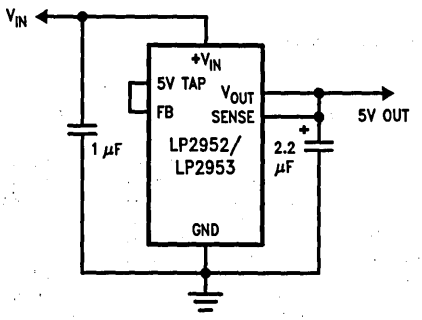
LP2953

Order Number	Temp. Range (T_J) °C	Package	NSC Drawing Number
LP2953IN	−40 to +125	16-Pin Molded DIP	N16A
LP2953AIN			
LP2953IM	−40 to +125	16-Pin Surface Mt.	M16A
LP2953AIM			

4

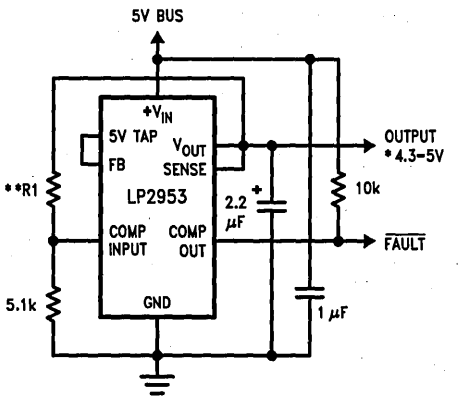
Typical Applications

Basic 5V Regulator



TL/H/11127–15

5V Current Limiter with Load Fault Indicator

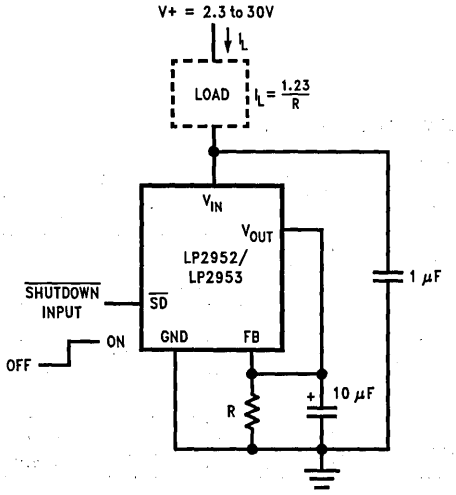


TL/H/11127–16

*Output voltage equals $+V_{IN}$ minum dropout voltage, which varies with output current. Current limits at a maximum of 380 mA (typical).

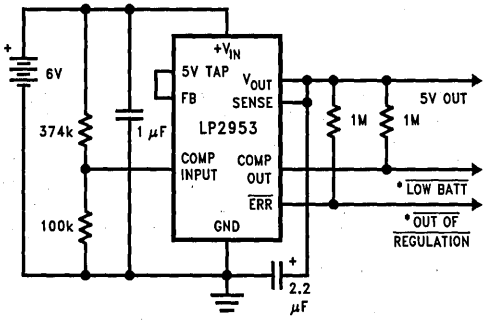
**Select R1 so that the comparator input voltage is 1.23V at the output voltage which corresponds to the desired fault current value.

Low T.C. Current Sink



TL/H/11127–17

5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION



TL/H/11127–18

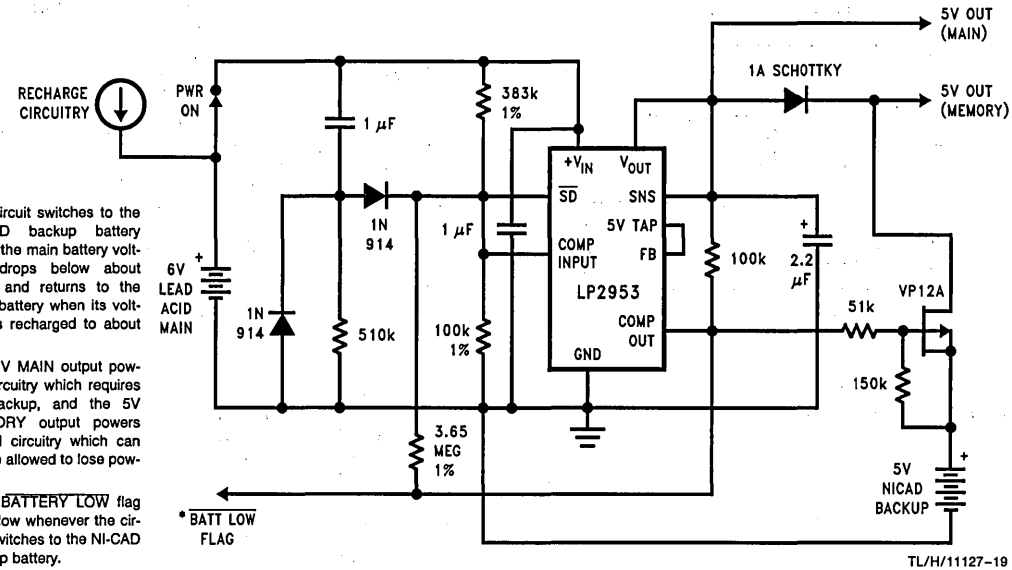
*Connect to Logic or μP control inputs.

LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or power down some hardware with high power requirements. The output is still in regulation at this time.

OUT OF REGULATION flag indicates when the battery is almost completely discharged, and can be used to initiate a power-down sequence.

Typical Applications (Continued)

5V Battery Powered Supply with Backup and Low Battery Flag



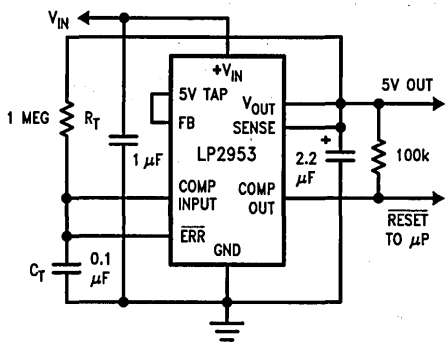
The circuit switches to the NI-CAD backup battery when the main battery voltage drops below about 5.6V, and returns to the main battery when its voltage is recharged to about 6V.

The 5V MAIN output powers circuitry which requires no backup, and the 5V MEMORY output powers critical circuitry which can not be allowed to lose power.

*The $\overline{\text{BATTERY LOW}}$ flag goes low whenever the circuit switches to the NI-CAD backup battery.

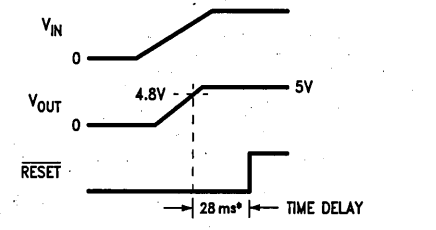
TL/H/11127–19

5V Regulator with Timed Power-On Reset



TL/H/11127–20

Timing Diagram for Timed Power-On Reset

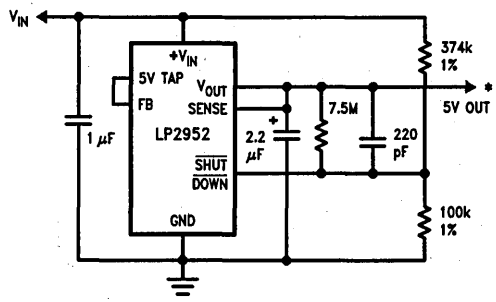


TL/H/11127–21

*R_T = 1 MEG, C_T = 0.1 μF

Typical Applications (Continued)

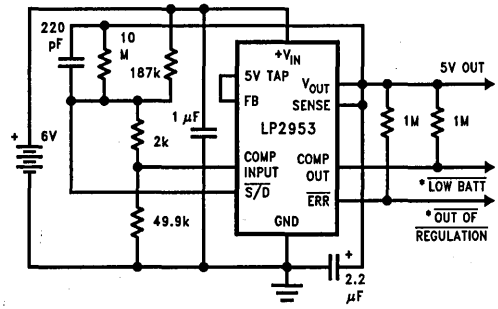
5V Regulator with Snap-On/Snap-Off Feature and Hysteresis



TL/H/11127–22

*Turns ON at V_{IN} = 5.87V
Turns OFF at V_{IN} = 5.64V
(for component values shown)

5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION with SNAP-ON/SNAP-OFF Output



TL/H/11127–23

*Connect to Logic or µP control inputs.

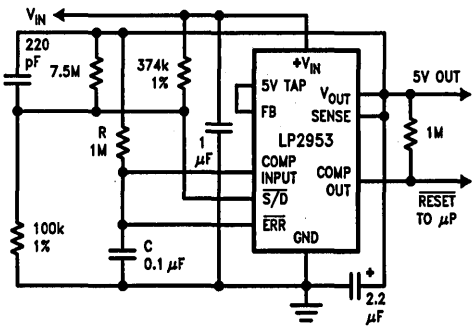
OUTPUT has SNAP-ON/SNAP-OFF feature.

LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or shut down hardware with high power requirements. The output is still in regulation at this time.

OUT OF REGULATION flag goes low if the output goes below about 4.7V, which could occur from a load fault.

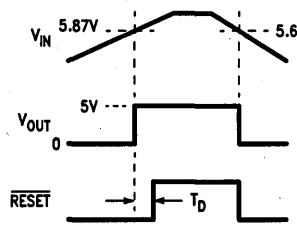
OUTPUT has SNAP-ON/SNAP-OFF feature. Regulator snaps ON at about 5.7V input, and OFF at about 5.6V.

5V Regulator with Timed Power-On Reset, Snap-On/Snap-Off Feature and Hysteresis



TL/H/11127–24

Timing Diagram



TL/H/11127–25

Td = (0.28) RC = 28 ms for components shown.

National Semiconductor

LM78S40
Universal Switching Regulator Subsystem

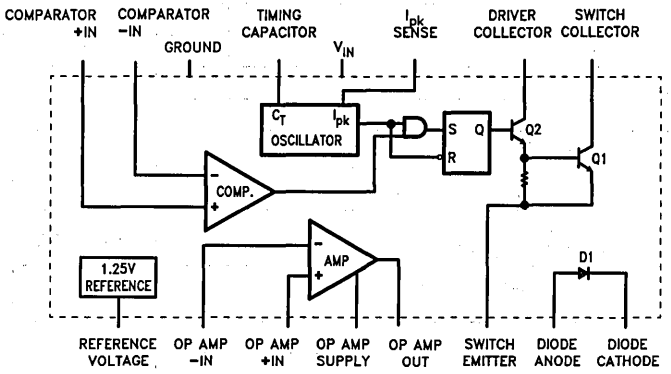
General Description

The LM78S40 is a monolithic regulator subsystem consisting of all the active building blocks necessary for switching regulator systems. The device consists of a temperature compensated voltage reference, a duty-cycle controllable oscillator with an active current limit circuit, an error amplifier, high current, high voltage output switch, a power diode and an uncommitted operational amplifier. The device can drive external NPN or PNP transistors when currents in excess of 1.5A or voltages in excess of 40V are required. The device can be used for step-down, step-up or inverting switching regulators as well as for series pass regulators. It features wide supply voltage range, low standby power dissipation, high efficiency and low drift. It is useful for any stand-alone, low part count switching system and works extremely well in battery operated systems.

Features

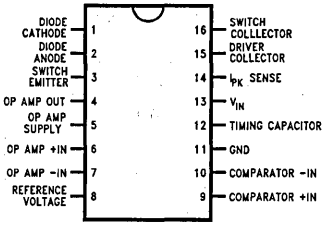
- Step-up, step-down or inverting switching regulators
- Output adjustable from 1.25V to 40V
- Peak currents to 1.5A without external transistors
- Operation from 2.5V to 40V input
- Low standby current drain
- 80 dB line and load regulation
- High gain, high current, independent op amp
- Pulse width modulation with no double pulsing

Block and Connection Diagrams



TL/H/10057–2

16-Lead DIP



TL/H/10057–1

Top View

Ordering Information

Device Code	Package Code	Package Description
LM78S40J	J16A	Ceramic DIP
LM78S40N	N16A	Molded DIP
LM78S40CJ	J16A	Ceramic DIP
LM78S40CN	N16A	Molded DIP

4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP: −65°C to +150°C

Operating Temperature Range
- Extended (LM78S40J): −55°C to +125°C
- Industrial (LM78S40N): −40°C to +125°C
- Commercial (LM78S40CN): 0°C to +70°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP (Soldering, 10 sec.): 265°C

Internal Power Dissipation (Notes 1, 2)
- 16L-Ceramic DIP: 1.50W
- 16L-Molded DIP: 1.04W

Input Voltage from V_{IN} to GND: 40V

Input Voltage from V^+ (Op Amp) to GND: 40V

Common Mode Input Range (Comparator and Op Amp): −0.3 to V+

Differential Input Voltage (Note 3): ±30V

Output Short Circuit Duration (Op Amp): Continuous

Current from V_{REF}: 10 mA

Voltage from Switch Collectors to GND: 40V

Voltage from Switch Emitters to GND: 40V

Voltage from Switch Collectors to Emitter: 40V

Voltage from Power Diode to GND: 40V

Reverse Power Diode Voltage: 40V

Current through Power Switch: 1.5A

Current through Power Diode: 1.5A

ESD Susceptibility: (to be determined)

LM78S40
Electrical Characteristics

T_A = Operating temperature range, V_{IN} = 5.0V, V^+(Op Amp) = 5.0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GENERAL CHARACTERISTICS						
I_{CC}	Supply Current (Op Amp Disconnected)	V_{IN} = 5.0V		1.8	3.5	mA
		V_{IN} = 40V		2.3	5.0	mA
I_{CC}	Supply Current (Op Amp Connected)	V_{IN} = 5.0V			4.0	mA
		V_{IN} = 40V			5.5	mA
REFERENCE SECTION						
V_{REF}	Reference Voltage	I_{REF} = 1.0 mA, Extend −55°C < T_A < +125°C, Comm 0 < T_A < +70°C, Indus −40°C < T_A < +85°C	1.180	1.245	1.310	V
$V_{R\ LINE}$	Reference Voltage Line Regulation	V_{IN} = 3.0V to V_{IN} = 40V, I_{REF} = 1.0 mA, T_A = 25°C		0.04	0.2	mV/V
$V_{R\ LOAD}$	Reference Voltage Load Regulation	I_{REF} = 1.0 mA to I_{REF} = 10 mA, T_A = 25°C		0.2	0.5	mV/mA
OSCILLATOR SECTION						
I_{CHG}	Charging Current	V_{IN} = 5.0V, T_A = 25°C	20		50	μA
I_{CHG}	Charging Current	V_{IN} = 40V, T_A = 25°C	20		70	μA
I_{DISCHG}	Discharge Current	V_{IN} = 5.0V, T_A = 25°C	150		250	μA
I_{DISCHG}	Discharge Current	V_{IN} = 40V, T_A = 25°C	150		350	μA
V_{OSC}	Oscillator Voltage Swing	V_{IN} = 5.0V, T_A = 25°C		0.5		V
t_{on}/t_{off}	Ratio of Charge/ Discharge Time			6.0		μs/μs

LM78S40
Electrical Characteristics (Continued)

T_A = Operating Temperature Range, V_{IN} = 5.0V, V^+(Op Amp) = 5.0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CURRENT LIMIT SECTION						
V_{CLS}	Current Limit Sense Voltage	T_A = 25°C	250		350	mV
OUTPUT SWITCH SECTION						
$V_{SAT\,1}$	Output Saturation Voltage 1	I_{SW} = 1.0A *(Figure 1)*		1.1	1.3	V
$V_{SAT\,2}$	Output Saturation Voltage 2	I_{SW} = 1.0A *(Figure 2)*		0.45	0.7	V
h_{FE}	Output Transistor Current Gain	I_C = 1.0A, V_{CE} = 5.0V, T_A = 25°C		70		
I_L	Output Leakage Current	V_O = 40V, T_A = 25°C		10		nA
POWER DIODE						
V_{FD}	Forward Voltage Drop	I_D = 1.0A		1.25	1.5	V
I_{DR}	Diode Leakage Current	V_D = 40V, T_A = 25°C		10		nA
COMPARATOR						
V_{IO}	Input Offset Voltage	V_{CM} = V_{REF}		1.5	15	mV
I_{IB}	Input Bias Current	V_{CM} = V_{REF}		35	200	nA
I_{IO}	Input Offset Current	V_{CM} = V_{REF}		5.0	75	nA
V_{CM}	Common Mode Voltage Range	T_A = 25°C	0		$V_{IN}-2$	V
PSRR	Power Supply Rejection Ratio	V_{IN} = 3.0V to 40V, T_A = 25°C	70	96		dB
OPERATIONAL AMPLIFIER						
V_{IO}	Input Offset Voltage	V_{CM} = 2.5V		4.0	15	mV
I_{IB}	Input Bias Current	V_{CM} = 2.5V		30	200	nA
I_{IO}	Input Offset Current	V_{CM} = 2.5V		5.0	75	nA
A_{VS}^+	Voltage Gain+	R_L = 2.0 kΩ to GND; V_O = 1.0V to 2.5V, T_A = 25°C	25	250		V/mV
A_{VS}^-	Voltage Gain−	R_L = 2.0 kΩ to V^+ (Op Amp) V_O = 1.0V to 2.5V, T_A = 25°C	25	250		V/mV
V_{CM}	Common Mode Voltage Range	T_A = 25°C	0		$V_{CC}-2$	V
CMR	Common Mode Rejection	V_{CM} = 0V to 3.0V, T_A = 25°C	76	100		dB
PSRR	Power Supply Rejection Ratio	V^+ (Op Amp) = 3.0V to 40V, T_A = 25°C	76	100		dB
I_O^+	Output Source Current	T_A = 25°C	75	150		mA
I_O^-	Output Sink Current	T_A = 25°C	10	35		mA
SR	Slew Rate	T_A = 25°C		0.6		V/μs
V_{OL}	Output Voltage LOW	I_L = −5.0 mA, T_A = 25°C			1.0	V
V_{OH}	Output Voltage High	I_L = 50 mA, T_A = 25°C	V + (Op Amp) − 3V			V

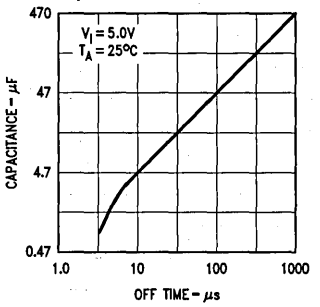
Note 1: $T_{J\,Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Note 3: For supply voltages less than 30V, the absolute maximum voltage is equal to the supply voltage.

Typical Performance Characteristics

C_T vs OFF Time



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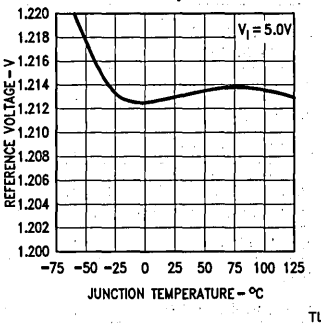
Reference Voltage vs Junction Temperature



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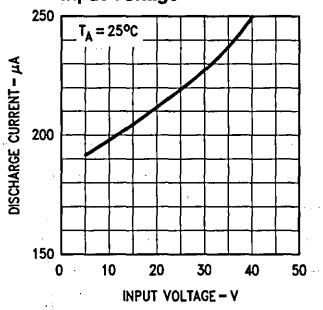
Discharge Current vs Input Voltage



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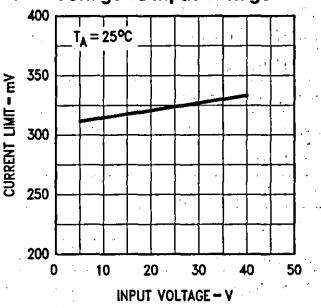
Current Limit Sense Voltage vs Input Voltage



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Design Formulas

Characteristic	Step-Down	Step-Up	Inverting	Units
$\frac{t_{on}}{t_{off}}$	$\frac{V_O + V_D}{V_I - V_{SAT} - V_O}$	$\frac{V_O + V_D - V_I}{V_I - V_{SAT}}$	$\frac{\lvert V_O \rvert + V_D}{V_I - V_{SAT}}$	
$(t_{on} + t_{off})$ Max	$\frac{1}{f_{Min}}$	$\frac{1}{f_{Min}}$	$\frac{1}{f_{MIN}}$	μs
C_T	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$	μF
I_{pk}	$2\, I_{O\,Max}$	$2\, I_{O\,Max} \bullet \frac{t_{on} + t_{off}}{t_{off}}$	$2\, I_{O\,Max} \bullet \frac{t_{on} + t_{off}}{t_{off}}$	A
L_{Min}	$\left(\frac{V_I - V_{SAT} - V_O}{I_{pk}}\right) t_{on\,Max}$	$\left(\frac{V_I - V_{SAT}}{I_{pk}}\right) t_{on\,Max}$	$\left(\frac{V_I - V_{SAT}}{I_{pk}}\right) t_{on\,Max}$	μH
R_{SC}	$0.33/I_{pk}$	$0.33/I_{pk}$	$0.33/I_{pk}$	Ω
C_O	$\frac{I_{pk}\,(t_{on} + t_{off})}{8\, V_{ripple}}$	$\approx \frac{I_O}{V_{ripple}} \bullet t_{on}$	$\approx \frac{I_O}{V_{ripple}} \bullet t_{on}$	μF

Note: V_{SAT} = Saturation voltage of the switching element.
V_D = Forward voltage of the flyback diode.

Functional Description

SWITCHING FREQUENCY CONTROL

The LM78S40 is a variable frequency, variable duty cycle device. The initial switching frequency is set by the timing capacitor. (Oscillator frequency is set by a single external capacitor and may be varied over a range of 100 Hz to 100 kHz). The initial duty cycle is 6:1. This switching frequency and duty cycle can be modified by two mechanisms—the current limit circuitry ($I_{pk\ sense}$) and the comparator.

The comparator modifies the OFF time. When the output voltage is correct, the comparator output is in the HIGH state and has no effect on the circuit operation. If the output voltage is too high then the comparator output goes LOW. In the LOW state the comparator inhibits the turn-on of the output stage switching transistors. As long as the comparator is LOW the system is in OFF time. As the output current rises the OFF time decreases. As the output current nears its maximum the OFF time approaches its minimum value. The comparator can inhibit several ON cycles, one ON cycle or any portion of an ON cycle. Once the ON cycle has begun the comparator cannot inhibit until the beginning of the next ON cycle.

The current limit modifies the ON time. The current limit is activated when a 300 mV potential appears between lead 13 (V_{CC}) and lead 14 (I_{pk}). This potential is intended to result when designed for peak current flows through R_{SC}. When the peak current is reached the current limit is turned on. The current limit circuitry provides for a quick end to ON time and the immediate start of OFF time.

Generally the oscillator is free running but the current limit action tends to reset the timing cycle.

Increasing load results in more current limited ON time and less OFF time. The switching frequency increases with load current.

USING THE INTERNAL REFERENCE, DIODE, AND SWITCH

The internal 1.245V reference (pin 8) must be bypassed, with 0.1 μF directly to the ground pin (pin 11) of the LM78S40, to assure its stability.

V_{FD} is the forward voltage drop across the internal power diode. It is listed on the data sheet as 1.25V typical, 1.5V maximum. If an external diode is used, then its own forward voltage drop must be used for V_{FD}.

V_{SAT} is the voltage across the switch element (output transistors Q1 and Q2) when the switch is closed or ON. This is listed on the data sheet as Output Saturation Voltage.

"Output saturation voltage 1" is defined as the switching element voltage for Q2 and Q1 in the Darlington configuration with collectors tied together. This applies to *Figure 1*, the step down mode.

"Output saturation voltage 2" is the switching element voltage for Q1 only when used as a transistor switch. This applies to *Figure 2*, the step up mode.

For the inverting mode, *Figure 3*, the saturation voltage of the external transistor should be used for V_{SAT}.

Typical Applications

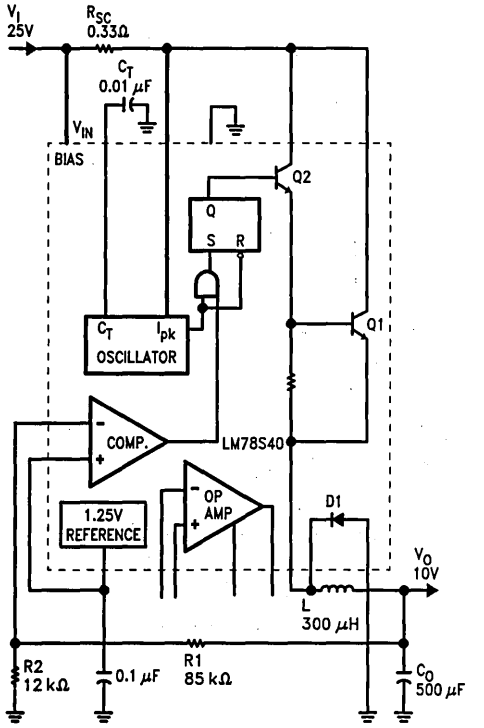

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FIGURE 1. Typical Step-Down Regulator and Operational Performance (T_A = 25°C)

Characteristic	Condition	Typical Value
Output Voltage	I_O = 200 mA	10V
Line Regulation	20V ≤ V_I ≤ 30V	1.5 mV
Load Regulation	5.0 mA ≤ I_O ≤ 300 mA	3.0 mV
Max Output Current	V_O = 9.5V	500 mA
Output Ripple	I_O = 200 mA	50 mV
Efficiency	I_O = 200 mA	74%
Standby Current	I_O = 200 mA	2.8 mA

Note A: For I_O ≥ 200 mA use external diode to limit on-chip power dissipation.

Typical Applications (Continued)

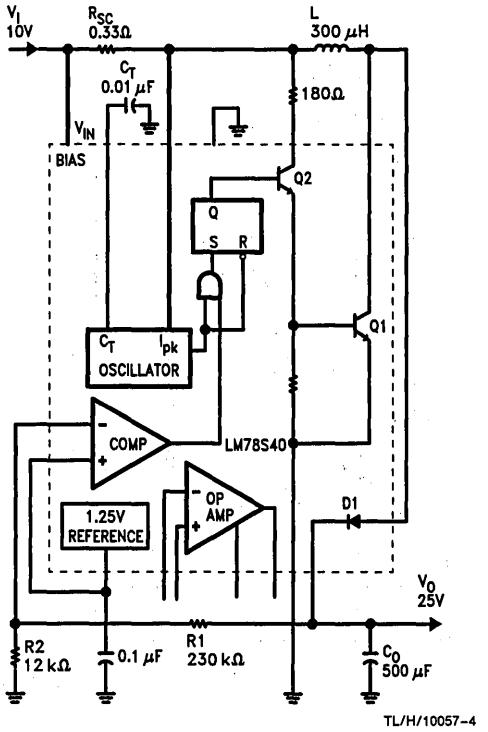

FIGURE 2. Typical Step-Up Regulator and Operational Performance (T_A = 25°C)

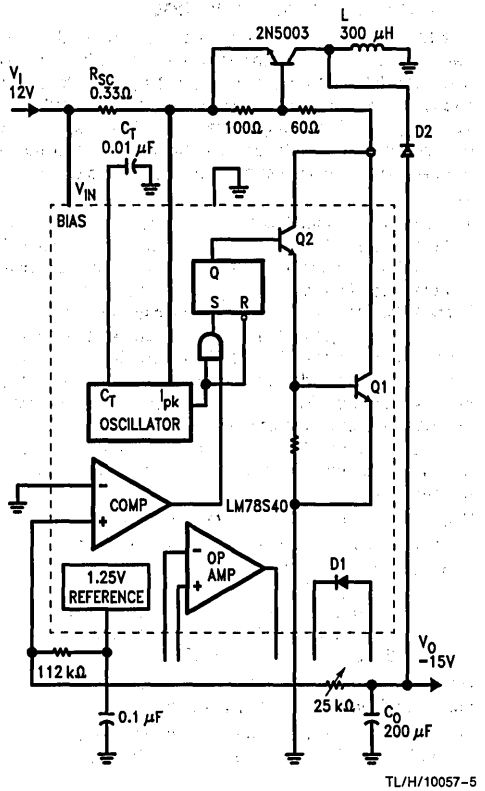

FIGURE 3. Typical Inverting Regulator and Operational Performance (T_A = 25°C)

Characteristic	Condition	Typical Value
Output Voltage	I_O = 50 mA	25V
Line Regulation	5.0V ≤ V_I ≤ 15V	4.0 mV
Load Regulation	5.0 mA ≤ I_O I_O ≤ 100 mA	2.0 mV
Max Output Current	V_O = 23.75V	160 mA
Output Ripple	I_O = 50 mA	30 mV
Efficiency	I_O = 50 mA	79%
Standby Current	I_O = 50 mA	2.6 mA

Characteristic	Condition	Typical Value
Output Voltage	I_O = 100 mA	−15V
Line Regulation	8.0V ≤ V_I ≤ 18V	5.0 mV
Load Regulation	5.0 mA ≤ I_O I_O ≤ 150 mA	3.0 mV
Max Output Current	V_O = 14.25V	160 mA
Output Ripple	I_O = 100 mA	20 mV
Efficiency	I_O = 100 mA	70%
Standby Current	I_O = 100 mA	2.3 mA

Typical Applications (Continued)

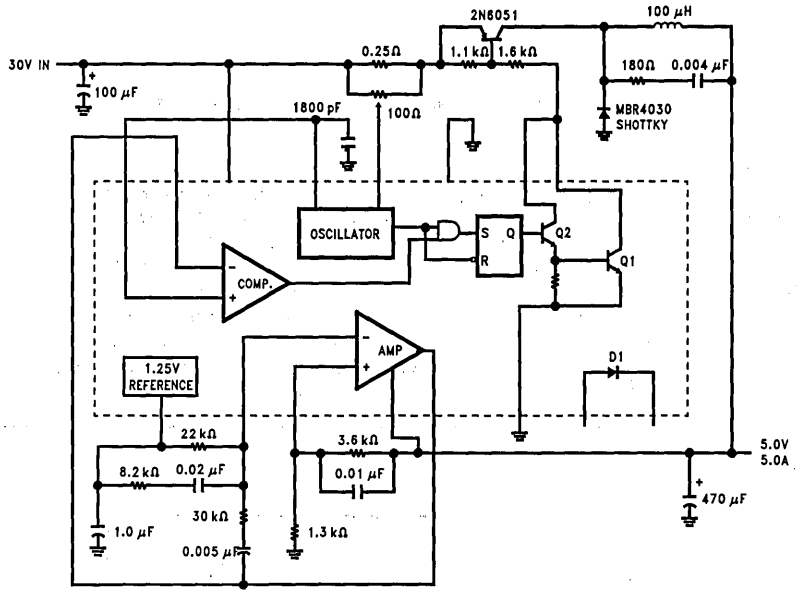

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FIGURE 4. Pulse Width Modulated Step-Down Regulator (f_{OSC} = 20 kHz)

National Semiconductor

LMC7660 Switched Capacitor Voltage Converter

General Description

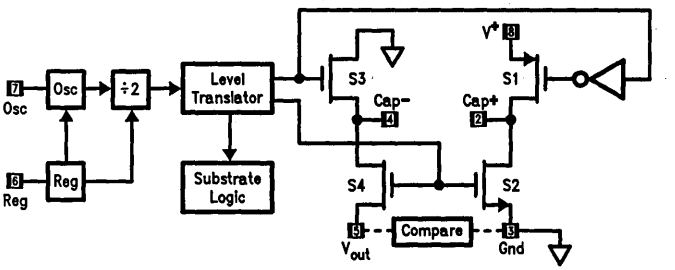
The LMC7660 is a CMOS voltage converter capable of converting a positive voltage in the range of +1.5V to +10V to the corresponding negative voltage of −1.5V to −10V. The LMC7660 is a pin-for-pin replacement for the industry-standard 7660. The converter features: operation over full temperature and voltage range without need for an external diode, low quiescent current, and high power efficiency.

The LMC7660 uses its built-in oscillator to switch 4 power MOS switches and charge two inexpensive electrolytic capacitors.

Features

- Operation over full temperature and voltage range without an external diode
- Low supply current, 200 μA max
- Pin-for-pin replacement for the 7660
- Wide operating range 1.5V to 10V
- 97% Voltage Conversion Efficiency
- 95% Power Conversion Efficiency
- Easy to use, only 2 external components
- Extended temperature range

Block Diagram



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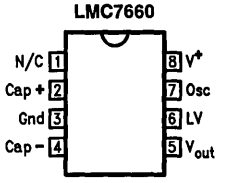
Pin Configuration



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Ordering Information

LMC7660MJ $-55°C \leq T_A \leq +125°C$

LMC7660IN $-40°C \leq T_A \leq +85°C$

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	10.5V
Input Voltage on Pin 6, 7 (Note 2)	−0.3V to (V+ + 0.3V) for V+ < 5.5V (V+ − 5.5V) to (V+ + 0.3V) for V+ > 5.5V
Current into Pin 6 (Note 2)	20 μA
Output Short Circuit Duration (V+ ≤ 5.5V)	Continuous

	Package J	Package N
Power Dissipation (Note 3)	0.9W	1.4W
T_j Max (Note 3)	150°C	150°C
θ_{ja} (Note 3)	140°C/W	90°C/W
Storage Temp. Range	−65°C ≤ T ≤ 150°C	
Lead Temp. (Soldering, 5 sec)	260°C	260°C
ESD Tolerance (Note 8)		±2000V

Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Typ	LMC7660MJ Tested Limit (Note 5)	LMC7660IN Tested Limit (Note 5)	LMC7660IN Design Limit (Note 6)	Units Limits
I_s	Supply Current	$R_L = \infty$	120	200 **400**	200	**400**	μA max
V^+_H	Supply Voltage Range High (Note 7)	R_L = 10 kΩ, Pin 6 Open Voltage Efficiency ≥ 90%	3 to 10	**3 to 10**	3 to 10	**3 to 10**	V
V^+_L	Supply Voltage Range Low	R_L = 10 kΩ, Pin 6 to Gnd. Voltage Efficiency ≥ 90%	1.5 to 3.5	**1.5 to 3.5**	1.5 to 3.5	**1.5 to 3.5**	V
R_{out}	Output Source Resistance	I_L = 20 mA	55	100 **150**	100	**120**	Ω max
		V = 2V, I_L = 3 mA Pin 6 Short to Gnd.	110	200 **300**	200	**300**	Ω max
F_{osc}	Oscillator Frequency		10				kHz
P_{eff}	Power Efficiency	R_L = 5 kΩ	97	95 **90**	95	**90**	% min
$V_{o\ eff}$	Voltage Conversion Efficiency	$R_L = \infty$	99.9	97 **95**	97	**95**	% min
I_{osc}	Oscillator Sink or Source Current	Pin 7 = Gnd. or V+	3				μA

Note 1: Absolute Maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 4 for conditions.

Note 2: Connecting any input terminal to voltages greater than V+ or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power-up" of the LMC7660.

Note 3: For operation at elevated temperature, these devices must be derated based on a thermal resistance of θ_{ja} and T_j max, $T_j = T_A + \theta_{ja} P_D$.

Note 4: **Boldface** numbers apply at temperature extremes. All other numbers apply at T_A = 25°C, V+ = 5V, C_{osc} = 0, and apply for the LMC7660 unless otherwise specified. Test circuit is shown in *Figure 1*.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed over the operating temperature range (but not 100% tested). These limits are not used to calculate outgoing quality levels.

Note 7: The LMC7660 can operate without an external diode over the full temperature and voltage range. The LMC7660 can also be used with the external diode Dx, when replacing previous 7660 designs.

Note 8: The test circuit consists of the human body model of 100 pF in series with 1500Ω.

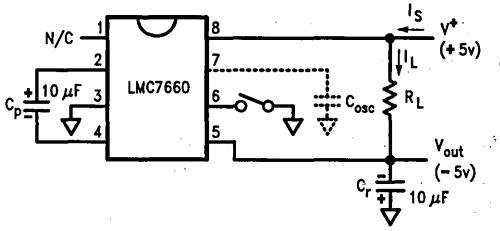
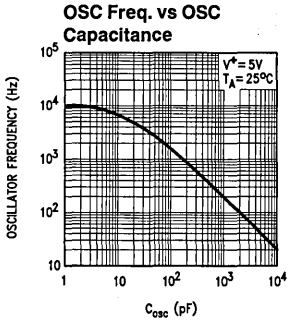
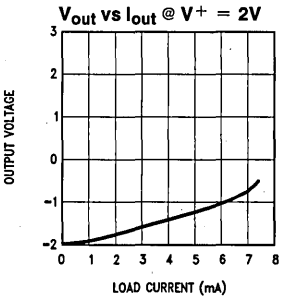
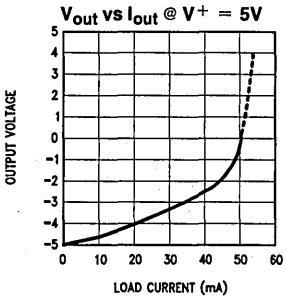


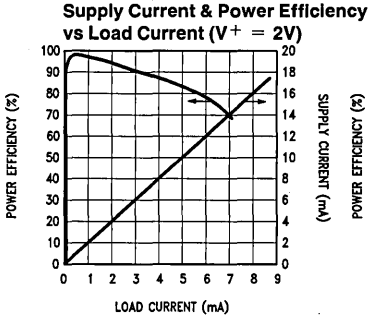
FIGURE 1. LMC7660 Test Circuit

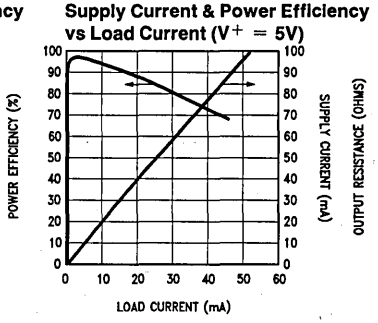
Typical Performance Characteristics

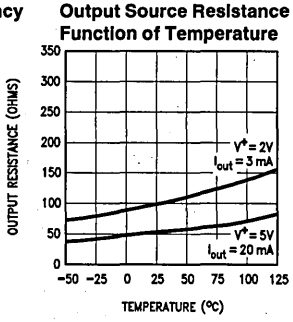


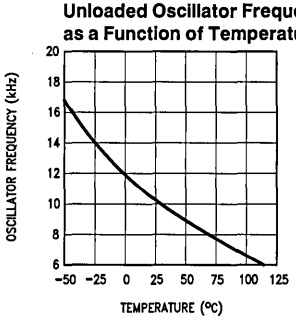


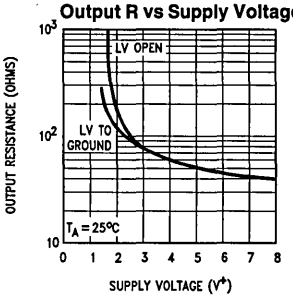


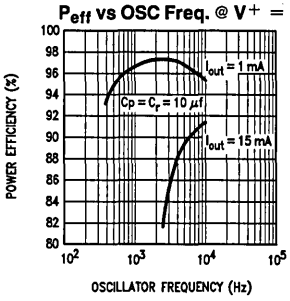












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CIRCUIT DESCRIPTION

The LMC7660 contains four large CMOS switches which are switched in a sequence to provide supply inversion $V_{out} = -V_{in}$. Energy transfer and storage are provided by two inexpensive electrolytic capacitors. *Figure 2* shows how the LMC7660 can be used to generate $-V^+$ from V^+. When switches S1 and S3 are closed, C_p charges to the supply voltage V^+. During this time interval, switches S2 and S4 are open. After C_p charges to V^+, S1 and S3 are opened, S2 and S4 are then closed. By connecting S2 to ground, C_p develops a voltage $-V^+/2$ on C_r. After a number of cycles C_r will be pumped to exactly $-V^+$. This transfer will be exact assuming no load on C_r, and no loss in the switches.

In the circuit of *Figure 2*, S1 is a P-channel device and S2, S3, and S4 are N-channel devices. Because the output is biased below ground, it is important that the p^- wells of S3 and S4 never become forward biased with respect to either their sources or drains. A substrate logic circuit guarantees that these p^- wells are always held at the proper voltage. Under all conditions S4 p^- well must be at the lowest potential in the circuit. To switch off S4, a level translator generates $V_{GS4} = 0V$, and this is accomplished by biasing the level translator from the S4 p^- well.

An internal RC oscillator and ÷ 2 circuit provide timing signals to the level translator. The built-in regulator biases the oscillator and divider to reduce power dissipation on high supply voltage. The regulator becomes active at about $V^+ = 6.5V$. Low voltage operation can be improved if the LV pin is shorted to ground for $V^+ \leq 3.5V$. For $V^+ \geq 3.5V$, the LV pin must be left open to prevent damage to the part.

POWER EFFICIENCY AND RIPPLE

It is theoretically possible to approach 100% efficiency if the following conditions are met:

1) The drive circuitry consumes little power.
2) The power switches are matched and have low R_{on}.
3) The impedance of the reservoir and pump capacitors are negligibly small at the pumping frequency.

The LMC7660 closely approaches 1 and 2 above. By using a large pump capacitor C_p, the charge removed while supplying the reservoir capacitor is small compared to C_p's total charge. Small removed charge means small changes in the pump capacitor voltage, and thus small energy loss and high efficiency. The energy loss by C_p is:

$$E = \tfrac{1}{2}C_p (V1^2 - V2^2)$$

By using a large reservoir capacitor, the output ripple can be reduced to an acceptable level. For example, if the load current is 5 mA and the accepted ripple is 200 mV, then the reservoir capacitor can omit approximately be calculated from:

$$Is = C_r \frac{dv}{dt}$$

$$\sim C_r \times \frac{V_{ripple\ p\text{-}p}}{4/F_{osc}} \qquad C_r = \frac{0.5\ mA}{0.5V/ms} = 10\ \mu F$$

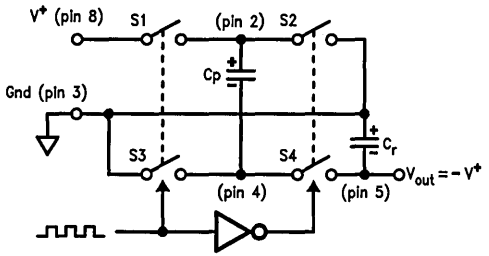
PRECAUTIONS

1) Do not exceed the maximum supply voltage or junction temperature.
2) Do not short pin 6 (LV terminal) to ground for supply voltages greater than 3.5V.
3) Do not short circuit the output to V^+.
4) External electrolytic capacitors C_r and C_p should have their polarities connected as shown in *Figure 1*.

REPLACING PREVIOUS 7660 DESIGNS

To prevent destructive latchup, previous 7660 designs require a diode in series with the output when operated at elevated temperature or supply voltage. Although this prevented the latchup problem of these designs, it lowered the available output voltage and increased the output series resistance.

The National LMC7660 has been designed to solve the inherent latch problem. The LCM7660 can operate over the



TL/H/9136-6

FIGURE 2. Idealized Voltage Converter

entire supply voltage and temperature range without the need for an output diode. When replacing existing designs, the LMC7660 can be operated with diode Dx.

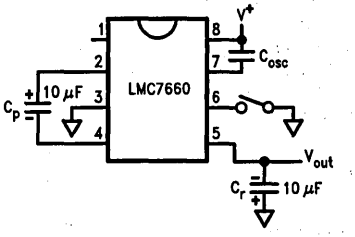
Typical Applications

Changing Oscillator Frequency

It is possible to dramatically reduce the quiescent operating current of the LMC7660 by lowering the oscillator frequency. The oscillator frequency can be lowered from a nominal 10 kHz to several hundred hertz, by adding a slow-down capacitor C_{osc} *(Figure 3)*. As shown in the Typical Performance Curves the supply current can be lowered to the 10 μA range. This low current drain can be extremely useful when used in μPower and battery back-up equipment. It must be understood that the lower operating frequency and supply current cause an increased impedance of C_r and C_p. The increased impedance, due to a lower switching rate, can be offset by raising C_r and C_p until ripple and load current requirements are met.

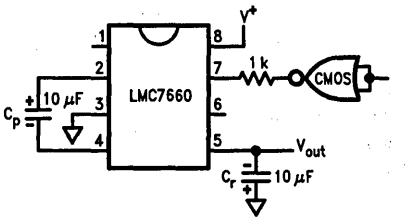
Synchronizing to an External Clock

Figure 4 shows an LMC7660 synchronized to an external clock. The CMOS gate overrides the internal oscillator when it is necessary to switch faster or reduce power supply interference. The external clock still passes through the ÷2 circuit in the 7660, so the pumping frequency will be ½ the external clock frequency.



TL/H/9136–7

FIGURE 3. Reduce Supply Current by Lowering Oscillator Frequency



TL/H/9136–8

FIGURE 4. Synchronizing to an External Clock

Typical Applications (Continued)

Lowering Output Impedance

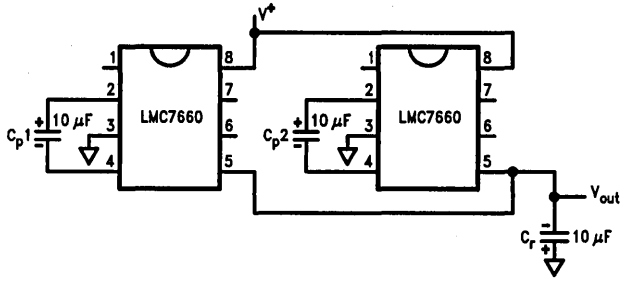
Paralleling two or more LMC7660's lowers output impedance. Each device must have it's own pumping capacitor C_p, but the reservoir capacitor C_r is shared as depicted in *Figure 5*. The composite output resistance is:

$$R_{out} = \frac{R_{out} \text{ of one LMC7660}}{\text{Number of devices}}$$

Increasing Output Voltage

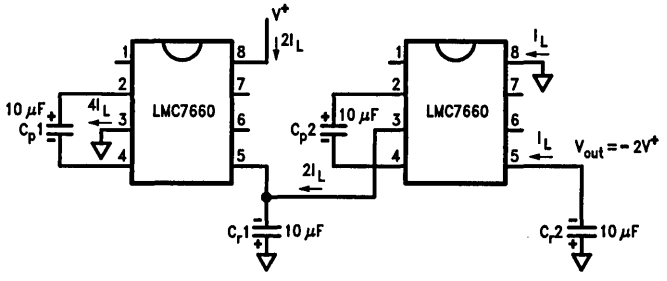
Stacking the LMC7660s is an easy way to produce a greater negative voltage. It should be noted that the input current required for each stage is twice the load current on that stage as shown in *Figure 6A*. The effective output resistance is approximately the sum of the individual R_{out} values, and so only a few levels of multiplication can be used.

It is possible to generate −15V from +5V by connecting the second 7660's pin 8 to +5V instead of ground as shown in *Figure 6B*. Note that the second 7660 sees a full 20V and the input supply should not be increased beyond +5V.



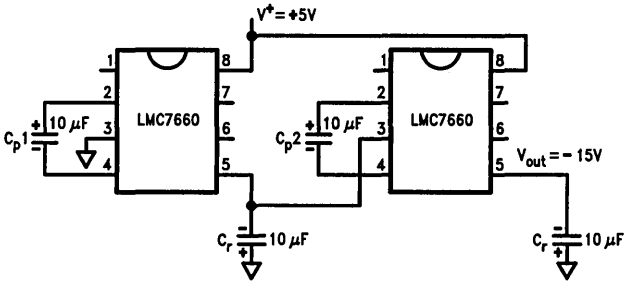
TL/H/9136–9

FIGURE 5. Lowering Output Resistance by Paralleling Devices



TL/H/9136–10

FIGURE 6A. Higher Voltage by Cascade



TL/H/9136–11

FIGURE 6B. Getting −15V from +5V

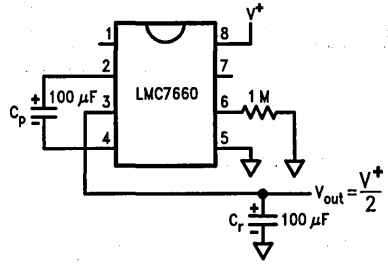
Typical Applications (Continued)

Split V^+ In Half

Figure 7 is one of the more interesting applications for the LMC7660. The circuit can be used as a precision voltage divider (for very light loads), alternately it is used to generate a ½ supply point in battery applications. In the ½ cycle when S1 and S3 are closed, the supply voltage divides across the capacitors in a conventional way proportional to their value. In the ½ cycle when S2 and S4 are closed, the capacitors switch from a series connection to a parallel connection. This forces the capacitors to have the same voltage; the charge redistributes to maintain precisely $V^+/2$, across C_p and C_r. In this application all devices are only $V^+/2$, and the supply voltage can be raised to 20V giving exactly 10V at V_{out}.

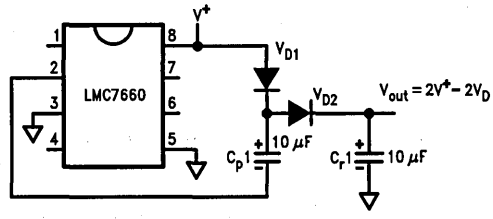
Getting Up . . . and Down

The LMC7660 can also be used as a positive voltage multiplier. This application, shown in *Figure 8*, requires 2 additional diodes. During the first ½ cycle S2 charges C_p1 through D1; D2 is reverse biased. In the next ½ cycle S2 is open and S1 is closed. Since C_p1 is charged to $V^+ - V_{D1}$ and is referenced to V^+ through S1, the junction of D1 and D2 is at $V^+ + (V^+ - V_{D1})$. D1 is reverse biased in this interval. This application uses only two of the four switches in the 7660. The other two switches can be put to use in performing a negative conversion at the same time as shown in *Figure 9*. In the ½ cycle that D1 is charging C_p1, C_p2 is connected from ground to $-V_{out}$ via S2 and S4, and C_r2 is storing C_p2's charge. In the interval that S1 and S3 are closed, C_p1 pumps the junction of D1 and D2 above V^+, while C_p2 is refreshed from V^+.



TL/H/9136–12

FIGURE 7. Split V^+ In Half



TL/H/9136–13

FIGURE 8. Positive Voltage Multiplier

Typical Applications (Continued)

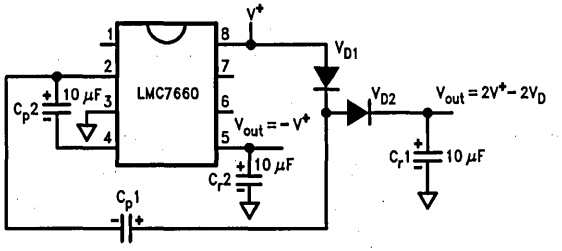


FIGURE 9. Combined Negative Converter and Positive Multiplier

Thermometer Spans 180°C

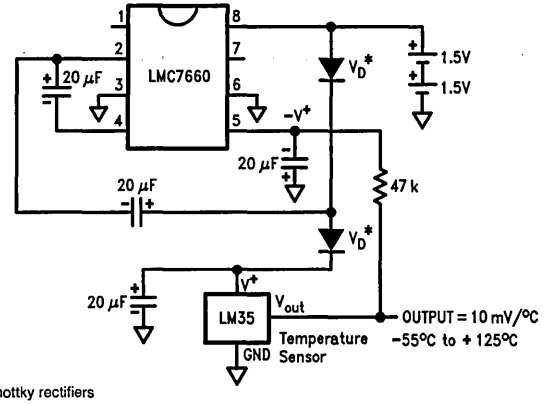
Using the combined negative and positive multiplier of *Figure 10* with an LM35 it is possible to make a μPower thermometer that spans a 180°C temperature range. The LM35 temperature sensor has an output sensitivity of 10 mV/°C, while drawing only 50 μA of quiescent current. In order for the LM35 to measure negative temperatures, a pull down to a negative voltage is required. *Figure 10* shows a thermometer circuit for measuring temperatures from −55°C to +125°C and requiring only two 1.5V cells. End of battery life can be extended by replacing the up converter diodes with Schottky's.

Regulating $-V_{out}$

It is possible to regulate the output of the LMC7660 and still maintain μPower performance. This is done by enclosing the LMC7660 in a loop with a LP2951. The circuit of *Figure 11* will regulate V_{out} to −5V for I_L = 10 mA, and V_{in} = 6V. For V_{in} > 7V, the output stays in regulation up to I_L = 25 mA. The error flag on pin 5 of the LP2951 sets low when the regulated output at pin 4 drops by about 5%. The LP2951 can be shutdown by taking pin 3 high; the LMC7660 can be shutdown by shorting pin 7 and pin 8.

The LP2951 can be reconfigured to an adjustable type regulator, which means the LMC7660 can give a regulated output from −2.0V to −10V dependent on the resistor ratios R1 and R2, as shown in *Figure 12*, V_{ref} = 1.235V:

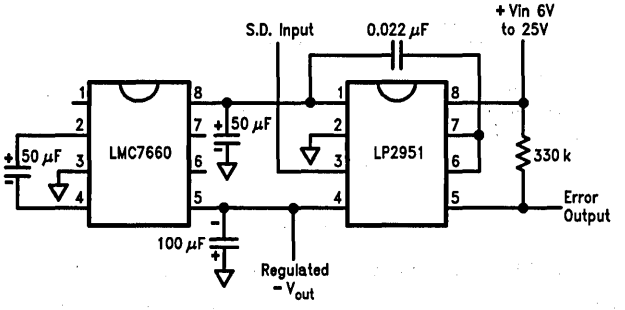
$$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right)$$



*For lower voltage operation, use Schottky rectifiers

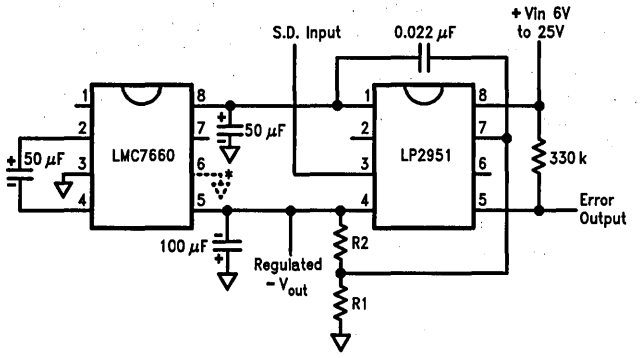
FIGURE 10. μPower Thermometer Spans 180°C, and Pulls Only 150 μA

Typical Applications (Continued)



TL/H/9136–16

FIGURE 11. Regulated −5V with 200 μA Standby Current



$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right)$

V_{ref} = 1.235V

*Low voltage operation

TL/H/9136–17

FIGURE 12. LMC7660 and LP2951 Make a Negative Adjustable Regulator

National Semiconductor

LM117A/LM117/LM317A/LM317 3-Terminal Adjustable Regulator

General Description

The LM117 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

For applications requiring greater output current, see LM150 series (3A) and LM138 series (5A) data sheets. For the negative complement, see LM137 series data sheet.

LM117 Series Packages and Power Capability

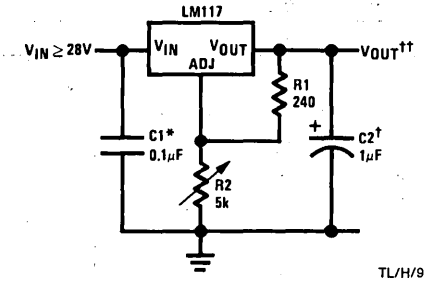
Part Number Suffix	Package	Rated Power Dissipation	Design Load Current
K	TO-3	20W	1.5A
H	TO-39	2W	0.5A
T	TO-220	20W	1.5A
MP	TO-202	2W	0.5A
E	LCC	2W	0.5A

Features

- Guaranteed 1% output voltage tolerance (LM117A, LM317A)
- Guaranteed max. 0.01%/V line regulation (LM117A, LM317A)
- Guaranteed max. 0.3% load regulation (LM117A, LM117)
- Guaranteed 1.5A output current
- Adjustable output down to 1.2V
- Current limit constant with temperature
- P+ Product Enhancement tested
- 80 dB ripple rejection
- Output is short-circuit protected

Typical Applications

1.2V–25V Adjustable Regulator



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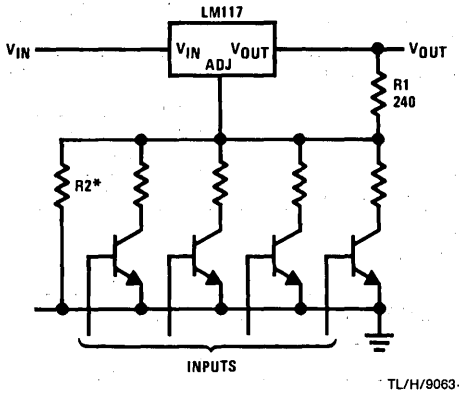
Full output current not available at high input-output voltages

*Needed if device is more than 6 inches from filter capacitors.

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

††$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$

Digitally Selected Outputs



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*Sets maximum V_{OUT}

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Power Dissipation	Internally Limited
Input-Output Voltage Differential	+40V, −0.3V
Storage Temperature	−65°C to +150°C
Lead Temperature	
Metal Package (Soldering, 10 seconds)	300°C
Plastic Package (Soldering, 4 seconds)	260°C
ESD Tolerance (Note 5)	3 kV

Operating Temperature Range

LM117A/LM117	$-55°C \le T_J \le +150°C$
LM317A	$-40°C \le T_J \le +125°C$
LM317	$0°C \le T_J \le +125°C$

Preconditioning

Thermal Limit Burn-In	All Devices 100%

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V, and I_{OUT} = 10 mA. (Note 3)

Parameter	Conditions	LM117A (Note 2)			LM117 (Note 2)			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage		1.238	1.250	1.262				V
	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10 mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	**1.225**	**1.250**	**1.270**	**1.20**	**1.25**	**1.30**	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$ (Note 4)		0.005	0.01		0.01	0.02	%/V
			0.01	**0.02**		**0.02**	**0.05**	%/V
Load Regulation	$10 mA \le I_{OUT} \le I_{MAX}$ (Note 4)		0.1	0.3		0.1	0.3	%
			0.3	**1**		**0.3**	**1**	%
Thermal Regulation	20 ms Pulse		0.03	0.07		0.03	0.07	%/W
Adjustment Pin Current			**50**	**100**		**50**	**100**	μA
Adjustment Pin Current Change	$10 mA \le I_{OUT} \le I_{MAX}$, $3V \le (V_{IN} - V_{OUT}) \le 40V$		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$		**3.5**	**5**		**3.5**	**5**	mA
Current Limit	$(V_{IN} - V_{OUT}) \le 15V$							
	K Package	**1.5**	**2.2**	**3.4**	**1.5**	**2.2**	**3.4**	A
	H, K Packages	**0.5**	**0.8**	**1.8**	**0.5**	**0.8**	**1.8**	A
	$(V_{IN} - V_{OUT}) = 40V$							
	K Package	0.3	0.4		0.3	0.4		A
	H, K Packages	0.15	0.2		0.15	0.2		A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.003			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF		**65**			**65**		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**66**	**80**		**66**	**80**		dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.3	1		0.3	1	%
Thermal Resistance, Junction-to-Case	K Package		2.3	3		2.3	3	°C/W
	H Package		12	15		12	15	°C/W
	E Package		5					°C/W
Thermal Resistance, Junction-to-Ambient (No Heat Sink)	K Package		35			35		°C/W
	H Package		140			140		°C/W
	E Package		88					°C/W

Electrical Characteristics (Continued)

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V, and I_{OUT} = 10 mA. (Note 3)

Parameter	Conditions	LM317A			LM317			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage		1.238	1.250	1.262				V
	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 40V, 10 mA ≤ I_{OUT} ≤ I_{MAX}, P ≤ P_{MAX}	**1.225**	**1.250**	**1.270**	**1.20**	**1.25**	**1.30**	V
Line Regulation	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 40V (Note 4)		0.005	0.01		0.01	0.04	%/V
			0.01	**0.02**		**0.02**	**0.07**	%/V
Load Regulation	10 mA ≤ I_{OUT} ≤ I_{MAX} (Note 4)		0.1	0.5		0.1	0.5	%
			0.3	**1**		**0.3**	**1.5**	%
Thermal Regulation	20 ms Pulse		0.04	0.07		0.04	0.07	%/W
Adjustment Pin Current			**50**	**100**		**50**	**100**	μA
Adjustment Pin Current Change	10 mA ≤ I_{OUT} ≤ I_{MAX}, 3V ≤ ($V_{IN} - V_{OUT}$) ≤ 40V		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	($V_{IN} - V_{OUT}$) = 40V		**3.5**	**10**		**3.5**	**10**	mA
Current Limit	($V_{IN} - V_{OUT}$) ≤ 15V							
	K, T Packages	**1.5**	**2.2**	**3.4**	**1.5**	**2.2**	**3.4**	A
	H, P Packages	**0.5**	**0.8**	**1.8**	**0.5**	**0.8**	**1.8**	A
	($V_{IN} - V_{OUT}$) = 40V							
	K, T Packages	0.15	0.4		0.15	0.4		A
	H, P Packages	0.075	0.2		0.075	0.2		A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.003			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF		**65**			**65**		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**66**	**80**		**66**	**80**		dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.3	1		0.3	1	%
Thermal Resistance, Junction-to-Case	K Package		2.3	3		2.3	3	°C/W
	H Package		12	15		12	15	°C/W
	T Package		4	5		4		°C/W
	P Package		7			7		°C/W
Thermal Resistance, Junction-to-Ambient (No Heat Sink)	K Package		35			35		°C/W
	H Package		140			140		°C/W
	T Package		50			50		°C/W
	P Package		80			80		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Refer to RETS117AH drawing for the LM117AH, the RETS117H drawing for the LM117H, the RETS117AK drawing for the LM117AK, or the RETS117K for the LM117K military specifications.

Note 3: Although power dissipation is internally limited, these specifications are applicable for maximum power dissipations of 2W for the TO-39 and TO-202, and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages and 0.5A for the TO-39 and TO-202 packages. All limits (i.e., the numbers in the Min. and Max. columns) are guaranteed to National's AOQL (Average Outgoing Quality Level).

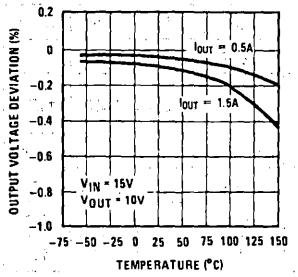
Note 4: Regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for thermal regulation.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

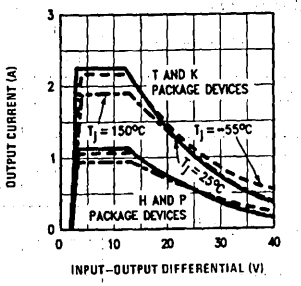
Typical Performance Characteristics

Output Capacitor = 0 μF unless otherwise noted

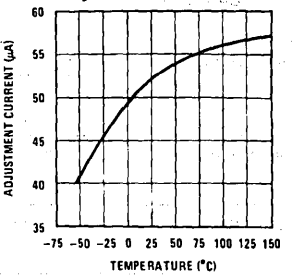
Load Regulation



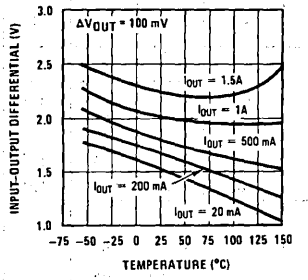
Current Limit



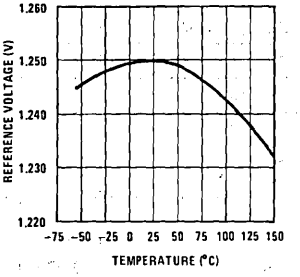
Adjustment Current



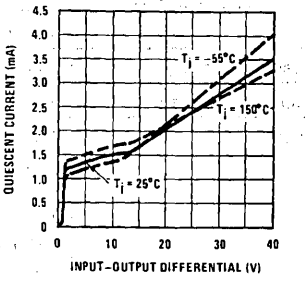
Dropout Voltage



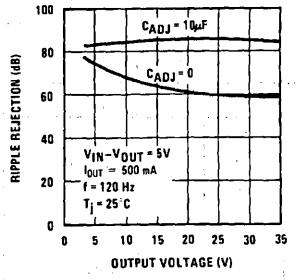
Temperature Stability



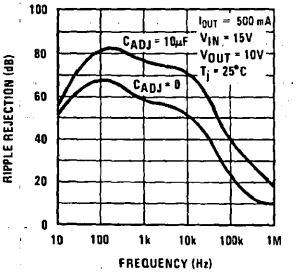
Minimum Operating Current



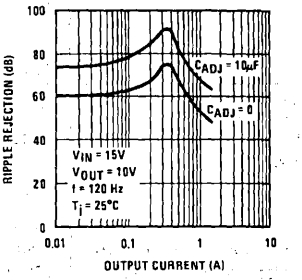
Ripple Rejection



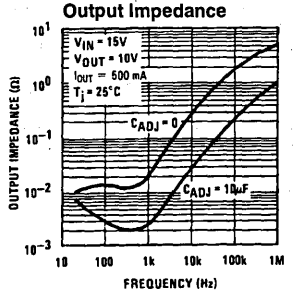
Ripple Rejection



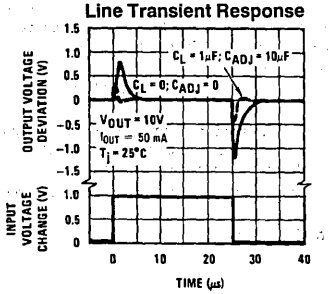
Ripple Rejection



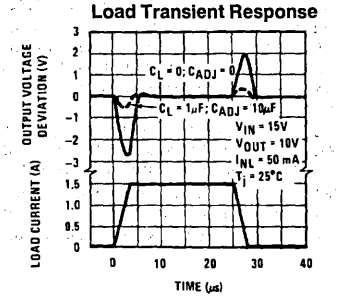
Output Impedance



Line Transient Response



Load Transient Response

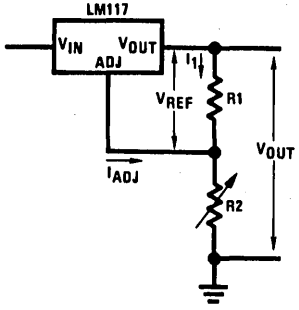


TL/H/9063–4

Application Hints

In operation, the LM117 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$



TL/H/9063–5

FIGURE 1

Since the 100 μA current from the adjustment terminal represents an error term, the LM117 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

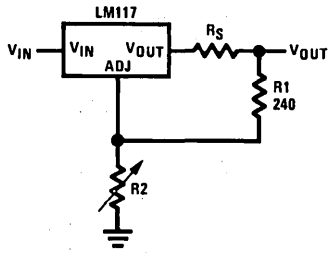
In general, the best type of capacitors to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of the load capacitance larger than 10 μF will merely improve the loop stability and output impedance.

Load Regulation

The LM117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9063–6

FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

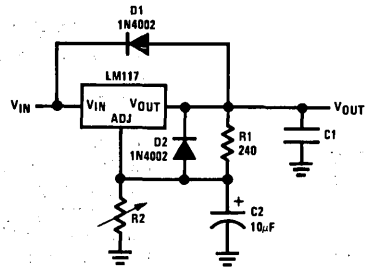
Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, there is no need to use diodes.

Application Hints (Continued)

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



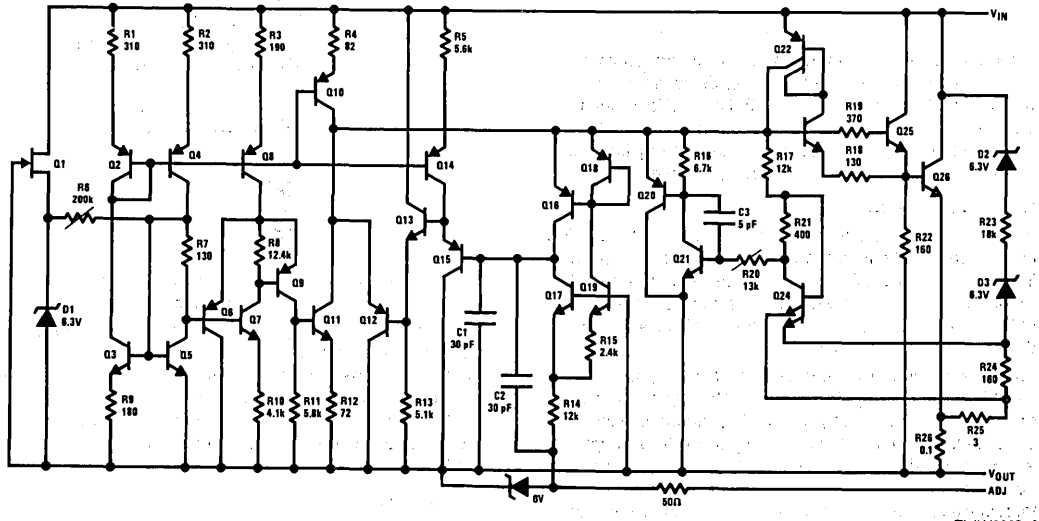
$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

D1 protects against C1
D2 protects against C2

TL/H/9063–7

FIGURE 3. Regulator with Protection Diodes

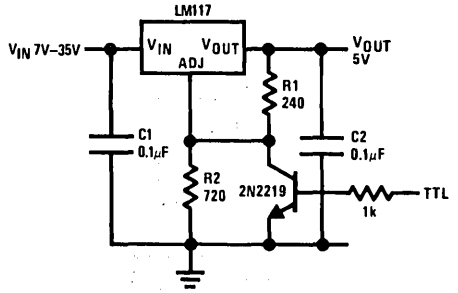
Schematic Diagram



TL/H/9063–8

Typical Applications (Continued)

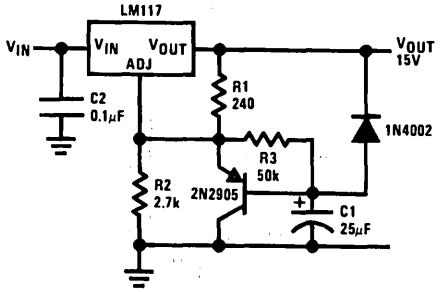
5V Logic Regulator with Electronic Shutdown*



*Min. output ≈ 1.2V

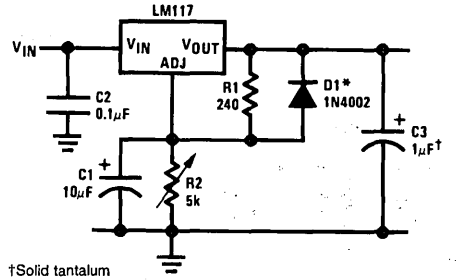
TL/H/9063-3

Slow Turn-On 15V Regulator



TL/H/9063-9

Adjustable Regulator with Improved Ripple Rejection

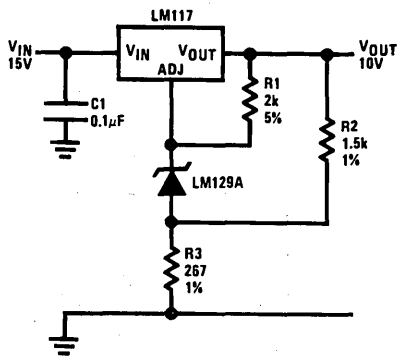


†Solid tantalum

*Discharges C1 if output is shorted to ground

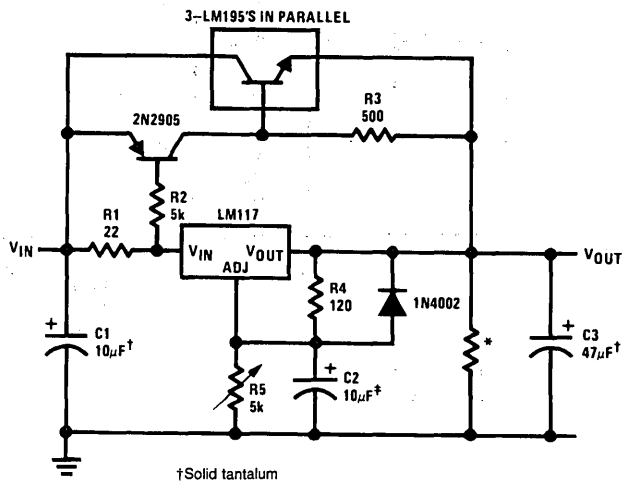
TL/H/9063-10

High Stability 10V Regulator



TL/H/9063-11

High Current Adjustable Regulator



†Solid tantalum

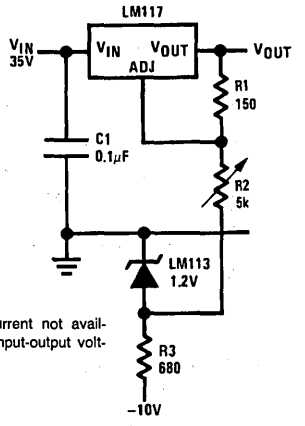
*Minimum load current = 30 mA

‡Optional—improves ripple rejection

TL/H/9063-12

Typical Applications (Continued)

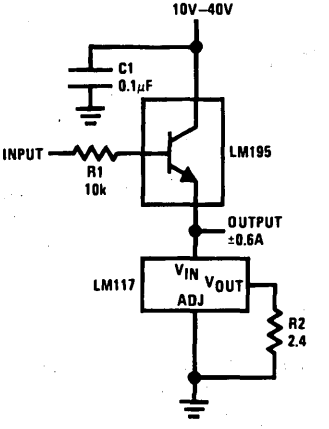
0 to 30V Regulator



Full output current not available at high input-output voltages

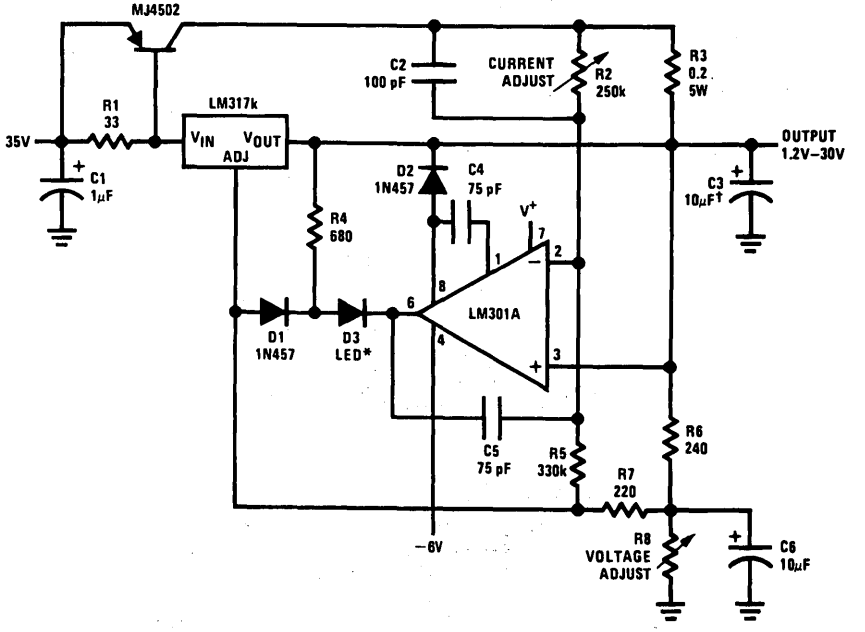
TL/H/9063–13

Power Follower



TL/H/9063–14

5A Constant Voltage/Constant Current Regulator



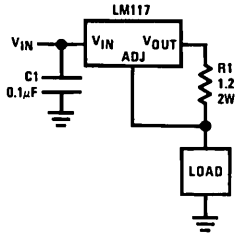
†Solid tantalum

*Lights in constant current mode

TL/H/9063–15

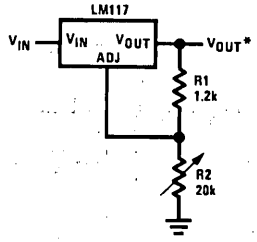
Typical Applications (Continued)

1A Current Regulator



TL/H/9063–16

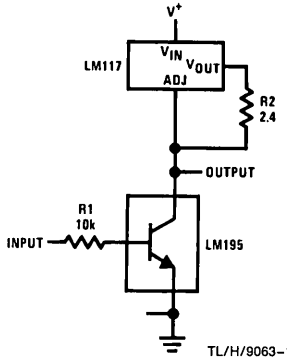
1.2V–20V Regulator with Minimum Program Current



TL/H/9063–17

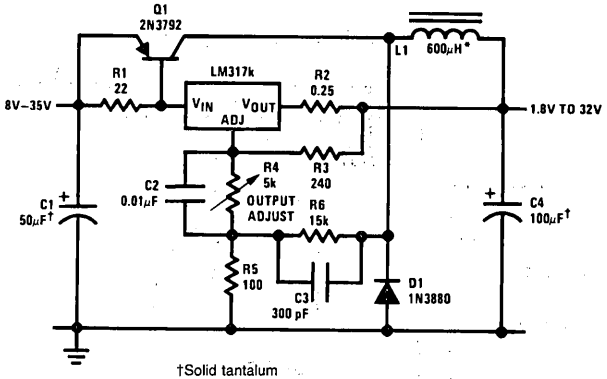
*Minimum load current ≈ 4 mA

High Gain Amplifier



TL/H/9063–18

Low Cost 3A Switching Regulator

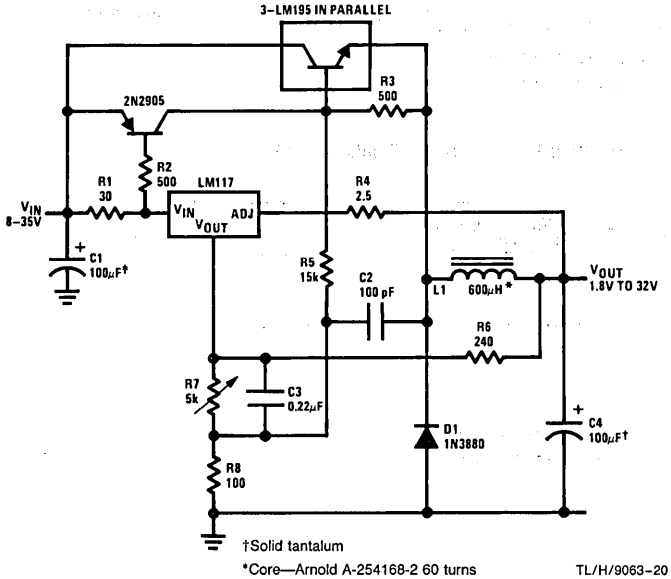


†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9063–19

4A Switching Regulator with Overload Protection

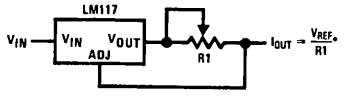


†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9063–20

Precision Current Limiter

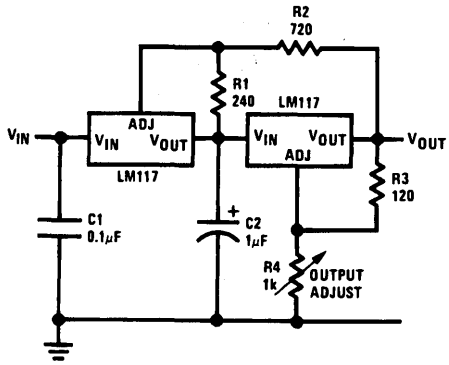


*0.8Ω ≤ R1 ≤ 120Ω

TL/H/9063–21

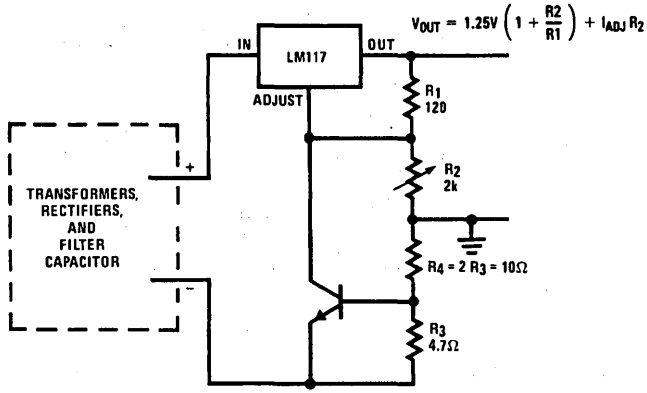
Typical Applications (Continued)

Tracking Preregulator



TL/H/9063-22

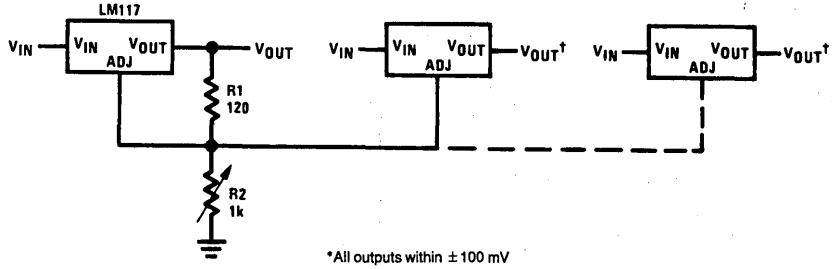
Current Limited Voltage Regulator



TL/H/9063-23

– Short circuit current is approximately $\frac{600\ mV}{R3}$, or 120 mA
(Compared to LM117's higher current limit)
– At 50 mA output only ¾ volt of drop occurs in R_3 and R_4

Adjusting Multiple On-Card Regulators with Single Control*

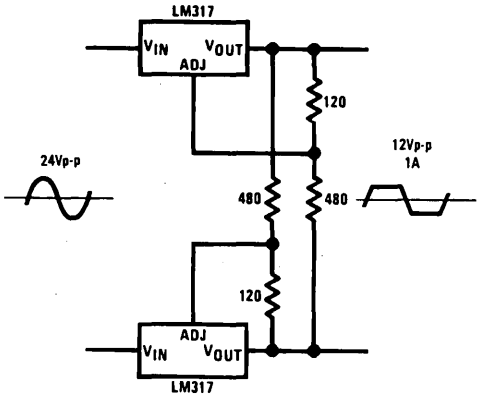


*All outputs within ±100 mV
†Minimum load—10 mA

TL/H/9063-24

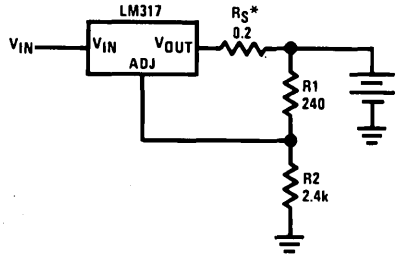
Typical Applications (Continued)

AC Voltage Regulator



TL/H/9063-25

12V Battery Charger

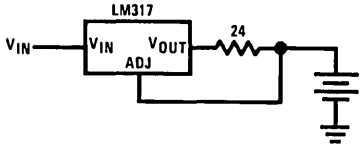


TL/H/9063-26

*R_S—sets output impedance of charger: $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

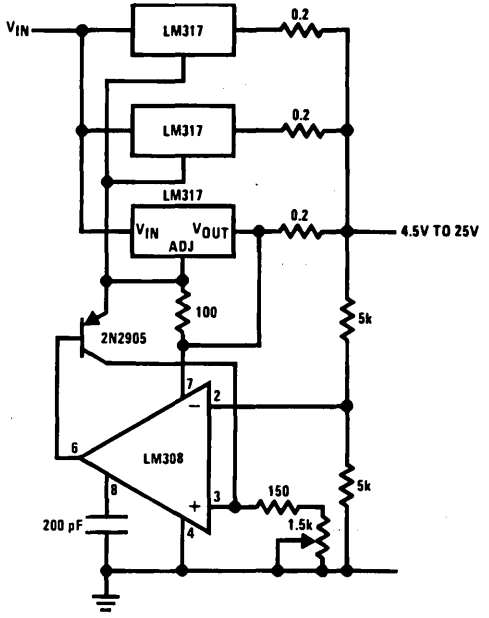
Use of R_S allows low charging rates with fully charged battery.

50 mA Constant Current Battery Charger



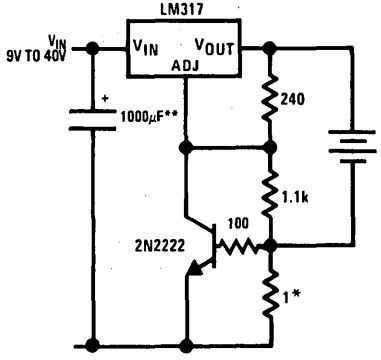
TL/H/9063-27

Adjustable 4A Regulator



TL/H/9063-28

Current Limited 6V Charger



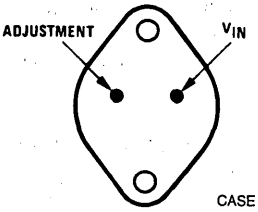
TL/H/9063-29

*Sets peak current (0.6A for 1Ω)

**The 1000 μF is recommended to filter out input transients

Connection Diagrams

(TO-3)
Metal Can Package



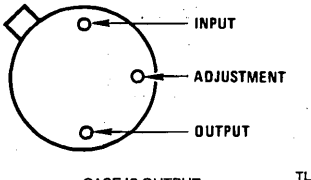
TL/H/9063-30

Bottom View

Steel Package
Order Number LM117AK STEEL, LM117AK/883, LM117K STEEL, LM117K STEEL/883, LM317AK STEEL or LM317K STEEL
See NS Package Number K02A

Aluminum Package
Order Number LM317KC
See NS Package Number KC02A

(TO-39)
Metal Can Package

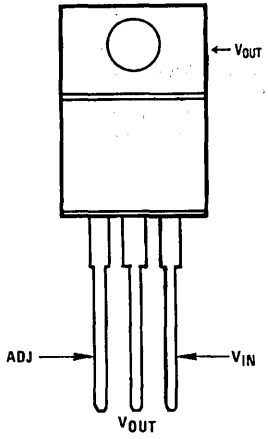


TL/H/9063-31

Bottom View

Order Number LM117AH, LM117AH/883, LM117H, LM117H/883, LM317AH or LM317H
See NS Package Number H03A

(TO-220)
Plastic Package

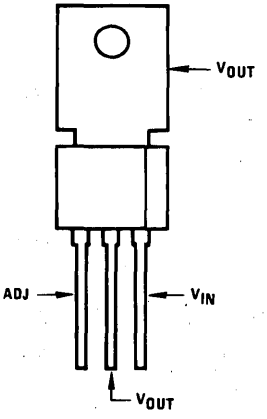


TL/H/9063-32

Front View

Order Number LM317AT or LM317T
See NS Package Number T03B

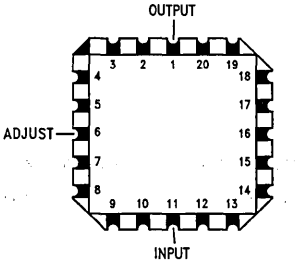
(TO-202)
Plastic Package



TL/H/9063-33

Front View

Order Number LM317AMP or LM317MP
See NS Package Number P03A



TL/H/9063-34

Top View

Order Number LM117E/883
See NS Package Number E20A

National Semiconductor

LM117HV/LM317HV 3-Terminal Adjustable Regulator

General Description

The LM117HV/LM317HV are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 57V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117HV is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117HV series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117HV is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e. do not short the output to ground.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117HV can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

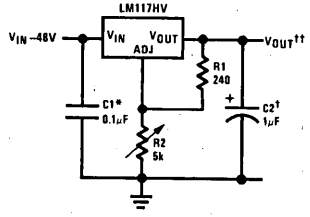
The LM117HVK STEEL and LM317HVK STEEL are packaged in standard TO-3 transistor packages, while the LM117HVH and LM317HVH are packaged in a solid Kovar base TO-39 transistor package. The LM317HVT uses a TO-220 plastic package. The LM117HV is rated for operation from −55°C to +150°C, and the LM317HV from 0°C to +125°C.

Features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short-circuit protected

Typical Applications

1.2V–45V Adjustable Regulator



TL/H/9062–1

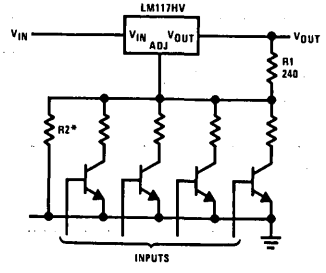
Full output current not available at high input-output voltages

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 inches from filter capacitors.

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R_2$$

Digitally Selected Outputs



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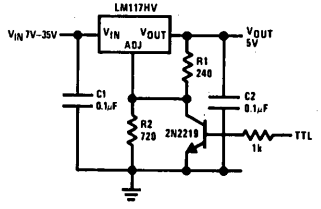
*Sets maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



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*Min. output ≈ 1.2V

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 3)

Power Dissipation	Internally limited
Input—Output Voltage Differential	+60V, −0.3V
Operating Junction Temperature Range	
LM117HV	−55°C to +150°C
LM317HV	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Preconditioning Burn-In in Thermal Limit	100% All Devices
ESD Tolerance (Note 4)	2000V

Electrical Characteristics (Note 1)

Parameter	Conditions	LM117HV			LM317HV			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	T_J = 25°C, 3V ≤ V_{IN} − V_{OUT} ≤ 60V (Note 2) I_L = 10 mA		0.01	0.02		0.01	0.04	%/V
Load Regulation	T_J = 25°C, 10 mA ≤ I_{OUT} ≤ I_{MAX}		0.1	0.3		0.1	0.5	%
Thermal Regulation	T_J = 25°C, 20 ms Pulse		0.03	0.07		0.04	0.07	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	10 mA ≤ I_L ≤ I_{MAX} 3.0 V ≤ (V_{IN} − V_{OUT}) ≤ 60V		0.2	5		0.2	5	μA
Reference Voltage	3.0 V ≤ (V_{IN} − V_{OUT}) ≤ 60V, (Note 3) 10 mA ≤ I_{OUT} ≤ I_{MAX}, P ≤ P_{MAX}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	3.0V ≤ (V_{IN} − V_{OUT}) ≤ 60V, I_L = 10 mA, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	10 mA ≤ I_{OUT} ≤ I_{MAX} (Note 2)		0.3	1		0.3	1.5	%
Temperature Stability	T_{MIN} ≤ T_J ≤ T_{MAX}		1			1		%
Minimum Load Current	(V_{IN} − V_{OUT}) = 60V		3.5	7		3.5	12	mA
Current Limit	(V_{IN} − V_{OUT}) ≤ 15V							
	K, T Packages	1.5	2.2	3.5	1.5	2.2	3.7	A
	H Package	0.5	0.8	1.8	0.5	0.8	1.9	A
	(V_{IN} − V_{OUT}) ≤ 60V							
	K, T Packages		0.1			0.1		A
	H Package		0.03			0.03		A
RMS Output Noise, % of V_{OUT}	T_J = 25°C, 10 Hz ≤ f ≤ 10 kHz		0.003			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz		65			65		dB
	C_{ADJ} = 10 μF	66	80		66	80		dB
Long-Term Stability	T_J = 125°C		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	°C/W
	T Package		4	5		4		°C/W
	K Package		2.3	3		2.3	3	°C/W
Thermal Resistance, Junction to Ambient (no heat sink)	H Package		140			140		°C/W
	T Package		50			50		°C/W
	K Package		35			35		°C/W

Note 1: Unless otherwise specified, these specifications apply: −55°C ≤ T_J ≤ +150°C for the LM117HV, and 0°C ≤ T_J ≤ +125°C for the LM317HV; V_{IN} − V_{OUT} = 5V and I_{OUT} = 0.1A for the TO-39 package and I_{OUT} = 0.5A for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 and 0.5A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

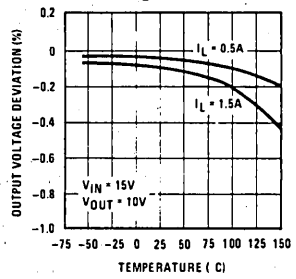
Note 3: Refer to RETS117HVH for LM117HVH or RETS117HVK for LM117HVK military specificatioins.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

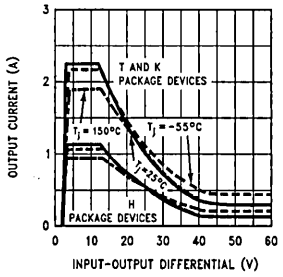
Typical Performance Characteristics

Output capacitor = 0 μF unless otherwise noted.

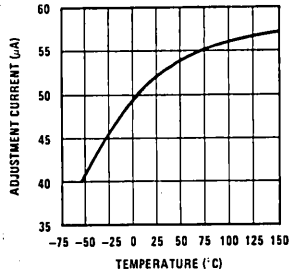
Load Regulation



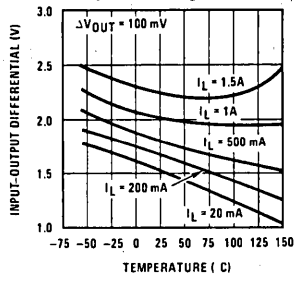
Current Limit



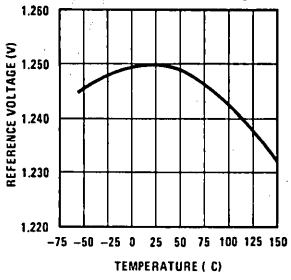
Adjustment Current



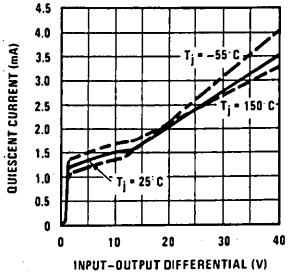
Dropout Voltage



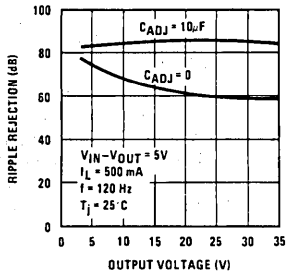
Temperature Stability



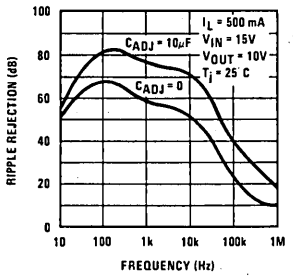
Minimum Operating Current



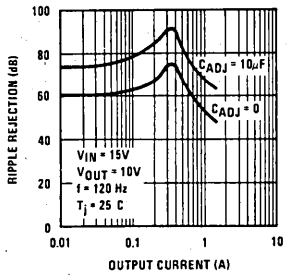
Ripple Rejection



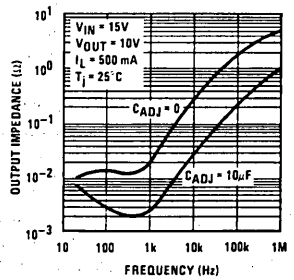
Ripple Rejection



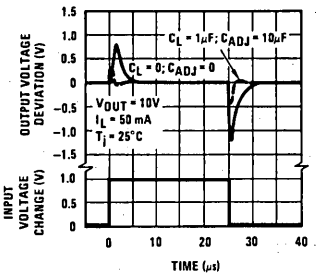
Ripple Rejection



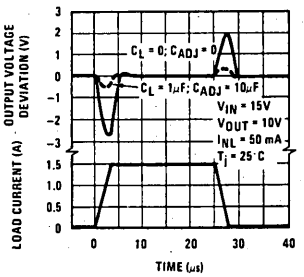
Output Impedance



Line Transient Response



Load Transient Response



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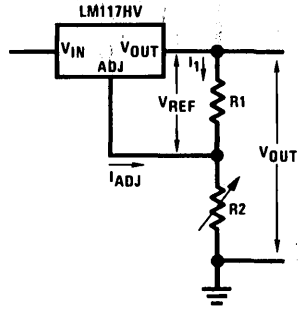
4

Application Hints

In operation, the LM117HV develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$



TL/H/9062–5

FIGURE 1

Since the 100 μA current from the adjustment terminal represents an error term, the LM117HV was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possiblity of problems.

The adjustment terminal can be bypassed to ground on the LM117HV to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

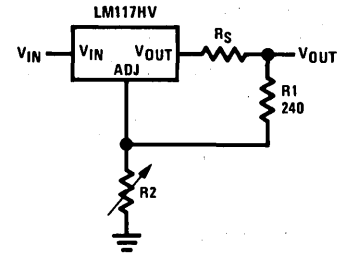
In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM117HV is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of load capacitance larger than 10 μF will merely improve the loop stability and output impedance.

Load Regulation

The LM117HV is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of $0.05\Omega \times I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9062–6

FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

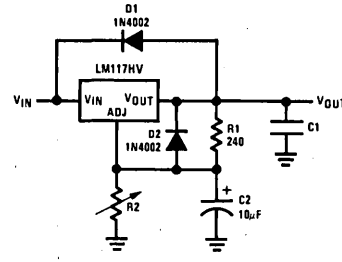
When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117HV, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117HV is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM117HV with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

Current Limit

Internal current limit will be activated whenever the output current exceeds the limit indicated in the Typical Performance Characteristics. However, if during a short circuit condition the regulator's differential voltage exceeds the Absolute Maximum Rating of 60V (e.g. $V_{IN} \geq 60V$, $V_{OUT} = 0V$), internal junctions in the regulator may break down and the device may be damaged or fail. Failure modes range from an apparent open or short from input to output of the regulator, to a destroyed package (most common with the TO-220 package). To protect the regulator, the user is advised to be aware of voltages that may be applied to the regulator during fault conditions, and to avoid violating the Absolute Maximum Ratings.



TL/H/9062–7

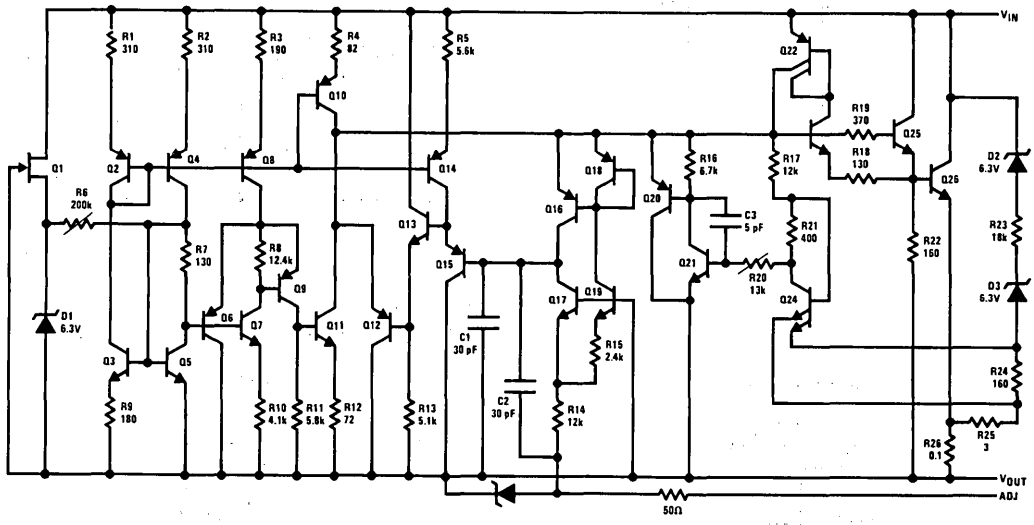
FIGURE 3. Regulator with Protection Diodes

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

D1 protects against C1

D2 protects against C2

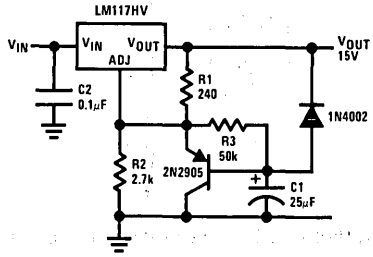
Schematic Diagram



TL/H/9062–8

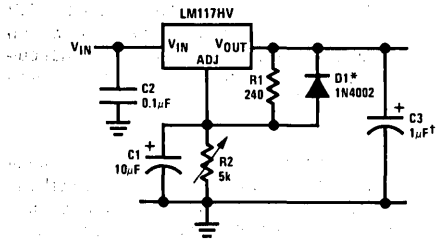
Typical Applications (Continued)

Slow Turn-On 15V Regulator



TL/H/9062–9

Adjustable Regulator with Improved Ripple Rejection

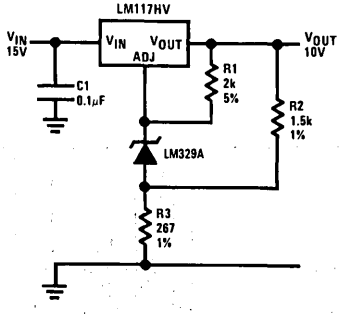


TL/H/9062–10

†Solid tantalum

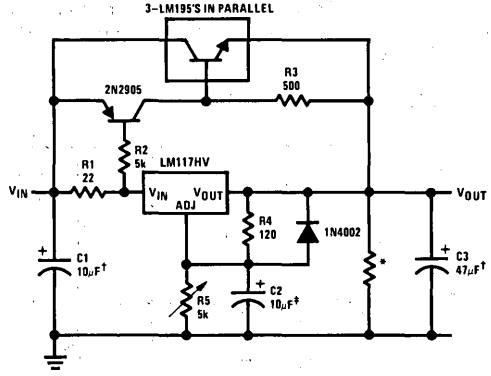
*Discharges C1 if output is shorted to ground

High Stability 10V Regulator



TL/H/9062–11

High Current Adjustable Regulator



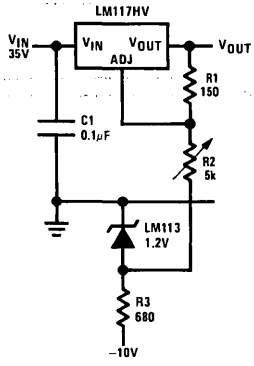
TL/H/9062–12

†Solid tantalum

*Minimum load current = 30 mA

‡Optional—improves ripple rejection

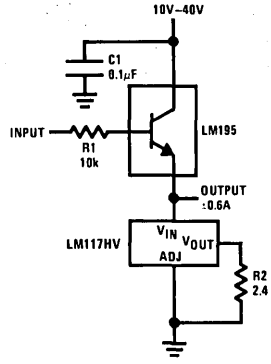
0 to 30V Regulator



TL/H/9062–13

Full output current not available at high input-output voltages

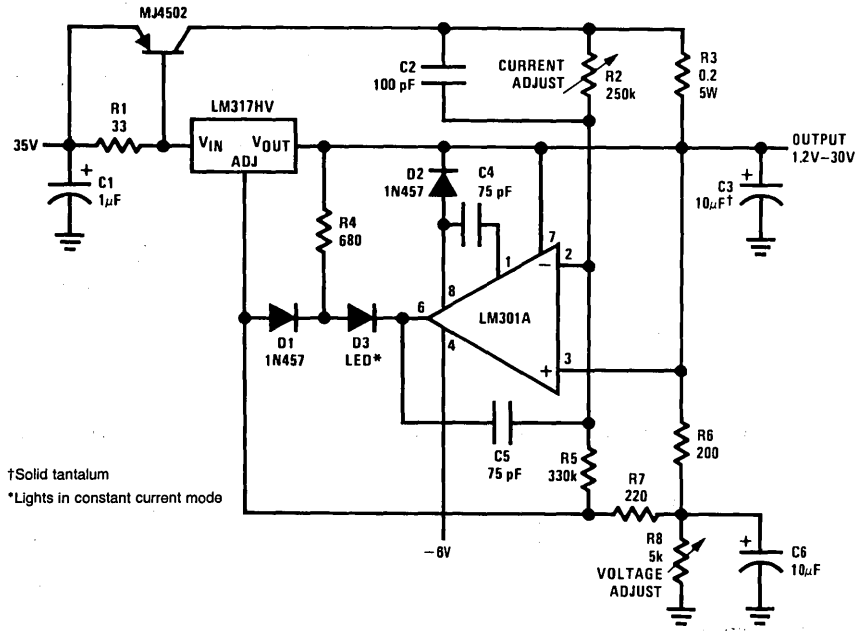
Power Follower



TL/H/9062–14

Typical Applications (Continued)

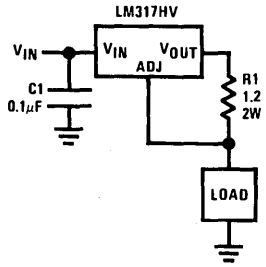
5A Constant Voltage/Constant Current Regulator



†Solid tantalum
*Lights in constant current mode

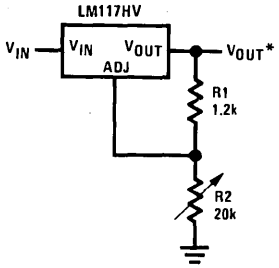
TL/H/9062–15

1A Current Regulator



TL/H/9062–16

1.2V–20V Regulator with Minimum Program Current

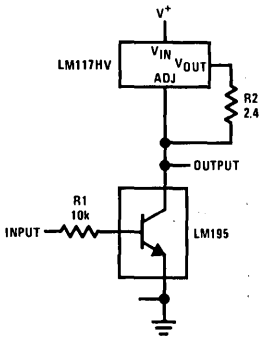


TL/H/9062–17

*Minimum load current ≈ 4 mA

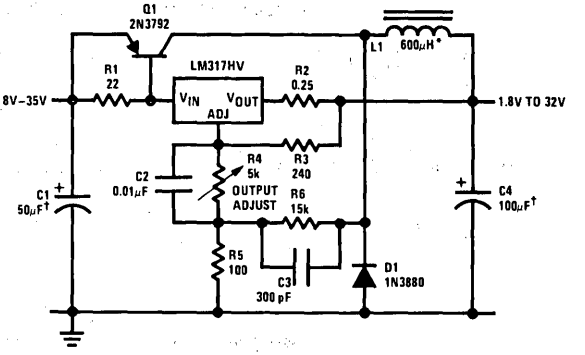
Typical Applications (Continued)

High Gain Amplifier



TL/H/9062–18

Low Cost 3A Switching Regulator

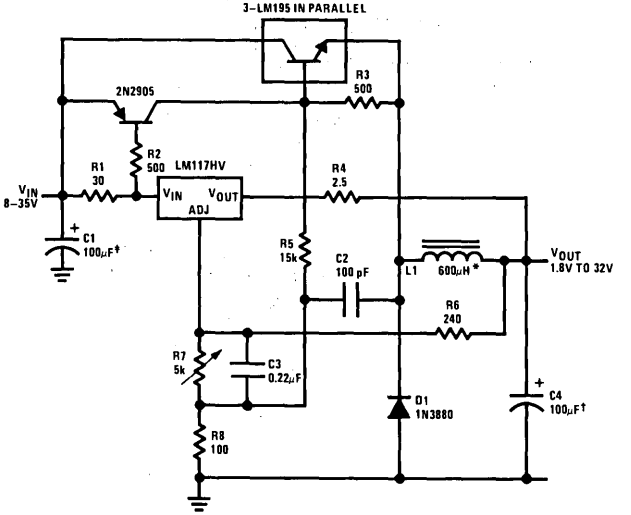


†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9062–19

4A Switching Regulator with Overload Protection

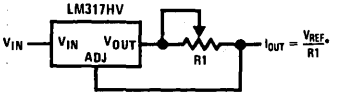


†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9062–20

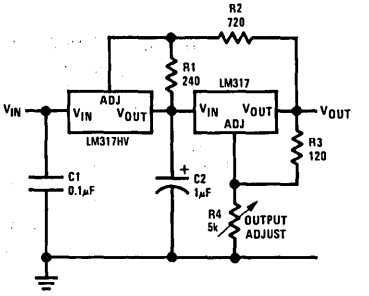
Precision Current Limiter



TL/H/9062–21

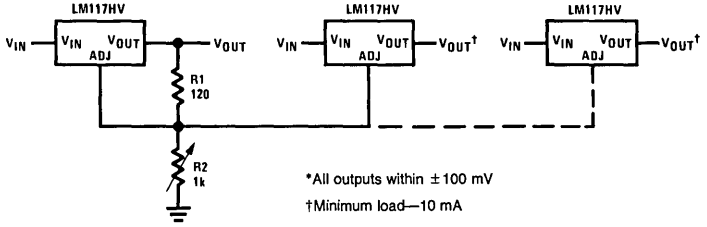
*0.8Ω ≤ R1 ≤ 120Ω

Tracking Preregulator



TL/H/9062–22

Adjustable Multiple On-Card Regulators with Single Control*



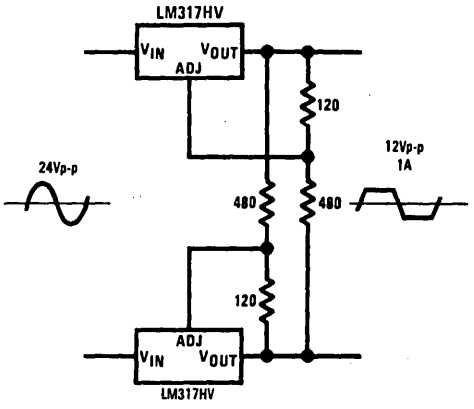
*All outputs within ±100 mV

†Minimum load—10 mA

TL/H/9062–23

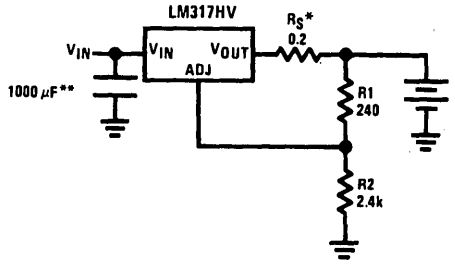
Typical Applications (Continued)

AC Voltage Regulator



TL/H/9062-24

12V Battery Charger



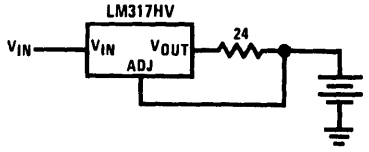
TL/H/9062-25

*R_S—sets output impedance of charger $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

Use of R_S allows low charging rates with fully charged battery.

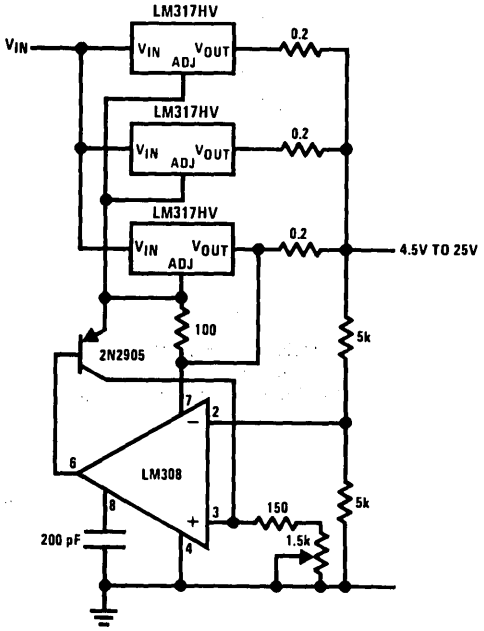
**The 1000 μF is recommended to filter out input transients

50 mA Constant Current Battery Charger



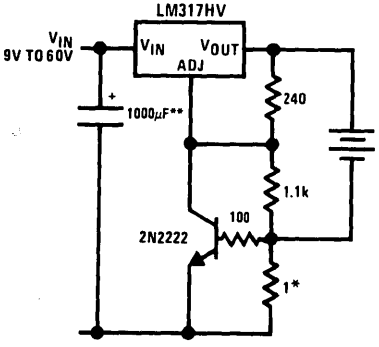
TL/H/9062-26

Adjustable 4A Regulator



TL/H/9062-27

Current Limited 6V Charger



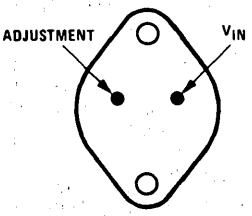
TL/H/9062-28

*Sets peak current (0.6A for 1Ω)

**The 1000 μF is recommended to filter out input transients

Connection Diagrams (See Physical Dimension section for further information)

(TO-3 Steel)
Metal Can Package

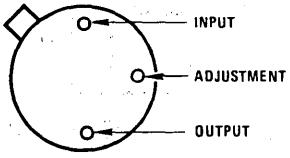


TL/H/9062-29

Case Is Output
Bottom View

Order Number LM117HVK STEEL,
LM317HVK STEEL
See NS Package Number K02A

(TO-39)
Metal Can Package

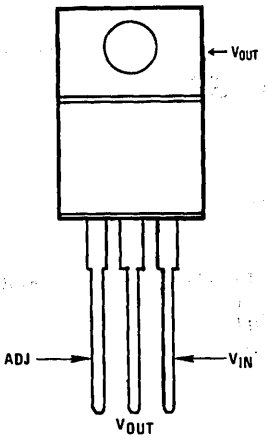


TL/H/9062-30

Case Is Output
Bottom View

Order Number LM117HVH,
or LM317HVH
See NS Package Number H03A

(TO-220 Steel)
Plastic Package



TL/H/9062-31

Front View

Order Number LM317HVT
See NS Package Number T03B

National Semiconductor

LM317L 3-Terminal Adjustable Regulator

General Description

The LM317L is an adjustable 3-terminal positive voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM317L is available packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM317L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short circuit protected

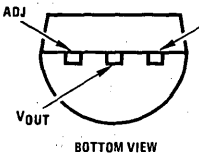
Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM317L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

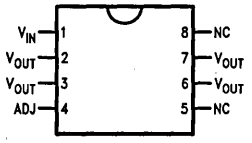
The LM317L is available in a standard TO-92 transistor package and the SO-8 package. The LM317L is rated for operation over a −25°C to 125°C range.

Connection Diagram



TL/H/9064-4

Order Number LM317LZ
See NS Package
Number Z03A

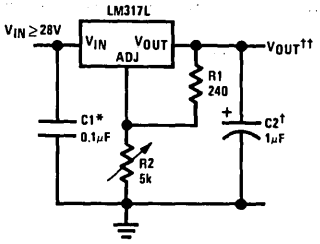


TL/H/9064-5

Order Number LM317LM
See NS Package
Number M08A

Typical Applications

1.2V–25V Adjustable Regulator



TL/H/9064-1

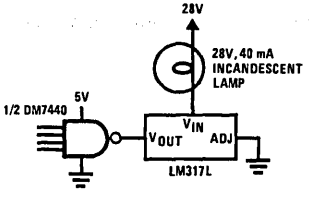
Full output current not available at high input-output voltages

†Optional—improves transient response

*Needed if device is more than 6 inches from filter capacitors

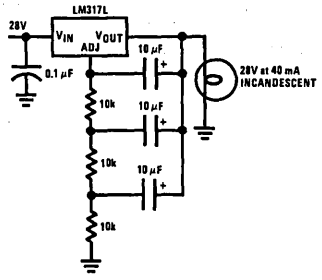
$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

Fully Protected (Bulletproof) Lamp Driver



TL/H/9064-2

Lamp Flasher



TL/H/9064-3

Output rate—4 flashes per second at 10% duty cycle

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Output is Short Circuit Protected

ESD rating to be determined.

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Line Regulation	$T_j = 25°C$, $3V \le (V_{IN} - V_{OUT}) \le 40V$, $I_L \le 20$ mA (Note 2)		0.01	0.04	%/V
Load Regulation	$T_j = 25°C$, 5 mA $\le I_{OUT} \le I_{MAX}$, (Note 2)		0.1	0.5	%
Thermal Regulation	$T_j = 25°C$, 10 ms Pulse		0.04	0.2	%/W
Adjustment Pin Current			50	100	μA
Adjustment Pin Current Change	5 mA $\le I_L \le$ 100 mA $3V \le (V_{IN} - V_{OUT}) \le 40V$, P ≤ 625 mW		0.2	5	μA
Reference Voltage	$3V \le (V_{IN} - V_{OUT}) \le 40V$, (Note 3) 5 mA $\le I_{OUT} \le$ 100 mA, P ≤ 625 mW	1.20	1.25	1.30	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $I_L \le 20$ mA (Note 2)		0.02	0.07	%/V
Load Regulation	5 mA $\le I_{OUT} \le$ 100 mA, (Note 2)		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{Max}$		0.65		%
Minimum Load Current	$(V_{IN} - V_{OUT}) \le 40V$ $3V \le (V_{IN} - V_{OUT}) \le 15V$		3.5 1.5	5 2.5	mA
Current Limit	$3V \le (V_{IN} - V_{OUT}) \le 13V$ $(V_{IN} - V_{OUT}) = 40V$	100 25	200 50	300 150	mA mA
Rms Output Noise, % of V_{OUT}	$T_j = 25°C$, 10 Hz ≤ f ≤ 10 kHz		0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, $C_{ADJ} = 0$ C_{ADJ} = 10 μF	 66	65 80		dB dB
Long-Term Stability	$T_j = 125°C$, 1000 Hours		0.3	1	%
Thermal Resistance Junction to Ambient	Z Package 0.4" Leads Z Package 0.125 Leads SO-8 Package		180 160 165		°C/W °C/W °C/W
Thermal Rating of SO Package			165		°C/W

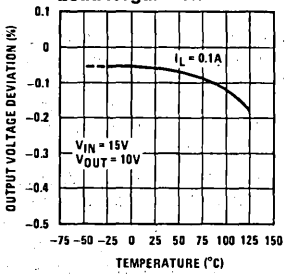
Note 1: Unless otherwise noted, these specifications apply: $-25°C \le T_j \le 125°C$ for the LM317L; $V_{IN} - V_{OUT} = 5V$ and I_{OUT} = 40 mA. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 625 mW. I_{MAX} is 100 mA.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

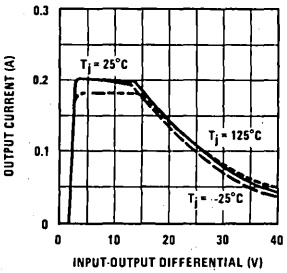
Note 3: Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to PC board.

Typical Performance Characteristics (Output capacitor = 0 μF unless otherwise noted.)

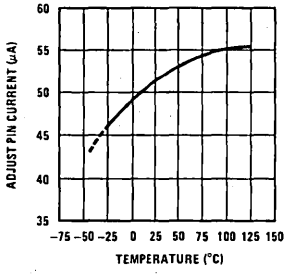
Load Regulation



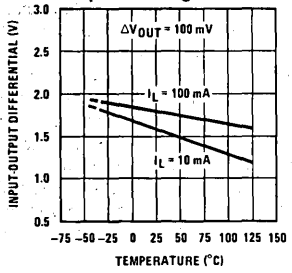
Current Limit



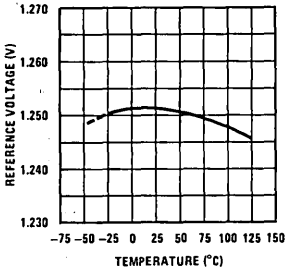
Adjustment Current



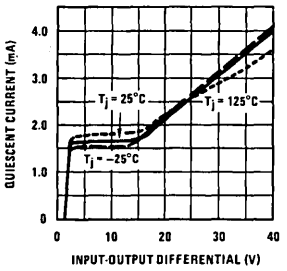
Dropout Voltage



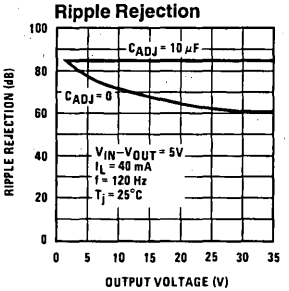
Reference Voltage Temperature Stability



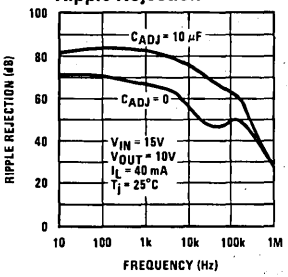
Minimum Operating Current



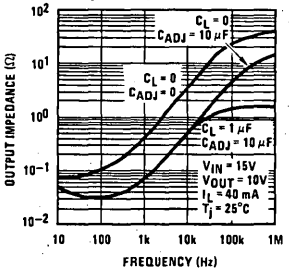
Ripple Rejection



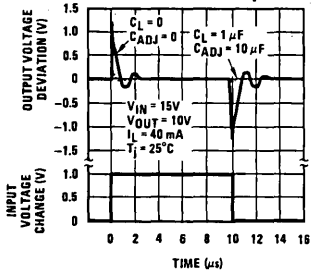
Ripple Rejection



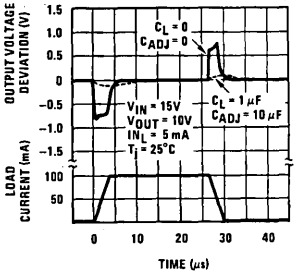
Output Impedance



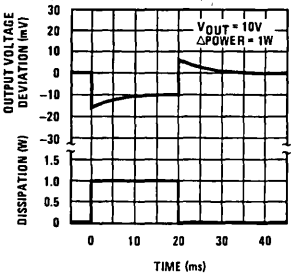
Line Transient Response



Load Transient Response



Thermal Regulation



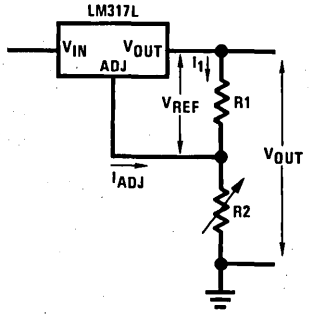
TL/H/9064–6

Application Hints

In operation, the LM317L develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R2)$$

Since the 100 μA current from the adjustment terminal represents an error term, the LM317L was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.



TL/H/9064–7

FIGURE 1

External Capacitors

An input bypass capacitor is recommended in case the regulator is more than 6 inches away from the usual large filter capacitor. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used, but the above values will eliminate the possiblity of problems.

The adjustment terminal can be bypassed to ground on the LM317L to improve ripple rejection and noise. This bypass capacitor prevents ripple and noise from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use is solid tantalum. *Solid tantalum capacitors have low impedance even at high frequencies.* Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, a 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

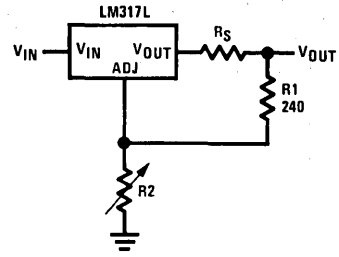
Although the LM317L is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM317L is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of $0.05\Omega \times I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

With the TO-92 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the output pin. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.



TL/H/9064–8

FIGURE 2. Regulator with Line Resistance in Output Lead

Application Hints (Continued)

Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per watt, within the first 10 ms after a step of power is applied. The LM317L specification is 0.2%/W, maximum.

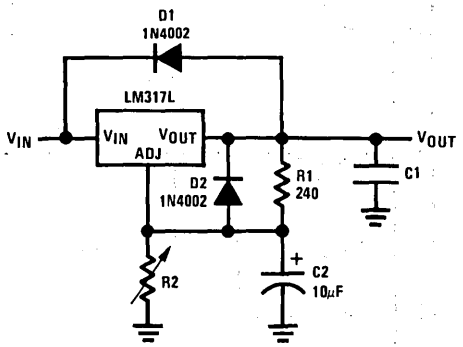
In the Thermal Regulation curve at the bottom of the Typical Performance Characteristics page, a typical LM317L's output changes only 7 mV (or 0.07% of $V_{OUT} = -10V$) when a 1W pulse is applied for 10 ms. This performance is thus well inside the specification limit of $0.2\%/W \times 1W = 0.2\%$ maximum. When the 1W pulse is ended, the thermal regulation again shows a 7 mV change as the gradients across the LM317L chip die out. Note that the load regulation error of about 14 mV (0.14%) is additional to the thermal regulation error.

Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM317L, this discharge path is through a large junction that is able to sustain a 2A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, the LM317L's ballast resistors and output structure limit the peak current to a low enough level so that there is no need to use a protection diode.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM317L is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM317L with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



TL/H/9064–9

FIGURE 3. Regulator with Protection Diodes

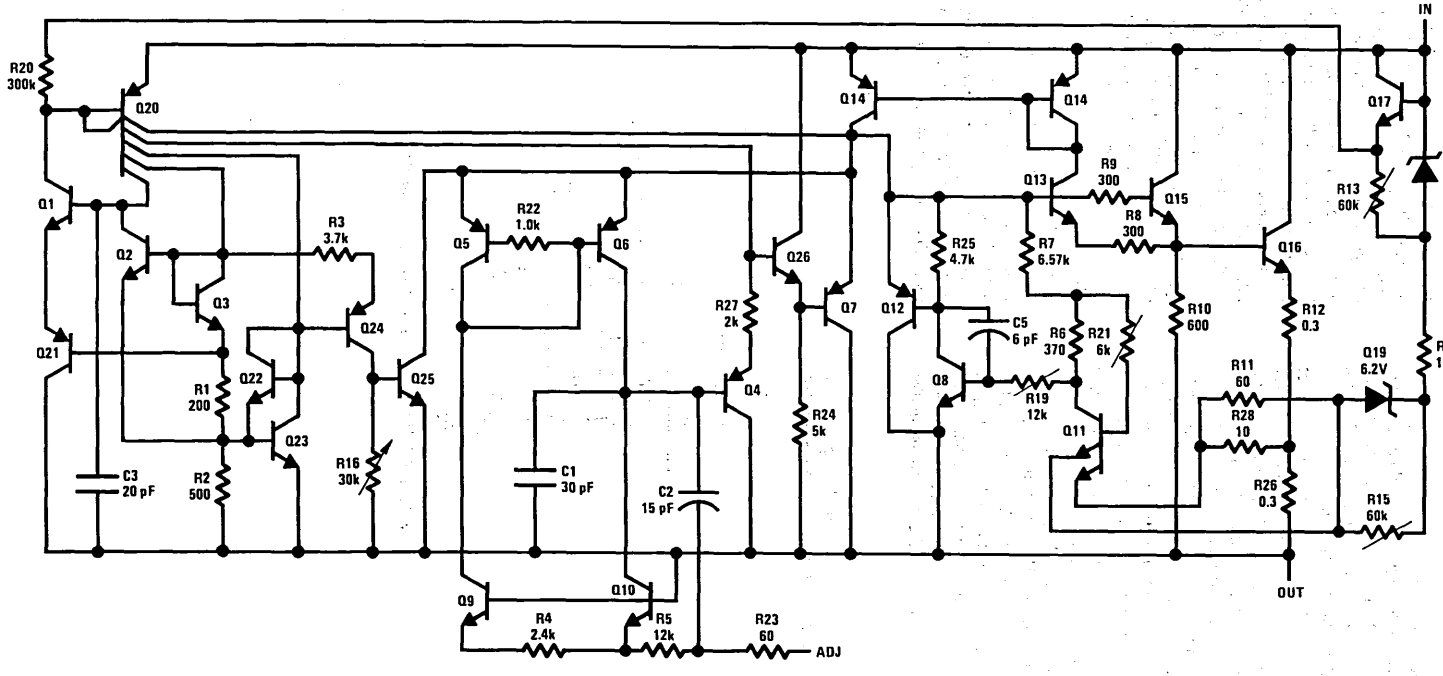
$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$

D1 protects against C1

D2 protects against C2

4

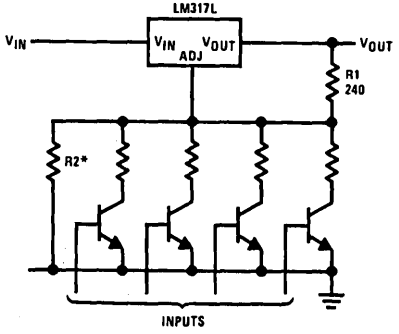
Schematic Diagram



TL/H/9064–10

Typical Applications (Continued)

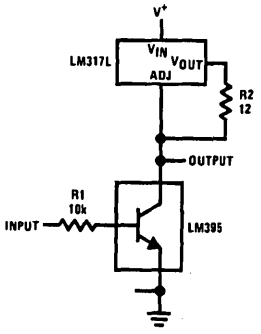
Digitally Selected Outputs



TL/H/9064–11

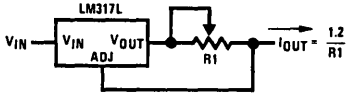
*Sets maximum V_{OUT}

High Gain Amplifier



TL/H/9064–12

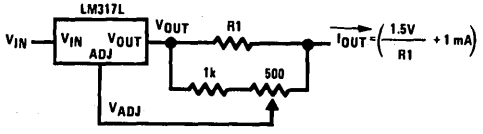
Adjustable Current Limiter



TL/H/9064–13

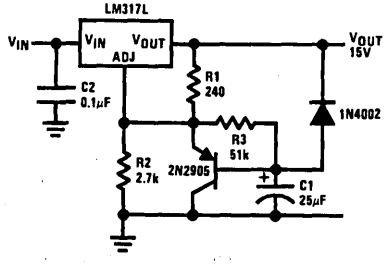
$12 \leq R1 \leq 240$

Precision Current Limiter



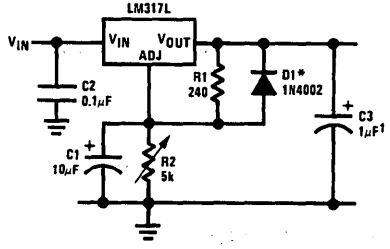
TL/H/9064–14

Slow Turn-On 15V Regulator



TL/H/9064–15

Adjustable Regulator with Improved Ripple Rejection

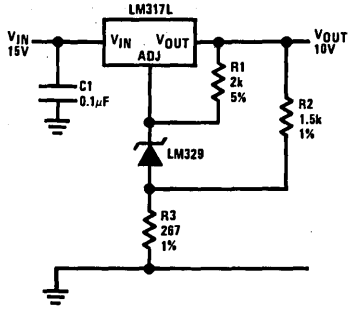


†Solid tantalum

*Discharges C1 if output is shorted to ground

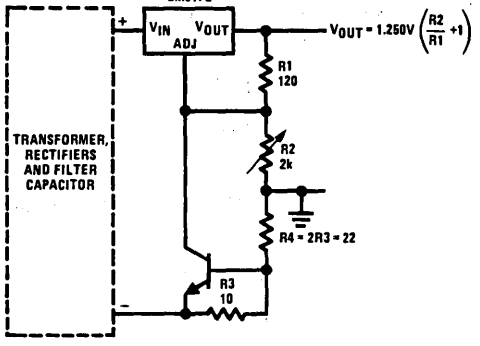
TL/H/9064–16

High Stability 10V Regulator



TL/H/9064–17

Adjustable Regulator with Current Limiter



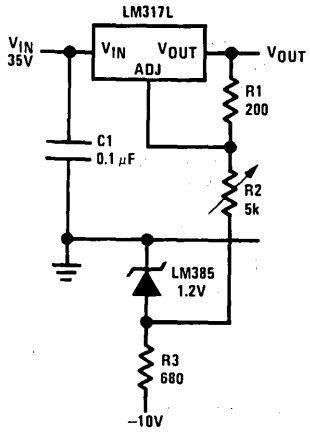
TL/H/9064–18

Short circuit current is approximately 600 mV/R3, or 60 mA (compared to LM317LZ's 200 mA current limit).

At 25 mA output only 3/4V of drop occurs in R3 and R4.

Typical Applications (Continued)

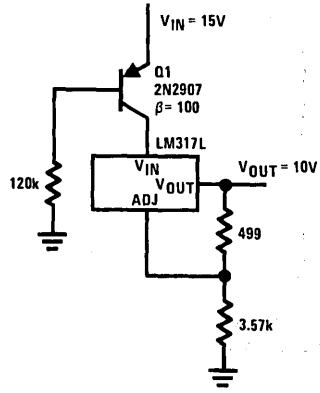
0V–30V Regulator



TL/H/9064–19

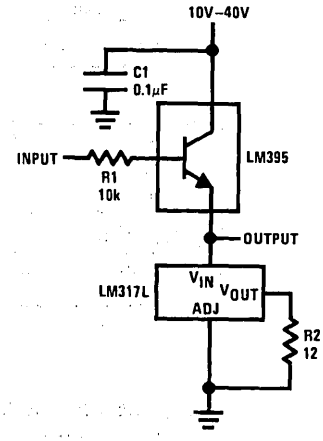
Full output current not available at high input-output voltages

Regulator With 15 mA Short Circuit Current



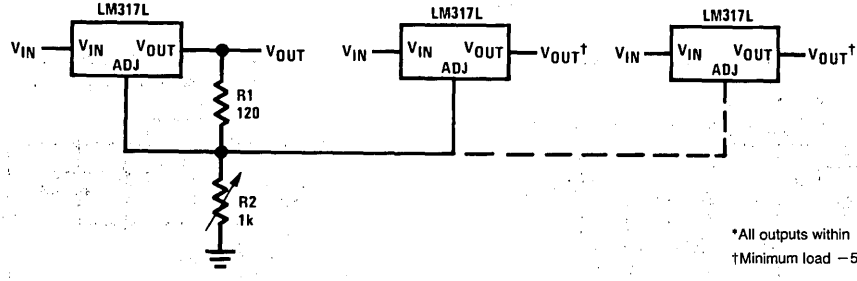
TL/H/9064–20

Power Follower



TL/H/9064–21

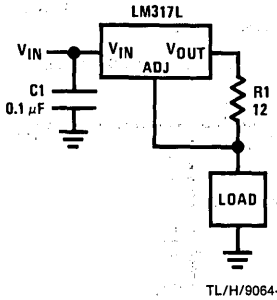
Adjusting Multiple On-Card Regulators with Single Control*



*All outputs within ± 100 mV
†Minimum load −5mA

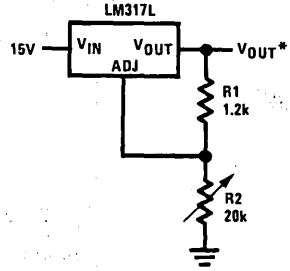
TL/H/9064–22

100 mA Current Regulator



TL/H/9064–23

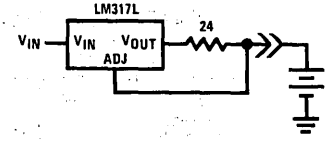
1.2V–12V Regulator with Minimum Program Current



*Minimum load current ≈ 2 mA

TL/H/9064–24

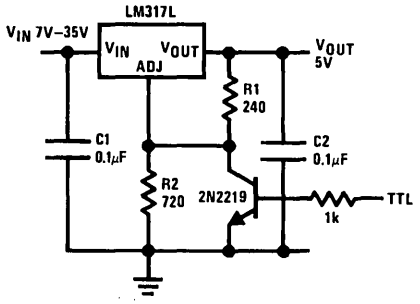
50 mA Constant Current Battery Charger for Nickel-Cadmium Batteries



TL/H/9064–25

Typical Applications (Continued)

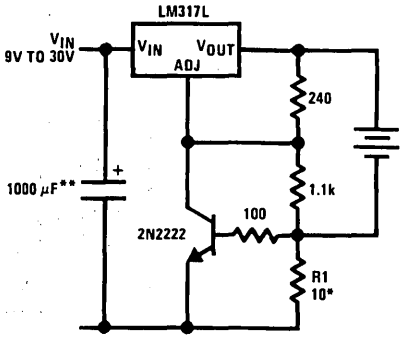
5V Logic Regulator with Electronic Shutdown*



TL/H/9064-26

*Minimum output ≈ 1.2V

Current Limited 6V Charger

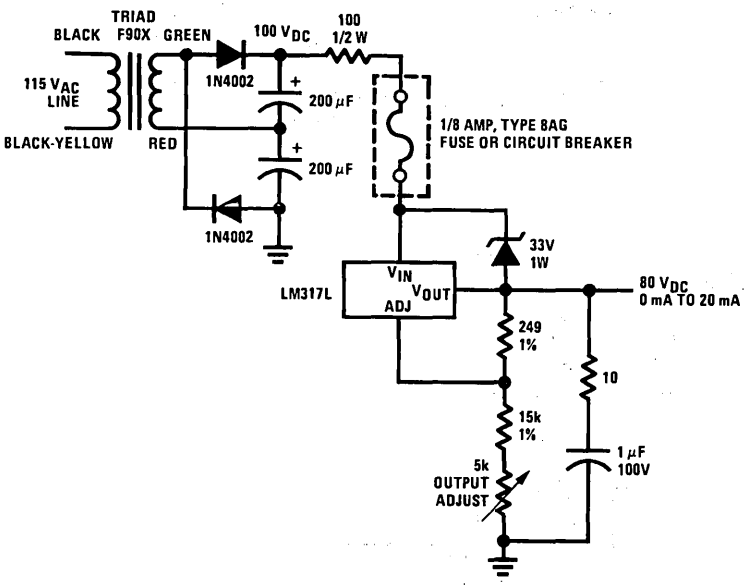


TL/H/9064-27

*Sets peak current, I_{PEAK} = 0.6V/R1

**1000 μF is recommended to filter out any input transients.

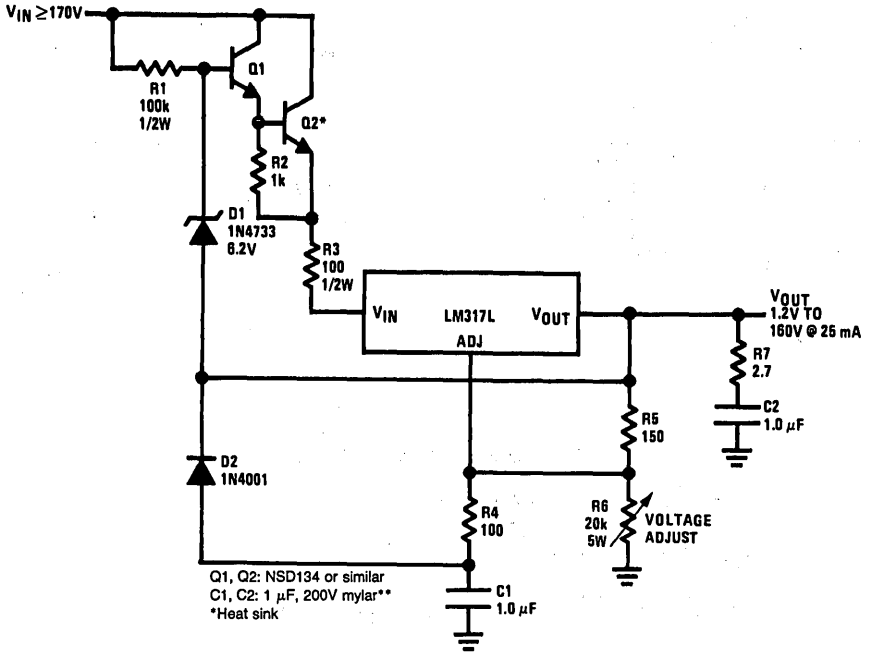
Short Circuit Protected 80V Supply



TL/H/9064-28

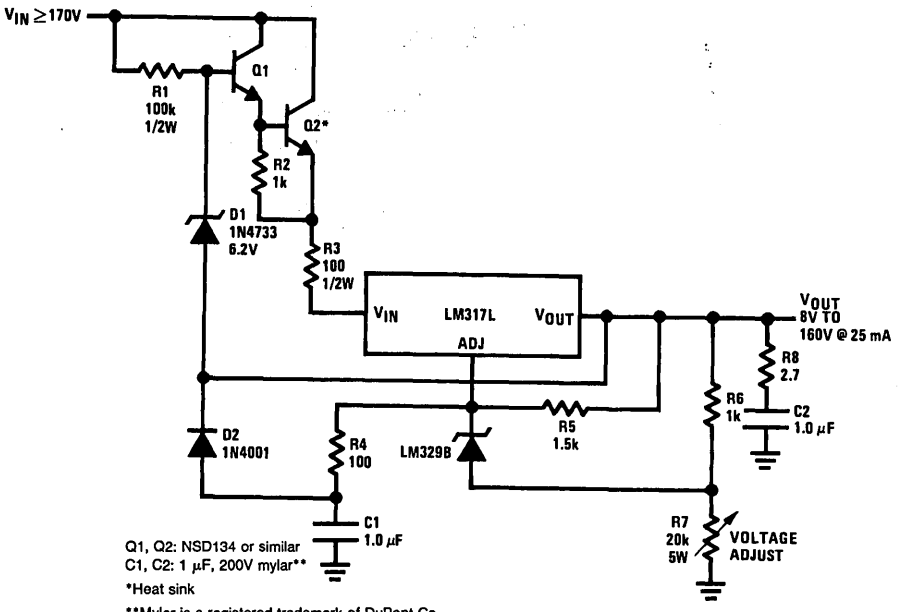
Typical Applications (Continued)

Basic High Voltage Regulator



TL/H/9064–29

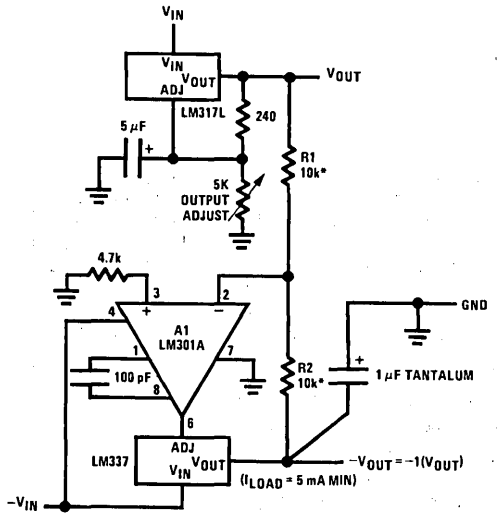
Precision High Voltage Regulator



TL/H/9064–30

Typical Applications (Continued)

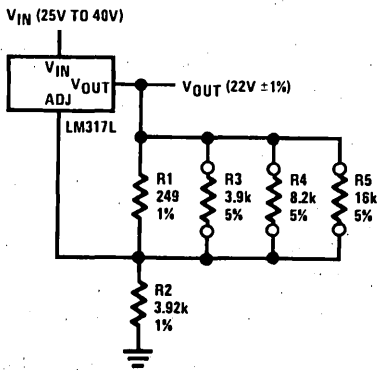
Tracking Regulator



TL/H/9064–31

A1 = LM301A, LM307, or LF13741 only
R1, R2 = matched resistors with good TC tracking

Regulator With Trimmable Output Voltage



TL/H/9064–32

Trim Procedure:

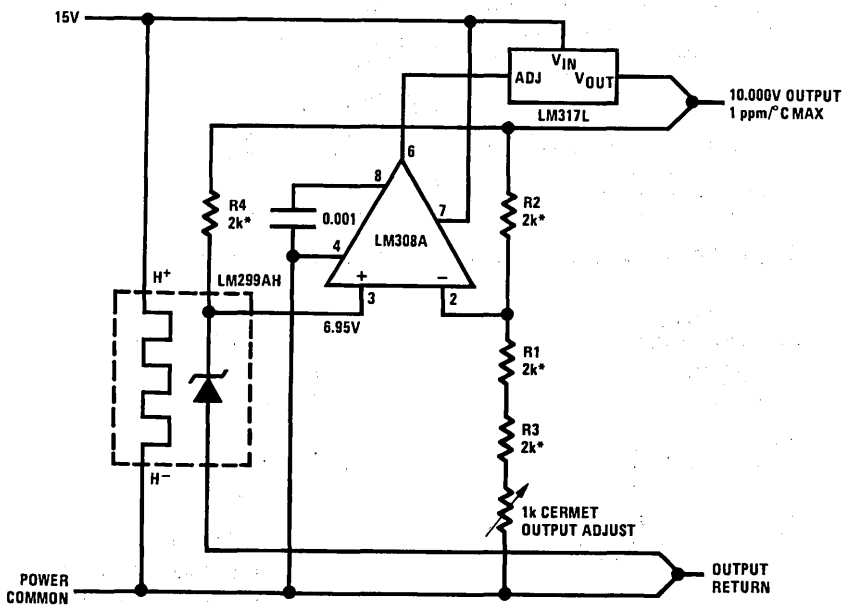
— If V_{OUT} is 23.08V or higher, cut out R3 (if lower, don't cut it out).

— Then if V_{OUT} is 22.47V or higher, cut out R4 (if lower, don't).

— Then if V_{OUT} is 22.16V or higher, cut out R5 (if lower, don't).

This will trim the output to well within ±1% of 22.00 V_{DC}, without any of the expense or uncertainty of a trim pot (see LB-46). Of course, this technique can be used at any output voltage level.

Precision Reference with Short-Circuit Proof Output



TL/H/9064–33

*R1–R4 from thin-film network,
Beckman 694-3-R2K-D or similar

National Semiconductor

LM138A/LM138, LM338A/LM338 5-Amp Adjustable Regulators

General Description

The LM138 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 5A over a 1.2V to 32V output range. They are exceptionally easy to use and require only 2 resistors to set the output voltage. Careful circuit design has resulted in outstanding load and line regulation—comparable to many commercial power supplies. The LM138 family is supplied in a standard 3-lead transistor package.

A unique feature of the LM138 family is time-dependent current limiting. The current limit circuitry allows peak currents of up to 12A to be drawn from the regulator for short periods of time. This allows the LM138 to be used with heavy transient loads and speeds start-up under full-load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe area protection for the power transistor. Overload protection remains functional even if the adjustment pin is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An output capacitor can be added to improve transient response, while bypassing the adjustment pin will increase the regulator's ripple rejection.

Besides replacing fixed regulators or discrete designs, the LM138 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., do not short-circuit output to ground. The part numbers in the LM138 series which have a K suffix are packaged in a standard Steel TO-3 package, while those with a T suffix are packaged in a TO-220 plastic package. The LM138A/LM138 are rated for $-55°C \leq T_J \leq +150°C$, while the LM338A is rated for $-40°C \leq T_J \leq +125°C$, and the LM338 is rated for $0°C \leq T_J \leq +125°C$.

Features

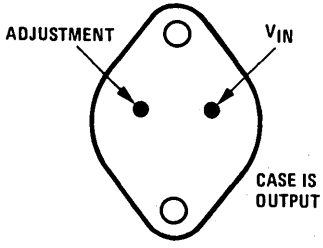
- Guaranteed 7A peak output current
- Guaranteed 5A output current
- Adjustable output down to 1.2V
- Guaranteed thermal regulation
- Current limit constant with temperature
- 100% electrical burn-in in thermal limit
- Output is short-circuit protected
- Guaranteed 1% output voltage tolerance (LM138A, LM338A)
- Guaranteed max. 0.01%/V line regulation (LM138A, LM338A)
- Guaranteed max. 0.3% load regulation (LM138A, LM338A)

Applications

- Adjustable power supplies
- Constant current regulators
- Battery chargers

Connection Diagrams (See Physical Dimension section for further information)

(TO-3 STEEL)
Metal Can Package

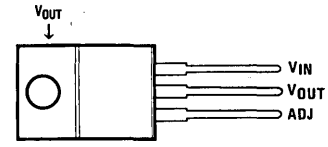


TL/H/9060–30

Bottom View

Order Number LM138AK STEEL/LM138K STEEL/ LM338AK STEEL/LM338K STEEL
See NS Package Number K02A

(TO-220)
Plastic Package



TL/H/9060–31

Front View

Order Number LM338AT/LM338T
See NS Package Number T03B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 4)

Power Dissipation	Internally limited
Input/Output Voltage Differential	+40V, −0.3V
Storage Temperature	−65°C to +150°C
Lead Temperature	
Metal Package (Soldering, 10 seconds)	300°C
Plastic Package (Soldering, 4 seconds)	260°C
ESD Tolerance	TBD

Operating Temperature Range

LM138A/LM138	$-55°C \le T_J \le +150°C$
LM338A	$-40°C \le T_J \le +125°C$
LM338	$0°C \le T_J \le +125°C$

Preconditioning

Thermal Limit Burn-In	All Devices 100%

Electrical Characteristics

Specifications with standard type face are for $T_J = 25°C$, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 10$ mA. (Note 2)

Parameter	Conditions	LM138A			LM138			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	$I_{OUT} = 10$ mA, $T_J = 25°C$	1.238	1.250	1.262				V
	$3V \le (V_{IN} - V_{OUT}) \le 35V$, $10 mA \le I_{OUT} \le 5A$, $P \le 50W$	**1.225**	**1.250**	**1.270**	**1.19**	**1.24**	**1.29**	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 35V$ (Note 3)		0.005	0.01		0.005	0.01	%/V
			0.02	**0.04**		**0.02**	**0.04**	%/V
Load Regulation	$10 mA \le I_{OUT}) \le 5V$ (Note 3)		0.1	0.3		0.1	0.3	%
			0.3	**0.6**		**0.3**	**0.6**	%
Thermal Regulation	20 ms Pulse		0.002	0.01		0.002	0.01	%/W
Adjustment Pin Current			**45**	**100**		**45**	**100**	μA
Adjustment Pin Current Change	$10 mA \le I_{OUT} \le 5A$, $3V \le (V_{IN} - V_{OUT}) \le 35V$		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	$V_{IN} - V_{OUT} = 35V$		**3.5**	**5**		**3.5**	**5**	mA
Current Limit	$V_{IN} - V_{OUT} \le 10V$							
	DC	**5**	**8**		**5**	**8**		A
	0.5 ms Peak	**7**	**12**		**7**	**12**		A
	$V_{IN} - V_{OUT} = 30V$			1			1	A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.001			0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz, $C_{ADJ} = 0$ μF		**60**			**60**		dB
	$V_{OUT} = 10V$, f = 120 Hz, $C_{ADJ} = 10$ μF	**60**	**75**		**60**	**75**		dB
Long-Term Stability	$T_J = 125°C$, 1000 Hrs		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package			1			1	°C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	K Package		35			35		°C/W

Electrical Characteristics (Continued)

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V; and I_{OUT} = 10 mA. (Note 2)

Parameter	Conditions	LM338A			LM338			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	I_{OUT} = 10 mA, T_J = 25°C	1.238	1.250	1.262				V
	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V, 10 mA ≤ I_{OUT} ≤ 5A, P ≤ 50W	**1.225**	**1.250**	**1.270**	**1.19**	**1.24**	**1.29**	V
Line Regulation	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V (Note 3)		0.005	0.01		0.005	0.03	%/V
			0.02	**0.04**		**0.02**	**0.06**	%/V
Load Regulation	10 mA ≤ I_{OUT}) ≤ 5V (Note 3)		0.1	0.3		0.1	0.5	%
			0.3	**0.6**		**0.3**	**1**	%
Thermal Regulation	20 ms Pulse		0.002	0.02		0.002	0.02	%/W
Adjustment Pin Current			**45**	**100**		**45**	**100**	μA
Adjustment Pin Current Change	10 mA ≤ I_{OUT} ≤ 5A, 3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	$V_{IN} - V_{OUT}$ = 35V		**3.5**	**10**		**3.5**	**10**	mA
Current Limit	$V_{IN} - V_{OUT}$ ≤ 10V DC 0.5 ms Peak	**5** **7**	**8** **12**		**5** **7**	**8** **12**		A A
	$V_{IN} - V_{OUT}$ = 30V			1			1	A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.001			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**60**	**60** **75**		**60**	**60** **75**		dB dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.3	1		0.3	1	%
Thermal Resistance Junction to Case	K Package T Package			1 4			1 4	°C/W °C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	K Package T Package		35 50			35 50		°C/W °C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

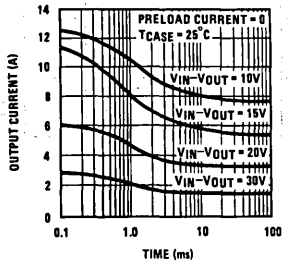
Note 2: These specifications are applicable for power dissipations up to 50W for the TO-3 (K) package and 25W for the TO-220 (T) package. Power dissipation is guaranteed at these values up to 15V input-output differential. Above 15V differential, power dissipation will be limited by internal protection circuitry. All limits (i.e., the numbers in the Min. and Max. columns) are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 3: Regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for thermal regulation.

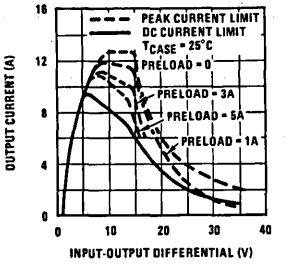
Note 4: Refer to RETS138K drawing for military specifications of LM138K.

Typical Performance Characteristics

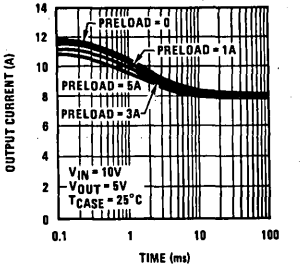
Current Limit



Current Limit



Current Limit



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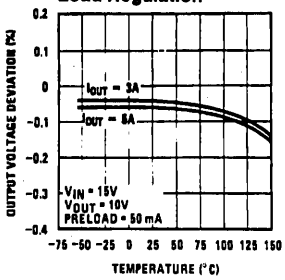
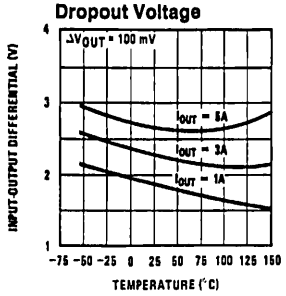
Typical Performance Characteristics (Continued)

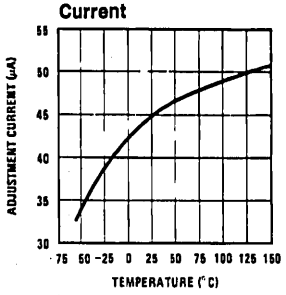
Load Regulation



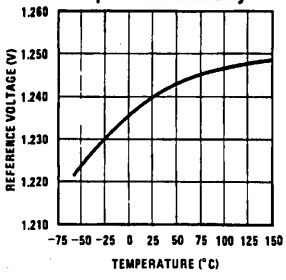
Dropout Voltage



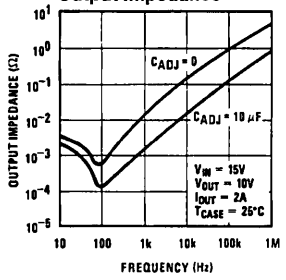
Adjustment Current



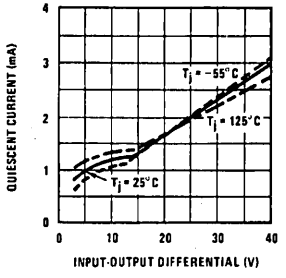
Temperature Stability



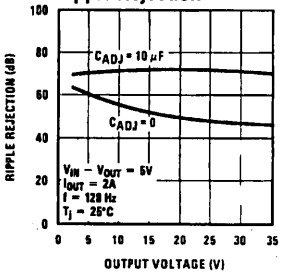
Output Impedance



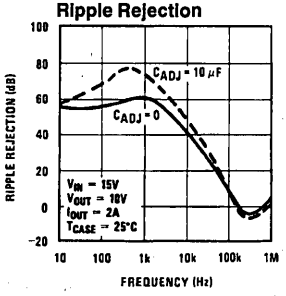
Minimum Operating Current



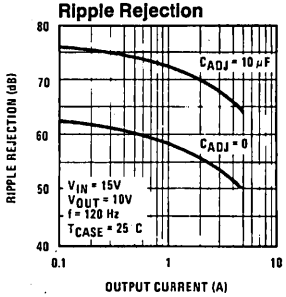
Ripple Rejection



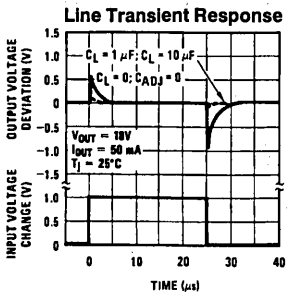
Ripple Rejection



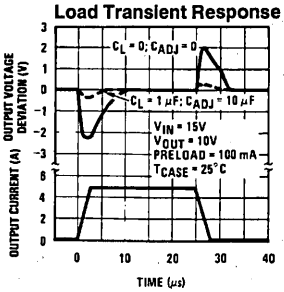
Ripple Rejection



Line Transient Response



Load Transient Response

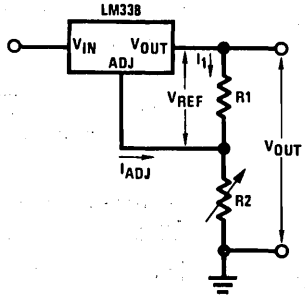


TL/H/9060–5

Application Hints

In operation, the LM138 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2.$$



TL/H/9060–6

FIGURE 1

Since the 50 μA current from the adjustment terminal represents an error term, the LM138 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassiing when adjustment or output capacitors are used but the above values will eliminate the possiblity of problems.

The adjustment terminal can be bypassed to ground on the LM138 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 75 dB ripple rejection is obtainable at any output level. Increases over 20 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

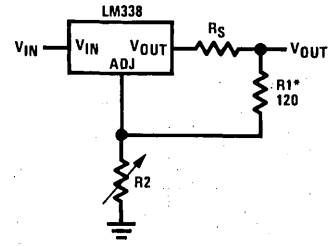
In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM138 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM138 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator (case) rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9060–7

FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using 2 separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

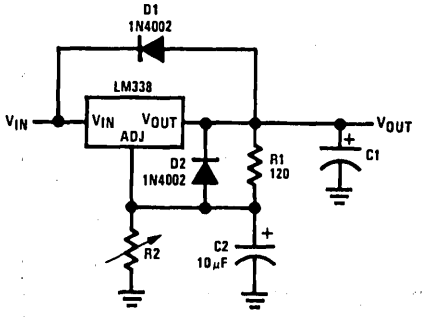
Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 20 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM138 this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 100 μF or less at output of 15V or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM138 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM138 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

Application Hints (Continued)



TL/H/9060–8

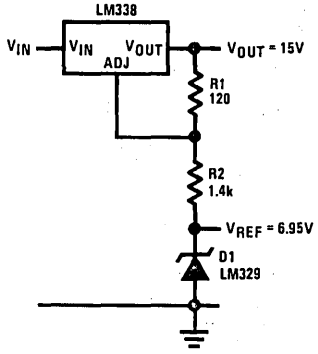
D1 protects against C1
D2 protects against C2

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

FIGURE 3. Regulator with Protection Diodes

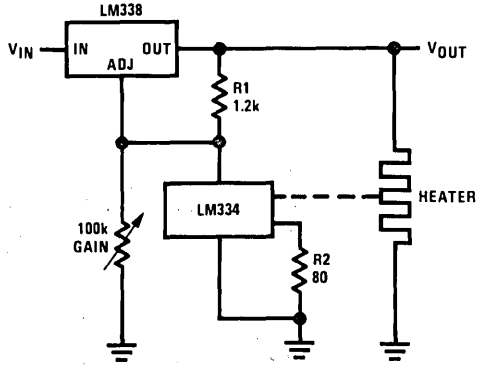
Typical Applications

Regulator and Voltage Reference



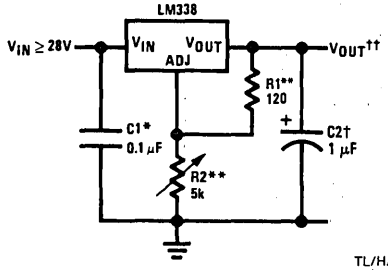
TL/H/9060–3

Temperature Controller



TL/H/9060–10

1.2V–25V Adjustable Regulator



TL/H/9060–1

Full output current not available
at high input-output voltages

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 inches from filter capacitors.

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,(R_2)$$

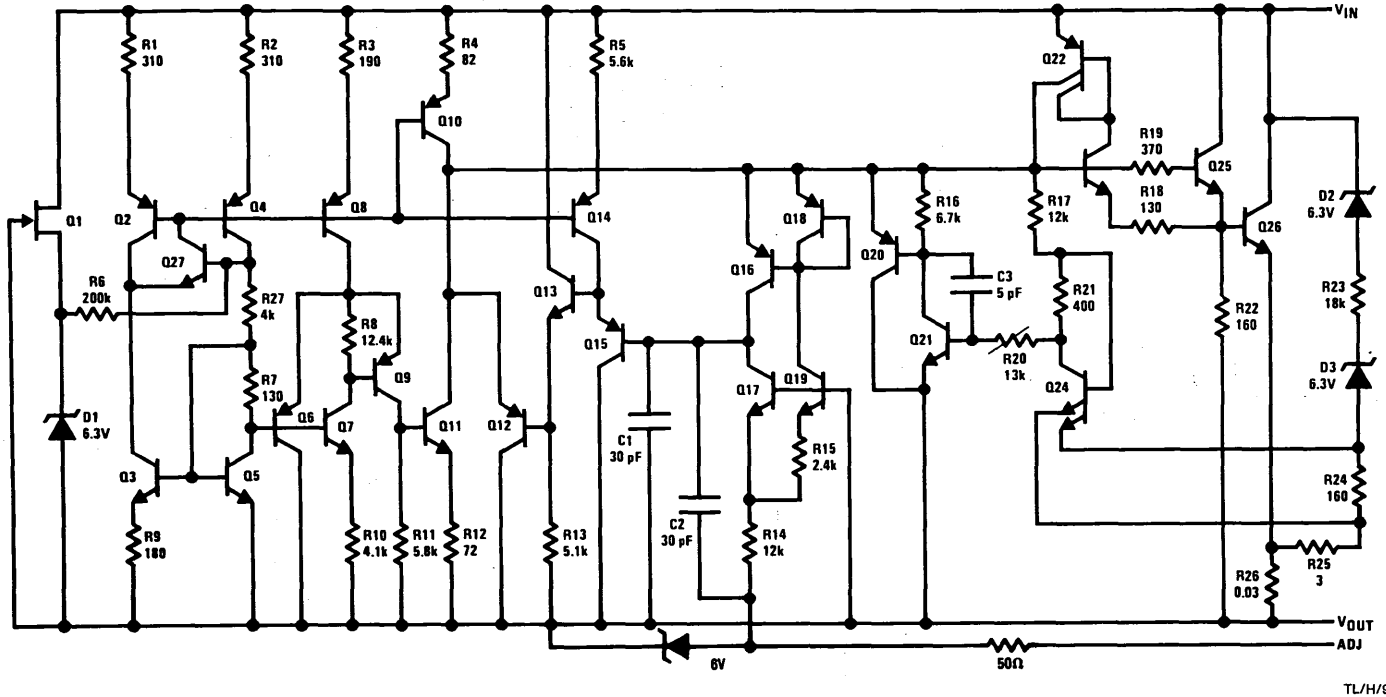
**R1 = 240Ω for LM138. R1, R2 as an assembly can be ordered from Bourns:

MIL part no. 7105A-AT2-502

COMM part no. 7105A-AT7-502

4

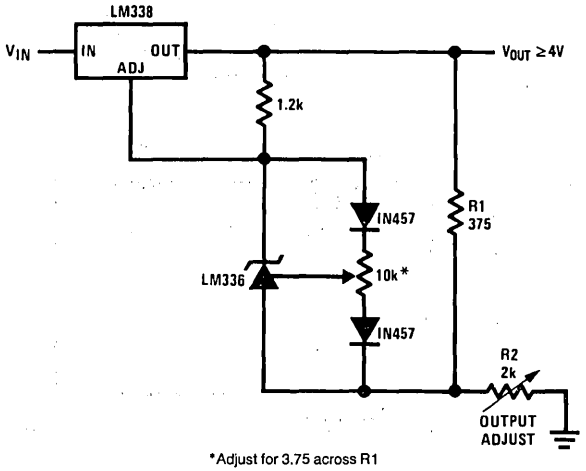
Schematic Diagram



TL/H/9060–9

Typical Applications (Continued)

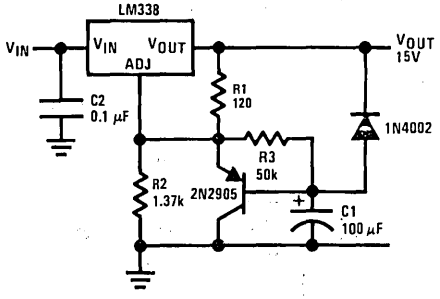
Precision Power Regulator with Low Temperature Coefficient



*Adjust for 3.75 across R1

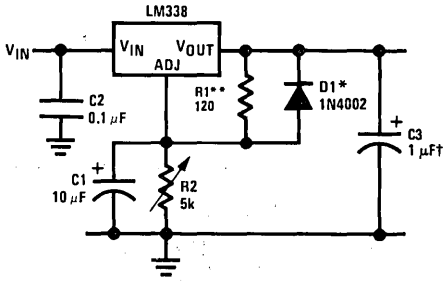
TL/H/9060–12

Slow Turn-On 15V Regulator



TL/H/9060–13

Adjustable Regulator with Improved Ripple Rejection



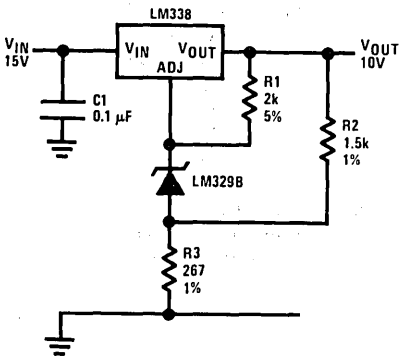
TL/H/9060–14

†Solid tantalum

*Discharges C1 if output is shorted to ground

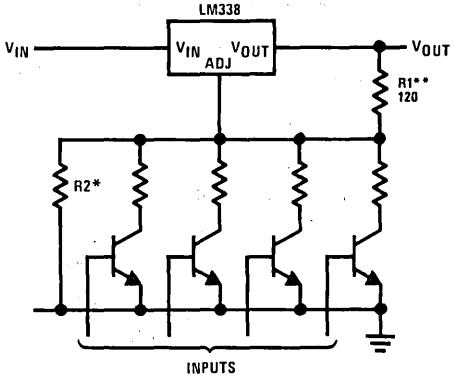
**R1 = 240Ω for LM138

High Stability 10V Regulator



TL/H/9060–15

Digitally Selected Outputs



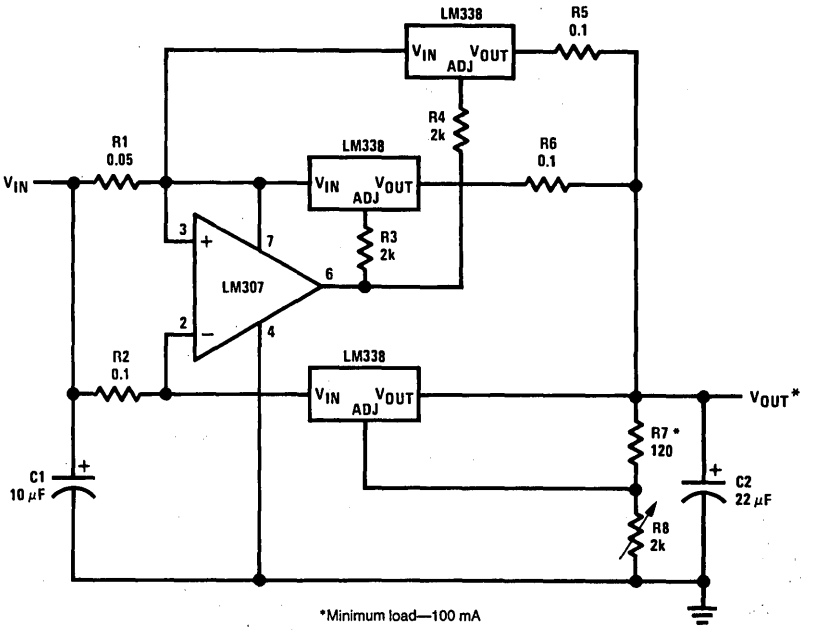
TL/H/9060–16

*Sets maximum V_{OUT}

**R1 = 240Ω for LM138

Typical Applications (Continued)

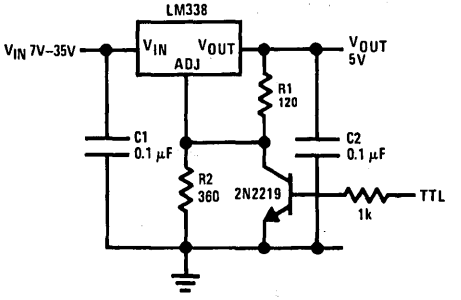
15A Regulator



*Minimum load—100 mA

TL/H/9060–17

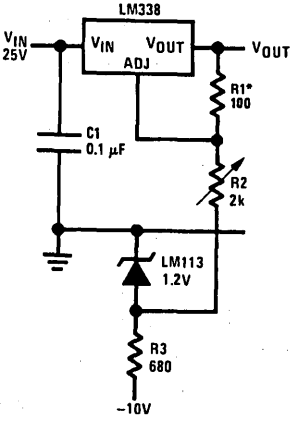
5V Logic Regulator with Electronic Shutdown**



**Minimum output ≈ 1.2V

TL/H/9060–18

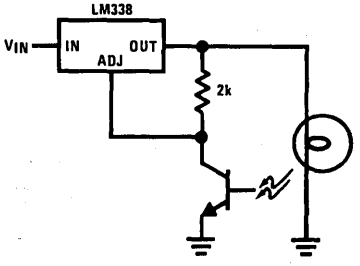
0 to 22V Regulator



TL/H/9060–19

*R1 = 240Ω, R2 = 5k for LM138
Full output current not available
at high input-output voltages

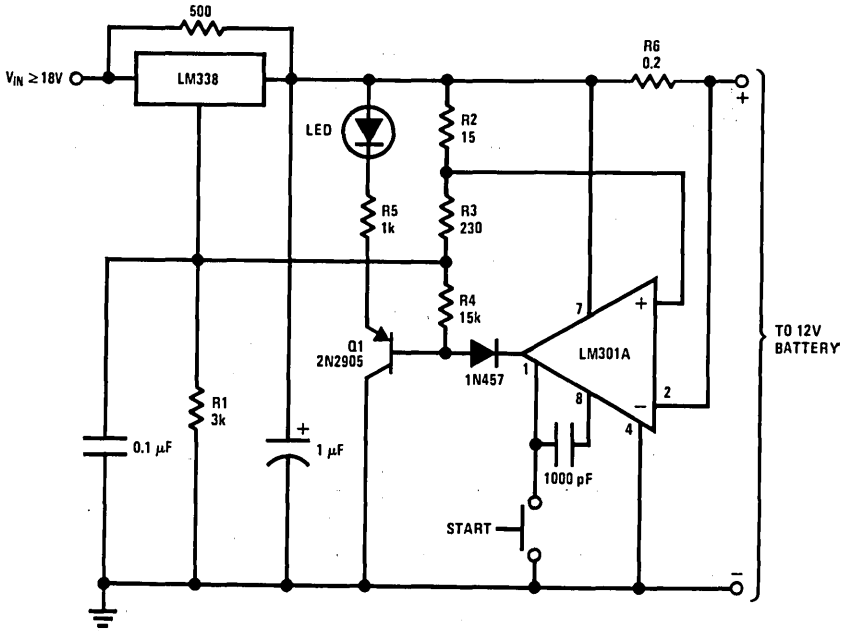
Light Controller



TL/H/9060–11

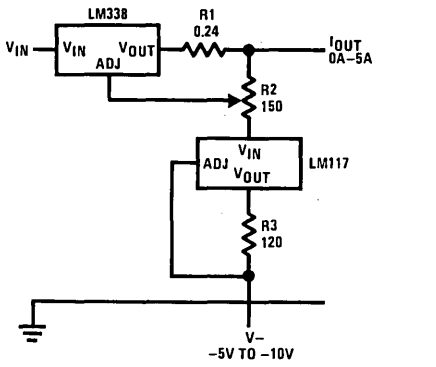
Typical Applications (Continued)

12V Battery Charger



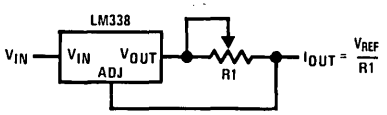
TL/H/9060–20

Adjustable Current Regulator



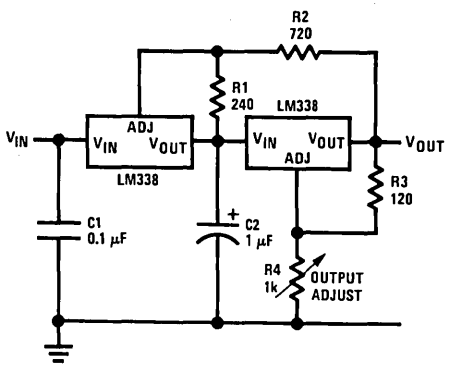
TL/H/9060–21

Precision Current Limiter



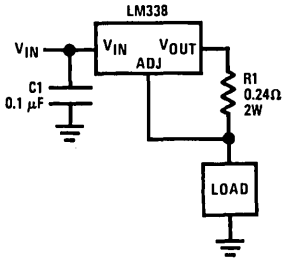
TL/H/9060–22

Tracking Preregulator



TL/H/9060–24

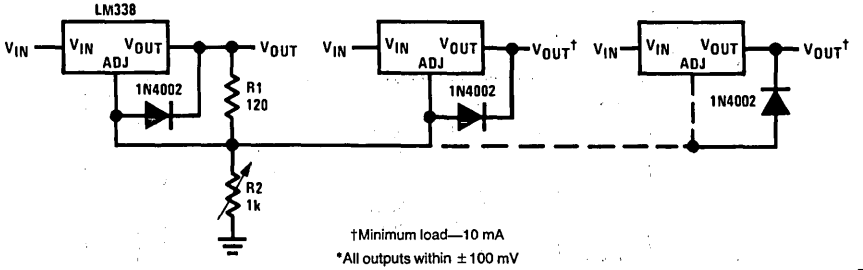
5A Current Regulator



TL/H/9060–23

Typical Applications (Continued)

Adjusting Multiple On-Card Regulators with Single Control*

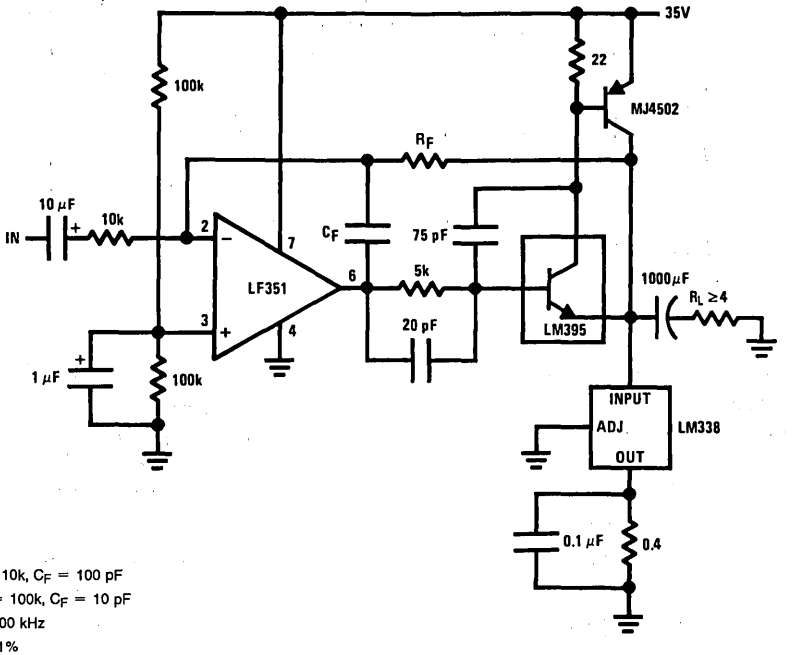


†Minimum load—10 mA

*All outputs within ±100 mV

TL/H/9060–25

Power Amplifier



A_V = 1, R_F = 10k, C_F = 100 pF

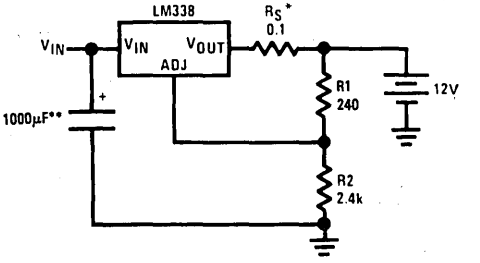
A_V = 10, R_F = 100k, C_F = 10 pF

Bandwidth ≥ 100 kHz

Distortion ≤ 0.1%

TL/H/9060–27

Simple 12V Battery Charger



TL/H/9060–28

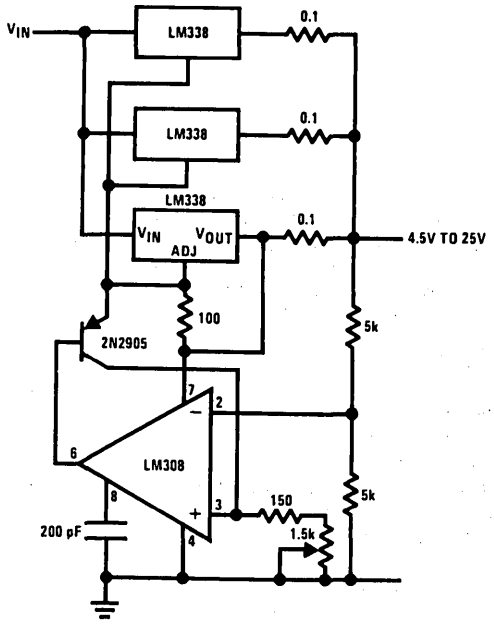
*R_S—sets output impedance of charger $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

Use of R_S allows low charging rates with fully charged battery.

**The 1000 μF is recommended to filter out input transients

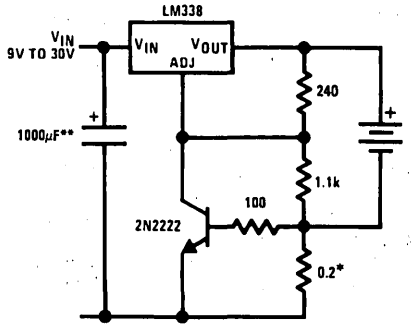
Typical Applications (Continued)

Adjustable 15A Regulator



TL/H/9060-26

Current Limited 6V Charger

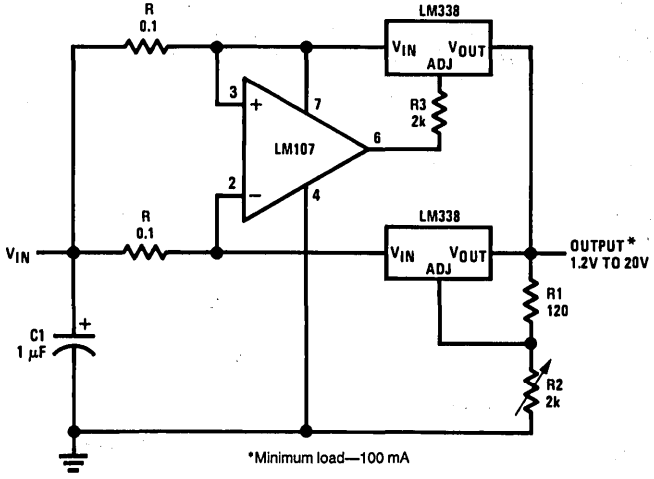


TL/H/9060-29

*Set max charge current to 3A

**The 1000 μF is recommended to filter out input transients.

10A Regulator



*Minimum load—100 mA

TL/H/9060-2

National Semiconductor

LM150A/LM150, LM350A/LM350 3-Amp Adjustable Regulators

General Description

The LM150 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 3A over a 1.2V to 33V output range. They are exceptionally easy to use and require only 2 external resistors to set the output voltage. Further, both line and load regulation are comparable to discrete designs. Also, the LM150 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM150 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An output capacitor can be added to improve transient response, while bypassing the adjustment pin will increase the regulator's ripple rejection.

Besides replacing fixed regulators or discrete designs, the LM150 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

By connecting a fixed resistor between the adjustment pin and output, the LM150 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The part numbers in the LM150 series which have a K suffix are packaged in a standard Steel TO-3 package, while those with a T suffix are packaged in a TO-220 plastic package. The LM150A/LM150 are rated for $-55°C \leq T_J \leq +150°C$, while the LM350A is rated for $-40°C \leq T_J \leq +125°C$, and the LM350 is rated for $0°C \leq T_J \leq +125°C$.

Features

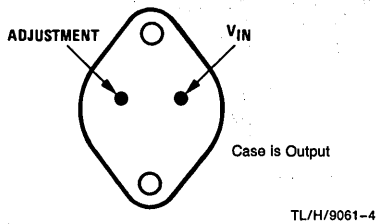
- Adjustable output down to 1.2V
- Guaranteed 3A output current
- Guaranteed thermal regulation
- Output is short circuit protected
- Current limit constant with temperature
- 100% electrical burn-in in thermal limit
- 86 dB ripple rejection
- Guaranteed 1% output voltage tolerance (LM150A, LM350A)
- Guaranteed max. 0.01%/V line regulation (LM150A, LM350A)
- Guaranteed max. 0.3% load regulation (LM150A, LM350A)

Applications

- Adjustable power supplies
- Constant current regulators
- Battery chargers

Connection Diagrams

(TO-3 STEEL)
Metal Can Package

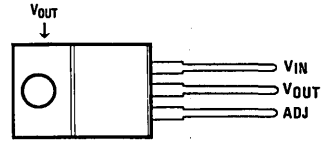


TL/H/9061–4

Bottom View

Order Number LM150AK STEEL, LM150K STEEL, LM350AK STEEL or LM350K STEEL
See NS Package Number K02A

(TO-220)
Plastic Package



TL/H/9061–5

Front View

Order Number LM350AT or LM350T
See NS Package Number T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Power Dissipation	Internally Limited
Input-Output Voltage Differential	+35V
Storage Temperature	−65°C to +150°C
Lead Temperature	
Metal Package (Soldering, 10 sec.)	300°C
Plastic Package (Soldering, 4 sec.)	260°C
ESD Tolerance	TBD
Operating Temperature Range	
LM150A/LM150	$-55°C \le T_J \le +150°C$
LM350A	$-40°C \le T_J \le +125°C$
LM350	$0°C \le T_J \le +125°C$

Preconditioning

Thermal Limit Burn-In	All Devices 100%

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V, and I_{OUT} = 10 mA. (Note 2)

Parameter	Conditions	LM150A			LM150			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	I_{OUT} = 10 mA, T_J = 25°C	1.238	1.250	1.262				V
	$3V \le (V_{IN} - V_{OUT}) \le 35V$, $10\ mA \le I_{OUT} \le 3A$, $P \le 30W$	**1.225**	**1.250**	**1.270**	**1.20**	**1.25**	**1.30**	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 35V$ (Note 3)		0.005	0.01		0.005	0.01	%/V
			0.02	**0.05**		**0.02**	**0.05**	%/V
Load Regulation	$10\ mA \le I_{OUT} \le 3A$ (Note 3)		0.1	0.3		0.1	0.3	%
			0.3	**1**		**0.3**	**1**	%
Thermal Regulation	20 ms Pulse		0.002	0.01		0.002	0.01	%/W
Adjustment Pin Current			**50**	**100**		**50**	**100**	μA
Adjustment Pin Current Change	$10\ mA \le I_{OUT} \le 3A$, $3V \le (V_{IN} - V_{OUT}) \le 35V$		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	$V_{IN} - V_{OUT}$ = 35V		**3.5**	**5**		**3.5**	**5**	mA
Current Limit	$V_{IN} - V_{OUT} \le 10V$	**3.0**	**4.5**		**3.0**	**4.5**		A
	$V_{IN} - V_{OUT}$ = 30V	0.3	1		0.3	1		A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.001			0.001		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF		**65**			**65**		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**66**	**86**		**66**	**86**		dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package		1.2	1.5		1.2	1.5	°C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	K Package		35			35		°C/W

Electrical Characteristics (Continued)

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V, and I_{OUT} = 10 mA. (Note 2) (Continued)

Parameter	Conditions	LM350A			LM350			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	I_{OUT} = 10 mA, T_J = 25°C	1.238	1.250	1.262				V
	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V, 10 mA ≤ I_{OUT} ≤ 3A, P ≤ 30W	**1.225**	**1.250**	**1.270**	**1.20**	**1.25**	**1.30**	V
Line Regulation	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V (Note 3)		0.005	0.01		0.005	0.03	%/V
			0.02	**0.05**		**0.02**	**0.07**	%/V
Load Regulation	10 mA ≤ I_{OUT} ≤ 3A (Note 3)		0.1	0.3		0.1	0.5	%
			0.3	**1**		**0.3**	**1.5**	%
Thermal Regulation	20 ms Pulse		0.002	0.01		0.002	0.03	%/W
Adjustment Pin Current			**50**	**100**		**50**	**100**	μA
Adjustment Pin Current Change	10 mA ≤ I_{OUT} ≤ 3A, 3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	$V_{IN} - V_{OUT}$ = 35V		**3.5**	**10**		**3.5**	**10**	mA
Current Limit	$V_{IN} - V_{OUT}$ ≤ 10V	**3.0**	**4.5**		**3.0**	**4.5**		A
	$V_{IN} - V_{OUT}$ = 30V	0.3	1		0.25	1		A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.001			0.001		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF		**65**			**65**		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**66**	**86**		**66**	**86**		dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.25	1		0.25	1	%
Thermal Resistance, Junction to Case	K Package		1.2	1.5		1.2	1.5	°C/W
	T Package		3	4		3	4	°C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	K Package		35			35		°C/W
	T Package		50			50		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

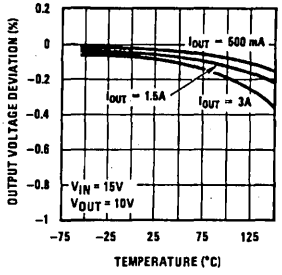
Note 2: These specifications are applicable for power dissipations up to 30W for the TO-3 (K) package and 25W for the TO-220 (T) package. Power dissipation is guaranteed at these values up to 15V input-output differential. Above 15V differential, power dissipation will be limited by internal protection circuitry. All limits (i.e., the numbers in the Min. and Max. columns) are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 3: Regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for thermal regulation.

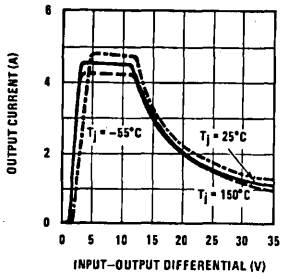
Note 4: Refer to RETS150K drawing for military specifications of the LM150K.

Typical Performance Characteristics

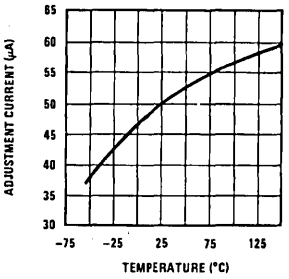
Load Regulation



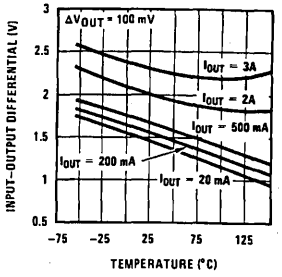
Current Limit



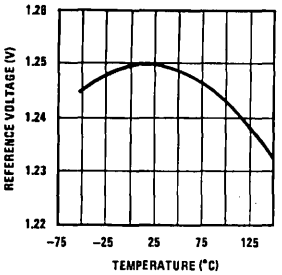
Adjustment Current



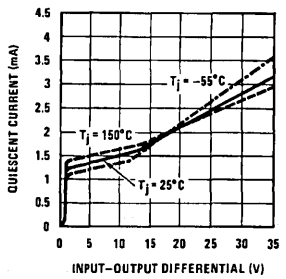
Dropout Voltage



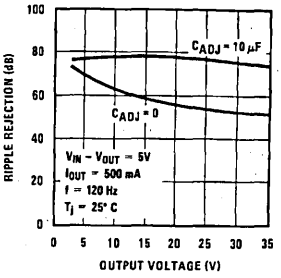
Temperature Stability



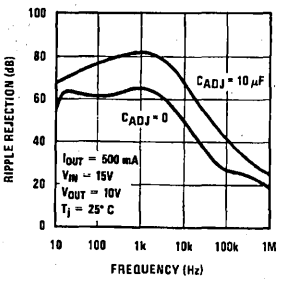
Minimum Operating Current



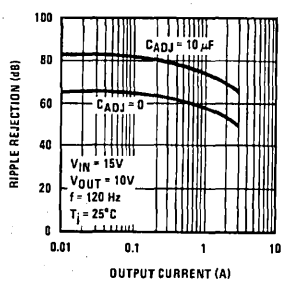
Ripple Rejection



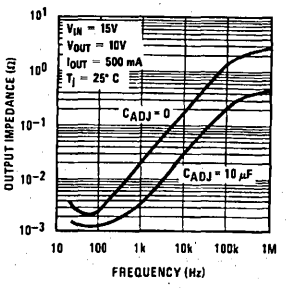
Ripple Rejection



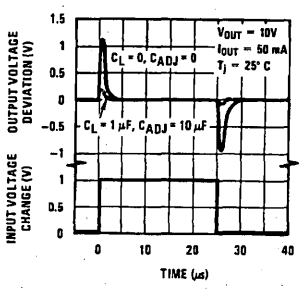
Ripple Rejection



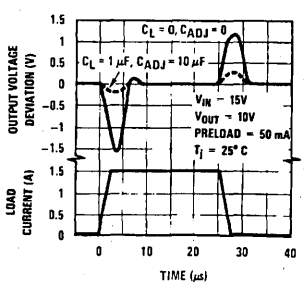
Output Impedance



Line Transient Response



Load Transient Response

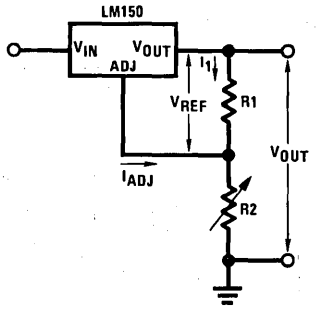


TL/H/9061–6

Application Hints

In operation, the LM150 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2.$$



TL/H/9061–7

FIGURE 1

Since the 50 μA current from the adjustment terminal represents an error term, the LM150 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

EXTERNAL CAPACITORS

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM150 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 86 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

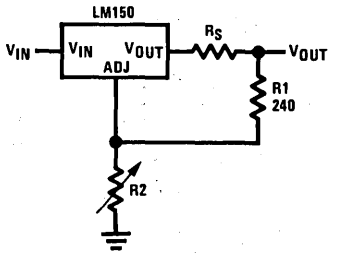
In general, the best type of capacitors to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM150 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

LOAD REGULATION

The LM150 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × I_{OUT}. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9061–8

FIGURE 2. Regulator with Line Resistance In Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

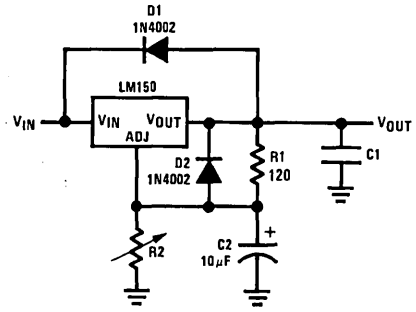
PROTECTION DIODES

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM150, this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM150 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM150 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

Application Hints (Continued)



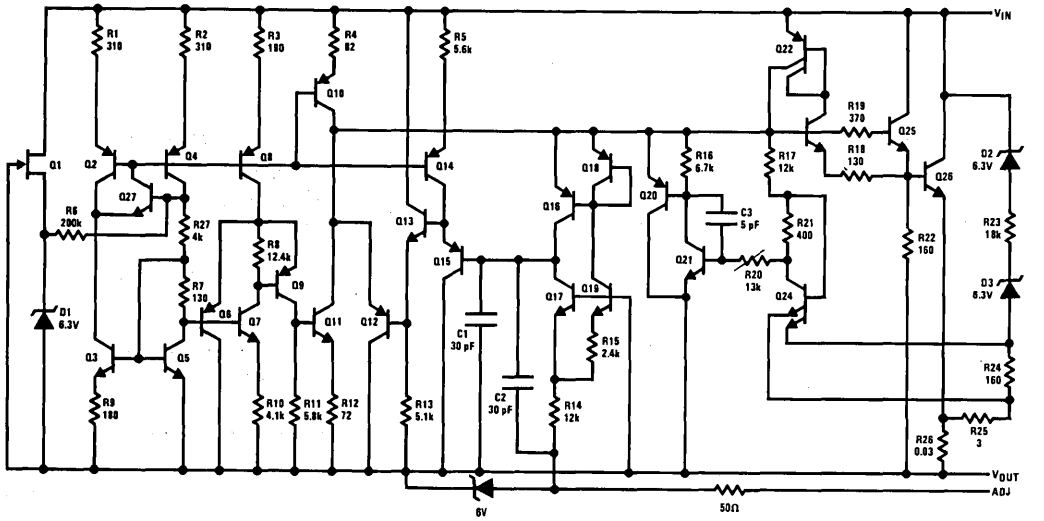
D1 protects against C1
D2 protects against C2

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

TL/H/9061–9

FIGURE 3. Regulator with Protection Diodes

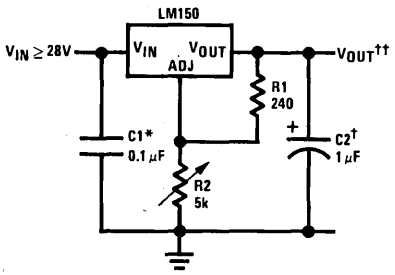
Schematic Diagram



TL/H/9061–10

Typical Applications

1.2V—25V Adjustable Regulator



TL/H/9061–1

Full output current not available at high input-output voltages.

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 inches from filter capacitors.

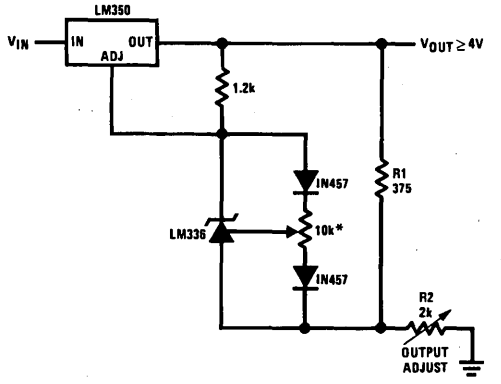
$$††V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R2)$$

Note: Usually R1 = 240Ω for LM150 and R1 = 120Ω for LM350.

4

Typical Applications (Continued)

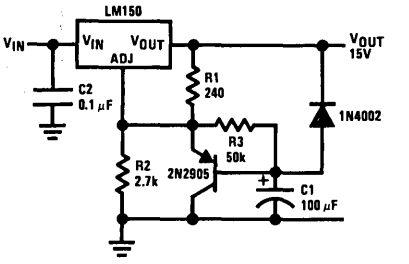
Precision Power Regulator with Low Temperature Coefficient



*Adjust for 3.75V across R1

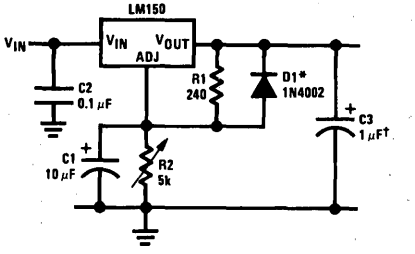
TL/H/9061–13

Slow Turn-ON 15V Regulator



TL/H/9061–14

Adjustable Regulator with Improved Ripple Rejection

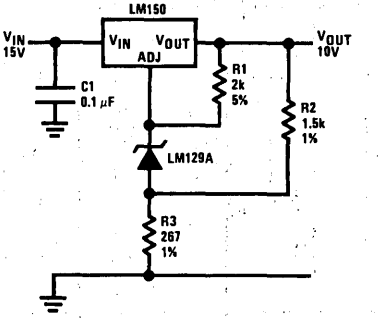


†Solid tantalum

*Discharges C1 if output is shorted to ground

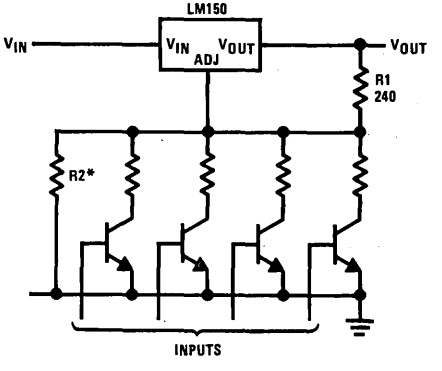
TL/H/9061–15

High Stability 10V Regulator



TL/H/9061–16

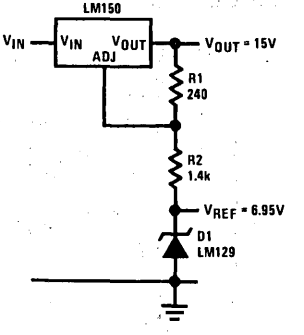
Digitally Selected Outputs



TL/H/9061–17

*Sets maximum V_{OUT}

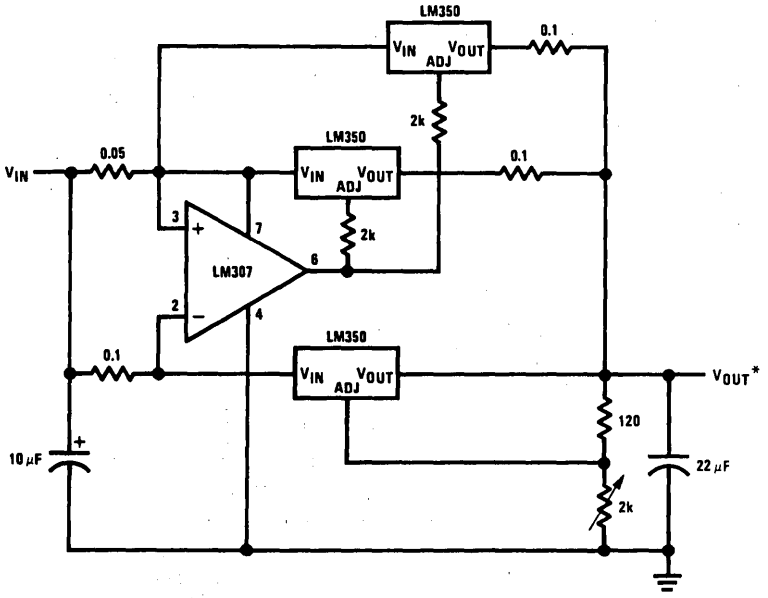
Regulator and Voltage Reference



TL/H/9061–3

Typical Applications (Continued)

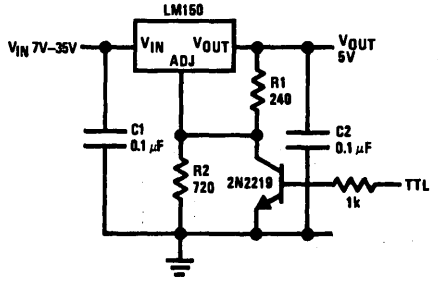
10A Regulator



*Minimum load current 50 mA

TL/H/9061–18

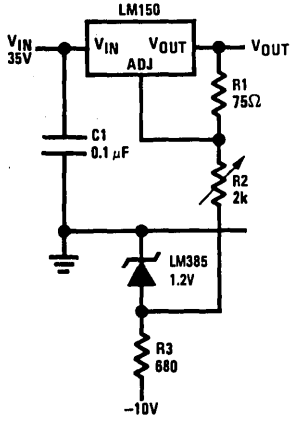
5V Logic Regulator with Electronic Shutdown*



TL/H/9061–19

*Min output ≈ 1.2V

0 to 30V Regulator

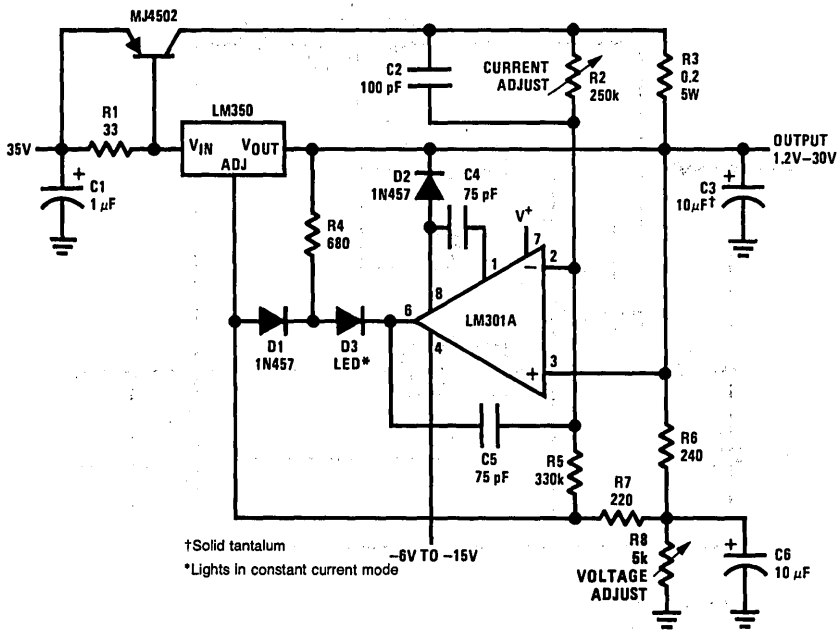


TL/H/9061–20

Full output current not available at high input-output voltages

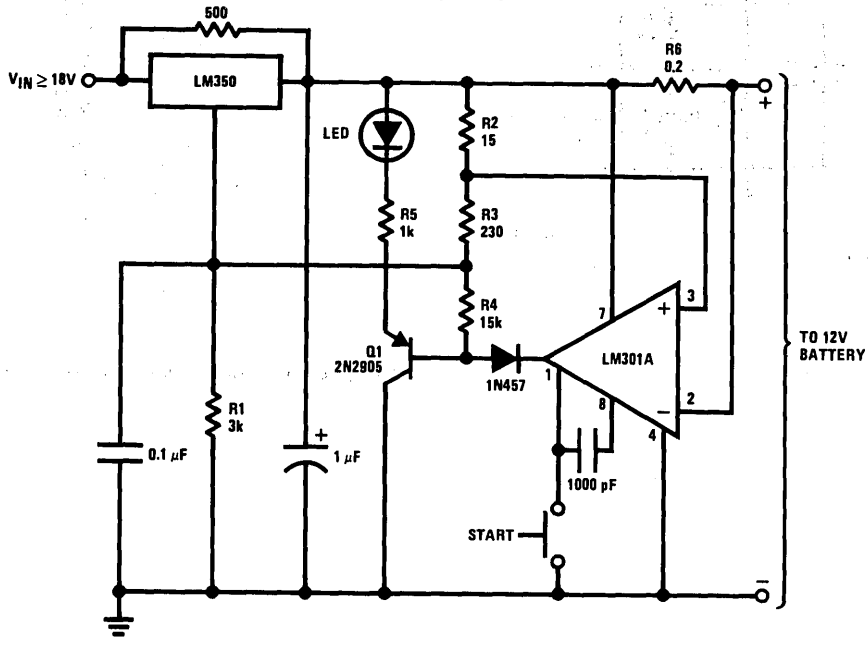
Typical Applications (Continued)

5A Constant Voltage/Constant Current Regulator



TL/H/9061–21

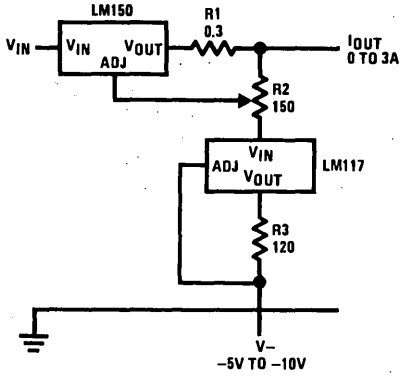
12V Battery Charger



TL/H/9061–22

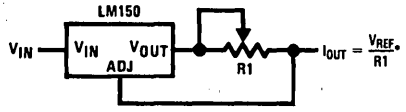
Typical Applications (Continued)

Adjustable Current Regulator



TL/H/9061–23

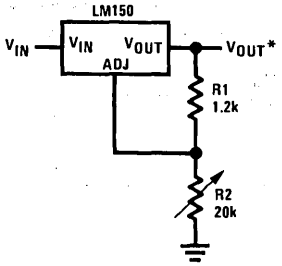
Precision Current Limiter



TL/H/9061–24

*0.4 ≤ R_1 ≤ 120Ω

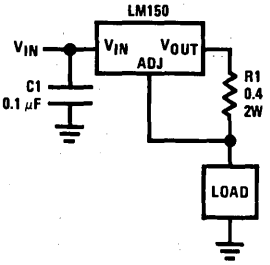
1.2V–20V Regulator with Minimum Program Current



TL/H/9061–25

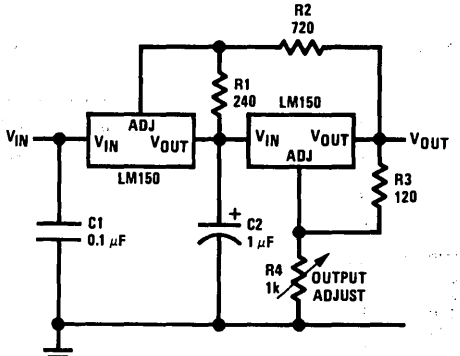
*Minimum output current ≈ 4 mA

3A Current Regulator



TL/H/9061–26

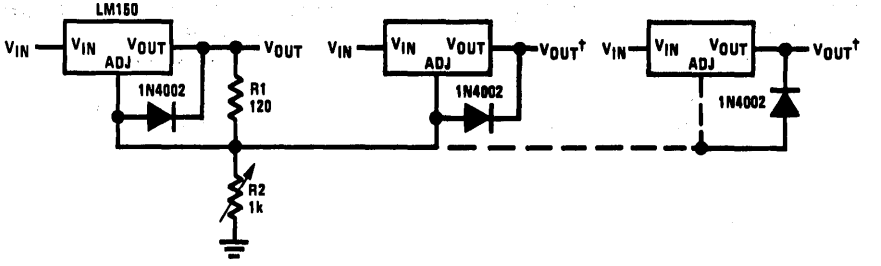
Tracking Preregulator



TL/H/9061–27

Typical Applications (Continued)

Adjusting Multiple On-Card Regulators with Single Control*

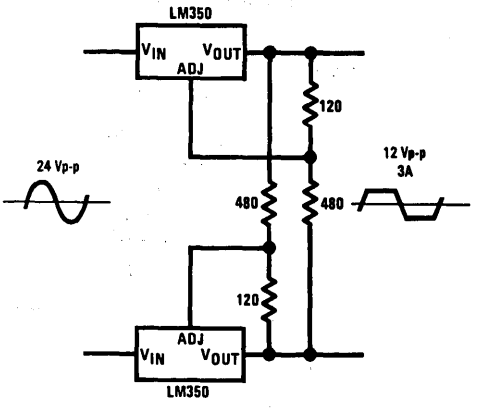


TL/H/9061-28

†Minimum load—10 mA

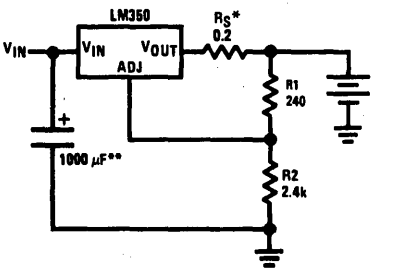
*All outputs within ±100 mV

AC Voltage Regulator



TL/H/9061-29

Simple 12V Battery Charger



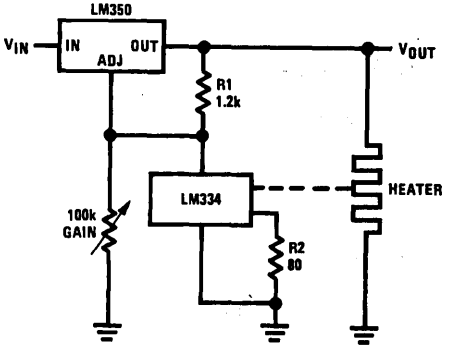
TL/H/9061-30

*R_S—sets output impedance of charger: $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

Use of R_S allows low charging rates with fully charged battery.

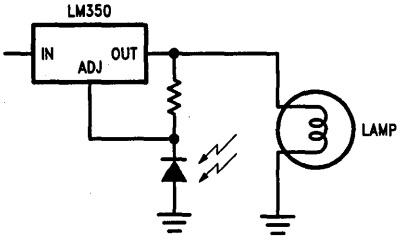
**1000 µF is recommended to filter out any input transients

Temperature Controller



TL/H/9061-11

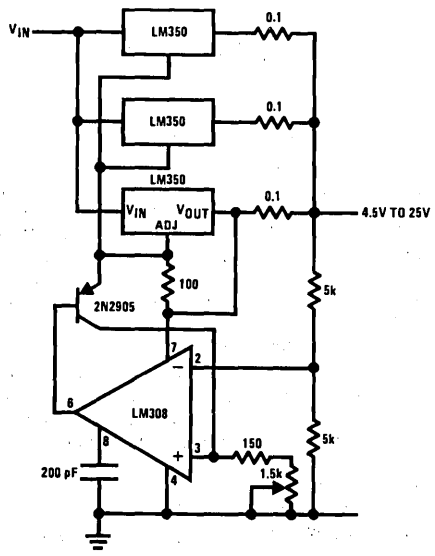
Light Controller



TL/H/9061-12

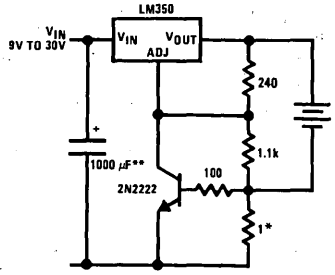
Typical Applications (Continued)

Adjustable 10A Regulator



TL/H/9061–31

Current Limited 6V Charger

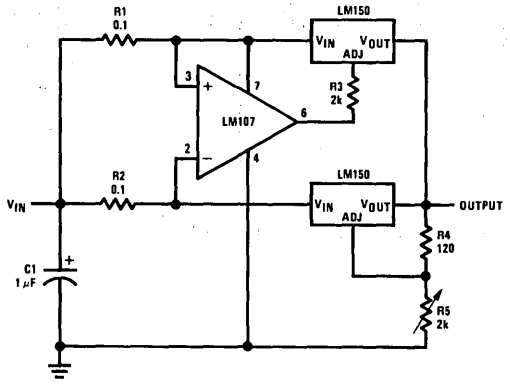


TL/H/9061–32

*Sets peak current (2A for 0.3Ω)

**1000 μF is recommended to filter out any input transients.

6A Regulator



TL/H/9061–2

National Semiconductor

LM196/LM396 10 Amp Adjustable Voltage Regulator

General Description

The LM196 is a 10 amp regulator, adjustable from 1.25V to 15V, which uses a revolutionary new IC fabrication structure to combine high power discrete transistor technology with modern monolithic linear IC processing. This combination yields a high-performance single-chip regulator capable of supplying in excess of 10 amps and operating at power levels up to 70 watts. The regulators feature on-chip trimming of reference voltage to ±0.8% and simultaneous trimming of reference temperature drift to 30 ppm/°C typical. Thermal interaction between control circuitry and the pass transistor which affects the output voltage has been reduced to extremely low levels by strict attention to isothermal layout. This interaction, called thermal regulation, is 100% tested.

These new regulators have all the protection features of popular lower power adjustable regulators such as LM117 and LM138, including current limiting and thermal limiting. The combination of these features makes the LM196 immune to blowout from output overloads or shorts, even if the adjustment pin is accidentally disconnected. All devices are "burned-in" in thermal shutdown to guarantee proper operation of these protective features under actual overload conditions.

Output voltage is continuously adjustable from 1.25V to 15V. Higher output voltages are possible if the maximum input-output voltage differential specification is not exceeded. Full load current of 10A is available at all output voltages, subject only to the maximum power limit of 70W and of course, maximum junction temperature.

The LM196 is exceptionally easy to use. Only two external resistors are used to to set output voltage. On-chip adjustment of the reference voltage allows a much tighter specification of output voltage, eliminating any need for trimming in most cases. The regulator will tolerate an extremely wide range of reactive loads, and does not depend on external capacitors for frequency stabilization. Heat sink requirements are much less stringent, because overload situations do not have to be accounted for—only worst-case full load conditions.

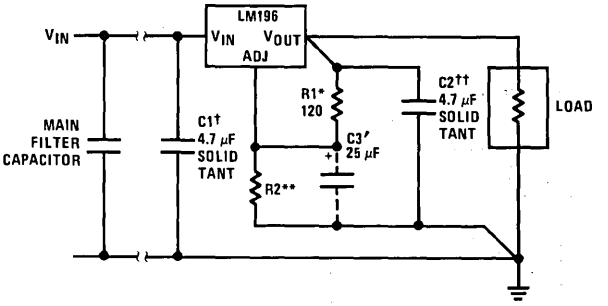
The LM196 is in a TO-3 package with oversized (0.060") leads to provide best possible load regulation. Operating junction temperature range is −55°C to +150°C. The LM396 is specified for a 0°C to +125°C junction temperature range.

Features

- Output pre-trimmed to ±0.8%
- 10A guaranteed output current
- 100% burn-in in thermal limit
- 70W maximum power dissipation
- Adjustable output—1.25V to 15V
- Internal current and power limiting
- Guaranteed thermal resistance
- Output voltage guaranteed under worst-case conditions
- Output is short circuit protected

Typical Applications

$$V_{OUT} = (1.25V)\left(\frac{R1 + R2}{R1}\right) + I_{ADJ}(R2)$$



TL/H/9059-1

FIGURE 1. Basic 1.25V to 15V Regulator

*For best TC of V_{OUT}, R1 should be wirewound or metal film, 1% or better.

**R2 should be same type as R1, with TC tracking of 30 ppm/°C or better.

†C1 is necessary only if main filter capacitor is more than 6" away, assuming #18 or larger leads.

††C2 is not absolutely necessary, but is suggested to lower high frequency output impedance. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

'C3 improves ripple rejection, output impedance, and noise. C2 should be 1 μF or larger close to the regulator if C3 is used.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input-Output Voltage Differential	20V
Operating Junction Temperature Range	
LM196 Control Section	−55°C to +150°C
Power Transistor	−55°C to +200°C
LM396 Control Section	0°C to +125°C
Power Transistor	0°C to +175°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD rating to be determined	

Pre-Conditioning

100% Burn-In in Thermal Limit

Electrical Characteristics (Note 1)

Parameter	Conditions	LM196			LM396			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	I_{OUT} = 10 mA	1.24	1.25	1.26	1.23	1.25	1.27	V
Reference Voltage (Note 2)	$V_{MIN} \le (V_{IN} - V_{OUT}) \le 20V$ 10 mA ≤ I_{OUT} 10A, P ≤ P_{MAX} Full Temperature Range	1.22	1.25	1.28	1.21	1.25	1.29	V
Line Regulation (Note 3)	$V_{MIN} \le (V_{IN} - V_{OUT}) \le 20V$ Full Temperature Range		0.005	0.01 0.05		0.005	0.02 0.05	%/V %/V
Load Regulation LM196/LM396 (Note 4)	10 mA ≤ I_{OUT} ≤ 10A $V_{MIN} \le V_{IN} - V_{OUT} \le 10V$, P ≤ P_{MAX} Full Temperature Range			0.1 0.15			0.1 0.15	%/V %/A
Ripple Rejection (Note 5)	C_{ADJ} = 25 μF, f = 120 Hz Full Temperature Range	60 54	74		66 54	74		dB dB
Thermal Regulation (Note 6)	$V_{IN} - V_{OUT}$ = 5V, I_{OUT} = 10A		0.003	0.005		0.003	0.015	%/W
Average Output Voltage Temperature Coefficient	$T_{jMIN} \le T_j \le T_{jMAX}$ (See Curves for Limits)		0.003			0.003		%/°C
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change (Note 7)	10 mA ≤ I_{OUT} ≤ 10A 3V ≤ $V_{IN} - V_{OUT}$ ≤ 20V P ≤ P_{MAX}, Full Temperature Range			3			3	μA
Minimum Load Current (Note 9)	2.5V ≤ $(V_{IN} - V_{OUT})$ ≤ 20V Full Temperature Range			10			10	mA
Current Limit (Note 8)	2.5 ≤ $(V_{IN} - V_{OUT}$ ≤ 7V $V_{IN} - V_{OUT}$ = 20V	10 1.5	14 3	20 8	10 1.5	14 3	20 8	A A
Rms Output Noise	10 Hz ≤ f ≤ 10 kHz		0.001			0.001		%V_{OUT}
Long Term Stability	T_j = 125°C, t = 1000 Hours		0.3	1.0		0.3	1.0	%
Thermal Resistance Junction to Case (Note 10)	Control Circuitry Power Transistor		0.3 1.0	0.5 1.2		0.3 1.0	0.5 1.2	°C/W °C/W

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions	LM196			LM396			Units
		Min	Typ	Max	Min	Typ	Max	
Power Dissipation (P_{MAX}) (Note 11)	$7.0V \le V_{IN} - V_{OUT} \le 12V$	70	100		70	100		W
	$V_{IN} - V_{OUT} = 15V$	50			50			W
	$V_{IN} - V_{OUT} = 18V$	36			36			W
Drop-Out Voltage LM196/LM396	$I_{OUT} = 10A$, Full Temperature Range		2.1	2.5 2.75		2.1	2.5 2.75	V

Note 1: Unless otherwise stated, these specifications apply for $T_j = 25°C$, $V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 10$ mA to 10A.

Note 2: This is a worst-case specification which includes all effects due to input voltage, output current, temperature, and power dissipation. Maximum power (P_{MAX}) is specified under Electrical Characteristics.

Note 3: Line regulation is measured on a short-pulse, low-duty-cycle basis to maintain constant junction temperature. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately. See discussion of Line Regulation under Application Hints.

Note 4: Load regulation on the 2-pin package is determined primarily by the voltage drop along the output pin. Specifications apply for an external Kelvin sense connnection at a point on the output pin ¼" from the bottom of the package. Testing is done on a short-pulse-width, low-duty-cycle basis to maintain constant junction temperature. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately. See discussion of Load Regulation under Application Hints.

Note 5: Ripple rejection is measured with the adjustment pin bypassed with 25 μF capacitor, and is therefore independent of output voltage. With no load or bypass capacitor, ripple rejection is determined by line regulation and may be calculated from; $RR = 20 \log_{10} [100/(K \times V_{OUT})]$ where K is line regulation expressed in %/V. At frequencies below 100 Hz, ripple rejection may be limited by thermal effects, if load current is above 1A.

Note 6: Thermal regulation is defined as the change in output voltage during the time period of 0.2 ms to 20 ms after a change in power dissipation in the regulator, due to either a change in input voltage or output current. See graphs and discussion of thermal effects under Application Hints.

Note 7: Adjustment pin current change is specified for the worst-case combination of input voltage, output current, and power dissipation. Changes due to temperature must be taken into account separately. See graph of adjustment pin current vs temperature.

Note 8: Current limit is measured 10 ms after a short is applied to the output. DC measurements may differ slightly due to the rapidly changing junction temperature, tending to drop slightly as temperature increases. A minimum available load current of 10A is guaranteed over the full temperature range as long as power dissipation does not exceed 70W, and $V_{IN} - V_{OUT}$ is less than 7.0V.

Note 9: Minimum load current of 10 mA is normally satisfied by the resistor divider which sets up output voltage.

Note 10: Total thermal resistance, junction-to-ambient, will include junction-to-case thermal resistance plus interface resistance and heat sink resistance. See discussion of Heat Sinking under Application Hints.

Note 11: Although power dissipation is internally limited, electrical specifications apply only for power dissipation up to the limits shown. Derating with temperature is a function of both power transistor temperature and control area temperature, which are specified differently. See discussion of Heat Sinking under Application Hints. For $V_{IN} - V_{OUT}$ less than 7V, power dissipation is limited by current limit of 10A.

Note 12: Dropout voltage is input-output voltage differential measured at a forced reference voltage of 1.15V, with a 10A load, and is a measurement of the minimum input/output differential at full load.

Application Hints

Further improvements in efficiency can be obtained by using Schottky diodes or high efficiency diodes with lower forward voltage, combined with larger filter capacitors to reduce ripple. However, this reduces the voltage difference between input and drive pins and may not allow sufficient voltage to fully saturate the pass transistor. Special transformers are available from Signal Transformer that have a 1V tap on the output winding to provide the extra voltage for the drive pin. The transformers are available as standard items for 5V applications at 5A, 10A and 20A. Other voltages are available on special request.

Heat Sinking

Because of its extremely high power dissipation capability, the *major limitation* in the load driving capability of the LM196 is *heat sinking*. Previous regulators such as LM109, LM340, LM117, etc., had internal power limiting circuitry which limited power dissipation to about 30W. The LM196 is guaranteed to dissipate up to 70W continuously, as long as the maximum junction temperature limit is not exceeded. This requires careful attention to all sources of thermal resistance from junction-to-ambient, including junction-to-case resistance, case-to-heat sink interface resistance (0.1–1.0°C/W), and heat sink resistance itself. A good thermal joint compound such as Wakefield type 120 or Thermalloy Thermocote must be used when mounting the LM196, especially if an electrical insulator is used to isolate the regulator from the heat sink. Interface resistance without this compound will be no better than 0.5°C/W, and probably much worse. With the compound, and no insulator, interface resistance will be 0.2°C/W or less, assuming 0.005" or less combined flatness run-out of TO-3 and heat sink. Proper torquing of the mounting bolts is important to achieve minimum thermal resistance. Four to six inch pounds is recommended. Keep in mind that good electrical, as well as thermal, contact must be made to the case.

Application Hints (Continued)

The actual heat sink chosen for the LM196 will be determined by the worst-case continuous full load current, input voltage and maximum ambient temperature. Overload or short circuit output conditions do not normally have to be considered when selecting a heat sink because the thermal shutdown built into the LM196 will protect it under these conditions. An exception to this is in situations where the regulator must recover very quickly from overload. The LM196 may take some time to recover to within specified output tolerance following an extended overload, if the regulator is cooling from thermal shutdown temperature (approximately 175°) to specified operating temperature (125°C or 150°C). The procedure for heat sink selection is as follows:

Calculate worst-case *continuous* average power dissipation in the regulator from $P = (V_{IN} - V_{OUT}) \times (I_{OUT})$. To do this, you must know the raw power supply voltage/current characteristics fairly accurately. For example, consider a 10V output with 15V nominal input voltage. At full load of 10A, the regulator will dissipate $P = (15 - 10) \times (10) = 50W$. If input voltage rises by 10%, power dissipation will increase to $(16.5 - 10) \times (10) = 65W$, a *30% increase.* It is strongly suggested that a raw supply be assembled and tested to determine its average DC output voltage *under full load with maximum line voltage.* Do not over-design by using unloaded voltage as a worst-case, since the regulator will not be dissipating any power under no load conditions. Worst-case regulator dissipation normally occurs under full load conditions except when the effective DC resistance of the raw supply ($\Delta V/\Delta I$) is larger than $(V_{IN}^* - V_{OUT})/2I_{fL}$, where V_{IN}^* is the lightly-loaded raw supply voltage and I_{fL} is full load current. For $(V_{IN}^* - V_{OUT}) = 5V - 8V$, and $I_{fL} = 5A-10A$, this gives a resistance of 0.25Ω to 0.8Ω. If raw supply resistance is higher than this, the regulator power dissipation may be *less* at full load current, then at some intermediate current, due to the large drop in input voltage. Fortunately, most well designed raw supplies have low enough output resistance that regulator dissipation does maximize at full load current, or very close to it, so tedious testing is not usually required to find worst-case power dissipation.

A very important consideration is the size of the filter capacitor in the raw supply. At these high current levels, capacitor size is usually dictated by ripple current ratings rather than just obtaining a certain ripple voltage. Capacitor ripple current (rms) is 2–3 times the DC output current of the filter. If the capacitor has just 0.05Ω DC resistance, this can cause 30W internal power dissipation at 10A output current. Capacitor life is very sensitive to operating temperature, decreasing by a factor of two for each 15°C rise in internal temperature. Since capacitor life is not all that great to start with, it is obvious that a small capacitor with a large internal temperature rise is inviting very short mean-time-to-failure. A second consideration is the loss of usable input voltage to the regulator. If the capacitor is small, the large dips in the input voltage may cause the LM196 to drop out of regulation. 2000 μF per ampere of load current is the *minimum* recommended value, yielding about 2 Vp-p ripple of 120 Hz. Larger values will have longer life and the reduced ripple will allow lower DC input voltage to the regulator, with subsequent cost savings in the transformer and heat sink. Sometimes several capacitors in parallel are better to decrease series resistance and increase heat dissipating area.

After the raw supply characteristics have been determined, and worst-case power dissipation in the LM196 is known, the heat sink thermal resistance can be found from the graphs titled Maximum Heat Sink Thermal Resistance. These curves indicate the minimim size heat sink required as a function of ambient temperature. They are derived from a case-to-control area thermal resistance of 0.5°C/W and a case-to-power transistor thermal resistance of 1.2°C/W. 0.2°C/W is assumed for interface resistance. A maximum control area temperature of 150°C is used for the LM196 and 125°C for the LM396. Maximum power transistor temperature is 200°C for the LM196 and 175°C for the LM396. For conservative designs, it is suggested that when using these curves, you assume an ambient temperature 25°C–50°C higher than is actually anticipated, to avoid running the regulator right at its design limits of operating temperature.

A quick look at the curves show that heat sink resistance (θ_{SA}) will normally fall into the range of 0.2°C/W–1.5°C/W. These are *not* small heat sinks. A model 441, for instance, which is sold by several manufacturers, has a θ_{SA} of 0.6°C/W with natural convection and is about five inches on a side. Smaller sinks are more volumetrically efficient, and larger sinks, less so. A rough formula for estimating the volume of heat sink required is: $V = 50/\theta_{SA}^{1.5}$ CU. IN. This holds for natural convection only. If the heat sink is inside a small sealed enclosure, θ_{SA} will increase substantially because the air is not free to form natural convection currents. Fan-forced convection can reduce θ_{SA} by a factor of two at 200 FPM air velocity, and by four at 1000 FPM.

Ripple Rejection

Ripple rejection at the normal ripple frequency of 120 Hz is a function of both electrical and thermal effects in the LM196. If the adjustment pin is not bypassed with a capacitor, it is also dependent on output voltage. A 25 μF capacitor from the adjustment pin to ground will make ripple rejection independent of output voltage for frequencies above 100 Hz. If lower ripple frequencies are encountered, the capacitor should be increased proportionally.

To keep in mind that the bypass capacitor on the adjustment pin will limit the turn-on time of the regulator. A 25 μF capacitor, combined with the output divider resistance, will give an extended output voltage settling time following the application of input power.

Load Regulation (LM196/LM396)

Because the LM196 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the output pin and the wire connecting the regulator to the load. For the data sheet specification, regulation is measured 1/4" from the bottom of the package on the output pin. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load.

Application Hints (Continued)

Although it may not be immediately obvious, best load regulation is obtained when the top of the divider is connected *directly* to the output pin, *not to the load*. This is illustrated in *Figure 2*. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$(Rw) \times \left(\frac{R2 + R1}{R1}\right)$$

Rw = Line Resistance

Connected as shown, Rw is not multiplied by the divider ratio. Rw is about 0.004Ω per foot using 16 gauge wire. This translates to 40 mV/ft at 10A load current, so it is important to keep the positive lead between regulator and load as short as possible.

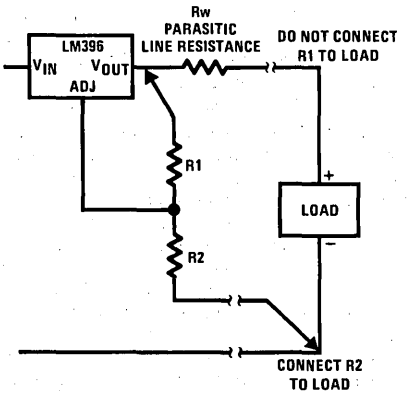


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FIGURE 2. Proper Divider Connection

The input resistance of the sense pin is typically 6 kΩ, modeled as a resistor between the sense pin and the output pin. Load regulation will start to degrade if a resistance higher than 10Ω is inserted in series with the sense. This assumes a worst-case condition of 0.5V between output and sense pins. Lower differential voltage will allow higher sense series resistance.

Thermal Load Regulation

Thermal, as well as electrical, load regulation must be considered with IC regulators. Electrical load regulation occurs in microseconds, thermal regulation due to die thermal gradients occurs in the 0.2 ms-20 ms time frame, and regulation due to overall temperature changes in the die occurs over a 20 ms to 20 minute period, depending on the time constant of the heat sink used. Gradient induced load regulation is calculated from

$$\Delta V_{OUT} = (V_{IN} - V_{OUT}) \times (\Delta I_{OUT}) \times (\beta)$$

β = Thermal regulation specified on data sheet.

For V_{IN} = 9V, V_{OUT} = 5V, ΔI_{OUT} = 10A, and β = 0.005%/W, this yields a 0.2% change in output voltage. Changes in output voltage due to overall temperature rise are calculated from

$$V_{OUT} = (V_{IN} - V_{OUT}) \times (\Delta I_{OUT}) \times (TC) \times (\theta_{jA})$$

TC = Temperature coefficient of output voltage.

θ_{jA} = Thermal resistance from junction to ambient. θ_{jA} is approximately 0.5°C/W + θ of heat sink.

For the same conditions as before, with TC = 0.003%/°C, and θ_{jA} = 1.5°C/W, the change in output voltage will be 0.18%. Because these two thermal terms can have either polarity, they may subtract from, or add to, electrical load regulation. For worst-case analysis, they must be assumed to add. If the output of the regulator is trimmed under load, only that portion of the load that changes need be used in the previous calculations, significantly improving output accuracy.

Line Regulation

Electrical line regulation is very good on the LM196—typically less than 0.005% change in output voltage for a 1V change in input. This level of regulation is achieved only for very low load currents, however, because of thermal effects. Even with a thermal regulation of 0.002%.W, and a temperature coefficient of 0.003%/°C, DC line regulation will be dominated by thermal effects as shown by the following example:

Assume V_{OUT} = 5V, V_{IN} = 9V, I_{OUT} = 8A

Following a 10% change in input voltage (0.9), the output will change quickly (≤100 μs), due to electrical effects, by (0.005%V) × (0.9V) = 0.0045%. In the next 20 ms, the output will change an additional (0.002%/W) × (8A) × (0.9V) = 0.0144% due to thermal gradients across the die. After a much longer time, determined by the time constant of the heat sink, the output will change an additional (0.003%/°C) × (8A) × (0.9V) × (2°C/W) = 0.043% due to the temperature coefficient of output voltage and the thermal resistance from die to ambient. (2°C/W was chosen for this calculation). The sign of these last two terms varies from part to part, so no assumptions can be made about any cancelling effects. All three terms must be added for a proper analysis. This yields 0.0045 + 0.0144 + 0.043 = 0.062% using *typical* values for thermal regulation and temperature coefficient. For worst-case analysis, the maximum data sheet specifications for thermal regulation and temperature coefficient should be used, along with the *actual* thermal resistance of the heat sink being used.

Paralleling Regulators

Direct paralleling of regulators is not normally recommended because they do not share currents equally. The regulator with the highest reference voltage will supply all the current to the load until it current limits. With an 18A load, for instance, one regulator might be operating in current limit at 16A while the second device is only carrying 2A. Power dissipation in the high current regulator is extremely high with attendant high junction temperatures. Long term reliability cannot be guaranteed under these conditions.

Quasi-paralleling may be accomplished if load regulation is not critical. The connection shown in *Figure 5a* will typically share to within 1A, with a worst-case of about 3A. Load regulation is degraded by 150 mV at 20A loads. An external op amp may be used as in *Figure 5b* to improve load regulation and provide remote sensing.

Application Hints (Continued)

Input and Output Capacitors

The LM196 will tolerate a wide range of input and output capacitance, but long wire runs or small values of output capacitance can sometimes cause problems. If an output capacitor is used, it should be 1 μF or larger. We suggest 10 μF solid tantalum if significant improvements in high frequency output impedance are needed (see output impedance graph). This capacitor should be as close to the regulator as possible, with short leads, to reduce the effects of lead inductance. No input capacitor is needed if the regulator is within 6 inches of the power supply filter capacitor, using 18 gauge stranded wire. For longer wire runs, the LM196 input should be bypassed locally with a 4.7 μF (or larger) solid tantalum capacitor, or a 100 μF (or larger) aluminum electrolytic capacitor.

Correcting for Output Wire Losses (LM196/LM396)

Three-terminal regulators can only provide partial Kelvin load sensing (see Load Regulation). Full remote sensing can be added by using an external op amp to cancel the effect of voltage drops in the unsensed positive output lead. In *Figure 7*, the LM301A op amp forces the voltage loss across the unsensed output lead to appear across R3. The current through R3 then flows out the V^- pin of the op amp through R4. The voltage drop across R4 will raise the output voltage by an amount equal to the line loss, just cancelling the line loss itself. A small ($\cong$ 40 mV) initial output voltage error is created by the quiescent current of the op amp. Cancellation range is limited by the maximum output current of the op amp, about 300 mV as shown. This can be raised by increasing R3 or R4 at the expense of more initial output error.

Transformers and Diodes

Proper transformer ratings are very important in a high current supply because of the conflicting requirements of efficiency and tolerance to low-line conditions. A transformer with a high secondary voltage will waste power and cause unnecessary heating in the regulator. Too low a secondary voltage will cause loss of regulation under low-line conditions. The following formulas may be used to calculate the required secondary voltage and current ratings using a full-wave center tap:

$$V_{rms} = \left(\frac{V_{OUT} + V_{REG} + V_{RECT} + V_{RIPPLE}}{\sqrt{2}}\right)\left(\frac{V_{NOM}}{V_{LOW}}\right)\left((1.1)^*\right)$$

$$I_{rms} = (I_{OUT})(1.2) \qquad \text{(Full-wave center tap)}$$

where:

V_{OUT} = DC regulated output voltage

V_{REG} = Minimum input-output voltage of regulator

V_{RECT} = Rectifier forward voltage drop at three times DC output current

V_{RIPPLE} = 1/2 peak-to-peak capacitor ripple voltage

$$= \frac{(5.3 \times 10^{-3})(I_{OUT})}{2C}$$

*The factor of 1.1 is only an approximate factor accounting for load regulation of the transformer.

V_{NOM} = Nominal line voltage AC rms

V_{LOW} = Low line voltage AC rms

I_{OUT} = DC output current

Example: I_{OUT} = 10A, V_{OUT} = 5V

Assume: V_{REG} = 2.2V, V_{RECT} = 1.2V

V_{RIPPLE} = 2 Vp-p, V_{NOM} = 115V,

V_{LOW} = 105V

$$V_{rms} = \left(\frac{5 + 2.2 + 1.2 + 1}{\sqrt{2}}\right)\left(\frac{115}{105}\right)1.1$$

$$= 8.01\ V_{rms}$$

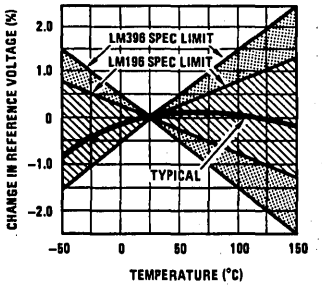
$$\text{Capacitor C} = \frac{(5.3 \times 10^{-3})(I_{OUT})}{2 \times V_{RIPPLE}}$$

$$= \frac{(5.3 \times 10^{-3})(10)}{2} = 26{,}500\ \mu F$$

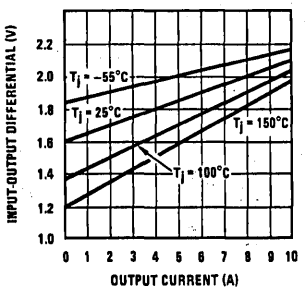
The diodes used in a full-wave rectified capacitor input supply must have a DC current rating considerably higher than the average current flowing through them. In a 10A supply, for instance, the average current through each diode is only 5A, but the diodes should have a rating of 10A–15A. There are many reasons for this, both thermal and electrical. The diodes conduct current in pulses about 3.5 ms wide with a peak value of 5–8 times the average value, and an rms value 1.5–2.0 times the average value. This results in long term diode heating roughly equivalent to 10A DC current. The most demanding condition however, may be the one cycle surge through the diode during power turn on. The peak value of the surge is about 10–20 times the DC output current of the supply, or 100A–200A for a 10A supply. The diodes must have a one cycle non-repetitive surge rating of 200A or more, and this is usually not found in a diode with less than 10A average current rating. Keep in mind that even though the LM196 may be used at current levels below 10A, the diodes may still have to survive shorted output conditions where average current could rise to 12A–15A. Smaller transformers and filter capacitors used in lower current supplies will reduce surge currents, but unless specific information is available on worst-case surges, it is best not to economize on diodes. Stud-mounted devices in a DO-4 package are recommended. Cathode-to-case types may be bolted directly to the same heat sink as the LM196 because the case of the regulator is its power input. Part numbers to consider are the 1N1200 series rated at 12A average current in a DO-4 stud package. Additional types include common cathode duals in a TO-3 package, both standard and Schottky, and various duals in plastic filled assemblies. Schottky diodes will improve efficiency, especially in low voltage applications. In a 5V supply for instance, Schottky diodes will decrease wasted power by up to 6W, or alternatively provide an additional 5% "drop out" margin for low-line conditions. Several manufacturers are producing "high efficiency" diodes with a forward voltage drop nearly as good as Schottkys at high current levels. These devices do not have the low breakdown voltages of Schottkys, so are much less prone to reverse breakdown induced failures.

Typical Performance Characteristics

Reference Drift

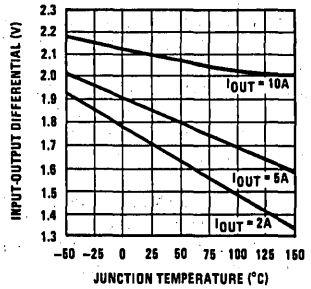


Minimum Input-Output Differential*



*V_{IN} is reduced until output drops 2%

Minimum Input-Output Differential*



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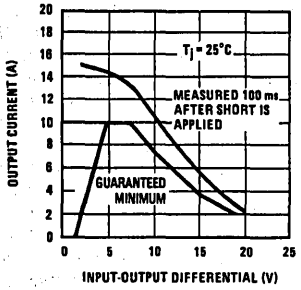
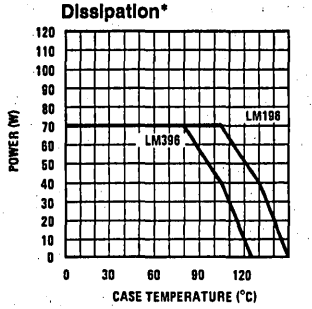
*V_{IN} is reduced until output drops 2%

Current Limit

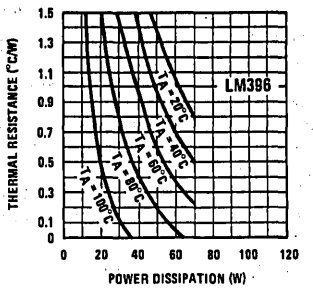


Maximum Power Dissipation*



*As limited by maximum junction temperature.

Maximum Heat Sink Thermal Resistance*



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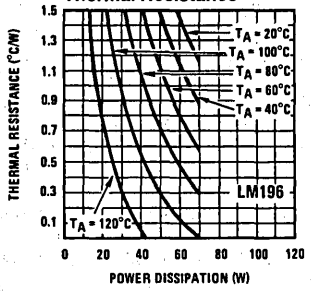
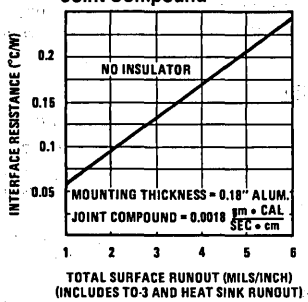
*See "Heat Sinking" under Applications Hints.

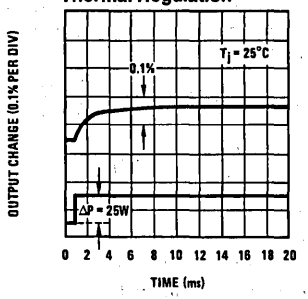
Maximum Heat Sink Thermal Resistance*



TO-3 Interface Thermal Resistance Using Thermal Joint Compound



Thermal Regulation



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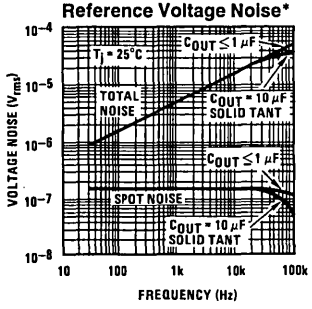
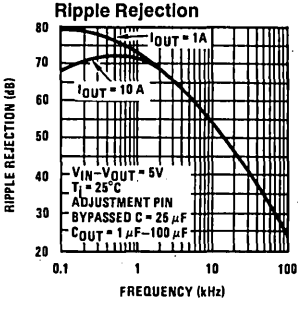
*See "Heat Sinking" under Application Hints.

Typical Performance Characteristics (Continued)

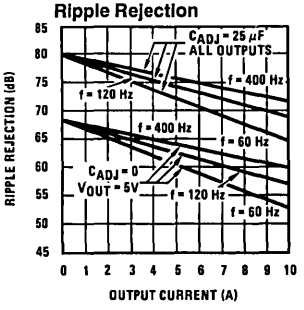
Reference Voltage Noise*



Ripple Rejection



Ripple Rejection



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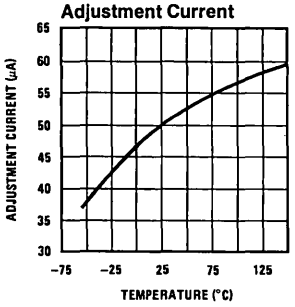
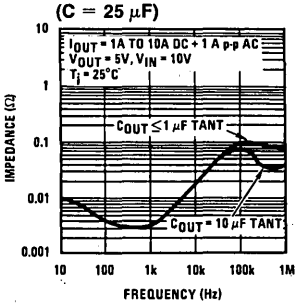
*To obtain output noise, multiply by $V_{OUT}/1.25$ if adjustment pinis not bypassed.

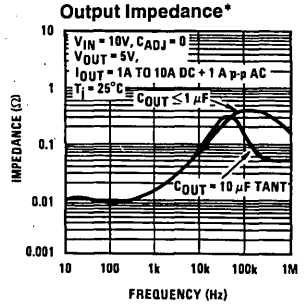
Adjustment Current



Output Impedance Adjustment Pin Bypassed (C = 25 μF)



Output Impedance*



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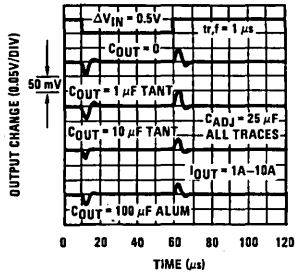
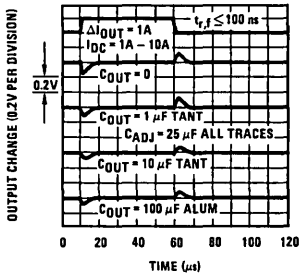
*For output voltages other than 5V, multiply vertical scale readings by $V_{OUT}/5$.

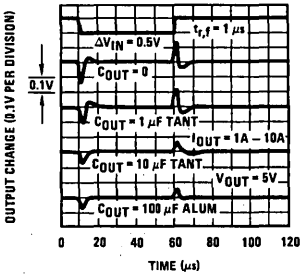
Line Transient Response Adjustment Pin Bypassed



Load Transient Response Adjustment Pin Bypassed



Line Transient Response*



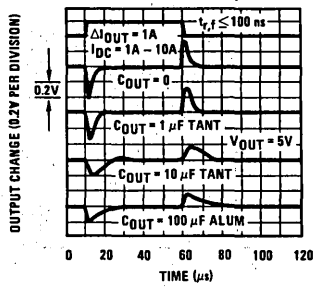
TL/H/9059–8

*With no adjustment pin bypass. For output voltages other than 5V, multiply vertical scale by $V_{OUT}/5$.

4

Typical Performance Characteristics (Continued)

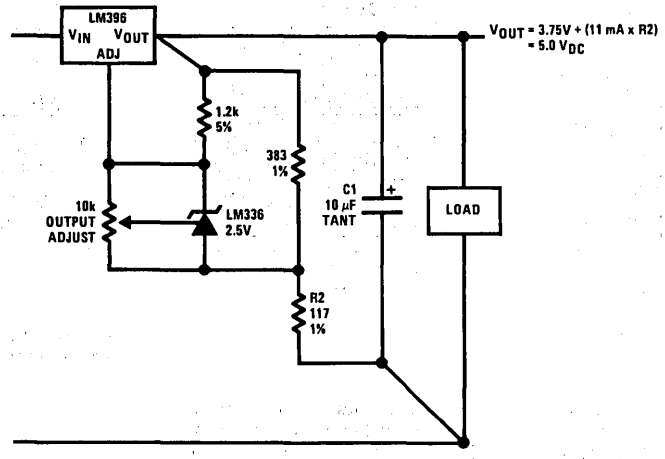
Load Transient Response*



TL/H/9059–9

*With no adjustment pin bypass. For output voltages other than 5V, multiply vertical scale by $V_{OUT}/5$.

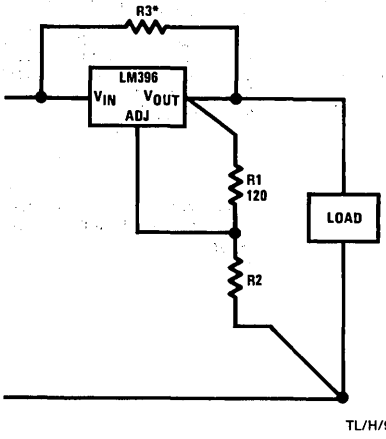
Typical Applications (Continued)



TL/H/9059–10

*Regulation can be improved by adding an LM336 reference diode to increase the effective reference voltage to 3.75V. Load and line regulation are improved by 3:1, including thermal effects.

FIGURE 3. Improving Regulation*



TL/H/9059–11

*R3 is selected to supply partial load current. Therefore, a minimum load must always be maintained to prevent the regulated output from rising uncontrolled. R3 must be greater than $(V_{MAX} - V_{OUT})/I_{MIN}$, where V_{MAX} is worst-case high input voltage, and I_{MIN} is the minimum load current. R3 must be rated for at least $(V_{IN} - V_{OUT})^2/R3$ watts. Regulator power dissipation will be reduced by a factor of 2–3 in a typical situation where minimum load current is 1/2 full load current. Regulator dissipation will peak at:

$$V_{IN} = \frac{(R3)(I_{OUT})}{2} + V_{OUT}$$

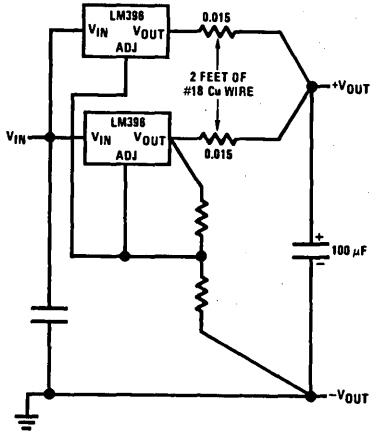
and will be equal to:

$$P_{MAX} = \frac{(R3)(I_{OUT})^2}{4} \text{ Assuming: } (R3)(I_{OUT}) \leq V_{MAX} - V_{OUT}$$

A few words of caution; (1) R3 power rating must be increased to $(V_{MAX})^2/R3$ if continuous output shorts are possible. (2) Under normal load conditions, system power dissipation is not changed, but under short circuit conditions *system* power dissipation increases by $(V_{IN})^2/R3$ watts over the already high power of a shorted regulator. The LM196 will not be harmed and neither will R3 if it is rated properly, but the raw supply components must be able to withstand the overload also. Thermal shutdown of the LM196 will probably occur for sustained shorts, somewhat alleviating the problem.

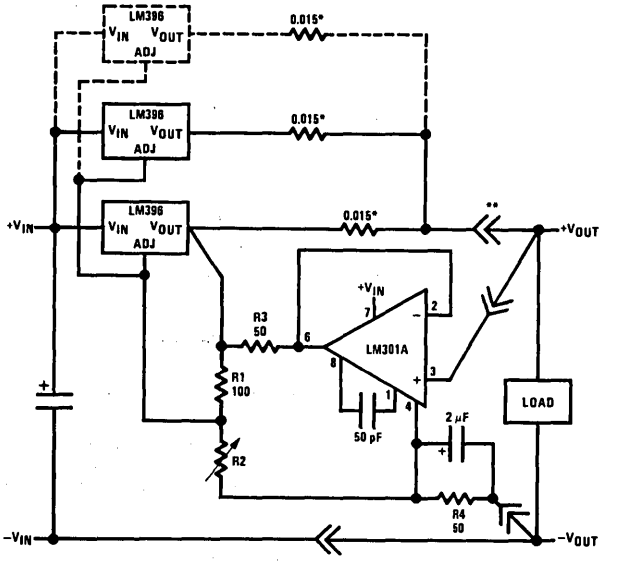
FIGURE 4. Reducing Regulator Power Dissipation

Typical Applications (Continued)



TL/H/9059–12

FIGURE 5a. Paralleling Regulators

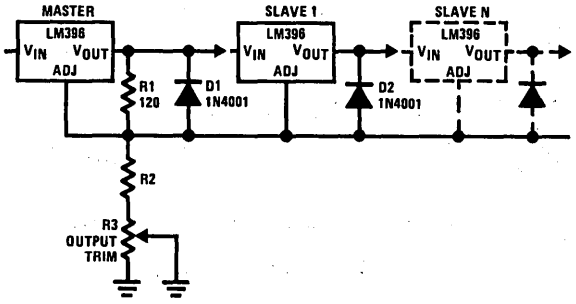


TL/H/9059–13

*2 feet of #18 CU wire

**Total voltage drop across output wire and connector should not exceed 0.3V

FIGURE 5b

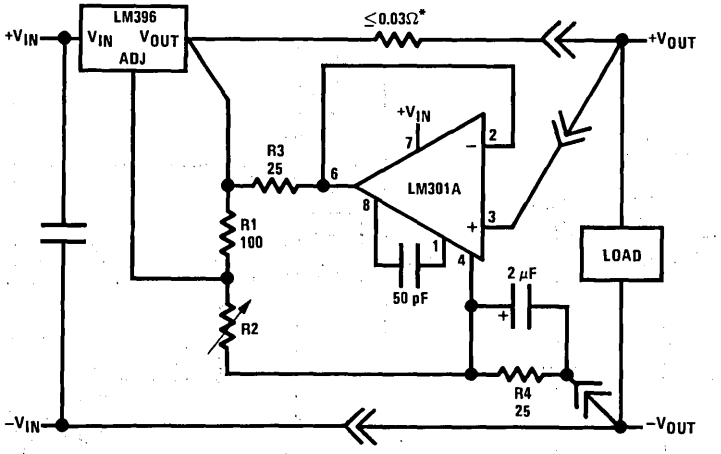


TL/H/9059–14

Output will be within ±20 mV at 25°C, no load. Regulation of tracking units is improved by $V_{OUT}/1.25$ compared to a normal connection. Regulation of master unit is unchanged. Load or input voltage changes on slave units do not affect other units, but all units will be affected by changes on master. A short on any output will cause all other outputs to drop to approximately 2V.

FIGURE 6. Tracking Regulators

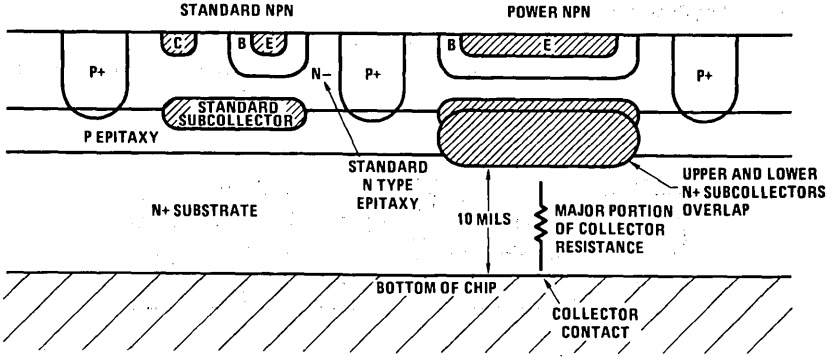
Typical Applications (Continued)



TL/H/9059–15

*Parasatic line resistance created by wiring connectors, or parallel ballasting.

FIGURE 7. Correcting for Line Losses



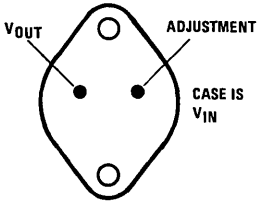
TL/H/9059–16

Power NPNs have low collecter resistance, and do not require collector bond wires. Collectors are all common to substrate. Standard NPNs are still isolated.

FIGURE 8. Process Technology

Connection Diagram

Metal Can Package

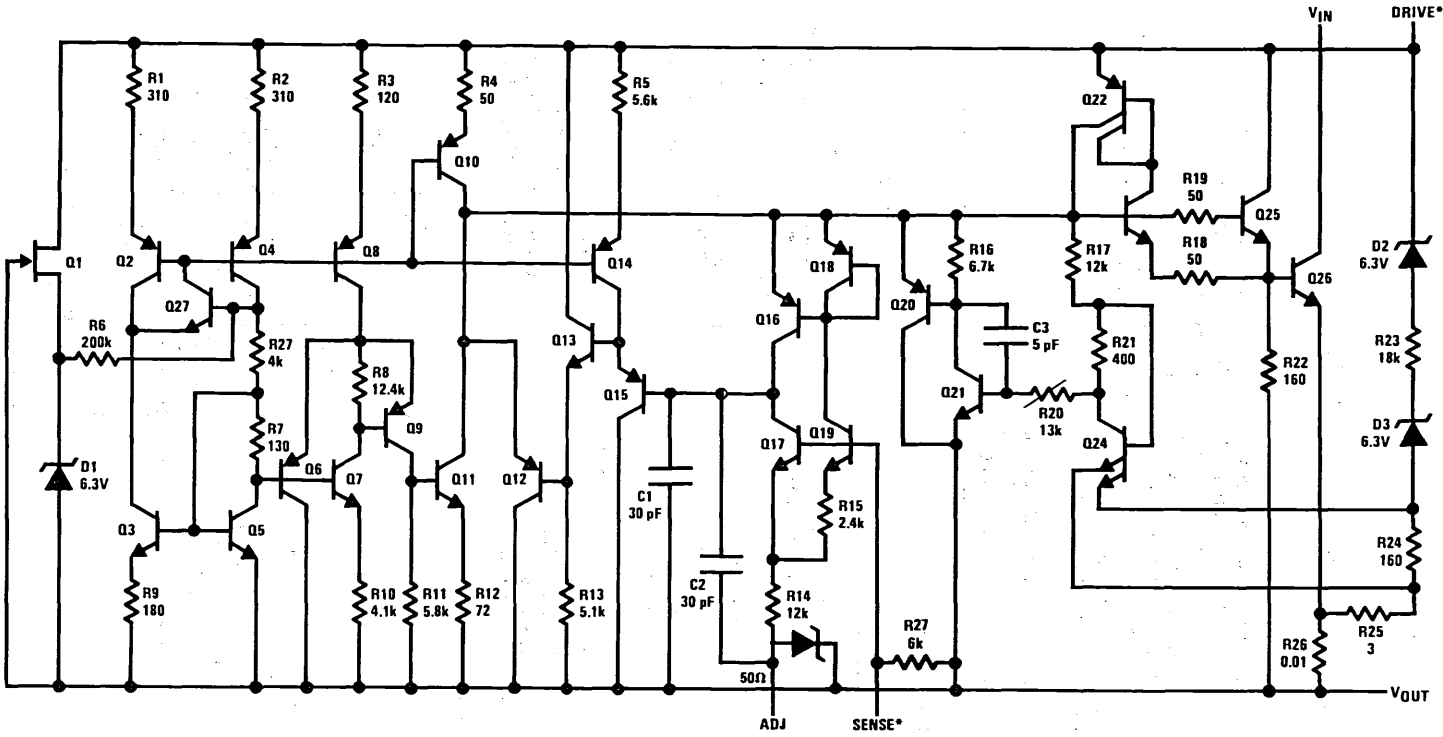


TL/H/9059–18

Bottom View

Order Number LM196K STEEL or LM396K STEEL
See NS Package Number K02B

Schematic Diagram*



TL/H/9059–17

*Drive is tied to V_{IN} and sense is tied to V_{OUT} on LM196 and LM396.

National Semiconductor

LM723/LM723C Voltage Regulator

General Description

The LM723/LM723C is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723/LM723C is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

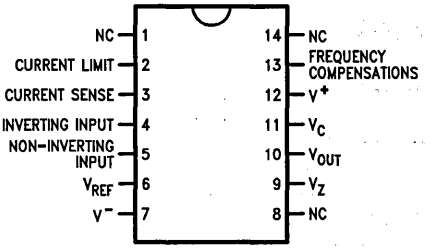
The LM723C is identical to the LM723 except that the LM723C has its performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Features

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

Connection Diagrams

Dual-In-Line Package

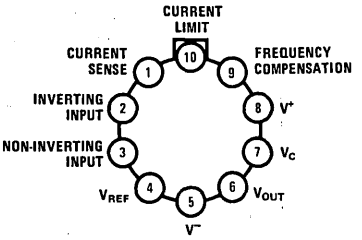


TL/H/8563-2

Top View

Order Number LM723J, LM723CJ, LM723CM or LM723CN
See NS Package J14A, M14A or N14A

Metal Can Package



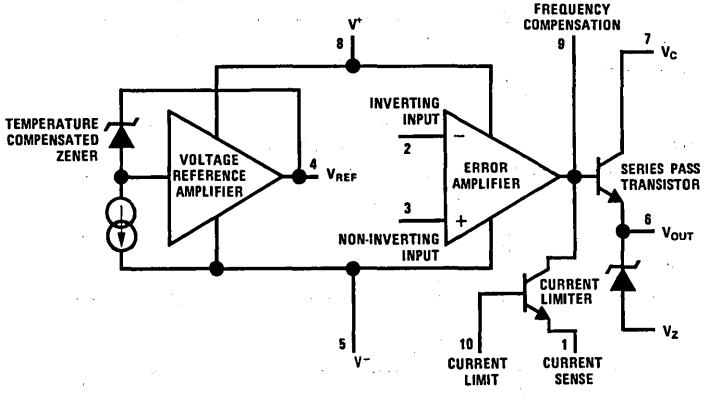
TL/H/8563-3

Note: Pin 5 connected to case.

Top View

Order Number LM723H or LM723CH
See NS Package H10C

Equivalent Circuit*



TL/H/8563-4

*Pin numbers refer to metal can package.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

Pulse Voltage from V^+ to V^- (50 ms)	50V
Continuous Voltage from V^+ to V^-	40V
Input-Output Voltage Differential	40V
Maximum Amplifier Input Voltage (Either Input)	8.5V
Maximum Amplifier Input Voltage (Differential)	5V
Current from V_Z	25 mA
Current from V_{REF}	15 mA

Internal Power Dissipation Metal Can (Note 1)	800 mW
Cavity DIP (Note 1)	900 mW
Molded DIP (Note 1)	660 mW
Operating Temperature Range LM723	−55°C to +150°C
LM723C	0°C to +70°C
Storage Temperature Range Metal Can	−65°C to +150°C
Molded DIP	−55°C to +150°C
Lead Temperature (Soldering, 4 sec. max.)	
Hermetic Package	300°C
Plastic Package	260°C
ESD Tolerance (Human body model, 1.5 kΩ in series with 100 pF)	1200V

Electrical Characteristics (Note 2)

Parameter	Conditions	LM723			LM723C			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		0.01	0.1		0.01	0.1	% V_{OUT}
	−55°C ≤ T_A ≤ +125°C			0.3				% V_{OUT}
	0°C ≤ T_A ≤ +70°C						0.3	% V_{OUT}
	V_{IN} = 12V to V_{IN} = 40V		0.02	0.2		0.1	0.5	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.15		0.03	0.2	% V_{OUT}
	−55°C ≤ T_A ≤ +125°C			0.6				% V_{OUT}
	0°C ≤ T_A ≤ +70°C						0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86			86		dB
Average Temperature Coefficient of Output Voltage (Note 8)	−55°C ≤ T_A ≤ +125°C		0.002	0.015				%/°C
	0°C ≤ T_A ≤ +70°C					0.003	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		86			86		μVrms
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5			2.5		μVrms
Long Term Stability			0.05			0.05		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		1.7	3.5		1.7	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input-Output Voltage Differential		3.0		38	3.0		38	V
θ_{JA}	Molded DIP		105			105		°C/W
θ_{JA}	Cavity DIP		150			150		°C/W
θ_{JA}	H10C Board Mount in Still Air		165			165		°C/W
θ_{JA}	H10C Board Mount in 400 LF/Min Air Flow		66			66		°C/W
θ_{JA}	SO					125		°C/W
θ_{JC}			22			22		°C/W

Note 1: See derating curves for maximum power rating above 25°C.

Note 2: Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in *Figure 1.* Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

Note 3: L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

Note 4: Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.

Note 5: Replace R1/R2 in figures with divider shown in *Figure 13.*

Note 6: V^+ and V_{CC} must be connected to a +3V or greater supply.

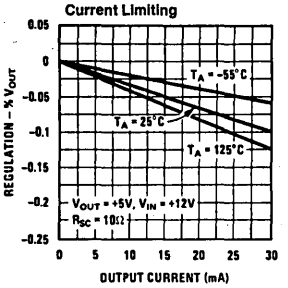
Note 7: For metal can applications where V_Z is required, an external 6.2V zener diode should be connected in series with V_{OUT}.

Note 8: Guaranteed by correlation to other tests.

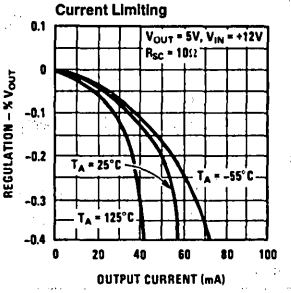
Note 9: Refer to RETS723X military specifications for the LM723.

Typical Performance Characteristics

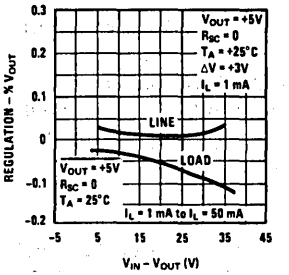
Load Regulation Characteristics with Current Limiting



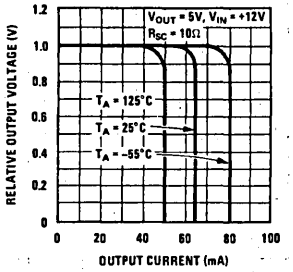
Load Regulation Characteristics with Current Limiting



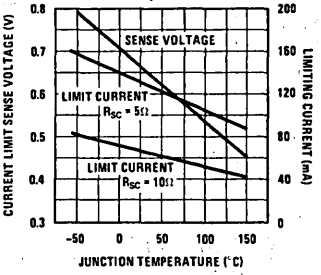
Load & Line Regulation vs Input-Output Voltage Differential



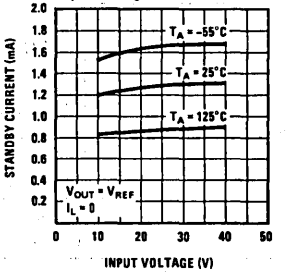
Current Limiting Characteristics



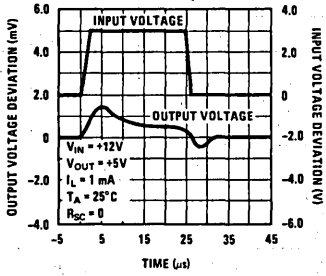
Current Limiting Characteristics vs Junction Temperature



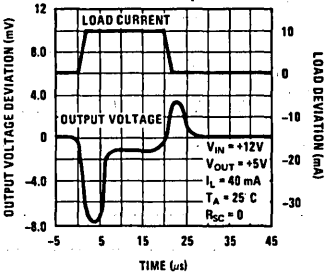
Standby Current Drain vs Input Voltage



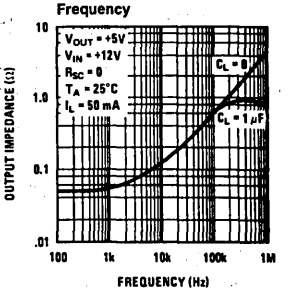
Line Transient Response



Load Transient Response



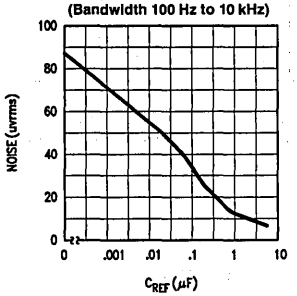
Output Impedence vs Frequency



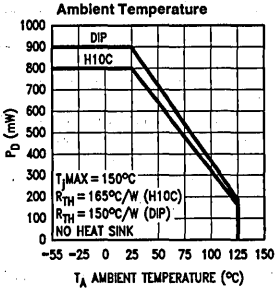
TL/H/8563–6

Maximum Power Ratings

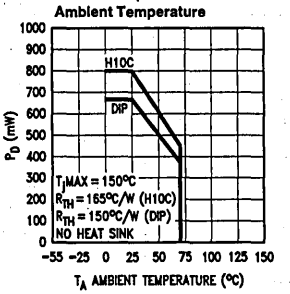
Noise vs Filter Capacitor (C_{REF} in Circuit of *Figure 1*) (Bandwidth 100 Hz to 10 kHz)



LM723 Power Dissipation vs Ambient Temperature



LM723C Power Dissipation vs Ambient Temperature



TL/H/8563–7

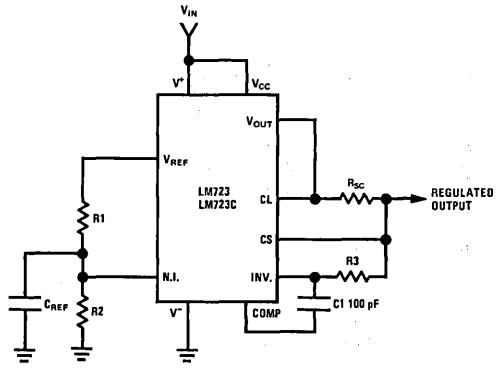
TABLE I. Resistor Values (kΩ) for Standard Output Voltage

Positive Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10% (Note 5)			Negative Output Voltage	Applicable Figures	Fixed Output ±5%		5% Output Adjustable ±10%		
	(Note 4)	R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	0.75	0.5	2.2	−6 (Note 6)	3, (10)	3.57	2.43	1.2	0.5	0.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 9, 12)	1.87	7.15	0.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II. Formulae for Intermediate Output Voltages

Outputs from +2 to +7 volts (*Figures 1, 5, 6, 9, 12, [4]*) $V_{OUT} = \left(V_{REF} \times \frac{R2}{R1 + R2}\right)$	**Outputs from +4 to +250 volts** (*Figure 7*) $V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1}\right)$; R3 = R4	**Current Limiting** $I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$
Outputs from +7 to +37 volts (*Figures 2, 4, [5, 6, 9, 12]*) $V_{OUT} = \left(V_{REF} \times \frac{R1 + R2}{R2}\right)$	**Outputs from −6 to −250 volts** (*Figures 3, 8, 10*) $V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1}\right)$; R3 = R4	**Foldback Current Limiting** $I_{KNEE} = \left(\frac{V_{OUT}\,R3}{R_{SC}\,R4} + \frac{V_{SENSE}\,(R3 + R4)}{R_{SC}\,R4}\right)$ $I_{SHORT\ CKT} = \left(\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right)$

Typical Applications



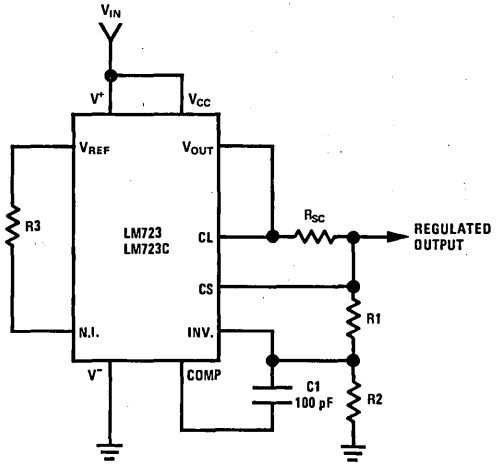
TL/H/8563–8

Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.

Typical Performance

Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 1. Basic Low Voltage Regulator (V_{OUT} = 2 to 7 Volts)



TL/H/8563–9

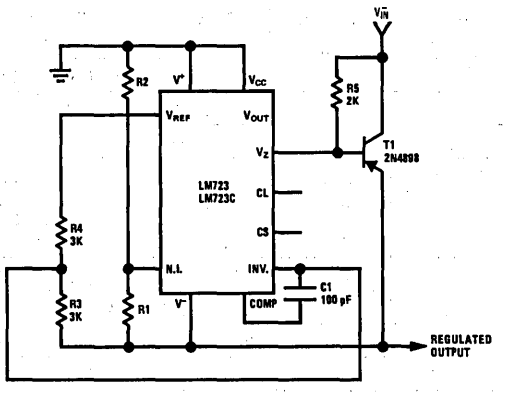
Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift. R3 may be eliminated for minimum component count.

Typical Performance

Regulated Output Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 50 mA)	4.5 mV

FIGURE 2. Basic High Voltage Regulator (V_{OUT} = 7 to 37 Volts)

Typical Applications (Continued)

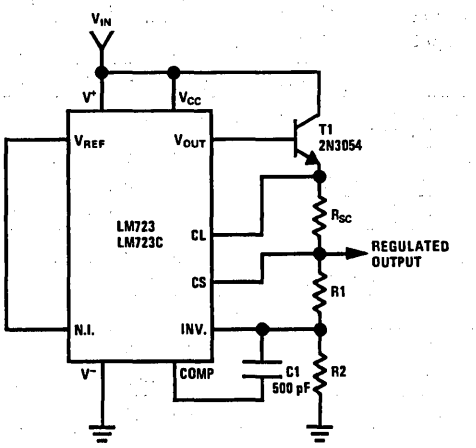


TL/H/8563–10

Typical Performance

Regulated Output Voltage	−15V
Line Regulation (ΔV_{IN} = 3V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

FIGURE 3. Negative Voltage Regulator

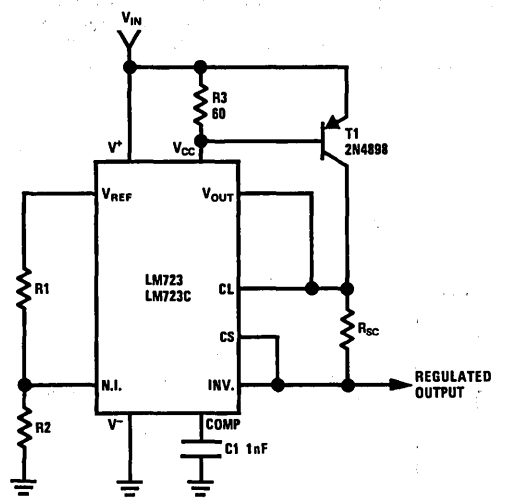


TL/H/8563–11

Typical Performance

Regulated Output Voltage	+15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 1A)	15 mV

FIGURE 4. Positive Voltage Regulator (External NPN Pass Transistor)

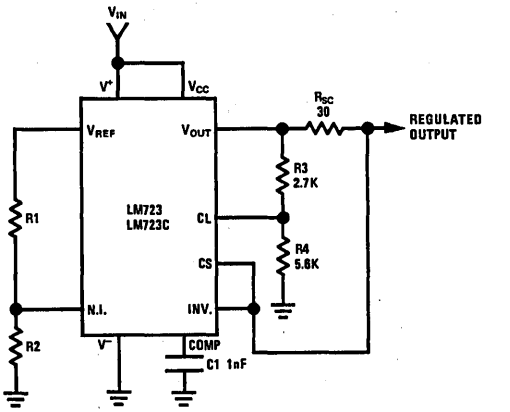


TL/H/8563–12

Typical Performance

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 1A)	5 mV

FIGURE 5. Positive Voltage Regulator (External PNP Pass Transistor)



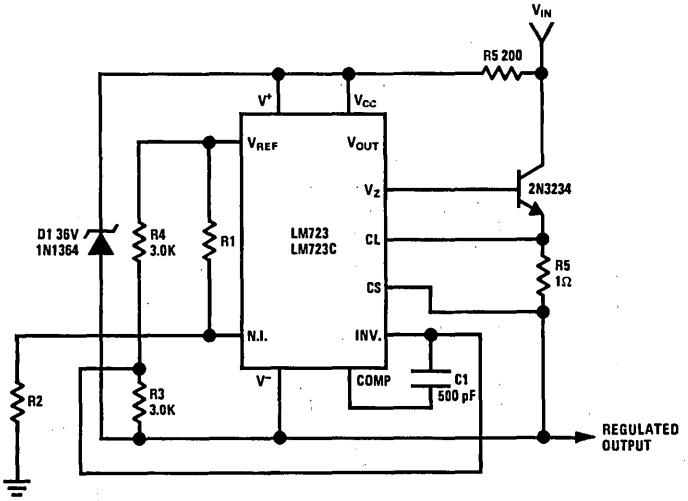
TL/H/8563–13

Typical Performance

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Short Circuit Current	20 mA

FIGURE 6. Foldback Current Limiting

Typical Applications (Continued)

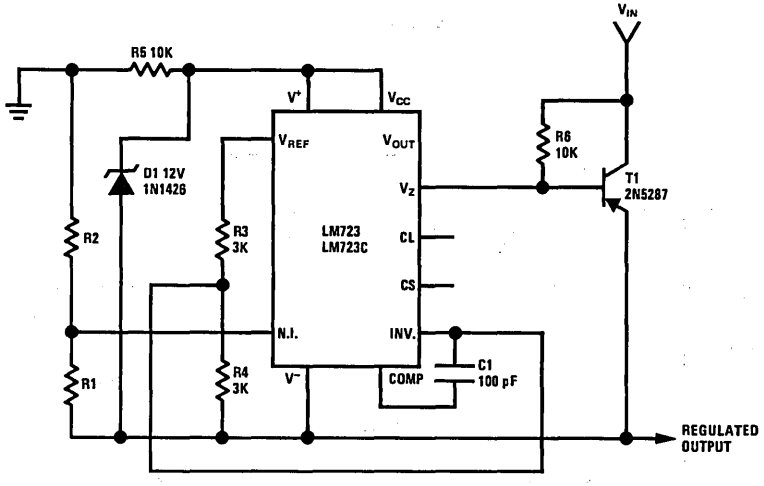


TL/H/8563–14

Typical Performance

Regulated Output Voltage	+50V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

FIGURE 7. Positive Floating Regulator



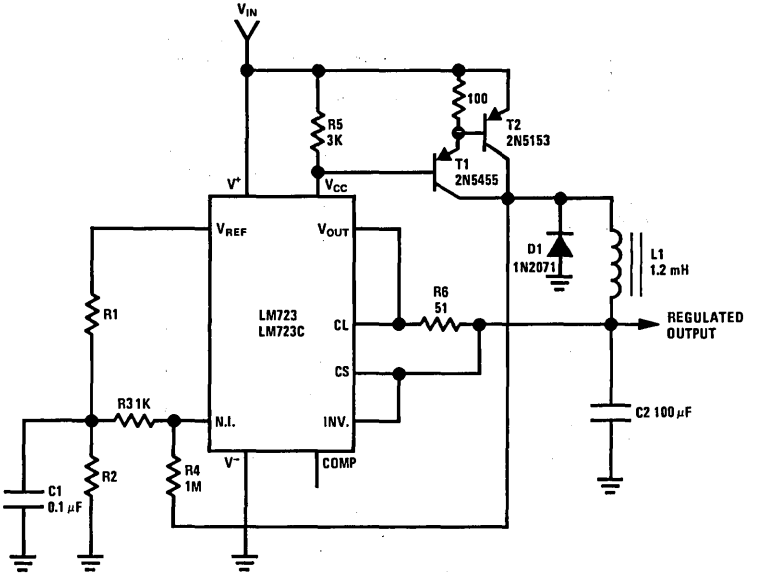
TL/H/8563–15

Typical Performance

Regulated Output Voltage	−100V
Line Regulation (ΔV_{IN} = 20V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

FIGURE 8. Negative Floating Regulator

Typical Applications (Continued)

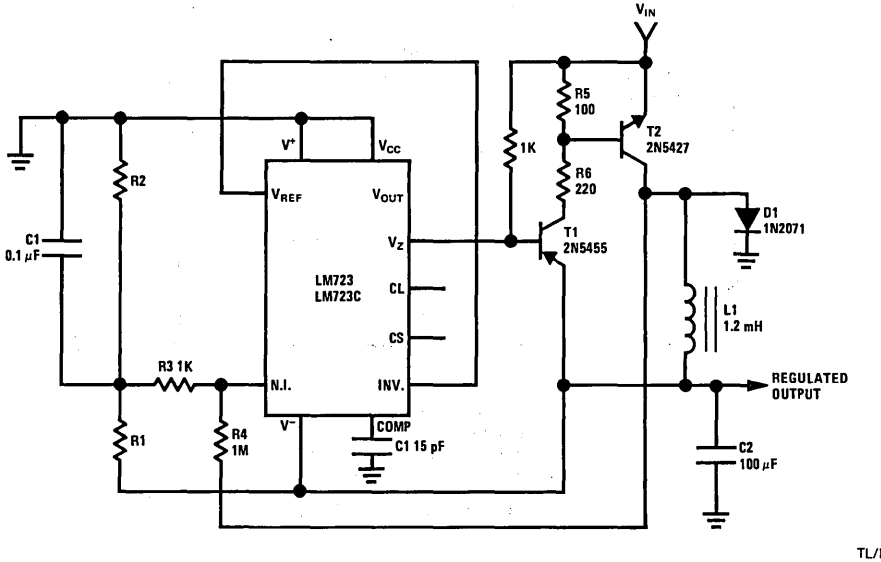


TL/H/8563–16

Typical Performance

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (ΔI_L = 2A)	80 mV

FIGURE 9. Positive Switching Regulator



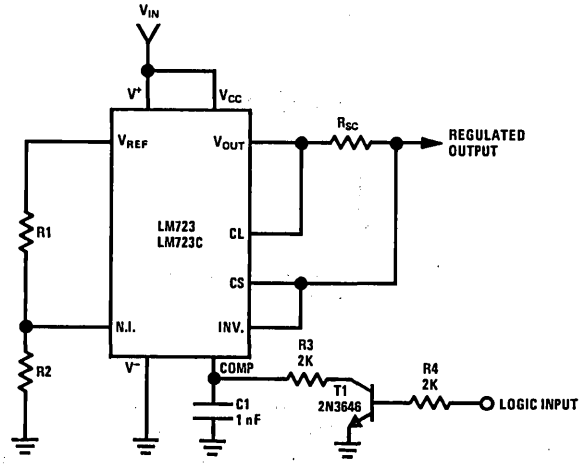
TL/H/8563–17

Typical Performance

Regulated Output Voltage	−15V
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (ΔI_L = 2A)	6 mV

FIGURE 10. Negative Switching Regulator

Typical Applications (Continued)



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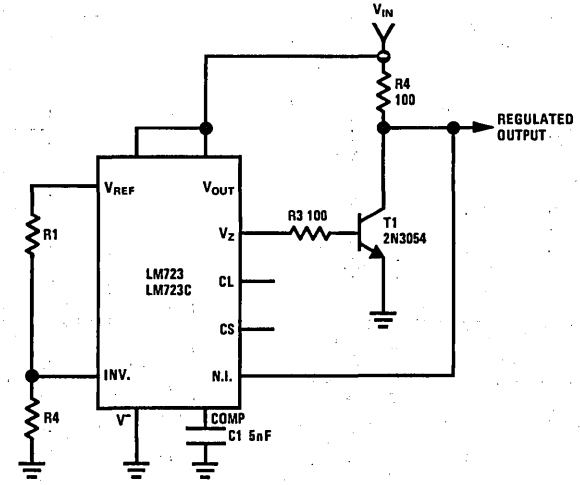
Note: Current limit transistor may be used for shutdown if current limiting is not required.

Typical Performance

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 11. Remote Shutdown Regulator with Current Limiting



TL/H/8563–19

Typical Performance

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 10V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

FIGURE 12. Shunt Regulator

Typical Applications (Continued)

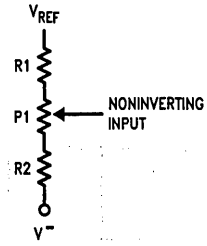


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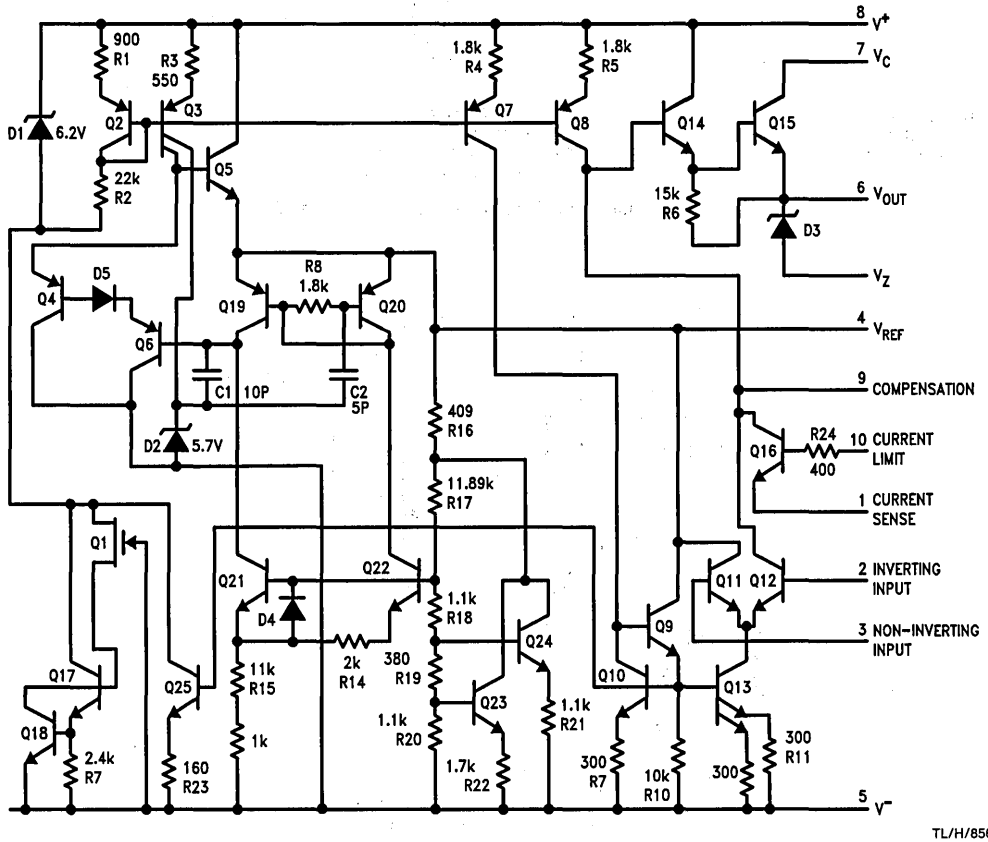
FIGURE 13. Output Voltage Adjust (See Note 5)

Schematic Diagram



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Section 5

EPROM, EEPROM, and SRAM

Section 5 Contents

National Semiconductor

PRELIMINARY

NM27LV512
524,288-Bit (64k x 8) Low Voltage EPROM

General Description

The NM27LV512 is a high performance Low Voltage Electrical Programmable Read Only Memory. It is manufactured using National's latest 1.2μ CMOS split gate SVG EPROM technology. This technology allows the part to operate at speeds as fast as 200 ns over commercial temperature (0°C to 70°C), and 250 ns over industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive handheld and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

National still maintains its' commitment to high quality and reliability with EPI processing on the NM27LV512. Latch-up immunity is guaranteed for stresses up to 200 mA on address and data pins from −1V to V_{CC} + 0.3V. ESD protection is guaranteed to 2000V.

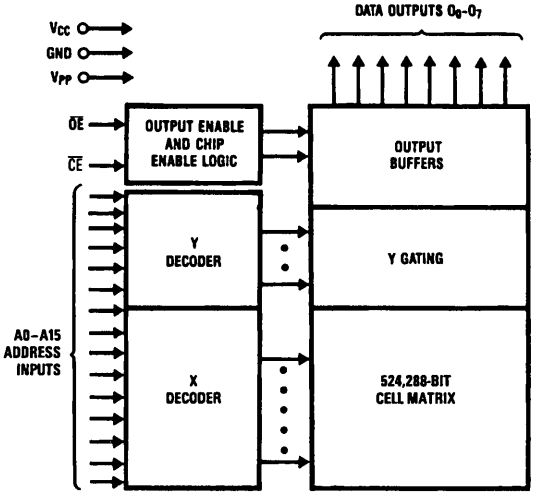
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has forseen this need and provides windowed LCC for prototyping and software development, PLCC for production runs, and TSOP for PC board space sensitive users.

The NM27LV512 is one member of National's growing Low Voltage product family.

Features

- 3.0V to 5.5V operation
- 200 ns access time
- Low current operation
  - — 15 mA I_{CC} Active Current @ 5 MHz
  - — 20 μA I_{CC} Standby Current @ 5 MHz
- Ultra Low Power operation
  - — 50 μW Standby Power @ 3.3V
  - — 50 mW Active Power @ 3.3V
- High reliability EPI processing
  - — Latch up immunity up to 200 mA
  - — 2000V ESD protection
- Surface mount package options
  - — 28-pin CERPACK
  - — 32-pin PLCC

Block Diagram



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5

Connection Diagram

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Access Time (ns)*
NM27LV512 L, V 200	200
NM27LV512 L, V 250	250
NM27LV512 L, V 300	300

Extended Temp Range (−40°C to +85°C)

Parameter/Order Number	Access Time (ns)*
NM27LV512 LE, VE, TE 250	250

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

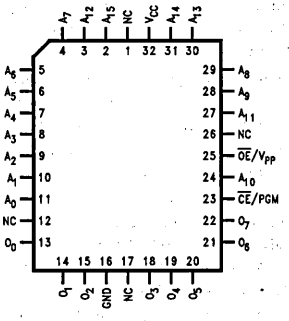
*All versions are guaranteed to function for slower speeds.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

Package Types: NM27LV512 L, T, V
V = PLCC Package
L = LCC Package

PLCC



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature −65°C to +150°C

All Input Voltages Except A9 with Respect to Ground −0.6V to +7V

V_{PP} and A9 with Respect to Ground −0.7V to +14V

V_{CC} Supply Voltage with Respect to Ground −0.6V to +7V

ESD Protection (MIL Std. 883, Method 3015.2) >2000V

All Output Voltages with Respect to Ground V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Comm'l	0°C to +70°C	3.3V	±0.3V
Industrial	−40°C to +85°C	3.3V	±0.3V

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.3	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage (TTL)	I_{OL} = 2.0 mA			0.4	V
V_{OH1}	Output High Voltage (TTL)	I_{OH} = −2.0 mA		2.4		V
V_{OL2}	Output Low Voltage (CMOS)	I_{OL} = 100 μA			0.2	V
V_{OH2}	Output High Voltage (CMOS)	I_{OH} = −100 μA		V_{CC} − 0.3		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V			20	μA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH}			50	μA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	f = 5 MHz		15	mA
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA C, I Temp Ranges			15	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 3.3V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 3.3V or GND		−1	1	μA

AC Electrical Characteristics

Symbol	Parameter	200		250		300		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	
t_{OE}	$\overline{OE}$ to Output Delay		75		100		120	
t_{DF}	Output Disable to Output Float	0	60	0	60	0	105	
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	20	25	pF

AC Test Conditions

Output Load: 1 TTL Gate and $C_L = 100$ pF (Note 8)

Input Rise and Fall Times: ≤5 ns

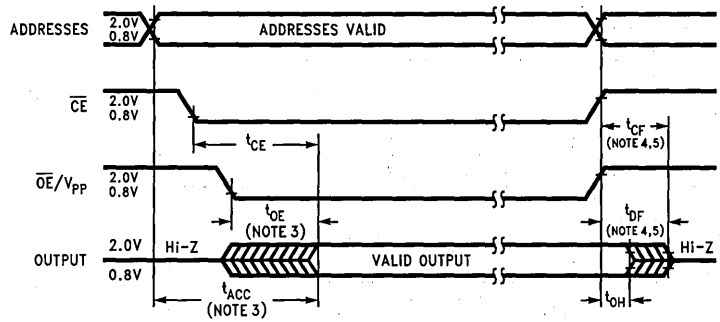
Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level (Note 9)

Inputs: 0.8V and 2V

Outputs: 0.8V and 2V

AC Waveforms (Notes 6, 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.

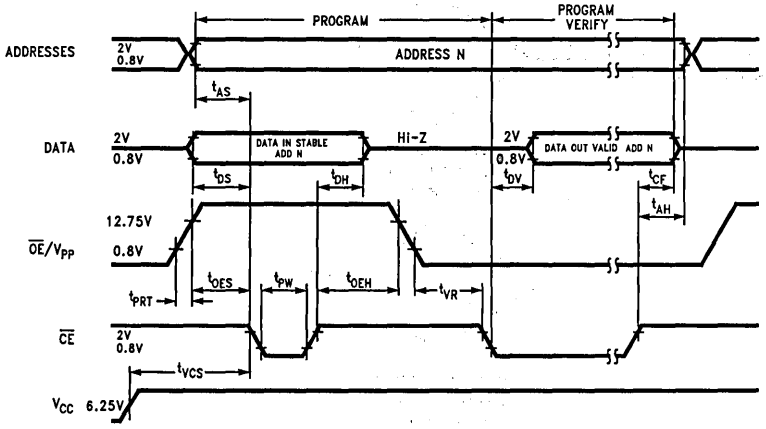
Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1 and 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing Reference Voltage		0.8		2	V

Programming Waveforms



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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Same as NMC27C512A)

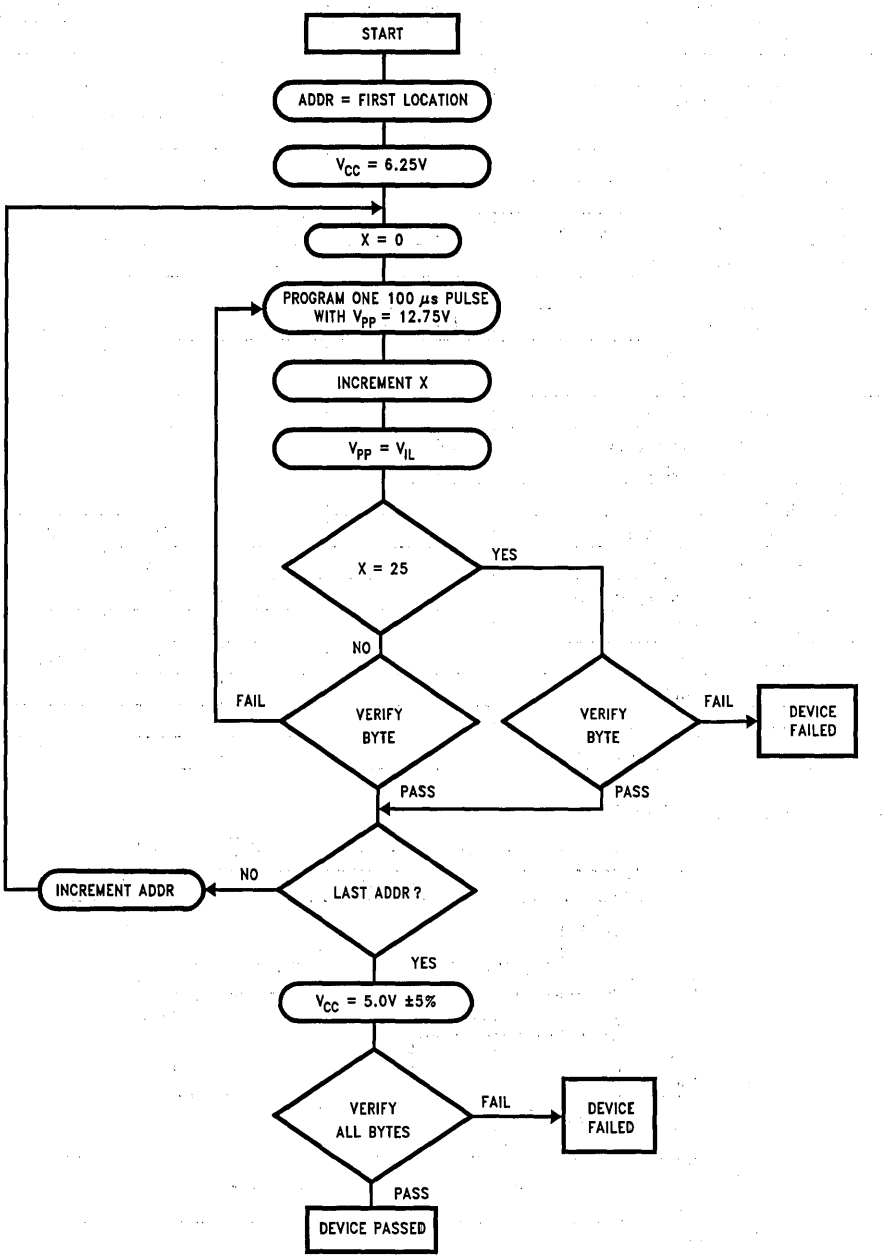

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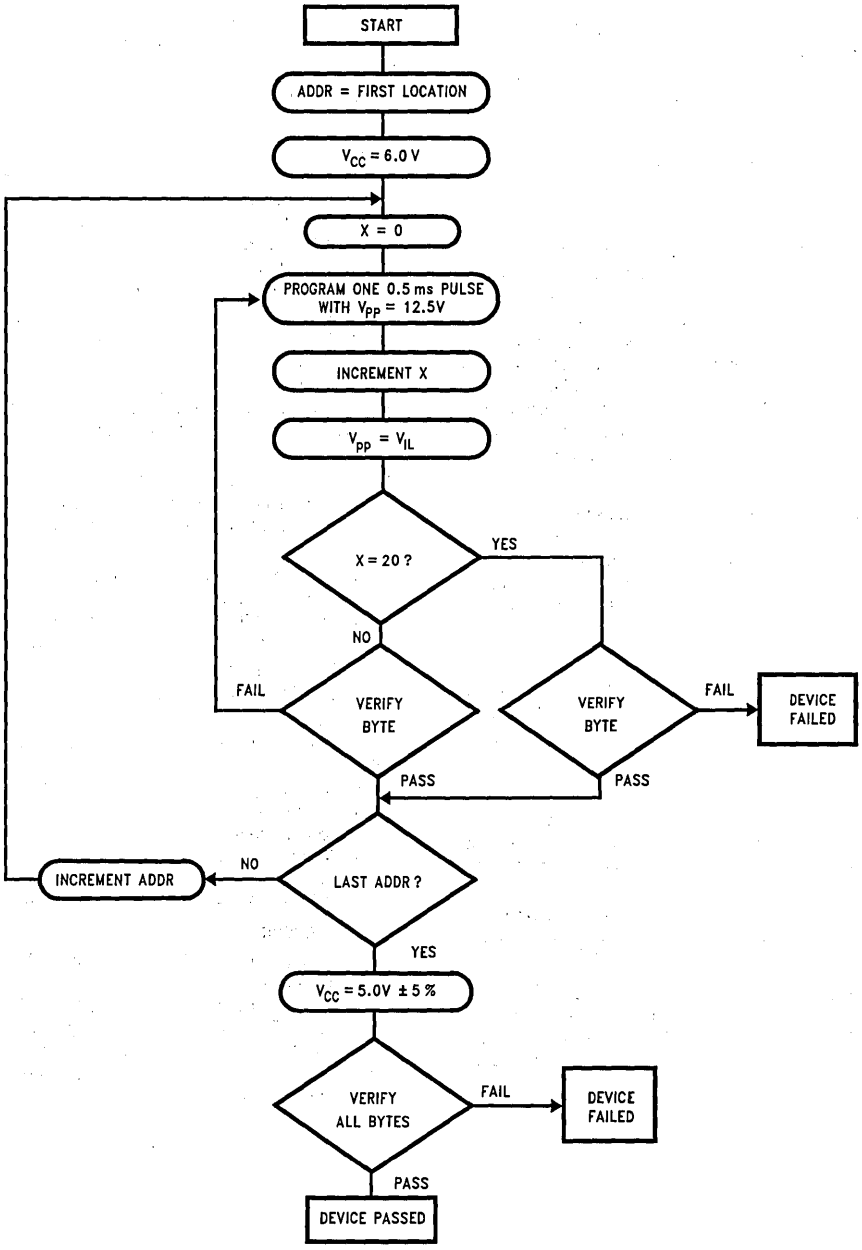
FIGURE 1

Interactive Programming Algorithm Flow Chart



TL/D/11375–8

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and $\overline{OE}/V_{PP}$. The $\overline{OE}/V_{PP}$ power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 44 mW to 110 μW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the OE/V_{PP} is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed.

The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled EPROM.

Note: Some programmer manufacturers, due to equipment limitation, may offer interactive program Algorithm (shown in *Figure 2*).

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}/V_{PP}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROMs from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified T_{DV} after the falling edge of $\overline{CE}$.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27LV512 is "8F85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A15, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27LV512 are listed in Table I. A single 3.3V power supply is required in the read mode. All inputs are TTL levels excepts for V_{PP} and A9 for device signature.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	3.3V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	3.3V	High Z
Standby	V_{IH}	X	3.3V	High Z
Programming	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	0	1	85

National Semiconductor

NM27LV010
1,048,576-Bit (128k x 8) Low Voltage EPROM

General Description

The NM27LV010 is a high performance Low Voltage Electrically Programmable Read Only Memory. It is manufactured using National's latest 1.2μ CMOS split gate SVG EPROM technology. This technology allows the part to operate at speeds as fast as 200 ns over Industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

National still maintains its commitment to high quality and reliability with EPI processing on the NM27LV010. Latch-up immunity is guaranteed for stresses up to 200 mA on address and data pins from −1V to V_{CC} + 0.3V. ESD protection is guaranteed for 2000V.

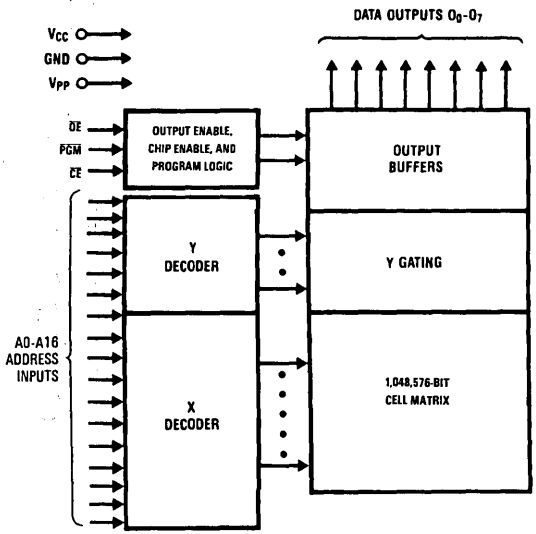
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has foreseen this need and provides windowed LCC for prototyping and software development, PLCC for production runs, and TSOP for PC board sensitive applications.

The NM27C010 is one member of National's growing Low Voltage product Family.

Features

- 3.0V to 5.5V operation
- 200 ns access time
- Low current operation
  - 15 mA I_{CC} active current @ 5 MHz
  - 20 μA I_{CC} standby current @ 5 MHz
- Ultra low power operation
  - 33 μW standby power @ 3.3V
  - 50 mW active power @ 3.3V
- High reliability EPI processing
  - Latch-up immunity up to 200 mA
  - 2000V ESD protection
- Surface mount package options
  - TSOP package
  - 32-pin PLCC

Block Diagram



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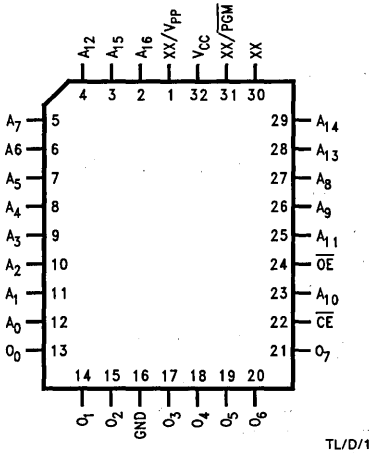
Connection Diagram

PLCC and CLCC Pin Configuration



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Top View

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 3.3 ± 0.3

Parameter/Order Number	Access Time (ns)
NM27LV010 L, V, T 200	200
NM27LV010 L, V, T 250	250
NM27LV010 L, V, T 300	300

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
V_{PP}	Programming Voltage

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 3.3 ± 0.3

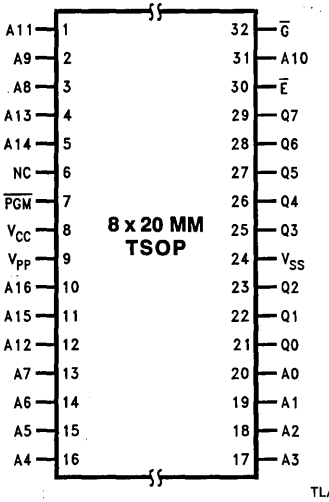
Parameter/Order Number	Access Time (ns)
NM27LV010 LE, VE, TE	250
NM27LV010 LE, VE, TE	300

Note: Surface mount PLCC available for commercial and extended temperature ranges only.

Package Types: NM27LV010 L, V, T
L = Quartz-Windowed LCC Package
T = TSOP
V = PLCC

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

TSOP Pin Configuration



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	3.3V	±0.3
Industrial	−40°C to +85°C	3.3V	±0.3

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.3	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage (TTL)	I_{OL} = 2.0 mA			0.4	V
V_{OH1}	Output High Voltage (TTL)	I_{OH} = −2.0 mA		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 100 μA			0.2	V
V_{OH2}	Output High Voltage (CMOS)	I_{OH} = −100 μA		V_{CC} − 0.3		
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V			20	μA
I_{SB2}	V_{CC} Standby Current(TTL)	$\overline{CE}$ = V_{IH}			100	μA
I_{CC}	V_{CC} Active Current	$\overline{CE}$ + $\overline{OE}$ = V_{IL}, I/O = 0 μA	f = 5 MHz		15	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 3.0V or GND			1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 3.0V or GND		−1	1	μA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	200		250		300		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	
t_{OE}	$\overline{OE}$ to Output Delay		70		70		75	
t_{DF} (Note 2)	Output Disable to Output Float		50		50		60	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

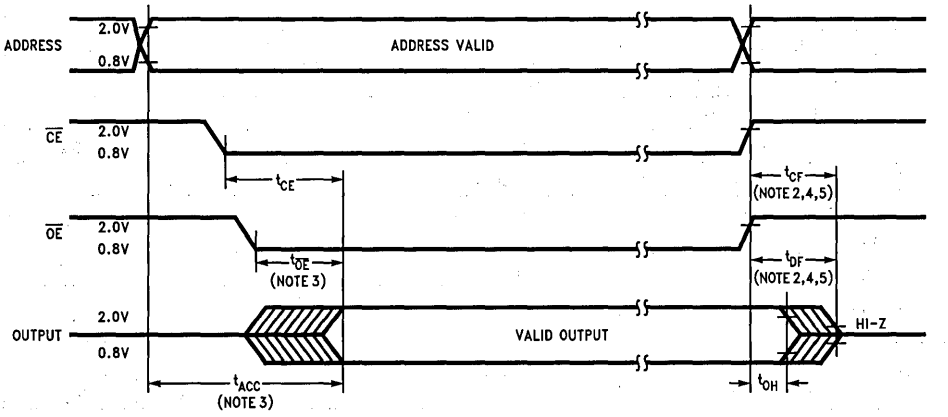
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, and 9)



TL/D/11377–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.2 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

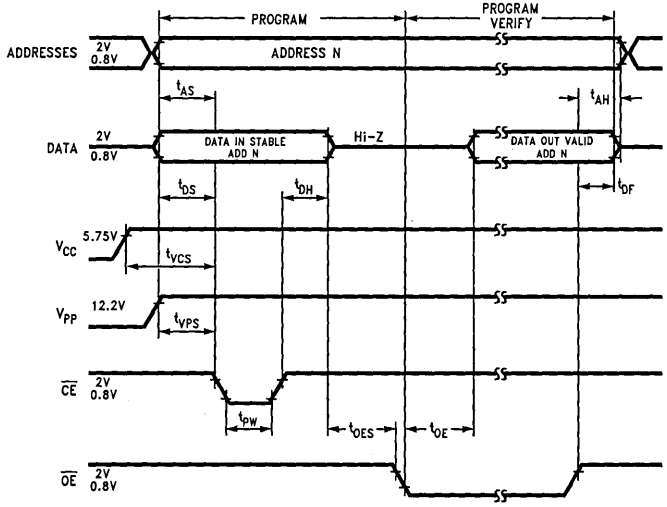
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			20	mA
I_{CC}	V_{CC} Supply Current				20	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveform (Note 3)



TL/D/11377–4

Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

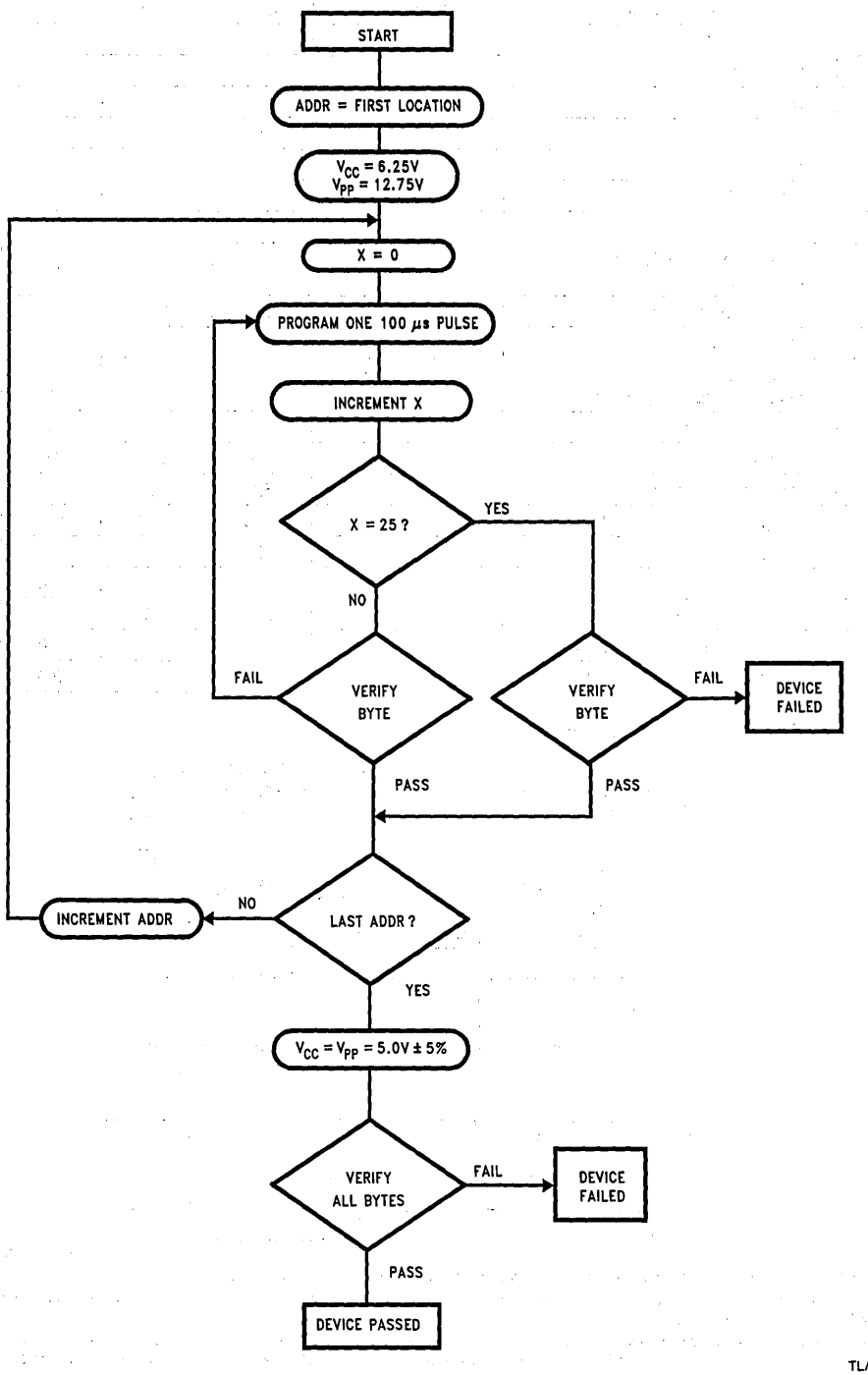
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/11377–5

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 50 mW to 33 μW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP} and V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27LV010 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1 Megabit (128k x 8) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O0–07. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27LV010 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	3.3V	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	3.3V	High Z
Standby	V_{IH}	X	V_{CC}	3.3V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	12.75V	12.75V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	1	0	86

National Semiconductor

PRELIMINARY

NM27LV210
1,048,576-Bit (64K x 16) Low Voltage EPROM

General Description

The NM27LV210 is a high performance Low Voltage Electrical Programmable read only memory. It is manufactured using National's latest 1.2μ CMOS split gate SVG EPROM technology. This technology allows the part to operate at speeds as fast as 200 ns over commercial temperature (0°C to +70°C) and 250 ns over industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

National still maintains its commitment to High Quality and Reliability with EPI processing on the NM27LV210. Latch up immunity is guaranteed for stresses up to 200 mA on address and data pins from −1V to V_{CC} + 0.3V. ESD protection is also guaranteed up to 2000V.

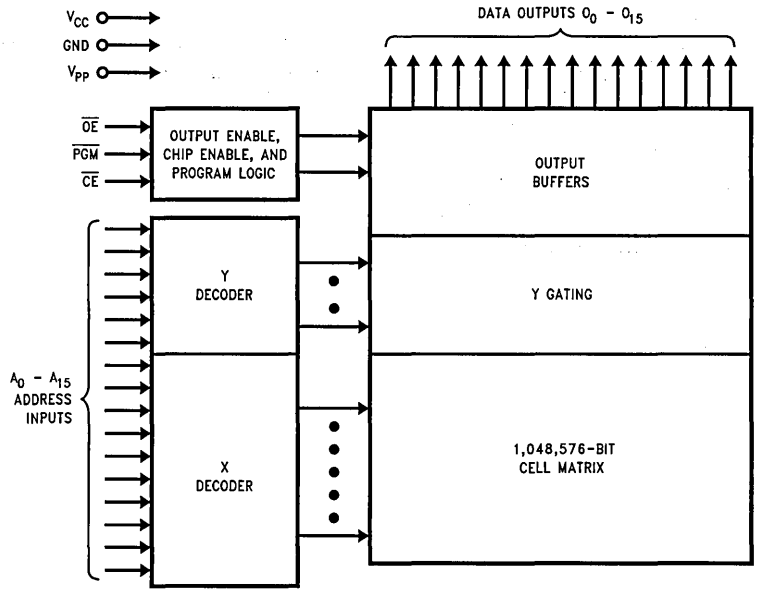
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has foreseen this need and provides windowed LCC for prototyping and software development, PLCC for production runs, and TSOP for PC board sensitive users.

The NM27LV010 is one member of National's growing Low Voltage product family.

Features

- 3.0V to 5.5V operation
- 200 ns maximum access time
- Low current operation
  - 15 mA I_{CC} active current @ 5 MHz
  - 20 μA I_{CC} standby current @ 5 MHz
- Ultra low power operation
  - 60 μA standby power @ 3.3V
  - 50 mW active power @ 3.3V
- High reliability EPI processing
  - Latch up immunity up to 200 mA
  - 2000V ESD protection
- Surface mount package options
  - TSOP package
  - 44-Pin PLCC

Block Diagram



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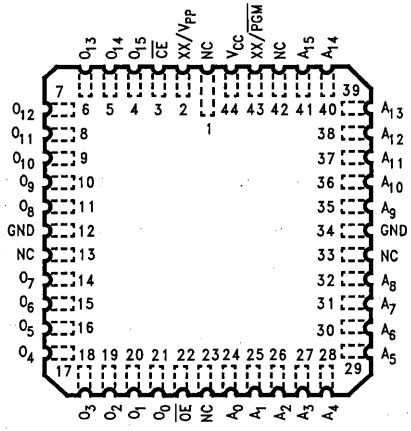
TSOP Pin Configuration

PLCC Pin Configuration



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Top View

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LV210 V, T	200
NM27LV210 V, T	250
NM27LV210 V, T	300

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LV210 VE, TE	250
NM27LV210 VE, TE	300

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
NC	No Connect
V_{PP}	Programming Voltage

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

Package Types: NM27LV210 V, TXXX
T = TSOP Type 1
V = PLCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	3.3	±0.3
Industrial	−40°C to +85°C	3.3	±0.3

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.3	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} ±0.3	V
V_{OL1}	Output Low Voltage (TTL)				0.4	V
V_{OH1}	Output High Voltage (TTL)			2.4		V
V_{OL2}	Output Low Voltage (CMOS)				0.2	V
V_{OH2}	Output High Voltage (CMOS)			V_A −0.3		V
I_{SB1}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$			50	μA
I_{SB2}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC}$ ±0.3V			20	μA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 μA	f = 5 MHz		20	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
I_{LI}	Input Load Current	V_{IN} = 3.3 or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 3.3V or GND		−1	1	μA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	200		250		300		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	
t_{OE}	$\overline{OE}$ to Output Delay		70		70		75	
t_{DF} (Note 2)	Output Disable to Output Float	0	50	0	50	0	60	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

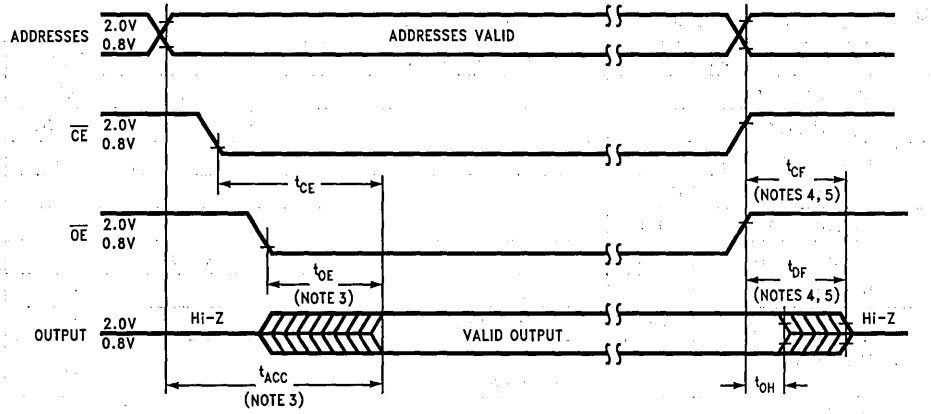
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	12	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
C_L: 100 pF includes fixture capacitance.

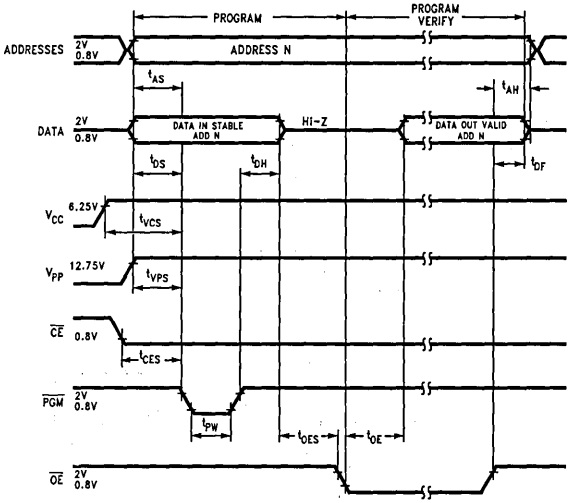
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4 & 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

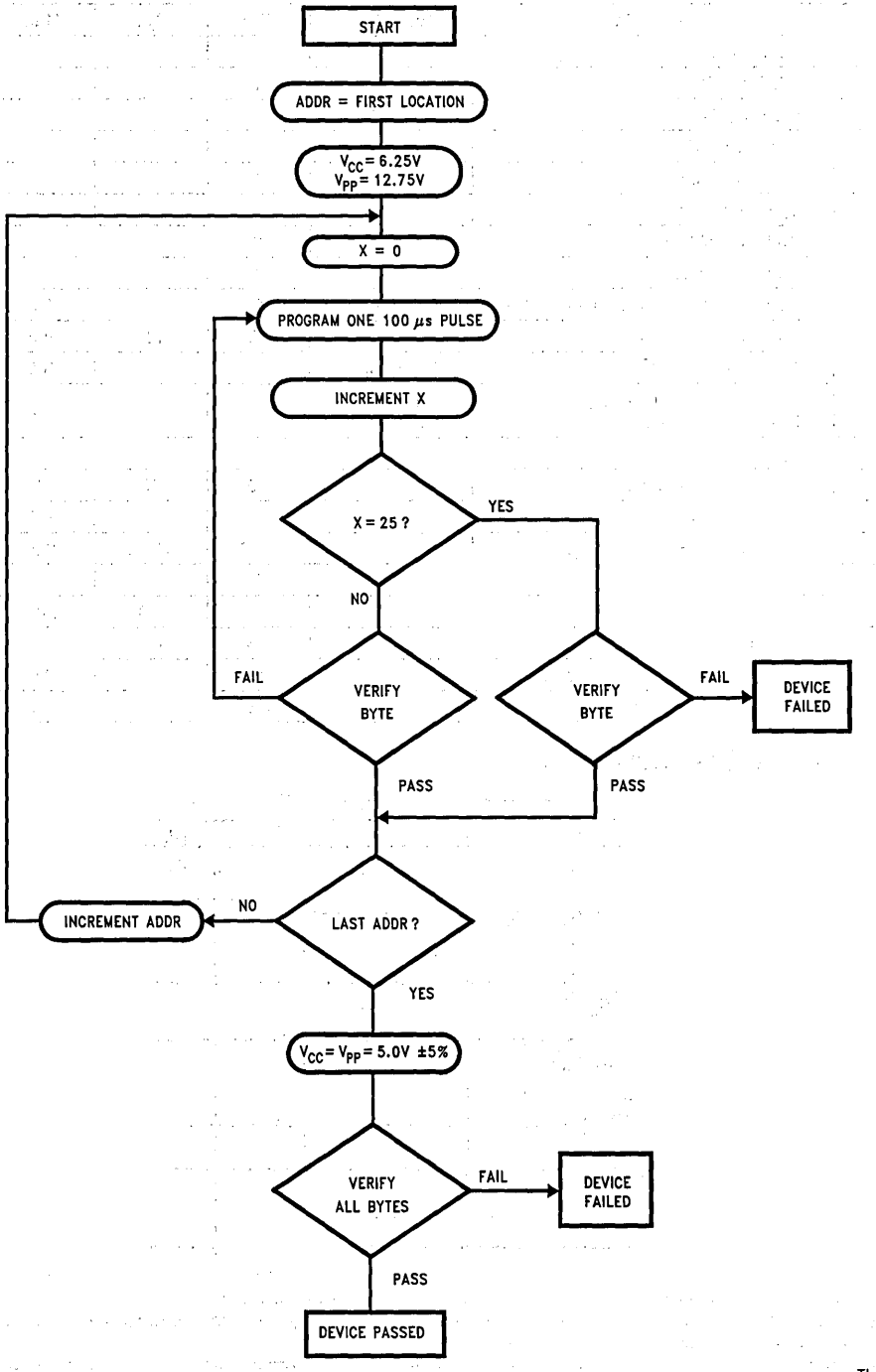
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/11376–6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 66 mW to 0.66 μW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Functional Description (Continued)

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27LV210 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V ±0.5V to address pin A_9. Addresses A_1-A_8, $A_{10}-A_{15}$, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0-O_7. Proper code access is only guaranteed at 25°C ± 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27LV210 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	3.3V	D_{OUT}
Output Disable	X	V_{IH}	X	X	3.3V	High Z
Standby	V_{IH}	X	X	X	3.3V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

National Semiconductor

NM93C06L/C46L/C56L/C66L 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.0V t0 5.5V)

General Description

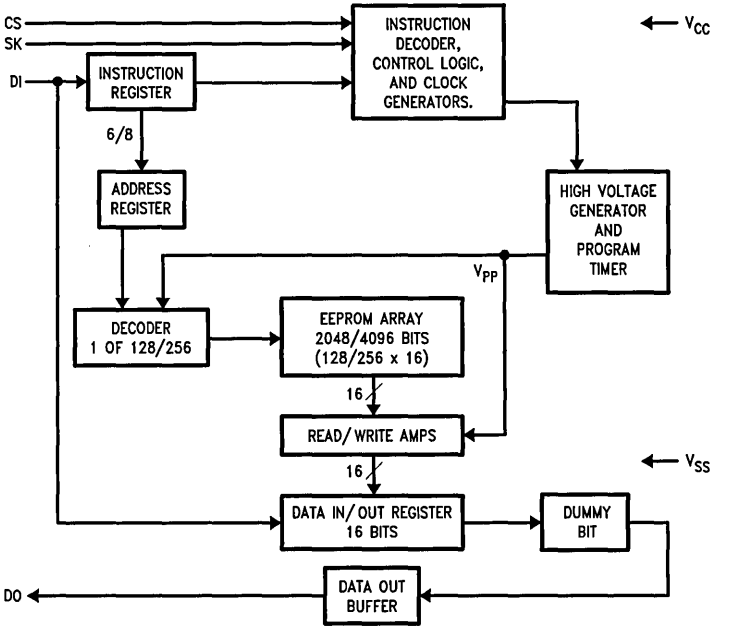
The NM93C06L/C46L/C56L/C66L devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CxxL Family functions in an extended voltage operating range, requires only a single power supply and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. These devices are available in an SO package for small space considerations.

The NM93CxxL Family interfaces to microprocessors and microcontrollers via a single 4-wire MICROWIRE™ bus which possesses the following parameters: SK (Serial Clock), CS (Chip Select), DI (Data Input) and DO (Data-Output). DI includes: instruction, address and data to be written. DO offers data read and programming status information. Serial interfacing allows 8-pin DIP or 8-pin SO packaging to minimize board space. The following seven instructions (op codes) control device operation: EWEN (Erase/Write Enable), EWDS (Erase/Write Disable), READ (Read), ERAL (Erase all registers), ERASE (Erase a register/address), WRAL (Write all registers with 16 bits of data) and WRITE (Write a register/address).

Features

- 2.0V to 5.5V operation in read mode
- 2.5V to 5.5V operation in all other modes
- Typical active current of 400 μA; Typical standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

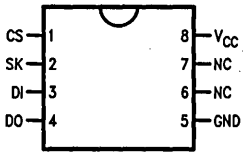
Block Diagram



TL/D/10045–1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/10045-2

Top View

See NS Package Number N08E or M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C06LN/NM93C46LN
NM93C56LN/NM93C66LN
NM93C06LM8/NM93C46LM8
NM93C56LM8/NM93C66LM8

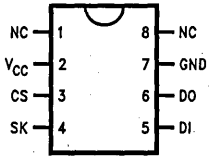
Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C06LEN/NM93C46LEN
NM93C56LEN/NM93C66LEN
NM93C06LEM8/NM93C46LEM8
NM93C56LEM8/NM93C66LEM8

Alternate (Turned) SO Pinout

Order Number
NM93C46TLM8/NM93C46TLEM8

Alternate SO Pinout (TM8)



TL/D/10045-12

See NS Package Number M08A

LOW VOLTAGE (<4.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06L–NM93C66L	0°C to +70°C
NM93C06LE–NM93C66LE	−40°C to +85°C
Power Supply (V_{CC}) Range	
Read Mode	2.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 250 kHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 250 kHz 4.5V ≤ V_{CC} ≤ 5.5V		3 3	mA
I_{CC3}	Standby Current	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V ≤ V_{CC} ≤ 5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		2V ≤ V_{CC} ≤ 4.5V	−0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		2V ≤ V_{CC} ≤ 4.5V I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		0 0	250 250	kHz
t_{SKH}	SK High Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2)	1 1		μs
t_{SKL}	SK Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2)	1 1		μs
t_{SKS}	SK Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 3)	1 1		μs
t_{CSS}	CS Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	0.2 0.2		μs
t_{DH}	DO Hold Time		Relative to SK	10		ns

LOW VOLTAGE (<4.5V) SPECIFICATIONS

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	0.4 0.4		μs
t_{CSH}	CS Hold Time		Relative to SK	0		μs
t_{DIH}	DI Hold Time		Relative to SK	0.4		μs
t_{PD1}	Output Delay to "1"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		2 2	μs
t_{PD0}	Output Delay to "0"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		2 2	μs
t_{SV}	CS to Status Valid	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		1 1	μs
t_{DF}	CS to DO in TRI-STATE®	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test CS = V_{IL}		0.4 0.4	μs
t_{WP}	Write Cycle Time				15	ms

Capacitance (Note 4)

T_A = 25°C f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load: 1 TTL Gate and C_L = 100 pF		
V_{CC} Range	**AC Test Conditions**	
4.5V < V_{CC} < 5.5V	Input Pulse Levels	0.8V and 2.0V
	Timing Measurement Level (V_{IL}/V_{IH})	0.9V and 1.9V
	Timing Measurement Level (V_{OL}/V_{OH})	0.8V and 2.0V
	(TTL Load Conditions: I_{OL} = 2.1 mA, I_{OH} = −0.4 mA)	
2.0V < V_{CC} < 4.5V	Input Pulse Levels	0.3V and 1.8V
	Timing Measurement Level (V_{IL}/V_{IH})	0.4V and 1.6V
	Timing Measurement Level (V_{OL}/V_{OH})	0.8V and 1.6V
	(CMOS Load Conditions: I_{OL} = 10 μA, I_{OH} = −10 μA)	

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The above SK frequency specifies a minimum SK clock period of 4 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. For example, if t_{SKL} = 1 μs, then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

STANDARD VOLTAGE (4.5V ≤ V_{CC} ≤ 5.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06L–NM93C66L	0°C to +70°C
NM93C06LE–NM93C66LE	−40°C to +85°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 1 MHz SK = 1 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 1 MHz SK = 1 MHz		3 3	mA
I_{CC3}	Standby Current	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	I_{OL} = 2.1 mA I_{OL} = 2.1 mA		0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage	NM93C06LE-NM93C66LE	I_{OL} = 10 μA		0.2	V
f_{SK}	SK Clock Frequency	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		0 0	1 1	MHz
t_{SKH}	SK High Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2) (Note 3)	250 300		ns
t_{SKL}	SK Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2) (Note 3)	250 250		ns
t_{CS}	Minimum CS Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 4) (Note 5)	250 250		ns
t_{CSS}	CS Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	50 50		ns
t_{DH}	DO Hold Time		Relative to SK	10		ns

STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		500 500	ns
t_{PD0}	Output Delay to "0"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		500 500	ns
t_{SV}	CS to Status Valid	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		500 500	ns
t_{DF}	CS to DO in TRI-STATE	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test CS = V_{IL}		100 100	ns
t_{WP}	Write Cycle Time				10	ms

Note: Throughout this table "M" refers to temperature range (−55°C to +125°C), not package.

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial and Extended temperature range parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93CxxL Family has seven instruction sets as described below. Note that each instruction set is broken down into the Start Bit (SB), Op code, Address (if applicable) and Data (if applicable). As shown in the timing diagrams and INSTRUCTION SET tables, address bits will have 6 bits for the NM93C06 and NM93C46 and 8 bits for the NM93C56 and NM93C66 devices. All instruction bits are entered into the device on the SK low-to-high transitions.

Programming is enabled by bringing CS to a Logical 0 state for the required t_{CS} period. After this t_{CS} period the self-timed operation may be monitored by bringing CS to a logical 1 and observing the DO status: Logical 1 = READY (Ready for the next instruction) and Logical 0 = BUSY (Programming in progress).

Erase/Write Enable (EWEN):

When V_{CC} is applied to the device, it powers up in the programming Erase/Write disabled state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once this instruction is executed, programming remains enabled until the Erase/Write Disable (EWDS) instruction is executed or until V_{CC} is removed from the part.

Erase/Write Disable (EWDS):

To protect against accidental data disturbance, the Erase/Write Disable instruction disables all programming modes and should follow the end of all programming cycles.

Read (READ):

The READ instruction outputs the specified address data on the DO pin. After the READ instruction is received, the instruction and address are decoded and data is transferred from the address to a 16-bit shift register output buffer. A dummy bit (logical 0) precedes all 16-bit data out strings. The READ instruction may be executed from either the enabled or disabled state.

Erase (ERASE):

This instruction, when followed by an address location, programs all bits in the selected register/address to a 1 state (Register erase).

Erase All (ERAL):

This instruction programs all registers/addresses in the memory array to a 1 state, (Bulk erase).

Write (WRITE):

This instruction, when followed by an address location and 16 bits of data, programs the selected register/address.

Write All (WRAL):

This instruction, when followed by 16 bits of data, programs all registers/addresses in the memory array with the specified data pattern, (Bulk write).

Instruction Set for the NM93C06L and NM93C46L

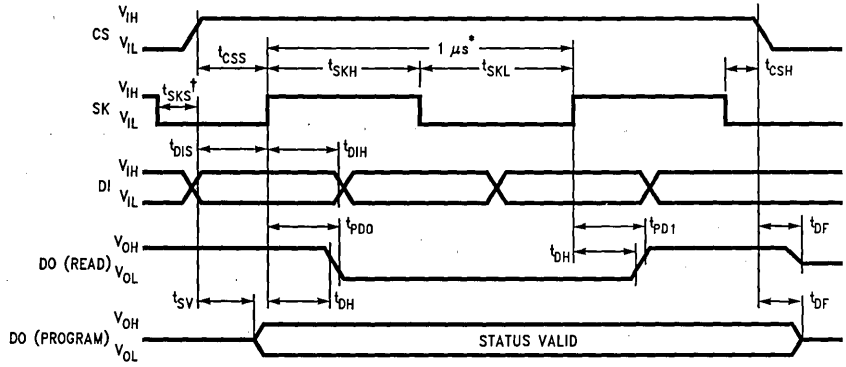
Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory at specified address.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erases all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

Instruction Set for the NM93C56L and NM93C66L

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory at specified address.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
ERASE	1	11	A7–A0		Erase register A7A6A5A4A3A2A1A0.
WRITE	1	01	A7–A0	D15–D0	Writes register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXXXX		Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing

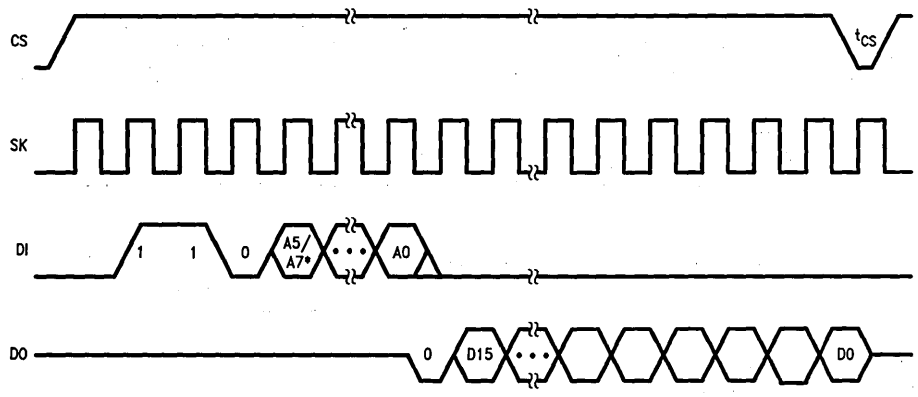


TL/D/10045–13

*This is the minimum SK period (Note 2).

†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ:

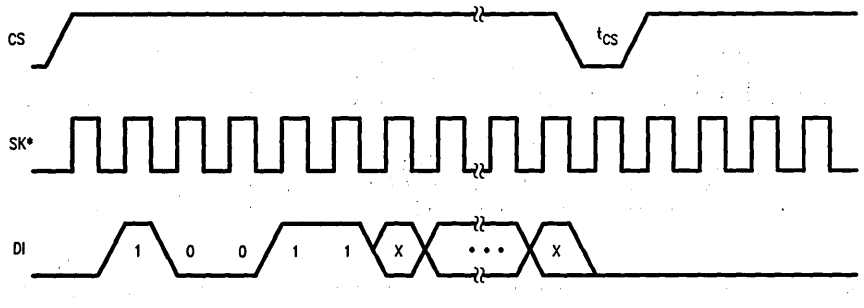


TL/D/10045–5

*Address bits A_5 and A_4 become "don't care" for NM93C06L.

*Address bit A_7 becomes a "don't care" for NM93C56L.

EWEN:

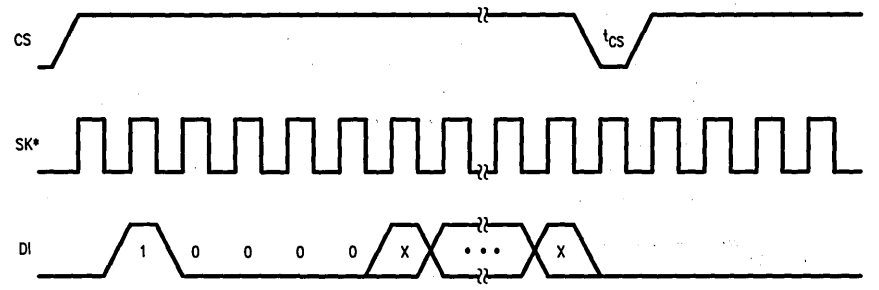


TL/D/10045–6

*The NM93C56L and NM93C66L require a minimum of 11 clock cycles. The NM93C06L and NM93C46L require a minimum of 9 clock cycles.

Timing Diagrams (Continued)

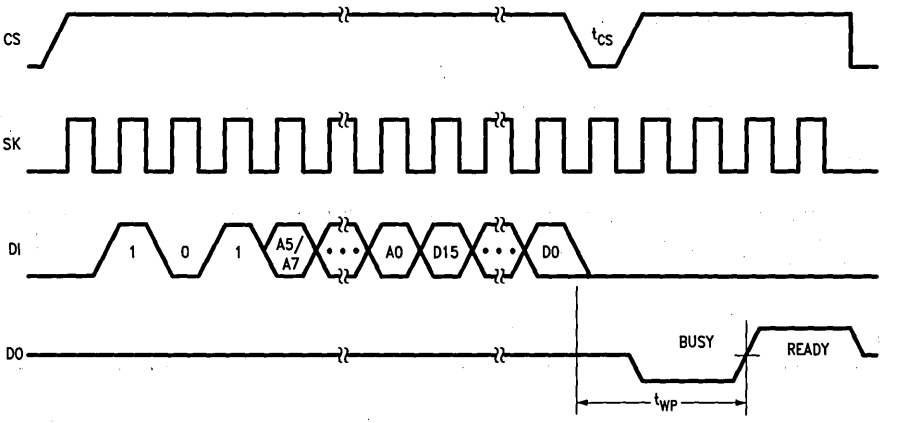
EWDS:



TL/D/10045–7

*The NM93C56L and NM93C66L require a minimum of 11 clock cycles. The NM93C06L and NM93C46L require a minimum of 9 clock cycles.

WRITE:

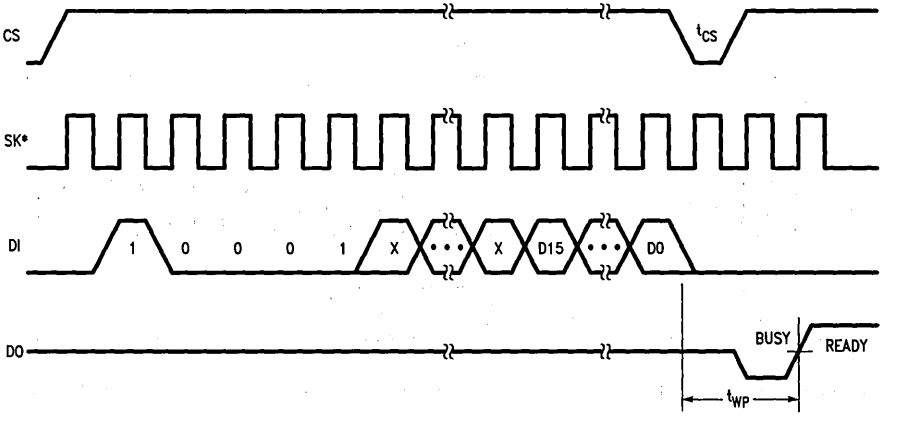


TL/D/10045–8

*Address bit A_5 and A_4 become "don't care" for NM93C06L.

*Address bit A_7 becomes a "don't care" for NM93C56L.

WRAL:

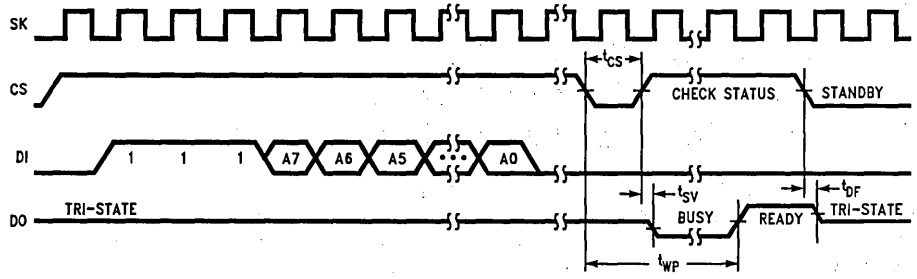


TL/D/10045–9

*The NM93C56L and NM93C66L require a minimum of 11 clock cycles. The NM93C06L and NM93C46L require a minimum of 9 clock cycles.

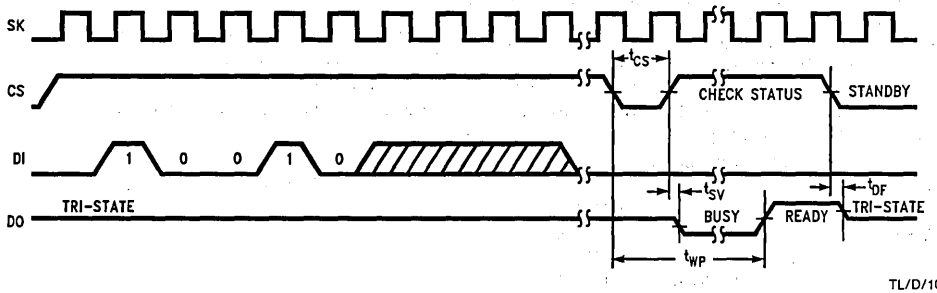
Timing Diagrams (Continued)

ERASE:



TL/D/10045–10

ERAL:



TL/D/10045–11

5

National Semiconductor

NM93CS06L/CS46L/CS56L/CS66L 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.0V to 5.5V) and Data Protect

General Description

The NM93CS06L/CS46L/CS56L/CS66L devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CSxxL Family functions in an extended voltage operating range and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. N registers ($N \leq 16$, $N \leq 64$, $N \leq 128$, $N \leq 256$) can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification. Additionally, this address can be "locked" into the device, making all future attempts to change data impossible.

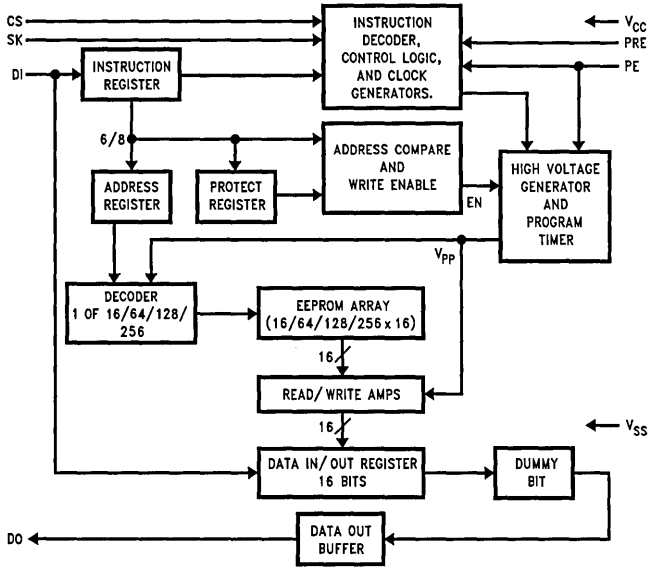
These devices are available in an SO package for small space considerations.

The serial interface that control these EEPROMs is MICROWIRE™ compatible, providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PREN, PRCLEAR, and PRDS.

Features

- Sequential register read
- Write protection in a user defined section of memory
- 2.0V to 5.5V operating range in read mode
- 2.5V to 5.5V operating range in other modes
- Typical active current of 400 μA; typical standby current of 25 μA
- Direct Write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: 10^6 data changes
- Packages Available: 8-pin SO, 8-pin DIP

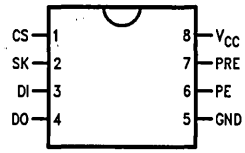
Block Diagram



TL/D/10044–1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO Package (M8)



TL/D/10044-2

Top View

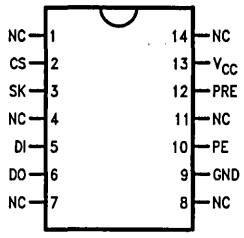
See NS Package Number N08E (N)
See NS Package Number M08A (M8)

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:

SO Package (M)



TL/D/10044-3

Top View

See NS Package Number M14A (M)

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93CS06LN/NM93CS46LN/NM93CS56LN/NM93CS66LN NM93CS06LM8/NM93CS46LM8/NM93CS56LM8/NM93CS66LM*

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93CS06LEN/NM93CS46LEN/NM93CS56LEN/NM93CS66LEN NM93CS06LEM8/NM93CS46LEM8/NM93CS56LEM8/NM93CS66LEM*

*The NM93CS66 is available in 8-pin DIP and 14-pin SO only.

Note: 14-pin SO availability on the 93CS06, CS46 and CS56, contact your local National Semiconductor Sales Office.

LOW VOLTAGE (<4.5) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CSxxL	0°C to +70°C
NM93CSxxLE	−40°C to +85°C
Power Supply (V_{CC}) Range	
Read Mode	2.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
V_{RPP}	Power Supply Ripple		Peak-to-Peak (Note 5)		0.1 V_{CC}	V
I_{CC1}	Operating Current CMOS Input Levels	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	CS = V_{IH}, SK = 250 kHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93CS06L–NM93CS66L NM93CS06LE–NM93CSS66LE	CS = V_{IH}, SK = 250 kHz 4.5V≤V_{CC}≤5.5V		3 3	mA
I_{CC3}	Standby Current	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93CS06L–NM93CS66L NM93CS06LE–NM93CSS66LE	V_{OUT} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V≤V_{CC}≤5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		2V≤V_{CC}≤4.5V	−0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		4.5V≤V_{CC}≤5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		2V≤V_{CC}≤4.5V I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}	0.1 V_{CC}	V
f_{SK}	SK Clock Frequency	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE		0 0	250 250	kHz
t_{SKH}	SK High Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	(Note 2)	1 1		μs
t_{SKL}	SK Low Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	(Note 2)	1 1		μs
t_{SKS}	SK Setup Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	(Note 3)	1 1		μs
t_{CSS}	CS Setup Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to SK	0.2 0.2		μs
t_{PRES}	PRE Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	0.2 0.2		μs

LOW VOLTAGE (<4.5) SPECIFICATIONS (Continued)

DC and AC Electrical Characteristics (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to SK	0.2 0.2		μs
t_{DIS}	DI Setup Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to SK	0.4 0.4		μs
t_{DH}	DO Hold Time		Relative to SK	10		ns
t_{CSH}	CS Hold Time		Relative to SK	0		μs
t_{PEH}	PE Hold Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to CS Relative to CS	0.4 0.4		μs
t_{PREH}	PRE Hold Time		Relative to SK	0		μs
t_{DIH}	DI Hold Time		Relative to SK	0.4		μs
t_{PD1}	Output Delay to "1"	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	AC Test		2 2	μs
t_{PD0}	Output Delay to "0"	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	AC Test		2 2	μs
t_{SV}	CS to Status Valid	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	AC Test		1 1	μs
t_{DF}	CS to DO in TRI-STATE®	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	$CS = V_{IL}$ AC Test		0.4 0.4	μs
t_{WP}	Write Cycle Time				15	ms

Capacitance (Note 4)

T_A = 25°C, f = 1MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load: 1 TTL Gate and C_L = 100 pF

V_{CC} Range	AC Test Conditions	
4.5V < V_{CC} < 5.5V	Input Pulse Levels	0.8V and 2.0V
	Timing Measurement Level (V_{IL}/V_{IN}):	0.9V and 1.9V
	Timing Measurement Level (V_{OL}/V_{OH}):	0.8V and 2.0V
	(TTL Load Conditions: I_{OL} = 2.1 mA; I_{OH} = −0.4 mA)	
2.0V < V_{CC} < 4.5V	Input Pulse Levels:	0.3V and 1.8V
	Timing Measurement Level (V_{IL}/V_{IH}):	0.4V and 1.6V
	Timing Measurement Level (V_{OL}/V_{OH}):	0.8V and 1.6V
	(CMOS Load Conditions: I_{OL} = 10 μA; I_{OH} = − 10 μA)	

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The above SK frequency specifies a minimum SK clock period of 4 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. For example, if t_{SKL} = 1 μs, then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Note 5: Rate of voltage change must be less than 0.5 V/ms.

STANDARD VOLTAGE ($4.5 \leq V \leq 5.5$) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 second)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CSxxL	0°C to +70°C
NM93CSxxLE	−40°C to +85°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Throughout this table "M" refers to temperature range (−55°C to +125°C) not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	CS = V_{IH}, SK = 1.0 MHz SK = 1.0 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	CS = V_{IH}, SK = 1.0 MHz SK = 1.0 MHz		3 3	mA
I_{CC3}	Standby Current	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	V_{OUT} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC}+1	V
V_{OL1}	Output Low Voltage	NM93CS06LE-NM93CS66LE NM93CS06LE-NM93CS66LE	I_{OL} = 2.1 mA I_{OL} = 2.1 mA		0.4 0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OL} = −10 μA	 V_{CC}−0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE		0 0	1 1	MHz
t_{SKH}	SK High Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	(Note 2) (Note 2)	250 300		ns
t_{SKL}	SK Low Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	(Note 2) (Note 2)	250 250		ns
t_{CS}	Minimum CS Low Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	(Note 4) (Note 4)	250 250		ns
t_{CSS}	CS Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	50 50		ns
t_{PRES}	PRE Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	50 50		ns
t_{DH}	DO Hold Time		Relative to SK	10		ns

STANDARD VOLTAGE ($4.5 \leq V \leq 5.5$) SPECIFICATIONS (Continued)

DC and AC Electrical Characteristics

V_{CC} = 4.5V to 5.5V unless otherwise specified

Throughout this table "M" refers to temperature range (−55°C to +125°C) not package. (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	50 50		ns
t_{DIS}	DI Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	100 100		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to CS Relative to CS	250 250		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	AC Test		500 500	ns
t_{PD0}	Output Delay to "0"	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	AC Test		500 500	ns
t_{SV}	CS to Status Valid	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	AC Test		500 500	ns
t_{DF}	CS to DO in TRI-STATE®	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	AC Test CS = V_{IL}		100 100	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

T_A = 25°C f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended parts specifies a minimum SK clock period of 1 microsecond; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 microseconds; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial and Extended parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The extended voltage EEPROMs of the NM93CSxxL Family have 10 instructions as described below. Note that there is a difference in the length of the instruction for the NM93CS06L and NM93CS46L vs. the NM93CS56L and NM93CS66L since the two larger devices require 2 additional address bits which are not required for the smaller devices. Within the two groups of devices the number of address bits remain constant even though in some cases the most significant bit(s) are not used. In every instruction, the first bit is always a "1" and is viewed as a start bit. The next 8 or 10 bits, depending on device size, carry the op code and address. The address is either 6 or 8 bits, depending on the device size.

Read and Sequential Register Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **Sequential Read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is allocated to the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and that the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and therefore enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction; however, after loading the PRCLEAR instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction. The Protect Register will be read as 0s after it is cleared.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register which is the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction, the Protect Register must first be cleared by executing a PRCLEAR operation and the PRE and PE pins **must** be held high while loading the instruction; however, after loading the PRWRITE instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Instruction Set for the NM93CS06L and NM93CS46L

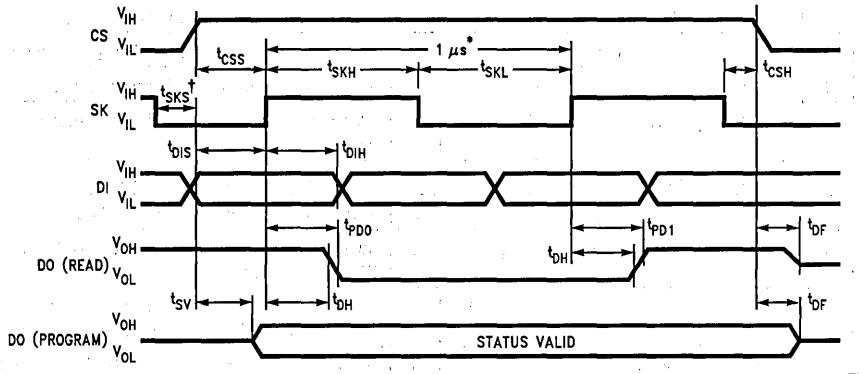
Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE. Cleared state is read as 0's.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Instruction Set for the NM93CS56L and NM93CS66L

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE. Cleared state is read as 0's.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Timing Diagrams

Synchronous Data Timing



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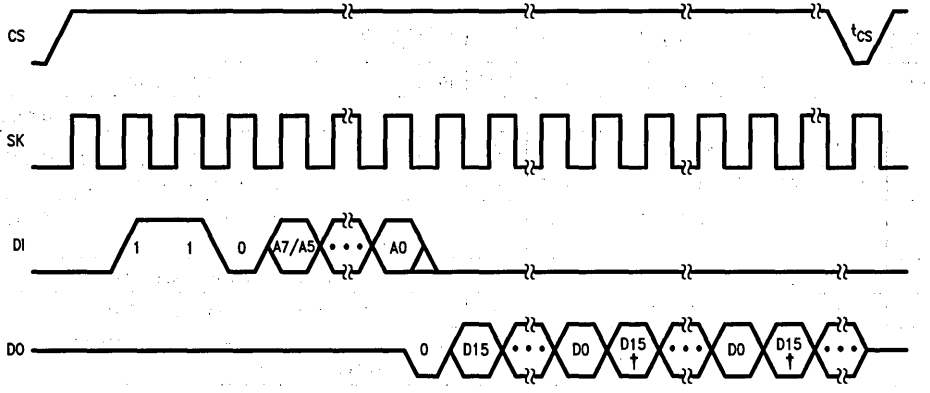
*This is the minimum SK period (Note 2).
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ:
PRE = 0, PE = X

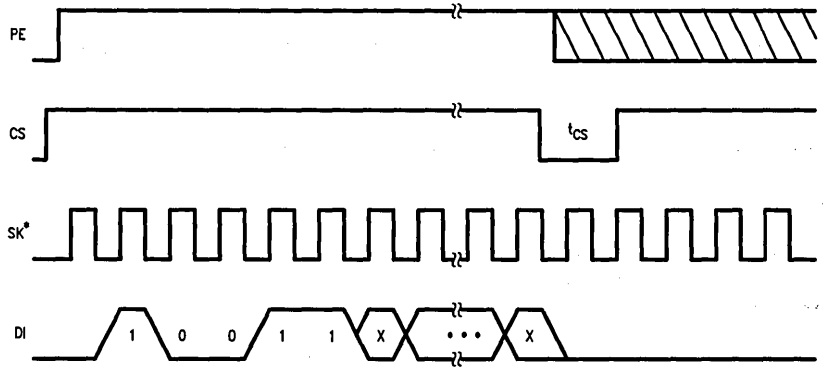


TL/D/10044–5

*Address bit A7 becomes "don't care" for NM93CS56L.
*Address bits A5 and A4 become "don't cares" for NM93CS06L.
†The memory automatically cycles to the next register.

Timing Diagrams (Continued)

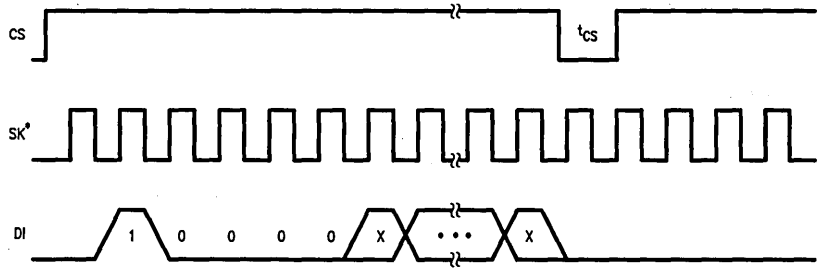
WEN:
PRE = 0, DO = TRI-STATE



TL/D/10044–6

*The NM93CS56L and NM93CS66L require a minimum of 11 clock cycles. The NM93CS06L and NM93CS46L require a minimum of 9 clock cycles.

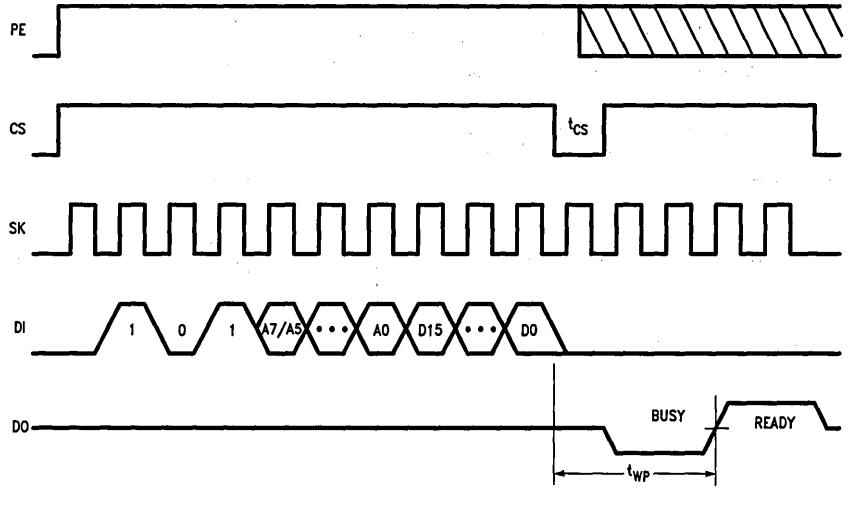
WDS:
PRE = 0, PE = X, DO = TRI-STATE



TL/D/10044–7

*The NM93CS56L and NM93CS66L require a minimum of 11 clock cycles. The NM93CS06L and NM93CS46L require a minimum of 9 clock cycles.

WRITE:
PRE = 0

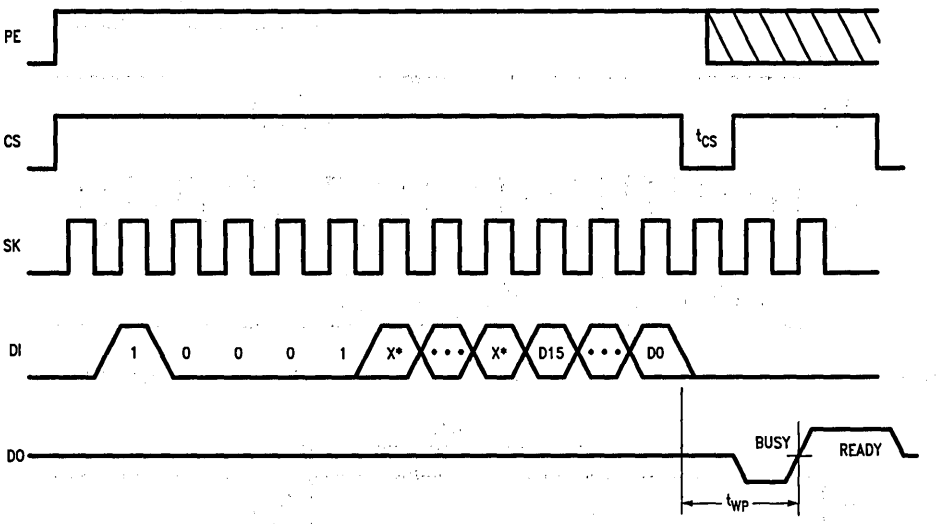


TL/D/10044–8

- Address bit A7 becomes a "don't care" for NM93CS56L.
- Address bits A5 and A4 become "don't cares" for NM93CS06L.

Timing Diagrams (Continued)

WRALL:
PRE = 0

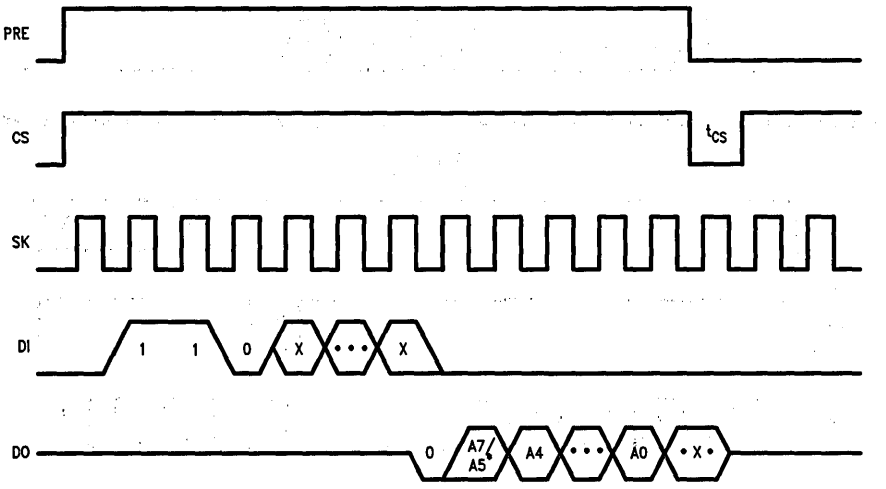


*Don't care

†Protect Register **MUST** be cleared.

TL/D/10044–9

PRREAD:
PE = X

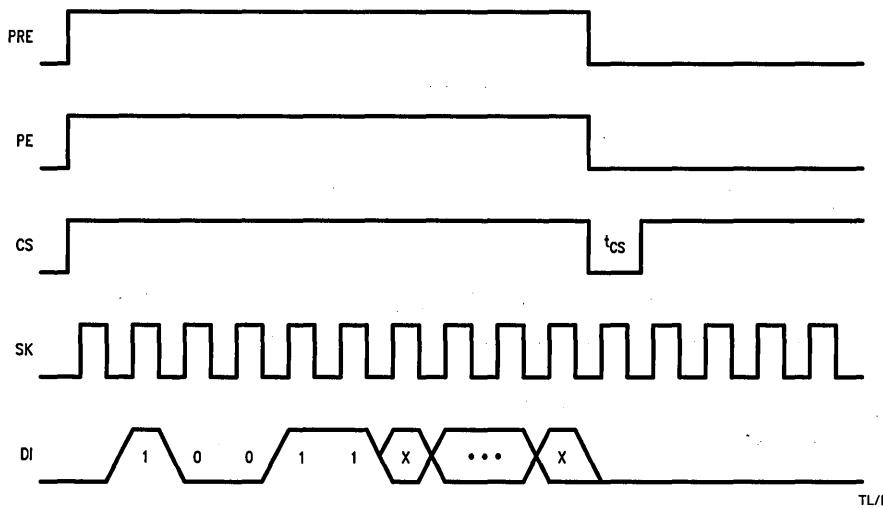


TL/D/10044–10

•Address bits A5 and A4 become "don't cares" for NM93CS06L.
•Address bit A7 becomes "don't care" for NM93CS56L.

Timing Diagrams (Continued)

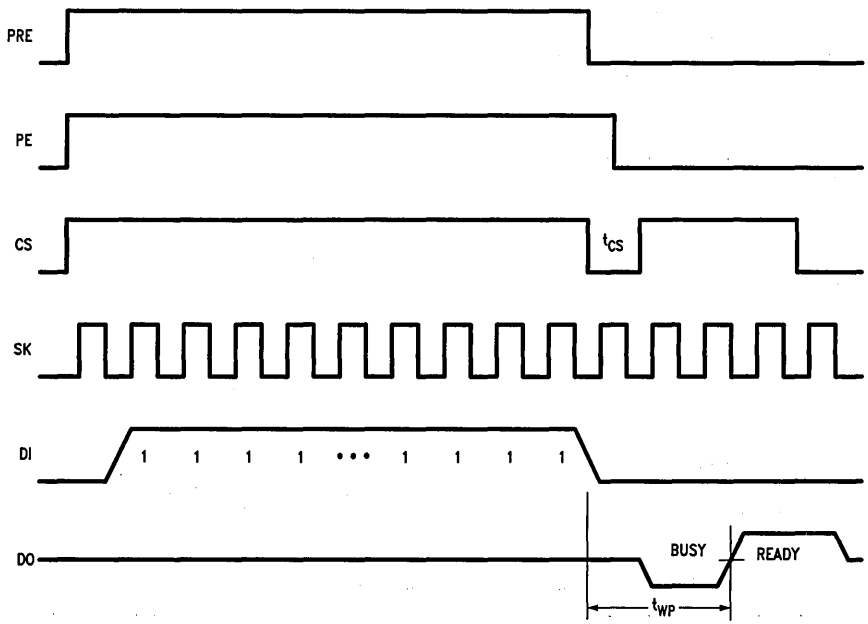
PREN*:
DO = TRI-STATE



TL/D/10044–11

*A WEN cycle must precede a PREN cycle.

PRCLEAR*:



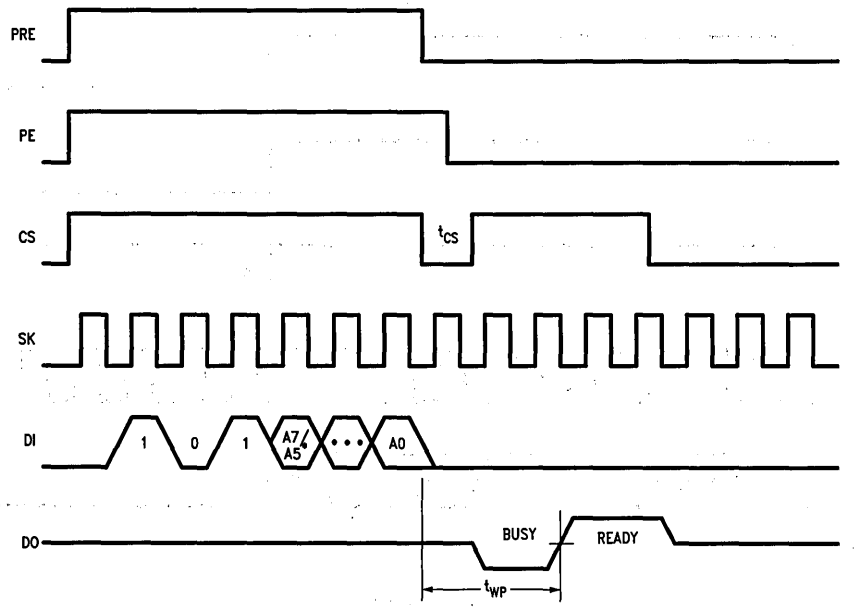
*A PREN cycle must **immediately** precede a PRCLEAR cycle.

TL/D/10044–12

5

Timing Diagrams (Continued)

PRWRITE†:

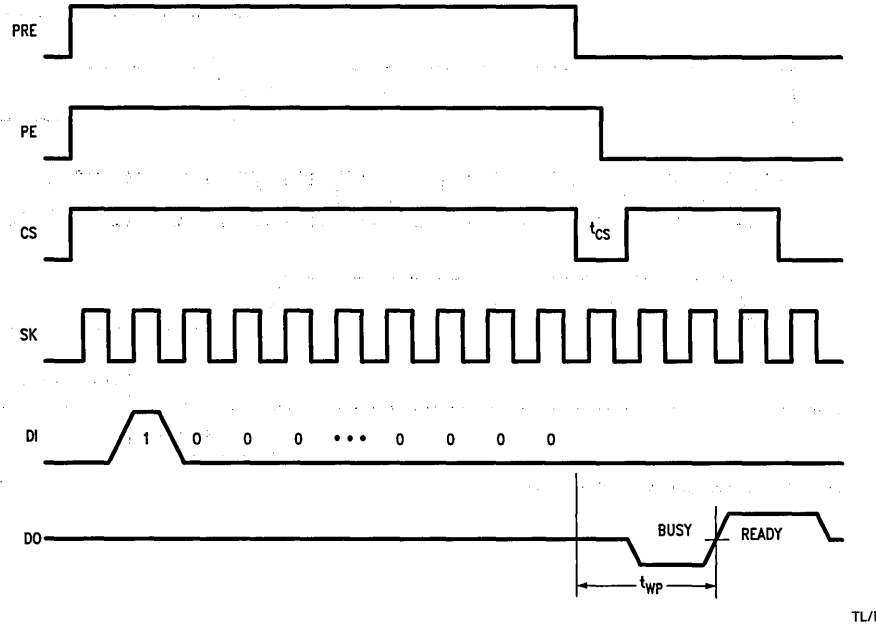


TL/D/10044–13

*Address bit A7 becomes a "don't care" for NM93CS56L.
*Address bits A5 and A4 become "don't cares" for NM93CS06L.

†Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS*:



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***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

National Semiconductor

NM93C46AL
1024-Bit Serial EEPROM
64 x 16-Bit or 128 x 8-Bit Configurable

General Description

The NM93C46AL is 1024 bits of CMOS non-volatile electrically erasable memory organized as either 64 16-bit registers or 128 8-bit registers. The organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, low power consumption and a wide operating voltage range.

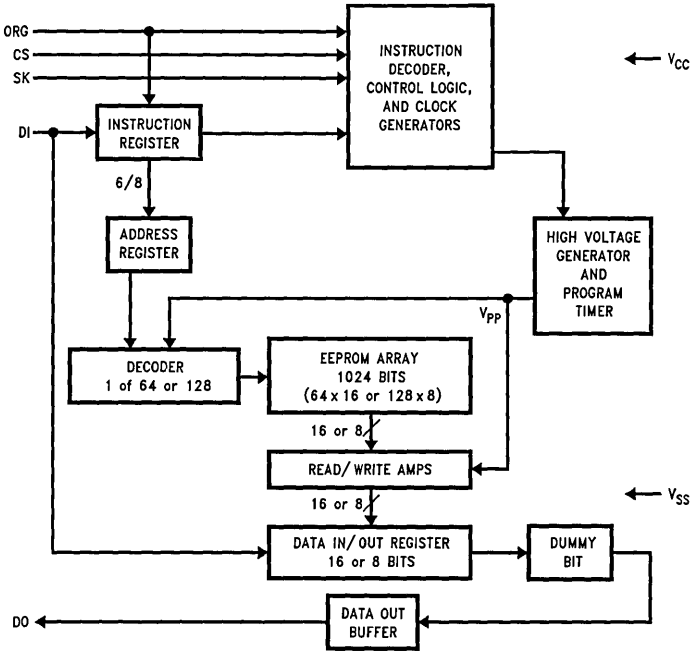
The interface is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C46AL: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C46AL is compatible with National Semiconductor's NM93C46L if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC} to default to the 64 x 16 configuration.

Features

- 2.0V to 5.5V operation in read mode
- 2.5V to 5.5V operation in all other modes
- Typical active current of 400 μA; typical standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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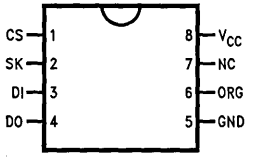
Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



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Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Organization

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46ALN
NM93C46ALM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C46ALEN
NM93C46ALEM8

LOW VOLTAGE (<4.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46AL	0°C to +70°C
NM93C46ALE	−40°C to +85°C
Power Supply Range	
Read Mode	2.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 250 kHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 250 kHz 4.5V ≤ V_{CC} ≤ 5.5V		3 3	mA
I_{CC3}	Standby Current	NM93C46AL NM93C46ALE	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
	Pin 6			−10	10	
I_{OL}	Output Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V ≤ V_{CC} ≤ 5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		2V ≤ V_{CC} ≤ 4.5V	−0.1 0.8 V_{CC}	0.2 V_{CC} V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	NM93C46AL NM93C46ALE	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2}	Output Low Voltage		2V ≤ V_{CC} ≤ 4.5V I_{OL} = 10 μA		0.1 V_{CC}	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	0.9 V_{CC}		V
f_{SK}	SK Clock Frequency	NM93C46AL NM93C46ALE		0 0	250 250	kHz
t_{SKH}	SK High Time	NM93C46AL NM93C46ALE	(Note 2)	1 1		μs
t_{SKL}	SK Low Time	NM93C46AL NM93C46ALE	(Note 2)	1 1		μs
t_{CS}	Minimum CS Low Time	NM93C46AL NM93C46ALE	(Note 3)	1 1		μs

LOW VOLTAGE (<4.5V) SPECIFICATIONS

DC and AC Electrical Characteristics (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C46AL NM93C46ALE	Relative to SK	0.2 0.2		μs
t_{DIS}	DI Setup Time	NM93C46AL NM93C46ALE	Relative to SK	0.4 0.4		μs
t_{CSH}	CS Hold Time		Relative to SK	0		μs
t_{DIH}	DI Hold Time		Relative to SK	0.4		μs
t_{PD1}	Output Delay to "1"	NM93C46AL NM93C46ALE	AC Test		2 2	μs
t_{PD0}	Output Delay to "0"	NM93C46AL NM93C46ALE	AC Test		2 2	μs
t_{SV}	CS to Status Valid	NM93C46AL NM93C46ALE	AC Test		1 1	μs
t_{DF}	CS to DO in TRI-STATE®	NM93C46AL NM93C46ALE	AC Test CS = V_{IL}		0.4 0.4	μs
t_{WP}	Write Cycle Time				15	ms
t_{DH}	DO Hold Time		Relative to SK	10		ns

Capacitance (Note 4)

T_A = +25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

AC Test Conditions (>4.5V)

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 4 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. For example, if t_{SKL} = 1 μs, then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: For Commercial parts, CS must be brought low for a minimum of 1 μs between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

STANDARD VOLTAGE ($4.5 \leq V \leq 5.5$)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46AL	0°C to +70°C
NM93C46ALE	−40°C to +85°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 1 MHZ SK = 0.5 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz		3 3	mA
I_{CC3}	Standby Current	NM93C46AL NM93C46ALE	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC}+1	V
V_{OL1}	Output Low Voltage	NM93C46AL NM93C46ALE	I_{OL} = 2.1 mA I_{OL} = 2.1 mA		0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NM93C46AL NM93C46ALE		0 0	1 0.5	MHz
t_{SKH}	SK High Time	NM93C46AL NM93C46ALE	(Note 2) (Note 3)	250 500		ns
t_{SKL}	SK Low Time	NM93C46AL NM93C46ALE	(Note 2) (Note 3)	250 500		ns
t_{CS}	Minimum CS Low Time	NM93C46AL NM93C46ALE	(Note 4) (Note 5)	250 500		ns

STANDARD VOLTAGE ($4.5 \leq V \leq 5.5$) (Continued)

DC and AC Electrical Characteristics (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C46AL NM93C46ALE	Relative to SK	50 100		ns
t_{DIS}	DI Setup Time	NM93C46AL NM93C46ALE	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NM93C46AL NM93C46ALE	Relative to SK	100 200		ns
t_{PD1}	Output Delay to "1"	NM93C46AL NM93C46ALE	AC Test		500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C46AL NM93C46ALE	AC Test		500 1000	ns
t_{SV}	CS to Status Valid	NM93C46AL NM93C46ALE	AC Test		500 1000	ns
t_{DF}	CS to DO in TRI-STATE	NM93C46AL NM93C46ALE	AC Test CS = V_{IL}		100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

T_A = +25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

AC Test Conditions (>4.5V)

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C46AL has seven instruction sets as described below. Note that each instruction set is broken down into the Start Bit (SB), Op code, Address (if applicable) and Data (if applicable). As shown in the timing diagrams and INSTRUCTION SET tables, address bits will have 6/7 bits and 8/16 bits for the data. All instruction bits are entered into the device on the SK low-to-high transitions.

Programming is enabled by bringing CS to a Logical 0 state for the required t_{CS} period. After this t_{CS} period the self-timed operation may be monitored by bringing CS to a logical 1 and observing the DO status: Logical 1 = READY (Ready for the next instruction) and Logical 0 = BUSY (Programming in progress).

Erase/Write Enable (EWEN):

When V_{CC} is applied to the device, it powers up in the programming Erase/Write disabled state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once this instruction is executed, programming remains enabled until the Erase/Write Disable (EWDS) instruction is executed or until V_{CC} is removed from the part.

Erase/Write Disable (EWDS):

To protect against accidental data disturbance, the Erase/Write Disable instruction disables all programming modes and should follow the end of all programming cycles.

Read (READ):

The Read instruction outputs the specified address data on the DO pin. After the READ instruction is received, the instruction and address are decoded and data is transferred from the address to an 8-/16-bit shift register output buffer. A dummy bit (logical 0) precedes all 8-/16-bit data out strings. The READ instruction may be executed from either the enabled or disabled state.

Erase (ERASE):

This instruction, when followed by an address location, programs all bits in the selected register/address to a 1 state (Register erase).

Erase All (ERAL):

This instruction programs all registers/addresses in the memory array to a 1 state (Bulk erase).

Write (WRITE):

This instruction, when followed by an address location and 8/16 bits of data, programs the selected register/address.

Write All (WRAL):

This instruction, when followed by 8/16 bits of data, programs all registers/addresses in the memory array with the specified data pattern (Bulk write).

Note: The NM93C46AL device does not require an 'ERASE' or 'ERASE ALL' prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with the NMOS NMC9346.

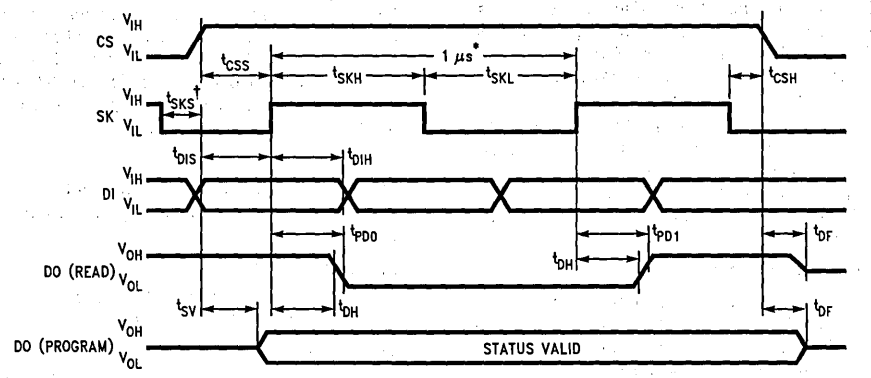
Instruction Set

Instruction	Start Bit	Opcode		Address*		Data		Comments
				128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1	0	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	1	1	A6–A0	A5–A0			Erase Address AN–A0
WRITE	1	0	1	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0	0	11XXXXX	11XXXX			Program Enable
EWDS	1	0	0	00XXXXX	00XXXX			Program Disable
ERAL	1	0	0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0	0	01XXXXX	01XXXX	D7–D0	D15–D0	Program All Addresses

*It is necessary to clock in the "Don't Care" Address Bits.

Timing Diagrams

Synchronous Data Timing



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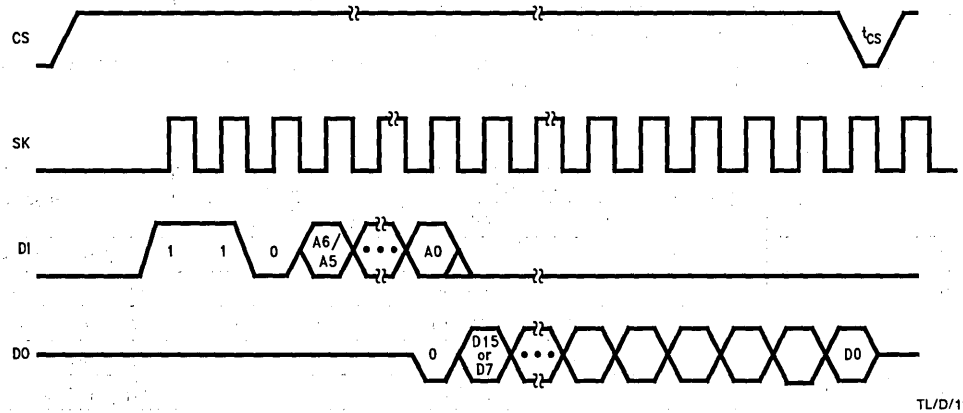
*This is the minimum SK period (Note 2).
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ



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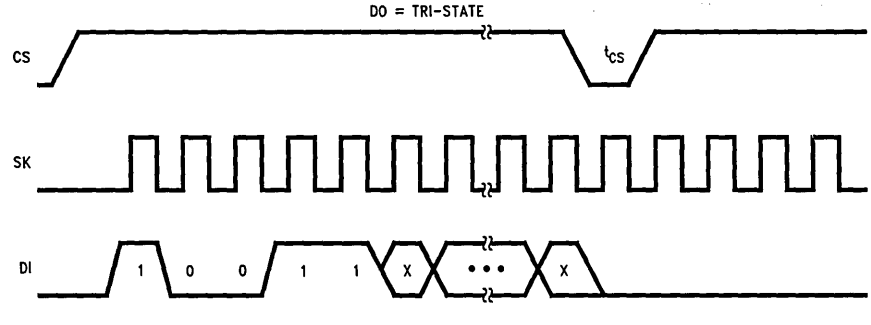
EWEN†



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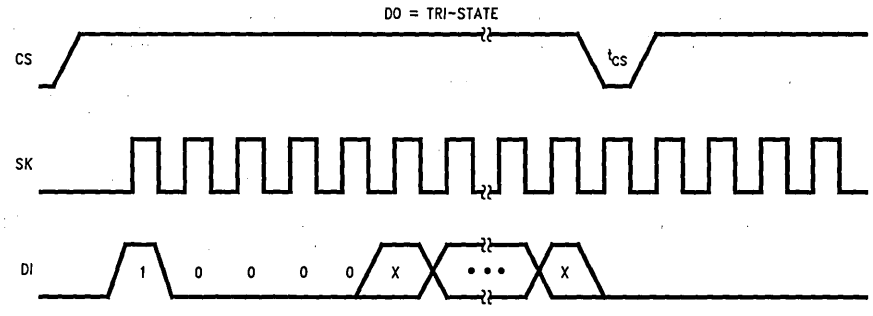
†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

Timing Diagrams (Continued)

EWDS†



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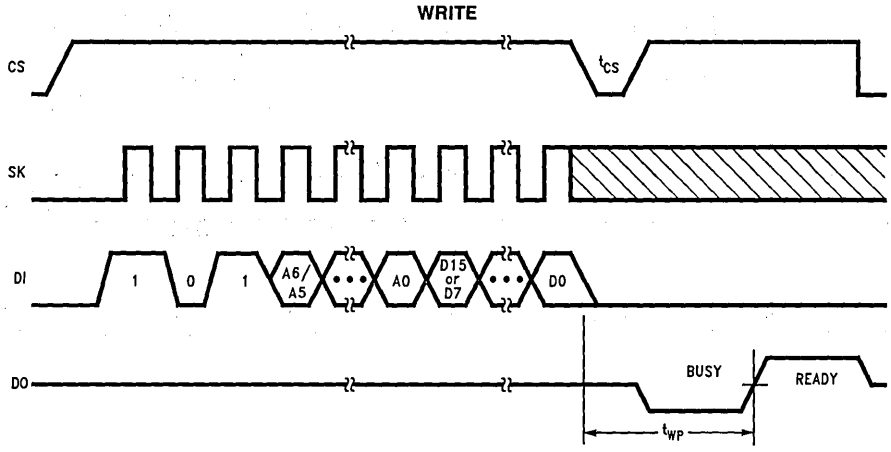
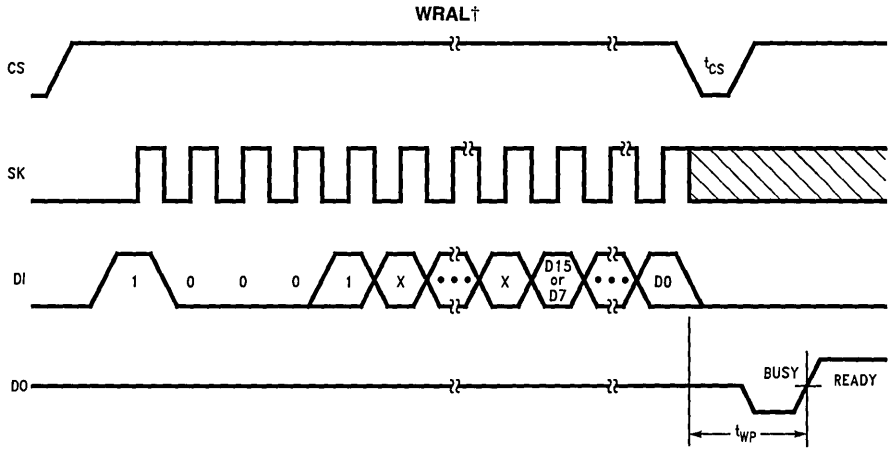
WRITE



TL/D/11330–7

WRAL†

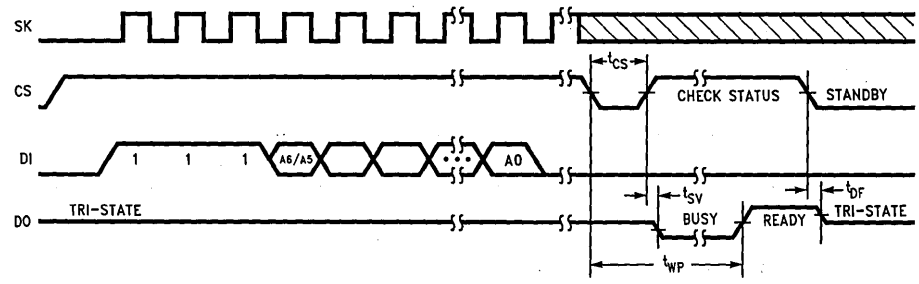


TL/D/11330–8

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

Timing Diagrams (Continued)

ERASE



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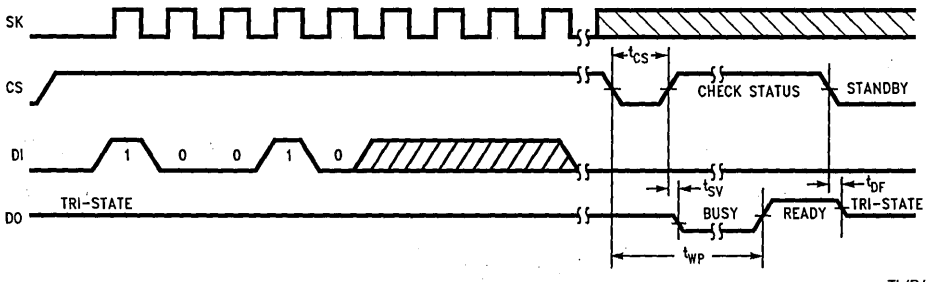
ERAL†



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†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

National Semiconductor

NM24C02L/C04L
2K-/4K-Bit Serial EEPROM with Extended Voltage (I²C Synchronous 2-Wire Bus)

General Description

The NM24C02L/04L devices are 2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I²C 2-wire protocol and are designed to minimize device pin count and simplify PC board layout requirements. National EEPROMs are designed and tested for applications requiring high reliability, high endurance and low power consumption.

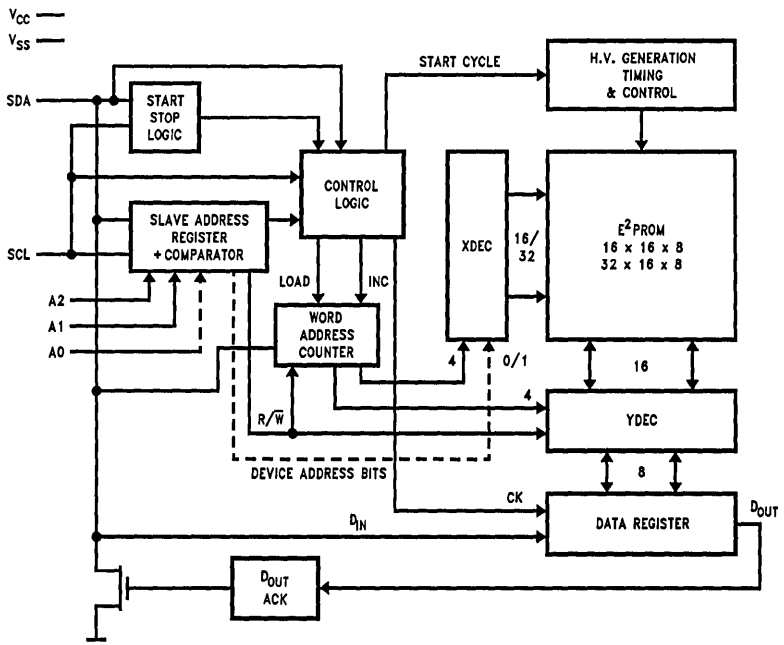
These devices have an operating voltage range of 2.5V to 5.5V and are offered in an 8-pin small outline (SO) package, making these devices perfectly suited for low power applications that require minimal board space usage.

This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

Features

- Extended operating voltage, 2.5V–5.5V
- Low Power CMOS
  - — 2 mA active current typical
  - — 60 μA standby current typical
- 2-wire I²C serial interface
  - — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP or 8 pin SO package

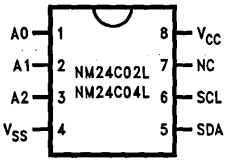
Functional Diagram



TL/D/11272–1

Connection Diagrams

Dual-In-Line Package (N) and SO Package (M8)



TL/D/11272–2

Top View

See NS Package Number M08A (M8) and N08E (N)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Connection
V_{CC}	+5V

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C02LN/NM24C04LN
NM24C02LM/NM24C04LM

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C02LEN/NM24C04LEN
NM24C02LEM/NM24C04LEM

LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM2402L/C04L	0°C to +70°C
NM24C02EL/04EL	−40°C to +85°C
Positive Power Supply (V_{CC})	2.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.5V to 4.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 200 μA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL, WP)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

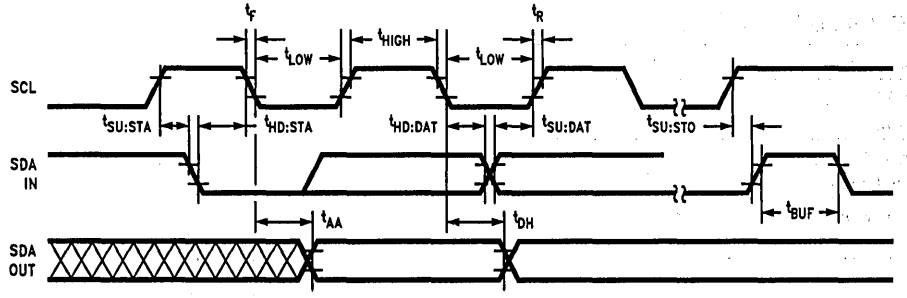
LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.5		μs
t_{LOW}	Clock Low Period	6.7		μs
t_{HIGH}	Clock High Period	4.5		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	500		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24C02L/C04L	0°C to +70°C
NM24C02EL/C04EL	−40°C to +85°C
Positive Power Supply (V_{CC})	2.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

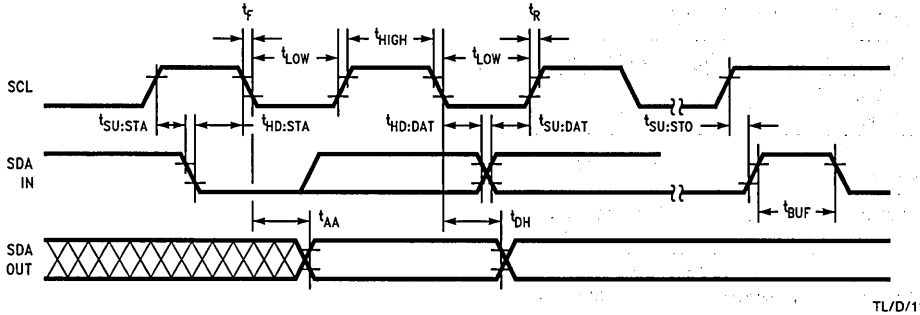
STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMs on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

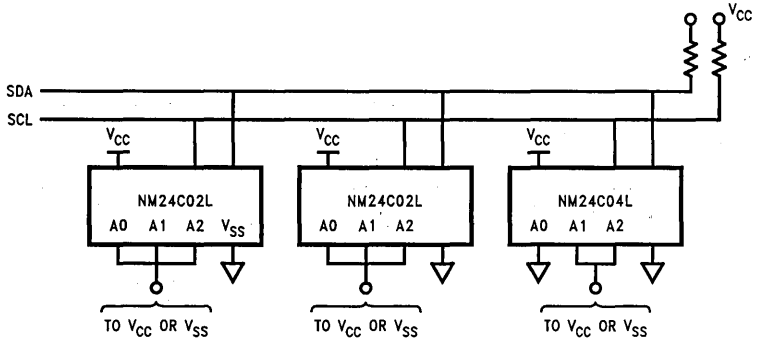
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (Tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any I²C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 8K (½ of Maximum Size) of Memory on 2-Wire Bus



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Note 1: The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.

Note 2: The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.

Note 3: It is recommended that the total line capacitance be less than 400 pF.

Note 4: Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C02L	DA	DA	DA	2048 Bits	1
NM24C04L	V_{SS}	DA	DA	4096 Bits	2

DA: Device Address

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Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24Cxx device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C02	ADR	ADR	ADR	$2^3 = 8$ (8) × (2K) = 16K
NM24C04	X	ADR	ADR	$2^2 = 4$ (4) × (4K) = 16K
NM24C08	X	X	ADR	$2^1 = 2$ (2) × (8K) = 16K
NM24C16	X	X	X	$2^0 = 1$ (1) × (16K) = 16K

ADR: Denotes an active pin used for device addressing

X: Not used for addressing (must be tied to Ground/V_{SS})

Device Operation

The NM24C02L/C04L supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the NM24C02L/C04L will be considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

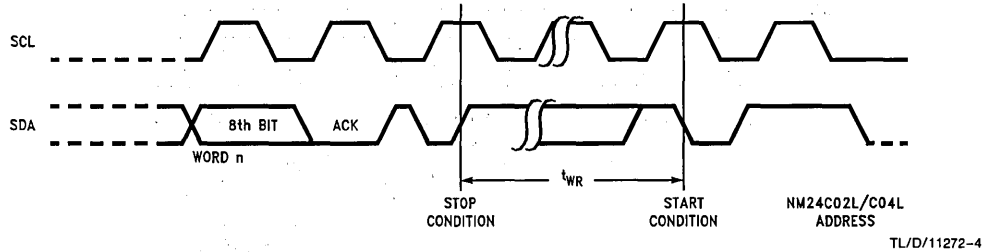
START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24CxxL continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

Write Cycle Timing



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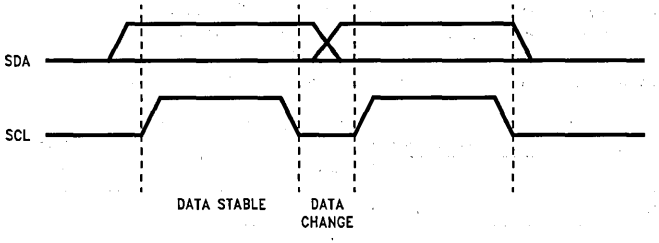

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FIGURE 1. Data Validity

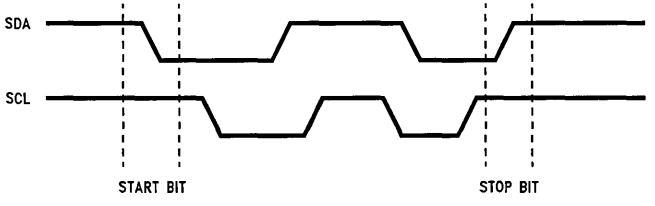

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FIGURE 2. Definition of Start and Stop

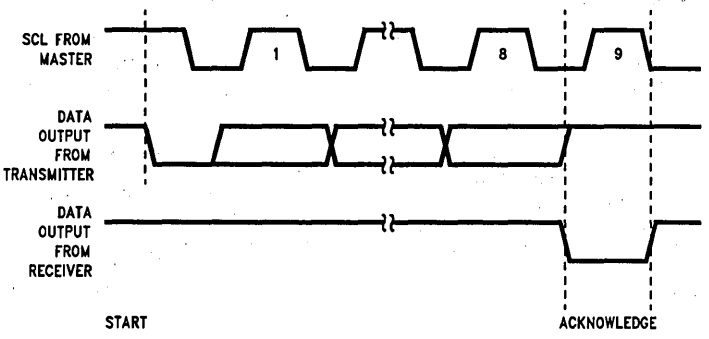

FIGURE 3. Acknowledge Response from Receiver

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24CxxL will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24CxxL will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24CxxL will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier, (see *Figure 4*). This is fixed as 1010 for both devices: NM24C02L and NM24C04L.

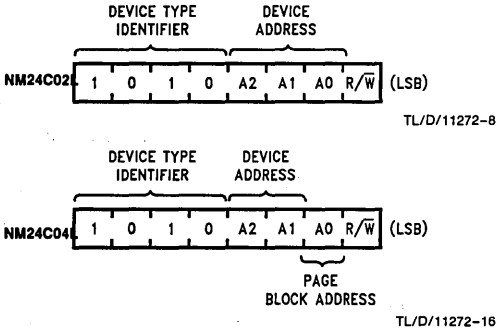

FIGURE 4. Slave Addresses

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C02	A	A	A	1 (2K)	(NONE)
NM24C04	P	A	A	2 (4K)	0 1
NM24C08	P	P	A	4 (8K)	00 01 10 11
NM24C02	P	P	P	8 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin

P: Refers to an internal PAGE BLOCK memory segment

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

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Device Addressing (Continued)

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed and a "0" initiates the write mode.

A simple review: After the NM24C02L/C04L recognizes the start condition, the devices interfaced to the I²C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24C02L/C04L responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24CxxL begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24CxxL inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24CxxL is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24CxxL will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

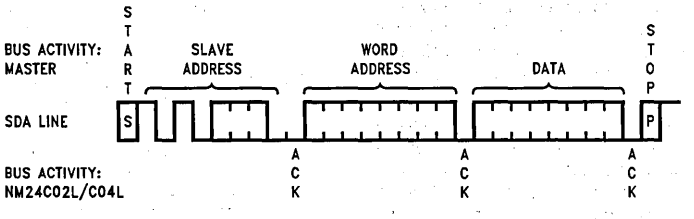

FIGURE 5. Byte Write

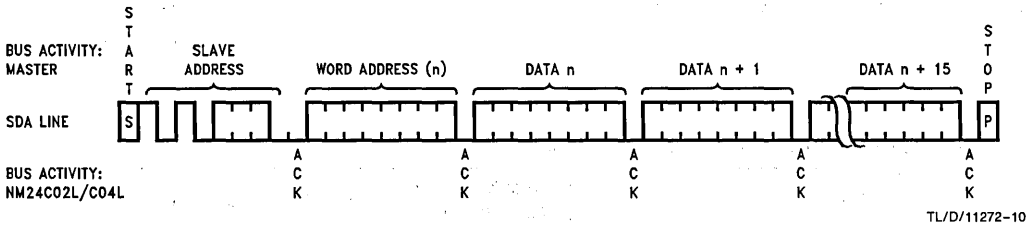

FIGURE 6. Page Write

Write Operations (Continued)

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation, the NM24CxxL initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24CxxL is still busy with the write operation, no ACK will be returned. If the NM24CxxL has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24CxxL contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24CxxL issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24CxxL discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24CxxL and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and the NM24CxxL discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24CxxL continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24CxxL continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

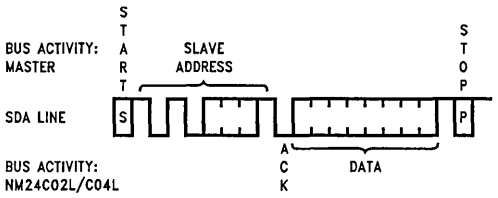

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FIGURE 7. Current Address Read

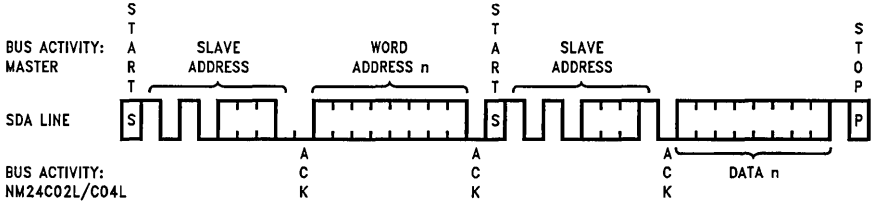

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FIGURE 8. Random Read

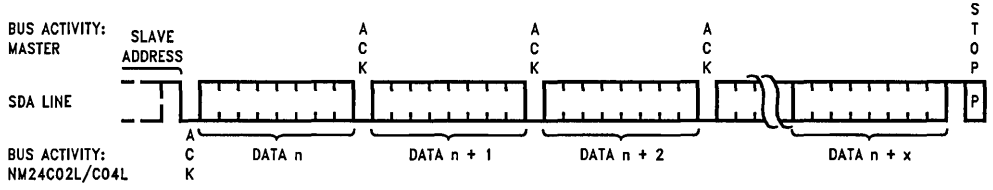

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FIGURE 9. Sequential Read

Write Operations (Continued)

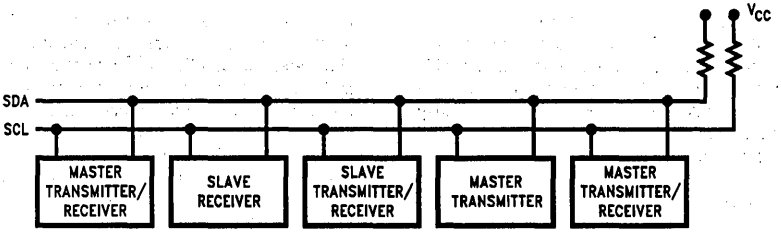

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FIGURE 10. Typical System Configuration

National Semiconductor

NM24C03L/C05L
2K-/4K-Bit Serial EEPROM with Write Protect and Extended Voltage (I^2C Synchronous 2-Wire Bus)

General Description

The NM24C03L/C05L devices are 2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I^2C 2-wire protocol, and are designed to minimize device pin count and simplify PC board layout requirements. National EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption.

The upper half of the memory can be disabled (Write Protected) by connecting the WP pin to V_{CC}. This section of memory then becomes ROM.

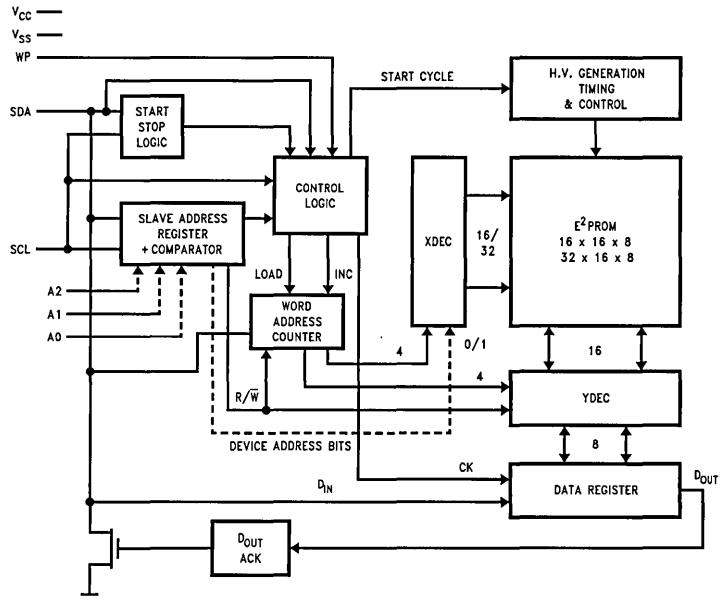
These devices have an operating voltage range of 2.5V to 5.5V and are offered in an 8-pin small outline (SO) package, making these devices perfectly suited for low power applications that require minimal board space usage.

This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

Features

- Hardwire write protect for upper block
- Low Power CMOS
  - 2 mA active current typical
  - 60 μA standby current typical
- 2-wire I^2C serial interface
  - Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - Minimizes total write time per byte
- Self timed write cycle
  - Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8-pin mini-DIP or 14-pin SO package

Functional Diagram



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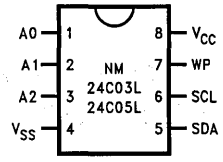
Connection Diagram

Dual-In-Line Package (N)



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Top View

See NS Package Number N08E (N) and M08A (M8)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
V_{CC}	+5V
WP	Write Protect

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C03LN/NM24C05LN NM24C03LM8/NM24C05LM8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C03LEN/NM24C05LEN NM24C03LEM8/NM24C05LEM8

LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24C03L/C05L	0°C to +70°C
NM24C03LE/C05LE	−40°C to +85°C
Positive Power Supply (V_{CC})	2.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.5V to 4.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 200 μA			0.4	V

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL, WP)	V_{IN} = 0V	6	pF

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

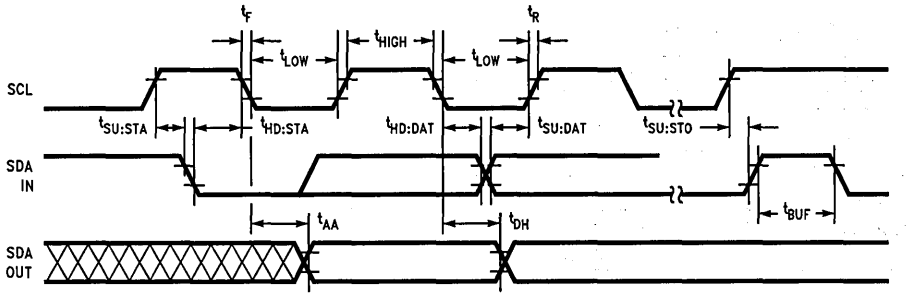
LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.5		μs
t_{LOW}	Clock Low Period	6.7		μs
t_{HIGH}	Clock High Period	4.5		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	500		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24C03L/C05L	0°C to +70°C
NM24C03LE/C05LE	−40°C to +85°C
Positive Power Supply (V_{CC})	2.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

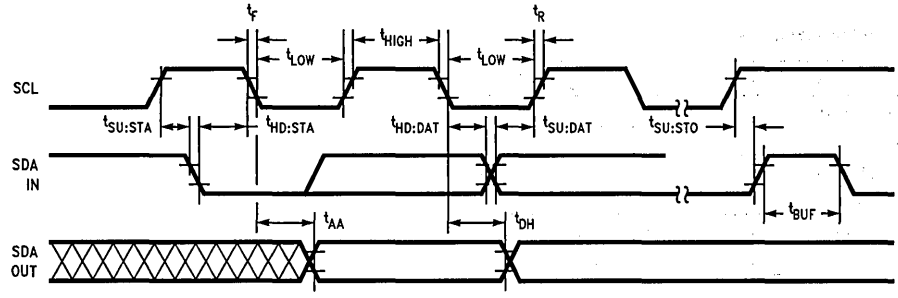
STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In additon, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMs on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

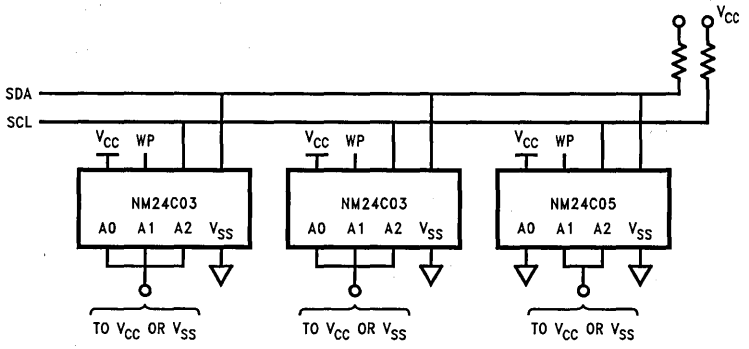
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string)

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any I²C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 8k (½ Maximum Size) of Memory on 2-Wire Bus



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Notes:

The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.
It is recommended that the total line capacitance be less than 400 pF.
Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C03L	DA	DA	DA	2048 Bits	1
NM24C05L	V_{SS}	DA	DA	4096 Bits	2

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24Cxx device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C03L	ADR	ADR	ADR	$2^3 = 8$ (8) × (2K) = 16K
NM24C05L	X	ADR	ADR	$2^2 = 4$ (4) × (4K) = 16K

ADR: Denotes an active pin used for device addressing

X: Not used for addressing (must be tied to Ground/V_{SS})

WP WRITE PROTECTION

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible.

If tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C03L/C05L supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24Cxx is considered a slave in all applications.

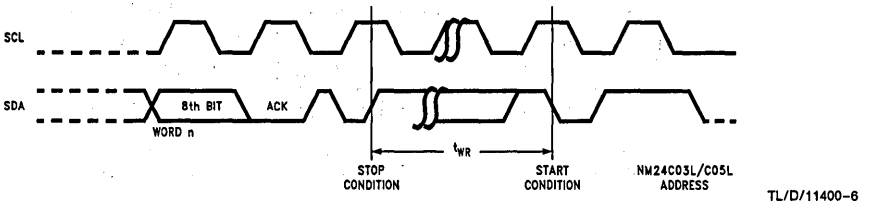
CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24Cxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Write Cycle Timing



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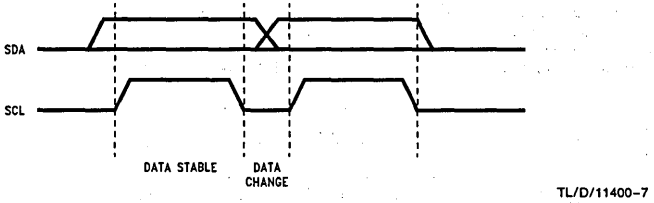

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FIGURE 1. Data Validity

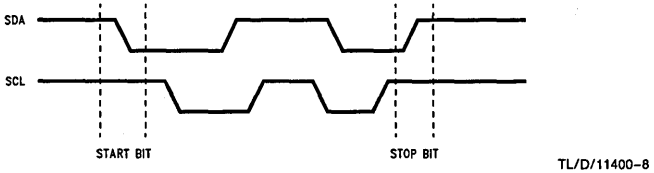

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FIGURE 2. Definition of Start and Stop

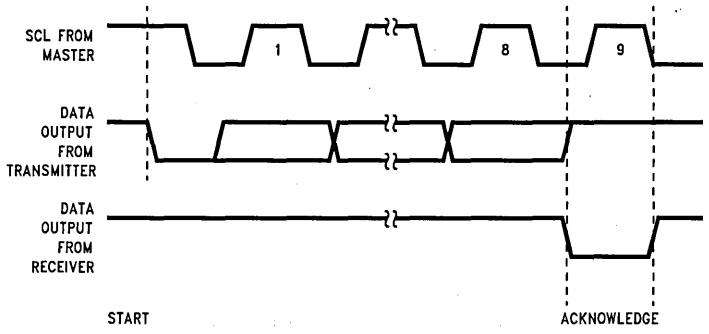

FIGURE 3. Acknowledge Response from Receiver

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24Cxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24Cxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24Cxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier, (see *Figure 4*). This is fixed as 1010 for both devices: NM24C03L and NM24C05L.

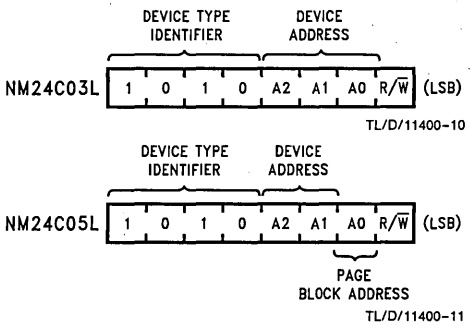

FIGURE 4. Slave Addresses

Device Addressing (Continued)

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C03L	A	A	A	1 (2K)	(None)
NM24C05L	P	A	A	2 (4K)	0 1

A: Refers to a hardware configured Device Address pin

P: Refers to an internal PAGE BLOCK memory segment

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed and a "0" initiates the write mode.

A simple review: After the NM24C03L/C05L recognizes the start condition, the devices interfaced to the I²C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24Cxx responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

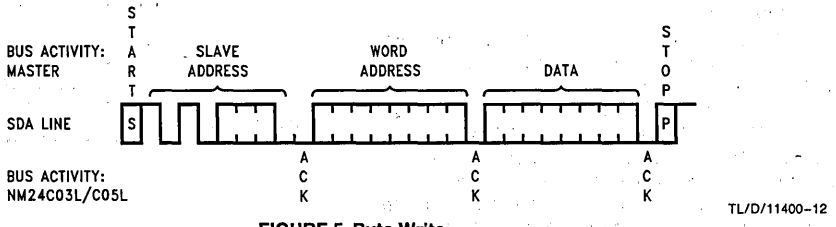

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FIGURE 5. Byte Write

Write Operations (Continued)

PAGE WRITE

The NM24Cxx is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24Cxx will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation, the NM24Cxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24Cxx is still busy with the write operation, no ACK will be returned. If the NM24Cxx has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the NM24Cxx is connected to V_{CC} (+5V). The NM24Cxx will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24Cxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24Cxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24Cxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24Cxx discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24Cxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24Cxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

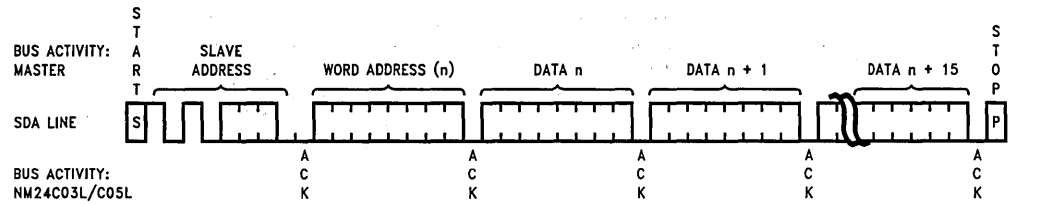

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FIGURE 6. Page Write

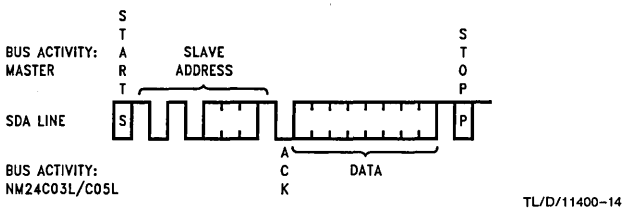

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FIGURE 7. Current Address Read

Read Operations (Continued)

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24Cxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24Cxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

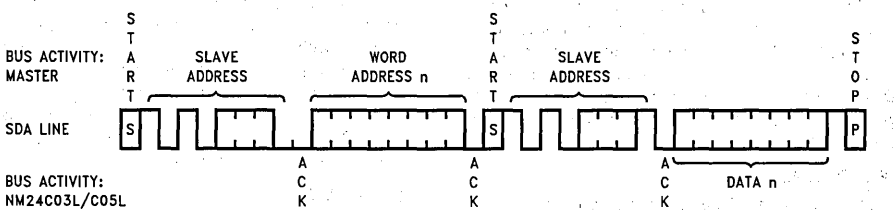

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FIGURE 8. Random Read

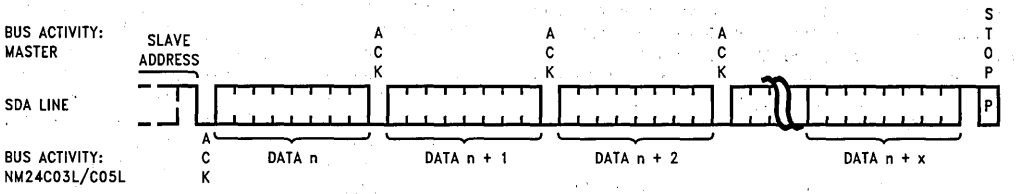

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FIGURE 9. Sequential Read

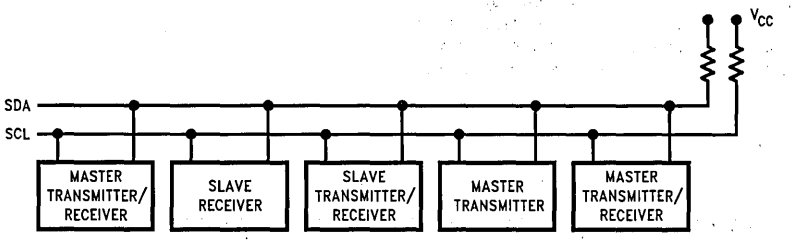

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FIGURE 10. Typical System Configuration

National Semiconductor

PRELIMINARY

NMS64X8EV
8k x 8 High Speed CMOS Static Ram with Extended Operating Voltage

General Description

The NSC NMS64X8EV is a very high speed, low power, 8192 words by 8-bit static RAM. It is fabricated using NSC's high performance CMOS double metal technology. This highly reliable process coupled with innovative circuit design technology, yields access times as fast as 25 ns with low power consumption.

When $\overline{CE}1$ is high or CE2 is low (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 25 μW (typical) with CMOS input levels.

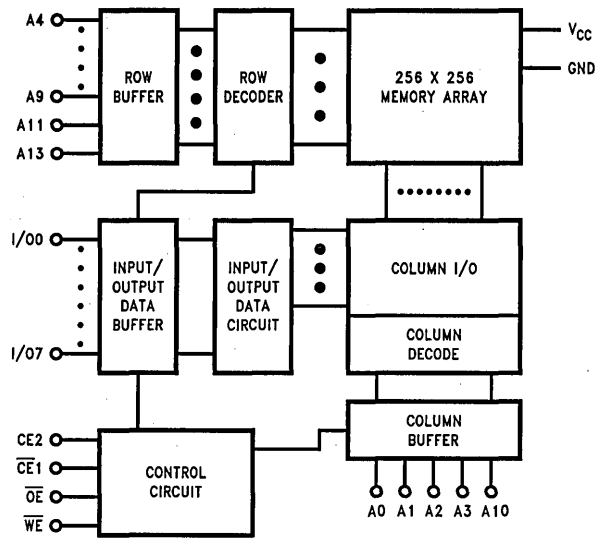
Easy memory expansion is provided by using two chip Enable inputs, $\overline{CE}1$ and CE2. The active low Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The NMS64X8EV is packaged in the JEDEC standard 28-pin, 300 mil DIP and SOJ surface mount packages.

Features

- Very high speed–25, 30, 35 ns (max)
- Fast output enable (t_{OE}) for cache applications
- Automatic power-down when chip is deselected
- CMOS low power operation
  - — 165 mW (typical) operating
  - — 6 mW (typical) standby
  - — 25 μW (typical) power-down
- TTL compatible interface levels
- Single power supply–3.0V to 5.5V
- Fully static operation—no clock refresh required
- Three state outputs
- Two chip enables ($\overline{CE}1$ and CE2) for simple memory expansion
- Data retention as low as 2V for battery back-up

Functional Block Diagram



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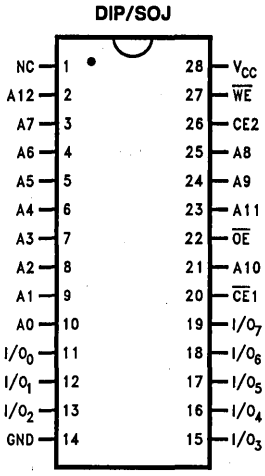
Pin Configuration



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5

Absolute Maximum Ratings (Note 1)

Terminal Voltage with Respect to GND (V_{TERM})	−0.5V to +6.0V
Temperature under Bias (T_{BIAS})	−55°C to +125°C
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation (P_T)	0.8W
DC Output Current (low) (I_{OUT})	20 mA

Note 1: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to 70°C	3.3V ±0.3V

Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Conditions		NMS64X8EV-25		NMS64X8EV-30		NMS64X8EV-35		Units
				Min	Max	Min	Max	Min	Max	
V_{OH}	Output High Voltage	V_{CC} = 3V, I_{OH} = −1.0 mA V_{CC} = 5V, I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input High Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage (Note 2)			−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}		−10	10	−10	10	10	−10	μA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled		−10	10	−10	10	10	−10	μA
I_{OS}	Output Short Circuit Current (Note 1)	V_{CC} = Max, V_{OUT} = GND			−150		−150		−150	mA
I_{CC1}	V_{CC} Operating Supply Current (Note 3)	V_{CC} = Max I_{OUT} = 0 mA, f = 0	V_{CC} = 5V		150		150		130	mA
			V_{CC} = 3V		70		60		60	
I_{CC2}	V_{CC} Dynamic Operating Supply Current (Note 3)	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{max}	V_{CC} = 5V		180		180		155	mA
			V_{CC} = 3V		90		80		70	
I_{SB1}	TTL Standby Current (TTL Inputs) (Note 3)	V_{IN} = V_{IH} or V_{IN} = V_{IL}, $\overline{CE}1$ ≥ V_{IH} or CE2 ≤ V_{IL}, V_{CC} = Max, f = 0	V_{CC} = 5V		25		20		20	mA
			V_{CC} = 3V		6		6		6	
I_{SB2}	CMOS Standby Current (CMOS Inputs) (Note 3)	V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V, f = 0 $\overline{CE}1$ ≥ V_{CC} − 0.2V, CE2 ≤ 0.2V, V_{CC} = Max	V_{CC} = 5V		4		3		3	mA
			V_{CC} = 3V		2		2		2	

Note 1: Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Note 2: V_{IL} = −3.0V for pulse width less than 10 ns.

Note 3: At f = f_{max} address and data input are cycling at the maximum frequency, f = 0 means no input lines change.

Capacitance (Notes 1, 2)

Symbol	Parameter	Conditions	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Note 1: This parameter is guaranteed and not tested.

Note 2: Test condition: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

Truth Table

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	V_{CC} Current
Not Selected (Power Down)	X	H	X	X	High Z	I_{SB1}, I_{SB2}
	X	X	L	X	High Z	I_{SB1}, I_{SB2}
Output Disababled	H	L	H	H	High Z	I_{CC1}, I_{CC2}
Read	H	L	H	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	H	X	D_{IN}	I_{CC1}, I_{CC2}

Switching Characteristics Over Operating Range (Note 1)

Symbol	Parameter	NMS64X8EV-25		NMS64X8EV-30		NMS64X8EV-35		Units
		Min	Max	Min	Max	Min	Max	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address Access Time		25		30		35	ns
t_{OHA}	Output Hold Time	3		3		3		ns
t_{ACE1}	$\overline{CE1}$ Access Time		25		30		35	ns
t_{ACE2}	CE2 Access Time		25		30		35	ns
t_{DOE}	$\overline{OE}$ Access Time		9		12		15	ns
t_{LZOE}	$\overline{OE}$ to Low Z Output	0		0		0		ns
t_{HZOE} (Note 2)	$\overline{OE}$ to High Z Output		9		12		15	ns
t_{LZCE1}	$\overline{CE1}$ to Low Z Output	3		3		3		ns
t_{LZCE2}	CE2 to Low Z Output	3		3		3		ns
t_{HZCE} (Note 2)	$\overline{CE1}$ or CE2 to High Z Output		12		15		18	ns
t_{PU}	$\overline{CE1}$ or CE2 to Power Up	0		0		0		ns
t_{PD}	$\overline{CE1}$ or CE2 to Power Down		20		20		20	ns
WRITE CYCLE (Note 3)								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCE1}	$\overline{CE1}$ to Write End	22		25		28		ns
t_{SCE2}	CE2 to Write End	22		25		28		ns
t_{AW}	Address Set-Up Time to Write End	20		25		28		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up Time	0		0		0		ns
t_{PWE} (Note 4)	$\overline{WE}$ Pulse Width	15		18		20		ns
t_{SD}	Data Set-Up to Write End	12		15		18		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE} (Note 2)	$\overline{WE}$ Low to High Z Output		12		15		18	ns
t_{LZWE}	$\overline{WE}$ High to Low Z Output	0		0		0		ns

Note 1: Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, Input pulse levels of 0V to 3.0V and output loading specified in *Figure 1a.*

Note 2: Tested with the load in *Figure 1b.* Transition is measured ± 500 mV from steady state voltage.

Note 3: The internal write time is defined by the overlap of $\overline{CE1}$ low, CE2 high and $\overline{WE}$ low. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

Note 4: Tested with $\overline{OE}$ high.

Note 5: $\overline{WE}$ is high for a Read Cycle.

Note 6: The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}.

Note 7: Address is valid prior to or coincident with $\overline{CE1}$ Low and CE2 High transitions.

Note 8: I/O will assume the High Z state if $\overline{OE}$ = V_{IH}.

AC Test Conditions

Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V

AC Test Loads and Waveforms

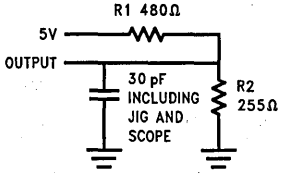

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FIGURE 1a

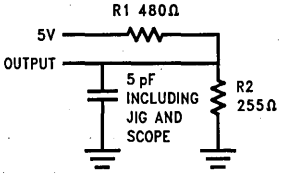

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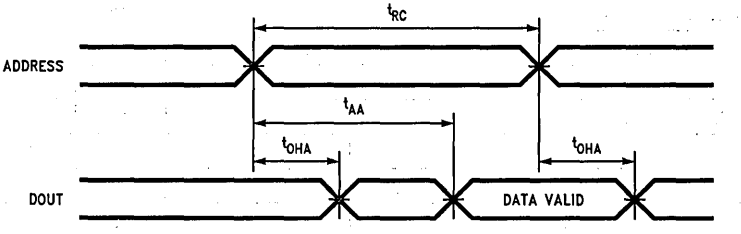
FIGURE 1b

AC Waveforms

Read Cycle No. 1 (Notes 5, 6)



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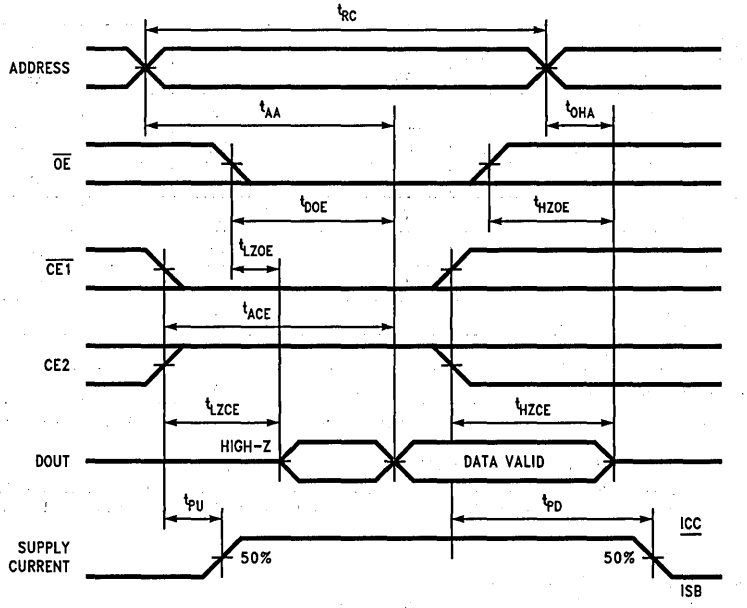
Read Cycle No. 2 (Notes 5, 7)



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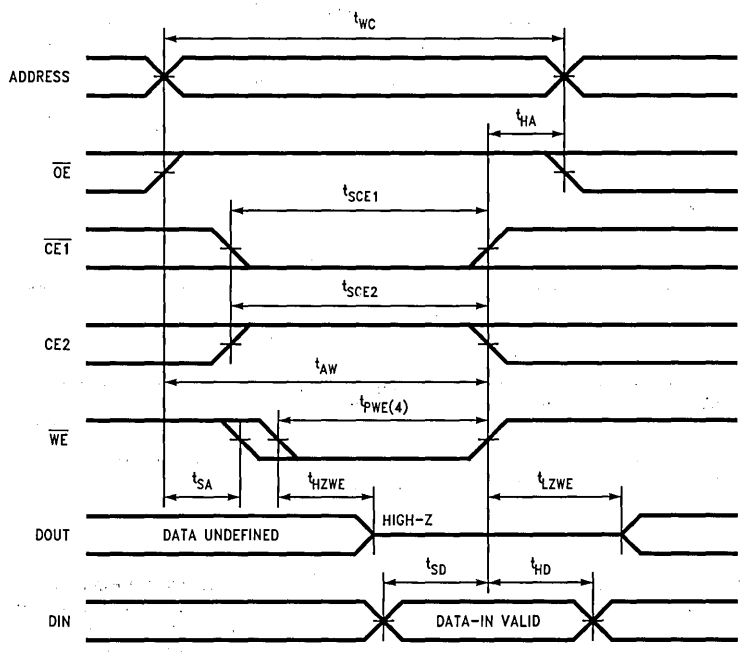
AC Waveforms (Continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Notes 3, 8)



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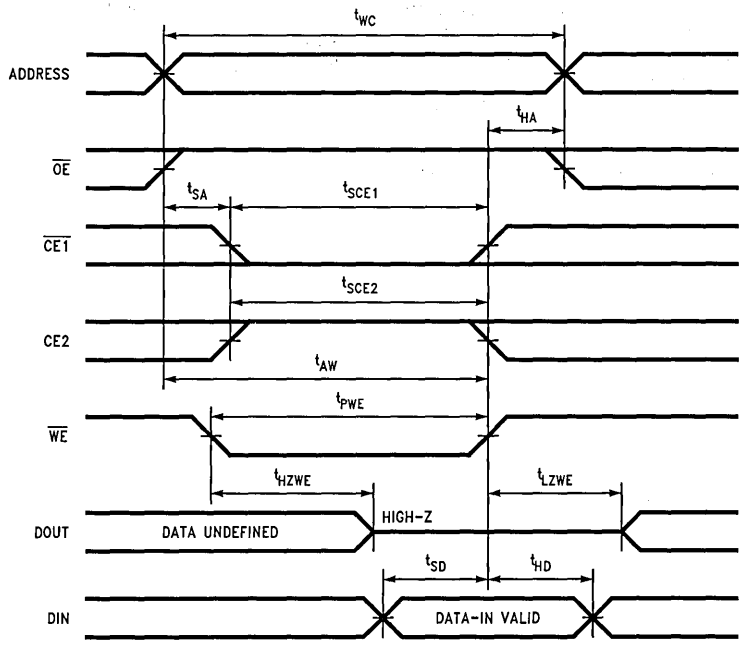
Write Cycle No. 2 ($\overline{CE1}$, CE2 Controlled) (Notes 3, 8)



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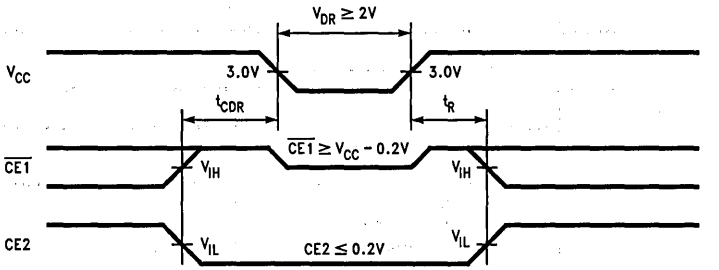
Data Retention Characteristics (L Version Only)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Retention of Data	V_{CC} = 2.0V $\overline{CE1} \geq V_{CC} - 0.2V$ CE2 ≤ 0.2V, CMOS Inputs	2.0	—	V
I_{CCDR}	Data Retention Current		—	100	μA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	ns
t_R	Operation Recovery Time		t_{RC}	—	ns
I_{LI}	Input Leakage Current		—	2	μA

Data Retention Waveform



TL/D/11398–9

Pin Descriptions

A0–A2 **Address Inputs.** These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{CE1}$, CE2 **Chip Enable 1 Input, Chip Enable 2 Input.** $\overline{CE1}$ is active Low and CE2 is active High. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

$\overline{OE}$ **Output Enable Input.** The output enable input is active Low. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the I/O pins. The I/O pins will be in the high-impedance state when $\overline{OE}$ is inactive.

$\overline{WE}$ **Write Enable Input.** The write enable input is active Low and controls read and write operations. With the chip selected, when $\overline{WE}$ is Low input data present on the I/O pins will be written into the selected memory location.

I/O0–I/O7 These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} **Power**

GND **Ground**

National Semiconductor

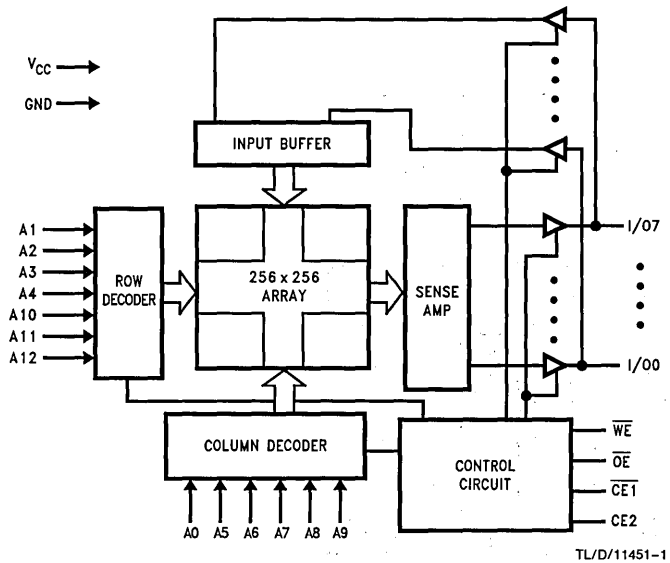
ADVANCE INFORMATION

NMS64X8LV
8k x 8 High Speed CMOS SRAM (3.3V) with Low Operating Voltage

Features

- Organization: 8,192 words x 8 bits
- Power Supply: V_{CC} = 3.3V ±0.3V
- High Speed:
  — 15/20/25/35 ns t_{AA}/t_{ACE} access time
  — 4/5/5/8 ns t_{OE} access time
- Low Standby Current:
  Full standby current of 2 μA maximum
- 2V Data Retention for battery back-up operation
  Data Retention of 60 μA maximum
- TTL compatible inputs and outputs
- Reduced power after initial access for lap-top computer applications
- Automatic power-down when de-selected
- Completely static memory; no clocks or timing strobe required
- Equal access and cycle times
- JEDEC pin compatible
- For high density, a slim 300 mil, 28-pin DIP or SOJ
- ESD protection exceeds 2000V
- Latch-up current > 200 mA

Logic Block Diagram



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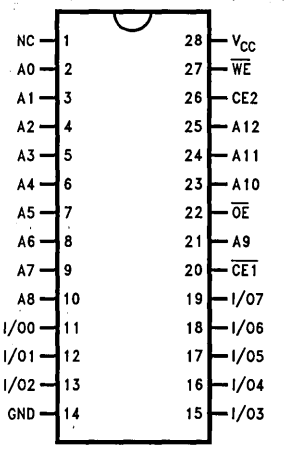
Pin Arrangement

28-Pin DIP/SOJ



TL/D/11451–2

Selection Guide

		NMS64X8LV-15	NMS64X8LV-20	NMS64X8LV-25	NMS64X8LV-35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)		65	60	55	50
Maximum Standby Current (mA)		1.0	1.0	1.0	1.0
	L	0.05	0.05	0.05	0.05

5

National Semiconductor

PRELIMINARY

NMS64X4EV
16k x 4 High Speed CMOS Static RAM with Extended Operating Voltage

General Description

The NSC NMS64X4EV is a very high speed, low power, 16,384-words by 4-bit static RAM. The device is fabricated using NSC's high performance CMOS double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 25 ns with low power consumption.

When $\overline{CE}1$ is high the device assumes a standby with low power consumption mode at which the power dissipation can be reduced down to 25 μW (typical) with CMOS input levels.

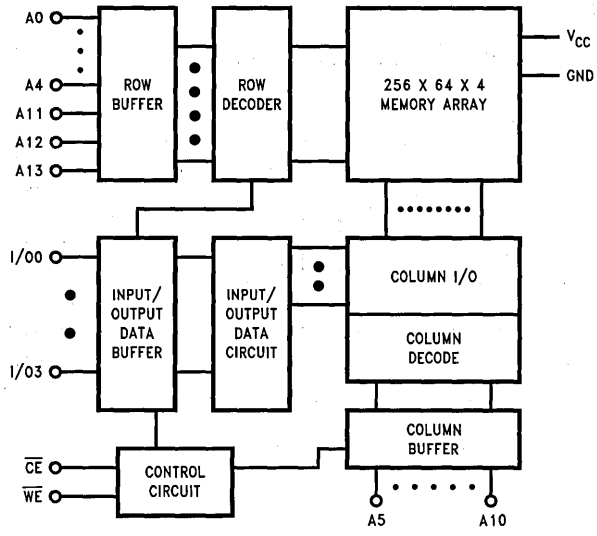
Easy memory expansion is provided by using active low Chip Enable, $\overline{CE}$ and three state drivers.

The NMS64X4EV is packaged in the JEDEC standard 22-pin 300 mil DIP and JEDEC Standard 24-pin SOJ surface mount packages.

Features

- Very high speed 25, 30, 35 ns (Max)
- Automatic power-down when chip is deselected
- CMOS low power operation
  - — 165 mW (typical) operating
  - — 6 mW (typical) standby
  - — 25 μW (typical) power-down
- TTL compatible interface levels
- Single power supply −3.0V to 5.5V
- Fully static operating—no clock refresh required
- Three state outputs
- Chip enables ($\overline{CE}1$ for simple memory expansion)
- Data retention as low as 2V for battery back-up (L-version)

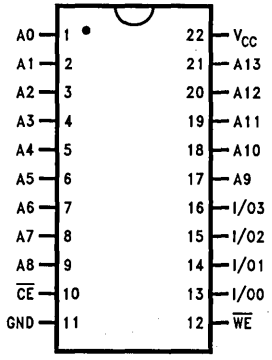
Functional Block Diagram



TL/D/11397–1

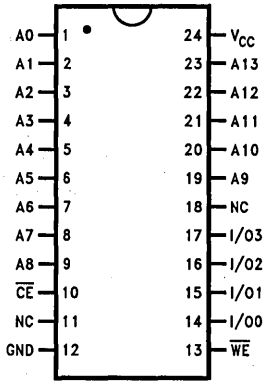
Pin Configuration

DIP



TL/D/11397-2

SOJ



TL/D/11397-3

Truth Table

Mode	$\overline{WE}$	$\overline{CE}$	I/O Operation	V_{CC} Current
Not Select (Power Down)	X	H	High Z	I_{SB_1}, I_{SB_2}
Read	H	L	D_{OUT}	I_{CC_1}, I_{CC_2}
Write	L	L	D_{IN}	I_{CC_1}, I_{CC_2}

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Absolute Maximum Ratings(Note 1)

Terminal Voltage with Respect to GND (V_{TERM})	−0.5V to +6.0V
Temperature under Bias (T_{BIAS})	−55°C to +125°C
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation (P_T)	0.8W
DC Output Current (Low) (I_{OUT})	20 mA

Note 1: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ±0.3V

Electrical Characteristics over Operating Range

Symbol	Parameter	Test Conditions		NMS64X4EV-25		NMS64X4EV-30		NMS64X4EV-35		Units
				Min	Max	Min	Max	Min	Max	
V_{OH}	Output High Voltage	V_{CC} = 3V, I_{OH} = −1.0 mA V_{CC} = 5V, I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input High Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage (Note 2)			−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}		−10	10	−10	10	10	−10	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled		−10	10	−10	10	10	−10	µA
I_{OS}	Output Short Circuit Current (Note 1)	V_{CC} = Max, V_{OUT} = GND			−150		−150		−150	mA
I_{CC_1}	V_{CC} Operating Supply Current (Note 3)	V_{CC} = Max, I_{OUT} = 0 mA, f = 0	V_{CC} = 5V		150		150		130	mA
			V_{CC} = 3V		70		60		60	
I_{CC_2}	V_{CC} Dynamic Operating Supply Current (Note 3)	V_{CC} = Max I_{OUT} = 0 mA, f = f_{MAX}	V_{CC} = 5V		180		180		155	mA
			V_{CC} = 3V		90		80		70	
I_{SB_1}	TTL Standby Current (TTL (Inputs) (Note 3)	V_{IN} = V_{IH} or V_{IN} = V_{IL}, $\overline{CE1}$ ≥ V_{IH} or CE2 ≤ V_{IL}, V_{CC} = Max, f = 0	V_{CC} = 5V		25		20		20	mA
			V_{CC} = 3V		6		6		6	
I_{SB_2}	CMOS Standby Current (CMOS Inputs) (Note 3)	V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V, f = 0 $\overline{CE1}$ ≥ V_{CC} − 0.2V, CE2 ≤ 0.2V, V_{CC} = Max	V_{CC} = 5V		4		3		3	mA
			V_{CC} = 3V		2		2		2	

Note 1: Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Note 2: V_{IL} = −3.0V for pulse width less than 10 ns.

Note 3: At f = f_{max} address and data input are cycling at the maximum frequency, f = 0 means no input lines change.

Switching Characteristics over Operating Range (Note 1)

Symbol	Parameter	NMS64X4EV-25		NMS64X4EV-30		NMS64X4EV-35		Units
		Min	Max	Min	Max	Min	Max	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address Access Time		25		30		35	ns
t_{OHA}	Output Hold Time	3		3		3		ns
t_{ACE}	$\overline{CE}$ Access Time		25		30		35	ns
t_{LZCE}	$\overline{CE}$ to Low Z Output	3		3		3		ns
t_{HZCE} (Note 2)	$\overline{CE}$ to High Z Output		12		15		18	ns
t_{PU}	$\overline{CE}$ to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ to Power Down		20		20		20	ns
WRITE CYCLE (Note 3)								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCE}	$\overline{CE}$ to Write End	22		25		28		ns
t_{AW}	Address Setup Time to Write End	20		25		28		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Setup Time	0		0		0		ns
t_{PWE} (Note 4)	$\overline{WE}$ Pulse Width	20		25		28		ns
t_{SD}	Data Setup to Write End	12		15		18		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z Output		8		10		12	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	0		0		0		ns

Note 1: Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in *Figure 1a*.

Note 2: Tested with the load in *Figure 1b*. Transition is measured ±500 mV from steady state voltage.

Note 3: The internal write time is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data input Setup and Hold timing are referenced to the rising edge of the signal that terminates the write.

Note 4: Apply input data after $\overline{WE}$ TRI-STATE® the output.

Note 5: $\overline{WE}$ is high for a Read Cycle.

Note 6: The device is continuously selected. $\overline{CE} = V_{IL}$.

Note 7: Address is valid prior to or coincident with $\overline{CE}$ Low transitions.

Capacitance (Notes 1, 2)

Symbol	Parameter	Conditions	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

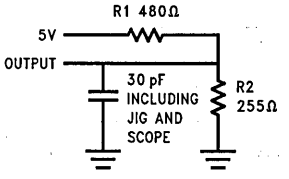
Note 1. This parameter is guaranteed and not tested.

Note 2. Test condition: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V

AC Test Conditions

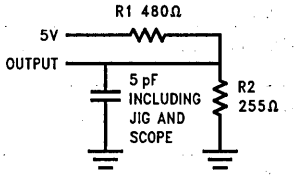
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V

AC Test Loads and Waveforms



TL/D/11397–4

FIGURE 1a

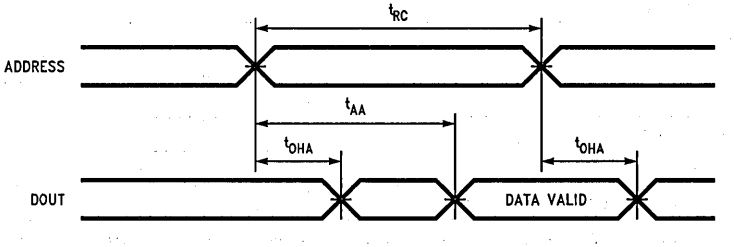


TL/D/11397–5

FIGURE 1b

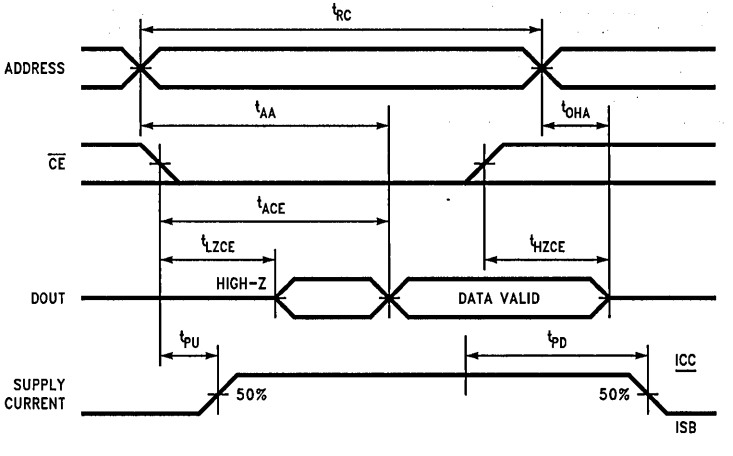
AC Waveforms

READ CYCLE NO. 1 (Notes 5, 6)



TL/D/11397–6

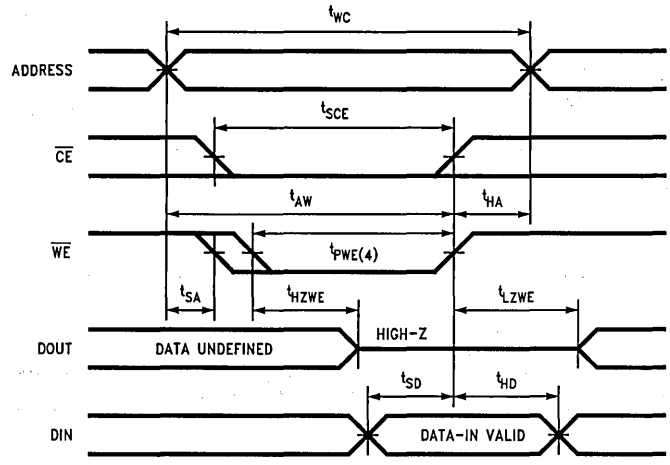
READ CYCLE NO. 2 (Notes 5, 7)



TL/D/11397–7

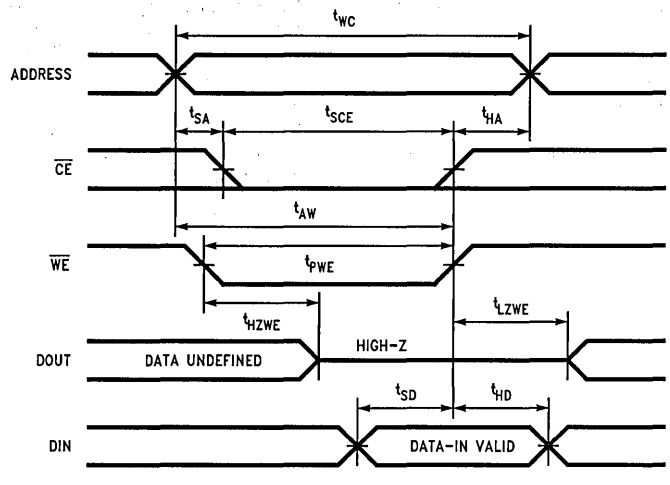
AC Waveforms (Continued)

WRITE CYCLE No. 1 ($\overline{WE}$ Controlled) (Note 3)



TL/D/11397–8

WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled) (Note 3)



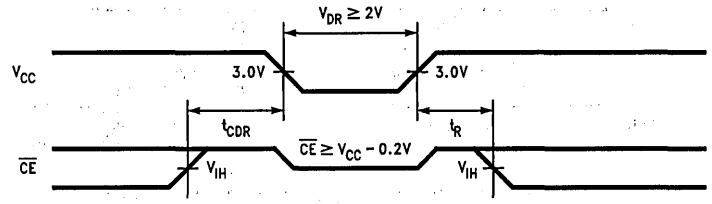
TL/D/11397–9

5

Data Retention Characteristics (L Version Only)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{DR}	V_{CC} for Retention of Data	V_{CC} = 2.0V $\overline{CE} \geq V_{CC} - 0.2V$ CMOS Inputs	2.0		V
I_{CCDR}	Data Retention Current			100	μA
t_{CDR}	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		t_{RC}		ns
I_{LI}	Input Leakage Current			2	μA

Data Retention Waveform



TL/D/11397–10

Pin Descriptions

A0–A13 Address Inputs

These 14 address inputs select one of the 16,384 4-bit words in the RAM.

$\overline{CE}$ Chip Enable Input

$\overline{CE}$ is active Low. The chip enable must be active to read from or write to the device. If the chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

GND—Ground

$\overline{WE}$ Write Enable Input

The write enable input is active Low and controls read and write operations. With the chip selected, when $\overline{WE}$ is Low, Input data present on the I/O pins will be written into the selected memory location.

I/O0–I/O3

These 4 bidirectional ports are used to read data from or write data into the RAM.

V_{CC}—Power

National Semiconductor

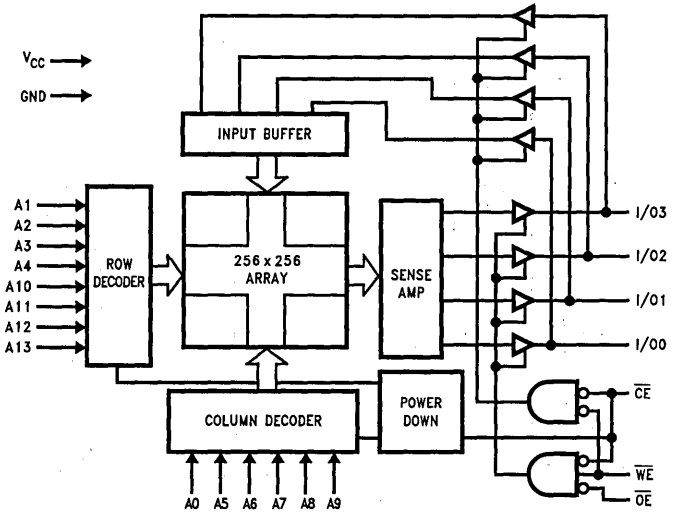
ADVANCE INFORMATION

NMS64X4LV
16k x 4 High Speed CMOS SRAM with Low Operating Voltage

Features

- Organization: 16,384 words x 4 bits
- Power Supply: V_{CC} = 3.3V ± 0.3V
- High Speed:
  15/20/25/35 ns t_{AA}/t_{ACE} access time
  4/5/5/8 ns t_{OE} access time
- Low Standby Current:
  Full standby current of 50 μA maximum
- 2V Data Retention for battery back-up operation
  Data Retention of 20 μA maximum
- TTL compatible inputs and outputs
- Reduced power consumption after initial access for lap-top computer applications
- Output Enable ($\overline{OE}$) Feature (NMS64X4)
- Automatic power-down when de-selected
- Completely static memory. No clocks or timing strobes required
- Equal access and cycle times
- JEDEC standard compatible pinout
- Slim 300 mil, 20- and 24-pin plastic as well as 24-pin J-Bend SOIC
- ESD protection exceeds 2000V
- Latch-up current > 200 mA

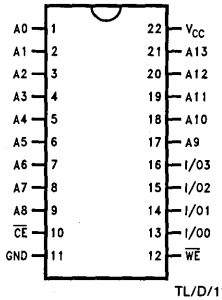
Logic Block Diagram



TL/D/11452-1

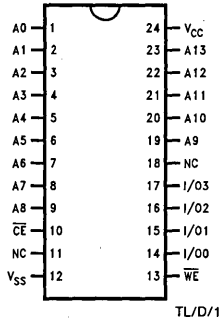
Pin Arrangement

DIP



TL/D/11452-2

SOJ



TL/D/11452-3

Selection Guide

		NMS64X4LV-15	NMS64X4LV-20	NMS64X4LV-25	NMS64X4LV-35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)		65	60	55	50
Maximum Standby Current (mA)		1.0	1.0	1.0	1.0
	L	0.05	0.05	0.05	0.05

5

National Semiconductor

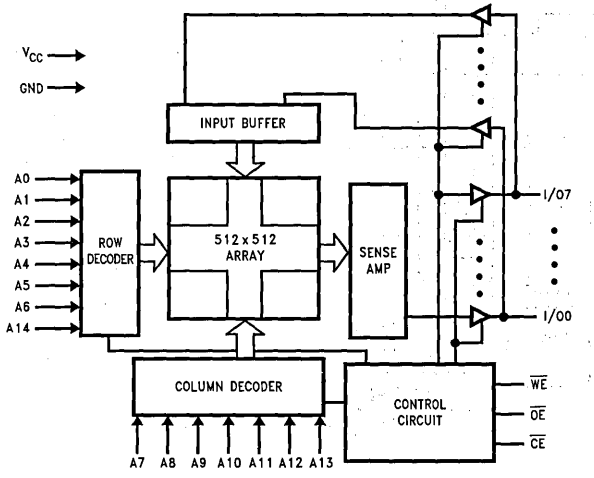
ADVANCE INFORMATION

NMS256X8LV
High Performance 32K x 8 CMOS SRAM with Low Operating Voltage

Features

- Organization: 32,768 words x 8 bits
- Power Supply: V_{CC} = 3.3V ±0.3V
- Specifications optimized for notebook/laptop applications at 25/33/40 MHz
- High Speed:
  — 20/25/35 ns t_{AA} access time
  — 5/5/8 ns t_{OE} access time
- Low Standby Current:
  Full standby current of 50 μA maximum
- 2V Data Retention for battery back-up operations
  Data Retention current of 20 μA maximum
- TTL compatible inputs and outputs
- Reduced power consumption after initial access for notebook/laptop computer applications
- Automatic power-down when de-selected
- Completely static memory. No clocks or timing strobe required
- Equal access and cycle times
- JEDEC standard compatible pinout
- Slim 300 mil 28-pin plastic DIP as well as a J-bend, SOJ package for high board density
- ESD protection exceeds 2000V
- Latch-up current ≥ 200 mA

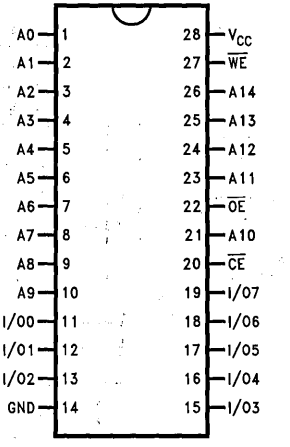
Logic Block Diagram



TL/D/11396–1

Pin Arrangement

28-Pin DIP/SOJ



TL/D/11396–2

Selection Guide

		NMS256X8LV-20	NMS256X8LV-25	NMS256X8LV-35
Maximum Access Time (ns)		20	25	35
Maximum Operating Current (mA)		60	55	55
	L	55	50	50
Maximum Standby Current (mA)		1.0	1.0	1.0
	L	0.05	0.05	0.05

National Semiconductor

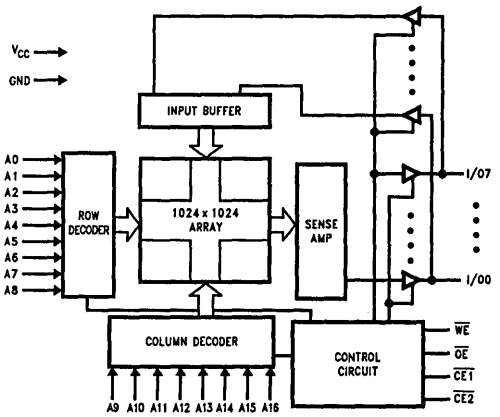
ADVANCE INFORMATION

NMS1024X8LV
High Performance 128K x 8 CMOS SRAM with Low Operating Voltage

Features

- Organization: 131,072 words x 8 bits
- Power Supply: V_{CC} = 3.3V ±0.3V
- Specifications optimized for notebook/laptop applications at 25/33/40/50 MHz
- High Speed:
  - 25/35/45 ns t_{OE} access time
  - 5/8/8 ns t_{OE} access time
- Low Standby Current:
  Full standby current of 50 µA maximum
- 2V Data Retention for battery back-up operation
  Data Retention current of 20 µA maximum
- TTL compatible inputs and outputs
- Reduced power consumption after initial access for notebook/laptop computer applications
- Automatic power-down when de-selected
- Completely static memory. No clocks or timing strobe required
- Equal access and cycle time
- JEDEC standard compatible pinout
- Slim 300 mil 32-pin plastic DIP as well as SOJ surface mount package for high board density
- ESD protection exceeds 2000V
- Latch-up current ≥ 200 mA

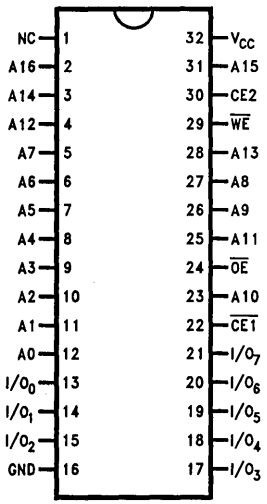
Logic Block Diagram



TL/D/11399-1

Pin Arrangement

32-Pin DIP/SOJ



TL/D/11399-2

Selection Guide

		NMS1024X8LV-25	NMS1024X8LV-35	NMS1024X8LV-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)		55	50	50
	L	50	45	45
Maximum Standby Current (mA)		1.0	1.0	1.0
	L	0.05	0.05	0.05

Section 6
ASIC

Section 6 Contents

National Semiconductor

PRELIMINARY

SCLA 0.8μ CMOS Standard Cell Family

1.0 General Description

National Semiconductor's CMOS standard cell family utilizes a 0.8 micron Leffective (1.0 micron drawn) dual metal, silicon gate CMOS technology (microCMOS). This high performance process is capable of achieving operating speeds similar to Schottky-TTL but with the inherent lower power dissipation of standard CMOS technology. All I/O and pad cells in the microCMOS family have high noise immunity and are protected from static discharge.

Supporting the needs for low power systems, National Semiconductor provides libraries characterized for low voltage operation. The libraries enable designers to accurately simulate designs with power supplies centered around 3.0V, 3.3V, and 5.0V operation while maintaining the capability for implementing high density "systems on a chip."

National Semiconductor supports standard cell designs with a variety of design interfaces. This ranges from producing integrated circuits from the user's schematic to accepting his database for mask generation. A large dedicated staff of integrated circuit design consultants are readily available at National's Technology Centers to help the users determine the most efficient and cost effective way to meet their semi-custom integrated circuit requirements.

A well rounded package of easy-to-use design automation software is available to help the user quickly and easily implement and verify the design. These tools include workstation design kits, as well as sun-based software for design integrity verification, logic and timing simulation, automatic cell placement and routing, and IC layout design verification. The system is tailored to allow the user to participate in the development of his circuit to whatever level he desires.

2.0 Product Features

- State-of-the-art N-well CMOS technology with 0.8 μ Leffective, (1.0μ drawn) geometries, silicon gates and dual-metal layered interconnects
- Libraries characterized for low voltage operation
- Ultra-high performance; 0.5 ns typical gate delay
- Minimal power dissipation
- All inputs fully protected from over-voltage, latch-up, and static discharge
- A full range of I/O cells for a variety of off-chip interfaces and drive capabilities:
  - — Bidirectional inputs/outputs
  - — Inputs compatible with TTL, CMOS, or Schmitt Trigger levels
  - — Push-pull or TRI-STATE outputs
  - — High current output drivers available
- A variety of packaging configurations with up to 323 pins
- Multiple cell families available:
  - — Large number of logical functions and I/O configurations
  - — RAMs, ROMs
  - — Design compatibility with National Semiconductor SCL 2.0μ standard cell family
- Module generator of high density static RAMs and ROMs
- Separate power ring for core and for I/O to minimize noise
- Optional on-chip test circuitry for outputs and I/O buffers to facilitate parametric testing

ON-CHIP TEST CIRCUIT

National Semiconductor's CMOS standard cell family provides the optional On-Chip Test Circuitry, at the cost of a single input pin, to create the TEST MODE for parametric testing.

With this pin active (low), two additional pre-defined inputs are jointly employed to force all outputs and bidirectional IOs to high, low or hi-Z states and thus reduce test time in gathering output parametrics.

The dedicated Test Mode Control (TMC) pin, when low, activates the On-Chip Test Circuitry. The Data Test (DT) and the TRI-STATE Test Control (TSTC) pins can be used in the user's design as the normal input pin without any performance penalty. Any input will be assigned to DT or TSTC test pin when the selected macro has the suffix td or ts respectively. The DT and TSTC pins are only active when the TMC input is enabled.

Note: The TMC pin has an internal pull-up resistor of typical 120 kΩ.

Truth Table of the On-Chip Test Circuit

TMC	DT(1)	TSTC(1)	Push-Pull Output	TRI-STATE Output(2)
1	X	X	Normal Operation	
0	1	0	0	0
0	0	0	1	1
0	X	1	NA	Z

Note 1: The state of the DT and TSTC test pins is given for a non-inverting input buffer. The state will be inverted in case an inverting input buffer is used.

Note 2: Including all bidirectional I/O buffer.

Module Generated Functional Blocks

Module Generated Functional Block	Maximum Size (Per Block)	Possible Configuration
Single Port RAM	18 Kbits	4 to 36 Bits/Word, 16 to 1024 Words
ROM	64 Kbits	1 to 64 Bits/Word, 1 to 64K Words
Dual Port RAM	18 Kbits	6 to 72 Bits/Word, 16 to 1024 Words

Section 7

Embedded Controllers

Section 7 Contents

National Semiconductor

COP410C/COP411C/COP310C/COP311C Single-Chip CMOS Microcontrollers

General Description

The COP410C, COP411C, COP310C, and COP311C fully static, single-chip CMOS microcontrollers are members of the COPS™ family, fabricated using double-poly, silicon-gate CMOS technology. These controller-oriented processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, and BCD data manipulation. The COP411C is identical to the COP410C but with 16 I/O lines instead of 20. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized controller-oriented processor at a low end-product cost.

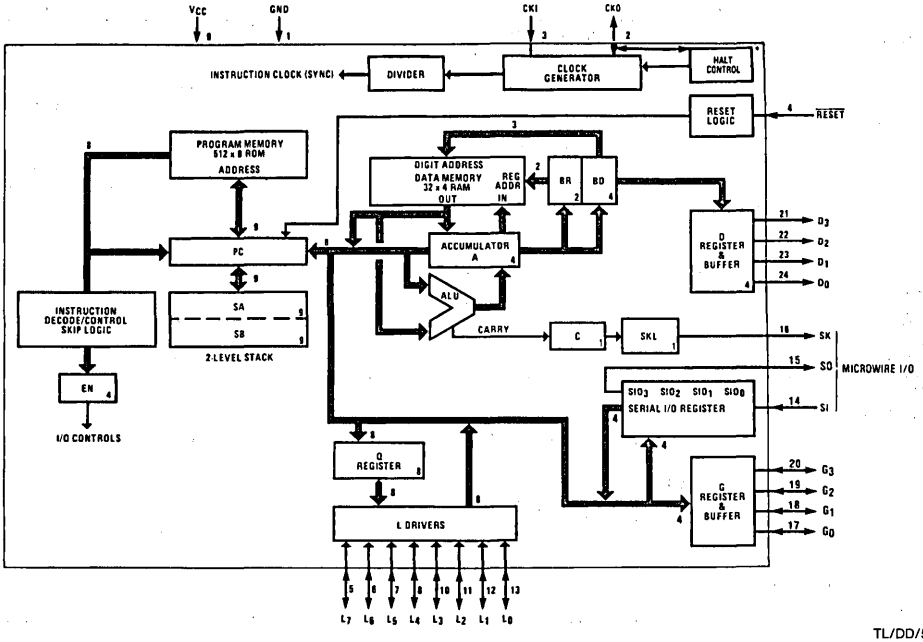
The COP310C/COP311C is the extended temperature range version of the COP410C/COP411C.

The COP404C should be used for exact emulation.

Features

- Lowest power dissipation (40 μW typical)
- Low cost
- Power-saving HALT Mode with Continue function
- Powerful instruction set
- 512 x 8 ROM, 32 x 4 RAM
- 20 I/O lines (COP410C)
- Two-level subroutine stack
- DC to 4 μs instruction time
- Single supply operation (2.4V to 5.5V)
- General purpose and TRI-STATE® outputs
- Internal binary counter register with MICROWIRE™ compatible serial I/O
- LSTTL/CMOS compatible in and out
- Software/hardware compatible with other members of the COP400 family
- Extended temperature (−40°C to +85°C) devices available
- The military temperature range devices (−55°C to +125°C) are specified on COP210C/211C data sheet.

Block Diagram



TL/DD/5015–1

FIGURE 1. COP410C

COP410C/COP411C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Voltage at Any Pin	−0.3V to V_{CC}+0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $0°C \le T_A \le 70°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (Notes 5, 6)			0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 2.4V, t_c = 125 μs V_{CC} = 5.0V, t_c = 16 μs V_{CC} = 5.0V, t_c = 4 μs (t_c is instruction cycle time)		80 500 2000	μA μA μA
HALT Mode Current (Note 2)	V_{CC} = 5.0V, F_{IN} = 0 kHz V_{CC} = 2.4V, F_{IN} = 0 kHz		30 10	μA μA
Input Voltage Levels RESET, CKI Logic High Logic Low All Other Inputs Logic High Logic Low		 0.9 V_{CC} 0.7 V_{CC}	 0.1 V_{CC} 0.2 V_{CC}	 V V V V
Hi-Z Input Leakage		−1	+1	μA
Input Capacitance (Note 6)			7	pF
Output Voltage Levels LSTTL Operation Logic High Logic Low CMOS Operation Logic High Logic Low	Standard Outputs V_{CC} = 5.0V ±10% I_{OH} = −25 μA I_{OL} = 400 μA I_{OH} = −10 μA I_{OL} = 10 μA	 2.7 V_{CC}−0.2	 0.4 0.2	 V V V V
Output Current Levels (Note 4) (Except CKO) Sink Source (Standard Option) Source (Low Current Option)	 V_{CC} = 4.5V, V_{OUT} = V_{CC} V_{CC} = 2.4V, V_{OUT} = V_{CC} V_{CC} = 4.5V, V_{OUT} = 0V V_{CC} = 2.4V, V_{OUT} = 0V V_{CC} = 4.5V, V_{OUT} = 0V V_{CC} = 2.4V, V_{OUT} = 0V	 1.2 0.2 −0.5 −0.1 −30 −6	 −330 −80	 mA mA mA mA μA μA
CKO Current Levels (As Clock Out) Sink ÷4 ÷8 ÷16 Source ÷4 ÷8 ÷16	 V_{CC} = 4.5V, CKI = V_{CC}, V_{OUT} = V_{CC} V_{CC} = 4.5V, CKI = 0V, V_{OUT} = 0V 	 0.3 0.6 1.2 −0.3 −0.6 −1.2	 	 mA mA mA mA mA mA
Allowable Sink/Source Current Per Pin (Note 4)			5	mA

COP410C/COP411C

DC Electrical Characteristics (Continued)

Parameter	Conditions	Min	Max	Units
Allowable Loading on CKO (as HALT I/O pin)			100	pF
Current Needed to Override HALT[3]				
To Continue	V_{CC} = 4.5V, V_{IN} = 0.2 V_{CC}		0.6	mA
To Halt	V_{CC} = 4.5V, V_{IN} = 0.7 V_{CC}		1.6	mA
TRI-STATE or Open Drain Leakage Current		−2	+2	μA

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 5k resistors. See current drain equation on page 13.

Note 2: The Halt mode will stop CKI from oscillating in the RC and crystal configurations.

Note 3: When forcing HALT, current is only needed for a short time (approximately 200 ns) to flip the HALT flip-flop.

Note 4: SO output sink current must be limited to keep V_{OL} less than 0.2 V_{CC} when part is running in order to prevent entering test mode.

Note 5: Voltage change must be less than 0.5V in a 1 ms period.

Note 6: This parameter is only sampled and not 100% tested.

Note 7: Variation due to the device included.

COP410C/COP411C

AC Electrical Characteristics $0°C \le T_A \le 70°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (t_c)	$V_{CC} \ge 4.5V$	4	DC	μs
	4.5V > $V_{CC} \ge$ 2.4V	16	DC	μs
Operating CKI ÷4 mode Frequency	$V_{CC} \ge 4.5V$	DC	1.0	MHz
÷8 mode	$V_{CC} \ge 4.5V$	DC	2.0	MHz
÷16 mode	$V_{CC} \ge 4.5V$	DC	4.0	MHz
÷4 mode	4.5V > $V_{CC} \ge$ 2.4V	DC	250	kHz
÷8 mode	4.5V > $V_{CC} \ge$ 2.4V	DC	500	kHz
÷16 mode	4.5V > $V_{CC} \ge$ 2.4V	DC	1.0	MHz
Instruction Cycle Time RC Oscillator[7]	R = 30k ± 5%, V_{CC} = 5V C = 82 pF ± 5% (÷4 Mode)	8	16	μs
Duty Cycle[6]	f_I = 4 MHz	40	60	%
Rise Time[6]	f_I = 4 MHz External Clock		60	ns
Fall Time[6]	f_I = 4 MHz External Clock		40	ns
Inputs (See *Figure 3*)				
t_{SETUP} G Inputs	$V_{CC} \ge 4.5V$	tc/4+0.7		μs
t_{SETUP} SI Input	$V_{CC} \ge 4.5V$	0.3		μs
t_{SETUP} All Others	$V_{CC} \ge 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \ge 4.5V$	0.25		μs
	$V_{CC} \ge 2.4V$	1.0		μs
Output Propagation Delay	V_{OUT} = 1.5V, C_L = 100 pF, R_L = 5k			
t_{PD1}, t_{PD0}	$V_{CC} \le 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$V_{CC} \le 2.4V$		4.0	μs

COP310C/COP311C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Voltage at Any Pin	−0.3V to V_{CC}+0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		3.0	5.5V	V
Power Supply Ripple (Notes 5, 6)			0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 3.0V, t_c = 125 μs V_{CC} = 5.0V, t_c = 16 μs V_{CC} = 5.0V, t_c = 4 μs (t_c is instruction cycle time)		100 600 2500	μA μA μA
HALT Mode Current (Note 2)	V_{CC} = 5.0V, F_{IN} = 0 kHz V_{CC} = 3.0V, F_{IN} = 0 kHz		50 20	μA μA
Input Voltage Levels $\overline{RESET}$, CKI Logic High Logic Low All Other Inputs Logic High Logic Low		 0.9 V_{CC} 0.7 V_{CC}	 0.1 V_{CC} 0.2 V_{CC}	 V V V V
Hi-Z Input Leakage		−2	+2	μA
Input Capacitance (Note 6)			7	pF
Output Voltage Levels LSTTL Operation Logic High Logic Low CMOS Operation Logic High Logic Low	Standard Outputs V_{CC} = 5.0V ±10% I_{OH} = −25 μA I_{OL} = 400 μA I_{OH} = −10 μA I_{OL} = 10 μA	 2.7 V_{CC}−0.2 	 0.4 0.2	 V V V V
Output Current Levels (Note 4) (Except CKO) Sink Source (Standard Option) Source (Low Current Option)	 V_{CC} = 4.5V, V_{OUT} = V_{CC} V_{CC} = 3.0V, V_{OUT} = V_{CC} V_{CC} = 4.5V, V_{OUT} = 0V V_{CC} = 3.0V, V_{OUT} = 0V V_{CC} = 4.5V, V_{OUT} = 0V V_{CC} = 3.0V, V_{OUT} = 0V	 1.2 0.2 −0.5 −0.1 −30 −8	 −440 −200	 mA mA mA mA μA μA
CKO Current Levels (As Clock Out) Sink ÷4 ÷8 ÷16 Source ÷4 ÷8 ÷16	 V_{CC} = 4.5V, CKI = V_{CC}, V_{OUT} = V_{CC} V_{CC} = 4.5V, CKI = 0V, V_{OUT} = 0V 	 0.3 0.6 1.2 −0.3 −0.6 −1.2	 	 mA mA mA mA mA mA
Allowable Sink/Source Current Per Pin (Note 4)			5	mA

COP310C/COP311C

DC Electrical Characteristics (Continued)

Parameter	Conditions	Min	Max	Units
Allowable Loading on CKO (as HALT I/O pin)			100	pF
Current Needed to Override HALT[3]				
To Continue	$V_{CC} = 4.5V$, $V_{IN} = 0.2\ V_{CC}$		0.8	mA
To Halt	$V_{CC} = 4.5V$, $V_{IN} = 0.7\ V_{CC}$		2.0	mA
TRI-STATE or Open Drain Leakage Current		−4	+4	μA

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 5k resistors. See current drain equation on page 13.

Note 2: The Halt mode will stop CKI from oscillating in the RC and crystal configurations.

Note 3: When forcing HALT, current is only needed for a short time (approximately 200 ns) to flip the HALT flip-flop.

Note 4: SO output sink current must be limited to keep V_{OL} less than 0.2 V_{CC} when part is running in order to prevent entering test mode.

Note 5: Voltage change must be less than 0.5V in a 1 ms period.

Note 6: This parameter is only sampled and not 100% tested.

Note 7: Variation due to the device included.

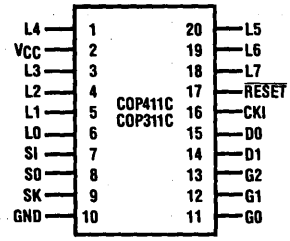
COP310C/COP311C

AC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (t_c)	$V_{CC} \ge 4.5V$	4	DC	μs
	$4.5V > V_{CC} \ge 3.0V$	16	DC	μs
Operating CKI Frequency ÷4 mode	$V_{CC} \ge 4.5V$	DC	1.0	MHz
÷8 mode	$V_{CC} \ge 4.5V$	DC	2.0	MHz
÷16 mode	$V_{CC} \ge 4.5V$	DC	4.0	MHz
÷4 mode	$4.5V > V_{CC} \ge 3.0V$	DC	250	kHz
÷8 mode	$4.5V > V_{CC} \ge 3.0V$	DC	500	kHz
÷16 mode	$4.5V > V_{CC} \ge 3.0V$	DC	1.0	MHz
Instruction Cycle Time RC Oscillator[7]	R = 30k ±5%, V_{CC} = 5V C = 82 pF ±5% (÷4 Mode)	8	16	μs
Duty Cycle[6]	f_I = 4 MHz	40	60	%
Rise Time[6]	f_I = 4 MHz External Clock		60	ns
Fall Time[6]	f_I = 4 MHz External Clock		40	ns
Inputs (See *Figure 3*)				
t_{SETUP} G Inputs	$V_{CC} \ge 4.5V$	tc/4+0.7		μs
t_{SETUP} SI Input	$V_{CC} \ge 4.5V$	0.3		μs
t_{SETUP} All Others	$V_{CC} \ge 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \ge 4.5V$	0.25		μs
	$V_{CC} \ge 3.0V$	1.0		μs
Output Propagation Delay	V_{OUT} = 1.5V, C_L = 100 pF, R_L = 5k			
t_{PD1}, t_{PD0}	$V_{CC} \le 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$V_{CC} \le 3.0V$		4.0	μs

Connection Diagrams

S.O. Wide and DIP



TL/DD/5015-2

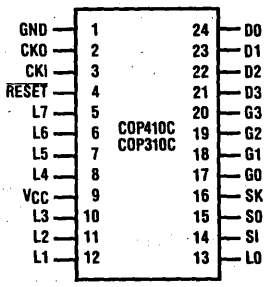
Top View

Order Number COP311C-XXX/D or COP411C-XXX/D
See NS Hermetic Package Number D20A
(Prototype Package Only)

Order Number COP311C-XXX/N or COP411C-XXX/N
See NS Molded Package Number N20A

Order Number COP311C-XXX/WM or
COP411C-XXX/WM
See NS Surface Mount Package Number M20B

S.O. Wide and DIP



TL/DD/5015-3

Top View

Order Number COP310C-XXX/D or COP410C-XXX/D
See NS Hermetic Package Number D24C
(Prototype Package Only)

Order Number COP310C-XXX/N or COP410C-XXX/N
See NS Molded Package Number N24A

Order Number COP310C-XXX/WM or
COP410C-XXX/WM
See NS Surface Mount Package Number M24B

FIGURE 2

Pin Descriptions

Pin	Description	Pin	Description
L_7–L_0	8-bit bidirectional I/O port with TRI-STATE	SK	Logic-controlled clock (or general purpose output)
G_3–G_0	4-bit bidirectional I/O port (G_2–G_0 for 20-pin package)	CKI	System oscillator input
D_3–D_0	4-bit general purpose output port (D_1–D_0 for 20-pin package)	CKO	Crystal oscillator output, or HALT mode I/O port (24-pin package only)
SI	Serial input (or counter input)	$\overline{\text{RESET}}$	System reset input
SO	Serial output (or general purpose output)	V_{CC}	System power supply
		GND	System Ground

Timing Diagram

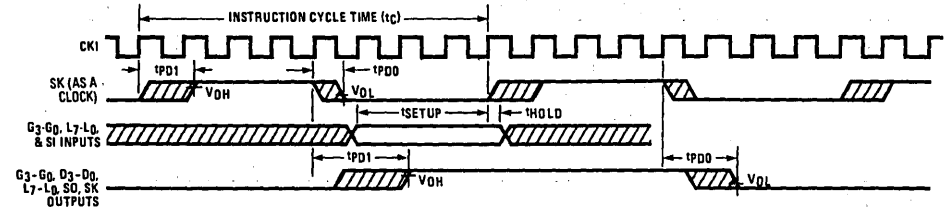


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FIGURE 3. Input/Output (Divide-by-8 Mode)

Functional Description

To ease reading of this description, only COP410C and/or COP411C are referenced; however, all such references apply equally to COP310C and/or COP311C, respectively.

A block diagram of the COP410C is given in *Figure 1.* Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1"; when a bit is reset, it is a logic "0".

PROGRAM MEMORY

Program memory consists of a 512-byte ROM. As can be seen by an examination of the COP410C/411C instruction set, these words may be program instructions, program data, or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, and LQID instructions, ROM must often be thought of as being organized into 8 pages of 64 words (bytes) each.

ROM ADDRESSING

ROM addressing is accomplished by a 9-bit PC register. Its binary value selects one of the 512 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 9-bit binary count value. Two levels of subroutine nesting are implemented by two 9-bit subroutine save registers, SA and SB.

ROM instruction words are fetched, decoded, and executed by the instruction decode, control and skip logic circuitry.

DATA MEMORY

Data Memory consists of a 128-bit RAM, organized as four data registers of 8 × 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper two bits (Br) selects one of four data registers and lower three bits of the 4-bit Bd select one of eight 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the XAD 3, 15 instruction. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

The most significant bit of Bd is not used to select a RAM digit. Hence, each physical digit of RAM may be selected by two different values of Bd as shown in *Figure 4.* The skip condition for XIS and XDS instructions will be true if Bd changes between 0 to 15, but *not* between 7 and 8 (see Table III).

INTERNAL LOGIC

The internal logic of the COP410C/411C is designed to ensure fully static operation of the device.

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Bd portion of the B register, to load four bits of the 8-bit Q latch data and to perform data exchanges with the SIO register.

The 4-bit adder performs the arithmetic and logic functions of the COP410C/411C, storing its results in A. It also outputs the carry information to a 1-bit carry register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description below.)

The G register contents are outputs to four general purpose bidirectional I/O ports.

The Q register is an internal, latched, 8-bit register, used to hold data loaded from RAM and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The eight L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and RAM.

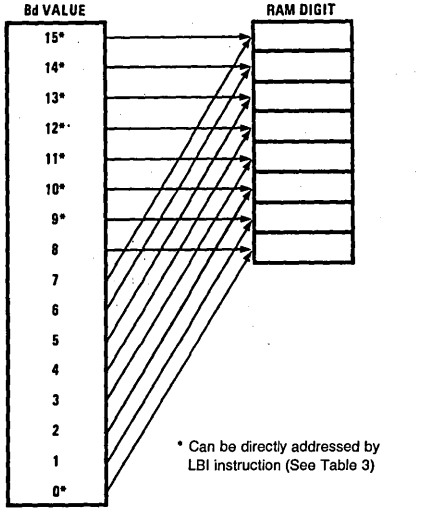

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FIGURE 4. RAM Digit Address to Physical RAM Digit Mapping

Functional Description (Continued)

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter, depending upon the contents of the EN register. (See EN register description below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. With SIO functioning as a serial-in/serial-out shift register and SK as a sync clock, the COP410C/411C is MICROWIRE compatible.

The D register provides four general purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK is a sync clock, inhibited when SKL is a logic "0".

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN3–EN0).

1. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or as a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN3. With EN0 reset, SIO is a serial shift register, shifting left each instruction cycle time. The data present at SI is shifted into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each instruction cycle time. (See 4, below.) The SK output becomes a logic-controlled clock.
2. EN 1 is not used, it has no effect on the COP410C/411C.
3. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN2 disables the L drivers, placing the L I/O ports in a high impedance input state.
4. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected), SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected, disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0".

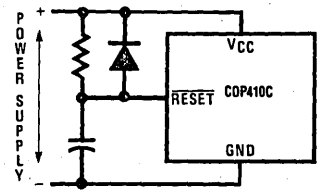
INITIALIZATION

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1 ms and if the operating frequency at CKI is greater than 32 kHz, otherwise the external RC network shown in *Figure 5* must be connected to the $\overline{\text{RESET}}$ pin. The $\overline{\text{RESET}}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{\text{RESET}}$ input, providing it stays low for at least three instruction cycle times.

When V_{CC} power is applied, the internal reset logic will keep the chip in initialization mode for up to 2500 instruction cycles. If the CKI clock is running at a low frequency, this could take a long time, therefore, the internal logic should be disabled by a mask option with initialization controlled solely by $\overline{\text{RESET}}$ pin.

Note: If CKI clock is less than 32 kHz, the internal reset logic (Option 25 = 1) *must* be disabled and the external RC network *must* be present.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. Data memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).



TL/DD/5015–6

RC > 5 × Power Supply Rise Time
and RC > 100 × CKI Period

FIGURE 5. Power-Up Clear Circuit

COP411C

If the COP410C is bonded as a 20-pin package, it becomes the COP411C, illustrated in *Figure 2,* COP410C/411C Connection Diagrams. Note that the COP411C does not contain D2, D3, G3, or CKO. Use of this option, of course, precludes use of D2, D3, G3, and CKO options. All other options are available for the COP411C.

TABLE I. Enable Register Modes — Bits EN0 and EN3

EN0	EN3	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Binary Counter	Input to Counter	0	SK = SKL
1	1	Binary Counter	Input to Counter	1	SK = SKL

Functional Description (Continued)

HALT MODE

The COP410C/411C is a *fully static* circuit; therefore, the user may stop the system oscillator at any time to halt the chip. The chip also may be halted by the HALT instruction or by forcing CKO high when it is used as a HALT I/O port. Once in the HALT mode, the internal circuitry does not receive any clock signal, and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The HALT mode is the minimum power dissipation state.

The HALT mode has slight differences depending upon the type of oscillator used.

a. 1-pin oscillator—RC or external

The HALT mode may be entered into by either program control (HALT instruction) or by forcing CKO to a logic "1" state.

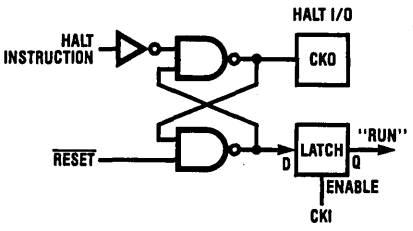
The circuit may be awakened by one of two different methods:

1) Continue function. By forcing CKO to a logic "0", the system clock is re-enabled and the circuit continues to operate from the point where it was stopped.

2) Restart. Forcing the $\overline{\text{RESET}}$ pin to a logic "0" will restart the chip regardless of HALT or CKO (see initialization).

b. 2-pin oscillator—crystal

The HALT mode may be entered into by program control (HALT instruction) which forces CKO to a logic "1" state. The circuit can be awakened only by the $\overline{\text{RESET}}$ function.



Halt I/O Port

CKO Pin Options

In a crystal-controlled oscillator system, CKO is used as an output to the crystal network. CKO will be forced high during the execution of a HALT instruction, thus inhibiting the crystal network. If a 1-pin oscillator system is chosen (RC or external), CKO will be selected as HALT and is an I/O flip-flop which is an indicator of the HALT status. An external signal can override this pin to start and stop the chip. By forcing a high level to CKO, the chip will stop as soon as CKI is high and the CKO output will go high to keep the chip stopped. By forcing a low level to CKO, the chip will continue and CKO output will go low.

All features associated with the CKO I/O pin are available with the 24-pin package only.

OSCILLATOR OPTIONS

There are three options available that define the use of CKI and CKO.

a. Crystal-Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optionally by 8 or 4).

b. External Oscillator. CKI is configured as LSTTL-compatible input accepting an external clock signal. The external frequency is divided by 16 (optionally by 8 or 4) to give the instruction cycle time. CKO is the HALT I/O port.

c. RC-Controlled Oscillator. CKI is configured as a single pin RC-controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is the HALT I/O port.

The RC oscillator is not recommended in systems that require accurate timing or low current. The RC oscillator draws more current than an external oscillator (typically an additional 100 μA at 5V). However, when the part halts, it stops with CKI high and the halt current is at the minimum.

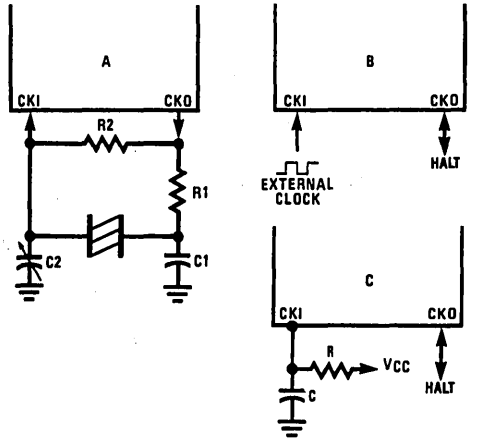


FIGURE 6. COP410C Oscillator

Crystal or Resonator

Crystal Value	Component Value R1	R2	C1 pF	C2 pF
32 kHz	220k	20M	30	5-36
455 kHz	5k	10M	80	40
2.096 MHz	2k	1M	30	6-36
4.0 MHz	1k	1M	30	6-36

RC-Controlled Oscillator

R	C	Cycle Time	V_{CC}
15k	82 pF	4-9 μs	≥4.5V
30k	82 pF	8-16 μs	≥4.5V
47k	100 pF	16-32 μs	2.4 to 4.5
Note: 15k ≤ R ≤ 150k, 50 pf ≤ C ≤ 150 pF			

COP410C/COP411C Instruction Set

Table II is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table III provides the mnemonic, operand, machine code, data flow, skip conditions and description associated with each instruction in the COP410C/411C instruction set.

TABLE II. COP410C/411C Instruction Set Table Symbols

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	9-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	9-bit Subroutine Save Register A
SB	9-bit Subroutine Save Register B
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
r	2-bit Operand Field, 0-3 binary (RAM Register Select)
a	9-bit Operand Field, 0-511 binary (ROM Address)
y	4-bit Operand Field, 0-15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
−	Minus
→	Replaces
↔	Is exchanged with
=	Is equal to
$\overline{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values

TABLE III. COP410C/411C Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	|0011|0000|	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	|0011|0001|	A + RAM(B) → A	None	Add RAM to A
AISC	y	5−	|0101| y |	A + y → A	Carry	Add immediate, Skip on Carry (y ≠ 0)
CLRA		00	|0000|0000|	0 → A	None	Clear A
COMP		40	|0100|0000|	$\overline{A}$ → A	None	One's complement of A to A
NOP		44	|0100|0100|	None	None	No Operation
RC		32	|0011|0010|	"0" → C	None	Reset C
SC		22	|0010|0010|	"1" → C	None	Set C
XOR		02	|0000|0010|	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A

Instruction Set (Continued)

TABLE III. COP410C/411C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111 | 1111	ROM (PC_8, A,M) → $PC_{7:0}$	None	Jump Indirect (Note 2)
JMP	a	6–	0110 | 000 | a_8	a → PC	None	Jump
		–	$a_{7:0}$			
JP	a	–	1 | $a_{6:0}$ (pages 2,3 only)	a → $PC_{6:0}$	None	Jump within Page (Note 1)
			or			
		–	11 | $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	–	10 | $a_{5:0}$	PC + 1 → SA → SB 010 → $PC_{8:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 2)
JSR	a	6–	0110 | 100 | a_8	PC + 1 → SA → SB a → PC	None	Jump to Subroutine
		–	$a_{7:0}$			
RET		48	0100 | 1000	SB → SA → PC	None	Return from Subroutine
RETSK		49	0100 | 10011	SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33	0011 | 0011		None	Halt processor
		38	0011 | 1000			
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33	0011 | 0011	A → $Q_{7:4}$ RAM(B) → $Q_{3:0}$	None	Copy A, RAM to Q
		3C	0011 | 1100			
CQMA		33	0011 | 0011	$Q_{7:4}$ → RAM(B) $Q_{3:0}$ → A	None	Copy Q to RAM, A
		2C	0010 | 1100			
LD	r	–5	00 | r | 0101	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A Exclusive-OR Br with r
LQID		BF	1011 | 1111	ROM(PC_8,A,M) → Q SA → SB	None	Load Q Indirect
RMB	0	4C	0100 | 1100	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	0100 | 0101	0 → $RAM(B)_1$		
	2	42	0100 | 0010	0 → $RAM(B)_2$		
	3	43	0100 | 0011	0 → $RAM(B)_3$		
SMB	0	4D	0100 | 1101	1 → $RAM(B)_0$	None	Set RAM Bit
	1	47	0100 | 0111	1 → $RAM(B)_1$		
	2	46	0100 | 0110	1 → $RAM(B)_2$		
	3	4B	0100 | 1011	1 → $RAM(B)_3$		
STII	y	7–	0111 | y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	–6	00 | r | 0110	RAM(B) ⟷ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	3,15	23	0010 | 0011	RAM(3,15) ⟷ A	None	Exchange A with RAM (3,15)
		BF	1011 | 1111			

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Instruction Set (Continued)

TABLE III. COP410C/411C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS (Continued)						
XDS	r	−7	00 | r | 0111	RAM(B) ⟷ A Bd − 1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd Exclusive-OR Br with r
XIS	r	−4	00 | r | 0100	RAM(B) ⟷ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101 | 0000	A → Bd	None	Copy A to Bd
CBA		4E	0100 | 1110	Bd → A	None	Copy Bd to A
LBI	r,d	–	00 | r | (d − 1) (d = 0,9:15)	r,d → B	Skip until not a LBI	Load B Immediate with r,d
LEI	y	33 6–	0011 | 0011 0010 | y	y → EN	None	Load EN Immediate
TEST INSTRUCTIONS						
SKC		20	0010 | 0000		C = "1"	Skip if C is True
SKE		21	0010 | 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0011 | 0011 0010 | 0001		$G_{3:0} = 0$	Skip if G is Zero (all 4 bits)
SKGBZ		33	0011 | 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 | 0001	2nd byte	$G_0 = 0$	
	1	11	0001 | 0001	2nd byte	$G_1 = 0$	
	2	03	0000 | 0011	2nd byte	$G_2 = 0$	
	3	13	0010 | 0011	2nd byte	$G_3 = 0$	
SKMBZ	0	01	0000 | 0001		$RAM(B)_0 = 0$	Skip if RAM Bit is Zero
	1	11	0001 | 0001		$RAM(B)_1 = 0$	
	2	03	0000 | 0011		$RAM(B)_2 = 0$	
	3	13	0001 | 0011		$RAM(B)_3 = 0$	
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0011 | 0011 0010 | 1010	G → A	None	Input G Ports to A
INL		33 2E	0011 | 0011 0010 | 1110	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM, A
OBD		33 3E	0011 | 0011 0011 | 1110	Bd → D	None	Output Bd to D Outputs
OMG		33 3A	0011 | 0011 0011 | 1010	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0100 | 1111	A ⟷ SIO, C → SKL	None	Exchange A with SIO

Note 1: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 2: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Description of Selected Instructions

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing COP410C/411C programs.

XAS INSTRUCTION

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register). If SIO is selected as a shift register, an XAS instruction must be performed once every four instruction cycle times to effect a continuous data stream.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower eight bits of the ROM address register PC with the contents of ROM addressed by the 9-bit word, PC_8, A, M. PC_8 is not affected by this instruction.

Note: JID uses two instruction cycles if executed, one if skipped.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 9-bit word PC_8, A, M. LQID can be used for table look-up or code conversion such as BCD to 7-segment. The LQID instruction "pushes" the stack (PC + 1 $\rightarrow$ SA $\rightarrow$ SB) and replaces the least significant eight bits of the PC as follows: A $\rightarrow$ $PC_{7:4}$, RAM(B) $\rightarrow$ $PC_{3:0}$, leaving PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SB $\rightarrow$ SA $\rightarrow$ PC), restoring the saved value of the PC to continue sequential program execution. Since LQID pushes SA $\rightarrow$ SB, the previous contents of SB are lost.

Note: LQID uses two instruction cycles if executed, one if skipped.

INSTRUCTION SET NOTES

a. The first word of a COP410C/411C program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths take the same number of cycle times whether instructions are skipped or executed (except JID and LQID).

c. The ROM is organized into eight pages of 64 words each. The program counter is a 9-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: A JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word in page 3 or 7 will access data in the next group of four pages.

POWER DISSIPATION

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, to minimize power consumption, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to ensure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal- or resonator-generated clock will draw additional current. An RC oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate the COP410C current drain.

$$Ic = Iq + (V \times 20 \times Fi) + (V \times 1280 \times FI/Dv)$$

where Ic = chip current drain in microamps
Iq = quiescent leakage current (from curve)
FI = CKI frequency in megahertz
V = chip V_{CC} in volts
Dv = divide by option selected

For example, at 5V V_{CC} and 400 kHz (divide by 4),

$$Ic = 10 + (5 \times 20 \times 0.4) + (5 \times 1280 \times 0.4/4)$$

$$Ic = 10 + 40 + 640 = 690\ \mu A$$

I/O OPTIONS

COP410C/411C outputs have the following optional configurations, illustrated in *Figure 7*:

a. Standard. A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b. Low Current. This is the same configuration as (a) above except that the sourcing current is much less.

c. Open Drain. An N-channel device to ground only, allowing external pull-up as required by the user's application.

d. Standard TRI-STATE L Output. A CMOS output buffer similar to (a) which may be disabled by program control.

e. Low-Current TRI-STATE L Output. This is the same as (d) above except that the sourcing current is much less.

f. Open-Drain TRI-STATE L Output. This has the N-channel device to ground only.

The SI and $\overline{\text{RESET}}$ inputs are Hi-Z inputs (*Figure 7g*).

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available: Select the low-current output option. Now, by setting the output registers to a logic "1" level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion, the Q registers must be set to a logic "1" level and the L drivers *must be enabled* by an LEI instruction.

Functional Description (Continued)

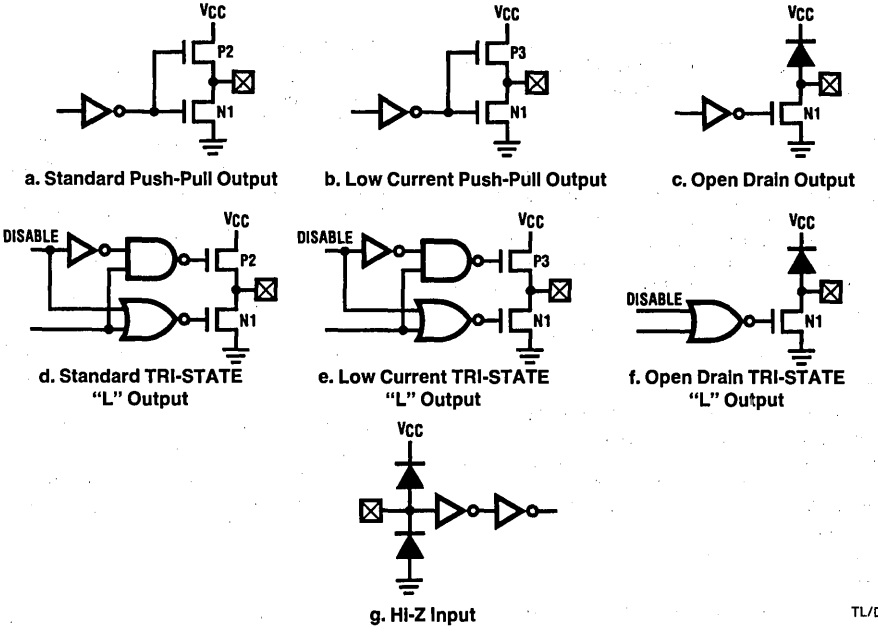

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FIGURE 7. I/O Configurations

Typical Performance Characteristics

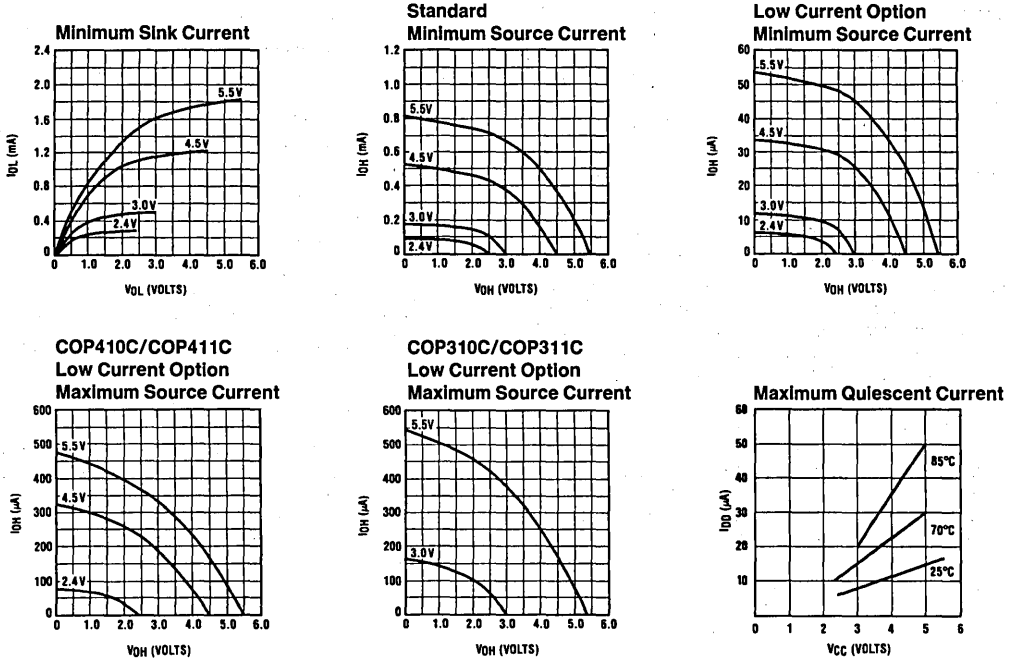

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FIGURE 8

All output drivers uses one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 8* for each of these devices to allow the designer to effectively use these I/O configurations.

Option List

The COP410C/411C mask-programmable options are assigned numbers which correspond with the COP410C pins.

The following is a list of COP410C options. When specifying a COP411 chip, options 20, 21, and 22 must be set to 0. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1: 0 = Ground Pin. No options available.

Option 2: CKO I/O Port. (Determined by Option 3.)
= 0: No option.
(a. is crystal oscillator output for two pin oscillator.
b. is HALT I/O for one pin oscillator.)

Option 3: CKI Input.
= 0: Crystal-controlled oscillator input (÷ 4).
= 1: Single-pin RC-controlled oscillator (÷ 4).
= 2: External oscillator input (÷ 4).
= 3: Crystal oscillator input (÷ 8).
= 4: External oscillator input (÷ 8).
= 5: Crystal oscillator input (÷ 16).
= 6: External oscillator input (÷ 16).

Option 4: $\overline{\text{RESET}}$ Input = 1: Hi-Z input. No option available.

Option 5: L_7 Driver
= 0: Standard TRI-STATE push-pull output.
= 1: Low-current TRI-STATE push-pull output.
= 2: Open-drain TRI-STATE output.

Option 6: L_6 Driver. (Same as Option 5.)

Option 7: L_5 Driver. (Same as Option 5.)

Option 8: L_4 Driver. (Same as Option 5.)

Option 9: V_{CC} Pin = 0 no option.

Option 10: L_3 Driver. (Same as Option 5.)

Option 11: L_2 Driver. (Same as Option 5.)

Option 12: L_1 Driver. (Same as Option 5.)

Option 13: L_0 Driver. (Same as Option 5.)

Option 14: SI Input.
No option available.
= 1: Hi-Z input.

Option 15: SO Output.
= 0: Standard push-pull output.
= 1: Low-current push-pull output.
= 2: Open-drain output.

Option 16: SK Driver. (Same as Option 15.)

Option 17: G_0 I/O Port. (Same as Option 15.)

Option 18: G_1 I/O Port. (Same as Option 15.)

Option 19: G_2 I/O Port. (Same as Option 15.)

Option 20: G_3 I/O Port. (Same as Option 15.)

Option 21: D_3 Output. (Same as Option 15.)

Option 22: D_2 Output. (Same as Option 15.)

Option 23: D_1 Output. (Same as Option 15.)

Option 24: D_0 Output. (Same as Option 15.)

Option 25: Internal Initialization Logic.
= 0: Normal operation.
= 1: No internal initialization logic.

Option 26: No option available.

Option 27: COP Bonding
= 0: COP410C (24-pin device).
= 1: COP411C (20-pin device). See note.
= 2: COP410C and COP411C. See note.

Note: If opt. #27 = 1 or 2 then opt #20 must = 0.

Option Table

Please fill out a photocopy of the option table and send it along with your EPROM.

Option Table

Option 1 Value =	0	is: Ground Pin	
Option 2 Value =	0	is: CKO Pin	
Option 3 Value =		is: CKI Input	
Option 4 Value =	1	is: $\overline{\text{RESET}}$ Input	
Option 5 Value =		is: L_7 Driver	
Option 6 Value =		is: L_6 Driver	
Option 7 Value =		is: L_5 Driver	
Option 8 Value =		is: L_4 Driver	
Option 9 Value =	0	is: V_{CC} Pin	
Option 10 Value =		is: L_3 Driver	
Option 11 Value =		is: L_2 Driver	
Option 12 Value =		is: L_1 Driver	
Option 13 Value =		is: L_0 Driver	
Option 14 Value =	1	is: SI Input	
Option 15 Value =		is: SO Output	
Option 16 Value =		is: SK Driver	
Option 17 Value =		is: G_0 I/O Port	
Option 18 Value =		is: G_1 I/O Port	
Option 19 Value =		is: G_2 I/O Port	
Option 20 Value =		is: G_3 I/O Port	
Option 21 Value =		is: D_3 Output	
Option 22 Value =		is: D_2 Output	
Option 23 Value =		is: D_1 Output	
Option 24 Value =		is: D_0 Output	
Option 25 Value =		is: Internal Initialization Logic	
Option 26 Value =	0	is: N/A	
Option 27 Value =		is: COP Bonding	

National Semiconductor

COP413C/COP413CH/COP313C/COP313CH Single-Chip CMOS Microcontrollers

General Description

The COP413C, COP413CH, COP313C, and COP313CH fully static, single-chip CMOS microcontrollers are members of the COPS™ family, fabricated using double-poly, silicon-gate CMOS technology. These controller-oriented processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, with an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, and BCD data manipulation. The COP413CH is identical to the COP413C except for operating voltage and frequency. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide a customized controller-oriented processor at a low end-product cost.

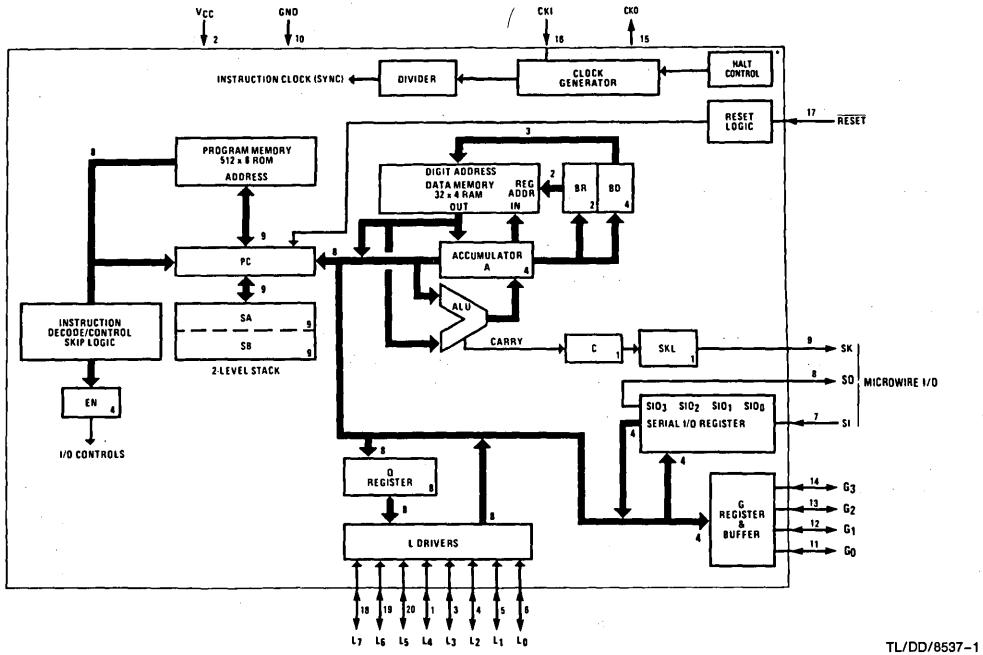
The COP313C/COP313CH is the extended temperature range version of the COP413C/COP413CH.

For emulation use the ROMless COP404C.

Features

- Lowest power dissipation (40 μW typical)
- Low cost
- Power-saving HALT Mode
- Powerful instruction set
- 512 x 8 ROM, 32 x 4 RAM
- 15 I/O lines
- Two-level subroutine stack
- DC to 4 μs instruction time
- Single supply operation (3V to 5.5V)
- General purpose and TRI-STATE® outputs
- Internal binary counter register with MICROWIRE™ compatible serial I/O
- Software/hardware compatible with other members of the COP400 family
- Extended temperature (−40°C to +85°C) devices available

Block Diagram



TL/DD/8537-1

FIGURE 1. COP413C/413CH

COP413C/COP413CH

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Conditions	COP413C		COP413CH		Units
		Min	Max	Min	Max	
Operating Voltage		3.0	5.5	4.5	5.5	V
Power Supply Ripple (Notes 4, 5)			0.1 V_{CC}		0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 5.0V, t_c = Min V_{CC} = 3.0V, t_c = Min (t_c is inst. cycle)		500 300		2000	µA µA
HALT Mode Current (Note 2)	V_{CC} = 5.0V, F_I = 0 kHz V_{CC} = 3.0V, F_I = 0 kHz		30 10		30	µA µA
Input Voltage Levels $\overline{RESET}$, CKI Logic High Logic Low All Other Inputs Logic High Logic Low		 0.9 V_{CC} 0.7 V_{CC} 	 0.1 V_{CC} 0.2 V_{CC}	 0.9 V_{CC} 0.7 V_{CC} 	 0.1 V_{CC} 0.2 V_{CC}	 V V V V
$\overline{RESET}$, SI Input Leakage		−1	+1	−1	+1	µA
Input Capacitance (Notes 5, 6)			7		7	pF
Output Voltage Levels (SO, SK, L Port) Logic High Logic Low	 I_{OH} = −10 µA I_{OL} = 10 µA	 V_{CC} − 0.2 	 0.2	 V_{CC} − 0.2 	 0.2	 V V
Output Current Levels Sink (Note 3) Source (SO, SK, L Port) Source (G Port)	 V_{CC} = Min, V_{OUT} = V_{CC} V_{CC} = Min, V_{OUT} = 0V V_{CC} = Min, V_{OUT} = 0V	 0.2 −0.1 −8	 −150	 1.2 −0.5 −30	 −330	 mA mA µA
Allowable Sink/Source Current Per Pin (Note 3)			5		5	mA
TRI-STATE Leakage Current		−2	+2	−2	+2	µA

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COP413C/COP413CH

AC Electrical Characteristics $0°C \leq T_A \leq 70°C$ unless otherwise specified

Parameter	Conditions	COP413C		COP413CH		Units
		Min	Max	Min	Max	
Instruction Cycle Time		16	DC	4	DC	μs
Operating CKI Frequency	÷8 Mode	DC	500	DC	2000	kHz
Instruction Cycle Time RC Oscillator ÷ 4	R = 30k ±5%, V_{CC} = 5V C = 82 pF ± 5%			8	16	μs
Instruction Cycle Time RC Oscillator ÷ 4 (Note 6)	R = 56k ±5%, V_{CC} = 5V C = 100 pF ± 5%	16	32	16	32	μs
Duty Cycle (Note 5)	Fi = Max freq ext clk	40	60	40	60	%
Rise Time (Note 5)	Fi = Max freq ext clk		60		60	ns
Fall Time (Note 5)	Fi = Max freq ext clk		40		40	ns
Inputs (See *Figure 3*)						
t_{SETUP}	G Inputs	tc/4 + 2.8		tc/4 + 0.7		μs
	SI Input	1.2		0.3		μs
	L Inputs	6.8		1.7		μs
t_{HOLD}		1.0		0.25		μs
Output Propagation Delay t_{PD1}, t_{PD0}	V_{OUT} = 1.5, C_L = 100 pF R_L = 5k		4.0		1.0	μs

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled to V_{CC} with 5k resistors.

Note 2: The Halt mode will stop CKI from oscillating.

Note 3: SO output sink current must be limited to keep V_{OL} less tha 0.2 V_{CC} when part is running in order to prevent entering test mode.

Note 4: Voltage change must be less than 0.5V in a 1 ms period.

Note 5: This parameter is only sampled and not 100% tested.

Note 6: Variation due to the device included.

COP313C/COP313CH

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	COP313C		COP313CH		Units
		Min	Max	Min	Max	
Operating Voltage		3.0	5.5	4.5	5.5	V
Power Supply Ripple (Notes 4, 5)			0.1 V_{CC}		0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 5.0V, t_c = Min V_{CC} = 3.0V, t_c = Min (t_c is inst. cycle)		600 360		2500	μA μA
Halt Mode Current (Note 2)	V_{CC} = 5.0V, Fi = 0 kHz V_{CC} = 3.0V, Fi = 0 kHz		50 20		50	μA μA
Input Voltage Levels RESET, CKI Logic High Logic Low All Other Inputs Logic High Logic Low		 0.9 V_{CC} 0.7 V_{CC}	 0.1 V_{CC} 0.2 V_{CC}	 0.9 V_{CC} 0.7 V_{CC}	 0.1 V_{CC} 0.2 V_{CC}	 V V V V
RESET, SI Input Leakage		−2	+2	−2	+2	μA
Input Capacitance (Notes 5, 6)			7		7	pF
Output Voltage Levels (SO, SK, L Port) Logic High Logic Low	 I_{OH} = −10 μA I_{OL} = 10 μA	 V_{CC} − 0.2	 0.2	 V_{CC} − 0.2	 0.2	 V V
Output Current Levels Sink (Note 3) Source (SO, SK, L Port) Source (G Port)	 V_{CC} = Min, V_{OUT} = V_{CC} V_{CC} = Min, V_{OUT} = 0V V_{CC} = Min, V_{OUT} = 0V	 0.2 −0.1 −8	 −200	 1.2 −0.5 −30	 −440	 mA mA μA
Allowable Sink/Source Current Per Pin (Note 3)			5		5	mA
TRI-STATE Leakage Current (Note 3)		−4	+4	−4	+4	μA

COP313C/COP313CH

AC Electrical Characteristics $-40°C \leq T_A \leq +85°C$ unless otherwise specified

Parameter	Conditions	COP313C		COP313CH		Units
		Min	Max	Min	Max	
Instruction Cycle Time		16	DC	4	DC	μs
Operating CKI Frequency	÷ 8 Mode	DC	500	DC	2000	kHz
Instruction Cycle Time RC Oscillator ÷ 4	R = 30k ±5%, V_{CC} = 5V C = 82 pF ± 5%			8	16	μs
Instruction Cycle Time RC Oscillator ÷ 4 (Note 6)	R = 56k ±5%, V_{CC} = 5V C = 100 pF ± 5%	16	32	16	32	μs
Duty Cycle (Note 5)	Fi = Max Freq Ext Clk	40	60	40	60	%
Rise Time (Note 5)	Fi = Max Freq Ext Clk		60		60	ns
Fall Time (Note 5)	Fi = Max Freq Ext Clk		40		40	ns
Inputs (See *Figure 3*)						
t_{SETUP}	G Inputs	tc/4 + 2.8		tc/4 + 0.7		μs
	SI Input	1.2		0.3		μs
	L Inputs	6.8		1.7		μs
t_{HOLD}		1.0		0.25		μs
Output Propagation Delay t_{PD1}, t_{PD0}	V_{OUT} = 1.5V, C_L = 100 pF R_L = 5k		4.0		1.0	μs

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 5k resistors. See current drain equation on page 13.

Note 2: The Halt mode will stop CKI from oscillating.

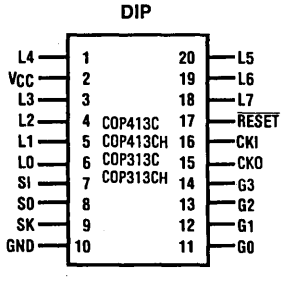
Note 3: SO output sink current must be limited to keep V_{OL} less than 0.2 V_{CC} when part is running in order to prevent entering test mode.

Note 4: Voltage change must be less than 0.5V in a 1 ms period.

Note 5: This parameter is only sampled and not 100% tested.

Note 6: Variation due to the device included.

Connection Diagram



Top View

Pin Descriptions

Pin	Description
L_7–L_0	8-bit bidirectional I/O port with TRI-STATE
G_3–G_0	4-bit bidirectional I/O port
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	Crystal oscillator output, or NC
$\overline{RESET}$	System reset input
V_{CC}	System power supply
GND	System Ground

FIGURE 2

Order Number COP313C-XXX/D, COP313CH-XXX/D, COP413C-XXX/D or COP413CH-XXX/D
See NS Hermetic Package Number D20A

Order Number COP313C-XXX/N, COP313CH-XXX/N, COP413C-XXX/N or COP413CH-XXX/N
See NS Molded Package Number N20A

Order Number COP313C-XXX/WM or COP413C-XXX/WM
See NS Small Outline Package Number M20B

Timing Waveform

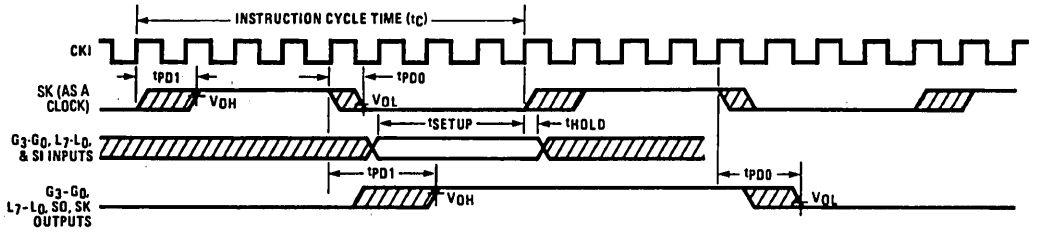


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FIGURE 3. Input/Output Timing Diagrams (Divide-by-8 Mode)

Development Support

The MOLE (Microcontroller On Line Emulator) is a low cost development system and real time emulator for COPS' products. They also include TMP, 8050 and the new 16 bit HPC microcontroller family. The MOLE provides effective support for the development of both software and hardware in the user's application.

The purpose of the MOLE is to provide a tool to write and assemble code, emulate code for the target microcontroller and assist in debugging of the system.

The MOLE can be connected to various hosts, IBM PC, STARPLEX™, Kaypro, Apple and Intel systems, via RS-232 port. This link facilitates the up loading/down loading of code, supports host assembly and mass storage.

The MOLE consists of three parts; brain, personality and optional host software.

The brain board is the computing engine of the system. It is a self-contained computer with its own firmware which provides for all system operation, emulation control, communication, from programming and diagnostic operation. It has three serial ports which can be connected to a terminal, host system, printer, modem or to other MOLE's in a multi-MOLE environment.

The personality board contains the necessary hardware and firmware needed to emulate the target microcontroller. The emulation cable which replaces the target controller attaches to this board. The software contains a cross assembler and a communications program for up loading and down loading code from the MOLE.

MOLE Ordering Information

P/N	Description
MOLE-BRAIN	MOLE Computer Board
MOLE-COPS-PB1	COPS Personality Board
MOLE-XXX-YYY	Optional Software

Where XXX = COPS
YYY = Host System, IBM, Apple, KAY (Kaypro), CP/M

Functional Description

To ease reading of this description, only COP413C is referenced; however, all such references apply equally to COP413CH, COP313C, and COP313CH.

A block diagram of the COP413C is given in *Figure 1.* Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1"; when a bit is reset, it is a logic "0".

PROGRAM MEMORY

Program memory consists of a 512-byte ROM. As can be seen by an examination of the COP413C instruction set, these words may be program instructions, program data, or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, and LQID instructions, ROM must often be thought of as being organized into 8 pages of 64 words (bytes) each.

ROM ADDRESSING

ROM addressing is accomplished by a 9-bit PC register. Its binary value selects one of the 512 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 9-bit binary count value. Two levels of subroutine nesting are implemented by two 9-bit subroutine save registers, SA and SB.

ROM instruction words are fetched, decoded, and executed by the instruction decode, control and skip logic circuitry.

DATA MEMORY

Data Memory consists of a 128-bit RAM, organized as four data registers of 8 × 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper two bits (Br) selects one of four data registers and lower three bits of the 4-bit Bd select one of eight 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the XAD 3, 15 instruction.

The most significant bit of Bd is not used to select a RAM digit. Hence, each physical digit of RAM may be selected by two different values of Bd as shown in *Figure 4.* The skip condition for XIS and XDS instructions will be true if Bd changes between 0 to 15, but *not* between 7 and 8 (see Table III).

INTERNAL LOGIC

The internal logic of the COP413C is designed to ensure fully static operation of the device.

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Bd portion of the B register, to load four bits of the 8-bit Q latch data and to perform data exchanges with the SIO register.

The 4-bit adder performs the arithmetic and logic functions of the COP413C, storing its results in A. It also outputs the carry information to a 1-bit carry register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description below.)

The G register contents are outputs to four general purpose bidirectional I/O ports.

The Q register is an internal, latched, 8-bit register, used to hold data loaded from RAM and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The eight L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and RAM.

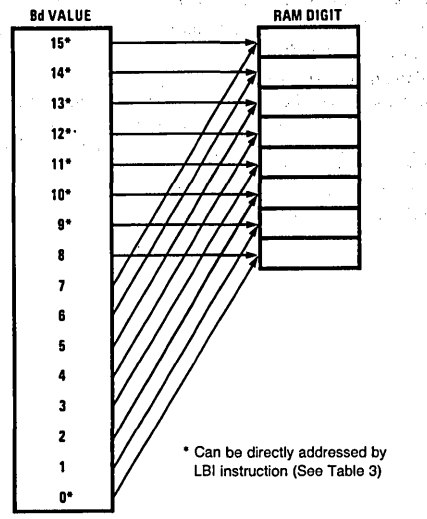

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FIGURE 4. RAM Digit Address to Physical RAM Digit Mapping

Functional Description (Continued)

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter, depending upon the contents of the EN register. (See EN register description below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. With SIO functioning as a serial-in/serial-out shift register and SK as a sync clock, the COP413C is MICROWIRE compatible.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK is a sync clock, inhibited when SKL is a logic "0".

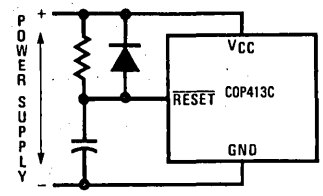
The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN3–EN0).

1. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or as a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN3. With EN0 reset, SIO is a serial shift register, shifting left each instruction cycle time. The data present at SI is shifted into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each instruction cycle time. (See 4, below.) The SK output becomes a logic-controlled clock.
2. EN 1 is not used, it has no effect on the COP413C.
3. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN2 disables the L drivers, placing the L I/O ports in a high impedance input state.
4. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected), SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected, disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0".

INITIALIZATION

The external RC network shown in *Figure 5* must be connected to the $\overline{\text{RESET}}$ pin. The $\overline{\text{RESET}}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{\text{RESET}}$ input, providing it stays low for at least three instruction cycle times.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. Data memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).



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RC > 5 × Power Supply Rise Time
and RC > 100 × CKI Period

FIGURE 5. Power-Up Clear Circuit

TABLE I. Enable Register Modes—Bits EN0 and EN3

EN0	EN3	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Binary Counter	Input to Counter	0	SK = SKL
1	1	Binary Counter	Input to Counter	1	SK = SKL

Functional Description (Continued)

HALT MODE

The COP413C is a *fully static* circuit; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may be halted by the HALT instruction. Once in the HALT mode, the internal circuitry does not receive any clock signal, and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The HALT mode is the minimum power dissipation state.

The HALT mode may be entered into by program control (HALT instruction) which forces CKO to a logic "1" state. The circuit can be awakened only by the $\overline{\text{RESET}}$ function.

POWER DISSIPATION

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, to minimize power consumption, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to ensure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal- or resonator-generated clock will draw more than a square-wave input. An RC oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate the COP413C current drain.

$Ic = Iq + (V \times 20 \times Fi) + (V \times 1280 \times Fl/Dv)$

where Ic = chip current drain in microamps

Iq = quiescent leakage current (from curve)

Fl = CKI frequency in megahertz

V = chip V_{CC} in volts

Dv = divide by option selected

For example, at 5V V_{CC} and 400 kHz (divide by 8),

$Ic = 30 + (5 \times 20 \times 0.4) + (5 \times 1280 \times 0.4/8)$

$Ic = 30 + 40 + 320 = 390\ \mu A$

OSCILLATOR OPTIONS

There are two options available that define the use of CKI and CKO.

a. Cyrstal-Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 8.

b. RC-Controlled Oscillator. CKI is configured as a single pin RC-controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is NC.

The RC oscillator is not recommended in systems that require accurate timing or low current. The RC oscillator draws more current than an external oscillator (typically an additional 100 μA at 5V). However, when the part halts, it stops with CKI high and the halt current is at the minimum.

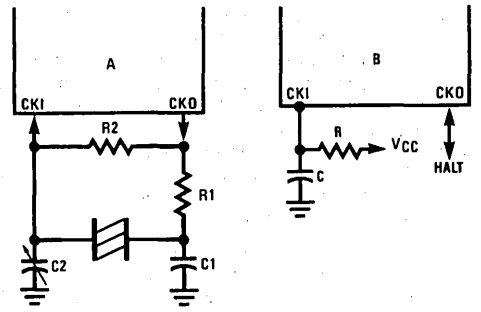

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FIGURE 6. COP413C Oscillator

Crystal or Resonator					RC-Controlled Oscillator			
Crystal Value	Component Value R1	R2	C1 pF	C2 pF	R	C	Cycle Time	V_{CC}
32 kHz	220k	20M	30	5–36	15k	82 pF	4–9 μs	≥ 4.5V COP413CH Only
455 kHz	5k	10M	80	40	30k	82 pF	8–16 μs	≥ 4.5V COP413CH Only
2.000 MHz	2k	1M	30	6–36	47k	100 pF	16–32 μs	3.0 to 4.5V COP413C Only
					56k	100 pF	16–32 μs	≥ 4.5V
					Note: 15k ≤ R ≤ 150k, 50 pF ≤ C ≤ 150 pF			

Functional Description (Continued)

I/O CONFIGURATIONS

COP413C outputs have the following configurations, illustrated in *Figure 7*:

a. Standard SO, SK Output. A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

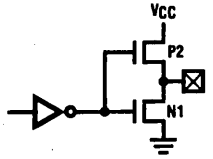
b. Low Current G Output. This is the same configuration as (a) above except that the sourcing current is much less.

c. Standard TRI-STATE L Output. L output is a CMOS output buffer similar to (a) which may be disabled by program control.

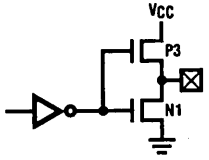
The SI and $\overline{\text{RESET}}$ inputs are Hi-Z inputs (*Figure 7d*).

When using the G I/O port as an input, set the output register to a logic "1" level. The P-channel device will act as a pull-up load. When using the L I/O port as an input, disable the L drivers with the LEI instruction. The drivers are then in TRI-STATE mode and can be driven externally.

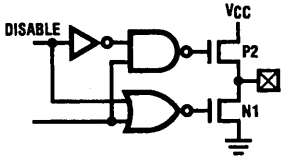
All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 8* for each of these devices to allow the designer to effectively use these I/O configurations.



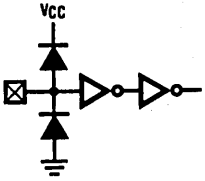
a. Standard Push-Pull Output



b. Low Current Push-Pull Output



c. Standard TRI-STATE "L" Output



d. Hi-Z Input

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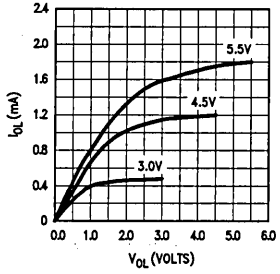
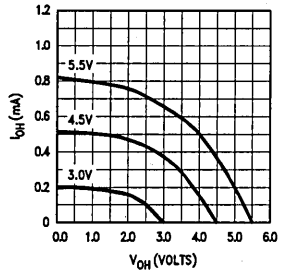
FIGURE 7. I/O Configurations

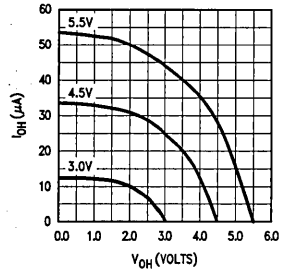
SO, SK, L Port, G Port Minimum Sink Current



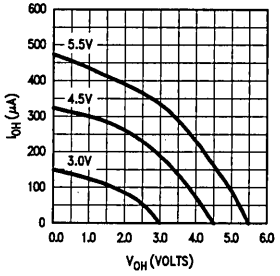
SO, SK, L Port Standard Minimum Source Current



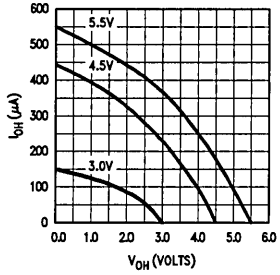
G Port Low Current Minimum Source Current



COP413C/COP413CH Low Current G Port Maximum Source Current



COP313C/COP313CH Low Current G Port Maximum Source Current



Maximum Quiescent Current

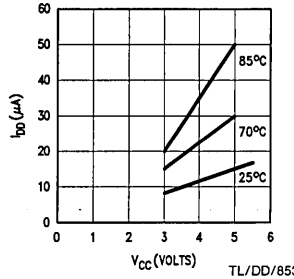


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FIGURE 8

COP413C Instruction Set

Table II is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table III provides the mnemonic, operand, machine code, data flow, skip conditions and description associated with each instruction in the COP413C instruction set.

TABLE II. COP413C Instruction Set Table Symbols

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	9-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	9-bit Subroutine Save Register A
SB	9-bit Subroutine Save Register B
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0–15 binary (RAM Digit Select)
r	2-bit Operand Field, 0–3 binary (RAM Register Select)
a	9-bit Operand Field, 0–511 binary (ROM Address)
y	4-bit Operand Field, 0–15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
−	Minus
→	Replaces
↔	Is exchanged with
=	Is equal to
$\overline{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values

TABLE III. COP413C Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011 | 0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0011 | 0001	A + RAM(B) → A	None	Add RAM to A
AISC	y	5–	0101 | y	A + y → A	Carry	Add immediate, Skip on Carry (y ≠ 0)
CLRA		00	0000 | 0000	0 → A	None	Clear A
COMP		40	0100 | 0000	$\overline{A}$ → A	None	One's complement of A to A
NOP		44	0100 | 0100	None	None	No Operation
RC		32	0011 | 0010	"0" → C	None	Reset C
SC		22	0010 | 0010	"1" → C	None	Set C
XOR		02	0000 | 0010	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A

COP413C Instruction Set (Continued)

TABLE III. COP413C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111 | 1111	ROM (PC_8, A,M) → $PC_{7:0}$	None	Jump Indirect (Note 2)
JMP	a	6–	0110 | 000 | a_8	a → PC	None	Jump
		–	$a_{7:0}$			
JP	a	–	1 | $a_{6:0}$ (pages 2, 3 only)	a → $PC_{6:0}$	None	Jump within Page (Note 1)
			or			
		–	11 | $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	–	10 | $a_{5:0}$	PC + 1 → SA → SB	None	Jump to Subroutine Page (Note 2)
				010 → $PC_{8:6}$ a → $PC_{5:0}$		
JSR	a	6–	0110 | 100 | a_8	PC + 1 → SA → SB	None	Jump to Subroutine
		–	$a_{7:0}$	a → PC		
RET		48	0100 | 1000	SB → SA → PC	None	Return from Subroutine
RETSK		49	0100 | 10011	SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33	0011 | 0011		None	Halt processor
		38	0011 | 1000			
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33	0011 | 0011	A → $Q_{7:4}$	None	Copy A, RAM to Q
		3C	0011 | 1100	RAM(B) → $Q_{3:0}$		
CQMA		33	0011 | 0011	$Q_{7:4}$ → RAM(B)	None	Copy Q to RAM, A
		2C	0010 | 1100	$Q_{3:0}$ → A		
LD	r	–5	00 | r | 0101	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A Exclusive-OR Br with r
LQID		BF	1011 | 1111	ROM(PC_8,A,M) → Q SA → SB	None	Load Q Indirect
RMB	0	4C	0100 | 1100	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	0100 | 0101	0 → $RAM(B)_1$		
	2	42	0100 | 0010	0 → $RAM(B)_2$		
	3	43	0100 | 0011	0 → $RAM(B)_3$		
SMB	0	4D	0100 | 1101	1 → $RAM(B)_0$	None	Set RAM Bit
	1	47	0100 | 0111	1 → $RAM(B)_1$		
	2	46	0100 | 0110	1 → $RAM(B)_2$		
	3	4B	0100 | 1011	1 → $RAM(B)_3$		
STII	y	7–	0111 | y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	–6	00 | r | 0110	RAM(B) ⟷ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	3,15	23	0010 | 0011	RAM(3,15) ⟷ A	None	Exchange A with RAM (3,15)
		BF	1011 | 1111			

COP413C Instruction Set (Continued)

TABLE III. COP413C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS (Continued)						
XDS	r	−7	|00|r|0111|	RAM(B) ⟷ A Bd − 1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd Exclusive-OR Br with r
XIS	r	−4	|00|r|0100|	RAM(B) ⟷ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	|0101|0000|	A → Bd	None	Copy A to Bd
CBA		4E	|0100|1110|	Bd → A	None	Copy Bd to A
LBI	r,d	–	|00|r|(d - 1)| (d = 0,9:15)	r,d → B	Skip until not a LBI	Load B Immediate with r,d
LEI	y	33 6–	|0011|0011| |0010| y |	y → EN	None	Load EN Immediate
TEST INSTRUCTIONS						
SKC		20	|0010|0000|		C = "1"	Skip if C is True
SKE		21	|0010|0001|		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	|0011|0011| |0010|0001|		$G_{3:0}$ = 0	Skip if G is Zero (all 4 bits)
SKGBZ		33	|0011|0011|	1st byte		Skip if G Bit is Zero
	0	01	|0000|0001|	2nd byte	G_0 = 0	
	1	11	|0001|0001|	2nd byte	G_1 = 0	
	2	03	|0000|0011|	2nd byte	G_2 = 0	
	3	13	|0010|0011|	2nd byte	G_3 = 0	
SKMBZ	0	01	|0000|0001|		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	|0001|0001|		$RAM(B)_1$ = 0	
	2	03	|0000|0011|		$RAM(B)_2$ = 0	
	3	13	|0001|0011|		$RAM(B)_3$ = 0	
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	|0011|0011| |0010|1010|	G → A	None	Input G Ports to A
INL		33 2E	|0011|0011| |0010|1110|	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM, A
OMG		33 3A	|0011|0011| |0011|1010|	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	|0100|1111|	A ⟷ SIO, C → SKL	None	Exchange A with SIO

Note 1: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 2: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Description of Selected Instructions

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing COP413C programs.

XAS INSTRUCTION

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register.) If SIO is selected as a shift register, an XAS instruction must be performed once every four instruction cycle times to effect a continuous data stream.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower eight bits of the ROM address register PC with the contents of ROM addressed by the 9-bit word, PC_8, A, M. PC_8 is not affected by this instruction.

Note: JID uses two instruction cycles if executed, one if skipped.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 9-bit word PC_8, A, M. LQID can be used for table look-up or code conversion such as BCD to 7-segment. The LQID instruction "pushes" the stack (PC + 1 $\rightarrow$ SA $\rightarrow$ SB) and replaces the least significant eight bits of the PC as follows: A $\rightarrow$ $PC_{7:4}$, RAM(B) $\rightarrow$ $PC_{3:0}$, leaving PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SB $\rightarrow$ SA $\rightarrow$ PC), restoring the saved value of the PC to continue sequential program execution. Since LQID pushes SA $\rightarrow$ SB, the previous contents of SB are lost.

Note: LQID uses two instruction cycles if executed, one if skipped.

INSTRUCTION SET NOTES

a. The first word of a COP413C program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths take the same number of cycle times whether instructions are skipped or executed (except JID and LQID).

c. The ROM is organized into eight pages of 64 words each. The program counter is a 9-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: A JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word in page 3 or 7 will access data in the next group of four pages.

COPS Programming Manual

For detailed information on writing. COPS programs, the COPS Programming Manual 424410284-001 provides an in-depth discussion of the COPS architecture, instruction set and general techniques of COPS programming. This manual is written with the programmer in mind.

OPTION LIST—OSCILLATOR SELECTION

The oscillator option selected must be sent in with the EPROM of ROM Code for masking into the COP413C. Select the appropriate option, make a photocopy of the table and send it with the EPROM.

COP413C/COP313C

Option 1: Oscillator selection

= 0 Ceramic Resonator input frequency divided by 8. CKO is oscillator output.

= 1 Single pin RC controlled oscillator divided by 4. CKO is no connection.

Note: The following option information is to be sent to National along with the EPROM.

Option 1: Value = ____ is Oscillator Selected.

National Semiconductor

COP424C, COP425C, COP426C, COP324C, COP325C, COP326C and COP444C, COP445C, COP344C, COP345C Single-Chip 1k and 2k CMOS Microcontrollers

General Description

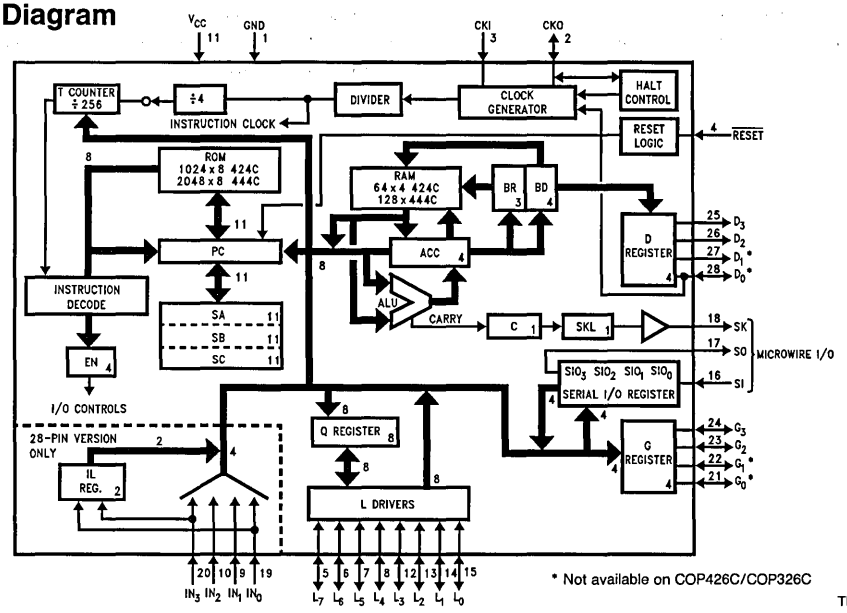
The COP424C, COP425C, COP426C, COP444C and COP445C fully static, Single-Chip CMOS Microcontrollers are members of the COPS™ family, fabricated using double-poly, silicon gate microCMOS technology. These Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The COP424C and COP444C are 28 pin chips. The COP425C and COP445C are 24-pin versions (4 inputs removed) and COP426C is 20-pin version with 15 I/O lines. Standard test procedures and reliable high-density techniques provide the medium to large volume customers with a customized microcontroller at a low end-product cost. These microcontrollers are appropriate choices in many demanding control environments especially those with human interface.

The COP424C is an improved product which replaces the COP420C.

Features

- Lowest power dissipation (50 μW typical)
- Fully static (can turn off the clock)
- Power saving IDLE state and HALT mode
- 4 μs instruction time, plus software selectable clocks
- 2k x 8 ROM, 128 x 4 RAM (COP444C/COP445C)
- 1k x 8 ROM, 64 x 4 RAM (COP424C/COP425C/COP426C)
- 23 I/O lines (COP444C and COP424C)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- Single supply operation (2.4V to 5.5V)
- Programmable read/write 8-bit timer/event counter
- Internal binary counter register with MICROWIRE™ serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS output compatible
- Microbus™ compatible
- Software/hardware compatible with COP400 family
- Extended temperature range devices COP324C/COP325C/COP326C and COP344C/COP345C (−40°C to +85°C)
- Military devices (−55°C to +125°C) to be available

Block Diagram



* Not available on COP426C/COP326C

TL/DD/5259–1

FIGURE 1

COP424C/COP425C/COP426C and COP444C/COP445C

Absolute Maximum Ratings

Supply Voltage (V_{CC})	6V
Voltage at any Pin	−0.3V to V_{CC} + 0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $0°C \le T_A \le 70°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (Notes 4, 5)	Peak to Peak		0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 2.4V, tc = 64 μs		120	μA
	V_{CC} = 5.0V, tc = 16 μs		700	μA
	V_{CC} = 5.0V, tc = 4 μs (tc is instruction cycle time)		3000	μA
HALT Mode Current (Note 2)	V_{CC} = 5.0V, F_{IN} = 0 kHz		40	μA
	V_{CC} = 2.4V, F_{IN} = 0 kHz		12	μA
Input Voltage Levels				
RESET, CKI, D_0 (clock input)				
Logic High		0.9 V_{CC}		V
Logic Low			0.1 V_{CC}	V
All Other Inputs				
Logic High		0.7 V_{CC}		V
Logic Low			0.2 V_{CC}	V
Input Pull-Up Current	V_{CC} = 4.5V, V_{IN} = 0	−30	−330	μA
Hi-Z Input Leakage		−1	+1	μA
Input Capacitance (Note 4)			7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0V ± 10%			
Logic High	I_{OH} = −100 μA	2.7		V
Logic Low	I_{OL} = 400 μA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 μA	V_{CC} − 0.2		V
Logic Low	I_{OL} = 10 μA		0.2	V
Output Current Levels (except CKO)				
Sink (Note 6)	V_{CC} = 4.5V, V_{OUT} = V_{CC}	1.2		mA
	V_{CC} = 2.4V, V_{OUT} = V_{CC}	0.2		mA
Source (Standard Option)	V_{CC} = 4.5V, V_{OUT} = 0V	−0.5		mA
	V_{CC} = 2.4V, V_{OUT} = 0V	−0.1		mA
Source (Low Current Option)	V_{CC} = 4.5V, V_{OUT} = 0V	−30	−330	μA
	V_{CC} = 2.4V, V_{OUT} = 0V	−6	−80	μA
CKO Current Levels (As Clock Out)				
Sink ÷4	V_{CC} = 4.5V, CKI = V_{CC}, V_{OUT} = V_{CC}	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Source ÷4	V_{CC} = 4.5V, CKI = 0V, V_{OUT} = 0V	−0.3		mA
÷8		−0.6		mA
÷16		−1.2		mA
Allowable Sink/Source Current per Pin (Note 6)			5	mA
Allowable Loading on CKO (as HALT)			100	pF
Current Needed to Over-Ride HALT (Note 3)				
To Continue	V_{CC} = 4.5V, V_{IN} = 0.2V_{CC}		0.7	mA
To Halt	V_{CC} = 4.5V, V_{IN} = 0.7V_{CC}		1.6	mA
TRI-STATE or Open Drain Leakage Current		−2.5	+2.5	μA

COP324C/COP325C/COP326C and COP344C/COP345C

Absolute Maximum Ratings

Supply Voltage	6V
Voltage at any Pin	−0.3V to V_{CC} + 0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		3.0	5.5	V
Power Supply Ripple (Notes 4, 5)	Peak to Peak		0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 3.0V, tc = 64 μs		180	μA
	V_{CC} = 5.0V, tc = 16 μs		800	μA
	V_{CC} = 5.0V, tc = 4 μs (tc is instruction cycle time)		3600	μA
HALT Mode Current (Note 2)	V_{CC} = 5.0V, F_{IN} = 0 kHz		60	μA
	V_{CC} = 3.0V, F_{IN} = 0 kHz		30	μA
Input Voltage Levels				
RESET, CKI, D_O (clock input)				
Logic High		0.9 V_{CC}		V
Logic Low			0.1 V_{CC}	V
All Other Inputs				
Logic High		0.7 V_{CC}		V
Logic Low			0.2 V_{CC}	V
Input Pull-Up Current	V_{CC} = 4.5V, V_{IN} = 0	−30	−440	μA
Hi-Z Input Leakage		−2	+2	μA
Input Capacitance (Note 4)			7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0V ±10%			
Logic High	I_{OH} = −100 μA	2.7		V
Logic Low	I_{OL} = 400 μA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 μA	V_{CC} − 0.2		V
Logic Low	I_{OL} = 10 μA		0.2	V
Output Current Levels (except CKO)				
Sink (Note 6)	V_{CC} = 4.5V, V_{OUT} = V_{CC}	1.2		mA
	V_{CC} = 3.0V, V_{OUT} = V_{CC}	0.2		mA
Source (Standard Option)	V_{CC} = 4.5V, V_{OUT} = 0V	−0.5		mA
	V_{CC} = 3.0V, V_{OUT} = 0V	−0.1		mA
Source (Low Current Option)	V_{CC} = 4.5V, V_{OUT} = 0V	−30	−440	μA
	V_{CC} = 3.0V, V_{OUT} = 0V	−8	−200	μA
CKO Current Levels (As Clock Out)				
Sink ÷4	V_{CC} = 4.5V, CKI = V_{CC}, V_{OUT} = V_{CC}	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Source ÷4	V_{CC} = 4.5V, CKI = 0V, V_{OUT} = 0V	−0.3		mA
÷8		−0.6		mA
÷16		−1.2		mA
Allowable Sink/Source Current per Pin (Note 6)			5	mA
Allowable Loading on CKO (as HALT)			100	pF
Current Needed to Over-Ride HALT (Note 3)				
To Continue	V_{CC} = 4.5V, V_{IN} = 0.2V_{CC}		0.9	mA
To Halt	V_{CC} = 4.5V, V_{IN} = 0.7V_{CC}		2.1	mA
TRI-STATE or Open Drain Leakage Current		−5	+5	μA

COP424C/COP425C/COP426C and COP444C/COP445C

AC Electrical Characteristics $0°C \le T_A \le 70°C$ unless otherwise specified.

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (tc)	$V_{CC} \ge 4.5V$	4	DC	μs
	$4.5V > V_{CC} \ge 2.4V$	16	DC	μs
Operating CKI Frequency ÷4 mode	$V_{CC} \ge 4.5V$	DC	1.0	MHz
÷8 mode	$V_{CC} \ge 4.5V$	DC	2.0	MHz
÷16 mode	$V_{CC} \ge 4.5V$	DC	4.0	MHz
÷4 mode	$4.5V > V_{CC} \ge 2.4V$	DC	250	kHz
÷8 mode	$4.5V > V_{CC} \ge 2.4V$	DC	500	kHz
÷16 mode	$4.5V > V_{CC} \ge 2.4V$	DC	1.0	MHz
Duty Cycle (Note 4)	$f_1 = 4$ MHz	40	60	%
Rise Time (Note 4)	$f_1 = 4$ MHz External Clock		60	ns
Fall Time (Note 4)	$f_1 = 4$ MHz External Clock		40	ns
Instruction Cycle Time RC Oscillator (Note 4)	$R = 30k \pm 5\%$, $V_{CC} = 5V$ $C = 82$ pF ±5% (÷4 Mode)	5	11	μs
Inputs: (See *Figure 3*)				
t_{SETUP} G Inputs	$V_{CC} \ge 4.5V$	tc/4+.7		μs
t_{SETUP} SI Input	$V_{CC} \ge 4.5V$	0.3		μs
t_{SETUP} All Others	$V_{CC} \ge 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \ge 4.5V$	0.25		μs
	$4.5V > V_{CC} \ge 2.4V$	1.0		μs
Output Propagation Delay	$V_{OUT} = 1.5V$, $C_L = 100$ pF, $R_L = 5k$			
t_{PD1}, t_{PD0}	$V_{CC} \ge 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$4.5V > V_{CC} \ge 2.4V$		4.0	μs
Microbus Timing	$CL = 50$ pF, $V_{CC} = 5V \pm 5\%$			
Read Operation (*Figure 4*)				
Chip Select Stable before $\overline{RD}$ $-t_{CSR}$		65		ns
Chip Select Hold Time for $\overline{RD}$ $-t_{RCS}$		20		ns
$\overline{RD}$ Pulse Width $-t_{RR}$		400		ns
Data Delay from $\overline{RD}$ $-t_{RD}$			375	ns
$\overline{RD}$ to Data Floating $-t_{DF}$ (Note 4)			250	ns
Write Operation (*Figure 5*)				
Chip Select Stable before $\overline{WR}$ $-t_{CSW}$		65		ns
Chip Select Hold Time for $\overline{WR}$ $-t_{WCS}$		20		ns
$\overline{WR}$ Pulse Width $-t_{WW}$		400		ns
Data Set-Up Time for $\overline{WR}$ $-t_{DW}$		320		ns
Data Hold Time for $\overline{WR}$ $-t_{WD}$		100		ns
INTR Transition Time from $\overline{WR}$ $-t_{WI}$			700	ns

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 5k resistors. See current drain equation on page 17.

Note 2: The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions: all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all outputs low and tied to ground.

Note 3: When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

Note 4: This parameter is only sampled and not 100% tested. Variation due to the device included.

Note 5: Voltage change must be less than 0.5 volts in a 1 ms period.

Note 6: SO output sink current must be limited to keep V_{OL} less than $0.2V_{CC}$ when part is running in order to prevent entering test mode.

COP324C/COP325C/COP326C and COP344C/COP345C

AC Electrical Characteristics $-40°C \leq T_A \leq +85°C$ unless otherwise specified.

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (tc)	$V_{CC} \geq 4.5V$	4	DC	μs
	$4.5V > V_{CC} \geq 3.0V$	16	DC	μs
Operating CKI Frequency ÷4 mode	$V_{CC} \geq 4.5V$	DC	1.0	MHz
÷8 mode	$V_{CC} \geq 4.5V$	DC	2.0	MHz
÷16 mode	$V_{CC} \geq 4.5V$	DC	4.0	MHz
÷4 mode	$4.5V > V_{CC} \geq 3.0V$	DC	250	kHz
÷8 mode	$4.5V > V_{CC} \geq 3.0V$	DC	500	kHz
÷16 mode	$4.5V > V_{CC} \geq 3.0V$	DC	1.0	MHz
Duty Cycle (Note 4)	$f_1 = 4$ MHz	40	60	%
Rise Time (Note 4)	$f_1 = 4$ MHz external clock		60	ns
Fall Time (Note 4)	$f_1 = 4$ MHz external clock		40	ns
Instruction Cycle Time RC Oscillator (Note 4)	R = 30k ±5%, V_{CC} = 5V C = 82 pF ±5% (÷4 Mode)	5	11	μs
Inputs: (See *Figure 3*)				
t_{SETUP} G Inputs	$V_{CC} \geq 4.5V$	tc/4+.7		μs
t_{SETUP} SI Inputs	$V_{CC} \geq 4.5V$	0.3		μs
t_{SETUP} All Others	$V_{CC} \geq 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \geq 4.5V$	0.25		μs
	$4.5V > V_{CC} \geq 3.0V$	1.0		μs
Output Propagation Delay	$V_{OUT} = 1.5V$, $C_L = 100$ pF, $R_L = 5k$			
t_{PD1}, t_{PD0}	$V_{CC} \geq 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$4.5V > V_{CC} \geq 3.0V$		4.0	μs
Microbus Timing	$C_L = 50$ pF, $V_{CC} = 5V \pm 5\%$			
Read Operation (*Figure 4*)				
Chip Select Stable before $\overline{RD}$ – t_{CSR}		65		ns
Chip Select Hold Time for $\overline{RD}$ – t_{RCS}		20		ns
$\overline{RD}$ Pulse Width – t_{RR}		400		ns
Data Delay from $\overline{RD}$ – t_{RD}			375	ns
$\overline{RD}$ to Data Floating – t_{DF} (Note 4)			250	ns
Write Operation (*Figure 5*)				
Chip Select Stable before $\overline{WR}$ – t_{CSW}		65		ns
Chip Select Hold Time for $\overline{WR}$ – t_{WCS}		20		ns
$\overline{WR}$ Pulse Width – t_{WW}		400		ns
Data Set-Up Time for $\overline{WR}$ – t_{DW}		320		ns
Data Hold Time for $\overline{WR}$ – t_{WD}		100		ns
INTR Transition Time from $\overline{WR}$ – t_{WI}			700	ns

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 5k resistors. See current drain equation on page 17.

Note 2: The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions: all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all outputs low and tied to ground.

Note 3: When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

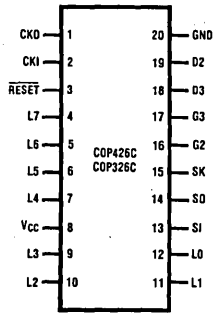
Note 4: This parameter is only sampled and not 100% tested. Variation due to the device included.

Note 5: Voltage change must be less than 0.5 volts in a 1 ms period.

Note 6: SO output sink current must be limited to keep V_{OL} less than $0.2V_{CC}$ when part is running in order to prevent entering test mode.

Connection Diagrams

DIP and S.O. Wide



TL/DD/5259-16

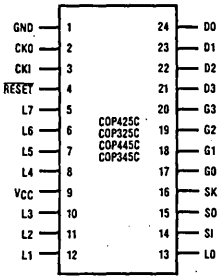
Top View

Order Number COP326C-XXX/D or COP426C-XXX/D
See NS Hermetic Package D20A
(Prototype Package Only)

Order Number COP326C-XXX/N or COP426C-XXX/N
See NS Molded Package N20A

Order Number COP326C-XXX/WM or COP426C-XXX/WM
See NS Surface Mount Package M20B

DIP and S.O. Wide



TL/DD/5259-2

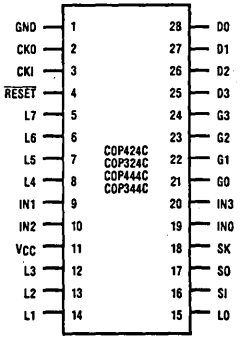
Top View

Order Number COP325C-XXX/D, COP445C-XXX/D, COP425C-XXX/D or COP345C-XXX/D
See NS Hermetic Package D24C
(Prototype Package Only)

Order Number COP325C-XXX/N, COP345C-XXX/N, COP425C-XXX/N or COP445C-XXX/N
See NS Molded Package N24A

Order Number COP325C-XXX/WM, COP345C-XXX/WM, COP425C-XXX/WM or COP445C-XXX/WM
See NS Surface Mount Package M24B

Dual-In-Line Package



TL/DD/5259-3

Top View

Order Number COP324C-XXX/D, COPC324-XXX/WM, COP344C-XXX/D, COP424C-XXX/D, COPC424-XXX/WM or COP444C-XXX/D
See NS Hermetic Package D28C
(Prototype Package Only)

Order Number COP324C-XXX/N, COP344C-XXX/N, COPC344-XXX/WM, COP424C-XXX/N, COP444C-XXX/N or COPC444-XXX/WM
See NS Molded Package N28B

FIGURE 2

Pin	Description
L7–L0	8-bit bidirectional port with TRI-STATE
G3–G0	4-bit bidirectional I/O port
D3–D0	4-bit output port
IN3–IN0	4-bit input port (28-pin package only)
SI	Serial input or counter input
SO	Serial or general purpose output

Pin	Description
SK	Logic controlled clock output
CKI	Chip oscillator input
CKO	Oscillator output, HALT I/O port or general purpose input
$\overline{\text{RESET}}$	Reset input
V_{CC}	Most positive power supply
GND	Ground

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Functional Description

The internal architecture is shown in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1", when a bit is reset, it is a logic "0".

For ease of reading only the COP424C/425C/COP426C/444C/445C are referenced; however, all such references apply equally to COP324C/325C/COP326C/344C/345C.

PROGRAM MEMORY

Program Memory consists of ROM, 1024 bytes for the COP424C/425C/426C and 2048 bytes for the COP444C/445C. These bytes of ROM may be program instructions, constants or ROM addressing data.

ROM addressing is accomplished by a 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

Three levels of subroutine nesting are implemented by a three level deep stack. Each subroutine call or interrupt pushes the next PC address into the stack. Each return pops the stack back into the PC register.

DATA MEMORY

Data memory consists of a 512-bit RAM for the COP444C/445C, organized as 8 data registers of 16 × 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register.

Data memory consists of a 256-bit RAM for the COP424C/425C/426C, organized as 4 data registers of 16 × 4-bits digits. The B register is 6 bits long. Upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or T counter or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate operand field of these instructions.

The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

INTERNAL LOGIC

The processor contains its own 4-bit A register (accumulator) which is the source and destination register for most I/O, arithmetic, logic, and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch or T counter, to input 4 bits of L I/O ports data, to input 4-bit G, or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register in conjunction with the XAS instruction and the EN register, also serves to control the SK output.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. When the T counter overflows, an overflow flag will be set (see SKT and IT instructions below). The T counter is cleared on reset. A functional block diagram of the timer/counter is illustrated in *Figure 10a*.

Four general-purpose inputs, IN3-IN0, are provided. IN1, IN2 and IN3 may be selected, by a mask-programmable option as Read Strobe, Chip Select, and Write Strobe inputs, respectively, for use in Microbus application.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. In the dual clock mode, D0 latch controls the clock selection (see dual oscillator below).

The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port. G0 may be mask-programmed as an output for Microbus applications.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control. With the Microbus option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU.

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O port. Also, the contents of L may be read directly into A and M. As explained above, the Microbus option allows L I/O port data to be latched into the Q register.

Functional Description (Continued)

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and COPS peripherals, or as a binary counter (depending on the contents of the EN register). Its contents can be exchanged with A.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

EN is an internal 4-bit register loaded by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register:

0. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, decrementing its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output equals the value of EN3. With EN0 reset, SIO is a serial shift register left shifting 1 bit each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. The SK outputs SKL ANDed with the instruction cycle clock.
1. With EN1 set, interrupt is enabled. Immediately following an interrupt, EN1 is reset to disable further interrupts.
2. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O port. Resetting EN2 disables the L drivers, placing the L I/O port in a high-impedance input state.

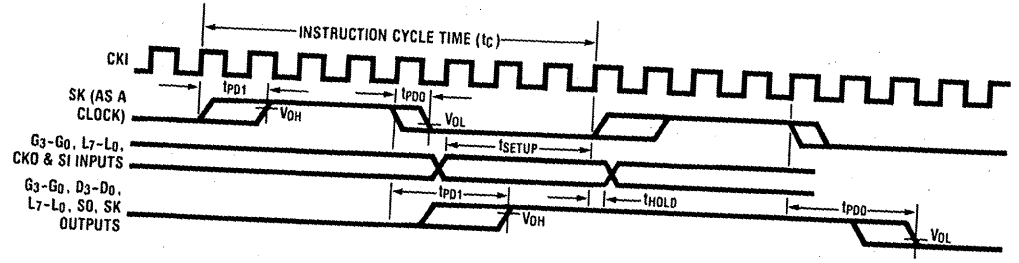

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FIGURE 3. Input/Output Timing Diagrams (divide by 8 mode)

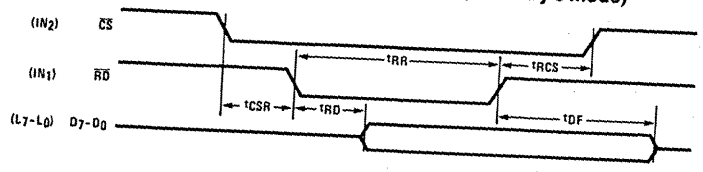

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FIGURE 4. Microbus Read Operation Timing

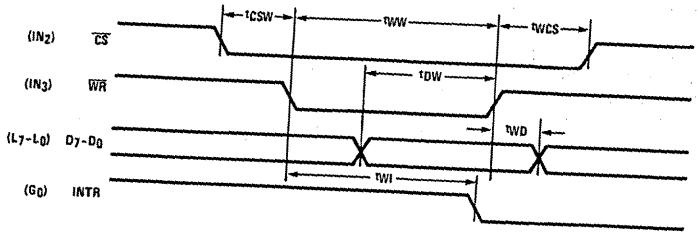

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FIGURE 5. Microbus Write Operation Timing

Functional Description (Continued)

3. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected) SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains set to "0".

INTERRUPT

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once recognized as explained below, pushes the next sequential program counter address (PC+1) onto the stack. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN1 is reset.

b. An interrupt will be recognized only on the following conditions:
   1. EN1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide has occurred on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. All successive transfer of control instructions and successive LBIs have been completed (e.g. if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the end of the interrupt routine, a RET instruction is executed to pop the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines should not be nested within the interrupt service routine, since their popping of the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The instruction at hex address 0FF must be a NOP.

e. An LEI instruction may be put immediately before the RET instruction to re-enable interrupts.

MICROBUS INTERFACE

The COP444C/424C has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from and to a host microprocessor (μP). IN1, IN2 and IN3 general purpose inputs become Microbus compatible read-strobe, chip-select, and write-strobe lines, respectively. IN1 becomes $\overline{RD}$ — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the uP. IN2 becomes $\overline{CS}$ — a logic "0" on this line selects the COP444C/424C as the uP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several peripheral components. IN3 becomes $\overline{WR}$ — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the COP444C/424C. G0 becomes INTR a "ready" output, reset by a write pulse from the uP on the $\overline{WR}$ line, providing the "handshaking" capability necessary for asynchronous data transfer between the host CPU and the COP444C/424C.

This option has been designed for compatibility with National's Microbus — a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See Microbus National Publication.) The functioning and timing relationships between the signal lines affected by this option are as specified for the Microbus interface, and are given in the AC electrical characteristics and shown in the timing diagrams (*Figures 4* and *5*). Connection of the COP444C/424C to the Microbus is shown in *Figure 6*.

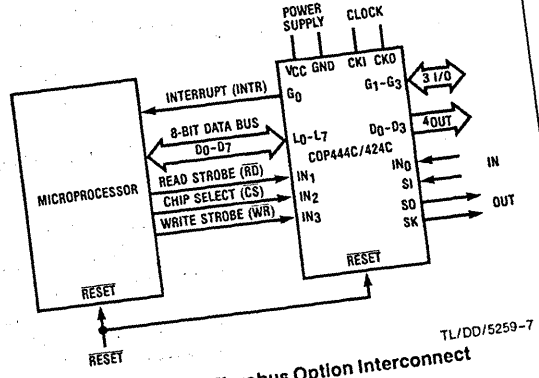

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FIGURE 6. Microbus Option Interconnect

TABLE I. Enable Register Modes — Bits EN0 and EN3

EN0	EN3	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Binary Counter	Input to Counter	0	SK = SKL
1	1	Binary Counter	Input to Counter	1	SK = SKL

Functional Description (Continued)

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and COPS peripherals, or as a binary counter (depending on the contents of the EN register). Its contents can be exchanged with A.

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EN is an internal 4-bit register loaded by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register:

0. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, decrementing its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output equals the value of EN3. With EN0 reset, SIO is a serial shift register left shifting 1 bit each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. The SK outputs SKL ANDed with the instruction cycle clock.
1. With EN1 set, interrupt is enabled. Immediately following an interrupt, EN1 is reset to disable further interrupts.
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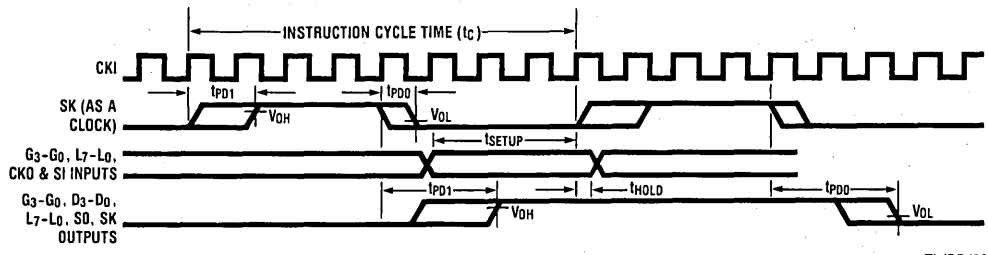

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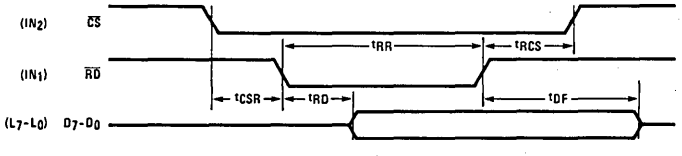

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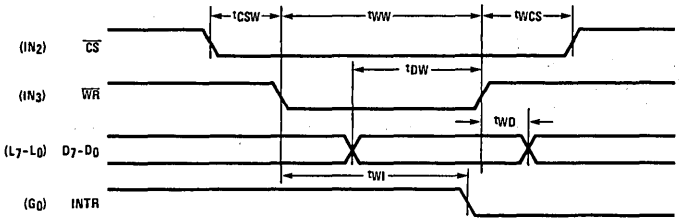

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FIGURE 5. Microbus Write Operation Timing

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Functional Description (Continued)

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IN3 becomes $\overline{WR}$ — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the COP444C/424C. G0 becomes INTR a "ready" output, reset by a write pulse from the uP on the $\overline{WR}$ line, providing the "handshaking" capability necessary for asynchronous data transfer between the host CPU and the COP444C/424C.

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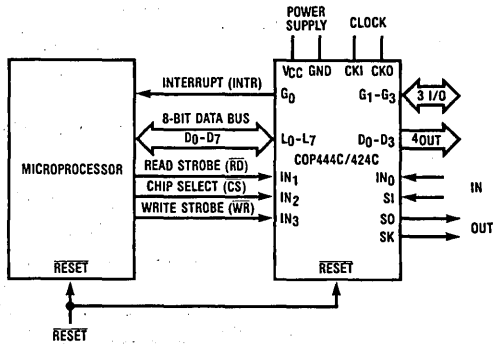

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FIGURE 6. Microbus Option Interconnect

TABLE I. Enable Register Modes — Bits EN0 and EN3

EN0	EN3	SIO	SI	SO	SK
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0	1	Shift Register	Input to Shift Register	Serial out	If SKL=1,SK=clock If SKL=0,SK=0
1	0	Binary Counter	Input to Counter	0	SK=SKL
1	1	Binary Counter	Input to Counter	1	SK=SKL

Functional Description (Continued)

INITIALIZATION

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1 ms and if the operating frequency at CKI is greater than 32 kHz, otherwise the external RC network shown in *Figure 7* must be connected to the $\overline{\text{RESET}}$ pin (the conditions in *Figure 7* must be met). The $\overline{\text{RESET}}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{\text{RESET}}$ input, providing it stays low for at least three instruction cycle times.

Note: If CKI clock is less than 32 kHz, the internal reset logic (option #29 = 1) MUST be disabled and the external RC circuit must be used.

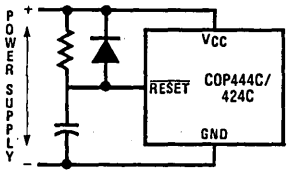

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FIGURE 7. Power-Up Circuit

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, IL, T and G registers are cleared. The SKL latch is set, thus enabling SK as a clock output. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

TIMER

The timer can be operated as a time-base counter.

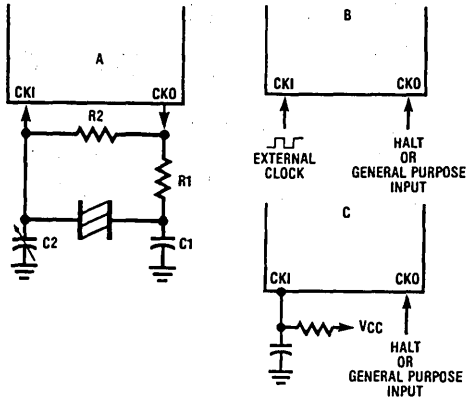
The instruction cycle frequency generated from CKI passes through a 2-bit divide-by-4 prescaler. The output of this prescaler increments the 8-bit T counter thus providing a 10-bit timer. The pre-scaler is cleared during execution of a CAMT instruction and on reset.

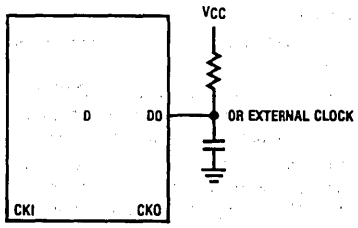
For example, using a 4 MHz crystal with a divide-by-16 option, the instruction cycle frequency of 250 kHz increments the 10-bit timer every 4 μs. By presetting the counter and detecting overflow, accurate timeouts between 16 μs (4 counts) and 4.096 ms (1024 counts) are possible. Longer timeouts can be achieved by accumulating, under software control, multiple overflows.

HALT MODE

The COP444C/445C/424C/425C/426C is a FULLY STATIC circuit; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may also be halted by the HALT instruction or by forcing CKO high when it is mask-programmed as an HALT I/O port. Once in the HALT mode, the internal circuitry does not receive any clock signal and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The chip may be awakened by one of two different methods:

- Continue function: by forcing CKO low, if it mask-programmed as an HALT I/O port, the system clock is re-enabled and the circuit continues to operate from the point where it was stopped.
- Restart: by forcing the $\overline{\text{RESET}}$ pin low (see Initialization).





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Crystal or Resonator

Crystal Value	Component Values			
	R1	R2	C1(pF)	C2(pF)
32 kHz	220k	20M	30	6–36
455 kHz	5k	10M	80	40
2.096 MHz	2k	1M	30	6–36
4.0 MHz	1k	1M	30	6–36

RC Controlled Oscillator (±5% R, ±5% C)

R	C	Cycle Time	V_{CC}
30k	82 pF	5–11 μs	≥4.5V
60k	100 pF	12–24 μs	2.4–4.5V

Note: 15k≤R≤150k
50 pF≤C≤150 pF

FIGURE 8. Oscillator Component Values

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Functional Description (Continued)

The HALT mode is the minimum power dissipation state.

Note: If the user has selected dual-clock with D0 as external oscillator (option 30=2) AND the COP444C/424C is running with the D0 clock, the HALT mode — either hardware or software — will NOT be entered. Thus, the user should switch to the CKI clock to HALT. Alternatively, the user may stop the D0 clock to minimize power.

CKO PIN OPTIONS

a. Two-pin oscillator — (Crystal). See *Figure 9A*.

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. The HALT mode may be entered by program control (HALT instruction) which forces CKO high, thus inhibiting the crystal network. The circuit can be awakened only by forcing the $\overline{\text{RESET}}$ pin to a logic "0" (restart).

b. One-pin oscillator — (RC or external). See *Figure 9B*.

If a one-pin oscillator system is chosen, two options are available for CKO:

- CKO can be selected as the HALT I/O port. In that case, it is an I/O flip-flop which is an indicator of the HALT status. An external signal can over-ride this pin to start and stop the chip. By forcing a high level to CKO, the chip will stop as soon as CKI is high and CKO output will stay high to keep the chip stopped if the external driver returns to high impedance state. By forcing a low level to CKO, the chip will continue and CKO will stay low.
- As another option, CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction.

OSCILLATOR OPTIONS

There are four basic clock oscillator configurations available as shown by *Figure 8*.

a. Crystal Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency optionally divided by 4, 8 or 16.

b. External Oscillator. The external frequency is optionally divided by 4, 8 or 16 to give the instruction cycle time. CKO is the HALT I/O port or a general purpose input.

c. RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is the HALT I/O port or a general purpose input.

d. Dual oscillator. By selecting the dual clock option, pin D0 is now a single pin oscillator input. Two configurations are available: RC controlled Schmitt trigger oscillator or external oscillator.

The user may software select between the D0 oscillator (in that case, the instruction cycle time equals the D0 oscillation frequency divided by 4) by setting the D0 latch high or the CKI (CKO) oscillator by resetting D0 latch low. Note that even in dual clock mode, the counter, if mask-programmed as a time-base counter, is always connected to the CKI oscillator.

For example, the user may connect up to a 1 MHz RC circuit to D0 for faster processing and a 32 kHz watch crystal to CKI and CKO for minimum current drain and time keeping.

Note: CTMA instruction is not allowed when chip is running from D0 clock.

Figures 10A and *10B* show the clock and timer diagrams with and without Dual clock.

COP445C AND COP425C 24-PIN PACKAGE OPTION

If the COP444C/424C is bonded in a 24-pin package, it becomes the COP445C/425C, illustrated in *Figure 2*, Connection diagrams. Note that the COP445C/425C does not contain the four general purpose IN inputs (IN3–IN0). Use of this option precludes, of course, use of the IN options, interrupt feature, external event counter feature, and the Microbus option which uses IN1–IN3. All other options are available for the COP445C/425C.

Note: If user selects the 24-pin package, options 9, 10, 19 and 20 must be selected as a "0" (load to V_{CC} on the IN inputs). See option list.

COP426C 20-PIN PACKAGE OPTION

If the COP425C is bonded as 20-pin device it becomes the COP426C. Note that the COP426C contains all the COP425C pins except D_0, D_1, G_0, and G_1.

Block Diagram (Continued)

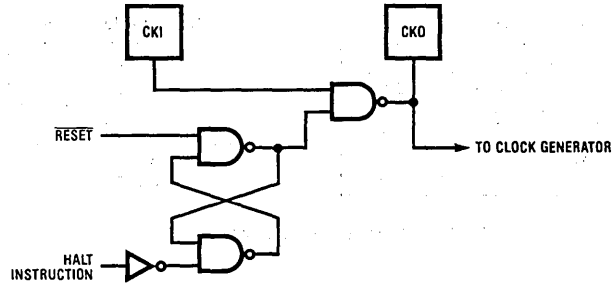

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FIGURE 9A. Halt Mode — Two-Pin Oscillator

Block Diagram (Continued)

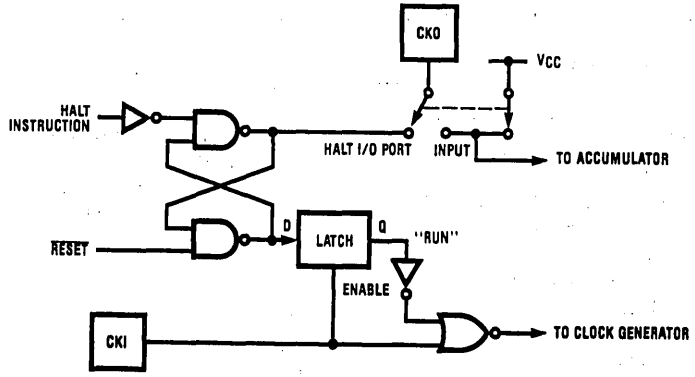

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FIGURE 9B. Halt Mode — One-Pin Oscillator

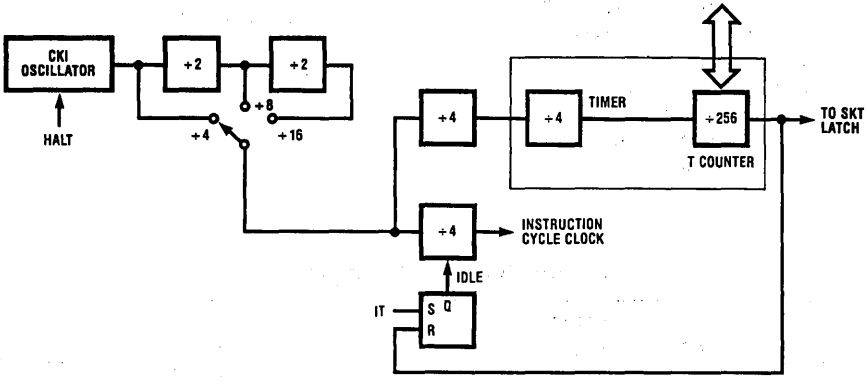

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FIGURE 10A. Clock and Timer without Dual-Clock

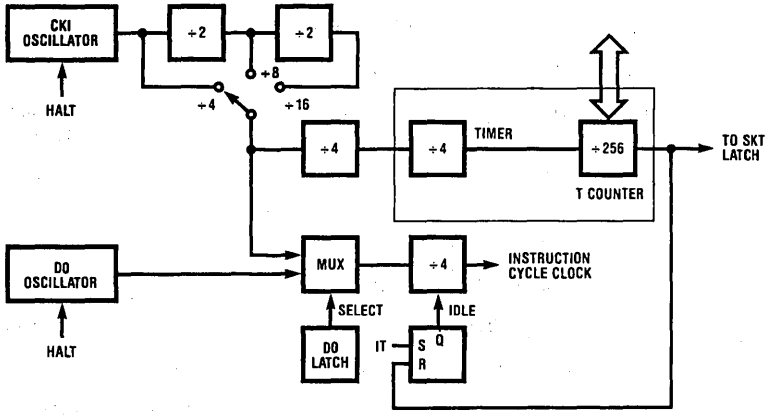

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FIGURE 10B. Clock and Timer with Dual-Clock

7

Instruction Set

Table II is a symbol table providing internal architecture, instruction operan and operation symbols used in the instruction set table.

TABLE II. Instruction Set Table Symbols

Symbol	Definition
Internal Architecture Symbols	
A	4-bit accumulator
B	7-bit RAM address register (6-bit for COP424C)
Br	Upper 3 bits of B (register address) (2-bit for COP424C)
Bd	Lower 4 bits of B (digit address)
C	1-bit carry register
D	4-bit data output port
EN	4-bit enable register
G	4-bit general purpose I/O port
IL	two 1-bit (IN0 and IN3) latches
IN	4-bit input port
L	8-bit TRI-STATE I/O port
M	4-bit contents of RAM addressed by B
PC	11-bit ROM address program counter
Q	8-bit latch for L port
SA,SB,SC	11-bit 3-level subroutine stack
SIO	4-bit shift register and counter
SK	Logic-controlled clock output
SKL	1-bit latch for SK output
T	8-bit timer

Table III provides the mnemonic, operand, machine code data flow, skip conditions and description of each instruction.

Instruction Operand Symbols	
d	4-bit operand field, 0–15 binary (RAM digit select)
r	3(2)-bit operand field, 0–7(3) binary (RAM register select)
a	11-bit operand field, 0–2047 (1023)
y	4-bit operand field, 0–15 (immediate data)
RAM(x)	RAM addressed by variable x
ROM(x)	ROM addressed by variable x

Operational Symbols	
+	Plus
−	Minus
→	Replaces
↔	Is exchanged with
=	Is equal to
$\overline{A}$	One's complement of A
⊕	Exclusive-or
:	Range of values

TABLE III. COP444C/445C Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011 | 0000	A+C+RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0011 | 0001	A+RAM(B) → A	None	Add RAM to A
ADT		4A	0100 | 1010	A+10_{10} → A	None	Add Ten to A
AISC	y	5–	0101 | y	A+y → A	Carry	Add Immediate. Skip on Carry (y ≠ 0)
CASC		10	0001 | 0000	$\overline{A}$+RAM(B)+C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0000 | 0000	0 → A	None	Clear A
COMP		40	0100 | 0000	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	0100 | 0100	None	None	No Operation
RC		32	0011 | 0010	"0" → C	None	Reset C
SC		22	0010 | 0010	"1" → C	None	Set C
XOR		02	0000 | 0010	A⊕RAM(B) → A	None	Exclusive-OR RAM with A

Instruction Set (Continued)

Table III. COP444C/445C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER CONTROL INSTRUCTIONS						
JID		FF	1111 | 1111	ROM ($PC_{10:8}$ A,M) → $PC_{7:0}$	None	Jump Indirect (Notes 1, 3)
JMP	a	6–	0110 | 0 | $a_{10:8}$	a → PC	None	Jump
		––	$a_{7:0}$			
JP	a	––	1 | $a_{6:0}$ (pages 2,3 only)	a → $PC_{6:0}$	None	Jump within Page (Note 4)
			or			
		––	11 | $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	––	10 | $a_{5:0}$	PC+1 → SA → SB → SC 00010 → $PC_{10:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6–	0110 | 1 | $a_{10:8}$	PC+1 → SA → SB → SC	None	Jump to Subroutine
		––	$a_{7:0}$	a → PC		
RET		48	0100 | 1000	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0100 | 1001	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33	0011 | 0011		None	HALT Processor
		38	0011 | 1000			
IT		33	0011 | 0011			IDLE till Timer
		39	0011 | 1001		None	Overflows then Continues
MEMORY REFERENCE INSTRUCTIONS						
CAMT		33	0011 | 0011	A → $T_{7:4}$		
		3F	0011 | 1111	RAM(B) → $T_{3:0}$	None	Copy A, RAM to T
CTMA		33	0011 | 0011	$T_{7:4}$ → RAM(B)		
		2F	0010 | 1111	$T_{3:0}$ → A	None	Copy T to RAM, A (Note 9)
CAMQ		33	0011 | 0011	A → $Q_{7:4}$	None	Copy A, RAM to Q
		3C	0011 | 1100	RAM(B) → $Q_{3:0}$		
CQMA		33	0011 | 0011	$Q_{7:4}$ → RAM(B)	None	Copy Q to RAM, A
		2C	0010 | 1100	$Q_{3:0}$ → A		
LD	r	–5	00 | r | 0101 (r=0:3)	RAM(B) → A Br⊕r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23	0010 | 0011	RAM(r,d) → A	None	Load A with RAM pointed to directly by r,d
		––	0 | r | d			
LQID		BF	1011 | 1111	ROM($PC_{10:8}$,A,M) → Q SB → SC	None	Load Q Indirect (Note 3)
RMB	0	4C	0100 | 1100	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	0100 | 0101	0 → $RAM(B)_1$		
	2	42	0100 | 0010	0 → $RAM(B)_2$		
	3	43	0100 | 0011	0 → $RAM(B)_3$		
SMB	0	4D	0100 | 1101	1 → $RAM(B)_0$	None	Set RAM Bit
	1	47	0100 | 0111	1 → $RAM(B)_1$		
	2	46	0100 | 0110	1 → $RAM(B)_2$		
	3	4B	0100 | 1011	1 → $RAM(B)_3$		

Instruction Set (Continued)

Table III. COP444C/445C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS (Continued)						
STII	y	7–	|0111| y |	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate 1 and Increment Bd
X	r	–6	|00| r |0110| (r=0:3)	RAM(B) ⟷ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 – –	|0010|0011| |1| r | d |	RAM(r,d) ⟷ A	None	Exchange A with RAM Pointed to Directly by r,d
XDS	r	–7	|00|r|0111| (r=0:3)	RAM(B) ⟷ A Bd–1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd. Exclusive-OR Br with r
XIS	r	–4	|00| r |0100| (r=0:3)	RAM(B) ⟷ A Bd+1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	|0101|0000|	A → Bd	None	Copy A to Bd
CBA		4E	|0100|1110|	Bd → A	None	Copy Bd to A
LBI	r,d	– –	|00|r|(d–1)| (r=0:3; d=0,9:15) or	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 6)
		33 – –	|0011|0011| |1| r | d | (any r, any d)			
LEI	y	33 6–	|0011|0011| |0110| y |	y → EN	None	Load EN Immediate (Note 7)
XABR		12	|0001|0010|	A ⟷ Br	None	Exchange A with Br (Note 8)
TEST INSTRUCTIONS						
SKC		20	|0010|0000|		C="1"	Skip if C is True
SKE		21	|0010|0001|		A=RAM(B)	Skip if A Equals RAM
SKGZ		33 21	|0011|0011| |0010|0001|		$G_{3:0}=0$	Skip if G is Zero (all 4 bits)
SKGBZ		33	|0011|0011|	1st byte		Skip if G Bit is Zero
	0	01	|0000|0001|	2nd byte	$G_0=0$	
	1	11	|0001|0001|	2nd byte	$G_1=0$	
	2	03	|0000|0011|	2nd byte	$G_2=0$	
	3	13	|0001|0011|	2nd byte	$G_3=0$	
SKMBZ	0	01	|0000|0001|		$RAM(B)_0=0$	Skip if RAM Bit is Zero
	1	11	|0001|0001|		$RAM(B)_1=0$	
	2	03	|0000|0011|		$RAM(B)_2=0$	
	3	13	|0001|0011|		$RAM(B)_3=0$	
SKT		41	|0100|0001|		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)

Instruction Set (Continued)

Table III. COP444C/445C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0011 | 0011 0010 | 1010	G → A	None	Input G Ports to A
ININ		33 28	0011 | 0011 0010 | 1000	IN → A	None	Input IN Inputs to A (Note 2)
INIL		33 29	0011 | 0011 0010 | 1001	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Note 3)
INL		33 2E	0011 | 0011 0010 | 1110	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM,A
OBD		33 3E	0011 | 0011 0011 | 1110	Bd → D	None	Output Bd to D Outputs
OGI	y	33 5–	0011 | 0011 0101 | y	y → G	None	Output to G Ports Immediate
OMG		33 3A	0011 | 0011 0011 | 1010	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0100 | 1111	A ⟷ SIO, C → SKL	None	Exchange A with SIO (Note 3)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The ININ instruction is not available on the 24-pin packages since these devices do not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B(Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register.)

Note 8: For 2K ROM devices, A ⟷ Br (0 → A3). For 1K ROM devices, A ⟷ Br (0,0 → A3, A2).

Note 9: Do not use CTMA instruction when dual-clock option is selected and part is running from D_0 clocks.

Description of Selected Instructions

XAS INSTRUCTION

XAS (Exchange A with SIO) copies C to the SKL latch and exchanges the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. If SIO is selected as a shift register, an XAS instruction can be performed once every 4 instruction cycles to effect a continuous data stream.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC10:PC8,A,M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC+1 → SA → SB → SC) and replaces the least significant 8 bits of the PC as follows: A → PC(7:4), RAM(B) → PC(3:0), leaving PC(10), PC(9) and PC(8) unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost.

Note: LQID uses 2 instruction cycles if executed, one if skipped.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, PC10:8,A,M. PC10,PC9 and PC8 are not affected by JID.

Note: JID uses 2 instruction cycles if executed, one if skipped.

SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of the T counter overflow latch (see internal logic, above), executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

Note: If the most significant bit of the T counter is a 1 when a CAMT instruction loads the counter, the overflow flag will be set. The following sample of codes should be used when loading the counter:

```
CAMT   ; load T counter
SKT    ; skip if overflow flag is set and reset it
NOP
```

IT INSTRUCTION

The IT (idle till timer) instruction halts the processor and puts it in an idle state until the time-base counter overflows. This idle state reduces current drain since all logic (except the oscillator and time base counter) is stopped.

INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL3 and IL0, CKO and 0 into A. The IL3 and IL0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN3 and IN0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A0 is input into A1. IL latches are cleared on reset. IL latches are not available on the COP445C/425C, and COP426C.

INSTRUCTION SET NOTES

a. The first word of a program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, they are still fetched from the program memory. Thus program paths take the same number of cycles whether instructions are skipped or executed except for JID, and LQID.

c. The ROM is organized into pages of 64 words each. The Program Counter is a 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID is the last word of a page, it operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a JID or LQID located in the last word of every fourth page (i.e. hex address 0FF, 1FF, 2FF, 3FF, 4FF, etc.) will access data in the next group of four pages.

Note: The COP424C/425C/426C needs only 10 bits to address its ROM. Therefore, the eleventh bit (P10) is ignored.

Power Dissipation

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to insure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal or resonator generated clock input will draw additional current. An R/C oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate operating current drain.

$$I_{CO} = I_Q + V \times 40 \times Fi + V \times 1400 \times Fi/Dv$$

where I_{CO} = chip operating current drain in microamps
I_Q quiescent leakage current (from curve)
Fi CKI frequency in MegaHertz
V chip V_{CC} in volts
Dv divide by option selected

For example at 5 volts V_{CC} and 400 kHz (divide by 4)

$I_{CO} = 20 + 5 \times 40 \times 0.4 + 5 \times 1400 \times 0.4/4$

$I_{CO} = 20 + 80 + 700 = 800\ \mu A$

At 2.4 volts V_{CC} and 30 kHz (divide by 4)

$I_{CO} = 6 + 2.4 \times 40 \times 0.03 + 2.4 \times 1400 \times 0.03/4$

$I_{CO} = 6 + 2.88 + 25.2 = 34.08\ \mu A$

Power Dissipation (Continued)

If an IT instruction is executed, the chip goes into the IDLE mode until the timer overflows. In IDLE mode, the current drain can be calculated from the following equation:

$$Ici = I_Q + V \times 40 \times Fi$$

For example, at 5 volts V_{CC} and 400 kHz

$$Ici = 20 + 5 \times 40 \times 0.4 = 100\ \mu A$$

The total average current will then be the weighted average of the operating current and the idle current:

$$Ita = I_{CO} \times \frac{To}{To+Ti} + Ici \times \frac{Ti}{To+Ti}$$

where: Ita = total average current
I_{CO} = operating current
Ici = idle current
To = operating time
Ti = idle time

I/O OPTIONS

Outputs have the following optional configurations, illustrated in *Figure 11*:

a. Standard — A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b. Low Current — This is the same configuration as a. above except that the sourcing current is much less.

c. Open Drain — An N-channel device to ground only, allowing external pull-up as required by the user's application.

d. Standard TRI-STATE L Output — A CMOS output buffer similar to a. which may be disabled by program control.

e. Low-Current TRI-STATE L Output — This is the same as d. above except that the sourcing current is much less.

f. Open-Drain TRI-STATE L Output — This has the N-channel device to ground only.

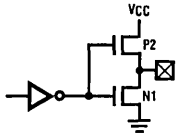
All inputs have the following options:

g. Input with on chip load device to V_{CC}.

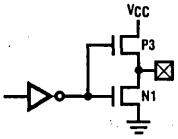
h. Hi-Z input which must be driven by the users logic.

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available: Select the low-current output option. Now, by setting the output registers to a logic "1" level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion the Q registers must be set to a logic "1" level and the L drivers MUST BE ENABLED by an LEI instruction (see description above).

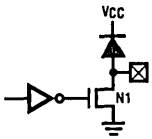
All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 12* for each of these devices to allow the designer to effectively use these I/O configurations.



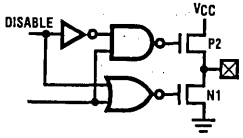
a. Standard Push-Pull Output



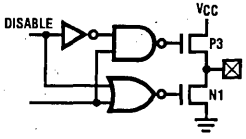
b. Low Current Push-Pull Output



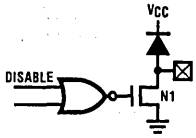
c. Open-Drain Output



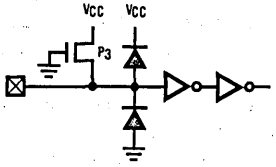
d. Standard TRI-STATE "L" Output



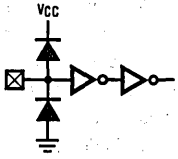
e. Low Current TRI-STATE "L" Output



f. Open Drain TRI-STATE "L" Output



g. Input with Load



h. Hi-Z Input

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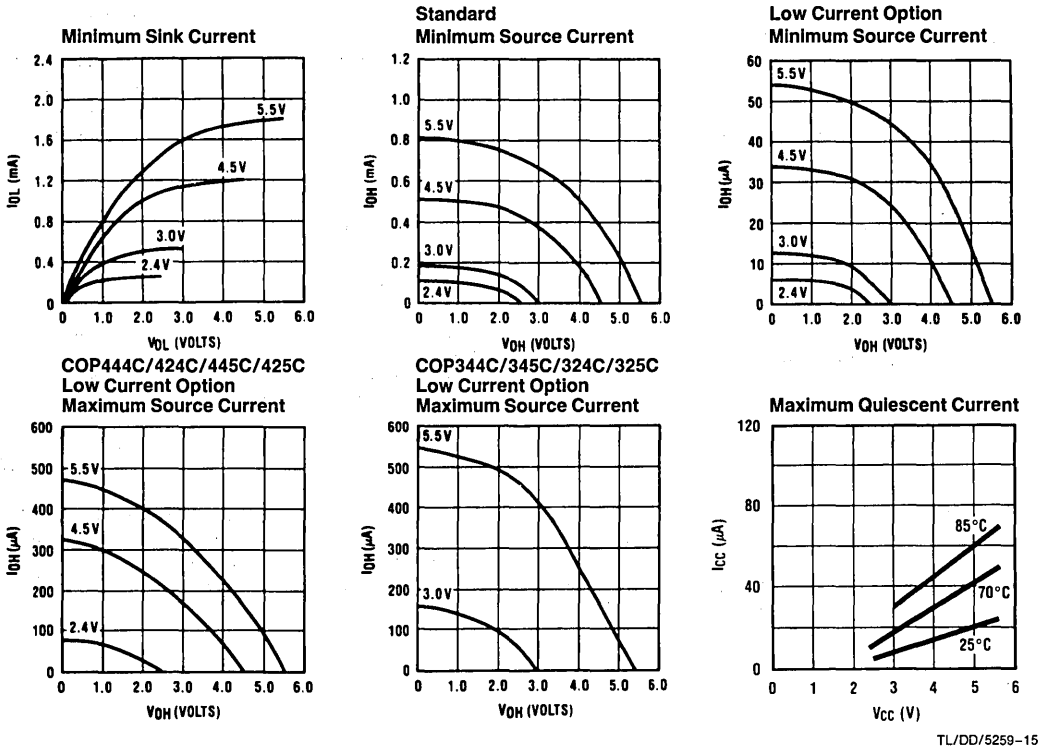
FIGURE 11. Input/Output Configurations

Power Dissipation (Continued)



TL/DD/5259–15

FIGURE 12. Input/Output Characteristics

Option List

The COP444C/445C/424C/425C/COP426C mask-programmable options are assigned numbers which correspond with the COP444C/424C pins.

The following is a list of options. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

PLEASE FILL OUT THE OPTION TABLE on the next page. Xerox the option data and send it in with your disk or EPROM.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Pin
- = 0: clock generator output to crystal/resonator
- = 1: HALT I/O port
- = 2: general purpose input with load device to V_{CC}
- = 3: general purpose input, high-Z

Option 3: CKI input
- = 0: Crystal controlled oscillator input divide by 4
- = 1: Crystal controlled oscillator input divide by 8
- = 2: Crystal controlled oscillator input divide by 16
- = 4: Single-pin RC controlled oscillator (divide by 4)
- = 5: External oscillator input divide by 4
- = 6: External oscillator input divide by 8
- = 7: External oscillator input divide by 16

Option 4: $\overline{\text{RESET}}$ input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 5: L7 Driver
- = 0: Standard TRI-STATE push-pull output
- = 1: Low-current TRI-STATE push-pull output
- = 2: Open-drain TRI-STATE output

Option 6: L6 Driver — (same as option 5)

Option 7: L5 Driver — (same as option 5)

Option 8: L4 Driver — (same as option 5)

Option 9: IN1 input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 10: IN2 input — (same as option 9)

Option 11 = 0: V_{CC} Pin — no option available

Option 12: L3 Driver — (same as option 5)

Option 13: L2 Driver — (same as option 5)

Option 14: L1 Driver — (same as option 5)

Option 15: L0 Driver — (same as option 5)

Option 16: SI input — (same as option 9)

Option 17: SO Driver
- = 0: Standard push-pull output
- = 1: Low-current push-pull output
- = 2: Open-drain output

Option List (Continued)

Option 18: SK Driver — (same as option 17)
Option 19: IN0 Input — (same as option 9)
Option 20: IN3 Input — (same as option 9)
Option 21: G0 I/O Port — (same as option 17)
Option 22: G1 I/O Port — (same as option 17)
Option 23: G2 I/O Port — (same as option 17)
Option 24: G3 I/O Port — (same as option 17)
Option 25: D3 Output — (same as option 17)
Option 26: D2 Output — (same as option 17)
Option 27: D1 Output — (same as option 17)
Option 28: D0 Output — (same as option 17)
Option 29: Internal Initialization Logic
=0: Normal operation
=1: No internal initialization logic
Option 30: Dual Clock
=0: Normal operation
=1: Dual Clock. D0 RC oscillator
=2: Dual Clock. D0 ext. clock input
} (opt. #28 must=2)
Option 31: Timer
=0: No Option Available
Option 32: Microbus
=0: Normal
=1: Microbus (opt. #31 must=0)
Option 33: COP bonding
(1k and 2K Microcontroller)
=0: 28-pin package
=1: 24-pin package
=2: Same die purchased in both 24 and 28 pin version.
(1K Microcontroller only)
=3: 20-pin package
=4: 28- and 20-pin package
=5: 24- and 20-pin package
=6: 28-, 24- and 20-pin package

Note:—if opt. #33=1 or 2 then opt. #9, 10, 19, 20 and 32 must = 0—if opt. #33=3, 4, 5 or 6 then opt. #9, 10, 19, 20, 21, 22, 30 and 32 must = 0.

Option Table

The following option information is to be sent to National along with the EPROM.

OPTION DATA		OPTION DATA	
OPTION 1 VALUE = 0	IS: GROUND PIN	OPTION 17 VALUE = _____	IS: SO DRIVER
OPTION 2 VALUE = _____	IS: CKO PIN	OPTION 18 VALUE = _____	IS: SK DRIVER
OPTION 3 VALUE = _____	IS: CKI INPUT	OPTION 19 VALUE = _____	IS: IN0 INPUT
OPTION 4 VALUE = _____	IS: RESET INPUT	OPTION 20 VALUE = _____	IS: IN3 INPUT
OPTION 5 VALUE = _____	IS: L(7) DRIVER	OPTION 21 VALUE = _____	IS: G0 I/O PORT
OPTION 6 VALUE = _____	IS: L(6) DRIVER	OPTION 22 VALUE = _____	IS: G1 I/O PORT
OPTION 7 VALUE = _____	IS: L(5) DRIVER	OPTION 23 VALUE = _____	IS: G2 I/O PORT
OPTION 8 VALUE = _____	IS: L(4) DRIVER	OPTION 24 VALUE = _____	IS: G3 I/O PORT
OPTION 9 VALUE = _____	IS: IN1 INPUT	OPTION 25 VALUE = _____	IS: D3 OUTPUT
OPTION 10 VALUE = _____	IS: IN2 INPUT	OPTION 26 VALUE = _____	IS: D2 OUTPUT
OPTION 11 VALUE = _____	IS: VCC PIN	OPTION 27 VALUE = _____	IS: D1 OUTPUT
OPTION 12 VALUE = _____	IS: L(3) DRIVER	OPTION 28 VALUE = _____	IS: D0 OUTPUT
OPTION 13 VALUE = _____	IS: L(2) DRIVER	OPTION 29 VALUE = _____	IS: INT INIT LOGIC
OPTION 14 VALUE = _____	IS: L(1) DRIVER	OPTION 30 VALUE = _____	IS: DUAL CLOCK
OPTION 15 VALUE = _____	IS: L(0) DRIVER	OPTION 31 VALUE = 0	IS: TIMER
OPTION 16 VALUE = _____	IS: SI INPUT	OPTION 32 VALUE = _____	IS: MICROBUS
		OPTION 33 VALUE = _____	IS: COP BONDING

National Semiconductor

COP620C/COP622C/COP640C/COP642C/ COP820C/COP822C/COP840C/COP842C/ COP920C/COP922C/COP940C/COP942C Single-Chip microCMOS Microcontrollers

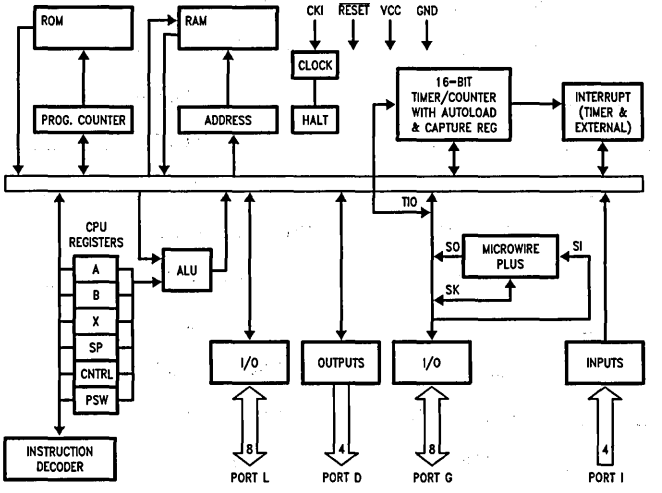
General Description

The COP820C and COP840C are members of the COPS™ microcontroller family. They are fully static parts, fabricated using double-metal silicon gate microCMOS technology. This low cost microcontroller is a complete microcomputer containing all system timing, interrupt logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS™ serial I/O, a 16-bit timer/counter with capture register and a multi-sourced interrupt. Each I/O pin has software selectable options to adapt the COP820C and COP840C to the specific application. The part operates over a voltage range of 2.5 to 6.0V. High throughput is achieved with an efficient, regular instruction set operating at a 1 microsecond per instruction rate.

Features

- Low Cost 8-bit microcontroller
- Fully static CMOS
- 1 μs instruction time (10 MHz clock)
- Low current drain (2.2 mA at 3 μs instruction rate) Low current static HALT mode (Typically < 1 μA)
- Single supply operation: 2.5 to 6.0V
- 1024 bytes ROM/64 Bytes RAM—COP820C
- 2048 bytes ROM/128 Bytes RAM—COP840C
- 16-bit read/write timer operates in a variety of modes
  - — Timer with 16-bit auto reload register
  - — 16-bit external event counter
  - — Timer with 16-bit capture register (selectable edge)
- Multi-source interrupt
  - — Reset master clear
  - — External interrupt with selectable edge
  - — Timer interrupt or capture interrupt
  - — Software interrupt
- 8-bit stack pointer (stack in RAM)
- Powerful instruction set, most instructions single byte
- BCD arithmetic instructions
- MICROWIRE/PLUS serial I/O
- 28 pin package (optionally 20 pin package)
- 24 input/output pins (28-pin package)
- Software selectable I/O options (TRI-STATE®, push-pull, weak pull-up)
- Schmitt trigger inputs on Port G
- Temperature ranges: 0°C to +70°C, −40°C to +85°C, −55°C to +125°C
- Form Factor emulation devices
- Fully supported by National's development system

Block Diagram



TL/DD/9103–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	50 mA
Total Current out of GND Pin (Sink)	60 mA
Storage Temperature Range	−65°C to +140°C

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics COP92XC, COP94XC; 0°C ≤ T_A ≤ +70°C unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage					
COP9XXC		2.3		4.0	V
COP9XXCH		4.0		6.0	V
Power Supply Ripple (Note 1)	Peak to Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, tc = 1 μs			7.5	mA
CKI = 4 MHz	V_{CC} = 6V, tc = 2.5 μs			4.0	mA
CKI = 4 MHz	V_{CC} = 4V, tc = 2.5 μs			2.0	mA
CKI = 1 MHz	V_{CC} = 4V, tc = 10 μs			1.2	mA
HALT Current	V_{CC} = 6V, CKI = 0 MHz		<0.7	8.0	μA
(Note 3)	V_{CC} = 4V, CKI = 0 MHz		<0.4	5.0	μA
Input Levels					
$\overline{\text{RESET}}$, CKI					
Logic High		0.9 V_{CC}			V
Logic Low				0.1 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6.0V	−1		+1	μA
Input Pullup Current	V_{CC} = 6.0V	40		250	μA
G Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
	V_{CC} = 2.3V, V_{OH} = 1.6V	0.2			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1.0V	10			mA
	V_{CC} = 2.3V, V_{OL} = 0.4V	2			mA
All Others					
Source (Weak Pull-Up)	V_{CC} = 4.5V, V_{OH} = 3.2V	10		110	μA
	V_{CC} = 2.3V, V_{OH} = 1.6V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
	V_{CC} = 2.3V, V_{OH} = 1.6V	0.2			
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.3V, V_{OL} = 0.4V	0.7			
TRI-STATE Leakage	V_{CC} = 6.0V	−1.0		+1.0	μA
Allowable Sink/Source Current Per Pin					
D Outputs (Sink)				15	mA
All Others				3	mA
Maximum Input Current (Note 4) Without Latchup (Room Temp)	Room Temp			±100	mA
RAM Retention Voltage, Vr	500 ns Rise and Fall Time (Min)	2.0			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

DC Electrical Characteristics (Continued)

Note 1: Rate of voltage change must be less than 0.5V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports TRI-STATE and tied to ground, all outputs low and tied to ground.

Note 4: Except pin G7: +100 mA, −25 mA (COP920C only). Sampled and not 100% tested. Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

AC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (tc)					
Ext., Crystal/Resonator	$V_{CC} \ge 4.0V$	1		DC	μs
(Div-by 10)	$2.3V \le V_{CC} \le 4.0V$	2.5		DC	μs
R/C Oscillator Mode	$V_{CC} \ge 4.0V$	3		DC	μs
(Div-by 10)	$2.3V \le V_{CC} \le 4.0V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 5)	fr = Max	40		60	%
Rise Time (Note 5)	fr = 10 MHz Ext Clock			12	ns
Fall Time (Note 5)	fr = 10 MHz Ext Clock			8	ns
Inputs					
t_{SETUP}	$V_{CC} \ge 4.0V$	200			ns
	$2.3V \le V_{CC} \le 4.0V$	500			ns
t_{HOLD}	$V_{CC} \ge 4.0V$	60			ns
	$2.3V \le V_{CC} \le 4.0V$	150			ns
Output Propagation Delay	$C_L = 100$ pF, $R_L = 2.2$ kΩ				
t_{PD1}, t_{PD0}					
SO, SK	$V_{CC} \ge 4.0V$			0.7	μs
	$2.5V \le V_{CC} \le 4.0V$			1.75	μs
All Others	$V_{CC} \ge 4.0V$			1	μs
	$2.5V \le V_{CC} \le 4.0V$			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		t_C			
Interrupt Input Low Time		t_C			
Timer Input High Time		t_C			
Timer Input Low Time		t_C			
Reset Pulse Width		1.0			μs

Note 5: Parameter sampled (not 100% tested).

COP820C/COP822C/COP840C/COP842C
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	50 mA
Total Current out of GND Pin (Sink)	60 mA
Storage Temperature Range	−65°C to +140°C

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics COP82XC, COP84XC: $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage		2.5		6.0	V
Power Supply Ripple (Note 1)	Peak to Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, tc = 1 μs			7.5	mA
CKI = 4 MHz	V_{CC} = 6V, tc = 2.5 μs			4.0	mA
CKI = 4 MHz	V_{CC} = 4.0V, tc = 2.5 μs			2.0	mA
CKI = 1 MHz	V_{CC} = 4.0V, tc = 10 μs			1.2	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<1	10	μA
Input Levels					
RESET, CKI					
Logic High		0.9 V_{CC}			V
Logic Low				0.1 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6.0V	−2		+2	μA
Input Pullup Current	V_{CC} = 6.0V	40		250	μA
G Port Input Hysteresis			0.35 V_{CC}		V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1.0V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2			mA
All Others					
Source (Weak Pull-Up)	V_{CC} = 4.5V, V_{OH} = 3.2V	10		110	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			
TRI-STATE Leakage		−2.0		+2.0	μA
Allowable Sink/Source Current Per Pin					
D Outputs (Sink)				15	mA
All Others				3	mA
Maximum Input Current (Note 4) Without Latchup (Room Temp)	Room Temp			±100	mA
RAM Retention Voltage, Vr	500 ns Rise and Fall Time (Min)	2.0			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

Note 1: Rate of voltage change must be less than 0.5V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports TRI-STATE and tied to ground, all outputs low and tied to ground.

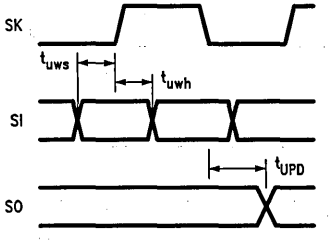
Note 4: Except pin G7: +100 mA, −25 mA (COP820C only). Sampled and not 100% tested. Pins G6 and RESET are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

AC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (tc)					
Ext. or Crystal/Resonator	$V_{CC} \ge 4.5V$	1		DC	μs
(Div-by 10)	$2.5V \le V_{CC} < 4.5V$	2.5		DC	μs
R/C Oscillator Mode	$V_{CC} \ge 4.5V$	3		DC	μs
(Div-by 10)	$2.5V \le V_{CC} < 4.5V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 6)	fr = Max	40		60	%
Rise Time (Note 6)	fr = 10 MHz Ext Clock			12	ns
Fall Time (Note 6)	fr = 10 MHz Ext Clock			8	ns
Inputs					
t_{SETUP}	$V_{CC} \ge 4.5V$	200			ns
	$2.5V \le V_{CC} < 4.5V$	500			ns
t_{HOLD}	$V_{CC} \ge 4.5V$	60			ns
	$2.5V \le V_{CC} < 4.5V$	150			ns
Output Propagation Delay	$C_L = 100$ pF, $R_L = 2.2$ kΩ				
t_{PD1}, t_{PD0}					
SO, SK	$V_{CC} \ge 4.5V$			0.7	μs
	$2.5V \le V_{CC} < 4.5V$			1.75	μs
All Others	$V_{CC} \ge 4.5V$			1	μs
	$2.5V \le V_{CC} < 4.5V$			2.5	μs
MICROWIRE Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output					
Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		t_C			
Interrupt Input Low Time		t_C			
Timer Input High Time		t_C			
Timer Input Low Time		t_C			
Reset Pulse Width		1.0			μs

Note 5: Parameter sampled (not 100% tested).

Timing Diagram



TL/DD/9103–19

FIGURE 2. MICROWIRE/PLUS Timing

COP620C/COP622C/COP640C/COP642C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6V
Voltage at any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	40 mA
Total Current out of GND Pin (Sink)	48 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

COP62XC, COP64XC: $-55°C \le T_A \le +125°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage		4.5		5.5	V
Power Supply Ripple (Note 1)	Peak to Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 5.5V, tc = 1 μs			7.5	mA
CKI = 4 MHz	V_{CC} = 5.5V, tc = 2.5 μs			4	mA
HALT Current (Note 3)	V_{CC} = 5.5V, CKI = 0 MHz		<10	30	μA
Input Levels					
RESET, CKI					
Logic High		0.9 V_{CC}			V
Logic Low				0.1 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 5.5V	−5		+5	μA
Input Pullup Current	V_{CC} = 4.5V	35		300	μA
G Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.8V	0.35			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1.0V	9			mA
All Others					
Source (Weak Pull-Up)	V_{CC} = 4.5V, V_{OH} = 3.2V	9		120	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.8V	0.35			mA
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.4			mA
TRI-STATE Leakage		−5.0		+5.0	μA
Allowable Sink/Source Current Per Pin					
D Outputs (Sink)				12	mA
All Others				2.5	mA
Maximum Input Current (Room Temp) Without Latchup (Note 5)	Room Temp			±100	mA
RAM Retention Voltage, Vr	500 ns Rise and Fall Time (Min)	2.5			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

Note 1: Rate of voltage change must be less than 0.5V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports TRI-STATE and tied to ground, all outputs low and tied to ground.

Note 4: Except pin G7: +100 mA, −25 mA (COP620C only). Sampled and not 100% tested. Pins G6 and RESET are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

COP620C/COP622C/COP640C/COP642C

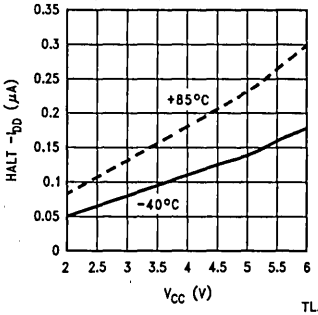
AC Electrical Characteristics $-55°C \le T_A \le +125°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (tc)					
Ext. or Crystal/Resonant (Div-by 10)	$V_{CC} \ge 4.5V$	1		DC	μs
CKI Clock Duty Cycle (Note 6)	fr = Max	40		60	%
Rise Time (Note 6)	fr = 10 MHz Ext Clock			12	ns
Fall Time (Note 6)	fr = 10 MHz Ext Clock			8	ns
Inputs					
t_{SETUP}	$V_{CC} \ge 4.5V$	220			ns
t_{HOLD}	$V_{CC} \ge 4.5V$	66			ns
Output Propagation Delay t_{PD1}, t_{PD0}	R_L = 2.2k, C_L = 100 pF				
SO, SK	$V_{CC} \ge 4.5V$			0.8	μs
All Others	$V_{CC} \ge 4.5V$			1.1	μs
MICROWIRE Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Valid Time (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		t_C			
Interrupt Input Low Time		t_C			
Timer Input High Time		t_C			
Timer Input Low Time		t_C			
Reset Pulse Width		1			μs

Note 5: Parameter sampled (not 100% tested).

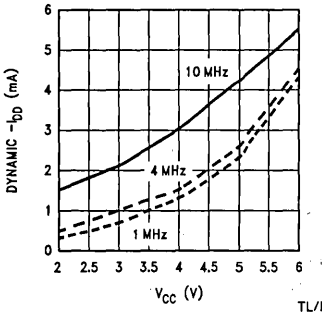
Typical Performance Characteristics ($-40°C \le T_A \le +85°C$)

Halt—I_{DD}



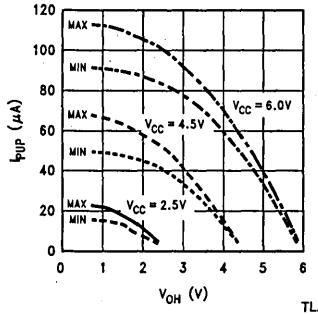
TL/DD/9103–20

Dynamic—I_{DD} (Crystal Clock Option)



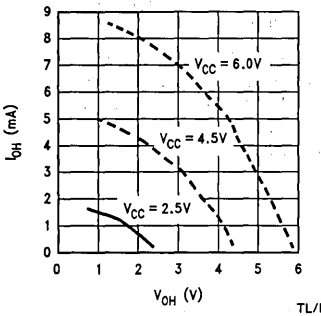
TL/DD/9103–21

Port L/G Weak Pull-Up Source Current



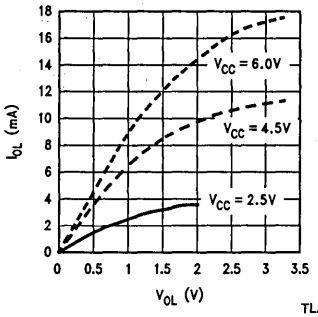
TL/DD/9103–22

Port L/G Push-Pull Source Current



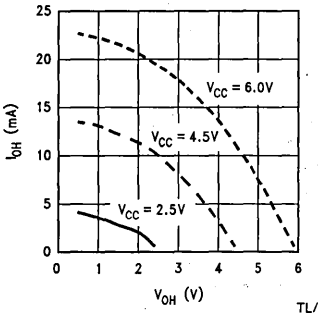
TL/DD/9103–23

Port L/G Push-Pull Sink Current



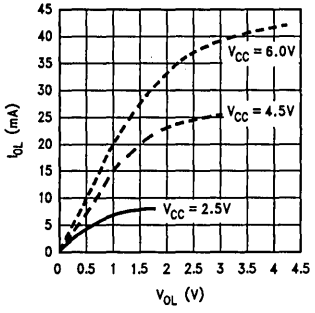
TL/DD/9103–24

Port D Source Current



TL/DD/9103–25

Port D Sink Current

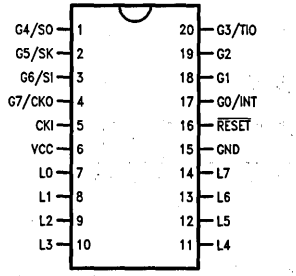


TL/DD/9103–26

Connection Diagrams

DUAL-IN-LINE PACKAGE

20 DIP

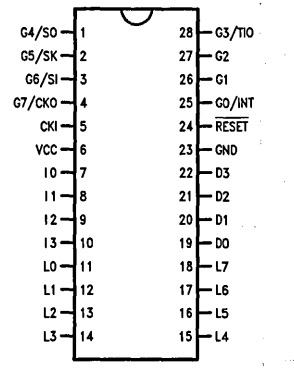


TL/DD/9103-3

Top View

Order Number COP622C-XXX/N, COP642C-XXX/N, COP822C-XXX/N, COP842C-XXX/N, COP922C-XXX/N or COP942C-XXX/N
See NS Package Number N20A

28 DIP

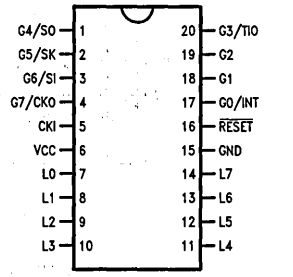


TL/DD/9103-5

Order Number COP620C-XXX/N, COP640C-XXX/N, COP820C-XXX/N, COP840C-XXX/D, COP920C-XXX/N or COP940C-XXX/N
See NS Package Number N28B

SURFACE MOUNT

20 SO Wide

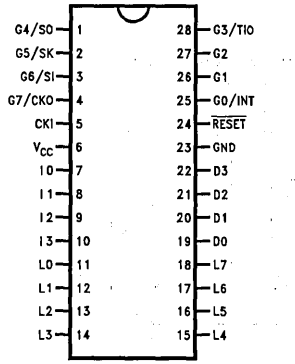


TL/DD/9103-3

Top View

Order Number COP822C-XXX/WM, COP842C-XXX/WM, COP922C-XXX/WM or COP942C-XXX/WM
See NS Package Number M20B

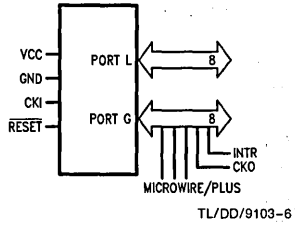
28-Lead SO P/N



TL/DD/9103-18

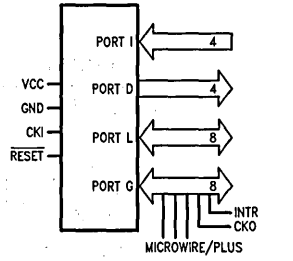
Order Number COP820C-XXX/WM, COP840C-XXX/WM, COP920C-XXX/WM or COP940C-XXX/WM
See NS Package Number M28A

20 DIP/SO



TL/DD/9103-6

28 DIP/SO



TL/DD/9103-8

FIGURE 3

Pin Descriptions

V_{CC} and GND are the power supply pins.

CKI is the clock input. This can come from an external source, a R/C generated oscillator or a crystal (in conjunction with CKO). See Oscillator description.

$\overline{\text{RESET}}$ is the master reset input. See Reset description.

PORT I is a four bit Hi-Z input port.

PORT L is an 8-bit I/O port.

There are two registers associated with each L I/O port: a data register and a configuration register. Therefore, each L I/O bit can be individually configured under software control as shown below:

Port L Config.	Port L Data	Port L Setup
0	0	Hi-Z Input (TRI-STATE)
0	1	Input With Weak Pull-Up
1	0	Push-Pull "0" Output
1	1	Push-Pull "1" Output

Three data memory address locations are allocated for these ports, one for data register, one for configuration register and one for the input pins.

PORT G is an 8-bit port with 6 I/O pins (G0–G5) and 2 input pins (G6, G7). All eight G-pins have Schmitt Triggers on the inputs. The G7 pin functions as an input pin under normal operation and as the continue pin to exit the HALT mode. There are two registers with each I/O port: a data register and a configuration register. Therefore, each I/O bit can be individually configured under software control as shown below.

Port G Config.	Port G Data	Port G Setup
0	0	Hi-Z Input (TRI-STATE)
0	1	Input With Weak Pull-Up
1	0	Push-Pull "0" Output
1	1	Push-Pull "1" Output

Three data memory address locations are allocated for these ports, one for data register, one for configuration register and one for the input pins. Since G6 and G7 are input only pins, any attempt by the user to set them up as outputs by writing a one to the configuration register will be disregarded. Reading the G6 and G7 configuration bits will return zeros. Note that the chip will be placed in the HALT mode by setting the G7 data bit.

Six bits of Port G have alternate features:

G0 INTR (an external interrupt)

G3 TIO (timer/counter input/output)

G4 SO (MICROWIRE serial data output)

G5 SK (MICROWIRE clock I/O)

G6 SI (MICROWIRE serial data input)

G7 CKO crystal oscillator output (selected by mask option) or HALT restart input (general purpose input)

Pins G1 and G2 currently do not have any alternate functions.

PORT D is a four bit output port that is set high when $\overline{\text{RESET}}$ goes low.

Functional Description

Figure 1 shows the block diagram of the internal architecture. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device.

ALU AND CPU REGISTERS

The ALU can do an 8-bit addition, subtraction, logical or shift operation in one cycle time.

There are five CPU registers:

A is the 8-bit Accumulator register

PU is the upper 7 bits of the program counter (PC)

PL is the lower 8 bits of the program counter (PC)

B is the 8-bit address register, can be auto incremented or decremented.

X is the 8-bit alternate address register, can be incremented or decremented.

SP is the 8-bit stack pointer, points to subroutine stack (in RAM).

B, X and SP registers are mapped into the on chip RAM. The B and X registers are used to address the on chip RAM. The SP register is used to address the stack in RAM during subroutine calls and returns.

PROGRAM MEMORY

Program memory for the COP820C consists of 1024 bytes of ROM (2048 bytes of ROM for the COP840C). These bytes may hold program instructions or constant data. The program memory is addressed by the 15-bit program counter (PC). ROM can be indirectly read by the LAID instruction for table lookup.

DATA MEMORY

The data memory address space includes on chip RAM, I/O and registers. Data memory is addressed directly by the instruction or indirectly by the B, X and SP registers.

The COP820C has 64 bytes of RAM and the COP840C has 128 bytes of RAM. Sixteen bytes of RAM are mapped as "registers" that can be loaded immediately, decremented or tested. Three specific registers: B, X and SP are mapped into this space, the other bytes are available for general usage.

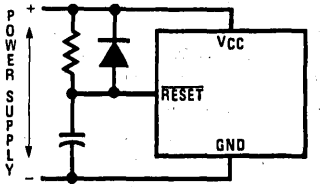
The instruction set permits any bit in memory to be set, reset or tested. All I/O and registers (except the A & PC) are memory mapped; therefore, I/O bits and register bits can be directly and individually set, reset and tested.

RESET

The $\overline{\text{RESET}}$ input when pulled low initializes the microcontroller. Initialization will occur whenever the $\overline{\text{RESET}}$ input is pulled low. Upon initialization, the ports L and G are placed in the TRI-STATE mode and the Port D is set high. The PC, PSW and CNTRL registers are cleared. The data and configuration registers for Ports L & G are cleared.

The external RC network shown in Figure 4 should be used to ensure that the $\overline{\text{RESET}}$ pin is held low until the power supply to the chip stabilizes.

Functional Description (Continued)



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RC ≥ 5X Power Supply Rise Time

FIGURE 4. Recommended Reset Circuit

OSCILLATOR CIRCUITS

Figure 5 shows the three clock oscillator configurations available for the COP820C and COP840C.

A. CRYSTAL OSCILLATOR

The COP820C/COP840C can be driven by a crystal clock. The crystal network is connected between the pins CKI and CKO.

Table I shows the component values required for various standard crystal values.

B. EXTERNAL OSCILLATOR

CKI can be driven by an external clock signal. CKO is available as a general purpose input and/or HALT restart control.

C. R/C OSCILLATOR

CKI is configured as a single pin RC controlled Schmitt trigger oscillator. CKO is available as a general purpose input and/or HALT restart control.

Table II shows the variation in the oscillator frequencies as functions of the component (R and C) values.

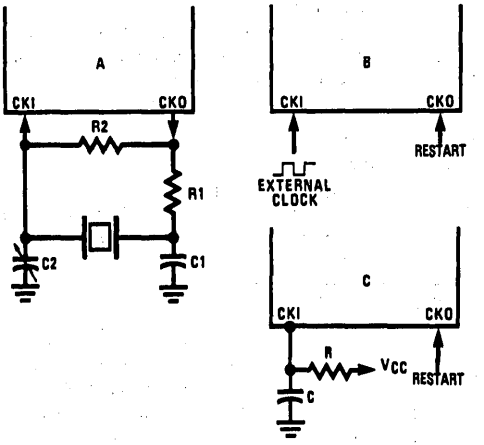

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FIGURE 5. Crystal and R-C Connection Diagrams

OSCILLATOR MASK OPTIONS

The COP820C and COP840C can be driven by clock inputs between DC and 10 MHz.

TABLE I. Crystal Oscillator Configuration, $T_A = 25°C$

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)	Conditions
0	1	30	30–36	10	$V_{CC} = 5V$
0	1	30	30–36	4	$V_{CC} = 5V$
0	1	200	100–150	0.455	$V_{CC} = 5V$

TABLE II. RC Oscillator Configuration, $T_A = 25°C$

R (kΩ)	C (pF)	CKI Freq. (MHz)	Instr. Cycle (μs)	Conditions
3.3	82	2.2 to 2.7	3.7 to 4.6	$V_{CC} = 5V$
5.6	100	1.1 to 1.3	7.4 to 9.0	$V_{CC} = 5V$
6.8	100	0.9 to 1.1	8.8 to 10.8	$V_{CC} = 5V$

Note: 3k ≤ R ≤ 200k, 50 pF ≤ C ≤ 200 pF

Functional Description (Continued)

The COP820C and COP840C microcontrollers have three mask options for configuring the clock input. The CKI and CKO pins are automatically configured upon selecting a particular option.

— Crystal (CKI/10) CKO for crystal configuration

— External (CKI/10) CKO available as G7 input

— R/C (CKI/10) CKO available as G7 input

G7 can be used either as a general purpose input or as a control input to continue from the HALT mode.

CURRENT DRAIN

The total current drain of the chip depends on:

1) Oscillator operating mode—I1

2) Internal switching current—I2

3) Internal leakage current—I3

4) Output source current—I4

5) DC current caused by external input not at V_{CC} or GND—I5

Thus the total current drain, It is given as

$$It = I1 + I2 + I3 + I4 + I5$$

To reduce the total current drain, each of the above components must be minimum.

The chip will draw the least current when in the normal mode. The high speed mode will draw additional current. The R/C mode will draw the most. Operating with a crystal network will draw more current than an external squarewave. Switching current, governed by the equation below, can be reduced by lowering voltage and frequency. Leakage current can be reduced by lowering voltage and temperature. The other two items can be reduced by carefully designing the end-user's system.

$$I2 = C \times V \times f$$

Where

C = equivalent capacitance of the chip.

V = operating voltage

f = CKI frequency

HALT MODE

The COP820C and COP840C support a power saving mode of operation: HALT. The controller is placed in the HALT mode by setting the G7 data bit, alternatively the user can stop the clock input. In the HALT mode all internal processor activities including the clock oscillator are stopped. The fully static architecture freezes the state of the controller and retains all information until continuing. In the HALT mode, power requirements are minimal as it draws only leakage currents and output current. The applied voltage (V_{CC}) may be decreased down to Vr (minimum RAM retention voltage) without altering the state of the machine.

There are two ways to exit the HALT mode: via the $\overline{\text{RESET}}$ or by the CKO pin. A low on the $\overline{\text{RESET}}$ line reinitializes the microcontroller and starts executing from the address 0000H. A low to high transition on the CKO pin causes the microcontroller to continue with no reinitialization from the address following the HALT instruction. This also resets the G7 data bit.

INTERRUPTS

The COP820C and COP840C have a sophisticated interrupt structure to allow easy interface to the real word. There are three possible interrupt sources, as shown below.

A maskable interrupt on external G0 input (positive or negative edge sensitive under software control)

A maskable interrupt on timer underflow or timer capture

A non-maskable software/error interrupt on opcode zero

INTERRUPT CONTROL

The GIE (global interrupt enable) bit enables the interrupt function. This is used in conjunction with ENI and ENTI to select one or both of the interrupt sources. This bit is reset when interrupt is acknowledged.

ENI and ENTI bits select external and timer interrupt respectively. Thus the user can select either or both sources to interrupt the microcontroller when GIE is enabled.

IEDG selects the external interrupt edge (0 = rising edge, 1 = falling edge). The user can get an interrupt on both rising and falling edges by toggling the state of IEDG bit after each interrupt.

IPND and TPND bits signal which interrupt is pending. After interrupt is acknowledged, the user can check these two bits to determine which interrupt is pending. This permits the interrupts to be prioritized under software. The pending flags have to be cleared by the user. Setting the GIE bit high inside the interrupt subroutine allows nested interrupts.

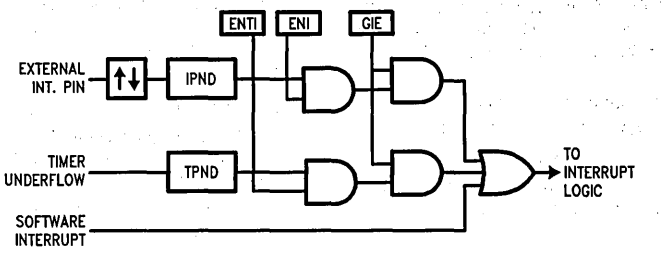
The software interrupt does not reset the GIE bit. This means that the controller can be interrupted by other interrupt sources while servicing the software interrupt.

INTERRUPT PROCESSING

The interrupt, once acknowledged, pushes the program counter (PC) onto the stack and the stack pointer (SP) is decremented twice. The Global Interrupt Enable (GIE) bit is reset to disable further interrupts. The microcontroller then vectors to the address 00FFH and resumes execution from that address. This process takes 7 cycles to complete. At the end of the interrupt subroutine, any of the following three instructions return the processor back to the main program: RET, RETSK or RETI. Either one of the three instructions will pop the stack into the program counter (PC). The stack pointer is then incremented twice. The RETI instruction additionally sets the GIE bit to re-enable further interrupts.

Any of the three instructions can be used to return from a hardware interrupt subroutine. The RETSK instruction should be used when returning from a software interrupt subroutine to avoid entering an infinite loop.

Functional Description (Continued)



TL/DD/9103–11

FIGURE 6. Interrupt Block Diagram

DETECTION OF ILLEGAL CONDITIONS

The COP820C and COP840C incorporate a hardware mechanism that allows it to detect illegal conditions which may occur from coding errors, noise and 'brown out' voltage drop situations. Specifically it detects cases of executing out of undefined ROM area and unbalanced stack situations.

Reading an undefined ROM location returns 00 (hexadecimal) as its contents. The opcode for a software interrupt is also '00'. Thus a program accessing undefined ROM will cause a software interrupt.

Reading an undefined RAM location returns an FF (hexadecimal). The subroutine stack on the COP820C and COP840C grows down for each subroutine call. By initializing the stack pointer to the top of RAM, the first unbalanced return instruction will cause the stack pointer to address undefined RAM. As a result the program will attempt to execute from FFFF (hexadecimal), which is an undefined ROM location and will trigger a software interrupt.

MICROWIRE/PLUS™

MICROWIRE/PLUS is a serial synchronous bidirectional communications interface. The MICROWIRE/PLUS capability enables the COP820C and COP840C to interface with any of National Semiconductor's MICROWIRE peripherals (i.e. A/D converters, display drivers, EEPROMS, etc.) and with other microcontrollers which support the MICROWIRE/PLUS interface. It consists of an 8-bit serial shift register (SIO) with serial data input (SI), serial data output (SO) and serial shift clock (SK). *Figure 7* shows the block diagram of the MICROWIRE/PLUS interface.

The shift clock can be selected from either an internal source or an external source. Operating the MICROWIRE/PLUS interface with the internal clock source is called the Master mode of operation. Similarly, operating the MICROWIRE/PLUS interface with an external shift clock is called the Slave mode of operation.

The CNTRL register is used to configure and control the MICROWIRE/PLUS mode. To use the MICROWIRE/PLUS, the MSEL bit in the CNTRL register is set to one. The SK clock rate is selected by the two bits, S0 and S1, in the CNTRL register. Table III details the different clock rates that may be selected.

TABLE III

S1	S0	SK Cycle Time
0	0	$2t_C$
0	1	$4t_C$
1	x	$8t_C$

where,

t_C is the instruction cycle clock.

MICROWIRE/PLUS OPERATION

Setting the BUSY bit in the PSW register causes the MICROWIRE/PLUS arrangement to start shifting the data. It gets reset when eight data bits have been shifted. The user may reset the BUSY bit by software to allow less than 8 bits to shift. The COP820C and COP840C may enter the MICROWIRE/PLUS mode either as a Master or as a Slave. *Figure 8* shows how two COP820C microcontrollers and several peripherals may be interconnected using the MICROWIRE/PLUS arrangement.

Master MICROWIRE/PLUS Operation

In the MICROWIRE/PLUS Master mode of operation the shift clock (SK) is generated internally by the COP820C. The MICROWIRE/PLUS Master always initiates all data exchanges. (See *Figure 8*). The MSEL bit in the CNTRL register must be set to enable the SO and SK functions onto the G Port. The SO and SK pins must also be selected as outputs by setting appropriate bits in the Port G configuration register. Table IV summarizes the bit settings required for Master mode of operation.

SLAVE MICROWIRE/PLUS OPERATION

In the MICROWIRE/PLUS Slave mode of operation the SK clock is generated by an external source. Setting the MSEL bit in the CNTRL register enables the SO and SK functions onto the G Port. The SK pin must be selected as an input and the SO pin is selected as an output pin by appropriately setting up the Port G configuration register. Table IV summarizes the settings required to enter the Slave mode of operation.

The user must set the BUSY flag immediately upon entering the Slave mode. This will ensure that all data bits sent by the Master will be shifted properly. After eight clock pulses the BUSY flag will be cleared and the sequence may be repeated. (See *Figure 8*.)

Functional Description (Continued)

TABLE IV

G4 Config. Bit	G5 Config. Bit	G4 Fun.	G5 Fun.	G6 Fun.	Operation
1	1	SO	Int. SK	SI	MICROWIRE Master
0	1	TRI-STATE	Int. SK	SI	MICROWIRE Master
1	0	SO	Ext. SK	SI	MICROWIRE Slave
0	0	TRI-STATE	Ext. SK	SI	MICROWIRE Slave

TIMER/COUNTER

The COP820C and COP840C have a powerful 16-bit timer with an associated 16-bit register enabling them to perform extensive timer functions. The timer T1 and its register R1 are each organized as two 8-bit read/write registers. Control bits in the register CNTRL allow the timer to be started and stopped under software control. The timer-register pair can be operated in one of three possible modes. Table V details various timer operating modes and their requisite control settings.

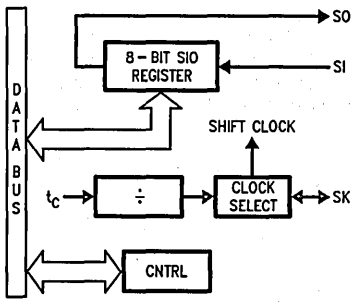


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FIGURE 7. MICROWIRE/PLUS Block Diagram

MODE 1. TIMER WITH AUTO-LOAD REGISTER

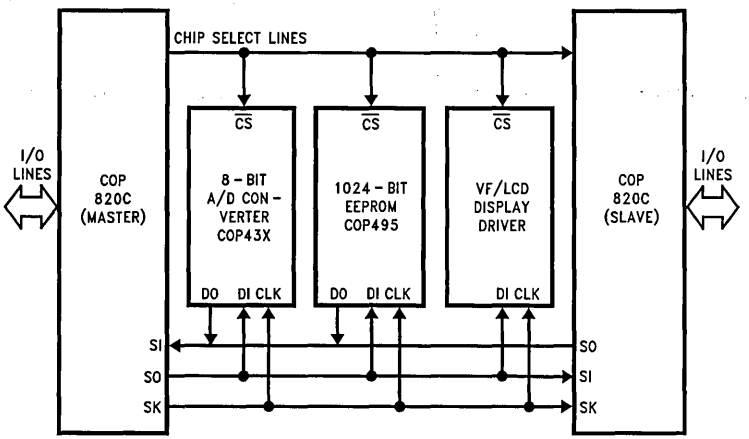
In this mode of operation, the timer T1 counts down at the instruction cycle rate. Upon underflow the value in the register R1 gets automatically reloaded into the timer which continues to count down. The timer underflow can be programmed to interrupt the microcontroller. A bit in the control register CNTRL enables the TIO (G3) pin to toggle upon timer underflows. This allow the generation of square-wave outputs or pulse width modulated outputs under software control. (See *Figure 9*)

MODE 2. EXTERNAL COUNTER

In this mode, the timer T1 becomes a 16-bit external event counter. The counter counts down upon an edge on the TIO pin. Control bits in the register CNTRL program the counter to decrement either on a positive edge or on a negative edge. Upon underflow the contents of the register R1 are automatically copied into the counter. The underflow can also be programmed to generate an interrupt. (See *Figure 9*)

MODE 3. TIMER WITH CAPTURE REGISTER

Timer T1 can be used to precisely measure external frequencies or events in this mode of operation. The timer T1 counts down at the instruction cycle rate. Upon the occurrence of a specified edge on the TIO pin the contents of the timer T1 are copied into the register R1. Bits in the control register CNTRL allow the trigger edge to be specified either as a positive edge or as a negative edge. In this mode the user can elect to be interrupted on the specified trigger edge. (See *Figure 10.*)



TL/DD/9103–13

FIGURE 8. MICROWIRE/PLUS Application

Functional Description (Continued)

TABLE V. Timer Operating Modes

CNTRL Bits 7 6 5	Operation Mode	T Interrupt	Timer Counts On
0 0 0	External Counter W/Auto-Load Reg.	Timer Carry	TIO Pos. Edge
0 0 1	External Counter W/Auto-Load Reg.	Timer Carry	TIO Neg. Edge
0 1 0	Not Allowed	Not Allowed	Not Allowed
0 1 1	Not Allowed	Not Allowed	Not Allowed
1 0 0	Timer W/Auto-Load Reg.	Timer Carry	t_C
1 0 1	Timer W/Auto-Load Reg./Toggle TIO Out	Timer Carry	t_C
1 1 0	Timer W/Capture Register	TIO Pos. Edge	t_C
1 1 1	Timer W/Capture Register	TIO Neg. Edge	t_C

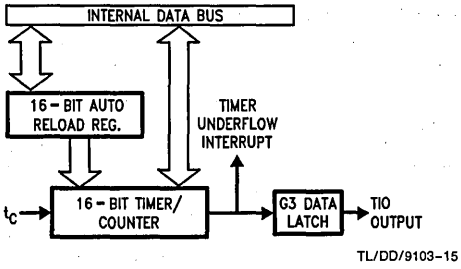


FIGURE 9. Timer/Counter Auto Reload Mode Block Diagram

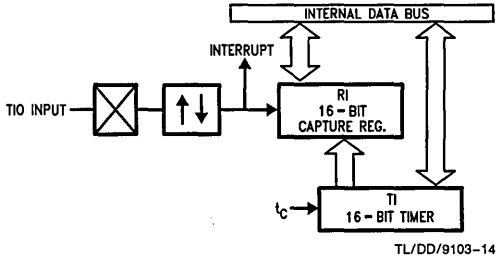


FIGURE 10. Timer Capture Mode Block Diagram

TIMER PWM APPLICATION

Figure 11 shows how a minimal component D/A converter can be built out of the Timer-Register pair in the Auto-Reload mode. The timer is placed in the "Timer with auto reload" mode and the TIO pin is selected as the timer output. At the outset the TIO pin is set high, the timer T1 holds the on time and the register R1 holds the signal off time. Setting TRUN bit starts the timer which counts down at the instruction cycle rate. The underflow toggles the TIO output and copies the off time into the timer, which continues to run. By alternately loading in the on time and the off time at each successive interrupt a PWM frequency can be easily generated.

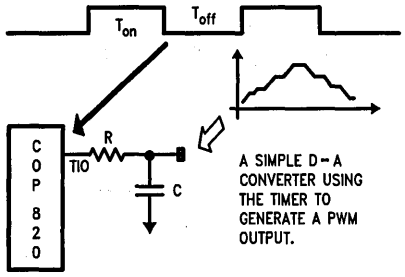


FIGURE 11. Timer Application

Control Registers

CNTRL REGISTER (ADDRESS X'00EE)

The Timer and MICROWIRE/PLUS control register contains the following bits:

S1 & S0 Select the MICROWIRE/PLUS clock divide-by

IEDG External interrupt edge polarity select (0 = rising edge, 1 = falling edge)

MSEL Enable MICROWIRE/PLUS functions SO and SK

TRUN Start/Stop the Timer/Counter (1 = run, 0 = stop)

TC3 Timer input edge polarity select (0 = rising edge, 1 = falling edge)

TC2 Selects the capture mode

TC1 Selects the timer mode

TC1	TC2	TC3	TRUN	MSEL	IEDG	S1	S0

BIT 7 BIT 0

PSW REGISTER (ADDRESS X'00EF)

The PSW register contains the following select bits:

GIE Global interrupt enable

ENI External interrupt enable

BUSY MICROWIRE/PLUS busy shifting

IPND External interrupt pending

ENTI Timer interrupt enable

TPND Timer interrupt pending

C Carry Flag

HC Half carry Flag

HC	C	TPND	ENTI	IPND	BUSY	ENI	GIE

Bit 7 Bit 0

Addressing Modes

REGISTER INDIRECT

This is the "normal" mode of addressing for COP820C and COP840C. The operand is the memory addressed by the B register or X register.

DIRECT

The instruction contains an 8-bit address field that directly points to the data memory for the operand.

IMMEDIATE

The instruction contains an 8-bit immediate field as the operand.

REGISTER INDIRECT (AUTO INCREMENT AND DECREMENT)

This is a register indirect mode that automatically increments or decrements the B or X register after executing the instruction.

RELATIVE

This mode is used for the JP instruction, the instruction field is added to the program counter to get the new program location. JP has a range of from −31 to +32 to allow a one byte relative jump (JP + 1 is implemented by a NOP instruction). There are no 'pages' when using JP, all 15 bits of PC are used.

Memory Map

All RAM, ports and registers (except A and PC) are mapped into data memory address space.

Address	Contents
COP820C	
00 to 2F	On Chip RAM Bytes
30 to 7F	Unused RAM Address Space (Reads as all Ones)
COP840C	
00 to 6F	On Chip RAM Bytes
70 to 7F	Unused RAM Address Space (Reads as all Ones)
COP820C and COP840C	
80 to BF	Expansion Space for on Chip EERAM
C0 to CF	Expansion Space for I/O and Registers
D0 to DF	On Chip I/O and Registers
D0	Port L Data Register
D1	Port L Configuration Register
D2	Port L Input Pins (Read Only)
D3	Reserved for Port L
D4	Port G Data Register
D5	Port G Configuration Register
D6	Port G Input Pins (Read Only)
D7	Port I Input Pins (Read Only)
D8–DB	Reserved for Port C
DC	Port D Data Register
DD–DF	Reserved for Port D
E0 to EF	On Chip Functions and Registers
E0–E7	Reserved for Future Parts
E8	Reserved
E9	MICROWIRE/PLUS Shift Register
EA	Timer Lower Byte
EB	Timer Upper Byte
EC	Timer Autoload Register Lower Byte
ED	Timer Autoload Register Upper Byte
EE	CNTRL Control Register
EF	PSW Register
F0 to FF	On Chip RAM Mapped as Registers
FC	X Register
FD	SP Register
FE	B Register

Reading unused memory locations below 7FH will return all ones. Reading other unused memory locations will return undefined data.

Instruction Set

REGISTER AND SYMBOL DEFINITIONS

Registers

A	8-bit Accumulator register
B	8-bit Address register
X	8-bit Address register
SP	8-bit Stack pointer register
PC	15-bit Program counter register
PU	upper 7 bits of PC
PL	lower 8 bits of PC
C	1-bit of PSW register for carry
HC	Half Carry
GIE	1-bit of PSW register for global interrupt enable

Symbols

[B]	Memory indirectly addressed by B register
[X]	Memory indirectly addressed by X register
Mem	Direct address memory or [B]
Meml	Direct address memory or [B] or Immediate data
Imm	8-bit Immediate data
Reg	Register memory: addresses F0 to FF (Includes B, X and SP)
Bit	Bit number (0 to 7)
←	Loaded with
↔	Exchanged with

Instruction Set

ADD	add	A ← A + Meml
ADC	add with carry	A ← A + Meml + C, C ← Carry HC ← Half Carry
SUBC	subtract with carry	A ← A + $\overline{\text{Meml}}$ +C, C ← Carry HC ← Half Carry
AND	Logical AND	A ← A and Meml
OR	Logical OR	A ← A or Meml
XOR	Logical Exclusive-OR	A ← A xor Meml
IFEQ	IF equal	Compare A and Meml, Do next if A = Meml
IFGT	IF greater than	Compare A and Meml, Do next if A > Meml
IFBNE	IF B not equal	Do next if lower 4 bits of B ≠ Imm
DRSZ	Decrement Reg. ,skip if zero	Reg ← Reg − 1, skip if Reg goes to 0
SBIT	Set bit	1 to bit, Mem (bit = 0 to 7 immediate)
RBIT	Reset bit	0 to bit, Mem
IFBIT	If bit	If bit, Mem is true, do next instr.
X	Exchange A with memory	A ↔ Mem
LD A	Load A with memory	A ← Meml
LD mem	Load Direct memory Immed.	Mem ← Imm
LD Reg	Load Register memory Immed.	Reg ← Imm
X	Exchange A with memory [B]	A ↔ [B] (B ← B±1)
X	Exchange A with memory [X]	A ↔ [X] (X ← X±1)
LD A	Load A with memory [B]	A ← [B] (B ← B±1)
LD A	Load A with memory [X]	A ← [X] (X ← X±1)
LD M	Load Memory Immediate	[B] ← Imm (B ← B±1)
CLRA	Clear A	A ← 0
INCA	Increment A	A ← A + 1
DECA	Decrement A	A ← A − 1
LAID	Load A indirect from ROM	A ← ROM(PU,A)
DCORA	DECIMAL CORRECT A	A ← BCD correction (follows ADC, SUBC)
RRCA	ROTATE A RIGHT THRU C	C → A7 → ... → A0 → C
SWAPA	Swap nibbles of A	A7 ... A4 ↔ A3 ... A0
SC	Set C	C ← 1, HC ← 1
RC	Reset C	C ← 0, HC ← 0
IFC	If C	If C is true, do next instruction
IFNC	If not C	If C is not true, do next instruction
JMPL	Jump absolute long	PC ← ii (ii = 15 bits, 0 to 32k)
JMP	Jump absolute	PC11..0 ← i (i = 12 bits)
JP	Jump relative short	PC ← PC + r (r is −31 to +32, not 1)
JSRL	Jump subroutine long	[SP] ← PL,[SP-1] ← PU,SP-2,PC ← ii
JSR	Jump subroutine	[SP] ← PL,[SP-1] ← PU,SP-2,PC11.. 0 ← i
JID	Jump indirect	PL ← ROM(PU,A)
RET	Return from subroutine	SP+2,PL ← [SP],PU ← [SP-1]
RETSK	Return and Skip	SP+2,PL ← [SP],PU ← [SP-1],Skip next instruction
RETI	Return from Interrupt	SP+2,PL ← [SP],PU ← [SP-1],GIE ← 1
INTR	Generate an interrupt	[SP] ← PL,[SP−1] ← PU,SP-2,PC ← 0FF
NOP	No operation	PC ← PC + 1

Bits 7–4

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
JP -15	JP -31	LD 0F0,#i	DRSZ 0F0	RRCA	RC	ADC A, #i	ADC A, [B]	IFBIT 0,[B]	*	LD B, 0F	IFBNE 0	JSR 0000-00FF	JMP 0000-00FF	JP + 17	INTR	0
JP -14	JP -30	LD 0F1,#i	DRSZ 0F1	*	SC	SUBC A, #i	SUBC A,[B]	IFBIT 1,[B]	*	LD B, 0E	IFBNE 1	JSR 0100-01FF	JMP 0100-01FF	JP + 18	JP + 2	1
JP -13	JP -29	LD 0F2,#i	DRSZ 0F2	X A, [X+]	X A, [B+]	IFEQ A, #i	IFEQ A,[B]	IFBIT 2,[B]	*	LD B, 0D	IFBNE 2	JSR 0200-02FF	JMP 0200-02FF	JP + 19	JP + 3	2
JP -12	JP -28	LD 0F3,#i	DRSZ 0F3	X A, [X−]	X A, [B−]	IFGT A, #i	IFGT A,[B]	IFBIT 3,[B]	*	LD B, 0C	IFBNE 3	JSR 0300-03FF	JMP 0300-03FF	JP + 20	JP + 4	3
JP -11	JP -27	LD 0F4,#i	DRSZ 0F4	*	LAID	ADD A, #i	ADD A,[B]	IFBIT 4,[B]	CLRA	LD B, 0B	IFBNE 4	JSR 0400-04FF	JMP 0400-04FF	JP + 21	JP + 5	4
JP -10	JP -26	LD 0F5,#i	DRSZ 0F5	*	JID	AND A, #i	AND A,[B]	IFBIT 5,[B]	SWAPA	LD B, 0A	IFBNE 5	JSR 0500-05FF	JMP 0500-05FF	JP + 22	JP + 6	5
JP -9	JP -25	LD 0F6,#i	DRSZ 0F6	X A, [X]	X A, [B]	XOR A, #i	XOR A,[B]	IFBIT 6,[B]	DCORA	LD B, 9	IFBNE 6	JSR 0600-06FF	JMP 0600-06FF	JP + 23	JP + 7	6
JP -8	JP -24	LD 0F7,#i	DRSZ 0F7	*	*	OR A, #i	OR A,[B]	IFBIT 7,[B]	*	LD B, 8	IFBNE 7	JSR 0700-07FF	JMP 0700-07FF	JP + 24	JP + 8	7
JP -7	JP -23	LD 0F8,#i	DRSZ 0F8	NOP	*	LD A, #i	IFC	SBIT 0,[B]	RBIT 0,[B]	LD B, 7	IFBNE 8	JSR 0800-08FF	JMP 0800-08FF	JP + 25	JP + 9	8
JP -6	JP -22	LD 0F9,#i	DRSZ 0F9	*	*	*	IFNC	SBIT 1,[B]	RBIT 1,[B]	LD B, 6	IFBNE 9	JSR 0900-09FF	JMP 0900-09FF	JP + 26	JP + 10	9
JP -5	JP -21	LD 0FA,#i	DRSZ 0FA	LD A, [X+]	LD A, [B+]	LD [B+],#i	INCA	SBIT 2,[B]	RBIT 2,[B]	LD B, 5	IFBNE 0A	JSR 0A00-0AFF	JMP 0A00-0AFF	JP + 27	JP + 11	A
JP -4	JP -20	LD 0FB,#i	DRSZ 0FB	LD A, [X−]	LD A, [B−]	LD [B−],#i	DECA	SBIT 3,[B]	RBIT 3,[B]	LD B, 4	IFBNE 0B	JSR 0B00-0BFF	JMP 0B00-0BFF	JP + 28	JP + 12	B
JP -3	JP -19	LD 0FC,#i	DRSZ 0FC	LD Md, #i	JMPL	X A,Md	*	SBIT 4,[B]	RBIT 4,[B]	LD B, 3	IFBNE 0C	JSR 0C00-0CFF	JMP 0C00-0CFF	JP + 29	JP +13	C
JP -2	JP -18	LD 0FD,#i	DRSZ 0FD	DIR	JSRL	LD A, Md	RETSK	SBIT 5,[B]	RBIT 5,[B]	LD B, 2	IFBNE 0D	JSR 0D00-0DFF	JMP 0D00-0DFF	JP + 30	JP +14	D
JP -1	JP -17	LD 0FE,#i	DRSZ 0FE	LD A, [X]	LD A, [B]	LD [B], #i	RET	SBIT 6, [B]	RBIT 6, [B]	LD B, 1	IFBNE 0E	JSR 0E00−0EFF	JMP 0E00−0EFF	JP + 31	JP +15	E
JP -0	JP -16	LD 0FF,#1	DRSZ 0FF	*	*	*	RETI	SBIT 7,[B]	RBIT 7,[B]	LD B, 0	IFBNE 0F	JSR 0F00-0FFF	JMP 0F00-0FFF	JP + 32	JP + 16	F

where, i is the immediate data Md is a directly addressed memory location * is an unused opcode (see following table)

Instruction Execution Time

Most instructions are single byte (with immediate addressing mode instruction taking two bytes).

Most single instructions take one cycle time to execute.

See the BYTES and CYCLES per INSTRUCTION table for details.

BYTES and CYCLES per INSTRUCTION

The following table shows the number of bytes and cycles for each instruction in the format of byte/cycle.

	[B]	Direct	Immed.
ADD	1/1	3/4	2/2
ADC	1/1	3/4	2/2
SUBC	1/1	3/4	2/2
AND	1/1	3/4	2/2
OR	1/1	3/4	2/2
XOR	1/1	3/4	2/2
IFEQ	1/1	3/4	2/2
IFGT	1/1	3/4	2/2
IFBNE	1/1		
DRSZ		1/3	
SBIT	1/1	3/4	
RBIT	1/1	3/4	
IFBIT	1/1	3/4	

The following table shows the instructions assigned to unused opcodes. This table is for information only. The operations performed are subject to change without notice. Do not use these opcodes.

Unused Opcode	Instruction	Unused Opcode	Instruction
60	NOP	A9	NOP
61	NOP	AF	LD A, [B]
62	NOP	B1	C → HC
63	NOP	B4	NOP
67	NOP	B5	NOP
8C	RET	B7	X A, [X]
99	NOP	B9	NOP
9F	LD [B], #i	BF	LD A, [X]
A7	X A, [B]		
A8	NOP		

Memory Transfer Instructions

	Register Indirect [B]	Register Indirect [X]	Direct	Immed.	Register Indirect Auto Incr & Decr [B+, B−]	Register Indirect Auto Incr & Decr [X+, X−]	
X A,*	1/1	1/3	2/3		1/2	1/3	
LD A,*	1/1	1/3	2/3	2/2	1/2	1/3	
LD B,Imm				1/1			(If B < 16)
LD B,Imm				2/3			(If B > 15)
LD Mem,Imm	2/2		3/3		2/2		
LD Reg,Imm				2/3			

* = > Memory location addressed by B or X or directly.

Instructions Using A & C

CLRA	1/1
INCA	1/1
DECA	1/1
LAID	1/3
DCORA	1/1
RRCA	1/1
SWAPA	1/1
SC	1/1
RC	1/1
IFC	1/1
IFNC	1/1

Transfer of Control Instructions

JMPL	3/4
JMP	2/3
JP	1/3
JSRL	3/5
JSR	2/5
JID	1/3
RET	1/5
RETSK	1/5
RETI	1/5
INTR	1/7
NOP	1/1

Option List

The COP820C/COP840C mask programmable options are listed out below. The options are programmed at the same time as the ROM pattern to provide the user with hardware flexibility to use a variety of oscillator configuration.

OPTION 1: CKI INPUT

= 1 Crystal (CKI/10) CKO for crystal configuration
= 2 External (CKI/10) CKO available as G7 input
= 3 R/C (CKI/10) CKO available as G7 input

OPTION 2: COP820C/COP840C BONDING

= 1 28 pin package
= 2 N.A.
= 3 20 pin package
= 4 20 SO package
= 5 28 SO package

The following option information is to be sent to National along with the EPROM.

Option Data

Option 1 Value__is: CKI Input
Option 2 Value__is: COP Bonding

How to Order

To order a complete development package, select the section for the microcontroller to be developed and order the parts listed.

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications Group. The Dial-A-Helper is an Electronic Bulletin Board information system.

Development Support

IN-CIRCUIT EMULATOR

The MetaLink iceMASTER™—COP8 Model 400 In-Circuit Emulator for the COP8 family of microcontrollers features high-performance operation, ease of use, and an extremely flexible user-interface for maximum productivity. Interchangeable probe cards, which connect to the standard common base, support the various configurations and packages of the COP8 family.

The iceMASTER provides real time, full speed emulation up to 10 MHz, 32 kBytes of emulation memory and 4k frames of trace buffer memory. The user may define as many as 32k trace and break triggers which can be enabled, disabled, set or cleared. They can be simple triggers based on code or address ranges or complex triggers based on code address, direct address, opcode value, opcode class or immediate operand. Complex breakpoints can be ANDed and ORed together. Trace information consists of address bus values, opcodes and user selectable probe clips status (external event lines). The trace buffer can be viewed as raw hex or as disassembled instructions. The probe clip bit values can be displayed in binary, hex or digital waveform formats.

During single-step operation the dynamically annotated code feature displays the contents of all accessed (read and write) memory locations and registers, as well as flow-of-control direction change markers next to each instruction executed.

The iceMASTER's performance analyzer offers a resolution of better than 6 μs. The user can easily monitor the time spent executing specific portions of code and find "hot spots" or "dead code". Up to 15 independent memory areas based on code address or label ranges can be defined. Analysis results can be viewed in bargraph format or as actual frequency count.

Emulator memory operations for program memory include single line assembler, disassembler, view, change and write to file. Data memory operations include fill, move, compare, dump to file, examine and modify. The contents of any memory space can be directly viewed and modified from the corresponding window.

The iceMASTER comes with an easy to use windowed interface. Each window can be sized, highlighted, color-controlled, added, or removed completely. Commands can be accessed via pull-down-menus and/or redefineable hot keys. A context sensitive hypertext/hyperlinked on-line help system explains clearly the options the user has from within any window.

The iceMASTER connects easily to a PC via the standard COMM port and its 115.2 kBaud serial link keeps typical program download time to under 3 seconds.

The following tables list the emulator and probe cards ordering information:

Emulator Ordering Information

Part Number	Description
IM-COP8/400	MetaLink Base Unit In-circuit Emulator for all COP8 Devices, Symbolic Debugger Software and RS-232 Serial Interface Cable
MHW-PS3	Power Supply 110V/60 Hz
MHW-PS4	Power Supply 220V/50 Hz

Probe Card Ordering Information

Part Number	Package	Voltage Range	Emulates
MHW-880C20D5PC	20 DIP	4.5V–5.5V	COP822C, 842C, 8782C
MHW-880C20DWPC	20 DIP	2.5V–6.0V	COP822C, 842C, 8782C
MHW-880C28D5PC	28 DIP	4.5V–5.5V	COP820C, 840C, 881C, 8781C
MHW-880C28DWPC	28 DIP	2.5V–6.0V	COP820C, 840C, 881C, 8781C

Development Support (Continued)

MACRO CROSS ASSEMBLER

National Semiconductor offers a COP8 macro cross assembler. It runs on industry standard compatible PCs and supports all of the full-symbolic debugging features of the MetaLink iceMASTER emulators.

Assembler Ordering Information

Part Number	Description	Manual
MOLE-COP8-IBM	COP8 Macro Cross Assembler for IBM PC-XT®, PC-AT® or Compatible	424410527-001

SIMULATOR

The COP8 Designer's is Tool Kit is available for evaluating National Semiconductor's COP8 microcontroller family. The kit contains programmer's manuals, device datasheets, pocket reference guide, assembler and simulator, which allows the user to write, test, debug and run code on an industry standard compatible PC. The simulator has a windowed user interface and can handle script files that simulate hardware inputs, interrupts and automatic command processing. The capture file feature enables the user to record to a file current cycle count and output port changes which are caused by the program under test.

Simulator Ordering Information

Part Number	Description	Manual
COP8-TOOL-KIT	COP8 Designer's Tool Kit Assembler and Simulator	420420270-001 424420269-001

SINGLE CHIP EMULATOR DEVICE

The COP8 family is fully supported by single chip form, fit, and function emulators. Two types of single chip emulators are available: Multi-Chip Module (MCM) emulators, which combine the microcontroller-die and an EPROM-die in one package, and emulators where the microcontroller's standard ROM is replaced with an on-chip EPROM. For more detailed information refer to the emulation device specific data sheets and the form, fit, function emulator selection table below.

Single Chip Emulator Selection Table

Device Number	Clock Option	Package	Description	Emulates
COP881CMHD-X	X = 1: Crystal X = 2: External X = 3: R/C	28 DIP	Multi-Chip Module (MCM), UV Erasable	COP840C, COP820C
COP881CMHEA-X	X = 1: Crystal X = 2: External X = 3: R/C	28 LCC	MCM, (Same Footprint as 28 SO), UV Erasable	COP840C, COP820C
COP842CMHD-X	X = 1: Crystal X = 2: External X = 3: R/C	20 DIP	MCM, UV Erasable	COP842C
COP822CMHD-X	X = 1: Crystal X = 2: External X = 3: R/C	20 DIP	MCM, UV Erasable	COP822C
COP8781CN	Programmable	28 DIP	One Time Programmable (OTP)	COP840C, COP820C
COP8781CJ	Programmable	28 DIP	UV Erasable	COP840C, COP820C
COP8781CWM	Programmable	28 SO	OTP	COP840C, COP820C
COP8781CMC	Programmable	28 SO	UV Erasable	COP840C, COP820C
COP8782CN	Programmable	20 DIP	OTP	COP842C, COP822C
COP8782CJ	Programmable	20 DIP	UV Erasable	COP842C, COP822C
COP8782CWM	Programmable	20 SO	OTP	COP842C, COP822C
COP8782CMC	Programmable	20 SO	UV Erasable	COP842C, COP822C

Development Support (Continued)

PROGRAMMING SUPPORT

Programming of the single chip emulator devices is supported by different sources. National Semiconductor offers a duplicator board which allows the transfer of program code from a standard programmed EPROM to the single chip emulator and vice versa.

Data I/O supports COP8 emulator device programming with its uniSite 48 and System 2900 programmers. Further information on Data I/O programmers can be obtained from any Data I/O sales office or the following USA numbers:

Telephone: (206) 881-6444 FAX: (206) 882-1043

Duplicator Board Ordering Information

Part Number	Description	Devices Supported
COP8-PRGM-28D	Duplicator Board for 28 DIP and for Use with Scrambler Boards	COP881CMHD
COP8-SCRM-DIP	Multi-Chip Module (MCM) Scrambler Board for 20 DIP Socket	COP842CMHD, COP822CMHD
COP8-SCRM-SBX	MCM Scrambler Board for 28 LCC Sockets	COP881CMHEA
COP8-PRGM-DIP	Duplicator Board with COP8-SCRM-DIP Scrambler Board	COP881CMHD, 842CMHD, 822CMHD
COP8-PRGM-87A	Duplicator Board with COP87XX Scrambler for 28 DIP and 28 SO	COP8781CN, 8781CJ, 8781CWM, 8781CMC
COP8-PRGM-87B	Duplicator Board with COP87XX Scrambler for 20 DIP and 20 SO	COP8782CN, 8782CJ, 8782CWM, 8782CMC

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down-loaded to disk for later use.

ORDER P/N: MOLE-DIAL-A-HLP

Information System Package contains:

- Dial-A-Helper Users Manual
- Public Domain Communications Software

FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factory applications support. If a user has questions, he can leave messages on our electronic bulletin board, which we will respond to.

Voice: (408) 721-5582

Modem: (408) 739-1162

Baud: 300 or 1200 baud

Setup: Length: 8-Bit

Parity: None

Stop Bit: 1

Operation: 24 Hrs. 7 Days

National Semiconductor

COP680C/COP681C/COP880C/COP881C/ COP980C/COP981C Microcontrollers

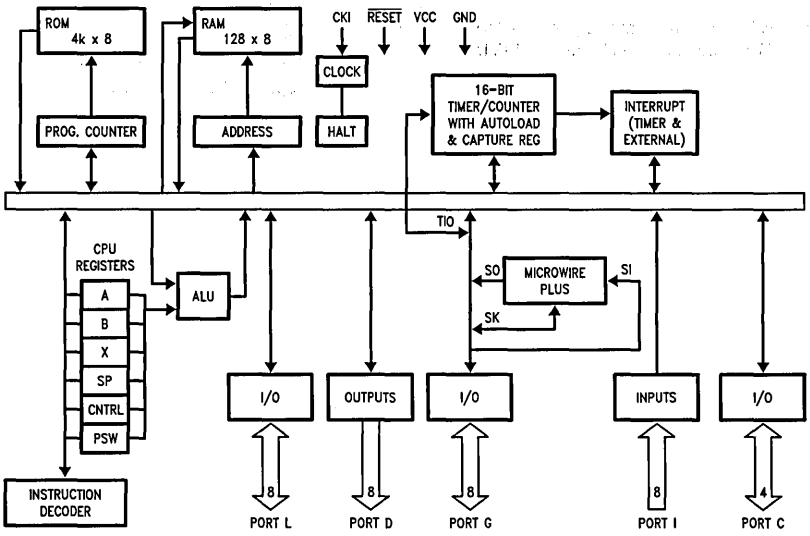
General Description

The COP880C and COP881C are members of the COPS™ microcontroller family. They are fully static parts, fabricated using double-metal silicon gate microCMOS technology. This low cost microcontroller is a complete microcomputer containing all system timing, interrupt logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS™ serial I/O, a 16-bit timer/counter with capture register and a multi-sourced interrupt. Each I/O pin has software selectable options to adapt the COP880C and COP881C to the specific application. The part operates over a voltage range of 2.5 to 6.0V. High throughput is achieved with an efficient, regular instruction set operating at a 1 microsecond per instruction rate.

Features

- Low cost 8-bit microcontroller
- Fully static CMOS
- 1 μs instruction time
- Low current drain
  Low current static HALT mode (Typically < 1 μA)
- Single supply operation: 2.5 to 6.0V
- 4096 bytes ROM/128 Bytes RAM
- 16-bit read/write timer operates in a variety of modes
  — Timer with 16-bit auto reload register
  — 16-bit external event counter
  — Timer with 16-bit capture register (selectable edge)
- Multi-source interrupt
  — Reset master clear
  — External interrupt with selectable edge
  — Timer interrupt or capture interrupt
  — Software interrupt
- 8-bit stack pointer (stack in RAM)
- Powerful instruction set, most instructions single byte
- BCD arithmetic instructions
- MICROWIRE PLUS™ serial I/O
- 44 PLCC, 36 I/O pins
- 40 DIP, 36 I/O pins
- 28 DIP and SO, 24 I/O pins
- Software selectable I/O options (TRI-STATE®, push-pull, weak pull-up)
- Schmitt trigger inputs on Port G
- Temperature ranges: COP98XC/COP98XCH 0°C to 70°C, COP88XC −40°C to +85°C, COP68XC −55°C to +125°C.
- Form factor emulation devices
- Fully supported by National's development system

Block Diagram



TL/DD/10802–1

FIGURE 1

COP980C/COP981C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	50 mA
Total Current out of GND Pin (Sink)	60 mA
Storage Temperature Range	−65°C to +140°C

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics COP980XC; 0°C ≤ T_A ≤ +70°C unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage					
98XC		2.3		4.0	V
98XCH		4.0		6.0	V
Power Supply Ripple (Note 1)	Peak to Peak			0.1 V_{CC}	V
Supply Current					
CKI = 10 MHz	V_{CC} = 6V, tc = 1 μs			8.0	mA
CKI = 4 MHz	V_{CC} = 6V, tc = 2.5 μs			4.4	mA
CKI = 4 MHz	V_{CC} = 4.0V, tc = 2.5 μs			2.2	mA
CKI = 1 MHz	V_{CC} = 4.0V, tc = 10 μs			1.4	mA
(Note 2)					
HALT Current	V_{CC} = 6V, CKI = 0 MHz		<0.7	8	μA
(Note 3)	V_{CC} = 4.0V, CKI = 0 MHz		<0.4	5	μA
Input Levels					
RESET, CKI					
Logic High		0.9 V_{CC}			V
Logic Low				0.1 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6.0V	−1.0		+1.0	μA
Input Pullup Current	V_{CC} = 6.0V	40		250	μA
G Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
	V_{CC} = 2.3V, V_{OH} = 1.6V	0.2			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1.0V	10			mA
	V_{CC} = 2.3V, V_{OL} = 0.4V	2			mA
All Others					
Source (Weak Pull-Up)	V_{CC} = 4.5V, V_{OH} = 3.2V	10		110	μA
	V_{CC} = 2.3V, V_{OH} = 1.6V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
	V_{CC} = 2.3V, V_{OH} = 1.6V	0.2			
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.3V, V_{OL} = 0.4V	0.7			
TRI-STATE Leakage	V_{CC} = 6.0V	−1.0		+1.0	μA
Allowable Sink/Source Current Per Pin					
D Outputs (Sink)				15	mA
All Others				3	mA
Maximum Input Current (Note 4) Without Latchup (Room Temp)	Room Temp			±100	mA
RAM Retention Voltage, Vr (Note 5)	500 ns Rise and Fall Time (Min)	2.0			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

COP980C/COP981C

DC Electrical Characteristics (Continued)

Note 1: Rate of voltage change must be less than 0.5V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L, C and G ports TRI-STATE and tied to ground, all outputs low and tied to ground.

Note 4: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typ). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Note 5: To maintain RAM integrity, the voltage must not be dropped or raised instantaneously.

AC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (tc)					
Crystal/Resonator or External	$V_{CC} \ge 4.0V$	1		DC	μs
(Div-by 10)	$2.3V \le V_{CC} \le 4.0V$	2.5		DC	μs
R/C Oscillator Mode	$V_{CC} \ge 4.0V$	3		DC	μs
(Div-by 10)	$2.3V \le V_{CC} \le 4.0V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 6)	fr = Max	40		60	%
Rise Time (Note 6)	fr = 10 MHz Ext Clock			12	ns
Fall Time (Note 6)	fr = 10 MHz Ext Clock			8	ns
Inputs					
t_{SETUP}	$V_{CC} \ge 4.0V$	200			ns
	$2.3V \le V_{CC} \le 4.0V$	500			ns
t_{HOLD}	$V_{CC} \ge 4.0V$	60			ns
	$2.3V \le V_{CC} \le 4.0V$	150			ns
Output Propagation Delay	$C_L = 100$ pF, $R_L = 2.2$ kΩ				
t_{PD1}, t_{PD0}					
SO, SK	$V_{CC} \ge 4.0V$			0.7	μs
	$2.3V \le V_{CC} \le 4.0V$			1.75	μs
All Others	$V_{CC} \ge 4.0V$			1	μs
	$2.3V \le V_{CC} \le 4.0V$			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output					
Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		t_C			
Interrupt Input Low Time		t_C			
Timer Input High Time		t_C			
Timer Input Low Time		t_C			
Reset Pulse Width		1.0			μs

Note 6: Parameter sampled (not 100% tested).

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Total Current into V_{CC} Pin (Source)	50 mA
Total Current out of GND Pin (Sink)	60 mA
Storage Temperature Range	$-65°C$ to $+140°C$

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics COP88XC; $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage		2.5		6.0	V
Power Supply Ripple (Note 1)	Peak to Peak			0.1 V_{CC}	V
Supply Current					
CKI = 10 MHz	V_{CC} = 6V, tc = 1 μs			8.0	mA
CKI = 4 MHz	V_{CC} = 6V, tc = 2.5 μs			4.4	mA
CKI = 4 MHz	V_{CC} = 4.0V, tc = 2.5 μs			2.2	mA
CKI = 1 MHz	V_{CC} = 4.0V, tc = 10 μs			1.4	mA
(Note 2)					
HALT Current	V_{CC} = 6V, CKI = 0 MHz		<1	10	μA
(Note 3)	V_{CC} = 3.5V, CKI = 0 MHz		<0.5	6	μA
Input Levels					
$\overline{\text{RESET}}$, CKI					
Logic High		0.9 V_{CC}			V
Logic Low				0.1 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6.0V	−2		+2	μA
Input Pullup Current	V_{CC} = 6.0V	40		250	μA
G Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1.0V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2			mA
All Others					
Source (Weak Pull-Up)	V_{CC} = 4.5V, V_{OH} = 3.2V	10		110	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			
TRI-STATE Leakage	V_{CC} = 6.0V	−2.0		+2.0	μA
Allowable Sink/Source Current Per Pin					
D Outputs (Sink)				15	mA
All Others				3	mA
Maximum Input Current (Note 4) Without Latchup (Room Temp)	Room Temp			±100	mA
RAM Retention Voltage, Vr (Note 5)	500 ns Rise and Fall Time (Min)	2.0			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

DC Electrical Characteristics (Continued)

Note 1: Rate of voltage change must be less than 0.5V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L, C and G ports TRI-STATE and tied to ground, all outputs low and tied to ground.

Note 4: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typ). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

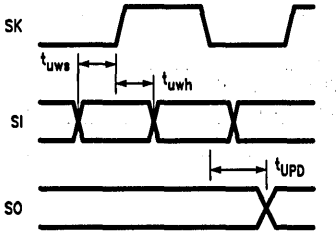
Note 5: To maintain RAM integrity, the voltage must not be dropped or raised instantaneously.

AC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (tc)					
Crystal/Resonator or External	$V_{CC} \ge 4.5V$	1		DC	μs
(Div-by 10)	$2.5V \le V_{CC} < 4.5V$	2.5		DC	μs
R/C Oscillator Mode	$V_{CC} \ge 4.5V$	3		DC	μs
(Div-by 10)	$2.5V \le V_{CC} < 4.5V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 6)	fr = Max	40		60	%
Rise Time (Note 6)	fr = 10 MHz Ext Clock			12	ns
Fall Time (Note 6)	fr = 10 MHz Ext Clock			8	ns
Inputs					
t_{SETUP}	$V_{CC} \ge 4.5V$	200			ns
	$2.5V \le V_{CC} < 4.5V$	500			ns
t_{HOLD}	$V_{CC} \ge 4.5V$	60			ns
	$2.5V \le V_{CC} < 4.5V$	150			ns
Output Propagation Delay	C_L = 100 pF, R_L = 2.2 kΩ				
t_{PD1}, t_{PD0}					
SO, SK	$V_{CC} \ge 4.5V$			0.7	μs
	$2.5V \le V_{CC} < 4.5V$			1.75	μs
All Others	$V_{CC} \ge 4.5V$			1	μs
	$2.5V \le V_{CC} < 4.5V$			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output					
Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		t_C			
Interrupt Input Low Time		t_C			
Timer Input High Time		t_C			
Timer Input Low Time		t_C			
Reset Pulse Width		1.0			μs

Note 6: Parameter sampled (not 100% tested).

Timing Diagram



TL/DD/10802-2

FIGURE 2. MICROWIRE/PLUS Timing

COP680C/COP681C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	40 mA
Total Current Out of GND Pin (Sink)	48 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics COP68XC: $-55°C \leq T_A \leq +125°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage		4.5		5.5	V
Power Supply Ripple (Note 1)	Peak to Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 5.5V, tc = 1 μs			8.0	mA
CKI = 4 MHz	V_{CC} = 5.5V, tc = 2.5 μs			4.4	mA
HALT Current (Note 3)	V_{CC} = 5.5V, CKI = 0 MHz		<10	30	μA
Input Levels					
$\overline{RESET}$, CKI					
Logic High		0.9 V_{CC}			V
Logic Low				0.1 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 5.5V	−5		+5	μA
Input Pullup Current	V_{CC} = 4.5V	35		300	μA
G Port Input Hysteresis			0.05 V_{CC}		V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.8V	0.35			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1.0V	9			mA
All Others					
Source (Weak Pull-Up)	V_{CC} = 4.5V, V_{OH} = 3.2V	9		120	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.2V	0.35			mA
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 3.8V	1.4			mA
TRI-STATE Leakage	V_{CC} = 5.5V	−5.0		+5.0	μA
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				12	mA
All Others				2.5	mA
Maximum Input Current (Room Temp) without Latchup (Note 4)	Room Temp			±100	mA
RAM Retention Voltage, Vr (Note 5)	500 ns Rise and Fall Time (Min)	2.5			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

Note 1: Rate of voltage change must be less than 0.5V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports TRI-STATE and tied to ground, all outputs low and tied to ground.

Note 4: Pins G6 and $\overline{RESET}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Note 5: To maintain RAM integrity, the voltage must not be dropped or raised instantaneously.

COP680C/COP681C

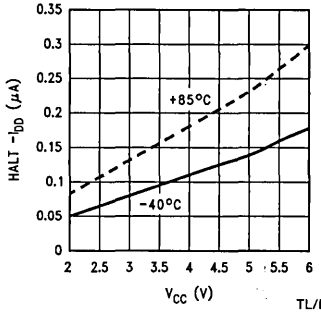
AC Electrical Characteristics $-55°C \leq T_A \leq +125°C$ unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (tc)					
Ext. or Crystal/Resonant (Div-by 10)	$V_{CC} \geq 4.5V$	1		DC	μs
CKI Clock Duty Cycle (Note 6)	fr = Max	40		60	%
Rise Time (Note 6)	fr = 10 MHz Ext Clock			12	ns
Fall Time (Note 6)	fr = 10 MHz Ext Clock			8	ns
Inputs					
t_{SETUP}	$V_{CC} \geq 4.5V$	220			ns
t_{HOLD}	$V_{CC} \geq 4.5V$	66			ns
Output Propagation Delay t_{PD1}, t_{PD0}	R_L = 2.2k, C_L = 100 pF				
SO, SK	$V_{CC} \geq 4.5V$			0.8	μs
All Others	$V_{CC} \geq 4.5V$			1.1	μs
MICROWIRE Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Valid Time (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		t_C			
Interrupt Input Low Time		t_C			
Timer Input High Time		t_C			
Timer Input Low Time		t_C			
Reset Pulse Width		1			μs

Note 6: Parameter sampled (not 100% tested).

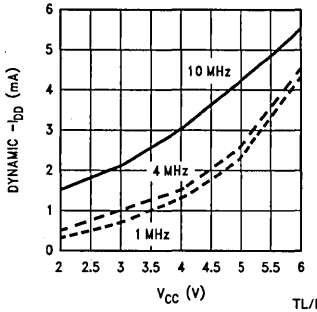
Typical Performance Characteristics ($-40°C \le T_A \le +85°C$)

Hall—I_{DD}



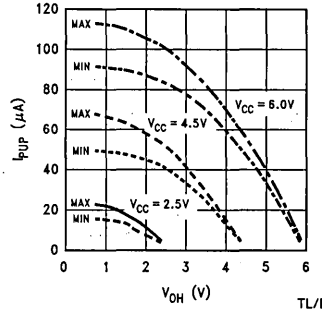
TL/DD/10802–16

Dynamic—I_{DD} (Crystal Clock Option)



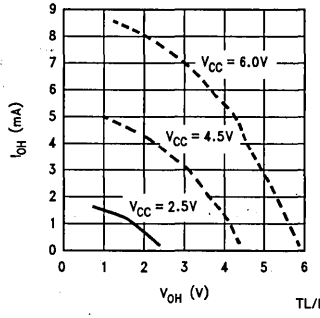
TL/DD/10802–17

Port L/C/G Weak Pull-Up Source Current



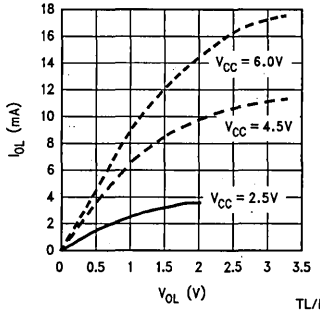
TL/DD/10802–18

Port L/C/G Push-Pull Source Current



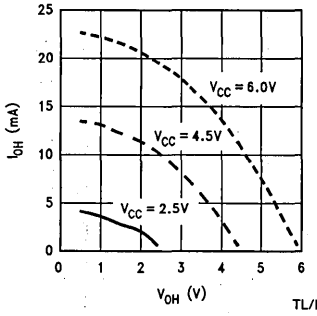
TL/DD/10802–19

Port L/C/G Push-Pull Sink Current



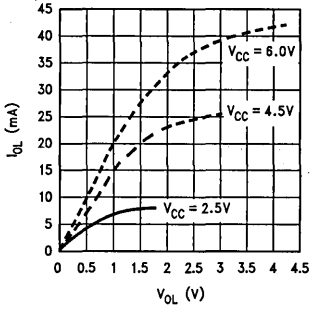
TL/DD/10802–20

Port D Source Current



TL/DD/10802–21

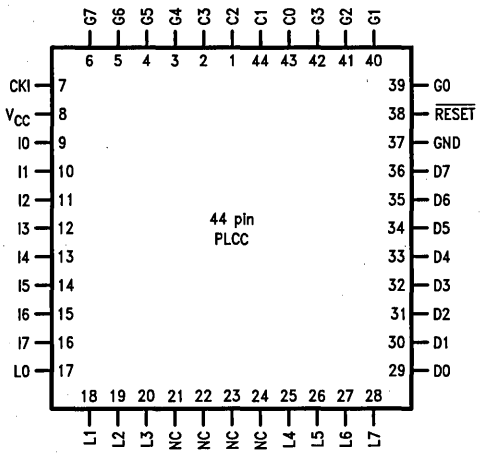
Port D Sink Current



TL/DD/10802–22

Connection Diagrams

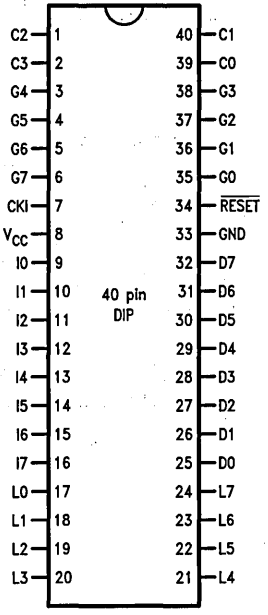
Plastic Chip Carrier



TL/DD/10802–3

Top View
Order Number COP680C-XXX/V, COP880C-XXX/V, COP980C-XXX/V or COP980CH-XXX/V

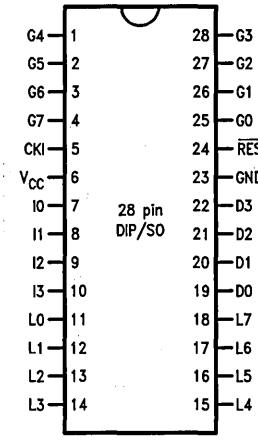
Dual-In-Line Package



TL/DD/10802–4

Top View
Order Number COP680C-XXX/N, COP880C-XXX/N, COP980C-XXX/N or COP980CH-XXX/N

Dual-In-Line Package (N) and 28 Wide SO (WM)



TL/DD/10802–5

Top View
Order Number COP881C-XXX/N, COP981C-XXX/N, COP881C-XXX/WM, COP981C-XXX/WM, COP981CH-XXX/N or COP981CH-XXX/WM

FIGURE 3

Pin Descriptions

V_{CC} and GND are the power supply pins.

CKI is the clock input. This can come from an external source, a R/C generated oscillator or a crystal (in conjunction with CKO). See Oscillator description.

$\overline{\text{RESET}}$ is the master reset input. See Reset description.

PORT I is an 8-bit Hi-Z input port.

PORT L is an 8-bit I/O port.

PORT C is a 4-bit I/O port.

Three memory locations are allocated for the L, G and C ports, one each for data register, configuration register and the input pins. Reading bits 4–7 of the C-Configuration register, data register, and input pins returns undefined data.

There are two registers associated with the L and C ports: a data register and a configuration register. Therefore, each L and C I/O bit can be individually configured under software control as shown below:

Config.	Data	Ports L and C Setup
0	0	Hi-Z Input (TRI-STATE Output)
0	1	Input with Pull-Up (Weak One Output)
1	0	Push-Pull Zero Output
1	1	Push-Pull One Output

On the 28-pin part, it is recommended that all bits of Port C be configured as outputs.

PORT G is an 8-bit port with 6 I/O pins (G0–G5) and 2 input pins (G6, G7). All eight G-pins have Schmitt Triggers on the inputs.

There are two registers associated with the G port: a data register and a configuration register. Therefore, each G port bit can be individually configured under software control as shown below:

Config.	Data	Port G Setup
0	0	Hi-Z Input (TRI-STATE Output)
0	1	Input with Pull-Up (Weak One Output)
1	0	Push-Pull Zero Output
1	1	Push-Pull One Output

Since G6 and G7 are input only pins, any attempt by the user to configure them as outputs by writing a one to the configuration register will be disregarded. Reading the G6 and G7 configuration bits will return zeros. The COP880C will be placed in the HALT mode by writing to the G7 bit in the G-port data register.

Six pins of Port G have alternate features:

G0 INTR (an external interrupt)

G3 TIO (timer/counter input/output)

G4 SO (MICROWIRE serial data output)

G5 SK (MICROWIRE clock I/O)

G6 SI (MICROWIRE serial data input)

G7 CKO crystal oscillator output (selected by mask option) or HALT restart input (general purpose input)

Pins G1 and G2 currently do not have any alternate functions.

PORT D is an 8-bit output port that is preset high when RESET goes low. Care must be exercised with the D2 pin operation. At RESET, the external loads on this pin must ensure that the output voltages stay above 0.9 V_{CC} to prevent the chip from entering special modes. Also, keep the external loading on D2 to less than 1000 pF.

Functional Description

Figure 1 shows the block diagram of the internal architecture. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device.

ALU AND CPU REGISTERS

The ALU can do an 8-bit addition, subtraction, logical or shift operation in one cycle time.

There are five CPU registers:

A is the 8-bit Accumulator register

PU is the upper 7 bits of the program counter (PC)

PL is the lower 8 bits of the program counter (PC)

B is the 8-bit address register, can be auto incremented or decremented.

X is the 8-bit alternate address register, can be incremented or decremented.

SP is the 8-bit stack pointer, points to subroutine stack (in RAM).

B, X and SP registers are mapped into the on chip RAM. The B and X registers are used to address the on chip RAM. The SP register is used to address the stack in RAM during subroutine calls and returns.

PROGRAM MEMORY

Program memory for the COP880C/COP881C consists of 4096 bytes of ROM. These bytes may hold program instructions or constant data. The program memory is addressed by the 15-bit program counter (PC). ROM can be indirectly read by the LAID instruction for table lookup.

DATA MEMORY

The data memory address space includes on chip RAM, I/O and registers. Data memory is addressed directly by the instruction or indirectly by the B, X and SP registers.

The COP880C/COP881C has 128 bytes of RAM. Sixteen bytes of RAM are mapped as "registers" that can be loaded immediately, decremented or tested. Three specific registers: B, X and SP are mapped into this space, the other bytes are available for general usage.

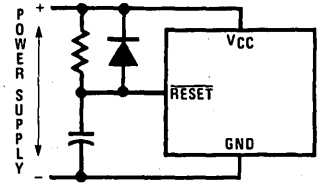
The instruction set permits any bit in memory to be set, reset or tested. All I/O and registers (except the A & PC) are memory mapped; therefore, I/O bits and register bits can be directly and individually set, reset and tested. A is not memory mapped, but bit operations can be still performed on it.

RESET

The $\overline{\text{RESET}}$ input when pulled low initializes the microcontroller. Initialization will occur whenever the $\overline{\text{RESET}}$ input is pulled low. Upon initialization, the ports L, G and C are placed in the TRI-STATE mode and the Port D is set high. The PC, PSW and CNTRL registers are cleared. The data and configuration registers for Ports L, G and C are cleared.

The external RC network shown in Figure 4 should be used to ensure that the $\overline{\text{RESET}}$ pin is held low until the power supply to the chip stabilizes.

Functional Description (Continued)



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RC ≥ 5X Power Supply Rise Time

FIGURE 4. Recommended Reset Circuit

OSCILLATOR CIRCUITS

Figure 5 shows the three clock oscillator configurations available for the COP880C and COP881C.

A. CRYSTAL OSCILLATOR

The COP880C/COP881C can be driven by a crystal clock. The crystal network is connected between the pins CKI and CKO.

Table I shows the component values required for various standard crystal values.

B. EXTERNAL OSCILLATOR

CKI can be driven by an external clock signal. CKO is available as a general purpose input and/or HALT restart control.

C. R/C OSCILLATOR

CKI is configured as a single pin RC controlled Schmitt trigger oscillator. CKO is available as a general purpose input and/or HALT restart control.

Table II shows the variation in the oscillator frequencies as functions of the component (R and C) values.

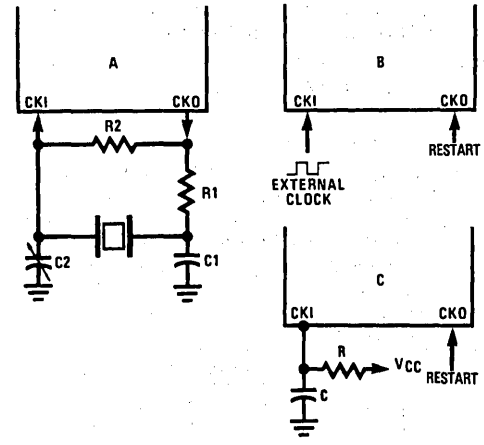

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FIGURE 5. Crystal and R-C Connection Diagrams

OSCILLATOR MASK OPTIONS

The COP880C and COP881C can be driven by clock inputs between DC and 10 MHz.

TABLE I. Crystal Oscillator Configuration, $T_A = 25°C$

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)	Conditions
0	1	30	30–36	10	$V_{CC} = 5V$
0	1	30	30–36	4	$V_{CC} = 2.5V$
5.6	1	200	100–150	0.455	$V_{CC} = 5V$

TABLE II. RC Oscillator Configuration, $T_A = 25°C$

R (kΩ)	C (pF)	CKI Freq. (MHz)	Instr. Cycle (μs)	Conditions
3.3	82	2.2 to 2.7	3.7 to 4.6	$V_{CC} = 5V$
5.6	100	1.1 to 1.3	7.4 to 9.0	$V_{CC} = 5V$
6.8	100	0.9 to 1.1	8.8 to 10.8	$V_{CC} = 5V$

Note: (R/C Oscillator Configuration): 3k ≤ R ≤ 200k, 50 pF ≤ C ≤ 200 pF.

Functional Description (Continued)

The COP880C and COP881C microcontrollers have five mask options for configuring the clock input. The CKI and CKO pins are automatically configured upon selecting a particular option.

— Crystal (CKI/10); CKO for crystal configuration

— External (CKI/10); CKO available as G7 input

— R/C (CKI/10); CKO available as G7 input

G7 can be used either as a general purpose input or as a control input to continue from the HALT mode.

CURRENT DRAIN

The total current drain of the chip depends on:

1) Oscillator operating mode—I1

2) Internal switching current—I2

3) Internal leakage current—I3

4) Output source current—I4

5) DC current caused by external input not at V_{CC} or GND—I5

Thus the total current drain, It is given as

$$It = I1 + I2 + I3 + I4 + I5$$

To reduce the total current drain, each of the above components must be minimum.

The chip will draw the least current when in the normal mode. The high speed mode will draw additional current. The R/C mode will draw the most. Operating with a crystal network will draw more current than an external square-wave. Switching current, governed by the equation below, can be reduced by lowering voltage and frequency. Leakage current can be reduced by lowering voltage and temperature. The other two items can be reduced by carefully designing the end-user's system.

$I2 = C \times V \times f$

Where

C = equivalent capacitance of the chip.

V = operating voltage

f = CKI frequency

HALT MODE

The COP880C and COP881C support a power saving mode of operation: HALT. The controller is placed in the HALT mode by setting the G7 data bit, alternatively the user can stop the clock input. In the HALT mode all internal processor activities including the clock oscillator are stopped. The fully static architecture freezes the state of the controller and retains all information until continuing. In the HALT mode, power requirements are minimal as it draws only leakage currents and output current. The applied voltage (V_{CC}) may be decreased down to Vr (minimum RAM retention voltage) without altering the state of the machine.

There are two ways to exit the HALT mode: via the $\overline{\text{RESET}}$ or by the CKO pin. A low on the $\overline{\text{RESET}}$ line reinitializes the microcontroller and starts executing from the address 0000H. A low to high transition on the CKO pin causes the microcontroller to continue with no reinitialization from the address following the HALT instruction. This also resets the G7 data bit.

INTERRUPTS

The COP880C and COP881C have a sophisticated interrupt structure to allow easy interface to the real world. There are three possible interrupt sources, as shown below.

A maskable interrupt on external G0 input (positive or negative edge sensitive under software control)

A maskable interrupt on timer underflow or timer capture

A non-maskable software/error interrupt on opcode zero

INTERRUPT CONTROL

The GIE (global interrupt enable) bit enables the interrupt function. This is used in conjunction with ENI and ENTI to select one or both of the interrupt sources. This bit is reset when interrupt is acknowledged.

ENI and ENTI bits select external and timer interrupt respectively. Thus the user can select either or both sources to interrupt the microcontroller when GIE is enabled.

IEDG selects the external interrupt edge (0 = rising edge, 1 = falling edge). The user can get an interrupt on both rising and falling edges by toggling the state of IEDG bit after each interrupt.

IPND and TPND bits signal which interrupt is pending. After interrupt is acknowledged, the user can check these two bits to determine which interrupt is pending. This permits the interrupts to be prioritized under software. The pending flags have to be cleared by the user. Setting the GIE bit high inside the interrupt subroutine allows nested interrupts.

The software interrupt does not reset the GIE bit. This means that the controller can be interrupted by other interrupt sources while servicing the software interrupt.

INTERRUPT PROCESSING

The interrupt, once acknowledged, pushes the program counter (PC) onto the stack and the stack pointer (SP) is decremented twice. The Global Interrupt Enable (GIE) bit is reset to disable further interrupts. The microcontroller then vectors to the address 00FFH and resumes execution from that address. This process takes 7 cycles to complete. At the end of the interrupt subroutine, any of the following three instructions return the processor back to the main program: RET, RETSK or RETI. Either one of the three instructions will pop the stack into the program counter (PC). The stack pointer is then incremented twice. The RETI instruction additionally sets the GIE bit to re-enable further interrupts.

Any of the three instructions can be used to return from a hardware interrupt subroutine. The RETSK instruction should be used when returning from a software interrupt subroutine to avoid entering an infinite loop.

Functional Description (Continued)

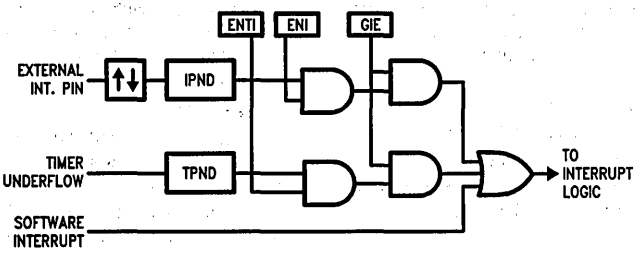

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FIGURE 6. Interrupt Block Diagram

DETECTION OF ILLEGAL CONDITIONS

The COP880C and COP881C incorporate a hardware mechanism that allows it to detect illegal conditions which may occur from coding errors, noise and 'brown out' voltage drop situations. Specifically it detects cases of executing out of undefined ROM area and unbalanced stack situations.

Reading an undefined ROM location returns 00 (hexadecimal) as its contents. The opcode for a software interrupt is also '00'. Thus a program accessing undefined ROM will cause a software interrupt.

Reading an undefined RAM location returns an FF (hexadecimal). The subroutine stack on the COP880C and COP881C grows down for each subroutine call. By initializing the stack pointer to the top of RAM, the first unbalanced return instruction will cause the stack pointer to address undefined RAM. As a result the program will attempt to execute from FFFF (hexadecimal), which is an undefined ROM location and will trigger a software interrupt.

MICROWIRE/PLUS™

MICROWIRE/PLUS is a serial synchronous bidirectional communications interface. The MICROWIRE/PLUS capability enables the COP880C and COP881C to interface with any of National Semiconductor's MICROWIRE peripherals (i.e. A/D converters, display drivers, EEPROMS, etc.) and with other microcontrollers which support the MICROWIRE/PLUS interface. It consists of an 8-bit serial shift register (SIO) with serial data input (SI), serial data output (SO) and serial shift clock (SK). *Figure 7* shows the block diagram of the MICROWIRE/PLUS interface.

The shift clock can be selected from either an internal source or an external source. Operating the MICROWIRE/PLUS interface with the internal clock source is called the Master mode of operation. Similarly, operating the MICROWIRE/PLUS interface with an external shift clock is called the Slave mode of operation.

The CNTRL register is used to configure and control the MICROWIRE/PLUS mode. To use the MICROWIRE/PLUS, the MSEL bit in the CNTRL register is set to one. The SK clock rate is selected by the two bits, S0 and S1, in the CNTRL register. Table III details the different clock rates that may be selected.

TABLE III

S1	S0	SK Cycle Time
0	0	$2t_C$
0	1	$4t_C$
1	x	$8t_C$

where,

t_C is the instruction cycle clock.

MICROWIRE/PLUS OPERATION

Setting the BUSY bit in the PSW register causes the MICROWIRE/PLUS arrangement to start shifting the data. It gets reset when eight data bits have been shifted. The user may reset the BUSY bit by software to allow less than 8 bits to shift. The COP880C and COP881C may enter the MICROWIRE/PLUS mode either as a Master or as a Slave. *Figure 8* shows how two COP880C microcontrollers and several peripherals may be interconnected using the MICROWIRE/PLUS arrangement.

Master MICROWIRE/PLUS Operation

In the MICROWIRE/PLUS Master mode of operation the shift clock (SK) is generated internally by the COP880C. The MICROWIRE/PLUS Master always initiates all data exchanges. (See *Figure 8*). The MSEL bit in the CNTRL register must be set to enable the SO and SK functions onto the G Port. The SO and SK pins must also be selected as outputs by setting appropriate bits in the Port G configuration register. Table IV summarizes the bit settings required for Master mode of operation.

SLAVE MICROWIRE/PLUS OPERATION

In the MICROWIRE/PLUS Slave mode of operation the SK clock is generated by an external source. Setting the MSEL bit in the CNTRL register enables the SO and SK functions onto the G Port. The SK pin must be selected as an input and the SO pin is selected as an output pin by appropriately setting up the Port G configuration register. Table IV summarizes the settings required to enter the Slave mode of operation.

The user must set the BUSY flag immediately upon entering the Slave mode. This will ensure that all data bits sent by the Master will be shifted properly. After eight clock pulses the BUSY flag will be cleared and the sequence may be repeated. (See *Figure 8*.)

Functional Description (Continued)

TABLE IV

G4 Config. Bit	G5 Config. Bit	G4 Fun.	G5 Fun.	G6 Fun.	Operation
1	1	SO	Int. SK	SI	MICROWIRE Master
0	1	TRI-STATE	Int. SK	SI	MICROWIRE Master
1	0	SO	Ext. SK	SI	MICROWIRE Slave
0	0	TRI-STATE	Ext. SK	SI	MICROWIRE Slave

TIMER/COUNTER

The COP880C and COP881C have a powerful 16-bit timer with an associated 16-bit register enabling them to perform extensive timer functions. The timer T1 and its register R1 are each organized as two 8-bit read/write registers. Control bits in the register CNTRL allow the timer to be started and stopped under software control. The timer-register pair can be operated in one of three possible modes. Table V details various timer operating modes and their requisite control settings.

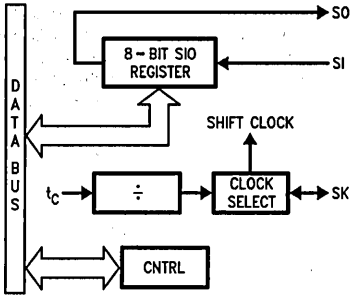

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FIGURE 7. MICROWIRE/PLUS Block Diagram

MODE 1. TIMER WITH AUTO-LOAD REGISTER

In this mode of operation, the timer T1 counts down at the instruction cycle rate. Upon underflow the value in the register R1 gets automatically reloaded into the timer which continues to count down. The timer underflow can be programmed to interrupt the microcontroller. A bit in the control register CNTRL enables the TIO (G3) pin to toggle upon timer underflows. This allow the generation of square-wave outputs or pulse width modulated outputs under software control. (See *Figure 9.*)

MODE 2. EXTERNAL COUNTER

In this mode, the timer T1 becomes a 16-bit external event counter. The counter counts down upon an edge on the TIO pin. Control bits in the register CNTRL program the counter to decrement either on a positive edge or on a negative edge. Upon underflow the contents of the register R1 are automatically copied into the counter. The underflow can also be programmed to generate an interrupt. (See *Figure 9*)

MODE 3. TIMER WITH CAPTURE REGISTER

Timer T1 can be used to precisely measure external frequencies or events in this mode of operation. The timer T1 counts down at the instruction cycle rate. Upon the occurrence of a specified edge on the TIO pin the contents of the timer T1 are copied into the register R1. Bits in the control register CNTRL allow the trigger edge to be specified either as a positive edge or as a negative edge. In this mode the user can elect to be interrupted on the specified trigger edge. (See *Figure 10.*)

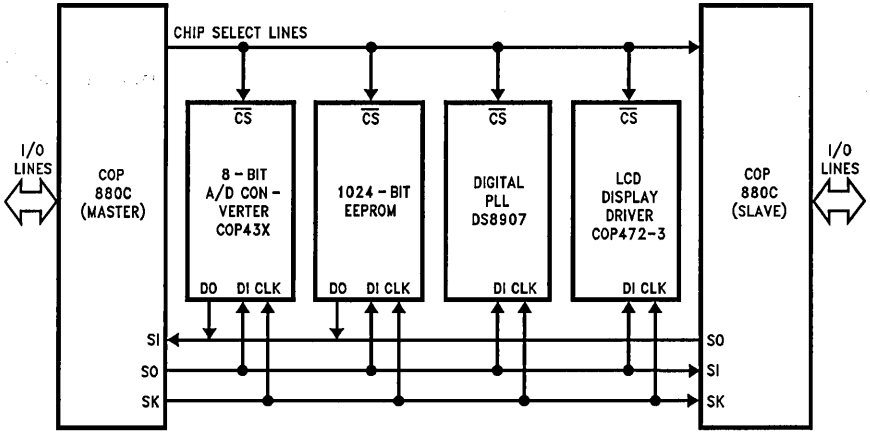

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FIGURE 8. MICROWIRE/PLUS Application

Functional Description (Continued)

TABLE V. Timer Operating Modes

CNTRL Bits 7 6 5	Operation Mode	T Interrupt	Timer Counts On
0 0 0	External Counter W/Auto-Load Reg.	Timer Carry	TIO Pos. Edge
0 0 1	External Counter W/Auto-Load Reg.	Timer Carry	TIO Neg. Edge
0 1 0	Not Allowed	Not Allowed	Not Allowed
0 1 1	Not Allowed	Not Allowed	Not Allowed
1 0 0	Timer W/Auto-Load Reg.	Timer Carry	t_C
1 0 1	Timer W/Auto-Load Reg./Toggle TIO Out	Timer Carry	t_C
1 1 0	Timer W/Capture Register	TIO Pos. Edge	t_C
1 1 1	Timer W/Capture Register	TIO Neg. Edge	t_C

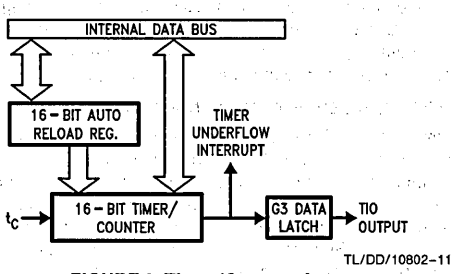


FIGURE 9. Timer/Counter Auto Reload Mode Block Diagram

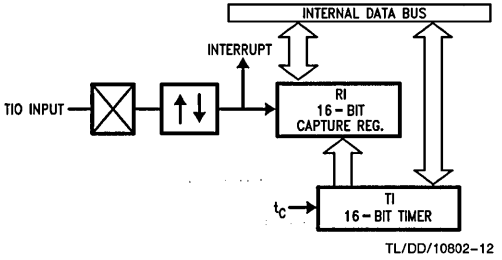


FIGURE 10. Timer Capture Mode Block Diagram

TIMER PWM APPLICATION

Figure 11 shows how a minimal component D/A converter can be built out of the Timer-Register pair in the Auto-Reload mode. The timer is placed in the "Timer with auto reload" mode and the TIO pin is selected as the timer output. At the outset the TIO pin is set high, the timer T1 holds the on time and the register R1 holds the signal off time. Setting TRUN bit starts the timer which counts down at the instruction cycle rate. The underflow toggles the TIO output and copies the off time into the timer, which continues to run. By alternately loading in the on time and the off time at each successive interrupt a PWM frequency can be easily generated.

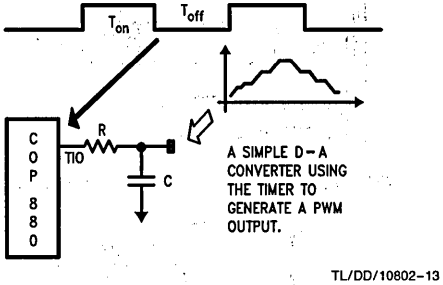


FIGURE 11. Timer Application

Control Registers

CNTRL REGISTER (ADDRESS X'00EE)

The Timer and MICROWIRE/PLUS control register contains the following bits:

S1 & S0 Select the MICROWIRE/PLUS clock divide-by

IEDG External interrupt edge polarity select (0 = rising edge, 1 = falling edge)

MSEL Enable MICROWIRE/PLUS functions SO and SK

TRUN Start/Stop the Timer/Counter (1 = run, 0 = stop)

TC3 Timer input edge polarity select (0 = rising edge, 1 = falling edge)

TC2 Selects the capture mode

TC1 Selects the timer mode

TC1	TC2	TC3	TRUN	MSEL	IEDG	S1	S0

BIT 7 BIT 0

PSW REGISTER (ADDRESS X'00EF)

The PSW register contains the following select bits:

GIE Global interrupt enable

ENI External interrupt enable

BUSY MICROWIRE/PLUS busy shifting

IPND External interrupt pending

ENTI Timer interrupt enable

TPND Timer interrupt pending

C Carry Flag

HC Half carry Flag

HC	C	TPND	ENTI	IPND	BUSY	ENI	GIE

Bit 7 Bit 0

Addressing Modes

REGISTER INDIRECT

This is the "normal" mode of addressing for COP880C and COP881C. The operand is the memory addressed by the B register or X register.

DIRECT

The instruction contains an 8-bit address field that directly points to the data memory for the operand.

IMMEDIATE

The instruction contains an 8-bit immediate field as the operand.

REGISTER INDIRECT (AUTO INCREMENT AND DECREMENT)

This is a register indirect mode that automatically increments or decrements the B or X register after executing the instruction.

RELATIVE

This mode is used for the JP instruction, the instruction field is added to the program counter to get the new program location. JP has a range of from −31 to +32 to allow a one byte relative jump (JP + 1 is implemented by a NOP instruction). There are no 'pages' when using JP, all 15 bits of PC are used.

Memory Map

All RAM, ports and registers (except A and PC) are mapped into data memory address space.

Address	Contents
00 to 6F	On Chip RAM Bytes
70 to 7F	Unused RAM Address Space (Reads as all Ones)
80 to BF	Expansion Space for on Chip EERAM
C0 to CF	Expansion Space for I/O and Registers
D0 to DF	On Chip I/O and Registers
D0	Port L Data Register
D1	Port L Configuration Register
D2	Port L Input Pins (Read Only)
D3	Reserved for Port L
D4	Port G Data Register
D5	Port G Configuration Register
D6	Port G Input Pins (Read Only)
D7	Port I Input Pins (Read Only)
D8	Port C Data Register
D9	Port C Configuration Register
DA	Port C Input Pins (Read Only)
DB	Reserved for Port C
DC	Port D Data Register
DD–DF	Reserved for Port D
E0 to EF	On Chip Functions and Registers
E0–E7	Reserved for Future Parts
E8	Reserved
E9	MICROWIRE/PLUS Shift Register
EA	Timer Lower Byte
EB	Timer Upper Byte
EC	Timer Autoload Register Lower Byte
ED	Timer Autoload Register Upper Byte
EE	CNTRL Control Register
EF	PSW Register
F0 to FF	On Chip RAM Mapped as Registers
FC	X Register
FD	SP Register
FE	B Register

Reading unused memory locations below 7FH will return all ones. Reading other unused memory locations will return undefined data.

Instruction Set

REGISTER AND SYMBOL DEFINITIONS

Registers

A	8-bit Accumulator register
B	8-bit Address register
X	8-bit Address register
SP	8-bit Stack pointer register
PC	15-bit Program counter register
PU	upper 7 bits of PC
PL	lower 8 bits of PC
C	1-bit of PSW register for carry
HC	Half Carry
GIE	1-bit of PSW register for global interrupt enable

Symbols

[B]	Memory indirectly addressed by B register
[X]	Memory indirectly addressed by X register
Mem	Direct address memory or [B]
Meml	Direct address memory or [B] or Immediate data
Imm	8-bit Immediate data
Reg	Register memory: addresses F0 to FF (Includes B, X and SP)
Bit	Bit number (0 to 7)
←	Loaded with
⟷	Exchanged with

Instruction Set

ADD	add	A ← A + Meml
ADC	add with carry	A ← A + Meml + C, C ← Carry HC ← Half Carry
SUBC	subtract with carry	A ← A + $\overline{\text{Meml}}$ + C, C ← Carry HC ← Half Carry
AND	Logical AND	A ← A and Meml
OR	Logical OR	A ← A or Meml
XOR	Logical Exclusive-OR	A ← A xor Meml
IFEQ	IF equal	Compare A and Meml, Do next if A = Meml
IFGT	IF greater than	Compare A and Meml, Do next if A > Meml
IFBNE	IF B not equal	Do next if lower 4 bits of B ≠ Imm
DRSZ	Decrement Reg. ,skip if zero	Reg ← Reg − 1, skip if Reg goes to 0
SBIT	Set bit	1 to bit, Mem (bit = 0 to 7 immediate)
RBIT	Reset bit	0 to bit, Mem
IFBIT	If bit	If bit, Mem is true, do next instr.
X	Exchange A with memory	A ⟷ Mem
LD A	Load A with memory	A ← Meml
LD mem	Load Direct memory Immed.	Mem ← Imm
LD Reg	Load Register memory Immed.	Reg ← Imm
X	Exchange A with memory [B]	A ⟷ [B] (B ← B±1)
X	Exchange A with memory [X]	A ⟷ [X] (X ← X±1)
LD A	Load A with memory [B]	A ← [B] (B ← B±1)
LD A	Load A with memory [X]	A ← [X] (X ← X±1)
LD M	Load Memory Immediate	[B] ← Imm (B ← B±1)
CLRA	Clear A	A ← 0
INCA	Increment A	A ← A + 1
DECA	Decrement A	A ← A − 1
LAID	Load A indirect from ROM	A ← ROM(PU,A)
DCORA	DECIMAL CORRECT A	A ← BCD correction (follows ADC, SUBC)
RRCA	ROTATE A RIGHT THRU C	C → A7 → ... → A0 → C
SWAPA	Swap nibbles of A	A7...A4 ⟷ A3...A0
SC	Set C	C ← 1, HC ← 1
RC	Reset C	C ← 0, HC ← 0
IFC	If C	If C is true, do next instruction
IFNC	If not C	If C is not true, do next instruction
JMPL	Jump absolute long	PC ← ii (ii = 15 bits, 0 to 32k)
JMP	Jump absolute	PC11..0 ← i (i = 12 bits)
JP	Jump relative short	PC ← PC + r (r is −31 to +32, not 1)
JSRL	Jump subroutine long	[SP] ← PL,[SP-1] ← PU,SP-2,PC ← ii
JSR	Jump subroutine	[SP] ← PL,[SP-1] ← PU,SP-2,PC11.. 0 ← i
JID	Jump indirect	PL ← ROM(PU,A)
RET	Return from subroutine	SP+2,PL ← [SP],PU ← [SP-1]
RETSK	Return and Skip	SP+2,PL ← [SP],PU ← [SP-1],Skip next instruction
RETI	Return from Interrupt	SP+2,PL ← [SP],PU ← [SP-1],GIE ← 1
INTR	Generate an interrupt	[SP] ← PL,[SP−1] ← PU,SP-2,PC ← 0FF
NOP	No operation	PC ← PC + 1

Bits 7–4

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
JP -15	JP -31	LD 0F0,#i	DRSZ 0F0	RRCA	RC	ADC A, #i	ADC A, [B]	IFBIT 0,[B]	*	LD B, 0F	IFBNE 0	JSR 0000-00FF	JMP 0000-00FF	JP + 17	INTR	0
JP -14	JP -30	LD 0F1,#i	DRSZ 0F1	*	SC	SUBC A, #i	SUBC A,[B]	IFBIT 1,[B]	*	LD B, 0E	IFBNE 1	JSR 0100-01FF	JMP 0100-01FF	JP + 18	JP + 2	1
JP -13	JP -29	LD 0F2,#i	DRSZ 0F2	X A, [X+]	X A, [B+]	IFEQ A, #i	IFEQ A,[B]	IFBIT 2,[B]	*	LD B, 0D	IFBNE 2	JSR 0200-02FF	JMP 0200-02FF	JP + 19	JP + 3	2
JP -12	JP -28	LD 0F3,#i	DRSZ 0F3	X A, [X−]	X A, [B−]	IFGT A, #i	IFGT A,[B]	IFBIT 3,[B]	*	LD B, 0C	IFBNE 3	JSR 0300-03FF	JMP 0300-03FF	JP + 20	JP + 4	3
JP -11	JP -27	LD 0F4,#i	DRSZ 0F4	*	LAID	ADD A, #i	ADD A,[B]	IFBIT 4,[B]	CLRA	LD B, 0B	IFBNE 4	JSR 0400-04FF	JMP 0400-04FF	JP + 21	JP + 5	4
JP -10	JP -26	LD 0F5,#i	DRSZ 0F5	*	JID	AND A, #i	AND A,[B]	IFBIT 5,[B]	SWAPA	LD B, 0A	IFBNE 5	JSR 0500-05FF	JMP 0500-05FF	JP + 22	JP + 6	5
JP -9	JP -25	LD 0F6,#i	DRSZ 0F6	X A, [X]	X A, [B]	XOR A, #i	XOR A,[B]	IFBIT 6,[B]	DCORA	LD B, 9	IFBNE 6	JSR 0600-06FF	JMP 0600-06FF	JP + 23	JP + 7	6
JP -8	JP -24	LD 0F7,#i	DRSZ 0F7	*	*	OR A, #i	OR A,[B]	IFBIT 7,[B]	*	LD B, 8	IFBNE 7	JSR 0700-07FF	JMP 0700-07FF	JP + 24	JP + 8	7
JP -7	JP -23	LD 0F8,#i	DRSZ 0F8	NOP	*	LD A, #i	IFC	SBIT 0,[B]	RBIT 0,[B]	LD B, 7	IFBNE 8	JSR 0800-08FF	JMP 0800-08FF	JP + 25	JP + 9	8
JP -6	JP -22	LD 0F9,#i	DRSZ 0F9	*	*	*	IFNC	SBIT 1,[B]	RBIT 1,[B]	LD B, 6	IFBNE 9	JSR 0900-09FF	JMP 0900-09FF	JP + 26	JP + 10	9
JP -5	JP -21	LD 0FA,#i	DRSZ 0FA	LD A, [X+]	LD A, [B+]	LD [B+],#i	INCA	SBIT 2,[B]	RBIT 2,[B]	LD B, 5	IFBNE 0A	JSR 0A00-0AFF	JMP 0A00-0AFF	JP + 27	JP + 11	A
JP -4	JP -20	LD 0FB,#i	DRSZ 0FB	LD A, [X−]	LD A, [B−]	LD [B−],#i	DECA	SBIT 3,[B]	RBIT 3,[B]	LD B, 4	IFBNE 0B	JSR 0B00-0BFF	JMP 0B00-0BFF	JP + 28	JP + 12	B
JP -3	JP -19	LD 0FC,#i	DRSZ 0FC	LD Md, #i	JMPL	X A,Md	*	SBIT 4,[B]	RBIT 4,[B]	LD B, 3	IFBNE 0C	JSR 0C00-0CFF	JMP 0C00-0CFF	JP + 29	JP +13	C
JP -2	JP -18	LD 0FD,#i	DRSZ 0FD	DIR	JSRL	LD A, Md	RETSK	SBIT 5,[B]	RBIT 5,[B]	LD B, 2	IFBNE 0D	JSR 0D00-0DFF	JMP 0D00-0DFF	JP + 30	JP +14	D
JP -1	JP -17	LD 0FE,#i	DRSZ 0FE	LD A, [X]	LD A, [B]	LD [B], #i	RET	SBIT 6, [B]	RBIT 6, [B]	LD B, 1	IFBNE 0E	JSR 0E00−0EFF	JMP 0E00−0EFF	JP + 31	JP +15	E
JP -0	JP -16	LD 0FF,#1	DRSZ 0FF	*	*	*	RETI	SBIT 7,[B]	RBIT 7,[B]	LD B, 0	IFBNE 0F	JSR 0F00-0FFF	JMP 0F00-0FFF	JP + 32	JP + 16	F

Bits 3–0

where, **i** is the immediate data Md is a directly addressed memory location * is an unused opcode (see following table)

Instruction Execution Time

Most instructions are single byte (with immediate addressing mode instruction taking two bytes).

Most single instructions take one cycle time to execute.

See the BYTES and CYCLES per INSTRUCTION table for details.

BYTES and CYCLES per INSTRUCTION

The following table shows the number of bytes and cycles for each instruction in the format of byte/cycle.

	[B]	Direct	Immed.
ADD	1/1	3/4	2/2
ADC	1/1	3/4	2/2
SUBC	1/1	3/4	2/2
AND	1/1	3/4	2/2
OR	1/1	3/4	2/2
XOR	1/1	3/4	2/2
IFEQ	1/1	3/4	2/2
IFGT	1/1	3/4	2/2
IFBNE	1/1		
DRSZ		1/3	
SBIT	1/1	3/4	
RBIT	1/1	3/4	
IFBIT	1/1	3/4	

Memory Transfer Instructions

	Register Indirect		Direct	Immed.	Register Indirect Auto Incr & Decr		
	[B]	[X]			[B+, B−]	[X+, X−]	
X A,*	1/1	1/3	2/3		1/2	1/3	
LD A,*	1/1	1/3	2/3	2/2	1/2	1/3	
LD B,Imm				1/1			(If B < 16)
LD B,Imm				2/3			(If B > 15)
LD Mem,Imm	2/2		3/3		2/2		
LD Reg,Imm				2/3			

* => Memory location addressed by B or X or directly.

Instructions Using A & C

CLRA	1/1
INCA	1/1
DECA	1/1
LAID	1/3
DCORA	1/1
RRCA	1/1
SWAPA	1/1
SC	1/1
RC	1/1
IFC	1/1
IFNC	1/1

Transfer of Control Instructions

JMPL	3/4
JMP	2/3
JP	1/3
JSRL	3/5
JSR	2/5
JID	1/3
RET	1/5
RETSK	1/5
RETI	1/5
INTR	1/7
NOP	1/1

BYTES and CYCLES per INSTRUCTION (Continued)

The following table shows the instructions assigned to unused opcodes. This table is for information only. The operations performed are subject to change without notice. Do not use these opcodes.

Unused Opcode	Instruction	Unused Opcode	Instruction
60	NOP	A9	NOP
61	NOP	AF	LD A, [B]
62	NOP	B1	C → HC
63	NOP	B4	NOP
67	NOP	B5	NOP
8C	RET	B7	X A, [X]
99	NOP	B9	NOP
9F	LD [B], #i	BF	LD A, [X]
A7	X A, [B]		
A8	NOP		

Option List

The COP880C/COP881C mask programmable options are listed out below. The options are programmed at the same time as the ROM pattern to provide the user with hardware flexibility to use a variety of oscillator configuration.

OPTION 1: CKI INPUT

= 1 Crystal (CKI/10) CKO for crystal configuration

= 2 External (CKI/10) CKO available as G7 input

= 3 R/C (CKI/10) CKO available as G7 input

OPTION 2: COP880C/COP881C BONDING

= 1 44-Pin PLCC

= 2 40-Pin DIP

= 3 28-Pin SO

= 4 28-Pin DIP

The following option information is to be sent to National along with the EPROM.

Option Data

Option 1 Value_is: CKI Input

Option 2 Value_is: COP Bonding

Development Support

IN-CIRCUIT EMULATOR

The MetaLink iceMASTER™-COP8 Model 400 In-Circuit Emulator for the COP8 family of microcontrollers features high-performance operation, ease of use, and an extremely flexible user-interface for maximum productivity. Interchangeable probe cards, which connect to the standard common base, support the various configurations and packages of the COP8 family.

The iceMASTER provides real-time, full-speed emulation up to 10 MHz, 32 kbytes of emulation memory and 4k frames of trace buffer memory. The user may define as many as 32k trace and break triggers which can be enabled, disabled, set or cleared. They can be simple triggers based on code or address ranges or complex triggers based on code address, direct address, opcode value, opcode class or immediate operand. Complex breakpoints can be ANDed and ORed together. Trace information consists of address bus values, opcodes and user selectable probe clips status (external event lines). The trace buffer can be viewed as raw hex or as disassembled instructions. The probe clip bit values can be displayed in binary, hex or digital waveform formats.

During single-step operation the dynamically annotated code feature displays the contents of all accessed (read and write) memory locations and registers, as well as flow-of-control direction change markers next to each instruction executed.

The iceMASTER's performance analyzer offers a resolution of better than 6 μs. The user can easily monitor the time spent executing specific portions of code and find "hot spots" or "dead code". Up to 15 independent memory areas based on code address or label ranges can be defined. Analysis results can be viewed in bargraph format or as actual frequency count.

Emulator memory operations for program memory include single line assembler, disassembler, view, change and write to file. Data memory operations include fill, move, compare, dump to file, examine and modify. The contents of any memory space can be directly viewed and modified from the corresponding window.

The iceMASTER comes with an easy-to-use windowed interface. Each window can be sized, highlighted, color-controlled, added, or removed completely. Commands can be accessed via pull-down menus and/or redefinable hot keys. A context sensitive hypertext/hyperlinked on-line help system explains clearly the options the user has from within any window.

The iceMASTER connects easily to a PC via the standard COMM port and its 115.2 kBaud serial link keeps typical program download time to under 3 seconds.

The following tables list the emulator and probe cards ordering information.

Emulator Ordering Information

Part Number	Description
IM-COP8/400	MetaLink base unit in-circuit emulator for all COP8 devices, symbolic debugger software and RS-232 serial interface cable
MHW-PS3	Power Supply 110V/60 Hz
MHW-PS4	Power Supply 220V/50 Hz

Probe Card Ordering Information

Part Number	Package	Voltage Range	Emulates
MHW-880C28D5PC	28 DIP	4.5V–5.5V	COP820C, 840C, 881C, 8781C
MHW-880C28DWPC	28 DIP	2.5V–6.0V	COP820C, 840C, 881C, 8781C
MHW-880C40D5PC	40 DIP	4.5V–5.5V	COP880C, 8780C
MHW-880C40DWPC	40 DIP	2.5V–6.0V	COP880C, 8780C
MHW-880C44D5PC	44 PLCC	4.5V–5.5V	COP880C, 8780C
MHW-880C44DWPC	44 PLCC	2.5V–6.0V	COP880C, 8780C

MACRO CROSS ASSEMBLER

National Semiconductor offers a COP8 macro cross assembler. It runs on industry standard compatible PCs and supports all of the full-symbolic debugging features of the MetaLink iceMASTER emulators.

Assembler Ordering Information

Part Number	Description	Manual
MOLE-COP8-IBM	COP8 macro cross assembler for IBM PC-XT®, PC-AT®, or compatible	424410527-001

Development Support (Continued)

SINGLE-CHIP EMULATOR DEVICE

The COP8 family is fully supported by single chip form, fit and function emulators. Two types of single-chip emulators are available: Multi-Chip Module emulators, which combine the microcontroller-die and an EPROM-die in one package, and emulators where the microcontroller's standard ROM has been replaced with an on-chip EPROM. For more detailed information, refer to the emulation device specific data sheets and the form, fit, function emulator selection table below.

Single-Chip Emulator Selection Table

Device Number	Clock Option	Package	Description	Emulates
COP880CMHEL-X	X = 1: Crystal X = 2: External X = 3: R/C	44 LDCC	Multi-Chip Module (MCM), UV Erasable	COP880C
COP880CMHD-X	X = 1: Crystal X = 2: External X = 3: R/C	40 DIP	MCM, UV Erasable	COP880C
COP881CMHD-X	X = 1: Crystal X = 2: External X = 3: R/C	28 DIP	MCM, UV Erasable	COP881C
COP881CMHEA-X	X = 1: Crystal X = 2: External X = 3: R/C	28 LCC	MCM (Same Footprint as 28 SO), UV Erasable	COP881C
COP8780CV	Programmable	44 PLCC	One-Time Programmable (OTP)	COP880C
COP8780CEL	Programmable	44 LDCC	UV Erasable	COP880C
COP8780CN	Programmable	40 DIP	OTP	COP880C
COP8780CJ	Programmable	40 DIP	UV Erasable	COP880C
COP8781CN	Programmable	28 DIP	OTP	COP881C
COP8781CJ	Programmable	28 DIP	UV Erasable	COP881C
COP8781CWM	Programmable	28 SO	OTP	COP881C
COP8781CMC	Programmable	28 SO	UV Erasable	COP881C

PROGRAMMING SUPPORT

Programming of the single-chip emulator devices is supported by different sources. National Semiconductor offers a duplicator board which allows the transfer of program code from a standard programmed EPROM to the single-chip emulator and vice versa. Data I/O supports COP8 emulator device programming with its UniSite 48 and System 2900 programmers. Further information on Data I/O programmers can be obtained from any Data I/O sales office or the following USA numbers:

Telephone: (206) 881-6444 FAX: (206) 882-1043

Duplicator Board Ordering Information

Part Number	Description	Devices Supported
COP8-PRGM-28D	Duplicator Board for 28 DIP Multi-Chip Module (MCM) and for Use with Scrambler Boards	COP881CMHD
COP8-SCRM-DIP	MCM Scrambler Board for 40 DIP Socket	COP880CMHD
COP8-SCRM-PCC	MCM Scrambler Board for 44 PLCC/LDCC	COP880CMHEL
COP8-SCRM-SBX	MCM Scrambler Board for 28 LCC Socket	COP881CMHEA
COP8-PRGM-DIP	Duplicator Board with COP8-SCRM-DIP Scrambler Board	COP881CMHD, COP880CMHD
COP8-PRGM-PCC	Duplicator Board with COP8-SCRM-PCC Scrambler Board	COP880CMEL, COP881CMHD
COP8-PRGM-87A	Duplicator Board with COP87XX Scrambler for 28 DIP, 28 SO, and 40 DIP	COP8781CN, COP8781CJ, COP8781CWM, COP8781CMC, COP8780CN, COP8780CJ
COP8-PRGM-87B	Duplicator Board with COP87XX Scrambler for 44 PLCC/LDCC	COP8780CV, COP8780CEL

Development Support (Continued)

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications Group. The Dial-A-Helper is an Electronic Bulletin Board information system.

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down-loaded to disk for later use.

FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factory applications support. If a user has questions, he can leave messages on our electronic bulletin board, which we will respond to, or under extraordinary circumstances he can arrange for us to actually take control of his system via modem for debugging purposes.

Voice: (408) 721-5582

Modem: (408) 739-1162

Baud:	300 or 1200 baud	
Setup:	Length:	8-Bit
	Parity:	None
	Stop Bit:	1
Operation:	24 Hrs. 7 Days	

National Semiconductor

COP988CF/COP984CF/COP888CF/COP884CF Single-Chip microCMOS Microcontroller

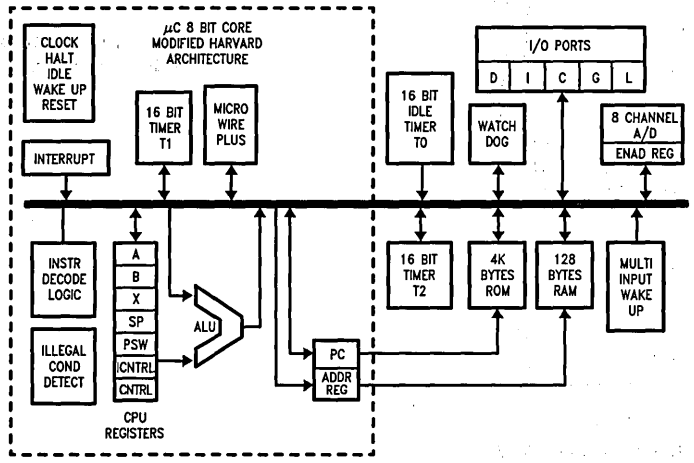
General Description

The COP888 family of microcontrollers uses an 8-bit single chip core architecture fabricated with National Semiconductor's M²CMOS™ process technology. The COP888CF is a member of this expandable 8-bit core processor family of microcontrollers. (Continued)

Features

- Low cost 8-bit microcontroller
- Fully static CMOS, with low current drain
- Two power saving modes: HALT and IDLE
- 1 μs instruction cycle time
- 4096 bytes on-board ROM
- 128 bytes on-board RAM
- Single supply operation: 2.5V–6V
- 8-channel A/D converter with prescaler and both differential and single ended modes
- MICROWIRE/PLUS™ serial I/O
- WATCHDOG™ and Clock Monitor logic
- Ten multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Two Timers (Each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS
- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- Two 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers (B and X)
- Versatile instruction set
- True bit manipulation
- Memory mapped I/O
- BCD arithmetic instructions
- Package: 44 PLCC or 40 N
  - — 44 PLCC with 37 I/O pins
  - — 40 N with 33 I/O pins
  - — 28 SO or 28 N, each with 23 I/O pins
- Software selectable I/O options
  - — TRI-STATE® Output
  - — Push-Pull Output
  - — Weak Pull Up Input
  - — High Impedance Input
- Schmitt trigger inputs on ports G and L
- Temperature ranges: 0°C to +70°C
  −40°C to+ 85°C
- Emulation device—COP888CFMH
- Real time emulation and full program debug offered by National's Development Systems

Block Diagram



TL/DD/9425–1

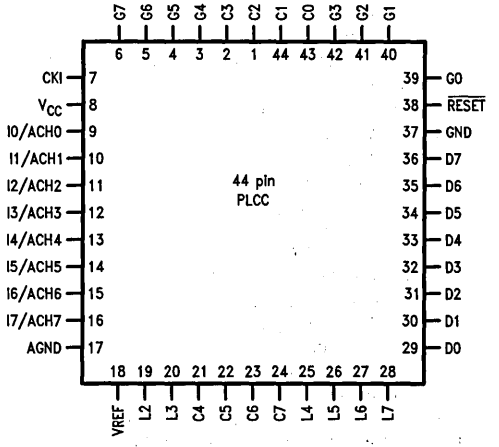
FIGURE 1. COP888CF Block Diagram

General Description (Continued)

It is a fully static part, fabricated using double-metal silicon gate microCMOS technology. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS serial I/O, two 16-bit timer/counters supporting three modes (Processor Independent PWM generation, External Event counter, and Input Capture mode capabilities), an 8-channel, 8-bit A/D converter with both differential and single ended modes, and two power savings modes (HALT and IDLE), both with a multi-sourced wakeup/interrupt capability. This multi-sourced interrupt capability may also be used independent of the HALT or IDLE modes. Each I/O pin has software selectable configurations. The COP888CF operates over a voltage range of 2.5V to 6V. High throughput is achieved with an efficient, regular instruction set operating at a maximum of 1 μs per instruction rate.

Connection Diagrams

Plastic Chip Carrier

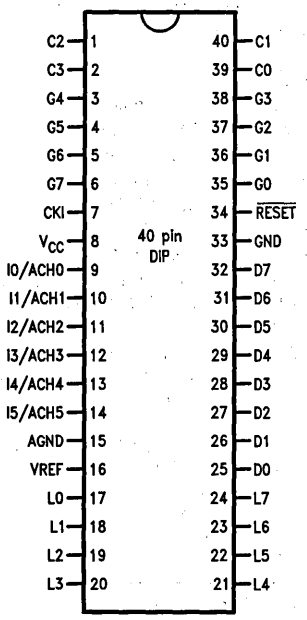


TL/DD/9425-2

Top View

Order Number COP888CF-XXX/V
See NS Plastic Chip Package Number V44A

Dual-In-Line Package

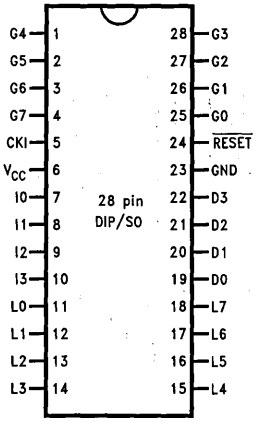


TL/DD/9425-4

Top View

Order Number COP888F-XXX/N
See NS Molded Package Number N40A

Dual-In-Line Package



TL/DD/9425-37

Top View

Order Number COP884CF-XXX/N
or COP884CF-XXX/WM
See NS Package Number D28G or M28B

FIGURE 2. COP888CF/COP884CF Connection Diagrams

Connection Diagrams (Continued)

COP888CF Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	—
L1	I/O	MIWU		12	18	—
L2	I/O	MIWU		13	19	19
L3	I/O	MIWU		14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU		17	23	27
L7	I/O	MIWU		18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
I0	I	ACH0		7	9	9
I1	I	ACH1		8	10	10
I2	I	ACH2			11	11
I3	I	ACH3			12	12
I4	I	ACH4			13	13
I5	I	ACH5			14	14
I6	I	ACH6				15
I7	I	ACH7				16
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{REF}	$+V_{REF}$			10	16	18
AGND	AGND			9	15	17
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics 988CF: $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage					
988CF		2.5		4.0	V
998CFH		4.0		6.0	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			5.5	mA
CKI = 4 MHz	V_{CC} = 4V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			1.4	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<0.7	8	μA
	V_{CC} = 4.0V, CKI = 0 MHz		<0.3	4	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4.0V, t_c = 10 μs			0.7	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6V	−1		+1	μA
Input Pullup Current	V_{CC} = 6V	40		250	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4V, V_{OL} = 1V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2.0			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4V, V_{OH} = 2.7V	10		100	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink (Push-Pull Mode)	V_{CC} = 4V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			mA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The A/D is disabled. V_{REF} is tied to AGND (effectively shorting the Reference resistor). The clock monitor is disabled.

DC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
TRI-STATE Leakage	$V_{CC} = 6.0V$	−1		+1	μA
Allowable Sink/Source Current per Pin D Outputs (Sink) All others				 15 3	 mA mA
Maximum Input Current without Latchup (Note 6)	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

A/D Converter Specifications $V_{CC} = 5V \pm 10\%$ $(V_{SS} - 0.050V) \le$ Any Input $\le (V_{CC} + 0.050V)$

Parameter	Conditions	Min	Typ	Max	Units
Resolution				8	Bits
Reference Voltage Input	AGND = 0V	3		V_{CC}	V
Absolute Accuracy	$V_{REF} = V_{CC}$			±1	LSB
Non-Linearity	$V_{REF} = V_{CC}$ Deviation from the Best Straight Line			±½	LSB
Differential Non-Linearity	$V_{REF} = V_{CC}$			±½	LSB
Input Reference Resistance		1.6		4.8	kΩ
Common Mode Input Range (Note 7)		AGND		V_{REF}	V
DC Common Mode Error				±¼	LSB
Off Channel Leakage Current			1		μA
On Channel Leakage Current			1		μA
A/D Clock Frequency (Note 5)		0.1		1.67	MHz
Conversion Time (Note 4)			12		A/D Clock Cycles

Note 4: Conversion Time includes sample and hold time.

Note 5: See Prescaler description.

Note 6: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Note 7: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input. The diodes will forward conduct for analog input voltages below ground or above the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

AC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal, Resonator	$4V \le V_{CC} \le 6V$	1		DC	μs
	$2.5V \le V_{CC} < 4V$	2.5		DC	μs
R/C Oscillator	$4V \le V_{CC} \le 6V$	3		DC	μs
	$2.5V \le V_{CC} < 4V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 8)	f_r = Max	40		60	%
Rise Time (Note 8)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 8)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	$4V \le V_{CC} \le 6V$	200			ns
	$2.5V \le V_{CC} < 4V$	500			ns
t_{HOLD}	$4V \le V_{CC} \le 6V$	60			ns
	$2.5V \le V_{CC} < 4V$	150			ns
Output Propagation Delay	R_L = 2.2k, C_L = 100 pF				
t_{PD1}, t_{PD0}					
SO, SK	$4V \le V_{CC} \le 6V$			0.7	μs
	$2.5V \le V_{CC} < 4V$			1.75	μs
All Others	$4V \le V_{CC} \le 6V$			1	μs
	$2.5V \le V_{CC} < 4V$			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 8: Parameter sample (not 100% tested).

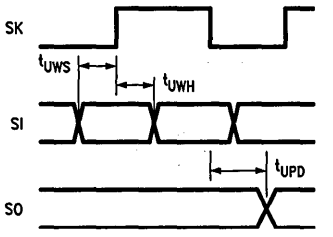


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FIGURE 3. MICROWIRE/PLUS Timing

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics 888CF: $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		2.5		6	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			5.5	mA
CKI = 4 MHz	V_{CC} = 4V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			1.4	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<1	10	μA
	V_{CC} = 4V, CKI = 0 MHz		<0.5	6	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			0.7	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6V	−2		+2	μA
Input Pullup Current	V_{CC} = 6V	40		250	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4V, V_{OL} = 1V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2.0			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4V, V_{OH} = 2.7V	10		100	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink (Push-Pull Mode)	V_{CC} = 4V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			mA
TRI-STATE Leakage	V_{CC} = 6.0V	−2		+2	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The A/D is disabled. V_{REF} is tied to AGND (effectively shorting the Reference resistor). The clock monitor is disabled.

DC Electrical Characteristics 888CF: $-40°C \le T_A \le +85°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin D Outputs (Sink) All others				 15 3	 mA mA
Maximum Input Current without Latchup (Note 6)	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

A/D Converter Specifications 888CF:

$V_{CC} = 5V \pm 10\%$ ($V_{SS} - 0.050V$) ≤ Any Input ≤ ($V_{CC} + 0.050V$)

Parameter	Conditions	Min	Typ	Max	Units
Resolution				8	Bits
Reference Voltage Input	AGND = 0V	3		V_{CC}	V
Absolute Accuracy	$V_{REF} = V_{CC}$			±1	LSB
Non-Linearity	$V_{REF} = V_{CC}$ Deviation from the Best Straight Line			±½	LSB
Differential Non-Linearity	$V_{REF} = V_{CC}$			±½	LSB
Input Reference Resistance		1.6		4.8	kΩ
Common Mode Input Range (Note 7)		AGND		V_{REF}	V
DC Common Mode Error				±¼	LSB
Off Channel Leakage Current			1		μA
On Channel Leakage Current			1		μA
A/D Clock Frequency (Note 5)		0.1		1.67	MHz
Conversion Time (Note 4)			12		A/D Clock Cycles

Note 4: Conversion Time includes sample and hold time.

Note 5: See Prescaler description.

Note 6: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Note 7: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input. The diodes will forward conduct for analog input voltages below ground or above the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

AC Electrical Characteristics 888CF: $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal, Resonator	$4V \le V_{CC} \le 6V$	1		DC	μs
	$2.5V \le V_{CC} < 4V$	2.5		DC	μs
R/C Oscillator	$4V \le V_{CC} \le 6V$	3		DC	μs
	$2.5V \le V_{CC} < 4V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 8)	f_r = Max	40		60	%
Rise Time (Note 8)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 8)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	$4V \le V_{CC} \le 6V$	200			ns
	$2.5V \le V_{CC} < 4V$	500			ns
t_{HOLD}	$4V \le V_{CC} \le 6V$	60			ns
	$2.5V \le V_{CC} < 4V$	150			ns
Output Propagation Delay	R_L = 2.2k, C_L = 100 pF				
t_{PD1}, t_{PD0}					
SO, SK	$4V \le V_{CC} \le 6V$			0.7	μs
	$2.5V \le V_{CC} < 4V$			1.75	μs
All Others	$4V \le V_{CC} \le 6V$			1	μs
	$2.5V \le V_{CC} < 4V$			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 8: Parameter sample (not 100% tested).

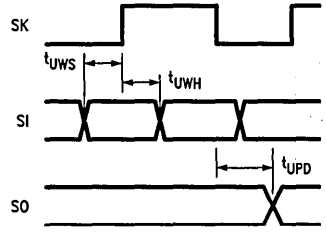

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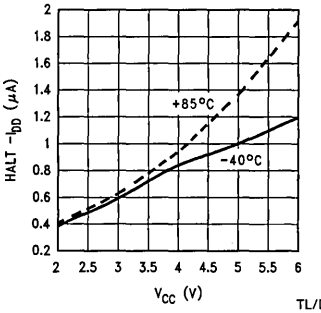
FIGURE 3. MICROWIRE/PLUS Timing

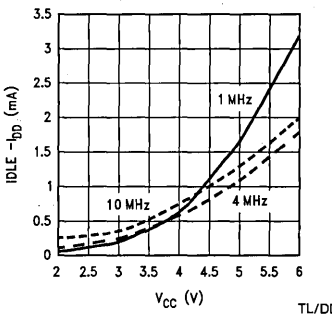
Typical Performance Characteristics

Halt—I_{DD} vs V_{CC}



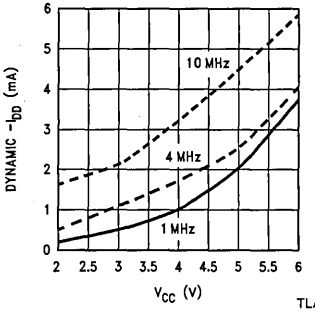
TL/DD/9425-29

Idle—I_{DD} (Crystal Clock Option)



TL/DD/9425-30

Dynamic—I_{DD} (Crystal Clock Option)



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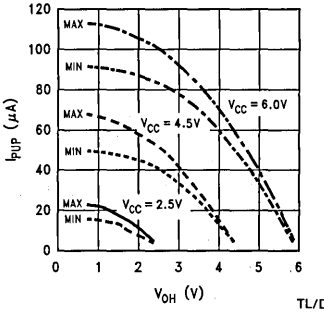
Port L/C/G Weak Pull-Up Source Current



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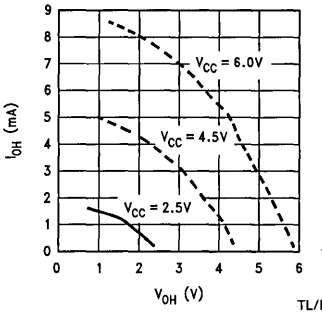
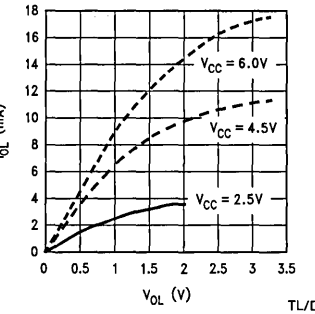
Port L/C/G Push-Pull Source Current



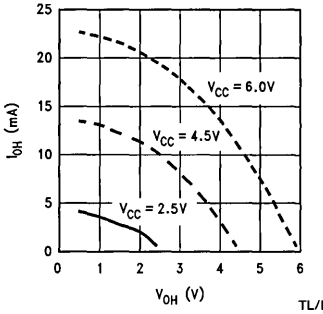
TL/DD/9425-33

Port L/C/G Push-Pull Sink Current



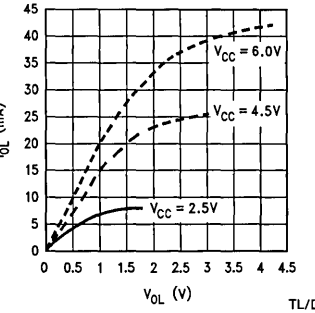
TL/DD/9425-34

Port D Source Current



TL/DD/9425-35

Port D Sink Current



TL/DD/9425-36

Pin Descriptions

V_{CC} and GND are the power supply pins.

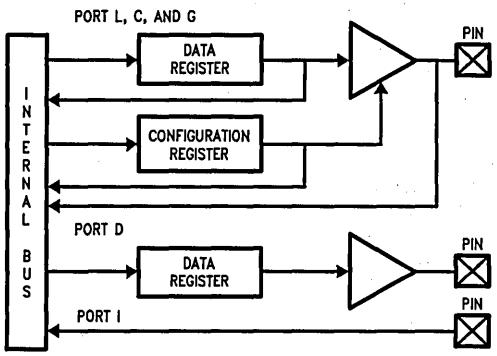
V_{REF} and AGND are the reference voltage pins for the on-board A/D converter.

CKI is the clock input. This can come from an R/C generated oscillator, or a crystal oscillator (in conjunction with CKO). See Oscillator Description section.

$\overline{\text{RESET}}$ is the master reset input. See Reset Description section.

The COP888CF contains three bidirectional 8-bit I/O ports (C, G and L), where each individual bit may be independently configured as an input (Schmitt trigger inputs on ports G and L), output or TRI-STATE under program control. Three data memory address locations are allocated for each of these I/O ports. Each I/O port has two associated 8-bit memory mapped registers, the CONFIGURATION register and the output DATA register. A memory mapped address is also reserved for the input pins of each I/O port. (See the COP888CF memory map for the various addresses associated with the I/O ports.) *Figure 4* shows the I/O port configurations for the COP888CF. The DATA and CONFIGURATION registers allow for each port bit to be individually configured under software control as shown below:

CONFIGURATION Register	DATA Register	Port Set-Up
0	0	Hi-Z Input (TRI-STATE Output)
0	1	Input with Weak Pull-Up
1	0	Push-Pull Zero Output
1	1	Push-Pull One Output



TL/DD/9425–6

FIGURE 4. I/O Port Configurations

PORT L is an 8-bit I/O port. All L-pins have Schmitt triggers on the inputs.

Port L supports Multi-Input Wakeup (MIWU) on all eight pins. L4 and L5 are used for the timer input functions T2A and T2B. L0 and L1 are not available on the 44-pin version of the COP888CF, since they are replaced by V_{REF} and AGND. L0 and L1 are not terminated on the 44-pin version. Consequently, reading L0 or L1 as inputs will return unreliable data with the 44-pin package, so this data should be masked out with user software when the L port is read for input data. It is recommended that the pins be configured as outputs.

Port L has the following alternate features:

- L0 MIWU
- L1 MIWU
- L2 MIWU
- L3 MIWU
- L4 MIWU or T2A
- L5 MIWU or T2B
- L6 MIWU
- L7 MIWU

Port G is an 8-bit port with 5 I/O pins (G0, G2–G5), an input pin (G6), and two dedicated output pins (G1 and G7). Pins G0 and G2–G6 all have Schmitt Triggers on their inputs. Pin G1 serves as the dedicated WDOUT WatchDog output, while pin G7 is either input or output depending on the oscillator mask option selected. With the crystal oscillator option selected, G7 serves as the dedicated output pin for the CKO clock output. With the single-pin R/C oscillator mask option selected, G7 serves as a general purpose input pin, but is also used to bring the device out of HALT mode with a low to high transition on G7. There are two registers associated with the G Port, a data register and a configuration register. Therefore, each of the 5 I/O bits (G0, G2–G5) can be individually configured under software control.

Since G6 is an input only pin and G7 is the dedicated CKO clock output pin or general purpose input (R/C clock configuration), the associated bits in the data and configuration registers for G6 and G7 are used for special purpose functions as outlined below. Reading the G6 and G7 data bits will return zeros.

Note that the chip will be placed in the HALT mode by writing a "1" to bit 7 of the Port G Data Register. Similarly the chip will be placed in the IDLE mode by writing a "1" to bit 6 of the Port G Data Register.

Writing a "1" to bit 6 of the Port G Configuration Register enables the MICROWIRE/PLUS to operate with the alternate phase of the SK clock. The G7 configuration bit, if set high, enables the clock start up delay after HALT when the R/C clock configuration is used.

	Config Reg.	Data Reg.
G7	CLKDLY	HALT
G6	Alternate SK	IDLE

Port G has the following alternate features:

- G0 INTR (External Interrupt Input)
- G2 T1B (Timer T1 Capture Input)
- G3 T1A (Timer T1 I/O)
- G4 SO (MICROWIRE Serial Data Output)
- G5 SK (MICROWIRE Serial Clock)
- G6 SI (MICROWIRE Serial Data Input)

Port G has the following dedicated functions:

- G1 WDOUT WatchDog and/or Clock Monitor dedicated output
- G7 CKO Oscillator dedicated output or general purpose input

Port C is an 8-bit I/O port. The 40-pin device does not have a full complement of Port C pins. The unavailable pins are not terminated. A read operation for these unterminated pins will return unpredictable values.

Pin Descriptions (Continued)

Port I is an 8-bit Hi-Z input port, and also provides the analog inputs to the A/D converter. The 28-pin device does not have a full complement of Port I pins. The unavailable pins are not terminated (i.e. they are floating). A read operation from these unterminated pins will return unpredictable values. The user should ensure that the software takes this into account by either masking out these inputs, or else restricting the accesses to bit operations only. If unterminated, Port I pins will draw power only when addressed.

Port D is an 8-bit output port that is preset high when RESET goes low. The user can tie two or more D port outputs together in order to get a higher drive.

Functional Description

The architecture of the COP888CF is modified Harvard architecture. With the Harvard architecture, the control store program memory (ROM) is separated from the data store memory (RAM). Both ROM and RAM have their own separate addressing space with separate address buses. The COP888CF architecture, though based on Harvard architecture, permits transfer of data from ROM to RAM.

CPU REGISTERS

The CPU can do an 8-bit addition, subtraction, logical or shift operation in one instruction (t_C) cycle time.

There are five CPU registers:

A is the 8-bit Accumulator Register

PC is the 15-bit Program Counter Register

PU is the upper 7 bits of the program counter (PC)
PL is the lower 8 bits of the program counter (PC)

B is an 8-bit RAM address pointer, which can be optionally post auto incremented or decremented.

X is an 8-bit alternate RAM address pointer, which can be optionally post auto incremented or decremented.

SP is the 8-bit stack pointer, which points to the subroutine/interrupt stack (in RAM). The SP is initialized to RAM address 06F with reset.

All the CPU registers are memory mapped with the exception of the Accumulator (A) and the Program Counter (PC).

PROGRAM MEMORY

Program memory for the COP888CF consists of 4096 bytes of ROM. These bytes may hold program instructions or constant data (data tables for the LAID instruction, jump vectors for the JID instruction, and interrupt vectors for the VIS instruction). The program memory is addressed by the 15-bit program counter (PC). All interrupts in the COP888CF vector to program memory location 0FF Hex.

DATA MEMORY

The data memory address space includes the on-chip RAM and data registers, the I/O registers (Configuration, Data and Pin), the control registers, the MICROWIRE/PLUS SIO shift register, and the various registers, and counters associated with the timers (with the exception of the IDLE timer). Data memory is addressed directly by the instruction or indirectly by the B, X and SP pointers.

The COP888CF has 128 bytes of RAM. Sixteen bytes of RAM are mapped as "registers" at addresses 0F0 to 0FF Hex. These registers can be loaded immediately, and also decremented and tested with the DRSZ (decrement register and skip if zero) instruction. The memory pointer registers X, SP, and B are memory mapped into this space at address locations 0FC to 0FE Hex respectively, with the other registers (other than reserved register 0FF) being available for general usage.

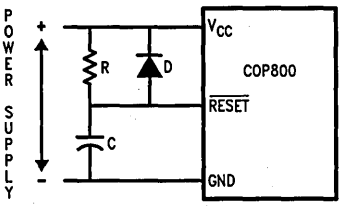
The instruction set of the COP888CF permits any bit in memory to be set, reset or tested. All I/O and registers on the COP888CF (except A and PC) are memory mapped; therefore, I/O bits and register bits can be directly and individually set, reset and tested. The accumulator (A) bits can also be directly and individually tested.

Reset

The $\overline{\text{RESET}}$ input when pulled low initializes the microcontroller. Initialization will occur whenever the $\overline{\text{RESET}}$ input is pulled low. Upon initialization, the data and configuration registers for Ports L, G, and C are cleared, resulting in these Ports being initialized to the TRI-STATE mode. Pin G1 of the G Port is an exception (as noted below) since pin G1 is dedicated as the WatchDog and/or Clock Monitor error output pin. Port D is initialized high with $\overline{\text{RESET}}$. The PC, PSW, CNTRL, ICNTRL, and T2CNTRL control registers are cleared. The Multi-Input Wakeup registers WKEN, WKEDG, and WKPND are cleared. The A/D control register ENAD is cleared, resulting in the ADC being powered down initially. The Stack Pointer, SP, is initialized to 06F Hex.

The COP888CF comes out of reset with both the WatchDog logic and the Clock Monitor detector armed, and with both the WatchDog service window bits set and the Clock Monitor bit set. The WatchDog and Clock Monitor detector circuits are inhibited during reset. The WatchDog service window bits are initialized to the maximum WatchDog service window of 64k t_C clock cycles. The Clock Monitor bit is initialized high, and will cause a Clock Monitor error following reset if the clock has not reached the minimum specified frequency at the termination of reset. A Clock Monitor error will cause an active low error output on pin G1. This error output will continue until 16–32 t_C clock cycles following the clock frequency reaching the minimum specified value, at which time the G1 output will enter the TRI-STATE mode.

The external RC network shown in *Figure 5* should be used to ensure that the $\overline{\text{RESET}}$ pin is held low until the power supply to the chip stabilizes.



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RC > 5 × Power Supply Rise Time

FIGURE 5. Recommended Reset Circuit

Oscillator Circuits

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (crystal configuration). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_c$).

Figure 6 shows the Crystal and R/C diagrams.

CRYSTAL OSCILLATOR

CKI and CKO can be connected to make a closed loop crystal (or resonator) controlled oscillator.

Table A shows the component values required for various standard crystal values.

R/C OSCILLATOR

By selecting CKI as a single pin oscillator input, a single pin R/C oscillator circuit can be connected to it. CKO is available as a general purpose input, and/or HALT restart pin.

Table B shows the variation in the oscillator frequencies as functions of the component (R and C) values.

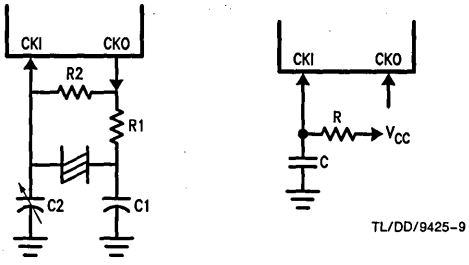

FIGURE 6. Crystal and R/C Oscillator Diagrams

TABLE A. Crystal Oscillator Configuration, $T_A = 25°C$

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)	Conditions
0	1	30	30–36	10	$V_{CC} = 5V$
0	1	30	30–36	4	$V_{CC} = 5V$
0	1	200	100–150	0.455	$V_{CC} = 5V$

TABLE B. R/C Oscillator Configuration, $T_A = 25°C$

R (kΩ)	C (pF)	CKI Freq (MHz)	Instr. Cycle (μs)	Conditions
3.3	82	2.2 to 2.7	3.7 to 4.6	$V_{CC} = 5V$
5.6	100	1.1 to 1.3	7.4 to 9.0	$V_{CC} = 5V$
6.8	100	0.9 to 1.1	8.8 to 10.8	$V_{CC} = 5V$

Note: $3k \leq R \leq 200k$
$50\ pF \leq C \leq 200\ pF$

Current Drain

The total current drain of the chip depends on:

1. Oscillator operation mode—I1
2. Internal switching current—I2
3. Internal leakage current—I3
4. Output source current—I4
5. DC current caused by external input not at V_{CC} or GND—I5
6. DC reference current contribution from the A/D converter—I6
7. Clock Monitor current when enabled—I7

Thus the total current drain, It, is given as

$$It = I1 + I2 + I3 + I4 + I5 + I6 + I7$$

To reduce the total current drain, each of the above components must be minimum.

The chip will draw more current as the CKI input frequency increases up to the maximum 10 MHz value. Operating with a crystal network will draw more current than an external square-wave. Switching current, governed by the equation, can be reduced by lowering voltage and frequency. Leakage current can be reduced by lowering voltage and temperature. The other two items can be reduced by carefully designing the end-user's system.

$$I2 = C \times V \times f$$

where C = equivalent capacitance of the chip
V = operating voltage
f = CKI frequency

Control Registers

CNTRL Register (Address X'00EE)

The Timer1 (T1) and MICROWIRE/PLUS control register contains the following bits:

SL1 & SL0	Select the MICROWIRE/PLUS clock divide by (00 = 2, 01 = 4, 1x = 8)
IEDG	External interrupt edge polarity select (0 = Rising edge, 1 = Falling edge)
MSEL	Selects G5 and G4 as MICROWIRE/PLUS signals SK and SO respectively
T1C0	Timer T1 Start/Stop control in timer modes 1 and 2 Timer T1 Underflow Interrupt Pending Flag in timer mode 3
T1C1	Timer T1 mode control bit
T1C2	Timer T1 mode control bit
T1C3	Timer T1 mode control bit

T1C3	T1C2	T1C1	T1C0	MSEL	IEDG	SL1	SL0

Bit 7 Bit 0

PSW Register (Address X'00EF)

The PSW register contains the following select bits:

GIE	Global interrupt enable (enables interrupts)
EXEN	Enable external interrupt
BUSY	MICROWIRE/PLUS busy shifting flag
EXPND	External interrupt pending
T1ENA	Timer T1 Interrupt Enable for Timer Underflow or T1A Input capture edge
T1PNDA	Timer T1 Interrupt Pending Flag (Autoreload RA in mode 1, T1 Underflow in Mode 2, T1A capture edge in mode 3)
C	Carry Flag
HC	Half Carry Flag

HC	C	T1PNDA	T1ENA	EXPND	BUSY	EXEN	GIE

Bit 7 Bit 0

Control Registers (Continued)

The Half-Carry bit is also affected by all the instructions that affect the Carry flag. The SC (Set Carry) and RC (Reset Carry) instructions will respectively set or clear both the carry flags. In addition to the SC and RC instructions, ADC, SUBC, RRC and RLC instructions affect the carry and Half Carry flags.

ICNTRL Register (Address X'00E8)

The ICNTRL register contains the following bits:

- T1ENB Timer T1 Interrupt Enable for T1B Input capture edge
- T1PNDB Timer T1 Interrupt Pending Flag for T1B capture edge
- μWEN Enable MICROWIRE/PLUS interrupt
- μWPND MICROWIRE/PLUS interrupt pending
- T0EN Timer T0 Interrupt Enable (Bit 12 toggle)
- T0PND Timer T0 Interrupt pending
- LPEN L Port Interrupt Enable (Multi-Input Wakeup/Interrupt)

  Bit 7 could be used as a flag

Unused	LPEN	T0PND	T0EN	μWPND	μWEN	T1PNDB	T1ENB
Bit 7							Bit 0

T2CNTRL Register (Address X'00C6)

The T2CNTRL register contains the following bits:

- T2ENB Timer T2 Interrupt Enable for T2B Input capture edge
- T2PNDB Timer T2 Interrupt Pending Flag for T2B capture edge
- T2ENA Timer T2 Interrupt Enable for Timer Underflow or T2A Input capture edge
- T2PNDA Timer T2 Interrupt Pending Flag (Autoreload RA in mode 1, T2 Underflow in mode 2, T2A capture edge in mode 3)
- T2C0 Timer T2 Start/Stop control in timer modes 1 and 2 Timer T2 Underflow Interrupt Pending Flag in timer mode 3
- T2C1 Timer T2 mode control bit
- T2C2 Timer T2 mode control bit
- T2C3 Timer T2 mode control bit

T2C3	T2C2	T2C1	T2C0	T2PNDA	T2ENA	T2PNDB	T2ENB
Bit 7							Bit 0

Timers

The COP888CF contains a very versatile set of timers (T0, T1, T2). All timers and associated autoreload/capture registers power up containing random data.

Figure 7 shows a block diagram for the timers on the COP888CF.

TIMER T0 (IDLE TIMER)

The COP888CF supports applications that require maintaining real time and low power with the IDLE mode. This IDLE mode support is furnished by the IDLE timer T0, which is a 16-bit timer. The Timer T0 runs continuously at the fixed rate of the instruction cycle clock, t_C. The user cannot read or write to the IDLE Timer T0, which is a count down timer.

The Timer T0 supports the following functions:

- Exit out of the Idle Mode (See Idle Mode description)
- WatchDog logic (See WatchDog description)
- Start up delay out of the HALT mode

The IDLE Timer T0 can generate an interrupt when the thirteenth bit toggles. This toggle is latched into the T0PND pending flag, and will occur every 4 ms at the maximum clock frequency (t_C = 1 μs). A control flag T0EN allows the interrupt from the thirteenth bit of Timer T0 to be enabled or disabled. Setting T0EN will enable the interrupt, while resetting it will disable the interrupt.

TIMER T1 AND TIMER T2

The COP888CF has a set of two powerful timer/counter blocks, T1 and T2. The associated features and functioning of a timer block are described by referring to the timer block Tx. Since the two timer blocks, T1 and T2, are identical, all comments are equally applicable to either timer block.

Each timer block consists of a 16-bit timer, Tx, and two supporting 16-bit autoreload/capture registers, RxA and RxB. Each timer block has two pins associated with it, TxA and TxB. The pin TxA supports I/O required by the timer block, while the pin TxB is an input to the timer block. The powerful and flexible timer block allows the COP888CF to

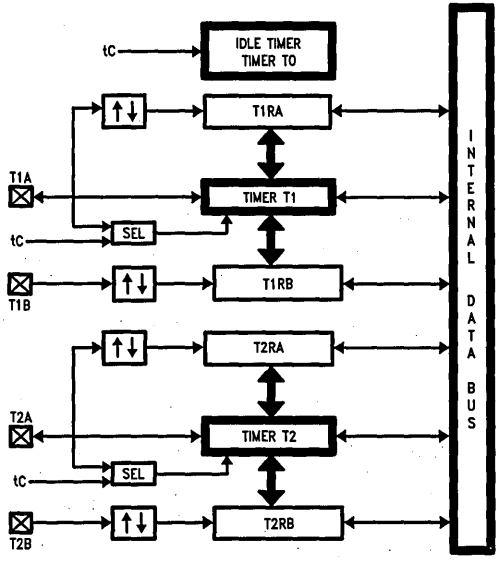

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FIGURE 7. Timers for the COP888CF

easily perform all timer functions with minimal software overhead. The timer block has three operating modes: Processor Independent PWM mode, External Event Counter mode, and Input Capture mode.

The control bits TxC3, TxC2, and TxC1 allow selection of the different modes of operation.

Timers (Continued)

Mode 1. Processor Independent PWM Mode

As the name suggests, this mode allows the COP888CF to generate a PWM signal with very minimal user intervention. The user only has to define the parameters of the PWM signal (ON time and OFF time). Once begun, the timer block will continuously generate the PWM signal completely independent of the microcontroller. The user software services the timer block only when the PWM parameters require updating.

In this mode the timer Tx counts down at a fixed rate of t_C. Upon every underflow the timer is alternately reloaded with the contents of supporting registers, RxA and RxB. The very first underflow of the timer causes the timer to reload from the register RxA. Subsequent underflows cause the timer to be reloaded from the registers alternately beginning with the register RxB.

The Tx Timer control bits, TxC3, TxC2 and TxC1 set up the timer for PWM mode operation.

Figure 8 shows a block diagram of the timer in PWM mode.

The underflows can be programmed to toggle the TxA output pin. The underflows can also be programmed to generate interrupts.

Underflows from the timer are alternately latched into two pending flags, TxPNDA and TxPNDB. The user must reset these pending flags under software control. Two control enable flags, TxENA and TxENB, allow the interrupts from the timer underflow to be enabled or disabled. Setting the timer enable flag TxENA will cause an interrupt when a timer underflow causes the RxA register to be reloaded into the timer. Setting the timer enable flag TxENB will cause an interrupt when a timer underflow causes the RxB register to be reloaded into the timer. Resetting the timer enable flags will disable the associated interrupts.

Either or both of the timer underflow interrupts may be enabled. This gives the user the flexibility of interrupting once per PWM period on either the rising or falling edge of the PWM output. Alternatively, the user may choose to interrupt on both edges of the PWM output.

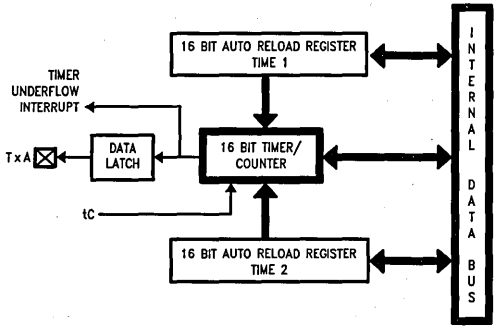

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FIGURE 8. Timer in PWM Mode

Mode 2. External Event Counter Mode

This mode is quite similar to the processor independent PWM mode described above. The main difference is that the timer, Tx, is clocked by the input signal from the TxA pin. The Tx timer control bits, TxC3, TxC2 and TxC1 allow the timer to be clocked either on a positive or negative edge from the TxA pin. Underflows from the timer are latched into the TxPNDA pending flag. Setting the TxENA control flag will cause an interrupt when the timer underflows.

In this mode the input pin TxB can be used as an independent positive edge sensitive interrupt input if the TxENB control flag is set. The occurrence of a positive edge on the TxB input pin is latched into the TxPNDB flag.

Figure 9 shows a block diagram of the timer in External Event Counter mode.

Note: The PWM output is not available in this mode since the TxA pin is being used as the counter input clock.

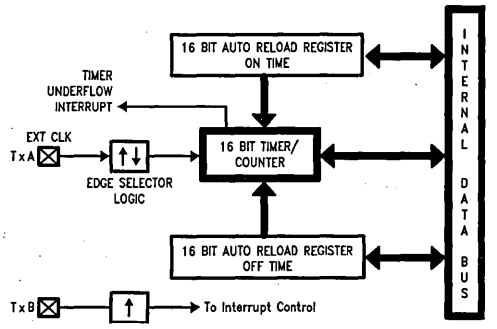

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FIGURE 9. Timer in External Event Counter Mode

Mode 3. Input Capture Mode

The COP888CF can precisely measure external frequencies or time external events by placing the timer block, Tx, in the input capture mode.

In this mode, the timer Tx is constantly running at the fixed t_C rate. The two registers, RxA and RxB, act as capture registers. Each register acts in conjunction with a pin. The register RxA acts in conjunction with the TxA pin and the register RxB acts in conjunction with the TxB pin.

The timer value gets copied over into the register when a trigger event occurs on its corresponding pin. Control bits, TxC3, TxC2 and TxC1, allow the trigger events to be specified either as a positive or a negative edge. The trigger condition for each input pin can be specified independently.

The trigger conditions can also be programmed to generate interrupts. The occurrence of the specified trigger condition on the TxA and TxB pins will be respectively latched into the pending flags, TxPNDA and TxPNDB. The control flag TxENA allows the interrupt on TxA to be either enabled or disabled. Setting the TxENA flag enables interrupts to be generated when the selected trigger condition occurs on the TxA pin. Similarly, the flag TxENB controls the interrupts from the TxB pin.

Underflows from the timer can also be programmed to generate interrupts. Underflows are latched into the timer TxC0 pending flag (the TxC0 control bit serves as the timer underflow interrupt pending flag in the Input Capture mode). Consequently, the TxC0 control bit should be reset when entering the Input Capture mode. The timer underflow interrupt is enabled with the TxENA control flag. When a TxA interrupt occurs in the Input Capture mode, the user must check both

Timers (Continued)

whether a TxA input capture or a timer underflow (or both) caused the interrupt.

Figure 10 shows a block diagram of the timer in Input Capture mode.

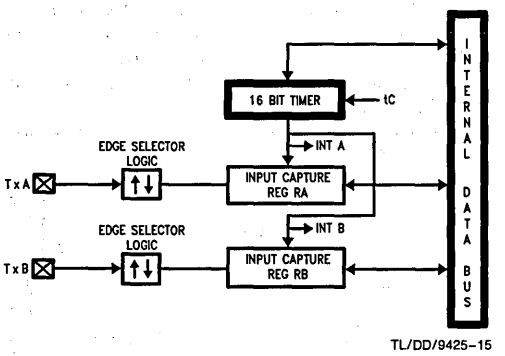

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FIGURE 10. Timer in Input Capture Mode

TIMER CONTROL FLAGS

The timers T1 and T2 have indentical control structures. The control bits and their functions are summarized below.

- TxC0 — Timer Start/Stop control in Modes 1 and 2 (Processor Independent PWM and External Event Counter), where 1 = Start, 0 = Stop
  Timer Underflow Interrupt Pending Flag in Mode 3 (Input Capture)
- TxPNDA — Timer Interrupt Pending Flag
- TxPNDB — Timer Interrupt Pending Flag
- TxENA — Timer Interrupt Enable Flag
- TxENB — Timer Interrupt Enable Flag
  1 = Timer Interrupt Enabled
  0 = Timer Interrupt Disabled
- TxC3 — Timer mode control
- TxC2 — Timer mode control
- TxC1 — Timer mode control

The timer mode control bits (TxC3, TxC2 and TxC1) are detailed below:

TxC3	TxC2	TxC1	Timer Mode	Interrupt A Source	Interrupt B Source	Timer Counts On
0	0	0	MODE 2 (External Event Counter)	Timer Underflow	Pos. TxB Edge	TxA Pos. Edge
0	0	1	MODE 2 (External Event Counter)	Timer Underflow	Pos. TxB Edge	TxA Neg. Edge
1	0	1	MODE 1 (PWM) TxA Toggle	Autoreload RA	Autoreload RB	t_C
1	0	0	MODE 1 (PWM) No TxA Toggle	Autoreload RA	Autoreload RB	t_C
0	1	0	MODE 3 (Capture) Captures: TxA Pos. Edge TxB Pos. Edge	Pos. TxA Edge or Timer Underflow	Pos. TxB Edge	t_C
1	1	0	MODE 3 (Capture) Captures: TxA Pos. Edge TxB Neg. Edge	Pos. TxA Edge or Timer Underflow	Neg. TxB Edge	t_C
0	1	1	MODE 3 (Capture) Captures: TxA Neg. Edge TxB Pos. Edge	Neg. TxB Edge or Timer Underflow	Pos. TxB Edge	t_C
1	1	1	MODE 3 (Capture) Captures: TxA Neg. Edge TxB Neg. Edge	Neg. TxA Edge or Timer Underflow	Neg. TxB Edge	t_C

Power Save Modes

The COP888CF offers the user two power save modes of operation: HALT and IDLE. In the HALT mode, all microcontroller activities are stopped. In the IDLE mode, the on-board oscillator circuitry and timer T0 are active but all other microcontroller activities are stopped. In either mode, all on-board RAM, registers, I/O states, and timers (with the exception of T0) are unaltered.

HALT MODE

The COP888CF is placed in the HALT mode by writing a "1" to the HALT flag (G7 data bit). All microcontroller activities, including the clock, timers, and A/D converter, are stopped. The WatchDog logic on the COP888CF is disabled during the HALT mode. However, the clock monitor circuitry if enabled remains active and will cause the WatchDog output pin (WDOUT) to go low. If the HALT mode is used and the user does not want to activate the WDOUT pin, the Clock Monitor should be disabled after the device comes out of reset (resetting the Clock Monitor control bit with the first write to the WDSVR register). In the HALT mode, the power requirements of the COP888CF are minimal and the applied voltage (V_{CC}) may be decreased to V_r (V_r = 2.0V) without altering the state of the machine.

The COP888CF supports three different ways of exiting the HALT mode. The first method of exiting the HALT mode is with the Multi-Input Wakeup feature on the L port. The second method is with a low to high transition on the CKO (G7) pin. This method precludes the use of the crystal clock configuration (since CKO becomes a dedicated output), and so may be used with an RC clock configuration. The third method of exiting the HALT mode is by pulling the $\overline{\text{RESET}}$ pin low.

Since a crystal or ceramic resonator may be selected as the oscillator, the Wakeup signal is not allowed to start the chip running immediately since crystal oscillators and ceramic resonators have a delayed start up time to reach full amplitude and frequency stability. The IDLE timer is used to generate a fixed delay to ensure that the oscillator has indeed stabilized before allowing instruction execution. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry is enabled. The IDLE timer is loaded with a value of 256 and is clocked with the t_c instruction cycle clock. The t_c clock is derived by dividing the oscillator clock down by a factor of 10. The Schmitt trigger following the CKI inverter on the chip ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

If an RC clock option is being used, the fixed delay is introduced optionally. A control bit, CLKDLY, mapped as configuration bit G7, controls whether the delay is to be introduced or not. The delay is included if CLKDLY is set, and excluded if CLKDLY is reset. The CLKDLY bit is cleared on reset.

The COP888CF has two mask options associated with the HALT mode. The first mask option enables the HALT mode feature, while the second mask option disables the HALT mode. With the HALT mode enable mask option, the COP888CF will enter and exit the HALT mode as described above. With the HALT disable mask option, the COP888CF cannot be placed in the HALT mode (writing a "1" to the HALT flag will have no effect).

The WatchDog detector circuit is inhibited during the HALT mode. However, the clock monitor circuit if enabled remains active during HALT mode in order to ensure a clock monitor error if the COP888CF inadvertently enters the HALT mode as a result of a runaway program or power glitch.

IDLE MODE

The COP888CF is placed in the IDLE mode by writing a "1" to the IDLE flag (G6 data bit). In this mode, all activity, except the associated on-board oscillator circuitry, the WatchDog logic, the clock monitor and the IDLE Timer T0, is stopped. The power supply requirements of the microcontroller in this mode of operation are typically around 30% of normal power requirement of the microcontroller.

As with the HALT mode, the COP888CF can be returned to normal operation with a reset, or with a Multi-Input Wakeup from the L Port. Alternately, the microcontroller resumes normal operation from the IDLE mode when the thirteenth bit (representing 4.096 ms at internal clock frequency of 1 MHz, t_c = 1 μs) of the IDLE Timer toggles.

This toggle condition of the thirteenth bit of the IDLE Timer T0 is latched into the T0PND pending flag.

The user has the option of being interrupted with a transition on the thirteenth bit of the IDLE Timer T0. The interrupt can be enabled or disabled via the T0EN control bit. Setting the T0EN flag enables the interrupt and vice versa.

The user can enter the IDLE mode with the Timer T0 interrupt enabled. In this case, when the T0PND bit gets set, the COP888CF will first execute the Timer T0 interrupt service routine and then return to the instruction following the "Enter Idle Mode" instruction.

Alternatively, the user can enter the IDLE mode with the IDLE Timer T0 interrupt disabled. In this case, the COP888CF will resume normal operation with the instruction immediately following the "Enter IDLE Mode" instruction.

Note: It is necessary to program two NOP instructions following both the set HALT mode and set IDLE mode instructions. These NOP instructions are necessary to allow clock resynchronization following the HALT or IDLE modes.

Multi-Input Wakeup

The Multi-Input Wakeup feature is used to return (wakeup) the COP888CF from either the HALT or IDLE modes. Alternately Multi-Input Wakeup/Interrupt feature may also be used to generate up to 8 edge selectable external interrupts.

Figure 11 shows the Multi-Input Wakeup logic for the COP888CF microcontroller.

The Multi-Input Wakeup feature utilizes the L Port. The user selects which particular L port bit (or combination of L Port bits) will cause the COP888CF to exit the HALT or IDLE modes. The selection is done through the Reg: WKEN. The Reg: WKEN is an 8-bit read/write register, which contains a control bit for every L port bit. Setting a particular WKEN bit enables a Wakeup from the associated L port pin.

The user can select whether the trigger condition on the selected L Port pin is going to be either a positive edge (low to high transition) or a negative edge (high to low transition). This selection is made via the Reg: WKEDG, which is an 8-bit control register with a bit assigned to each L Port pin. Setting the control bit will select the trigger condition to be a negative edge on that particular L Port pin. Resetting the bit selects the trigger condition to be a positive edge. Changing an edge select entails several steps in order to avoid a pseudo Wakeup condition as a result of the edge change. First, the associated WKEN bit should be reset, followed by the edge select change in WKEDG. Next, the associated WKPND bit should be cleared, followed by the associated WKEN bit being re-enabled.

An example may serve to clarify this procedure. Suppose we wish to change the edge select from positive (low going high) to negative (high going low) for L Port bit 5, where bit 5 has previously been enabled for an input interrupt. The program would be as follows:

```
RBIT  5, WKEN
SBIT  5, WKEDG
RBIT  5, WKPND
SBIT  5, WKEN
```

If the L port bits have been used as outputs and then changed to inputs with Multi-Input Wakeup/Interrupt, a safety procedure should also be followed to avoid inherited pseudo wakeup conditions. After the selected L port bits have been changed from output to input but before the associated WKEN bits are enabled, the associated edge select bits in WKEDG should be set or reset for the desired edge selects, followed by the associated WKPND bits being cleared.

This same procedure should be used following reset, since the L port inputs are left floating as a result of reset.

The occurrence of the selected trigger condition for Multi-Input Wakeup is latched into a pending register called WKPND. The respective bits of the WKPND register will be set on the occurrence of the selected trigger edge on the corresponding Port L pin. The user has the responsibility of clearing these pending flags. Since WKPND is a pending register for the occurrence of selected wakeup conditions, the COP888CF will not enter the HALT mode if any Wakeup bit is both enabled and pending. Consequently, the user has the responsibility of clearing the pending flags before attempting to enter the HALT mode.

The WKEN, WKPND and WKEDG are all read/write registers, and are cleared at reset.

PORT L INTERRUPTS

Port L provides the user with an additional eight fully selectable, edge sensitive interrupts which are all vectored into the same service subroutine.

The interrupt from Port L shares logic with the wake up circuitry. The register WKEN allows interrupts from Port L to be individually enabled or disabled. The register WKEDG specifies the trigger condition to be either a positive or a negative edge. Finally, the register WKPND latches in the pending trigger conditions.

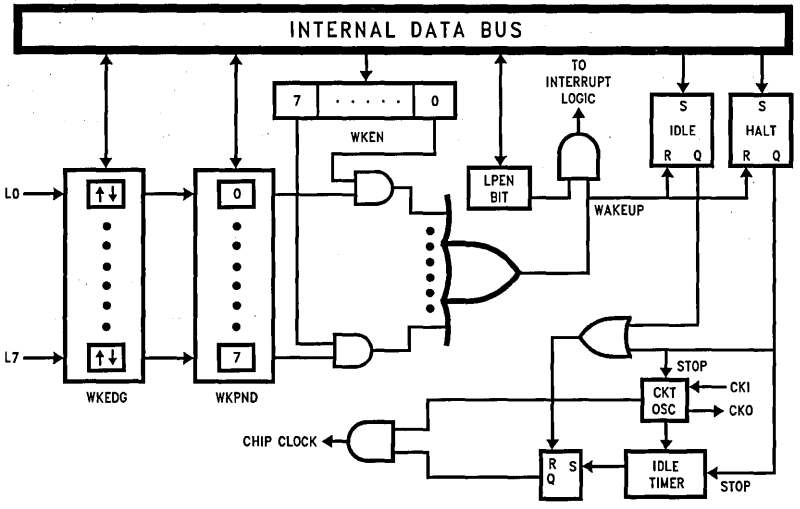

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FIGURE 11. Multi-Input Wake Up Logic

Multi-Input Wakeup (Continued)

The GIE (global interrupt enable) bit enables the interrupt function. A control flag, LPEN, functions as a global interrupt enable for Port L interrupts. Setting the LPEN flag will enable interrupts and vice versa. A separate global pending flag is not needed since the register WKPND is adequate.

Since Port L is also used for waking the COP888CF out of the HALT or IDLE modes, the user can elect to exit the HALT or IDLE modes either with or without the interrupt enabled. If he elects to disable the interrupt, then the COP888CF will restart execution from the instruction immediately following the instruction that placed the microcontroller in the HALT or IDLE modes. In the other case, the COP888CF will first execute the interrupt service routine and then revert to normal operation.

The Wakeup signal will not start the chip running immediately since crystal oscillators or ceramic resonators have a finite start up time. The IDLE Timer (T0) generates a fixed delay to ensure that the oscillator has indeed stabilized before allowing the COP888CF to execute instructions. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry and the IDLE Timer T0 are enabled. The IDLE Timer is loaded with a value of 256 and is clocked from the t_c instruction cycle clock. The t_c clock is derived by dividing down the oscillator clock by a factor of 10. A Schmitt trigger following the CKI on-chip inverter ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

If the RC clock option is used, the fixed delay is under software control. A control flag, CLKDLY, in the G7 configuration bit allows the clock start up delay to be optionally inserted. Setting CLKDLY flag high will cause clock start up delay to be inserted and resetting it will exclude the clock start up delay. The CLKDLY flag is cleared during reset, so the clock start up delay is not present following reset with the RC clock options.

A/D Converter

The COP888CF contains an 8-channel, multiplexed input, successive approximation, A/D converter. Two dedicated pins, V_{REF} and AGND are provided for voltage reference.

OPERATING MODES

The A/D converter supports ratiometric measurements. It supports both Single Ended and Differential modes of operation.

Four specific analog channel selection modes are supported. These are as follows:

Allow any specific channel to be selected at one time. The A/D converter performs the specific conversion requested and stops.

Allow any specific channel to be scanned continuously. In other words, the user will specify the channel and the A/D converter will keep on scanning it continuously. The user can come in at any arbitrary time and immediately read the result of the last conversion. The user does not have to wait for the current conversion to be completed.

Allow any differential channel pair to be selected at one time. The A/D converter performs the specific differential conversion requested and stops.

Allow any differential channel pair to be scanned continuously. In other words, the user will specify the differential channel pair and the A/D converter will keep on scanning it continuously. The user can come in at any arbitrary time and immediately read the result of the last differential conversion. The user does not have to wait for the current conversion to be completed.

The A/D converter is supported by two memory mapped registers, the result register and the mode control register. When the COP888CF is reset, the control register is cleared and the A/D is powered down. The A/D result register has unknown data following reset.

A/D Control Register

A control register, Reg: ENAD, contains 3 bits for channel selection, 3 bits for prescaler selection, and 2 bits for mode selection. An A/D conversion is initiated by writing to the ENAD control register. The result of the conversion is available to the user from the A/D result register, Reg: ADRSLT.

Reg: ENAD

CHANNEL SELECT	MODE SELECT	PRESCALER SELECT
Bits 7, 6, 5	Bits 4,3	Bits 2, 1, 0

CHANNEL SELECT

This 3-bit field selects one of eight channels to be the $V_{IN}+$. The mode selection determines the $V_{IN}-$ input.

Single Ended mode:

Bit 7	Bit 6	Bit 5	Channel No.
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Differential mode:

Bit 7	Bit 6	Bit 5	Channel Pairs (+. −)
0	0	0	0, 1
0	0	1	1, 0
0	1	0	2, 3
0	1	1	3, 2
1	0	0	4, 5
1	0	1	5, 4
1	1	0	6, 7
1	1	1	7, 6

MODE SELECT

This 2-bit field is used to select the mode of operation (single conversion, continuous conversions, differential, single ended) as shown in the following table.

Bit 4	Bit 3	Mode
0	0	Single Ended mode, single conversion
0	1	Single Ended mode, continuous scan of a single channel into the result register
1	0	Differential mode, single conversion
1	1	Differential mode, continuous scan of a channel pair into the result register

A/D Converter (Continued)

PRESCALER SELECT

This 3-bit field is used to select one of the seven prescaler clocks for the A/D converter. The prescaler also allows the A/D clock inhibit power saving mode to be selected. The following table shows the various prescaler options.

Bit 2	Bit 1	Bit 0	Clock Select
0	0	0	Inhibit A/D clock
0	0	1	Divide by 1
0	1	0	Divide by 2
0	1	1	Divide by 4
1	0	0	Divide by 6
1	0	1	Divide by 12
1	1	0	Divide by 8
1	1	1	Divide by 16

ADC Operation

The A/D converter interface works as follows. Writing to the A/D control register ENAD initiates an A/D conversion unless the prescaler value is set to 0, in which case the ADC clock is stopped and the ADC is powered down. The conversion sequence starts at the beginning of the write to ENAD operation powering up the ADC. At the first falling edge of the converter clock following the write operation (not counting the falling edge if it occurs at the same time as the write operation ends), the sample signal turns on for two clock cycles. The ADC is selected in the middle of the sample period. If the ADC is in single conversion mode, the conversion complete signal from the ADC will generate a power down for the A/D converter. If the ADC is in continuous mode, the conversion complete signal will restart the conversion sequence by deselecting the ADC for one converter clock cycle before starting the next sample. The ADC 8-bit result is loaded into the A/D result register (ADRSLT) except during LOAD clock high, which prevents transient data (resulting from the ADC writing a new result over an old one) being read from ADRSLT.

PRESCALER

The COP888CF A/D Converter (ADC) contains a prescaler option which allows seven different clock selections. The A/D clock frequency is equal to CKI divided by the prescaler value. Note that the prescaler value must be chosen such that the A/D clock falls within the specified range. The maximum A/D frequency is 1.67 MHz. This equates to a 600 ns ADC clock cycle.

The A/D converter takes 12 ADC clock cycles to complete a conversion. Thus the minimum ADC conversion time for the COP888CF is 7.2 μs when a prescaler of 6 has been selected. These 12 ADC clock cycles necessary for a conversion consist of 1 cycle at the beginning for reset, 2 cycles for sampling, 8 cycles for converting, and 1 cycle for loading the result into the COP888CF A/D result register (ADRSLT). This A/D result register is a read-only register. The COP888CF cannot write into ADRSLT.

The prescaler also allows an A/D clock inhibit option, which saves power by powering down the A/D when it is not in use.

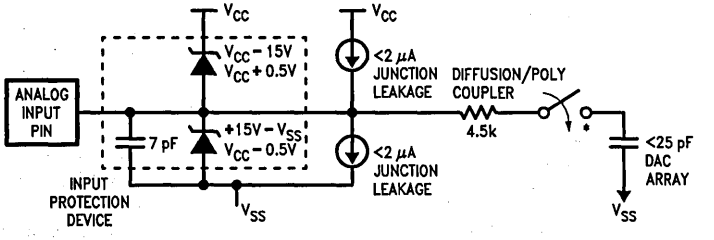
Note: The A/D converter is also powered down when the COP888CF is in either the HALT or IDLE modes. If the ADC is running when the COP888CF enters the HALT or IDLE modes, the ADC will power down during the HALT or IDLE, and then will reinitialize the conversion when the COP888CF comes out of the HALT or IDLE modes.

Analog Input and Source Resistance Considerations

Figure 12 shows the A/D pin model for the COP888CF in single ended mode. The differential mode has similiar A/D pin model. The leads to the analog inputs should be kept as short as possible. Both noise and digital clock coupling to an A/D input can cause conversion errors. The clock lead should be kept away from the analog input line to reduce coupling. The A/D channel input pins do not have any internal output driver circuitry connected to them because this circuitry would load the analog input signals due to output buffer leakage current.

Source impedances greater than 1 kΩ on the analog input lines will adversely affect internal RC charging time during input sampling. As shown in *Figure 12*, the analog switch to the DAC array is closed only during the 2 A/D cycle sample time. Large source impedances on the analog inputs may result in the DAC array not being charged to the correct voltage levels, causing scale errors.

If large source resistance is necessary, the recommended solution is to slow down the A/D clock speed in proportion to the source resistance. The A/D converter may be operated at the maximum speed for R_S less than 1 kΩ. For R_S greater than 1 kΩ, A/D clock speed needs to be reduced. For example, with R_S = 2 kΩ, the A/D converter may be operated at half the maximum speed. A/D converter clock speed may be slowed down by either increasing the A/D prescaler divide-by or decreasing the CKI clock frequency. The A/D clock speed may be reduced to its minimum frequency of 100 kHz.



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*The analog switch is closed only during the sample time.

FIGURE 12. A/D Pin Model (Single Ended Mode)

Interrupts

The COP888CF supports a vectored interrupt scheme. It supports a total of ten interrupt sources. The following table lists all the possible COP888CF interrupt sources, their arbitration ranking and the memory locations reserved for the interrupt vector for each source.

Two bytes of program memory space are reserved for each interrupt source. All interrupt sources except the software interrupt are maskable. Each of the maskable interrupts have an Enable bit and a Pending bit. A maskable interrupt is active if its associated enable and pending bits are set. If GIE = 1 and an interrupt is active, then the processor will be interrupted as soon as it is ready to start executing an instruction except if the above conditions happen during the Software Trap service routine. This exception is described in the Software Trap sub-section.

The interruption process is accomplished with the INTR instruction (opcode 00), which is jammed inside the Instruction Register and replaces the opcode about to be executed. The following steps are performed for every interrupt:

1. The GIE (Global Interrupt Enable) bit is reset.
2. The address of the instruction about to be executed is pushed into the stack.
3. The PC (Program Counter) branches to address 00FF. This procedure takes 7 t_c cycles to execute.

At this time, since GIE = 0, other maskable interrupts are disabled. The user is now free to do whatever context switching is required by saving the context of the machine in the stack with PUSH instructions. The user would then program a VIS (Vector Interrupt Select) instruction in order to branch to the interrupt service routine of the highest priority interrupt enabled and pending at the time of the VIS. Note that this is not necessarily the interrupt that caused the branch to address location 00FF Hex prior to the context switching.

Thus, if an interrupt with a higher rank than the one which caused the interruption becomes active before the decision of which interrupt to service is made by the VIS, then the interrupt with the higher rank will override any lower ones and will be acknowledged. The lower priority interrupt(s) are still pending, however, and will cause another interrupt immediately following the completion of the interrupt service routine associated with the higher priority interrupt just serviced. This lower priority interrupt will occur immediately following the RETI (Return from Interrupt) instruction at the end of the interrupt service routine just completed.

Inside the interrupt service routine, the associated pending bit has to be cleared by software. The RETI (Return from Interrupt) instruction at the end of the interrupt service routine will set the GIE (Global Interrupt Enable) bit, allowing the processor to be interrupted again if another interrupt is active and pending.

The VIS instruction looks at all the active interrupts at the time it is executed and performs an indirect jump to the beginning of the service routine of the one with the highest rank.

The addresses of the different interrupt service routines, called vectors, are chosen by the user and stored in ROM in a table starting at 01E0 (assuming that VIS is located between 00FF and 01DF). The vectors are 15-bit wide and therefore occupy 2 ROM locations.

VIS and the vector table must be located in the same 256-byte block (0y00 to 0yFF) except if VIS is located at the last address of a block. In this case, the table must be in the next block. The vector table cannot be inserted in the first 256-byte block.

The vector of the maskable interrupt with the lowest rank is located at 0yE0 (Hi-Order byte) and 0yE1 (Lo-Order byte) and so forth in increasing rank number. The vector of the

Arbitration Ranking	Source	Description	Vector Address Hi-Low Byte
(1) Highest	Software	INTR Instruction	0yFE–0yFF
	Reserved	for Future Use	0yFC–0yFD
(2)	External	Pin G0 Edge	0yFA–0yFB
(3)	Timer T0	Underflow	0yF8–0yF9
(4)	Timer T1	T1A/Underflow	0yF6–0yF7
(5)	Timer T1	T1B	0yF4–0yF5
(6)	MICROWIRE/PLUS	BUSY Goes Low	0yF2–0yF3
	Reserved	for Future Use	0yF0–0yF1
	Reserved	for UART	0yEE–0yEF
	Reserved	for UART	0yEC–0yED
(7)	Timer T2	T2A/Underflow	0yEA–0yEB
(8)	Timer T2	T2B	0yE8–0yE9
	Reserved	for Future Use	0yE6–0yE7
	Reserved	for Future Use	0yE4–0yE5
(9)	Port L/Wakeup	Port L Edge	0yE2–0yE3
(10) Lowest	Default	VIS Instr. Execution without Any Interrupts	0yE0–0yE1

y is VIS page, y ≠ 0

Interrupts (Continued)

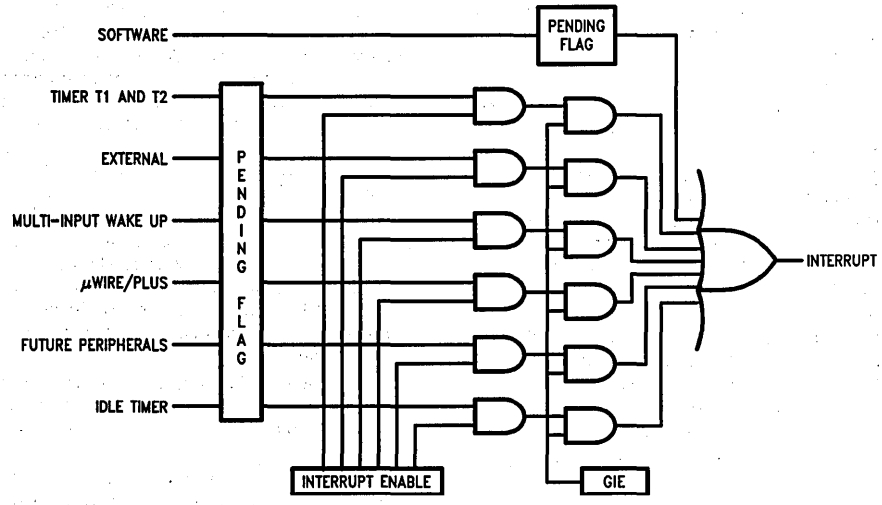

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FIGURE 13. COP888CF Interrupt Block Diagram

maskable interrupt with the highest rank is located at 0yFA (Hi-Order byte) and 0yFB (Lo-Order byte).

The Software Trap has the highest rank and its vector is located at 0yFE and 0yFF.

If, by accident, a VIS gets executed and no interrupt is active, then the PC (Program Counter) will branch to a vector located at 0yE0–0yE1. This vector can point to the Software Trap (ST) interrupt service routine, or to another special service routine as desired.

Figure 13 shows the COP888CF Interrupt block diagram.

SOFTWARE TRAP

The Software Trap (ST) is a special kind of non-maskable interrupt which occurs when the INTR instruction (used to acknowledge interrupts) is fetched from ROM and placed inside the instruction register. This may happen when the PC is pointing beyond the available ROM address space or when the stack is over-popped.

When an ST occurs, the user can re-initialize the stack pointer and do a recovery procedure (similar to RESET, but not necessarily containing all of the same initialization procedures) before restarting.

The occurrence of an ST is latched into the ST pending bit. The GIE bit is not affected and the ST pending bit **(not accessible by the user)** is used to inhibit other interrupts and to direct the program to the ST service routine with the VIS instruction. The RPND instruction is used to clear the software interrupt pending bit. This bit is also cleared on reset.

The ST has the highest rank among all interrupts.

Nothing (except another ST) can interrupt an ST being serviced.

WATCHDOG

The COP888CF contains a WATCHDOG and clock monitor. The WATCHDOG is designed to detect the user program getting stuck in infinite loops resulting in loss of program control or "runaway" programs. The Clock Monitor is used to detect the absence of a clock or a very slow clock below a specified rate on the CKI pin.

The WATCHDOG consists of two independent logic blocks: WD UPPER and WD LOWER. WD UPPER establishes the upper limit on the service window and WD LOWER defines the lower limit of the service window.

Servicing the WATCHDOG consists of writing a specific value to a WATCHDOG Service Register named WDSVR which is memory mapped in the RAM. This value is composed of three fields, consisting of a 2-bit Window Select, a 5-bit Key Data field, and the 1-bit Clock Monitor Select field. Table I shows the WDSVR register.

The lower limit of the service window is fixed at 2048 instruction cycles. Bits 7 and 6 of the WDSVR register allow the user to pick an upper limit of the service window.

Table II shows the four possible combinations of lower and upper limits for the WATCHDOG service window. This flexibility in choosing the WATCHDOG service window prevents any undue burden on the user software.

Bits 5, 4, 3, 2 and 1 of the WDSVR register represent the 5-bit Key Data field. The key data is fixed at 01100. Bit 0 of the WDSVR Register is the Clock Monitor Select bit.

TABLE I. WATCHDOG Service Register

Window Select		Key Data					Clock Monitor
X	X	0	1	1	0	0	Y
7	6	5	4	3	2	1	0

TABLE II. WATCHDOG Service Window Select

WDSVR Bit 7	WDSVR Bit 6	Service Window (Lower-Upper Limits)
0	0	2k-8k t_C Cycles
0	1	2k-16k t_C Cycles
1	0	2k-32k t_C Cycles
1	1	2k-64k t_C Cycles

Clock Monitor

The Clock Monitor aboard the COP888CF can be selected or deselected under program control. The Clock Monitor is guaranteed not to reject the clock if the instruction cycle clock ($1/t_c$) is greater or equal to 10 kHz. This equates to a clock input rate on CKI of greater or equal to 100 kHz.

WATCHDOG Operation

The WATCHDOG and Clock Monitor are disabled during reset. The COP888CF comes out of reset with the WATCHDOG armed, the WATCHDOG Window Select (bits 6, 7 of the WDSVR Register) set, and the Clock Monitor bit (bit 0 of the WDSVR Register) enabled. Thus, a Clock Monitor error will occur after coming out of reset, if the instruction cycle clock frequency has not reached a minimum specified value, including the case where the oscillator fails to start.

The WDSVR register can be written to only once after reset and the key data (bits 5 through 1 of the WDSVR Register) must match to be a valid write. This write to the WDSVR register involves two irrevocable choices: (i) the selection of the WATCHDOG service window (ii) enabling or disabling of the Clock Monitor. Hence, the first write to WDSVR Register involves selecting or deselecting the Clock Monitor, select the WATCHDOG service window and match the WATCHDOG key data. Subsequent writes to the WDSVR register will compare the value being written by the user to the WATCHDOG service window value and the key data (bits 7 through 1) in the WDSVR Register. Table III shows the sequence of events that can occur.

The user must service the WATCHDOG at least once before the upper limit of the service window expires. The WATCHDOG may not be serviced more than once in every lower limit of the service window. The user may service the WATCHDOG as many times as wished in the time period between the lower and upper limits of the service window. The first write to the WDSVR Register is also counted as a WATCHDOG service.

The WATCHDOG has an output pin associated with it. This is the WDOUT pin, on pin 1 of the port G. WDOUT is active low. The WDOUT pin is in the high impedance state in the inactive state. Upon triggering the WATCHDOG, the logic will pull the WDOUT (G1) pin low for an additional $16\ t_c$–$32\ t_c$ cycles after the signal level on WDOUT pin goes below the lower Schmitt trigger threshold. After this delay, the COP888CF will stop forcing the WDOUT output low.

The WATCHDOG service window will restart when the WDOUT pin goes high. It is recommended that the user tie the WDOUT pin back to V_{CC} through a resistor in order to pull WDOUT high.

A WATCHDOG service while the WDOUT signal is active will be ignored. The state of the WDOUT pin is not guaranteed on reset, but if it powers up low then the WATCHDOG will time out and WDOUT will enter high impedance state.

The Clock Monitor forces the G1 pin low upon detecting a clock frequency error. The Clock Monitor error will continue until the clock frequency has reached the minimum specified value, after which the G1 output will enter the high impedance TRI-STATE mode following $16\ t_c$–$32\ t_c$ clock cycles. The Clock Monitor generates a continual Clock Monitor error if the oscillator fails to start, or fails to reach the minimum specified frequency. The specification for the Clock Monitor is as follows:

$1/t_c > 10$ kHz—No clock rejection.

$1/t_c < 10$ Hz—Guaranteed clock rejection.

WATCHDOG AND CLOCK MONITOR SUMMARY

The following salient points regarding the COP888 WATCHDOG and CLOCK MONITOR should be noted:

- Both the WATCHDOG and Clock Monitor detector circuits are inhibited during RESET.
- Following RESET, the WATCHDOG and CLOCK MONITOR are both enabled, with the WATCHDOG having the maximum service window selected.
- The WATCHDOG service window and Clock Monitor enable/disable option can only be changed once, during the initial WATCHDOG service following RESET.
- The initial WATCHDOG service must match the key data value in the WATCHDOG Service register WDSVR in order to avoid a WATCHDOG error.
- Subsequent WATCHDOG services must match all three data fields in WDSVR in order to avoid WATCHDOG errors.
- The correct key data value cannot be read from the WATCHDOG Service register WDSVR. Any attempt to read this key data value of 01100 from WDSVR will read as key data value of all 0's.
- The WATCHDOG detector circuit is inhibited during both the HALT and IDLE modes.
- The Clock Monitor detector circuit is active during both the HALT and IDLE modes. Consequently, the COP888 inadvertently entering the HALT mode will be detected as a Clock Monitor error (provided that the Clock Monitor enable option has been selected by the program).
- With the single-pin R/C oscillator mask option selected and the CLKDLY bit reset, the WATCHDOG service window will resume following HALT mode from where it left off before entering the HALT mode.

TABLE III. WATCHDOG Service Actions

Key Data	Window Data	Clock Monitor	Action
Match	Match	Match	Valid Service: Restart Service Window
Don't Care	Mismatch	Don't Care	Error: Generate WATCHDOG Output
Mismatch	Don't Care	Don't Care	Error: Generate WATCHDOG Output
Don't Care	Don't Care	Mismatch	Error: Generate WATCHDOG Output

WATCHDOG Operation (Continued)

- With the crystal oscillator mask option selected, or with the single-pin R/C oscillator mask option selected and the CLKDLY bit set, the WATCHDOG service window will be set to its selected value from WDSVR following HALT. Consequently, the WATCHDOG should not be serviced for at least 2048 instruction cycles following HALT, but must be serviced within the selected window to avoid a WATCHDOG error.
- The IDLE timer T0 is not initialized with RESET.
- The user can sync in to the IDLE counter cycle with an IDLE counter (T0) interrupt or by monitoring the T0PND flag. The T0PND flag is set whenever the thirteenth bit of the IDLE counter toggles (every 4096 instruction cycles). The user is responsible for resetting the T0PND flag.
- A hardware WATCHDOG service occurs just as the COP888 exits the IDLE mode. Consequently, the WATCHDOG should not be serviced for at least 2048 instruction cycles following IDLE, but must be serviced within the selected window to avoid a WATCHDOG error.
- Following RESET, the initial WATCHDOG service (where the service window and the CLOCK MONITOR enable/disable must be selected) may be programmed anywhere within the maximum service window (65,536 instruction cycles) initialized by RESET. Note that this initial WATCHDOG service may be programmed within the initial 2048 instruction cycles without causing a WATCHDOG error.

Detection of Illegal Conditions

The COP888CF can detect various illegal conditions resulting from coding errors, transient noise, power supply voltage drops, runaway programs, etc.

Reading of undefined ROM gets zeros. The opcode for software interrupt is zero. If the program fetches instructions from undefined ROM, this will force a software interrupt, thus signaling that an illegal condition has occurred.

The subroutine stack grows down for each call (jump to subroutine), interrupt, or PUSH, and grows up for each return or POP. The stack pointer is initialized to RAM location 06F Hex during reset. Consequently, if there are more returns than calls, the stack pointer will point to addresses 070 and 071 Hex (which are undefined RAM). Undefined RAM from addresses 070 to 07F Hex is read as all 1's, which in turn will cause the program to return to address 7FFF Hex. This is an undefined ROM location and the instruction fetched (all 0's) from this location will generate a software interrupt signaling an illegal condition.

Thus, the chip can detect the following illegal conditions:

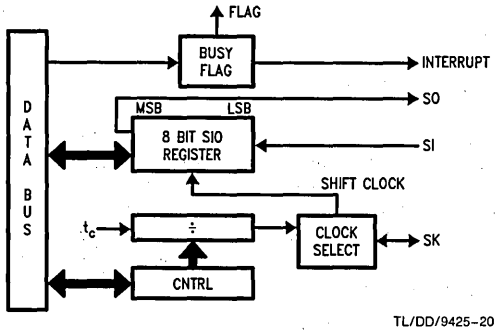
a. Executing from undefined ROM

b. Over "POP"ing the stack by having more returns than calls.

When the software interrupt occurs, the user can re-initialize the stack pointer and do a recovery procedure before restarting (this recovery program is probably similar to that following reset, but might not contain the same program initialization procedures).

MICROWIRE/PLUS

MICROWIRE/PLUS is a serial synchronous communications interface. The MICROWIRE/PLUS capability enables the COP888CF to interface with any of National Semiconductor's MICROWIRE peripherals (i.e. A/D converters, display drivers, E²PROMs etc.) and with other microcontrollers which support the MICROWIRE interface. It consists of an 8-bit serial shift register (SIO) with serial data input (SI), serial data output (SO) and serial shift clock (SK). *Figure 14* shows a block diagram of the MICROWIRE/PLUS logic.



TL/DD/9425–20

FIGURE 14. MICROWIRE/PLUS Block Diagram

The shift clock can be selected from either an internal source or an external source. Operating the MICROWIRE/PLUS arrangement with the internal clock source is called the Master mode of operation. Similarly, operating the MICROWIRE/PLUS arrangement with an external shift clock is called the Slave mode of operation.

The CNTRL register is used to configure and control the MICROWIRE/PLUS mode. To use the MICROWIRE/PLUS, the MSEL bit in the CNTRL register is set to one. In the master mode the SK clock rate is selected by the two bits, SL0 and SL1, in the CNTRL register. TABLE IV details the different clock rates that may be selected.

TABLE IV. MICROWIRE/PLUS Master Mode Clock Selection

SL1	SL0	SK
0	0	$2 \times t_c$
0	1	$4 \times t_c$
1	x	$8 \times t_c$

Where t_c is the instruction cycle clock

MICROWIRE/PLUS OPERATION

Setting the BUSY bit in the PSW register causes the MICROWIRE/PLUS to start shifting the data. It gets reset when eight data bits have been shifted. The user may reset the BUSY bit by software to allow less than 8 bits to shift. If enabled, an interrupt is generated when eight data bits have been shifted. The COP888CF may enter the MICROWIRE/PLUS mode either as a Master or as a Slave. *Figure 15* shows how two COP888CF microcontrollers and several peripherals may be interconnected using the MICROWIRE/PLUS arrangements.

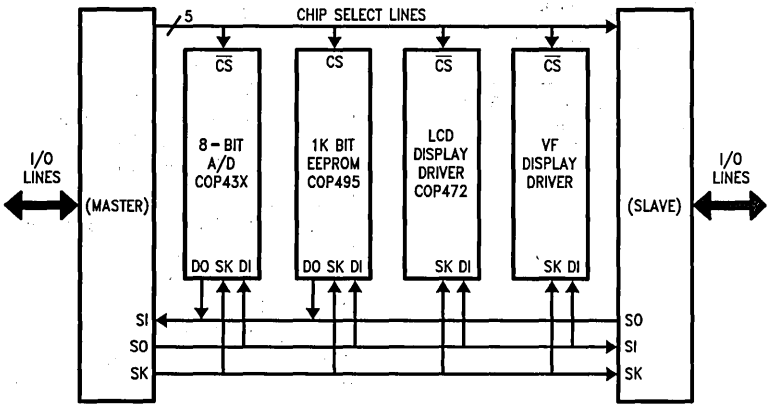
Warning:

The SIO register should only be loaded when the SK clock is low. Loading the SIO register while the SK clock is high will result in undefined data in the SIO register. SK clock is normally low when not shifting.

Setting the BUSY flag when the input SK clock is high in the MICROWIRE/PLUS slave mode may cause the current SK clock forthe SIO shift register to be narrow. For safety, the BUSY flag should only be set when the input SK clock is low.

MICROWIRE/PLUS Master Mode Operation

In the MICROWIRE/PLUS Master mode of operation the shift clock (SK) is generated internally by the COP888CF. The MICROWIRE Master always initiates all data exchanges. The MSEL bit in the CNTRL register must be set to enable the SO and SK functions onto the G Port. The SO and SK pins must also be selected as outputs by setting appropriate bits in the Port G configuration register. Table V summarizes the bit settings required for Master mode of operation.



TL/DD/9425–21

FIGURE 15. MICROWIRE/PLUS Application

MICROWIRE/PLUS (Continued)

MICROWIRE/PLUS Slave Mode Operation

In the MICROWIRE/PLUS Slave mode of operation the SK clock is generated by an external source. Setting the MSEL bit in the CNTRL register enables the SO and SK functions onto the G Port. The SK pin must be selected as an input and the SO pin is selected as an output pin by setting and resetting the appropriate bit in the Port G configuration register. Table V summarizes the settings required to enter the Slave mode of operation.

The user must set the BUSY flag immediately upon entering the Slave mode. This will ensure that all data bits sent by the Master will be shifted properly. After eight clock pulses the BUSY flag will be cleared and the sequence may be repeated.

Alternate SK Phase Operation

The COP888CF allows either the normal SK clock or an alternate phase SK clock to shift data in and out of the SIO register. In both the modes the SK is normally low. In the normal mode data is shifted in on the rising edge of the SK clock and the data is shifted out on the falling edge of the SK clock. The SIO register is shifted on each falling edge of the SK clock in the normal mode. In the alternate SK phase mode the SIO register is shifted on the rising edge of the SK clock.

A control flag, SKSEL, allows either the normal SK clock or the alternate SK clock to be selected. Resetting SKSEL causes the MICROWIRE/PLUS logic to be clocked from the normal SK signal. Setting the SKSEL flag selects the alternate SK clock. The SKSEL is mapped into the G6 configuration bit. The SKSEL flag will power up in the reset condition, selecting the normal SK signal.

TABLE V

This table assumes that the control flag MSEL is set.

G4 (SO) Config. Bit	G5 (SK) Config. Bit	G4 Fun.	G5 Fun.	Operation
1	1	SO	Int. SK	MICROWIRE/PLUS Master
0	1	TRI-STATE	Int. SK	MICROWIRE/PLUS Master
1	0	SO	Ext. SK	MICROWIRE/PLUS Slave
0	0	TRI-STATE	Ext. SK	MICROWIRE/PLUS Slave

Memory Map

All RAM, ports and registers (except A and PC) are mapped into data memory address space

Address	Contents
00 to 6F	On-Chip RAM bytes
70 to BF	Unused RAM Address Space
C0	Timer T2 Lower Byte
C1	Timer T2 Upper Byte
C2	Timer T2 Autoload Register T2RA Lower Byte
C3	Timer T2 Autoload Register T2RA Upper Byte
C4	Timer T2 Autoload Register T2RB Lower Byte
C5	Timer T2 Autoload Register T2RB Upper Byte
C6	Timer T2 Control Register
C7	WATCHDOG Service Register (Reg:WDSVR)
C8	MIWU Edge Select Register (Reg:WKEDG)
C9	MIWU Enable Register (Reg:WKEN)
CA	MIWU Pending Register (Reg:WKPND)
CB	A/D Converter Control Register (Reg:ENAD)
CC	A/D Converter Result Register (Reg: ADRSLT)
CD to CF	Reserved
D0	Port L Data Register
D1	Port L Configuration Register
D2	Port L Input Pins (Read Only)
D3	Reserved for Port L
D4	Port G Data Register
D5	Port G Configuration Register
D6	Port G Input Pins (Read Only)
D7	Port I Input Pins (Read Only)
D8	Port C Data Register
D9	Port C Configuration Register
DA	Port C Input Pins (Read Only)
DB	Reserved for Port C
DC	Port D Data Register
DD to DF	Reserved for Port D
E0 to E5	Reserved
E6	Timer T1 Autoload Register T1RB Lower Byte
E7	Timer T1 Autoload Register T1RB Upper Byte
E8	ICNTRL Register
E9	MICROWIRE Shift Register
EA	Timer T1 Lower Byte
EB	Timer T1 Upper Byte
EC	Timer T1 Autoload Register T1RA Lower Byte
ED	Timer T1 Autoload Register T1RA Upper Byte
EE	CNTRL Control Register
EF	PSW Register
F0 to FB	On-Chip RAM Mapped as Registers
FC	X Register
FD	SP Register
FE	B Register
FF	Reserved

Reading memory locations 70-7F Hex will return all ones. Reading other unused memory locations will return undefined data.

Addressing Modes

The COP888CF has ten addressing modes, six for operand addressing and four for transfer of control.

OPERAND ADDRESSING MODES

Register Indirect

This is the "normal" addressing mode for the COP888CF. The operand is the data memory addressed by the B pointer or X pointer.

Register Indirect (with auto post increment or decrement of pointer)

This addressing mode is used with the LD and X instructions. The operand is the data memory addressed by the B pointer or X pointer. This is a register indirect mode that automatically post increments or decrements the B or X register after executing the instruction.

Direct

The instruction contains an 8-bit address field that directly points to the data memory for the operand.

Immediate

The instruction contains an 8-bit immediate field as the operand.

Short Immediate

This addressing mode is used with the Load B Immediate instruction. The instruction contains a 4-bit immediate field as the operand.

Indirect

This addressing mode is used with the LAID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a data operand from the program memory.

TRANSFER OF CONTROL ADDRESSING MODES

Relative

This mode is used for the JP instruction, with the instruction field being added to the program counter to get the new program location. JP has a range from −31 to +32 to allow a 1-byte relative jump (JP + 1 is implemented by a NOP instruction). There are no "pages" when using JP, since all 15 bits of PC are used.

Absolute

This mode is used with the JMP and JSR instructions, with the instruction field of 12 bits replacing the lower 12 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory segment.

Absolute Long

This mode is used with the JMPL and JSRL instructions, with the instruction field of 15 bits replacing the entire 15 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory space.

Indirect

This mode is used with the JID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a location in the program memory. The contents of this program memory location serve as a partial address (lower 8 bits of PC) for the jump to the next instruction.

Note: The VIS is a special case of the Indirect Transfer of Control addressing mode, where the double byte vector associated with the interrupt is transferred from adjacent addresses in the program memory into the program counter (PC) in order to jump to the associated interrupt service routine.

Instruction Set

Register and Symbol Definition

Registers	
A	8-Bit Accumulator Register
B	8-Bit Address Register
X	8-Bit Address Register
SP	8-Bit Stack Pointer Register
PC	15-Bit Program Counter Register
PU	Upper 7 Bits of PC
PL	Lower 8 Bits of PC
C	1 Bit of PSW Register for Carry
HC	1 Bit of PSW Register for Half Carry
GIE	1 Bit of PSW Register for Global Interrupt Enable
VU	Interrupt Vector Upper Byte
VL	Interrupt Vector Lower Byte

Symbols	
[B]	Memory Indirectly Addressed by B Register
[X]	Memory Indirectly Addressed by X Register
MD	Direct Addressed Memory
Mem	Direct Addressed Memory or [B]
Meml	Direct Addressed Memory or [B] or Immediate Data
Imm	8-Bit Immediate Data
Reg	Register Memory: Addresses F0 to FF (Includes B, X and SP)
Bit	Bit Number (0 to 7)
←	Loaded with
↔	Exchanged with

Instruction Set (Continued)

INSTRUCTION SET

ADD	A,Meml	ADD	A ← A + Meml
ADC	A,Meml	ADD with Carry	A ← A + Meml + C, C ← Carry HC ← Half Carry
SUBC	A,Meml	Subtract with Carry	A ← A $\overline{\text{Meml}}$ + C, C ← Carry HC ← Half Carry
AND	A,Meml	Logical AND	A ← A and Meml
ANDSZ	A,Imm	Logical AND Immed., Skip if Zero	Skip next if (A and Imm) = 0
OR	A,Meml	Logical OR	A ← A or Meml
XOR	A,Meml	Logical EXclusive OR	A ← A xor Meml
IFEQ	MD,Imm	IF EQual	Compare MD and Imm, Do next if MD = Imm
IFEQ	A,Meml	IF EQual	Compare A and Meml, Do next if A = Meml
IFNE	A,Meml	IF Not Equal	Compare A and Meml, Do next if A ≠ Meml
IFGT	A,Meml	IF Greater Than	Compare A and Meml, Do next if A > Meml
IFBNE	#	If B Not Equal	Do next if lower 4 bits of B ≠ Imm
DRSZ	Reg	Decrement Reg., Skip if Zero	Reg ← Reg − 1, Skip if Reg = 0
SBIT	#,Mem	Set BIT	1 to bit, Mem (bit = 0 to 7 immediate)
RBIT	#,Mem	Reset BIT	0 to bit, Mem
IFBIT	#,Mem	IF BIT	If bit in A or Mem is true do next instruction
RPND		Reset PeNDing Flag	Reset Software Interrupt Pending Flag
X	A,Mem	EXchange A with Memory	A ⟷ Mem
X	A,[X]	EXchange A with Memory [X]	A ⟷ [X]
LD	A,Meml	LoaD A with Memory	A ← Meml
LD	A,[X]	LoaD A with Memory [X]	A ← [X]
LD	B,Imm	LoaD B with Immed.	B ← Imm
LD	Mem,Imm	LoaD Memory Immed	Mem ← Imm
LD	Reg,Imm	LoaD Register Memory Immed.	Reg ← Imm
X	A, [B ±]	EXchange A with Memory [B]	A ⟷ [B], (B ← B ±1)
X	A, [X ±]	EXchange A with Memory [X]	A ⟷ [X], (X ← ±1)
LD	A, [B±]	LoaD A with Memory [B]	A ← [B], (B ← B ±1)
LD	A, [X±]	LoaD A with Memory [X]	A ← [X], (X ← X±1)
LD	[B±],Imm	LoaD Memory [B] Immed.	[B] ← Imm, (B ← B±1)
CLR	A	CLeaR A	A ← 0
INC	A	INCrement A	A ← A + 1
DEC	A	DECrementA	A ← A − 1
LAID		Load A InDirect from ROM	A ← ROM (PU,A)
DCOR	A	Decimal CORrect A	A ← BCD correction of A (follows ADC, SUBC)
RRC	A	Rotate A Right thru C	C → A7 → ... → A0 → C
RLC	A	Rotate A Left thru C	C ← A7 ← ... ← A0 ← C
SWAP	A	SWAP nibbles of A	A7...A4 ⟷ A3...A0
SC		Set C	C ← 1, HC ← 1
RC		Reset C	C ← 0, HC ← 0
IFC		IF C	IF C is true, do next instruction
IFNC		IF Not C	If C is not true, do next instruction
POP	A	POP the stack into A	SP ← SP + 1, A ← [SP]
PUSH	A	PUSH A onto the stack	[SP] ← A, SP ← SP − 1
VIS		Vector to Interrupt Service Routine	PU ← [VU], PL ← [VL]
JMPL	Addr.	Jump absolute Long	PC ← ii (ii = 15 bits, 0 to 32k)
JMP	Addr.	Jump absolute	PC9...0 ← i (i = 12 bits)
JP	Disp.	Jump relative short	PC ← PC + r (r is −31 to +32, except 1)
JSRL	Addr.	Jump SubRoutine Long	[SP] ← PL, [SP−1] ← PU,SP−2, PC ← ii
JSR	Addr	Jump SubRoutine	[SP] ← PL, [SP−1] ← PU,SP−2, PC9...0 ← i
JID		Jump InDirect	PL ← ROM (PU,A)
RET		RETurn from subroutine	SP + 2, PL ← [SP], PU ← [SP−1]
RETSK		RETurn and SKip	SP + 2, PL ← [SP],PU ← [SP−1]
RETI		RETurn from Interrupt	SP + 2, PL ← [SP],PU ← [SP−1],GIE ← 1
INTR		Generate an Interrupt	[SP] ← PL, [SP−1] ← PU, SP−2, PC ← 0FF
NOP		No OPeration	PC ← PC + 1

Instruction Execution Time

Most instructions are single byte (with immediate addressing mode instructions taking two bytes).

Most single byte instructions take one cycle time to execute.

See the BYTES and CYCLES per INSTRUCTION table for details.

Bytes and Cycles per Instruction

The following table shows the number of bytes and cycles for each instruction in the format of byte/cycle.

	[B]	Direct	Immed.
ADD	1/1	3/4	2/2
ADC	1/1	3/4	2/2
SUBC	1/1	3/4	2/2
AND	1/1	3/4	2/2
OR	1/1	3/4	2/2
XOR	1/1	3/4	2/2
IFEQ	1/1	3/4	2/2
IFNE	1/1	3/4	2/2
IFGT	1/1	3/4	2/2
IFBNE	1/1		
DRSZ		1/3	
SBIT	1/1	3/4	
RBIT	1/1	3/4	
IFBIT	1/1	3/4	

RPND	1/1

Instructions Using A & C

CLRA	1/1
INCA	1/1
DECA	1/1
LAID	1/3
DCOR	1/1
RRCA	1/1
RLCA	1/1
SWAPA	1/1
SC	1/1
RC	1/1
IFC	1/1
IFNC	1/1
PUSHA	1/3
POPA	1/3
ANDSZ	2/2

Transfer of Control Instructions

JMPL	3/4
JMP	2/3
JP	1/3
JSRL	3/5
JSR	2/5
JID	1/3
VIS	1/5
RET	1/5
RETSK	1/5
RETI	1/5
INTR	1/7
NOP	1/1

Memory Transfer Instructions

	Register Indirect		Direct	Immed.	Register Indirect Auto Incr. & Decr.		
	[B]	[X]			[B+, B−]	[X+, X−]	
X A,*	1/1	1/3	2/3		1/2	1/3	
LD A,*	1/1	1/3	2/3	2/2	1/2	1/3	
LD B, Imm				1/1			(IF B < 16)
LD B, Imm				2/2			(IF B > 15)
LD Mem, Imm	2/2		3/3		2/2		
LD Reg, Imm			2/3				
IFEQ MD, Imm			3/3				

* = > Memory location addressed by B or X or directly.

COP888CF Opcode Table

Upper Nibble Along X-Axis
Lower Nibble Along Y-Axis

F	E	D	C	B	A	9	8	
JP −15	JP −31	LD 0F0, # i	DRSZ 0F0	RRCA	RC	ADC A,#i	ADC A,[B]	0
JP −14	JP −30	LD 0F1, # i	DRSZ 0F1	*	SC	SUBC A, #i	SUB A,[B]	1
JP −13	JP −29	LD 0F2, # i	DRSZ 0F2	X A, [X+]	X A,[B+]	IFEQ A,#i	IFEQ A,[B]	2
JP −12	JP −28	LD 0F3, # i	DRSZ 0F3	X A, [X−]	X A,[B−]	IFGT A,#i	IFGT A,[B]	3
JP −11	JP −27	LD 0F4, # i	DRSZ 0F4	VIS	LAID	ADD A,#i	ADD A,[B]	4
JP −10	JP −26	LD 0F5, # i	DRSZ 0F5	RPND	JID	AND A,#i	AND A,[B]	5
JP −9	JP −25	LD 0F6, # i	DRSZ 0F6	X A,[X]	X A,[B]	XOR A,#i	XOR A,[B]	6
JP −8	JP −24	LD 0F7, # i	DRSZ 0F7	*	*	OR A,#i	OR A,[B]	7
JP −7	JP −23	LD 0F8, # i	DRSZ 0F8	NOP	RLCA	LD A,#i	IFC	8
JP −6	JP −22	LD 0F9, # i	DRSZ 0F9	IFNE A,[B]	IFEQ Md,#i	IFNE A,#i	IFNC	9
JP −5	JP −21	LD 0FA, # i	DRSZ 0FA	LD A,[X+]	LD A,[B+]	LD [B+],#i	INCA	A
JP −4	JP −20	LD 0FB, # i	DRSZ 0FB	LD A,[X−]	LD A,[B−]	LD [B−],#i	DECA	B
JP −3	JP −19	LD 0FC, # i	DRSZ 0FC	LD Md,#i	JMPL	X A,Md	POPA	C
JP −2	JP −18	LD 0FD, # i	DRSZ 0FD	DIR	JSRL	LD A,Md	RETSK	D
JP −1	JP −17	LD 0FE, # i	DRSZ 0FE	LD A,[X]	LD A,[B]	LD [B],#i	RET	E
JP −0	JP −16	LD 0FF, # i	DRSZ 0FF	*	*	LD B,#i	RETI	F

COP888CF Opcode Table (Continued)

Upper Nibble Along X-Axis

Lower Nibble Along Y-Axis

7	6	5	4	3	2	1	0	
IFBIT 0,[B]	ANDSZ A, #i	LD B,#0F	IFBNE 0	JSR x000–x0FF	JMP x000–x0FF	JP +17	INTR	0
IFBIT 1,[B]	*	LD B,#0E	IFBNE 1	JSR x100–x1FF	JMP x100–x1FF	JP +18	JP + 2	1
IFBIT 2,[B]	*	LD B,#0D	IFBNE 2	JSR x200–x2FF	JMP x200–x2FF	JP +19	JP + 3	2
IFBIT 3,[B]	*	LD B,#0C	IFBNE 3	JSR x300–x3FF	JMP x300–x3FF	JP +20	JP + 4	3
IFBIT 4,[B]	CLRA	LD B,#0B	IFBNE 4	JSR x400–x4FF	JMP x400–x4FF	JP +21	JP + 5	4
IFBIT 5,[B]	SWAPA	LD B,#0A	IFBNE 5	JSR x500–x5FF	JMP x500–x5FF	JP +22	JP + 6	5
IFBIT 6,[B]	DCORA	LD B,#09	IFBNE 6	JSR x600–x6FF	JMP x600–x6FF	JP +23	JP + 7	6
IFBIT 7,[B]	PUSHA	LD B,#08	IFBNE 7	JSR x700–x7FF	JMP x700–x7FF	JP +24	JP + 8	7
SBIT 0,[B]	RBIT 0,[B]	LD B,#07	IFBNE 8	JSR x800–x8FF	JMP x800–x8FF	JP +25	JP + 9	8
SBIT 1,[B]	RBIT 1,[B]	LD B,#06	IFBNE 9	JSR x900–x9FF	JMP x900–x9FF	JP +26	JP + 10	9
SBIT 2,[B]	RBIT 2,[B]	LD B,#05	IFBNE 0A	JSR xA00–xAFF	JMP xA00–xAFF	JP +27	JP + 11	A
SBIT 3,[B]	RBIT 3,[B]	LD B,#04	IFBNE 0B	JSR xB00–xBFF	JMP xB00–xBFF	JP +28	JP + 12	B
SBIT 4,[B]	RBIT 4,[B]	LD B,#03	IFBNE 0C	JSR xC00–xCFF	JMP xC00–xCFF	JP +29	JP + 13	C
SBIT 5,[B]	RBIT 5,[B]	LD B,#02	IFBNE 0D	JSR xD00–xDFF	JMP xD00–xDFF	JP +30	JP + 14	D
SBIT 6,[B]	RBIT 6,[B]	LD B,#01	IFBNE 0E	JSR xE00–xEFF	JMP xE00–xEFF	JP +31	JP + 15	E
SBIT 7,[B]	RBIT 7,[B]	LD B,#00	IFBNE 0F	JSR xF00–xFFF	JMP xF00–xFFF	JP +32	JP + 16	F

Where,

i is the immediate data

Md is a directly addressed memory location

* is an unused opcode

Note: The opcode 60 Hex is also the opcode for IFBIT #i,A

Mask Options

The COP888CF mask programmable options are shown below. The options are programmed at the same time as the ROM pattern submission.

```
OPTION 1: CLOCK CONFIGURATION
  = 1     Crystal Oscillator (CKI/10)
              G7 (CKO) is clock generator
              output to crystal/resonator
              CKI is the clock input
  = 2     Single-pin RC controlled
              oscillator (CKI/10)
              G7 is available as a HALT
              restart and/or general purpose
              input

OPTION 2: HALT
  = 1     Enable HALT mode
  = 2     Disable HALT mode

OPTION 3: COP888CF BONDING
  = 1     44-Pin PLCC
  = 2     40-Pin DIP
  = 3     N/A
  = 4     28-Pin DIP
  = 5     28-Pin SO
```

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (if clock option-1 has been selected). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_C$).

Development Support

IN-CIRCUIT EMULATOR

The MetaLink iceMASTER™-COP8 Model 400 In-Circuit Emulator for the COP8 family of microcontrollers features high-performance operation, ease of use, and an extremely flexible user-interface or maximum productivity. Interchangeable probe cards, which connect to the standard common base, support the various configurations and packages of the COP8 family.

The iceMASTER provides real time, full speed emulation up to 10 MHz, 32 kBytes of emulation memory and 4k frames of trace buffer memory. The user may define as many as 32k trace and break triggers which can be enabled, disabled, set or cleared. They can be simple triggers based on code address, direct address, opcode value, opcode class or immediate operand. Complex breakpoints can be ANDed and ORed together. Trace information consists of address bus values, opcodes and user selectable probe clips status (external event lines). The trace buffer can be viewed as raw hex or as disassembled instructions. The probe clip bit values can be displayed in binary, hex or digital waveform formats.

During single-step operation the dynamically annotated code feature displays the contents of all accessed (read and write) memory locations and registers, as well as flow-of-control direction change markers next to each instruction executed.

The iceMASTER's performance analyzer offers a resolution of better than 6 μs. The user can easily monitor the time spent executing specific portions of code and find "hot spots" or "dead code". Up to 15 independent memory areas based on code address or label ranges can be defined. Analysis results can be viewed in bar graph format or as actual frequency count.

Emulator memory operations for program memory include single line assembler, disassembler, view, change and write to file. Data memory operations include fill, move, compare, dump to file, examine and modify. The contents of any memory space can be directly viewed and modified from the corresponding window.

The iceMASTER comes with an easy to use window interface. Each window can be sized, highlighted, color-controlled, added, or removed completely. Commands can be accessed via pull-down-menus and/or redefinable hot keys. A context sensitive hypertext/hyperlinked on-line help system explains clearly the options the user has from within any window.

The iceMASTER connects easily to a PC® via the standard COMM port and its 115.2 kBaud serial link keeps typical program download time to under 3 seconds.

The following tables list the emulator and probe cards ordering information.

Emulator Ordering Information

Part Number	Description
IM-COP8/400	MetaLink base unit in-circuit emulator for all COP8 devices, symbolic debugger software and RS 232 serial interface cable.
MHW-PS3	Power supply 110V/60 Hz
MHW-PS4	Power supply 220V/50 Hz

Probe Card Ordering Information

Part Number	Package	Voltage Range	Emulates
MHW-884CF28D5PC	28 DIP	4.5V–5.5V	COP884CF
MHW-884CF28DWPC	28 DIP	2.5V–6.0V	COP884CF
MHW-888CF40D5PC	40 DIP	4.5V–5.5V	COP888CF
MHW-888CF40DWPC	40 DIP	2.5V–6.0V	COP888CF
MWH-888CF44D5PC	44 PLCC	4.5V–5.5V	COP888CF
MHW-888CF44DWPC	44 PLCC	2.5V–6.0V	COP888CF

MACRO CROSS ASSEMBLER

National Semiconductor offers a COP8 macro cross assembler. It runs on industry standard compatible PCs and supports all of the full-symbolic debugging features of the MetaLink iceMASTER emulators.

Assembler Ordering Information

Part Number	Description	Manual
MOLE-COP8-IBM	COP8 macro cross assembler for IBM®, PC/XT®, PC-AT® or compatible.	424410527-001

Development Support (Continued)

SIMULATOR

The COP8 Designer's Tool Kit is available for evaluating National Semiconductor's COP8 microcontroller family. The kit contains programmer's manuals, device datasheets, pocket reference guide, assembler and simulator, which allows the user to write, test, debug and run code on an industry standard compatible PC. The simulator has a windowed user interface and can handle script files that simulate hardware inputs, interrupts and automatic command processing. The capture file feature enables the user to record to a file current cycle count and output port changes which are caused by the program under test.

Simulator Ordering Information

Part Number	Description	Manual
COP8-TOOL-KIT	COP8 Designer's Tool Kit Assembler and Simulator	420420270-001 424420269-001

SINGLE CHIP EMULATOR DEVICE

The COP8 family is fully supported by single chip form, fit and function emulators. For more detailed information refer to the emulation device specific datasheets and the form, fit, function emulator selection table below.

PROGRAMMING SUPPORT

Programming of the single chip emulator devices is supported by different sources. National Semiconductor offers a duplicator board, which allows the transfer of program code from a standard programmed EPROM to the single chip emulator and vice versa. Data I/O supports COP8 emulator device programming with its uniSite 48 and System 2900 programmers. Further information on Data I/O programmers can be obtained from any Data I/O sales office or the following USA numbers:

Telephone: (206) 881-6444 Fax: (206) 882-1043

Single Chip Emulator Selection Table

Device Number	Clock Option	Package	Description	Emulates
COP888CFMHEL-X	X = 1: crystal X = 3: R/C	44 LDCC	Multi-Chip Module (MCM), UV erasable	COP888CF
COP888CFMHD-X	X = 1: crystal X = 3: R/C	40 DIP	MCM, UV erasable	COP888CF
COP884CFMHD-X	X = 1: crystal X = 3: R/C	28 DIP	MCM, UV erasable	COP884CF
COP884CFMHEA-X	X = 1: crystal X = 3: R/C	28 LCC	MCM (same footprint as 28 SO), UV erasable	COP884CF

Duplicator Board Ordering Information

Part Number	Description	Devices Supported
COP8-PRGM-28D	Duplicator Board for 28 DIP Multi-Chip Module (MCM) and for use with Scrambler Boards	COP884CFMHD
COP8-SCRM-DIP	MCM Scrambler Board for 40 DIP socket	COP888CFMHD
COP8-SCRM-PCC	MCM Scrambler Board for 44 PLCC/LDCC	COP888CFMHEL
COP8-SCRM-SBX	Hybrid Scrambler Board for 28 LCC Socket	COP884CFMHEA
COP8-PRGM-DIP	Duplicator Board with COP8-SCRM-DIP Scrambler Board	COP884CFMHD, COP888CFMHD
COP8-PRGM-PCC	Duplicator Board with COP8-SCRM-PCC Scrambler Board	COP888CFMEL, COP884CFMHD

Development Support (Continued)

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications group. The Dial-A-Helper is an Electronic Bulletin Board Information system.

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down loaded to disk for later use.

ORDER P/N: MOLE-DIAL-A-HLP

Information System Package Contents:
- Dial-A-Helper Users Manual
- Public Domain Communications Software

FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factor applications support. If a user has questions, he can leave messages on our electronic bulletin board, which we will respond to.

Voice:	(408) 721-5582	
Modem:	(408) 739-1162	
	Baud:	300 or 1200 Baud
	Set-Up:	Length: 8-Bit
		Parity: None
		Stop Bit: 1
	Operation:	24 Hours, 7 Days

National Semiconductor

COP884CG/COP888CG
Single-Chip microCMOS Microcontrollers

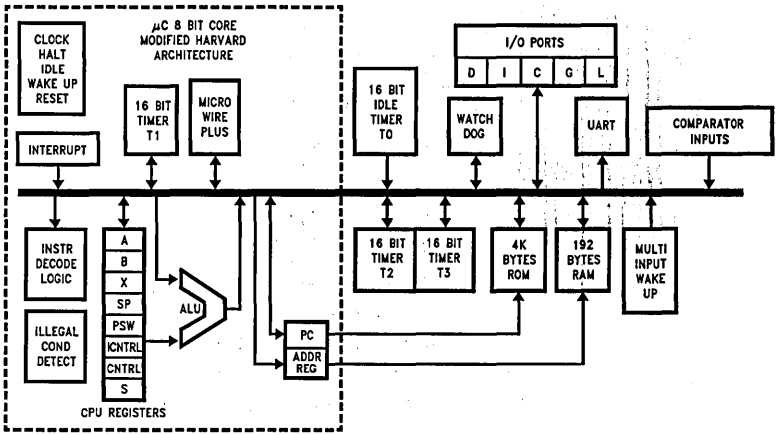
General Description

The COP888 family of microcontrollers uses an 8-bit single chip core architecture fabricated with National Semiconductor's M²CMOS™ process technology. The COP888CG is a member of this expandable 8-bit core processor family of microcontrollers. (Continued)

Features

- Low cost 8-bit microcontroller
- Fully static CMOS, with low current drain
- Two power saving modes: HALT and IDLE
- 1 μs instruction cycle time
- 4096 bytes on-board ROM (COP888CG)
- 192 bytes on-board RAM (COP888CG)
- Single supply operation: 2.5V–6V
- Full duplex UART
- Two analog comparators
- MICROWIRE/PLUS™ serial I/O
- WATCHDOG™ and Clock Monitor logic
- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- Three 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers (B and X)
- Fourteen multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Three Timers (Each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — UART (2)
  - — Default VIS
- Versatile instruction set
- True bit manipulation
- Memory mapped I/O
- BCD arithmetic instructions
- Package: 44 PLCC or 40 N or 28 N or 28 PLCC
  - — 44 PLCC with 39 I/O pins
  - — 40 N with 35 I/O pins
  - — 28 N with 23 I/O pins
- Software selectable I/O options
  - — TRI-STATE® Output
  - — Push-Pull Output
  - — Weak Pull Up Input
  - — High Impedance Input
- Schmitt trigger inputs on ports G and L
- Temperature ranges: −40°C to +85°C, −55°C to +125°C
- Form factor emulation devices
- Real time emulation and full program debug offered by National's Development Systems

Block Diagram



TL/DD/9765–1

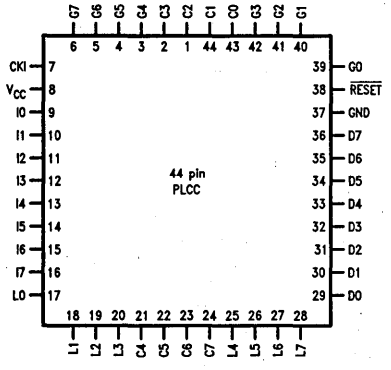
FIGURE 1. COP888CG Block Diagram

General Description (Continued)

They are fully static parts, fabricated using double-metal silicon gate microCMOS technology. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS serial I/O, three 16-bit timer/counters supporting three modes (Processor Independent PWM generation, External Event counter, and Input Capture mode capabilities), full duplex UART, two comparators, and two power savings modes (HALT and IDLE), both with a multi-sourced wakeup/interrupt capability. This multi-sourced interrupt capability may also be used independent of the HALT or IDLE modes. Each I/O pin has software selectable configurations. The devices operate over a voltage range of 2.5V to 6V. High throughput is achieved with an efficient, regular instruction set operating at a maximum of 1 μs per instruction rate.

Connection Diagrams

Plastic Chip Carrier

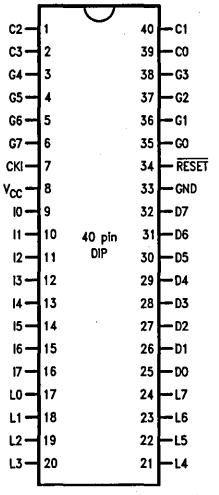


TL/DD/9765-2

Top View

Order Number COP888CG-XXX/V
See NS Plastic Chip Package Number V44A

Dual-In-Line Package

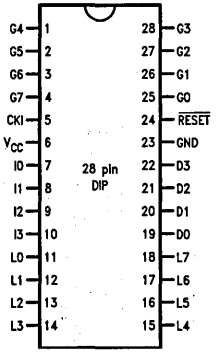


TL/DD/9765-4

Top View

Order Number COP888CG-XXX/N
See NS Molded Package Number N40A

Dual-In-Line Package



TL/DD/9765-5

Top View

Order Number COP884CG-XXX/N
See NS Molded Package Number N28A

FIGURE 2a. COP888CG Connection Diagrams

Connection Diagrams (Continued)

COP888CG Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU	CKX	12	18	18
L2	I/O	MIWU	TDX	13	19	19
L3	I/O	MIWU	RDX	14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU	T3A	17	23	27
L7	I/O	MIWU	T3B	18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
I0	I			7	9	9
I1	I	COMP1IN−		8	10	10
I2	I	COMP1IN+		9	11	11
I3	I	COMP1OUT		10	12	12
I4	I	COMP2IN−			13	13
I5	I	COMP2IN+			14	14
I6	I	COMP2OUT			15	15
I7	I				16	16
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		2.5		6	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			5.5	mA
CKI = 4 MHz	V_{CC} = 4.0V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4.0V, t_c = 10 μs			1.4	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<1	10	μA
	V_{CC} = 4.0V, CKI = 0 MHz		<0.5	6	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4.0V, t_c = 10 μs			0.7	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6V	−2		+2	μA
Input Pullup Current	V_{CC} = 6V	40		250	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4V, V_{OL} = 1V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2.0			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4V, V_{OH} = 2.7V	10		100	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink (Push-Pull Mode)	V_{CC} = 4V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			mA
TRI-STATE Leakage	V_{CC} = 6.0V	−2		+2	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a crystal/resonator oscillator, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L, C, and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor and the comparators are disabled.

DC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				15	mA
All others				3	mA
Maximum Input Current without Latchup (Note 5)	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

AC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal, Resonator,	$4V \le V_{CC} \le 6V$	1		DC	μs
R/C Oscillator	$2.5V \le V_{CC} < 4V$	2.5		DC	μs
	$4V \le V_{CC} \le 6V$	3		DC	μs
	$2.5V \le V_{CC} < 4V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 4)	f_r = Max	40		60	%
Rise Time (Note 4)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 4)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	$4V \le V_{CC} \le 6V$	200			ns
	$2.5V \le V_{CC} < 4V$	500			ns
t_{HOLD}	$4V \le V_{CC} \le 6V$	60			ns
	$2.5V \le V_{CC} < 4V$	150			ns
Output Propagation Delay	$R_L = 2.2k, C_L = 100$ pF				
t_{PD1}, t_{PD0}					
SO, SK	$4V \le V_{CC} \le 6V$			0.7	μs
	$2.5V \le V_{CC} < 4V$			1.75	μs
All Others	$4V \le V_{CC} \le 6V$			1	μs
	$2.5V \le V_{CC} < 4V$			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 4: Parameter sampled but not 100% tested.

Note 5: Except pin G7: −60 mA to +100 mA (sampled but not 100% tested).

Comparators AC and DC Characteristics V_{CC} = 5V, T_A = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	0.4V ≤ V_{IN} ≤ V_{CC} − 1.5V		±10	±25	mV
Input Common Mode Voltage Range		0.4		V_{CC} − 1.5	V
Low Level Output Current	V_{OL} = 0.4V	1.6			mA
High Level Output Current	V_{OH} = 4.6V	1.6			mA
DC Supply Current Per Comparator (When Enabled)				250	μA
Response Time	TBD mV Step, TBD mV Overdrive, 100 pF Load		1		μs

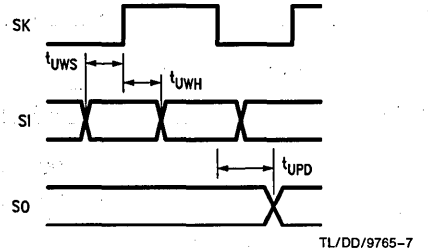


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FIGURE 2. MICROWIRE/PLUS Timing

Pin Descriptions

V_{CC} and GND are the power supply pins.

CKI is the clock input. This can come from an R/C generated oscillator, or a crystal oscillator (in conjunction with CKO). See Oscillator Description section.

$\overline{\text{RESET}}$ is the master reset input. See Reset Description section.

The COP888CG contains three bidirectional 8-bit I/O ports (C, G and L), where each individual bit may be independently configured as an input (Schmitt trigger inputs on ports L and G), output or TRI-STATE under program control. Three data memory address locations are allocated for each of these I/O ports. Each I/O port has two associated 8-bit memory mapped registers, the CONFIGURATION register and the output DATA register. A memory mapped address is also reserved for the input pins of each I/O port. (See the memory map for the various addresses associated with the I/O ports.) *Figure 3* shows the I/O port configurations. The DATA and CONFIGURATION registers allow for each port bit to be individually configured under software control as shown below:

CONFIGURATION Register	DATA Register	Port Set-Up
0	0	Hi-Z Input (TRI-STATE Output)
0	1	Input with Weak Pull-Up
1	0	Push-Pull Zero Output
1	1	Push-Pull One Output

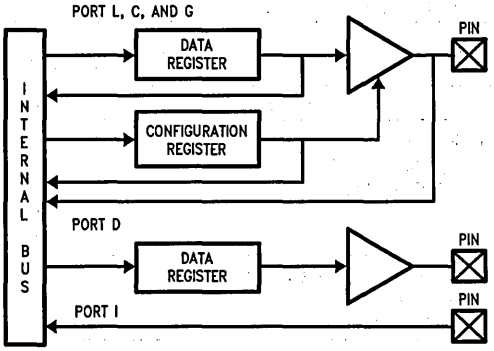

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FIGURE 3. I/O Port Configurations

PORT L is an 8-bit I/O port. All L-pins have Schmitt triggers on the inputs.

The Port L supports Multi-Input Wake Up on all eight pins. L1 is used for the UART external clock. L2 and L3 are used for the UART transmit and receive. L4 and L5 are used for the timer input functions T2A and T2B. L6 and L7 are used for the timer input functions T3A and T3B.

The Port L has the following alternate features:

- L0 MIWU
- L1 MIWU or CKX
- L2 MIWU or TDX
- L3 MIWU or RDX
- L4 MIWU or T2A
- L5 MIWU or T2B
- L6 MIWU or T3A
- L7 MIWU or T3B

Port G is an 8-bit port with 5 I/O pins (G0, G2–G5), an input pin (G6), and two dedicated output pins (G1 and G7). Pins G0 and G2–G6 all have Schmitt Triggers on their inputs. Pin G1 serves as the dedicated WDOUT WATCHDOG output, while pin G7 is either input or output depending on the oscillator mask option selected. With the crystal oscillator option selected, G7 serves as the dedicated output pin for the CKO clock output. With the single-pin R/C oscillator mask option selected, G7 serves as a general purpose input pin but is also used to bring the device out of HALT mode with a low to high transition on G7. There are two registers associated with the G Port, a data register and a configuration register. Therefore, each of the 5 I/O bits (G0, G2–G5) can be individually configured under software control.

Pin Descriptions (Continued)

Since G6 is an input only pin and G7 is the dedicated CKO clock output pin (crystal clock option) or general purpose input (R/C clock option), the associated bits in the data and configuration registers for G6 and G7 are used for special purpose functions as outlined below. Reading the G6 and G7 data bits will return zeros.

Note that the chip will be placed in the HALT mode by writing a "1" to bit 7 of the Port G Data Register. Similarly the chip will be placed in the IDLE mode by writing a "1" to bit 6 of the Port G Data Register.

Writing a "1" to bit 6 of the Port G Configuration Register enables the MICROWIRE/PLUS to operate with the alternate phase of the SK clock. The G7 configuration bit, if set high, enables the clock start up delay after HALT when the R/C clock configuration is used.

	Config Reg.	Data Reg.
G7	CLKDLY	HALT
G6	Alternate SK	IDLE

Port G has the following alternate features:

- G0 INTR (External Interrupt Input)
- G2 T1B (Timer T1 Capture Input)
- G3 T1A (Timer T1 I/O)
- G4 SO (MICROWIRE™ Serial Data Output)
- G5 SK (MICROWIRE Serial Clock)
- G6 SI (MICROWIRE Serial Data Input)

Port G has the following dedicated functions:

- G1 WDOUT WATCHDOG and/or Clock Monitor dedicated output
- G7 CKO Oscillator dedicated output or general purpose input

Port C is an 8-bit I/O port. The 40-pin device does not have a full complement of Port C pins. The unavailable pins are not terminated. A read operation for these unterminated pins will return unpredicatable values.

PORT I is an eight-bit Hi-Z input port. The 28-pin device does not have a full complement of Port I pins. The unavailable pins are not terminated i.e., they are floating. A read operation for these unterminated pins will return unpredictable values. The user must ensure that the software takes this into account by either masking or restricting the accesses to bit operations. The unterminated Port I pins will draw power only when addressed.

Port I1–I3 are used for Comparator 1. Port I4–I6 are used for Comparator 2.

The Port I has the following alternate features.

- I1 COMP1 − IN (Comparator 1 Negative Input)
- I2 COMP1 + IN (Comparator 1 Positive Input)
- I3 COMP1OUT (Comparator 1 Output)
- I4 COMP2 − IN (Comparator 2 Negative Input)
- I5 COMP2 + IN (Comparator 2 Positive Input)
- I6 COMP2OUT (Comparator 2 Output)

Port D is an 8-bit output port that is preset high when $\overline{\text{RESET}}$ goes low. The user can tie two or more D port outputs together in order to get a higher drive.

Functional Description

The architecture of the COP888CG is modified Harvard architecture. With the Harvard architecture, the control store program memory (ROM) is separated from the data store memory (RAM). Both ROM and RAM have their own separate addressing space with separate address buses. The architecture, though based on Harvard architecture, permits transfer of data from ROM to RAM.

CPU REGISTERS

The CPU can do an 8-bit addition, subtraction, logical or shift operation in one instruction (t_C) cycle time.

There are six CPU registers:

A is the 8-bit Accumulator Register

PC is the 15-bit Program Counter Register

PU is the upper 7 bits of the program counter (PC)
PL is the lower 8 bits of the program counter (PC)

B is an 8-bit RAM address pointer, which can be optionally post auto incremented or decremented.

X is an 8-bit alternate RAM address pointer, which can be optionally post auto incremented or decremented.

SP is the 8-bit stack pointer, which points to the subroutine/interrupt stack (in RAM). The SP is initialized to RAM address 06F with reset.

S is the 8-bit Data Segment Address Register used to extend the lower half of the address range (00 to 7F) into 256 data segments of 128 bytes each.

All the CPU registers are memory mapped with the exception of the Accumulator (A) and the Program Counter (PC).

PROGRAM MEMORY

The program memory consists of 4096 bytes of ROM. These bytes may hold program instructions or constant data (data tables for the LAID instruction, jump vectors for the JID instruction, and interrupt vectors for the VIS instruction). The program memory is addressed by the 15-bit program counter (PC). All interrupts in the devices vector to program memory location 0FF Hex.

DATA MEMORY

The data memory address space includes the on-chip RAM and data registers, the I/O registers (Configuration, Data and Pin), the control registers, the MICROWIRE/PLUS SIO shift register, and the various registers, and counters associated with the timers (with the exception of the IDLE timer). Data memory is addressed directly by the instruction or indirectly by the B, X, SP pointers and S register.

The COP888CG has 192 bytes of RAM. Sixteen bytes of RAM are mapped as "registers" at addresses 0F0 to 0FF Hex. These registers can be loaded immediately, and also decremented and tested with the DRSZ (decrement register and skip if zero) instruction. The memory pointer registers X, SP, B and S are memory mapped into this space at address locations 0FC to 0FF Hex respectively, with the other registers being available for general usage.

The instruction set permits any bit in memory to be set, reset or tested. All I/O and registers (except A and PC) are memory mapped; therefore, I/O bits and register bits can be directly and individually set, reset and tested. The accumulator (A) bits can also be directly and individually tested.

Data Memory Segment RAM Extension

Data memory address 0FF is used as a memory mapped location for the Data Segment Address Register (S).

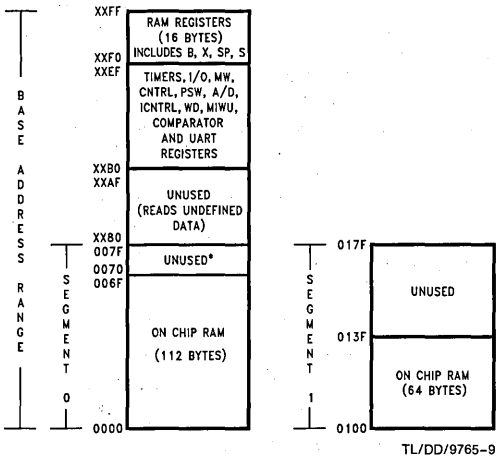
The data store memory is either addressed directly by a single byte address within the instruction, or indirectly relative to the reference of the B, X, or SP pointers (each contains a single-byte address). This single-byte address allows an addressing range of 256 locations from 00 to FF hex. The upper bit of this single-byte address divides the data store memory into two separate sections as outlined previously. With the exception of the RAM register memory from address locations 00F0 to 00FF, all RAM memory is memory mapped with the upper bit of the single-byte address being equal to zero. This allows the upper bit of the single-byte address to determine whether or not the base address range (from 0000 to 00FF) is extended. If this upper bit equals one (representing address range 0080 to 00FF), then address extension does not take place. Alternatively, if this upper bit equals zero, then the data segment extension register S is used to extend the base address range (from 0000 to 007F) from XX00 to XX7F, where XX represents the 8 bits from the S register. Thus the 128-byte data segment extensions are located from addresses 0100 to 017F for data segment 1, 0200 to 027F for data segment 2, etc., up to FF00 to FF7F for data segment 255. The base address range from 0000 to 007F represents data segment 0.

Figure 4 illustrates how the S register data memory extension is used in extending the lower half of the base address range (00 to 7F hex) into 256 data segments of 128 bytes each, with a total addressing range of 32 kbytes from XX00 to XX7F. This organization allows a total of 256 data segments of 128 bytes each with an additional upper base segment of 128 bytes. Furthermore, all addressing modes are available for all data segments. The S register must be changed under program control to move from one data segment (128 bytes) to another. However, the upper base segment (containing the 16 memory registers, I/O registers, control registers, etc.) is always available regardless of the contents of the S register, since the upper base segment (address range 0080 to 00FF) is independent of data segment extension.

The instructions that utilize the stack pointer (SP) always reference the stack as part of the base segment (Segment 0), regardless of the contents of the S register. The S register is not changed by these instructions. Consequently, the stack (used with subroutine linkage and interrupts) is always located in the base segment. The stack pointer will be initialized to point at data memory location 006F as a result of reset.

The 128 bytes of RAM contained in the base segment are split between the lower and upper base segments. The first 116 bytes of RAM are resident from address 0000 to 006F in the lower base segment, while the remaining 16 bytes of RAM represent the 16 data memory registers located at addresses 00F0 to 00FF of the upper base segment. No RAM is located at the upper sixteen addresses (0070 to 007F) of the lower base segment.

Additional RAM beyond these initial 128 bytes, however, will always be memory mapped in groups of 128 bytes (or less) at the data segment address extensions (XX00 to XX7F) of the lower base segment. The additional 64 bytes of RAM in the COP888CG (beyond the initial 128 bytes) are memory mapped at address locations 0100 to 013F hex.



*Reads as all ones.

FIGURE 4. RAM Organization

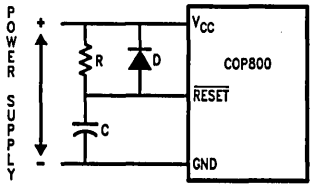
Reset

The $\overline{\text{RESET}}$ input when pulled low initializes the microcontroller. Initialization will occur whenever the $\overline{\text{RESET}}$ input is pulled low. Upon initialization, the data and configuration registers for ports L, G and C are cleared, resulting in these Ports being initialized to the TRI-STATE mode. Pin G1 of the G Port is an exception (as noted below) since pin G1 is dedicated as the WATCHDOG and/or Clock Monitor error output pin. Port D is set high. The PC, PSW, ICNTRL, CNTRL, T2CNTRL and T3CNTRL control registers are cleared. The UART registers PSR, ENU (except that TBMT bit is set), ENUR and ENUI are cleared. The Comparator Select Register is cleared. The S register is initialized to zero. The Multi-Input Wakeup registers WKEN, WKEDG and WKPND are cleared. The stack pointer, SP, is initialized to 6F Hex.

The device comes out of reset with both the WATCHDOG logic and the Clock Monitor detector armed, with the WATCHDOG service window bits set and the Clock Monitor bit set. The WATCHDOG and Clock Monitor circuits are inhibited during reset. The WATCHDOG service window bits being initialized high default to the maximum WATCHDOG service window of 64k t_C clock cycles. The Clock Monitor bit being initialized high will cause a Clock Monitor error following reset if the clock has not reached the minimum specified frequency at the termination of reset. A Clock Monitor error will cause an active low error output on pin G1. This error output will continue until 16 t_C–32 t_C clock cycles following the clock frequency reaching the minimum specified value, at which time the G1 output will enter the TRI-STATE mode.

The external RC network shown in *Figure 5* should be used to ensure that the $\overline{\text{RESET}}$ pin is held low until the power supply to the chip stabilizes.

Reset (Continued)



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RC > 5 × Power Supply Rise Time

FIGURE 5. Recommended Reset Circuit

Oscillator Circuits

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (crystal configuration). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_C$).

Figure 6 shows the Crystal and R/C diagrams.

CRYSTAL OSCILLATOR

CKI and CKO can be connected to make a closed loop crystal (or resonator) controlled oscillator.

Table A shows the component values required for various standard crystal values.

R/C OSCILLATOR

By selecting CKI as a single pin oscillator input, a single pin R/C oscillator circuit can be connected to it. CKO is available as a general purpose input, and/or HALT restart input.

Table B shows the variation in the oscillator frequencies as functions of the component (R and C) values.

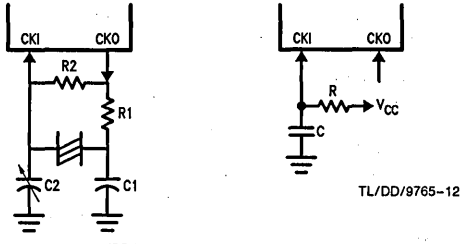

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FIGURE 6. Crystal and R/C Oscillator Diagrams

TABLE A. Crystal Oscillator Configuration, T_A = 25°C

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)	Conditions
0	1	30	30–36	10	V_{CC} = 5V
0	1	30	30–36	4	V_{CC} = 5.0V
0	1	200	100–150	0.455	V_{CC} = 5V

TABLE B. RC Oscillator Configuration, T_A = 25°C

R (kΩ)	C (pF)	CKI Freq (MHz)	Instr. Cycle (μs)	Conditions
3.3	82	2.2 to 2.7	3.7 to 4.6	V_{CC} = 5V
5.6	100	1.1 to 1.3	7.4 to 9.0	V_{CC} = 5V
6.8	100	0.9 to 1.1	8.8 to 10.8	V_{CC} = 5V

Note: 3k ≤ R ≤ 200k

50 pF ≤ C ≤ 200 pF

Current Drain

The total current drain of the chip depends on:

1. Oscillator operation mode—I1
2. Internal switching current—I2
3. Internal leakage current—I3
4. Output source current—I4
5. DC current caused by external input not at V_{CC} or GND—I5
6. Comparator DC supply current when enabled—I6
7. Clock Monitor current when enabled—I7

Thus the total current drain, It, is given as

$$It = I1 + I2 + I3 + I4 + I5 + I6 + I7$$

To reduce the total current drain, each of the above components must be minimum.

The chip will draw more current as the CKI input frequency increases up to the maximum 10 MHz value. Operating with a crystal network will draw more current than an external square-wave. Switching current, governed by the equation below, can be reduced by lowering voltage and frequency. Leakage current can be reduced by lowering voltage and temperature. The other two items can be reduced by carefully designing the end-user's system.

$$I2 = C \times V \times f$$

where C = equivalent capacitance of the chip
V = operating voltage
f = CKI frequency

Some sample current drain values at V_{CC} = 5V are:

CKI (MHz)	Inst. Cycle (μs)	It (mA)
10	1	15
3.58	2.8	5.4
2	5	3
0.3	33	0.45
0 (HALT)	—	<0.001 (typ.)

Control Registers

CNTRL Register (Address X'00EE)

The Timer1 (T1) and MICROWIRE/PLUS control register contains the following bits:

SL1 & SL0	Select the MICROWIRE/PLUS clock divide by (00 = 2, 01 = 4, 1x = 8)
IEDG	External interrupt edge polarity select (0 = Rising edge, 1 = Falling edge)
MSEL	Selects G5 and G4 as MICROWIRE/PLUS signals SK and SO respectively
T1C0	Timer T1 Start/Stop control in timer modes 1 and 2 Timer T1 Underflow Interrupt Pending Flag in timer mode 3
T1C1	Timer T1 mode control bit
T1C2	Timer T1 mode control bit
T1C3	Timer T1 mode control bit

T1C3	T1C2	T1C1	T1C0	MSEL	IEDG	SL1	SL0

Bit 7 Bit 0

Control Registers (Continued)

PSW Register (Address X'00EF)

The PSW register contains the following select bits:

- GIE Global interrupt enable (enables interrupts)
- EXEN Enable external interrupt
- BUSY MICROWIRE/PLUS busy shifting flag
- EXPND External interrupt pending
- T1ENA Timer T1 Interrupt Enable for Timer Underflow or T1A Input capture edge
- T1PNDA Timer T1 Interrupt Pending Flag (Autoreload RA in mode 1, T1 Underflow in Mode 2, T1A capture edge in mode 3)
- C Carry Flag
- HC Half Carry Flag

HC	C	T1PNDA	T1ENA	EXPND	BUSY	EXEN	GIE

Bit 7 Bit 0

The Half-Carry bit is also affected by all the instructions that affect the Carry flag. The SC (Set Carry) and RC (Reset Carry) instructions will respectively set or clear both the carry flags. In addition to the SC and RC instructions, ADC, SUBC, RRC and RLC instructions affect the carry and Half Carry flags.

ICNTRL Register (Address X'00E8)

The ICNTRL register contains the following bits:

- T1ENB Timer T1 Interrupt Enable for T1B Input capture edge
- T1PNDB Timer T1 Interrupt Pending Flag for T1B capture edge
- μWEN Enable MICROWIRE/PLUS interrupt
- μWPND MICROWIRE/PLUS interrupt pending
- T0EN Timer T0 Interrupt Enable (Bit 12 toggle)
- T0PND Timer T0 Interrupt pending
- LPEN L Port Interrupt Enable (Multi-Input Wakeup/Interrupt)

  Bit 7 could be used as a flag

Unused	LPEN	T0PND	T0EN	μWPND	μWEN	T1PNDB	T1ENB

Bit 7 Bit 0

T2CNTRL Register (Address X'00C6)

The T2CNTRL register contains the following bits:

- T2ENB Timer T2 Interrupt Enable for T2B Input capture edge
- T2PNDB Timer T2 Interrupt Pending Flag for T2B capture edge
- T2ENA Timer T2 Interrupt Enable for Timer Underflow or T2A Input capture edge
- T2PNDA Timer T2 Interrupt Pending Flag (Autoreload RA in mode 1, T2 Underflow in mode 2, T2A capture edge in mode 3)
- T2C0 Timer T2 Start/Stop control in timer modes 1 and 2 Timer T2 Underflow Interrupt Pending Flag in timer mode 3
- T2C1 Timer T2 mode control bit
- T2C2 Timer T2 mode control bit
- T2C3 Timer T2 mode control bit

T2C3	T2C2	T2C1	T2C0	T2PNDA	T2ENA	T2PNDB	T2ENB

Bit 7 Bit 0

T3CNTRL Register (Address X'00B6)

The T3CNTRL register contains the following bits:

- T3ENB Timer T3 Interrupt Enable for T3B
- T3PNDB Timer T3 Interrupt Pending Flag for T3B pin (T3B capture edge)
- T3ENA Timer T3 Interrupt Enable for Timer Underflow or T3A pin
- T3PNDA Timer T3 Interrupt Pending Flag (Autoload RA in mode 1, T3 Underflow in mode 2, T3a capture edge in mode 3)
- T3C0 Timer T3 Start/Stop control in timer modes 1 and 2

  Timer T3 Underflow Interrupt Pending Flag in timer mode 3
- T3C1 Timer T3 mode control bit
- T3C2 Timer T3 mode control bit
- T3C3 Timer T3 mode control bit

T3C3	T3C2	T3C1	T3C0	T3PNDA	T3ENA	T3PNDB	T3ENB

Bit 7 Bit 0

Timers

The COP888CG contains a very versatile set of timers (T0, T1, T2, T3). All timers and associated autoreload/capture registers power up containing random data.

TIMER T0 (IDLE TIMER)

The devices support applications that require maintaining real time and low power with the IDLE mode. This IDLE mode support is furnished by the IDLE timer T0, which is a 16-bit timer. The Timer T0 runs continuously at the fixed rate of the instruction cycle clock, t_C. The user cannot read or write to the IDLE Timer T0, which is a count down timer.

The Timer T0 supports the following functions:

Exit out of the Idle Mode (See Idle Mode description)
WATCHDOG logic (See WATCHDOG description)
Start up delay out of the HALT mode

The IDLE Timer T0 can generate an interrupt when the thirteenth bit toggles. This toggle is latched into the T0PND pending flag, and will occur every 4 ms at the maximum clock frequency (t_C = 1 μs). A control flag T0EN allows the interrupt from the thirteenth bit of Timer T0 to be enabled or disabled. Setting T0EN will enable the interrupt, while resetting it will disable the interrupt.

Timers (Continued)

TIMER T1, TIMER T2 AND TIMER T3

The devices have a set of three powerful timer/counter blocks, T1, T2 and T3. The associated features and functioning of a timer block are described by referring to the timer block Tx. Since the three timer blocks, T1, T2 and T3 are identical, all comments are equally applicable to any of the three timer blocks.

Each timer block consists of a 16-bit timer, Tx, and two supporting 16-bit autoreload/capture registers, RxA and RxB. Each timer block has two pins associated with it, TxA and TxB. The pin TxA supports I/O required by the timer block, while the pin TxB is an input to the timer block. The powerful and flexible timer block allows the device to easily perform all timer functions with minimal software overhead. The timer block has three operating modes: Processor Independent PWM mode, External Event Counter mode, and Input Capture mode.

The control bits TxC3, TxC2, and TxC1 allow selection of the different modes of operation.

Mode 1. Processor Independent PWM Mode

As the name suggests, this mode allows the device to generate a PWM signal with very minimal user intervention. The user only has to define the parameters of the PWM signal (ON time and OFF time). Once begun, the timer block will continuously generate the PWM signal completely independent of the microcontroller. The user software services the timer block only when the PWM parameters require updating.

In this mode the timer Tx counts down at a fixed rate of t_C. Upon every underflow the timer is alternately reloaded with the contents of supporting registers, RxA and RxB. The very first underflow of the timer causes the timer to reload from the register RxA. Subsequent underflows cause the timer to be reloaded from the registers alternately beginning with the register RxB.

The Tx Timer control bits, TxC3, TxC2 and TxC1 set up the timer for PWM mode operation.

Figure 7 shows a block diagram of the timer in PWM mode.

The underflows can be programmed to toggle the TxA output pin. The underflows can also be programmed to generate interrupts.

Underflows from the timer are alternately latched into two pending flags, TxPNDA and TxPNDB. The user must reset these pending flags under software control. Two control enable flags, TxENA and TxENB, allow the interrupts from the timer underflow to be enabled or disabled. Setting the timer enable flag TxENA will cause an interrupt when a timer underflow causes the RxA register to be reloaded into the timer. Setting the timer enable flag TxENB will cause an interrupt when a timer underflow causes the RxB register to be reloaded into the timer. Resetting the timer enable flags will disable the associated interrupts.

Either or both of the timer underflow interrupts may be enabled. This gives the user the flexibility of interrupting once per PWM period on either the rising or falling edge of the PWM output. Alternatively, the user may choose to interrupt on both edges of the PWM output.

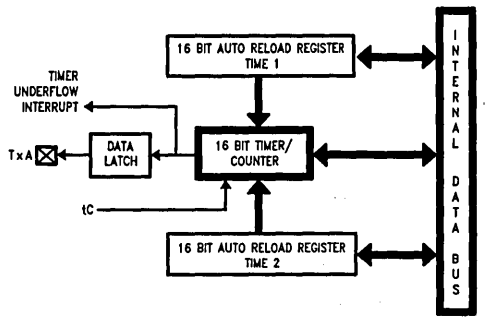

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FIGURE 7. Timer in PWM Mode

Mode 2. External Event Counter Mode

This mode is quite similar to the processor independent PWM mode described above. The main difference is that the timer, Tx, is clocked by the input signal from the TxA pin. The Tx timer control bits, TxC3, TxC2 and TxC1 allow the timer to be clocked either on a positive or negative edge from the TxA pin. Underflows from the timer are latched into the TxPNDA pending flag. Setting the TxENA control flag will cause an interrupt when the timer underflows.

In this mode the input pin TxB can be used as an independent positive edge sensitive interrupt input if the TxENB control flag is set. The occurrence of a positive edge on the TxB input pin is latched into the TxPNDB flag.

Figure 8 shows a block diagram of the timer in External Event Counter mode.

Note: The PWM output is not available in this mode since the TxA pin is being used as the counter input clock.

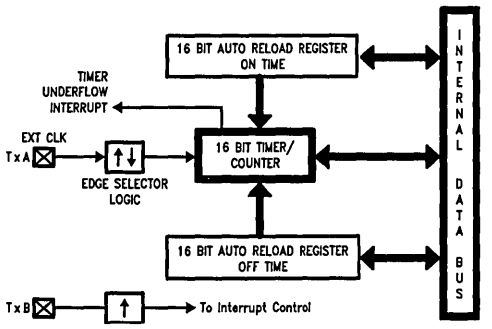

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FIGURE 8. Timer in External Event Counter Mode

Mode 3. Input Capture Mode

The device can precisely measure external frequencies or time external events by placing the timer block, Tx, in the input capture mode.

In this mode, the timer Tx is constantly running at the fixed t_C rate. The two registers, RxA and RxB, act as capture registers. Each register acts in conjunction with a pin. The register RxA acts in conjunction with the TxA pin and the register RxB acts in conjunction with the TxB pin.

Timers (Continued)

The timer value gets copied over into the register when a trigger event occurs on its corresponding pin. Control bits, TxC3, TxC2 and TxC1, allow the trigger events to be specified either as a positive or a negative edge. The trigger condition for each input pin can be specified independently.

The trigger conditions can also be programmed to generate interrupts. The occurrence of the specified trigger condition on the TxA and TxB pins will be respectively latched into the pending flags, TxPNDA and TxPNDB. The control flag TxENA allows the interrupt on TxA to be either enabled or disabled. Setting the TxENA flag enables interrupts to be generated when the selected trigger condition occurs on the TxA pin. Similarly, the flag TxENB controls the interrupts from the TxB pin.

Underflows from the timer can also be programmed to generate interrupts. Underflows are latched into the timer TxC0 pending flag (the TxC0 control bit serves as the timer underflow interrupt pending flag in the Input Capture mode). Consequently, the TxC0 control bit should be reset when entering the Input Capture mode. The timer underflow interrupt is enabled with the TxENA control flag. When a TxA interrupt occurs in the Input Capture mode, the user must check both the TxPNDA and TxC0 pending flags in order to determine whether a TxA input capture or a timer underflow (or both) caused the interrupt.

Figure 9 shows a block diagram of the timer in Input Capture mode.

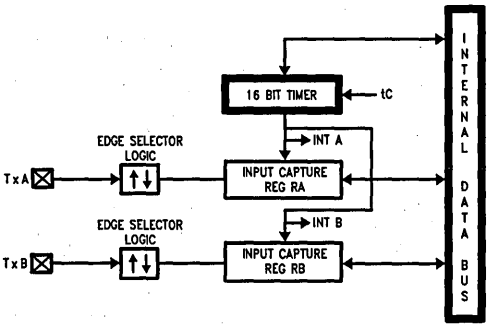

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FIGURE 9. Timer in Input Capture Mode

TIMER CONTROL FLAGS

The timers T1, T2 and T3 have indentical control structures. The control bits and their functions are summarized below.

TxC0	Timer Start/Stop control in Modes 1 and 2 (Processor Independent PWM and External Event Counter), where 1 = Start, 0 = Stop Timer Underflow Interrupt Pending Flag in Mode 3 (Input Capture)
TxPNDA	Timer Interrupt Pending Flag
TxPNDB	Timer Interrupt Pending Flag
TxENA	Timer Interrupt Enable Flag
TxENB	Timer Interrupt Enable Flag 1 = Timer Interrupt Enabled 0 = Timer Interrupt Disabled
TxC3	Timer mode control
TxC2	Timer mode control
TxC1	Timer mode control

Timers (Continued)

The timer mode control bits (TxC3, TxC2 and TxC1) are detailed below:

TxC3	TxC2	TxC1	Timer Mode	Interrupt A Source	Interrupt B Source	Timer Counts On
0	0	0	MODE 2 (External Event Counter)	Timer Underflow	Pos. TxB Edge	TxA Pos. Edge
0	0	1	MODE 2 (External Event Counter)	Timer Underflow	Pos. TxB Edge	TxA Neg. Edge
1	0	1	MODE 1 (PWM) TxA Toggle	Autoreload RA	Autoreload RB	t_C
1	0	0	MODE 1 (PWM) No TxA Toggle	Autoreload RA	Autoreload RB	t_C
0	1	0	MODE 3 (Capture) Captures: TxA Pos. Edge TxB Pos. Edge	Pos. TxA Edge or Timer Underflow	Pos. TxB Edge	t_C
1	1	0	MODE 3 (Capture) Captures: TxA Pos. Edge TxB Neg. Edge	Pos. TxA Edge or Timer Underflow	Neg. TxB Edge	t_C
0	1	1	MODE 3 (Capture) Captures: TxA Neg. Edge TxB Pos. Edge	Neg. TxB Edge or Timer Underflow	Pos. TxB Edge	t_C
1	1	1	MODE 3 (Capture) Captures: TxA Neg. Edge TxB Neg. Edge	Neg. TxA Edge or Timer Underflow	Neg. TxB Edge	t_C

Power Save Modes

The devices offer the user two power save modes of operation: HALT and IDLE. In the HALT mode, all microcontroller activities are stopped. In the IDLE mode, the on-board oscillator circuitry the WATCHDOG logic, the Clock Monitor and timer T0 are active but all other microcontroller activities are stopped. In either mode, all on-board RAM, registers, I/O states, and timers (with the exception of T0) are unaltered.

HALT MODE

The devices can be placed in the HALT mode by writing a "1" to the HALT flag (G7 data bit). All microcontroller activities, including the clock and timers, are stopped. The WATCHDOG logic on the device is disabled during the HALT mode. However, the clock monitor circuitry if enabled remains active and will cause the WATCHDOG output pin (WDOUT) to go low. If the HALT mode is used and the user does not want to activate the WDOUT pin, the Clock Monitor should be disabled after the device comes out of reset (resetting the Clock Monitor control bit with the first write to the WDSVR register). In the HALT mode, the power requirements of the device are minimal and the applied voltage (V_{CC}) may be decreased to V_r (V_r = 2.0V) without altering the state of the machine.

The devices support three different ways of exiting the HALT mode. The first method of exiting the HALT mode is with the Multi-Input Wakeup feature on the L port. The second method is with a low to high transition on the CKO (G7) pin. This method precludes the use of the crystal clock configuration (since CKO becomes a dedicated output), and so may be used with an RC clock configuration. The third method of exiting the HALT mode is by pulling the $\overline{\text{RESET}}$ pin low.

Since a crystal or ceramic resonator may be selected as the oscillator, the Wakeup signal is not allowed to start the chip running immediately since crystal oscillators and ceramic resonators have a delayed start up time to reach full amplitude and frequency stability. The IDLE timer is used to generate a fixed delay to ensure that the oscillator has indeed stabilized before allowing instruction execution. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry is enabled. The IDLE timer is loaded with a value of 256 and is clocked with the t_C instruction cycle clock. The t_C clock is derived by dividing the oscillator clock down by a factor of 10. The Schmitt trigger following the CKI inverter on the chip ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

If an RC clock option is being used, the fixed delay is introduced optionally. A control bit, CLKDLY, mapped as configuration bit G7, controls whether the delay is to be introduced or not. The delay is included if CLKDLY is set, and excluded if CLKDLY is reset. The CLKDLY bit is cleared on reset.

Power Save Modes (Continued)

The devices have two mask options associated with the HALT mode. The first mask option enables the HALT mode feature, while the second mask option disables the HALT mode. With the HALT mode enable mask option, the device will enter and exit the HALT mode as described above. With the HALT disable mask option, the device cannot be placed in the HALT mode (writing a "1" to the HALT flag will have no effect).

The WATCHDOG detector circuit is inhibited during the HALT mode. However, the clock monitor circuit if enabled remains active during HALT mode in order to ensure a clock monitor error if the device inadvertently enters the HALT mode as a result of a runaway program or power glitch.

IDLE MODE

The device is placed in the IDLE mode by writing a "1" to the IDLE flag (G6 data bit). In this mode, all activities, except the associated on-board oscillator circuitry, the WATCHDOG logic, the clock monitor and the IDLE Timer T0, are stopped. The power supply requirements of the micro-controller in this mode of operation are typically around 30% of normal power requirement of the microcontroller.

As with the HALT mode, the device can be returned to normal operation with a reset, or with a Multi-Input Wakeup from the L Port. Alternately, the microcontroller resumes normal operation from the IDLE mode when the thirteenth bit (representing 4.096 ms at internal clock frequency of 1 MHz, t_c = 1 μs) of the IDLE Timer toggles.

This toggle condition of the thirteenth bit of the IDLE Timer T0 is latched into the T0PND pending flag.

The user has the option of being interrupted with a transition on the thirteenth bit of the IDLE Timer T0. The interrupt can be enabled or disabled via the T0EN control bit. Setting the T0EN flag enables the interrupt and vice versa.

The user can enter the IDLE mode with the Timer T0 interrupt enabled. In this case, when the T0PND bit gets set, the device will first execute the Timer T0 interrupt service routine and then return to the instruction following the "Enter Idle Mode" instruction.

Alternatively, the user can enter the IDLE mode with the IDLE Timer T0 interrupt disabled. In this case, the device will resume normal operation with the instruction immediately following the "Enter IDLE Mode" instruction.

Note: It is necessary to program two NOP instructions following both the set HALT mode and set IDLE mode instructions. These NOP instructions are necessary to allow clock resynchronization following the HALT or IDLE modes.

Multi-Input Wakeup

The Multi-Input Wakeup feature is ued to return (wakeup) the device from either the HALT or IDLE modes. Alternately Multi-Input Wakeup/Interrupt feature may also be used to generate up to 8 edge selectable external interrupts.

Figure 10 shows the Multi-Input Wakeup logic for the COP888CG microcontroller.

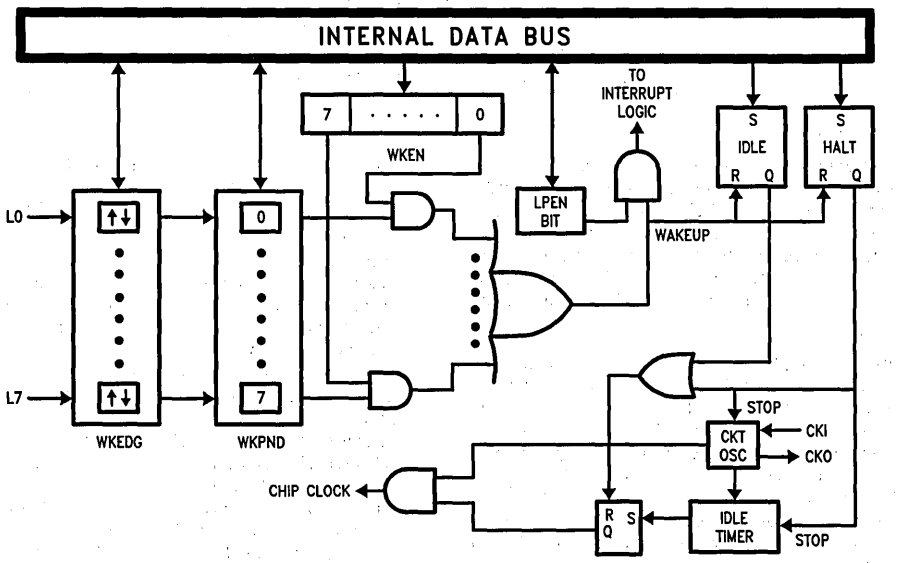

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FIGURE 10. Multi-Input Wake Up Logic

Multi-Input Wakeup (Continued)

The Multi-Input Wakeup feature utilizes the L Port. The user selects which particular L port bit (or combination of L Port bits) will cause the device to exit the HALT or IDLE modes. The selection is done through the Reg: WKEN. The Reg: WKEN is an 8-bit read/write register, which contains a control bit for every L port bit. Setting a particular WKEN bit enables a Wakeup from the associated L port pin.

The user can select whether the trigger condition on the selected L Port pin is going to be either a positive edge (low to high transition) or a negative edge (high to low transition). This selection is made via the Reg: WKEDG, which is an 8-bit control register with a bit assigned to each L Port pin. Setting the control bit will select the trigger condition to be a negative edge on that particular L Port pin. Resetting the bit selects the trigger condition to be a positive edge. Changing an edge select entails several steps in order to avoid a pseudo Wakeup condition as a result of the edge change. First, the associated WKEN bit should be reset, followed by the edge select change in WKEDG. Next, the associated WKPND bit should be cleared, followed by the associated WKEN bit being re-enabled.

An example may serve to clarify this procedure. Suppose we wish to change the edge select from positive (low going high) to negative (high going low) for L Port bit 5, where bit 5 has previously been enabled for an input interrupt. The program would be as follows:

```
RBIT  5, WKEN
SBIT  5, WKEDG
RBIT  5, WKPND
SBIT  5, WKEN
```

If the L port bits have been used as outputs and then changed to inputs with Multi-Input Wakeup/Interrupt, a safety procedure should also be followed to avoid inherited pseudo wakeup conditions. After the selected L port bits have been changed from output to input but before the associated WKEN bits are enabled, the associated edge select bits in WKEDG should be set or reset for the desired edge selects, followed by the associated WKPND bits being cleared.

This same procedure should be used following reset, since the L port inputs are left floating as a result of reset.

The occurrence of the selected trigger condition for Multi-Input Wakeup is latched into a pending register called WKPND. The respective bits of the WKPND register will be set on the occurrence of the selected trigger edge on the corresponding Port L pin. The user has the responsibility of clearing these pending flags. Since WKPND is a pending register for the occurrence of selected wakeup conditions, the device will not enter the HALT mode if any Wakeup bit is both enabled and pending. Consequently, the user has the responsibility of clearing the pending flags before attempting to enter the HALT mode.

WKEN, WKPND and WKEDG are all read/write registers, and are cleared at reset.

PORT L INTERRUPTS

Port L provides the user with an additional eight fully selectable, edge sensitive interrupts which are all vectored into the same service subroutine.

The interrupt from Port L shares logic with the wake up circuitry. The register WKEN allows interrupts from Port L to be individually enabled or disabled. The register WKEDG specifies the trigger condition to be either a positive or a negative edge. Finally, the register WKPND latches in the pending trigger conditions.

The GIE (Global Interrupt Enable) bit enables the interrupt function.

A control flag, LPEN, functions as a global interrupt enable for Port L interrupts. Setting the LPEN flag will enable interrupts and vice versa. A separate global pending flag is not needed since the register WKPND is adequate.

Since Port L is also used for waking the device out of the HALT or IDLE modes, the user can elect to exit the HALT or IDLE modes either with or without the interrupt enabled. If he elects to disable the interrupt, then the device will restart execution from the instruction immediately following the instruction that placed the microcontroller in the HALT or IDLE modes. In the other case, the device will first execute the interrupt service routine and then revert to normal operation.

The Wakeup signal will not start the chip running immediately since crystal oscillators or ceramic resonators have a finite start up time. The IDLE Timer (T0) generates a fixed delay to ensure that the oscillator has indeed stabilized before allowing the device to execute instructions. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry and the IDLE Timer T0 are enabled. The IDLE Timer is loaded with a value of 256 and is clocked from the t_C instruction cycle clock. The t_C clock is derived by dividing down the oscillator clock by a factor of 10. A Schmitt trigger following the CKI on-chip inverter ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

If the RC clock option is used, the fixed delay is under software control. A control flag, CLKDLY, in the G7 configuration bit allows the clock start up delay to be optionally inserted. Setting CLKDLY flag high will cause clock start up delay to be inserted and resetting it will exclude the clock start up delay. The CLKDLY flag is cleared during reset, so the clock start up delay is not present following reset with the RC clock options.

UART

The COP888CG contains a full-duplex software programmable UART. The UART *(Figure 11)* consists of a transmit shift register, a receiver shift register and seven addressable registers, as follows: a transmit buffer register (TBUF), a receiver buffer register (RBUF), a UART control and status register (ENU), a UART receive control and status register (ENUR), a UART interrupt and clock source register (ENUI), a prescaler select register (PSR) and baud (BAUD) register. The ENU register contains flags for transmit and receive functions; this register also determines the length of the data frame (7, 8 or 9 bits), the value of the ninth bit in transmission, and parity selection bits. The ENUR register flags framming, data overrun and parity errors while the UART is receiving.

Other functions of the ENUR register include saving the ninth bit received in the data frame, enabling or disabling the UART's attention mode of operation and providing additional receiver/transmitter status information via RCVG and XMTG bits. The determination of an internal or external clock source is done by the ENUI register, as well as selecting the number of stop bits and enabling or disabling transmit and receive interrupts. A control flag in this register can also select the UART mode of operation: asynchronous or synchronous.

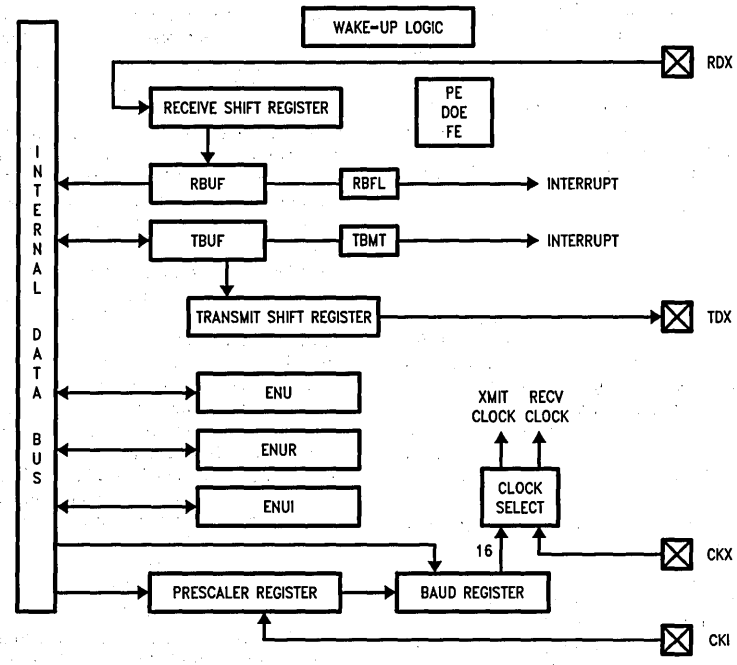

FIGURE 11. UART Block Diagram

UART (Continued)

UART CONTROL AND STATUS REGISTERS

The operation of the UART is programmed through three registers: ENU, ENUR and ENUI. The function of the individual bits in these registers is as follows:

ENU-UART Control and Status Register (Address at 0BA)

PEN	PSEL1	XBIT9/ PSEL0	CHL1	CHL0	ERR	RBFL	TBMT
0RW	0RW	0RW	0RW	0RW	0R	0R	1R

Bit 7 Bit 0

ENUR-UART Receive Control and Status Register (Address at 0BB)

DOE	FE	PE	SPARE	RBIT9	ATTN	XMTG	RCVG
0RD	0RD	0RD	0RW*	0R	0RW	0R	0R

Bit7 Bit0

ENUI-UART Interrupt and Clock Source Register (Address at 0BC)

STP2	STP78	ETDX	SSEL	XRCLK	XTCLK	ERI	ETI
0RW	0RW	0RW	0RW	0RW	0RW	0RW	0RW

Bit7 Bit0

*Bit is not used.

0 Bit is cleared on reset.

1 Bit is set to one on reset.

R Bit is read-only; it cannot be written by software.

RW Bit is read/write.

D Bit is cleared on read; when read by software as a one, it is cleared automatically. Writing to the bit does not affect its state.

DESCRIPTION OF UART REGISTER BITS

ENU—UART CONTROL AND STATUS REGISTER

TBMT: This bit is set when the UART transfers a byte of data from the TBUF register into the TSFT register for transmission. It is automatically reset when software writes into the TBUF register.

RBFL: This bit is set when the UART has received a complete character and has copied it into the RBUF register. It is automatically reset when software reads the character from RBUF.

ERR: This bit is a global UART error flag which gets set if any or a combination of the errors (DOE, FE, PE) occur.

CHL1, CHL0: These bits select the character frame format. Parity is not included and is generated/verified by hardware.

CHL1 = 0, CHL0 = 0 The frame contains eight data bits.
CHL1 = 0, CHL0 = 1 The frame contains seven data bits.
CHL1 = 1, CHL0 = 0 The frame contains nine data bits.
CHL1 = 1, CHL0 = 1 Loopback Mode selected. Transmitter output internally looped back to receiver input. Nine bit framing format is used.

XBIT9/PSEL0: Programs the ninth bit for transmission when the UART is operating with nine data bits per frame. For seven or eight data bits per frame, this bit in conjunction with PSEL1 selects parity.

PSEL1, PSEL0: Parity select bits.

PSEL1 = 0, PSEL0 = 0 Odd Parity (if Parity enabled)
PSEL1 = 0, PSEL0 = 1 Even Parity (if Parity enabled)
PSEL1 = 1, PSEL0 = 0 Mark(1) (if Parity enabled)
PSEL1 = 1, PSEL0 = 1 Space(0) (if Parity enabled)

PEN: This bit enables/disables Parity (7- and 8-bit modes only).

PEN = 0 Parity disabled.
PEN = 1 Parity enabled.

ENUR—UART RECEIVE CONTROL AND STATUS REGISTER

RCVG: This bit is set high whenever a framing error occurs and goes low when RDX goes high.

XMTG: This bit is set to indicate that the UART is transmitting. It gets reset at the end of the last frame (end of last Stop bit).

ATTN: ATTENTION Mode is enabled while this bit is set. This bit is cleared automatically on receiving a character with data bit nine set.

RBIT9: Contains the ninth data bit received when the UART is operating with nine data bits per frame.

SPARE: Reserved for future use.

PE: Flags a Parity Error.

PE = 0 Indicates no Parity Error has been detected since the last time the ENUR register was read.
PE = 1 Indicates the occurrence of a Parity Error.

FE: Flags a Framing Error.

FE = 0 Indicates no Framing Error has been detected since the last time the ENUR register was read.
FE = 1 Indicates the occurrence of a Framing Error.

DOE: Flags a Data Overrun Error.

DOE = 0 Indicates no Data Overrun Error has been detected since the last time the ENUR register was read.
DOE = 1 Indicates the occurrence of a Data Overrun Error.

ENUI—UART INTERRUPT AND CLOCK SOURCE REGISTER

ETI: This bit enables/disables interrupt from the transmitter section.

ETI = 0 Interrupt from the transmitter is disabled.
ETI = 1 Interrupt from the transmitter is enabled.

ERI: This bit enables/disables interrupt from the receiver section.

ERI = 0 Interrupt from the receiver is disabled.
ERI = 1 Interrupt from the receiver is enabled.

XTCLK: This bit selects the clock source for the transmitter-section.

XTCLK = 0 The clock source is selected through the PSR and BAUD registers.
XTCLK = 1 Signal on CKX (L1) pin is used as the clock.

XRCLK: This bit selects the clock source for the receiver section.

XRCLK = 0 The clock source is selected through the PSR and BAUD registers.
XRCLK = 1 Signal on CKX (L1) pin is used as the clock.

SSEL: UART mode select.

SSEL = 0 Asynchronous Mode.
SSEL = 1 Synchronous Mode.

UART (Continued)

ETDX: TDX (UART Transmit Pin) is the alternate function assigned to Port L pin L2; it is selected by setting ETDX bit. To simulate line break generation, software should reset ETDX bit and output logic zero to TDX pin through Port L data and configuration registers.

STP78: This bit is set to program the last Stop bit to be 7/8th of a bit in length.

STP2: This bit programs the number of Stop bits to be transmitted.

STP2 = 0 One Stop bit transmitted.
STP2 = 1 Two Stop bits transmitted.

Associated I/O Pins

Data is transmitted on the TDX pin and received on the RDX pin. TDX is the alternate function assigned to Port L pin L2; it is selected by setting ETDX (in the ENUI register) to one. RDX is an inherent function of Port L pin L3, requiring no setup.

The baud rate clock for the UART can be generated on-chip, or can be taken from an external source. Port L pin L1 (CKX) is the external clock I/O pin. The CKX pin can be either an input or an output, as determined by Port L Configuration and Data registers (Bit 1). As an input, it accepts a clock signal which may be selected to drive the transmitter and/or receiver. As an output, it presents the internal Baud Rate Generator output.

UART Operation

The UART has two modes of operation: asynchronous mode and synchronous mode.

ASYNCHRONOUS MODE

This mode is selected by resetting the SSEL (in the ENUI register) bit to zero. The input frequency to the UART is 16 times the baud rate.

The TSFT and TBUF registers double-buffer data for transmission. While TSFT is shifting out the current character on the TDX pin, the TBUF register may be loaded by software with the next byte to be transmitted. When TSFT finishes transmitting the current character the contents of TBUF are transferred to the TSFT register and the Transmit Buffer Empty Flag (TBMT in the ENU register) is set. The TBMT flag is automatically reset by the UART when software loads a new character into the TBUF register. There is also the XMTG bit which is set to indicate that the UART is transmitting. This bit gets reset at the end of the last frame (end of last Stop bit). TBUF is a read/write register.

The RSFT and RBUF registers double-buffer data being received. The UART receiver continually monitors the signal on the RDX pin for a low level to detect the beginning of a Start bit. Upon sensing this low level, it waits for half a bit time and samples again. If the RDX pin is still low, the receiver considers this to be a valid Start bit, and the remaining bits in the character frame are each sampled a single time, at the mid-bit position. Serial data input on the RDX pin is shifted into the RSFT register. Upon receiving the complete character, the contents of the RSFT register are copied into the RBUF register and the Received Buffer Full Flag (RBFL) is set. RBFL is automatically reset when software reads the character from the RBUF register. RBUF is a read only register. There is also the RCVG bit which is set high when a framing error occurs and goes low once RDX goes high. TBMT, XMTG, RBFL and RCVG are read only bits.

SYNCHRONOUS MODE

In this mode data is transferred synchronously with the clock. Data is transmitted on the rising edge and received on the falling edge of the synchronous clock.

This mode is selected by setting SSEL bit in the ENUI register. The input frequency to the UART is the same as the baud rate.

When an external clock input is selected at the CKX pin, data transmit and receive are performed synchronously with this clock through TDX/RDX pins.

If data transmit and receive are selected with the CKX pin as clock output, the device generates the synchronous clock output at the CKX pin. The internal baud rate generator is used to produce the synchronous clock. Data transmit and receive are performed synchronously with this clock.

FRAMING FORMATS

The UART supports several serial framing formats *(Figure 12)*. The format is selected using control bits in the ENU, ENUR and ENUI registers.

The first format (1, 1a, 1b, 1c) for data transmission (CHL0 = 1, CHL1 = 0) consists of Start bit, seven Data bits (excluding parity) and 7/8, one or two Stop bits. In applications using parity, the parity bit is generated and verified by hardware.

The second format (CHL0 = 0, CHL1 = 0) consists of one Start bit, eight Data bits (excluding parity) and 7/8, one or two Stop bits. Parity bit is generated and verified by hardware.

The third format for transmission (CHL0 = 0, CHL1 = 1) consists of one Start bit, nine Data bits and 7/8, one or two Stop bits. This format also supports the UART "ATTENTION" feature. When operating in this format, all eight bits of TBUF and RBUF are used for data. The ninth data bit is transmitted and received using two bits in the ENU and ENUR registers, called XBIT9 and RBIT9. RBIT9 is a read only bit. Parity is not generated or verified in this mode.

For any of the above framing formats, the last Stop bit can be programmed to be 7/8th of a bit in length. If two Stop bits are selected and the 7/8th bit is set (selected), the second Stop bit will be 7/8th of a bit in length.

The parity is enabled/disabled by PEN bit located in the ENU register. Parity is selected for 7- and 8-bit modes only. If parity is enabled (PEN = 1), the parity selection is then performed by PSEL0 and PSEL1 bits located in the ENU register.

Note that the XBIT9/PSEL0 bit located in the ENU register serves two mutually exclusive functions. This bit programs the ninth bit for transmission when the UART is operating with nine data bits per frame. There is no parity selection in this framing format. For other framing formats XBIT9 is not needed and the bit is PSEL0 used in conjunction with PSEL1 to select parity.

The frame formats for the receiver differ from the transmitter in the number of Stop bits required. The receiver only requires one Stop bit in a frame, regardless of the setting of the Stop bit selection bits in the control register. Note that an implicit assumption is made for full duplex UART operation that the framing formats are the same for the transmitter and receiver.

UART Operation (Continued)

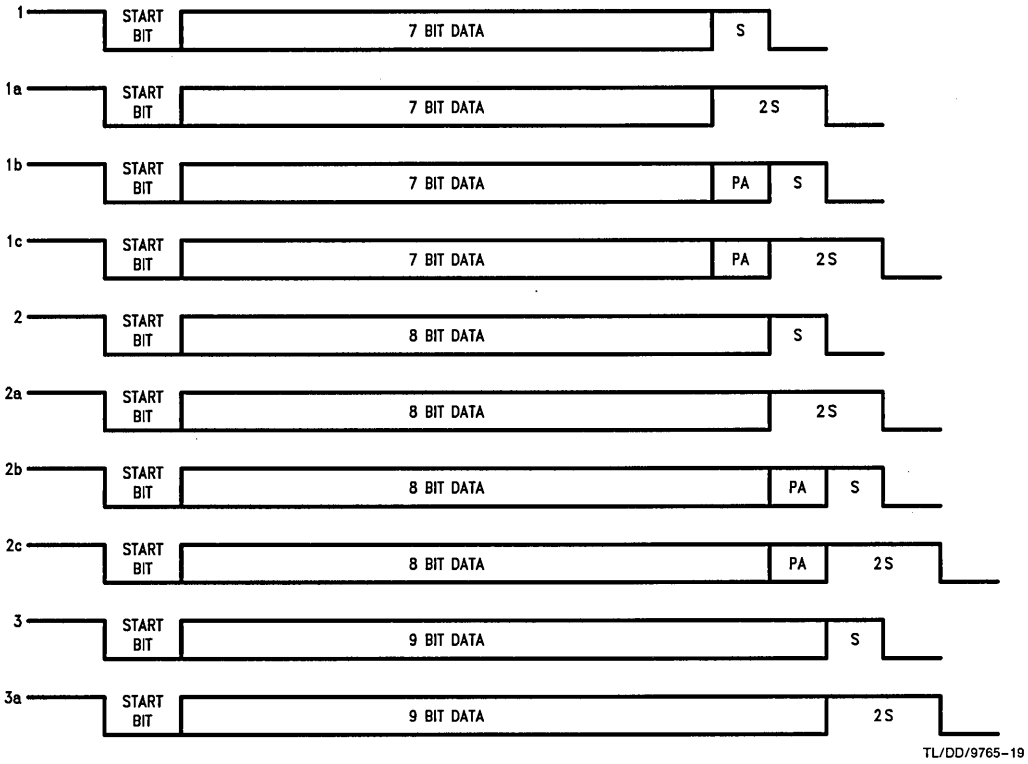

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FIGURE 12. Framing Formats

UART INTERRUPTS

The UART is capable of generating interrupts. Interrupts are generated on Receive Buffer Full and Transmit Buffer Empty. Both interrupts have individual interrupt vectors. Two bytes of program memory space are reserved for each interrupt vector. The two vectors are located at addresses 0xEC to 0xEF Hex in the program memory space. The interrupts can be individually enabled or disabled using Enable Transmit Interrupt (ETI) and Enable Receive Interrupt (ERI) bits in the ENUI register.

The interrupt from the Transmitter is set pending, and remains pending, as long as both the TBMT and ETI bits are set. To remove this interrupt, software must either clear the ETI bit or write to the TBUF register (thus clearing the TBMT bit).

The interrupt from the receiver is set pending, and remains pending, as long as both the RBFL and ERI bits are set. To remove this interrupt, software must either clear the ERI bit or read from the RBUF register (thus clearing the RBFL bit).

Baud Clock Generation

The clock inputs to the transmitter and receiver sections of the UART can be individually selected to come either from an external source at the CKX pin (port L, pin L1) or from a source selected in the PSR and BAUD registers. Internally, the basic baud clock is created from the oscillator frequency through a two-stage divider chain consisting of a 1–16 (increments of 0.5) prescaler and an 11-bit binary counter. *(Figure 13)* The divide factors are specified through two read/write registers shown in *Figure 14*. Note that the 11-bit Baud Rate Divisor spills over into the Prescaler Select Register (PSR). PSR is cleared upon reset.

As shown in Table I, a Prescaler Factor of 0 corresponds to NO CLOCK. NO CLOCK condition is the UART power down mode where the UART clock is turned off for power saving purpose. The user must also turn the UART clock off when a different baud rate is chosen.

The correspondences between the 5-bit Prescaler Select and Prescaler factors are shown in Table I. Therer are many ways to calculate the two divisor factors, but one particularly effective method would be to achieve a 1.8432 MHz frequency coming out of the first stage. The 1.8432 MHz prescaler output is then used to drive the software programmable baud rate counter to create a x16 clock for the following baud rates: 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19200 and 38400 (Table II). Other baud rates may be created by using appropriate divisors. The x16 clock is then divided by 16 to provide the rate for the serial shift registers of the transmitter and receiver.

Baud Clock Generation (Continued)

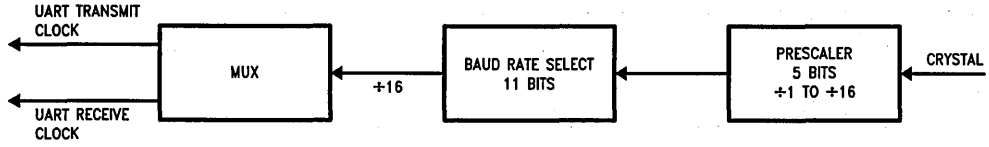

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FIGURE 13. UART BAUD Clock Generation

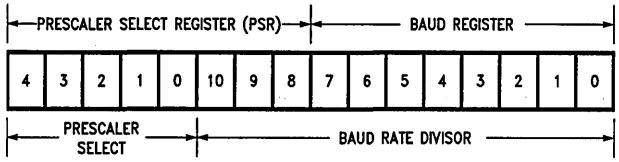

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FIGURE 14. UART BAUD Clock Divisor Registers

TABLE I. Prescaler Factors

Prescaler Select	Prescaler Factor
00000	NO CLOCK
00001	1
00010	1.5
00011	2
00100	2.5
00101	3
00110	3.5
00111	4
01000	4.5
01001	5
01010	5.5
01011	6
01100	6.5
01101	7
01110	7.5
01111	8
10000	8.5
10001	9
10010	9.5
10011	10
10100	10.5
10101	11
10110	11.5
10111	12
11000	12.5
11001	13
11010	13.5
11011	14
11100	14.5
11101	15
11110	15.5
11111	16

TABLE II. Baud Rate Divisors (1.8432 MHz Prescaler Output)

Baud Rate	Baud Rate Divisor − 1 (N-1)
110 (110.03)	1046
134.5 (134.58)	855
150	767
300	383
600	191
1200	95
1800	63
2400	47
3600	31
4800	23
7200	15
9600	11
19200	5
38400	2

The entries in Table II assume a prescaler output of 1.8432 MHz. In the asynchronous mode the baud rate could be as high as 625k.

As an example, considering the Asynchronous Mode and a CKI clock of 4.608 MHz, the prescaler factor selected is:

$$4.608/1.8432 = 2.5$$

The 2.5 entry is available in Table I. The 1.8432 MHz prescaler output is then used with proper Baud Rate Divisor (Table II) to obtain different baud rates. For a baud rate of 19200 e.g., the entry in Table II is 5.

$N - 1 = 5$ ($N - 1$ is the value from Table II)

$N = 6$ (N is the Baud Rate Divisor)

$$\text{Baud Rate} = 1.8432\ \text{MHz}/(16 \times 6) = 19200$$

The divide by 16 is performed because in the asynchronous mode, the input frequency to the UART is 16 times the baud rate. The equation to calculate baud rates is given below.

The actual Baud Rate may be found from:

$$BR = Fc/(16 \times N \times P)$$

Baud Clock Generation (Continued)

Where:

BR is the Baud Rate

Fc is the CKI frequency

N is the Baud Rate Divisor (Table II).

P is the Prescaler Divide Factor selected by the value in the Prescaler Select Register (Table I)

Note: In the Synchronous Mode, the divisor 16 is replaced by two.

Example:

Asynchronous Mode:

Crystal Frequency = 5 MHz

Desired baud rate = 9600

Using the above equation N × P can be calculated first.

$$N \times P = (5 \times 10^6)/(16 \times 9600) = 32.552$$

Now 32.552 is divided by each Prescaler Factor (Table II) to obtain a value closest to an integer. This factor happens to be 6.5 (P = 6.5).

$$N = 32.552/6.5 = 5.008 \ (N = 5)$$

The programmed value (from Table II) should be 4 (N − 1).

Using the above values calculated for N and P:

$$BR = (5 \times 10^6)/(16 \times 5 \times 6.5) = 9615.384$$

$$\% \text{ error} = (9615.385 - 9600)/9600 = 0.16$$

Effect of HALT/IDLE

The UART logic is reinitialized when either the HALT or IDLE modes are entered. This reinitialization sets the TBMT flag and resets all read only bits in the UART control and status registers. Read/Write bits remain unchanged. The Transmit Buffer (TBUF) is not affected, but the Transmit Shift register (TSFT) bits are set to one. The receiver registers RBUF and RSFT are not affected.

The device will exit from the HALT/IDLE modes when the Start bit of a character is detected at the RDX (L3) pin. This feature is obtained by using the Multi-Input Wakeup scheme provided on the device.

Before entering the HALT or IDLE modes the user program must select the Wakeup source to be on the RDX pin. This selection is done by setting bit 3 of WKEN (Wakeup Enable) register. The Wakeup trigger condition is then selected to be high to low transition. This is done via the WKEDG register (Bit 3 is zero.)

If the device is halted and crystal oscillator is used, the Wakeup signal will not start the chip running immediately because of the finite start up time requirement of the crystal oscillator. The idle timer (T0) generates a fixed delay to ensure that the oscillator has indeed stabilized before allowing the device to execute code. The user has to consider this delay when data transfer is expected immediately after exiting the HALT mode.

Diagnostic

Bits CHARL0 and CHARL1 in the ENU register provide a loopback feature for diagnostic testing of the UART. When these bits are set to one, the following occur: The receiver input pin (RDX) is internally connected to the transmitter output pin (TDX); the output of the Transmitter Shift Register is "looped back" into the Receive Shift Register input. In this mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and receive data paths of the UART.

Note that the framing format for this mode is the nine bit format; one Start bit, nine data bits, and 7/8, one or two Stop bits. Parity is not generated or verified in this mode.

Attention Mode

The UART Receiver section supports an alternate mode of operation, referred to as ATTENTION Mode. This mode of operation is selected by the ATTN bit in the ENUR register. The data format for transmission must also be selected as having nine Data bits and either 7/8, one or two Stop bits.

The ATTENTION mode of operation is intended for use in networking the device with other processors. Typically in such environments the messages consists of device addresses, indicating which of several destinations should receive them, and the actual data. This Mode supports a scheme in which addresses are flagged by having the ninth bit of the data field set to a 1. If the ninth bit is reset to a zero the byte is a Data byte.

While in ATTENTION mode, the UART monitors the communication flow, but ignores all characters until an address character is received. Upon receiving an address character, the UART signals that the character is ready by setting the RBFL flag, which in turn interrupts the processor if UART Receiver interrupts are enabled. The ATTN bit is also cleared automatically at this point, so that data characters as well as address characters are recognized. Software examines the contents of the RBUF and responds by deciding either to accept the subsequent data stream (by leaving the ATTN bit reset) or to wait until the next address character is seen (by setting the ATTN bit again).

Operation of the UART Transmitter is not affected by selection of this Mode. The value of the ninth bit to be transmitted is programmed by setting XBIT9 appropriately. The value of the ninth bit received is obtained by reading RBIT9. Since this bit is located in ENUR register where the error flags reside, a bit operation on it will reset the error flags.

Comparators

The devices contain two differential comparators, each with a pair of inputs (positive and negative) and an output. Ports I1–I3 and I4–I6 are used for the comparators. The following is the Port I assignment:

- I1 Comparator1 negative input
- I2 Comparator1 positive input
- I3 Comparator1 output
- I4 Comparator2 negative input
- I5 Comparator2 positive input
- I6 Comparator2 output

A Comparator Select Register (CMPSL) is used to enable the comparators, read the outputs of the comparators internally, and enable the outputs of the comparators to the pins. Two control bits (enable and output enable) and one result bit are associated with each comparator. The comparator result bits (CMP1RD and CMP2RD) are read only bits which will read as zero if the associated comparator is not enabled. The Comparator Select Register is cleared with reset, resulting in the comparators being disabled. The comparators should also be disabled before entering either the HALT or IDLE modes in order to save power. The configuration of the CMPSL register is as follows:

Comparators (Continued)

CMPSL REGISTER (ADDRESS X'00B7)

The CMPSL register contains the following bits:

CMP1EN Enable comparator 1

CMP1RD Comparator 1 result (this is a read only bit, which will read as 0 if the comparator is not enabled)

CMP10E Selects pin I3 as comparator 1 output provided that CMPIEN is set to enable the comparator

CMP2EN Enable comparator 2

CMP2RD Comparator 2 result (this is a read only bit, which will read as 0 if the comparator is not enabled)

CMP20E Selects pin I6 as comparator 2 output provided that CMP2EN is set to enable the comparator

Unused	CMP20E	CMP2RD	CMP2EN	CMP10E	CMP1RD	CMP1EN	Unused
Bit 7							Bit 0

Note that the two unused bits of CMPSL may be used as software flags.

Comparator outputs have the same spec as Ports L and G except that the rise and fall times are symmetrical.

Interrupts

The devices support a vectored interrupt scheme. It supports a total of fourteen interrupt sources. The following table lists all the possible device interrupt sources, their arbitration ranking and the memory locations reserved for the interrupt vector for each source.

Two bytes of program memory space are reserved for each interrupt source. All interrupt sources except the software interrupt are maskable. Each of the maskable interrupts have an Enable bit and a Pending bit. A maskable interrupt is active if its associated enable and pending bits are set. If GIE = 1 and an interrupt is active, then the processor will be interrupted as soon as it is ready to start executing an instruction except if the above conditions happen during the Software Trap service routine. This exception is described in the Software Trap sub-section.

The interruption process is accomplished with the INTR instruction (opcode 00), which is jammed inside the Instruction Register and replaces the opcode about to be executed. The following steps are performed for every interrupt:

1. The GIE (Global Interrupt Enable) bit is reset.
2. The address of the instruction about to be executed is pushed into the stack.
3. The PC (Program Counter) branches to address 00FF. This procedure takes 7 t_C cycles to execute.

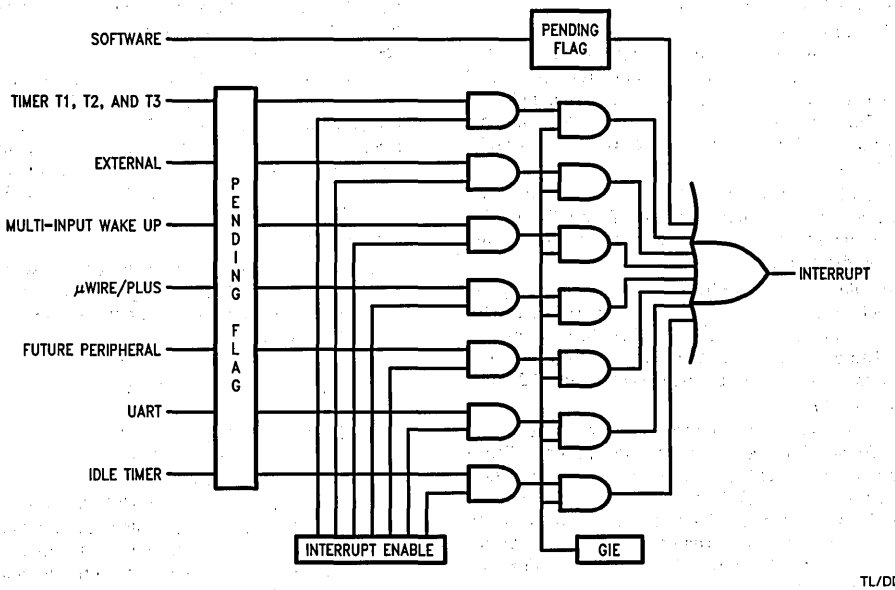

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FIGURE 15. Interrupt Block Diagram

Interrupts (Continued)

Arbitration Ranking	Source	Description	Vector Address Hi-Low Byte
(1) Highest	Software	INTR Instruction	0yFE–0yFF
	Reserved	for Future Use	0yFC–0yFD
(2)	External	Pin G0 Edge	0yFA–0yFB
(3)	Timer T0	Underflow	0yF8–0yF9
(4)	Timer T1	T1A/Underflow	0yF6–0yF7
(5)	Timer T1	T1B	0yF4–0yF5
(6)	MICROWIRE/PLUS	BUSY Goes Low	0yF2–0yF3
	Reserved	for Future Use	0yF0–0yF1
(7)	UART	Receive	0yEE–0yEF
(8)	UART	Transmit	0yEC–0yED
(9)	Timer T2	T2A/Underflow	0yEA–0yEB
(10)	Timer T2	T2B	0yE8–0yE9
(11)	Timer T3	T3A/Underflow	0yE6–0yE7
(12)	Timer T3	T3B	0yE4–0yE5
(13)	Port L/Wakeup	Port L Edge	0yE2–0yE3
(14) Lowest	Default	VIS Instr. Execution without Any Interrupts	0yE0–0yE1

y is VIS page, $y \neq 0$.

At this time, since GIE = 0, other maskable interrupts are disabled. The user is now free to do whatever context switching is required by saving the context of the machine in the stack with PUSH instructions. The user would then program a VIS (Vector Interrupt Select) instruction in order to branch to the interrupt service routine of the highest priority interrupt enabled and pending at the time of the VIS. Note that this is not necessarily the interrupt that caused the branch to address location 00FF Hex prior to the context switching.

Thus, if an interrupt with a higher rank than the one which caused the interruption becomes active before the decision of which interrupt to service is made by the VIS, then the interrupt with the higher rank will override any lower ones and will be acknowledged. The lower priority interrupt(s) are still pending, however, and will cause another interrupt immediately following the completion of the interrupt service routine associated with the higher priority interrupt just serviced. This lower priority interrupt will occur immediately following the RETI (Return from Interrupt) instruction at the end of the interrupt service routine just completed.

Inside the interrupt service routine, the associated pending bit has to be cleared by software. The RETI (Return from Interrupt) instruction at the end of the interrupt service routine will set the GIE (Global Interrupt Enable) bit, allowing the processor to be interrupted again if another interrupt is active and pending.

The VIS instruction looks at all the active interrupts at the time it is executed and performs an indirect jump to the beginning of the service routine of the one with the highest rank.

The addresses of the different interrupt service routines, called vectors, are chosen by the user and stored in ROM in a table starting at 01E0 (assuming that VIS is located between 00FF and 01DF). The vectors are 15-bit wide and therefore occupy 2 ROM locations.

VIS and the vector table must be located in the same 256-byte block (0y00 to 0yFF) except if VIS is located at the last address of a block. In this case, the table must be in the next block. The vector table cannot be inserted in the first 256-byte block ($y \neq 0$).

The vector of the maskable interrupt with the lowest rank is located at 0yE0 (Hi-Order byte) and 0yE1 (Lo-Order byte) and so forth in increasing rank number. The vector of the maskable interrupt with the highest rank is located at 0yFA (Hi-Order byte) and 0yFB (Lo-Order byte).

The Software Trap has the highest rank and its vector is located at 0yFE and 0yFF.

If, by accident, a VIS gets executed and no interrupt is active, then the PC (Program Counter) will branch to a vector located at 0yE0–0yE1. This vector can point to the Software Trap (ST) interrupt service routine, or to another special service routine as desired.

Figure 15 shows the Interrupt block diagram.

SOFTWARE TRAP

The Software Trap (ST) is a special kind of non-maskable interrupt which occurs when the INTR instruction (used to acknowledge interrupts) is fetched from ROM and placed inside the instruction register. This may happen when the PC is pointing beyond the available ROM address space or when the stack is over-popped.

Interrupts (Continued)

When an ST occurs, the user can re-initialize the stack pointer and do a recovery procedure (similar to reset, but not necessarily containing all of the same initialization procedures) before restarting.

The occurrence of an ST is latched into the ST pending bit. The GIE bit is not affected and the ST pending bit **(not accessible by the user)** is used to inhibit other interrupts and to direct the program to the ST service routine with the VIS instruction. The RPND instruction is used to clear the software interrupt pending bit. This pending bit is also cleared on reset.

The ST has the highest rank among all interrupts.

Nothing (except another ST) can interrupt an ST being serviced.

WATCHDOG

The devices contain a WATCHDOG and clock monitor. The WATCHDOG is designed to detect the user program getting stuck in infinite loops resulting in loss of program control or "runaway" programs. The Clock Monitor is used to detect the absence of a clock or a very slow clock below a specified rate on the CKI pin.

The WATCHDOG consists of two independent logic blocks: WD UPPER and WD LOWER. WD UPPER establishes the upper limit on the service window and WD LOWER defines the lower limit of the service window.

Servicing the WATCHDOG consists of writing a specific value to a WATCHDOG Service Register named WDSVR which is memory mapped in the RAM. This value is composed of three fields, consisting of a 2-bit Window Select, a 5-bit Key Data field, and the 1-bit Clock Monitor Select field. Table III shows the WDSVR register.

The lower limit of the service window is fixed at 2048 instruction cycles. Bits 7 and 6 of the WDSVR register allow the user to pick an upper limit of the service window.

Table IV shows the four possible combinations of lower and upper limits for the WATCHDOG service window. This flexibility in choosing the WATCHDOG service window prevents any undue burden on the user software.

Bits 5, 4, 3, 2 and 1 of the WDSVR register represent the 5-bit Key Data field. The key data is fixed at 01100. Bit 0 of the WDSVR Register is the Clock Monitor Select bit.

TABLE III. WATCHDOG Service Register (WDSVR)

Window Select		Key Data					Clock Monitor
X	X	0	1	1	0	0	Y
7	6	5	4	3	2	1	0

TABLE IV. WATCHDOG Service Window Select

WDSVR Bit 7	WDSVR Bit 6	Service Window (Lower-Upper Limits)
0	0	2k–8k t_C Cycles
0	1	2k–16k t_C Cycles
1	0	2k–32k t_C Cycles
1	1	2k–64k t_C Cycles

Clock Monitor

The Clock Monitor aboard the device can be selected or deselected under program control. The Clock Monitor is guaranteed not to reject the clock if the instruction cycle clock ($1/t_C$) is greater or equal to 10 kHz. This equates to a clock input rate on CKI of greater or equal to 100 kHz.

WATCHDOG Operation

The WATCHDOG and Clock Monitor are disabled during reset. The device comes out of reset with the WATCHDOG armed, the WATCHDOG Window Select bits (bits 6, 7 of the WDSVR Register) set, and the Clock Monitor bit (bit 0 of the WDSVR Register) enabled. Thus, a Clock Monitor error will occur after coming out of reset, if the instruction cycle clock frequency has not reached a minimum specified value, including the case where the oscillator fails to start.

The WDSVR register can be written to only once after reset and the key data (bits 5 through 1 of the WDSVR Register) must match to be a valid write. This write to the WDSVR register involves two irrevocable choices: (i) the selection of the WATCHDOG service window (ii) enabling or disabling of the Clock Monitor. Hence, the first write to WDSVR Register involves selecting or deselecting the Clock Monitor, select the WATCHDOG service window and match the WATCHDOG key data. Subsequent writes to the WDSVR register will compare the value being written by the user to the WATCHDOG service window value and the key data (bits 7 through 1) in the WDSVR Register. Table V shows the sequence of events that can occur.

The user must service the WATCHDOG at least once before the upper limit of the service window expires. The WATCHDOG may not be serviced more than once in every lower limit of the service window. The user may service the WATCHDOG as many times as wished in the time period between the lower and upper limits of the service window. The first write to the WDSVR Register is also counted as a WATCHDOG service.

The WATCHDOG has an output pin associated with it. This is the WDOUT pin, on pin 1 of the port G. WDOUT is active low. The WDOUT pin is in the high impedance state in the inactive state. Upon triggering the WATCHDOG, the logic will pull the WDOUT (G1) pin low for an additional 16 t_C–32 t_C cycles after the signal level on WDOUT pin goes below the lower Schmitt trigger threshold. After this delay, the device will stop forcing the WDOUT output low.

The WATCHDOG service window will restart when the WDOUT pin goes high. It is recommended that the user tie the WDOUT pin back to V_{CC} through a resistor in order to pull WDOUT high.

A WATCHDOG service while the WDOUT signal is active will be ignored. The state of the WDOUT pin is not guaranteed on reset, but if it powers up low then the WATCHDOG will time out and WDOUT will enter high impedance state.

The Clock Monitor forces the G1 pin low upon detecting a clock frequency error. The Clock Monitor error will continue until the clock frequency has reached the minimum specified value, after which the G1 output will enter the high impedance TRI-STATE mode following 16 t_C–32 t_C clock cycles. The Clock Monitor generates a continual Clock Monitor error if the oscillator fails to start, or fails to reach the minimum specified frequency. The specification for the Clock Monitor is as follows:

$1/t_C > 10$ kHz—No clock rejection.

$1/t_C < 10$ Hz—Guaranteed clock rejection.

Watchdog and Clock Monitor Summary

The following salient points regarding the COP888CG WATCHDOG and CLOCK MONITOR should be noted:

- Both the WATCHDOG and CLOCK MONITOR detector circuits are inhibited during RESET.
- Following RESET, the WATCHDOG and CLOCK MONITOR are both enabled, with the WATCHDOG having he maximum service window selected.
- The WATCHDOG service window and CLOCK MONITOR enable/disable option can only be changed once, during the initial WATCHDOG service following RESET.
- The initial WATCHDOG service must match the key data value in the WATCHDOG Service register WDSVR in order to avoid a WATCHDOG error.
- Subsequent WATCHDOG services must match all three data fields in WDSVR in order to avoid WATCHDOG errors.
- The correct key data value cannot be read from the WATCHDOG Service register WDSVR. Any attempt to read this key data value of 01100 from WDSVR will read as key data value of all 0's.
- The WATCHDOG detector circuit is inhibited during both the HALT and IDLE modes.
- The CLOCK MONITOR detector circuit is active during both the HALT and IDLE modes. Consequently, the COP888 inadvertently entering the HALT mode will be detected as a CLOCK MONITOR error (provided that the CLOCK MONITOR enable option has been selected by the program).
- With the single-pin R/C oscillator mask option selected and the CLKDLY bit reset, the WATCHDOG service window will resume following HALT mode from where it left off before entering the HALT mode.
- With the crystal oscillator mask option selected, or with the single-pin R/C oscillator mask option selected and the CLKDLY bit set, the WATCHDOG service window will be set to its selected value from WDSVR following HALT. Consequently, the WATCHDOG should not be serviced for at least 2048 instruction cycles following HALT, but must be serviced within the selected window to avoid a WATCHDOG error.
- The IDLE timer T0 is not initialized with RESET.
- The user can sync in to the IDLE counter cycle with an IDLE counter (T0) interrupt or by monitoring the T0PND flag. The T0PND flag is set whenever the thirteenth bit of the IDLE counter toggles (every 4096 instruction cycles). The user is responsible for resetting the T0PND flag.
- A hardware WATCHDOG service occurs just as the device exits the IDLE mode. Consequently, the WATCHDOG should not be serviced for at least 2048 instruction cycles following IDLE, but must be serviced within the selected window to avoid a WATCHDOG error.
- Following RESET, the initial WATCHDOG service (where the service window and the CLOCK MONITOR enable/disable must be selected) may be programmed anywhere within the maximum service window (65,536 instruction cycles) initialized by RESET. Note that this initial WATCHDOG service may be programmed within the initial 2048 instruction cycles without causing a WATCHDOG error.

Detection of Illegal Conditions

The device can detect various illegal conditions resulting from coding errors, transient noise, power supply voltage drops, runaway programs, etc.

Reading of undefined ROM gets zeros. The opcode for software interrupt is zero. If the program fetches instructions from undefined ROM, this will force a software interrupt, thus signaling that an illegal condition has occurred.

The subroutine stack grows down for each call (jump to subroutine), interrupt, or PUSH, and grows up for each return or POP. The stack pointer is initialized to RAM location 06F Hex during reset. Consequently, if there are more returns than calls, the stack pointer will point to addresses 070 and 071 Hex (which are undefined RAM). Undefined RAM from addresses 070 to 07F (Segment 0), 140 to 17F (Segment 1), and all other segments (i.e., Segments 3 . . . etc.) is read as all 1's, which in turn will cause the program to return to address 7FFF Hex. This is an undefined ROM location and the instruction fetched (all 0's) from this location will generate a software interrupt signaling an illegal condition.

Thus, the chip can detect the following illegal conditions:

a. Executing from undefined ROM

b. Over "POP"ing the stack by having more returns than calls.

When the software interrupt occurs, the user can re-initialize the stack pointer and do a recovery procedure before restarting (this recovery program is probably similar to that following reset, but might not contain the same program initialization procedures). The recovery program should reset the software interrupt pending bit using the RPND instruction.

MICROWIRE/PLUS

MICROWIRE/PLUS is a serial synchronous communications interface. The MICROWIRE/PLUS capability enables the device to interface with any of National Semiconductor's MICROWIRE peripherals (i.e. A/D converters, display drivers, E²PROMs etc.) and with other microcontrollers which support the MICROWIRE interface. It consists of an 8-bit serial shift register (SIO) with serial data input (SI), serial data output (SO) and serial shift clock (SK). *Figure 12* shows a block diagram of the MICROWIRE/PLUS logic.

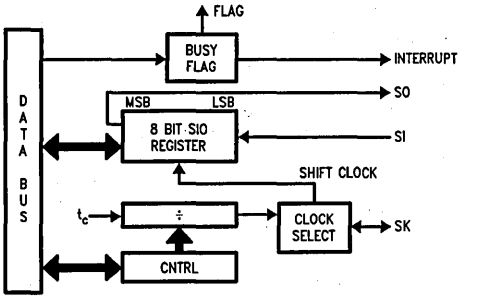

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FIGURE 16. MICROWIRE/PLUS Block Diagram

The shift clock can be selected from either an internal source or an external source. Operating the MICROWIRE/PLUS arrangement with the internal clock source is called the Master mode of operation. Similarly, operating the MICROWIRE/PLUS arrangement with an external shift clock is called the Slave mode of operation.

The CNTRL register is used to configure and control the MICROWIRE/PLUS mode. To use the MICROWIRE/PLUS, the MSEL bit in the CNTRL register is set to one. In the master mode, the SK clock rate is selected by the two bits, SL0 and SL1, in the CNTRL register. Table VI details the different clock rates that may be selected.

TABLE V. WATCHDOG Service Actions

Key Data	Window Data	Clock Monitor	Action
Match	Match	Match	Valid Service: Restart Service Window
Don't Care	Mismatch	Don't Care	Error: Generate WATCHDOG Output
Mismatch	Don't Care	Don't Care	Error: Generate WATCHDOG Output
Don't Care	Don't Care	Mismatch	Error: Generate WATCHDOG Output

TABLE VI. MICROWIRE/PLUS Master Mode Clock Select

SL1	SL0	SK
0	0	$2 \times t_c$
0	1	$4 \times t_c$
1	x	$8 \times t_c$

Where t_c is the instruction cycle clock

MICROWIRE/PLUS (Continued)

MICROWIRE/PLUS OPERATION

Setting the BUSY bit in the PSW register causes the MICROWIRE/PLUS to start shifting the data. It gets reset when eight data bits have been shifted. The user may reset the BUSY bit by software to allow less than 8 bits to shift. If enabled, an interrupt is generated when eight data bits have been shifted. The device may enter the MICROWIRE/PLUS mode either as a Master or as a Slave. *Figure 13* shows how two devices, microcontrollers and several peripherals may be interconnected using the MICROWIRE/PLUS arrangements.

Warning:

The SIO register should only be loaded when the SK clock is low. Loading the SIO register while the SK clock is high will result in undefined data in the SIO register. SK clock is normally low when not shifting.

Setting the BUSY flag when the input SK clock is high in the MICROWIRE/PLUS slave mode may cause the current SK clock forthe SIO shift register to be narrow. For safety, the BUSY flag should only be set when the input SK clock is low.

MICROWIRE/PLUS Master Mode Operation

In the MICROWIRE/PLUS Master mode of operation the shift clock (SK) is generated internally by the device. The MICROWIRE Master always initiates all data exchanges. The MSEL bit in the CNTRL register must be set to enable the SO and SK functions onto the G Port. The SO and SK pins must also be selected as outputs by setting appropriate bits in the Port G configuration register. Table VII summarizes the bit settings required for Master mode of operation.

MICROWIRE/PLUS Slave Mode Operation

In the MICROWIRE/PLUS Slave mode of operation the SK clock is generated by an external source. Setting the MSEL bit in the CNTRL register enables the SO and SK functions onto the G Port. The SK pin must be selected as an input and the SO pin is selected as an output pin by setting and resetting the appropriate bit in the Port G configuration register. Table VII summarizes the settings required to enter the Slave mode of operation.

The user must set the BUSY flag immediately upon entering the Slave mode. This will ensure that all data bits sent by the Master will be shifted properly. After eight clock pulses the BUSY flag will be cleared and the sequence may be repeated.

Alternate SK Phase Operation

The device allows either the normal SK clock or an alternate phase SK clock to shift data in and out of the SIO register. In both the modes the SK is normally low. In the normal mode data is shifted in on the rising edge of the SK clock and the data is shifted out on the falling edge of the SK clock. The SIO register is shifted on each falling edge of the SK clock. In the alternate SK phase operation, data is shifted in on the falling edge of the SK clock and shifted out on the rising edge of the SK clock.

A control flag, SKSEL, allows either the normal SK clock or the alternate SK clock to be selected. Resetting SKSEL causes the MICROWIRE/PLUS logic to be clocked from the normal SK signal. Setting the SKSEL flag selects the alternate SK clock. The SKSEL is mapped into the G6 configuration bit. The SKSEL flag will power up in the reset condition, selecting the normal SK signal.

TABLE VII

This table assumes that the control flag MSEL is set.

G4 (SO) Config. Bit	G5 (SK) Config. Bit	G4 Fun.	G5 Fun.	Operation
1	1	SO	Int. SK	MICROWIRE/PLUS Master
0	1	TRI-STATE	Int. SK	MICROWIRE/PLUS Master
1	0	SO	Ext. SK	MICROWIRE/PLUS Slave
0	0	TRI-STATE	Ext. SK	MICROWIRE/PLUS Slave

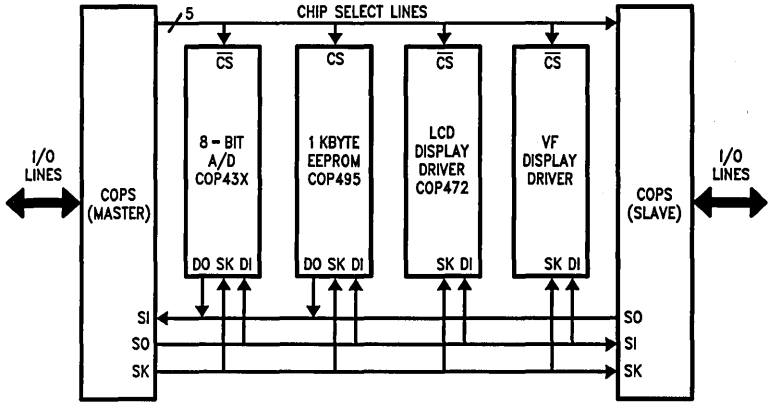

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FIGURE 17. MICROWIRE/PLUS Application

Memory Map

All RAM, ports and registers (except A and PC) are mapped into data memory address space.

Address S/ADD REG	Contents
0000 to 006F	On-Chip RAM bytes (112 bytes)
0070 to 007F	Unused RAM Address Space (Reads As All Ones)
xx80 to xxAF	Unused RAM Address Space (Reads Undefined Data)
xxB0	Timer T3 Lower Byte
XXB1	Timer T3 Upper Byte
xxB2	Timer T3 Autoload Register T3RA Lower Byte
xxB3	Timer T3 Autoload Register T3RA Upper Byte
xxB4	Timer T3 Autoload Register T3RB Lower Byte
xxB5	Timer T3 Autoload Register T3RB Upper Byte
xxB6	Timer T3 Control Register
xxB7	Comparator Select Register (CMPSL)
xxB8	UART Transmit Buffer (TBUF)
xxB9	UART Receive Buffer (RBUF)
xxBA	UART Control and Status Register (ENU)
xxBB	UART Receive Control and Status Register (ENUR)
xxBC	UART Interrupt and Clock Source Register (ENUI)
xxBD	UART Baud Register (BAUD)
xxBE	UART Prescale Select Register (PSR)
xxBF	Reserved for UART
xxC0	Timer T2 Lower Byte
xxC1	Timer T2 Upper Byte
xxC2	Timer T2 Autoload Register T2RA Lower Byte
xxC3	Timer T2 Autoload Register T2RA Upper Byte
xxC4	Timer T2 Autoload Register T2RB Lower Byte
xxC5	Timer T2 Autoload Register T2RB Upper Byte
xxC6	Timer T2 Control Register
xxC7	WATCHDOG Service Register (Reg:WDSVR)
xxC8	MIWU Edge Select Register (Reg:WKEDG)
xxC9	MIWU Enable Register (Reg:WKEN)
xxCA	MIWU Pending Register (Reg:WKPND)
xxCB	Reserved
xxCC	Reserved
xxCD to xxCF	Reserved

Address S/ADD REG	Contents
xxD0	Port L Data Register
xxD1	Port L Configuration Register
xxD2	Port L Input Pins (Read Only)
xxD3	Reserved for Port L
xxD4	Port G Data Register
xxD5	Port G Configuration Register
xxD6	Port G Input Pins (Read Only)
xxD7	Port I Input Pins (Read Only)
xxD8	Port C Data Register
xxD9	Port C Configuration Register
xxDA	Port C Input Pins (Read Only)
xxDB	Reserved for Port C
xxDC	Port D
xxDD to DF	Reserved for Port D
xxE0 to xxE5	Reserved for EE Control Registers
xxE6	Timer T1 Autoload Register T1RB Lower Byte
xxE7	Timer T1 Autoload Register T1RB Upper Byte
xxE8	ICNTRL Register
xxE9	MICROWIRE/PLUS Shift Register
xxEA	Timer T1 Lower Byte
xxEB	Timer T1 Upper Byte
xxEC	Timer T1 Autoload Register T1RA Lower Byte
xxED	Timer T1 Autoload Register T1RA Upper Byte
xxEE	CNTRL Control Register
xxEF	PSW Register
xxF0 to FB	On-Chip RAM Mapped as Registers
xxFC	X Register
xxFD	SP Register
xxFE	B Register
xxFF	S Register
0100–013F	On-Chip 64 RAM Bytes

Reading memory locations 0070H–007FH (Segment 0) will return all ones. Reading unused memory locations 0080H–00AFH (Segment 0) will return undefined data. Reading unused memory locations 0140–017F (Segment 1) will return all ones. Reading memory locations from other Segments (i.e., Segment 2, Segment 3, ... etc.) will return all ones.

Addressing Modes

There are ten addressing modes, six for operand addressing and four for transfer of control.

OPERAND ADDRESSING MODES

Register Indirect

This is the "normal" addressing mode. The operand is the data memory addressed by the B pointer or X pointer.

Register Indirect (with auto post increment or decrement of pointer)

This addressing mode is used with the LD and X instructions. The operand is the data memory addressed by the B pointer or X pointer. This is a register indirect mode that automatically post increments or decrements the B or X register after executing the instruction.

Direct

The instruction contains an 8-bit address field that directly points to the data memory for the operand.

Immediate

The instruction contains an 8-bit immediate field as the operand.

Short Immediate

This addressing mode is used with the Load B Immediate instruction. The instruction contains a 4-bit immediate field as the operand.

Indirect

This addressing mode is used with the LAID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a data operand from the program memory.

TRANSFER OF CONTROL ADDRESSING MODES

Relative

This mode is used for the JP instruction, with the instruction field being added to the program counter to get the new program location. JP has a range from −31 to +32 to allow a 1-byte relative jump (JP + 1 is implemented by a NOP instruction). There are no "pages" when using JP, since all 15 bits of PC are used.

Absolute

This mode is used with the JMP and JSR instructions, with the instruction field of 12 bits replacing the lower 12 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory segment.

Absolute Long

This mode is used with the JMPL and JSRL instructions, with the instruction field of 15 bits replacing the entire 15 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory space.

Indirect

This mode is used with the JID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a location in the program memory. The contents of this program memory location serve as a partial address (lower 8 bits of PC) for the jump to the next instruction.

Note: The VIS is a special case of the Indirect Transfer of Control addressing mode, where the double byte vector associated with the interrupt is transferred from adjacent addresses in the program memory into the program counter (PC) in order to jump to the associated interrupt service routine.

Instruction Set

Register and Symbol Definition

Registers	
A	8-Bit Accumulator Register
B	8-Bit Address Register
X	8-Bit Address Register
SP	8-Bit Stack Pointer Register
PC	15-Bit Program Counter Register
PU	Upper 7 Bits of PC
PL	Lower 8 Bits of PC
C	1 Bit of PSW Register for Carry
HC	1 Bit of PSW Register for Half Carry
GIE	1 Bit of PSW Register for Global Interrupt Enable
VU	Interrupt Vector Upper Byte
VL	Interrupt Vector Lower Byte

Symbols	
[B]	Memory Indirectly Addressed by B Register
[X]	Memory Indirectly Addressed by X Register
MD	Direct Addressed Memory
Mem	Direct Addressed Memory or [B]
Meml	Direct Addressed Memory or [B] or Immediate Data
Imm	8-Bit Immediate Data
Reg	Register Memory: Addresses F0 to FF (Includes B, X and SP)
Bit	Bit Number (0 to 7)
←	Loaded with
↔	Exchanged with

Instruction Set (Continued)

INSTRUCTION SET

ADD	A,Meml	ADD	A ← A + Meml
ADC	A,Meml	ADD with Carry	A ← A + Meml + C, C ← Carry HC ← Half Carry
SUBC	A,Meml	Subtract with Carry	A ← A − $\overline{\text{Meml}}$ + C, C ← Carry HC ← Half Carry
AND	A,Meml	Logical AND	A ← A and Meml
ANDSZ	A,Imm	Logical AND Immed., Skip if Zero	Skip next if (A and Imm) = 0
OR	A,Meml	Logical OR	A ← A or Meml
XOR	A,Meml	Logical EXclusive OR	A ← A xor Meml
IFEQ	MD,Imm	IF EQual	Compare MD and Imm, Do next if MD = Imm
IFEQ	A,Meml	IF EQual	Compare A and Meml, Do next if A = Meml
IFNE	A,Meml	IF Not Equal	Compare A and Meml, Do next if A ≠ Meml
IFGT	A,Meml	IF Greater Than	Compare A and Meml, Do next if A > Meml
IFBNE	#	If B Not Equal	Do next if lower 4 bits of B ≠ Imm
DRSZ	Reg	Decrement Reg., Skip if Zero	Reg ← Reg − 1, Skip if Reg = 0
SBIT	#,Mem	Set BIT	1 to bit, Mem (bit = 0 to 7 immediate)
RBIT	#,Mem	Reset BIT	0 to bit, Mem
IFBIT	#,Mem	IF BIT	If bit in A or Mem is true do next instruction
RPND		Reset PeNDing Flag	Reset Software Interrupt Pending Flag
X	A,Mem	EXchange A with Memory	A ⟷ Mem
X	A,[X]	EXchange A with Memory [X]	A ⟷ [X]
LD	A,Meml	LoaD A with Memory	A ← Meml
LD	A,[X]	LoaD A with Memory [X]	A ← [X]
LD	B,Imm	LoaD B with Immed.	B ← Imm
LD	Mem,Imm	LoaD Memory Immed	Mem ← Imm
LD	Reg,Imm	LoaD Register Memory Immed.	Reg ← Imm
X	A, [B ±]	EXchange A with Memory [B]	A ⟷ [B], (B ← B ±1)
X	A, [X ±]	EXchange A with Memory [X]	A ⟷ [X], (X ← ±1)
LD	A, [B±]	LoaD A with Memory [B]	A ← [B], (B ← B ±1)
LD	A, [X±]	LoaD A with Memory [X]	A ← [X], (X ← X±1)
LD	[B±],Imm	LoaD Memory [B] Immed.	[B] ← Imm, (B ← B±1)
CLR	A	CLeaR A	A ← 0
INC	A	INCrement A	A ← A + 1
DEC	A	DECrementA	A ← A − 1
LAID		Load A InDirect from ROM	A ← ROM (PU,A)
DCOR	A	Decimal CORrect A	A ← BCD correction of A (follows ADC, SUBC)
RRC	A	Rotate A Right thru C	C → A7 → ... → A0 → C
RLC	A	Rotate A Left thru C	C ← A7 ← ... ← A0 ← C
SWAP	A	SWAP nibbles of A	A7 ... A4 ⟷ A3 ... A0
SC		Set C	C ← 1, HC ← 1
RC		Reset C	C ← 0, HC ← 0
IFC		IF C	IF C is true, do next instruction
IFNC		IF Not C	If C is not true, do next instruction
POP	A	POP the stack into A	SP ← SP + 1, A ← [SP]
PUSH	A	PUSH A onto the stack	[SP] ← A, SP ← SP − 1
VIS		Vector to Interrupt Service Routine	PU ← [VU], PL ← [VL]
JMPL	Addr.	Jump absolute Long	PC ← ii (ii = 15 bits, 0 to 32k)
JMP	Addr.	Jump absolute	PC9 ... 0 ← i (i = 12 bits)
JP	Disp.	Jump relative short	PC ← PC + r (r is −31 to +32, except 1)
JSRL	Addr.	Jump SubRoutine Long	[SP] ← PL, [SP−1] ← PU,SP−2, PC ← ii
JSR	Addr	Jump SubRoutine	[SP] ← PL, [SP−1] ← PU,SP−2, PC9 ... 0 ← i
JID		Jump InDirect	PL ← ROM (PU,A)
RET		RETurn from subroutine	SP + 2, PL ← [SP], PU ← [SP−1]
RETSK		RETurn and SKip	SP + 2, PL ← [SP],PU ← [SP−1]
RETI		RETurn from Interrupt	SP + 2, PL ← [SP],PU ← [SP−1],GIE ← 1
INTR		Generate an Interrupt	[SP] ← PL, [SP−1] ← PU, SP−2, PC ← 0FF
NOP		No OPeration	PC ← PC + 1

Instruction Execution Time

Most instructions are single byte (with immediate addressing mode instructions taking two bytes).

Most single byte instructions take one cycle time to execute.

See the BYTES and CYCLES per INSTRUCTION table for details.

Bytes and Cycles per Instruction

The following table shows the number of bytes and cycles for each instruction in the format of byte/cycle.

	[B]	Direct	Immed.
ADD	1/1	3/4	2/2
ADC	1/1	3/4	2/2
SUBC	1/1	3/4	2/2
AND	1/1	3/4	2/2
OR	1/1	3/4	2/2
XOR	1/1	3/4	2/2
IFEQ	1/1	3/4	2/2
IFNE	1/1	3/4	2/2
IFGT	1/1	3/4	2/2
IFBNE	1/1		
DRSZ		1/3	
SBIT	1/1	3/4	
RBIT	1/1	3/4	
IFBIT	1/1	3/4	

RPND	1/1

Instructions Using A & C

CLRA	1/1
INCA	1/1
DECA	1/1
LAID	1/3
DCOR	1/1
RRCA	1/1
RLCA	1/1
SWAPA	1/1
SC	1/1
RC	1/1
IFC	1/1
IFNC	1/1
PUSHA	1/3
POPA	1/3
ANDSZ	2/2

Transfer of Control Instructions

JMPL	3/4
JMP	2/3
JP	1/3
JSRL	3/5
JSR	2/5
JID	1/3
VIS	1/5
RET	1/5
RETSK	1/5
RETI	1/5
INTR	1/7
NOP	1/1

Memory Transfer Instructions

	Register Indirect		Direct	Immed.	Register Indirect Auto Incr. & Decr.		
	[B]	[X]			[B+, B−]	[X+, X−]	
X A,*	1/1	1/3	2/3		1/2	1/3	
LD A,*	1/1	1/3	2/3	2/2	1/2	1/3	
LD B, Imm				1/1			(IF B < 16)
LD B, Imm				2/2			(IF B > 15)
LD Mem, Imm	2/2		3/3		2/2		
LD Reg, Imm			2/3				
IFEQ MD, Imm			3/3				

* = > Memory location addressed by B or X or directly.

7

Opcode Table

Upper Nibble Along X-Axis
Lower Nibble Along Y-Axis

F	E	D	C	B	A	9	8	
JP −15	JP −31	LD 0F0, # i	DRSZ 0F0	RRCA	RC	ADC A,#i	ADC A,[B]	0
JP −14	JP −30	LD 0F1, # i	DRSZ 0F1	*	SC	SUBC A, #i	SUB A,[B]	1
JP −13	JP −29	LD 0F2, # i	DRSZ 0F2	X A, [X+]	X A,[B+]	IFEQ A,#i	IFEQ A,[B]	2
JP −12	JP −28	LD 0F3, # i	DRSZ 0F3	X A, [X−]	X A,[B−]	IFGT A,#i	IFGT A,[B]	3
JP −11	JP −27	LD 0F4, # i	DRSZ 0F4	VIS	LAID	ADD A,#i	ADD A,[B]	4
JP −10	JP −26	LD 0F5, # i	DRSZ 0F5	RPND	JID	AND A,#i	AND A,[B]	5
JP −9	JP −25	LD 0F6, # i	DRSZ 0F6	X A,[X]	X A,[B]	XOR A,#i	XOR A,[B]	6
JP −8	JP −24	LD 0F7, # i	DRSZ 0F7	*	*	OR A,#i	OR A,[B]	7
JP −7	JP −23	LD 0F8, # i	DRSZ 0F8	NOP	RLCA	LD A,#i	IFC	8
JP −6	JP −22	LD 0F9, # i	DRSZ 0F9	IFNE A,[B]	IFEQ Md,#i	IFNE A,#i	IFNC	9
JP −5	JP −21	LD 0FA, # i	DRSZ 0FA	LD A,[X+]	LD A,[B+]	LD [B+],#i	INCA	A
JP −4	JP −20	LD 0FB, # i	DRSZ 0FB	LD A,[X−]	LD A,[B−]	LD [B−],#i	DECA	B
JP −3	JP −19	LD 0FC, # i	DRSZ 0FC	LD Md,#i	JMPL	X A,Md	POPA	C
JP −2	JP −18	LD 0FD, # i	DRSZ 0FD	DIR	JSRL	LD A,Md	RETSK	D
JP −1	JP −17	LD 0FE, # i	DRSZ 0FE	LD A,[X]	LD A,[B]	LD [B],#i	RET	E
JP −0	JP −16	LD 0FF, # i	DRSZ 0FF	*	*	LD B,#i	RETI	F

Opcode Table (Continued)

Upper Nibble Along X-Axis

Lower Nibble Along Y-Axis

7	6	5	4	3	2	1	0	
IFBIT 0,[B]	ANDSZ A, #I	LD B,#0F	IFBNE 0	JSR x000–x0FF	JMP x000–x0FF	JP +17	INTR	0
IFBIT 1,[B]	*	LD B,#0E	IFBNE 1	JSR x100–x1FF	JMP x100–x1FF	JP +18	JP + 2	1
IFBIT 2,[B]	*	LD B,#0D	IFBNE 2	JSR x200–x2FF	JMP x200–x2FF	JP +19	JP + 3	2
IFBIT 3,[B]	*	LD B,#0C	IFBNE 3	JSR x300–x3FF	JMP x300–x3FF	JP +20	JP + 4	3
IFBIT 4,[B]	CLRA	LD B,#0B	IFBNE 4	JSR x400–x4FF	JMP x400–x4FF	JP +21	JP + 5	4
IFBIT 5,[B]	SWAPA	LD B,#0A	IFBNE 5	JSR x500–x5FF	JMP x500–x5FF	JP +22	JP + 6	5
IFBIT 6,[B]	DCORA	LD B,#09	IFBNE 6	JSR x600–x6FF	JMP x600–x6FF	JP +23	JP + 7	6
IFBIT 7,[B]	PUSHA	LD B,#08	IFBNE 7	JSR x700–x7FF	JMP x700–x7FF	JP +24	JP + 8	7
SBIT 0,[B]	RBIT 0,[B]	LD B,#07	IFBNE 8	JSR x800–x8FF	JMP x800–x8FF	JP +25	JP + 9	8
SBIT 1,[B]	RBIT 1,[B]	LD B,#06	IFBNE 9	JSR x900–x9FF	JMP x900–x9FF	JP +26	JP + 10	9
SBIT 2,[B]	RBIT 2,[B]	LD B,#05	IFBNE 0A	JSR xA00–xAFF	JMP xA00–xAFF	JP +27	JP + 11	A
SBIT 3,[B]	RBIT 3,[B]	LD B,#04	IFBNE 0B	JSR xB00–xBFF	JMP xB00–xBFF	JP +28	JP + 12	B
SBIT 4,[B]	RBIT 4,[B]	LD B,#03	IFBNE 0C	JSR xC00–xCFF	JMP xC00–xCFF	JP +29	JP + 13	C
SBIT 5,[B]	RBIT 5,[B]	LD B,#02	IFBNE 0D	JSR xD00–xDFF	JMP xD00–xDFF	JP +30	JP + 14	D
SBIT 6,[B]	RBIT 6,[B]	LD B,#01	IFBNE 0E	JSR xE00–xEFF	JMP xE00–xEFF	JP +31	JP + 15	E
SBIT 7,[B]	RBIT 7,[B]	LD B,#00	IFBNE 0F	JSR xF00–xFFF	JMP xF00–xFFF	JP +32	JP + 16	F

Where,

i is the immediate data
Md is a directly addressed memory location
* is an unused opcode

Note: The opcode 60 Hex is also the opcode for IFBIT #i,A

Mask Options

The COP888CG mask programmable options are shown below. The options are programmed at the same time as the ROM pattern submission.

```
OPTION 1: CLOCK CONFIGURATION
  = 1     Crystal Oscillator (CKI/10)
              G7 (CKO) is clock generator
              output to crystal/resonator
              CKI is the clock input
  = 2     Single-pin RC controlled
              oscillator (CKI/10)
              G7 is available as a HALT
              restart and/or general purpose
              input
OPTION 2: HALT
  = 1     Enable HALT mode
  = 2     Disable HALT mode
OPTION 3: BONDING OPTIONS
  = 1     44-Pin PLCC
  = 2     40-Pin DIP
  = 3     N/A
  = 4     28-Pin DIP
```

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (if clock option-1 has been selected). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_C$).

Development Support

IN-CIRCUIT EMULATOR

The MetaLink iceMASTER™-COP8 Model 400 In-Circuit Emulator for the COP8 family of microcontrollers features high-performance operation, ease of use, and an extremely flexible user-interface or maximum productivity. Interchangeable probe cards, which connect to the standard common base, support the various configurations and packages of the COP8 family.

The iceMASTER provides real time, full speed emulation up to 10 MHz, 32 kBytes of emulation memory and 4k frames of trace buffer memory. The user may define as many as 32k trace and break triggers which can be enabled, disabled, set or cleared. They can be simple triggers based on code or address ranges or complex triggers based on code address, direct address, opcode value, opcode class or immediate operand. Complex breakpoints can be ANDed and ORed together. Trace information consists of address bus values, opcodes and user selectable probe clips status (external event lines). The trace buffer can be viewed as raw hex or as disassembled instructions. The probe clip bit values can be displayed in binary, hex or digital waveform formats.

During single-step operation the dynamically annotated code feature displays the contents of all accessed (read and write) memory locations and registers, as well as flow-of-control direction change markers next to each instruction executed.

The iceMASTER's performance analyzer offers a resolution of better than 6 μs. The user can easily monitor the time spent executing specific portions of code and find "hot spots" or "dead code". Up to 15 independent memory areas based on code address or label ranges can be defined. Analysis results can be viewed in bar graph format or as actual frequency count.

Emulator memory operations for program memory include single line assembler, disassembler, view, change and write to file. Data memory operations include fill, move, compare, dump to file, examine and modify. The contents of any memory space can be directly viewed and modified from the corresponding window.

The iceMASTER comes with an easy to use window interface. Each window can be sized, highlighted, color-controlled, added, or removed completely. Commands can be accessed via pull-down-menus and/or redefinable hot keys. A context sensitive hypertext/hyperlinked on-line help system explains clearly the options the user has from within any window.

The iceMASTER connects easily to a PC® via the standard COMM port and its 115.2 kBaud serial link keeps typical program download time to under 3 seconds.

The following tables list the emulator and probe cards ordering information.

Emulator Ordering Information

Part Number	Description
IM-COP8/400	MetaLink base unit in-circuit emulator for all COP8 devices, symbolic debugger software and RS-232 serial interface cable
MHW-PS3	Power supply 110V/60 MHz
MHW-PS4	Power supply 220V/50 Hz

Probe Card Ordering Information

Part Number	Package	Voltage Range	Emulates
MHW-884CG28D5PC	28 DIP	4.5V–5.5V	COP884CG
MHW-884CG28DWPC	28 DIP	2.5V–6.0V	COP884CG
MHW-888CG40D5PC	40 DIP	4.5V–5.5V	COP888CG
MHW-888CG40DWPC	40 DIP	2.5V–6.0V	COP888CG
MWH-888CG44D5PC	44 PLCC	4.5V–5.5V	COP888CG
MHW-888CG44DWPC	44 PLCC	2.5V–6.0V	COP888CG

MACRO CROSS ASSEMBLER

National Semiconductor offers a COP8 macro cross assembler. It runs on industry standard compatible PCs and supports all of the full-symbolic debugging features of the MetaLink iceMASTER emulators.

Assembler Ordering Information

Part Number	Description	Manual
MOLE-COP8-IBM	COP8 macro cross assembler for IBM®, PC-/XT®, PC-AT® or compatible	424410527-001

Development Support (Continued)

SIMULATOR

The COP8 Designer's Tool Kit is available for evaluating National Semiconductor's COP8 microcontroller family. The kit contains programmer's manuals, device datasheets, pocket reference guide, assembler and simulator, which allows the user to write, test, debug and run code on an industry standard compatible PC. The simulator has a windowed user interface and can handle script files that simulate hardware inputs, interrupts and automatic command processing. The capture file feature enables the user to record to a file current cycle count and output port changes which are caused by the program under test.

Simulator Ordering Information

Part Number	Description	Manual
COP8-TOOL-KIT	COP8 Designer's Tool Kit Assembler and Simulator	420420270-001 424420269-001

SINGLE CHIP EMULATOR DEVICE

The COP8 family is fully supported by single chip form, fit and function emulators. For more detailed information refer to the emulation device specific datasheets and the form, fit, function emulator selection table below.

PROGRAMMING SUPPORT

Programming of the single chip emulator devices is supported by different sources. National Semiconductor offers a duplicator board which allows the transfer of program code from a standard programmed EPROM to the single chip emulator and vice versa. Data I/O supports COP8 emulator device programming with its uniSite 48 and System 2900 programmers. Further information on Data I/O programmers can be obtained from any Data I/O sales office or the following USA numbers:

Telephone: (206) 881-6444 Fax: (206) 882-1043

Single Chip Emulator Selection Table

Device Number	Clock Option	Package	Description	Emulates
COP888CGMHEL-X	X = 1: crystal X = 3: R/C	44 LDCC	Multi-Chip Module (MCM), UV erasable	COP888CG
COP888CGMHD-X	X = 1: crystal X = 3: R/C	40 DIP	MCM, UV erasable	COP888CG
COP884CGMHD-X	X = 1: crystal X = 3: R/C	28 DIP	MCM, UV erasable	COP884CG

Duplicator Board Ordering Information

Part Number	Description	Devices Supported
COP8-PRGM-28D	Duplicator Board for 28 DIP Multi-Chip Module (MCM) and for use with Scrambler Boards	COP884CGMHD
COP8-SCRM-DIP	MCM Scrambler Board for 40 DIP socket	COP888CGMHD
COP8-SCRM-PCC	MCM Scrambler Board for 44 PLCC/LDCC	COP888CGMHEL
COP8-SCRM-SBX	MCM Scrambler board for 28 LCC socket	COP884CGMHEA
COP8-PRGM-DIP	Duplicator Board with COP8-SCRM-DIP scrambler board	COP884CGMHD, COP888CGMHD
COP8-PRGM-PCC	Duplicator Board with COP8-SCRM-PCC scrambler board	COP888CGMEL, COP884CGMHD

Development Support (Continued)

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications group. The Dial-A-Helper is an Electronic Bulletin Board Information system.

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down loaded to disk for later use.

ORDER P/N: MOLE-DIAL-A-HLP

Information System Package contains:
- Dial-A-Helper Users Manual
- Public Domain Communications Software

FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factor applications support. If a user has questions, he can leave messages on our electronic bulletin board, which we will respond to.

Voice: (408) 721-5582
Modem: (408) 739-1162
Baud: 300 or 1200 Baud
Set-up: Length: 8-Bit
Parity: None
Stop Bit: 1
Operation: 24 Hrs., 7 Days

National Semiconductor

COP688CL/COP684CL, COP888CL/COP884CL, COP988CL/COP984CL Single-Chip microCMOS Microcontroller

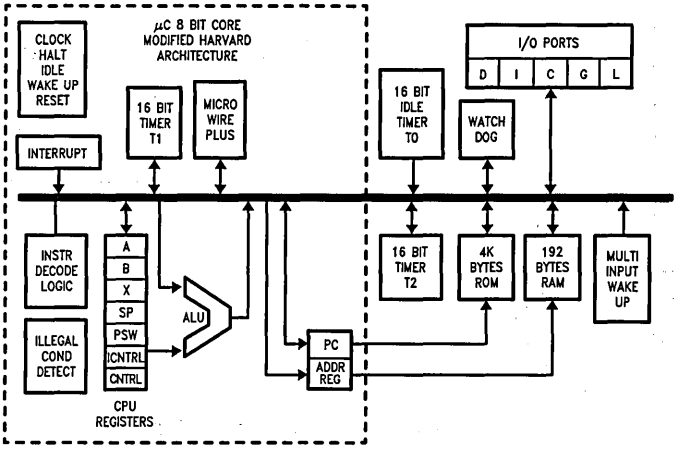
General Description

The COP888 family of microcontrollers uses an 8-bit single chip core architecture fabricated with National Semiconductor's M²CMOS™ process technology. The COP888CL is a member of this expandable 8-bit core processor family of microcontrollers. (Continued)

Features

- Low cost 8-bit microcontroller
- Fully static CMOS, with low current drain
- Two power saving modes: HALT and IDLE
- 1 μs instruction cycle time
- 4096 bytes on-board ROM
- 128 bytes on-board RAM
- Single supply operation: 2.5V–6V
- MICROWIRE/PLUS™ serial I/O
- WATCHDOG™ and Clock Monitor logic
- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- Ten multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Timers TA, TB (Each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS
- Two 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers (B and X)
- Versatile instruction set
- True bit manipulation
- Memory mapped I/O
- BCD arithmetic instructions
- Package: 44 PLCC or 40 N or 28 N or 28 SO
  - — 44 PLCC with 39 I/O pins
  - — 40 N with 33 I/O pins
  - — 28 SO or 28 N, each with 23 I/O pins
- Software selectable I/O options
  - — TRI-STATE® Output
  - — Push-Pull Output
  - — Weak Pull Up Input
  - — High Impedance Input
- Schmitt trigger inputs on ports G and L
- Temperature ranges: 0°C to +70°C,
  −40°C to +85°C,
  −55°C to +125°C
- Single chip hybrid emulation device COP888CLMH
- Real time emulation and full program debug offered by National's Development Systems

Block Diagram



TL/DD/9766–1

FIGURE 1. COP888CL Block Diagram

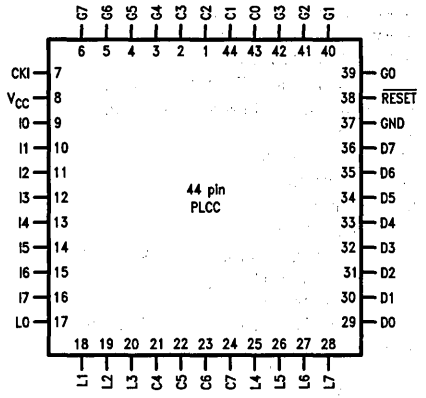
7

General Description (Continued)

It is a fully static part, fabricated using double-metal silicon gate microCMOS technology. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS serial I/O, two 16-bit timer/counters supporting three modes (Processor Independent PWM generation, External Event counter, and Input Capture mode capabilities), and two power savings modes (HALT and IDLE), both with a multi-sourced wakeup/interrupt capability. This multi-sourced interrupt capability may also be used independent of the HALT or IDLE modes. Each I/O pin has software selectable configurations. The COP888CL operates over a voltage range of 2.5V to 6V. High throughput is achieved with an efficient, regular instruction set operating at a maximum of 1 μs per instruction rate.

Connection Diagrams

Plastic Chip Carrier

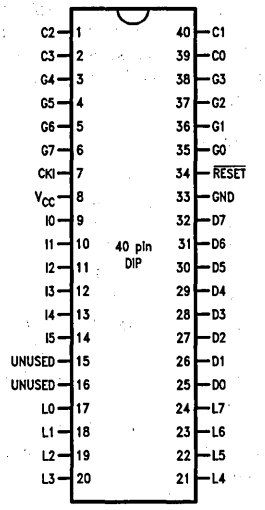


TL/DD/9766-2

Top View

Order Number COP688CL-XXX/V, COP888CL-XXX/V or COP988CL-XXX/V
See NS Plastic ChipPackage Number V44A

Dual-In-Line Package

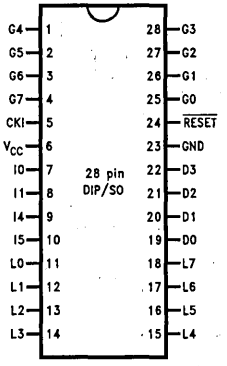


TL/DD/9766-4

Top View

Order Number COP688CL-XXX/N, COP888CL-XXX/N or COP988CL-XXX/N
See NS Molded Package Number N40A

Dual-In-Line Package



TL/DD/9766-5

Top View

Order Number COP688CL-XXX/N, COP884CL-XXX/N or COP984CL-XXX/N
See NS Molded Package Number N28B

Order Number COP684CL-XXX/WM, COP884CL-XXX/WM or COP984CL-XXX/WM
See NS Surface Mount Package Number M28B

FIGURE 2. COP888CL Connection Diagrams

Connection Diagrams (Continued)

COP888CL Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU		12	18	18
L2	I/O	MIWU		13	19	19
L3	I/O	MIWU		14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU		17	23	27
L7	I/O	MIWU		18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT RESTART		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
I0	I			7	9	9
I1	I			8	10	10
I2	I				11	11
I3	I				12	12
I4	I			9	13	13
I5	I			10	14	14
I6	I					15
I7	I					16
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
Unused*					16	
Unused*					15	
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

* = On the 40-pin package Pins 15 and 16 must be connected to GND.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

COP98XCL: 0°C ≤ T_A ≤ +70°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage					
COP98XCL		2.5		4.0	V
COP98XCLH		4.0		6.0	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			5.5	mA
CKI = 4 MHz	V_{CC} = 4V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			1.4	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<0.7	8	μA
	V_{CC} = 4V, CKI = 0 MHz		<0.4	5	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			0.7	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6V	−1		+1	μA
Input Pullup Current	V_{CC} = 6V	40		250	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4V, V_{OL} = 1V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2.0			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4V, V_{OH} = 2.7V	10		100	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink (Push-Pull Mode)	V_{CC} = 4V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			mA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor is disabled.

DC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
TRI-STATE Leakage	$V_{CC} = 6.0V$	−1		+1	μA
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				15	mA
All others				3	mA
Maximum Input Current without Latchup (Note 5)	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

AC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal or Resonator	$4V \le V_{CC} \le 6V$	1		DC	μs
	$2.5V \le V_{CC} < 4V$	2.5		DC	μs
R/C Oscillator	$4V \le V_{CC} \le 6V$	3		DC	μs
	$2.5V \le V_{CC} < 4V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 4)	f_r = Max	40		60	%
Rise Time (Note 4)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 4)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	$4V \le V_{CC} \le 6V$	200			ns
	$2.5V \le V_{CC} < 4V$	500			ns
t_{HOLD}	$4V \le V_{CC} \le 6V$	60			ns
	$2.5V \le V_{CC} < 4V$	150			ns
Output Propagation Delay	$R_L = 2.2k, C_L = 100$ pF				
t_{PD1}, t_{PD0}					
SO, SK	$4V \le V_{CC} \le 6V$			0.7	μs
	$2.5V \le V_{CC} < 4V$			1.75	μs
All Others	$4V \le V_{CC} \le 6V$			1	μs
	$2.5V \le V_{CC} < 4V$			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 4: Parameter sampled (not 100% tested).

Note 5: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics COP88XCL: $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		2.5		6	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			5.5	mA
CKI = 4 MHz	V_{CC} = 4V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			1.4	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<1	10	μA
	V_{CC} = 4V, CKI = 0 MHz		<0.5	6	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 4V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			0.7	mA
Input Levels					
$\overline{RESET}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6V	−1		+1	μA
Input Pullup Current	V_{CC} = 6V	40		250	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4V, V_{OL} = 1V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2.0			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4V, V_{OH} = 2.7V	10		100	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink (Push-Pull Mode)	V_{CC} = 4V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			mA
TRI-STATE Leakage	V_{CC} = 6.0V	−2		+2	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor is disabled.

DC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				15	mA
All others				3	mA
Maximum Input Current without Latchup (Note 5)	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

AC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal or Resonator	$4V \le V_{CC} \le 6V$	1		DC	μs
	$2.5V \le V_{CC} < 4V$	2.5		DC	μs
R/C Oscillator	$4V \le V_{CC} \le 6V$	3		DC	μs
	$2.5V \le V_{CC} < 4V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 4)	f_r = Max	40		60	%
Rise Time (Note 4)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 4)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	$4V \le V_{CC} \le 6V$	200			ns
	$2.5V \le V_{CC} < 4V$	500			ns
t_{HOLD}	$4V \le V_{CC} \le 6V$	60			ns
	$2.5V \le V_{CC} < 4V$	150			ns
Output Propagation Delay	$R_L = 2.2k, C_L = 100$ pF				
t_{PD1}, t_{PD0}					
SO, SK	$4V \le V_{CC} \le 6V$			0.7	μs
	$2.5V \le V_{CC} < 4V$			1.75	μs
All Others	$4V \le V_{CC} \le 6V$			1	μs
	$2.5V \le V_{CC} < 4V$			2.5	μs
MICROWIRE Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 4: Parameter sampled (not 100% tested).

Note 5: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Electrical Specifications

DC ELECTRICAL SPECIFICATIONS

COP688CL Absolute Specifications

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	90 mA
Total Current out of GND Pin (Sink)	100 mA
Storage Temperature Range	−65°C to +150°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

COP68XCL: $-55°C \le T_A \le +125°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		4.5		5.5	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 5.5V, t_c = 2.5 μs			5.5	mA
HALT Current (Note 3)	V_{CC} = 5.5V, CKI = 0 MHz		<10	30	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 5.5V, t_c = 2.5 μs			2.5	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 5.5V, V_{IN} = 0V	−5		+5	μA
Input Pullup Current	V_{CC} = 5.5V, V_{IN} = 0V	35		400	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1.0V	9			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4.5V, V_{OH} = 3.8V	9.0		140	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.4			mA
TRI-STATE Leakage	V_{CC} = 5.5V	−5.0		+5.0	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor is disabled.

DC Electrical Characteristics $-55°C \le T_A \le +25°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				12	mA
All others				2.5	mA
Maximum Input Current without Latchup (Note 5)				150	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2.0			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The Clock Monitor and the comparators are disabled.

AC Specifications for COP688CL

AC Electrical Characteristics $-55°C \le T_A \le +125°C$ unless otherwise specified

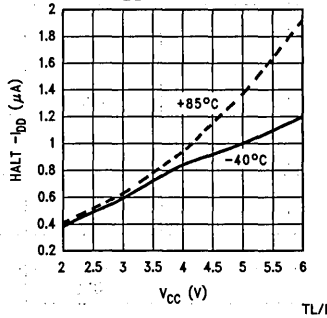
Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal, Resonator, or External Oscillator	$V_{CC} \ge 4.5V$	1		DC	μs
R/C Oscillator (div-by 10)	$V_{CC} \ge 4.5V$	3		DC	μs
CKI Clock Duty Cycle (Note 4) (Crystal Resonator or External Clock)	f_r = Max	45		55	%
Rise Time (Note 4)	f_r = 10 MHz Ext Clock			12	ns
Fall Time (Note 4)	f_r = 10 MHz Ext Clock			8	ns
Inputs					
t_{SETUP}	$V_{CC} \ge 4.5V$	200			ns
t_{HOLD}	$V_{CC} \ge 4.5V$	60			ns
Output Propagation Delay t_{PD1}, t_{PD0}	R_L = 2.2k, C_L = 100 pF				
SO, SK	$V_{CC} \ge 4.5V$			0.7	μs
All Others	$V_{CC} \ge 4.5V$			1	μs
MICROWIRE Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time(t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 4: Parameter sampled (not 100% tested).

Note 5: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

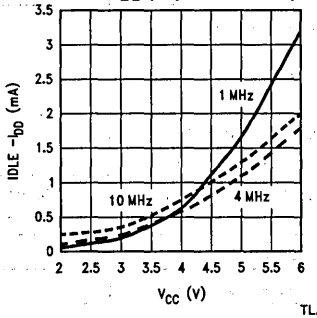
Typical Performance Characteristics ($-40°C \le T_A \le +85°C$)

Halt—I_{DD}



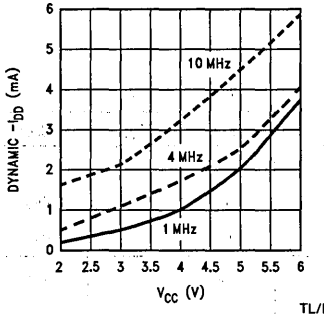
TL/DD/9766-27

Idle—I_{DD} (Crystal Clock Option)



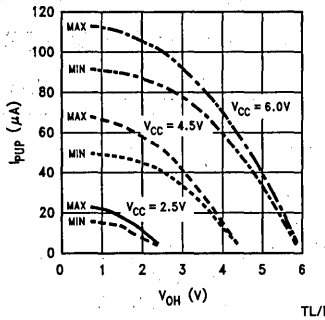
TL/DD/9766-28

Dynamic—I_{DD} vs V_{CC} (Crystal Clock Option)



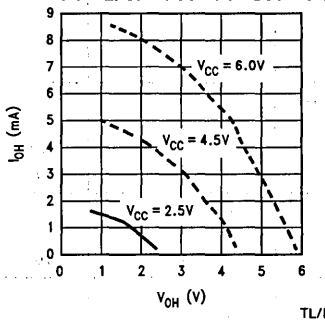
TL/DD/9766-29

Port L/C/G Weak Pull-Up Source Current



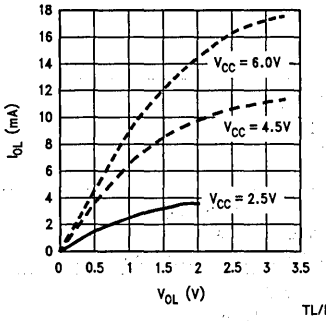
TL/DD/9766-30

Port L/C/G Push-Pull Source Current



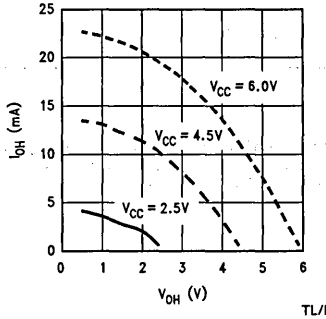
TL/DD/9766-31

Port L/C/G Push-Pull Sink Current



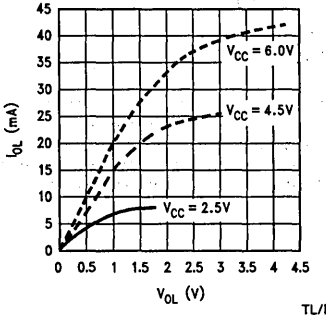
TL/DD/9766-32

Port D Source Current



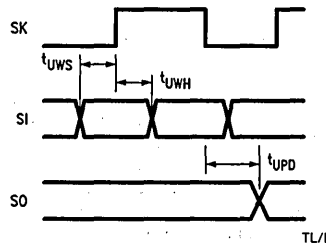
TL/DD/9766-33

Port D Sink Current



TL/DD/9766-34

AC Electrical Characteristics (Continued)



TL/DD/9766-26

FIGURE 2. MICROWIRE/PLUS Timing

Pin Descriptions

V_{CC} and GND are the power supply pins.

CKI is the clock input. This can come from an R/C generated oscillator, or a crystal oscillator (in conjunction with CKO). See Oscillator Description section.

$\overline{\text{RESET}}$ is the master reset input. See Reset Description section.

The COP888CL contains three bidirectional 8-bit I/O ports (C, G and L), where each individual bit may be independently configured as an input (Schmitt trigger inputs on ports G and L), output or TRI-STATE under program control. Three data memory address locations are allocated for each of these I/O ports. Each I/O port has two associated 8-bit memory mapped registers, the CONFIGURATION register and the output DATA register. A memory mapped address is also reserved for the input pins of each I/O port. (See the COP888CL memory map for the various addresses associated with the I/O ports.) *Figure 3* shows the I/O port configurations for the COP888CL. The DATA and CONFIGURATION registers allow for each port bit to be individually configured under software control as shown below:

CONFIGURATION Register	DATA Register	Port Set-Up
0	0	Hi-Z Input (TRI-STATE Output)
0	1	Input with Weak Pull-Up
1	0	Push-Pull Zero Output
1	1	Push-Pull One Output

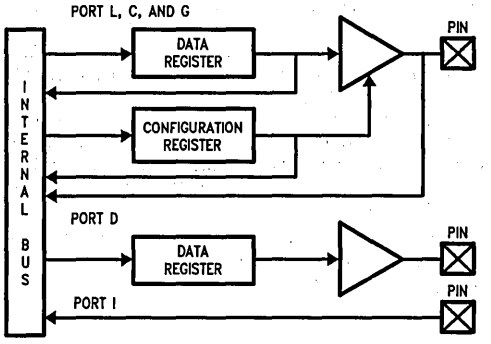


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FIGURE 3. I/O Port Configurations

PORT L is an 8-bit I/O port. All L-pins have Schmitt triggers on the inputs.

Port L supports Multi-Input Wakeup (MIWU) on all eight pins. L4 and L5 are used for the timer input functions T2A and T2B.

Port L has the following alternate features:

- L0 MIWU
- L1 MIWU
- L2 MIWU
- L3 MIWU
- L4 MIWU or T2A
- L5 MIWU or T2B
- L6 MIWU
- L7 MIWU

Port G is an 8-bit port with 5 I/O pins (G0, G2–G5), an input pin (G6), and two dedicated output pins (G1 and G7). Pins G0 and G2–G6 all have Schmitt Triggers on their inputs. Pin G1 serves as the dedicated WDOUT WATCHDOG output, while pin G7 is either input or output depending on the oscillator mask option selected. With the crystal oscillator option selected, G7 serves as the dedicated output pin for the CKO clock output. With the single-pin R/C oscillator mask option selected, G7 serves as a general purpose input pin, but is also used to bring the device out of HALT mode with a low to high transition. There are two registers associated with the G Port, a data register and a configuration register. Therefore, each of the 5 I/O bits (G0, G2–G5) can be individually configured under software control.

Since G6 is an input only pin and G7 is the dedicated CKO clock output pin or general purpose input (R/C clock configuration), the associated bits in the data and configuration registers for G6 and G7 are used for special purpose functions as outlined below. Reading the G6 and G7 data bits will return zeros.

Note that the chip will be placed in the HALT mode by writing a "1" to bit 7 of the Port G Data Register. Similarly the chip will be placed in the IDLE mode by writing a "1" to bit 6 of the Port G Data Register.

Writing a "1" to bit 6 of the Port G Configuration Register enables the MICROWIRE/PLUS to operate with the alternate phase of the SK clock. The G7 configuration bit, if set high, enables the clock start up delay after HALT when the R/C clock configuration is used.

	Config Reg.	Data Reg.
G7	CLKDLY	HALT
G6	Alternate SK	IDLE

Port G has the following alternate features:

- G0 INTR (External Interrupt Input)
- G2 T1B (Timer T1 Capture Input)
- G3 T1A (Timer T1 I/O)
- G4 SO (MICROWIRE™ Serial Data Output)
- G5 SK (MICROWIRE Serial Clock)
- G6 SI (MICROWIRE Serial Data Input)

Pin Descriptions (Continued)

Port G has the following dedicated functions:

- G1 WDOUT WATCHDOG and/or Clock Monitor dedicated output
- G7 CKO Oscillator dedicated output or general purpose input

Port C is an 8-bit I/O port. The 40-pin device does not have a full complement of Port C pins. The unavailable pins are not terminated. A read operation for these unterminated pins will return unpredictable values.

Port I is an 8-bit Hi-Z input port. The 40-pin device does not have a full complement of Port I pins. Pins 15 and 16 on this package must be connected to GND.

The 28-pin device has four I pins (I0, I1, I4, I5). The user should pay attention when reading port I to the fact that I4 and I5 are in bit positions 4 and 5 rather than 2 and 3.

The unavailable pins (I4–I7) are not terminated i.e., they are floating. A read operation for these unterminated pins will return unpredictable values. The user must ensure that the software takes into account by either masking or restricting the accesses to bit operations. The unterminated port I pins will draw power only when addressed.

Port D is an 8-bit output port that is preset high when RESET goes low. The user can tie two or more D port outputs together in order to get a higher drive.

Functional Description

The architecture of the COP888CL is modified Harvard architecture. With the Harvard architecture, the control store program memory (ROM) is separated from the data store memory (RAM). Both ROM and RAM have their own separate addressing space with separate address buses. The COP888CL architecture, though based on Harvard architecture, permits transfer of data from ROM to RAM.

CPU REGISTERS

The CPU can do an 8-bit addition, subtraction, logical or shift operation in one instruction (t_C) cycle time.

There are five CPU registers:

A is the 8-bit Accumulator Register

PC is the 15-bit Program Counter Register

- PU is the upper 7 bits of the program counter (PC)
- PL is the lower 8 bits of the program counter (PC)

B is an 8-bit RAM address pointer, which can be optionally post auto incremented or decremented.

X is an 8-bit alternate RAM address pointer, which can be optionally post auto incremented or decremented.

SP is the 8-bit stack pointer, which points to the subroutine/interrupt stack (in RAM). The SP is initialized to RAM address 06F with reset.

All the CPU registers are memory mapped with the exception of the Accumulator (A) and the Program Counter (PC).

PROGRAM MEMORY

Program memory for the COP888CL consists of 4096 bytes of ROM. These bytes may hold program instructions or constant data (data tables for the LAID instruction, jump vectors for the JID instruction, and interrupt vectors for the VIS instruction). The program memory is addressed by the 15-bit program counter (PC). All interrupts in the COP888CL vector to program memory location 0FF Hex.

DATA MEMORY

The data memory address space includes the on-chip RAM and data registers, the I/O registers (Configuration, Data and Pin), the control registers, the MICROWIRE/PLUS SIO shift register, and the various registers, and counters associated with the timers (with the exception of the IDLE timer). Data memory is addressed directly by the instruction or indirectly by the B, X and SP pointers.

The COP888CL has 128 bytes of RAM. Sixteen bytes of RAM are mapped as "registers" at addresses 0F0 to 0FF Hex. These registers can be loaded immediately, and also decremented and tested with the DRSZ (decrement register and skip if zero) instruction. The memory pointer registers X, SP, and B are memory mapped into this space at address locations 0FC to 0FE Hex respectively, with the other registers (other than reserved register 0FF) being available for general usage.

The instruction set of the COP888CL permits any bit in memory to be set, reset or tested. All I/O and registers on the COP888CL (except A and PC) are memory mapped; therefore, I/O bits and register bits can be directly and individually set, reset and tested. The accumulator (A) bits can also be directly and individually tested.

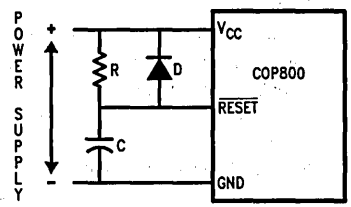
Reset

The $\overline{\text{RESET}}$ input when pulled low initializes the microcontroller. Initialization will occur whenever the $\overline{\text{RESET}}$ input is pulled low. Upon initialization, the data and configuration registers for Ports L, G, and C are cleared, resulting in these Ports being initialized to the TRI-STATE mode. Pin G1 of the G Port is an exception (as noted below) since pin G1 is dedicated as the WATCHDOG and/or Clock Monitor error output pin. Port D is initialized high with $\overline{\text{RESET}}$. The PC, PSW, CNTRL, ICNTRL, and T2CNTRL control registers are cleared. The Multi-Input Wakeup registers WKEN, WKEDG, and WKPND are cleared. The Stack Pointer, SP, is initialized to 06F Hex.

The COP888CL comes out of reset with both the WATCHDOG logic and the Clock Monitor detector armed, and with both the WATCHDOG service window bits set and the Clock Monitor bit set. The WATCHDOG and Clock Monitor detector circuits are inhibited during reset. The WATCHDOG service window bits are initialized to the maximum WATCHDOG service window of 64k t_C clock cycles. The Clock Monitor bit is initialized high, and will cause a Clock Monitor error following reset if the clock has not reached the minimum specified frequency at the termination of reset. A Clock Monitor error will cause an active low error output on pin G1. This error output will continue until 16–32 t_C clock cycles following the clock frequency reaching the minimum specified value, at which time the G1 output will enter the TRI-STATE mode.

The external RC network shown in *Figure 4* should be used to ensure that the $\overline{\text{RESET}}$ pin is held low until the power supply to the chip stabilizes.

Reset (Continued)



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RC > 5 × Power Supply Rise Time

FIGURE 4. Recommended Reset Circuit

Oscillator Circuits

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (crystal configuration). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_C$).

Figure 5 shows the Crystal and R/C diagrams.

CRYSTAL OSCILLATOR

CKI and CKO can be connected to make a closed loop crystal (or resonator) controlled oscillator.

Table A shows the component values required for various standard crystal values.

R/C OSCILLATOR

By selecting CKI as a single pin oscillator input, a single pin R/C oscillator circuit can be connected to it. CKO is available as a general purpose input, and/or HALT restart pin.

Table B shows the variation in the oscillator frequencies as functions of the component (R and C) values.

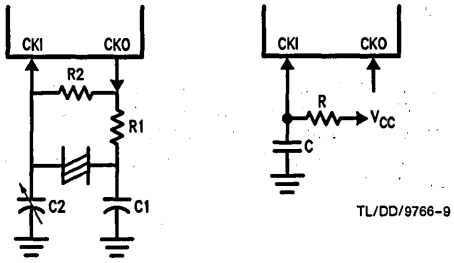

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FIGURE 5. Crystal and R/C Oscillator Diagrams

TABLE A. Crystal Oscillator Configuration, T_A = 25°C

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)	Conditions
0	1	30	30-36	10	V_{CC} = 5V
0	1	30	30-36	4	V_{CC} = 5.0V
0	1	200	100-150	0.455	V_{CC} = 5V

TABLE B. RC Oscillator Configuration, T_A = 25°C

R (kΩ)	C (pF)	CKI Freq (MHz)	Instr. Cycle (μs)	Conditions
3.3	82	2.2 to 2.7	3.7 to 4.6	V_{CC} = 5V
5.6	100	1.1 to 1.3	7.4 to 9.0	V_{CC} = 5V
6.8	100	0.9 to 1.1	8.8 to 10.8	V_{CC} = 5V

Note: 3k ≤ R ≤ 200k, 50 pF ≤ C ≤ 200 pF

Current Drain

The total current drain of the chip depends on:

1. Oscillator operation mode—I1
2. Internal switching current—I2
3. Internal leakage current—I3
4. Output source current—I4
5. DC current caused by external input not at V_{CC} or GND—I5
6. Clock Monitor current when enabled—I6

Thus the total current drain, It, is given as

$$It = I1 + I2 + I3 + I4 + I5 + I6$$

To reduce the total current drain, each of the above components must be minimum.

The chip will draw more current as the CKI input frequency increases up to the maximum 10 MHz value. Operating with a crystal network will draw more current than an external square-wave. Switching current, governed by the equation below, can be reduced by lowering voltage and frequency. Leakage current can be reduced by lowering voltage and temperature. The other two items can be reduced by carefully designing the end-user's system.

$$I2 = C \times V \times f$$

where C = equivalent capacitance of the chip
V = operating voltage
f = CKI frequency

Control Registers

CNTRL Register (Address X'00EE)

The Timer1 (T1) and MICROWIRE/PLUS control register contains the following bits:

SL1 & SL0 Select the MICROWIRE/PLUS clock divide by (00 = 2, 01 = 4, 1x = 8)

IEDG External interrupt edge polarity select (0 = Rising edge, 1 = Falling edge)

MSEL Selects G5 and G4 as MICROWIRE/PLUS signals SK and SO respectively

Control Registers (Continued)

T1C0 Timer T1 Start/Stop control in timer modes 1 and 2
Timer T1 Underflow Interrupt Pending Flag in timer mode 3

T1C1 Timer T1 mode control bit

T1C2 Timer T1 mode control bit

T1C3 Timer T1 mode control bit

T1C3	T1C2	T1C1	T1C0	MSEL	IEDG	SL1	SL0

Bit 7 Bit 0

PSW Register (Address X'00EF)

The PSW register contains the following select bits:

GIE Global interrupt enable (enables interrupts)

EXEN Enable external interrupt

BUSY MICROWIRE/PLUS busy shifting flag

EXPND External interrupt pending

T1ENA Timer T1 Interrupt Enable for Timer Underflow or T1A Input capture edge

T1PNDA Timer T1 Interrupt Pending Flag (Autoreload RA in mode 1, T1 Underflow in Mode 2, T1A capture edge in mode 3)

C Carry Flag

HC Half Carry Flag

HC	C	T1PNDA	T1ENA	EXPND	BUSY	EXEN	GIE

Bit 7 Bit 0

The Half-Carry bit is also affected by all the instructions that affect the Carry flag. The SC (Set Carry) and RC (Reset Carry) instructions will respectively set or clear both the carry flags. In addition to the SC and RC instructions, ADC, SUBC, RRC and RLC instructions affect the carry and Half Carry flags.

ICNTRL Register (Address X'00E8)

The ICNTRL register contains the following bits:

T1ENB Timer T1 Interrupt Enable for T1B Input capture edge

T1PNDB Timer T1 Interrupt Pending Flag for T1B capture edge

μWEN Enable MICROWIRE/PLUS interrupt

μWPND MICROWIRE/PLUS interrupt pending

T0EN Timer T0 Interrupt Enable (Bit 12 toggle)

T0PND Timer T0 Interrupt pending

LPEN L Port Interrupt Enable (Multi-Input Wakeup/Interrupt)
Bit 7 could be used as a flag

Unused	LPEN	T0PND	T0EN	μWPND	μWEN	T1PNDB	T1ENB

Bit 7 Bit 0

T2CNTRL Register (Address X'00C6)

The T2CNTRL register contains the following bits:

T2ENB Timer T2 Interrupt Enable for T2B Input capture edge

T2PNDB Timer T2 Interrupt Pending Flag for T2B capture edge

T2ENA Timer T2 Interrupt Enable for Timer Underflow or T2A Input capture edge

T2PNDA Timer T2 Interrupt Pending Flag (Autoreload RA in mode 1, T2 Underflow in mode 2, T2A capture edge in mode 3)

T2C0 Timer T2 Start/Stop control in timer modes 1 and 2 Timer T2 Underflow Interrupt Pending Flag in timer mode 3

T2C1 Timer T2 mode control bit

T2C2 Timer T2 mode control bit

T2C3 Timer T2 mode control bit

T2C3	T2C2	T2C1	T2C0	T2PNDA	T2ENA	T2PNDB	T2ENB

Bit 7 Bit 0

Timers

The COP888CL contains a very versatile set of timers (T0, T1, T2). All timers and associated autoreload/capture registers power up containing random data.

Figure 6 shows a block diagram for the timers on the COP888CL.

Timers (Continued)

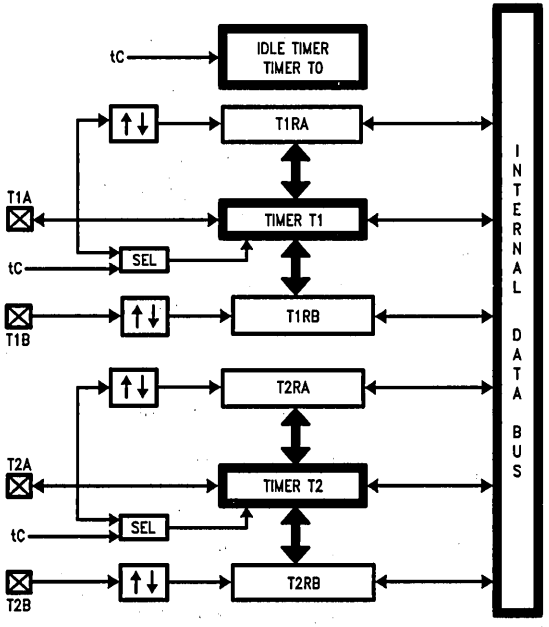

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FIGURE 6. Timers for the COP888CL

TIMER T0 (IDLE TIMER)

The COP888CL supports applications that require maintaining real time and low power with the IDLE mode. This IDLE mode support is furnished by the IDLE timer T0, which is a 16-bit timer. The Timer T0 runs continuously at the fixed rate of the instruction cycle clock, t_c. The user cannot read or write to the IDLE Timer T0, which is a count down timer.

The Timer T0 supports the following functions:

Exit out of the Idle Mode (See Idle Mode description)
WATCHDOG logic (See WATCHDOG description)
Start up delay out of the HALT mode

The IDLE Timer T0 can generate an interrupt when the thirteenth bit toggles. This toggle is latched into the T0PND pending flag, and will occur every 4 ms at the maximum clock frequency (t_c = 1 μs). A control flag T0EN allows the interrupt from the thirteenth bit of Timer T0 to be enabled or disabled. Setting T0EN will enable the interrupt, while resetting it will disable the interrupt.

TIMER T1 AND TIMER T2

The COP888CL has a set of two powerful timer/counter blocks, T1 and T2. The associated features and functioning of a timer block are described by referring to the timer block Tx. Since the two timer blocks, T1 and T2, are identical, all comments are equally applicable to either timer block.

Each timer block consists of a 16-bit timer, Tx, and two supporting 16-bit autoreload/capture registers, RxA and RxB. Each timer block has two pins associated with it, TxA and TxB. The pin TxA supports I/O required by the timer block, while the pin TxB is an input to the timer block. The powerful and flexible timer block allows the COP888CL to easily perform all timer functions with minimal software overhead. The timer block has three operating modes: Processor Independent PWM mode, External Event Counter mode, and Input Capture mode.

The control bits TxC3, TxC2, and TxC1 allow selection of the different modes of operation.

Mode 1. Processor Independent PWM Mode

As the name suggests, this mode allows the COP888CL to generate a PWM signal with very minimal user intervention.

The user only has to define the parameters of the PWM signal (ON time and OFF time). Once begun, the timer block will continuously generate the PWM signal completely independent of the microcontroller. The user software services the timer block only when the PWM parameters require updating.

In this mode the timer Tx counts down at a fixed rate of t_c. Upon every underflow the timer is alternately reloaded with the contents of supporting registers, RxA and RxB. The very first underflow of the timer causes the timer to reload from the register RxA. Subsequent underflows cause the timer to be reloaded from the registers alternately beginning with the register RxB.

The Tx Timer control bits, TxC3, TxC2 and TxC1 set up the timer for PWM mode operation.

Figure 7 shows a block diagram of the timer in PWM mode.

Timers (Continued)

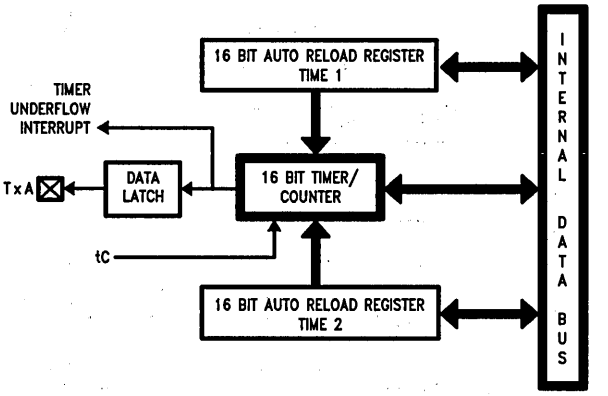

FIGURE 7. Timer in PWM Mode

The underflows can be programmed to toggle the TxA output pin. The underflows can also be programmed to generate interrupts.

Underflows from the timer are alternately latched into two pending flags, TxPNDA and TxPNDB. The user must reset these pending flags under software control. Two control enable flags, TxENA and TxENB, allow the interrupts from the timer underflow to be enabled or disabled. Setting the timer enable flag TxENA will cause an interrupt when a timer underflow causes the RxA register to be reloaded into the timer. Setting the timer enable flag TxENB will cause an interrupt when a timer underflow causes the RxB register to be reloaded into the timer. Resetting the timer enable flags will disable the associated interrupts.

Either or both of the timer underflow interrupts may be enabled. This gives the user the flexibility of interrupting once per PWM period on either the rising or falling edge of the PWM output. Alternatively, the user may choose to interrupt on both edges of the PWM output.

Mode 2. External Event Counter Mode

This mode is quite similar to the processor independent PWM mode described above. The main difference is that the timer, Tx, is clocked by the input signal from the TxA pin. The Tx timer control bits, TxC3, TxC2 and TxC1 allow the timer to be clocked either on a positive or negative edge from the TxA pin. Underflows from the timer are latched into the TxPNDA pending flag. Setting the TxENA control flag will cause an interrupt when the timer underflows.

In this mode the input pin TxB can be used as an independent positive edge sensitive interrupt input if the TxENB control flag is set. The occurrence of a positive edge on the TxB input pin is latched into the TxPNDB flag.

Figure 8 shows a block diagram of the timer in External Event Counter mode.

Note: The PWM output is not available in this mode since the TxA pin is being used as the counter input clock.

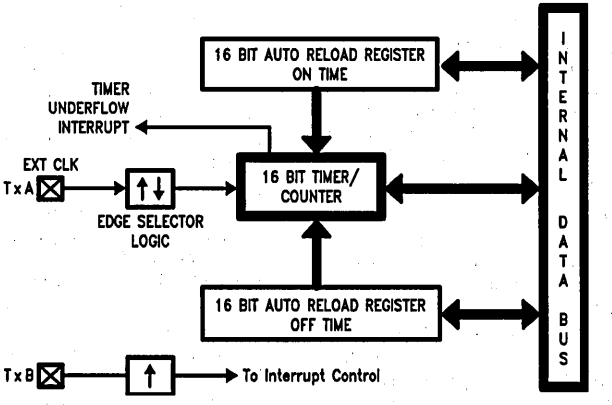

FIGURE 8. Timer in External Event Counter Mode

Timers (Continued)

Mode 3. Input Capture Mode

The COP888CL can precisely measure external frequencies or time external events by placing the timer block, Tx, in the input capture mode.

In this mode, the timer Tx is constantly running at the fixed t_C rate. The two registers, RxA and RxB, act as capture registers. Each register acts in conjunction with a pin. The register RxA acts in conjunction with the TxA pin and the register RxB acts in conjunction with the TxB pin.

The timer value gets copied over into the register when a trigger event occurs on its corresponding pin. Control bits, TxC3, TxC2 and TxC1, allow the trigger events to be specified either as a positive or a negative edge. The trigger condition for each input pin can be specified independently.

The trigger conditions can also be programmed to generate interrupts. The occurrence of the specified trigger condition on the TxA and TxB pins will be respectively latched into the pending flags, TxPNDA and TxPNDB. The control flag TxENA allows the interrupt on TxA to be either enabled or disabled. Setting the TxENA flag enables interrupts to be generated when the selected trigger condition occurs on the TxA pin. Similarly, the flag TxENB controls the interrupts from the TxB pin.

Underflows from the timer can also be programmed to generate interrupts. Underflows are latched into the timer TxC0 pending flag (the TxC0 control bit serves as the timer underflow interrupt pending flag in the Input Capture mode). Consequently, the TxC0 control bit should be reset when entering the Input Capture mode. The timer underflow interrupt is enabled with the TxENA control flag. When a TxA interrupt occurs in the Input Capture mode, the user must check both the TxPNDA and TxC0 pending flags in order to determine whether a TxA input capture or a timer underflow (or both) caused the interrupt.

Figure 9 shows a block diagram of the timer in Input Capture mode.

TIMER CONTROL FLAGS

The timers T1 and T2 have indentical control structures. The control bits and their functions are summarized below.

TxC0	Timer Start/Stop control in Modes 1 and 2 (Processor Independent PWM and External Event Counter), where 1 = Start, 0 = Stop Timer Underflow Interrupt Pending Flag in Mode 3 (Input Capture)
TxPNDA	Timer Interrupt Pending Flag
TxPNDB	Timer Interrupt Pending Flag
TxENA	Timer Interrupt Enable Flag
TxENB	Timer Interrupt Enable Flag 1 = Timer Interrupt Enabled 0 = Timer Interrupt Disabled
TxC3	Timer mode control
TxC2	Timer mode control
TxC1	Timer mode control

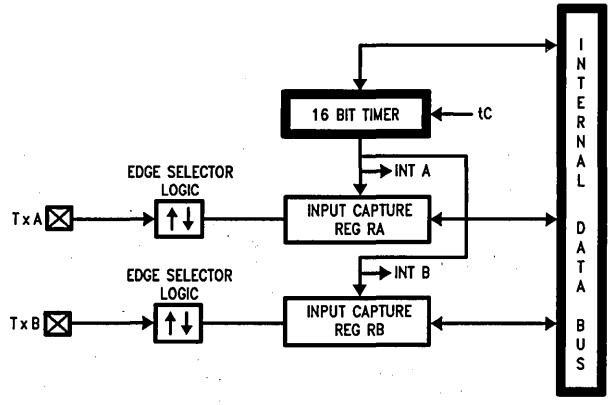

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FIGURE 9. Timer in Input Capture Mode

Timers (Continued)

The timer mode control bits (TxC3, TxC2 and TxC1) are detailed below:

TxC3	TxC2	TxC1	Timer Mode	Interrupt A Source	Interrupt B Source	Timer Counts On
0	0	0	MODE 2 (External Event Counter)	Timer Underflow	Pos. TxB Edge	TxA Pos. Edge
0	0	1	MODE 2 (External Event Counter)	Timer Underflow	Pos. TxB Edge	TxA Neg. Edge
1	0	1	MODE 1 (PWM) TxA Toggle	Autoreload RA	Autoreload RB	t_C
1	0	0	MODE 1 (PWM) No TxA Toggle	Autoreload RA	Autoreload RB	t_C
0	1	0	MODE 3 (Capture) Captures: TxA Pos. Edge TxB Pos. Edge	Pos. TxA Edge or Timer Underflow	Pos. TxB Edge	t_C
1	1	0	MODE 3 (Capture) Captures: TxA Pos. Edge TxB Neg. Edge	Pos. TxA Edge or Timer Underflow	Neg. TxB Edge	t_C
0	1	1	MODE 3 (Capture) Captures: TxA Neg. Edge TxB Pos. Edge	Neg. TxB Edge or Timer Underflow	Pos. TxB Edge	t_C
1	1	1	MODE 3 (Capture) Captures: TxA Neg. Edge TxB Neg. Edge	Neg. TxA Edge or Timer Underflow	Neg. TxB Edge	t_C

Power Save Modes

The COP888CL offers the user two power save modes of operation: HALT and IDLE. In the HALT mode, all microcontroller activities are stopped. In the IDLE mode, the on-board oscillator circuitry and timer T0 are active but all other microcontroller activities are stopped. In either mode, all on-board RAM, registers, I/O states, and timers (with the exception of T0) are unaltered.

HALT MODE

The COP888CL is placed in the HALT mode by writing a "1" to the HALT flag (G7 data bit). All microcontroller activities, including the clock, timers, are stopped. The WATCHDOG logic on the COP888CL is disabled during the HALT mode. However, the clock monitor circuitry, if enabled, remains active and will cause the WATCHDOG output pin (WDOUT) to go low. If the HALT mode is used and the user does not want to activate the WDOUT pin, the Clock Monitor should be disabled after the device comes out of reset (resetting the Clock Monitor control bit with the first write to the WDSVR register). In the HALT mode, the power requirements of the COP888CL are minimal and the applied voltage (V_{CC}) may be decreased to V_r (V_r = 2.0V) without altering the state of the machine.

The COP888CL supports three different ways of exiting the HALT mode. The first method of exiting the HALT mode is with the Multi-Input Wakeup feature on the L port. The second method is with a low to high transition on the CKO (G7) pin. This method precludes the use of the crystal clock configuration (since CKO becomes a dedicated output), and so may be used with an RC clock configuration. The third method of exiting the HALT mode is by pulling the $\overline{\text{RESET}}$ pin low.

Since a crystal or ceramic resonator may be selected as the oscillator, the Wakeup signal is not allowed to start the chip running immediately since crystal oscillators and ceramic resonators have a delayed start up time to reach full amplitude and frequency stability. The IDLE timer is used to generate a fixed delay to ensure that the oscillator has indeed stabilized before allowing instruction execution. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry is enabled. The IDLE timer is loaded with a value of 256 and is clocked with the t_C instruction cycle clock. The t_C clock is derived by dividing the oscillator clock down by a factor of 10. The Schmitt trigger following the CKI inverter on the chip ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

Power Save Modes (Continued)

If an RC clock option is being used, the fixed delay is introduced optionally. A control bit, CLKDLY, mapped as configuration bit G7, controls whether the delay is to be introduced or not. The delay is included if CLKDLY is set, and excluded if CLKDLY is reset. The CLKDLY bit is cleared on reset.

The COP888CL has two mask options associated with the HALT mode. The first mask option enables the HALT mode feature, while the second mask option disables the HALT mode. With the HALT mode enable mask option, the COP888CL will enter and exit the HALT mode as described above. With the HALT disable mask option, the COP888CL cannot be placed in the HALT mode (writing a "1" to the HALT flag will have no effect).

The WATCHDOG detector circuit is inhibited during the HALT mode. However, the clock monitor circuit, if enabled, remains active during HALT mode in order to ensure a clock monitor error if the COP888CL inadvertently enters the HALT mode as a result of a runaway program or power glitch.

IDLE MODE

The COP888CL is placed in the IDLE mode by writing a "1" to the IDLE flag (G6 data bit). In this mode, all activity, except the associated on-board oscillator circuitry, the WATCHDOG logic, the clock monitor and the IDLE Timer T0, is stopped. The power supply requirements of the microcontroller in this mode of operation are typically around 30% of normal power requirement of the microcontroller.

As with the HALT mode, the COP888CL can be returned to normal operation with a reset, or with a Multi-Input Wake-up from the L Port. Alternately, the microcontroller resumes normal operation from the IDLE mode when the thirteenth bit (representing 4.096 ms at internal clock frequency of 1 MHz, t_C = 1 μs) of the IDLE Timer toggles.

This toggle condition of the thirteenth bit of the IDLE Timer T0 is latched into the T0PND pending flag.

The user has the option of being interrupted with a transition on the thirteenth bit of the IDLE Timer T0. The interrupt can be enabled or disabled via the T0EN control bit. Setting the T0EN flag enables the interrupt and vice versa.

The user can enter the IDLE mode with the Timer T0 interrupt enabled. In this case, when the T0PND bit gets set, the COP888CL will first execute the Timer T0 interrupt service routine and then return to the instruction following the "Enter Idle Mode" instruction.

Alternatively, the user can enter the IDLE mode with the IDLE Timer T0 interrupt disabled. In this case, the COP888CL will resume normal operation with the instruction immediately following the "Enter IDLE Mode" instruction.

Note: It is necessary to program two NOP instructions following both the set HALT mode and set IDLE mode instructions. These NOP instructions are necessary to allow clock resynchronization following the HALT or IDLE modes.

Multi-Input Wakeup

The Multi-Input Wakeup feature is used to return (wakeup) the COP888CL from either the HALT or IDLE modes. Alternately Multi-Input Wakeup/Interrupt feature may also be used to generate up to 8 edge selectable external interrupts.

Figure 10 shows the Multi-Input Wakeup logic for the COP888CL microcontroller.

The Multi-Input Wakeup feature utilizes the L Port. The user selects which particular L port bit (or combination of L Port bits) will cause the COP888CL to exit the HALT or IDLE modes. The selection is done through the Reg: WKEN. The Reg: WKEN is an 8-bit read/write register, which contains a control bit for every L port bit. Setting a particular WKEN bit enables a Wakeup from the associated L port pin.

The user can select whether the trigger condition on the selected L Port pin is going to be either a positive edge (low to high transition) or a negative edge (high to low transition). This selection is made via the Reg: WKEDG, which is an 8-bit control register with a bit assigned to each L Port pin. Setting the control bit will select the trigger condition to be a negative edge on that particular L Port pin. Resetting the bit selects the trigger condition to be a positive edge. Changing an edge select entails several steps in order to avoid a pseudo Wakeup condition as a result of the edge change. First, the associated WKEN bit should be reset, followed by the edge select change in WKEDG. Next, the associated WKPND bit should be cleared, followed by the associated WKEN bit being re-enabled.

An example may serve to clarify this procedure. Suppose we wish to change the edge select from positive (low going high) to negative (high going low) for L Port bit 5, where bit 5 has previously been enabled for an input interrupt. The program would be as follows:

```
RBIT  5, WKEN
SBIT  5, WKEDG
RBIT  5, WKPND
SBIT  5, WKEN
```

If the L port bits have been used as outputs and then changed to inputs with Multi-Input Wakeup/Interrupt, a safety procedure should also be followed to avoid inherited pseudo wakeup conditions. After the selected L port bits have been changed from output to input but before the associated WKEN bits are enabled, the associated edge select bits in WKEDG should be set or reset for the desired edge selects, followed by the associated WKPND bits being cleared.

This same procedure should be used following reset, since the L port inputs are left floating as a result of reset.

The occurrence of the selected trigger condition for Multi-Input Wakeup is latched into a pending register called WKPND. The respective bits of the WKPND register will be set on the occurrence of the selected trigger edge on the corresponding Port L pin. The user has the responsibility of clearing these pending flags. Since WKPND is a pending register for the occurrence of selected wakeup conditions, the COP888CL will not enter the HALT mode if any Wakeup bit is both enabled and pending. Consequently, the user has the responsibility of clearing the pending flags before attempting to enter the HALT mode.

The WKEN, WKPND and WKEDG are all read/write registers, and are cleared at reset.

PORT L INTERRUPTS

Port L provides the user with an additional eight fully selectable, edge sensitive interrupts which are all vectored into the same service subroutine.

The interrupt from Port L shares logic with the wake up circuitry. The register WKEN allows interrupts from Port L to

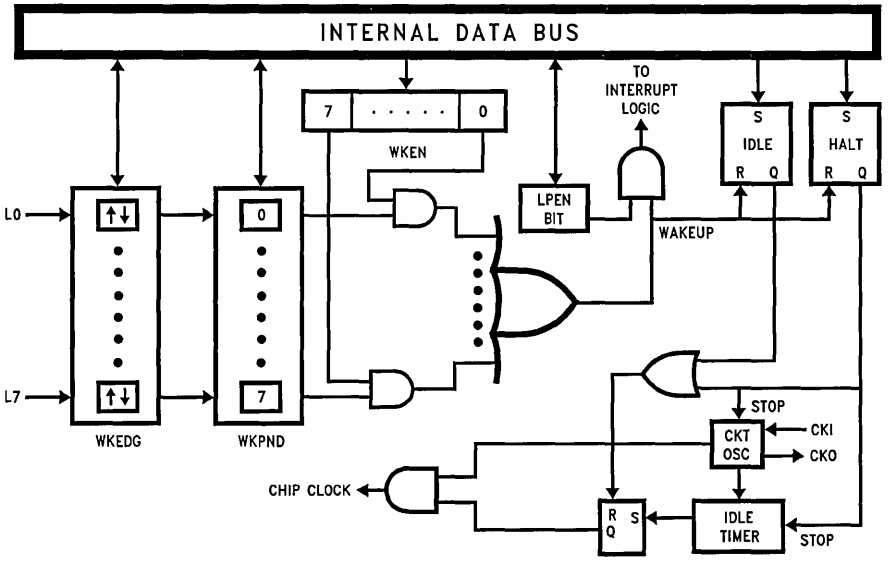

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FIGURE 10. Multi-Input Wake Up Logic

Multi-Input Wakeup (Continued)

be individually enabled or disabled. The register WKEDG specifies the trigger condition to be either a positive or a negative edge. Finally, the register WKPND latches in the pending trigger conditions.

The GIE (Global Interrupt Enable) bit enables the interrupt function.

A control flag, LPEN, functions as a global interrupt enable for Port L interrupts. Setting the LPEN flag will enable interrupts and vice versa. A separate global pending flag is not needed since the register WKPND is adequate.

Since Port L is also used for waking the COP888CL out of the HALT or IDLE modes, the user can elect to exit the HALT or IDLE modes either with or without the interrupt enabled. If he elects to disable the interrupt, then the COP888CL will restart execution from the instruction immediately following the instruction that placed the microcontroller in the HALT or IDLE modes. In the other case, the COP888CL will first execute the interrupt service routine and then revert to normal operation.

The Wakeup signal will not start the chip running immediately since crystal oscillators or ceramic resonators have a finite start up time. The IDLE Timer (T0) generates a fixed delay to ensure that the oscillator has indeed stabilized before allowing the COP888CL to execute instructions. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry and the IDLE Timer T0 are enabled. The IDLE Timer is loaded with a value of 256 and is clocked from the t_c instruction cycle clock. The t_c clock is derived by dividing down the oscillator clock by a factor of 10. A Schmitt trigger following the CKI on-chip inverter ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

If the RC clock option is used, the fixed delay is under software control. A control flag, CLKDLY, in the G7 configuration bit allows the clock start up delay to be optionally inserted. Setting CLKDLY flag high will cause clock start up delay to be inserted and resetting it will exclude the clock start up delay. The CLKDLY flag is cleared during reset, so the clock start up delay is not present following reset with the RC clock options.

Interrupts

The COP888CL supports a vectored interrupt scheme. It supports a total of ten interrupt sources. The following table lists all the possible COP888CL interrupt sources, their arbitration ranking and the memory locations reserved for the interrupt vector for each source.

Arbitration Ranking	Source	Description	Vector Address Hi-Low Byte
(1) Highest	Software	INTR Instruction	0yFE–0yFF
	Reserved	for Future Use	0yFC–0yFD
(2)	External	Pin G0 Edge	0yFA–0yFB
(3)	Timer T0	Underflow	0yF8–0yF9
(4)	Timer T1	T1A/Underflow	0yF6–0yF7
(5)	Timer T1	T1B	0yF4–0yF5
(6)	MICROWIRE/PLUS	BUSY Goes Low	0yF2–0yF3
	Reserved	for Future Use	0yF0–0yF1
	Reserved	for UART	0yEE–0yEF
	Reserved	for UART	0yEC–0yED
(7)	Timer T2	T2A/Underflow	0yEA–0yEB
(8)	Timer T2	T2B	0yE8–0yE9
	Reserved	for Future Use	0yE6–0yE7
	Reserved	for Future Use	0yE4–0yE5
(9)	Port L/Wakeup	Port L Edge	0yE2–0yE3
(10) Lowest	Default	VIS Instr. Execution without Any Interrupts	0yE0–0yE1

y is VIS page, $y \neq 0$.

Interrupts (Continued)

Two bytes of program memory space are reserved for each interrupt source. All interrupt sources except the software interrupt are maskable. Each of the maskable interrupts have an Enable bit and a Pending bit. A maskable interrupt is active if its associated enable and pending bits are set. If GIE = 1 and an interrupt is active, then the processor will be interrupted as soon as it is ready to start executing an instruction except if the above conditions happen during the Software Trap service routine. This exception is described in the Software Trap sub-section.

The interruption process is accomplished with the INTR instruction (opcode 00), which is jammed inside the Instruction Register and replaces the opcode about to be executed. The following steps are performed for every interrupt:

1. The GIE (Global Interrupt Enable) bit is reset.
2. The address of the instruction about to be executed is pushed into the stack.
3. The PC (Program Counter) branches to address 00FF. This procedure takes 7 t_C cycles to execute.

At this time, since GIE = 0, other maskable interrupts are disabled. The user is now free to do whatever context switching is required by saving the context of the machine in the stack with PUSH instructions. The user would then program a VIS (Vector Interrupt Select) instruction in order to branch to the interrupt service routine of the highest priority interrupt enabled and pending at the time of the VIS. Note that this is not necessarily the interrupt that caused the branch to address location 00FF Hex prior to the context switching.

Thus, if an interrupt with a higher rank than the one which caused the interruption becomes active before the decision of which interrupt to service is made by the VIS, then the interrupt with the higher rank will override any lower ones and will be acknowledged. The lower priority interrupt(s) are still pending, however, and will cause another interrupt immediately following the completion of the interrupt service routine associated with the higher priority interrupt just serviced. This lower priority interrupt will occur immediately following the RETI (Return from Interrupt) instruction at the end of the interrupt service routine just completed.

Inside the interrupt service routine, the associated pending bit has to be cleared by software. The RETI (Return from Interrupt) instruction at the end of the interrupt service routine will set the GIE (Global Interrupt Enable) bit, allowing the processor to be interrupted again if another interrupt is active and pending.

The VIS instruction looks at all the active interrupts at the time it is executed and performs an indirect jump to the beginning of the service routine of the one with the highest rank.

The addresses of the different interrupt service routines, called vectors, are chosen by the user and stored in ROM in a table starting at 01E0 (assuming that VIS is located between 00FF and 01DF). The vectors are 15-bit wide and therefore occupy 2 ROM locations.

VIS and the vector table must be located in the same 256-byte block (0y00 to 0yFF) except if VIS is located at the last address of a block. In this case, the table must be in the next block. The vector table cannot be inserted in the first 256-byte block.

The vector of the maskable interrupt with the lowest rank is located at 0yE0 (Hi-Order byte) and 0yE1 (Lo-Order byte) and so forth in increasing rank number. The vector of the maskable interrupt with the highest rank is located at 0yFA (Hi-Order byte) and 0yFB (Lo-Order byte).

The Software Trap has the highest rank and its vector is located at 0yFE and 0yFF.

If, by accident, a VIS gets executed and no interrupt is active, then the PC (Program Counter) will branch to a vector located at 0yE0–0yE1. This vector can point to the Software Trap (ST) interrupt service routine, or to another special service routine as desired.

Figure 11 shows the COP888CL Interrupt block diagram.

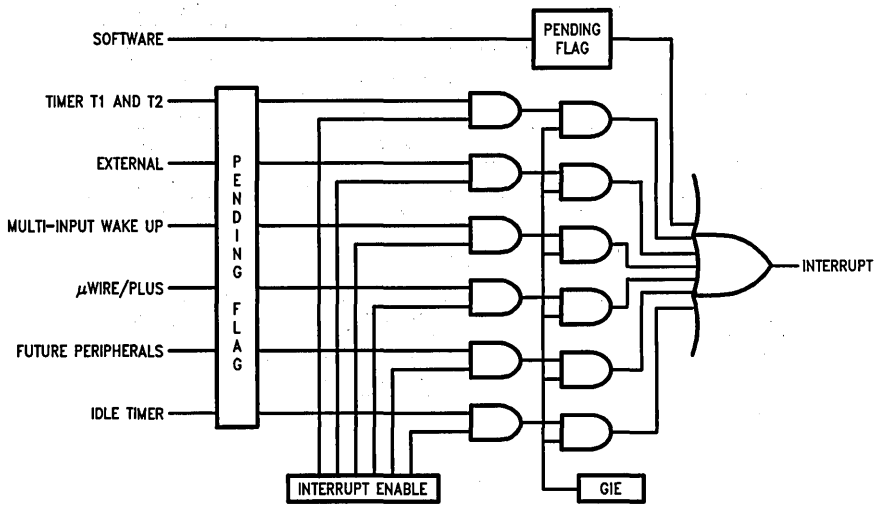

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FIGURE 11. COP888CL Interrupt Block Diagram

Interrupts (Continued)

SOFTWARE TRAP

The Software Trap (ST) is a special kind of non-maskable interrupt which occurs when the INTR instruction (used to acknowledge interrupts) is fetched from ROM and placed inside the instruction register. This may happen when the PC is pointing beyond the available ROM address space or when the stack is over-popped.

When an ST occurs, the user can re-initialize the stack pointer and do a recovery procedure (similar to reset, but not necessarily containing all of the same initialization procedures) before restarting.

The occurrence of an ST is latched into the ST pending bit. The GIE bit is not affected and the ST pending bit **(not accessible by the user)** is used to inhibit other interrupts and to direct the program to the ST service routine with the VIS instruction. The RPND instruction is used to clear the software interrupt pending bit. This pending bit is also cleared on reset.

The ST has the highest rank among all interrupts.

Nothing (except another ST) can interrupt an ST being serviced.

WATCHDOG

The COP888CL contains a WATCHDOG and clock monitor. The WATCHDOG is designed to detect the user program getting stuck in infinite loops resulting in loss of program control or "runaway" programs. The Clock Monitor is used to detect the absence of a clock or a very slow clock below a specified rate on the CKI pin.

The WATCHDOG consists of two independent logic blocks: WD UPPER and WD LOWER. WD UPPER establishes the upper limit on the service window and WD LOWER defines the lower limit of the service window.

Servicing the WATCHDOG consists of writing a specific value to a WATCHDOG Service Register named WDSVR which is memory mapped in the RAM. This value is composed of three fields, consisting of a 2-bit Window Select, a 5-bit Key Data field, and the 1-bit Clock Monitor Select field. Table I shows the WDSVR register.

The lower limit of the service window is fixed at 2048 instruction cycles. Bits 7 and 6 of the WDSVR register allow the user to pick an upper limit of the service window.

Table II shows the four possible combinations of lower and upper limits for the WATCHDOG service window. This flexibility in choosing the WATCHDOG service window prevents any undue burden on the user software.

Bits 5, 4, 3, 2 and 1 of the WDSVR register represent the 5-bit Key Data field. The key data is fixed at 01100. Bit 0 of the WDSVR Register is the Clock Monitor Select bit.

TABLE I. WATCHDOG Service Register (WDSVR)

Window Select		Key Data					Clock Monitor
X	X	0	1	1	0	0	Y
7	6	5	4	3	2	1	0

TABLE II. WATCHDOG Service Window Select

WDSVR Bit 7	WDSVR Bit 6	Service Window (Lower-Upper Limits)
0	0	2k-8k t_c Cycles
0	1	2k-16k t_c Cycles
1	0	2k-32k t_c Cycles
1	1	2k-64k t_c Cycles

Clock Monitor

The Clock Monitor aboard the COP888CL can be selected or deselected under program control. The Clock Monitor is guaranteed not to reject the clock if the instruction cycle clock ($1/t_c$) is greater or equal to 10 kHz. This equates to a clock input rate on CKI of greater or equal to 100 kHz.

WATCHDOG Operation

The WATCHDOG and Clock Monitor are disabled during reset. The COP888CL comes out of reset with the WATCHDOG armed, the WATCHDOG Window Select bits (bits 6, 7 of the WDSVR Register) set, and the Clock Monitor bit (bit 0 of the WDSVR Register) enabled. Thus, a Clock Monitor error will occur after coming out of reset, if the instruction cycle clock frequency has not reached a minimum specified value, including the case where the oscillator fails to start.

The WDSVR register can be written to only once after reset and the key data (bits 5 through 1 of the WDSVR Register) must match to be a valid write. This write to the WDSVR register involves two irrevocable choices: (i) the selection of the WATCHDOG service window (ii) enabling or disabling of the Clock Monitor. Hence, the first write to WDSVR Register involves selecting or deselecting the Clock Monitor, select the WATCHDOG service window and match the WATCHDOG key data. Subsequent writes to the WDSVR register will compare the value being written by the user to the WATCHDOG service window value and the key data (bits 7 through 1) in the WDSVR Register. Table III shows the sequence of events that can occur.

The user must service the WATCHDOG at least once before the upper limit of the serivce window expires. The WATCHDOG may not be serviced more than once in every lower limit of the service window. The user may service the WATCHDOG as many times as wished in the time period between the lower and upper limits of the service window. The first write to the WDSVR Register is also counted as a WATCHDOG service.

The WATCHDOG has an output pin associated with it. This is the WDOUT pin, on pin 1 of the port G. WDOUT is active low. The WDOUT pin is in the high impedance state in the inactive state. Upon triggering the WATCHDOG, the logic will pull the WDOUT (G1) pin low for an additional 16 t_c–32 t_c cycles after the signal level on WDOUT pin goes below the lower Schmitt trigger threshold. After this delay, the COP888CL will stop forcing the WDOUT output low.

The WATCHDOG service window will restart when the WDOUT pin goes high It is recommended that the user tie the WDOUT pin back to V_{CC} through a resistor in order to pull WDOUT high.

A WATCHDOG service while the WDOUT signal is active will be ignored. The state of the WDOUT pin is not guaranteed on reset, but if it powers up low then the WATCHDOG will time out and WDOUT will enter high impedance state.

WATCHDOG Operation (Continued)

TABLE III. WATCHDOG Service Actions

Key Data	Window Data	Clock Monitor	Action
Match	Match	Match	Valid Service: Restart Service Window
Don't Care	Mismatch	Don't Care	Error: Generate WATCHDOG Output
Mismatch	Don't Care	Don't Care	Error: Generate WATCHDOG Output
Don't Care	Don't Care	Mismatch	Error: Generate WATCHDOG Output

TABLE IV. MICROWIRE/PLUS Master Mode Clock Select

SL1	SL0	SK
0	0	$2 \times t_c$
0	1	$4 \times t_c$
1	x	$8 \times t_c$

Where t_c is the instruction cycle clock

The Clock Monitor forces the G1 pin low upon detecting a clock frequency error. The Clock Monitor error will continue until the clock frequency has reached the minimum specified value, after which the G1 output will enter the high impedance TRI-STATE mode following 16 t_c–32 t_c clock cycles. The Clock Monitor generates a continual Clock Monitor error if the oscillator fails to start, or fails to reach the minimum specified frequency. The specification for the Clock Monitor is as follows:

$1/t_c > 10$ kHz—No clock rejection.

$1/t_c < 10$ Hz—Guaranteed clock rejection.

WATCHDOG AND CLOCK MONITOR SUMMARY

The following salient points regarding the COP888 WATCHDOG and Clock Monitor should be noted:

- Both WATCHDOG and Clock Monitor detector circuits are inhibited during reset.
- Following reset, the WATCHDOG and Clock Monitor are both enabled, with the WATCHDOG having the maximum service window selected.
- The WATCHDOG service window and Clock Monitor enable/disable option can only be changed once, during the initial WATCHDOG service following reset.
- The initial WATCHDOG service must match the key data value in the WATCHDOG Service register WDSVR in order to avoid a WATCHDOG error.
- Subsequent WATCHDOG services must match all three data fields in WDSVR in order to avoid WATCHDOG errors.
- The correct key data value cannot be read from the WATCHDOG Service register WDSVR. Any attempt to read this key data value of 01100 from WDSVR will read as key data value of all 0's.
- The WATCHDOG detector circuit is inhibited during both the HALT and IDLE modes.
- The Clock Monitor detector circuit is active during both the HALT and IDLE modes. Consequently, the COP888 inadvertently entering the HALT mode will be detected as a Clock Monitor error (provided that the Clock Monitor enable option has been selected by the program).
- With the single-pin R/C oscillator mask option selected and the CLKDLY bit reset, the WATCHDOG service window will resume following HALT mode from where it left off before entering the HALT mode.
- With the crystal oscillator mask option selected, or with the single-pin R/C oscillator mask option selected and the CLKDLY bit set, the WATCHDOG service window will be set to its selected value from WDSVR following HALT. Consequently, the WATCHDOG should not be serviced for at least 2048 instruction cycles following HALT, but must be serviced within the selected window to avoid a WATCHDOG error.
- The IDLE timer T0 is not initialized with reset.
- The user can sync in to the IDLE counter cycle with an IDLE counter (T0) interrupt or by monitoring the T0PND flag. The T0PND flag is set whenever the thirteenth bit of the IDLE counter toggles (every 4096 instruction cycles). The user is responsible for resetting the T0PND flag.
- A hardware WATCHDOG service occurs just as the COP888 exits the IDLE mode. Consequently, the Watchdog should not be serviced for at least 2048 instruction cycles following IDLE, but must be serviced within the selected window to avoid a WATCHDOG error.
- Following reset, the initial WATCHDOG service (where the service window and the Clock Monitor enable/disable must be selected) may be programmed anywhere within the maximum service window (65,536 instruction cycles) initialized by RESET. Note that this initial WATCHDOG service may be programmed within the initial 2048 instruction cycles without causing a WATCHDOG error.

Detection of Illegal Conditions

The COP888CL can detect various illegal conditions resulting from coding errors, transient noise, power supply voltage drops, runaway programs, etc.

Reading of undefined ROM gets zeros. The opcode for software interrupt is zero. If the program fetches instructions from undefined ROM, this will force a software interrupt, thus signaling that an illegal condition has occurred.

Detection of Illegal Conditions (Continued)

The subroutine stack grows down for each call (jump to subroutine), interrupt, or PUSH, and grows up for each return or POP. The stack pointer is initialized to RAM location 06F Hex during reset. Consequently, if there are more returns than calls, the stack pointer will point to addresses 070 and 071 Hex (which are undefined RAM). Undefined RAM from addresses 070 to 07F Hex is read as all 1's, which in turn will cause the program to return to address 7FFF Hex. This is an undefined ROM location and the instruction fetched (all 0's) from this location will generate a software interrupt signaling an illegal condition.

Thus, the chip can detect the following illegal conditions:

a. Executing from undefined ROM

b. Over "POP"ing the stack by having more returns than calls.

When the software interrupt occurs, the user can re-initialize the stack pointer and do a recovery procedure before restarting (this recovery program is probably similar to that following reset, but might not contain the same program initialization procedures). The recovery program should reset the software interrupt pending bit using the RPND instruction.

MICROWIRE/PLUS

MICROWIRE/PLUS is a serial synchronous communications interface. The MICROWIRE/PLUS capability enables the COP888CL to interface with any of National Semiconductor's MICROWIRE peripherals (i.e. A/D converters, display drivers, E^2PROMs etc.) and with other microcontrollers which support the MICROWIRE interface. It consists of an 8-bit serial shift register (SIO) with serial data input (SI), serial data output (SO) and serial shift clock (SK). *Figure 12* shows a block diagram of the MICROWIRE logic.

The shift clock can be selected from either an internal source or an external source. Operating the MICROWIRE/PLUS arrangement with the internal clock source is called the Master mode of operation. Similarly, operating the MICROWIRE arrangement with an external shift clock is called the Slave mode of operation.

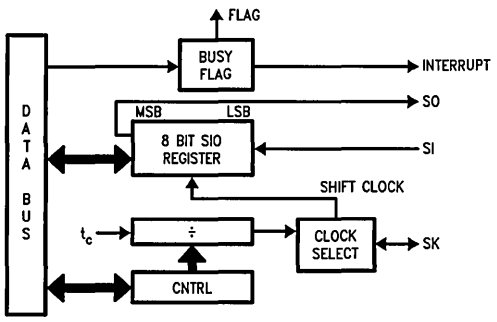

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FIGURE 12. MICROWIRE/PLUS Block Diagram

The CNTRL register is used to configure and control the MICROWIRE/PLUS mode. To use the MICROWIRE/PLUS, the MSEL bit in the CNTRL register is set to one. In the master mode, the SK clock rate is selected by the two bits, SL0 and SL1, in the CNTRL register. Table IV details the different clock rates that may be selected.

MICROWIRE/PLUS OPERATION

Setting the BUSY bit in the PSW register causes the MICROWIRE/PLUS to start shifting the data. It gets reset when eight data bits have been shifted. The user may reset the BUSY bit by software to allow less than 8 bits to shift. If enabled, an interrupt is generated when eight data bits have been shifted. The COP888CL may enter the MICROWIRE/PLUS mode either as a Master or as a Slave. *Figure 13* shows how two COP888CL microcontrollers and several peripherals may be interconnected using the MICROWIRE/PLUS arrangements.

Warning:

The SIO register should only be loaded when the SK clock is low. Loading the SIO register while the SK clock is high will result in undefined data in the SIO register. The SK clock is normally low when not shifting.

Setting the BUSY flag when the input SK clock is high in the MICROWIRE/PLUS slave mode may cause the current SK clock forthe SIO shift register to be narrow. For safety, the BUSY flag should only be set when the input SK clock is low.

MICROWIRE/PLUS Master Mode Operation

In the MICROWIRE/PLUS Master mode of operation the shift clock (SK) is generated internally by the COP888CL. The MICROWIRE Master always initiates all data exchanges. The MSEL bit in the CNTRL register must be set to enable the SO and SK functions onto the G Port. The SO and SK pins must also be selected as outputs by setting appropriate bits in the Port G configuration register. Table V summarizes the bit settings required for Master mode of operation.

MICROWIRE/PLUS Slave Mode Operation

In the MICROWIRE/PLUS Slave mode of operation the SK clock is generated by an external source. Setting the MSEL bit in the CNTRL register enables the SO and SK functions onto the G Port. The SK pin must be selected as an input and the SO pin is selected as an output pin by setting and resetting the appropriate bit in the Port G configuration register. Table V summarizes the settings required to enter the Slave mode of operation.

The user must set the BUSY flag immediately upon entering the Slave mode. This will ensure that all data bits sent by the Master will be shifted properly. After eight clock pulses the BUSY flag will be cleared and the sequence may be repeated.

Alternate SK Phase Operation

The COP888CL allows either the normal SK clock or an alternate phase SK clock to shift data in and out of the SIO register. In both the modes the SK is normally low. In the normal mode data is shifted in on the rising edge of the SK clock and the data is shifted out on the falling edge of the SK clock. The SIO register is shifted on each falling edge of the SK clock. In the alternate SK phase operation, data is shifted in on the falling edge of the SK clock and shifted out on the rising edge of the SK clock.

MICROWIRE/PLUS (Continued)

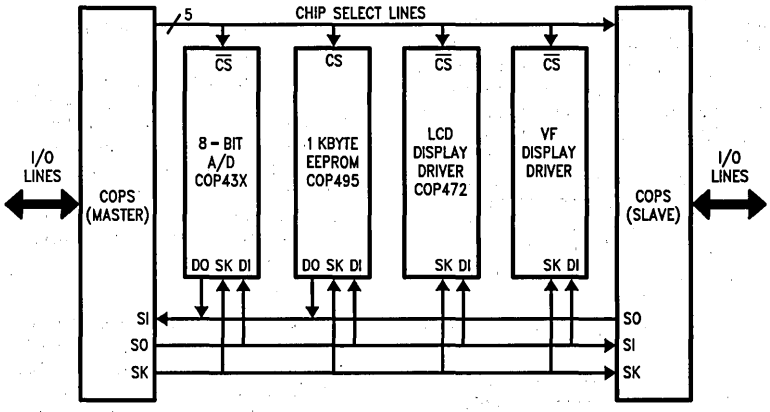

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FIGURE 13. MICROWIRE/PLUS Application

A control flag, SKSEL, allows either the normal SK clock or the alternate SK clock to be selected. Resetting SKSEL causes the MICROWIRE/PLUS logic to be clocked from the normal SK signal. Setting the SKSEL flag selects the alternate SK clock. The SKSEL is mapped into the G6 configuration bit. The SKSEL flag will power up in the reset condition, selecting the normal SK signal.

TABLE V

This table assumes that the control flag MSEL is set.

G4 (SO) Config. Bit	G5 (SK) Config. Bit	G4 Fun.	G5 Fun.	Operation
1	1	SO	Int. SK	MICROWIRE/PLUS Master
0	1	TRI-STATE	Int. SK	MICROWIRE/PLUS Master
1	0	SO	Ext. SK	MICROWIRE/PLUS Slave
0	0	TRI-STATE	Ext. SK	MICROWIRE/PLUS Slave

Memory Map

All RAM, ports and registers (except A and PC) are mapped into data memory address space

Address	Contents
00 to 6F	On-Chip RAM bytes
70 to BF	Unused RAM Address Space
C0	Timer T2 Lower Byte
C1	Timer T2 Upper Byte
C2	Timer T2 Autoload Register T2RA Lower Byte
C3	Timer T2 Autoload Register T2RA Upper Byte
C4	Timer T2 Autoload Register T2RB Lower Byte
C5	Timer T2 Autoload Register T2RB Upper Byte
C6	Timer T2 Control Register
C7	WATCHDOG Service Register (Reg:WDSVR)
C8	MIWU Edge Select Register (Reg:WKEDG)
C9	MIWU Enable Register (Reg:WKEN)
CA	MIWU Pending Register (Reg:WKPND)
CB	Reserved
CC	Reserved
CD to CF	Reserved
D0	Port L Data Register
D1	Port L Configuration Register
D2	Port L Input Pins (Read Only)
D3	Reserved for Port L
D4	Port G Data Register
D5	Port G Configuration Register
D6	Port G Input Pins (Read Only)
D7	Port I Input Pins (Read Only)
D8	Port C Data Register
D9	Port C Configuration Register
DA	Port C Input Pins (Read Only)
DB	Reserved for Port C
DC	Port D Data Register
DD to DF	Reserved for Port D
E0 to E5	Reserved
E6	Timer T1 Autoload Register T1RB Lower Byte
E7	Timer T1 Autoload Register T1RB Upper Byte
E8	ICNTRL Register
E9	MICROWIRE Shift Register
EA	Timer T1 Lower Byte
EB	Timer T1 Upper Byte
EC	Timer T1 Autoload Register T1RA Lower Byte
ED	Timer T1 Autoload Register T1RA Upper Byte
EE	CNTRL Control Register
EF	PSW Register
F0 to FB	On-Chip RAM Mapped as Registers
FC	X Register
FD	SP Register
FE	B Register
FF	Reserved

Reading memory locations 70-7F Hex will return all ones. Reading other unused memory locations will return undefined data.

Addressing Modes

The COP888CL has ten addressing modes, six for operand addressing and four for transfer of control.

OPERAND ADDRESSING MODES

Register Indirect

This is the "normal" addressing mode for the COP888CL. The operand is the data memory addressed by the B pointer or X pointer.

Register Indirect (with auto post increment or decrement of pointer)

This addressing mode is used with the LD and X instructions. The operand is the data memory addressed by the B pointer or X pointer. This is a register indirect mode that automatically post increments or decrements the B or X register after executing the instruction.

Direct

The instruction contains an 8-bit address field that directly points to the data memory for the operand.

Immediate

The instruction contains an 8-bit immediate field as the operand.

Short Immediate

This addressing mode is used with the Load B Immediate instruction. The instruction contains a 4-bit immediate field as the operand.

Indirect

This addressing mode is used with the LAID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a data operand from the program memory.

TRANSFER OF CONTROL ADDRESSING MODES

Relative

This mode is used for the JP instruction, with the instruction field being added to the program counter to get the new program location. JP has a range from −31 to +32 to allow a 1-byte relative jump (JP + 1 is implemented by a NOP instruction). There are no "pages" when using JP, since all 15 bits of PC are used.

Absolute

This mode is used with the JMP and JSR instructions, with the instruction field of 12 bits replacing the lower 12 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory segment.

Absolute Long

This mode is used with the JMPL and JSRL instructions, with the instruction field of 15 bits replacing the entire 15 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory space.

Indirect

This mode is used with the JID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a location in the program memory. The contents of this program memory location serve as a partial address (lower 8 bits of PC) for the jump to the next instruction.

Note: The VIS is a special case of the Indirect Transfer of Control addressing mode, where the double byte vector associated with the interrupt is transferred from adjacent addresses in the program memory into the program counter (PC) in order to jump to the associated interrupt service routine.

Instruction Set

Register and Symbol Definition

Registers	
A	8-Bit Accumulator Register
B	8-Bit Address Register
X	8-Bit Address Register
SP	8-Bit Stack Pointer Register
PC	15-Bit Program Counter Register
PU	Upper 7 Bits of PC
PL	Lower 8 Bits of PC
C	1 Bit of PSW Register for Carry
HC	1 Bit of PSW Register for Half Carry
GIE	1 Bit of PSW Register for Global Interrupt Enable
VU	Interrupt Vector Upper Byte
VL	Interrupt Vector Lower Byte

Symbols	
[B]	Memory Indirectly Addressed by B Register
[X]	Memory Indirectly Addressed by X Register
MD	Direct Addressed Memory
Mem	Direct Addressed Memory or [B]
Meml	Direct Addressed Memory or [B] or Immediate Data
Imm	8-Bit Immediate Data
Reg	Register Memory: Addresses F0 to FF (Includes B, X and SP)
Bit	Bit Number (0 to 7)
←	Loaded with
↔	Exchanged with

Instruction Set (Continued)

INSTRUCTION SET

ADD	A,Meml	ADD	A ← A + Meml
ADC	A,Meml	ADD with Carry	A ← A + Meml + C, C ← Carry HC ← Half Carry
SUBC	A,Meml	Subtract with Carry	A ← A − $\overline{\text{Meml}}$ + C, C ← Carry HC ← Half Carry
AND	A,Meml	Logical AND	A ← A and Meml
ANDSZ	A,Imm	Logical AND Immed., Skip if Zero	Skip next if (A and Imm) = 0
OR	A,Meml	Logical OR	A ← A or Meml
XOR	A,Meml	Logical EXclusive OR	A ← A xor Meml
IFEQ	MD,Imm	IF EQual	Compare MD and Imm, Do next if MD = Imm
IFEQ	A,Meml	IF EQual	Compare A and Meml, Do next if A = Meml
IFNE	A,Meml	IF Not Equal	Compare A and Meml, Do next if A ≠ Meml
IFGT	A,Meml	IF Greater Than	Compare A and Meml, Do next if A > Meml
IFBNE	#	If B Not Equal	Do next if lower 4 bits of B ≠ Imm
DRSZ	Reg	Decrement Reg., Skip if Zero	Reg ← Reg − 1, Skip if Reg = 0
SBIT	#,Mem	Set BIT	1 to bit, Mem (bit = 0 to 7 immediate)
RBIT	#,Mem	Reset BIT	0 to bit, Mem
IFBIT	#,Mem	IF BIT	If bit in A or Mem is true do next instruction
RPND		Reset PeNDing Flag	Reset Software Interrupt Pending Flag
X	A,Mem	EXchange A with Memory	A ⟷ Mem
X	A,[X]	EXchange A with Memory [X]	A ⟷ [X]
LD	A,Meml	LoaD A with Memory	A ← Meml
LD	A,[X]	LoaD A with Memory [X]	A ← [X]
LD	B,Imm	LoaD B with Immed.	B ← Imm
LD	Mem,Imm	LoaD Memory Immed	Mem ← Imm
LD	Reg,Imm	LoaD Register Memory Immed.	Reg ← Imm
X	A, [B ±]	EXchange A with Memory [B]	A ⟷ [B], (B ← B ± 1)
X	A, [X ±]	EXchange A with Memory [X]	A ⟷ [X], (X ← ±1)
LD	A, [B ±]	LoaD A with Memory [B]	A ← [B], (B ← B ± 1)
LD	A, [X ±]	LoaD A with Memory [X]	A ← [X], (X ← X ± 1)
LD	[B ±],Imm	LoaD Memory [B] Immed.	[B] ← Imm, (B ← ±1)
CLR	A	CLeaR A	A ← 0
INC	A	INCrement A	A ← A + 1
DEC	A	DECrementA	A ← A − 1
LAID		Load A InDirect from ROM	A ← ROM (PU,A)
DCOR	A	Decimal CORrect A	A ← BCD correction of A (follows ADC, SUBC)
RRC	A	Rotate A Right thru C	C ⟷ A7 ⟷ . . . ⟷ A0 ⟷ C
RLC	A	Rotate A Left thru C	C ← A7 ← . . . ← A0 ← C
SWAP	A	SWAP nibbles of A	A7 . . . A4 ⟷ A3 . . . A0
SC		Set C	C ← 1, HC ← 1
RC		Reset C	C ← 0, HC ← 0
IFC		IF C	IF C is true, do next instruction
IFNC		IF Not C	If C is not true, do next instruction
POP	A	POP the stack into A	SP ← SP + 1, A ← [SP]
PUSH	A	PUSH A onto the stack	[SP] ← A, SP ← SP − 1
VIS		Vector to Interrupt Service Routine	PU ← [VU], PL ← [VL]
JMPL	Addr.	Jump absolute Long	PC ← ii (ii = 15 bits, 0 to 32k)
JMP	Addr.	Jump absolute	PC9 . . . 0 ← i (i = 12 bits)
JP	Disp.	Jump relative short	PC ← PC + r (r is −31 to +32, except 1)
JSRL	Addr.	Jump SubRoutine Long	[SP] ← PL, [SP−1] ← PU,SP−2, PC ← ii
JSR	Addr	Jump SubRoutine	[SP] ← PL, [SP−1] ← PU,SP−2, PC9 . . . 0 ← i
JID		Jump InDirect	PL ← ROM (PU,A)
RET		RETurn from subroutine	SP+2, PL ← [SP], PU ← [SP−1]
RETSK		RETurn and SKip	SP+2, PL ← [SP],PU ← [SP−1]
RETI		RETurn from Interrupt	SP+2, PL ← [SP],PU ← [SP−1],GIE ← 1
INTR		Generate an Interrupt	[SP] ← PL, [SP−1] ← PU, SP−2, PC ← 0FF
NOP		No OPeration	PC ← PC+1

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Instruction Execution Time

Most instructions are single byte (with immediate addressing mode instructions taking two bytes).

Most single byte instructions take one cycle time to execute.

See the BYTES and CYCLES per INSTRUCTION table for details.

Bytes and Cycles per Instruction

The following table shows the number of bytes and cycles for each instruction in the format of byte/cycle.

	[B]	Direct	Immed.
ADD	1/1	3/4	2/2
ADC	1/1	3/4	2/2
SUBC	1/1	3/4	2/2
AND	1/1	3/4	2/2
OR	1/1	3/4	2/2
XOR	1/1	3/4	2/2
IFEQ	1/1	3/4	2/2
IFNE	1/1	3/4	2/2
IFGT	1/1	3/4	2/2
IFBNE	1/1		
DRSZ		1/3	
SBIT	1/1	3/4	
RBIT	1/1	3/4	
IFBIT	1/1	3/4	

RPND	1/1

Instructions Using A & C

CLRA	1/1
INCA	1/1
DECA	1/1
LAID	1/3
DCOR	1/1
RRCA	1/1
RLCA	1/1
SWAPA	1/1
SC	1/1
RC	1/1
IFC	1/1
IFNC	1/1
PUSHA	1/3
POPA	1/3
ANDSZ	2/2

Transfer of Control Instructions

JMPL	3/4
JMP	2/3
JP	1/3
JSRL	3/5
JSR	2/5
JID	1/3
VIS	1/5
RET	1/5
RETSK	1/5
RETI	1/5
INTR	1/7
NOP	1/1

Memory Transfer Instructions

	Register Indirect		Direct	Immed.	Register Indirect Auto Incr. & Decr.		
	[B]	[X]			[B+, B−]	[X+, X−]	
X A,*	1/1	1/3	2/3		1/2	1/3	
LD A,*	1/1	1/3	2/3	2/2	1/2	1/3	
LD B, Imm				1/1			(IF B < 16)
LD B, Imm				2/2			(IF B > 15)
LD Mem, Imm	2/2		3/3		2/2		
LD Reg, Imm			2/3				
IFEQ MD, Imm			3/3				

* = > Memory location addressed by B or X or directly.

COP888CL Opcode Table

Upper Nibble Along X-Axis

Lower Nibble Along Y-Axis

F	E	D	C	B	A	9	8	
JP −15	JP −31	LD 0F0, # i	DRSZ 0F0	RRCA	RC	ADC A, #i	ADC A,[B]	0
JP −14	JP −30	LD 0F1, # i	DRSZ 0F1	*	SC	SUBC A, #i	SUB A,[B]	1
JP −13	JP −29	LD 0F2, # i	DRSZ 0F2	X A, [X+]	X A,[B+]	IFEQ A,#i	IFEQ A,[B]	2
JP −12	JP −28	LD 0F3, # i	DRSZ 0F3	X A, [X−]	X A,[B−]	IFGT A,#i	IFGT A,[B]	3
JP −11	JP −27	LD 0F4, # i	DRSZ 0F4	VIS	LAID	ADD A,#i	ADD A,[B]	4
JP −10	JP −26	LD 0F5, # i	DRSZ 0F5	RPND	JID	AND A,#i	AND A,[B]	5
JP −9	JP −25	LD 0F6, # i	DRSZ 0F6	X A,[X]	X A,[B]	XOR A,#i	XOR A,[B]	6
JP −8	JP −24	LD 0F7, # i	DRSZ 0F7	*	*	OR A,#i	OR A,[B]	7
JP −7	JP −23	LD 0F8, # i	DRSZ 0F8	NOP	RLCA	LD A,#i	IFC	8
JP −6	JP −22	LD 0F9, # i	DRSZ 0F9	IFNE A,[B]	IFEQ Md,#i	IFNE A,#i	IFNC	9
JP −5	JP −21	LD 0FA, # i	DRSZ 0FA	LD A,[X+]	LD A,[B+]	LD [B+],#i	INCA	A
JP −4	JP −20	LD 0FB, # i	DRSZ 0FB	LD A,[X−]	LD A,[B−]	LD [B−],#i	DECA	B
JP −3	JP −19	LD 0FC, # i	DRSZ 0FC	LD Md,#i	JMPL	X A,Md	POPA	C
JP −2	JP −18	LD 0FD, # i	DRSZ 0FD	DIR	JSRL	LD A,Md	RETSK	D
JP −1	JP −17	LD 0FE, # i	DRSZ 0FE	LD A,[X]	LD A,[B]	LD [B],#i	RET	E
JP −0	JP −16	LD 0FF, # i	DRSZ 0FF	*	*	LD B,#i	RETI	F

COP888CL Opcode Table (Continued)

Upper Nibble Along X-Axis

Lower Nibble Along Y-Axis

7	6	5	4	3	2	1	0	
IFBIT 0,[B]	ANDSZ A, #i	LD B,#0F	IFBNE 0	JSR x000–x0FF	JMP x000–x0FF	JP +17	INTR	0
IFBIT 1,[B]	*	LD B,#0E	IFBNE 1	JSR x100–x1FF	JMP x100–x1FF	JP +18	JP + 2	1
IFBIT 2,[B]	*	LD B,#0D	IFBNE 2	JSR x200–x2FF	JMP x200–x2FF	JP +19	JP + 3	2
IFBIT 3,[B]	*	LD B,#0C	IFBNE 3	JSR x300–x3FF	JMP x300–x3FF	JP +20	JP + 4	3
IFBIT 4,[B]	CLRA	LD B,#0B	IFBNE 4	JSR x400–x4FF	JMP x400–x4FF	JP +21	JP + 5	4
IFBIT 5,[B]	SWAPA	LD B,#0A	IFBNE 5	JSR x500–x5FF	JMP x500–x5FF	JP +22	JP + 6	5
IFBIT 6,[B]	DCORA	LD B,#09	IFBNE 6	JSR x600–x6FF	JMP x600–x6FF	JP +23	JP + 7	6
IFBIT 7,[B]	PUSHA	LD B,#08	IFBNE 7	JSR x700–x7FF	JMP x700–x7FF	JP +24	JP + 8	7
SBIT 0,[B]	RBIT 0,[B]	LD B,#07	IFBNE 8	JSR x800–x8FF	JMP x800–x8FF	JP +25	JP + 9	8
SBIT 1,[B]	RBIT 1,[B]	LD B,#06	IFBNE 9	JSR x900–x9FF	JMP x900–x9FF	JP +26	JP + 10	9
SBIT 2,[B]	RBIT 2,[B]	LD B,#05	IFBNE 0A	JSR xA00–xAFF	JMP xA00–xAFF	JP +27	JP + 11	A
SBIT 3,[B]	RBIT 3,[B]	LD B,#04	IFBNE 0B	JSR xB00–xBFF	JMP xB00–xBFF	JP +28	JP + 12	B
SBIT 4,[B]	RBIT 4,[B]	LD B,#03	IFBNE 0C	JSR xC00–xCFF	JMP xC00–xCFF	JP +29	JP + 13	C
SBIT 5,[B]	RBIT 5,[B]	LD B,#02	IFBNE 0D	JSR xD00–xDFF	JMP xD00–xDFF	JP +30	JP + 14	D
SBIT 6,[B]	RBIT 6,[B]	LD B,#01	IFBNE 0E	JSR xE00–xEFF	JMP xE00–xEFF	JP +31	JP + 15	E
SBIT 7,[B]	RBIT 7,[B]	LD B,#00	IFBNE 0F	JSR xF00–xFFF	JMP xF00–xFFF	JP +32	JP + 16	F

Where,

i is the immediate data

Md is a directly addressed memory location

* is an unused opcode

Note: The opcode 60 Hex is also the opcode for IFBIT #i,A

Mask Options

The COP888CL mask programmable options are shown below. The options are programmed at the same time as the ROM pattern submission.

```
OPTION 1: CLOCK CONFIGURATION
  = 1     Crystal Oscillator (CKI/10)
              G7 (CKO) is clock generator
              output to crystal/resonator
              CKI is the clock input
  = 2     Single-pin RC controlled
              oscillator (CKI/10)
              G7 is available as a HALT
              restart and/or general purpose
              input

OPTION 2: HALT
  = 1     Enable HALT mode
  = 2     Disable HALT mode

OPTION 3: COP888CL BONDING
  = 1     44-Pin PCC
  = 2     40-Pin DIP
  = 3     N.A.
  = 4     28-Pin DIP
  = 5     28-Pin SO
```

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (if clock option-1 has been selected). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_c$).

Development Support

IN-CIRCUIT EMULATOR

The MetaLink iceMASTER™-COP8 Model 400 In-Circuit Emulator for the COP8 family of microcontrollers features high-performance operation, ease of use, and an extremely flexible user-interface for maximum productivity. Interchangeable probe cards, which connect to the standard common base, support the various configurations and packages of the COP8 family.

The iceMASTER provides real-time, full-speed emulation, up to 10 MHz, 32 kBytes of emulation memory and 4k frames of trace buffer memory. The user may define as many as 32k trace and break triggers which can be enabled, disabled, set or cleared. They can be simple triggers based on code or address ranges or complex triggers based on code address, direct address, opcode value, opcode class or immediate operand. Complex breakpoints can be ANDed and ORed together. Trace information consists of address bus values, opcodes and user-selectable probe clips status (external event lines). The trace buffer can be viewed as raw hex or as disassembled instructions. The probe clip bit values can be displayed in binary, hex or digital waveform formats.

During single-step operation the dynamically annotated code feature displays the contents of all accessed (read and write) memory locations and registers, as well as flow-of-control direction change markers next to each instruction executed.

The iceMASTER's performance analyzer offers a resolution of better than 6 μs. The user can easily monitor the time spent executing specific portions of code and find "hot spots" or "dead code". Up to 15 independent memory areas based on code address or label ranges can be defined. Analysis results can be viewed in bar graph format or as actual frequency count.

Emulator memory operations for program memory include single line assembler, disassembler, view, change and write to file. Data memory operations include fill, move, compare, dump to file, examine and modify. The contents of any memory space can be directly viewed and modified from the corresponding window.

The iceMASTER comes with an easy to use windowed interface. Each window can be sized, highlighted, color-controlled, added, or removed completely. Commands can be accessed via pull-down-menus and/or redefinable hot keys. A context sensitive hypertext/hyperlinked on-line help system explains clearly the options the user has from within any window.

The iceMASTER connects easily to a PC® via the standard COMM port and its 115.2 kBaud serial link keeps typical program download time to under 3 seconds.

The following tables list the emulator and probe cards ordering information.

Emulator Ordering Information

Part Number	Description
IM-COP8/400	MetaLink base unit in-circuit emulator for all COP8 devices, symbolic debugger software and RS 232 serial interface cable
MHW-PS3	Power Supply 110V/60 Hz
MHW-PS4	Power Supply 220V/50 Hz

Probe Card Ordering Information

Part Number	Package	Voltage Range	Emulates
MHW-884CL28D5PC	28 DIP	4.5V–5.5V	COP884CL
MHW-884CL28DWPC	28 DIP	2.5V–6.0V	COP884CL
MHW-888CL40D5PC	40 DIP	4.5V–5.5V	COP888CL
MHW-888CL40DWPC	40 DIP	2.5V–6.0V	COP888CL
MHW-888CL44D5PC	44 PLCC	4.5V–5.5V	COP888CL
MHW-888CL44DWPC	44 PLCC	2.5V–6.0V	COP888CL

MACRO CROSS ASSEMBLER

National Semiconductor offers a COP8 macro cross assembler. It runs on industry standard compatible PCs and supports all of the full-symbolic debugging features of the MetaLink iceMASTER emulators.

Assembler Ordering Information

Part Number	Description	Manual
MOLE-COP8-IBM	COP8 macro cross assembler for IBM® PC-XT®, PC-AT® or compatible	424410527-001

Development Support (Continued)

SIMULATOR

The COP8 Designer's Tool Kit is available for evaluating National Semiconductor's COP8 microcontroller family. The kit contains programmer's manuals, device datasheets, pocket reference guide, assembler and simulator, which allows the user to write, test, debug and run code on an industry standard compatible PC. The simulator has a windowed user interface and can handle script files that simulate hardware inputs, interrupts and automatic command processing. The capture file feature enables the user to record to a file current cycle and output port changes which are caused by the program under test.

Simulator Ordering Information

Part Number	Description	Manual
COP8-TOOL-KIT	COP8 Designer's Tool Kit Assembler and Simulator	420420270-001 424420269-001

SINGLE-CHIP EMULATOR DEVICE

The COP8 family is fully supported by single chip form, fit and function emulators. For more detailed information refer to the emulation device specific data sheets and the form, fit, function emulator selection table below.

PROGRAM SUPPORT

Programming of the single-chip emulator devices is supported by different sources. National Semiconductor offers a duplicator board which allows the transfer of program code from a standard programmed EPROM to the single-chip emulator and vice versa. Data I/O supports COP8 emulator device programming with its uniSite 48 and System 2900 programmers. Further information on Data I/O programmers can be obtained from any Data I/O sales office or the following USA numbers:

Telephone: (206) 881-6444 FAX: (206) 882-104

Duplicate Board Ordering Information

Part Number	Description	Devices Supported
COP8-PRGM-28D	Duplicator Board for 28 DIP Multi-Chip Module (MCM) and for use with Scrambler Boards	COP884CLMHD
COP8-SCRM-DIP	MCM Scrambler Board for 40 DIP Socket	COP888CLMHD
COP8-SCRM-PCC	MCM Scrambler Board for 44 PLCC/ LDCC	COP888CLMHEL
COP8-SCRM-SBX	MCM Scrambler Board for 28 LCC Socket	COP884CLMHEA
COP8-PRGM-DIP	Duplicator Board with COP8-SCRM-DIP Scrambler Board	COP884CLMHD, COP888CLMHD
COP8-PRGM-PCC	Duplicator Board with COP8-SCRM-PCC Scrambler Board	COP888CLMEL, COP884CLMHD

Single-Chip Emulator Selection Table

Device Number	Clock Option	Package	Description	Emulates
COP888CLMHEL-X	X = 1: crystal X = 3: R/C	44 LDCC	Multi-Chip Module (MCM), UV Erasable	COP888CL
COP888CLMHD-X	X = 1: crystal X = 3: R/C	40 DIP	MCM, UV Erasable	COP888CL
COP884CLMHD-X	X = 1: crystal X = 3: R/C	28 DIP	MCM, UV Erasable	COP884CL
COP884CLMHEA-X	X = 1: crystal X = 3: R/C	28 LCC	MCM (same footprint as 28 SO), UV Erasable	COP884CL

Development Support (Continued)

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications group. The Dial-A-Helper is an Electronic Bulletin Board Information System.

Order P/N: MOLE-DIAL-A-HLP

Information System Package Contents
- Dial-A-Helper User Manual P/N
- Public Domain Communications Software

Information System

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down loaded to disk for later use.

Factory Applications Support

Dial-A-Helper also provides immediate factor applications support. If a user has questions, he can leave messages on our electronic bulletin board, which we will respond to.

Voice: (408) 721-5582
Modem: (408) 739-1162
Baud: 300 or 1200 baud
Set-up: Length: 8-Bit
Parity: None
Stop Bit 1
Operation: 24 Hours, 7 Days

National Semiconductor

COP688CS/COP684CS/COP888CS/COP884CS/ COP988CS/COP984CS Single-Chip microCMOS Microcontroller

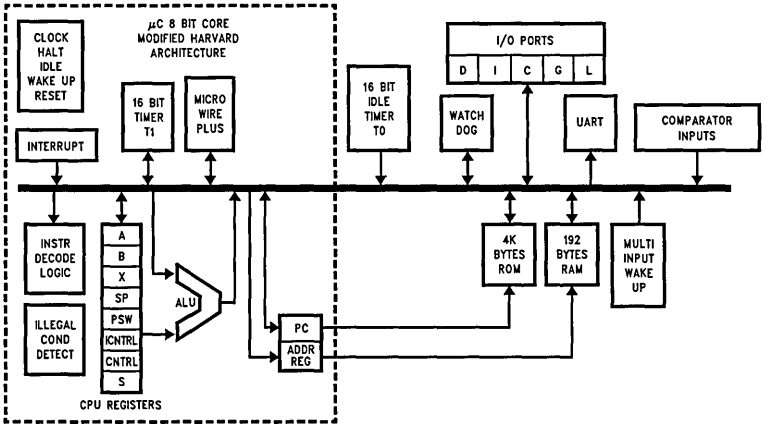
General Description

The COP888 family of microcontrollers uses an 8-bit single chip core architecture fabricated with National Semiconductor's M²CMOS™ process technology. The COP888CS is a member of this expandable 8-bit core processor family of microcontrollers. (Continued)

Features

- Low cost 8-bit microcontroller
- Fully static CMOS, with low current drain
- Two power saving modes: HALT and IDLE
- 1 μs instruction cycle time
- 4096 bytes on-board ROM
- 192 bytes on-board RAM
- Single supply operation: 2.5V–6V
- Full duplex UART
- One analog comparator
- MICROWIRE/PLUS™ serial I/O
- WATCHDOG™ and Clock Monitor logic
- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- One 16-bit timer, with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers (B and X)
- Ten multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Timer (2)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — UART (2)
  - — Default VIS
- Versatile instruction set
- True bit manipulation
- Memory mapped I/O
- BCD arithmetic instructions
- Package: 44 PLCC or 40 N or 28 N or 28 SOIC
  - — 44 PLCC with 39 I/O pins
  - — 40 N with 35 I/O pins
  - — 28 SO or 28 N, each with 23 I/O pins
- Software selectable I/O options
  - — TRI-STATE® Output
  - — Push-Pull Output
  - — Weak Pull Up Input
  - — High Impedance Input
- Schmitt trigger inputs on ports G and L
- Form factor emulation devices
- Real time emulation and full program debug offered by National's Development Systems
- For other COP800 devices with a UART see COP888CG and COP888EG

Block Diagram



TL/DD/10830–1

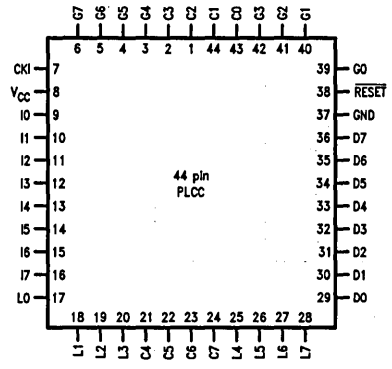
FIGURE 1. COP888CS Block Diagram

General Description (Continued)

It is a fully static part, fabricated using double-metal silicon gate microCMOS technology. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS serial I/O, one 16-bit timer/counter supporting three modes (Processor Independent PWM generation, External Event counter, and Input Capture mode capabilities), full duplex UART, one comparator, and two power savings modes (HALT and IDLE), both with a multi-sourced wakeup/interrupt capability. This multi-sourced interrupt capability may also be used independent of the HALT or IDLE modes. Each I/O pin has software selectable configurations. The COP888CS operates over a voltage range of 2.5V to 6V. High throughput is achieved with an efficient, regular instruction set operating at a maximum of 1 μs per instruction rate.

Connection Diagrams

Plastic Chip Carrier

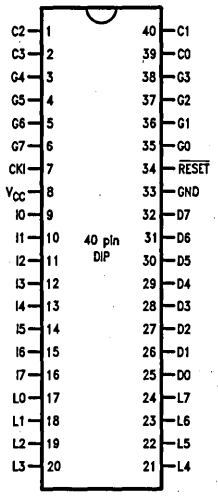


TL/DD/10830–2

Top View

Order Number COP888CS-XXX/V
See NS Package Number V44A

Dual-In-Line Package

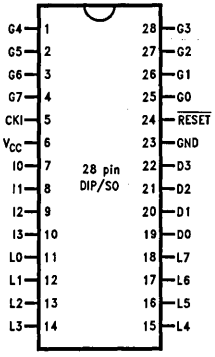


TL/DD/10830–3

Top View

Order Number COP888S-XXX/N
See NS Package Number N40A

Dual-In-Line Package



TL/DD/10830–5

Top View

Order Number COP884CS-XXX/N
See NS Package Number N28B

Order Number COP884CS-XXX/WM
See NS Package Number M28B

FIGURE 2. COP888CS Connection Diagrams

Connection Diagrams (Continued)

COP888CS Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU	CKX	12	18	18
L2	I/O	MIWU	TDX	13	19	19
L3	I/O	MIWU	RDX	14	20	20
L4	I/O	MIWU		15	21	25
L5	I/O	MIWU		16	22	26
L6	I/O	MIWU		17	23	27
L7	I/O	MIWU		18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
I0	I			7	9	9
I1	I	COMP1IN−		8	10	10
I2	I	COMP1IN+		9	11	11
I3	I	COMP1OUT		10	12	12
I4	I				13	13
I5	I				14	14
I6	I				15	15
I7	I				16	16
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics 98XCS: 0°C ≤ T_A ≤ +70°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage COP98XCS		2.5		4.0	V
COP98XCSH		4.0		6.0	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			5.5	mA
CKI = 4 MHz	V_{CC} = 4V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			1.4	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<0.7	8	μA
	V_{CC} = 4V, CKI = 0 MHz		<0.3	4	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			0.7	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6V, V_{IN} = 0V	−1		+1	μA
Input Pullup Current	V_{CC} = 6V, V_{IN} = 0V	40		250	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4V, V_{OL} = 1V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2.0			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4V, V_{OH} = 2.7V	10		100	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink (Push-Pull Mode)	V_{CC} = 4V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			mA
TRI-STATE Leakage	V_{CC} = 6.0V	−1		+1	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor and the comparators are disabled.

DC Electrical Characteristics 98XCS: 0°C ≤ T_A ≤ +70°C unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				15	mA
All others				3	mA
Maximum Input Current without Latchup (Note 6)	T_A = 25°C			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

AC Electrical Characteristics 98XCS: 0°C ≤ T_A ≤ +70°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)	4V ≤ V_{CC} ≤ 6V	1		DC	μs
Crystal, Resonator,	2.5V ≤ V_{CC} < 4V	2.5		DC	μs
R/C Oscillator	4V ≤ V_{CC} ≤ 6V	3		DC	μs
	2.5V ≤ V_{CC} < 4V	7.5		DC	μs
CKI Clock Duty Cycle (Note 5)	f_r = Max	40		60	%
Rise Time (Note 5)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 5)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	4V ≤ V_{CC} ≤ 6V	200			ns
	2.5V ≤ V_{CC} < 4V	500			ns
t_{HOLD}	4V ≤ V_{CC} ≤ 6V	60			ns
	2.5V ≤ V_{CC} < 4V	150			ns
Output Propagation Delay	R_L = 2.2k, C_L = 100 pF				
t_{PD1}, t_{PD0}					
SO, SK	4V ≤ V_{CC} ≤ 6V			0.7	μs
	2.5V ≤ V_{CC} < 4V			1.75	μs
All Others	4V ≤ V_{CC} ≤ 6V			1	μs
	2.5V ≤ V_{CC} < 4V			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 5: Parameter sampled but not 100% tested.

Note 6: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics 88XCS: $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		2.5		6	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			5.5	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<1	10	μA
	V_{CC} = 4V, CKI = 0 MHz		<0.5	6	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHZ	V_{CC} = 4V, t_c = 10 μs			0.7	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6V, V_{IN} = 0V	−2		+2	μA
Input Pullup Current	V_{CC} = 6V, V_{IN} = 0V	40		250	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4V, V_{OL} = 1V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2.0			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4V, V_{OH} = 2.7V	10		100	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink (Push-Pull Mode)	V_{CC} = 4V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			mA
TRI-STATE Leakage		−2		+2	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor and the comparators are disabled.

DC Electrical Characteristics 88XCS: $-40°C \le T_A \le +85°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				15	mA
All others				3	mA
Maximum Input Current without Latchup (Note 6)	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

AC Electrical Characteristics 88XCS: $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)	$4V \le V_{CC} \le 6V$	1		DC	μs
Crystal, Resonator,	$2.5V \le V_{CC} < 4V$	2.5		DC	μs
R/C Oscillator	$4V \le V_{CC} \le 6V$	3		DC	μs
	$2.5V \le V_{CC} < 4V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 5)	f_r = Max	40		60	%
Rise Time (Note 5)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 5)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	$4V \le V_{CC} \le 6V$	200			ns
	$2.5V \le V_{CC} < 4V$	500			ns
t_{HOLD}	$4V \le V_{CC} \le 6V$	60			ns
	$2.5V \le V_{CC} < 4V$	150			ns
Output Propagation Delay	R_L = 2.2k, C_L = 100 pF				
t_{PD1}, t_{PD0}					
SO, SK	$4V \le V_{CC} \le 6V$			0.7	μs
	$2.5V \le V_{CC} < 4V$			1.75	μs
All Others	$4V \le V_{CC} \le 6V$			1	μs
	$2.5V \le V_{CC} < 4V$			2.5	μs
MICROWIRE Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 5: Parameter sampled but not 100% tested.

Note 6: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics 68XCS: −55°C ≤ T_A ≤ +125°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		4.5		5.5	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 5.5V, t_c = 2.5 μs			5.5	mA
HALT Current (Note 3)	V_{CC} = 5.5V, CKI = 0 MHz		<10	30	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 5.5V, t_c = 2.5 μs			2.5	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 5.5V, V_{IN} = 0V	−5		+5	μA
Input Pullup Current	V_{CC} = 5.5V, V_{IN} = 0V	35		400	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1V	9			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4.5V, V_{OH} = 3.2V	9		140	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.8V	0.4			mA
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.4			mA
TRI-STATE Leakage	V_{CC} = 5.5V	−5		+5	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor and the comparators are disabled.

DC Electrical Characteristics 68XCS: $-55°C \le T_A \le +125°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				12	mA
All others				2.5	mA
Maximum Input Current without Latchup (Note 6)	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

AC Electrical Characteristics 68XCS: $-55°C \le T_A \le +125°C$ unless otherwise specified

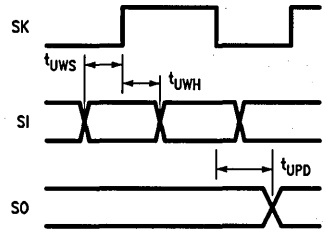
Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)	$4.5V \le V_{CC} \le 5.5V$	1		DC	μs
Crystal, Resonator, R/C Oscillator	$4.5V \le V_{CC} \le 5.5V$	3		DC	μs
CKI Clock Duty Cycle (Note 5)	f_r = Max	45		55	%
Rise Time (Note 5)	f_r = 10 MHz Ext Clock			12	ns
Fall Time (Note 5)	f_r = 10 MHz Ext Clock			8	ns
Inputs					
t_{SETUP}	$4.5V \le V_{CC} \le 5.5V$	200			ns
t_{HOLD}	$4.5V \le V_{CC} \le 5.5V$	60			ns
Output Propagation Delay	R_L = 2.2k, C_L = 100 pF				
t_{PD1}, t_{PD0}					
SO, SK	$4.5V \le V_{CC} \le 5.5V$			0.7	μs
All Others	$4.5V \le V_{CC} \le 5.5V$			1	μs
MICROWIRE Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 5: Parameter sampled but not 100% tested.

Note 6: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Comparator AC and DC Characteristics $V_{CC} = 5V, T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$0.4V \le V_{IN} \le V_{CC} - 1.5V$		±10	±25	mV
Input Common Mode Voltage Range		0.4		$V_{CC} - 1.5$	V
Low Level Output Current	$V_{OL} = 0.4V$	1.6			mA
High Level Output Current	$V_{OH} = 4.6V$	1.6			mA
DC Supply Current (When Enabled)				250	μA
Response Time	TBD mV Step, TBD mV Overdrive, 100 pF Load		1		μs

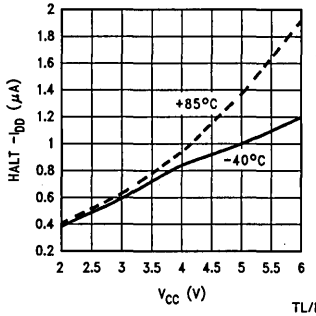


TL/DD/10830–6

FIGURE 3. MICROWIRE/PLUS Timing

Typical Performance Characteristics (−40°C to +85°C)

Halt—I_{DD}



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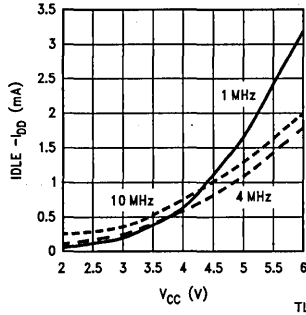
Idle—I_{DD} (Crystal Clock Option)



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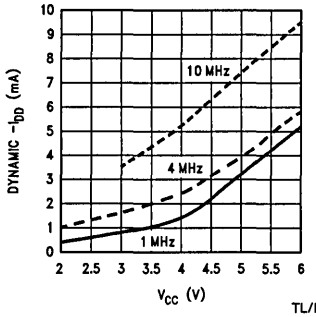
Dynamic—I_{DD} (Crystal Clock Option)



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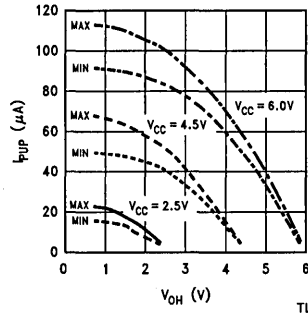
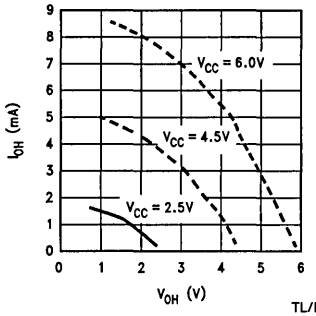
Port L/C/G Weak Pull-Up Source Current



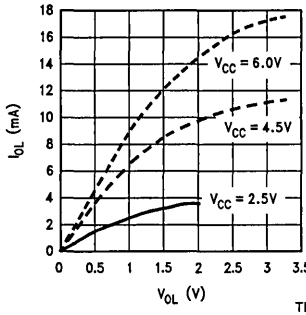
TL/DD/10830–27

Port L/C/G Push-Pull Source Current



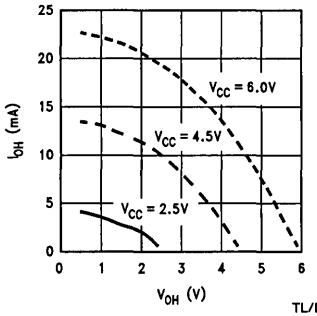
TL/DD/10830–28

Port L/C/G/ Push-Pull Sink Current



TL/DD/10830–29

Port D Source Current



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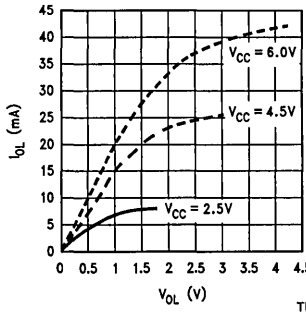
Port D Sink Current



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Pin Descriptions

V_{CC} and GND are the power supply pins.

CKI is the clock input. This can come from an R/C generated oscillator, or a crystal oscillator (in conjunction with CKO). See Oscillator Description section.

$\overline{\text{RESET}}$ is the master reset input. See Reset Description section.

The COP888CS contains three bidirectional 8-bit I/O ports (C, G and L), where each individual bit may be independently configured as an input (Schmitt trigger inputs on ports L and G), output or TRI-STATE under program control. Three data memory address locations are allocated for each of these I/O ports. Each I/O port has two associated 8-bit memory mapped registers, the CONFIGURATION register and the output DATA register. A memory mapped address is also reserved for the input pins of each I/O port. (See the COP888CS memory map for the various addresses associated with the I/O ports.) *Figure 4* shows the I/O port configurations for the COP888CS. The DATA and CONFIGURATION registers allow for each port bit to be individually configured under software control as shown below:

CONFIGURATION Register	DATA Register	Port Set-Up
0	0	Hi-Z Input (TRI-STATE Output)
0	1	Input with Weak Pull-Up
1	0	Push-Pull Zero Output
1	1	Push-Pull One Output

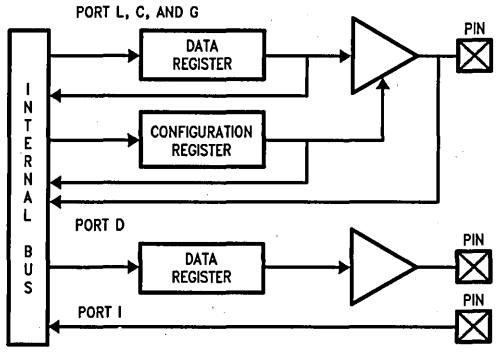

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FIGURE 4. I/O Port Configurations

Port L is an 8-bit I/O port. All L-pins have Schmitt triggers on the inputs.

The Port L supports Multi-Input Wake Up on all eight pins. L1 is used for the UART external clock. L2 and L3 are used for the UART transmit and receive.

The Port L has the following alternate features:

- L0 MIWU
- L1 MIWU or CKX
- L2 MIWU or TDX
- L3 MIWU or RDX
- L4 MIWU
- L5 MIWU
- L6 MIWU
- L7 MIWU

Port G is an 8-bit port with 5 I/O pins (G0, G2–G5), an input pin (G6), and two dedicated output pins (G1 and G7). Pins G0 and G2–G6 all have Schmitt Triggers on their inputs. Pin G1 serves as the dedicated WDOUT WATCHDOG output, while pin G7 is either input or output depending on the oscillator mask option selected. With the crystal oscillator option selected, G7 serves as the dedicated output pin for the CKO clock output. With the single-pin R/C oscillator mask option selected, G7 serves as a general purpose input pin but is also used to bring the device out of HALT mode with a low to high transition on G7. There are two registers associated with the G Port, a data register and a configuration register. Therefore, each of the 5 I/O bits (G0, G2–G5) can be individually configured under software control.

Since G6 is an input only pin and G7 is the dedicated CKO clock output pin (crystal clock option) or general purpose input (R/C clock option), the associated bits in the data and configuration registers for G6 and G7 are used for special purpose functions as outlined below. Reading the G6 and G7 data bits will return zeros.

Note that the chip will be placed in the HALT mode by writing a "1" to bit 7 of the Port G Data Register. Similarly the chip will be placed in the IDLE mode by writing a "1" to bit 6 of the Port G Data Register.

Writing a "1" to bit 6 of the Port G Configuration Register enables the MICROWIRE/PLUS to operate with the alternate phase of the SK clock. The G7 configuration bit, if set high, enables the clock start up delay after HALT when the R/C clock configuration is used.

	Config Reg.	Data Reg.
G7	CLKDLY	HALT
G6	Alternate SK	IDLE

Port G has the following alternate features:

- G0 INTR (External Interrupt Input)
- G2 T1B (Timer T1 Capture Input)
- G3 T1A (Timer T1 I/O)
- G4 SO (MICROWIRE Serial Data Output)
- G5 SK (MICROWIRE Serial Clock)
- G6 SI (MICROWIRE Serial Data Input)

Port G has the following dedicated functions:

- G1 WDOUT WATCHDOG and/or Clock Monitor dedicated output
- G7 CKO Oscillator dedicated output or general purpose input

Port C is an 8-bit I/O port. The 40-pin device does not have a full complement of Port C pins. The unavailable pins are not terminated. A read operation for these unterminated pins will return unpredictable values.

Port I is an eight-bit Hi-Z input port. The 28-pin device does not have a full complement of Port I pins. The unavailable

Pin Descriptions (Continued)

pins are not terminated i.e., they are floating. A read operation for these unterminated pins will return unpredictable values. The user must ensure that the software takes this into account by either masking or restricting the accesses to bit operations. The unterminated Port I pins will draw power only when addressed.

Ports I1–I3 are used for Comparator 1.

Ports I1–I3 have the following alternate features.

I1 COMP1 − IN (Comparator 1 Negative Input)

I2 COMP1 + IN (Comparator 1 Positive Input)

I3 COMP1OUT (Comparator 1 Output)

Port D is an 8-bit output port that is preset high when $\overline{\text{RESET}}$ goes low. The user can tie two or more D port outputs together in order to get a higher drive.

Functional Description

The architecture of the COP888CS is modified Harvard architecture. With the Harvard architecture, the control store program memory (ROM) is separated from the data store memory (RAM). Both ROM and RAM have their own separate addressing space with separate address buses. The COP888CS architecture, though based on Harvard architecture, permits transfer of data from ROM to RAM.

CPU REGISTERS

The CPU can do an 8-bit addition, subtraction, logical or shift operation in one instruction (t_c) cycle time.

There are six CPU registers:

A is the 8-bit Accumulator Register

PC is the 15-bit Program Counter Register

PU is the upper 7 bits of the program counter (PC)
PL is the lower 8 bits of the program counter (PC)

B is an 8-bit RAM address pointer, which can be optionally post auto incremented or decremented.

X is an 8-bit alternate RAM address pointer, which can be optionally post auto incremented or decremented.

SP is the 8-bit stack pointer, which points to the subroutine/interrupt stack (in RAM). The SP is initialized to RAM address 06F with reset.

S is the 8-bit Data Segment Address Register used to extend the lower half of the address range (00 to 7F) into 256 data segments of 128 bytes each.

All the CPU registers are memory mapped with the exception of the Accumulator (A) and the Program Counter (PC).

PROGRAM MEMORY

Program memory for the COP888CS consists of 4096 bytes of ROM. These bytes may hold program instructions or constant data (data tables for the LAID instruction, jump vectors for the JID instruction, and interrupt vectors for the VIS instruction). The program memory is addressed by the 15-bit program counter (PC). All interrupts in the COP888CS vector to program memory location 0FF Hex.

DATA MEMORY

The data memory address space includes the on-chip RAM and data registers, the I/O registers (Configuration, Data and Pin), the control registers, the MICROWIRE/PLUS SIO shift register, and the various registers, and counters associated with the timers (with the exception of the IDLE timer). Data memory is addressed directly by the instruction or indirectly by the B, X, SP pointers and S register.

The COP888CS has 192 bytes of RAM. Sixteen bytes of RAM are mapped as "registers" at addresses 0F0 to 0FF Hex. These registers can be loaded immediately, and also decremented and tested with the DRSZ (decrement register and skip if zero) instruction. The memory pointer registers X, SP, B and S are memory mapped into this space at address locations 0FC to 0FF Hex respectively, with the other registers being available for general usage.

The instruction set of the COP888CS permits any bit in memory to be set, reset or tested. All I/O and registers on the COP888CS (except A and PC) are memory mapped; therefore, I/O bits and register bits can be directly and individually set, reset and tested. The accumulator (A) bits can also be directly and individually tested.

Data Memory Segment RAM Extension

Data memory address 0FF is used as a memory mapped location for the Data Segment Address Register (S) in the COP888CS.

The data store memory is either addressed directly by a single byte address within the instruction, or indirectly relative to the reference of the B, X, or SP pointers (each contains a single-byte address). This single-byte address allows an addressing range of 256 locations from 00 to FF hex. The upper bit of this single-byte address divides the data store memory into two separate sections as outlined previously. With the exception of the RAM register memory from address locations 00F0 to 00FF, all RAM memory is memory mapped with the upper bit of the single-byte address being equal to zero. This allows the upper bit of the single-byte address to determine whether or not the base address range (from 0000 to 00FF) is extended. If this upper bit equals one (representing address range 0080 to 00FF), then address extension does not take place. Alternatively, if this upper bit equals zero, then the data segment extension register S is used to extend the base address range (from 0000 to 007F) from XX00 to XX7F, where XX represents the 8 bits from the S register. Thus the 128-byte data segment extensions are located from addresses 0100 to 017F for data segment 1, 0200 to 027F for data segment 2, etc., up to FF00 to FF7F for data segment 255. The base address range from 0000 to 007F represents data segment 0.

Figure 5 illustrates how the S register data memory extension is used in extending the lower half of the base address range (00 to 7F hex) into 256 data segments of 128 bytes each, with a total addressing range of 32 kbytes from XX00 to XX7F. This organization allows a total of 256 data segments of 128 bytes each with an additional upper base segment of 128 bytes. Furthermore, all addressing modes are available for all data segments. The S register must be changed under program control to move from one data segment (128 bytes) to another. However, the upper base segment (containing the 16 memory registers, I/O registers, control registers, etc.) is always available regardless of the

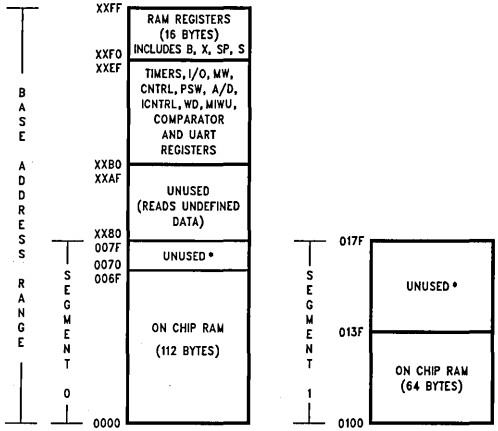
Data Memory Segment RAM Extension (Continued)

contents of the S register, since the upper base segment (address range 0080 to 00FF) is independent of data segment extension.

The instructions that utilize the stack pointer (SP) always reference the stack as part of the base segment (Segment 0), regardless of the contents of the S register. The S register is not changed by these instructions. Consequently, the stack (used with subroutine linkage and interrupts) is always located in the base segment. The stack pointer will be initialized to point at data memory location 006F as a result of reset.

The 128 bytes of RAM contained in the base segment are split between the lower and upper base segments. The first 112 bytes of RAM are resident from address 0000 to 006F in the lower base segment, while the remaining 16 bytes of RAM represent the 16 data memory registers located at addresses 00F0 to 00FF of the upper base segment. No RAM is located at the upper sixteen addresses (0070 to 007F) of the lower base segment.

Additional RAM beyond these initial 128 bytes, however, will always be memory mapped in groups of 128 bytes (or less) at the data segment address extensions (XX00 to XX7F) of the lower base segment. The additional 64 bytes of RAM in the COP888CS (beyond the initial 128 bytes) are memory mapped at address locations 0100 to 013F hex.



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*Reads as all ones.

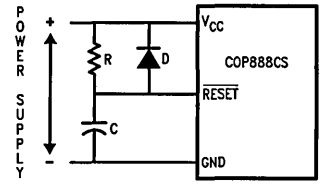
FIGURE 5. RAM Organization

Reset

The $\overline{\text{RESET}}$ input when pulled low initializes the microcontroller. Initialization will occur whenever the $\overline{\text{RESET}}$ input is pulled low. Upon initialization, the data and configuration registers for ports L, G and C are cleared, resulting in these Ports being initialized to the TRI-STATE mode. Pin G1 of the G Port is an exception (as noted below) since pin G1 is dedicated as the WATCHDOG and/or Clock Monitor error output pin. Port D is set high. The PC, PSW, ICNTRL, CNTRL, are cleared. The UART registers PSR, ENU (except that TBMT bit is set), ENUR and ENUI are cleared. The Comparator Select Register is cleared. The S register is initialized to zero. The Multi-Input Wakeup registers WKEN, WKEDG and WKPND are cleared. The stack pointer, SP, is initialized to 6F Hex.

The COP888CS comes out of reset with both the WATCHDOG logic and the Clock Monitor detector armed, with the WATCHDOG service window bits set and the Clock Monitor bit set. The WATCHDOG and Clock Monitor circuits are inhibited during reset. The WATCHDOG service window bits being initialized high default to the maximum WATCHDOG service window of 64k t_C clock cycles. The Clock Monitor bit being initialized high will cause a Clock Monitor error following reset if the clock has not reached the minimum specified frequency at the termination of reset. A Clock Monitor error will cause an active low error output on pin G1. This error output will continue until 16 t_C–32 t_C clock cycles following the clock frequency reaching the minimum specified value, at which time the G1 output will enter the TRI-STATE mode.

The external RC network shown in *Figure 6* should be used to ensure that the $\overline{\text{RESET}}$ pin is held low until the power supply to the chip stabilizes.



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RC > 5 × Power Supply Rise Time

FIGURE 6. Recommended Reset Circuit

Oscillator Circuits

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (crystal configuration). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_c$).

Figure 7 shows the Crystal and R/C diagrams.

CRYSTAL OSCILLATOR

CKI and CKO can be connected to make a closed loop crystal (or resonator) controlled oscillator.

Table A shows the component values required for various standard crystal values.

R/C OSCILLATOR

By selecting CKI as a single pin oscillator input, a single pin R/C oscillator circuit can be connected to it. CKO is available as a general purpose input, and/or HALT restart input.

Table B shows the variation in the oscillator frequencies as functions of the component (R and C) values.

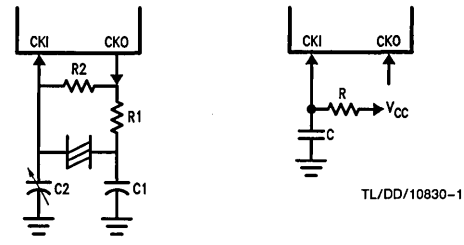

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FIGURE 7. Crystal and R/C Oscillator Diagrams

Oscillator Circuits (Continued)

TABLE A. Crystal Oscillator Configuration, T_A = 25°C

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)	Conditions
0	1	30	30–36	10	V_{CC} = 5V
0	1	30	30–36	4	V_{CC} = 5.0V
0	1	200	100–150	0.455	V_{CC} = 2.5V

TABLE B. RC Oscillator Configuration, T_A = 25°C

R (kΩ)	C (pF)	CKI Freq (MHz)	Instr. Cycle (μs)	Conditions
3.3	82	2.2 to 2.7	3.7 to 4.6	V_{CC} = 5V
5.6	100	1.1 to 1.3	7.4 to 9.0	V_{CC} = 5V
6.8	100	0.9 to 1.1	8.8 to 10.8	V_{CC} = 5V

Note: 3k ≤ R ≤ 200k
50 pF ≤ C ≤ 200 pF

Current Drain

The total current drain of the chip depends on:

1. Oscillator operation mode—I1
2. Internal switching current—I2
3. Internal leakage current—I3
4. Output source current—I4
5. DC current caused by external input not at V_{CC} or GND—I5
6. Comparator DC supply current when enabled—I6
7. Clock Monitor current when enabled—I7

Thus the total current drain, It, is given as

$$It = I1 + I2 + I3 + I4 + I5 + I6 + I7$$

To reduce the total current drain, each of the above components must be minimum.

The chip will draw more current as the CKI input frequency increases up to the maximum 10 MHz value. Operating with a crystal network will draw more current than an external square-wave. Switching current, governed by the equation below, can be reduced by lowering voltage and frequency. Leakage current can be reduced by lowering voltage and temperature. The other two items can be reduced by carefully designing the end-user's system.

$$I2 = C \times V \times f$$

where C = equivalent capacitance of the chip
V = operating voltage
f = CKI frequency

Control Registers

CNTRL Register (Address X'00EE)

The Timer1 (T1) and MICROWIRE/PLUS control register contains the following bits:

- SL1 & SL0 — Select the MICROWIRE/PLUS clock divide by (00 = 2, 01 = 4, 1x = 8)
- IEDG — External interrupt edge polarity select (0 = Rising edge, 1 = Falling edge)
- MSEL — Selects G5 and G4 as MICROWIRE/PLUS signals SK and SO respectively
- T1C0 — Timer T1 Start/Stop control in timer modes 1 and 2
  Timer T1 Underflow Interrupt Pending Flag in timer mode 3
- T1C1 — Timer T1 mode control bit
- T1C2 — Timer T1 mode control bit
- T1C3 — Timer T1 mode control bit

T1C3	T1C2	T1C1	T1C0	MSEL	IEDG	SL1	SL0

Bit 7 Bit 0

PSW Register (Address X'00EF)

The PSW register contains the following select bits:

- GIE — Global interrupt enable (enables interrupts)
- EXEN — Enable external interrupt
- BUSY — MICROWIRE/PLUS busy shifting flag
- EXPND — External interrupt pending
- T1ENA — Timer T1 Interrupt Enable for Timer Underflow or T1A Input capture edge
- T1PNDA — Timer T1 Interrupt Pending Flag (Autoreload RA in mode 1, T1 Underflow in Mode 2, T1A capture edge in mode 3)
- C — Carry Flag
- HC — Half Carry Flag

HC	C	T1PNDA	T1ENA	EXPND	BUSY	EXEN	GIE

Bit 7 Bit 0

The Half-Carry bit is also affected by all the instructions that affect the Carry flag. The SC (Set Carry) and RC (Reset Carry) instructions will respectively set or clear both the carry flags. In addition to the SC and RC instructions, ADC, SUBC, RRC and RLC instructions affect the carry and Half Carry flags.

Control Registers (Continued)

ICNTRL Register (Address X'00E8)

The ICNTRL register contains the following bits:

T1ENB	Timer T1 Interrupt Enable for T1B Input capture edge
T1PNDB	Timer T1 Interrupt Pending Flag for T1B capture edge
μWEN	Enable MICROWIRE/PLUS interrupt
μWPND	MICROWIRE/PLUS interrupt pending
T0EN	Timer T0 Interrupt Enable (Bit 12 toggle)
T0PND	Timer T0 Interrupt pending
LPEN	L Port Interrupt Enable (Multi-Input Wakeup/Interrupt)
	Bit 7 could be used as a flag

Unused	LPEN	T0PND	T0EN	μWPND	μWEN	T1PNDB	T1ENB

Bit 7 Bit 0

Timers

The COP888CS contains a very versatile set of timers (T0, T1). All timers and associated autoreload/capture registers power up containing random data.

TIMER T0 (IDLE TIMER)

The COP888CS supports applications that require maintaining real time and low power with the IDLE mode. This IDLE mode support is furnished by the IDLE timer T0, which is a 16-bit timer. The Timer T0 runs continuously at the fixed rate of the instruction cycle clock, t_c. The user cannot read or write to the IDLE Timer T0, which is a count down timer.

The Timer T0 supports the following functions:

Exit out of the Idle Mode (See Idle Mode description)
WATCHDOG logic (See WATCHDOG description)
Start up delay out of the HALT mode

The IDLE Timer T0 can generate an interrupt when the thirteenth bit toggles. This toggle is latched into the T0PND pending flag, and will occur every 4 ms at the maximum clock frequency (t_c = 1 μs). A control flag T0EN allows the interrupt from the thirteenth bit of Timer T0 to be enabled or disabled. Setting T0EN will enable the interrupt, while resetting it will disable the interrupt.

TIMER T1

The COP888CS has a powerful timer/counter block.

The timer block consists of a 16-bit timer, T1, and two supporting 16-bit autoreload/capture registers, R1A and R1B. It has two pins associated with it, T1A and T1B. The pin T1A supports I/O required by the timer block, while the pin T1B is an input to the timer block. The powerful and flexible timer block allows the COP888CS to easily perform all timer functions with minimal software overhead. The timer block has three operating modes: Processor Independent PWM mode, External Event Counter mode, and Input Capture mode.

The control bits T1C3, T1C2, and T1C1 allow selection of the different modes of operation.

Mode 1. Processor Independent PWM Mode

As the name suggests, this mode allows the COP888CS to generate a PWM signal with very minimal user intervention.

The user only has to define the parameters of the PWM signal (ON time and OFF time). Once begun, the timer block will continuously generate the PWM signal completely independent of the microcontroller. The user software services the timer block only when the PWM parameters require updating.

In this mode the timer T1 counts down at a fixed rate of t_c. Upon every underflow the timer is alternately reloaded with the contents of supporting registers, R1A and R1B. The very first underflow of the timer causes the timer to reload from the register R1A. Subsequent underflows cause the timer to be reloaded from the registers alternately beginning with the register R1B.

The T1 Timer control bits, T1C3, T1C2 and T1C1 set up the timer for PWM mode operation.

Figure 8 shows a block diagram of the timer in PWM mode.

The underflows can be programmed to toggle the T1A output pin. The underflows can also be programmed to generate interrupts.

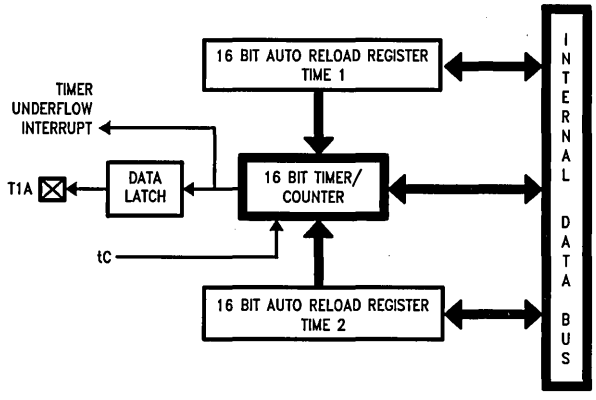

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FIGURE 8. Timer in PWM Mode

Timers (Continued)

Underflows from the timer are alternately latched into two pending flags, T1PNDA and T1PNDB. The user must reset these pending flags under software control. Two control enable flags, T1ENA and T1ENB, allow the interrupts from the timer underflow to be enabled or disabled. Setting the timer enable flag T1ENA will cause an interrupt when a timer underflow causes the R1A register to be reloaded into the timer. Setting the timer enable flag T1ENB will cause an interrupt when a timer underflow causes the R1B register to be reloaded into the timer. Resetting the timer enable flags will disable the associated interrupts.

Either or both of the timer underflow interrupts may be enabled. This gives the user the flexibility of interrupting once per PWM period on either the rising or falling edge of the PWM output. Alternatively, the user may choose to interrupt on both edges of the PWM output.

Mode 2. External Event Counter Mode

This mode is quite similar to the processor independent PWM mode described above. The main difference is that the timer, T1, is clocked by the input signal from the T1A pin. The Tx timer control bits, T1C3, T1C2 and T1C1 allow the timer to be clocked either on a positive or negative edge from the T1A pin. Underflows from the timer are latched into the T1PNDA pending flag. Setting the T1ENA control flag will cause an interrupt when the timer underflows.

In this mode the input pin T1B can be used as an independent positive edge sensitive interrupt input if the T1ENB control flag is set. The occurrence of a positive edge on the T1B input pin is latched into the T1PNDB flag.

Figure 9 shows a block diagram of the timer in External Event Counter mode.

Note: The PWM output is not available in this mode since the T1A pin is being used as the counter input clock.

Mode 3. Input Capture Mode

The COP888CS can precisely measure external frequencies or time external events by placing the timer block, T1, in the input capture mode.

In this mode, the timer T1 is constantly running at the fixed t_C rate. The two registers, R1A and R1B, act as capture registers. Each register acts in conjunction with a pin. The register R1A acts in conjunction with the T1A pin and the register R1B acts in conjunction with the T1B pin.

The timer value gets copied over into the register when a trigger event occurs on its corresponding pin. Control bits, T1C3, T1C2 and T1C1, allow the trigger events to be specified either as a positive or a negative edge. The trigger condition for each input pin can be specified independently.

The trigger conditions can also be programmed to generate interrupts. The occurrence of the specified trigger condition on the T1A and T1B pins will be respectively latched into the pending flags, T1PNDA and T1PNDB. The control flag T1ENA allows the interrupt on T1A to be either enabled or disabled. Setting the T1ENA flag enables interrupts to be generated when the selected trigger condition occurs on the T1A pin. Similarly, the flag T1ENB controls the interrupts from the T1B pin.

Underflows from the timer can also be programmed to generate interrupts. Underflows are latched into the timer T1C0 pending flag (the T1C0 control bit serves as the timer underflow interrupt pending flag in the Input Capture mode). Consequently, the T1C0 control bit should be reset when entering the Input Capture mode. The timer underflow interrupt is enabled with the T1ENA control flag. When a T1A interrupt occurs in the Input Capture mode, the user must check both the T1PNDA and T1C0 pending flags in order to determine whether a T1A input capture or a timer underflow (or both) caused the interrupt.

Figure 10 shows a block diagram of the timer in Input Capture mode.

TIMER CONTROL FLAGS

The control bits and their functions are summarized below.

T1C0	Timer Start/Stop control in Modes 1 and 2 (Processor Independent PWM and External Event Counter), where 1 = Start, 0 = Stop Timer Underflow Interrupt Pending Flag in Mode 3 (Input Capture)
T1PNDA	Timer Interrupt Pending Flag
T1PNDB	Timer Interrupt Pending Flag
T1ENA	Timer Interrupt Enable Flag
T1ENB	Timer Interrupt Enable Flag 1 = Timer Interrupt Enabled 0 = Timer Interrupt Disabled
T1C3	Timer mode control
T1C2	Timer mode control
T1C1	Timer mode control

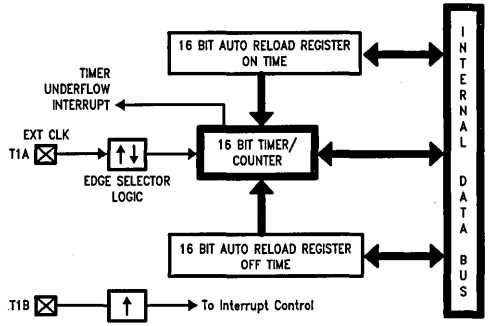

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FIGURE 9. Timer in External Event Counter Mode

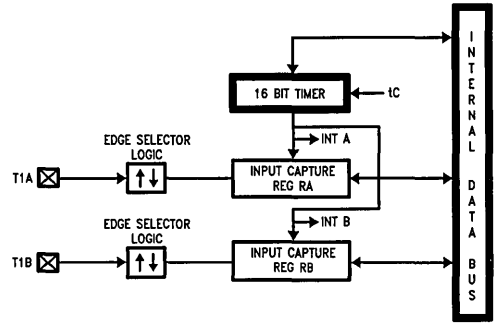

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FIGURE 10. Timer in Input Capture Mode

Timers (Continued)

The timer mode control bits (T1C3, T1C2 and T1C1) are detailed below:

T1C3	T1C2	T1C1	Timer Mode	Interrupt A Source	Interrupt B Source	Timer Counts On
0	0	0	MODE 2 (External Event Counter)	Timer Underflow	Pos. T1B Edge	T1A Pos. Edge
0	0	1	MODE 2 (External Event Counter)	Timer Underflow	Pos. T1B Edge	T1A Neg. Edge
1	0	1	MODE 1 (PWM) T1A Toggle	Autoreload RA	Autoreload RB	t_C
1	0	0	MODE 1 (PWM) No T1A Toggle	Autoreload RA	Autoreload RB	t_C
0	1	0	MODE 3 (Capture) Captures: T1A Pos. Edge T1B Pos. Edge	Pos. T1A Edge or Timer Underflow	Pos. T1B Edge	t_C
1	1	0	MODE 3 (Capture) Captures: T1A Pos. Edge T1B Neg. Edge	Pos. T1A Edge or Timer Underflow	Neg. T1B Edge	t_C
0	1	1	MODE 3 (Capture) Captures: T1A Neg. Edge T1B Pos. Edge	Neg. T1B Edge or Timer Underflow	Pos. T1B Edge	t_C
1	1	1	MODE 3 (Capture) Captures: T1A Neg. Edge T1B Neg. Edge	Neg. T1A Edge or Timer Underflow	Neg. T1B Edge	t_C

Power Save Modes

The COP888CS offers the user two power save modes of operation: HALT and IDLE. In the HALT mode, all microcontroller activities are stopped. In the IDLE mode, the on-board oscillator circuitry the WATCHDOG logic, the Clock Monitor and timer T0 are active but all other microcontroller activities are stopped. In either mode, all on-board RAM, registers, I/O states, and timers (with the exception of T0) are unaltered.

HALT MODE

The COP888CS is placed in the HALT mode by writing a "1" to the HALT flag (G7 data bit). All microcontroller activities, including the clock and timers, are stopped. The WATCHDOG logic on the COP888CS is disabled during the HALT mode. However, the clock monitor circuitry if enabled remains active and will cause the WATCHDOG output pin (WDOUT) to go low. If the HALT mode is used and the user does not want to activate the WDOUT pin, the Clock Monitor should be disabled after the device comes out of reset (resetting the Clock Monitor control bit with the first write to the WDSVR register). In the HALT mode, the power requirements of the COP888CS are minimal and the applied voltage (V_{CC}) may be decreased to V_r (V_r = 2.0V) without altering the state of the machine.

The COP888CS supports three different ways of exiting the HALT mode. The first method of exiting the HALT mode is with the Multi-Input Wakeup feature on the L port. The second method is with a low to high transition on the CKO (G7) pin. This method precludes the use of the crystal clock configuration (since CKO becomes a dedicated output), and so may be used with an RC clock configuration. The third method of exiting the HALT mode is by pulling the $\overline{\text{RESET}}$ pin low.

Since a crystal or ceramic resonator may be selected as the oscillator, the Wakeup signal is not allowed to start the chip running immediately since crystal oscillators and ceramic resonators have a delayed start up time to reach full amplitude and frequency stability. The IDLE timer is used to generate a fixed delay to ensure that the oscillator has indeed stabilized before allowing instruction execution. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry is enabled. The IDLE timer is loaded with a value of 256 and is clocked with the t_C instruction cycle clock. The t_C clock is derived by dividing the oscillator clock down by a factor of 10. The Schmitt trigger following the CKI inverter on the chip ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

Power Save Modes (Continued)

If an RC clock option is being used, the fixed delay is introduced optionally. A control bit, CLKDLY, mapped as configuration bit G7, controls whether the delay is to be introduced or not. The delay is included if CLKDLY is set, and excluded if CLKDLY is reset. The CLKDLY bit is cleared on reset.

The COP888CS has two mask options associated with the HALT mode. The first mask option enables the HALT mode feature, while the second mask option disables the HALT mode. With the HALT mode enable mask option, the COP888CS will enter and exit the HALT mode as described above. With the HALT disable mask option, the COP888CS cannot be placed in the HALT mode (writing a "1" to the HALT flag will have no effect).

The WATCHDOG detector circuit is inhibited during the HALT mode. However, the clock monitor circuit if enabled remains active during HALT mode in order to ensure a clock monitor error if the COP888CS inadvertently enters the HALT mode as a result of a runaway program or power glitch.

IDLE MODE

The COP888CS is placed in the IDLE mode by writing a "1" to the IDLE flag (G6 data bit). In this mode, all activities, except the associated on-board oscillator circuitry, the WATCHDOG logic, the clock monitor and the IDLE Timer T0, are stopped. The power supply requirements of the micro-controller in this mode of operation are typically around 30% of normal power requirement of the microcontroller.

As with the HALT mode, the COP888CS can be returned to normal operation with a reset, or with a Multi-Input Wakeup from the L Port. Alternately, the microcontroller resumes normal operation from the IDLE mode when the thirteenth bit (representing 4.096 ms at internal clock frequency of 1 MHz, t_C = 1 μs) of the IDLE Timer toggles.

This toggle condition of the thirteenth bit of the IDLE Timer T0 is latched into the T0PND pending flag.

The user has the option of being interrupted with a transition on the thirteenth bit of the IDLE Timer T0. The interrupt can be enabled or disabled via the T0EN control bit. Setting the T0EN flag enables the interrupt and vice versa.

The user can enter the IDLE mode with the Timer T0 interrupt enabled. In this case, when the T0PND bit gets set, the COP888CS will first execute the Timer T0 interrupt service routine and then return to the instruction following the "Enter Idle Mode" instruction.

Alternatively, the user can enter the IDLE mode with the IDLE Timer T0 interrupt disabled. In this case, the COP888CS will resume normal operation with the instruction immediately following the "Enter IDLE Mode" instruction.

Note: It is necessary to program two NOP instructions following both the set HALT mode and set IDLE mode instructions. These NOP instructions are necessary to allow clock resynchronization following the HALT or IDLE modes.

Multi-Input Wakeup

The Multi-Input Wakeup feature is ued to return (wakeup) the COP888CS from either the HALT or IDLE modes. Alternately Multi-Input Wakeup/Interrupt feature may also be used to generate up to 8 edge selectable external interrupts.

Figure 11 shows the Multi-Input Wakeup logic for the COP888CS microcontroller.

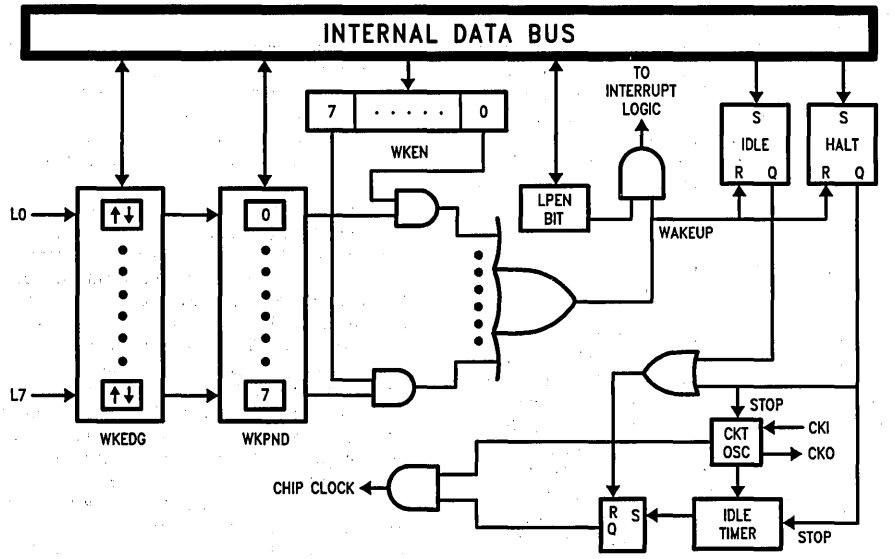

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FIGURE 11. Multi-Input Wake Up Logic

Multi-Input Wakeup (Continued)

The Multi-Input Wakeup feature utilizes the L Port. The user selects which particular L port bit (or combination of L Port bits) will cause the COP888CS to exit the HALT or IDLE modes. The selection is done through the Reg: WKEN. The Reg: WKEN is an 8-bit read/write register, which contains a control bit for every L port bit. Setting a particular WKEN bit enables a Wakeup from the associated L port pin.

The user can select whether the trigger condition on the selected L Port pin is going to be either a positive edge (low to high transition) or a negative edge (high to low transition). This selection is made via the Reg: WKEDG, which is an 8-bit control register with a bit assigned to each L Port pin. Setting the control bit will select the trigger condition to be a negative edge on that particular L Port pin. Resetting the bit selects the trigger condition to be a positive edge. Changing an edge select entails several steps in order to avoid a pseudo Wakeup condition as a result of the edge change. First, the associated WKEN bit should be reset, followed by the edge select change in WKEDG. Next, the associated WKPND bit should be cleared, followed by the associated WKEN bit being re-enabled.

An example may serve to clarify this procedure. Suppose we wish to change the edge select from positive (low going high) to negative (high going low) for L Port bit 5, where bit 5 has previously been enabled for an input interrupt. The program would be as follows:

```
RBIT  5, WKEN
SBIT  5, WKEDG
RBIT  5, WKPND
SBIT  5, WKEN
```

If the L port bits have been used as outputs and then changed to inputs with Multi-Input Wakeup/Interrupt, a safety procedure should also be followed to avoid inherited pseudo wakeup conditions. After the selected L port bits have been changed from output to input but before the associated WKEN bits are enabled, the associated edge select bits in WKEDG should be set or reset for the desired edge selects, followed by the associated WKPND bits being cleared.

This same procedure should be used following reset, since the L port inputs are left floating as a result of reset.

The occurrence of the selected trigger condition for Multi-Input Wakeup is latched into a pending register called WKPND. The respective bits of the WKPND register will be set on the occurrence of the selected trigger edge on the corresponding Port L pin. The user has the responsibility of clearing these pending flags. Since WKPND is a pending register for the occurrence of selected wakeup conditions, the COP888CS will not enter the HALT mode if any Wakeup bit is both enabled and pending. Consequently, the user has the responsibility of clearing the pending flags before attempting to enter the HALT mode.

WKEN, WKPND and WKEDG are all read/write registers, and are cleared at reset.

PORT L INTERRUPTS

Port L provides the user with an additional eight fully selectable, edge sensitive interrupts which are all vectored into the same service subroutine.

The interrupt from Port L shares logic with the wake up circuitry. The register WKEN allows interrupts from Port L to be individually enabled or disabled. The register WKEDG specifies the trigger condition to be either a positive or a negative edge. Finally, the register WKPND latches in the pending trigger conditions.

The GIE (Global Interrupt Enable) bit enables the interrupt function.

A control flag, LPEN, functions as a global interrupt enable for Port L interrupts. Setting the LPEN flag will enable interrupts and vice versa. A separate global pending flag is not needed since the register WKPND is adequate.

Since Port L is also used for waking the COP888CS out of the HALT or IDLE modes, the user can elect to exit the HALT or IDLE modes either with or without the interrupt enabled. If he elects to disable the interrupt, then the COP888CS will restart execution from the instruction immediately following the instruction that placed the microcontroller in the HALT or IDLE modes. In the other case, the COP888CS will first execute the interrupt service routine and then revert to normal operation.

The Wakeup signal will not start the chip running immediately since crystal oscillators or ceramic resonators have a finite start up time. The IDLE Timer (T0) generates a fixed delay to ensure that the oscillator has indeed stabilized before allowing the COP888CS to execute instructions. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry and the IDLE Timer T0 are enabled. The IDLE Timer is loaded with a value of 256 and is clocked from the t_c instruction cycle clock. The t_c clock is derived by dividing down the oscillator clock by a factor of 10. A Schmitt trigger following the CKI on-chip inverter ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

If the RC clock option is used, the fixed delay is under software control. A control flag, CLKDLY, in the G7 configuration bit allows the clock start up delay to be optionally inserted. Setting CLKDLY flag high will cause clock start up delay to be inserted and resetting it will exclude the clock start up delay. The CLKDLY flag is cleared during reset, so the clock start up delay is not present following reset with the RC clock options.

UART

The COP888CS contains a full-duplex software programmable UART. The UART *(Figure 12)* consists of a transmit shift register, a receiver shift register and seven addressable registers, as follows: a transmit buffer register (TBUF), a receiver buffer register (RBUF), a UART control and status register (ENU), a UART receive control and status register (ENUR), a UART interrupt and clock source register (ENUI), a prescaler select register (PSR) and baud (BAUD) register. The ENU register contains flags for transmit and receive functions; this register also determines the length of the data frame (7, 8 or 9 bits), the value of the ninth bit in transmission, and parity selection bits. The ENUR register flags framming, data overrun and parity errors while the UART is receiving.

Other functions of the ENUR register include saving the ninth bit received in the data frame, enabling or disabling the UART's attention mode of operation and providing additional receiver/transmitter status information via RCVG and XMTG bits. The determination of an internal or external clock source is done by the ENUI register, as well as selecting the number of stop bits and enabling or disabling transmit and receive interrupts. A control flag in this register can also select the UART mode of operation: asynchronous or synchronous.

UART CONTROL AND STATUS REGISTERS

The operation of the UART is programmed through three registers: ENU, ENUR and ENUI. The function of the individual bits in these registers is as follows:

ENU-UART Control and Status Register (Address at 0BA)

PEN	PSEL1	XBIT9/ PSEL0	CHL1	CHL0	ERR	RBFL	TBMT
0RW	0RW	0RW	0RW	0RW	0R	0R	1R

Bit 7 Bit 0

ENUR-UART Receive Control and Status Register (Address at 0BB)

DOE	FE	PE	SPARE	RBIT9	ATTN	XMTG	RCVG
0RD	0RD	0RD	0RW*	0R	0RW	0R	0R

Bit7 Bit0

ENUI-UART Interrupt and Clock Source Register (Address at 0BC)

STP2	STP78	ETDX	SSEL	XRCLK	XTCLK	ERI	ETI
0RW	0RW	0RW	0RW	0RW	0RW	0RW	0RW

Bit7 Bit0

*Bit is not used.

0 Bit is cleared on reset.

1 Bit is set to one on reset.

R Bit is read-only; it cannot be written by software.

RW Bit is read/write.

D Bit is cleared on read; when read by software as a one, it is cleared automatically. Writing to the bit does not affect its state.

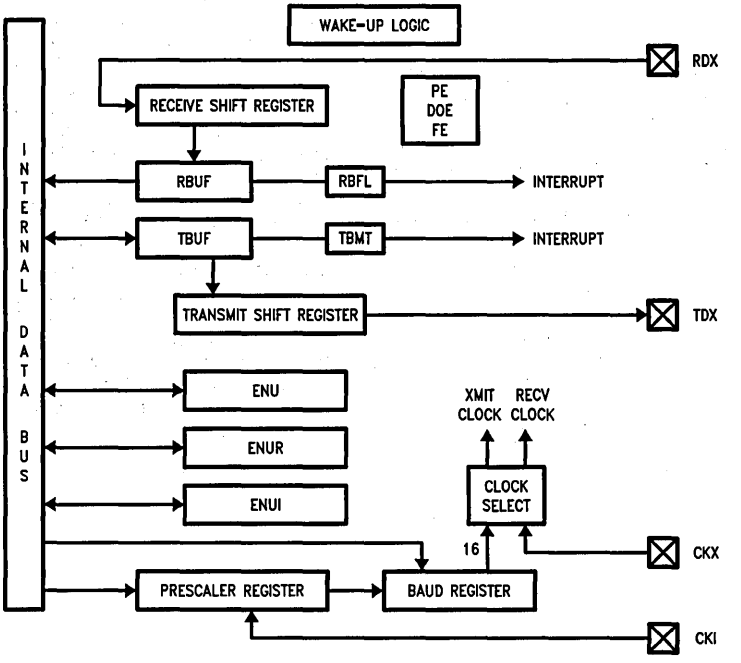

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FIGURE 12. UART Block Diagram

UART (Continued)

DESCRIPTION OF UART REGISTER BITS

ENU—UART CONTROL AND STATUS REGISTER

TBMT: This bit is set when the UART transfers a byte of data from the TBUF register into the TSFT register for transmission. It is automatically reset when software writes into the TBUF register.

RBFL: This bit is set when the UART has received a complete character and has copied it into the RBUF register. It is automatically reset when software reads the character from RBUF.

ERR: This bit is a global UART error flag which gets set if any or a combination of the errors (DOE, FE, PE) occur.

CHL1, CHL0: These bits select the character frame format. Parity is not included and is generated/verified by hardware.

CHL1 = 0, CHL0 = 0 The frame contains eight data bits.
CHL1 = 0, CHL0 = 1 The frame contains seven data bits.
CHL1 = 1, CHL0 = 0 The frame contains nine data bits.
CHL1 = 1, CHL0 = 1 Loopback Mode selected. Transmitter output internally looped back to receiver input. Nine bit framing format is used.

XBIT9/PSEL0: Programs the ninth bit for transmission when the UART is operating with nine data bits per frame. For seven or eight data bits per frame, this bit in conjunction with PSEL1 selects parity.

PSEL1, PSEL0: Parity select bits.

PSEL1 = 0, PSEL0 = 0 Odd Parity (if Parity enabled)
PSEL1 = 0, PSEL0 = 1 Even Parity (if Parity enabled)
PSEL1 = 1, PSEL0 = 0 Mark(1) (if Parity enabled)
PSEL1 = 1, PSEL0 = 1 Space(0) (if Parity enabled)

PEN: This bit enables/disables Parity (7- and 8-bit modes only).

PEN = 0 Parity disabled.
PEN = 1 Parity enabled.

ENUR—UART RECEIVE CONTROL AND STATUS REGISTER

RCVG: This bit is set high whenever a framing error occurs and goes low when RDX goes high.

XMTG: This bit is set to indicate that the UART is transmitting. It gets reset at the end of the last frame (end of last Stop bit).

ATTN: ATTENTION Mode is enabled while this bit is set. This bit is cleared automatically on receiving a character with data bit nine set.

RBIT9: Contains the ninth data bit received when the UART is operating with nine data bits per frame.

SPARE: Reserved for future use.

PE: Flags a Parity Error.

PE = 0 Indicates no Parity Error has been detected since the last time the ENUR register was read.
PE = 1 Indicates the occurence of a Parity Error.

FE: Flags a Framing Error.

FE = 0 Indicates no Framing Error has been detected since the last time the ENUR register was read.
FE = 1 Indicates the occurence of a Framing Error.

DOE: Flags a Data Overrun Error.

DOE = 0 Indicates no Data Overrun Error has been detected since the last time the ENUR register was read.
DOE = 1 Indicates the occurence of a Data Overrun Error.

ENUI—UART INTERRUPT AND CLOCK SOURCE REGISTER

ETI: This bit enables/disables interrupt from the transmitter section.

ETI = 0 Interrupt from the transmitter is disabled.
ETI = 1 Interrupt from the transmitter is enabled.

ERI: This bit enables/disables interrupt from the receiver section.

ERI = 0 Interrupt from the receiver is disabled.
ERI = 1 Interrupt from the receiver is enabled.

XTCLK: This bit selects the clock source for the transmitter-section.

XTCLK = 0 The clock source is selected through the PSR and BAUD registers.
XTCLK = 1 Signal on CKX (L1) pin is used as the clock.

XRCLK: This bit selects the clock source for the receiver section.

XRCLK = 0 The clock source is selected through the PSR and BAUD registers.
XRCLK = 1 Signal on CKX (L1) pin is used as the clock.

SSEL: UART mode select.

SSEL = 0 Asynchronous Mode.
SSEL = 1 Synchronous Mode.

ETDX: TDX (UART Transmit Pin) is the alternate function assigned to Port L pin L2; it is selected by setting ETDX bit. To simulate line break generation, software should reset ETDX bit and output logic zero to TDX pin through Port L data and configuration registers.

STP78: This bit is set to program the last Stop bit to be 7/8th of a bit in length.

STP2: This bit programs the number of Stop bits to be transmitted.

STP2 = 0 One Stop bit transmitted.
STP2 = 1 Two Stop bits transmitted.

Associated I/O Pins

Data is transmitted on the TDX pin and received on the RDX pin. TDX is the alternate function assigned to Port L pin L2; it is selected by setting ETDX (in the ENUI register) to one. RDX is an inherent function of Port L pin L3, requiring no setup.

The baud rate clock for the UART can be generated on-chip, or can be taken from an external source. Port L pin L1 (CKX) is the external clock I/O pin. The CKX pin can be either an input or an output, as determined by Port L Configuration and Data registers (Bit 1). As an input, it accepts a clock signal which may be selected to drive the transmitter and/or receiver. As an output, it presents the internal Baud Rate Generator output.

UART Operation

The UART has two modes of operation: asynchronous mode and synchronous mode.

ASYNCHRONOUS MODE

This mode is selected by resetting the SSEL (in the ENUI register) bit to zero. The input frequency to the UART is 16 times the baud rate.

The TSFT and TBUF registers double-buffer data for transmission. While TSFT is shifting out the current character on the TDX pin, the TBUF register may be loaded by software with the next byte to be transmitted. When TSFT finishes transmitting the current character the contents of TBUF are transferred to the TSFT register and the Transmit Buffer Empty Flag (TBMT in the ENU register) is set. The TBMT flag is automatically reset by the UART when software loads a new character into the TBUF register. There is also the XMTG bit which is set to indicate that the UART is transmitting. This bit gets reset at the end of the last frame (end of last Stop bit). TBUF is a read/write register.

The RSFT and RBUF registers double-buffer data being received. The UART receiver continually monitors the signal on the RDX pin for a low level to detect the beginning of a Start bit. Upon sensing this low level, it waits for half a bit time and samples again. If the RDX pin is still low, the receiver considers this to be a valid Start bit, and the remaining bits in the character frame are each sampled a single time, at the mid-bit position. Serial data input on the RDX pin is shifted into the RSFT register. Upon receiving the complete character, the contents of the RSFT register are copied into the RBUF register and the Received Buffer Full Flag (RBFL) is set. RBFL is automatically reset when software reads the character from the RBUF register. RBUF is a read only register. There is also the RCVG bit which is set high when a framing error occurs and goes low once RDX goes high. TBMT, XMTG, RBFL and RCVG are read only bits.

SYNCHRONOUS MODE

In this mode data is transferred synchronously with the clock. Data is transmitted on the rising edge and received on the falling edge of the synchronous clock.

This mode is selected by setting SSEL bit in the ENUI register. The input frequency to the UART is the same as the baud rate.

When an external clock input is selected at the CKX pin, data transmit and receive are performed synchronously with this clock through TDX/RDX pins.

If data transmit and receive are selected with the CKX pin as clock output, the μC generates the synchronous clock output at the CKX pin. The internal baud rate generator is used to produce the synchronous clock. Data transmit and receive are performed synchronously with this clock.

FRAMING FORMATS

The UART supports several serial framing formats *(Figure 13)*. The format is selected using control bits in the ENU, ENUR and ENUI registers.

The first format (1, 1a, 1b, 1c) for data transmission (CHL0 = 1, CHL1 = 0) consists of Start bit, seven Data bits (excluding parity) and 7/8, one or two Stop bits. In applications using parity, the parity bit is generated and verified by hardware.

The second format (CHL0 = 0, CHL1 = 0) consists of one Start bit, eight Data bits (excluding parity) and 7/8, one or two Stop bits. Parity bit is generated and verified by hardware.

The third format for transmission (CHL0 = 0, CHL1 = 1) consists of one Start bit, nine Data bits and 7/8, one or two Stop bits. This format also supports the UART "ATTENTION" feature. When operating in this format, all eight bits of TBUF and RBUF are used for data. The ninth data bit is transmitted and received using two bits in the ENU and ENUR registers, called XBIT9 and RBIT9. RBIT9 is a read only bit. Parity is not generated or verified in this mode.

For any of the above framing formats, the last Stop bit can be programmed to be 7/8th of a bit in length. If two Stop bits are selected and the 7/8th bit is set (selected), the second Stop bit will be 7/8th of a bit in length.

The parity is enabled/disabled by PEN bit located in the ENU register. Parity is selected for 7- and 8-bit modes only. If parity is enabled (PEN = 1), the parity selection is then performed by PSEL0 and PSEL1 bits located in the ENU register.

Note that the XBIT9/PSEL0 bit located in the ENU register serves two mutually exclusive functions. This bit programs the ninth bit for transmission when the UART is operating with nine data bits per frame. There is no parity selection in this framing format. For other framing formats XBIT9 is not needed and the bit is PSEL0 used in conjunction with PSEL1 to select parity.

The frame formats for the receiver differ from the transmitter in the number of Stop bits required. The receiver only requires one Stop bit in a frame, regardless of the setting of the Stop bit selection bits in the control register. Note that an implicit assumption is made for full duplex UART operation that the framing formats are the same for the transmitter and receiver.

UART Operation (Continued)

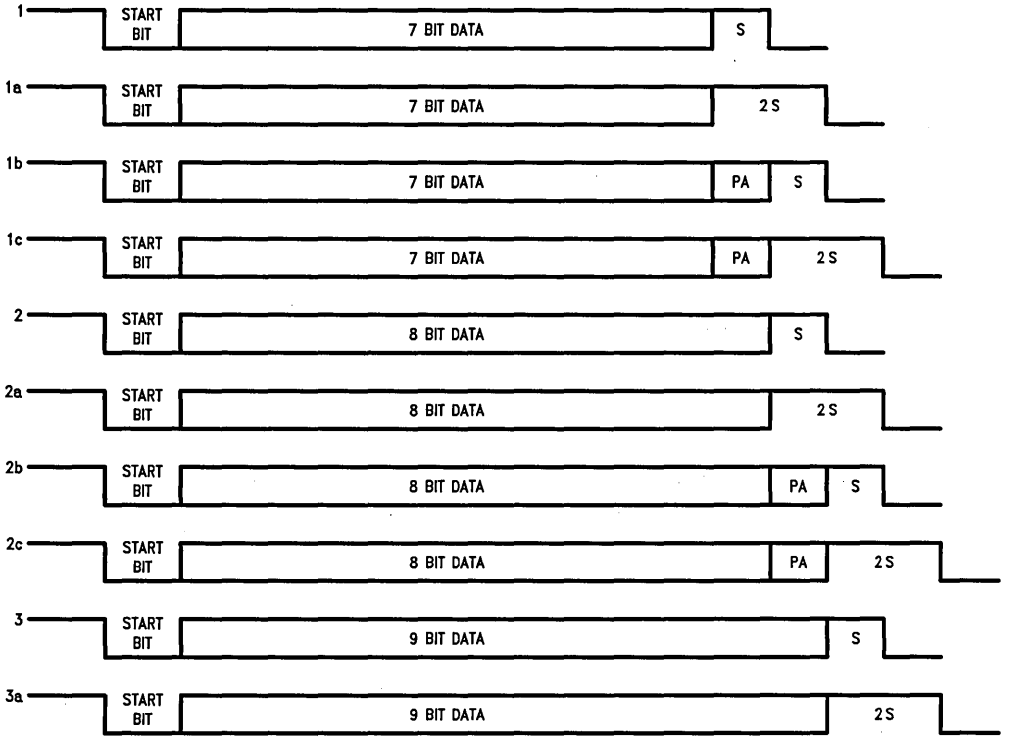

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FIGURE 13. Framing Formats

UART INTERRUPTS

The UART is capable of generating interrupts. Interrupts are generated on Receive Buffer Full and Transmit Buffer Empty. Both interrupts have individual interrupt vectors. Two bytes of program memory space are reserved for each interrupt vector. The two vectors are located at addresses 0xEC to 0xEF Hex in the program memory space. The interrupts can be individually enabled or disabled using Enable Transmit Interrupt (ETI) and Enable Receive Interrupt (ERI) bits in the ENUI register.

The interrupt from the Transmitter is set pending, and remains pending, as long as both the TBMT and ETI bits are set. To remove this interrupt, software must either clear the ETI bit or write to the TBUF register (thus clearing the TBMT bit).

The interrupt from the receiver is set pending, and remains pending, as long as both the RBFL and ERI bits are set. To remove this interrupt, software must either clear the ERI bit or read from the RBUF register (thus clearing the RBFL bit).

Baud Clock Generation

The clock inputs to the transmitter and receiver sections of the UART can be individually selected to come either from an external source at the CKX pin (port L, pin L1) or from a source selected in the PSR and BAUD registers. Internally, the basic baud clock is created from the oscillator frequency through a two-stage divider chain consisting of a 1–16 (increments of 0.5) prescaler and an 11-bit binary counter. *(Figure 14)* The divide factors are specified through two read/write registers shown in *Figure 15.* Note that the 11-bit Baud Rate Divisor spills over into the Prescaler Select Register (PSR). PSR is cleared upon reset.

As shown in Table I, a Prescaler Factor of 0 corresponds to NO CLOCK. NO CLOCK condition is the UART power down mode where the UART clock is turned off for power saving purpose. The user must also turn the UART clock off when a different baud rate is chosen.

The correspondences between the 5-bit Prescaler Select and Prescaler factors are shown in Table I. Therer are many ways to calculate the two divisor factors, but one particularly effective method would be to achieve a 1.8432 MHz frequency coming out of the first stage. The 1.8432 MHz prescaler output is then used to drive the software programmable baud rate counter to create a x16 clock for the following baud rates: 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19200 and 38400 (Table II). Other baud rates may be created by using appropriate divisors. The x16 clock is then divided by 16 to provide the rate for the serial shift registers of the transmitter and receiver.

Baud Clock Generation (Continued)

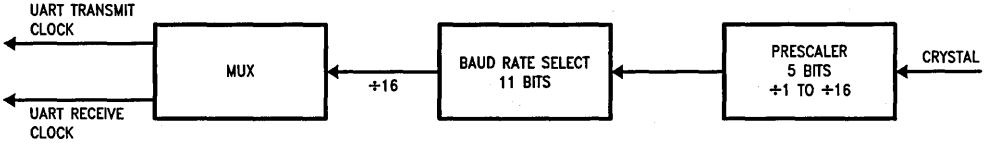

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FIGURE 14. UART BAUD Clock Generation

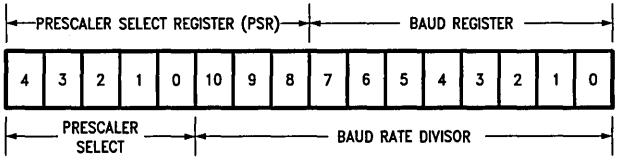

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FIGURE 15. UART BAUD Clock Divisor Registers

TABLE I. Prescaler Factors

Prescaler Select	Prescaler Factor
00000	NO CLOCK
00001	1
00010	1.5
00011	2
00100	2.5
00101	3
00110	3.5
00111	4
01000	4.5
01001	5
01010	5.5
01011	6
01100	6.5
01101	7
01110	7.5
01111	8
10000	8.5
10001	9
10010	9.5
10011	10
10100	10.5
10101	11
10110	11.5
10111	12
11000	12.5
11001	13
11010	13.5
11011	14
11100	14.5
11101	15
11110	15.5
11111	16

TABLE II. Baud Rate Divisors (1.8432 MHz Prescaler Output)

Baud Rate	Baud Rate Divisor − 1 (N-1)
110 (110.03)	1046
134.5 (134.58)	855
150	767
300	383
600	191
1200	95
1800	63
2400	47
3600	31
4800	23
7200	15
9600	11
19200	5
38400	2

The entries in Table II assume a prescaler output of 1.8432 MHz. In the asynchronous mode the baud rate could be as high as 625k.

As an example, considering the Asynchronous Mode and a CKI clock of 4.608 MHz, the prescaler factor selected is:

$$4.608/1.8432 = 2.5$$

The 2.5 entry is available in Table I. The 1.8432 MHz prescaler output is then used with proper Baud Rate Divisor (Table II) to obtain different baud rates. For a baud rate of 19200 e.g., the entry in Table II is 5.

$N - 1 = 5$ ($N - 1$ is the value from Table II)

$N = 6$ (N is the Baud Rate Divisor)

Baud Rate $= 1.8432\ \text{MHz}/(16 \times 6) = 19200$

The divide by 16 is performed because in the asynchronous mode, the input frequency to the UART is 16 times the baud rate. The equation to calculate baud rates is given below.

The actual Baud Rate may be found from:

$$BR = Fc/(16 \times N \times P)$$

Baud Clock Generation (Continued)

Where:

BR is the Baud Rate

Fc is the CKI frequency

N is the Baud Rate Divisor (Table II).

P is the Prescaler Divide Factor selected by the value in the Prescaler Select Register (Table I)

Note: In the Synchronous Mode, the divisor 16 is replaced by two if internal Baud Rate generator is used. Replaced by one if external clock is used.

Example:

Asynchronous Mode:

Crystal Frequency = 5 MHz

Desired baud rate = 9600

Using the above equation N × P can be calculated first.

$$N \times P = (5 \times 10^6)/(16 \times 9600) = 32.552$$

Now 32.552 is divided by each Prescaler Factor (Table II) to obtain a value closest to an integer. This factor happens to be 6.5 (P = 6.5).

$$N = 32.552/6.5 = 5.008\ (N = 5)$$

The programmed value (from Table II) should be 4 (N − 1).

Using the above values calculated for N and P:

$$BR = (5 \times 10^6)/(16 \times 5 \times 6.5) = 9615.384$$

$$\%\ \text{error} = (9615.385 - 9600)/9600 = 0.16$$

Effect of HALT/IDLE

The UART logic is reinitialized when either the HALT or IDLE modes are entered. This reinitialization sets the TBMT flag and resets all read only bits in the UART control and status registers. Read/Write bits remain unchanged. The Transmit Buffer (TBUF) is not affected, but the Transmit Shift register (TSFT) bits are set to one. The receiver registers RBUF and RSFT are not affected.

The μC will exit from the HALT/IDLE modes when the Start bit of a character is detected at the RDX (L3) pin. This feature is obtained by using the Multi-Input Wakeup scheme provided on the μC.

Before entering the HALT or IDLE modes the user program must select the Wakeup source to be on the RDX pin. This selection is done by setting bit 3 of WKEN (Wakeup Enable) register. The Wakeup trigger condition is then selected to be high to low transition. This is done via the WKEDG register (Bit 3 is zero.)

If the microcontroller is halted and crystal oscillator is used, the Wakeup signal will not start the chip running immediately because of the finite start up time requirement of the crystal oscillator. The idle timer (T0) generates a fixed delay to ensure that the oscillator has indeed stabilized before allowing the μC to execute code. The user has to consider this delay when data transfer is expected immediately after exiting the HALT mode.

Diagnostic

Bits CHARL0 and CHARL1 in the ENU register provide a loopback feature for diagnostic testing of the UART. When these bits are set to one, the following occur: The receiver input pin (RDX) is internally connected to the transmitter output pin (TDX); the output of the Transmitter Shift Register is "looped back" into the Receive Shift Register input. In this mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and receive data paths of the UART.

Note that the framing format for this mode is the nine bit format; one Start bit, nine data bits, and 7/8, one or two Stop bits. Parity is not generated or verified in this mode.

Attention Mode

The UART Receiver section supports an alternate mode of operation, referred to as ATTENTION Mode. This mode of operation is selected by the ATTN bit in the ENUR register. The data format for transmission must also be selected as having nine Data bits and either 7/8, one or two Stop bits.

The ATTENTION mode of operation is intended for use in networking the COP888CS with other processors. Typically in such environments the messages consists of device addresses, indicating which of several destinations should receive them, and the actual data. This Mode supports a scheme in which addresses are flagged by having the ninth bit of the data field set to a 1. If the ninth bit is reset to a zero the byte is a Data byte.

While in ATTENTION mode, the UART monitors the communication flow, but ignores all characters until an address character is received. Upon receiving an address character, the UART signals that the character is ready by setting the RBFL flag, which in turn interrupts the processor if UART Receiver interrupts are enabled. The ATTN bit is also cleared automatically at this point, so that data characters as well as address characters are recognized. Software examines the contents of the RBUF and responds by deciding either to accept the subsequent data stream (by leaving the ATTN bit reset) or to wait until the next address character is seen (by setting the ATTN bit again).

Operation of the UART Transmitter is not affected by selection of this Mode. The value of the ninth bit to be transmitted is programmed by setting XBIT9 appropriately. The value of the ninth bit received is obtained by reading RBIT9. Since this bit is located in ENUR register where the error flags reside, a bit operation on it will reset the error flags.

Comparator

The COP888CS contains one differential comparator, with a pair of inputs (positive and negative) and an output. Ports I1–I3 are used for the comparator. The following is the Port I assignment:

- I1 Comparator1 negative input
- I2 Comparator1 positive input
- I3 Comparator1 output

A Comparator Select Register (CMPSL) is used to enable the comparators, read the outputs of the comparator internally, and enable the output of the comparator to the pins. Two control bits (enable and output enable) and one result bit are associated with the comparator. The comparator result bit (CMP1RD) is read only bit which will read as zero if the comparator is not enabled. The Comparator Select Register is cleared with reset, resulting in the comparator being disabled. The comparator should also be disabled before entering either the HALT or IDLE modes in order to save power. The configuration of the CMPSL register is as follows:

Comparator (Continued)

CMPSL REGISTER (ADDRESS X'00B7)

The CMPSL register contains the following bits:

CMP1EN Enable comparator 1

CMP1RD Comparator 1 result (this is a read only bit, which will read as 0 if the comparator is not enabled)

CMP10E Selects pin I3 as comparator 1 output provided that CMPIEN is set to enable the comparator

Unused	Unused	Unused	Unused	CMP10E	CMP1RD	CMP1EN	Unused
Bit 7							Bit 0

Comparator outputs have the same spec as Ports L and G except that the rise and fall times are symmetrical.

Interrupts

The COP888CS supports a vectored interrupt scheme. It supports a total of fourteen interrupt sources. The following table lists all the possible COP888CS interrupt sources, their arbitration ranking and the memory locations reserved for the interrupt vector for each source.

Two bytes of program memory space are reserved for each interrupt source. All interrupt sources except the software interrupt are maskable. Each of the maskable interrupts have an Enable bit and a Pending bit. A maskable interrupt is active if its associated enable and pending bits are set. If GIE = 1 and an interrupt is active, then the processor will be interrupted as soon as it is ready to start executing an instruction except if the above conditions happen during the Software Trap service routine. This exception is described in the Software Trap sub-section.

The interruption process is accomplished with the INTR instruction (opcode 00), which is jammed inside the Instruction Register and replaces the opcode about to be executed. The following steps are performed for every interrupt:

1. The GIE (Global Interrupt Enable) bit is reset.
2. The address of the instruction about to be executed is pushed into the stack.
3. The PC (Program Counter) branches to address 00FF. This procedure takes 7 t_c cycles to execute.

At this time, since GIE = 0, other maskable interrupts are disabled. The user is now free to do whatever context switching is required by saving the context of the machine in the stack with PUSH instructions. The user would then program a VIS (Vector Interrupt Select) instruction in order to branch to the interrupt service routine of the highest priority interrupt enabled and pending at the time of the VIS. Note that this is not necessarily the interrupt that caused the branch to address location 00FF Hex prior to the context switching.

Thus, if an interrupt with a higher rank than the one which caused the interruption becomes active before the decision of which interrupt to service is made by the VIS, then the interrupt with the higher rank will override any lower ones and will be acknowledged. The lower priority interrupt(s) are still pending, however, and will cause another interrupt immediately following the completion of the interrupt service routine associated with the higher priority interrupt just serviced. This lower priority interrupt will occur immediately following the RETI (Return from Interrupt) instruction at the end of the interrupt service routine just completed.

Inside the interrupt service routine, the associated pending bit has to be cleared by software. The RETI (Return from Interrupt) instruction at the end of the interrupt service rou-

Arbitration Ranking	Source	Description	Vector Address Hi-Low Byte
(1) Highest	Software	INTR Instruction	0yFE–0yFF
	Reserved	for Future Use	0yFC–0yFD
(2)	External	Pin G0 Edge	0yFA–0yFB
(3)	Timer T0	Underflow	0yF8–0yF9
(4)	Timer T1	T1A/Underflow	0yF6–0yF7
(5)	Timer T1	T1B	0yF4–0yF5
(6)	MICROWIRE/PLUS	BUSY Goes Low	0yF2–0yF3
	Reserved	for Future Use	0yF0–0yF1
(7)	UART	Receive	0yEE–0yEF
(8)	UART	Transmit	0yEC–0yED
(9)	Reserved		0yEA–0yEB
(10)	Reserved		0yE8–0yE9
(11)	Reserved		0yE6–0yE7
(12)	Reserved		0yE4–0yE5
(13)	Port L/Wakeup	Port L Edge	0yE2–0yE3
(14) Lowest	Default	VIS Instr. Execution without Any Interrupts	0yE0–0yE1

y is VIS page, $y \neq 0$.

Interrupts (Continued)

tine will set the GIE (Global Interrupt Enable) bit, allowing the processor to be interrupted again if another interrupt is active and pending.

The VIS instruction looks at all the active interrupts at the time it is executed and performs an indirect jump to the beginning of the service routine of the one with the highest rank.

The addresses of the different interrupt service routines, called vectors, are chosen by the user and stored in ROM in a table starting at 01E0 (assuming that VIS is located between 00FF and 01DF). The vectors are 15-bit wide and therefore occupy 2 ROM locations.

VIS and the vector table must be located in the same 256-byte block (0y00 to 0yFF) except if VIS is located at the last address of a block. In this case, the table must be in the next block. The vector table cannot be inserted in the first 256-byte block (y ≠ 0).

The vector of the maskable interrupt with the lowest rank is located at 0yE0 (Hi-Order byte) and 0yE1 (Lo-Order byte) and so forth in increasing rank number. The vector of the maskable interrupt with the highest rank is located at 0yFA (Hi-Order byte) and 0yFB (Lo-Order byte).

The Software Trap has the highest rank and its vector is located at 0yFE and 0yFF.

If, by accident, a VIS gets executed and no interrupt is active, then the PC (Program Counter) will branch to a vector located at 0yE0–0yE1. This vector can point to the Software Trap (ST) interrupt service routine, or to another special service routine as desired.

Figure 16 shows the COP888CS Interrupt block diagram.

SOFTWARE TRAP

The Software Trap (ST) is a special kind of non-maskable interrupt which occurs when the INTR instruction (used to acknowledge interrupts) is fetched from ROM and placed inside the instruction register. This may happen when the PC is pointing beyond the available ROM address space or when the stack is over-popped.

When an ST occurs, the user can re-initialize the stack pointer and do a recovery procedure (similar to reset, but not necessarily containing all of the same initialization procedures) before restarting.

The occurrence of an ST is latched into the ST pending bit. The GIE bit is not affected and the ST pending bit **(not accessible by the user)** is used to inhibit other interrupts and to direct the program to the ST service routine with the VIS instruction. The RPND instruction is used to clear the software interrupt pending bit. This pending bit is also cleared on reset.

The ST has the highest rank among all interrupts.

Nothing (except another ST) can interrupt an ST being serviced.

WATCHDOG

The COP888CS contains a WATCHDOG and clock monitor. The WATCHDOG is designed to detect the user program getting stuck in infinite loops resulting in loss of program control or "runaway" programs. The Clock Monitor is used to detect the absence of a clock or a very slow clock below a specified rate on the CKI pin.

The WATCHDOG consists of two independent logic blocks: WD UPPER and WD LOWER. WD UPPER establishes the upper limit on the service window and WD LOWER defines the lower limit of the service window.

Servicing the WATCHDOG consists of writing a specific value to a WATCHDOG Service Register named WDSVR which is memory mapped in the RAM. This value is composed of three fields, consisting of a 2-bit Window Select, a 5-bit Key Data field, and the 1-bit Clock Monitor Select field. Table III shows the WDSVR register.

The lower limit of the service window is fixed at 2048 instruction cycles. Bits 7 and 6 of the WDSVR register allow the user to pick an upper limit of the service window.

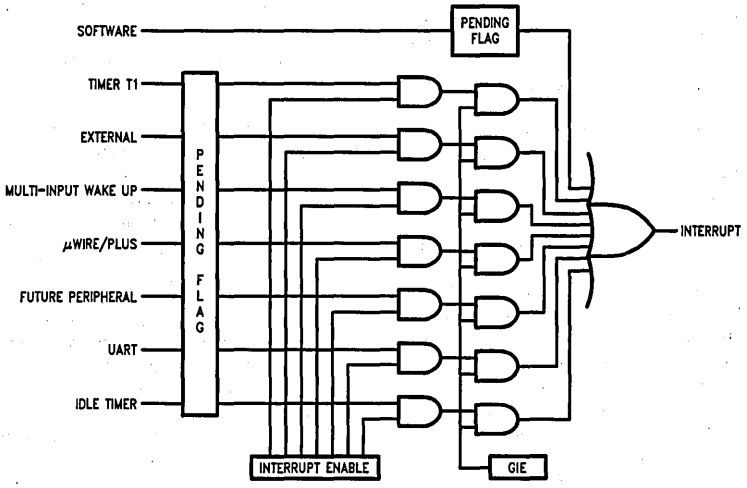

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FIGURE 16. COP888CS Interrupt Block Diagram

WATCHDOG (Continued)

Table IV shows the four possible combinations of lower and upper limits for the WATCHDOG service window. This flexibility in choosing the WATCHDOG service window prevents any undue burden on the user software.

Bits 5, 4, 3, 2 and 1 of the WDSVR register represent the 5-bit Key Data field. The key data is fixed at 01100. Bit 0 of the WDSVR Register is the Clock Monitor Select bit.

TABLE III. WATCHDOG Service Register (WDSVR)

Window Select		Key Data					Clock Monitor
X	X	0	1	1	0	0	Y
7	6	5	4	3	2	1	0

TABLE IV. WATCHDOG Service Window Select

WDSVR Bit 7	WDSVR Bit 6	Service Window (Lower-Upper Limits)
0	0	2k–8k t_C Cycles
0	1	2k–16k t_C Cycles
1	0	2k–32k t_C Cycles
1	1	2k–64k t_C Cycles

Clock Monitor

The Clock Monitor aboard the COP888CS can be selected or deselected under program control. The Clock Monitor is guaranteed not to reject the clock if the instruction cycle clock ($1/t_C$) is greater or equal to 10 kHz. This equates to a clock input rate on CKI of greater or equal to 100 kHz.

WATCHDOG Operation

The WATCHDOG and Clock Monitor are disabled during reset. The COP888CS comes out of reset with the WATCHDOG armed, the WATCHDOG Window Select bits (bits 6, 7 of the WDSVR Register) set, and the Clock Monitor bit (bit 0 of the WDSVR Register) enabled. Thus, a Clock Monitor error will occur after coming out of reset, if the instruction cycle clock frequency has not reached a minimum specified value, including the case where the oscillator fails to start.

The WDSVR register can be written to only once after reset and the key data (bits 5 through 1 of the WDSVR Register) must match to be a valid write. This write to the WDSVR register involves two irrevocable choices: (i) the selection of the WATCHDOG service window (ii) enabling or disabling of the Clock Monitor. Hence, the first write to WDSVR Register involves selecting or deselecting the Clock Monitor, select the WATCHDOG service window and match the WATCHDOG key data. Subsequent writes to the WDSVR register will compare the value being written by the user to the WATCHDOG service window value and the key data (bits 7 through 1) in the WDSVR Register. Table V shows the sequence of events that can occur.

The user must service the WATCHDOG at least once before the upper limit of the service window expires. The WATCHDOG may not be serviced more than once in every lower limit of the service window. The user may service the WATCHDOG as many times as wished in the time period between the lower and upper limits of the service window. The first write to the WDSVR Register is also counted as a WATCHDOG service.

The WATCHDOG has an output pin associated with it. This is the WDOUT pin, on pin 1 of the port G. WDOUT is active low. The WDOUT pin is in the high impedance state in the inactive state. Upon triggering the WATCHDOG, the logic will pull the WDOUT (G1) pin low for an additional 16 t_C–32 t_C cycles after the signal level on WDOUT pin goes below the lower Schmitt trigger threshold. After this delay, the COP888CS will stop forcing the WDOUT output low.

The WATCHDOG service window will restart when the WDOUT pin goes high. It is recommended that the user tie the WDOUT pin back to V_{CC} through a resistor in order to pull WDOUT high.

A WATCHDOG service while the WDOUT signal is active will be ignored. The state of the WDOUT pin is not guaranteed on reset, but if it powers up low then the WATCHDOG will time out and WDOUT will enter high impedance state.

The Clock Monitor forces the G1 pin low upon detecting a clock frequency error. The Clock Monitor error will continue until the clock frequency has reached the minimum specified value, after which the G1 output will enter the high impedance TRI-STATE mode following 16 t_C–32 t_C clock cycles. The Clock Monitor generates a continual Clock Monitor error if the oscillator fails to start, or fails to reach the minimum specified frequency. The specification for the Clock Monitor is as follows:

$1/t_C > 10$ kHz—No clock rejection.

$1/t_C < 10$ Hz—Guaranteed clock rejection.

WATCHDOG AND CLOCK MONITOR SUMMARY

The following salient points regarding the COP888 WATCHDOG and CLOCK MONITOR should be noted:

- Both the WATCHDOG and Clock Monitor detector circuits are inhibited during RESET.
- Following RESET, the WATCHDOG and CLOCK MONITOR are both enabled, with the WATCHDOG having the maximum service window selected.
- The WATCHDOG service window and Clock Monitor enable/disable option can only be changed once, during the initial WATCHDOG service following RESET.
- The initial WATCHDOG service must match the key data value in the WATCHDOG Service register WDSVR in order to avoid a WATCHDOG error.
- Subsequent WATCHDOG services must match all three data fields in WDSVR in order to avoid WATCHDOG errors.
- The correct key data value cannot be read from the WATCHDOG Service register WDSVR. Any attempt to read this key data value of 01100 from WDSVR will read as key data value of all 0's.
- The WATCHDOG detector circuit is inhibited during both the HALT and IDLE modes.
- The Clock Monitor detector circuit is active during both the HALT and IDLE modes. Consequently, the COP888 inadvertently entering the HALT mode wil be detected as a Clock Monitor error (provided that the Clock Monitor enable option has been selected by the program).
- With the single-pin R/C oscillator mask option selected and the CLKDLY bit reset, the WATCHDOG service window will resume following HALT mode from where it left off before entering the HALT mode.
- With the crystal oscillator mask option selected, or with the single-pin R/C oscillator mask option selected and the CLKDLY bit set, the WATCHDOG service window will

WATCHDOG Operation (Continued)

be set to its selected value from WDSVR following HALT. Consequently, the WATCHDOG should not be serviced for at least 2048 instruction cycles following HALT, but must be serviced within the selected window to avoid a WATCHDOG error.

- The IDLE timer T0 is not initialized with RESET.
- The user can sync in to the IDLE counter cycle with an IDLE counter (T0) interrupt or by monitoring the T0PND flag. The T0PND flag is set whenever the thirteenth bit of the IDLE counter toggles (every 4096 instruction cycles). The user is responsible for resetting the T0PND flag.
- A hardware WATCHDOG service occurs just as the COP888 exits the IDLE mode. Consequently, the WATCHDOG should not be serviced for at least 2048 instruction cycles following IDLE, but must be serviced within the selected window to avoid a WATCHDOG error.
- Following RESET, the initial WATCHDOG service (where the service window and the CLOCK MONITOR enable/disable must be selected) may be programmed anywhere within the maximum service window (65,536 instruction cycles) initialized by RESET. Note that this initial WATCHDOG service may be programmed within the initial 2048 instruction cycles without causing a WATCHDOG error.

Detection of Illegal Conditions

The COP888CS can detect various illegal conditions resulting from coding errors, transient noise, power supply voltage drops, runaway programs, etc.

Reading of undefined ROM gets zeros. The opcode for software interrupt is zero. If the program fetches instructions from undefined ROM, this will force a software interrupt, thus signaling that an illegal condition has occurred.

The subroutine stack grows down for each call (jump to subroutine), interrupt, or PUSH, and grows up for each return or POP. The stack pointer is initialized to RAM location 06F Hex during reset. Consequently, if there are more returns than calls, the stack pointer will point to addresses 070 and 071 Hex (which are undefined RAM). Undefined RAM from addresses 070 to 07F (Segment 0), 140 to 17F (Segment 1), and all other segments (i.e., Segments 3 . . . etc.) is read as all 1's, which in turn will cause the program to return to address 7FFF Hex. This is an undefined ROM location and the instruction fetched (all 0's) from this location will generate a software interrupt signaling an illegal condition.

Thus, the chip can detect the following illegal conditions:

a. Executing from undefined ROM

b. Over "POP"ing the stack by having more returns than calls.

When the software interrupt occurs, the user can re-initialize the stack pointer and do a recovery procedure before restarting (this recovery program is probably similar to that following reset, but might not contain the same program initialization procedures). The recovery program should reset the software interrupt pending bit using the RPND instruction.

MICROWIRE/PLUS

MICROWIRE/PLUS is a serial synchronous communications interface. The MICROWIRE/PLUS capability enables the COP888CS to interface with any of National Semiconductor's MICROWIRE peripherals (i.e. A/D converters, display drivers, E^2PROMs etc.) and with other microcontrollers which support the MICROWIRE interface. It consists of an 8-bit serial shift register (SIO) with serial data input (SI), serial data output (SO) and serial shift clock (SK). *Figure 17* shows a block diagram of the MICROWIRE/PLUS logic.

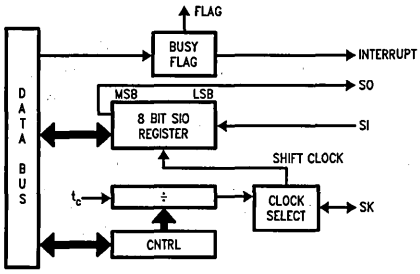

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FIGURE 17. MICROWIRE/PLUS Block Diagram

The shift clock can be selected from either an internal source or an external source. Operating the MICROWIRE/PLUS arrangement with the internal clock source is called the Master mode of operation. Similarly, operating the MICROWIRE/PLUS arrangement with an external shift clock is called the Slave mode of operation.

The CNTRL register is used to configure and control the MICROWIRE/PLUS mode. To use the MICROWIRE/PLUS, the MSEL bit in the CNTRL register is set to one. In the master mode, the SK clock rate is selected by the two bits, SL0 and SL1, in the CNTRL register. Table VI details the different clock rates that may be selected.

TABLE V. WATCHDOG Service Actions

Key Data	Window Data	Clock Monitor	Action
Match	Match	Match	Valid Service: Restart Service Window
Don't Care	Mismatch	Don't Care	Error: Generate WATCHDOG Output
Mismatch	Don't Care	Don't Care	Error: Generate WATCHDOG Output
Don't Care	Don't Care	Mismatch	Error: Generate WATCHDOG Output

TABLE VI. MICROWIRE/PLUS
Master Mode Clock Select

SL1	SL0	SK
0	0	$2 \times t_c$
0	1	$4 \times t_c$
1	x	$8 \times t_c$

Where t_c is the instruction cycle clock

MICROWIRE/PLUS (Continued)

MICROWIRE/PLUS OPERATION

Setting the BUSY bit in the PSW register causes the MICROWIRE/PLUS to start shifting the data. It gets reset when eight data bits have been shifted. The user may reset the BUSY bit by software to allow less than 8 bits to shift. If enabled, an interrupt is generated when eight data bits have been shifted. The COP888CS may enter the MICROWIRE/PLUS mode either as a Master or as a Slave. *Figure 14* shows how two COP888CS microcontrollers and several peripherals may be interconnected using the MICROWIRE/PLUS arrangements.

Warning:

The SIO register should only be loaded when the SK clock is low. Loading the SIO register while the SK clock is high will result in undefined data in the SIO register. SK clock is normally low when not shifting.

Setting the BUSY flag when the input SK clock is high in the MICROWIRE/PLUS slave mode may cause the current SK clock for the SIO shift register to be narrow. For safety, the BUSY flag should only be set when the input SK clock is low.

MICROWIRE/PLUS Master Mode Operation

In the MICROWIRE/PLUS Master mode of operation the shift clock (SK) is generated internally by the COP888CS. The MICROWIRE Master always initiates all data exchanges. The MSEL bit in the CNTRL register must be set to enable the SO and SK functions onto the G Port. The SO and SK pins must also be selected as outputs by setting appropriate bits in the Port G configuration register. Table VII summarizes the bit settings required for Master mode of operation.

MICROWIRE/PLUS Slave Mode Operation

In the MICROWIRE/PLUS Slave mode of operation the SK clock is generated by an external source. Setting the MSEL bit in the CNTRL register enables the SO and SK functions onto the G Port. The SK pin must be selected as an input and the SO pin is selected as an output pin by setting and resetting the appropriate bit in the Port G configuration register. Table VII summarizes the settings required to enter the Slave mode of operation.

The user must set the BUSY flag immediately upon entering the Slave mode. This will ensure that all data bits sent by the Master will be shifted properly. After eight clock pulses the BUSY flag will be cleared and the sequence may be repeated.

Alternate SK Phase Operation

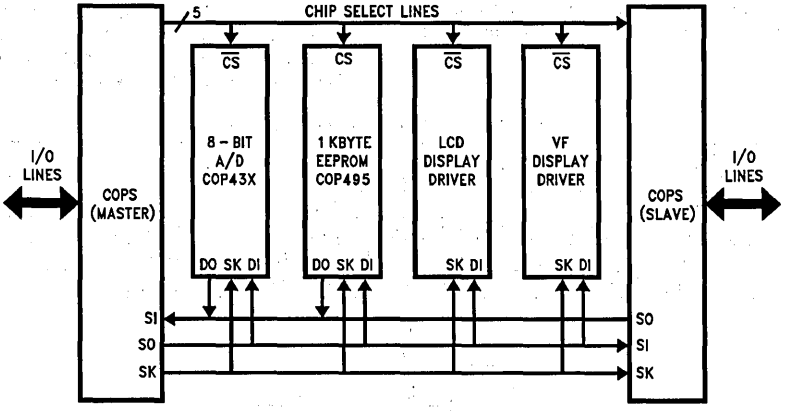
The COP888CS allows either the normal SK clock or an alternate phase SK clock to shift data in and out of the SIO register. In both the modes the SK is normally low. In the normal mode data is shifted in on the rising edge of the SK clock and the data is shifted out on the falling edge of the SK clock. The SIO register is shifted on each falling edge of the SK clock in the normal mode. In the alternate SK phase operation, data is shifted in on the falling edge of the SK clock and shifted out on the rising edge of the SK clock.

A control flag, SKSEL, allows either the normal SK clock or the alternate SK clock to be selected. Resetting SKSEL causes the MICROWIRE/PLUS logic to be clocked from the normal SK signal. Setting the SKSEL flag selects the alternate SK clock. The SKSEL is mapped into the G6 configuration bit. The SKSEL flag will power up in the reset condition, selecting the normal SK signal.

TABLE VII

This table assumes that the control flag MSEL is set.

G4 (SO) Config. Bit	G5 (SK) Config. Bit	G4 Fun.	G5 Fun.	Operation
1	1	SO	Int. SK	MICROWIRE/PLUS Master
0	1	TRI-STATE	Int. SK	MICROWIRE/PLUS Master
1	0	SO	Ext. SK	MICROWIRE/PLUS Slave
0	0	TRI-STATE	Ext. SK	MICROWIRE/PLUS Slave



TL/DD/10830–22

FIGURE 18. MICROWIRE/PLUS Application

Memory Map

All RAM, ports and registers (except A and PC) are mapped into data memory address space.

Address S/ADD REG	Contents
0000 to 006F	On-Chip RAM bytes (112 bytes)
0070 to 007F	Unused RAM Address Space (Reads As All Ones)
xx80 to xxAF	Unused RAM Address Space (Reads Undefined Data)
xxB0 to xxB6	Reserved
xxB7	Comparator Select Register (CMPSL)
xxB8	UART Transmit Buffer (TBUF)
xxB9	UART Receive Buffer (RBUF)
xxBA	UART Control and Status Register (ENU)
xxBB	UART Receive Control and Status Register (ENUR)
xxBC	UART Interrupt and Clock Source Register (ENUI)
xxBD	UART Baud Register (BAUD)
xxBE	UART Prescale Select Register (PSR)
xxBF	Reserved for UART
xxC0 to xxC6	Reserved
xxC7	WATCHDOG Service Register (Reg:WDSVR)
xxC8	MIWU Edge Select Register (Reg:WKEDG)
xxC9	MIWU Enable Register (Reg:WKEN)
xxCA	MIWU Pending Register (Reg:WKPND)
xxCB	Reserved
xxCC	Reserved
xxCD to xxCF	Reserved

Address S/ADD REG	Contents
xxD0	Port L Data Register
xxD1	Port L Configuration Register
xxD2	Port L Input Pins (Read Only)
xxD3	Reserved for Port L
xxD4	Port G Data Register
xxD5	Port G Configuration Register
xxD6	Port G Input Pins (Read Only)
xxD7	Port I Input Pins (Read Only)
xxD8	Port C Data Register
xxD9	Port C Configuration Register
xxDA	Port C Input Pins (Read Only)
xxDB	Reserved for Port C
xxDC	Port D
xxDD to DF	Reserved for Port D
xxE0 to xxE5	Reserved for EE Control Registers
xxE6	Timer T1 Autoload Register T1RB Lower Byte
xxE7	Timer T1 Autoload Register T1RB Upper Byte
xxE8	ICNTRL Register
xxE9	MICROWIRE/PLUS Shift Register
xxEA	Timer T1 Lower Byte
xxEB	Timer T1 Upper Byte
xxEC	Timer T1 Autoload Register T1RA Lower Byte
xxED	Timer T1 Autoload Register T1RA Upper Byte
xxEE	CNTRL Control Register
xxEF	PSW Register
xxF0 to FB	On-Chip RAM Mapped as Registers
xxFC	X Register
xxFD	SP Register
xxFE	B Register
xxFF	S Register
0100–013F	On-Chip RAM Bytes (64 bytes)

Reading memory locations 0070H–007FH (Segment 0) will return all ones. Reading unused memory locations 0080H–00AFH (Segment 0) will return undefined data. Reading unused memory locations 0140–017F (Segment 1) will return all ones. Reading memory locations from other Segments (i.e., Segment 2, Segment 3, ... etc.) will return all ones.

All reserved location reads undefined data.

Addressing Modes

The COP888CS has ten addressing modes, six for operand addressing and four for transfer of control.

OPERAND ADDRESSING MODES

Register Indirect

This is the "normal" addressing mode for the COP888CS. The operand is the data memory addressed by the B pointer or X pointer.

Register Indirect (with auto post increment or decrement of pointer)

This addressing mode is used with the LD and X instructions. The operand is the data memory addressed by the B pointer or X pointer. This is a register indirect mode that automatically post increments or decrements the B or X register after executing the instruction.

Direct

The instruction contains an 8-bit address field that directly points to the data memory for the operand.

Immediate

The instruction contains an 8-bit immediate field as the operand.

Short Immediate

This addressing mode is used with the Load B Immediate instruction. The instruction contains a 4-bit immediate field as the operand.

Indirect

This addressing mode is used with the LAID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a data operand from the program memory.

TRANSFER OF CONTROL ADDRESSING MODES

Relative

This mode is used for the JP instruction, with the instruction field being added to the program counter to get the new program location. JP has a range from −31 to +32 to allow a 1-byte relative jump (JP + 1 is implemented by a NOP instruction). There are no "pages" when using JP, since all 15 bits of PC are used.

Absolute

This mode is used with the JMP and JSR instructions, with the instruction field of 12 bits replacing the lower 12 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory segment.

Absolute Long

This mode is used with the JMPL and JSRL instructions, with the instruction field of 15 bits replacing the entire 15 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory space.

Indirect

This mode is used with the JID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a location in the program memory. The contents of this program memory location serve as a partial address (lower 8 bits of PC) for the jump to the next instruction.

Note: The VIS is a special case of the Indirect Transfer of Control addressing mode, where the double byte vector associated with the interrupt is transferred from adjacent addresses in the program memory into the program counter (PC) in order to jump to the associated interrupt service routine.

Instruction Set

Register and Symbol Definition

Registers	
A	8-Bit Accumulator Register
B	8-Bit Address Register
X	8-Bit Address Register
SP	8-Bit Stack Pointer Register
PC	15-Bit Program Counter Register
PU	Upper 7 Bits of PC
PL	Lower 8 Bits of PC
C	1 Bit of PSW Register for Carry
HC	1 Bit of PSW Register for Half Carry
GIE	1 Bit of PSW Register for Global Interrupt Enable
VU	Interrupt Vector Upper Byte
VL	Interrupt Vector Lower Byte

Symbols	
[B]	Memory Indirectly Addressed by B Register
[X]	Memory Indirectly Addressed by X Register
MD	Direct Addressed Memory
Mem	Direct Addressed Memory or [B]
Meml	Direct Addressed Memory or [B] or Immediate Data
Imm	8-Bit Immediate Data
Reg	Register Memory: Addresses F0 to FF (Includes B, X and SP)
Bit	Bit Number (0 to 7)
←	Loaded with
↔	Exchanged with

Instruction Set (Continued)

INSTRUCTION SET

ADD	A,Meml	ADD	A ← A + Meml
ADC	A,Meml	ADD with Carry	A ← A + Meml + C, C ← Carry HC ← Half Carry
SUBC	A,Meml	Subtract with Carry	A ← A − $\overline{\text{Meml}}$ + C, C ← Carry HC ← Half Carry
AND	A,Meml	Logical AND	A ← A and Meml
ANDSZ	A,Imm	Logical AND Immed., Skip if Zero	Skip next if (A and Imm) = 0
OR	A,Meml	Logical OR	A ← A or Meml
XOR	A,Meml	Logical EXclusive OR	A ← A xor Meml
IFEQ	MD,Imm	IF EQual	Compare MD and Imm, Do next if MD = Imm
IFEQ	A,Meml	IF EQual	Compare A and Meml, Do next if A = Meml
IFNE	A,Meml	IF Not Equal	Compare A and Meml, Do next if A ≠ Meml
IFGT	A,Meml	IF Greater Than	Compare A and Meml, Do next if A > Meml
IFBNE	#	If B Not Equal	Do next if lower 4 bits of B ≠ Imm
DRSZ	Reg	Decrement Reg., Skip if Zero	Reg ← Reg − 1, Skip if Reg = 0
SBIT	#,Mem	Set BIT	1 to bit, Mem (bit = 0 to 7 immediate)
RBIT	#,Mem	Reset BIT	0 to bit, Mem
IFBIT	#,Mem	IF BIT	If bit in A or Mem is true do next instruction
RPND		Reset PeNDing Flag	Reset Software Interrupt Pending Flag
X	A,Mem	EXchange A with Memory	A ⟷ Mem
LD	A,Meml	LoaD A with Memory	A ← Meml
LD	B,Imm	LoaD B with Immed.	B ← Imm
LD	Mem,Imm	LoaD Memory Immed	Mem ← Imm
LD	Reg,Imm	LoaD Register Memory Immed.	Reg ← Imm
X	A, [B ±]	EXchange A with Memory [B]	A ⟷ [B], (B ← B ±1)
X	A, [X ±]	EXchange A with Memory [X]	A ⟷ [X], (X ← ±1)
LD	A, [B±]	LoaD A with Memory [B]	A ← [B], (B ← B ±1)
LD	A, [X±]	LoaD A with Memory [X]	A ← [X], (X ← X±1)
LD	[B±],Imm	LoaD Memory [B] Immed.	[B] ← Imm, (B ← B±1)
CLR	A	CLeaR A	A ← 0
INC	A	INCrement A	A ← A + 1
DEC	A	DECrementA	A ← A − 1
LAID		Load A InDirect from ROM	A ← ROM (PU,A)
DCOR	A	Decimal CORrect A	A ← BCD correction of A (follows ADC, SUBC)
RRC	A	Rotate A Right thru C	C → A7 → ... → A0 → C
RLC	A	Rotate A Left thru C	C ← A7 ← ... ← A0 ← C
SWAP	A	SWAP nibbles of A	A7...A4 ⟷ A3...A0
SC		Set C	C ← 1, HC ← 1
RC		Reset C	C ← 0, HC ← 0
IFC		IF C	IF C is true, do next instruction
IFNC		IF Not C	If C is not true, do next instruction
POP	A	POP the stack into A	SP ← SP + 1, A ← [SP]
PUSH	A	PUSH A onto the stack	[SP] ← A, SP ← SP − 1
VIS		Vector to Interrupt Service Routine	PU ← [VU], PL ← [VL]
JMPL	Addr.	Jump absolute Long	PC ← ii (ii = 15 bits, 0 to 32k)
JMP	Addr.	Jump absolute	PC9...0 ← i (i = 12 bits)
JP	Disp.	Jump relative short	PC ← PC + r (r is −31 to +32, except 1)
JSRL	Addr.	Jump SubRoutine Long	[SP] ← PL, [SP−1] ← PU,SP−2, PC ← ii
JSR	Addr	Jump SubRoutine	[SP] ← PL, [SP−1] ← PU,SP−2, PC9...0 ← i
JID		Jump InDirect	PL ← ROM (PU,A)
RET		RETurn from subroutine	SP + 2, PL ← [SP], PU ← [SP−1]
RETSK		RETurn and SKip	SP + 2, PL ← [SP],PU ← [SP−1]
RETI		RETurn from Interrupt	SP + 2, PL ← [SP],PU ← [SP−1],GIE ← 1
INTR		Generate an Interrupt	[SP] ← PL, [SP−1] ← PU, SP−2, PC ← 0FF
NOP		No OPeration	PC ← PC + 1

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Instruction Execution Time

Most instructions are single byte (with immediate addressing mode instructions taking two bytes).

Most single byte instructions take one cycle time to execute.

See the BYTES and CYCLES per INSTRUCTION table for details.

Bytes and Cycles per Instruction

The following table shows the number of bytes and cycles for each instruction in the format of byte/cycle.

	[B]	Direct	Immed.
ADD	1/1	3/4	2/2
ADC	1/1	3/4	2/2
SUBC	1/1	3/4	2/2
AND	1/1	3/4	2/2
OR	1/1	3/4	2/2
XOR	1/1	3/4	2/2
IFEQ	1/1	3/4	2/2
IFNE	1/1	3/4	2/2
IFGT	1/1	3/4	2/2
IFBNE	1/1		
DRSZ		1/3	
SBIT	1/1	3/4	
RBIT	1/1	3/4	
IFBIT	1/1	3/4	

RPND	1/1

Instructions Using A & C

CLRA	1/1
INCA	1/1
DECA	1/1
LAID	1/3
DCOR	1/1
RRCA	1/1
RLCA	1/1
SWAPA	1/1
SC	1/1
RC	1/1
IFC	1/1
IFNC	1/1
PUSHA	1/3
POPA	1/3
ANDSZ	2/2

Transfer of Control Instructions

JMPL	3/4
JMP	2/3
JP	1/3
JSRL	3/5
JSR	2/5
JID	1/3
VIS	1/5
RET	1/5
RETSK	1/5
RETI	1/5
INTR	1/7
NOP	1/1

Memory Transfer Instructions

	Register Indirect		Direct	Immed.	Register Indirect Auto Incr. & Decr.		
	[B]	[X]			[B+, B−]	[X+, X−]	
X A,*	1/1	1/3	2/3		1/2	1/3	
LD A,*	1/1	1/3	2/3	2/2	1/2	1/3	
LD B, Imm				1/1			(IF B < 16)
LD B, Imm				2/2			(IF B > 15)
LD Mem, Imm	2/2		3/3		2/2		
LD Reg, Imm			2/3				
IFEQ MD, Imm			3/3				

* = > Memory location addressed by B or X or directly.

COP888CS Opcode Table

Upper Nibble Along X-Axis

Lower Nibble Along Y-Axis

F	E	D	C	B	A	9	8	
JP −15	JP −31	LD 0F0, # i	DRSZ 0F0	RRCA	RC	ADC A,#i	ADC A,[B]	0
JP −14	JP −30	LD 0F1, # i	DRSZ 0F1	*	SC	SUBC A, #i	SUB A,[B]	1
JP −13	JP −29	LD 0F2, # i	DRSZ 0F2	X A, [X+]	X A,[B+]	IFEQ A,#i	IFEQ A,[B]	2
JP −12	JP −28	LD 0F3, # i	DRSZ 0F3	X A, [X−]	X A,[B−]	IFGT A,#i	IFGT A,[B]	3
JP −11	JP −27	LD 0F4, # i	DRSZ 0F4	VIS	LAID	ADD A,#i	ADD A,[B]	4
JP −10	JP −26	LD 0F5, # i	DRSZ 0F5	RPND	JID	AND A,#i	AND A,[B]	5
JP −9	JP −25	LD 0F6, # i	DRSZ 0F6	X A,[X]	X A,[B]	XOR A,#i	XOR A,[B]	6
JP −8	JP −24	LD 0F7, # i	DRSZ 0F7	*	*	OR A,#i	OR A,[B]	7
JP −7	JP −23	LD 0F8, # i	DRSZ 0F8	NOP	RLCA	LD A,#i	IFC	8
JP −6	JP −22	LD 0F9, # i	DRSZ 0F9	IFNE A,[B]	IFEQ Md,#i	IFNE A,#i	IFNC	9
JP −5	JP −21	LD 0FA, # i	DRSZ 0FA	LD A,[X+]	LD A,[B+]	LD [B+],#i	INCA	A
JP −4	JP −20	LD 0FB, # i	DRSZ 0FB	LD A,[X−]	LD A,[B−]	LD [B−],#i	DECA	B
JP −3	JP −19	LD 0FC, # i	DRSZ 0FC	LD Md,#i	JMPL	X A,Md	POPA	C
JP −2	JP −18	LD 0FD, # i	DRSZ 0FD	DIR	JSRL	LD A,Md	RETSK	D
JP −1	JP −17	LD 0FE, # i	DRSZ 0FE	LD A,[X]	LD A,[B]	LD [B],#i	RET	E
JP −0	JP −16	LD 0FF, # i	DRSZ 0FF	*	*	LD B,#i	RETI	F

COP888CS Opcode Table (Continued)

Upper Nibble Along X-Axis

Lower Nibble Along Y-Axis

7	6	5	4	3	2	1	0	
IFBIT 0,[B]	ANDSZ A, #i	LD B,#0F	IFBNE 0	JSR x000–x0FF	JMP x000–x0FF	JP +17	INTR	0
IFBIT 1,[B]	*	LD B,#0E	IFBNE 1	JSR x100–x1FF	JMP x100–x1FF	JP +18	JP + 2	1
IFBIT 2,[B]	*	LD B,#0D	IFBNE 2	JSR x200–x2FF	JMP x200–x2FF	JP +19	JP + 3	2
IFBIT 3,[B]	*	LD B,#0C	IFBNE 3	JSR x300–x3FF	JMP x300–x3FF	JP +20	JP + 4	3
IFBIT 4,[B]	CLRA	LD B,#0B	IFBNE 4	JSR x400–x4FF	JMP x400–x4FF	JP +21	JP + 5	4
IFBIT 5,[B]	SWAPA	LD B,#0A	IFBNE 5	JSR x500–x5FF	JMP x500–x5FF	JP +22	JP + 6	5
IFBIT 6,[B]	DCORA	LD B,#09	IFBNE 6	JSR x600–x6FF	JMP x600–x6FF	JP +23	JP + 7	6
IFBIT 7,[B]	PUSHA	LD B,#08	IFBNE 7	JSR x700–x7FF	JMP x700–x7FF	JP +24	JP + 8	7
SBIT 0,[B]	RBIT 0,[B]	LD B,#07	IFBNE 8	JSR x800–x8FF	JMP x800–x8FF	JP +25	JP + 9	8
SBIT 1,[B]	RBIT 1,[B]	LD B,#06	IFBNE 9	JSR x900–x9FF	JMP x900–x9FF	JP +26	JP + 10	9
SBIT 2,[B]	RBIT 2,[B]	LD B,#05	IFBNE 0A	JSR xA00–xAFF	JMP xA00–xAFF	JP +27	JP + 11	A
SBIT 3,[B]	RBIT 3,[B]	LD B,#04	IFBNE 0B	JSR xB00–xBFF	JMP xB00–xBFF	JP +28	JP + 12	B
SBIT 4,[B]	RBIT 4,[B]	LD B,#03	IFBNE 0C	JSR xC00–xCFF	JMP xC00–xCFF	JP +29	JP + 13	C
SBIT 5,[B]	RBIT 5,[B]	LD B,#02	IFBNE 0D	JSR xD00–xDFF	JMP xD00–xDFF	JP +30	JP + 14	D
SBIT 6,[B]	RBIT 6,[B]	LD B,#01	IFBNE 0E	JSR xE00–xEFF	JMP xE00–xEFF	JP +31	JP + 15	E
SBIT 7,[B]	RBIT 7,[B]	LD B,#00	IFBNE 0F	JSR xF00–xFFF	JMP xF00–xFFF	JP +32	JP + 16	F

Where,

i is the immediate data

Md is a directly addressed memory location

* is an unused opcode

Note: The opcode 60 Hex is also the opcode for IFBIT #i,A

Mask Options

The COP888CS mask programmable options are shown below. The options are programmed at the same time as the ROM pattern submission.

```
OPTION 1: CLOCK CONFIGURATION
  = 1     Crystal Oscillator (CKI/10)
              G7 (CKO) is clock generator
              output to crystal/resonator
              CKI is the clock input
  = 2     Single-pin RC controlled
              oscillator (CKI/10)
              G7 is available as a HALT
              restart and/or general purpose
              input

OPTION 2: HALT
  = 1     Enable HALT mode
  = 2     Disable HALT mode

OPTION 3: OPTIONS BONDING
  = 1     44-Pin PLCC
  = 2     40-Pin DIP
  = 3     NA
  = 4     28-Pin DIP
  = 5     28-Pin SO
```

Development Support

IN-CIRCUIT EMULATOR

The MetaLink iceMASTER™-COP8 Model 400 In-Circuit Emulator for the COP8 family of microcontrollers features high-performance operation, ease of use, and an extremely flexible user-interface for maximum productivity. Interchangeable probe cards, which connect to the standard common base, support the various configurations and packages of the COP8 family.

The iceMASTER provides real time, full speed emulation up to 10 MHz, 32 kBytes of emulation memory and 4k frames of trace buffer memory. The user may define as many as 32k trace and break triggers which can be enabled, disabled, set or cleared. They can be simple triggers based on code or address ranges or complex triggers based on code address, direct address, opcode value, opcode class or immediate operand. Complex breakpoints can be ANDed and ORed together. Trace information consists of address bus values, opcodes and user selectable probe clips status (external event lines). The trace buffer can be viewed as raw hex or as diassembled instructions. The probe clip bit values can be displayed in binary, hex or digital waveform formats.

During single-step operation the dynamically annotated code feature displays the contents of all accessed (read and write) memory locations and registers, as well as flow-of-control direction change markers next to each instruction executed.

The iceMASTER's performance analyzer offers a resolution of better than 6 μs. The user can easily monitor the time spent executing specific portions of code and find "hot spots" or "dead code". Up to 15 independent memory areas based on code address or label ranges can be defined. Analysis results can be viewed in bar graph format or as actual frequency count.

Emulator memory operations for program memory include single line assembler, disassembler, view, change and write to file. Data memory operations include fill, move, compare, dump to file, examine and modify. The contents of any memory space can be directly viewed and modified from the corresponding window.

The iceMASTER comes with an easy to use windowed interface. Each window can be sized, highlighted, color-controlled, added, or removed completely. Commands can be accessed via pull-down-menus and/or redefineable hot keys. A context sensitive hypertext/hyperlinked on-line help system explains clearly the options the user has from within any window.

The iceMASTER connects easily to a PC® via the standard COMM port and its 115.2 kBaud serial link keeps typical program download time to under 3 seconds.

The following tables list the emulator and probe cards ordering information.

Emulator Ordering Information

Part Number	Description
IM-COP8/400	MetaLink base unit in-circuit emulator for all COP8 devices, symbolic debugger software and RS-232 serial interface cable
MHW-PS3	Power Supply 110V/60 Hz
MHW-PS4	Power Supply 220V/50 Hz

Probe Card Ordering Information

Part Number	Package	Voltage Range	Emulates
MHW-884CG28D5PC	28 DIP	4.5V–5.5V	COP884CS
MHW-884CG28DWPC	28 DIP	2.5V–6.0V	COP884CS
MHW-888CG40D5PC	40 DIP	4.5V–5.5V	COP888CS
MHW-888CG40DWPC	40 DIP	2.5V–6.0V	COP888CS
MHW-888CG44D5PC	44 PLCC	4.5V–5.5V	COP888CS
MHW-888CG44DWPC	44 PLCC	2.5V–6.0V	COP888CS

Development Support (Continued)

MACRO CROSS ASSEMBLER

National Semiconductor offers a COP8 macro cross assembler. It runs on industry standard compatible PCs and supports all of the full-symbolic debugging features of the MetaLink iceMASTER emulators.

SINGLE CHIP EMULATOR DEVICE

The COP8 family is fully supported by single chip form, fit and function emulators. For more detailed information refer to the emulation device specific data sheets and the form, fit, function emulator selection table below.

PROGRAMMING SUPPORT

Programming of the single chip emulator devices is supported by different sources. National Semiconductor offers a duplicator board which allows the transfer of program code from a standard programmed EPROM to the single chip emulator and vice versa. Data I/O supports COP8 emulator device programming with its uniSite 48 and System 2900 programmers. Further information on Data I/O programmers can be obtained from any Data I/O sales office or the following USA numbers:

Telephone: (206) 881-6444 FAX: (206) 882-1043

Assembler Ordering Information

Part Number	Description	Manual
MOLE-COP8-IBM	COP8 macro cross assembler for IBM® PC/XT®, PC-AT® or compatible	424410527-001

Single Chip Emulator Selection Table

Device Number	Clock Option	Package	Description	Emulates
COP888CSMHEL-X	X = 1 : Crystal X = 3 : R/C	44 LDCC	Multi-Chip Module (MCM), UV Erasable	COP888CS
COP888CSMHD-X	X = 1 : Crystal X = 3 : R/C	40 DIP	MCM, UV Erasable	COP888CS
COP884CSMHD-X	X = 1 : Crystal X = 3 : R/C	28 DIP	MCM, UV Erasable	COP884CS
COP884CSMHEA-X	X = 1 : Crystal X = 3 : R/C	28 LCC	MCM (Same Footprint as 28 SO), UV Erasable	COP884CS

Duplicator Board Ordering Information

Part Number	Description	Devices Supported
COP8-PRGM-28D	Duplicator Board for 28 DIP Multi-Chip Module (MCM) and for use with Scrambler Boards	COP884CSMHD
COP8-SCRM-DIP	MCM Scrambler Board for 40 DIP Socket	COP888CSMHD
COP8-SCRM-PCC	MCM Scrambler Board for 44 PLCC/LDCC	COP888CSMHEL
COP8-SCRM-SBX	MCM Scrambler Board for 28 LCC Socket	COP884CSMHEA
COP8-PRGM-DIP	Duplicator Board with COP8-SCRM-DIP Scrambler Board	COP884CSMHD, COP888CSMHD
COP8-PRGM-PCC	Duplicator Board with COP8-SCRM-PCC Scrambler Board	COP888CSMEL, COP884CSMHD

Development Support (Continued)

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications group. The Dial-A-Helper is an Electronic Bulletin Board Information system.

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down loaded to disk for later use.

ORDER P/N: MOLE-DIAL-A-HLP

Information System Package contains:
- Dial-A-Helper Users Manual
- Public Domain Communications Software

FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factor applications support. If a user has questions, he can leave messages on our electronic bulletin board, which we will respond to.

Voice:	(408) 721-5582	
Modem:	(408) 739-1162	
	Baud:	300 or 1200 Baud
	Set-up:	Length: 8-Bit
		Parity: None
		Stop Bit: 1
	Operation:	24 Hrs., 7 Days

National Semiconductor

COP688EG/COP684EG/COP888EG/COP884EG/ COP988EG/COP984EG Single-Chip microCMOS Microcontrollers

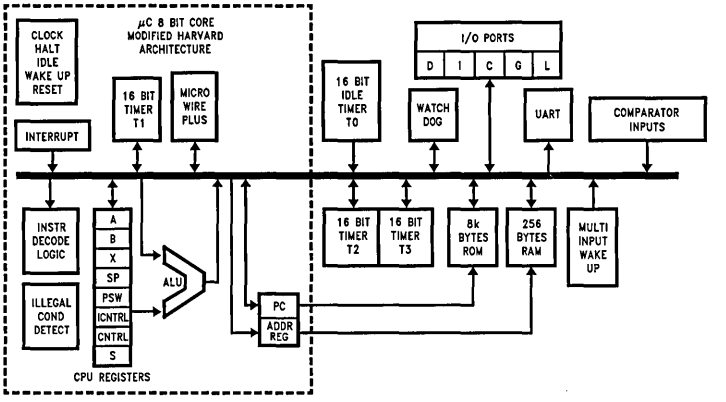
General Description

The COP888 family of microcontrollers uses an 8-bit single chip core architecture fabricated with National Semiconductor's M²CMOS™ process technology. The COP888EG/ COP884EG is a member of this expandable 8-bit core processor family of microcontrollers. (Continued)

Features

- Low cost 8-bit microcontroller
- Fully static CMOS, with low current drain
- Two power saving modes: HALT and IDLE
- 1 μs instruction cycle time
- 8k bytes on-board ROM
- 256 bytes on-board RAM
- Single supply operation: 2.5V–6V
- Full duplex UART
- Two analog comparators
- MICROWIRE/PLUS™ serial I/O
- WATCHDOG™ and Clock Monitor logic
- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- Three 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers (B and X)
- Fourteen multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Three Timers (Each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — UART (2)
  - — Default VIS
- Versatile instruction set
- True bit manipulation
- Memory mapped I/O
- BCD arithmetic instructions
- Package: 44 PLCC or 40 N or 28 N or 28 SO
  - — 44 PLCC with 39 I/O pins
  - — 40 N with 35 I/O pins
  - — 28 SO or 28 N, each with 23 I/O pins
- Software selectable I/O options
  - — TRI-STATE® Output
  - — Push-Pull Output
  - — Weak Pull Up Input
  - — High Impedance Input
- Schmitt trigger inputs on ports G and L
- Temperature ranges: 0°C to +70°C,
  −40°C to +85°C
  −55°C to +125°C
- Form factor emulation devices
- Real time emulation and full program debug offered by National's Development Systems

Block Diagram



TL/DD/11214–1

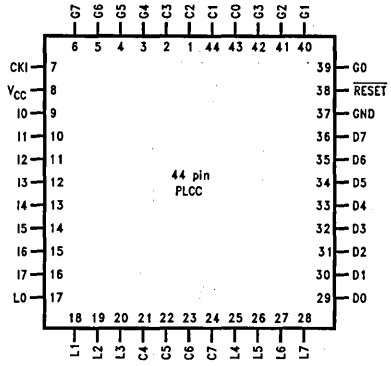
FIGURE 1. COP888EG Block Diagram

General Description (Continued)

They are fully static parts, fabricated using double-metal silicon gate microCMOS technology. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS serial I/O, three 16-bit timer/counters supporting three modes (Processor Independent PWM generation, External Event counter, and Input Capture mode capabilities), full duplex UART, two comparators, and two power savings modes (HALT and IDLE), both with a multi-sourced wakeup/interrupt capability. This multi-sourced interrupt capability may also be used independent of the HALT or IDLE modes. Each I/O pin has software selectable configurations. The devices operate over a voltage range of 2.5V to 6V. High throughput is achieved with an efficient, regular instruction set operating at a maximum of 1 μs per instruction rate.

Connection Diagrams

Plastic Chip Carrier

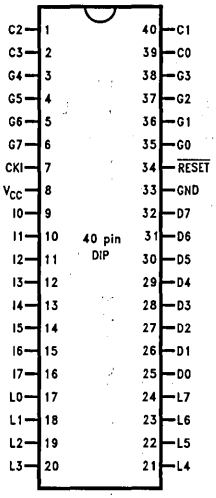


TL/DD/11214–2

Top View

Order Number COP888EG-XXX/V
See NS Plastic Chip Package Number V44A

Dual-In-Line Package

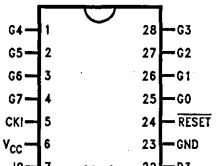


TL/DD/11214–3

Top View

Order Number COP888EG-XXX/N
See NS Molded Package Number N40A

Dual-In-Line Package



TL/DD/11214–4

Top View

Order Number COP884EG-XXX/WM or COP884EG-XXX/N
See NS Molded Package Number M28B or N28A

FIGURE 2a. COP888EG Connection Diagrams

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Connection Diagrams (Continued)

COP888EG Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU	CKX	12	18	18
L2	I/O	MIWU	TDX	13	19	19
L3	I/O	MIWU	RDX	14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU	T3A	17	23	27
L7	I/O	MIWU	T3B	18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
I0	I			7	9	9
I1	I	COMP1IN−		8	10	10
I2	I	COMP1IN+		9	11	11
I3	I	COMP1OUT		10	12	12
I4	I	COMP2IN−			13	13
I5	I	COMP2IN+			14	14
I6	I	COMP2OUT			15	15
I7	I				16	16
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics 98XEG: 0°C ≤ T_A ≤ +70°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage COP98XCS		2.5		4.0	V
COP98XCSH		4.0		6.0	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			5.5	mA
CKI = 4 MHz	V_{CC} = 4V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			1.4	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<0.7	8	μA
	V_{CC} = 4V, CKI = 0 MHz		<0.3	4	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4V, t_c = 10 μs			0.7	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6V, V_{IN} = 0V	−1		+1	μA
Input Pullup Current	V_{CC} = 6V, V_{IN} = 0V	40		250	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4V, V_{OL} = 1V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2.0			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4V, V_{OH} = 2.7V	10		100	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink (Push-Pull Mode)	V_{CC} = 4V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			mA
TRI-STATE Leakage	V_{CC} = 6.0V	−1		+1	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor and the comparators are disabled.

DC Electrical Characteristics 98XEG: 0°C ≤ T_A ≤ +70°C unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				15	mA
All others				3	mA
Maximum Input Current without Latchup (Note 6)	T_A = 25°C			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

AC Electrical Characteristics 98XEG: 0°C ≤ T_A ≤ +70°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)	4V ≤ V_{CC} ≤ 6V	1		DC	μs
Crystal, Resonator,	2.5V ≤ V_{CC} < 4V	2.5		DC	μs
R/C Oscillator	4V ≤ V_{CC} ≤ 6V	3		DC	μs
	2.5V ≤ V_{CC} < 4V	7.5		DC	μs
CKI Clock Duty Cycle (Note 5)	f_r = Max	40		60	%
Rise Time (Note 5)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 5)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	4V ≤ V_{CC} ≤ 6V	200			ns
	2.5V ≤ V_{CC} < 4V	500			ns
t_{HOLD}	4V ≤ V_{CC} ≤ 6V	60			ns
	2.5V ≤ V_{CC} < 4V	150			ns
Output Propagation Delay	R_L = 2.2k, C_L = 100 pF				
t_{PD1}, t_{PD0}					
SO, SK	4V ≤ V_{CC} ≤ 6V			0.7	μs
	2.5V ≤ V_{CC} < 4V			1.75	μs
All Others	4V ≤ V_{CC} ≤ 6V			1	μs
	2.5V ≤ V_{CC} < 4V			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 5: Parameter sampled but not 100% tested.

Note 6: Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than V_{CC} and the pins will have sink current to V_{CC} when biased at voltages greater than V_{CC} (the pins do not have source current when biased at a voltage below V_{CC}). The effective resistance to V_{CC} is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

888EG: $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		2.5		6	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			5.5	mA
CKI = 4 MHz	V_{CC} = 4.0V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4.0V, t_c = 10 μs			1.4	mA
HALT Current (Note 3)	V_{CC} = 6V, CKI = 0 MHz		<1	10	μA
	V_{CC} = 4.0V, CKI = 0 MHz		<0.5	6	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 6V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 6V, t_c = 2.5 μs			2.5	mA
CKI = 1 MHz	V_{CC} = 4.0V, t_c = 10 μs			0.7	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 6V	−2		+2	μA
Input Pullup Current	V_{CC} = 6V	40		250	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink	V_{CC} = 4V, V_{OL} = 1V	10			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	2.0			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4V, V_{OH} = 2.7V	10		100	μA
	V_{CC} = 2.5V, V_{OH} = 1.8V	2.5		33	μA
Source (Push-Pull Mode)	V_{CC} = 4V, V_{OH} = 3.3V	0.4			mA
	V_{CC} = 2.5V, V_{OH} = 1.8V	0.2			mA
Sink (Push-Pull Mode)	V_{CC} = 4V, V_{OL} = 0.4V	1.6			mA
	V_{CC} = 2.5V, V_{OL} = 0.4V	0.7			mA
TRI-STATE Leakage	V_{CC} = 6.0V	−2		+2	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a crystal/resonator oscillator, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L, C, and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor and the comparators are disabled.

DC Electrical Characteristics 888EG: $-40°C \le T_A \le +85°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				15	mA
All others				3	mA
Maximum Input Current without Latchup	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

AC Electrical Characteristics 888EG: $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal, Resonator,	$4V \le V_{CC} \le 6V$	1		DC	μs
R/C Oscillator	$2.5V \le V_{CC} < 4V$	2.5		DC	μs
	$4V \le V_{CC} \le 6V$	3		DC	μs
	$2.5V \le V_{CC} < 4V$	7.5		DC	μs
CKI Clock Duty Cycle (Note 4)	f_r = Max	40		60	%
Rise Time (Note 4)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 4)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	$4V \le V_{CC} \le 6V$	200			ns
	$2.5V \le V_{CC} < 4V$	500			ns
t_{HOLD}	$4V \le V_{CC} \le 6V$	60			ns
	$2.5V \le V_{CC} < 4V$	150			ns
Output Propagation Delay	$R_L = 2.2k, C_L = 100$ pF				
t_{PD1}, t_{PD0}					
SO, SK	$4V \le V_{CC} \le 6V$			0.7	μs
	$2.5V \le V_{CC} < 4V$			1.75	μs
All Others	$4V \le V_{CC} \le 6V$			1	μs
	$2.5V \le V_{CC} < 4V$			2.5	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 4: Parameter sampled but not 100% tested.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics 688EG: −55°C ≤ T_A ≤ +125°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		4.5		6	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2)					
CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			12.5	mA
CKI = 4 MHz	V_{CC} = 5.5V, t_c = 2.5 μs			5.5	mA
HALT Current (Note 3)	V_{CC} = 5.5V, CKI = 0 MHz		<10	30	μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			3.5	mA
CKI = 4 MHz	V_{CC} = 5.5V, t_c = 2.5 μs			2.5	mA
Input Levels					
$\overline{\text{RESET}}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 5.5V	−5		+5	μA
Input Pullup Current	V_{CC} = 5.5V	35		400	μA
G and L Port Input Hysteresis				0.35 V_{CC}	V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.3V	0.4			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1V	9			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4.5V, V_{OH} = 2.7V	9		140	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.3V	0.4			mA
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.4			mA
TRI-STATE Leakage	V_{CC} = 5.5V	−5		+5	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a crystal/resonator oscillator, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L, C, and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor and the comparators are disabled.

DC Electrical Characteristics 688EG: $-55°C \le T_A \le +125°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				12	mA
All others				2.5	mA
Maximum Input Current without Latchup	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

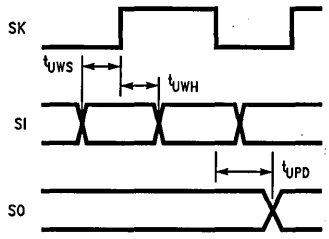
AC Electrical Characteristics 688EG: $-55°C \le T_A \le +125°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal, Resonator,	$V_{CC} \ge 4.5V$	1		DC	μs
R/C Oscillator	$V_{CC} \ge 4.5V$	3		DC	μs
CKI Clock Duty Cycle (Note 4)	f_r = Max	45		55	%
Rise Time (Note 5)	f_r = 10 MHz Ext Clock			12	ns
Fall Time (Note 5)	f_r = 10 MHz Ext Clock			8	ns
Inputs					
t_{SETUP}	$V_{CC} \ge 4.5V$	200			ns
t_{HOLD}	$V_{CC} \ge 4.5V$	60			ns
Output Propagation Delay	R_L = 2.2k, C_L = 100 pF				
t_{PD1}, t_{PD0}					
SO, SK	$V_{CC} \ge 4.5V$			0.7	μs
All Others	$V_{CC} \ge 4.5V$			1	μs
MICROWIRE Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 4: Parameter sampled but not 100% tested.

Comparators AC and DC Characteristics $V_{CC} = 5V, T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$0.4V \le V_{IN} \le V_{CC} - 1.5V$		±10	±25	mV
Input Common Mode Voltage Range		0.4		$V_{CC} - 1.5$	V
Low Level Output Current	$V_{OL} = 0.4V$	1.6			mA
High Level Output Current	$V_{OH} = 4.6V$	1.6			mA
DC Supply Current Per Comparator (When Enabled)				250	μA
Response Time	TBD mV Step, TBD mV Overdrive, 100 pF Load		1		μs

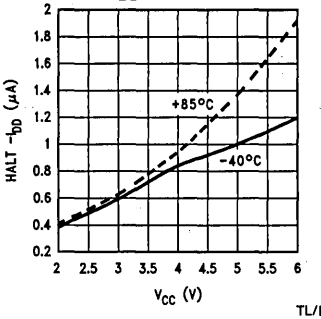


TL/DD/11214–5

FIGURE 2. MICROWIRE/PLUS Timing

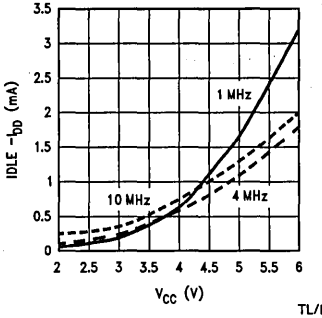
Typical Performance Characteristics ($-40°C \le T_A \le +85°C$)

Halt—I_{DD}



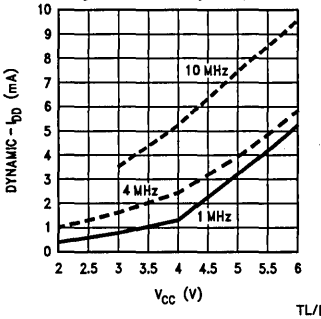
TL/DD/11214-7

Idle—I_{DD} (Crystal Clock Option)



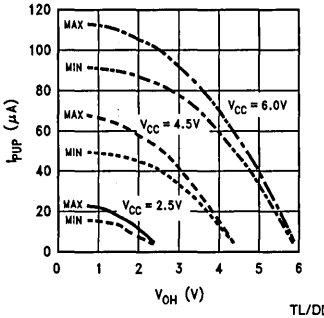
TL/DD/11214-8

Dynamic—I_{DD} vs V_{CC} (Crystal Clock Option)



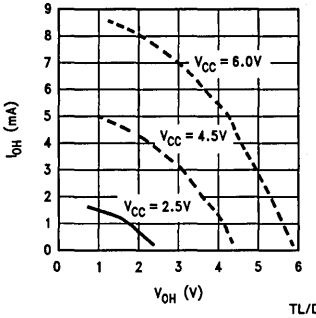
TL/DD/11214-9

Port L/C/G Weak Pull-Up Source Current



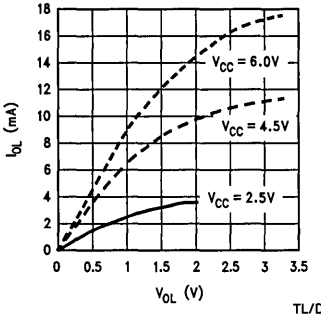
TL/DD/11214-10

Port L/C/G Push-Pull Source Current



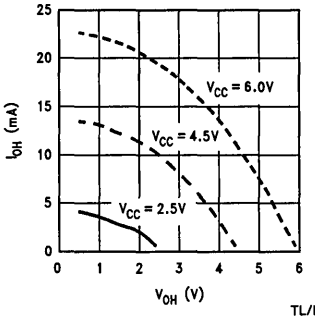
TL/DD/11214-11

Port L/C/G Push-Pull Sink Current



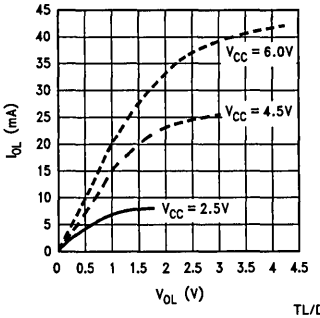
TL/DD/11214-12

Port D Source Current



TL/DD/11214-13

Port D Sink Current



TL/DD/11214-14

Pin Descriptions

V_{CC} and GND are the power supply pins.

CKI is the clock input. This can come from an R/C generated oscillator, or a crystal oscillator (in conjunction with CKO). See Oscillator Description section.

$\overline{\text{RESET}}$ is the master reset input. See Reset Description section.

The device contains three bidirectional 8-bit I/O ports (C, G and L), where each individual bit may be independently configured as an input (Schmitt trigger inputs on ports L and G), output or TRI-STATE under program control. Three data memory address locations are allocated for each of these I/O ports. Each I/O port has two associated 8-bit memory mapped registers, the CONFIGURATION register and the output DATA register. A memory mapped address is also reserved for the input pins of each I/O port. (See the memory map for the various addresses associated with the I/O ports.) *Figure 3* shows the I/O port configurations. The DATA and CONFIGURATION registers allow for each port bit to be individually configured under software control as shown below:

CONFIGURATION Register	DATA Register	Port Set-Up
0	0	Hi-Z Input (TRI-STATE Output)
0	1	Input with Weak Pull-Up
1	0	Push-Pull Zero Output
1	1	Push-Pull One Output

PORT L is an 8-bit I/O port. All L-pins have Schmitt triggers on the inputs.

The Port L supports Multi-Input Wake Up on all eight pins. L1 is used for the UART external clock. L2 and L3 are used for the UART transmit and receive. L4 and L5 are used for the timer input functions T2A and T2B. L6 and L7 are used for the timer input functions T3A and T3B.

The Port L has the following alternate features:

- L0 MIWU
- L1 MIWU or CKX
- L2 MIWU or TDX
- L3 MIWU or RDX
- L4 MIWU or T2A
- L5 MIWU or T2B
- L6 MIWU or T3A
- L7 MIWU or T3B

Port G is an 8-bit port with 5 I/O pins (G0, G2–G5), an input pin (G6), and two dedicated output pins (G1 and G7). Pins G0 and G2–G6 all have Schmitt Triggers on their inputs. Pin G1 serves as the dedicated WDOUT WATCHDOG output, while pin G7 is either input or output depending on the oscillator mask option selected. With the crystal oscillator option selected, G7 serves as the dedicated output pin for the CKO clock output. With the single-pin R/C oscillator mask option selected, G7 serves as a general purpose input pin but is also used to bring the device out of HALT mode with a low to high transition on G7. There are two registers associated with the G Port, a data register and a configuration register. Therefore, each of the 5 I/O bits (G0, G2–G5) can be individually configured under software control.

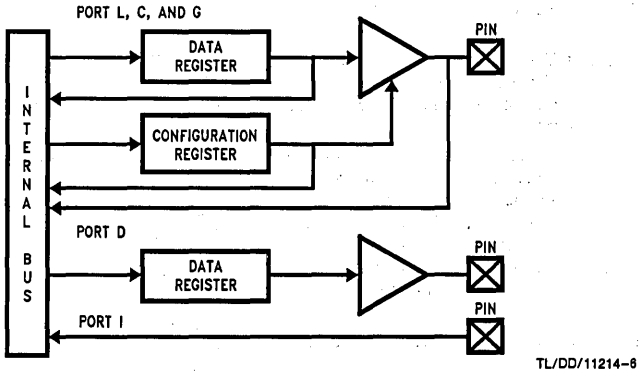


FIGURE 3. I/O Port Configurations

Pin Descriptions (Continued)

Since G6 is an input only pin and G7 is the dedicated CKO clock output pin (crystal clock option) or general purpose input (R/C clock option), the associated bits in the data and configuration registers for G6 and G7 are used for special purpose functions as outlined below. Reading the G6 and G7 data bits will return zeros.

Note that the chip will be placed in the HALT mode by writing a "1" to bit 7 of the Port G Data Register. Similarly the chip will be placed in the IDLE mode by writing a "1" to bit 6 of the Port G Data Register.

Writing a "1" to bit 6 of the Port G Configuration Register enables the MICROWIRE/PLUS to operate with the alternate phase of the SK clock. The G7 configuration bit, if set high, enables the clock start up delay after HALT when the R/C clock configuration is used.

	Config Reg.	Data Reg.
G7	CLKDLY	HALT
G6	Alternate SK	IDLE

Port G has the following alternate features:

- G0 INTR (External Interrupt Input)
- G2 T1B (Timer T1 Capture Input)
- G3 T1A (Timer T1 I/O)
- G4 SO (MICROWIRE™ Serial Data Output)
- G5 SK (MICROWIRE Serial Clock)
- G6 SI (MICROWIRE Serial Data Input)

Port G has the following dedicated functions:

- G1 WDOUT WATCHDOG and/or Clock Monitor dedicated output
- G7 CKO Oscillator dedicated output or general purpose input

Port C is an 8-bit I/O port. The 40-pin device does not have a full complement of Port C pins. The unavailable pins are not terminated. A read operation for these unterminated pins will return unpredicatable values.

PORT I is an eight-bit Hi-Z input port. The 28-pin device does not have a full complement of Port I pins. The unavailable pins are not terminated i.e., they are floating. A read operation for these unterminated pins will return unpredictable values. The user must ensure that the software takes this into account by either masking or restricting the accesses to bit operations. The unterminated Port I pins will draw power only when addressed.

Port I1–I3 are used for Comparator 1. Port I4–I6 are used for Comparator 2.

The Port I has the following alternate features.

- I1 COMP1−IN (Comparator 1 Negative Input)
- I2 COMP1+IN (Comparator 1 Positive Input)
- I3 COMP1OUT (Comparator 1 Output)
- I4 COMP2−IN (Comparator 2 Negative Input)
- I5 COMP2+IN (Comparator 2 Positive Input)
- I6 COMP2OUT (Comparator 2 Output)

Port D is an 8-bit output port that is preset high when $\overline{\text{RESET}}$ goes low. The user can tie two or more D port outputs together in order to get a higher drive.

Functional Description

The architecture of the device is modified Harvard architecture. With the Harvard architecture, the control store program memory (ROM) is separated from the data store memory (RAM). Both ROM and RAM have their own separate addressing space with separate address buses. The architecture, though based on Harvard architecture, permits transfer of data from ROM to RAM.

CPU REGISTERS

The CPU can do an 8-bit addition, subtraction, logical or shift operation in one instruction (t_C) cycle time.

There are six CPU registers:

A is the 8-bit Accumulator Register

PC is the 15-bit Program Counter Register

PU is the upper 7 bits of the program counter (PC)
PL is the lower 8 bits of the program counter (PC)

B is an 8-bit RAM address pointer, which can be optionally post auto incremented or decremented.

X is an 8-bit alternate RAM address pointer, which can be optionally post auto incremented or decremented.

SP is the 8-bit stack pointer, which points to the subroutine/interrupt stack (in RAM). The SP is initialized to RAM address 06F with reset.

S is the 8-bit Data Segment Address Register used to extend the lower half of the address range (00 to 7F) into 256 data segments of 128 bytes each.

All the CPU registers are memory mapped with the exception of the Accumulator (A) and the Program Counter (PC).

PROGRAM MEMORY

The program memory consists of 8092 bytes of ROM. These bytes may hold program instructions or constant data (data tables for the LAID instruction, jump vectors for the JID instruction, and interrupt vectors for the VIS instruction). The program memory is addressed by the 15-bit program counter (PC). All interrupts in the devices vector to program memory location 0FF Hex.

DATA MEMORY

The data memory address space includes the on-chip RAM and data registers, the I/O registers (Configuration, Data and Pin), the control registers, the MICROWIRE/PLUS SIO shift register, and the various registers, and counters associated with the timers (with the exception of the IDLE timer). Data memory is addressed directly by the instruction or indirectly by the B, X, SP pointers and S register.

The data memory consists of 256 bytes of RAM. Sixteen bytes of RAM are mapped as "registers" at addresses 0F0 to 0FF Hex. These registers can be loaded immediately, and also decremented and tested with the DRSZ (decrement register and skip if zero) instruction. The memory pointer registers X, SP, B and S are memory mapped into this space at address locations 0FC to 0FF Hex respectively, with the other registers being available for general usage.

The instruction set permits any bit in memory to be set, reset or tested. All I/O and registers (except A and PC) are memory mapped; therefore, I/O bits and register bits can be directly and individually set, reset and tested. The accumulator (A) bits can also be directly and individually tested.

Data Memory Segment RAM Extension

Data memory address 0FF is used as a memory mapped location for the Data Segment Address Register (S).

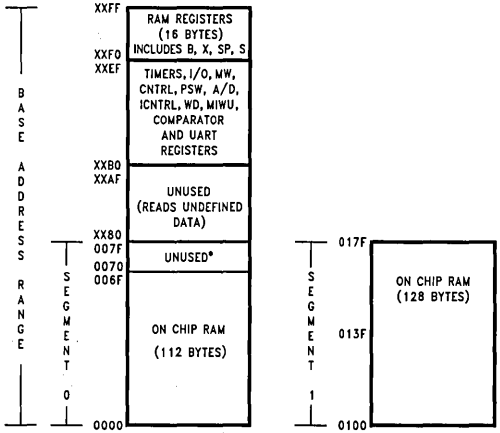
The data store memory is either addressed directly by a single byte address within the instruction, or indirectly relative to the reference of the B, X, or SP pointers (each contains a single-byte address). This single-byte address allows an addressing range of 256 locations from 00 to FF hex. The upper bit of this single-byte address divides the data store memory into two separate sections as outlined previously. With the exception of the RAM register memory from address locations 00F0 to 00FF, all RAM memory is memory mapped with the upper bit of the single-byte address being equal to zero. This allows the upper bit of the single-byte address to determine whether or not the base address range (from 0000 to 00FF) is extended. If this upper bit equals one (representing address range 0080 to 00FF), then address extension does not take place. Alternatively, if this upper bit equals zero, then the data segment extension register S is used to extend the base address range (from 0000 to 007F) from XX00 to XX7F, where XX represents the 8 bits from the S register. Thus the 128-byte data segment extensions are located from addresses 0100 to 017F for data segment 1, 0200 to 027F for data segment 2, etc., up to FF00 to FF7F for data segment 255. The base address range from 0000 to 007F represents data segment 0.

Figure 4 illustrates how the S register data memory extension is used in extending the lower half of the base address range (00 to 7F hex) into 256 data segments of 128 bytes each, with a total addressing range of 32 kbytes from XX00 to XX7F. This organization allows a total of 256 data segments of 128 bytes each with an additional upper base segment of 128 bytes. Furthermore, all addressing modes are available for all data segments. The S register must be changed under program control to move from one data segment (128 bytes) to another. However, the upper base segment (containing the 16 memory registers, I/O registers, control registers, etc.) is always available regardless of the contents of the S register, since the upper base segment (address range 0080 to 00FF) is independent of data segment extension.

The instructions that utilize the stack pointer (SP) always reference the stack as part of the base segment (Segment 0), regardless of the contents of the S register. The S register is not changed by these instructions. Consequently, the stack (used with subroutine linkage and interrupts) is always located in the base segment. The stack pointer will be initialized to point at data memory location 006F as a result of reset.

The 128 bytes of RAM contained in the base segment are split between the lower and upper base segments. The first 116 bytes of RAM are resident from address 0000 to 006F in the lower base segment, while the remaining 16 bytes of RAM represent the 16 data memory registers located at addresses 00F0 to 00FF of the upper base segment. No RAM is located at the upper sixteen addresses (0070 to 007F) of the lower base segment.

Additional RAM beyond these initial 128 bytes, however, will always be memory mapped in groups of 128 bytes (or less) at the data segment address extensions (XX00 to XX7F) of the lower base segment. The additional 128 bytes of RAM are memory mapped at address locations 0100 to 017F hex.



*Reads as all ones.

FIGURE 4. RAM Organization

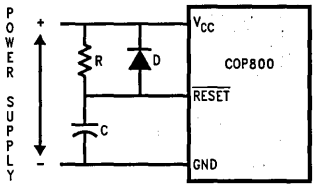
Reset

The $\overline{\text{RESET}}$ input when pulled low initializes the microcontroller. Initialization will occur whenever the $\overline{\text{RESET}}$ input is pulled low. Upon initialization, the data and configuration registers for ports L, G and C are cleared, resulting in these Ports being initialized to the TRI-STATE mode. Pin G1 of the G Port is an exception (as noted below) since pin G1 is dedicated as the WATCHDOG and/or Clock Monitor error output pin. Port D is set high. The PC, PSW, ICNTRL, CNTRL, T2CNTRL and T3CNTRL control registers are cleared. The UART registers PSR, ENU (except that TBMT bit is set), ENUR and ENUI are cleared. The Comparator Select Register is cleared. The S register is initialized to zero. The Multi-Input Wakeup registers WKEN, WKEDG and WKPND are cleared. The stack pointer, SP, is initialized to 6F Hex.

The device comes out of reset with both the WATCHDOG logic and the Clock Monitor detector armed, with the WATCHDOG service window bits set and the Clock Monitor bit set. The WATCHDOG and Clock Monitor circuits are inhibited during reset. The WATCHDOG service window bits being initialized high default to the maximum WATCHDOG service window of 64k t_C clock cycles. The Clock Monitor bit being initialized high will cause a Clock Monitor error following reset if the clock has not reached the minimum specified frequency at the termination of reset. A Clock Monitor error will cause an active low error output on pin G1. This error output will continue until 16 t_C–32 t_C clock cycles following the clock frequency reaching the minimum specified value, at which time the G1 output will enter the TRI-STATE mode.

The external RC network shown in *Figure 5* should be used to ensure that the $\overline{\text{RESET}}$ pin is held low until the power supply to the chip stabilizes.

Reset (Continued)



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RC > 5 × Power Supply Rise Time

FIGURE 5. Recommended Reset Circuit

Oscillator Circuits

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (crystal configuration). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_c$).

Figure 6 shows the Crystal and R/C diagrams.

CRYSTAL OSCILLATOR

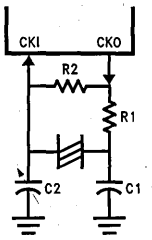
CKI and CKO can be connected to make a closed loop crystal (or resonator) controlled oscillator.

Table A shows the component values required for various standard crystal values.

R/C OSCILLATOR

By selecting CKI as a single pin oscillator input, a single pin R/C oscillator circuit can be connected to it. CKO is available as a general purpose input, and/or HALT restart input.

Table B shows the variation in the oscillator frequencies as functions of the component (R and C) values.



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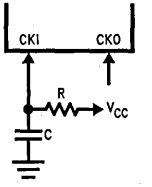

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FIGURE 6. Crystal and R/C Oscillator Diagrams

TABLE A. Crystal Oscillator Configuration, T_A = 25°C

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)	Conditions
0	1	30	30-36	10	V_{CC} = 5V
0	1	30	30-36	4	V_{CC} = 5V
0	1	200	100-150	0.455	V_{CC} = 5V

TABLE B. RC Oscillator Configuration, T_A = 25°C

R (kΩ)	C (pF)	CKI Freq (MHz)	Instr. Cycle (μs)	Conditions
3.3	82	2.2 to 2.7	3.7 to 4.6	V_{CC} = 5V
5.6	100	1.1 to 1.3	7.4 to 9.0	V_{CC} = 5V
6.8	100	0.9 to 1.1	8.8 to 10.8	V_{CC} = 5V

Note: 3k ≤ R ≤ 200k

50 pF ≤ C ≤ 200 pF

Current Drain

The total current drain of the chip depends on:

1. Oscillator operation mode—I1
2. Internal switching current—I2
3. Internal leakage current—I3
4. Output source current—I4
5. DC current caused by external input not at V_{CC} or GND—I5
6. Comparator DC supply current when enabled—I6
7. Clock Monitor current when enabled—I7

Thus the total current drain, It, is given as

$$It = I1 + I2 + I3 + I4 + I5 + I6 + I7$$

To reduce the total current drain, each of the above components must be minimum.

The chip will draw more current as the CKI input frequency increases up to the maximum 10 MHz value. Operating with a crystal network will draw more current than an external square-wave. Switching current, governed by the equation below, can be reduced by lowering voltage and frequency. Leakage current can be reduced by lowering voltage and temperature. The other two items can be reduced by carefully designing the end-user's system.

$$I2 = C \times V \times f$$

where C = equivalent capacitance of the chip
V = operating voltage
f = CKI frequency

Control Registers

CNTRL Register (Address X'00EE)

The Timer1 (T1) and MICROWIRE/PLUS control register contains the following bits:

SL1 & SL0	Select the MICROWIRE/PLUS clock divide by (00 = 2, 01 = 4, 1x = 8)
IEDG	External interrupt edge polarity select (0 = Rising edge, 1 = Falling edge)
MSEL	Selects G5 and G4 as MICROWIRE/PLUS signals SK and SO respectively
T1C0	Timer T1 Start/Stop control in timer modes 1 and 2 Timer T1 Underflow Interrupt Pending Flag in timer mode 3
T1C1	Timer T1 mode control bit
T1C2	Timer T1 mode control bit
T1C3	Timer T1 mode control bit

T1C3	T1C2	T1C1	T1C0	MSEL	IEDG	SL1	SL0

Bit 7 Bit 0

Control Registers (Continued)

PSW Register (Address X'00EF)

The PSW register contains the following select bits:

- GIE Global interrupt enable (enables interrupts)
- EXEN Enable external interrupt
- BUSY MICROWIRE/PLUS busy shifting flag
- EXPND External interrupt pending
- T1ENA Timer T1 Interrupt Enable for Timer Underflow or T1A Input capture edge
- T1PNDA Timer T1 Interrupt Pending Flag (Autoreload RA in mode 1, T1 Underflow in Mode 2, T1A capture edge in mode 3)
- C Carry Flag
- HC Half Carry Flag

HC	C	T1PNDA	T1ENA	EXPND	BUSY	EXEN	GIE

Bit 7 Bit 0

The Half-Carry bit is also affected by all the instructions that affect the Carry flag. The SC (Set Carry) and RC (Reset Carry) instructions will respectively set or clear both the carry flags. In addition to the SC and RC instructions, ADC, SUBC, RRC and RLC instructions affect the carry and Half Carry flags.

ICNTRL Register (Address X'00E8)

The ICNTRL register contains the following bits:

- T1ENB Timer T1 Interrupt Enable for T1B Input capture edge
- T1PNDB Timer T1 Interrupt Pending Flag for T1B capture edge
- μWEN Enable MICROWIRE/PLUS interrupt
- μWPND MICROWIRE/PLUS interrupt pending
- T0EN Timer T0 Interrupt Enable (Bit 12 toggle)
- T0PND Timer T0 Interrupt pending
- LPEN L Port Interrupt Enable (Multi-Input Wakeup/Interrupt)

  Bit 7 could be used as a flag

Unused	LPEN	T0PND	T0EN	μWPND	μWEN	T1PNDB	T1ENB

Bit 7 Bit 0

T2CNTRL Register (Address X'00C6)

The T2CNTRL register contains the following bits:

- T2ENB Timer T2 Interrupt Enable for T2B Input capture edge
- T2PNDB Timer T2 Interrupt Pending Flag for T2B capture edge
- T2ENA Timer T2 Interrupt Enable for Timer Underflow or T2A Input capture edge
- T2PNDA Timer T2 Interrupt Pending Flag (Autoreload RA in mode 1, T2 Underflow in mode 2, T2A capture edge in mode 3)
- T2C0 Timer T2 Start/Stop control in timer modes 1 and 2 Timer T2 Underflow Interrupt Pending Flag in timer mode 3
- T2C1 Timer T2 mode control bit
- T2C2 Timer T2 mode control bit
- T2C3 Timer T2 mode control bit

T2C3	T2C2	T2C1	T2C0	T2PNDA	T2ENA	T2PNDB	T2ENB

Bit 7 Bit 0

T3CNTRL Register (Address X'00B6)

The T3CNTRL register contains the following bits:

- T3ENB Timer T3 Interrupt Enable for T3B
- T3PNDB Timer T3 Interrupt Pending Flag for T3B pin (T3B capture edge)
- T3ENA Timer T3 Interrupt Enable for Timer Underflow or T3A pin
- T3PNDA Timer T3 Interrupt Pending Flag (Autoload RA in mode 1, T3 Underflow in mode 2, T3a capture edge in mode 3)
- T3C0 Timer T3 Start/Stop control in timer modes 1 and 2

  Timer T3 Underflow Interrupt Pending Flag in timer mode 3
- T3C1 Timer T3 mode control bit
- T3C2 Timer T3 mode control bit
- T3C3 Timer T3 mode control bit

T3C3	T3C2	T3C1	T3C0	T3PNDA	T3ENA	T3PNDB	T3ENB

Bit 7 Bit 0

Timers

The device contains a very versatile set of timers (T0, T1, T2, T3). All timers and associated autoreload/capture registers power up containing random data.

TIMER T0 (IDLE TIMER)

The devices support applications that require maintaining real time and low power with the IDLE mode. This IDLE mode support is furnished by the IDLE timer T0, which is a 16-bit timer. The Timer T0 runs continuously at the fixed rate of the instruction cycle clock, t_c. The user cannot read or write to the IDLE Timer T0, which is a count down timer.

The Timer T0 supports the following functions:

Exit out of the Idle Mode (See Idle Mode description)
WATCHDOG logic (See WATCHDOG description)
Start up delay out of the HALT mode

The IDLE Timer T0 can generate an interrupt when the thirteenth bit toggles. This toggle is latched into the T0PND pending flag, and will occur every 4 ms at the maximum clock frequency (t_c = 1 μs). A control flag T0EN allows the interrupt from the thirteenth bit of Timer T0 to be enabled or disabled. Setting T0EN will enable the interrupt, while resetting it will disable the interrupt.

Timers (Continued)

TIMER T1, TIMER T2 AND TIMER T3

The devices have a set of three powerful timer/counter blocks, T1, T2 and T3. The associated features and functioning of a timer block are described by referring to the timer block Tx. Since the three timer blocks, T1, T2 and T3 are identical, all comments are equally applicable to any of the three timer blocks.

Each timer block consists of a 16-bit timer, Tx, and two supporting 16-bit autoreload/capture registers, RxA and RxB. Each timer block has two pins associated with it, TxA and TxB. The pin TxA supports I/O required by the timer block, while the pin TxB is an input to the timer block. The powerful and flexible timer block allows the device to easily perform all timer functions with minimal software overhead. The timer block has three operating modes: Processor Independent PWM mode, External Event Counter mode, and Input Capture mode.

The control bits TxC3, TxC2, and TxC1 allow selection of the different modes of operation.

Mode 1. Processor Independent PWM Mode

As the name suggests, this mode allows the device to generate a PWM signal with very minimal user intervention. The user only has to define the parameters of the PWM signal (ON time and OFF time). Once begun, the timer block will continuously generate the PWM signal completely independent of the microcontroller. The user software services the timer block only when the PWM parameters require updating.

In this mode the timer Tx counts down at a fixed rate of t_C. Upon every underflow the timer is alternately reloaded with the contents of supporting registers, RxA and RxB. The very first underflow of the timer causes the timer to reload from the register RxA. Subsequent underflows cause the timer to be reloaded from the registers alternately beginning with the register RxB.

The Tx Timer control bits, TxC3, TxC2 and TxC1 set up the timer for PWM mode operation.

Figure 7 shows a block diagram of the timer in PWM mode. The underflows can be programmed to toggle the TxA output pin. The underflows can also be programmed to generate interrupts.

Underflows from the timer are alternately latched into two pending flags, TxPNDA and TxPNDB. The user must reset these pending flags under software control. Two control enable flags, TxENA and TxENB, allow the interrupts from the timer underflow to be enabled or disabled. Setting the timer enable flag TxENA will cause an interrupt when a timer underflow causes the RxA register to be reloaded into the timer. Setting the timer enable flag TxENB will cause an interrupt when a timer underflow causes the RxB register to be reloaded into the timer. Resetting the timer enable flags will disable the associated interrupts.

Either or both of the timer underflow interrupts may be enabled. This gives the user the flexibility of interrupting once per PWM period on either the rising or falling edge of the PWM output. Alternatively, the user may choose to interrupt on both edges of the PWM output.

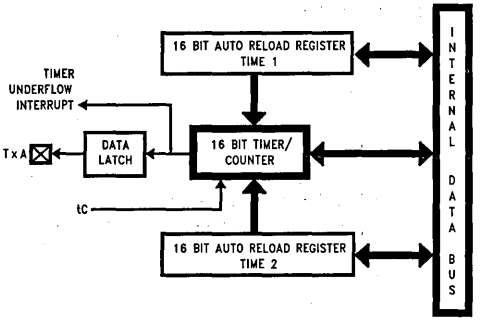

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FIGURE 7. Timer in PWM Mode

Mode 2. External Event Counter Mode

This mode is quite similar to the processor independent PWM mode described above. The main difference is that the timer, Tx, is clocked by the input signal from the TxA pin. The Tx timer control bits, TxC3, TxC2 and TxC1 allow the timer to be clocked either on a positive or negative edge from the TxA pin. Underflows from the timer are latched into the TxPNDA pending flag. Setting the TxENA control flag will cause an interrupt when the timer underflows.

In this mode the input pin TxB can be used as an independent positive edge sensitive interrupt input if the TxENB control flag is set. The occurrence of a positive edge on the TxB input pin is latched into the TxPNDB flag.

Figure 8 shows a block diagram of the timer in External Event Counter mode.

Note: The PWM output is not available in this mode since the TxA pin is being used as the counter input clock.

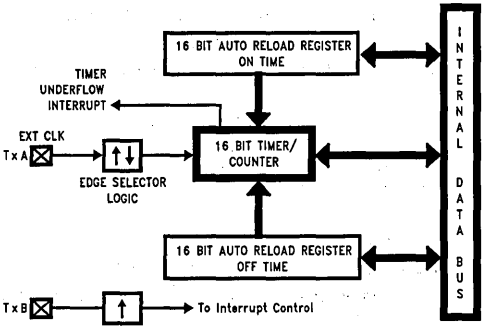

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FIGURE 8. Timer in External Event Counter Mode

Mode 3. Input Capture Mode

The device can precisely measure external frequencies or time external events by placing the timer block, Tx, in the input capture mode.

In this mode, the timer Tx is constantly running at the fixed t_C rate. The two registers, RxA and RxB, act as capture registers. Each register acts in conjunction with a pin. The register RxA acts in conjunction with the TxA pin and the register RxB acts in conjunction with the TxB pin.

Timers (Continued)

The timer value gets copied over into the register when a trigger event occurs on its corresponding pin. Control bits, TxC3, TxC2 and TxC1, allow the trigger events to be specified either as a positive or a negative edge. The trigger condition for each input pin can be specified independently.

The trigger conditions can also be programmed to generate interrupts. The occurrence of the specified trigger condition on the TxA and TxB pins will be respectively latched into the pending flags, TxPNDA and TxPNDB. The control flag TxENA allows the interrupt on TxA to be either enabled or disabled. Setting the TxENA flag enables interrupts to be generated when the selected trigger condition occurs on the TxA pin. Similarly, the flag TxENB controls the interrupts from the TxB pin.

Underflows from the timer can also be programmed to generate interrupts. Underflows are latched into the timer TxC0 pending flag (the TxC0 control bit serves as the timer underflow interrupt pending flag in the Input Capture mode). Consequently, the TxC0 control bit should be reset when entering the Input Capture mode. The timer underflow interrupt is enabled with the TxENA control flag. When a TxA interrupt occurs in the Input Capture mode, the user must check both the TxPNDA and TxC0 pending flags in order to determine whether a TxA input capture or a timer underflow (or both) caused the interrupt.

Figure 9 shows a block diagram of the timer in Input Capture mode.

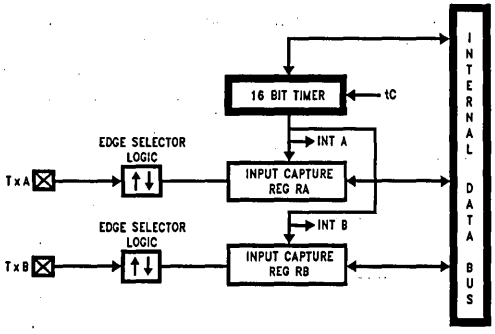

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FIGURE 9. Timer in Input Capture Mode

TIMER CONTROL FLAGS

The timers T1, T2 and T3 have indentical control structures. The control bits and their functions are summarized below.

TxC0	Timer Start/Stop control in Modes 1 and 2 (Processor Independent PWM and External Event Counter), where 1 = Start, 0 = Stop Timer Underflow Interrupt Pending Flag in Mode 3 (Input Capture)
TxPNDA	Timer Interrupt Pending Flag
TxPNDB	Timer Interrupt Pending Flag
TxENA	Timer Interrupt Enable Flag
TxENB	Timer Interrupt Enable Flag 1 = Timer Interrupt Enabled 0 = Timer Interrupt Disabled
TxC3	Timer mode control
TxC2	Timer mode control
TxC1	Timer mode control

Timers (Continued)

The timer mode control bits (TxC3, TxC2 and TxC1) are detailed below:

TxC3	TxC2	TxC1	Timer Mode	Interrupt A Source	Interrupt B Source	Timer Counts On
0	0	0	MODE 2 (External Event Counter)	Timer Underflow	Pos. TxB Edge	TxA Pos. Edge
0	0	1	MODE 2 (External Event Counter)	Timer Underflow	Pos. TxB Edge	TxA Neg. Edge
1	0	1	MODE 1 (PWM) TxA Toggle	Autoreload RA	Autoreload RB.	t_c
1	0	0	MODE 1 (PWM) No TxA Toggle	Autoreload RA	Autoreload RB	t_c
0	1	0	MODE 3 (Capture) Captures: TxA Pos. Edge TxB Pos. Edge	Pos. TxA Edge or Timer Underflow	Pos. TxB Edge	t_c
1	1	0	MODE 3 (Capture) Captures: TxA Pos. Edge TxB Neg. Edge	Pos. TxA Edge or Timer Underflow	Neg. TxB Edge	t_c
0	1	1	MODE 3 (Capture) Captures: TxA Neg. Edge TxB Pos. Edge	Neg. TxB Edge or Timer Underflow	Pos. TxB Edge	t_c
1	1	1	MODE 3 (Capture) Captures: TxA Neg. Edge TxB Neg. Edge	Neg. TxA Edge or Timer Underflow	Neg. TxB Edge	t_c

Power Save Modes

The devices offer the user two power save modes of operation: HALT and IDLE. In the HALT mode, all microcontroller activities are stopped. In the IDLE mode, the on-board oscillator circuitry the WATCHDOG logic, the Clock Monitor and timer T0 are active but all other microcontroller activities are stopped. In either mode, all on-board RAM, registers, I/O states, and timers (with the exception of T0) are unaltered.

HALT MODE

The devices can be placed in the HALT mode by writing a "1" to the HALT flag (G7 data bit). All microcontroller activities, including the clock and timers, are stopped. The WATCHDOG logic on the device is disabled during the HALT mode. However, the clock monitor circuitry if enabled remains active and will cause the WATCHDOG output pin (WDOUT) to go low. If the HALT mode is used and the user does not want to activate the WDOUT pin, the Clock Monitor should be disabled after the device comes out of reset (resetting the Clock Monitor control bit with the first write to the WDSVR register). In the HALT mode, the power requirements of the device are minimal and the applied voltage (V_{CC}) may be decreased to V_r (V_r = 2.0V) without altering the state of the machine.

The devices support three different ways of exiting the HALT mode. The first method of exiting the HALT mode is with the Multi-Input Wakeup feature on the L port. The second method is with a low to high transition on the CKO (G7) pin. This method precludes the use of the crystal clock configuration (since CKO becomes a dedicated output), and so may be used with an RC clock configuration. The third method of exiting the HALT mode is by pulling the $\overline{\text{RESET}}$ pin low.

Since a crystal or ceramic resonator may be selected as the oscillator, the Wakeup signal is not allowed to start the chip running immediately since crystal oscillators and ceramic resonators have a delayed start up time to reach full amplitude and frequency stability. The IDLE timer is used to generate a fixed delay to ensure that the oscillator has indeed stabilized before allowing instruction execution. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry is enabled. The IDLE timer is loaded with a value of 256 and is clocked with the t_c instruction cycle clock. The t_c clock is derived by dividing the oscillator clock down by a factor of 10. The Schmitt trigger following the CKI inverter on the chip ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

If an RC clock option is being used, the fixed delay is introduced optionally. A control bit, CLKDLY, mapped as configuration bit G7, controls whether the delay is to be introduced or not. The delay is included if CLKDLY is set, and excluded if CLKDLY is reset. The CLKDLY bit is cleared on reset.

Power Save Modes (Continued)

The devices have two mask options associated with the HALT mode. The first mask option enables the HALT mode feature, while the second mask option disables the HALT mode. With the HALT mode enable mask option, the device will enter and exit the HALT mode as described above. With the HALT disable mask option, the device cannot be placed in the HALT mode (writing a "1" to the HALT flag will have no effect).

The WATCHDOG detector circuit is inhibited during the HALT mode. However, the clock monitor circuit if enabled remains active during HALT mode in order to ensure a clock monitor error if the device inadvertently enters the HALT mode as a result of a runaway program or power glitch.

IDLE MODE

The device is placed in the IDLE mode by writing a "1" to the IDLE flag (G6 data bit). In this mode, all activities, except the associated on-board oscillator circuitry, the WATCHDOG logic, the clock monitor and the IDLE Timer T0, are stopped. The power supply requirements of the micro-controller in this mode of operation are typically around 30% of normal power requirement of the microcontroller.

As with the HALT mode, the device can be returned to normal operation with a reset, or with a Multi-Input Wakeup from the L Port. Alternately, the microcontroller resumes normal operation from the IDLE mode when the thirteenth bit (representing 4.096 ms at internal clock frequency of 1 MHz, t_c = 1 μs) of the IDLE Timer toggles.

This toggle condition of the thirteenth bit of the IDLE Timer T0 is latched into the T0PND pending flag.

The user has the option of being interrupted with a transition on the thirteenth bit of the IDLE Timer T0. The interrupt can be enabled or disabled via the T0EN control bit. Setting the T0EN flag enables the interrupt and vice versa.

The user can enter the IDLE mode with the Timer T0 interrupt enabled. In this case, when the T0PND bit gets set, the device will first execute the Timer T0 interrupt service routine and then return to the instruction following the "Enter Idle Mode" instruction.

Alternatively, the user can enter the IDLE mode with the IDLE Timer T0 interrupt disabled. In this case, the device will resume normal operation with the instruction immediately following the "Enter IDLE Mode" instruction.

Note: It is necessary to program two NOP instructions following both the set HALT mode and set IDLE mode instructions. These NOP instructions are necessary to allow clock resynchronization following the HALT or IDLE modes.

Multi-Input Wakeup

The Multi-Input Wakeup feature is ued to return (wakeup) the device from either the HALT or IDLE modes. Alternately Multi-Input Wakeup/Interrupt feature may also be used to generate up to 8 edge selectable external interrupts.

Figure 10 shows the Multi-Input Wakeup logic.

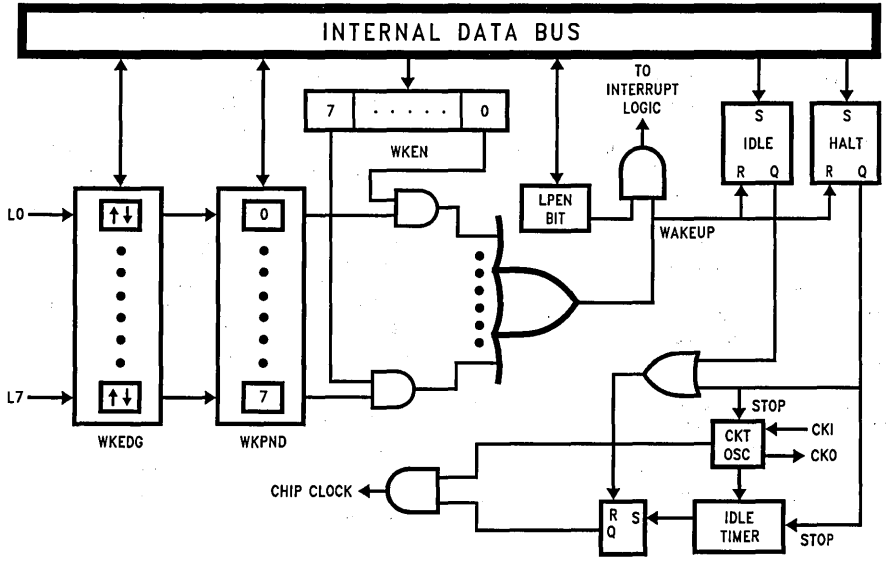

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FIGURE 10. Multi-Input Wake Up Logic

Multi-Input Wakeup (Continued)

The Multi-Input Wakeup feature utilizes the L Port. The user selects which particular L port bit (or combination of L Port bits) will cause the device to exit the HALT or IDLE modes. The selection is done through the Reg: WKEN. The Reg: WKEN is an 8-bit read/write register, which contains a control bit for every L port bit. Setting a particular WKEN bit enables a Wakeup from the associated L port pin.

The user can select whether the trigger condition on the selected L Port pin is going to be either a positive edge (low to high transition) or a negative edge (high to low transition). This selection is made via the Reg: WKEDG, which is an 8-bit control register with a bit assigned to each L Port pin. Setting the control bit will select the trigger condition to be a negative edge on that particular L Port pin. Resetting the bit selects the trigger condition to be a positive edge. Changing an edge select entails several steps in order to avoid a pseudo Wakeup condition as a result of the edge change. First, the associated WKEN bit should be reset, followed by the edge select change in WKEDG. Next, the associated WKPND bit should be cleared, followed by the associated WKEN bit being re-enabled.

An example may serve to clarify this procedure. Suppose we wish to change the edge select from positive (low going high) to negative (high going low) for L Port bit 5, where bit 5 has previously been enabled for an input interrupt. The program would be as follows:

```
RBIT  5, WKEN
SBIT  5, WKEDG
RBIT  5, WKPND
SBIT  5, WKEN
```

If the L port bits have been used as outputs and then changed to inputs with Multi-Input Wakeup/Interrupt, a safety procedure should also be followed to avoid inherited pseudo wakeup conditions. After the selected L port bits have been changed from output to input but before the associated WKEN bits are enabled, the associated edge select bits in WKEDG should be set or reset for the desired edge selects, followed by the associated WKPND bits being cleared.

This same procedure should be used following reset, since the L port inputs are left floating as a result of reset.

The occurrence of the selected trigger condition for Multi-Input Wakeup is latched into a pending register called WKPND. The respective bits of the WKPND register will be set on the occurrence of the selected trigger edge on the corresponding Port L pin. The user has the responsibility of clearing these pending flags. Since WKPND is a pending register for the occurrence of selected wakeup conditions, the device will not enter the HALT mode if any Wakeup bit is both enabled and pending. Consequently, the user has the responsibility of clearing the pending flags before attempting to enter the HALT mode.

WKEN, WKPND and WKEDG are all read/write registers, and are cleared at reset.

PORT L INTERRUPTS

Port L provides the user with an additional eight fully selectable, edge sensitive interrupts which are all vectored into the same service subroutine.

The interrupt from Port L shares logic with the wake up circuitry. The register WKEN allows interrupts from Port L to be individually enabled or disabled. The register WKEDG specifies the trigger condition to be either a positive or a negative edge. Finally, the register WKPND latches in the pending trigger conditions.

The GIE (Global Interrupt Enable) bit enables the interrupt function.

A control flag, LPEN, functions as a global interrupt enable for Port L interrupts. Setting the LPEN flag will enable interrupts and vice versa. A separate global pending flag is not needed since the register WKPND is adequate.

Since Port L is also used for waking the device out of the HALT or IDLE modes, the user can elect to exit the HALT or IDLE modes either with or without the interrupt enabled. If he elects to disable the interrupt, then the device will restart execution from the instruction immediately following the instruction that placed the microcontroller in the HALT or IDLE modes. In the other case, the device will first execute the interrupt service routine and then revert to normal operation.

The Wakeup signal will not start the chip running immediately since crystal oscillators or ceramic resonators have a finite start up time. The IDLE Timer (T0) generates a fixed delay to ensure that the oscillator has indeed stabilized before allowing the device to execute instructions. In this case, upon detecting a valid Wakeup signal, only the oscillator circuitry and the IDLE Timer T0 are enabled. The IDLE Timer is loaded with a value of 256 and is clocked from the t_C instruction cycle clock. The t_C clock is derived by dividing down the oscillator clock by a factor of 10. A Schmitt trigger following the CKI on-chip inverter ensures that the IDLE timer is clocked only when the oscillator has a sufficiently large amplitude to meet the Schmitt trigger specifications. This Schmitt trigger is not part of the oscillator closed loop. The startup timeout from the IDLE timer enables the clock signals to be routed to the rest of the chip.

If the RC clock option is used, the fixed delay is under software control. A control flag, CLKDLY, in the G7 configuration bit allows the clock start up delay to be optionally inserted. Setting CLKDLY flag high will cause clock start up delay to be inserted and resetting it will exclude the clock start up delay. The CLKDLY flag is cleared during reset, so the clock start up delay is not present following reset with the RC clock options.

UART

The device contains a full-duplex software programmable UART. The UART *(Figure 11)* consists of a transmit shift register, a receiver shift register and seven addressable registers, as follows: a transmit buffer register (TBUF), a receiver buffer register (RBUF), a UART control and status register (ENU), a UART receive control and status register (ENUR), a UART interrupt and clock source register (ENUI), a prescaler select register (PSR) and baud (BAUD) register. The ENU register contains flags for transmit and receive functions; this register also determines the length of the data frame (7, 8 or 9 bits), the value of the ninth bit in transmission, and parity selection bits. The ENUR register flags framming, data overrun and parity errors while the UART is receiving.

Other functions of the ENUR register include saving the ninth bit received in the data frame, enabling or disabling the UART's attention mode of operation and providing additional receiver/transmitter status information via RCVG and XMTG bits. The determination of an internal or external clock source is done by the ENUI register, as well as selecting the number of stop bits and enabling or disabling transmit and receive interrupts. A control flag in this register can also select the UART mode of operation: asynchronous or synchronous.

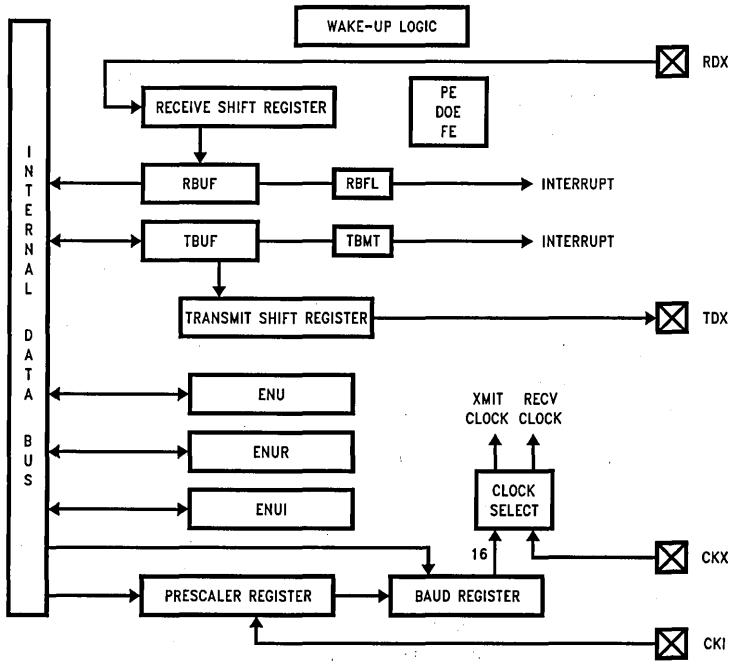

FIGURE 11. UART Block Diagram

UART (Continued)

UART CONTROL AND STATUS REGISTERS

The operation of the UART is programmed through three registers: ENU, ENUR and ENUI. The function of the individual bits in these registers is as follows:

ENU-UART Control and Status Register (Address at 0BA)

PEN	PSEL1	XBIT9/ PSEL0	CHL1	CHL0	ERR	RBFL	TBMT
0RW	0RW	0RW	0RW	0RW	0R	0R	1R

Bit 7 Bit 0

ENUR-UART Receive Control and Status Register (Address at 0BB)

DOE	FE	PE	SPARE	RBIT9	ATTN	XMTG	RCVG
0RD	0RD	0RD	0RW*	0R	0RW	0R	0R

Bit7 Bit0

ENUI-UART Interrupt and Clock Source Register (Address at 0BC)

STP2	STP78	ETDX	SSEL	XRCLK	XTCLK	ERI	ETI
0RW	0RW	0RW	0RW	0RW	0RW	0RW	0RW

Bit7 Bit0

*Bit is not used.

0 Bit is cleared on reset.

1 Bit is set to one on reset.

R Bit is read-only; it cannot be written by software.

RW Bit is read/write.

D Bit is cleared on read; when read by software as a one, it is cleared automatically. Writing to the bit does not affect its state.

DESCRIPTION OF UART REGISTER BITS

ENU—UART CONTROL AND STATUS REGISTER

TBMT: This bit is set when the UART transfers a byte of data from the TBUF register into the TSFT register for transmission. It is automatically reset when software writes into the TBUF register.

RBFL: This bit is set when the UART has received a complete character and has copied it into the RBUF register. It is automatically reset when software reads the character from RBUF.

ERR: This bit is a global UART error flag which gets set if any or a combination of the errors (DOE, FE, PE) occur.

CHL1, CHL0: These bits select the character frame format. Parity is not included and is generated/verified by hardware.

CHL1 = 0, CHL0 = 0 The frame contains eight data bits.
CHL1 = 0, CHL0 = 1 The frame contains seven data bits.
CHL1 = 1, CHL0 = 0 The frame contains nine data bits.
CHL1 = 1, CHL0 = 1 Loopback Mode selected. Transmitter output internally looped back to receiver input. Nine bit framing format is used.

XBIT9/PSEL0: Programs the ninth bit for transmission when the UART is operating with nine data bits per frame. For seven or eight data bits per frame, this bit in conjunction with PSEL1 selects parity.

PSEL1, PSEL0: Parity select bits.

PSEL1 = 0, PSEL0 = 0 Odd Parity (if Parity enabled)
PSEL1 = 0, PSEL0 = 1 Even Parity (if Parity enabled)
PSEL1 = 1, PSEL0 = 0 Mark(1) (if Parity enabled)
PSEL1 = 1, PSEL0 = 1 Space(0) (if Parity enabled)

PEN: This bit enables/disables Parity (7- and 8-bit modes only).

PEN = 0 Parity disabled.
PEN = 1 Parity enabled.

ENUR—UART RECEIVE CONTROL AND STATUS REGISTER

RCVG: This bit is set high whenever a framing error occurs and goes low when RDX goes high.

XMTG: This bit is set to indicate that the UART is transmitting. It gets reset at the end of the last frame (end of last Stop bit).

ATTN: ATTENTION Mode is enabled while this bit is set. This bit is cleared automatically on receiving a character with data bit nine set.

RBIT9: Contains the ninth data bit received when the UART is operating with nine data bits per frame.

SPARE: Reserved for future use.

PE: Flags a Parity Error.

PE = 0 Indicates no Parity Error has been detected since the last time the ENUR register was read.
PE = 1 Indicates the occurrence of a Parity Error.

FE: Flags a Framing Error.

FE = 0 Indicates no Framing Error has been detected since the last time the ENUR register was read.
FE = 1 Indicates the occurrence of a Framing Error.

DOE: Flags a Data Overrun Error.

DOE = 0 Indicates no Data Overrun Error has been detected since the last time the ENUR register was read.
DOE = 1 Indicates the occurrence of a Data Overrun Error.

ENUI—UART INTERRUPT AND CLOCK SOURCE REGISTER

ETI: This bit enables/disables interrupt from the transmitter section.

ETI = 0 Interrupt from the transmitter is disabled.
ETI = 1 Interrupt from the transmitter is enabled.

ERI: This bit enables/disables interrupt from the receiver section.

ERI = 0 Interrupt from the receiver is disabled.
ERI = 1 Interrupt from the receiver is enabled.

XTCLK: This bit selects the clock source for the transmitter-section.

XTCLK = 0 The clock source is selected through the PSR and BAUD registers.
XTCLK = 1 Signal on CKX (L1) pin is used as the clock.

XRCLK: This bit selects the clock source for the receiver section.

XRCLK = 0 The clock source is selected through the PSR and BAUD registers.
XRCLK = 1 Signal on CKX (L1) pin is used as the clock.

SSEL: UART mode select.

SSEL = 0 Asynchronous Mode.
SSEL = 1 Synchronous Mode.

UART (Continued)

ETDX: TDX (UART Transmit Pin) is the alternate function assigned to Port L pin L2; it is selected by setting ETDX bit. To simulate line break generation, software should reset ETDX bit and output logic zero to TDX pin through Port L data and configuration registers.

STP78: This bit is set to program the last Stop bit to be 7/8th of a bit in length.

STP2: This bit programs the number of Stop bits to be transmitted.

STP2 = 0 One Stop bit transmitted.
STP2 = 1 Two Stop bits transmitted.

Associated I/O Pins

Data is transmitted on the TDX pin and received on the RDX pin. TDX is the alternate function assigned to Port L pin L2; it is selected by setting ETDX (in the ENUI register) to one. RDX is an inherent function of Port L pin L3, requiring no setup.

The baud rate clock for the UART can be generated on-chip, or can be taken from an external source. Port L pin L1 (CKX) is the external clock I/O pin. The CKX pin can be either an input or an output, as determined by Port L Configuration and Data registers (Bit 1). As an input, it accepts a clock signal which may be selected to drive the transmitter and/or receiver. As an output, it presents the internal Baud Rate Generator output.

UART Operation

The UART has two modes of operation: asynchronous mode and synchronous mode.

ASYNCHRONOUS MODE

This mode is selected by resetting the SSEL (in the ENUI register) bit to zero. The input frequency to the UART is 16 times the baud rate.

The TSFT and TBUF registers double-buffer data for transmission. While TSFT is shifting out the current character on the TDX pin, the TBUF register may be loaded by software with the next byte to be transmitted. When TSFT finishes transmitting the current character the contents of TBUF are transferred to the TSFT register and the Transmit Buffer Empty Flag (TBMT in the ENU register) is set. The TBMT flag is automatically reset by the UART when software loads a new character into the TBUF register. There is also the XMTG bit which is set to indicate that the UART is transmitting. This bit gets reset at the end of the last frame (end of last Stop bit). TBUF is a read/write register.

The RSFT and RBUF registers double-buffer data being received. The UART receiver continually monitors the signal on the RDX pin for a low level to detect the beginning of a Start bit. Upon sensing this low level, it waits for half a bit time and samples again. If the RDX pin is still low, the receiver considers this to be a valid Start bit, and the remaining bits in the character frame are each sampled a single time, at the mid-bit position. Serial data input on the RDX pin is shifted into the RSFT register. Upon receiving the complete character, the contents of the RSFT register are copied into the RBUF register and the Received Buffer Full Flag (RBFL) is set. RBFL is automatically reset when software reads the character from the RBUF register. RBUF is a read only register. There is also the RCVG bit which is set high when a framing error occurs and goes low once RDX goes high. TBMT, XMTG, RBFL and RCVG are read only bits.

SYNCHRONOUS MODE

In this mode data is transferred synchronously with the clock. Data is transmitted on the rising edge and received on the falling edge of the synchronous clock.

This mode is selected by setting SSEL bit in the ENUI register. The input frequency to the UART is the same as the baud rate.

When an external clock input is selected at the CKX pin, data transmit and receive are performed synchronously with this clock through TDX/RDX pins.

If data transmit and receive are selected with the CKX pin as clock output, the device generates the synchronous clock output at the CKX pin. The internal baud rate generator is used to produce the synchronous clock. Data transmit and receive are performed synchronously with this clock.

FRAMING FORMATS

The UART supports several serial framing formats *(Figure 12)*. The format is selected using control bits in the ENU, ENUR and ENUI registers.

The first format (1, 1a, 1b, 1c) for data transmission (CHL0 = 1, CHL1 = 0) consists of Start bit, seven Data bits (excluding parity) and 7/8, one or two Stop bits. In applications using parity, the parity bit is generated and verified by hardware.

The second format (CHL0 = 0, CHL1 = 0) consists of one Start bit, eight Data bits (excluding parity) and 7/8, one or two Stop bits. Parity bit is generated and verified by hardware.

The third format for transmission (CHL0 = 0, CHL1 = 1) consists of one Start bit, nine Data bits and 7/8, one or two Stop bits. This format also supports the UART "ATTENTION" feature. When operating in this format, all eight bits of TBUF and RBUF are used for data. The ninth data bit is transmitted and received using two bits in the ENU and ENUR registers, called XBIT9 and RBIT9. RBIT9 is a read only bit. Parity is not generated or verified in this mode.

For any of the above framing formats, the last Stop bit can be programmed to be 7/8th of a bit in length. If two Stop bits are selected and the 7/8th bit is set (selected), the second Stop bit will be 7/8th of a bit in length.

The parity is enabled/disabled by PEN bit located in the ENU register. Parity is selected for 7- and 8-bit modes only. If parity is enabled (PEN = 1), the parity selection is then performed by PSEL0 and PSEL1 bits located in the ENU register.

Note that the XBIT9/PSEL0 bit located in the ENU register serves two mutually exclusive functions. This bit programs the ninth bit for transmission when the UART is operating with nine data bits per frame. There is no parity selection in this framing format. For other framing formats XBIT9 is not needed and the bit is PSEL0 used in conjunction with PSEL1 to select parity.

The frame formats for the receiver differ from the transmitter in the number of Stop bits required. The receiver only requires one Stop bit in a frame, regardless of the setting of the Stop bit selection bits in the control register. Note that an implicit assumption is made for full duplex UART operation that the framing formats are the same for the transmitter and receiver.

UART Operation (Continued)

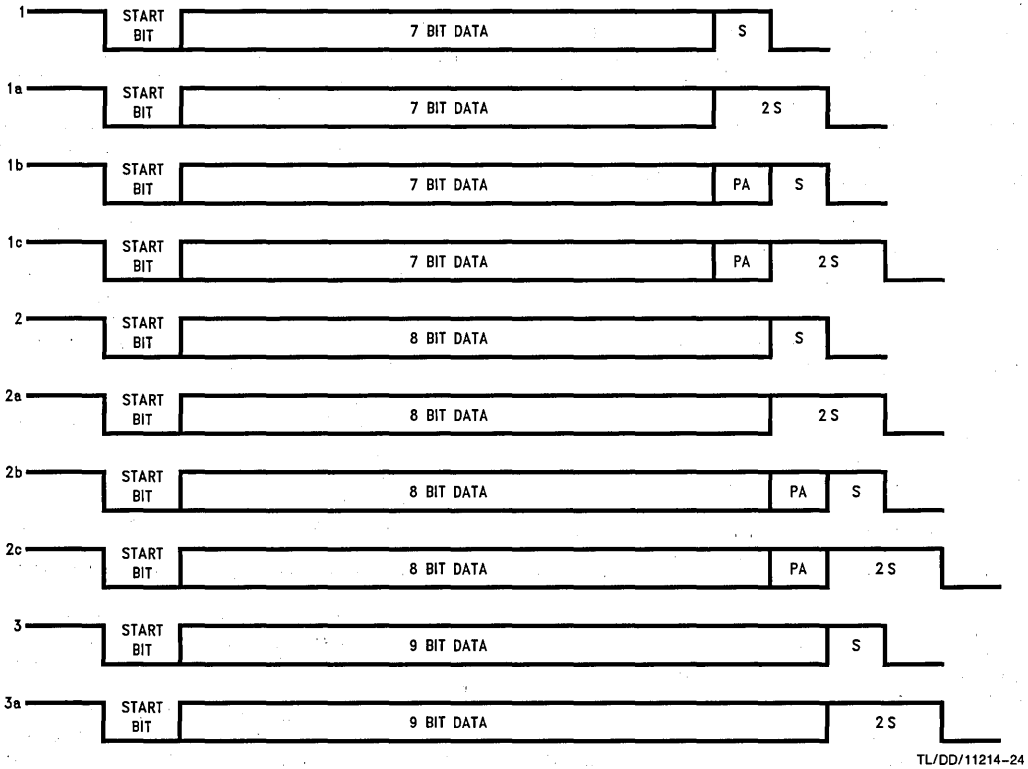

FIGURE 12. Framing Formats

UART INTERRUPTS

The UART is capable of generating interrupts. Interrupts are generated on Receive Buffer Full and Transmit Buffer Empty. Both interrupts have individual interrupt vectors. Two bytes of program memory space are reserved for each interrupt vector. The two vectors are located at addresses 0xEC to 0xEF Hex in the program memory space. The interrupts can be individually enabled or disabled using Enable Transmit Interrupt (ETI) and Enable Receive Interrupt (ERI) bits in the ENUI register.

The interrupt from the Transmitter is set pending, and remains pending, as long as both the TBMT and ETI bits are set. To remove this interrupt, software must either clear the ETI bit or write to the TBUF register (thus clearing the TBMT bit).

The interrupt from the receiver is set pending, and remains pending, as long as both the RBFL and ERI bits are set. To remove this interrupt, software must either clear the ERI bit or read from the RBUF register (thus clearing the RBFL bit).

Baud Clock Generation

The clock inputs to the transmitter and receiver sections of the UART can be individually selected to come either from an external source at the CKX pin (port L, pin L1) or from a source selected in the PSR and BAUD registers. Internally, the basic baud clock is created from the oscillator frequency through a two-stage divider chain consisting of a 1–16 (increments of 0.5) prescaler and an 11-bit binary counter. *(Figure 13)* The divide factors are specified through two read/write registers shown in *Figure 14*. Note that the 11-bit Baud Rate Divisor spills over into the Prescaler Select Register (PSR). PSR is cleared upon reset.

As shown in Table I, a Prescaler Factor of 0 corresponds to NO CLOCK. NO CLOCK condition is the UART power down mode where the UART clock is turned off for power saving purpose. The user must also turn the UART clock off when a different baud rate is chosen.

The correspondences between the 5-bit Prescaler Select and Prescaler factors are shown in Table I. Therer are many ways to calculate the two divisor factors, but one particularly effective method would be to achieve a 1.8432 MHz frequency coming out of the first stage. The 1.8432 MHz prescaler output is then used to drive the software programmable baud rate counter to create a x16 clock for the following baud rates: 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19200 and 38400 (Table II). Other baud rates may be created by using appropriate divisors. The x16 clock is then divided by 16 to provide the rate for the serial shift registers of the transmitter and receiver.

Baud Clock Generation (Continued)

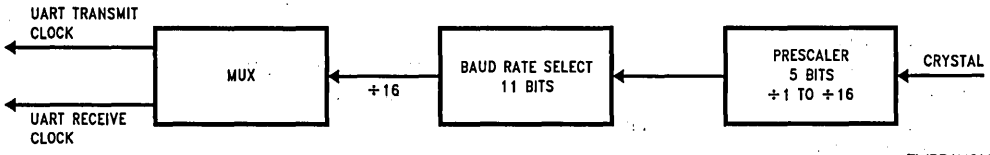

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FIGURE 13. UART BAUD Clock Generation

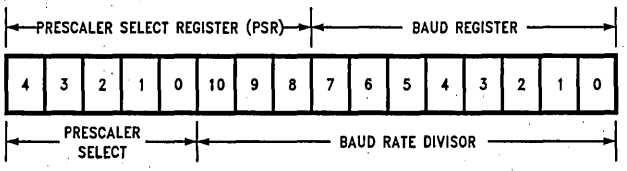

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FIGURE 14. UART BAUD Clock Divisor Registers

TABLE I. Prescaler Factors

Prescaler Select	Prescaler Factor
00000	NO CLOCK
00001	1
00010	1.5
00011	2
00100	2.5
00101	3
00110	3.5
00111	4
01000	4.5
01001	5
01010	5.5
01011	6
01100	6.5
01101	7
01110	7.5
01111	8
10000	8.5
10001	9
10010	9.5
10011	10
10100	10.5
10101	11
10110	11.5
10111	12
11000	12.5
11001	13
11010	13.5
11011	14
11100	14.5
11101	15
11110	15.5
11111	16

TABLE II. Baud Rate Divisors (1.8432 MHz Prescaler Output)

Baud Rate	Baud Rate Divisor − 1 (N-1)
110 (110.03)	1046
134.5 (134.58)	855
150	767
300	383
600	191
1200	95
1800	63
2400	47
3600	31
4800	23
7200	15
9600	11
19200	5
38400	2

The entries in Table II assume a prescaler output of 1.8432 MHz. In the asynchronous mode the baud rate could be as high as 625k.

As an example, considering the Asynchronous Mode and a CKI clock of 4.608 MHz, the prescaler factor selected is:

$$4.608/1.8432 = 2.5$$

The 2.5 entry is available in Table I. The 1.8432 MHz prescaler output is then used with proper Baud Rate Divisor (Table II) to obtain different baud rates. For a baud rate of 19200 e.g., the entry in Table II is 5.

$N - 1 = 5$ ($N - 1$ is the value from Table II)

$N = 6$ (N is the Baud Rate Divisor)

$$\text{Baud Rate} = 1.8432\ \text{MHz}/(16 \times 6) = 19200$$

The divide by 16 is performed because in the asynchronous mode, the input frequency to the UART is 16 times the baud rate. The equation to calculate baud rates is given below.

The actual Baud Rate may be found from:

$$BR = Fc/(16 \times N \times P)$$

7

Baud Clock Generation (Continued)

Where:

BR is the Baud Rate

Fc is the CKI frequency

N is the Baud Rate Divisor (Table II).

P is the Prescaler Divide Factor selected by the value in the Prescaler Select Register (Table I)

Note: In the Synchronous Mode, the divisor 16 is replaced by two.

Example:

Asynchronous Mode:

Crystal Frequency = 5 MHz

Desired baud rate = 9600

Using the above equation N × P can be calculated first.

$$N \times P = (5 \times 10^6)/(16 \times 9600) = 32.552$$

Now 32.552 is divided by each Prescaler Factor (Table II) to obtain a value closest to an integer. This factor happens to be 6.5 (P = 6.5).

$$N = 32.552/6.5 = 5.008 \text{ (N = 5)}$$

The programmed value (from Table II) should be 4 (N − 1).

Using the above values calculated for N and P:

$$BR = (5 \times 10^6)/(16 \times 5 \times 6.5) = 9615.384$$

$$\% \text{ error} = (9615.385 - 9600)/9600 = 0.16$$

Effect of HALT/IDLE

The UART logic is reinitialized when either the HALT or IDLE modes are entered. This reinitialization sets the TBMT flag and resets all read only bits in the UART control and status registers. Read/Write bits remain unchanged. The Transmit Buffer (TBUF) is not affected, but the Transmit Shift register (TSFT) bits are set to one. The receiver registers RBUF and RSFT are not affected.

The device will exit from the HALT/IDLE modes when the Start bit of a character is detected at the RDX (L3) pin. This feature is obtained by using the Multi-Input Wakeup scheme provided on the device.

Before entering the HALT or IDLE modes the user program must select the Wakeup source to be on the RDX pin. This selection is done by setting bit 3 of WKEN (Wakeup Enable) register. The Wakeup trigger condition is then selected to be high to low transition. This is done via the WKEDG register (Bit 3 is zero.)

If the device is halted and crystal oscillator is used, the Wakeup signal will not start the chip running immediately because of the finite start up time requirement of the crystal oscillator. The idle timer (T0) generates a fixed delay to ensure that the oscillator has indeed stabilized before allowing the device to execute code. The user has to consider this delay when data transfer is expected immediately after exiting the HALT mode.

Diagnostic

Bits CHARL0 and CHARL1 in the ENU register provide a loopback feature for diagnostic testing of the UART. When these bits are set to one, the following occur: The receiver input pin (RDX) is internally connected to the transmitter output pin (TDX); the output of the Transmitter Shift Register is "looped back" into the Receive Shift Register input. In this mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and receive data paths of the UART.

Note that the framing format for this mode is the nine bit format; one Start bit, nine data bits, and 7/8, one or two Stop bits. Parity is not generated or verified in this mode.

Attention Mode

The UART Receiver section supports an alternate mode of operation, referred to as ATTENTION Mode. This mode of operation is selected by the ATTN bit in the ENUR register. The data format for transmission must also be selected as having nine Data bits and either 7/8, one or two Stop bits.

The ATTENTION mode of operation is intended for use in networking the device with other processors. Typically in such environments the messages consists of device addresses, indicating which of several destinations should receive them, and the actual data. This Mode supports a scheme in which addresses are flagged by having the ninth bit of the data field set to a 1. If the ninth bit is reset to a zero the byte is a Data byte.

While in ATTENTION mode, the UART monitors the communication flow, but ignores all characters until an address character is received. Upon receiving an address character, the UART signals that the character is ready by setting the RBFL flag, which in turn interrupts the processor if UART Receiver interrupts are enabled. The ATTN bit is also cleared automatically at this point, so that data characters as well as address characters are recognized. Software examines the contents of the RBUF and responds by deciding either to accept the subsequent data stream (by leaving the ATTN bit reset) or to wait until the next address character is seen (by setting the ATTN bit again).

Operation of the UART Transmitter is not affected by selection of this Mode. The value of the ninth bit to be transmitted is programmed by setting XBIT9 appropriately. The value of the ninth bit received is obtained by reading RBIT9. Since this bit is located in ENUR register where the error flags reside, a bit operation on it will reset the error flags.

Comparators

The devices contain two differential comparators, each with a pair of inputs (positive and negative) and an output. Ports I1–I3 and I4–I6 are used for the comparators. The following is the Port I assignment:

- I1 Comparator1 negative input
- I2 Comparator1 positive input
- I3 Comparator1 output
- I4 Comparator2 negative input
- I5 Comparator2 positive input
- I6 Comparator2 output

A Comparator Select Register (CMPSL) is used to enable the comparators, read the outputs of the comparators internally, and enable the outputs of the comparators to the pins. Two control bits (enable and output enable) and one result bit are associated with each comparator. The comparator result bits (CMP1RD and CMP2RD) are read only bits which will read as zero if the associated comparator is not enabled. The Comparator Select Register is cleared with reset, resulting in the comparators being disabled. The comparators should also be disabled before entering either the HALT or IDLE modes in order to save power. The configuration of the CMPSL register is as follows:

Comparators (Continued)

CMPSL REGISTER (ADDRESS X'00B7)

The CMPSL register contains the following bits:

CMP1EN	Enable comparator 1
CMP1RD	Comparator 1 result (this is a read only bit, which will read as 0 if the comparator is not enabled)
CMP10E	Selects pin I3 as comparator 1 output provided that CMPIEN is set to enable the comparator
CMP2EN	Enable comparator 2
CMP2RD	Comparator 2 result (this is a read only bit, which will read as 0 if the comparator is not enabled)
CMP20E	Selects pin I6 as comparator 2 output provided that CMP2EN is set to enable the comparator

Unused	CMP20E	CMP2RD	CMP2EN	CMP10E	CMP1RD	CMP1EN	Unused
Bit 7							Bit 0

Note that the two unused bits of CMPSL may be used as software flags.

Comparator outputs have the same spec as Ports L and G except that the rise and fall times are symmetrical.

Interrupts

The devices support a vectored interrupt scheme. It supports a total of fourteen interrupt sources. The following table lists all the possible device interrupt sources, their arbitration ranking and the memory locations reserved for the interrupt vector for each source.

Two bytes of program memory space are reserved for each interrupt source. All interrupt sources except the software interrupt are maskable. Each of the maskable interrupts have an Enable bit and a Pending bit. A maskable interrupt is active if its associated enable and pending bits are set. If GIE = 1 and an interrupt is active, then the processor will be interrupted as soon as it is ready to start executing an instruction except if the above conditions happen during the Software Trap service routine. This exception is described in the Software Trap sub-section.

The interruption process is accomplished with the INTR instruction (opcode 00), which is jammed inside the Instruction Register and replaces the opcode about to be executed. The following steps are performed for every interrupt:

1. The GIE (Global Interrupt Enable) bit is reset.
2. The address of the instruction about to be executed is pushed into the stack.
3. The PC (Program Counter) branches to address 00FF. This procedure takes 7 t_c cycles to execute.

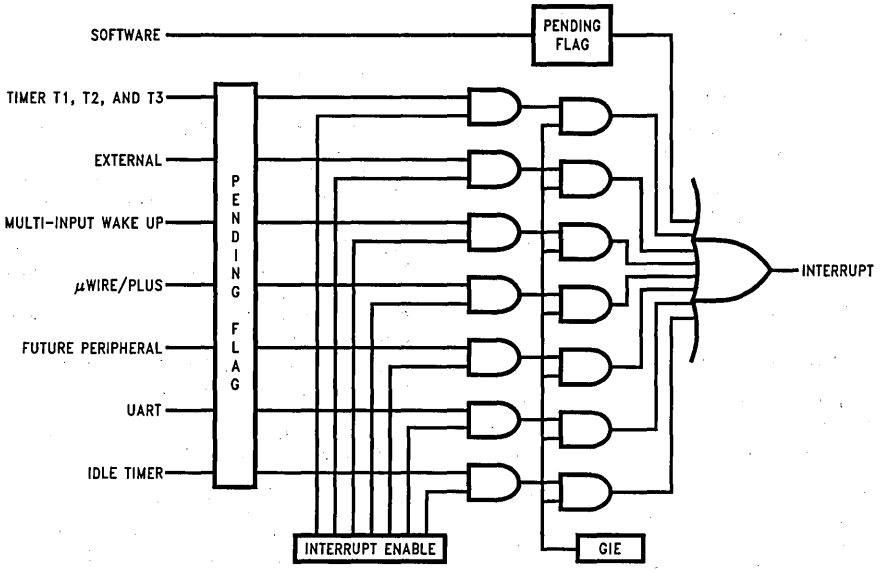

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FIGURE 15. Interrupt Block Diagram

Interrupts (Continued)

Arbitration Ranking	Source	Description	Vector Address HI-Low Byte
(1) Highest	Software	INTR Instruction	0yFE–0yFF
	Reserved	for Future Use	0yFC–0yFD
(2)	External	Pin G0 Edge	0yFA–0yFB
(3)	Timer T0	Underflow	0yF8–0yF9
(4)	Timer T1	T1A/Underflow	0yF6–0yF7
(5)	Timer T1	T1B	0yF4–0yF5
(6)	MICROWIRE/PLUS	BUSY Goes Low	0yF2–0yF3
	Reserved	for Future Use	0yF0–0yF1
(7)	UART	Receive	0yEE–0yEF
(8)	UART	Transmit	0yEC–0yED
(9)	Timer T2	T2A/Underflow	0yEA–0yEB
(10)	Timer T2	T2B	0yE8–0yE9
(11)	Timer T3	T3A/Underflow	0yE6–0yE7
(12)	Timer T3	T3B	0yE4–0yE5
(13)	Port L/Wakeup	Port L Edge	0yE2–0yE3
(14) Lowest	Default	VIS Instr. Execution without Any Interrupts	0yE0–0yE1

y is VIS page, $y \neq 0$.

At this time, since GIE = 0, other maskable interrupts are disabled. The user is now free to do whatever context switching is required by saving the context of the machine in the stack with PUSH instructions. The user would then program a VIS (Vector Interrupt Select) instruction in order to branch to the interrupt service routine of the highest priority interrupt enabled and pending at the time of the VIS. Note that this is not necessarily the interrupt that caused the branch to address location 00FF Hex prior to the context switching.

Thus, if an interrupt with a higher rank than the one which caused the interruption becomes active before the decision of which interrupt to service is made by the VIS, then the interrupt with the higher rank will override any lower ones and will be acknowledged. The lower priority interrupt(s) are still pending, however, and will cause another interrupt immediately following the completion of the interrupt service routine associated with the higher priority interrupt just serviced. This lower priority interrupt will occur immediately following the RETI (Return from Interrupt) instruction at the end of the interrupt service routine just completed.

Inside the interrupt service routine, the associated pending bit has to be cleared by software. The RETI (Return from Interrupt) instruction at the end of the interrupt service routine will set the GIE (Global Interrupt Enable) bit, allowing the processor to be interrupted again if another interrupt is active and pending.

The VIS instruction looks at all the active interrupts at the time it is executed and performs an indirect jump to the beginning of the service routine of the one with the highest rank.

The addresses of the different interrupt service routines, called vectors, are chosen by the user and stored in ROM in a table starting at 01E0 (assuming that VIS is located between 00FF and 01DF). The vectors are 15-bit wide and therefore occupy 2 ROM locations.

VIS and the vector table must be located in the same 256-byte block (0y00 to 0yFF) except if VIS is located at the last address of a block. In this case, the table must be in the next block. The vector table cannot be inserted in the first 256-byte block ($y \neq 0$).

The vector of the maskable interrupt with the lowest rank is located at 0yE0 (Hi-Order byte) and 0yE1 (Lo-Order byte) and so forth in increasing rank number. The vector of the maskable interrupt with the highest rank is located at 0yFA (Hi-Order byte) and 0yFB (Lo-Order byte).

The Software Trap has the highest rank and its vector is located at 0yFE and 0yFF.

If, by accident, a VIS gets executed and no interrupt is active, then the PC (Program Counter) will branch to a vector located at 0yE0–0yE1. This vector can point to the Software Trap (ST) interrupt service routine, or to another special service routine as desired.

Figure 15 shows the Interrupt block diagram.

SOFTWARE TRAP

The Software Trap (ST) is a special kind of non-maskable interrupt which occurs when the INTR instruction (used to acknowledge interrupts) is fetched from ROM and placed inside the instruction register. This may happen when the PC is pointing beyond the available ROM address space or when the stack is over-popped.

Interrupts (Continued)

When an ST occurs, the user can re-initialize the stack pointer and do a recovery procedure (similar to reset, but not necessarily containing all of the same initialization procedures) before restarting.

The occurrence of an ST is latched into the ST pending bit. The GIE bit is not affected and the ST pending bit **(not accessible by the user)** is used to inhibit other interrupts and to direct the program to the ST service routine with the VIS instruction. The RPND instruction is used to clear the software interrupt pending bit. This pending bit is also cleared on reset.

The ST has the highest rank among all interrupts.

Nothing (except another ST) can interrupt an ST being serviced.

WATCHDOG

The devices contain a WATCHDOG and clock monitor. The WATCHDOG is designed to detect the user program getting stuck in infinite loops resulting in loss of program control or "runaway" programs. The Clock Monitor is used to detect the absence of a clock or a very slow clock below a specified rate on the CKI pin.

The WATCHDOG consists of two independent logic blocks: WD UPPER and WD LOWER. WD UPPER establishes the upper limit on the service window and WD LOWER defines the lower limit of the service window.

Servicing the WATCHDOG consists of writing a specific value to a WATCHDOG Service Register named WDSVR which is memory mapped in the RAM. This value is composed of three fields, consisting of a 2-bit Window Select, a 5-bit Key Data field, and the 1-bit Clock Monitor Select field. Table III shows the WDSVR register.

The lower limit of the service window is fixed at 2048 instruction cycles. Bits 7 and 6 of the WDSVR register allow the user to pick an upper limit of the service window.

Table IV shows the four possible combinations of lower and upper limits for the WATCHDOG service window. This flexibility in choosing the WATCHDOG service window prevents any undue burden on the user software.

Bits 5, 4, 3, 2 and 1 of the WDSVR register represent the 5-bit Key Data field. The key data is fixed at 01100. Bit 0 of the WDSVR Register is the Clock Monitor Select bit.

TABLE III. WATCHDOG Service Register (WDSVR)

Window Select		Key Data					Clock Monitor
X	X	0	1	1	0	0	Y
7	6	5	4	3	2	1	0

TABLE IV. WATCHDOG Service Window Select

WDSVR Bit 7	WDSVR Bit 6	Service Window (Lower-Upper Limits)
0	0	2k–8k t_c Cycles
0	1	2k–16k t_c Cycles
1	0	2k–32k t_c Cycles
1	1	2k–64k t_c Cycles

Clock Monitor

The Clock Monitor aboard the device can be selected or deselected under program control. The Clock Monitor is guaranteed not to reject the clock if the instruction cycle clock ($1/t_c$) is greater or equal to 10 kHz. This equates to a clock input rate on CKI of greater or equal to 100 kHz.

WATCHDOG Operation

The WATCHDOG and Clock Monitor are disabled during reset. The device comes out of reset with the WATCHDOG armed, the WATCHDOG Window Select bits (bits 6, 7 of the WDSVR Register) set, and the Clock Monitor bit (bit 0 of the WDSVR Register) enabled. Thus, a Clock Monitor error will occur after coming out of reset, if the instruction cycle clock frequency has not reached a minimum specified value, including the case where the oscillator fails to start.

The WDSVR register can be written to only once after reset and the key data (bits 5 through 1 of the WDSVR Register) must match to be a valid write. This write to the WDSVR register involves two irrevocable choices: (i) the selection of the WATCHDOG service window (ii) enabling or disabling of the Clock Monitor. Hence, the first write to WDSVR Register involves selecting or deselecting the Clock Monitor, select the WATCHDOG service window and match the WATCHDOG key data. Subsequent writes to the WDSVR register will compare the value being written by the user to the WATCHDOG service window value and the key data (bits 7 through 1) in the WDSVR Register. Table V shows the sequence of events that can occur.

The user must service the WATCHDOG at least once before the upper limit of the service window expires. The WATCHDOG may not be serviced more than once in every lower limit of the service window. The user may service the WATCHDOG as many times as wished in the time period between the lower and upper limits of the service window. The first write to the WDSVR Register is also counted as a WATCHDOG service.

The WATCHDOG has an output pin associated with it. This is the WDOUT pin, on pin 1 of the port G. WDOUT is active low. The WDOUT pin is in the high impedance state in the inactive state. Upon triggering the WATCHDOG, the logic will pull the WDOUT (G1) pin low for an additional 16 t_c–32 t_c cycles after the signal level on WDOUT pin goes below the lower Schmitt trigger threshold. After this delay, the device will stop forcing the WDOUT output low.

The WATCHDOG service window will restart when the WDOUT pin goes high. It is recommended that the user tie the WDOUT pin back to V_{CC} through a resistor in order to pull WDOUT high.

A WATCHDOG service while the WDOUT signal is active will be ignored. The state of the WDOUT pin is not guaranteed on reset, but if it powers up low then the WATCHDOG will time out and WDOUT will enter high impedance state.

The Clock Monitor forces the G1 pin low upon detecting a clock frequency error. The Clock Monitor error will continue until the clock frequency has reached the minimum specified value, after which the G1 output will enter the high impedance TRI-STATE mode following 16 t_c–32 t_c clock cycles. The Clock Monitor generates a continual Clock Monitor error if the oscillator fails to start, or fails to reach the minimum specified frequency. The specification for the Clock Monitor is as follows:

$1/t_c > 10$ kHz—No clock rejection.

$1/t_c < 10$ Hz—Guaranteed clock rejection.

WATCHDOG Operation (Continued)

WATCHDOG AND CLOCK MONITOR SUMMARY

The following salient points regarding the COP888EG WATCHDOG and CLOCK MONITOR should be noted:

- Both the WATCHDOG and CLOCK MONITOR detector circuits are inhibited during RESET.
- Following RESET, the WATCHDOG and CLOCK MONITOR are both enabled, with the WATCHDOG having he maximum service window selected.
- The WATCHDOG service window and CLOCK MONITOR enable/disable option can only be changed once, during the initial WATCHDOG service following RESET.
- The initial WATCHDOG service must match the key data value in the WATCHDOG Service register WDSVR in order to avoid a WATCHDOG error.
- Subsequent WATCHDOG services must match all three data fields in WDSVR in order to avoid WATCHDOG errors.
- The correct key data value cannot be read from the WATCHDOG Service register WDSVR. Any attempt to read this key data value of 01100 from WDSVR will read as key data value of all 0's.
- The WATCHDOG detector circuit is inhibited during both the HALT and IDLE modes.
- The CLOCK MONITOR detector circuit is active during both the HALT and IDLE modes. Consequently, the COP888 inadvertently entering the HALT mode will be detected as a CLOCK MONITOR error (provided that the CLOCK MONITOR enable option has been selected by the program).
- With the single-pin R/C oscillator mask option selected and the CLKDLY bit reset, the WATCHDOG service window will resume following HALT mode from where it left off before entering the HALT mode.
- With the crystal oscillator mask option selected, or with the single-pin R/C oscillator mask option selected and the CLKDLY bit set, the WATCHDOG service window will be set to its selected value from WDSVR following HALT. Consequently, the WATCHDOG should not be serviced for at least 2048 instruction cycles following HALT, but must be serviced within the selected window to avoid a WATCHDOG error.
- The IDLE timer T0 is not initialized with RESET.
- The user can sync in to the IDLE counter cycle with an IDLE counter (T0) interrupt or by monitoring the T0PND flag. The T0PND flag is set whenever the thirteenth bit of the IDLE counter toggles (every 4096 instruction cycles). The user is responsible for resetting the T0PND flag.
- A hardware WATCHDOG service occurs just as the device exits the IDLE mode. Consequently, the WATCHDOG should not be serviced for at least 2048 instruction cycles following IDLE, but must be serviced within the selected window to avoid a WATCHDOG error.
- Following RESET, the initial WATCHDOG service (where the service window and the CLOCK MONITOR enable/disable must be selected) may be programmed anywhere within the maximum service window (65,536 instruction cycles) initialized by RESET. Note that this initial WATCHDOG service may be programmed within the initial 2048 instruction cycles without causing a WATCHDOG error.

Detection of Illegal Conditions

The device can detect various illegal conditions resulting from coding errors, transient noise, power supply voltage drops, runaway programs, etc.

Reading of undefined ROM gets zeros. The opcode for software interrupt is zero. If the program fetches instructions from undefined ROM, this will force a software interrupt, thus signaling that an illegal condition has occurred.

The subroutine stack grows down for each call (jump to subroutine), interrupt, or PUSH, and grows up for each return or POP. The stack pointer is initialized to RAM location 06F Hex during reset. Consequently, if there are more returns than calls, the stack pointer will point to addresses 070 and 071 Hex (which are undefined RAM). Undefined RAM from addresses 070 to 07F (Segment 0), 140 to 17F (Segment 1), and all other segments (i.e., Segments 3 . . . etc.) is read as all 1's, which in turn will cause the program to return to address 7FFF Hex. This is an undefined ROM location and the instruction fetched (all 0's) from this location will generate a software interrupt signaling an illegal condition.

Thus, the chip can detect the following illegal conditions:

a. Executing from undefined ROM

b. Over "POP"ing the stack by having more returns than calls.

When the software interrupt occurs, the user can re-initialize the stack pointer and do a recovery procedure before restarting (this recovery program is probably similar to that following reset, but might not contain the same program initialization procedures). The recovery program should reset the software interrupt pending bit using the RPND instruction.

MICROWIRE/PLUS

MICROWIRE/PLUS is a serial synchronous communications interface. The MICROWIRE/PLUS capability enables the device to interface with any of National Semiconductor's MICROWIRE peripherals (i.e. A/D converters, display drivers, E^2PROMs etc.) and with other microcontrollers which support the MICROWIRE interface. It consists of an 8-bit serial shift register (SIO) with serial data input (SI), serial data output (SO) and serial shift clock (SK). *Figure 12* shows a block diagram of the MICROWIRE/PLUS logic.

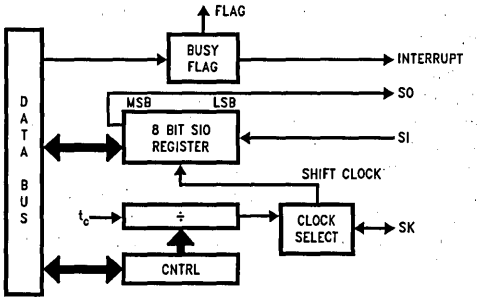

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FIGURE 16. MICROWIRE/PLUS Block Diagram

The shift clock can be selected from either an internal source or an external source. Operating the MICROWIRE/PLUS arrangement with the internal clock source is called the Master mode of operation. Similarly, operating the MICROWIRE/PLUS arrangement with an external shift clock is called the Slave mode of operation.

The CNTRL register is used to configure and control the MICROWIRE/PLUS mode. To use the MICROWIRE/PLUS, the MSEL bit in the CNTRL register is set to one. In the master mode, the SK clock rate is selected by the two bits, SL0 and SL1, in the CNTRL register. Table VI details the different clock rates that may be selected.

TABLE V. WATCHDOG Service Actions

Key Data	Window Data	Clock Monitor	Action
Match	Match	Match	Valid Service: Restart Service Window
Don't Care	Mismatch	Don't Care	Error: Generate WATCHDOG Output
Mismatch	Don't Care	Don't Care	Error: Generate WATCHDOG Output
Don't Care	Don't Care	Mismatch	Error: Generate WATCHDOG Output

TABLE VI. MICROWIRE/PLUS Master Mode Clock Select

SL1	SL0	SK
0	0	$2 \times t_c$
0	1	$4 \times t_c$
1	x	$8 \times t_c$

Where t_c is the instruction cycle clock

7

MICROWIRE/PLUS (Continued)

MICROWIRE/PLUS OPERATION

Setting the BUSY bit in the PSW register causes the MICROWIRE/PLUS to start shifting the data. It gets reset when eight data bits have been shifted. The user may reset the BUSY bit by software to allow less than 8 bits to shift. If enabled, an interrupt is generated when eight data bits have been shifted. The device may enter the MICROWIRE/PLUS mode either as a Master or as a Slave. *Figure 13* shows how two devices, microcontrollers and several peripherals may be interconnected using the MICROWIRE/PLUS arrangements.

Warning:

The SIO register should only be loaded when the SK clock is low. Loading the SIO register while the SK clock is high will result in undefined data in the SIO register. SK clock is normally low when not shifting.

Setting the BUSY flag when the input SK clock is high in the MICROWIRE/PLUS slave mode may cause the current SK clock forthe SIO shift register to be narrow. For safety, the BUSY flag should only be set when the input SK clock is low.

MICROWIRE/PLUS Master Mode Operation

In the MICROWIRE/PLUS Master mode of operation the shift clock (SK) is generated internally by the device. The MICROWIRE Master always initiates all data exchanges. The MSEL bit in the CNTRL register must be set to enable the SO and SK functions onto the G Port. The SO and SK pins must also be selected as outputs by setting appropriate bits in the Port G configuration register. Table VII summarizes the bit settings required for Master mode of operation.

MICROWIRE/PLUS Slave Mode Operation

In the MICROWIRE/PLUS Slave mode of operation the SK clock is generated by an external source. Setting the MSEL bit in the CNTRL register enables the SO and SK functions onto the G Port. The SK pin must be selected as an input and the SO pin is selected as an output pin by setting and resetting the appropriate bit in the Port G configuration register. Table VII summarizes the settings required to enter the Slave mode of operation.

The user must set the BUSY flag immediately upon entering the Slave mode. This will ensure that all data bits sent by the Master will be shifted properly. After eight clock pulses the BUSY flag will be cleared and the sequence may be repeated.

Alternate SK Phase Operation

The device allows either the normal SK clock or an alternate phase SK clock to shift data in and out of the SIO register. In both the modes the SK is normally low. In the normal mode data is shifted in on the rising edge of the SK clock and the data is shifted out on the falling edge of the SK clock. The SIO register is shifted on each falling edge of the SK clock. In the alternate SK phase operation, data is shifted in on the falling edge of the SK clock and shifted out on the rising edge of the SK clock.

A control flag, SKSEL, allows either the normal SK clock or the alternate SK clock to be selected. Resetting SKSEL causes the MICROWIRE/PLUS logic to be clocked from the normal SK signal. Setting the SKSEL flag selects the alternate SK clock. The SKSEL is mapped into the G6 configuration bit. The SKSEL flag will power up in the reset condition, selecting the normal SK signal.

TABLE VII

This table assumes that the control flag MSEL is set.

G4 (SO) Config. Bit	G5 (SK) Config. Bit	G4 Fun.	G5 Fun.	Operation
1	1	SO	Int. SK	MICROWIRE/PLUS Master
0	1	TRI-STATE	Int. SK	MICROWIRE/PLUS Master
1	0	SO	Ext. SK	MICROWIRE/PLUS Slave
0	0	TRI-STATE	Ext. SK	MICROWIRE/PLUS Slave

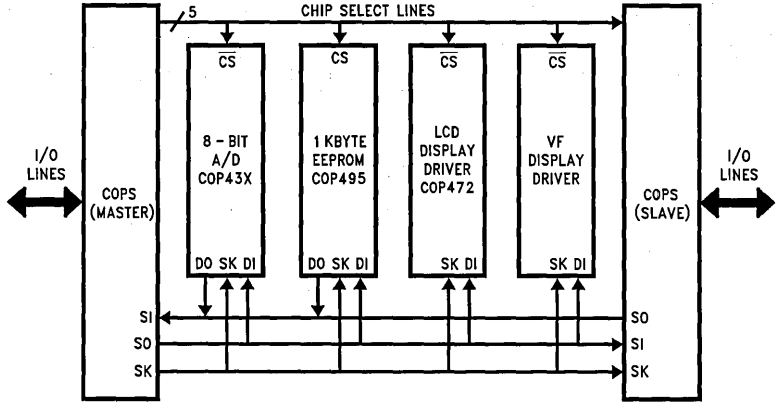

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FIGURE 17. MICROWIRE/PLUS Application

Memory Map

All RAM, ports and registers (except A and PC) are mapped into data memory address space.

Address S/ADD REG	Contents
0000 to 006F	On-Chip RAM bytes (112 bytes)
0070 to 007F	Unused RAM Address Space (Reads As All Ones)
xx80 to xxAF	Unused RAM Address Space (Reads Undefined Data)
xxB0	Timer T3 Lower Byte
XXB1	Timer T3 Upper Byte
xxB2	Timer T3 Autoload Register T3RA Lower Byte
xxB3	Timer T3 Autoload Register T3RA Upper Byte
xxB4	Timer T3 Autoload Register T3RB Lower Byte
xxB5	Timer T3 Autoload Register T3RB Upper Byte
xxB6	Timer T3 Control Register
xxB7	Comparator Select Register (CMPSL)
xxB8	UART Transmit Buffer (TBUF)
xxB9	UART Receive Buffer (RBUF)
xxBA	UART Control and Status Register (ENU)
xxBB	UART Receive Control and Status Register (ENUR)
xxBC	UART Interrupt and Clock Source Register (ENUI)
xxBD	UART Baud Register (BAUD)
xxBE	UART Prescale Select Register (PSR)
xxBF	Reserved for UART
xxC0	Timer T2 Lower Byte
xxC1	Timer T2 Upper Byte
xxC2	Timer T2 Autoload Register T2RA Lower Byte
xxC3	Timer T2 Autoload Register T2RA Upper Byte
xxC4	Timer T2 Autoload Register T2RB Lower Byte
xxC5	Timer T2 Autoload Register T2RB Upper Byte
xxC6	Timer T2 Control Register
xxC7	WATCHDOG Service Register (Reg:WDSVR)
xxC8	MIWU Edge Select Register (Reg:WKEDG)
xxC9	MIWU Enable Register (Reg:WKEN)
xxCA	MIWU Pending Register (Reg:WKPND)
xxCB	Reserved
xxCC	Reserved
xxCD to xxCF	Reserved

Address S/ADD REG	Contents
xxD0	Port L Data Register
xxD1	Port L Configuration Register
xxD2	Port L Input Pins (Read Only)
xxD3	Reserved for Port L
xxD4	Port G Data Register
xxD5	Port G Configuration Register
xxD6	Port G Input Pins (Read Only)
xxD7	Port I Input Pins (Read Only)
xxD8	Port C Data Register
xxD9	Port C Configuration Register
xxDA	Port C Input Pins (Read Only)
xxDB	Reserved for Port C
xxDC	Port D
xxDD to DF	Reserved for Port D
xxE0 to xxE5	Reserved for EE Control Registers
xxE6	Timer T1 Autoload Register T1RB Lower Byte
xxE7	Timer T1 Autoload Register T1RB Upper Byte
xxE8	ICNTRL Register
xxE9	MICROWIRE/PLUS Shift Register
xxEA	Timer T1 Lower Byte
xxEB	Timer T1 Upper Byte
xxEC	Timer T1 Autoload Register T1RA Lower Byte
xxED	Timer T1 Autoload Register T1RA Upper Byte
xxEE	CNTRL Control Register
xxEF	PSW Register
xxF0 to FB	On-Chip RAM Mapped as Registers
xxFC	X Register
xxFD	SP Register
xxFE	B Register
xxFF	S Register
0100–017F	On-Chip 128 RAM Bytes

Reading memory locations 0070H–007FH (Segment 0) will return all ones. Reading unused memory locations 0080H–00AFH (Segment 0) will return undefined data. Reading memory locations from other Segments (i.e., Segment 2, Segment 3, ... etc.) will return all ones.

Addressing Modes

There are ten addressing modes, six for operand addressing and four for transfer of control.

OPERAND ADDRESSING MODES

Register Indirect

This is the "normal" addressing mode. The operand is the data memory addressed by the B pointer or X pointer.

Register Indirect (with auto post increment or decrement of pointer)

This addressing mode is used with the LD and X instructions. The operand is the data memory addressed by the B pointer or X pointer. This is a register indirect mode that automatically post increments or decrements the B or X register after executing the instruction.

Direct

The instruction contains an 8-bit address field that directly points to the data memory for the operand.

Immediate

The instruction contains an 8-bit immediate field as the operand.

Short Immediate

This addressing mode is used with the Load B Immediate instruction. The instruction contains a 4-bit immediate field as the operand.

Indirect

This addressing mode is used with the LAID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a data operand from the program memory.

TRANSFER OF CONTROL ADDRESSING MODES

Relative

This mode is used for the JP instruction, with the instruction field being added to the program counter to get the new program location. JP has a range from −31 to +32 to allow a 1-byte relative jump (JP + 1 is implemented by a NOP instruction). There are no "pages" when using JP, since all 15 bits of PC are used.

Absolute

This mode is used with the JMP and JSR instructions, with the instruction field of 12 bits replacing the lower 12 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory segment.

Absolute Long

This mode is used with the JMPL and JSRL instructions, with the instruction field of 15 bits replacing the entire 15 bits of the program counter (PC). This allows jumping to any location in the current 4k program memory space.

Indirect

This mode is used with the JID instruction. The contents of the accumulator are used as a partial address (lower 8 bits of PC) for accessing a location in the program memory. The contents of this program memory location serve as a partial address (lower 8 bits of PC) for the jump to the next instruction.

Note: The VIS is a special case of the Indirect Transfer of Control addressing mode, where the double byte vector associated with the interrupt is transferred from adjacent addresses in the program memory into the program counter (PC) in order to jump to the associated interrupt service routine.

Instruction Set

Register and Symbol Definition

Registers	
A	8-Bit Accumulator Register
B	8-Bit Address Register
X	8-Bit Address Register
SP	8-Bit Stack Pointer Register
PC	15-Bit Program Counter Register
PU	Upper 7 Bits of PC
PL	Lower 8 Bits of PC
C	1 Bit of PSW Register for Carry
HC	1 Bit of PSW Register for Half Carry
GIE	1 Bit of PSW Register for Global Interrupt Enable
VU	Interrupt Vector Upper Byte
VL	Interrupt Vector Lower Byte

Symbols	
[B]	Memory Indirectly Addressed by B Register
[X]	Memory Indirectly Addressed by X Register
MD	Direct Addressed Memory
Mem	Direct Addressed Memory or [B]
Meml	Direct Addressed Memory or [B] or Immediate Data
Imm	8-Bit Immediate Data
Reg	Register Memory: Addresses F0 to FF (Includes B, X and SP)
Bit	Bit Number (0 to 7)
←	Loaded with
↔	Exchanged with

Instruction Set (Continued)

INSTRUCTION SET

ADD	A,Meml	ADD	A ← A + Meml
ADC	A,Meml	ADD with Carry	A ← A + Meml + C, C ← Carry HC ← Half Carry
SUBC	A,Meml	Subtract with Carry	A ← A − $\overline{\text{Meml}}$ + C, C ← Carry HC ← Half Carry
AND	A,Meml	Logical AND	A ← A and Meml
ANDSZ	A,Imm	Logical AND Immed., Skip if Zero	Skip next if (A and Imm) = 0
OR	A,Meml	Logical OR	A ← A or Meml
XOR	A,Meml	Logical EXclusive OR	A ← A xor Meml
IFEQ	MD,Imm	IF EQual	Compare MD and Imm, Do next if MD = Imm
IFEQ	A,Meml	IF EQual	Compare A and Meml, Do next if A = Meml
IFNE	A,Meml	IF Not Equal	Compare A and Meml, Do next if A ≠ Meml
IFGT	A,Meml	IF Greater Than	Compare A and Meml, Do next if A > Meml
IFBNE	#	If B Not Equal	Do next if lower 4 bits of B ≠ Imm
DRSZ	Reg	Decrement Reg., Skip if Zero	Reg ← Reg − 1, Skip if Reg = 0
SBIT	#,Mem	Set BIT	1 to bit, Mem (bit = 0 to 7 immediate)
RBIT	#,Mem	Reset BIT	0 to bit, Mem
IFBIT	#,Mem	IF BIT	If bit in A or Mem is true do next instruction
RPND		Reset PeNDing Flag	Reset Software Interrupt Pending Flag
X	A,Mem	EXchange A with Memory	A ⟷ Mem
X	A,[X]	EXchange A with Memory [X]	A ⟷ [X]
LD	A,Meml	LoaD A with Memory	A ← Meml
LD	A,[X]	LoaD A with Memory [X]	A ← [X]
LD	B,Imm	LoaD B with Immed.	B ← Imm
LD	Mem,Imm	LoaD Memory Immed	Mem ← Imm
LD	Reg,Imm	LoaD Register Memory Immed.	Reg ← Imm
X	A, [B ±]	EXchange A with Memory [B]	A ⟷ [B], (B ← B ±1)
X	A, [X ±]	EXchange A with Memory [X]	A ⟷ [X], (X ← ±1)
LD	A, [B±]	LoaD A with Memory [B]	A ← [B], (B ← B ±1)
LD	A, [X±]	LoaD A with Memory [X]	A ← [X], (X ← X±1)
LD	[B±],Imm	LoaD Memory [B] Immed.	[B] ← Imm, (B ← B±1)
CLR	A	CLeaR A	A ← 0
INC	A	INCrement A	A ← A + 1
DEC	A	DECrementA	A ← A − 1
LAID		Load A InDirect from ROM	A ← ROM (PU,A)
DCOR	A	Decimal CORrect A	A ← BCD correction of A (follows ADC, SUBC)
RRC	A	Rotate A Right thru C	C → A7 → . . . → A0 → C
RLC	A	Rotate A Left thru C	C ← A7 ← . . . ← A0 ← C
SWAP	A	SWAP nibbles of A	A7 . . . A4 ⟷ A3 . . . A0
SC		Set C	C ← 1, HC ← 1
RC		Reset C	C ← 0, HC ← 0
IFC		IF C	IF C is true, do next instruction
IFNC		IF Not C	If C is not true, do next instruction
POP	A	POP the stack into A	SP ← SP + 1, A ← [SP]
PUSH	A	PUSH A onto the stack	[SP] ← A, SP ← SP − 1
VIS		Vector to Interrupt Service Routine	PU ← [VU], PL ← [VL]
JMPL	Addr.	Jump absolute Long	PC ← ii (ii = 15 bits, 0 to 32k)
JMP	Addr.	Jump absolute	PC9 . . . 0 ← i (i = 12 bits)
JP	Disp.	Jump relative short	PC ← PC + r (r is −31 to +32, except 1)
JSRL	Addr.	Jump SubRoutine Long	[SP] ← PL, [SP−1] ← PU,SP−2, PC ← ii
JSR	Addr	Jump SubRoutine	[SP] ← PL, [SP−1] ← PU,SP−2, PC9 . . . 0 ← i
JID		Jump InDirect	PL ← ROM (PU,A)
RET		RETurn from subroutine	SP + 2, PL ← [SP], PU ← [SP−1]
RETSK		RETurn and SKip	SP + 2, PL ← [SP],PU ← [SP−1]
RETI		RETurn from Interrupt	SP + 2, PL ← [SP],PU ← [SP−1],GIE ← 1
INTR		Generate an Interrupt	[SP] ← PL, [SP−1] ← PU, SP−2, PC ← 0FF
NOP		No OPeration	PC ← PC + 1

Instruction Execution Time

Most instructions are single byte (with immediate addressing mode instructions taking two bytes).

Most single byte instructions take one cycle time to execute.

See the BYTES and CYCLES per INSTRUCTION table for details.

Bytes and Cycles per Instruction

The following table shows the number of bytes and cycles for each instruction in the format of byte/cycle.

	[B]	Direct	Immed.
ADD	1/1	3/4	2/2
ADC	1/1	3/4	2/2
SUBC	1/1	3/4	2/2
AND	1/1	3/4	2/2
OR	1/1	3/4	2/2
XOR	1/1	3/4	2/2
IFEQ	1/1	3/4	2/2
IFNE	1/1	3/4	2/2
IFGT	1/1	3/4	2/2
IFBNE	1/1		
DRSZ		1/3	
SBIT	1/1	3/4	
RBIT	1/1	3/4	
IFBIT	1/1	3/4	

RPND	1/1

Instructions Using A & C

CLRA	1/1
INCA	1/1
DECA	1/1
LAID	1/3
DCOR	1/1
RRCA	1/1
RLCA	1/1
SWAPA	1/1
SC	1/1
RC	1/1
IFC	1/1
IFNC	1/1
PUSHA	1/3
POPA	1/3
ANDSZ	2/2

Transfer of Control Instructions

JMPL	3/4
JMP	2/3
JP	1/3
JSRL	3/5
JSR	2/5
JID	1/3
VIS	1/5
RET	1/5
RETSK	1/5
RETI	1/5
INTR	1/7
NOP	1/1

Memory Transfer Instructions

	Register Indirect		Direct	Immed.	Register Indirect Auto Incr. & Decr.		
	[B]	[X]			[B+, B−]	[X+, X−]	
X A,*	1/1	1/3	2/3		1/2	1/3	
LD A,*	1/1	1/3	2/3	2/2	1/2	1/3	
LD B, Imm				1/1			(IF B < 16)
LD B, Imm				2/2			(IF B > 15)
LD Mem, Imm	2/2		3/3		2/2		
LD Reg, Imm			2/3				
IFEQ MD, Imm			3/3				

* = > Memory location addressed by B or X or directly.

Opcode Table

Upper Nibble Along X-Axis
Lower Nibble Along Y-Axis

F	E	D	C	B	A	9	8	
JP −15	JP −31	LD 0F0, # i	DRSZ 0F0	RRCA	RC	ADC A,#i	ADC A,[B]	0
JP −14	JP −30	LD 0F1, # i	DRSZ 0F1	*	SC	SUBC A, #i	SUB A,[B]	1
JP −13	JP −29	LD 0F2, # i	DRSZ 0F2	X A, [X+]	X A,[B+]	IFEQ A,#i	IFEQ A,[B]	2
JP −12	JP −28	LD 0F3, # i	DRSZ 0F3	X A, [X−]	X A,[B−]	IFGT A,#i	IFGT A,[B]	3
JP −11	JP −27	LD 0F4, # i	DRSZ 0F4	VIS	LAID	ADD A,#i	ADD A,[B]	4
JP −10	JP −26	LD 0F5, # i	DRSZ 0F5	RPND	JID	AND A,#i	AND A,[B]	5
JP −9	JP −25	LD 0F6, # i	DRSZ 0F6	X A,[X]	X A,[B]	XOR A,#i	XOR A,[B]	6
JP −8	JP −24	LD 0F7, # i	DRSZ 0F7	*	*	OR A,#i	OR A,[B]	7
JP −7	JP −23	LD 0F8, # i	DRSZ 0F8	NOP	RLCA	LD A,#i	IFC	8
JP −6	JP −22	LD 0F9, # i	DRSZ 0F9	IFNE A,[B]	IFEQ Md,#i	IFNE A,#i	IFNC	9
JP −5	JP −21	LD 0FA, # i	DRSZ 0FA	LD A,[X+]	LD A,[B+]	LD [B+],#i	INCA	A
JP −4	JP −20	LD 0FB, # i	DRSZ 0FB	LD A,[X−]	LD A,[B−]	LD [B−],#i	DECA	B
JP −3	JP −19	LD 0FC, # i	DRSZ 0FC	LD Md,#i	JMPL	X A,Md	POPA	C
JP −2	JP −18	LD 0FD, # i	DRSZ 0FD	DIR	JSRL	LD A,Md	RETSK	D
JP −1	JP −17	LD 0FE, # i	DRSZ 0FE	LD A,[X]	LD A,[B]	LD [B],#i	RET	E
JP −0	JP −16	LD 0FF, # i	DRSZ 0FF	*	*	LD B,#i	RETI	F

Opcode Table (Continued)

Upper Nibble Along X-Axis

Lower Nibble Along Y-Axis

7	6	5	4	3	2	1	0	
IFBIT 0,[B]	ANDSZ A, #i	LD B,#0F	IFBNE 0	JSR x000–x0FF	JMP x000–x0FF	JP +17	INTR	0
IFBIT 1,[B]	*	LD B,#0E	IFBNE 1	JSR x100–x1FF	JMP x100–x1FF	JP +18	JP + 2	1
IFBIT 2,[B]	*	LD B,#0D	IFBNE 2	JSR x200–x2FF	JMP x200–x2FF	JP +19	JP + 3	2
IFBIT 3,[B]	*	LD B,#0C	IFBNE 3	JSR x300–x3FF	JMP x300–x3FF	JP +20	JP + 4	3
IFBIT 4,[B]	CLRA	LD B,#0B	IFBNE 4	JSR x400–x4FF	JMP x400–x4FF	JP +21	JP + 5	4
IFBIT 5,[B]	SWAPA	LD B,#0A	IFBNE 5	JSR x500–x5FF	JMP x500–x5FF	JP +22	JP + 6	5
IFBIT 6,[B]	DCORA	LD B,#09	IFBNE 6	JSR x600–x6FF	JMP x600–x6FF	JP +23	JP + 7	6
IFBIT 7,[B]	PUSHA	LD B,#08	IFBNE 7	JSR x700–x7FF	JMP x700–x7FF	JP +24	JP + 8	7
SBIT 0,[B]	RBIT 0,[B]	LD B,#07	IFBNE 8	JSR x800–x8FF	JMP x800–x8FF	JP +25	JP + 9	8
SBIT 1,[B]	RBIT 1,[B]	LD B,#06	IFBNE 9	JSR x900–x9FF	JMP x900–x9FF	JP +26	JP + 10	9
SBIT 2,[B]	RBIT 2,[B]	LD B,#05	IFBNE 0A	JSR xA00–xAFF	JMP xA00–xAFF	JP +27	JP + 11	A
SBIT 3,[B]	RBIT 3,[B]	LD B,#04	IFBNE 0B	JSR xB00–xBFF	JMP xB00–xBFF	JP +28	JP + 12	B
SBIT 4,[B]	RBIT 4,[B]	LD B,#03	IFBNE 0C	JSR xC00–xCFF	JMP xC00–xCFF	JP +29	JP + 13	C
SBIT 5,[B]	RBIT 5,[B]	LD B,#02	IFBNE 0D	JSR xD00–xDFF	JMP xD00–xDFF	JP +30	JP + 14	D
SBIT 6,[B]	RBIT 6,[B]	LD B,#01	IFBNE 0E	JSR xE00–xEFF	JMP xE00–xEFF	JP +31	JP + 15	E
SBIT 7,[B]	RBIT 7,[B]	LD B,#00	IFBNE 0F	JSR xF00–xFFF	JMP xF00–xFFF	JP +32	JP + 16	F

Where,

i is the immediate data
Md is a directly addressed memory location
* is an unused opcode

Note: The opcode 60 Hex is also the opcode for IFBIT #i,A

Mask Options

The mask programmable options are shown below. The options are programmed at the same time as the ROM pattern submission.

```
OPTION 1: CLOCK CONFIGURATION
  = 1     Crystal Oscillator (CKI/10)
              G7 (CKO) is clock generator
              output to crystal/resonator
              CKI is the clock input
  = 2     Single-pin RC controlled
              oscillator (CKI/10)
              G7 is available as a HALT
              restart and/or general purpose
              input
OPTION 2: HALT
  = 1     Enable HALT mode
  = 2     Disable HALT mode
OPTION 3: BONDING OPTIONS
  = 1     44-Pin PLCC
  = 2     40-Pin DIP
  = 3     N/A
  = 4     28-Pin DIP
  = 5     28-Pin SO
```

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (if clock option-1 has been selected). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_C$).

Development Support

IN-CIRCUIT EMULATOR

The MetaLink iceMASTER™-COP8 Model 400 In-Circuit Emulator for the COP8 family of microcontrollers features high-performance operation, ease of use, and an extremely flexible user-interface or maximum productivity. Interchangeable probe cards, which connect to the standard common base, support the various configurations and packages of the COP8 family.

The iceMASTER provides real time, full speed emulation up to 10 MHz, 32 kBytes of emulation memory and 4k frames of trace buffer memory. The user may define as many as 32k trace and break triggers which can be enabled, disabled, set or cleared. They can be simple triggers based on code or address ranges or complex triggers based on code address, direct address, opcode value, opcode class or immediate operand. Complex breakpoints can be ANDed and ORed together. Trace information consists of address bus values, opcodes and user selectable probe clips status (external event lines). The trace buffer can be viewed as raw hex or as disassembled instructions. The probe clip bit values can be displayed in binary, hex or digital waveform formats.

During single-step operation the dynamically annotated code feature displays the contents of all accessed (read and write) memory locations and registers, as well as flow-of-control direction change markers next to each instruction executed.

The iceMASTER's performance analyzer offers a resolution of better than 6 μs. The user can easily monitor the time spent executing specific portions of code and find "hot spots" or "dead code". Up to 15 independent memory areas based on code address or label ranges can be defined. Analysis results can be viewed in bar graph format or as actual frequency count.

Emulator memory operations for program memory include single line assembler, disassembler, view, change and write to file. Data memory operations include fill, move, compare, dump to file, examine and modify. The contents of any memory space can be directly viewed and modified from the corresponding window.

The iceMASTER comes with an easy to use window interface. Each window can be sized, highlighted, color-controlled, added, or removed completely. Commands can be accessed via pull-down-menus and/or redefinable hot keys. A context sensitive hypertext/hyperlinked on-line help system explains clearly the options the user has from within any window.

The iceMASTER connects easily to a PC® via the standard COMM port and its 115.2 kBaud serial link keeps typical program download time to under 3 seconds.

The following tables list the emulator and probe cards ordering information.

Emulator Ordering Information

Part Number	Description
IM-COP8/400	MetaLink base unit in-circuit emulator for all COP8 devices, symbolic debugger software and RS-232 serial interface cable
MHW-PS3	Power supply 110V/60 MHz
MHW-PS4	Power supply 220V/50 Hz

Probe Card Ordering Information

Part Number	Package	Voltage Range	Emulates
MHW-884EG28D5PC	28 DIP	4.5V–5.5V	COP884EG
MHW-884EG28DWPC	28 DIP	2.5V–6.0V	COP884EG
MHW-888EG40D5PC	40 DIP	4.5V–5.5V	COP888EG
MHW-888EG40DWPC	40 DIP	2.5V–6.0V	COP888EG
MWH-888EG44D5PC	44 PLCC	4.5V–5.5V	COP888EG
MHW-888EG44DWPC	44 PLCC	2.5V–6.0V	COP888EG

MACRO CROSS ASSEMBLER

National Semiconductor offers a COP8 macro cross assembler. It runs on industry standard compatible PCs and supports all of the full-symbolic debugging features of the MetaLink iceMASTER emulators.

Assembler Ordering Information

Part Number	Description	Manual
MOLE-COP8-IBM	COP8 macro cross assembler for IBM®, PC-/XT®, PC-AT® or compatible	424410527-001

Development Support (Continued)

SINGLE CHIP EMULATOR DEVICE

The COP8 family is fully supported by single chip form, fit and function emulators. For more detailed information refer to the emulation device specific datasheets and the form, fit, function emulator selection table below.

PROGRAMMING SUPPORT

Programming of the single chip emulator devices is supported by different sources. National Semiconductor offers a duplicator board which allows the transfer of program code from a standard programmed EPROM to the single chip emulator and vice versa. Data I/O supports COP8 emulator device programming with its uniSite 48 and System 2900 programmers. Further information on Data I/O programmers can be obtained from any Data I/O sales office or the following USA numbers:

Telephone: (206) 881-6444 Fax: (206) 882-1043

Single Chip Emulator Selection Table

Device Number	Clock Option	Package	Description	Emulates
COP888EGMHEL-X	X = 1: crystal X = 3: R/C	44 LDCC	Multi-Chip Module (MCM), UV erasable	COP888EG
COP888EGMHD-X	X = 1: crystal X = 3: R/C	40 DIP	MCM, UV erasable	COP888EG

Duplicator Board Ordering Information

Part Number	Description	Devices Supported
COP8-SCRM-DIP	MCM Scrambler Board for 40 DIP socket	COP888EGMHD
COP8-SCRM-PCC	MCM Scrambler Board for 44 PLCC/ LDCC	COP888EGMHEL
COP8-PRGM-DIP	Duplicator Board with COP8-SCRM-DIP scrambler board	COP888EGMHD
COP8-PRGM-PCC	Duplicator Board with COP8-SCRM-PCC scrambler board	COP888EGMEL

Development Support (Continued)

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications group. The Dial-A-Helper is an Electronic Bulletin Board Information system.

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down loaded to disk for later use.

ORDER P/N: MOLE-DIAL-A-HLP

Information System Package contains:
- Dial-A-Helper Users Manual
- Public Domain Communications Software

FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factor applications support. If a user has questions, he can leave messages on our electronic bulletin board, which we will respond to.

Voice: (408) 721-5582
Modem: (408) 739-1162
Baud: 300 or 1200 Baud
Set-up: Length: 8-Bit
Parity: None
Stop Bit: 1
Operation: 24 Hrs., 7 Days

Section 8

Physical Dimensions

Section 8 Contents

National Semiconductor

Ordering Information for Low Voltage Logic (LVQ)

The device number is used to form part of a simplified purchasing code where a package type and temperature range is defined as follows:

74LVQ XXX S C QR

- 74LVQ — Temperature Range Family
  - 74LVQ = Commercial
  - 54LVQ = Military
- XXX — Device Type
- S — Package Code
  - D = Ceramic DIP
  - F = Flatpak
  - L = Ceramic Leadless Chip Carrier (LCC)
  - S = Small Outline Package (SOIC)
  - QS = Small Outline Package (0.150" Wide QSOP)
- C — Temperature Range
  - C = Commercial (−40°C to +85°C)
  - M = Military (−55°C to +125°C)
- QR — Special Variations
  - X = Device shipped in 13" reels
  - QR = Commercial grade device with burn-in
  - QB = Military grade device with environmental and burn-in processing shipped in tubes

Ordering Information for Low Voltage CMOS SRAMs

NM S xxx X x EV M 15

- NM — NSC Memory
- S — SRAMs
- xxx X x — Organization
  - i.e. 64 x 4 = 16k x 4
  - 64 x 8 = 8k x 8
  - 1024 x 8 = 128k x 8
- 15 — Access Time (ns)
  - 15
  - 20
  - 25
  - 30
  - 35
- M — Package Code
  - M = 300-mil Plastic SOJ
  - N = 300-mil Plastic DIP
- EV — Low Voltage Designator
  - LV = Low Voltage, V_{CC} = 3.3V
  - EV = Extended Voltage, V_{CC} = 3.0V–5.5V

Example: NMS64X8EVN20 = 8k x 8 CMOS SRAM, V_{CC} = 3.0V–5.5V, 300-mil Plastic DIP, 20 ns.

Ordering Information for Clock Generation and Support (CGS)

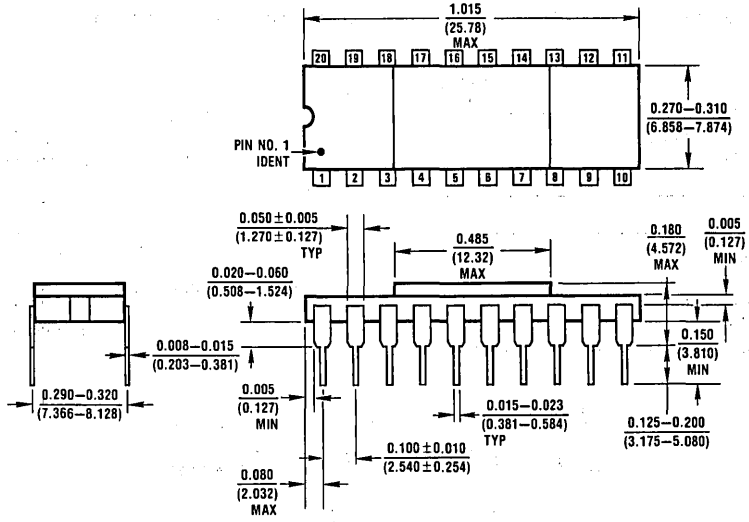
CGS 74 C 2525 N

- CGS — Clock Generation and Support
- 74 — Operating Temperature Range
  - 54 = Military
  - 74 = Commercial
- C — Technology
  - C = CMOS
- 2525 — Device Type
- N — Package Code
  - M = S.O.I.C. (JEDEC Standard)
  - N = Plastic DIP

National Semiconductor

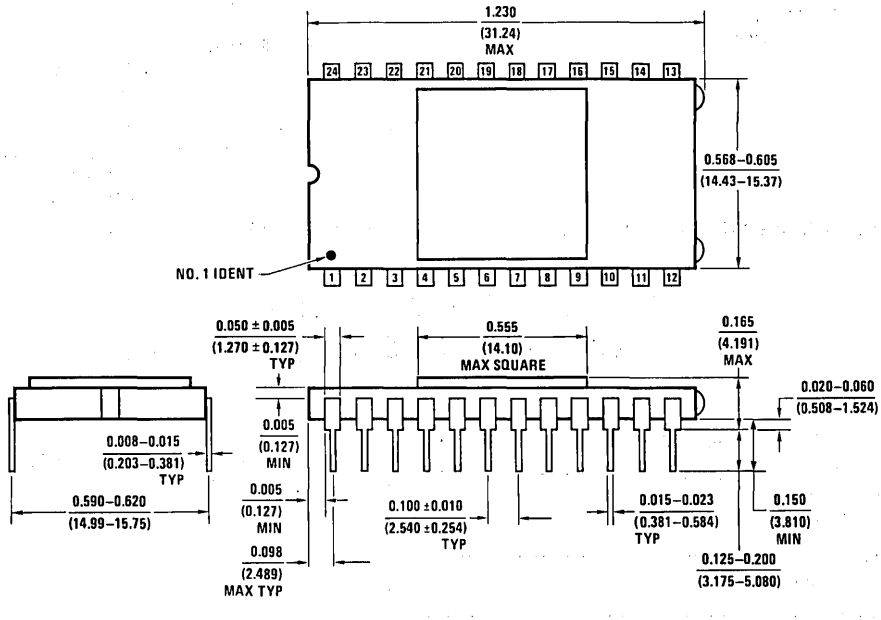
All dimensions are in inches (millimeters)

20 Lead Hermetic Dual-In-Line Package
NS Package Number D20A



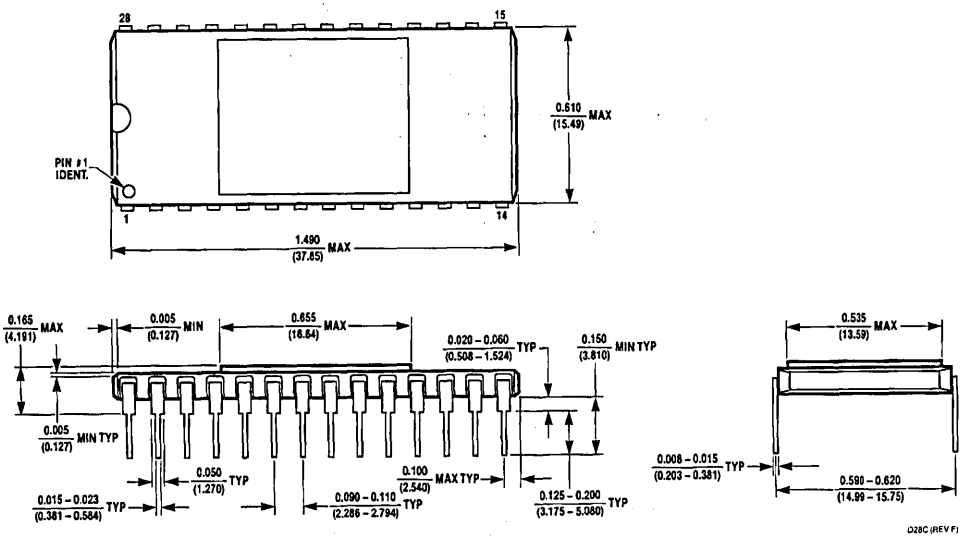
D20A (REV D)

24 Lead Hermetic Dual-In-Line Package
NS Package Number D24C



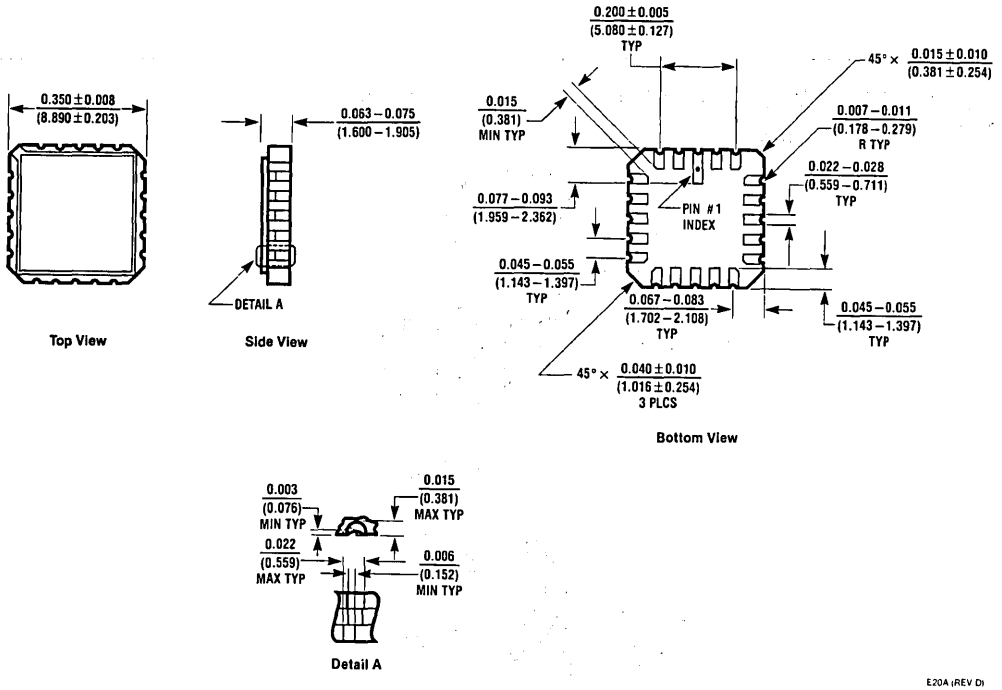
D24C (REV G)

28 Lead Hermetic Dual-In-Line Package
NS Package Number D28C



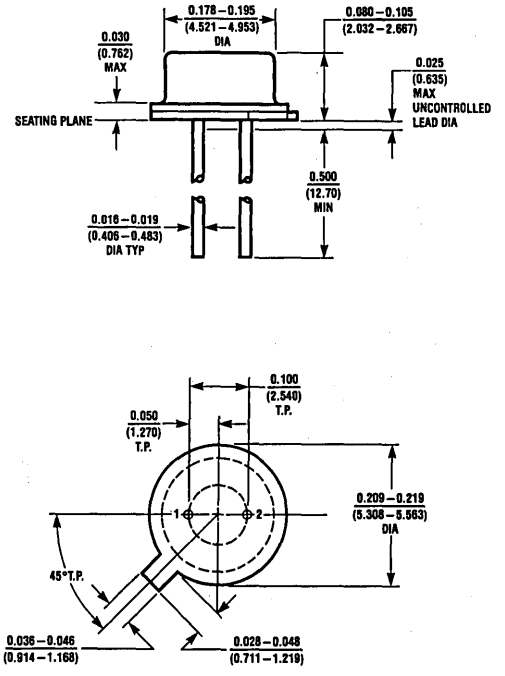
D28C (REV F)

20 Terminal Ceramic Leadless Chip Carrier
NS Package Number E20A



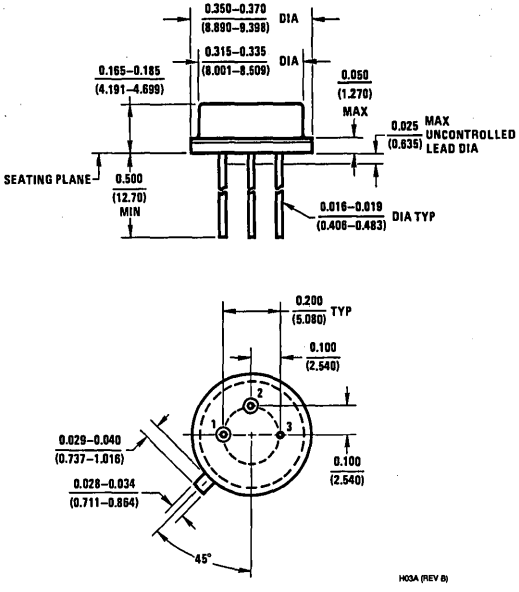
E20A (REV D)

2 Lead (0.100″ Diameter P.C.) TO-46 Metal Can Package
NS Package Number H02A



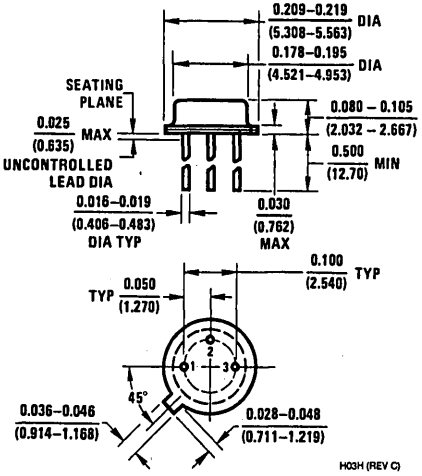
H02A (REV C)

3 Lead (0.200″ Diameter P.C.) Metal Can Package
NS Package Number H03A

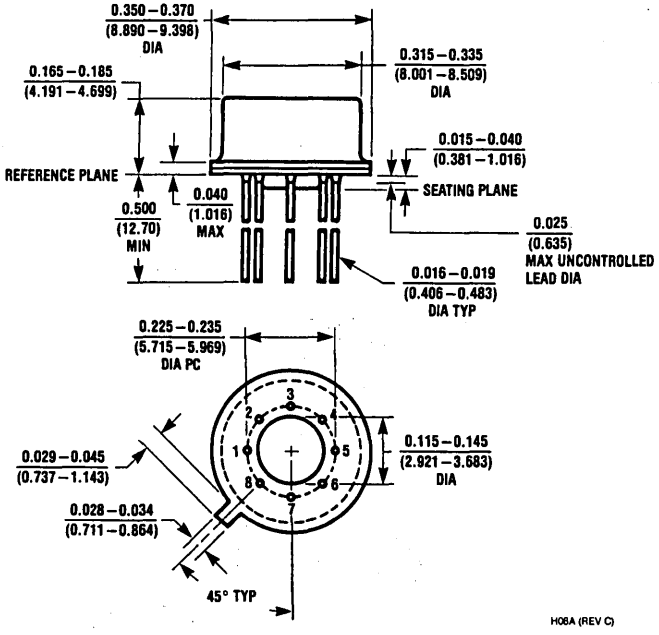


H03A (REV B)

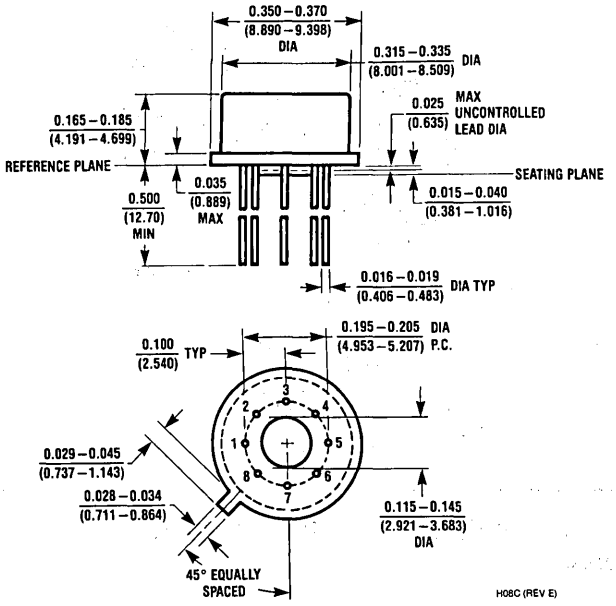
3 Lead (0.100" Diameter P.C.) TO-46 Metal Can Package
NS Package Number H03H



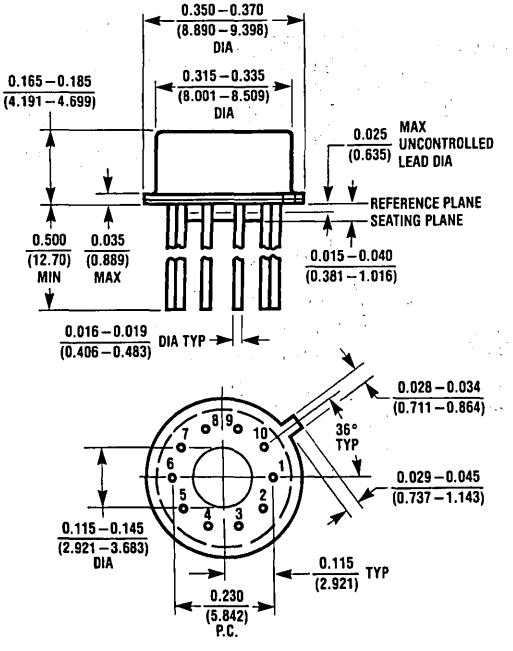
8 Lead (0.230" Diameter P.C.) Metal Can Package
NS Package Number H08A



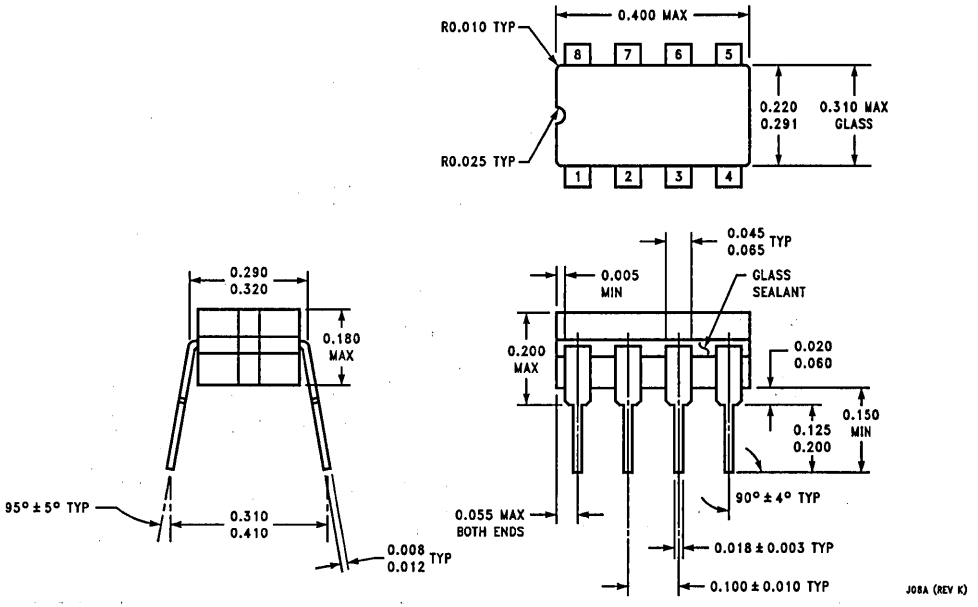
8 Lead (0.200" Diameter P.C.) TO-99 Metal Can Package
NS Package Number H08C



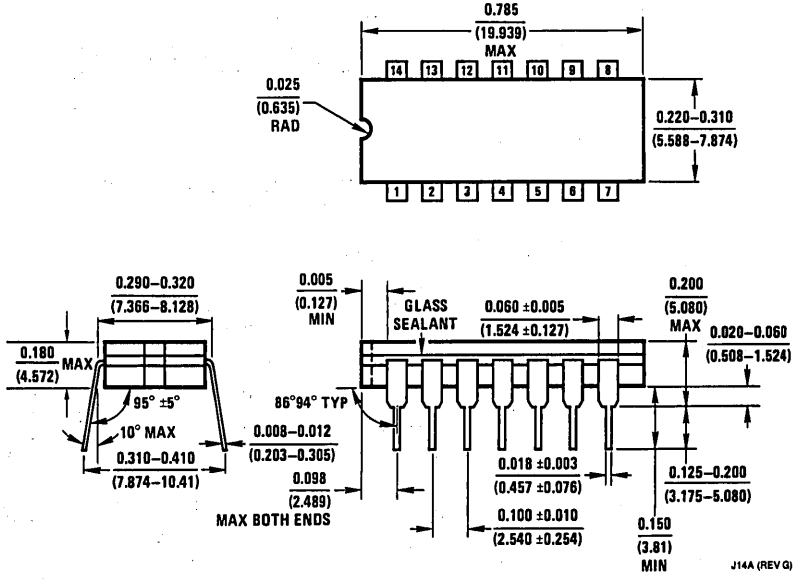
10 Lead (0.230" Diameter P.C.) TO-100 Metal Can Package
NS Package Number H10C



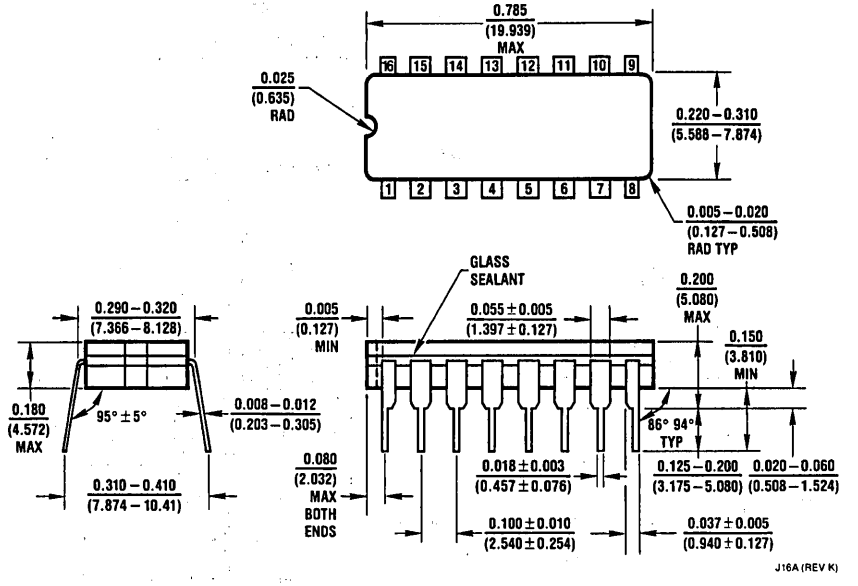
8 Narrow Lead Ceramic Dual-In-Line Package
NS Package Number J08A



14 Lead Ceramic Dual-In-Line Package
NS Package Number J14A

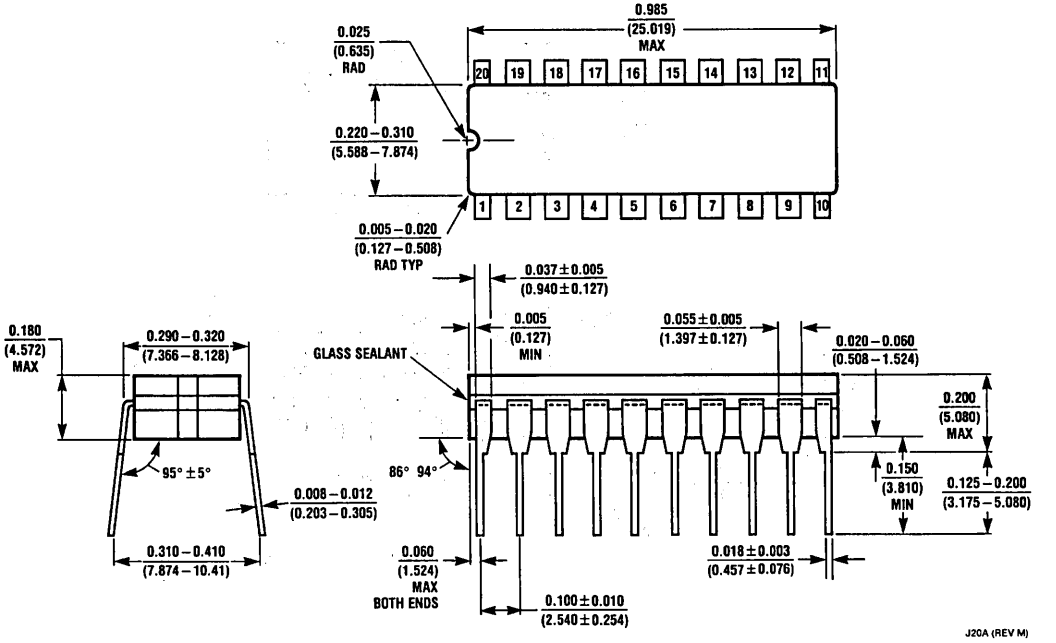


16 Lead Ceramic Dual-In-Line Package
NS Package Number J16A



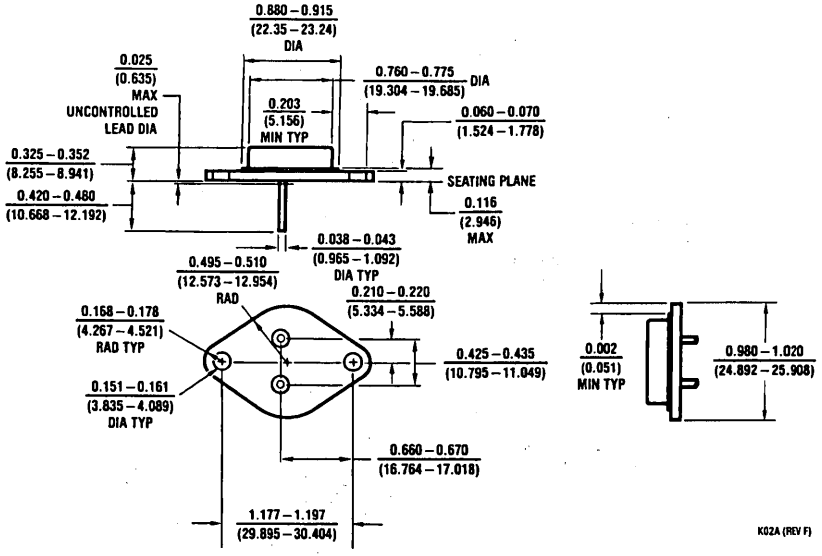
J16A (REV K)

20 Lead Ceramic Dual-In-Line Package
NS Package Number J20A

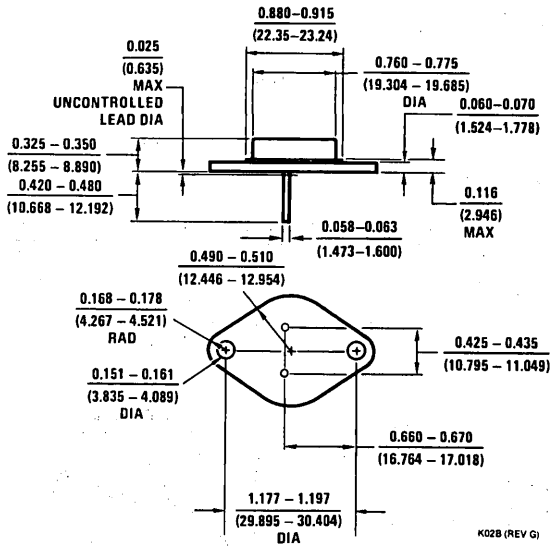


J20A (REV M)

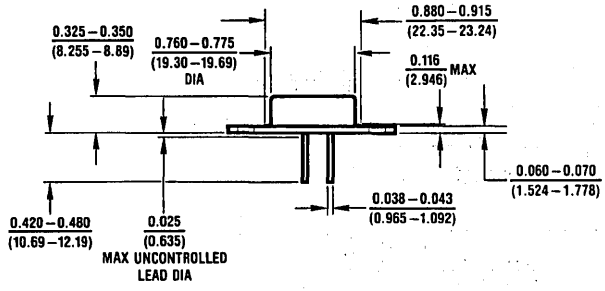
2 Lead TO-3 Metal Can Package
NS Package Number K02A

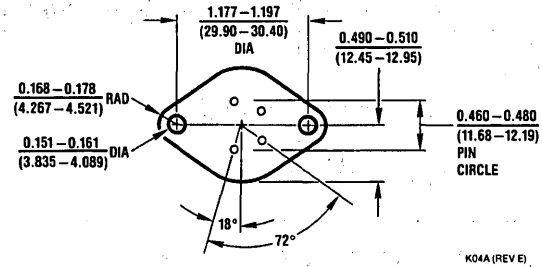


2 Lead (.060 Diameter) TO-3 Metal Can Package
NS Package Number K02B



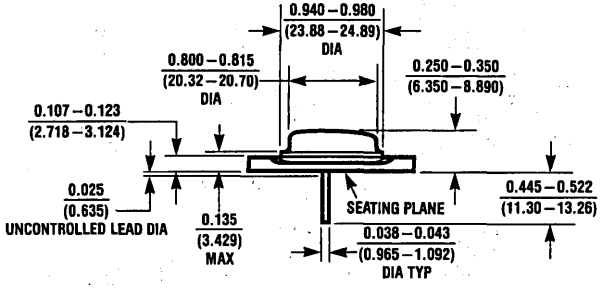
4 Lead TO-3 Metal Can Package
NS Package Number K04A

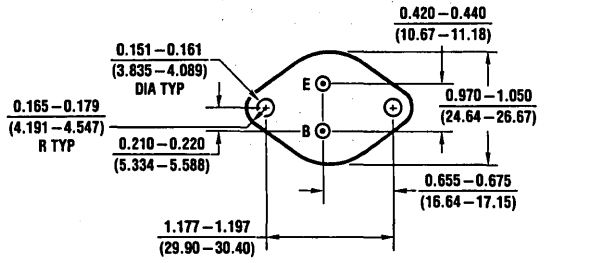




K04A (REV E)

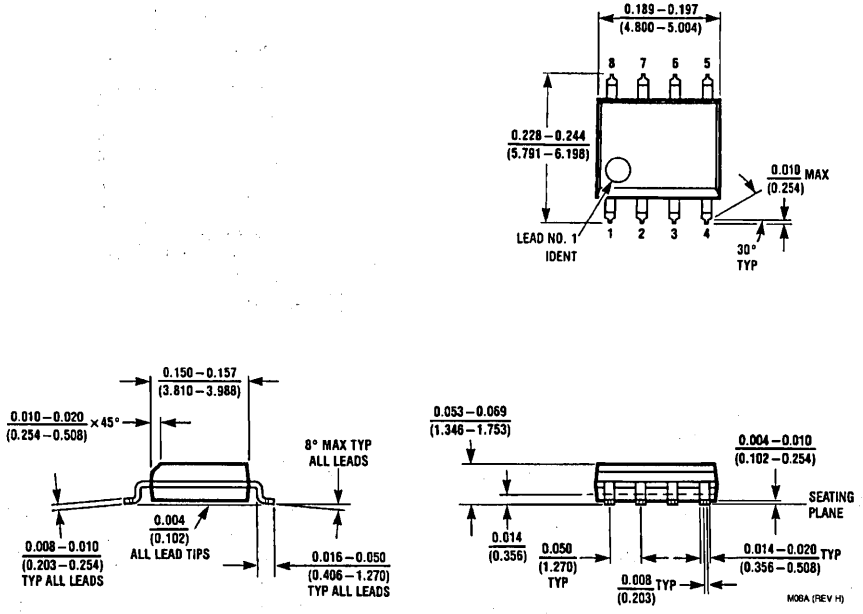
2 Lead TO-3 Aluminum Metal Can Package
NS Package Number KC02A



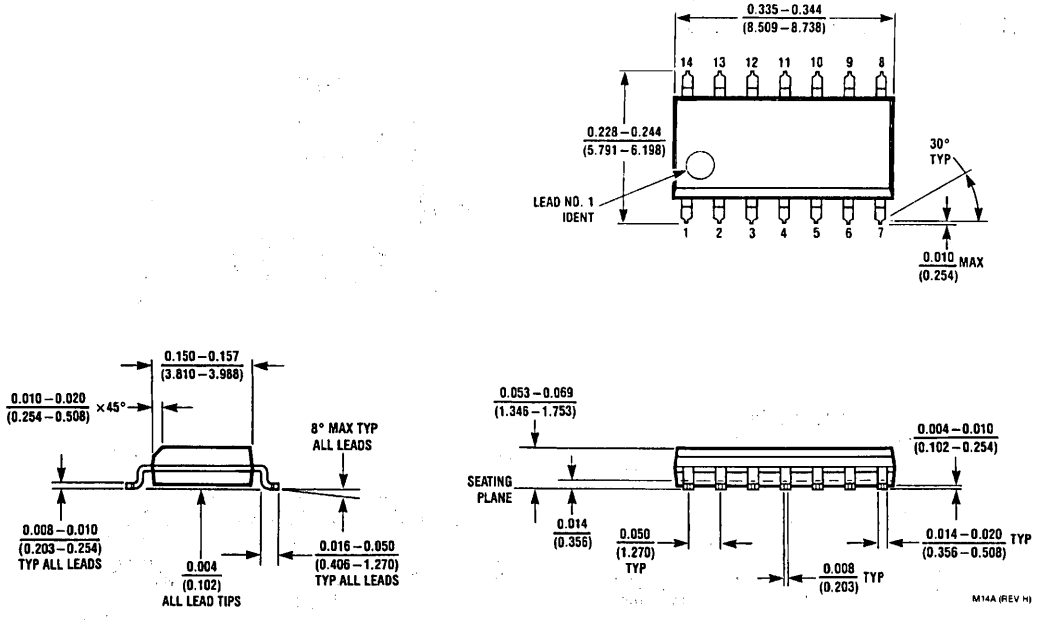


KC02A (REV C)

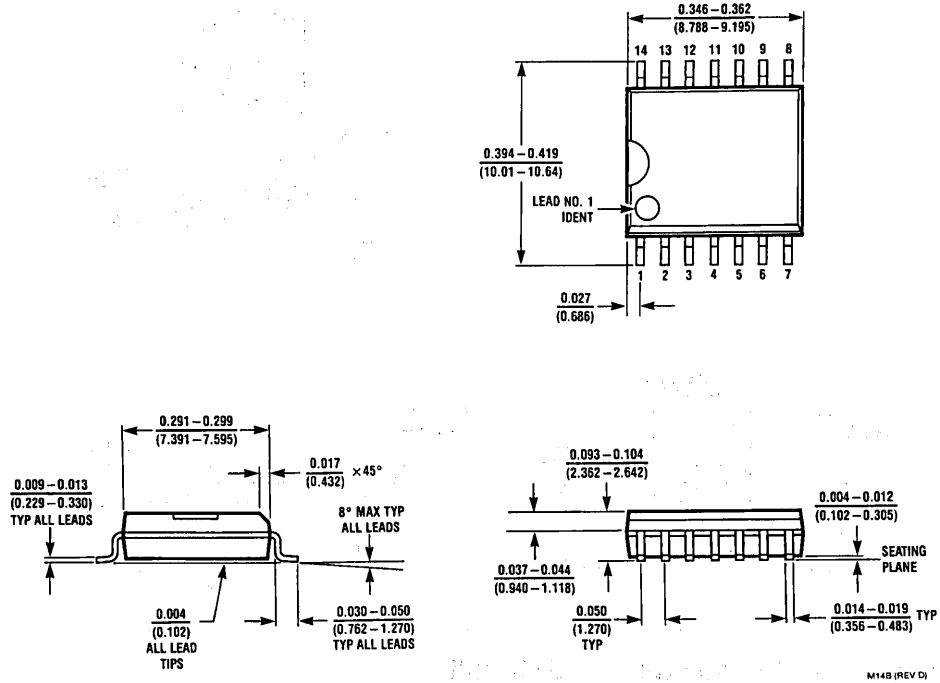
8 Lead (0.150" Wide) Small Outline Integrated Circuit
NS Package Number M08A



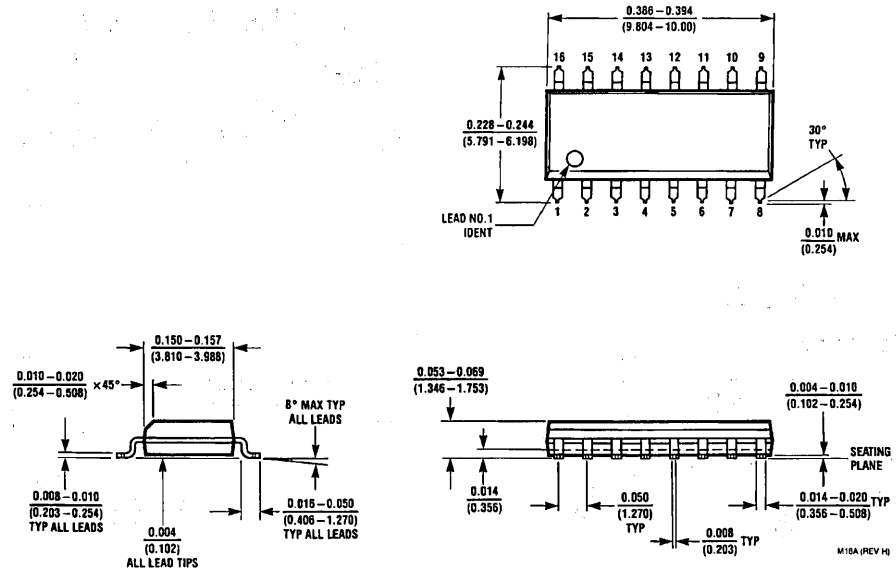
14 Lead Small Outline Integrated Circuit
NS Package Number M14A



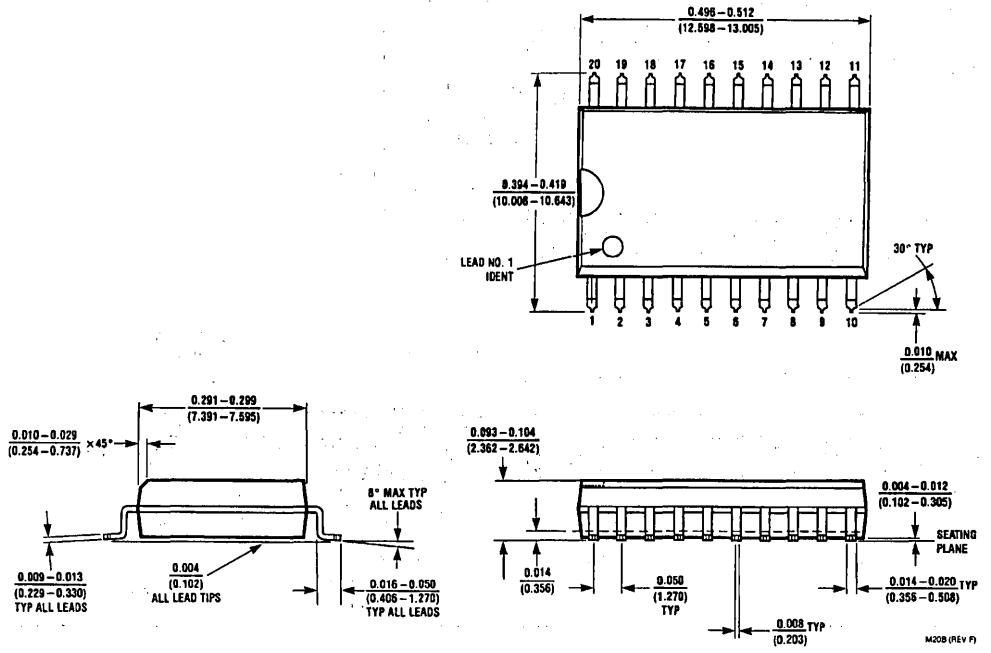
14 Lead Small Outline Integrated Circuit
NS Package Number M14B



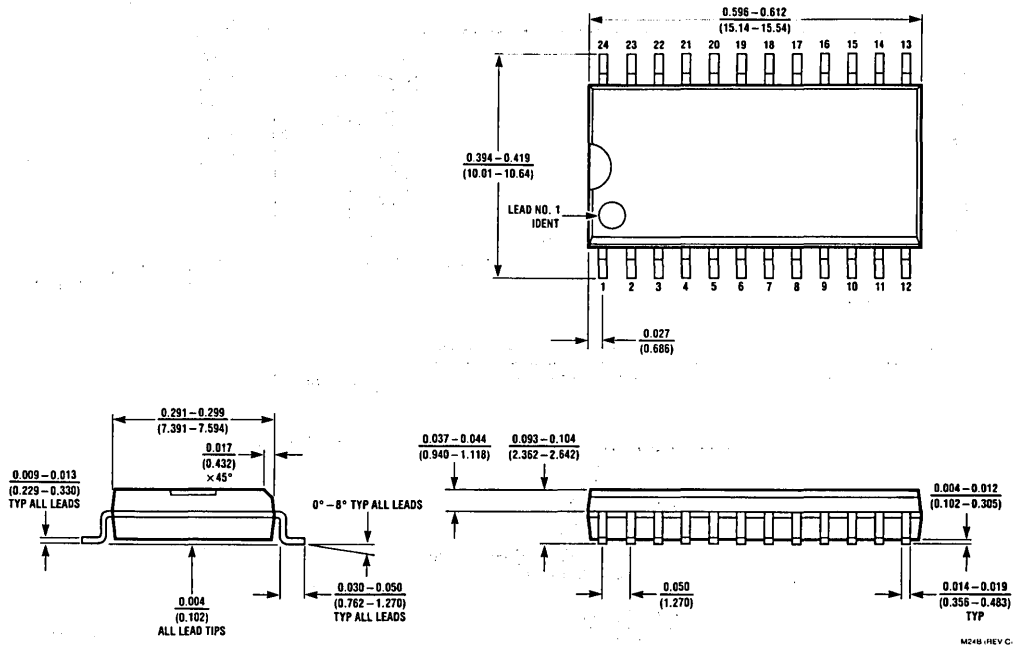
16 Lead Small Outline Integrated Circuit
NS Package Number M16A



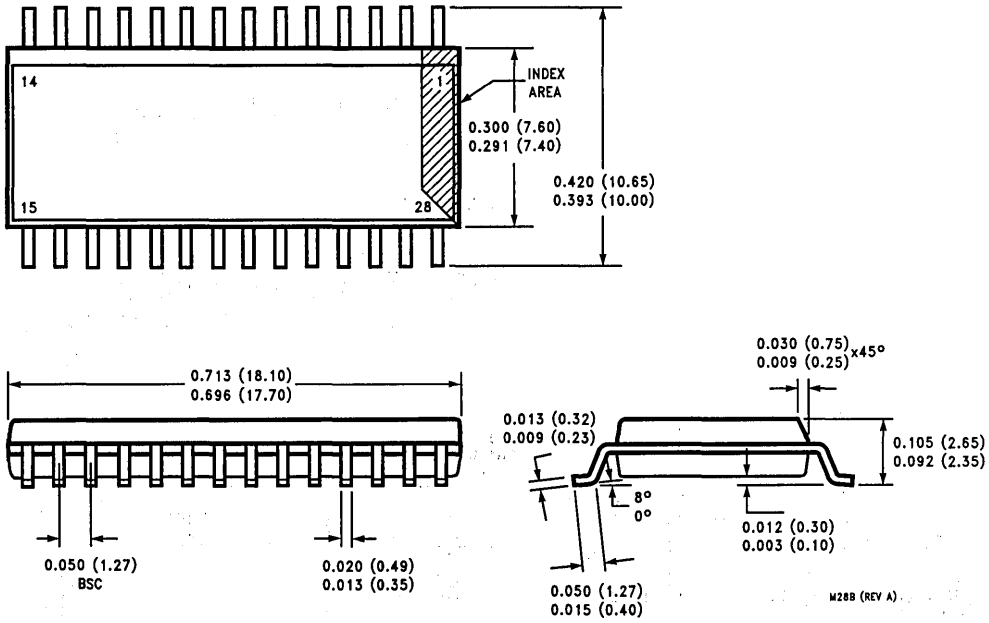
20 Lead Small Outline Integrated Circuit
NS Package Number M20B



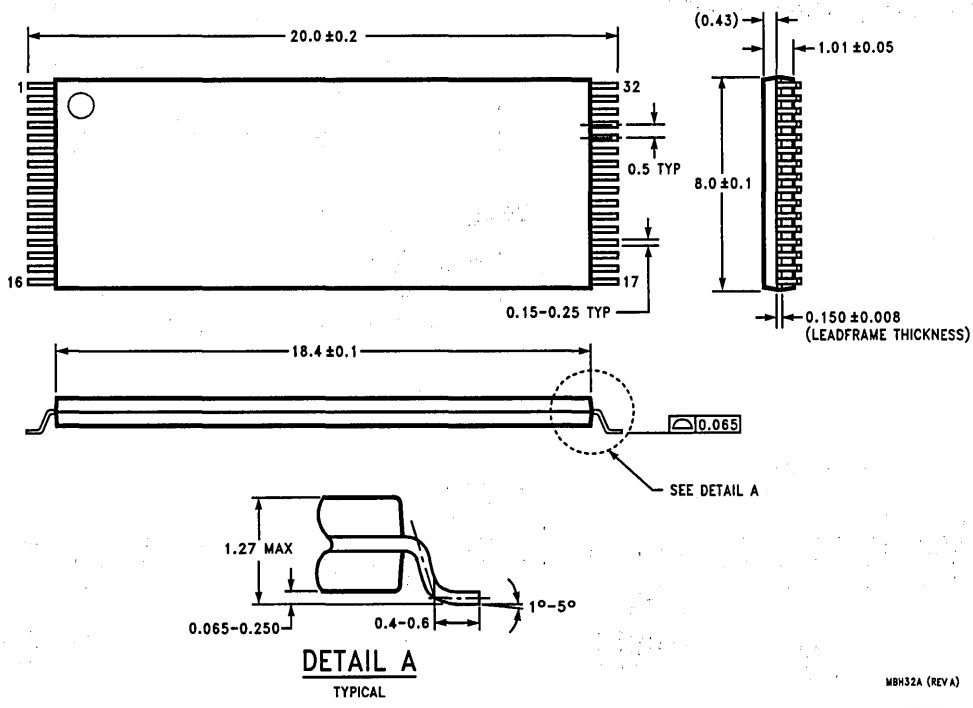
24 Lead Small Outline Integrated Circuit
NS Package Number M24B



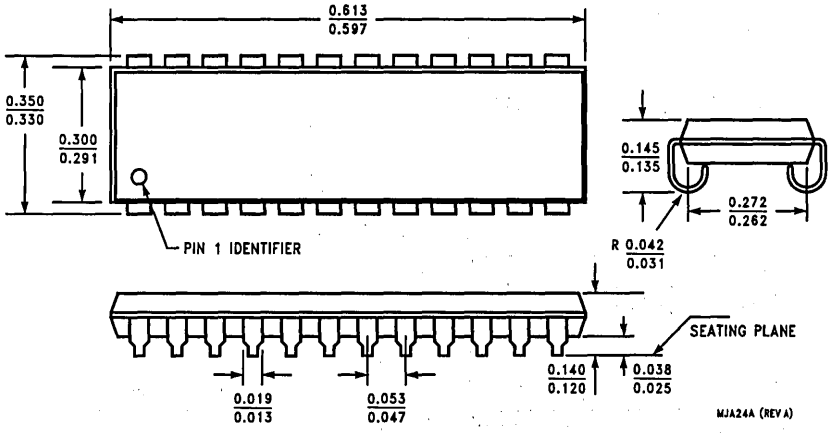
28 Lead Small Outline Integrated Circuit
NS Package Number M28B



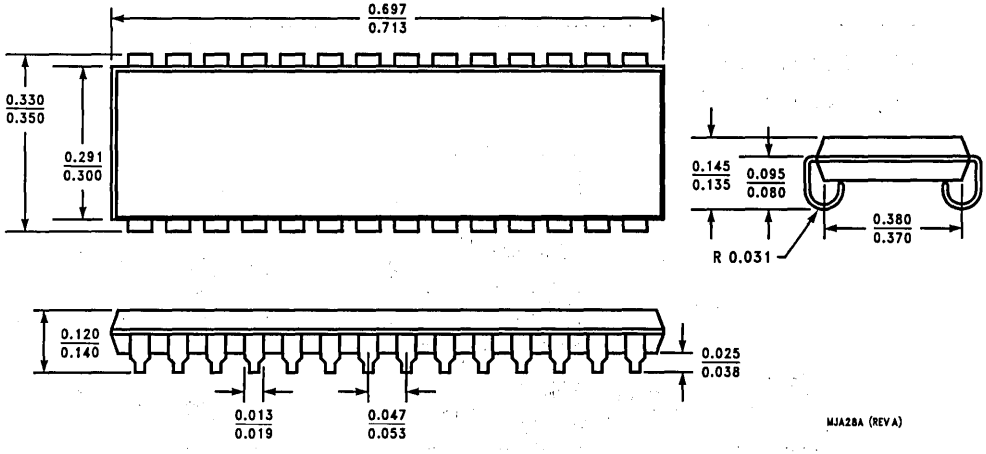
32 Lead TSOP, Type I - EIAJ
NS Package Number MBH32A



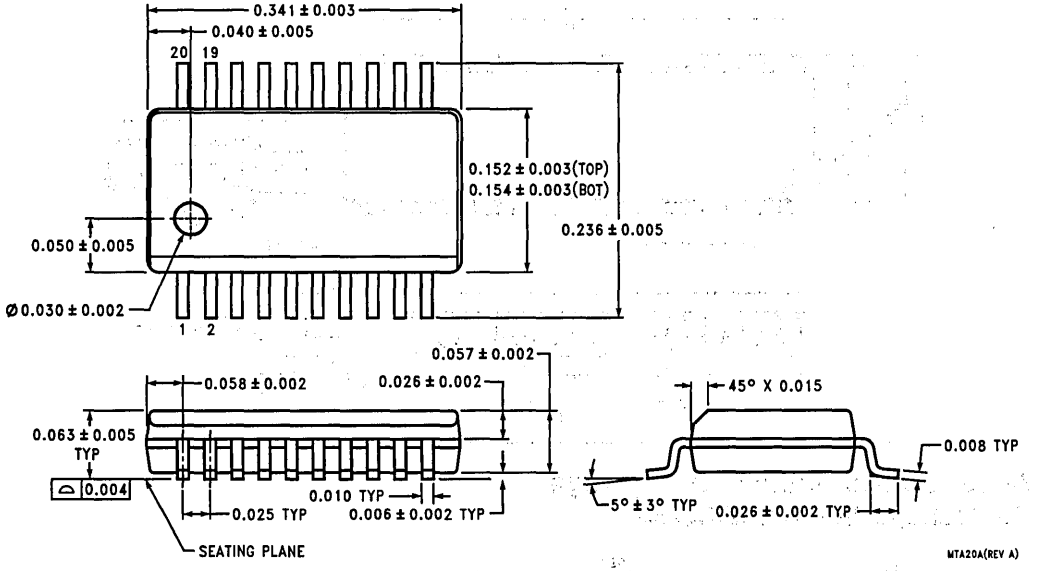
24 Lead Small Outline SOJ Package
NS Package Number MJA24A



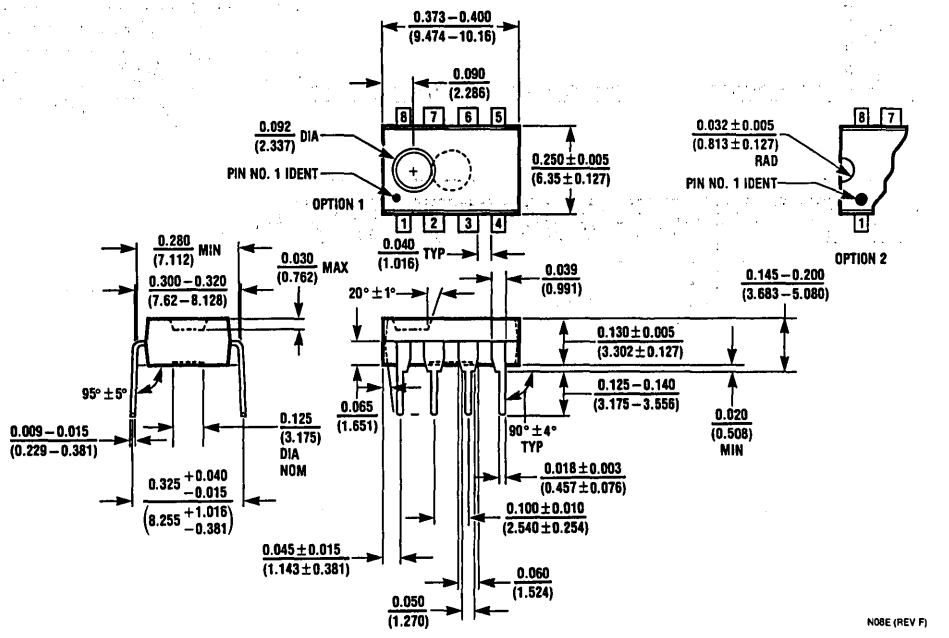
28 Lead Small Outline SOJ Package
NS Package Number MJA28A



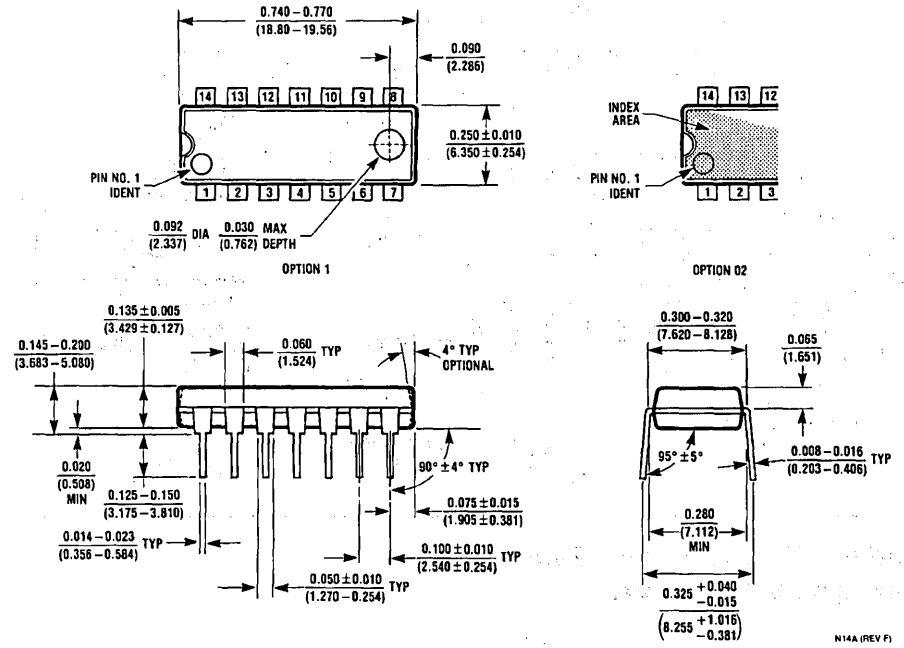
20 Lead Small Outline SOJ Package
NS Package Number MTA20A



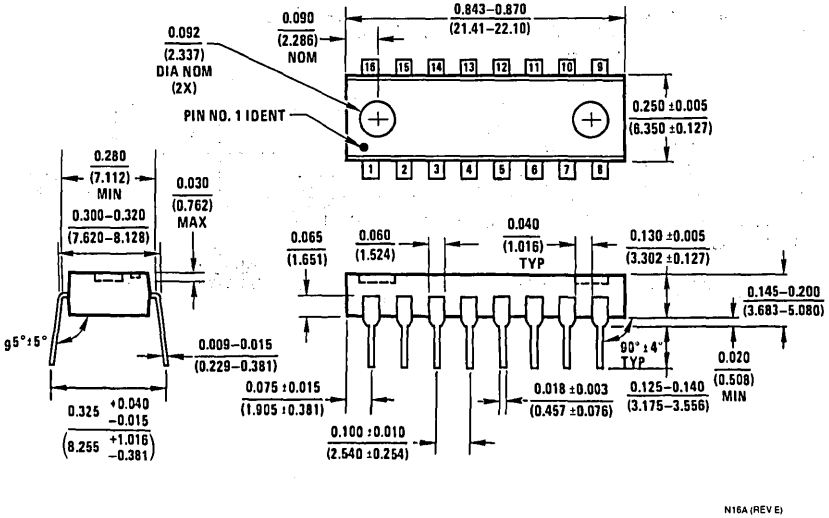
8 Lead Plastic Dual-In-Line Package
NS Package Number N08E



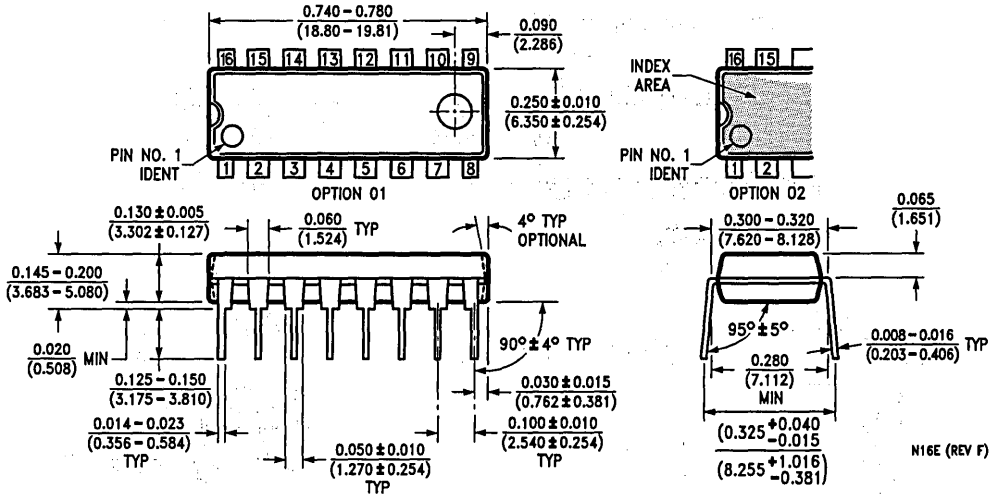
14 Lead Plastic Dual-In-Line Package
NS Package Number N14A



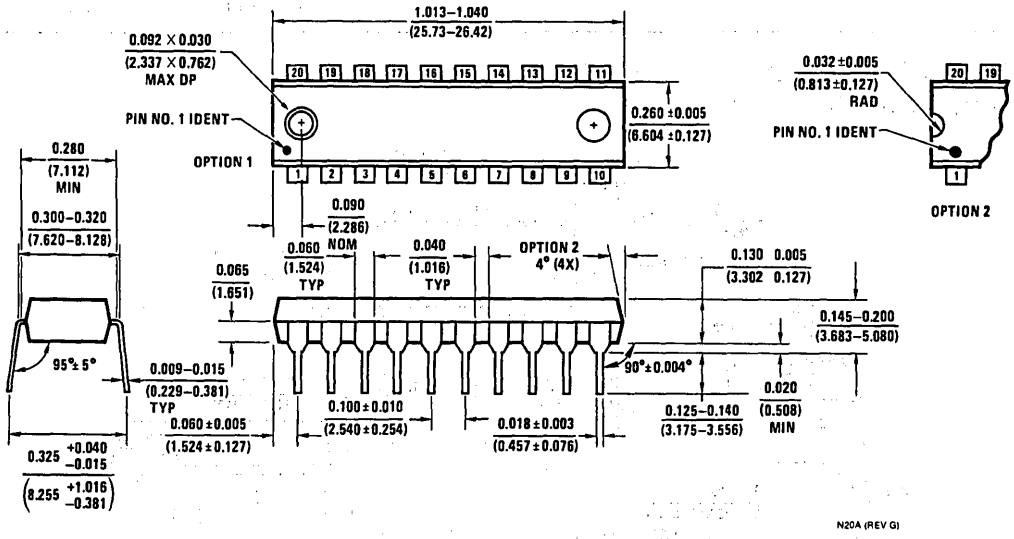
16 Lead Plastic Dual-In-Line Package
NS Package Number N16A



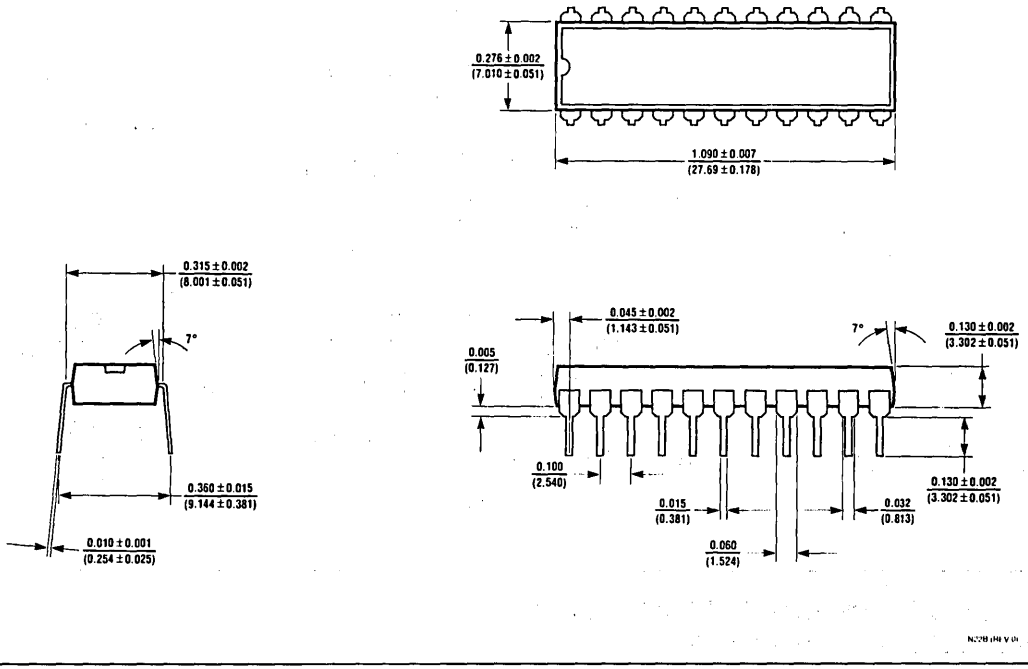
16 Lead Plastic Dual-In-Line Package
NS Package Number N16E



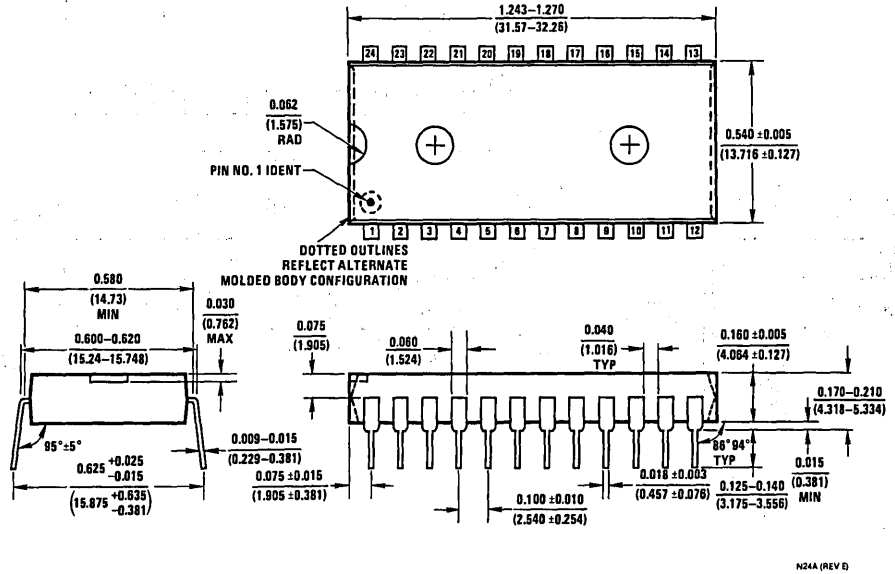
20 Lead Plastic Dual-In-Line Package
NS Package Number N20A



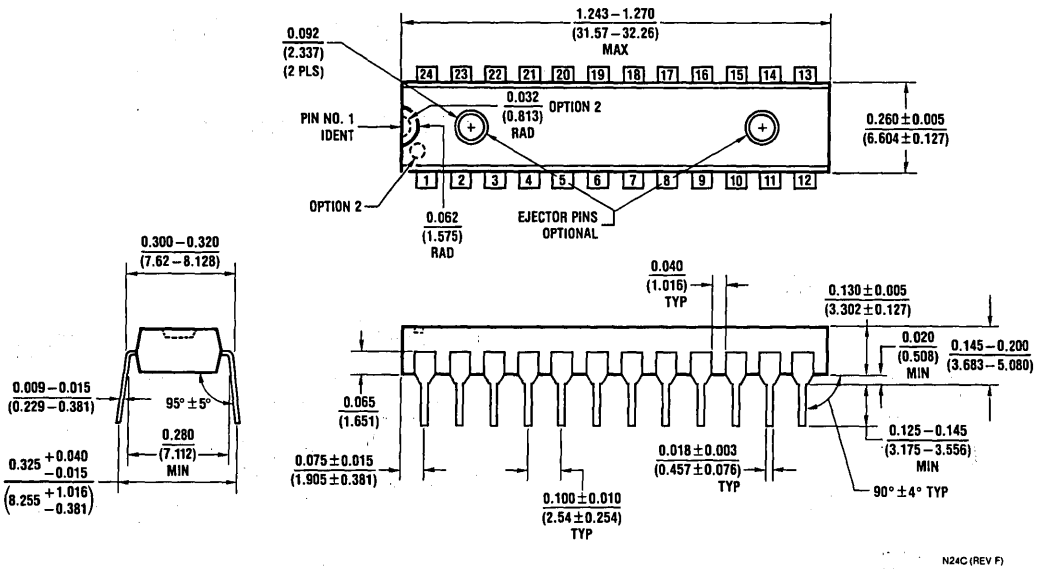
22 Lead Plastic Dual-In-Line Package
NS Package Number N22B



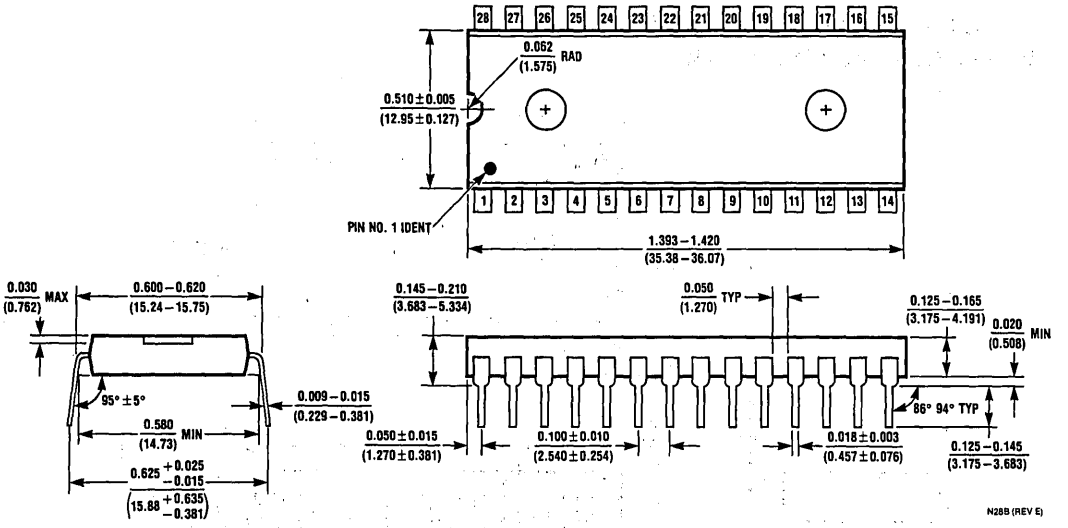
24 Lead Plastic Dual-In-Line Package
NS Package Number N24A



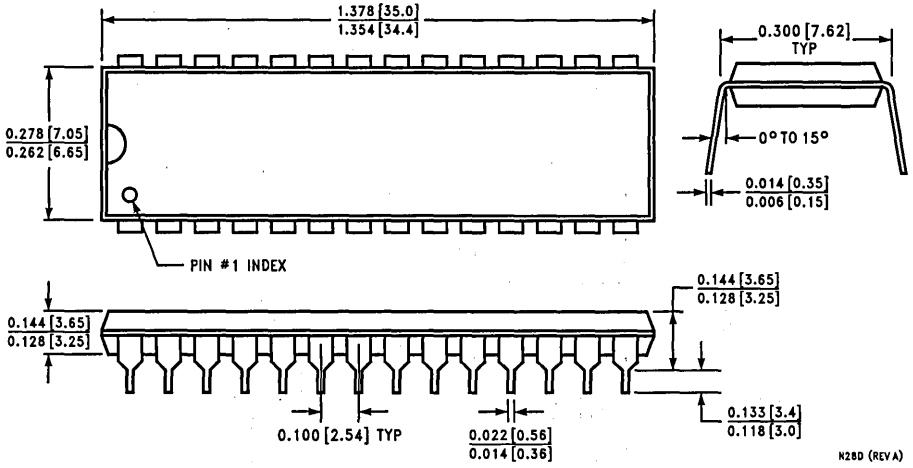
24 Lead Slim (0.300″ Wide) Plastic Dual-In-Line Package
NS Package Number N24C



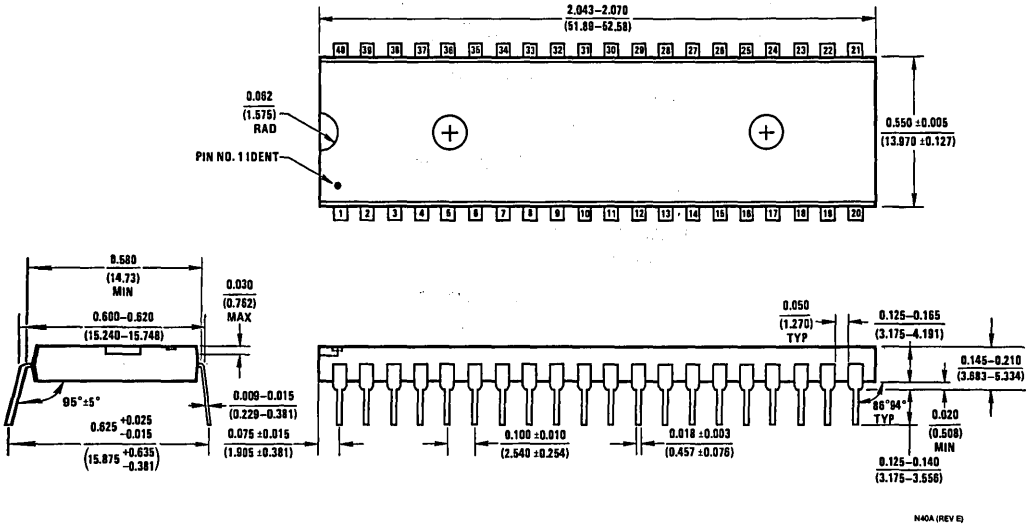
28 Lead Plastic Dual-In-Line Package
NS Package Number N28B



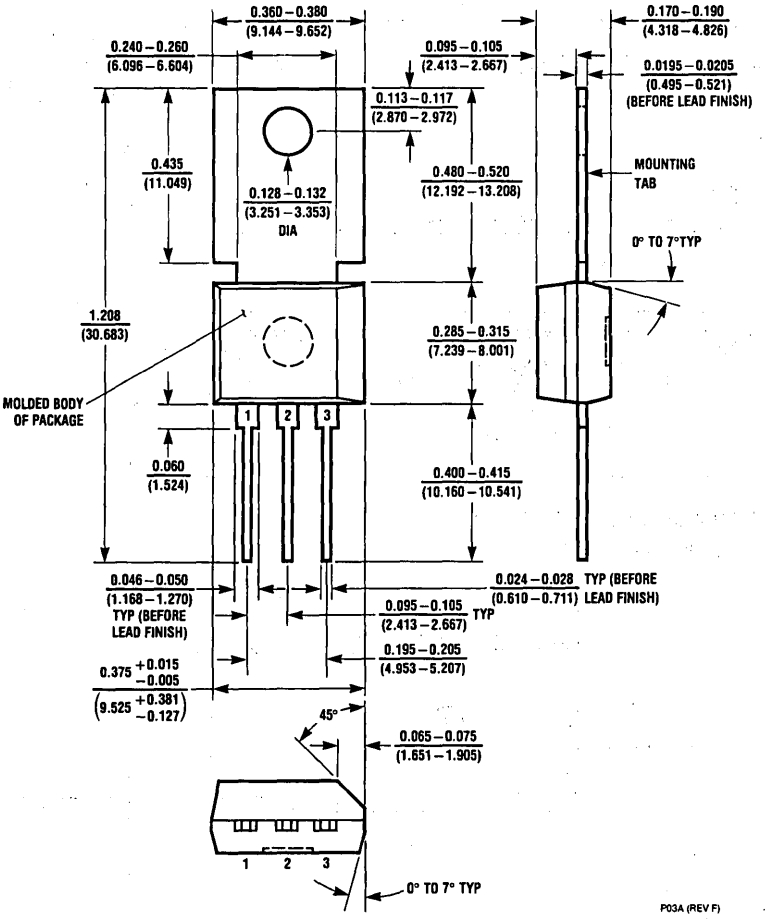
28 Lead (300 MIL) Plastic Dual-In-Line Package
NS Package Number N28D



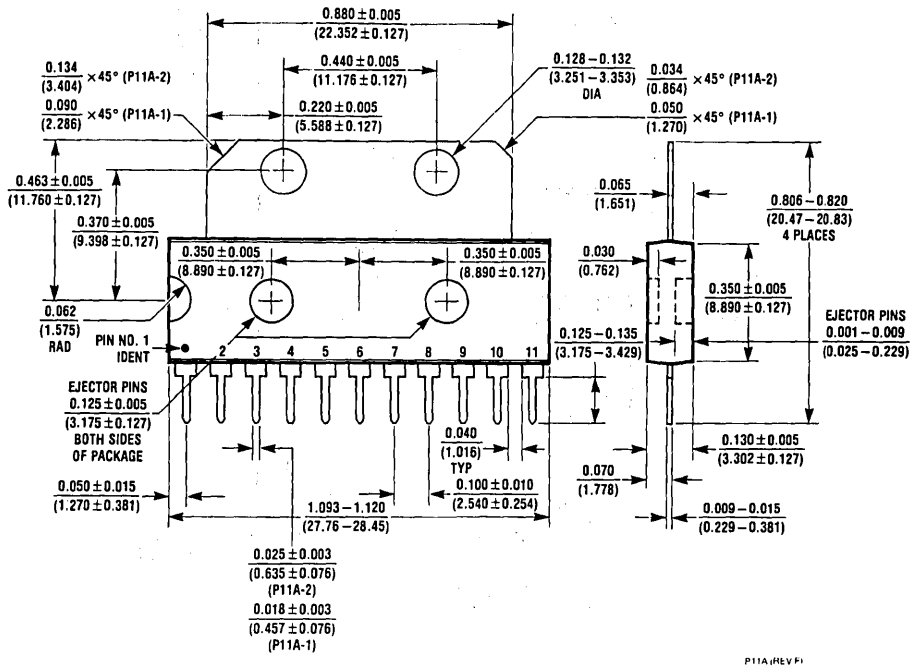
40 Lead Plastic Dual-In-Line Package
NS Package Number N40A



3 Lead TO-202 Molded Package
NS Package Number P03A

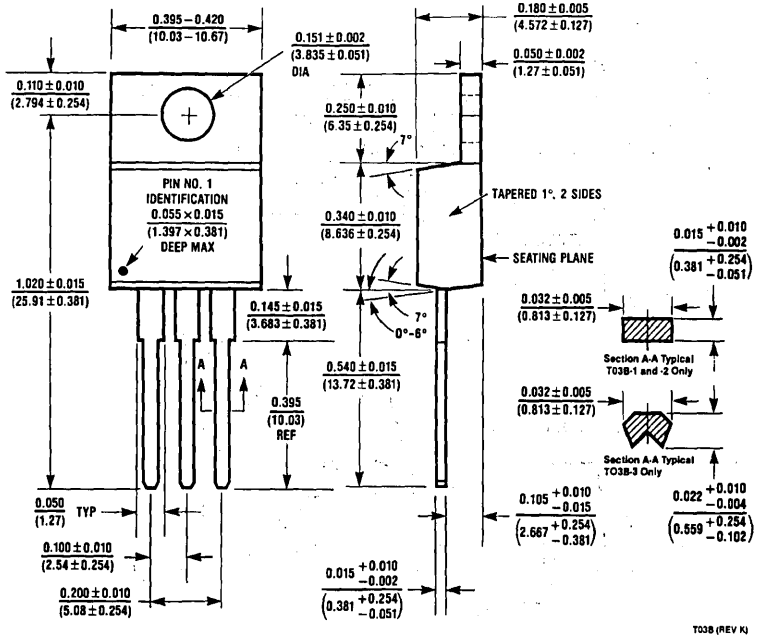


11 Lead Molded SIP
NS Package Number P11A



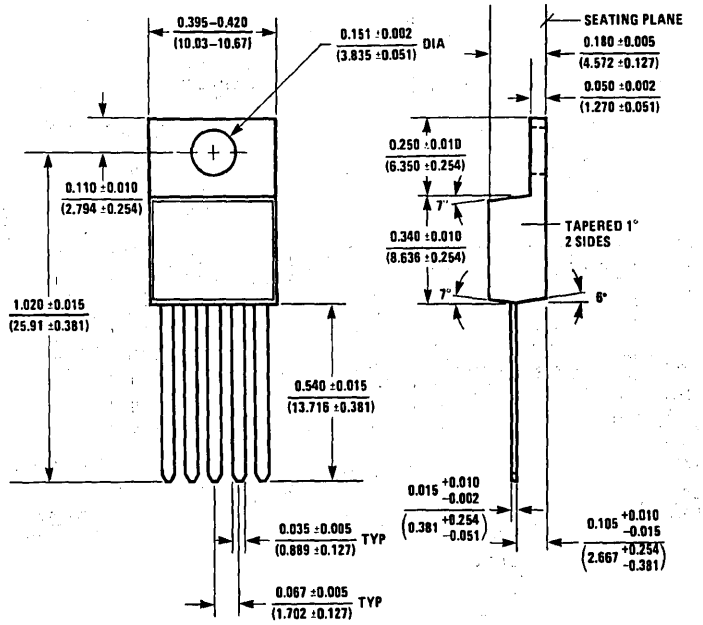
P11A (REV F)

3 Lead TO-220 Molded Package
NS Package Number T03B



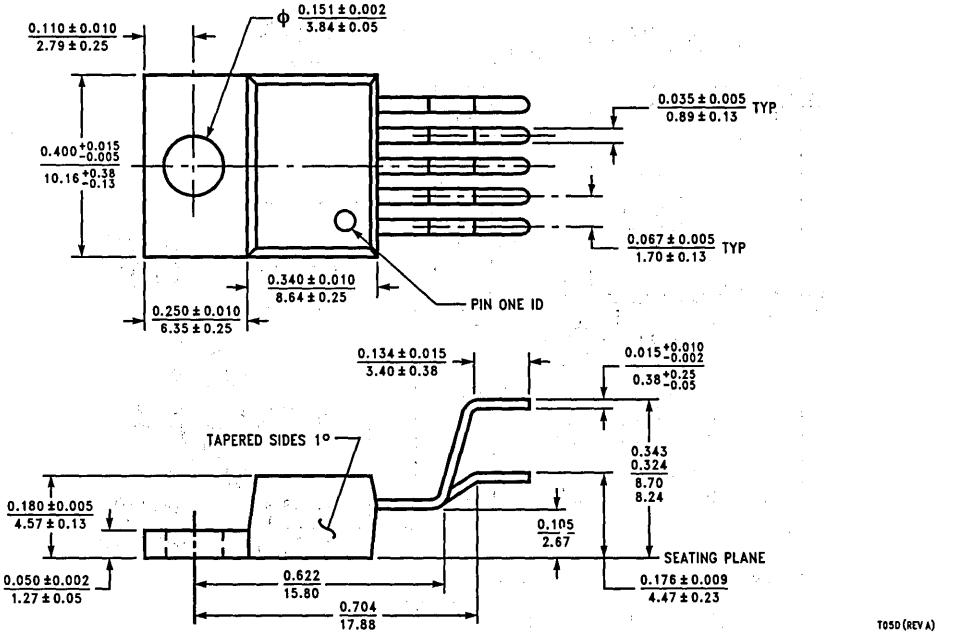
T03B (REV K)

5 Lead TO-220 Molded Package
NS Package Number T05A



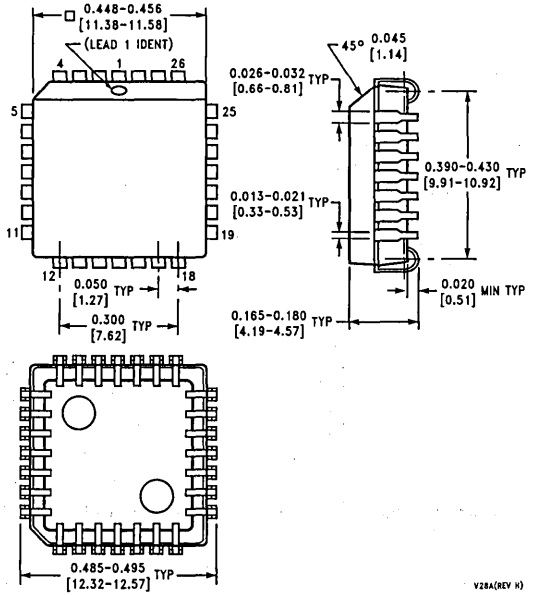
T05A (REV H)

5 Lead TO-220 Molded Package
NS Package Number T05D

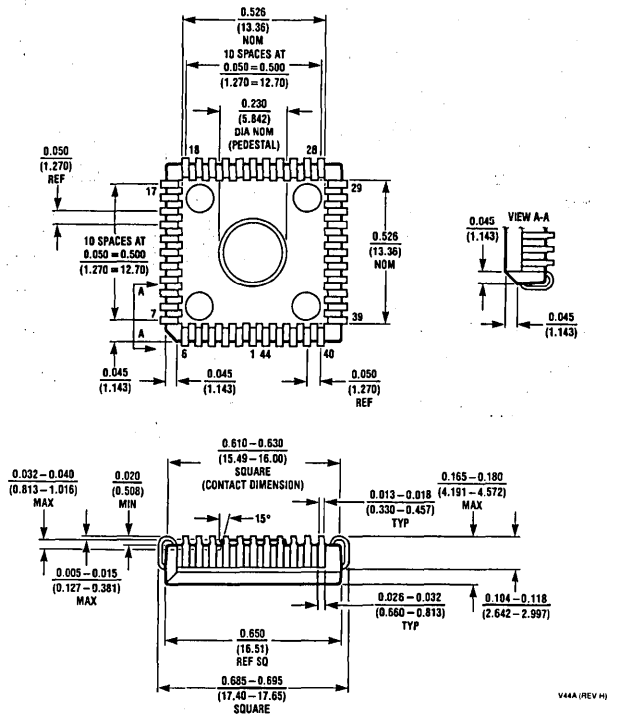


T05D (REV A)

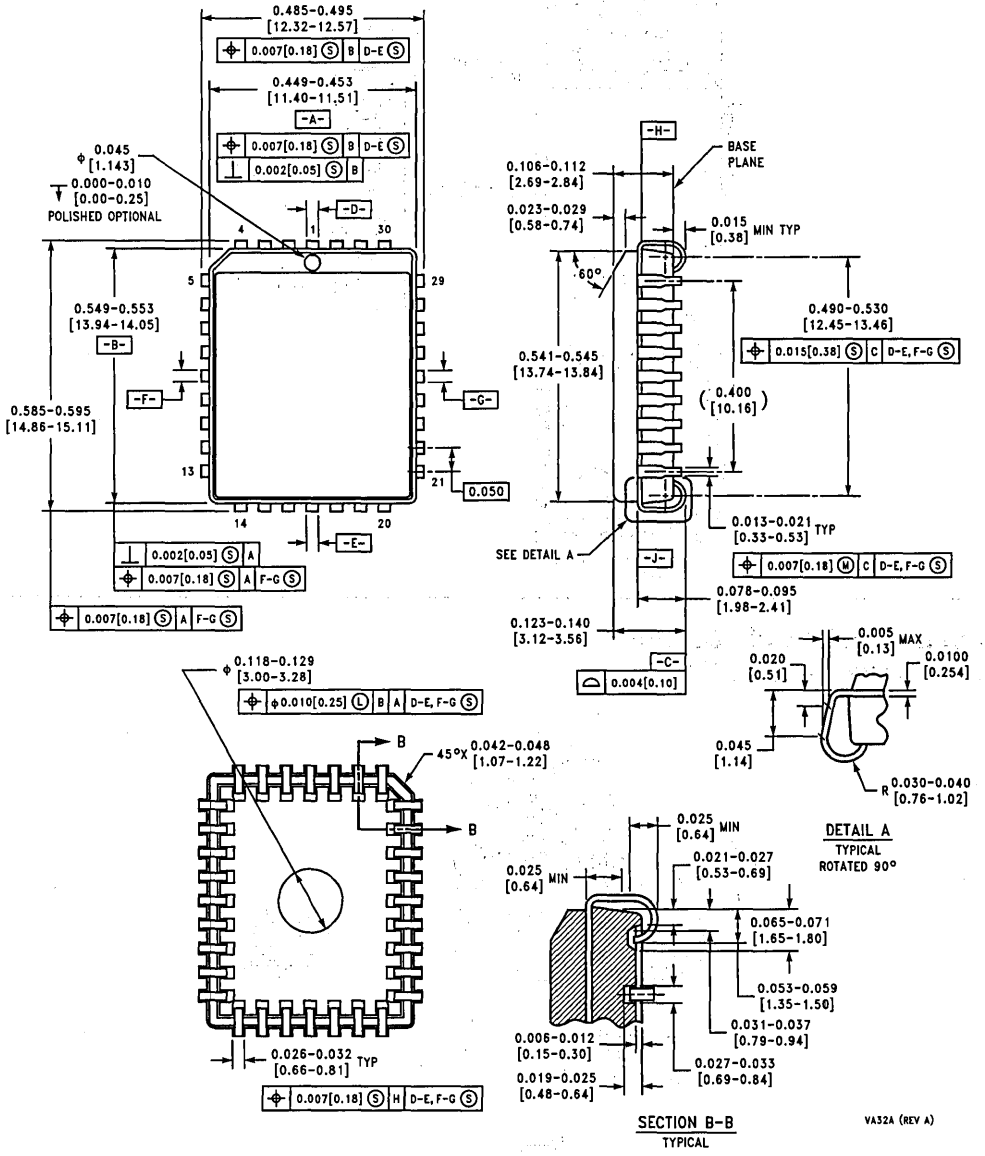
28 Lead Plastic Chip Carrier
NS Package Number V28A



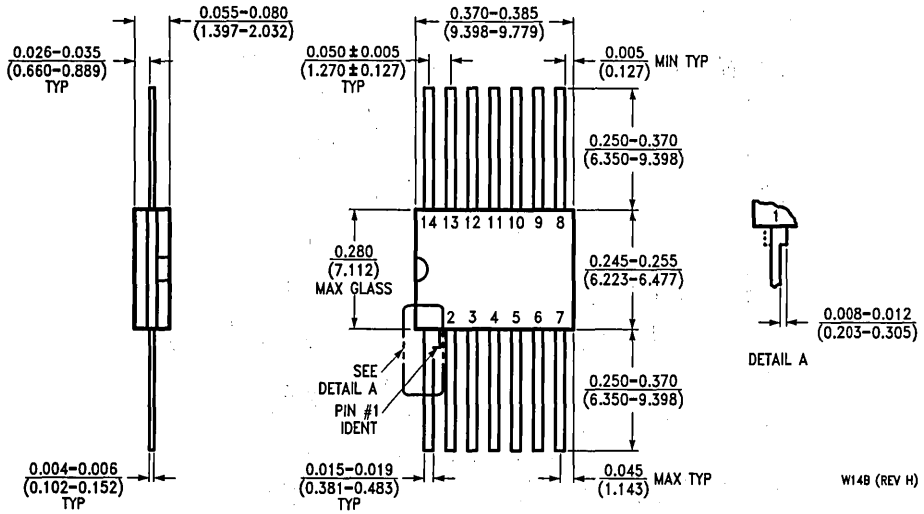
44 Lead Plastic Chip Carrier
NS Package Number V44A



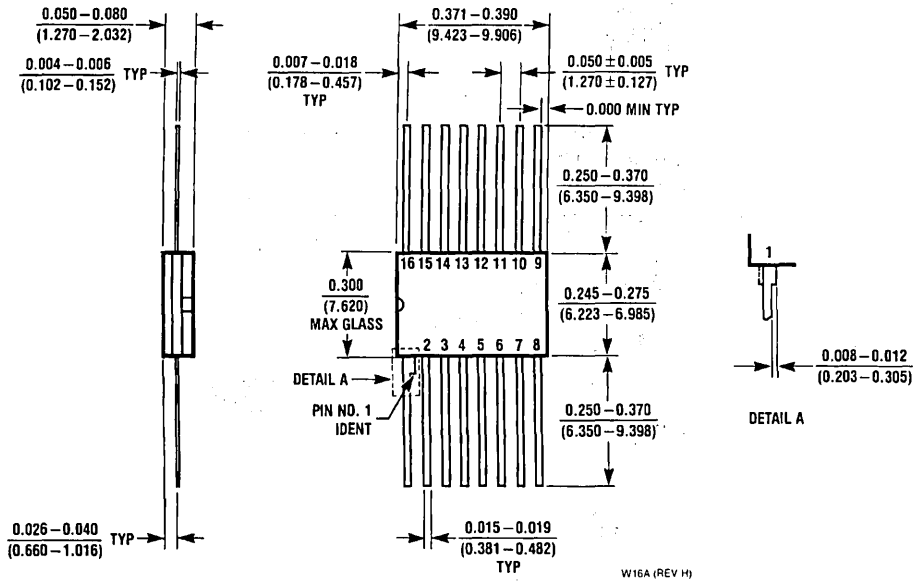
32 Lead Plastic Chip Carrier
NS Package Number VA32A



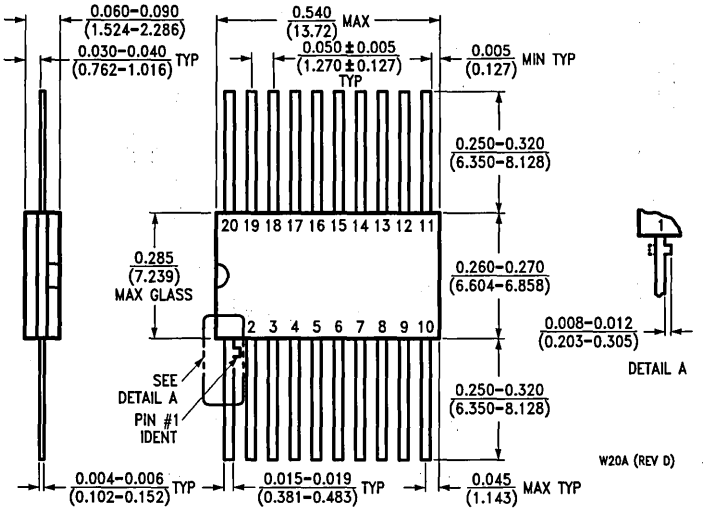
14 Lead Ceramic Flatpak
NS Package Number W14B



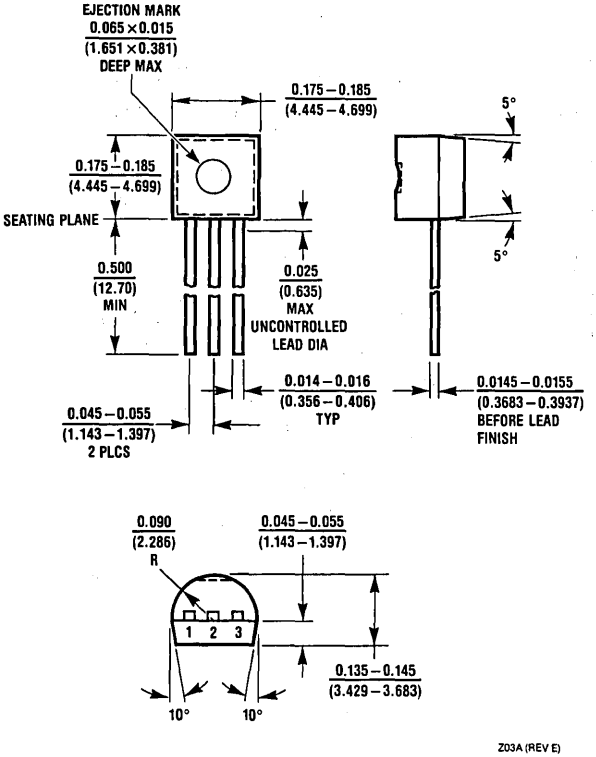
16 Lead Ceramic Flatpak
NS Package Number W16A



20 Lead Ceramic Flatpak
NS Package Number W20A



3 Lead TO-92 Molded Package
NS Package Number Z03A



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