400003

National Semiconductor

Advanced BiCMOS Logic Databook

ABTC
Integrated Bus Functions
BCT

ADVANCED BiCMOS LOGIC
DATABOOK

1993 Edition

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Introduction

Advanced BiCMOS Technology—ABTC

National Semiconductor has gone beyond conventional logic with its new ABTC BiCMOS family. Speeds on octal devices are 20% faster than ABT logic (1.0 ns faster) combined with value-added specifications and guaranteed live insertion protection.

ABTC offers higher performance for manufacturers of high-end computing:

- Faster speed (3.6 ns max. on the ABT245C)
- Propagation delays specified with 1 to 8 multiple outputs switching and 50 pF to 250 pF capacitive loads
- Low static and dynamic power consumption
- Tight skew to squeeze even more out of the designer's timing budget

ABTC provides increased up-time for manufacturers of telecommunications systems:

- Guaranteed high impedance through the entire power-up/power-down cycle
- ABTC eliminates bus disruption during live board insertion
- Power up/down TRI-STATE® to prevent loading of the bus during power down
- Low noise $V_{OLP} < 0.8V$ (ABT244C)

In addition, ABTC proprietary circuitry provides faster disable times than enable times—an automatic way to avoid bus contention. ABTC guarantees are specified in an easy-to-read table. Given lower margin of performance error, a system can be pushed to even higher levels by using ABTC's extended AC specifications.

Octal devices are available in 20- and 24-lead SOIC JEDEC, 20-lead SOIC EIAJ, and 20- and 24-lead fine-pitch SSOP Type II. The 16-bit devices are available in 48- and 56-lead SSOP, which are pin compatible with TI Widebus™ devices.

Integrated Bus Function (IBF)

National's IBF products are an extension of today's logic products targeted at areas where integration optimizes system performance. National sees market opportunities for these products in the areas of computing (from laptops through parallel processing), local area networking, and telecommunications.

The current offerings target two specific areas: bus-to-bus communication and CPU to memory datapath communication. Bus-to-bus communication features include byte-swapping to facilitate system design in areas such as big endian-little endian. CPU to memory datapath communication solutions include a synchronous datapath multiplexer targeted at memory interleaving with additional potential applications in parallel processing. The products have been developed on various technologies within National including FACT Quiet Series™ with the additional feature of TTL I/O, the recently released ABTC 1.0μ BiCMOS technology, and National's FASTr™ technology.

BiCMOS Technology—BCT

National's BCT provides a balanced solution between CMOS and Bipolar circuit features, offering low noise, FAST-like speeds, high drive 64 mA outputs, and the low static power of CMOS. Based on two well-known reliable processes, FAST® and FACT™, BCT combines the favorable properties and high quality from both families.

BCT allows designers to optimize system performance, providing the designer with the ideal speed/power/noise solution for high performance bus and clock distribution applications in personal/desktop computers, PC LAN servers, PC peripherals, workstations, telecommunication switches/multiplexers, fiber optic equipment, and automatic test equipment (ATE).

There are currently 20 BCT products available including buffers, drivers, and transceivers. National BCT parts are pin and functionally compatible to TI's SN74BCTxxx parts.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The data sheet is printed for reference information only.

Alpha-Numeric Index

Alpha-Numeric Index (Continued)

Section 1

ABTC Description and Family Characteristics

Section 1 Contents

National Semiconductor

Technology and Family Characteristics

National has gone beyond conventional logic with its new **ABTC** BiCMOS family. Speeds that are 20% faster than ABT logic (1.0 ns faster) combine with value-added specifications and guaranteed live insertion protection.

ABTC for Computing

- ABTC offers higher performance for manufacturers of high-end computing equipment
  - — Faster speed (3.6 ns max on the 74ABT245C)
  - — Propagation delays that are specified with 1 to 8 multiple outputs switching and 50 pF to 250 pF capacitive load
  - — Low static and dynamic power consumption
  - — Tight skew to squeeze even more out of the designer's timing budget

ABTC for Telecom

- ABTC provides increased uptime for manufacturers of telecommunication systems
  - — Guaranteed live (hot) insertion
  - — Power up/down TRI-STATE® to prevent loading of the bus during power down. This unique high impedance guarantee provides a glitch-free bus interface during the entire power-up and power-down cycle.
  - — Low power consumption

In addition, proprietary ABTC circuitry provides for faster disable times than enable times—an automatic way to avoid bus contention. ABTC guarantees are specified in an easy-to-read table. Given lower margin of performance error, a system can be pushed to even higher levels by using ABTC's extended AC specifications. ABTC products are socket compatible with ABT, so upgrades are easily accomplished. In the critical areas of I/O levels, thresholds and edge rate specifications, ABTC is fully compatible with ABT. ABTC can be dropped into more than 80% of ABT sockets with no performance problems. Set-up and hold times on a couple of sequential ABTC functions don't match those of ABT, and actually improve upon the timing. However, prudent double checking would eliminate potential problems.

ABTC recognizes the need for advanced packaging technology and offers both SOIC (JEDEC and EIAJ) and fine-pitch SSOP Type-II for 20-lead and 24-lead devices.

16-BIT COMPATIBILITY

Until now, users had no alternate source on 16-bit ABT products, e.g., one ABT manufacturer packages its 16-bit products in SSOP while the other uses 44-lead PQFP. National has tipped the scale by putting its 16-bit ABTC products in the more popular SSOP. While National's ABTC octal products are faster than the competition, other specifications are compatible, making ABTC a de facto alternate source for competitive ABT products in SSOP.

Family Comparison Chart

Depending on system architecture and purpose, logic devices are selected to optimize system performance. National offers several logic families, and the comparison chart is provided to assist you with your selection criteria. Speed, power, noise, drive, etc. may weight differently in importance depending on whether the end system requires computing speed, low standby power, low EMI to meet FCC regulations or must meet any one of many bus standards.

Logic Family and ABTC Comparison

Criteria	Significance	ABT245C	ACTQ245	BCT245	FCT245A	FCT245	FR245
Guaranteed Speed—t_{PLH} ns	Faster system performance	3.6	10.5	7.0	4.6	7.5	3.9
Guaranteed MOS t_{PLH} ns	Realistic system performance (Note 2)	5.2	NG	9.0	NG	NG	NG
Static Power I_{CCL} (mA) (Outputs Low)	Lower quiescent supply current, less power consumption, and less cooling required	30 mA	80 μA	70 mA	1.5 mA	1.5 mA	110 mA
Guaranteed Dynamic Power I_{CCD} (mA/MHz)	Lower system power consumption under heavier loading conditions	0.1 (Note 3)	NS	NS (Note 3)	0.40 (Note 3)	0.40 (Note 3)	NS
Guaranteed Noise V_{OLP} (5V, 25°C)	Less data disruption, especially when switching 8 outputs at a time	0.8	1.5	1.2	2.5 NS (Note 1)	1.5 NS (Note 1)	0.8 NS
Dynamic Threshold V_{ILD} V_{IHD} (5V, 25°C)	Less data disruption, especially when connected to a bus	0.6 2.0	0.8 2.2	NS	NS 1.8 − 1.2 1.8 − 2.2	NS 0.8 − 1.2 1.8 + 2.2	NS
20/24 Pin Package 16-Bit Devices	Customers need viable alternate source	SOIC/SSOP SSOP	SOIC/QSOP SSOP	SOIC	SOIC/QSOP	SOIC/QSOP	SOIC SSOP
Capacitance C_{IN} (pF) $C_{I/O}$ (pF)	Lower capacitance means less bus loading, notwithstanding-frequency	5 11	4.5 15	11.2 10.2	10 12	10 12	8/17 NS
I_{OL}/I_{OH} Output Drive (mA)		64/−32	24/−24	64/−15	64/−15	64/−15	64/−15
ESD (Note 4)	Easier handling	>2000V	>4000V	>4000V	>4000V	>4000V	>4000V

NG = Not Guaranteed; NA = Not Available; NS = Not Specified

Assumptions: Device is '245.

Note 1: V_{OLP} is measured on '244 function.

Note 2: Specified with 8 outputs switching and no load.

Note 3: I_{CCD} measured 1 bit toggling, 0V to 5V, 50% duty cycle, outputs loaded with 50 pF, no resistor.

Note 4: Typical values for HBM ESD.

ABTC Circuit and Design Architecture

The basic circuitry for an ABTC non-inverting Buffer with TRI-STATE control logic is shown in *Figure 1*. Robust bipolar components form the dual rail ESD protection networks for both input and output structures. The Q6 and D6 ESD circuits provide protection to the V_{CC} rail and have a high enough breakdown voltage rating to remain high impedance (I_{ZZ} < 100 μA) during powered-down applications. The Schottky transistors Q5, Q7 and Q8 provide protection to the Ground rail and double functionally as highly conductive undershoot clamps.

The TRI-STATE output structure is formed with Bipolar components to produce high drive (I_{OL} = 64 mA; I_{OH} = −32 mA) and high speed TTL compatible logic swings. The pull-up stage utilizes cascaded emitter followers Q3 and Q4 to provide high source current drive for the charging of capacitive loads. The no-load TTL compatible V_{OH} level is one forward-biased V_{BE} (Q3) drop and one forward-biased V_{FD} Schottky diode (D4) drop below the V_{CC} rail yielding typical 3.8V V_{OH} at 5V V_{CC}, 25°C and 10 μA source current. The ON source impedance of this pull-up stage is typically less than 10Ω for source currents between −5 mA to −40 mA at 25°C. This initial low impedance turn-on characteristic allows the pull-up stage to easily provide a V_{OH} level of 2V minimum at I_{OH} source current of −32 mA over the operating V_{CC} and temperature ranges. See *Figure 6*. At 25°C and source currents above −50 mA, the pull-up stage becomes limited by voltage drop across the RI_{OS} resistor and the effective source impedance becomes 25Ω typically. Schottky diodes D3, D4 and D5 also provide blocking to insure that the pull-up stage remains high impedance during power down applications.

When the output is enabled by a logic low on the $\overline{OE}$ input and a logic high is on the Data input, the base of Q3 is driven to the V_{CC} rail by the CMOS inverter in the data path. The open drain CMOS NAND gate is logic high-open (non-conducting) and allows the base of Q4 to be driven ON by Q3. The CMOS NOR gate goes low turning Q1 OFF and turning ON the CMOS AC/DC Miller Killer circuitry which grounds the base of Q2, quickly turning it OFF. This circuitry provides an active shunt for any charge coupled by the Miller Effect of the Q2 collector-base capacitance during the low to high output transition. Use of this active circuitry improves output rise time and serves to reduce simultaneous conduction of pull-up and pull-down stages during LH transitions. The AC/DC Miller Killer circuit is also active when the output goes to TRI-STATE to prevent Q2 base injection by the LH transitions of other outputs on a bus, therefore dynamic bus loading will be capacitive only.

Power Down Miller Killer circuitry at the base of Q2 is inactive when V_{CC} is applied. When V_{CC} is powered down, the Power Down Miller Killer circuitry provides an active shunt to transient energy coupled to the Q2 base by its collector base capacitance. This prevents momentary turn-on of Q2 during LH transitions in partial power down bus applications and maintains the powered off output as only a Hi-Z light capacitive load (I_{ZZ} < 100 μA) to the bus.

Note that Q1 drives only the Q2 pull-down stage and does not function as the Phase Splitter driver typical of TTL logic. The pull-up stage is controlled by CMOS logic independent of Q1. This feature allows the input threshold voltages for the CMOS logic driving the pull-up stage to be set independent of the logic driving the pull-down stage.

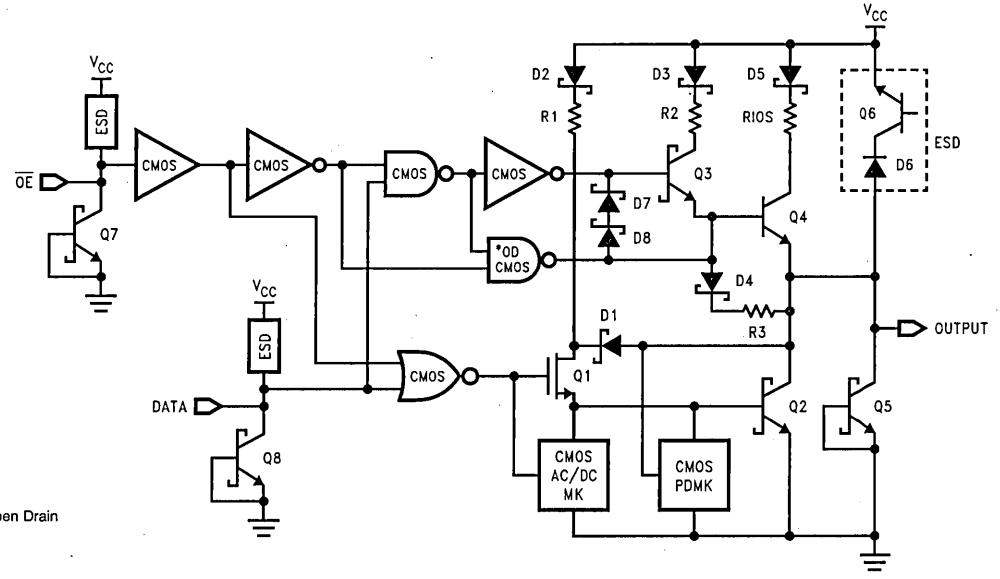

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FIGURE 1. Basic ABTC TRI-STATE Buffer Schematic

ABTC Circuit and Design Architecture (Continued)

The transfer function for the non-inverting ABTC Buffer shown in *Figure 2* indicates that the data input switching threshold for the pull-down stage is approximately 200 mV lower than the pull-up stage. As the Data input is swept from logic LOW to logic HIGH, the output switches from active LOW to high impedance at an input threshold of about 1.3V at 25°C and a V_{CC} of 5.0V. When the input reaches about 1.5V, the output switches from high impedance to HIGH. This design feature serves to reduce simultaneous conduction of the stages during switching. Also, the 200 mV offset in Data input switching thresholds acts like hysteresis and causes the buffer to be very tolerant of slow data input edge rates, i.e., edge rates slower than 10 ns/V can easily be tolerated without output oscillation. The switching threshold is proportional to V_{CC} as indicated in *Figure 3* and is quite stable as a function of temperature as indicated by *Figure 4*.

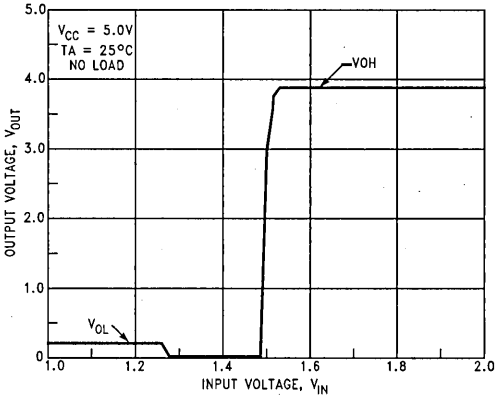

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FIGURE 2. Buffer Transfer Function @ Room Temperature V_{CC} = 5V, T_A = 25°C, No Load

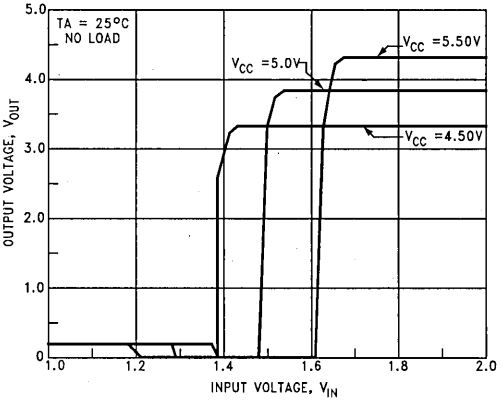

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FIGURE 3. Transfer Function vs V_{CC} T_A = 25°C, No Load

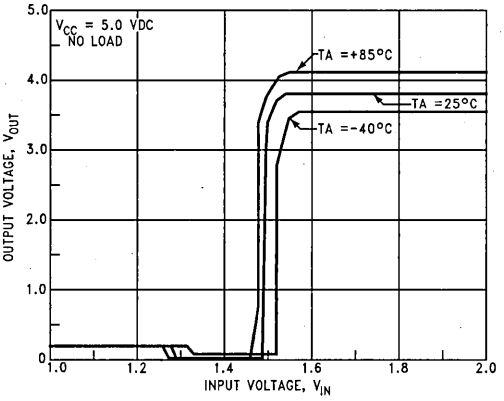

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FIGURE 4. Transfer Function vs Temperature V_{CC} = 5V DC, No Load

With the output enabled by a LOW on the $\overline{OE}$ input, a LOW on the Data input forces active LOWS on both the CMOS inverter and the open drain CMOS NAND gate outputs, which then simultaneously turn OFF Q3 and Q4. The CMOS NOR gate output goes HIGH, turning the AC/DC Miller Killer circuitry OFF and Q1 ON to drive Q2 ON. Q2 is designed to easily sink 64 mA I_{OL}, at V_{OL} < 0.55V. During HL output transitions, Schottky diode D1 assists the pull-down stage in providing a low impedance discharge path for the output load capacitance. As the stage turns on, part of the charge on the output load passes through D1 and Q1 to momentarily increase the base drive to Q2 and increase Q2's current sink capability. See output characteristics in *Figure 5*, I_{OL} vs V_{OL}.

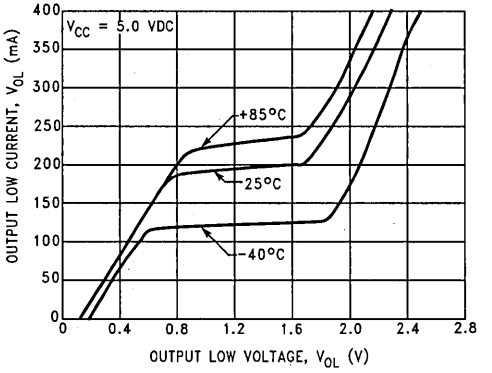

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FIGURE 5. Output Low Characteristics V_{CC} = 5V DC

ABTC Circuit and Design Architecture (Continued)

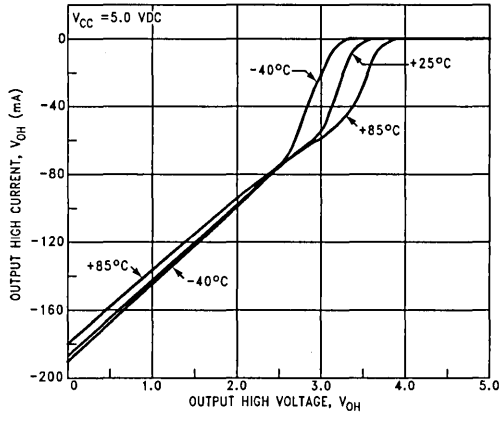

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FIGURE 6. Output High Characteristics V_{CC} = 5V DC

When the output is disabled by a HIGH on the $\overline{OE}$ input, the enable CMOS logic quickly overrides the Data path logic and cuts off drive to whichever stage is ON. In the case of an LZ transition, the CMOS NOR gate is driven LOW turning OFF Q1 and turning ON the AC/DC Miller Killer circuitry to insure Q2 is quickly turned off. In the case of a HZ transition, the CMOS inverter goes hard LOW to turn off Q3 and quickly discharge the base of Q4 through Schottky diodes D7 and D8. The effect of disable time (t_{PLZ}, t_{PHZ}) being typically faster than enable time (t_{PZL}, t_{PZH}) inherently helps avoid bus contention.

Since the CMOS Enable logic remains active to V_{CC}'s well below 2V, high impedance control can be maintained to V_{CC} voltages below the turn-on V_{CC} thresholds of the Bipolar output stage. This insures the capability for glitch free power ON/OFF high impedance outputs with the provision that the $\overline{OE}$ input is maintained logic HIGH at or greater than the data sheet specified 2.0V minimum V_{IH} during the V_{CC} power ramp. However, since the CMOS logic switching threshold varies proportional to V_{CC}, a practical worst case $\overline{OE}$ logic high of 2.0V or 50% of V_{CC}, will maintain the power ON/OFF TRI-STATE condition during the V_{CC} transition.

ABTC is designed to be tolerant of controlled live insertion at the PCB level. Controlled means that the insertion or removal methodology is accomplished in such a way that power to the PCB is applied in a preferred sequence and that control signals are provided to the PCB also in the preferred sequence such that output control is asserted to prevent contention of outputs attached to a bus during the power up or down sequence.

Tolerant means that ABTC is designed and guaranteed to behave in a predictable manner during controlled PCB live insertion in systems requiring fault-tolerant or noninterruptable applications. Additionally, ABTC has features which facilitate design of systems which must utilize power partitioning for redundant circuitry or for powering saving of inactive circuits.

All ABTC input, output, and I/O pins are protected with robust Bipolar components with respect to both V_{CC} and Ground rails. This circuitry is designed to withstand 2000V (Human Body Model) and also to provide clamping action for voltage undershoot while preserving low capacitive loading of the pin. The clamping action by the undershoot clamp begins aggressively at voltages more negative than −0.5V relative to Ground, but this clamp remains nonconductive at voltages up to 7V. Relative to the V_{CC} rail, the ESD circuitry begins clamping only at voltages greater than 5.5V above V_{CC}. These ESD circuits remain high impedance and non-conductive for applied input or output voltages between −0.4V to 5.5V with V_{CC} = 0V to 5.5V.

ABTC CMOS input stages are Hi-Z with or without V_{CC} applied. The I_{IL}, I_{IH}, and I_{BVI} data sheet specification guarantees high DC impedance for inputs with V_{CC} applied. The V_{ID} specification guarantees Hi-Z inputs with V_{CC} = 0V.

High impedance output and I/O pins are capable of maintaining Hi-Z status with V_{CC} = 0 and during the application or removal of V_{CC}. The ABTC data sheet parameters I_{OZH} and I_{OZL} guarantee < 50 μA output leakage for applied V_{OUT} voltages of 2.7V or 0.5V at any V_{CC} between 5.5V and 0V with the output disabled and with the appropriate logic input voltage maintained on the $\overline{OE}$ input pin. An additional I_{ZZ} bus drainage specification guarantees < 100 μA output leakage at V_{OUT} = 5.5V with V_{CC} = 0V. Therefore, ABTC outputs are guaranteed to remain glitch-free during the power cycle and at power down V_{CC} = 0V. Refer to Application Section for a more detailed discussion of live insertion and powerup/down TRI-STATE capabilities of ABTC.

Threshold and Noise Margin

Figure 1 describes the input signal voltage levels for use with ABTC products. The AC testing input levels follow industry convention which require 0.0V for a logic LOW and 3.0V level for a logic HIGH. DC input levels are typically 0.0V to V_{IL}, and high input levels are typically V_{IH} to V_{CC}. DC testing uses a combination of threshold and hard levels to assure datasheet guarantees. Input threshold levels are usually guaranteed through V_{OL} and V_{OH} tests.

High level noise immunity is the difference between V_{OH} and V_{IH} and low level noise immunity is the difference between V_{IL} and V_{OL}. Noise-free V_{IH} or V_{IL} levels should not induce a switch on the appropriate output of an ABTC device. When testing in an automated environment, extreme caution should be taken to ensure that input levels plus noise do not go into the transition region.

Dynamic System Power Dissipation

One of several advantages to using BiCMOS logic is its low power when compared to bipolar technologies. As well, it has reduced dynamic output power because of the reduced output swing in comparison to CMOS devices. In the static or quiescent high state, ABTC will consume power like a pure CMOS device, and in the quiescent low state all power goes to driving the bipolar output pull-down transistor.

Total power consumption under AC conditions comes from three sources; quiescent power, internal dynamic power, and output dynamic power.

In other words: $P_{TOTAL} = P_{DQ} + P_{DINT} + P_{DOUT}$

Where:

P_{TOTAL} = Total Power Dissipation
P_{DQ} = Quiescent Power Dissipation
P_{DINT} = Internal Dynamic Power Dissipation
P_{DOUT} = Output Power Dissipation

First the Quiescent power can be derived from the following equation.

$$P_{DQ} = \left[\frac{I_{CCL}}{N} * N_{QOL} * V_{CC}\right] + \left[DI_{CC} * N_{QIH} * V_{CC}\right] + \left[\frac{I_{CCH}}{N} * N_{QOH} * V_{CC}\right]$$

Where:

P_{DQ} = Quiescent Power Dissipation
I_{CCH} = Quiescent Power Supply Current with All Outputs High
I_{CCL} = Quiescent Power Supply Current with All Outputs Low
N_{QOL} = Number of Quiescent Outputs Low
N_{QOH} = Number of Quiescent Outputs High
N_{QIH} = Number of Quiescent Inputs High
N = Number of Active Outputs
DI_{CC} = Power Supply Current for Input with V_{IN} other than V_{CC}

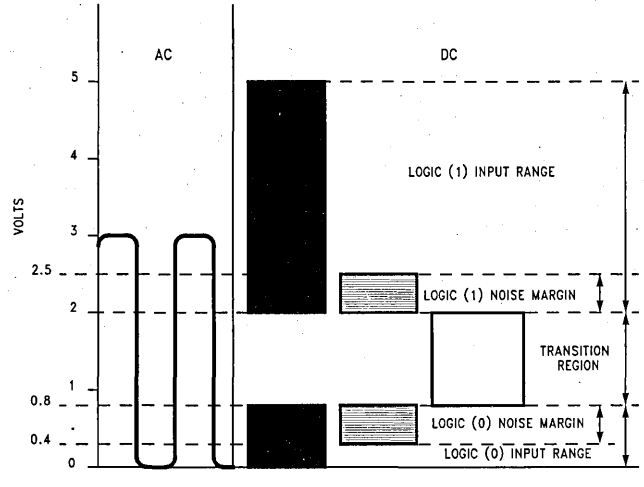

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FIGURE 1

Dynamic System Power Dissipation (Continued)

Secondly, an ABTC device will dissipate power internally by charging and discharging internal capacitance. The following equation takes into account the duty cycle of inputs and outputs and current due to the internal switching of capacitances.

$$P_{DINT} = [(DI_{CC}*DH*NS)*V_{DD}] + \left[\left(\frac{I_{CCL}}{N}*NS*DL\right)*V_{CC}\right] + [(I_{CCD}*f*NS)*V_{CC}]$$

Where:

- P_{DINT} = Internal Dynamic Power Dissipation
- V_{CC} = Power Supply Voltage
- DI_{CC} = Power Supply Current for Input with V_{IN} other than V_{CC} (For example, a typical TTL input voltage is considered to be 3.4V)
  - **Note:** The farther away an input (V_{IN}) is from threshold (1.5V), the less power supply current the IC will consume.
- N = Number of Active Outputs
- DH = Duty Cycle for Switching Inputs High
- DL = Duty Cycle for Switching Outputs Low
- I_{CCL} = Data book specification for power supply current with all outputs low
- I_{CCD} = Power consumption coefficient (mA/MHz) for 1-bit toggling
- f = Frequency of Outputs
- NS = Number of Outputs Switching

Finally, at high frequencies a significant amount of current is consumed by a device to drive its output load. ABTC has an advantage here because of its reduced output swing compared to CMOS devices. For a simple case, if we assume only capacitive components to the load, we can use the following equation.

$$P_{OUT} = [C_L * VS * f] * V_{CC}$$

Where:

- P_{DOUT} = Output Power Dissipation
- C_L = Load Capacitance
- VS = Output Voltage Swing
- f = Output Operating Frequency
- V_{CC} = Power Supply Voltage

Take for an example an ABT244C with all 8 outputs switching at 16 MHz. How much power would be consumed by the IC in this case?

Assumptions:

1. V_{CC} = 5V
2. The data and control inputs are being driven with 0V and 3.4V voltages for logic levels.
3. Data input frequency = 16 MHz @ 50% duty cycle.
4. C_L = 50 pF
5. There are no DC loads on the outputs. i.e., outputs are either unterminated or terminated with an AC shunt termination.
6. Since the output high voltage is produced by a Darlington transistor pair, the output voltage swing will be assumed to be V_{CC} − 1.6V or 5.0 − 1.6V = 3.4V. Therefore VS = 3.4V with V_{CC} = 5.0V.

For quiescent current, all data inputs and outputs are switching leaving only the 2 $\overline{OE}$ inputs static low.

$$P_{DQ} = \left[\frac{I_{CCL}}{N}*N_{QOL}*V_{CC}\right] + [DI_{CC}*N_{QIH}*V_{CC}] + \left[\frac{I_{CCH}}{N}*N_{QOH}*V_{CC}\right]$$

$$= 0 + 0 + 0 = 0$$

Internal Dynamic Current

$$P_{DINT} = [(DI_{CC}*NS*DH)*V_{DD}] + [(\frac{I_{CCL}}{N}*NS*DL)*V_{CC}] + [(I_{CCD}*f*NS)*V_{CC}]$$

$$P_{DINT} = [(2.5e-3*8*0.5)*5.0] + [(\frac{30e-3}{8}*8*0.5)*5.0] + [(0.1*16*8)*5.0]$$

$$= [10.0e-3*5] + [15.0e-3*5.0] + [12.8e-3*5.0]$$

$$= 189\ mW$$

Finally the Output Current

$$P_{OUT} = [C_L * VS * f] * V_{CC}$$

$$P_{OUT} = [50.e-12*3.4V*16e6] * 5.0$$

$$= [2.72e-3]*5$$

$$= 13.5\ mW$$

$$P_{TOTAL} = P_{DQ} + P_{DINT} + P_{DOUT}$$

$$= 0 + 189\ mW + 13.5\ mW$$

$$P_{TOTAL} = 202.6\ mW$$

ABTC Process Characteristics

PROCESS CHARACTERISTICS

National's 1.0 BCT combines bipolar and CMOS transistors in a single process to achieve high speed, high drive characteristics while maintaining low tri-state power and the ability to control noise.

National's 1.0 BCT provides a suitable platform for migration to higher performance levels with minor technology enhancements planned for the near future. In its present form, the technology supports Interface, Digital, Bus and Telecom products from National Semiconductor.

PROCESS FEATURES

- 18 masking layers using stepper lithography
- 100% ion implantation utilized for dopant placement
- Localized retrograde wells tailored for high performance
- Optimized recessed and field isolation sequence for CMOS/bipolar
- NMOS LDD (Lightly Doped Drain), PMOS Halo architecture
- 150Å gate oxide
- Self aligned bipolar contact set utilizing minimum geometries
- Localized retrograde sub-emitter collector
- Advanced planarization on all topographies
- PtSi Schottky diodes, all contacts use platinum for resistance reduction
- Barrier metal of TiW
- Dual layer metal of Al-Si-Cu for long term reliability
- Metal pitch of 3.5 microns

PROCESS FLOW

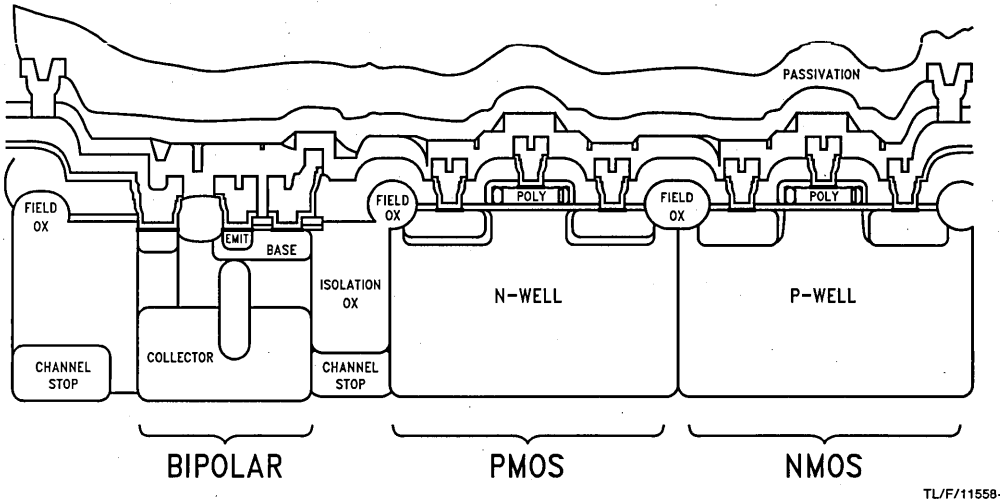
1.0	Buried Layer
2.0	P-Well
3.0	N-Well
4.0	Isolation
5.0	Sink
6.0	Active
7.0	Active Strip
8.0	Poly
9.0	Base
10.0	Bipolar Contact
11.0	Emitter
12.0	P+ Source/Drain
13.0	N+ Source/Drain
14.0	Contact
15.0	Metal 1
16.0	Via
17.0	Metal 2
18.0	Passivation

PROCESS PARAMETERS

- Bipolar Performance: 10 GHz Ft with gains greater than 100
- CMOS Performance: 0.5 μm min Leff
- Platinum Schottky diodes for TTL
- Typical ESD Performance: >2000V, Human Body Method
- Robust latch-up and punch-through protection with retrograde wells
- Advanced interconnect supports superior temperature cycle performance

PROCESS CROSS-SECTION

1.0 BCT Cross Section



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Section 2

ABTC Ratings, Specifications and Waveforms

Section 2 Contents

National Semiconductor

ABTC Ratings, Specifications and Waveforms

Definition of Terms

DC Characteristics

Currents: Positive current is defined as conventional current flow into a device. Negative current is defined as current flow out of a device. All current limits are specified as absolute values.

Voltages: All voltages are referenced to the ground pin. All voltage limits are specified as absolute values.

I_{BVI} Input HIGH Current (Breakdown Test). The current flowing into an input when a specified Absolute MAX HIGH voltage is applied to that input.

I_{BVIT} I/O Pin HIGH Current (Breakdown Test). The current flowing into a disabled (output is high impedance) I/O pin when a specified Absolute MAX HIGH voltage is applied to that I/O pin.

I_{CEX} Output HIGH Leakage Current. The current flowing into a HIGH output due to the application of a specified HIGH voltage to that output.

I_{CCH} The current flowing into the V_{CC} supply terminal when the outputs are in the HIGH state.

I_{CCL} The current flowing into the V_{CC} supply terminal when the outputs are in the LOW state.

I_{CCT} Additional I_{CC} due to TTL HIGH levels forced on CMOS inputs.

I_{CCZ} The current flowing into the V_{CC} supply terminal when the outputs are disabled (high impedance).

I_{IL} Input LOW Current. The current flowing out of an input when a specified LOW voltage is applied to that input.

I_{IH} Input HIGH Current. The current flowing into an input when a specified HIGH voltage is applied to that input.

I_{OH} Output HIGH Current. The current flowing out of an output which is in the HIGH state.

I_{OL} Output LOW Current. The current flowing into an output which is in the LOW state.

I_{OS} Output Short Circuit Current. The current flowing out of an output in the HIGH state when that output is shorted to ground (or other specified potential).

I_{OZL} Output OFF current (LOW). The current flowing out of a disabled TRI-STATE® output when a specified LOW voltage is applied to that output.

I_{OZH} Output OFF current (HIGH). The current flowing into a disabled TRI-STATE output when a specified HIGH voltage is applied to that output.

I_{ZZ} Bus Drainage. The current flowing into an output or I/O pin when a specified HIGH level is applied to the output or I/O pin of a power-down device.

V_{CC} Supply Voltage. The range of power supply voltages over which the device is guaranteed to operate.

V_{CD} Input Clamp Diode Voltage. The voltage on an input (−) when a specified current is pulled from that input.

V_{ID} Input Breakdown Voltage. The voltage on an input of a powered-down device when a specified current is forced into that input.

V_{IH} Input HIGH Voltage. The minimum input voltage that is recognized as a DC HIGH-level.

V_{IHD} Dynamic Input HIGH Voltage. The minimum input voltage that is recognized as a HIGH-level during a Multiple Output Switching (MOS) operation.

V_{IL} Input LOW Voltage. The maximum input voltage that is recognized as a DC LOW-level.

V_{ILD} Dynamic Input LOW Voltage. The maximum input voltage that is recognized as a LOW-level during Multiple Output Switching (MOS) operation.

V_{OH} Output HIGH Voltage. The voltage at an output conditioned HIGH with a specified output load and V_{CC} supply voltage.

V_{OHV} Minimum (valley) voltage induced on a static HIGH high output during switching of other outputs.

V_{OL} Output LOW Voltage. The voltage at an output conditioned LOW with a specified output load and V_{CC} supply voltage.

V_{OLP} Maximum (peak) voltage induced on a static LOW output during switching of other outputs.

V_{OLV} Minimum (valley) voltage induced on a static LOW output during switching of other outputs.

AC Characteristics

f_t Maximum Transistor Operating Frequency—The frequency at which the gain of the transistor has dropped by three decibels.

f_{max} Toggle Frequency/Operating Frequency—The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} Propagation Delay Time—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation Delay Time—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_w Pulse Width—The time between 1.5V amplitude points of the leading and trailing edges of a pulse.

t_h Hold Time—The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s Setup Time—The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} Output Disable Time (of a TRI-STATE Output) from HIGH Level—The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} Output Disable Time (of a TRI-STATE Output) from LOW Level—The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

t_{PZH} Output Enable Time (of a TRI-STATE Output) to a HIGH Level—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} Output Enable Time (of a TRI-STATE Output) to a LOW Level—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW levels.

t_{rec} Recovery Time—The time between the 1.5V level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

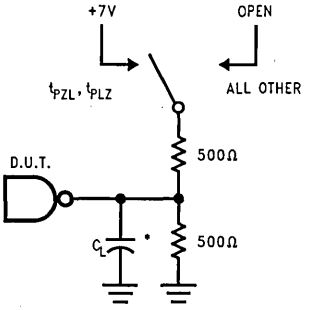
AC Loading and Waveforms

Figure 1 shows the AC loading circuit used in characterizing and specifying propagation delays of all ABTC devices, unless otherwise specified in the data sheet of a specific device. The value of the capacitive load (C_L) is variable and is defined in the AC Electrical Characteristics.

The 500Ω resistor to ground in *Figure 1* is intended to slightly load the output and limit the quiescent HIGH-state voltage to about +3.5V. Also shown in *Figure 1* is a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with open-collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establishes a quiescent HIGH level of +3.5V, which correlates with the HIGH level discussed in the preceding paragraph.

Figures 2a and *2b* describe the input pulse requirements necessary when testing ABTC circuits. *Figures 3* and *5* show waveforms for all propagation delay and pulse width measurements while *Figure 4* shows waveforms for TRI-STATE enable and disable times. The waveforms shown in *Figure 6* describe setup, hold and recovery times. These diagrams define all input and output measure points used in testing ABTC devices.

AC Loading



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*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

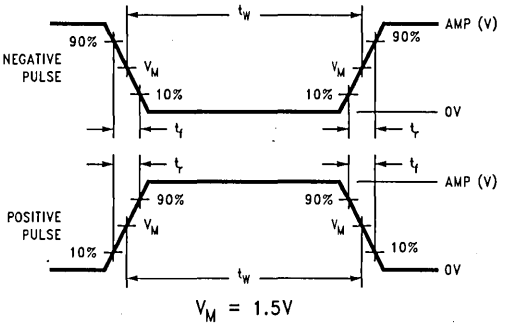

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FIGURE 2a. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Test Input Signal Requirements

AC Waveforms

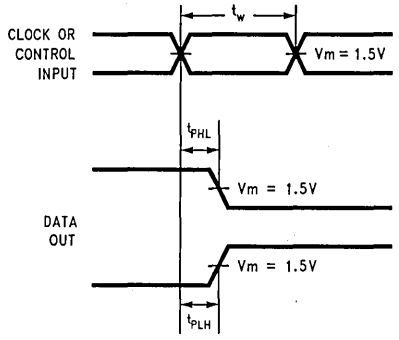

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FIGURE 3. Propagation Delay, Pulse Width Waveforms

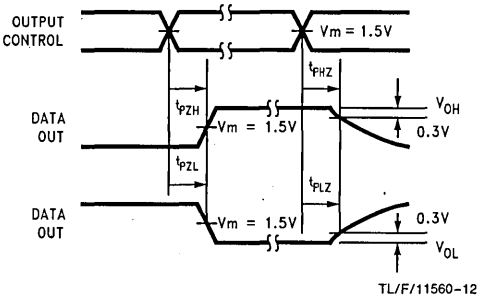

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FIGURE 4. TRI-STATE Output HIGH and LOW Enable and Disable Times

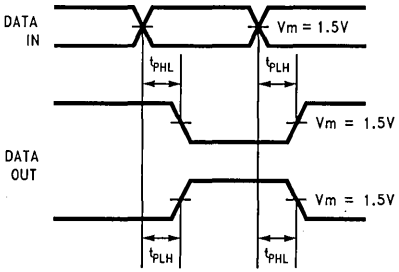

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FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

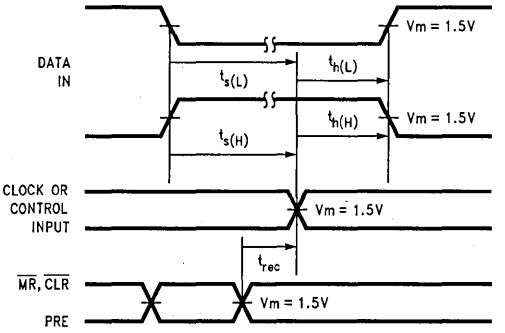

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FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Skew Definitions and Examples

Minimizing output skew is a key design criteria in today's high-speed clocking schemes, and National has incorporated skew specifications into the ABTC family of devices.

This section provides general definitions and examples of skew.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s). See *Figure 8*.

Example:

If signal appears at out #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device, duty cycle and device-to-device delay differences.

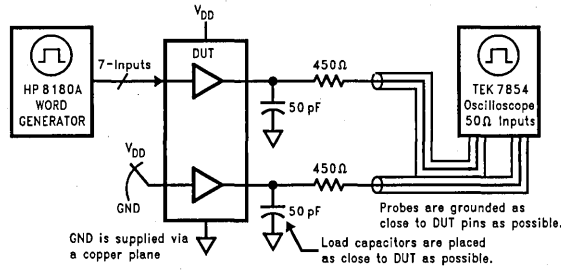

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FIGURE 7. Simultaneous Switching Test Circuit

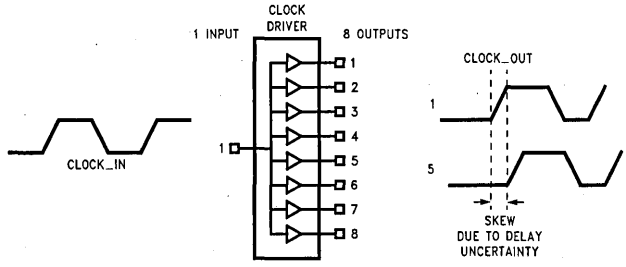

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FIGURE 8. Clock Output Skew

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

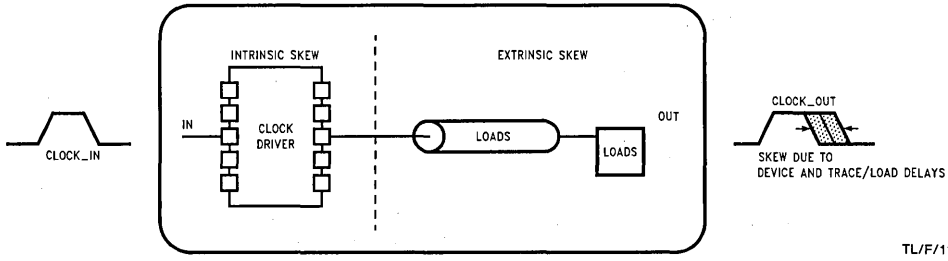

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FIGURE 9. Sources of Clock Skew

Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles

Total system skew budget = 10% of clock cycle = 2 ns* → 2 ns

If extrinsic skew = 1 ns → − 1 ns

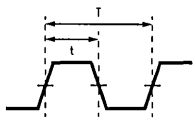
Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design *Rule of thumb.*

Skew Definitions and Examples (Continued)

CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is *High* or *Low* in a given clock cycle.



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Duty Cycle = t/T * 100%

FIGURE 10. Duty Cycle Calculation

Clock Signal

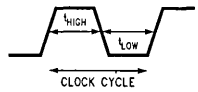

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FIGURE 11. Clock Cycle

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.

Clock + Skew

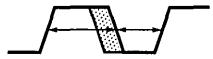

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FIGURE 12. Clock Skew

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE I

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle		
50 MHz	0 ns	10 ns	10 ns	50/50%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%		
50 MHz	1 ns	11 ns	9 ns	55/45%		
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

$t_{OSHL} = |t_{PHL_{MAX}} - t_{PHL_{MIN}}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLH_{MAX}} - t_{PLH_{MIN}}|$

Propagation delays are measured across the outputs of any given device.

Example

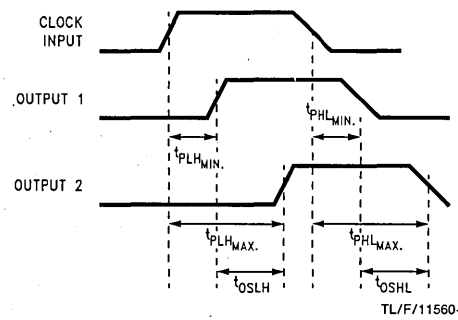

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FIGURE 13. t_{OSLH}, t_{OSHL}

Definition of Parameters (Continued)

t_{PS} (Pin Skew or Transition Skew)

t_{PS}, describes opposite edge skews, i.e., the difference between the delay of the low-to-high transition and the high-to-low transition on the same pin. This parameter is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. Ideally this number needs to be 0 ns. Effectively, 0 ns means that there is no degradation of the input signal's Duty Cycle.

Many of today's microprocessors require a minimum of a 45:55 percent Duty Cycle. System clock designers typically achieve this in one of two ways. The first method is with an expensive crystal oscillator which meets the 45:55 percent Duty Cycle requirement. An alternative approach is to use a less expensive crystal oscillator and implement a divide by two function. Some microprocessors have addressed this by internally performing the divide by two.

Since Duty Cycle is defined as a percentage, the room for error becomes tighter as the system clock frequency increases. For example in a 25 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 4 ns (t_{PLH} of 18 ns and t_{PLH} of 22 ns) and still meet the Duty Cycle requirement. However for a 50 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 2 ns (t_{PLH} of 9 ns and t_{PHL} of 11 ns) and still meet the Duty Cycle requirement. This analysis assumes a perfect 50:50 percent Duty Cycle input signal.

Definition

t_{PS} (Pin Skew or Transition Skew):

$t_{PS} = |t_{PHL} - t_{PLH}|$

Both high-to-low and low-to-high propagation delays are measured at each output pin across the given device.

Example

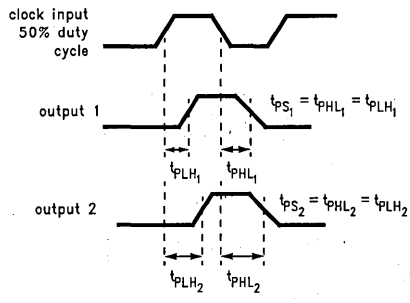

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FIGURE 14. t_{PS}

Example: A 33 MHz, 50/50% duty cycle input signal would be degraded by 2.6% due to a t_{PS} = 0.8 ns. (See Table and Illustration below.)

Note: Output symmetry degradation also depends on input duty cycle.

TABLE II. Duty Cycle Degradation of 33 MHz

f (MHz)	Input			Device	Output			% Δ DC Input to Output
	DC Input	t_{IN} (ns)	T_{IN} (ns)	t_{PS} (ns)	t_{OUT} (ns)	T_{OUT} (ns)	DC Output	
33	**50%/50%**	15.15/15.15	30.3	**0.8**	14.35/15.95	30.3	47.4%/52.6%	**2.6%**
	45%/55%	13.6/16.6	30.3	**1.5**	12.1/18.1	30.3	39.9%/60.1%	**5.1%**

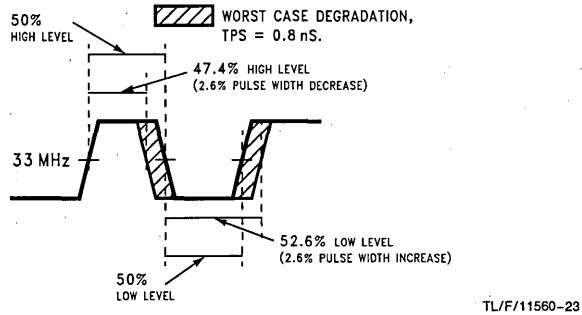

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FIGURE 15. Pulse Width Degradation

Definition of Parameters (Continued)

t_{OST} (Opposite Edge Skew)

t_{OST} defines the difference between the fastest and the slowest of both transitions within a given chip. Given a specific system with two components, one being positive-edge triggered and one being negative-edge triggered, t_{OST} helps to calculate the required delay elements if synchronization of the positive- and negative-clock edges is required.

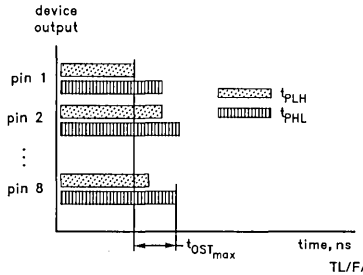

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FIGURE 16. t_{OST}

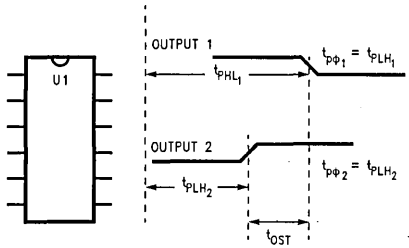
Definition

t_{OST} (Opposite Edge Skew):

$t_{OST} = |t_{P\phi m} - t_{P\phi n}|$

where ϕ is any edge transition (high-to-low or low-to-high) measured between any two outputs (m or n) within any given device.

Example



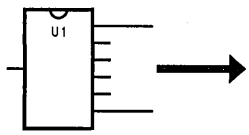
TL/F/11560–25

FIGURE 17. t_{OST}

t_{PV} (Part Variation Skew)

t_{PV} illustrates the distribution of propagation delays between the outputs of any two devices.

Part-to-part skew, t_{PV}, becomes a critical parameter as the driving scheme becomes more complicated. This usually applies to higher-end systems which go from single clock drivers to distributed clock trees to increase fanout (shown below). In a distributed clock tree, part-to-part skew between U2 and U3 must be minimized to optimize system clock frequency. In the case of the clock tree, the total skew becomes a function of $t_{OSLH/HL}$ of U1 plus t_{PV} of U2 and U3.

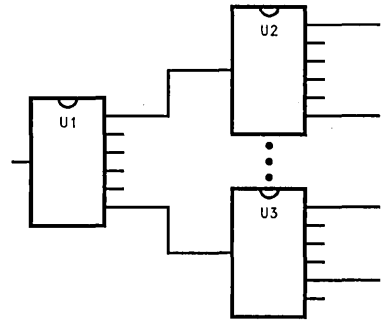


TL/F/11560–26

FIGURE 18. Clock Distribution

Case 1: Single Clock Driver

Total Skew = Pin-to-Pin Skew U1
= t_{OSLH} or t_{OSHL} of U1



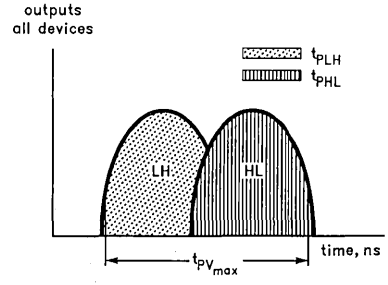
TL/F/11560–27

Definition

t_{PV} (Part Variation Skew):

$t_{PV} = |t_{P\phi u,v} - t_{P\phi x,y}|$

where ϕ is any edge transition (high-to-low or low-to-high) measured from the outputs of any two devices.



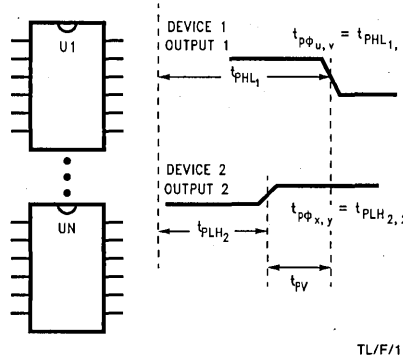
TL/F/11560–28

FIGURE 19. t_{PV}

Case 2: Distributed Clock Tree

Total Skew (U2, U3) = Pin-to-Pin Skew (U1) + Part-to-Part Skew (U2, U3)

Example



TL/F/11560–29

FIGURE 20. t_{PV}

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics (except as noted on device datasheet)

Symbol	Parameter		ABT245C Min	ABT245C Typ	ABT245C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5 5	μA	Max	V_{IN} = 2.7V V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	μA	Max	V_{IN} = 5.5V
I_{IL}	Input LOW Current				−5 −5	μA	Max	V_{IN} = 0.5V V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V (I/O Pins)
I_{IL} + I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V (I/O Pins)
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	V_{OUT} = HIGH Z
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or GND
								$\overline{OE}$ = V_{CC}; V_{OUT} = HIGH Z

Characterization and Extended Test Specifications

Philosophy

During the National new product introduction process for logic IC's, a new ABTC IC design will undergo a rigorous characterization to baseline its performance. This data is required to correlate with simulation models, determine product specifications, compare performance to other product, provide a feedback mechanism to the fabrication process, and for customer information. National's Logic IC characterizations are designed to get as much information as possible about the product and potential customer application performance.

National's logic IC characterization methodology uses past knowledge of design performance, simulation, and process parametrics to determine what electrical parameters to characterize. Characterization samples are selected so that they have key process parametrics (e.g., Drive, Beta, V_{tn}, V_{tp} L_{eff}, etc.) which have been shown to significantly affect device electrical parameters. Data is acquired and processed using statistical analysis software. Manufacturing test limits are then set using the knowledge of variations due to fabrication, package, tester, V_{CC}, temperature, and condition. This allows product to be shipped on demand without problems or delays.

The following are brief summaries of characterization tests performed.

Test Summaries

AC Electrical Characteristics

Single Output Switching propagation delays
Testing includes measured propagation delays at 50 pF and 250 pF output load capacitances.

t_{PLH} t_{PHL}	Active Propagation Delays
t_{PZH} t_{PZL}	Enable Propagation Delays
t_{PLZ} t_{PHZ}	Disable Propagation Delays

Also included are input timing parameters

t_S	Setup Time
t_H	Hold Time

Multiple (Simultaneous) Output Switching Propagation Delays
These tests are used to ensure compliance to the extended databook specifications and include active propagation delays, disable and enable times at 50 pF and 250 pF output loads.

Multiple Output Switching Skew
Performance data from the Multiple Output Switching propagation delay testing is analyzed to obtain information regarding output skew of an IC.

FMAX (synchronous logic)
FMAX determines the minimum frequency at which the device is guaranteed to operate for a clocked IC. This test is package and test environment sensitive.

Pulse Width (synchronous logic)
Pulse Width testing is used to define the minimum pulse duration that a flip-flop or latch input will accept and still function properly. This test is package and test environment sensitive.

F-Toggle (asynchronous logic)
F-Toggle is the minimum frequency at which the IC is guaranteed to function under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

AC Dynamic (Noise) Characteristics

V_{OLP}, V_{OLV}—Ground Bounce (Quiet Output Switching)
Measured parameters with 50 pF loading relate the amount that a static conditioned output will change in voltage under multiple outputs switching condition with outputs operating in phase. They are heavily influenced by the magnitude that V_{CC} and Ground move internal to the IC.

V_{ILD}, V_{IHD}—Dynamic Threshold
Dynamic threshold measures the shift of an IC's input threshold due to noise generated while under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

Input Edge Rate
This test is performed to determine what minimum edge rate can be applied to an input and have the corresponding output transition with no abnormalities such as glitches or oscillations.

DC Electrical Characteristics

Automated Test Equipment (ATE) DC Tests
DC test data gathered show the performance of an IC to statically applied voltages and currents.

Functional Shmoo
The function shmoo shows the function operational window of an IC at a wide range of V_{CC}'s and temperatures.

Power Up & Power Down Output Shmoo
Similar to the function shmoo, the power up and power down output shmoo shows the DC operation of an output during power up and power down conditions.

Transfer Characteristic (V_{IN}/V_{OUT})

Input Traces (V_{IN}/I_{IN})
Output Traces (V_{OL}/I_{OL}, V_{OH}/I_{OH})

Power

Power-Up I_{CC} Traces
Shows how the supply current reacts to various input conditions during power up.

I_{CC} vs V_{IN} Traces
Traces of I_{CC} vs V_{IN} show how the supply current changes with input voltage.

Power (Continued)

I_{CCD} (Dynamic I_{CC})

Determines the amount of current an IC will consume at frequency.

Capacitance

Input/Output Capacitance (C_{IN}/C_{OUT})

Reliability Tests

Latch-up

Testing determines if an IC is susceptible to latch-up from over-current or over-voltage stresses per MIL-STD-883 JEDEC method 17.

HBM Electrostatic Discharge, Human Body Model

Per MIL-STD-883C method 3015.6.

Extended Specifications

With the introduction of the ABTC product family, National has taken new steps in aiding the system designer with a better method to predict device performance in his application. National now offers system oriented performance specifications so a designer can feel confident in the way a device will preform over a wider variety of switching conditions. Performance specifications in the form of Extended Specifications are provided with each product datasheet

In the past, most extended databook specifications depended on a representative product family function to provide the guaranteed performance data for the rest of the family. The drawback from this method of test and specmanship leaves rather large process, tester and function guardbands in the final maximum or minimum specifications. The test data for National's ABTC product family, taken during product development on each function, provides the ABTC family with device specific and guaranteed extended specifications that can be passed directly to the system designers. National offers the extended specifications with the belief that customers can reduce their incoming test requirements and in essence reduce the cost and time for product design-in.

Additional guaranteed specifications provided by National include: Single Output Switching (SOS) for 250 pF loads; Multiple Output Switching (MOS) for 50 pF and 250 pF loads; Skew; Quiet Output Switching (QOS) V_{OLP}, V_{OLV}, V_{OHP}, V_{OHV} and Dynamic Threshold (DVTH), V_{ILH}, and V_{IHD}.

Each of the guaranteed extended specifications involve multiple output switching events, with exception to the SOS specifications. During a multiple output switching event, stray inductance and capacitance inhibit product performance. National has developed standardized hardware that aligns with the industry for ABTC product evaluations. Some of the features of the test fixturing include ground planes and low inductive connections, critical in evaluating the product and not the fixture. See Section 2.7 for more information on test fixture hardware.

The extended specfication tests have very similiar if not identical test setups. The results of the measurements from each test depend on the application focus. The quantitative analysis from the tests provides insight into product performance. The parameters and typical results from each test type can be easily explained in the sections that follow. Sample plots are generated from National's ABT244C and represent room temperature data at 5.0V V_{CC}.

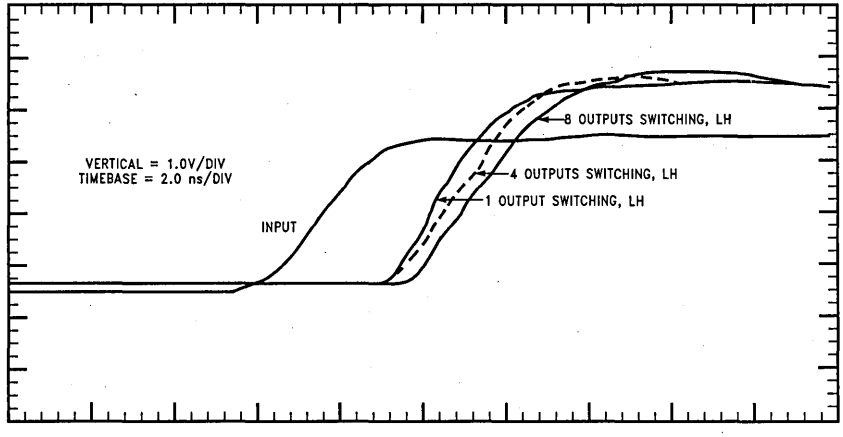
TABLE III. Test Conditions for MOS, Skew, QOS, DVTH

Parameter	Value
Input Edge Rate	2.5 ns
Input Skew	< 300 pS
Input Amplitude	0V to 3.0V
Input Frequency	1 MHz
Output Load	50 pF, 500Ω; 250 pF, 500Ω

MULTIPLE OUTPUT SWITCHING

Multiple output switching simulates a worst case switching environment. With input edges deskewed to < 300 pS, the device has to provide simultaneous switching current for the output. The cumulative effect of environmental inductance and capacitance impacts the output edge rate and ultimately impacts propagation delay and noise immunity performance.

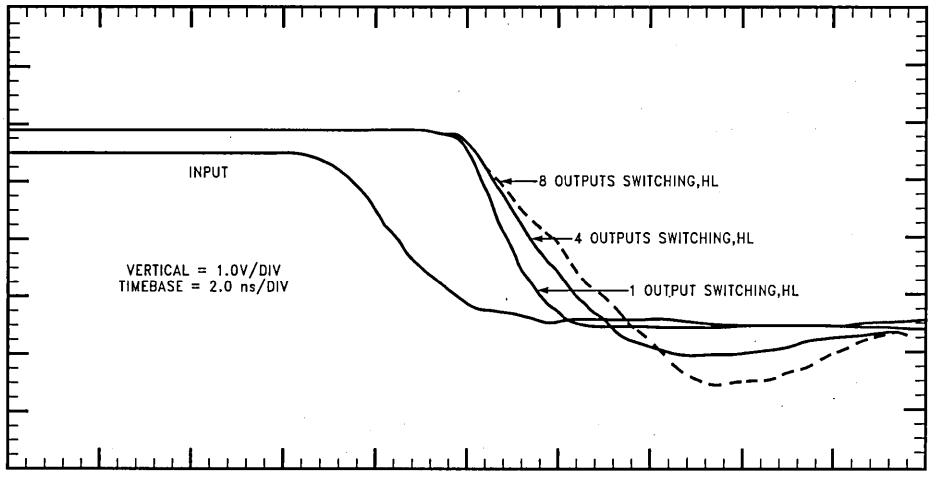
The plots of *Figures 21–26* demonstrate the ability of the ABTC product family to minimize enviromental inductance and capacitance effects as well as propagation delay degradation from increased number of outputs switching.



TL/F/11560–30

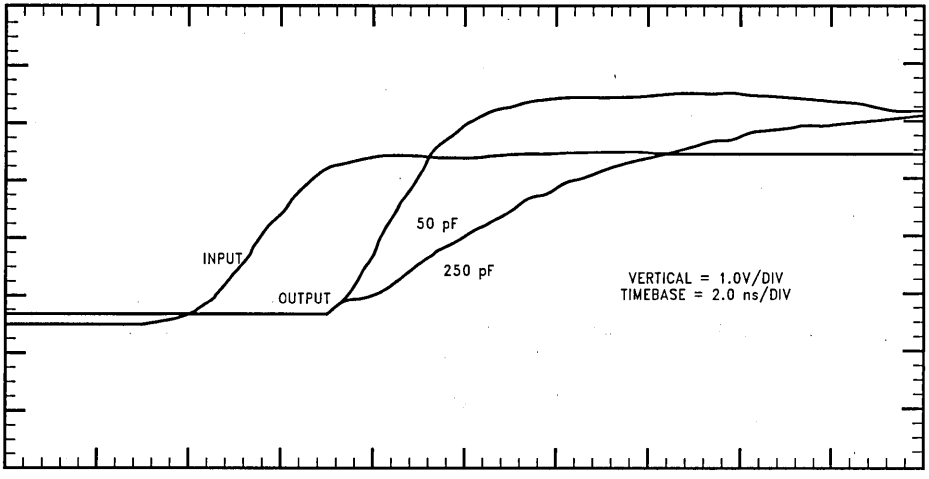
FIGURE 21. Multiple Outputs Switching, LH, 1, 4, 8 Outputs
74ABT244C, V_{CC} = 5.0V, T_A = 25°C

Extended Specifications (Continued)



TL/F/11560–31

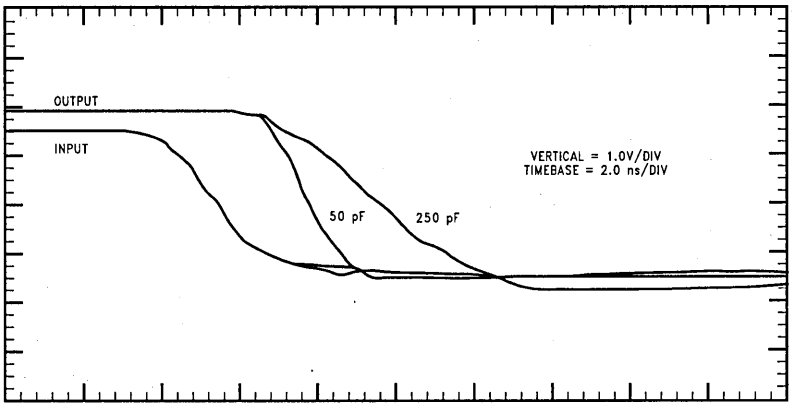
FIGURE 22. Multiple Output Switching, HL, 1, 4, 8 Outputs
74ABT244C, V_{CC} = 5.0V, T_A = 25°C



TL/F/11560–32

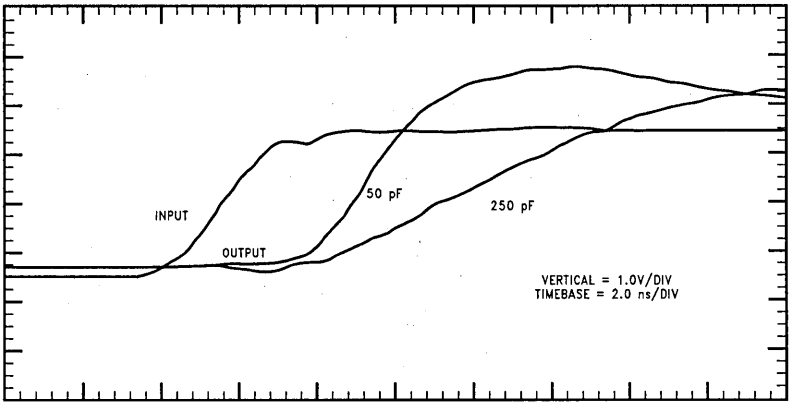
FIGURE 23. Single Output Switching, LH, 50 pF, 250 pF Capacitive Loading
74ABT244C, V_{CC} = 5.0V, T_A = 25°C

Extended Specifications (Continued)



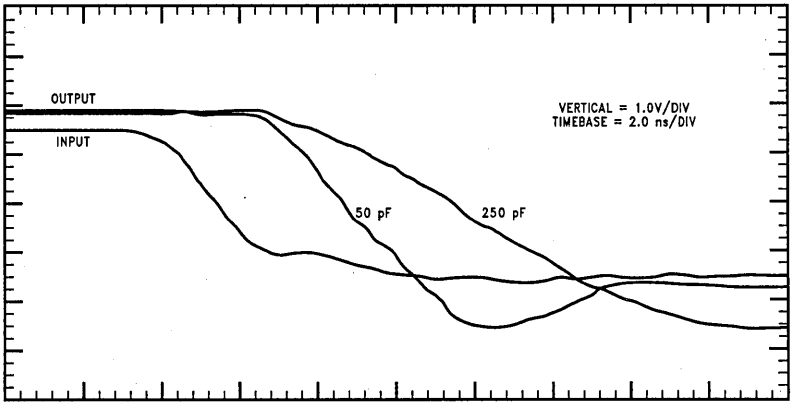
TL/F/11560–33

FIGURE 24. Single Output Switching, HL, 50 pF, 250 pF Capacitive Loading
74ABT244C, V_{CC} = 5.0V, T_A = 25°C



TL/F/11560–34

FIGURE 25. Multiple Outputs Switching (8) LH, 50 pF, 250 pF Capacitive Loading
74ABT244C, V_{CC} 5.0V, T_A = 25°C



TL/F/11560–35

FIGURE 26. Multiple Output Switching (8) HL, 50 pF, 250 pF Capacitive Loading
74ABT244C, V_{CC} = 5.0V, T_A = 25°C

Extended Specifications (Continued)

SKEW

Skew specifications provide a system designer with up front critical timing information to speed design cycle time. Skew measurements are derived from MOS propagation delay data rather than SOS propagation delay data. The advantage of MOS skew from a design engineer's viewpoint, is that MOS is a more realistic condition under which skew becomes critical.

Three modes of skew testing are published for each device in the ABTC product family. Each skew mode describes a variance either within a pin (i.e. duty cycle), across to pins or across parts (i.e. process) for a given device function.

Within-a-Pin Skew, t_{PS}

Within-a-pin skew is designated by t_{PS} (pin skew), and describes each pin on a part and its ability to maintain 50% duty cycle. Pin skew is a calculation from the MOS propagation delays, t_{PLH} and t_{PHL} on each pin.

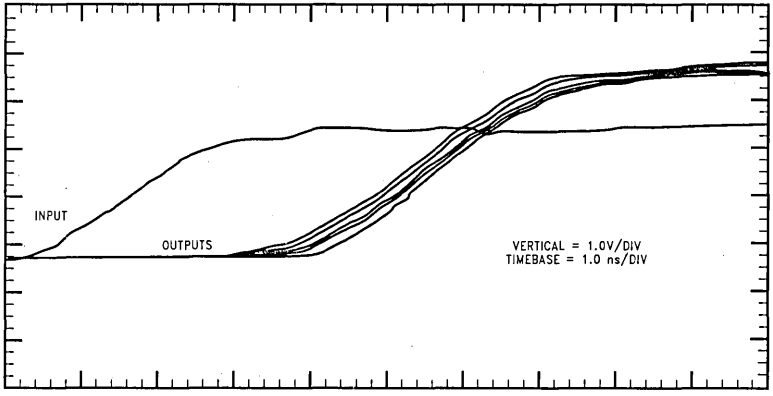
Across-Pin Skew, t_{OS}

Across-pin skew is designated by t_{OS} (output skew), and describes the MOS output edge difference across all output pins on a part. Across-pin skew can be broken down further into t_{OSLH}, t_{OSHL} and t_{OST}. The $(_{LH})$ indicates that output skew is measured across all outputs while switching low-to-high. The $(_{HL})$ indicates output skew measured on the high-to-low transition. The (t) infers that skew is measured across the outputs independent of a low-to- high or high-to-low edge or total output skew. Total output skew is calculated from the MOS propagation delays, t_{PLH} and t_{PHL}, across all pins.

Across-Part Skew, t_{PV}

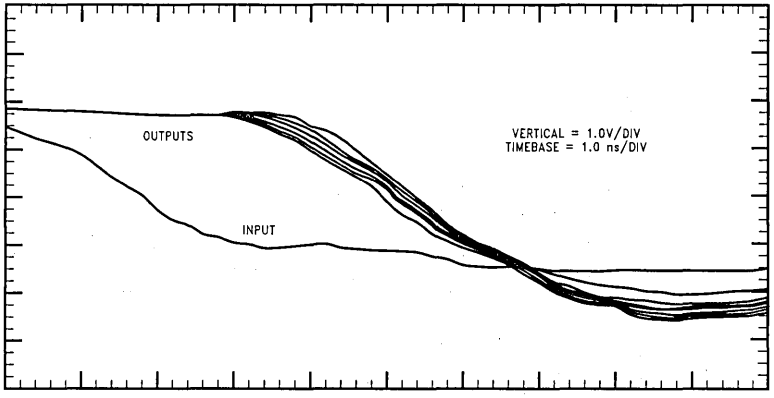
Across-part skew is designated by t_{PV} (part variation), and describes the MOS output edge difference across all output pins on all parts in the population. Across-part skew is calculated from the MOS propagation delays, t_{PLH} and t_{PHL}, across all pins and all parts.

The plots in *Figures 27–28* describe skew performance in a 50 pF, 500Ω environment.



TL/F/11560–36

FIGURE 27. Skew 8 Outputs Switching, LH
74ABT244C, V_{CC} = 5.0V, T_A = 25°C



TL/F/11560–37

FIGURE 28. Skew 8 Outputs Switching, HL
74ABT244C, V_{CC} = 5.0V, T_A = 25°C

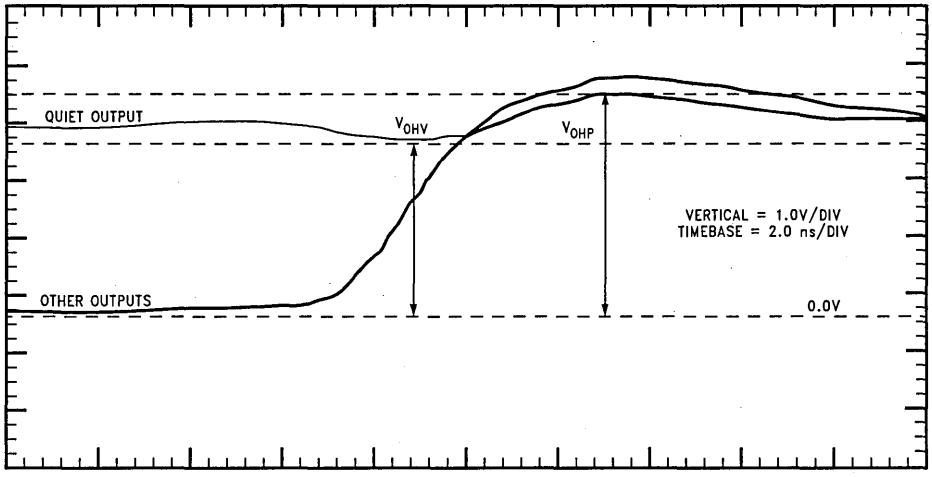
Extended Specifications (Continued)

QUIET OUTPUT SWITCHING

Quiet output switching, (QOS), specifications provide the system designer quantification of ABTC's effective control of noise and performance to threshold specifications. The QOS specification is a representation of the resultant shift of an output voltage, either from a static high or low level on a single bit, while the other bits switch simutaneously in phase. The voltage shift from a quiet output is specified through four parameters.

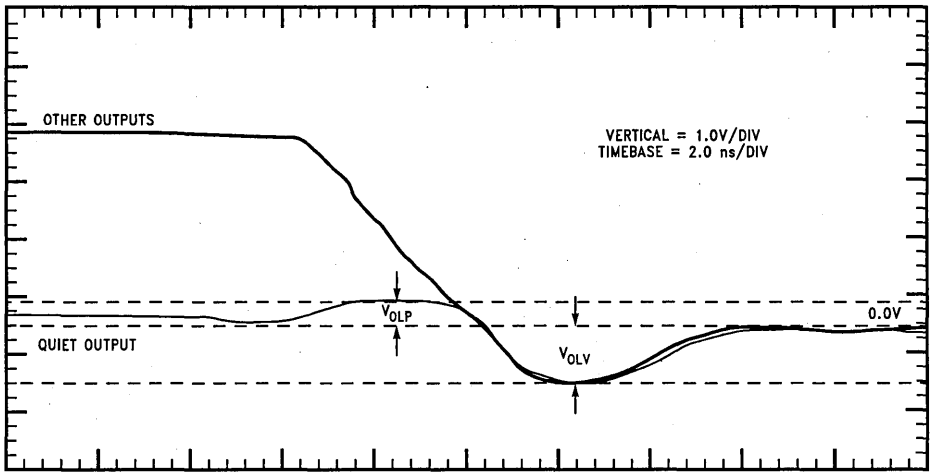
- V_{OLP} and V_{OLV} describe the peak or valley of a voltage shift for a quiet output low level.
- V_{OHP} and V_{OHV} describe the peak or valley of a voltage shift for a quiet output high level.

The concern for the system designer evolves from the possiblity that the quiet output voltage shift could impact attached circuitry. V_{OLP} values on some product families peak above threshold high and become recognized as a logic HIGH. The period of time the voltage shift spends in the opposite state is short, in the neighborhood of 10–100 pS, and may not disrupt sequencial circuitry if it is level sensing. If the attached circuitry needs a rising edge, such as a clock input, the sequencial circuitry may take the inadvertent deflection and interpret it. National provides the QOS specification to assist in noise margin planning.



TL/F/11560–38

FIGURE 29. V_{OLP}, V_{OLV}
LH Transition
74ABT244C, V_{CC} = 5.0V, T_A = 25°C



TL/F/11560–39

FIGURE 30. V_{OLP}, V_{OLV}
HL Transition
74ABCT244C, V_{CC} = 5.0V, T_A = 25°C

Extended Specifications (Continued)

DYNAMIC THRESHOLD

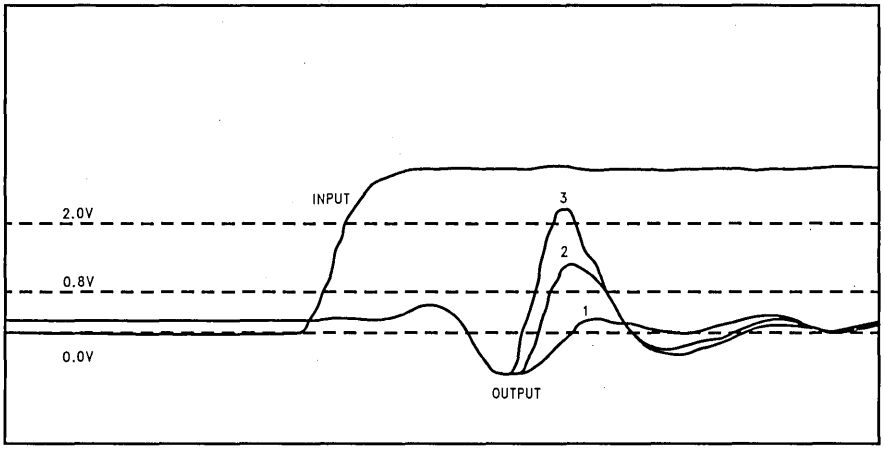
Dynamic threshold data, (DVTH), like QOS data, provides the system designer with noise performance criteria. DVTH specifications quantify the magnitude of output voltage deflection that a logic high or low might experience under an MOS switching condition. The voltage deflection is a result of an apparent shift of an input's threshold due to noise generated from MOS switching on the internal die ground and V_{CC} busses. The phenomenon occurs during any logic state transition: LH, HL, ZL, etc. As a practice, National determines the worse case transition for each product and generates the specification based on that transition.

Dynamic threshold specifications are denoted by the nomenclature, V_{ILD} and V_{IHD}, where the "D" represents "Dynamic". The definitions for each are as follows,

- V_{ILD} - The maximum LOW input level such that normal switching/functional characteristics are observed on the output
- V_{IHD} - The minimum HIGH input level such that normal switching/functional characteristics are observed on the output

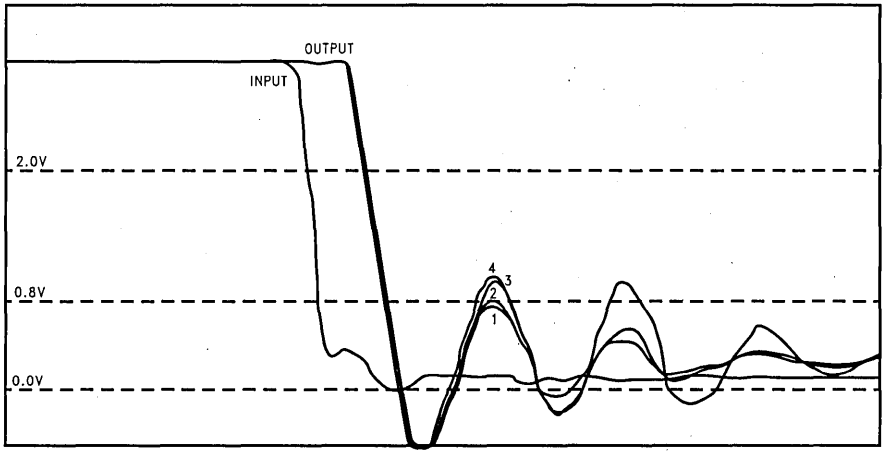
Dynamic threshold failures are bundled into five main failure modes. The most predominant failure is an output deflection in violation of an input threshold level. Others include propagation delay step out in excess of an MOS propagation delay specification, state changes and oscillations. A detailed definition of each failure can be described as follows,

1. On a low output, the LOW level will not rise above an input threshold low level of 0.8V after the transition of the output. *Figures 31* and *32*. Numbered output curve deflections are a result of 10 mV incremental changes on the low input signal level.



TL/F/11560–40

FIGURE 31. V_{ILD} 7 Outputs Switching
V_{CC} = 5.0V, T_A = 25°C

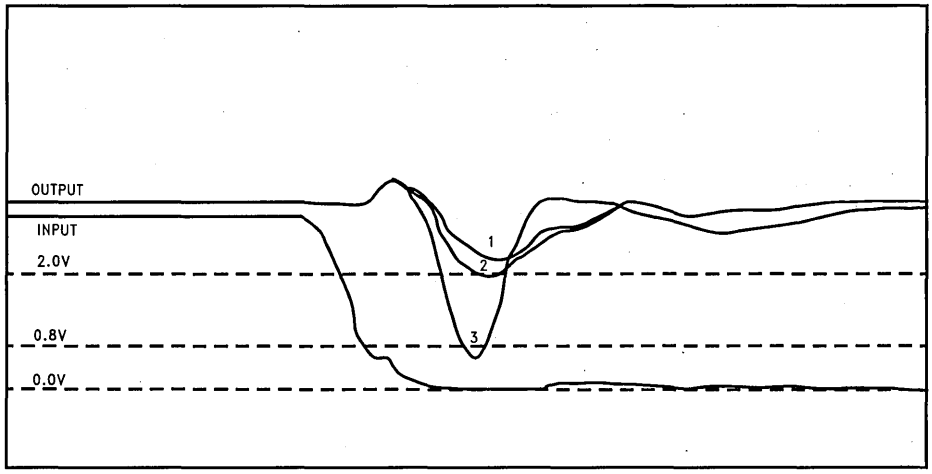


TL/F/11560–41

FIGURE 32. V_{ILD} 8 Outputs Switching
V_{CC} = 5.0V, T_A = 25°C

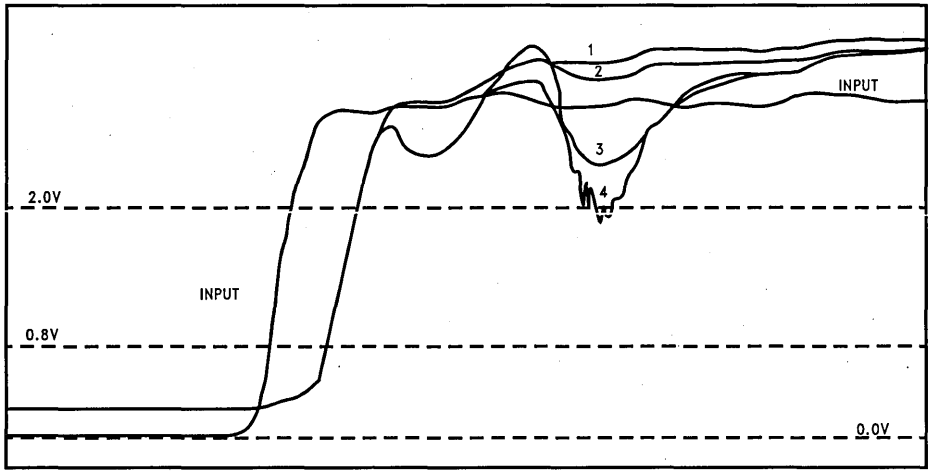
Extended Specifications (Continued)

2. On a high output, the HIGH level will not drop below an input threshold high level of 2.0V after the transition of the output. *Figures 33* and *34*. Numbered output curve deflections are a result of 10 mV incremental changes on the high input signal level.



TL/F/11560–42

FIGURE 33. V_{IHD}
7 Outputs Switching
V_{CC} = 5.0V, T_A = 25°C

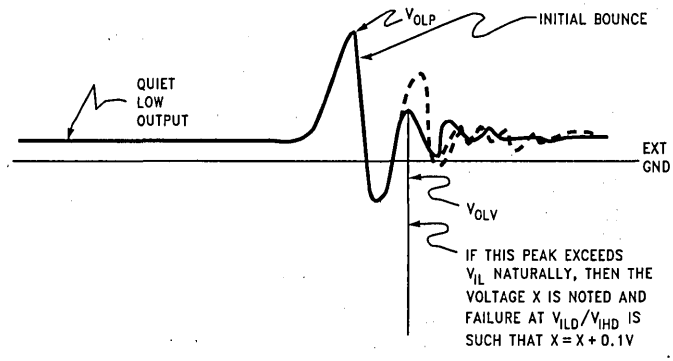


TL/F/11560–43

FIGURE 34. V_{IHD}
8 Outputs Switching
V_{CC} = 5.0V, T_A = 25°C

Extended Specifications (Continued)

3. If the natural ringing, other than the initial bounce, of the output violates an input threshold level, the starting voltage level is noted and monitored until a 100 mV amplitute change towards threshold. If no amplitude change occurs, then the next peak or valley on the output is monitored for input threshold violation. *Figure 35.*
4. The propagation delay is monitored and is determined a failure when it exceeds the MOS propagation delay for that transition.
5. Gross failures including oscillation and functional state changes.



TL/F/11560–44

FIGURE 35

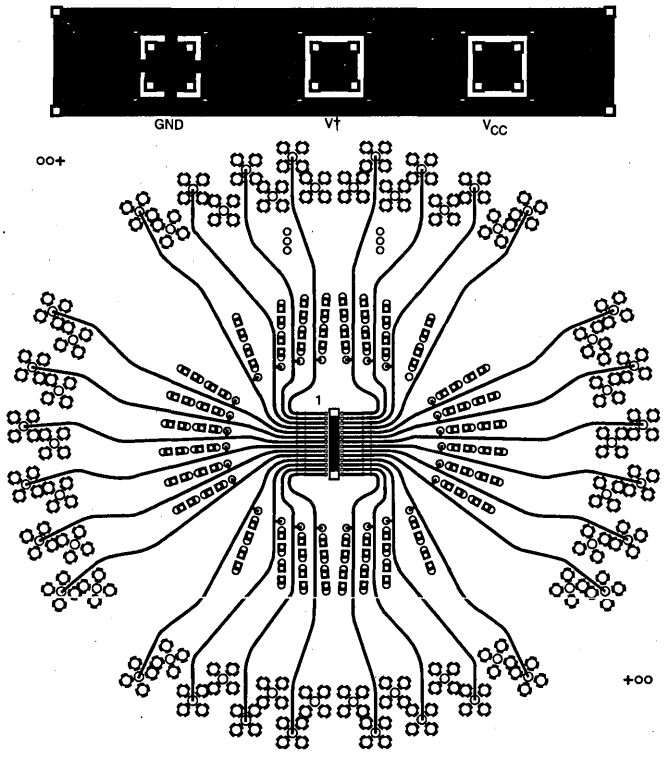
Characterization Fixture

With the introduction of ABTC product family with system level specifications that are guaranteed in a high performance AC enivronment, there is a necessity for a precise and repeatable test environment. Keeping in mind the defacto standards presented by Philips ABT fixture coupled with the understanding that our customers would like to correlate performance of like technologies, National reproduced an electrical equivalent AC fixture to that of the Signetics board documented in their Application Note 602.

To maximize correlation to National's product characterization one must match the environment in which the product was evaluated and make sure that National's implementation of load configuration, board, and DUT connection is followed as shown below.

Unique device pinouts, (20-, 24-, 48-lead, etc.) are used to obtain picosecond accuracy and repeatability. For this reason NSC recommends values of lumped and distributed capacitance used on its AC fixtures to prevent large variations in speed affected by transmission line capacitance.

Bare Board Front Layout Shown

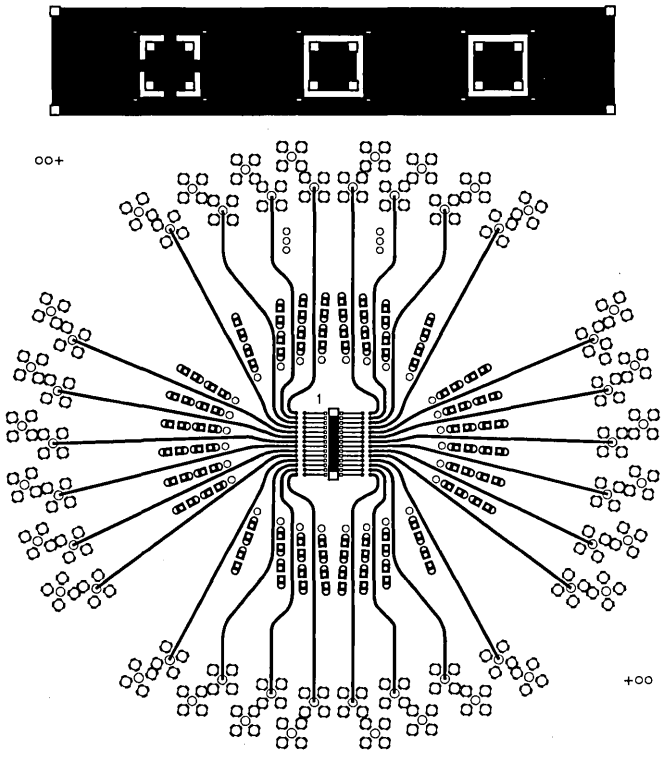


TL/F/11560–1

FIGURE 36. 28-Pin SOIC TOP (Viewed from Top)

Characterization Fixture (Continued)

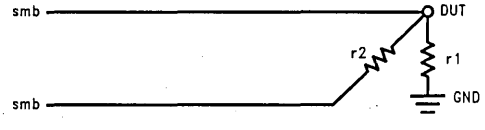
Bare Board Back Layout Shown



TL/F/11560–2

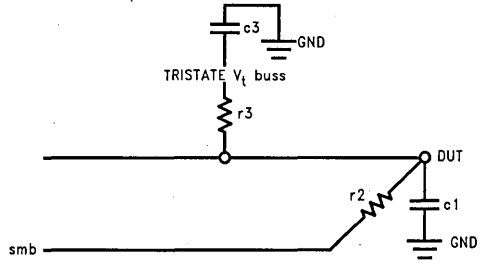
FIGURE 37. 28-Pin SOIC BOTTOM (Viewed from Top)

The blank AC fixture board can be used to implement the following input and output loads and terminations to provide the most repeatable environment in which to test a device.



TL/F/11560–3

FIGURE 38. Input



TL/F/11560–4

FIGURE 39. Output (TRI-STATE/Open Collector)

Characterization Fixture (Continued)

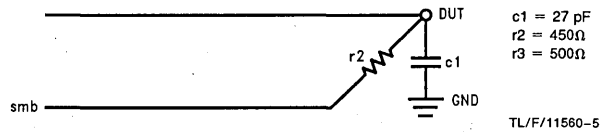


FIGURE 40a. Output (2-State)

Note: TRI-STATE and V_{IH} busses are bypassed to ground with a 0.1 μF capacitor V_{IH}/TRI-STATE Buss.

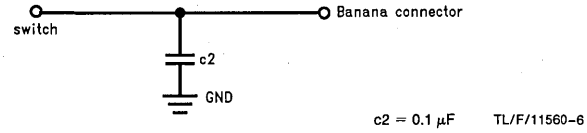


FIGURE 40b

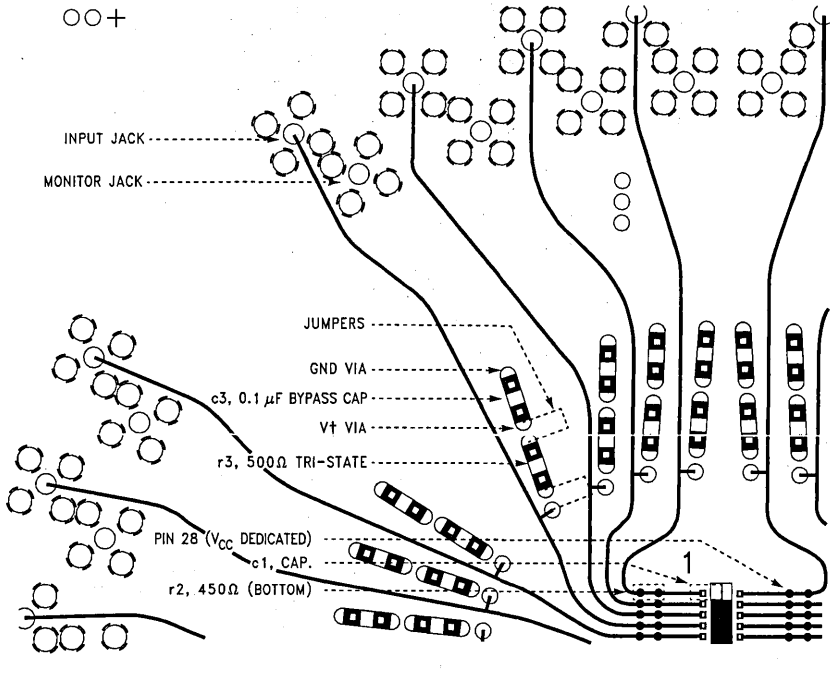


FIGURE 41. Component Placement on PC Board

National's AC fixture has the advantage of providing:

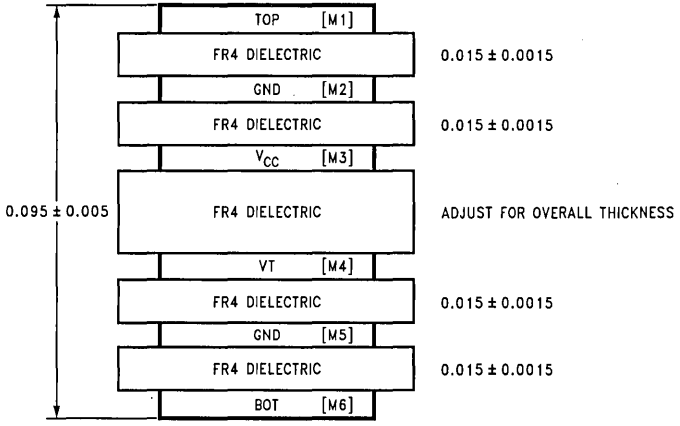
- — low inductance V_{CC} and GND connections
- — V_{CC} and GND planes to minimize cross talk and enhance power supply by-passing
- — equal length 50Ω impedance signal and monitor lines to eliminate skew
- — 50Ω input termination for ease of use
- — 10:1 voltage reduction of the input and output signals to provide ease of use with standard oscilloscope inputs
- — TRI-STATE load is integrated onto the same AC fixture and is connected via jumper to alleviate shunting effects when it is not required

Traces are spaced, and monitor lines are placed, on a different plane than the signal lines to reduce cross talk. *Figure 42* shows a cross section of layers used in the manufacture of National's AC test board. Vias in the signal trace are not used to ensure bandwidth. Ground connections are directly underneath the DUT to reduce the distance to the ground plane. Sense resistors are located directly adjacent to the DUT to reduce reflections.

Characterization Fixture (Continued)

For connection of the device to the board, a custom socket firmly presses the device against the board traces without any layers in between that add inductance or change their resitivity over temperature. The socket provides a minimum of contact resistance for the most accurate results. National designed a custom surface mount socket that provides the needed performance without damaging the device under test. Because of its shape and appearance, we call it the ferrari fixture.

In the characterization of National's product, we made efforts to correlate performance with other manufacturers. If a customer wishes to verify NSC results and requires an AC fixture, we recommend using Signetics AN-602 to build one. While the board that National uses is probably cost equivalent to the Signetics board, the socket used is expensive. If you wish to build a National fixture, please call the factory at 1-800-341-0392 and ask for applications. We can provide you with the component and manufacturer list for a National board along with a socket.



TL/F/11560–8

FIGURE 42. Layer Stacking Diagram

Section 3

Quality and Reliability

Section 3 Contents

National Semiconductor

Quality and Reliability

Introduction

Product qualification is a disciplined, team activity which focuses on demonstrating, through the acquisition and analysis of engineering data, that a device design, fab process, or package design meets or exceeds minimum standards of performance. In most cases, this involves running samples of product through a series of tests which expose the samples to operating stresses far in excess of those which would be encountered in even the most severe "real life" operating environment. These tests are called either accelerated stress tests or accelerated life tests. A properly designed qualification test sequence exposes, within a matter of days or weeks, those design, materials, or workmanship defects which would lead to device failure in the customer's application after months or even years of operation.

In order to be considered a "world class" supplier of semiconductor devices, NSC designs and manufactures products which are capable of meeting the reliability expectations of its most demanding customers. While customer requirements and expectations vary on the subject of reliability requirements for devices, virtually all large users have general procurement specifications which establish failure rate goals or objectives for the suppliers of the components used in their products.

Failure rate goals for infant mortality and long-term-failure-rate-in-service have been established for all NSC product lines. These goals are published internally at the beginning of each fiscal half-year (usually June and December). The actual performance of the product against these goals is measured monthly using life test data gathered from various sources including the Fast Reaction and Long Term Audit Program. Performance is reviewed every six (6) months by Reliability and Product Group management and adjusted as necessary to reflect customer expectations, competitive data, and/or historical performance trends.

Given that product reliability is an overriding corporate objective, and that any deficiency in design, materials, procedures, or workmanship, has a potential for adversely affecting the reliability of the product, Manufacturing and Engineering organizations within NSC, its subsidiaries, and its sub-contractors, involved in introducing a new device, process, or package, share a joint responsibility for demonstrating that the product does conform to NSC standards and to the standards and expectations of NSC's customers.

As a matter of policy, it is NSC's goal to design and manufacture product that is 100% defect-free and capable of surviving the qualification tests with zero failures. This policy is not interpreted as a directive to abandon a qualification program when failures occur or to delay new product releases until perfection has been achieved. Rather, the policy is intended to focus engineering resources on the identification and elimination of the design, process, or workmanship deficiencies that are the root causes of the failures and then to engineer a solution to correct those deficiencies.

Results from the initial qualification for the ABTC family are published in the BiCMOS LOGIC self qualification handbook. Additional stress testing is performed regularly as a reliability monitor as part of the Fast Reaction Program and Long Term Audit Program. The BiCMOS Logic self qualification handbook contains the data typically requested by customers as part of joint qualification programs in addition to detailed explanations of all tests performed. The BiCMOS Logic self qualification handbook may be obtained by contacting Logic QA at 1-800-775-8100, x8208.

Qualification Requirements for Logic Integrated Circuits

Test	Test Method	Test/Stress Conditions	Sample Size Each Lot
Operating Life	SOP-5-049-RA Method 107	1000 Hours @T_A = 125°C	77
High Temperature Storage	SOP-5-049-RA Method 103	1000 Hours @150°C	45
Temperature Cycle	SOP-5-049-RA Method 105	1000 Cycles −65°C to +150°C	77
Temperature Cycle with Preconditioning	SOP-5-049-RA Method 105	1000 Cycles −65°C to +150°C	77
Temperature-Humidity-Bias	SOP-5-049-RA Method 104	1000 Hours 85°C @ 85%RH	77
Temperature-Humidity-Bias with Preconditioning	Method 112 Method 104	Precondition plus 100 hours 85°C to 85%RH	77
Autoclave	Method 101	500 hours 121°C @ 15 psig	45
Thermal Shock	Method 106	100 Cycles −65°C to +150°C	22
Salt Atmosphere	Method 209	25 Hours 35°C	22
Resistance to Solvents	Method 207	4 Solvents	3 Each Solvent
Lead Integrity	Method 205	Condition as Appropriate to Package	22 Leads
Solderability	Method 203	8 Hour Steam 5 secs @260°C	22
Solder Heat	Method 204	12 secs 260°C	22

Quality Information and Communication (QUIC) System

BACKGROUND

National's Quality Assurance Systems Development group (QASD) maintains a variety of data tracking systems such as: Electronic Reliability Data Management (ERDM), Failure Analysis (F/A), Burn-in Board Inventory, and a number of others.

QUIC users will find a user friendly, menu-driven, real-time system that gives them a simultaneous-user environment with timely data inputs from sites around the world. QUIC is programmed to recognize each individual user of the system at the point of logging on to the mainframe, and provides an appropriate list of menu options consistent with the user's level of access requirements.

National grants access to QUIC by customers that provides a sufficient level of security over the entire system, thus precluding the possibility of accidental access (or even damage) to various files.

HOW A CUSTOMER LINKS TO QUIC

1. Check to make sure you have the hardware components listed below. (An attached printer is desirable but not imperative.)

   IBM/PC compatible computer with at least 128k memory.

   Hayes compatible 1200 baud modem (or 2400, 4800 or 9600).

   Touch tone phone.
2. Request access to QUIC by contacting your National sales representative or Customer Service Center at 1-800-272-9959, who will coordinate all activities necessary to provide access for your company and arrange training (usually handled over the telephone).
3. Identify the person who will be your company's main contact and user of the QUIC system. This person will assume responsibility for the USERID assigned to your company and will receive training on how to access and use the QUIC system.
4. National will provide a USERID, password and account number with appropriate menus and a communications software package called EXECULINK, which allows the customer's PC to talk with NSC's host computer and also turns the PC into a virtual host terminal, with full-screen editing capability and full use of program function (PF) keys. EXECULINK also provides for file transferring between host and PC and spooling of print files to a PC-attached printer.

ONGOING IMPROVEMENTS

As we receive feedback from the users of QUIC, we (QASD) will continue to enhance the "User Friendliness" of the system and add new features which, we hope, will help promote a true sense of teamwork between us and our customers.

Wafer Level Reliability (WLR)

BACKGROUND

The conventional methods of reliability screening, that of short-term burn-in to eliminate infant mortalities and long-term life tests at high temperature, will soon become impractical for many devices. The reasons for this are tighter infant mortality ppm requirements, higher costs, and shortened lifetimes.

As device complexity increases, the testing sample size required to ensure infant mortality ppm levels in the 0–10 ppm range will quickly deplete reliability test capacity. While burn-in eliminates inferior devices, it can also substantially shorten the lifetimes of "good" devices to an unacceptable level, creating an expensive and somewhat risky procedure. New technology advances which minimize geometry, have moved our device lifetime distributions closer to our customer's expected system life. As device geometries shrink, resulting in higher current densities, electric fields, and chip temperatures, tighter fab process control and instant feedback become critical.

THE GOAL OF WAFER-LEVEL-RELIABILITY TESTING-PROCESS RELIABILITY

Wafer-level-reliability testing represents a proactive, correlation and control approach to ensuring device reliability. WLR is not meant to replace classical reliability testing. Instead it is used to supplement existing methods.

WLR testing is used to:

1. Identify shifts in On-Line Process Controls (fab monitors) which affect product reliability.
2. Reduce process qualification cycle time.
3. Improve process qualification success rate.
4. Assess reliability trends of production processes.
5. Quantify the reliability impact of process modifications.

WLR provides faster feedback for fab process control. The collection of WLR test data during and at the end of wafer fab processing provide a reliability baseline for each of our fab processes. Shifts in WLR test results, whether intentional (a process change or qualification) or unintentional (a process control problem), signal an increase or decrease in product reliability risk. WLR monitoring of production processes using Statistical Quality Control (SQC) techniques provides engineering with the information required to find and fix process control problems faster, and to determine the effectiveness of on-line process controls from a reliability standpoint. In this way, WLR testing is used to link on-line process controls to the traditional accelerated life testing methods.

NATIONAL'S WLR PROGRAM

National developed a corporate-wide WLR program which continues to implement powerful, new test techniques. WLR testing has been used effectively to help understand how process variability affects product reliability. It is also used to help build-in reliability at the design stage for new process technologies such as that used by ABTC, a 1.0 μm BiCMOS process.

WLR tests and test structures have been designed to increase the likelihood and predict a rate of a reliability failure mechanism occurrence. In addition, National has developed a partnership with a leading parametric test system supplier. Working together, a WLR test system was designed and developed to meet the unique requirements of Wafer-Level-Reliability testing. These systems are capable of testing to the voltage, current, and temperature extremes required for inducing the desired failure mechanisms in a short period of time. Some examples of the reliability failure mechanisms that are monitored using WLR techniques include:

Wafer Level Reliability (WLR) (Continued)

Interlayer Dielectric Integrity

Unique high voltage testing (to 1500V) is used to test for dielectric particles, metal hillocks or contamination, and poor dielectric stop coverage. Designed experiments have been successful in correlating the high voltage WLR test results to fab process monitors (such as deposition temperature and etch selectivity), and to accelerated life test results (Op-life, Temp Cycle, and Thermal Shock).

Metal Step Coverage

High current testing of large area metal serpentine structures is performed to detect restrictions in the conducting stripe. Designed experiments have been successful in correlating the high current WLR test results to fab process monitors such as metal thickness, critical dimensions, and via size.

Mobile Ions

A 200°C hot chuck is used with custom-built high temperature probe cards to accurately measure transistor threshold voltage shifts for a variety of oxide layers. Other methods for detecting mobile ion contamination include the use of self-heated polysilicon gate test structures and Triangular Voltage Sweep (TVS) test techniques.

Metal Stress Voids

High current resistance measurements are taken before and after wafers are processed through a series of heating and cooling cycles. This heat treatment is designed to mimic the high temperature processing incurred during device assembly (such as a seal-dip furnace), and it has been shown to accelerate metal void formation when the stress of the overlying film is high enough. Significant increases in the final resistance indicate the formation of metal stress voids.

Gate Oxide Integrity:

JEDEC J_{RAMP}, V_{RAMP} and Q_{BD} test techniques are used to monitor gate oxide quality. The WLR tester is also used to perform very sensitive leakage current measurements, using a specially designed picoammeter module, which allows us to detect subtle differences in gate oxide quality.

Passivation Integrity

A novel wafer-level-autoclave test technique has been developed which allows us to quantify the level of protection the passivation film provides when the wafer is subjected to a high temperature, high humidity environment.

Hot Electron Degradation

Two wafer level tests are performed to indicate device susceptibility to hot electron damage. First, the maximum substrate current is measured to indicate the level of impact ionization occurring at the drain edge. Second, gate current measurements are taken to gauge the magnitude of electron injection during device operation. Long-term DC stressing of transistors at peak substrate current conditions is also monitored.

Electromigration

A Standard Wafer Electromigration Accelerated Test (SWEAT) technique is used to measure the sensitivity of a metal line to electromigration failures. SWEAT is used as a relative test of the reliability of a line.

Contact Electromigration

Risk of failures due to contact spiking and solid phase epitaxial growth (SPEG) are monitored by forcing current through specially designed test structures, and monitoring increases in resistance and substrate leakage.

Electrostatic Discharge Sensitivity (ESD)

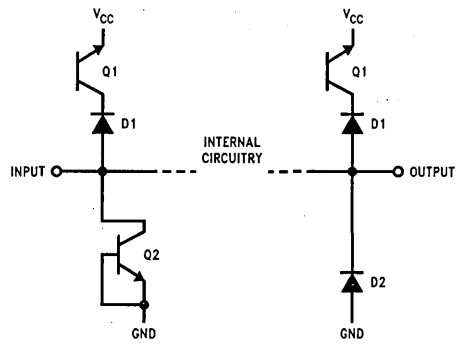
National ABTC logic has designed special dual-rail ESD protection circuitry to increase its level of ESD performance over non-protected inputs and outputs. This protection is standard on all ABTC designs and was first used in National's FAST® family.

By design, this circuitry limits product vulnerability to both positive and negative Human Body Model (HBM) ESD and Electrical Overstress (EOS) voltages by protecting inputs and outputs connected to V_{CC} as well as ground. Protection to ground is provided through the transistor Q2 and diode D2, standard Schottky clamp. The path to V_{CC} is protected through the BVCEO breakdown mechanism of Q1. Diode D1 ensures isolation of the input or output from V_{CC} leakages.

The device design and layout ensures dependable turn-on characteristics as well as robustness.

ESD protection was achieved with no appreciable affect on speed or increase in capacitance.

ESD Protection Circuit

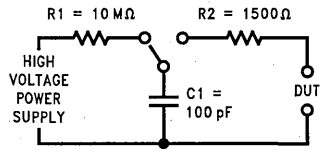


TL/F/11564–1

Electrostatic Discharge Sensitivity (ESD) (Continued)

ABTC logic ESD sensitivity is typically greater than 2000V, using the MIL-STD-883C, test method 3015 for Human Body Model (HBM) ESD.

HBM Test Circuit



TL/F/11564–2

Normal handling precautions should be observed as in the case of any semiconductor.

Power Sensitivities for Minimum Geometry Products

The demand for high performance process technology capable of sub 4 ns speeds, minimal noise and lower operating voltages drives the microelectronics industry towards decreasing layout geometries. Advanced process technology minimizes gate widths, gate oxide thickness and junction depths to improve gate switching speeds. In contrast, the decreased geometries reduce the ability of the devices built on advanced processes to resist electrical overstresses. As geometries decrease, emphasis shifts towards the reduction of environmentally induced electrical overstresses to ensure system and component reliability.

Market trends continue to drive the need for smaller geometries with reduced power supply voltages. Current 5.0V technologies are migrating towards 3.0V technologies while 3.0V technologies have shown a greater sensitivity to electrical overstresses. Sensitivities to electrical overstresses have been observed in as large as 1.0 μm geometries.

Device damage from electrical overstresses vary and the categories include, but are not limited to: Electrical-Over-Stress (EOS) due to excessive current or voltage exposure and Electro-Static-Discharge (ESD) be it exposure by Human Body Model, Charged Device Model or Machine Model. Sources of electrically induced overstresses are difficult to determine; however, investigation of failures from small geometry devices may show that environmental hazards such as unregulated and unconditioned power supplies in the field exceed "Absolute Maximum Ratings" causing unrecoverable device damage.

Advanced processes such as BiCMOS include small dimension current density limited geometries that are sensitive to electrically induced overstresses. The combination of internal bipolar and CMOS gates provides current capabilities for maximum device performance. In an unconditioned supply environment, the bipolar section of a BiCMOS circuit can source excessive current through the CMOS section and cause damage due to the CMOS circuit's current density limited geometries.

In an effort to resolve device sensitivities to electrical overstresses, designers and engineers can reference device databooks. Databook specifications include "Absolute Maximum Ratings" and adherence to this specification is essential in ensuring component and system level reliability.

1. A. Amerasekera, A. Chatterjee, *"An Investigation of BiCMOS ESD Protection Circuit Elements and Applications in Submicron Technologies"*, EOS/ESD Symposium, p5B.6.1.

Advanced BiCMOS and Latchup Testing

Latchup in CMOS and bipolar circuits can vary in severity from being a temporary condition of excessive ICC current and functional failure, to total destruction requiring a new unit. The latchup condition is usually caused by applying a stimulus that is able to cause a regenerative condition in a PNP-NPN structure. For a more detailed description of definitions and causes of latchup, see National Semiconductor Application Note 600 (located in the "FACT Advanced CMOS Logic Databook" Lit. # 400019).

National has characterized its ABTC logic for robustness using the JEDEC 17 method and an IMCS 4600 Automated Latchup Test System. The automated test equipment approach to latchup provides a repeatable test setup and application of test conditions, reduces the amount of time for evaluation, and provides a more comprehensive set of vectors and stimuli over a shorter period of time.

The JEDEC 17 method is a standard measurement procedure for the characterization of CMOS integrated circuit latchup susceptability/immunity, measured under static conditions. The method allows for overcurrent/overvoltage stressing of inputs and outputs to detect latchup.

In short the JEDEC 17 method follows a sequence of:

1. Apply power
2. Setup I/O conditions to place device in desired state
3. Apply trigger source for desired duration
4. Measure supply current
5. Remove power supply if ICC ≥ test limit
6. Inspect for electrical damage

The time for each parameter as well as the temperature is critical for correlation of latchup. National characterizes latchup on the ABTC family at 125°C and with the critical timing parameters on Table I. Close correlation can only be accomplished by using the same trigger duration, V_{CC}, test temperature, and magnitude of trigger stimulus.

TABLE I. Critical Timing Parameters

Symbol	Parameter	Time
T_W	Trigger Duration	500 μs
t_{COOL}	Cool Down Time	10 ms

Advanced BiCMOS and Latchup Testing (Continued)

For ABTC products, logic states are checked for a susceptability to latchup with all outputs high, all outputs low and all outputs in TRI-STATE®. If the device is a bi-directional device, then the logic states are tested in each direction. All inputs and outputs are tested for each logic state and direction.

Because the ABTC family is designed for live insertion, a Positive Voltage Trigger (PVT) and a Negative Current Trigger (NIT) is applied to the inputs and outputs to check for latchup.

Forcing a current in the positive direction overstresses the inputs and outputs by causing a breakdown. Such breakdowns consume enough power in the breakdown area to cause the junction permanent damage. PVT stresses the inputs and outputs while keeping the input and output devices out of any breakdown region.

Finally all inputs and outputs have clamp diodes, requiring a negative current trigger as a stimulus for latchup. The clamp diodes are designed to allow current flow into ground without injecting carriers into the substrate that could cause a parasitic PNP-NPN. Supply and stimulus values used by National for latchup testing the ABTC family are in Table II.

TABLE II. Supply and Stimulus Values

Stimulus	Parameter	V_{CC}	Stimulus
PVT	Positive Voltage Trigger	7.0V	V_{CC} + 3V (10V)
NIT	Negative Current Trigger	7.0V	−500 mA

Verification of any unusual observations is performed with a curve tracer manually. For example, when ABTC outputs are brought below ground, the NMOS transistor feeding current to the bipolar output will turn on and current from V_{CC} will come out of the output pull-down device. This condition is unavoidable by design and is not latchup. Thus good analysis of observations will tell one whether latchup has occurred.

Due to the high trigger stresses, devices used for latchup testing should be discarded and not used for design, production, or other tests. Latchup testing is potentially destructive and may limit the life of a device.

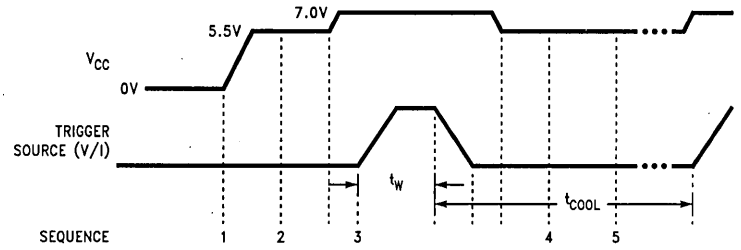


FIGURE 1

Section 4

ABTC Applications and Design Considerations

Section 4 Contents

ABTC Design Considerations for Fault Tolerant Backplanes

National Semiconductor
Application Note 881
R. Craig Klem
Application Engineer

INTRODUCTION

National Semiconductor's high speed Advanced BiCMOS Technology, ABTC is a 1.0 μm process product introduced to provide a high speed fault tolerant solution for interface needs. Some of the targeted interface environments include computer servers, mainframes and central office switches.

Each of these interface environments suffer from glitching or level degradation on their backplane or bus, generated from either live insertion of a board or a power up and down cycle used when performing maintenance on a system. Board designers need to address live insertion and power cycling requirements when designing a fault tolerant system. Definitions and applications of live insertion and power cycling change based on the product that interfaces with a backplane environment.

Discussion of a fault tolerant benefits from a review of definitions and solutions for fault tolerant interfacing and a review of device specs and how they contribute to a fault tolerant environment.

DEFINITION OF TERMS

— Live Insertion

Boards like those seen in a telephone company's central office switch are often removed and inserted while the backplane remains active. Insertion and removal generates glitches and voltage level changes on the backplane. The level of isolation that a board mounted interface device provides the backplane can be broken down into three major groups.

— **1st Level of Isolation** is defined as the ability of the interface devices to allow insertion of the board to which it is mounted without having to power the system down. Requirements include a method of suspending the bus activity to prevent glitch or level corruption of bus data.

— **2nd Level of Isolation** is defined as the ability of the interface devices to allow insertion of the board without the need to power the system down or suspend bus activity. Requirements include a method by which the bus can check for, and correct, faults introduced on the backplane during board insertion or a method for providing proper biasing of the board interface devices with a staggered pin arrangement on the board-backplane connector. Precondition biasing circuitry for the interface device may also provide the required isolation.

— **3rd Level of Isolation** is defined as the ability of the interface devices to allow board insertion without any limitations, restrictions or requirements of other circuits on the preservation of bus data.

The level of isolation that an interface device mounted on a board provides for the backplane has a direct impact on system uptime. Increasing levels of isolation allow for increased serviceability without system interruption. Board isolation provided by an interface device gives more freedom to the designer for focusing on purpose built board functions, reducing board design complexity and ultimately, board cost. ABTC products reward the board designer and the board user these benefits with a 2nd Level isolation solution.

— Fault Tolerance

Fault tolerance in a backplane environment is the ability of the bus to detect and/or correct errant signals from any source including glitches, level changes, etc., generated from the insertion or extraction of a board into a backplane. A system populated with ABTC products minimizes the need for errant signal processing associated with the live insertion and extraction process when biased correctly.

— Power Up/Down TRI-STATE®

When the devices that interface with the backplane power up or down, their connection to the bus will ideally maintain a high impedance state. With respect to the ABTC product family, the output enable circuitry has control of the output state of the interface device during power up and down so as to prevent intermittent low impedance loading or glitch generation commonly associated with conventional CMOS and Bipolar devices.

— Partial System Power Down

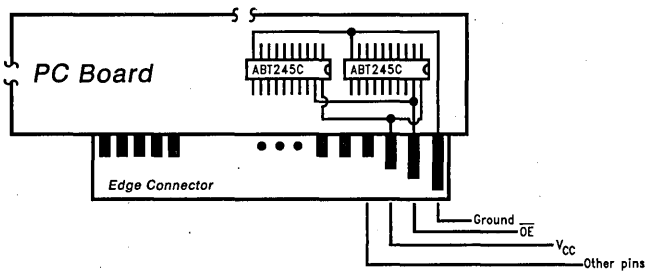
Partial system power down implies that a system comprised of a combination of hardware and firmware provides power switching control of a backplane slot to allow for insertion, or removal of a board. Partial system power down facilitates system serviceability. Board-mounted ABTC interface products enhance serviceability for permitting backplane slot power cycling while maintaining high impedance, glitch free isolation with the board and its backplane.

SOLUTIONS FOR FAULT TOLERANT INTERFACING

The achievement of a fault tolerant system solution with live insertion capabilities begins with a review of some of the bus protection solutions available. Options available to the ABTC product family include:

— Staggered Pin Arrangement

For a PC edge connector arrangement, the solution in *Figure 1* can be adopted to provide proper biasing of the output enable pin ($\overline{OE}$) to ensure high impedance on the backplane. It will satisfy both insert and removal requirements. While this configuration provides an ideal connector, constraints often limit the number of different pin lengths to two. By offsetting the $\overline{OE}$ pin, we want to ensure that it will either reach a high level of ≥2.0V, before V_{CC} is applied, or that $\overline{OE}$ will maintain a ≥50% V_{CC} level during the V_{CC} ramp.



TL/F/11554–1

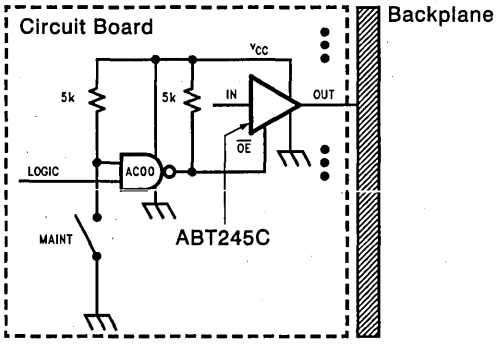
FIGURE 1

— Isolation Circuitry

Isolation circuitry provides another option for board and backplane isolation. Again, this solution will provide the necessary $\overline{OE}$ pin biasing to assure a level of 2.0V or to assure $\overline{OE}$ maintains ≥50% of V_{CC} as V_{CC} powers up or down for guaranteed high impedance interface to the backplane.

The design of Circuit-1 below provides >50% of V_{CC} for the $\overline{OE}$ pin throughout the V_{CC} ramp then switches to a voltage level of a logic high once the AC00 reaches its turn-on V_{CC}. After board insertion, the MAINT switch is opened and the LOGIC pin becomes the $\overline{OE}$ control. Live insertion or removal for this solution requires a technician to manually operate the maintenance switch (MAINT) to ensure proper biasing of $\overline{OE}$ and board-backplane isolation.

Circuit-1



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SPECIFICATIONS AND THEIR CONTRIBUTION TO FAULT TOLERANT SYSTEMS

DC specifications and their characteristic input/output curves help map out the loading effects of an interface device on bus or backplane. The loading characteristics of typical ABTC input and output pins are shown in *Figures 2–4.* National Semiconductor's ABT245C characteristic curves are used for this demonstration.

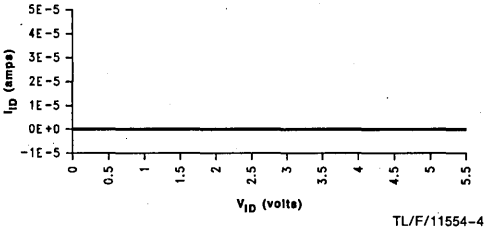
— Powered Down Backplane Isolation

The power down leakage characteristics of a bus interface device assist the interface board designer in understanding the effects of loading on his backplane. During live insertion, the board is not powered up and the instantaneous loading upon contact would look like the curves of VID and IZZ in *Figures 2* and *3.* Typically, loading leakages in the +200 μA range begin to affect the V_{OH}/V_{OL} levels in a backplane application. The VID and IZZ curves illustrate the loading effects on the backplane over a range of backplane voltages from 0.0V to 5.5V.

— VID

VID is a voltage that is measured on an input pin at a current loading of 1.9 μA in a power off condition such as when V_{CC} and the non-measurement pins are at 0.0V.

The curve of VID vs IID in *Figure 2* shows the current leakage of a typical ABTC input pin. The ABTC inputs limit loading leakage to <1.9 μA over an input voltage range from 0V to 5.5V.



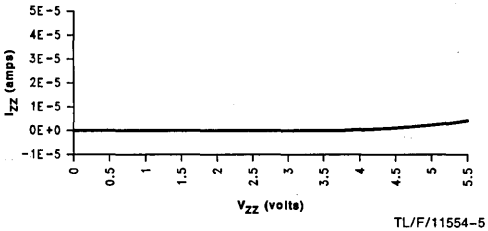
TL/F/11554–4

FIGURE 2

— IZZ

IZZ is a current that is measured on an output pin at a voltage of 5.5V during a power off condition such as when V_{CC} and the non-measurement pins are at 0.0V.

The curve of VZZ vs IZZ in *Figure 3* shows the current leakage of a typical ABTC input/output (I/O) pin and how it loads a bus or backplane over a range of bus voltages from 0.0V to 5.5V. I/O pin configurations exhibit combined current characteristics from components of the input circuitry and output circuitry. ABTC I/O pins specify loading leakage at 100 μA max. with a typical loading leakage at 3 μA at room temperature.



TL/F/11554–5

FIGURE 3

— Powered Up Backplane Isolation

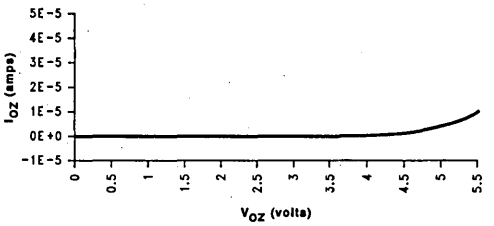
During power up operation, the output enable pin, $\overline{OE}$, controls backplane isolation. The IOZH/IOZL parameters provide the interface board designer with the leakage characteristics of the interface device during a tri-stated condition.

— IOZL/IOZH

IOZL is a parameter that quantifies the output leakage current while the part is powered up and the output is conditioned low before it was tri-stated (disabled). IOZH is the same as IOZL except that the output was conditioned high before being tri-stated.

The IOZL/H curve in *Figure 4* shows an I/O pin leakage characteristic during TRI-STATE operation over a range of bus voltages from 0.0V to 5.5V. ABTC devices specify IOZH/L at a maximum of 50 μA while typical leakage is in the vicinity of 12 μA at room temperature.

— IOZL/IOZH



TL/F/11554-6

FIGURE 4

— Powering Cycling and Backplane Isolation

During the transition of a power up or power down cycle, an interface device output might act erratically by glitching or seeking a voltage level that is disruptive to the backplane. These transition characteristics degrade fault tolerant systems and would increase system down time.

The curves in *Figures 5* and *6* demonstrate the capability of the ABT245C to maintain isolation from an active bus and provide a glitch free output while being powered up and down. With the $\overline{OE}$ pin conditioned high, V_{CC} was cycled between 0.0V and 5.5V to monitor the output voltage levels as they would appear on a bus. Bus loads of 1 kΩ pull-up and pull-down were used. The bus voltage level disruption is in the micro-volts range attesting to the minimal impact ABTC interface products would have on the backplane.

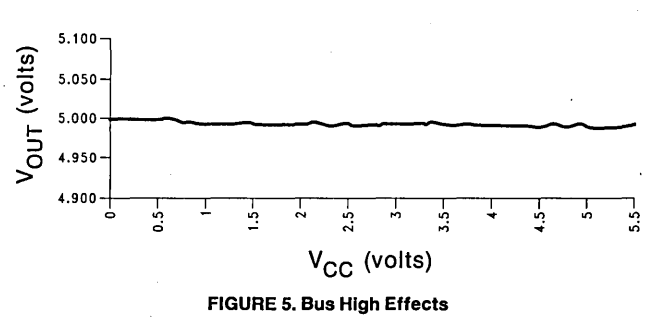


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FIGURE 5. Bus High Effects

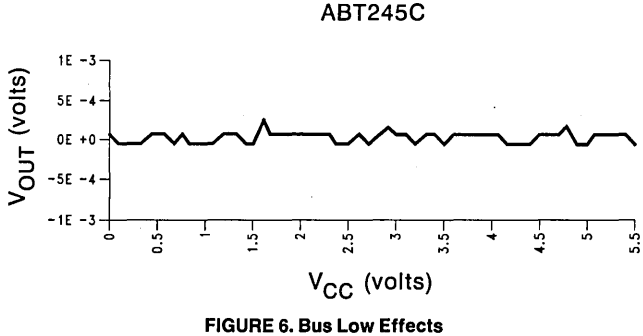

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FIGURE 6. Bus Low Effects

SUMMARY

ABTC interface devices offer glitch free power cycling provided that the $\overline{OE}$ pin is held at the device specified V_{IH} (2.0V) level. In practice, $\overline{OE}$ will provide an output high impedance condition if $\overline{OE}$ maintains a level of $\geq$50% of V_{CC} through the 0V to 5.5V range. In fact, the $\overline{OE}$ pin circuitry gains control once V_{CC} is $\geq$1.0V. Interface device output characteristics for V_{CC} levels before 1.0V are controlled through the isolation circuitry discussed earlier.

ABTC designs and specifications recognize the need for more fault tolerant interface devices. Live insertion guarantees such as VID/IZZ, IOZL/H and glitch free power cycling all promote better system uptime, especially for telecom switching environments. Together with extended AC specifications that reduce the need for complex performance evaluations, ABTC live insertion guarantees allow designers to spend more time on total system performance features and not worry about the logic.

National Semiconductor

ABTC Applications

Avoiding Bus Contention

ABTC devices typically disable (to high impedance) faster than they enable (to active state) and therefore offer an inherent way to minimize bus contention. System designers must be aware of the effects of bus interface device exposure to contention. Some advice is offered in the following discussion.

Ideally the system designer should insure that the disabling signal to the active driver always precedes the enabling signal to the next driver to insure minimum contention; i.e., t_{SETUP} time disable-to-enable should be a positive number. If the interface devices on the bus (as NSC ABTC devices typically do by design) exhibit disable times (t_{PHZ}/t_{PLZ}) quicker than enable times (t_{PZH}/t_{PZL}), then the t_{SETUP} time disable-to-enable can be reduced to zero or slightly negative and not cause significant contention.

The typical t_{SETUP} time is approximated from the typical enable/disable time specs: t_{SETUP} disable-to-enable = $t_{PLZ} - t_{PZH}$ or = $t_{PHZ} - t_{PZL}$; whichever yields the most positive number governs. Obviously if disable time is larger than enable time then t_{SETUP} is a positive time. Worst case t_{SETUP} is calculated from the min/max enable times: t_{PLZ} (max) − t_{PZH} (min) or t_{PHZ} (max) − t_{PZL} (min) and will always yield a safer positive number.

Data taken on a '245 function in a bus contention test fixture may be helpful to illustrate the effects of varying the t_{SETUP} from a value which caused no contention to values which caused significant contention in *Figures 1–3*.

No reliability data to calculate fit rates to support a degree of contention resilience is offered at this time. Deliberate contention is not recommended. For instance a designer should be rightly concerned about the magnitude of current that can flow when a 64 mA (min) bus interface sink (I_{OL}) stage contends with a −225 mA (max) source (I_{OS}) stage for a large overlap time period with multiple outputs switching. Particularly true for the newer bus interface parts like ABTC which have I_{OS} specifications more negative than the −225 mA max.

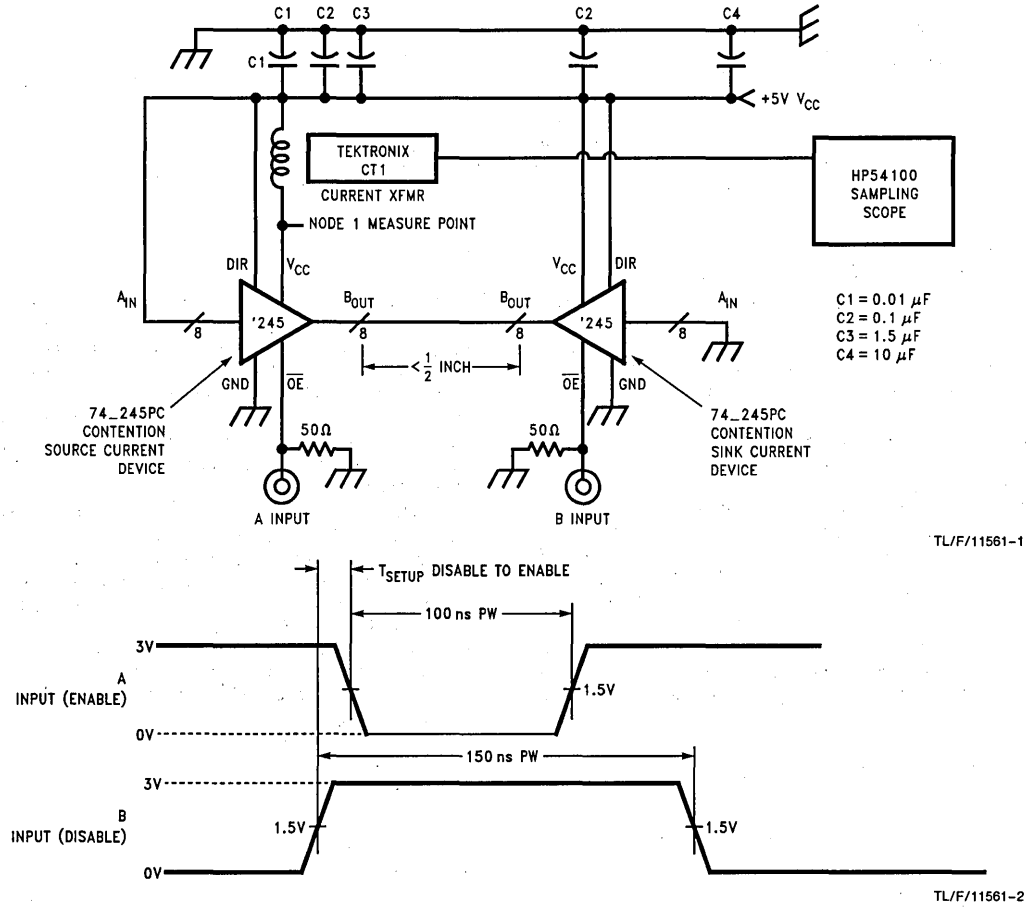
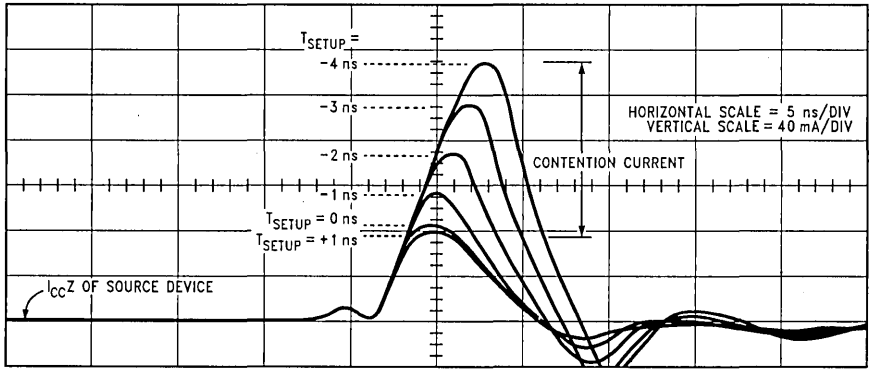


FIGURE 1. '245 Function Bus Contention Test Fixture

Procedure: Adjust t_{SETUP} by varying the delay of B pulse. Monitor contention current of OR-tied B outputs at node 1.



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At T_{SETUP} = +1 ns, there is no contention current, merely normal capacitive charging during LH transition. Bus contention is measured with 8 outputs switching in phase on both devices. This example used the 74F245PC, with the monitor on pin 18, B_{OUT}.

FIGURE 2. Bus Contention Current

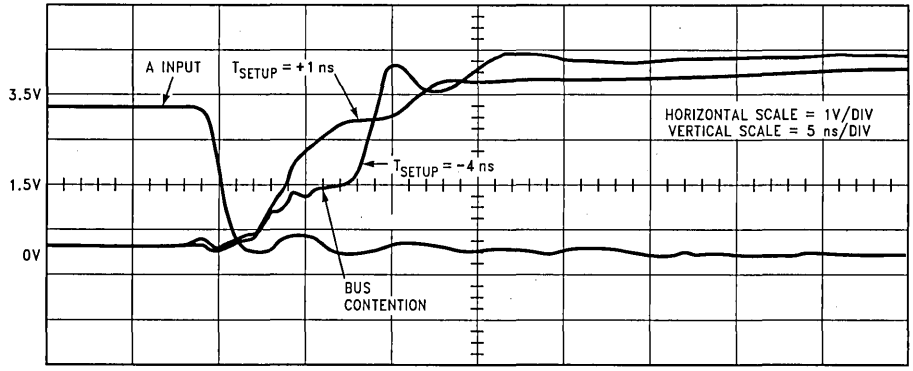

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FIGURE 3. Output Response in Bus Contention Test Fixture

Power Down Characteristics

Power-down characteristics provide the system designer's with an understanding of the loading effects from a device when the device power supply is at 0.0V. The device's powered-down characteristics effect the system bus or backplane in a number of ways and can be characterized by its input and output capacitance and current loading. The measured parameters that provide the designers with loading information include; C_{IN}/C_{OUT}, input/output capacitance; IZZ, tri-stateable output power-down current loading; VID, input power-down current loading.

A device's input and output capacitance define the effective bus and backplane loading through the charging and discharging of the interface pins. ABTC devices have typical capacitance values of 5 pF for input pins and 9 pF for output pins, while I/O pins have a typical value of 11 pF. National tests capacitance in accordance with the procedures outlined in the MIL-STD-883, method 3012.

The power-down leakage characteristics of an ABTC device provide the effects of current loading on a bus or backplane. Typically, loading leakages in the $+200$ μA range begin to effect the V_{OH}/V_{OL} levels in a backplane application. The VID and IZZ curves in *Figures 4* and *5* illustrate the loading effects on the backplane over a range of backplane voltages from 0.0V to 5.5V while the power supply is kept at 0.0V.

— VID

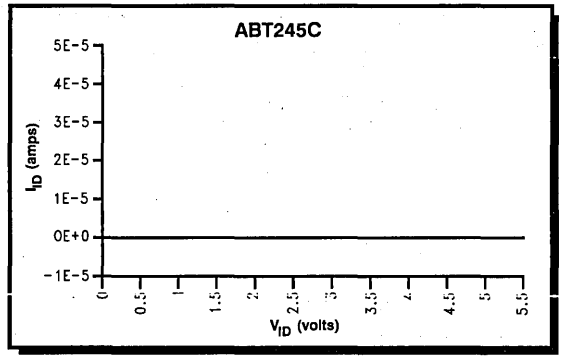
VID is a voltage that is measured on an input pin at a current loading of 1.9 μA in a power off condition such as when V_{CC} and the non-measurement pins are at 0.0V.

The curve of VID vs IID in *Figure 4* shows the current leakage of a typical ABTC input pin. ABTC inputs typically limit loading leakage to <1.9 μA over an input voltage range from 0V to 5.5V at room temperature.

— IZZ

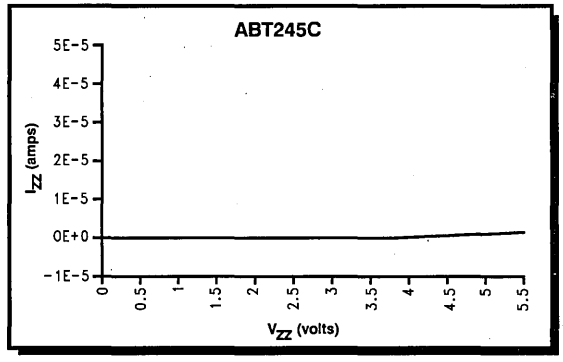
IZZ is a current that is measured on an output pin at a voltage of 5.5V during a power off condition such as when V_{CC} and the non-measurement pins are at 0.0V.

The curve of VZZ vs IZZ in *Figure 5* shows the current leakage of a typical ABTC input/output (I/O) pin and how it loads a bus or backplane over a range of bus voltages from 0.0V to 5.5V. I/O pin configurations exhibit combined current characteristics from components of the input circuitry and output circuitry. ABTC I/O pins specify maximum loading leakage at 100 μA with a typical loading leakage at 3 μA at room temperature.



TL/F/11561–5

FIGURE 4



TL/F/11561–6

FIGURE 5

Models

National Semiconductor in conjunction with Quad Design, offers SPICE and TLC models for the system designer. Each model provides information on parameters that speed design-in activities. The description, use and availability of the two types of models is outlined below.

SPICE

Description: The SPICE input files are valid representations of the input, output, I/O and associated circuitry used on the logic device modeled. The circuit and device models were designed and verified using SPICE 2G6. National Semiconductor makes no guarantee that identical results will be produced by other hardware/software combinations. Proper execution of these models is not guaranteed if any changes are made to its files.

File Name Conventions:

FFFDDDDS.TTT
- FFF — family code (ABT)
- DDDD — device designation (245)
- S — step revision of model file
- TTT — valid temperature of file with a preceding m representing minus

Exceptions may be seen in file names such as 16 bit devices.

Use: While SPICE simulation input files may be a useful and beneficial tool to the system designer for the purpose of modeling bus loading and DC drive characteristics, and due to the complexities indigenous to the modeling of transient phenomenon, National Semiconductor recommends that simulated results be supported by laboratory characterization prior to making final judgments regarding device transient performance.

The input files incorporate single bit models over cold, room and hot die temperatures as well as package models.

Availability: If an ABTC product is orderable, the SPICE models is available through the Applications Engineering Group at National Semiconductor.

333 Western Avenue
South Portland, Maine 04106
Telephone: (800) 341-0392

TLC

Description: Transmission Line Calculator, (TLC) Models provide the system designer with transmission line characteristics such as signal quality. TLC predicts ringing, undershoot and overshoot, performs automated analysis of entire PCB designs and offers accurate delay data for ABTC products. National provides AC, DC and capacitance characteristics for the model which Quad Design compiles and makes available for customers. The characteristics are generated either empirically or from SPICE simulations. The AC characteristics include output edge rate and the DC characteristics include output drive capacity and input/output leakage data.

Use: The TLC models are most often used for signal analysis in PCB designs. TLC program features include predictability of ringing, non-incident switching, undershoot, overshoot, and time delay for networks of arbitrary topology and construction. The program may also be used to evaluate network loading and termination strategies. Additionally, TLC provides users with critical clock and backplane signal analysis tools as well as tools for viewing the effects of tristate bus contention.

Availability: TLC models on orderable product may be obtained by contacting:

Quad Design
1385 Del Norte Road
Camarillo, California 93010
Telephone: (805) 988-8250
FAX: (805) 988-8259

Section 5

ABTC Datasheets

Section 5 Contents

National Semiconductor

54ABT/74ABT244C
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ABT244C is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

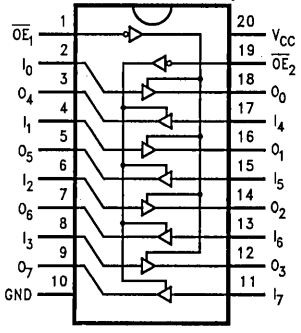
Features

- Non-inverting buffers
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code: See Section 11

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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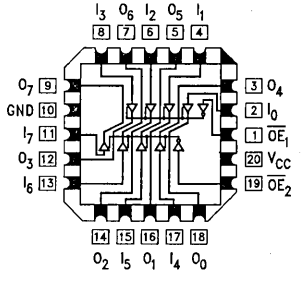
Pin Assignment for LCC



TL/F/10992–2

Truth Table

$\overline{OE}_1$	I_{0-3}	O_{0-3}	$\overline{OE}_2$	I_{4-7}	O_{4-7}
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active Low)
I_0–I_7	Inputs
O_0–O_7	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT244C Min	ABT244C Typ	ABT244C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}_n$ = V_{CC}; All Others at V_{CC} or Ground
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or Ground
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.1	mA/MHz	Max	Outputs Open $\overline{OE}_n$ = GND, (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.
Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.5	0.8	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.3	−0.8		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.7	3.1		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.5		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.1	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP package): See Section 2

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	1.0	2.5	3.6			1.0	3.6	ns	2-3, 5
t_{PHL}	Data to Outputs	1.0	2.3	3.6			1.0	3.6		
t_{PZH}	Output Enable	1.5	3.5	6.0			1.5	6.0	ns	2-4
t_{PZL}	Time	1.5	3.6	6.0			1.5	6.0		
t_{PHZ}	Output Disable	1.0	3.5	5.6			1.0	5.6	ns	2-4
t_{PLZ}	Time	1.0	3.3	5.6			1.0	5.6		

Extended AC Electrical Characteristics (SOIC package): See Section 2

Symbol	Parameter	74ABT −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF, 8 Outputs Switching (Note 4)			74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 1 Output Switching (Note 5)		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.5	ns	2-3, 5
t_{PHL}	Data to Outputs	1.5		5.0	1.5	6.0	2.5	8.5		
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.5	2.5	10.0	ns	2-4
t_{PZL}		1.5		6.5	2.5	7.5	2.5	12.0		
t_{PHZ}	Output Disable Time	1.0		5.6	(Note 7)		(Note 7)		ns	2-4
t_{PLZ}		1.0		5.6						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew (SOIC package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	0.8	1.8	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	0.8	1.8	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	1.0	2.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	1.0	2.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	1.5	3.0	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

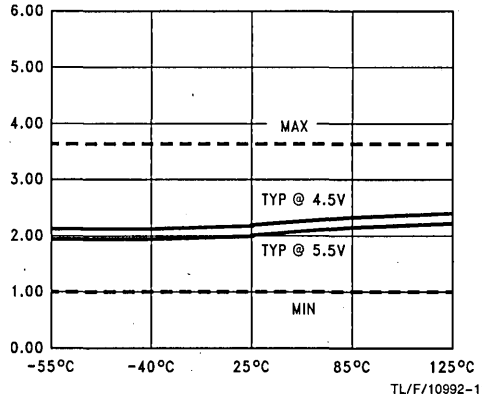
Note 5: This describes the difference between the delay of the Low-to-High and the High-to-Low transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

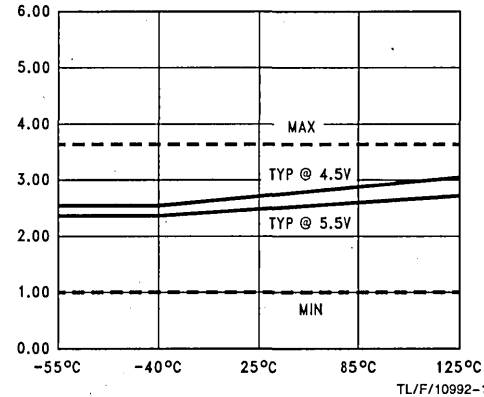
Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



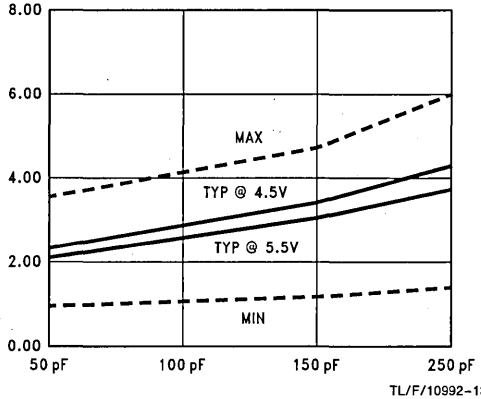
TL/F/10992–11

t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



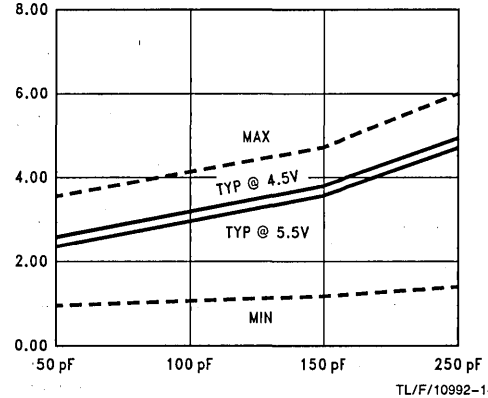
TL/F/10992–12

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



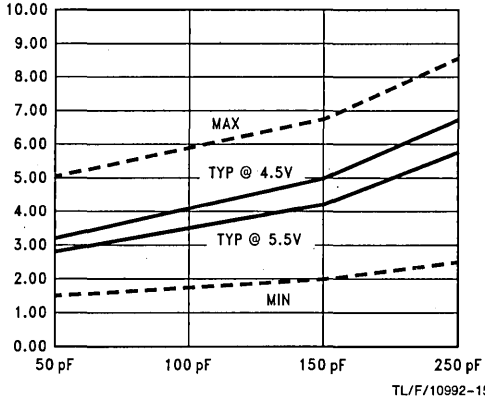
TL/F/10992–13

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



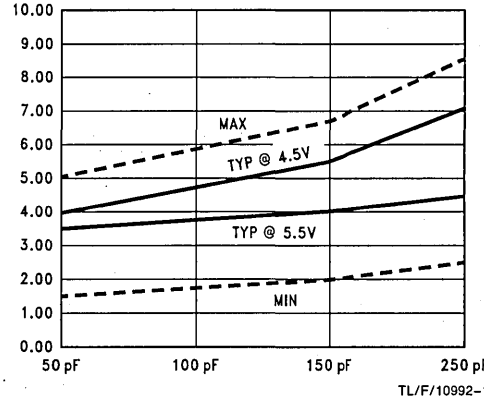
TL/F/10992–14

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



TL/F/10992–15

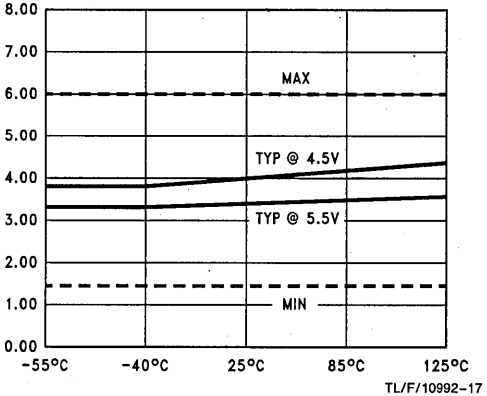
t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



TL/F/10992–16

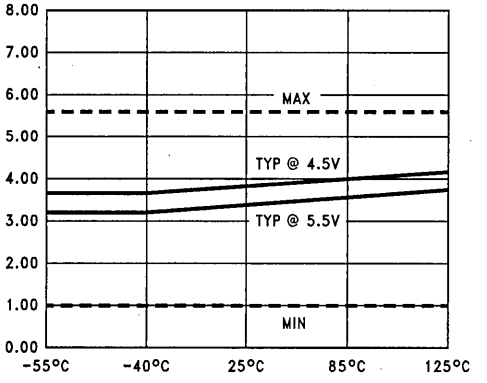
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



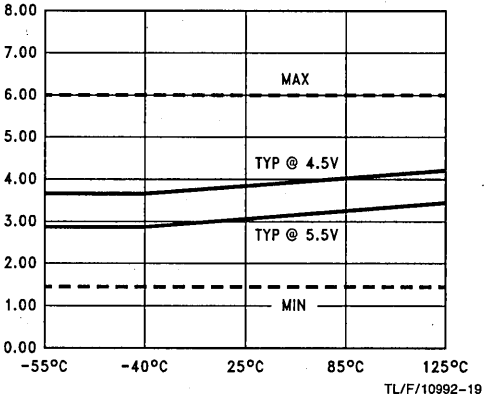
TL/F/10992–17

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



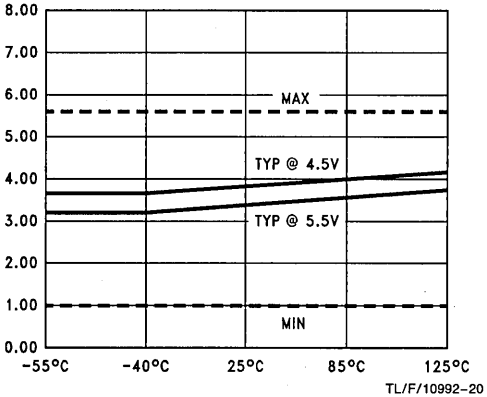
TL/F/10992–18

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



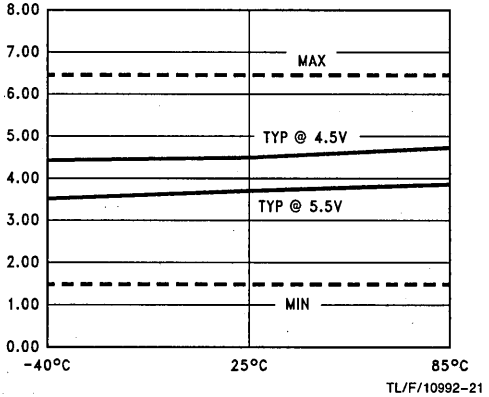
TL/F/10992–19

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



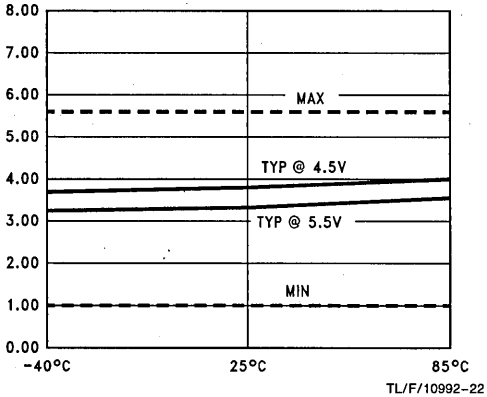
TL/F/10992–20

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



TL/F/10992–21

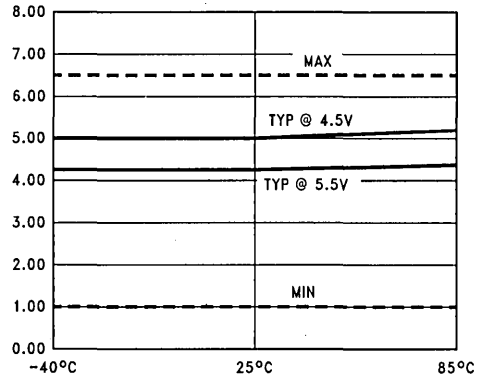
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



TL/F/10992–22

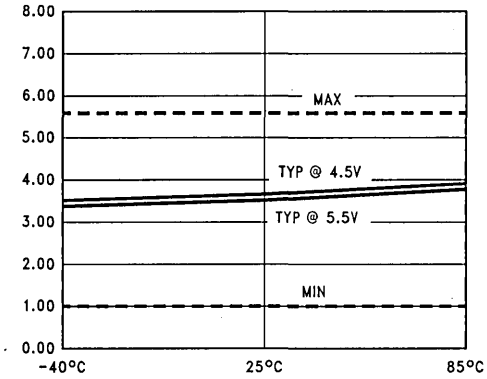
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



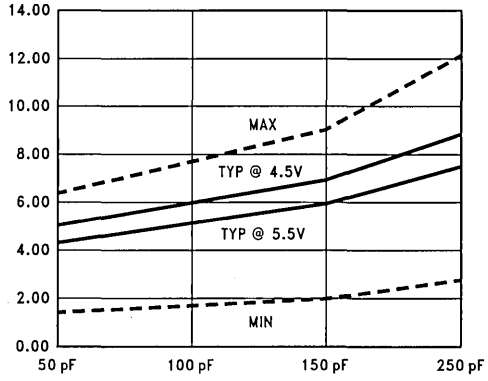
TL/F/10992-23

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



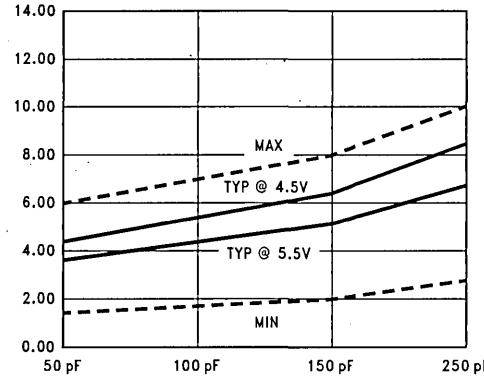
TL/F/10992-24

t_{PZL} vs Load Capacitance
8 Outputs Switching
T_A = 25°C



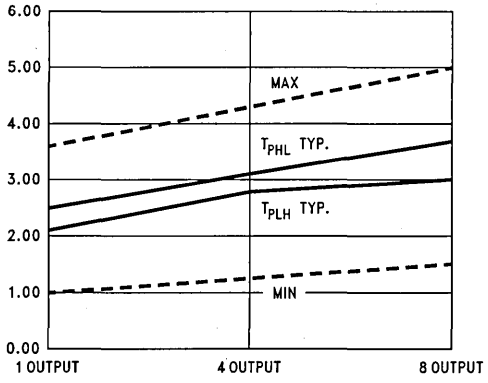
TL/F/10992-25

t_{PZH} vs Load Capacitance
8 Outputs Switching
T_A = 25°C



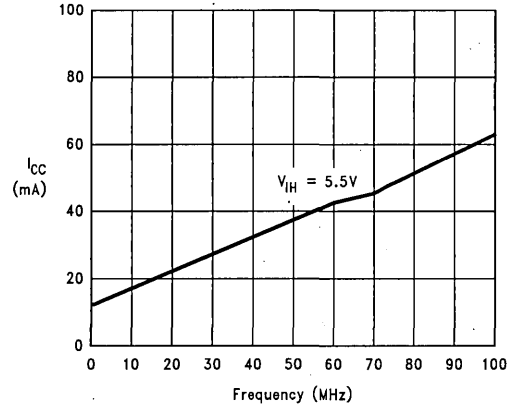
TL/F/10992-26

t_{PLH} and t_{PHL} vs Number
Outputs Switching V_{CC} = 5.0V,
T_A = 25°C, C_L = 50 pF



TL/F/10992-27

I_{CC} vs Frequency,
Average, T_A = 25°C,
All Outputs Unloaded/Unterminated



TL/F/10992-28

Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

National Semiconductor

54ABT/74ABT245C
Octal Bidirectional Transceiver with TRI-STATE® Outputs

General Description

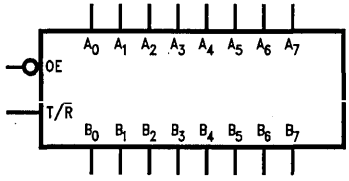
The 'ABT245C contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA on both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

Features

- Bidirectional non-inverting buffers
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time is less than enable time to avoid bus contention

Ordering Code: See Section 11

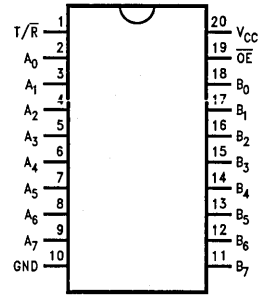
Logic Symbol



TL/F/10945–1

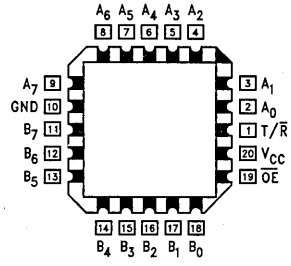
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10945–5

Pin Assignment for LCC



TL/F/10945–3

Pin Descriptions

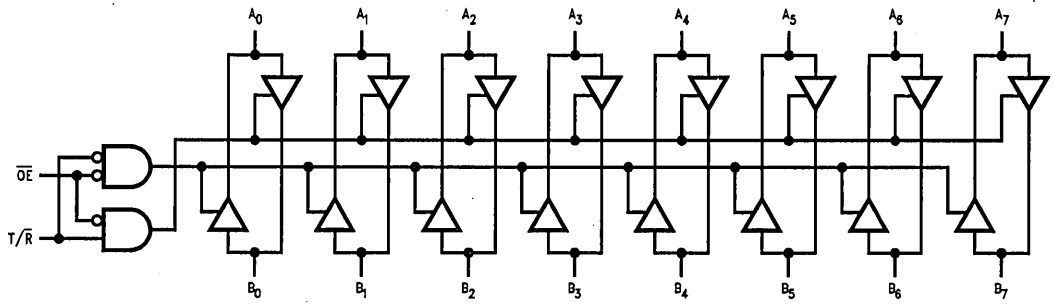
Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Truth Table

Inputs		Output
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/10945–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT245C Min	ABT245C Typ	ABT245C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA ($\overline{OE}$, T/$\overline{R}$)
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA (A_n, B_n)
		54ABT	2.0			V	Min	I_{OH} = −12 mA (A_n, B_n)
		74ABT	2.0			V	Min	I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA (A_n, B_n)
		74ABT			0.55			I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input HIGH Current				5 5	μA	Max	V_{IN} = 2.7V ($\overline{OE}$, T/$\overline{R}$) V_{IN} = V_{CC} ($\overline{OE}$, T/$\overline{R}$)
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V ($\overline{OE}$, T/$\overline{R}$)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−5 −5	μA	Max	V_{IN} = 0.5V ($\overline{OE}$, T/$\overline{R}$) V_{IN} = 0.0V ($\overline{OE}$, T/$\overline{R}$)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA ($\overline{OE}$, T/$\overline{R}$) All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V (A_n, B_n)
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC}, T/$\overline{R}$ = GND or V_{CC}; All Other GND or V_{CC}

DC Electrical Characteristics (Continued)

Symbol	Parameter		ABT245C Min	ABT245C Typ	ABT245C Max	Units	V_{CC}	Conditions
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	$V_I = V_{CC} - 2.1V$
		Outputs TRI-STATE			2.5	mA		$\overline{OE}$, $T/\overline{R}$ $V_I = V_{CC} - 2.1V$
		Outputs TRI-STATE			50	μA		Data Input $V_I = V_{CC} - 2.1V$
								All Others at V_{CC} or GND.
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.1	mA/ MHz	Max	Outputs Open $\overline{OE}$ = GND, $T/\overline{R}$ = GND or V_{CC} One Bit Toggling, 50% Duty Cycle (Note 1)

Note 1: For 8 bits toggling, $I_{CCD} < 0.8$ mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.0	V	5.0	$T_A = 25°C$ (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.3	−1.0		V	5.0	$T_A = 25°C$ (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.7	3.1		V	5.0	$T_A = 25°C$ (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	$T_A = 25°C$ (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.9	0.6	V	5.0	$T_A = 25°C$ (Note 2)

Note 1: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP package) : See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50$ pF Min	Typ	Max	54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF Min	Max	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PLH}	Propagation Delay	1.0	2.1	3.6			1.0	3.6	ns	2-3, 5
t_{PHL}	Data to Outputs	1.0	2.4	3.6			1.0	3.6		2-3, 5
t_{PZH}	Output Enable	1.5	3.2	6.0			1.5	6.0	ns	2-4
t_{PZL}	Time	1.5	3.7	6.0			1.5	6.0		
t_{PHZ}	Output Disable	1.0	3.6	5.6			1.0	5.6	ns	2-4
t_{PLZ}	Time	1.0	3.3	5.6			1.0	5.6		

Extended AC Electrical Characteristics (SOIC package) : See Section 2 for Waveforms

Symbol	Parameter	74ABT $-40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4) Min	Typ	Max	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5) Min	Max	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6) Min	Max	Units	Fig. No.
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.5	ns	2-3, 5
t_{PHL}	Data to Outputs	1.5		5.0	1.5	6.0	2.5	8.5		

Extended AC Electrical Characteristics (SOIC package) : See Section 2 for Waveforms (Continued)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)			74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.5	2.5	9.5	ns	2-4
t_{PZL}		1.5		6.5	2.5	7.5	2.5	11.0		
t_{PHZ}	Output Disable Time	1.0		6.5	(Note 7)		(Note 7)		ns	2-4
t_{PLZ}		1.0		5.6						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew (SOIC package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.3	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.8	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	3.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	3.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	3.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

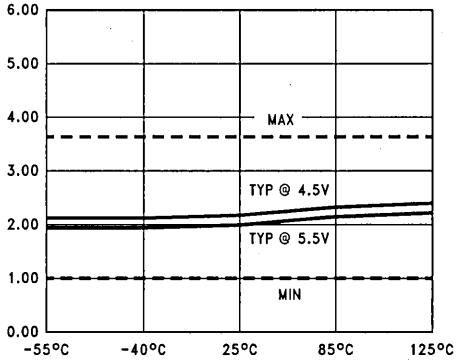
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$ ($\overline{OE}$, T/$\overline{R}$)
$C_{I/O}$ (Note 1)	I/O Capacitance	11.0	pF	$V_{CC} = 5.0V$ (A_n, B_n)

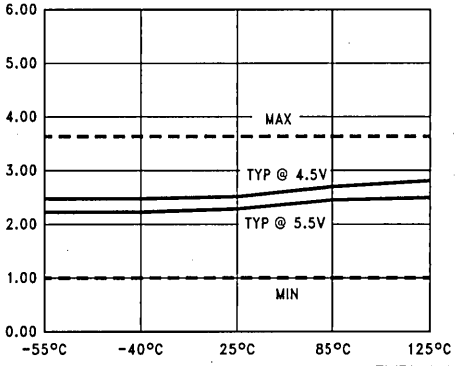
Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



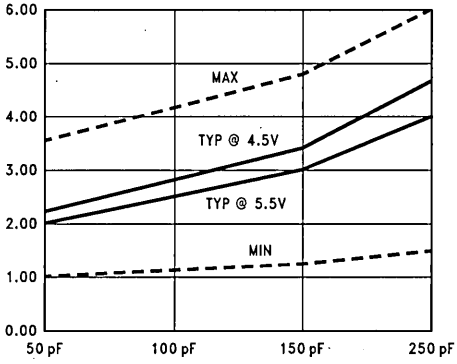
TL/F/10945–14

t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



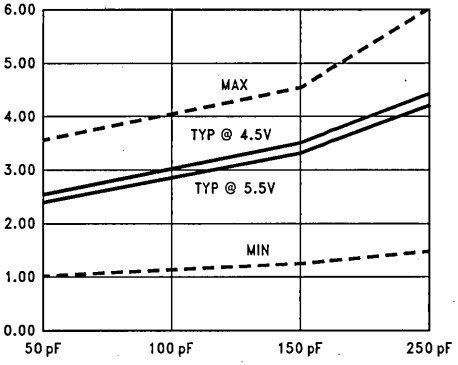
TL/F/10945–15

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



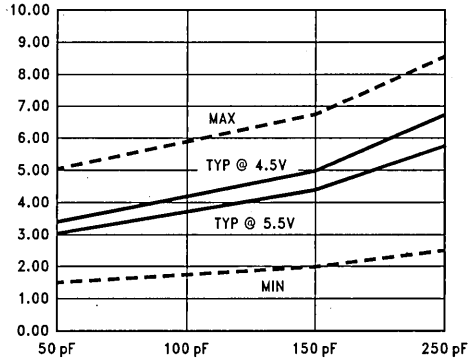
TL/F/10945–16

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



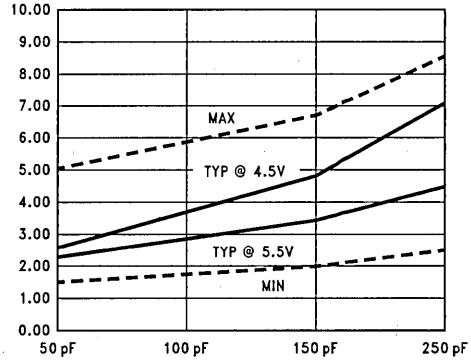
TL/F/10945–17

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = −40°C to +85°C



TL/F/10945–18

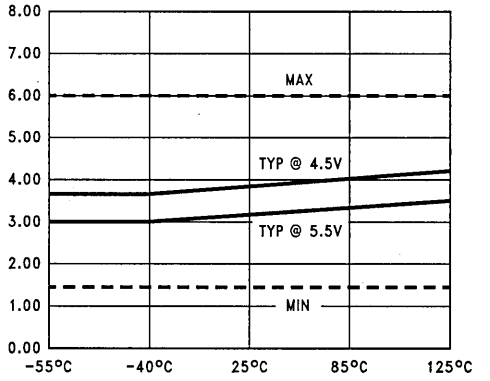
t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



TL/F/10945–19

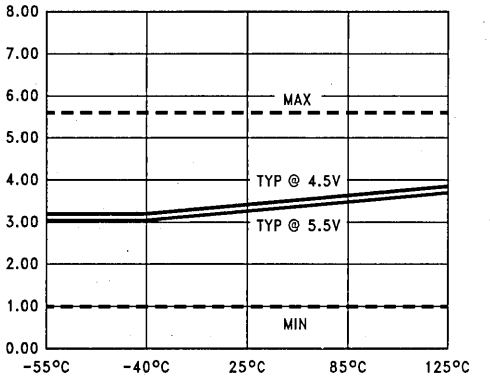
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



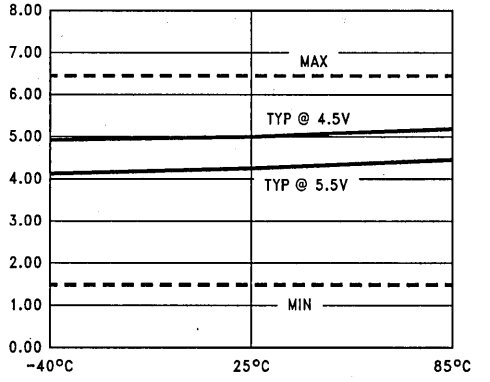
TL/F/10945–20

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



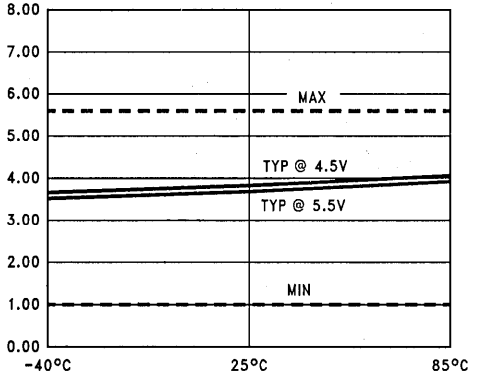
TL/F/10945–21

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



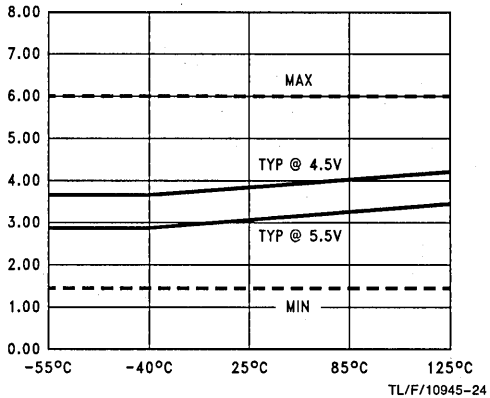
TL/F/10945–22

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



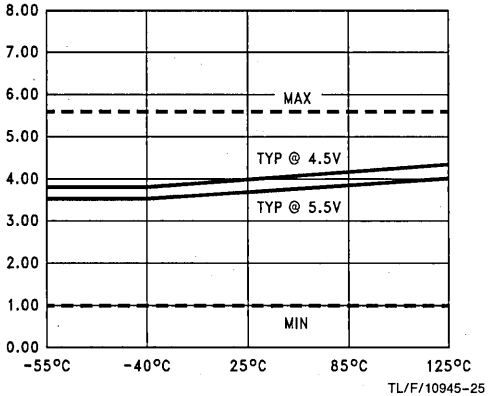
TL/F/10945–23

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



TL/F/10945–24

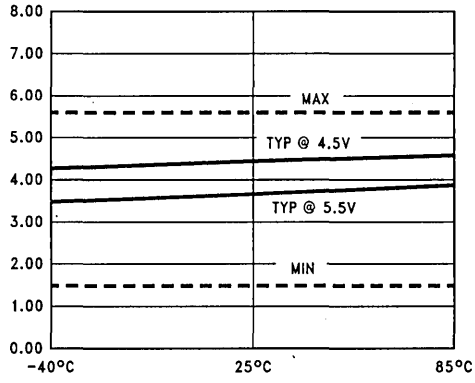
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



TL/F/10945–25

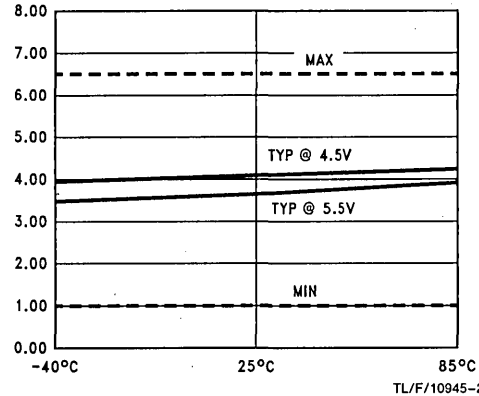
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



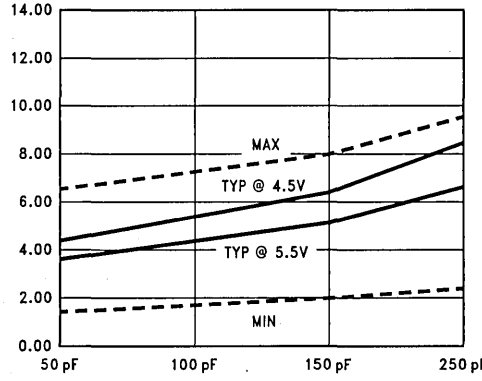
TL/F/10945-26

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



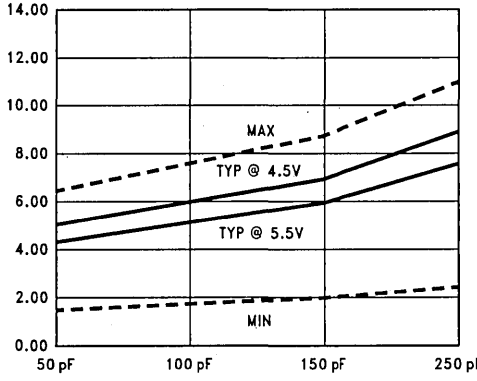
TL/F/10945-27

t_{PZH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



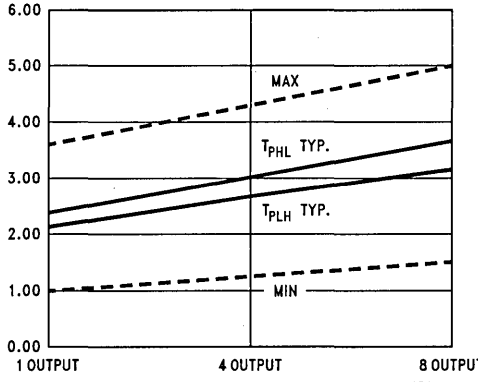
TL/F/10945-28

t_{PZL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



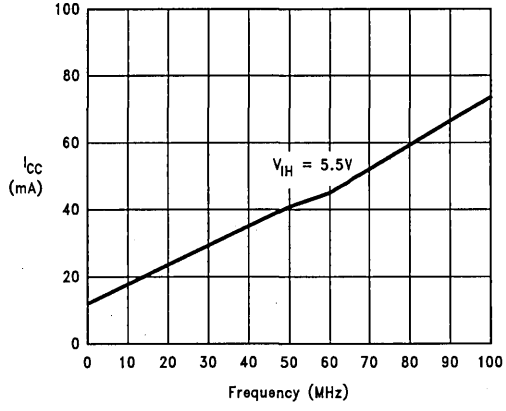
TL/F/10945-29

t_{PLH} and t_{PHL} vs Number Outputs Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



TL/F/10945-30

I_{CC} vs Frequency, Average, T_A = 25°C,
All Outputs Unloaded/Unterminated



TL/F/10945-31

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

5

National Semiconductor

PRELIMINARY

54ABT/74ABT373C
Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'ABT373C consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

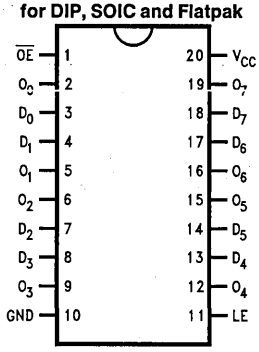
Features

- TRI-STATE outputs for bus interfacing
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention.

Ordering Code: See Section 11

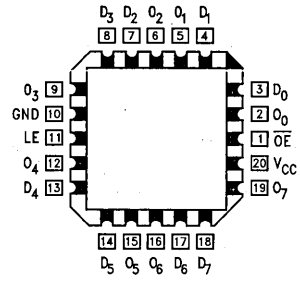
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/11547–1

Pin Assignment for LCC



TL/F/11547–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Latch Outputs

Preliminary Data
National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

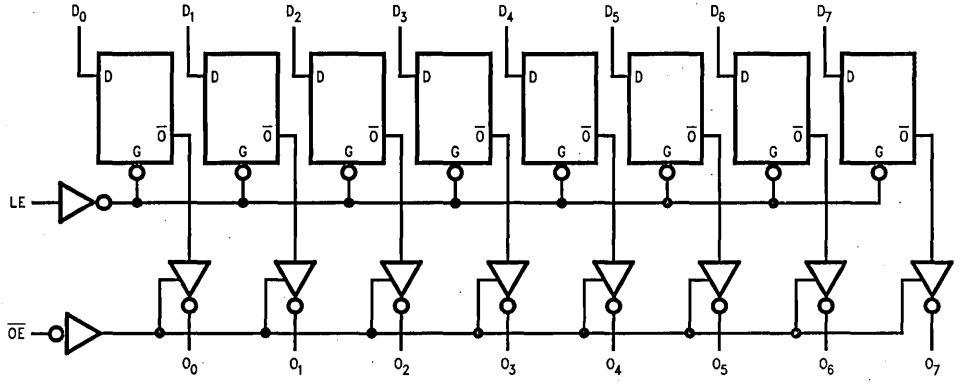
The 'ABT373C contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Output
LE	$\overline{OE}$	D_n	O_n
H	L	H	H
H	L	L	L
L	L	X	O_n (no change)
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance State

Logic Diagram



TL/F/11547–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT373C Min	ABT373C Typ	ABT373C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0					I_{OH} = −12 mA
		74ABT	2.0					I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input							V_I = V_{CC} − 2.1V
		Outputs Enabled			2.5	mA	Max	Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.1	mA/ MHz	Max	Outputs Open $\overline{OE}$ = GND, (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.
Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.8	1.2	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.8		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.0	3.1		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	0.8		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.7	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms (SOIC and SSOP package)

Symbol	Parameter	74ABTC T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			54ABTC T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABTC T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	1.5 1.5					1.5 1.5	4.0 4.0	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	1.5 1.5					1.5 1.5	4.5 4.5	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5					1.5 1.5	6.5 6.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5					1.5 1.5	6.0 6.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABTC T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			54ABTC T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABTC T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to LE						2.5 2.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to LE						1.5 1.5		ns	2-6
$t_w(H)$	Pulse Width, LE HIGH						3.0 3.0		ns	2-3

Extended AC Electrical Characteristics: See Section 2 for Waveforms

(SOIC package)

Symbol	Parameter	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 5)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	1.5	5.5	1.5	6.5	2.5	8.0	ns	2-3, 5
t_{PHL}	D_n to O_n	1.5	5.5	1.5	6.5	2.5	8.0		
t_{PLH}	Propagation Delay	1.5	6.0	1.5	7.0	2.5	8.5	ns	2-3, 5
t_{PHL}	LE to O_n	1.5	6.0	1.5	7.0	2.5	8.5		
t_{PZH}	Output Enable Time	1.5	6.5	2.5	7.5	2.5	10.0	ns	2-4
t_{PZL}		1.5	6.5	2.5	7.5	2.5	12.0		
t_{PHZ}	Output Disable Time	1.5	6.0	(Note 7)		(Note 7)		ns	2-4
t_{PZL}		1.5	6.0						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in plce of the 50 pF load capacitors in the standard AC load. This specificaiton pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (SOIC package) (Note 3)

Symbol	Parameter	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.3	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.8	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	3.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	3.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	3.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions (T_A = 25°C)
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0V
C_{OUT} (Note 1)	Output Capacitance	9	pF	V_{CC} = 5.0V

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

PRELIMINARY

54ABT/74ABT374C
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'ABT374C is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

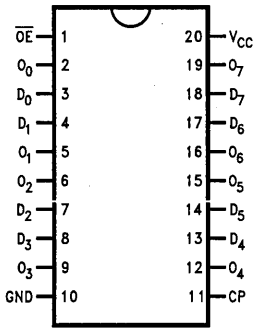
Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code: See Section 11

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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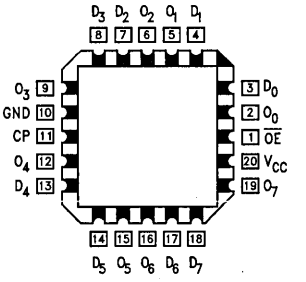
Pin Assignment for LCC



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Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Outputs

Preliminary Data
National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

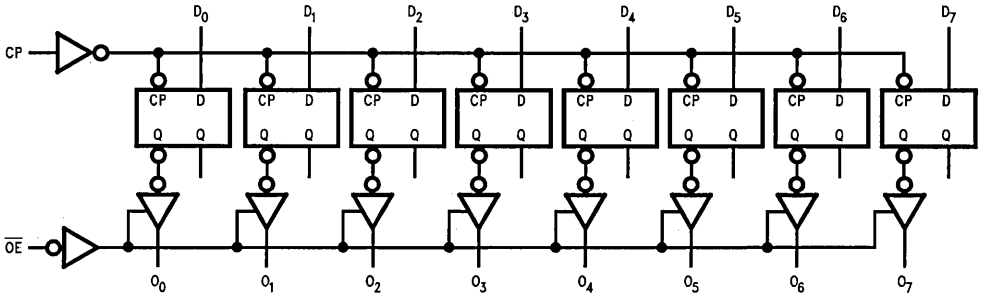
The 'ABT374C consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT374C Min	ABT374C Typ	ABT374C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others V_{CC} or GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC}; All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.1	mA/MHz	Max	Outputs Open $\overline{OE}$ = GND, (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8-bit toggling, I_{CCD} < 0.8 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.8	1.2	V	5.0	$T_A = 25°C$ (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.8		V	5.0	$T_A = 25°C$ (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.0	3.1		V	5.0	$T_A = 25°C$ (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.2	0.8		V	5.0	$T_A = 25°C$ (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	$T_A = 25°C$ (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms (SOIC and SSOP package)

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency		100						MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	1.5 1.5					1.5 1.5	4.0 4.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5					1.5 1.5	6.5 6.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5					1.5 1.5	6.0 6.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.5 2.5				2.5 2.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	1.5 1.5				1.5 1.5		ns	2-6
$t_w(H)$ $t_w(L)$	Pulse Width, CP HIGH or LOW	3.0 3.0				3.0 3.0		ns	2-3

Extended AC Electrical Characteristics: See Section 2 for Waveforms (SOIC package)

Symbol	Parameter	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 5)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Progagation Delay CP to O_n	1.5 1.5	5.5 5.5	1.5 1.5	6.5 6.5	2.5 2.5	8.0 8.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5	6.5 6.5	2.5 2.5	7.5 7.5	2.5 2.5	10.0 12.0	ns	2-4
t_{PHZ} t_{PZL}	Output Disable Time	1.5 1.5	6.0 6.0	(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in plce of the 50 pF load capacitors in the standard AC load. This specificaiton pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (SOIC package) (Note 3)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.3	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.8	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	3.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	3.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	3.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions ($T_A = 25°C$)
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

54ABT/74ABT541C
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ABT541C is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The 'ABT541C is similar to the 'ABT244C with broadside pinout.

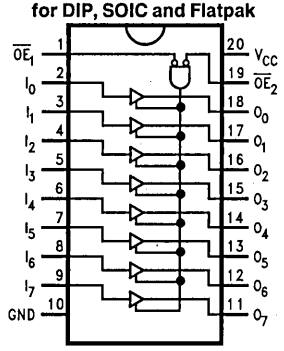
Features

- Non-inverting buffers
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Flow-through pinout for ease of PC board layout
- Disable time less than enable time to avoid bus contention

Ordering Code: See Section 11

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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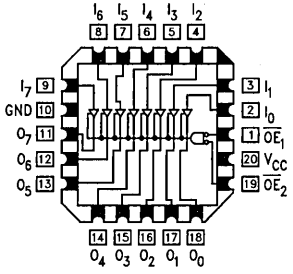
Pin Assignment for LCC



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Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	ABT541C
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active Low)
I_0–I_7	Inputs
O_0–O_7	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT541C Min	ABT541C Typ	ABT541C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}_n$ = V_{CC}; All Others at V_{CC} or Ground
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V; All Others at V_{CC} or Ground
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.1	mA/MHz	Max	Outputs Open, $\overline{OE}_n$ = GND, One Bit Toggling (Note 1), 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.0	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.3	−0.8		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.7	3.1		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.4		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.1	0.6	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP package) : See Section 2

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Outputs	1.0 1.0	2.0 2.4	3.6 3.6			1.0 1.0	3.6 3.6	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5	3.1 3.7	6.0 6.0			1.5 1.5	6.0 6.0	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time	1.0 1.0	3.5 3.1	5.6 5.6			1.0 1.0	5.6 5.6	ns	2-4

Extended AC Electrical Characteristics (SOIC package) : See Section 2

Symbol	Parameter	74ABT −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF, 8 Outputs Switching (Note 4)			74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 1 Output Switching (Note 5)		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH} t_{PHL}	Propagation Delay Data to Outputs	1.5 1.5		5.0 5.0	1.5 1.5	6.0 6.0	2.5 2.5	8.5 8.5	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5		6.5 6.5	2.5 2.5	7.5 7.5	2.5 2.5	9.5 10.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time	1.0 1.0		5.6 5.6	(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew (SOIC package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew, HL Transitions	1.3	2.3	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew, LH Transitions	1.0	1.8	ns	2-15
t_{PS} (Note 5)	Duty Cycle, LH/HL Skew	2.0	3.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew, LH/HL Transitions	2.0	3.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew, LH/HL Transitions	2.0	3.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

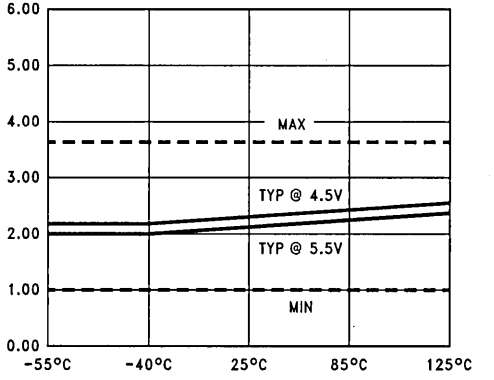
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0V$
C_{OUT}	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency of f = 1 MHz, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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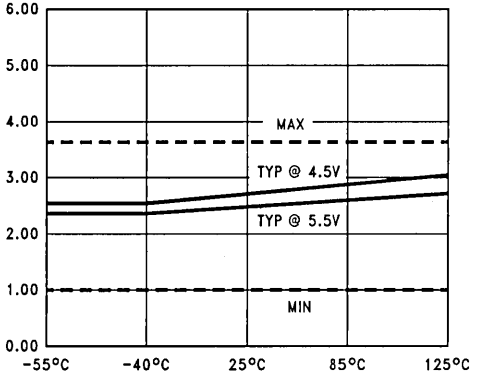
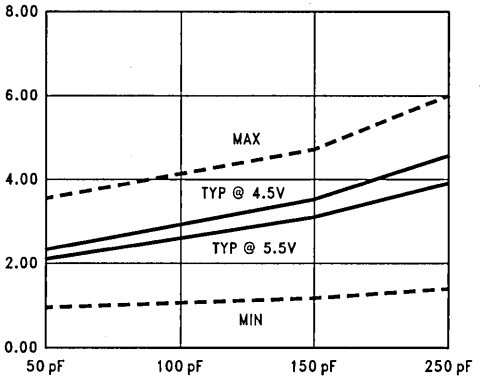
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



TL/F/11501–12

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



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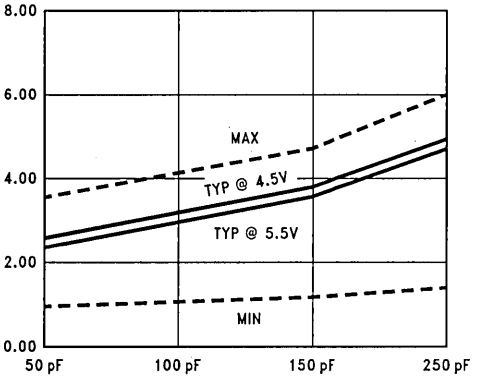
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



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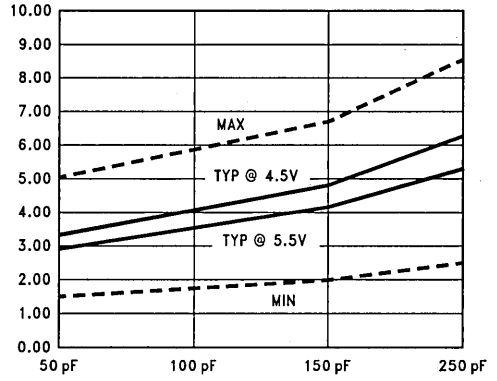
t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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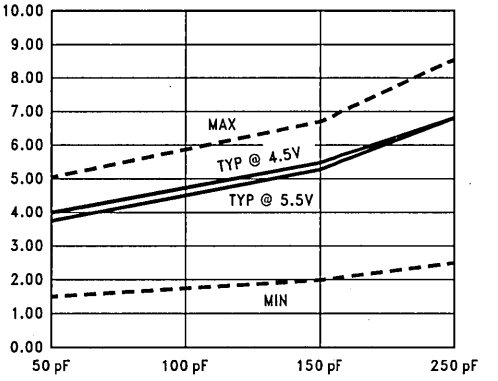
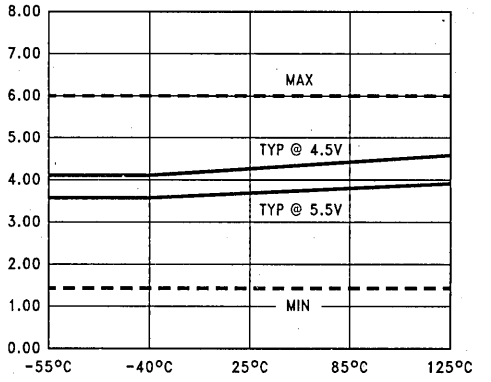
t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



TL/F/11501–16

Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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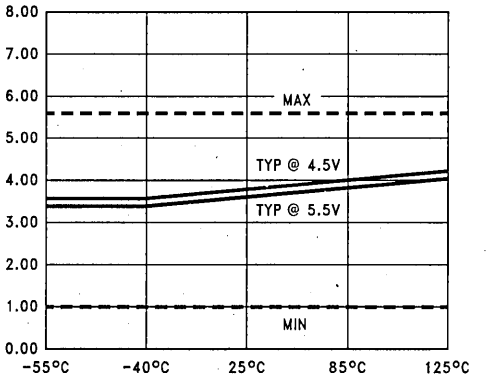
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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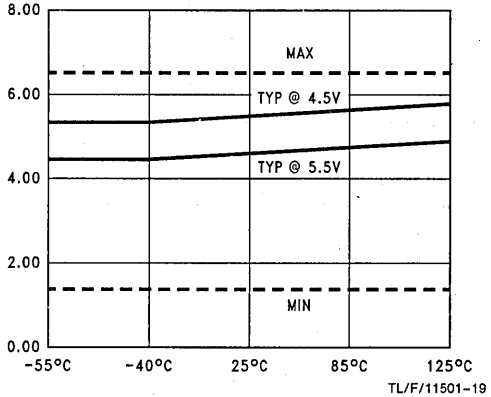
t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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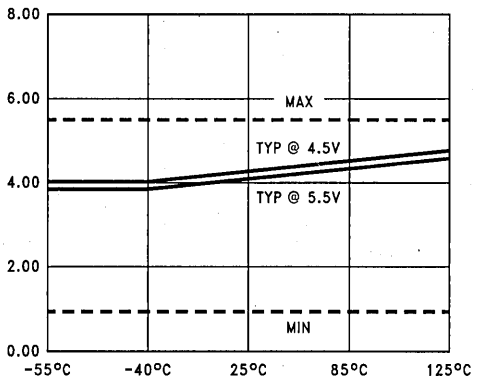
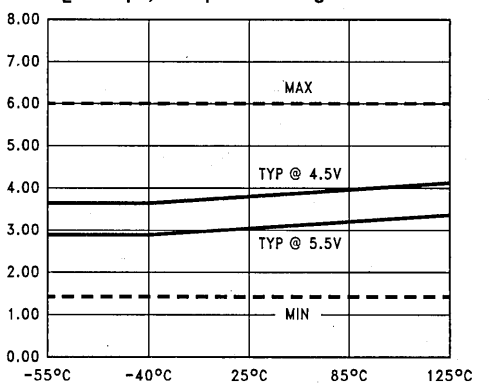
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



TL/F/11501–20

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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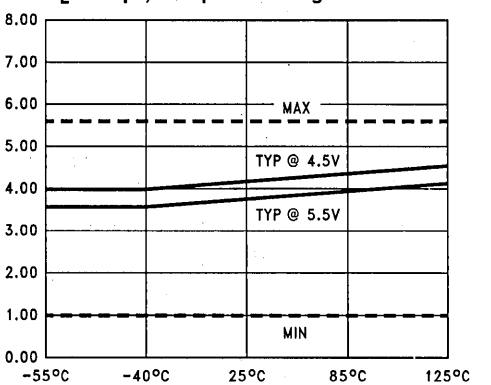
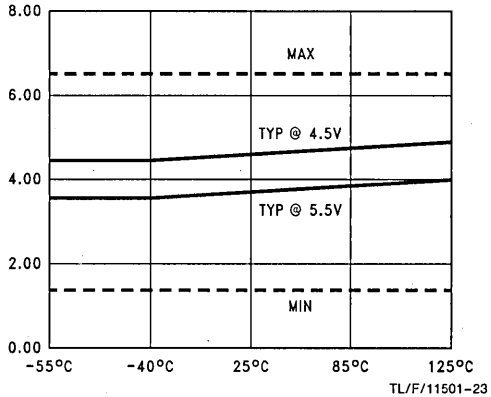
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



TL/F/11501–22

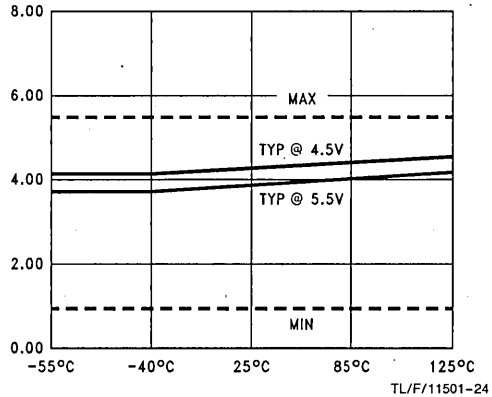
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



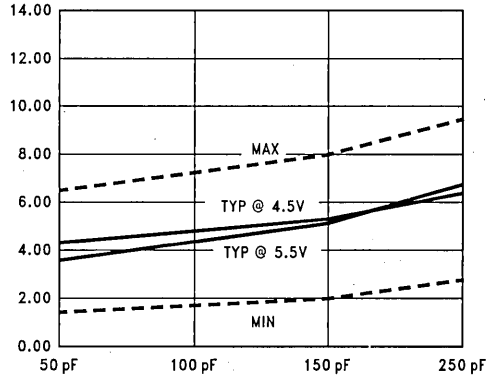
TL/F/11501–23

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



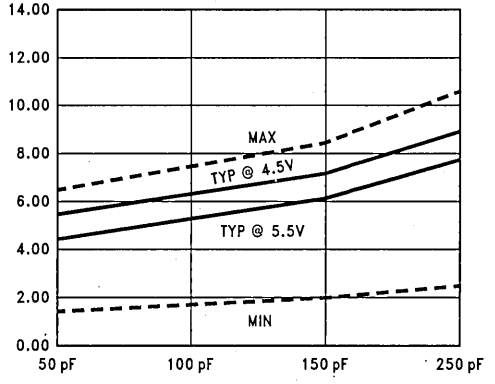
TL/F/11501–24

t_{PZH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



TL/F/11501–25

t_{PZL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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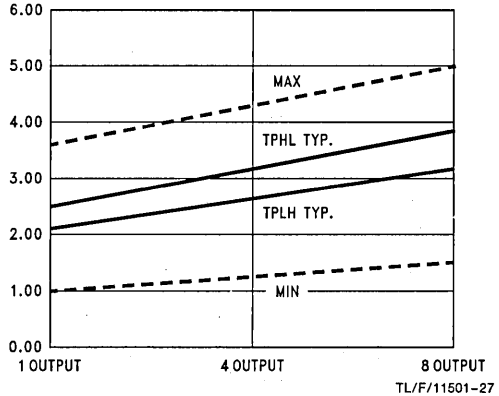
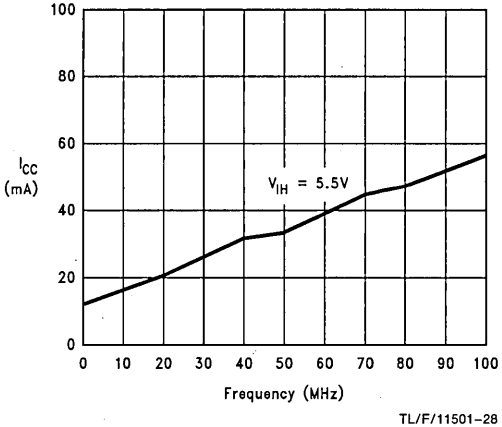
t_{PLH} and t_{PHL} vs Number Outputs Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



TL/F/11501–27

I_{CC} vs Frequency,
Average, T_A = 25°C,
All Outputs Unloaded/Unterminated



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Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

National Semiconductor

54ABT/74ABT543C
Octal Latched Transceiver with TRI-STATE® Outputs

General Description

The 'ABT543C octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

Features

- Back-to-back registers for storage
- Bidirectional data path
- A and B outputs have current sourcing capability of 32 mA and current sinking capability of 64 mA
- Separate controls for data flow in each direction
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

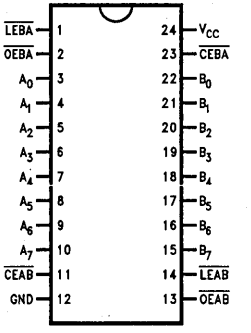
Ordering Code: See Section 11

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable Inputs
$\overline{CEAB}$, $\overline{CEBA}$	Chip Enable Inputs
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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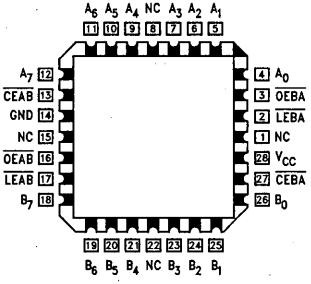
Pin Assignment for LCC



TL/F/11508–2

Functional Description

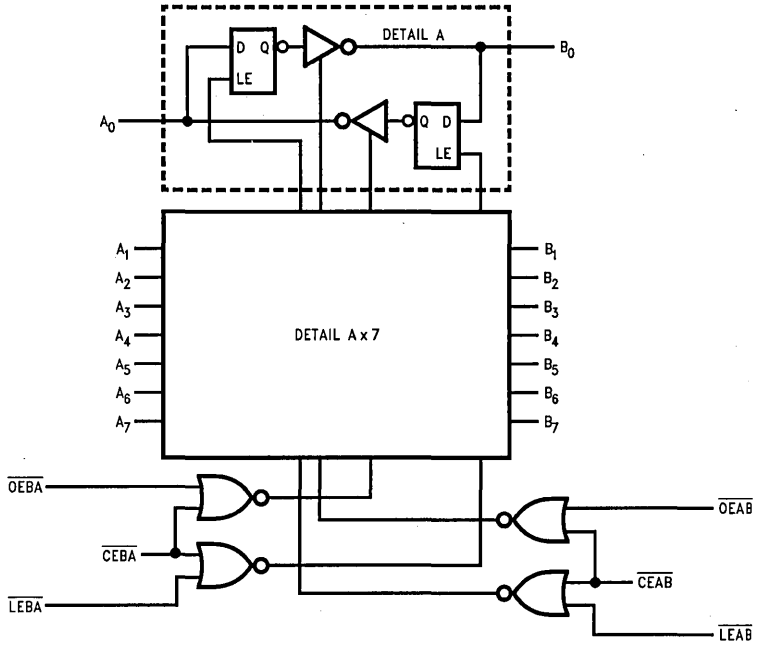
The 'ABT543C contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT543C Min	ABT543C Typ	ABT543C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA, (A_n, B_n)
	54ABT	2.0					I_{OH} = −24 mA, (A_n, B_n)
	74ABT	2.0					I_{OH} = −32 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage 54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n)
	74ABT			0.55			I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V or V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V or 0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{IL} + I_{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	μA	Max	Outputs TRI-STATE All Others at V_{CC} or GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT543C Min	ABT543C Typ	ABT543C Max	Units	V_{CC}	Conditions
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	$V_I = V_{CC} - 2.1V$ All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open, $\overline{CEAB}$ and $\overline{OEAB}$ = GND, $\overline{CEBA}$ = V_{CC}, One Bit Toggling, 50% Duty Cycle, (Note 1)

Note 1: For 8-bit toggling. $I_{CCD} < 1.4$ mA/MHz.
Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC Package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.0	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.8		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25° (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.7	0.9	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.
Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.
Note 3: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP Packages): See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF Min	Typ	Max	54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF Min	Max	74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF Min	Max	Units	Fig. No.
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.5	3.1	4.8			1.5	4.8	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.5	3.4	5.3			1.5	5.3	ns	2-3, 5
t_{PZH} t_{PZL}	Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5	3.6	5.8			1.5	5.8	ns	2-4
t_{PHZ} t_{PLZ}	Disable Time $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5	4.0	6.5			1.5	6.5	ns	2-4

AC Operating Requirements (SOIC and SSOP Packages): See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF Min	Max	54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF Min	Max	74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF Min	Max	Units	Fig. No.
t_S(H) t_S(L)	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	1.5 1.5				1.5 1.5		ns	2-6
t_H(H) t_H(L)	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0 2.0				2.0 2.0		ns	2-6
t_W(L)	Pulse Width, LOW	3.0				3.0		ns	2-3

Extended AC Electrical Characteristics (SOIC Package): See Section 2

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)			74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH}	Progagation Delay	1.5		6.2	2.0	7.5	2.5	10.0	ns	2-3, 5
t_{PHL}	A_n to B_n or B_n to A_n	1.5		6.2	2.0	7.5	2.5	10.0		
t_{PLH}	Progagation Delay	1.5		6.5	2.0	8.0	2.5	10.5	ns	2-3, 5
t_{PHL}	$\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.5		6.5	2.0	8.0	2.5	10.5		
t_{PZH}	Output Enable Time									
t_{PZL}	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5		7.5	2.0	8.5	2.5	11.0	ns	2-4
	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5		7.5	2.0	8.5	2.5	11.0		
t_{PHZ}	Output Disable Time									
t_{PLZ}	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5		8.5	(Note 7)		(Note 7)		ns	2-4
	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5		8.5						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet

Skew (SOIC Package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	2.0	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.3	2.0	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	4.0	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	4.0	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	4.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions: $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$ (non I/O pins)
$C_{I/O}$ (Note 1)	Output Capacitance	11.0	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency, f = 1 MHz, PER MLT-STD-883B, METHOD 3012.

National Semiconductor

PRELIMINARY

54ABT/74ABT573C
Octal D-Type Latch with TRI-STATE® Outputs

General Description

The 'ABT573C is an octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally identical to the 'ABT373C but has different pinouts.

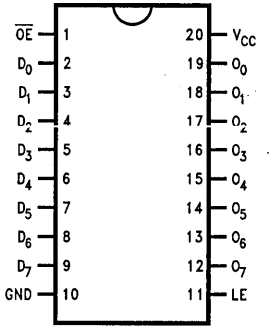
Features

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ABT373C
- TRI-STATE outputs for bus interfacing
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down
- Nondestructive hot insertion capability
- Disable Time less than enable time to avoid bus contention.

Ordering Code: See Section 11

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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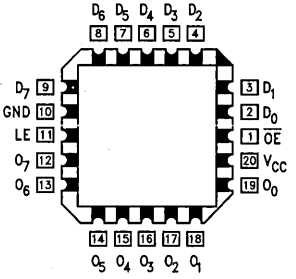
Pin Assignment for LCC



TL/F/11548–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Latch Outputs

Preliminary Data
National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

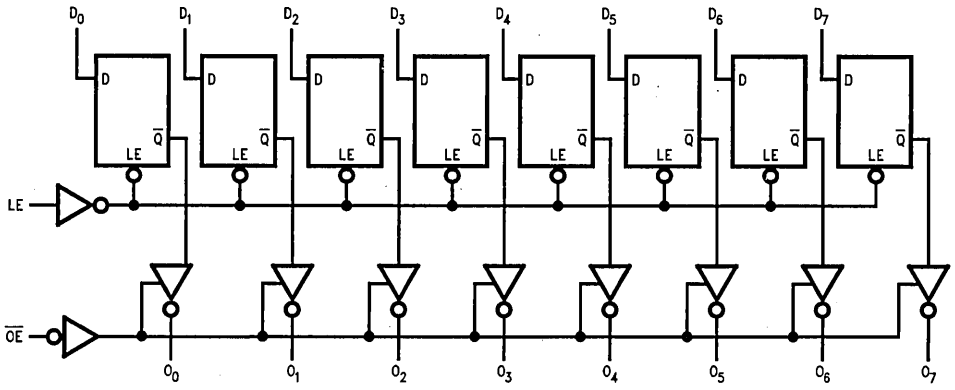
The 'ABT573C contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
O_0 = Value stored from previous clock cycle

Logic Diagram



TL/F/11548–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min), HBM	1000V
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT573C Min	ABT573C Typ	ABT573C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0					I_{OH} = −12 mA
		74ABT	2.0					I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.1	mA/MHz	Max	Outputs Open $\overline{OE}$ = GND, (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 2: Guaranteed but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.8	1.2	V	5.0	$T_A = 25°C$ (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.8		V	5.0	$T_A = 25°C$ (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.0	3.1		V	5.0	$T_A = 25°C$ (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.2	0.8		V	5.0	$T_A = 25°C$ (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	$T_A = 25°C$ (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms (SOIC and SSOP package)

Symbol	Parameter	74ABTC $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54ABTC $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	1.5 1.5		6.0 6.5			1.5 1.5	6.0 6.5	ns	2–3, 5
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	1.5 1.5		6.0 6.5			1.5 1.5	6.0 6.5	ns	2–3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5		6.5 6.5			1.5 1.5	6.5 6.5	ns	2–4
t_{PHZ} t_{PLZ}	Output Disable Time Time	1.5 1.5		6.0 6.0			1.5 1.5	6.0 6.0	ns	2–4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABTC $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54ABTC $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
$t_s(H)$ $t_s(L)$	Set Time, HIGH or LOW D_n to LE						2.5 2.5		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to LE						1.5 1.5		ns	2–6
$t_w(H)$	Pulse Width, LE HIGH						3.0 3.0		ns	2–3

Extended AC Electrical Characteristics: See Section 2 for Waveforms (SOIC package)

Symbol	Parameter	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 5)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	1.5 1.5	7.5 7.5	1.5 1.5	8.0 8.0	2.5 2.5	9.0 9.0	ns	2–3, 5
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	1.5 1.5	7.5 7.5	2.5 2.5	8.5 8.5	2.5 2.5	9.5 9.5	ns	2–3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5	8.0 8.0	2.5 2.5	10.0 10.0	2.5 2.5	11.0 13.0	ns	2–4
t_{PHZ} t_{PLZ}	Output Disable Time	1.0 1.0	7.5 7.5	(Note 7)		(Note 7)		ns	2–4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (SOIC package) (Note 3)

Symbol	Parameter	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.3	ns	2–15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.8	ns	2–15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	3.5	ns	2–16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	3.5	ns	2–19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	3.5	ns	2–22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions (T_A = 25°C)
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0V
C_{OUT} (Note 1)	Output Capacitance	9	pF	V_{CC} = 5.0V

Note 1: C_{OUT} is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012.

National Semiconductor

PRELIMINARY

54ABT/74ABT574C
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'ABT574C is an octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The device is functionally identical to the 'ABT374C except for the pinouts.

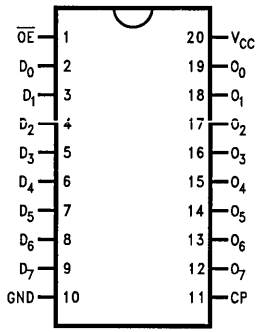
Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ABT374C
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code: See Section 11

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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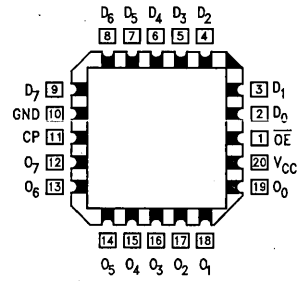
Pin Assignment for LCC



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Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Outputs

Functional Description

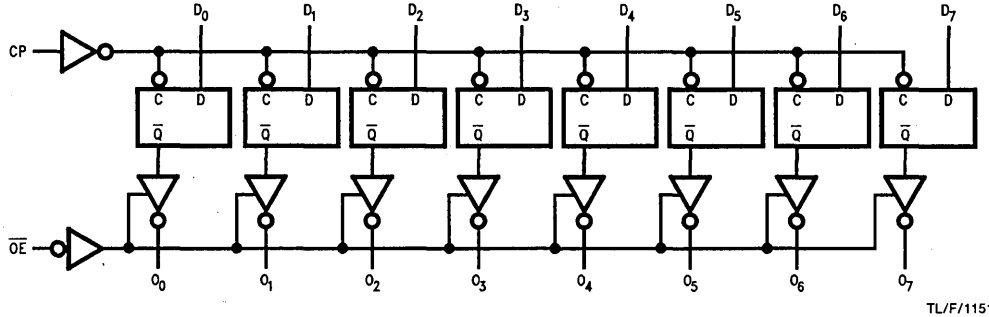
The 'ABT574C consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H or L	L	NC	Z	Hold
H	H or L	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H or L	L	NC	NC	No Change in Data
L	H or L	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT574C Min	ABT574C Typ	ABT574C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Other GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.1	mA/MHz	Max	Outputs Open, $\overline{OE}$ = GND, One Bit Toggling (Note 1), 50% Duty Cycle

Note 1: For 8-bit toggling, I_{CCD} < 0.8 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	1.0	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.5	−1.0		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.0	3.1		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.2	0.8		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for waveforms (SOIC and SSOP Package)

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency		100						MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	1.5 1.5					1.5 1.5	4.0 4.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5					1.5 1.5	6.5 6.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5					1.5 1.5	6.0 6.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF		54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW D_n to CP					2.5 2.5		ns	2-6
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to CP					1.5 1.5		ns	2-6
t_w(H) t_w(L)	Pulse Width, CP, HIGH or LOW					3.0 3.0		ns	2-3

Extended AC Electrical Characteristics: See Section 2 for Waveforms

(SOIC package)

Symbol	Parameter	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 5)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Progagation Delay CP to O_n	1.5 1.5	5.5 5.5	1.5 1.5	6.5 6.5	2.5 2.5	8.0 8.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5	6.5 6.5	2.5 2.5	7.5 7.5	2.5 2.5	10.0 12.0	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5	6.0 6.0	(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in plce of the 50 pF load capacitors in the standard AC load. This specificaiton pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE Delay Times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (SOIC package) (Note 3)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.3	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.8	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	3.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	3.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	3.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

54ABT/74ABT646C
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

The 'ABT646C consists of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{OE}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{OE}$ is Active LOW. In the isolation mode (control $\overline{OE}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

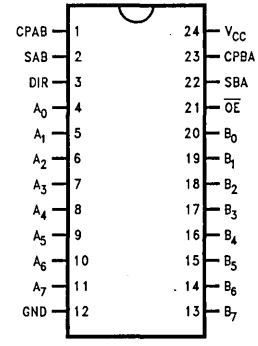
Ordering Code: See Section 11

Pin Descriptions

Pin Names	Description
A_0–A_7	Data Register A Inputs/ TRI-STATE Outputs
B_0–B_7	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
$\overline{OE}$	Output Enable Input
DIR	Direction Control Input

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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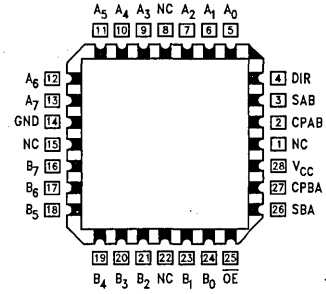
Pin Assignment for LCC



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Real Time Transfer A-Bus to B-Bus

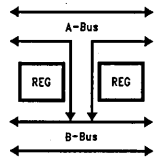

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FIGURE 1

Real Time Transfer B-Bus to A-Bus

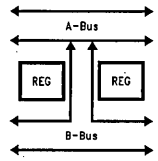

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FIGURE 2

Storage from Bus to Register

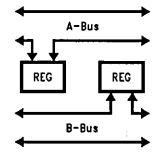

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FIGURE 3

Transfer from Register to Bus

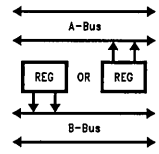

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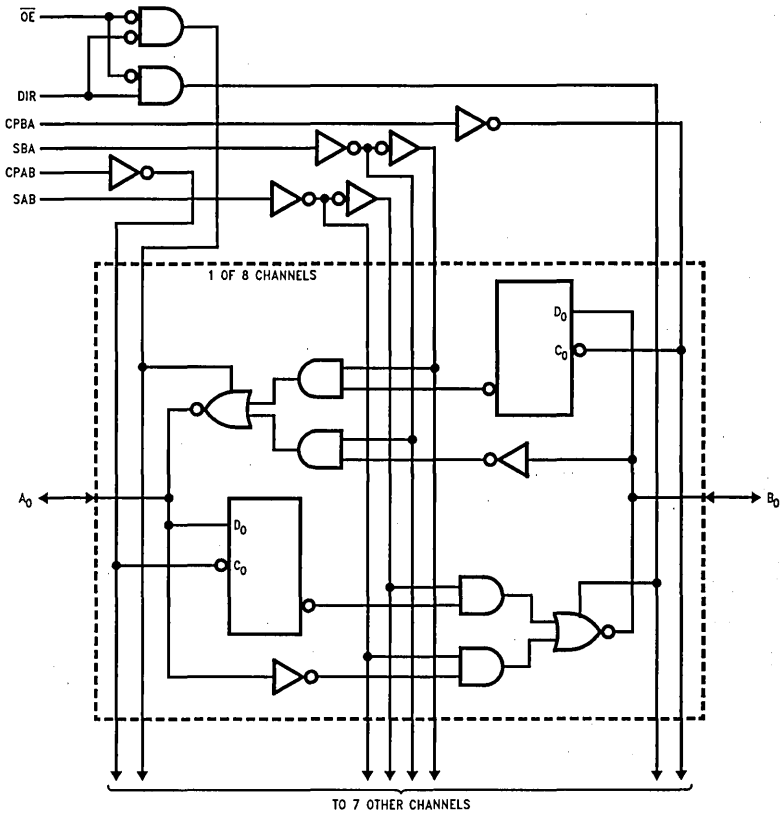
FIGURE 4

Inputs						Data I/O*		Function
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock A_n Data into A Register
H	X	X	↑	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↑	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↑	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT646C Min	ABT646C Typ	ABT646C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 54ABT/74ABT 54ABT' 74ABT	2.5 2.0 2.0			V	Min	I_{OH} = −3 mA, (A_n, B_n) I_{OH} = −24 mA, (A_n, B_n) I_{OH} = −32 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage 54ABT 74ABT			0.55 0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n) I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V or V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V or 0V (Non-I/O Pins)
$I_{IH} + I_{OZH}$	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OE}$ = 2.0V
$I_{IL} + I_{OZL}$	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			250	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	μA	Max	Outputs TRI-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All Other Outputs at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open $\overline{OE}$ and DIR = GND, Non-I/O = GND or V_{CC} (Note 1) One Bit toggling, 50% duty cycle

Note 1: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

Note 2: Guaranteed but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	0.8	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.9		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25° (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.2	1.8		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	0.5	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n -- 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP package): See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	200					200		MHz	
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5 1.5	3.0 3.4	4.9 4.9			1.5 1.5	4.9 4.9	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5 1.5	2.6 3.0	4.5 4.5			1.5 1.5	4.5 4.5	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A_n to B_n	1.5 1.5	3.0 3.4	5.0 5.0			1.5 1.5	5.0 5.0	ns	2-3, 5
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to A_n or B_n	1.5 1.5	3.2 3.5	5.5 5.5			1.5 1.5	5.5 5.5	ns	2-4
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ to A_n or B_n	1.5 1.5	3.7 3.2	6.0 6.0			1.5 1.5	6.0 6.0	ns	2-4
t_{PZH} t_{PZL}	Enable Time DIR to A_n or B_n	1.5 1.5	3.4 3.7	5.5 5.5			1.5 1.5	5.5 5.5	ns	2-4
t_{PHZ} t_{PLZ}	Disable Time DIR to A_n or B_n	1.5 1.5	3.8 3.2	6.0 6.0			1.5 1.5	6.0 6.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF		54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW Bus to Clock	1.5				1.5		ns	2-6
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW Bus to Clock	1.0				1.0		ns	2-6
$t_W(H)$ $t_W(L)$	Pulse Width, HIGH or LOW	3.0				3.0		ns	2-3

Extended AC Electrical Characteristics (SOIC package): See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Progagation Delay Clock to Bus	1.5 1.5	5.5 5.5	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns	2-3, 5
t_{PLH} t_{PHL}	Progagation Delay Bus to Bus	1.5 1.5	6.0 6.0	2.0 2.0	7.0 7.0	2.5 2.5	9.5 9.5	ns	2-3, 5
t_{PLH} t_{PHL}	Progagation Delay SBA or SAB to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_n$ or DIR to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	8.0 8.0	2.5 2.5	10.5 10.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_n$ or DIR to A_n or B_n	1.5 1.5	6.0 6.0	(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (SOIC package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.5	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	2.0	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	4.0		2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	4.0	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	4.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

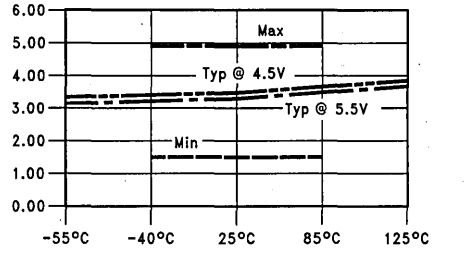
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$ (non I/O pins)
$C_{I/O}$ (Note 1)	Output Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Clock to Bus



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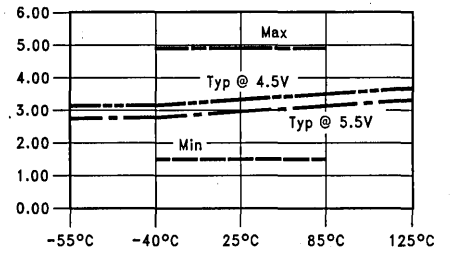
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Clock to Bus



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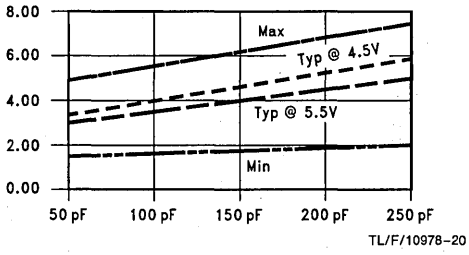
t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C
Clock to Bus



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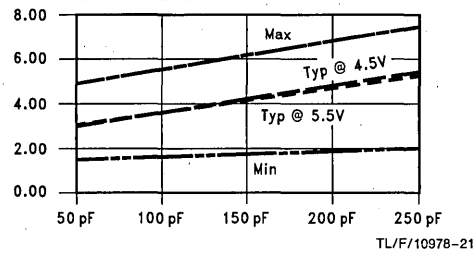
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C
Clock to Bus



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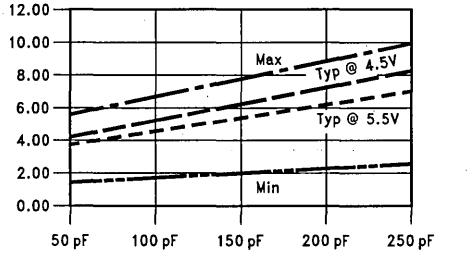
t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Clock to Bus



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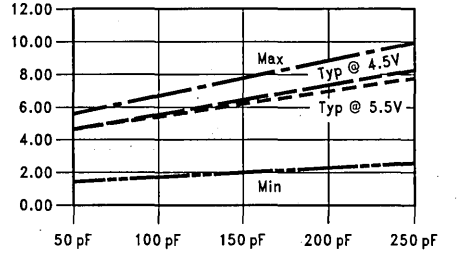
t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Clock to Bus



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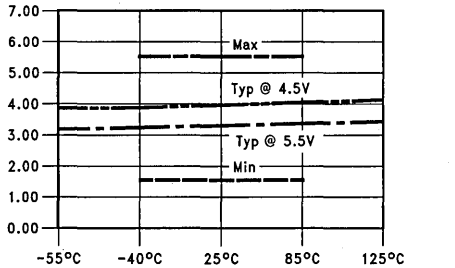
t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
$\overline{OE}$ to Bus



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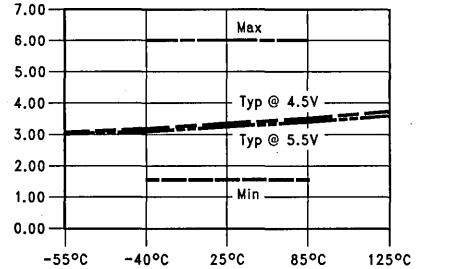
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
$\overline{OE}$ to Bus



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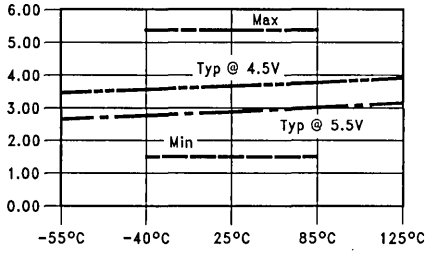
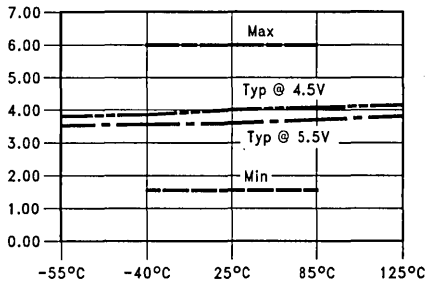
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



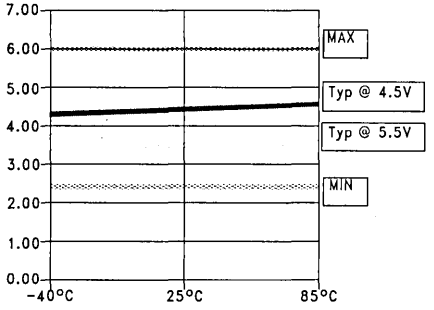
TL/F/10978-26

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
$\overline{OE}$ to Bus



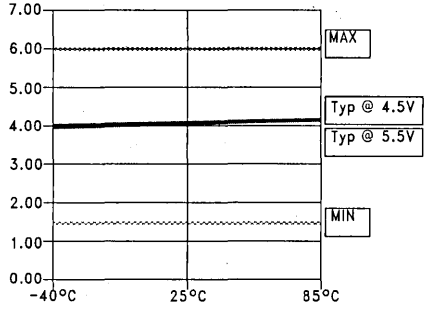
TL/F/10978-27

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching
$\overline{OE}$ to Bus



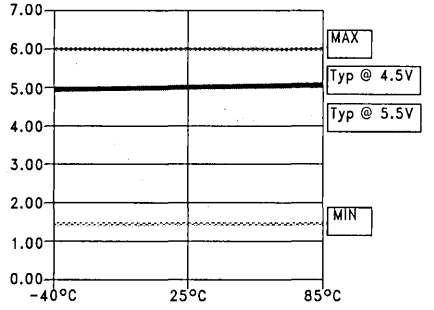
TL/F/10978-28

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching
$\overline{OE}$ to Bus



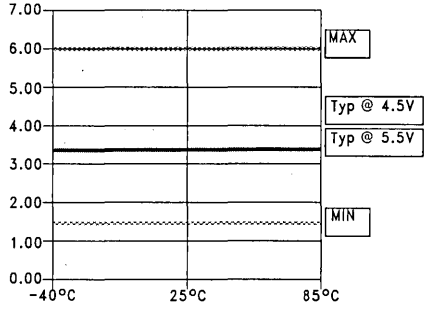
TL/F/10978-29

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching
$\overline{OE}$ to Bus



TL/F/10978-30

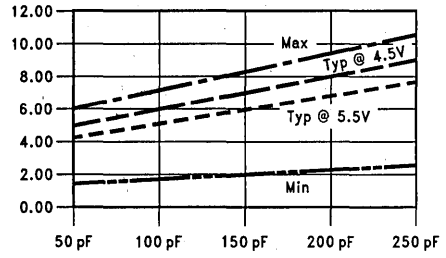
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching
$\overline{OE}$ to Bus



TL/F/10978-31

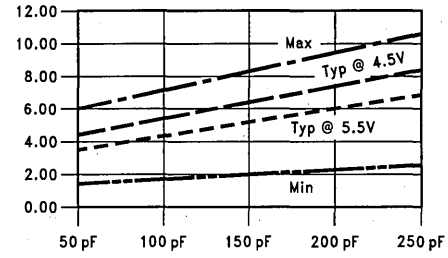
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PZL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
$\overline{OE}$ to Bus



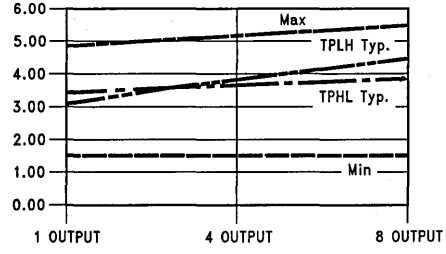
TL/F/10978–32

t_{PZH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
$\overline{OE}$ to Bus



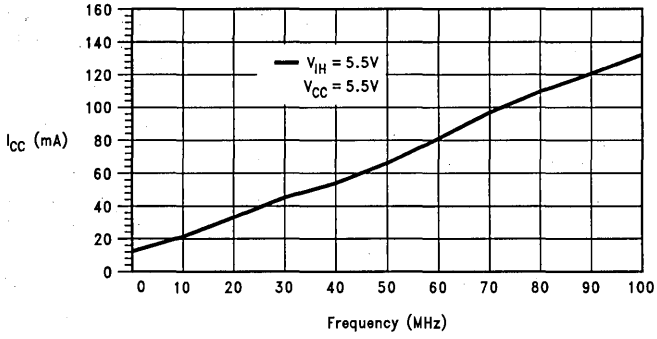
TL/F/10978–33

t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C
C_L = 50 pF, Clock to Bus



TL/F/10978–34

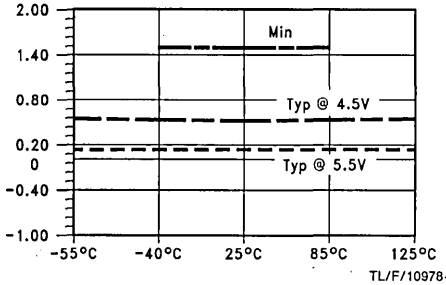
I_{CC} vs Frequency, Average,
T_A = 25°C, V_{CC} = 5.5V
All Outputs Unloaded/Unterminated;
All Outputs Switching in phase @50% Duty Cycle



TL/F/10978–35

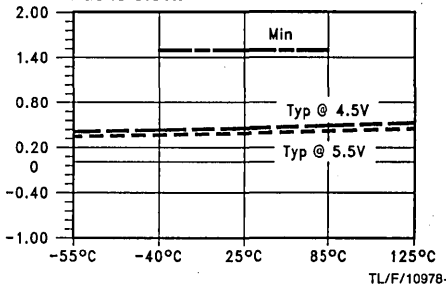
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{SET} LOW vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Clock



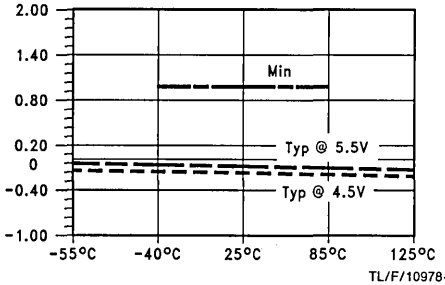
TL/F/10978-36

t_{SET} HIGH vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Clock



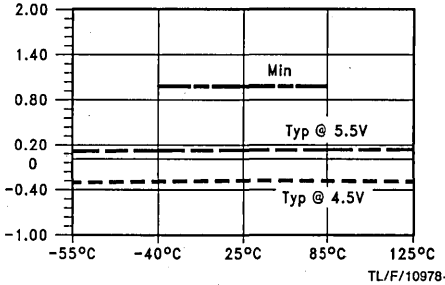
TL/F/10978-37

t_{HOLD} LOW vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Clock



TL/F/10978-38

t_{HOLD} HIGH vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Clock



TL/F/10978-39

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

National Semiconductor

54ABT/74ABT652C
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

The 'ABT652C consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

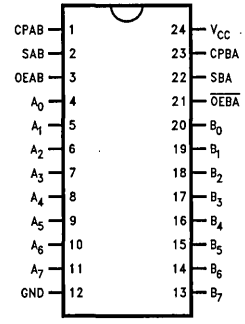
Ordering Code: See Section 11

Pin Descriptions

Pin Names	Description
A_0–A_7	Data Register A Inputs/ TRI-STATE Outputs
B_0–B_7	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

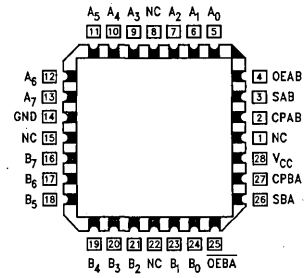
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



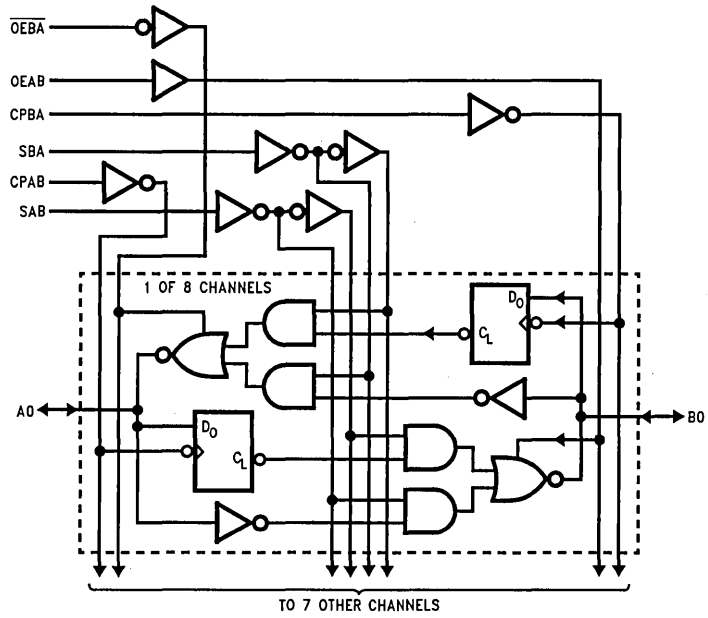
TL/F/11512–1

Pin Assignment for LCC



TL/F/11512–2

Logic Diagram



TL/F/11512–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

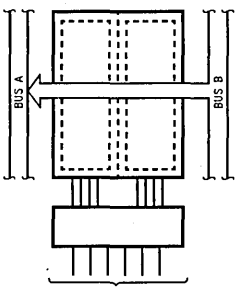
The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the 'ABT652C.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Functional Description (Continued)

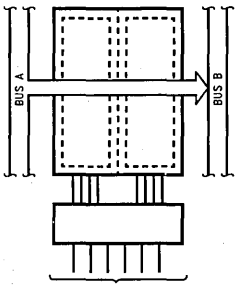
Note A: Real-Time Transfer Bus B to Bus A



TL/F/11512–4

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

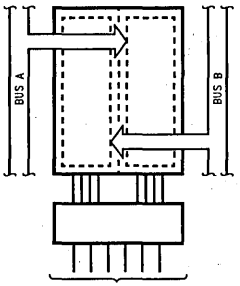
Note B: Real-Time Transfer Bus A to Bus B



TL/F/11512–5

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

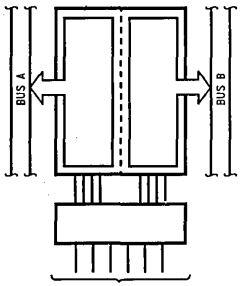
Note C: Storage



TL/F/11512–6

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↓	X	X	X
L	X	X	↓	X	X
L	H	↓	↓	X	X

Note D: Transfer Storage Data to A or B



TL/F/11512–7

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	X

FIGURE 1

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↓	↓	X	X			Store A and B Data
X	H	↓	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↓	↓	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↓	X	X	Not Specified	Input	Hold A, Store B
L	L	↓	↓	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT652C			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA, (A_n, B_n)
	54ABT	2.0					I_{OH} = −24 mA, (A_n, B_n)
	74ABT	2.0					I_{OH} = −32 mA, (A_n, B_n)
V_{OL}	Output LOW 54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n)
	Voltage 74ABT			0.55			I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V or V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V or 0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEBA}$ = 2.0V and OEAB = GND = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEBA}$ = 2.0V and OEAB = GND = 2.0V

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT652C Min	ABT652C Typ	ABT652C Max	Units	V_{CC}	Conditions
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			250	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	μA	Max	Outputs TRI-STATE; All others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open (Note 1) OEAB = $\overline{OEBA}$ = GND One bit toggling, 50% duty cycle (Note 1)

Note 1: For 8 outputs toggling, I_{CCD} < 1.4 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	0.8	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.9		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25° (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.2	1.8		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	0.4	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP package): See Section 2

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF Min	Typ	Max	54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF Min	Max	74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF Min	Max	Units	Fig. No.
f_{max}	Max Clock Frequency	200					200		MHz	
t_{PLH}	Propagation Delay	1.5	3.0	4.9			1.5	4.9	ns	2-3, 5
t_{PHL}	Clock to Bus	1.5	3.4	4.9			1.5	4.9		
t_{PLH}	Propagation Delay	1.5	2.6	4.5			1.5	4.5	ns	2-3, 5
t_{PHL}	Bus to Bus	1.5	3.0	4.5			1.5	4.5		
t_{PLH}	Propagation Delay	1.5	3.0	5.0			1.5	5.0	ns	2-3, 5
t_{PHL}	SBA or SAB to A_n to B_n	1.5	3.4	5.0			1.5	5.0		
t_{PZH}	Enable Time	1.5	3.3	5.5			1.5	5.5	ns	2-4
t_{PZL}	$\overline{OEBA}$ or OEAB to A_n or B_n	1.5	3.7	5.5			1.5	5.5		
t_{PHZ}	Disable Time	1.5	3.7	6.0			1.5	6.0	ns	2-4
t_{PLZ}	$\overline{OEBA}$ or OEAB to A_n or B_n	1.5	3.3	6.0			1.5	6.0		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		54ABT $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW Bus to Clock	1.5				1.5		ns	2-6
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW Bus to Clock	1.0				1.0		ns	2-6
$t_W(H)$ $t_W(L)$	Pulse Width, HIGH or LOW	3.0				3.0		ns	2-3

Extended AC Electrical Characteristics (SOIC package): See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 4)		74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Progagation Delay Clock to Bus	1.5 1.5	5.5 5.5	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns	2-3, 5
t_{PLH} t_{PHL}	Progagation Delay Bus to Bus	1.5 1.5	6.0 6.0	2.0 2.0	7.0 7.0	2.5 2.5	9.5 9.5	ns	2-3, 5
t_{PLH} t_{PHL}	Progagation Delay SBA or SAB to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	8.0 8.0	2.5 2.5	11.5 11.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.5 1.5	6.0 6.0	(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (SOIC Package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.5	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	2.0	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	4.0		2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	4.0	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	4.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

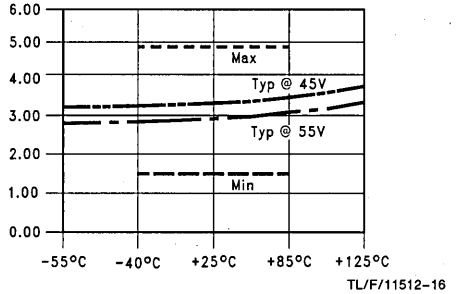
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions ($T_A = 25°C$)
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$ (non I/O pins)
$C_{I/O}$ (Note 1)	I/O Capacitance	11.0	pF	$V_{CC} = 5.0V$ (A_n, B_n)

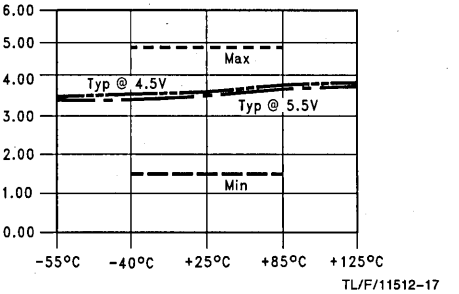
Note 1: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883D, Method 3012.

t_{PLH} vs Temperature (T_A)
$C_L = 50$ pF, 1 Output Switching
Clock to Bus



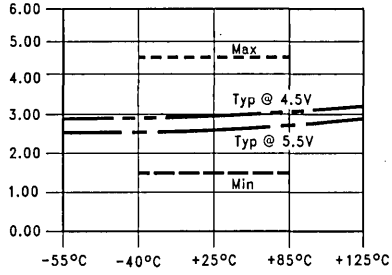
TL/F/11512–16

t_{PHL} vs Temperature (T_A)
$C_L = 50$ pF, 1 Output Switching
Clock to Bus



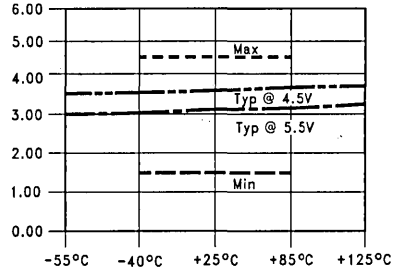
TL/F/11512–17

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Bus



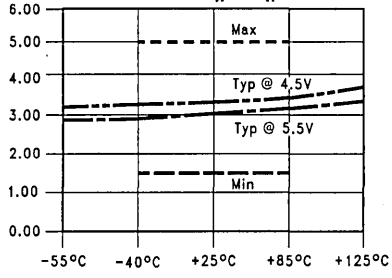
TL/F/11512–18

t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Bus



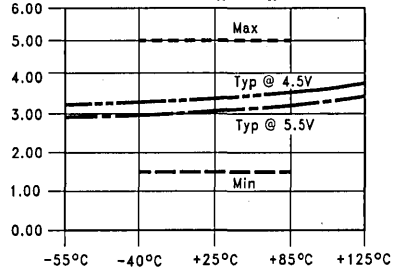
TL/F/11512–19

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
SBA or SAB to A_n or B_n



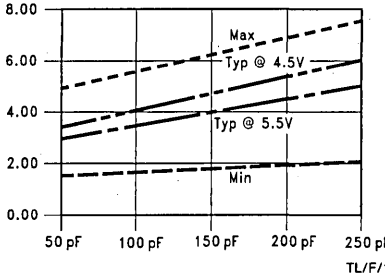
TL/F/11512–20

t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
SBA or SAB to A_n or B_n



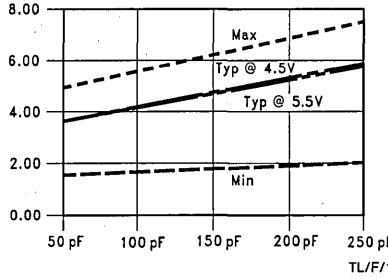
TL/F/11512–21

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C
Clock to Bus



TL/F/11512–22

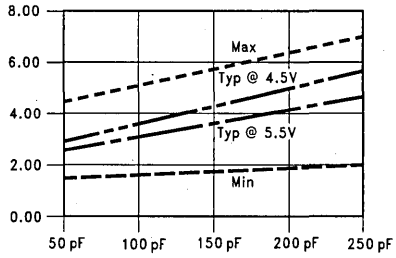
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C
Clock to Bus



TL/F/11512–23

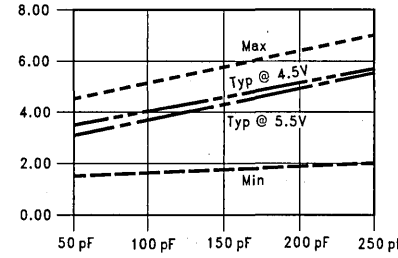
5

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C
Bus to Bus



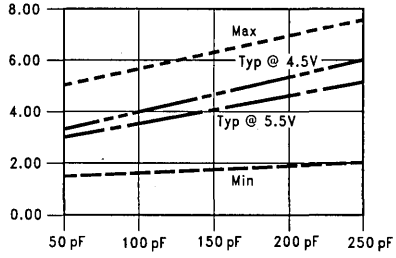
TL/F/11512-24

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C
Bus to Bus



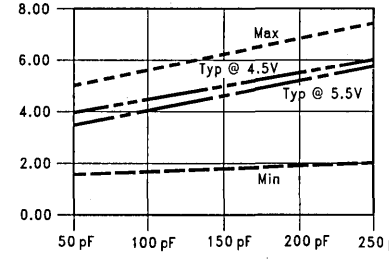
TL/F/11512-25

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C
SBA or SAB to A_n or B_n



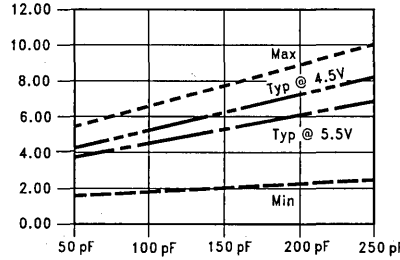
TL/F/11512-26

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C
SBA or SAB to A_n or B_n



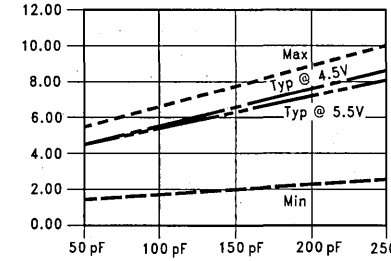
TL/F/11512-27

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Clock to Bus



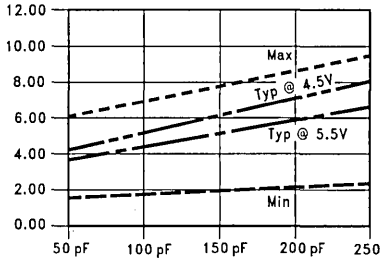
TL/F/11512-28

t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Clock to Bus



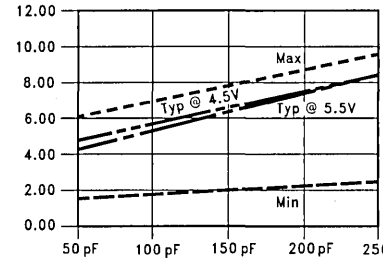
TL/F/11512-29

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Bus to Bus



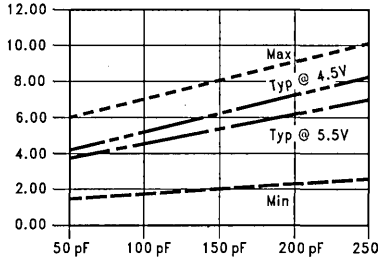
TL/F/11512–30

t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Bus to Bus



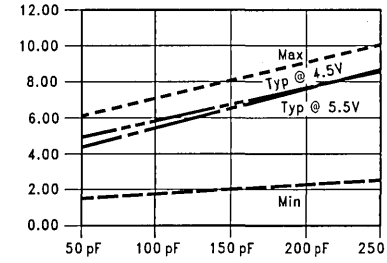
TL/F/11512–31

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
SBA or SAB to A_n or B_n



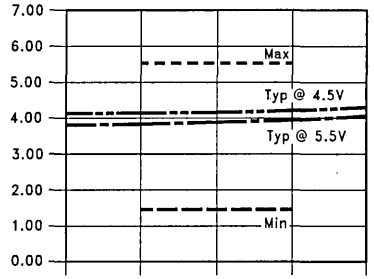
TL/F/11512–32

t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
SBA or SAB to A_n or B_n



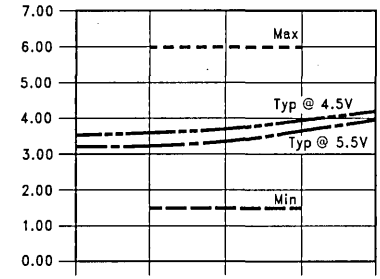
TL/F/11512–33

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



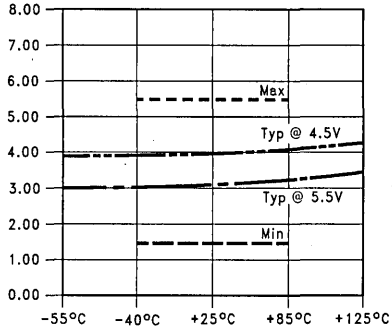
TL/F/11512–34

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



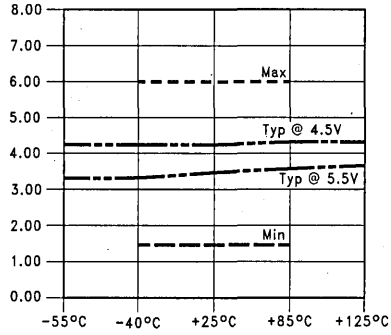
TL/F/11512–35

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



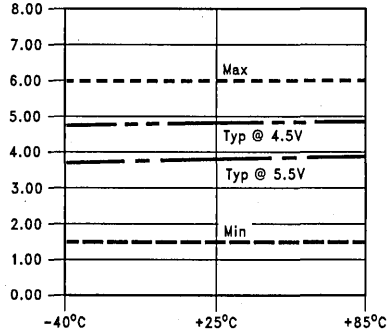
TL/F/11512-36

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



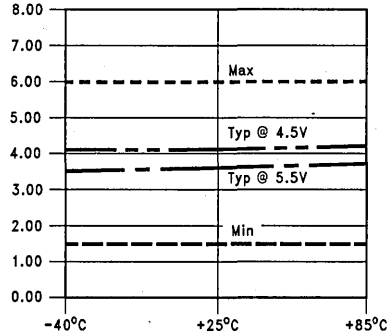
TL/F/11512-37

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



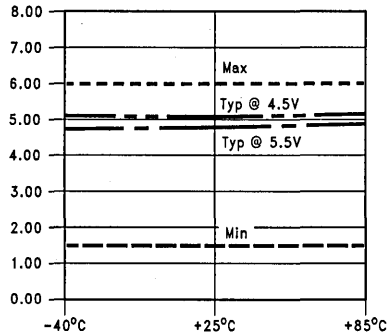
TL/F/11512-38

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



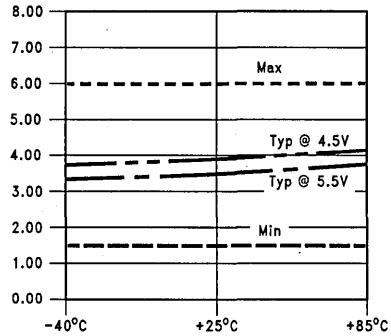
TL/F/11512-39

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



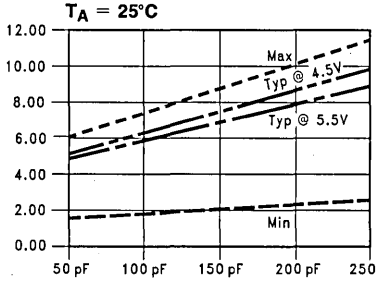
TL/F/11512-40

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



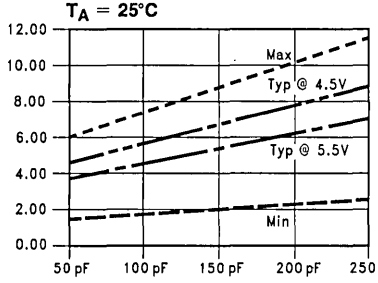
TL/F/11512-41

t_{PZL} vs Load Capacitance
8 Outputs Switching
$T_A = 25°C$



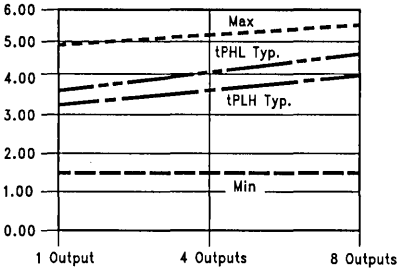
TL/F/11512–42

t_{PZH} vs Load Capacitance
8 Outputs Switching
$T_A = 25°C$



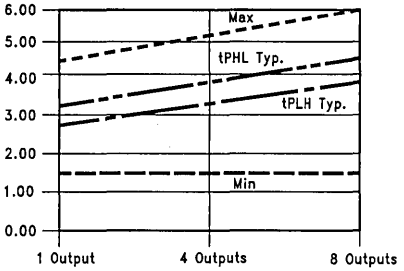
TL/F/11512–43

t_{PLH} and t_{PHL} vs Number Output Switching
$V_{CC} = 5V, T_A = 25°C, C_L = 50$ pF
Clock to Bus



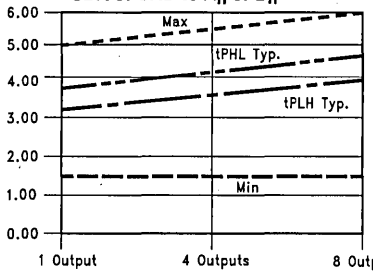
TL/F/11512–44

t_{PLH} and t_{PHL} vs Number Output Switching
$V_{CC} = 5V, T_A = 25°C, C_L = 50$ pF
Bus to Bus



TL/F/11512–45

t_{PLH} and t_{PHL} vs Number Output Switching
$V_{CC} = 5V, T_A = 25°C, C_L = 50$ pF
SBA or SAB to A_n or B_n



TL/F/11512–46

National Semiconductor

PRELIMINARY

54ABT/74ABT899
9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

The 'ABT899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction.

The 'ABT899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

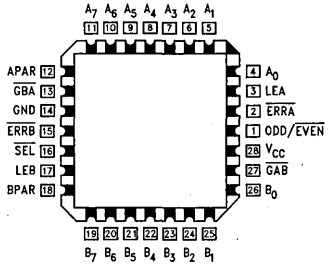
Features

- Latchable transceiver with output sink of 64 mA
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enables for A-to-B and B-to-A directions
- Select pin for ODD/$\overline{\text{EVEN}}$ parity
- $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in systems applications in place of the '543 and '280
- May be used in system applications in place of the '657 and '373 (no need to change T/$\overline{\text{R}}$ to check parity)
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code: See Section 11

Connection Diagrams

Pin Assignment for PCC



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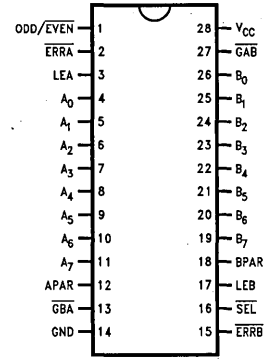
Pin Assignment for DIP, SOIC and Flatpak



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Pin Names	Description
A_0–A_7	A Bus Data Inputs/Data Outputs
B_0–B_7	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs/Outputs
ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ Parity Select, Active LOW for EVEN Parity
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output Enables for A or B Bus, Active LOW
$\overline{\text{SEL}}$	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The 'ABT899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

— Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select ($\overline{SEL}$) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by $\overline{ERRB}$ ($\overline{ERRA}$).

— Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{SEL}$ is HIGH. Parity is still generated and checked as $\overline{ERRA}$ and $\overline{ERRB}$ in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).

— Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table below).

Function Table

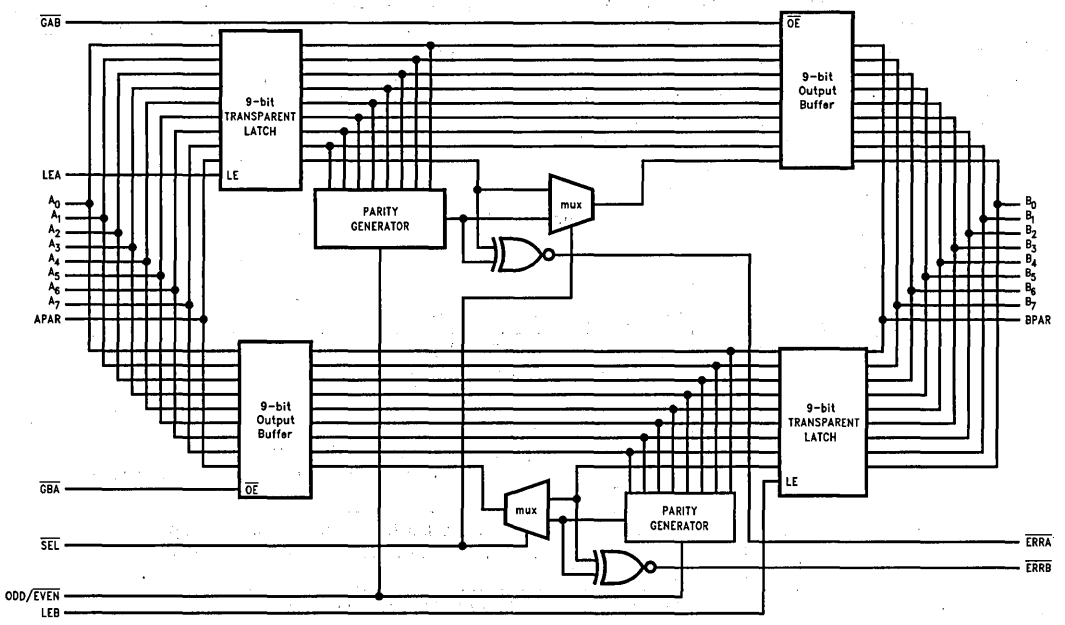
Inputs					Operation
$\overline{GAB}$	$\overline{GBA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	Busses A and B are TRI-STATE®.
H	L	L	L	H	Generates parity from B[0:7] based on O/$\overline{E}$ (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	L	H	H	Generates parity from B[0:7] based on O/$\overline{E}$. Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$. Generated parity also fed back through the A latch for generate/check as $\overline{ERRA}$.
H	L	L	X	L	Generates parity from B latch data based on O/$\overline{E}$. Generated parity → APAR. Generated parity checked against latched BPAR and output as $\overline{ERRB}$.
H	L	H	X	H	BPAR/B[0:7] → APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	H	H	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$. Generated parity also fed back through the A latch for generate/check as $\overline{ERRA}$.
L	H	L	H	L	Generates parity for A[0:7] based on O/$\overline{E}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	L	H	H	Generates parity from A[0:7] based on O/$\overline{E}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$. Generated parity also fed back through the B latch for generate/check as $\overline{ERRB}$.
L	H	L	L	X	Generates parity from A latch data based on O/$\overline{E}$. Generated parity → BPAR. Generated parity checked against latched APAR and output as $\overline{ERRA}$.
L	H	H	H	L	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	H	H	H	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$. Generated parity also fed back through the B latch for generate/check as $\overline{ERRB}$.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Note 1: O/$\overline{E}$ = ODD/$\overline{EVEN}$

5

Functional Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT899 Min	ABT899 Typ	ABT899 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA, (A_n, B_n, APAR, BPAR)
	54ABT	2.0					I_{OH} = −24 mA, (A_n, B_n, APAR, BPAR)
	74ABT	2.0					I_{OH} = −32 mA, (A_n, B_n, APAR, BPAR)
V_{OL}	Output LOW Voltage 54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n, APAR, BPAR)
	74ABT			0.55			I_{OL} = 64 mA, (A_n, B_n, APAR, BPAR)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V or V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n, APAR, BPAR)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V or 0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{GAB}$ and $\overline{GBA}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{GAB}$ and $\overline{GBA}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n, APAR, BPAR)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n, APAR, BPAR)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n, APAR, BPAR); All Others GND
I_{CCH}	Power Supply Current			100	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			34	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			100	μA	Max	Outputs TRI-STATE All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open $\overline{GAB}$ or $\overline{GBA}$ = GND, Non-I/O = GND or V_{CC} One bit toggling, 50% duty cycle

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (PLCC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.8	1.0	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.8		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (PLCC package): See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, APAR to B_n, BPAR	1.0 1.0		4.9 4.6			1.0 1.0	4.9 4.6	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to BPAR, APAR	3.0 2.5		9.0 7.5			3.0 2.5	9.0 7.5	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$	2.8 2.8		8.2 8.1			2.8 2.8	8.2 8.1	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	1.0 1.0		5.3 5.5			1.0 1.0	5.3 5.5	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay ODD/EVEN to APAR, BPAR	2.0 2.0		7.5 7.8			2.0 2.0	7.5 7.8	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	1.8 1.8		6.8 7.3			1.8 1.8	6.8 7.3	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay SEL to APAR, BPAR	1.0 1.0		5.3 4.8			1.0 1.0	5.3 4.8	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay LEA, LEB to B_n, A_n	1.0 1.0		4.9 4.8			1.0 1.0	4.9 4.8	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay LEA, LEB to BPAR, APAR	1.5 1.5		9.5 8.3			1.5 1.5	9.5 8.3	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$	1.6 1.6		8.4 9.2			1.6 1.6	8.4 9.2	ns	2-3, 5
t_{PZH} t_{PZL}	Output enable time $\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	1.0 1.3		6.0 6.0			1.0 1.3	6.0 6.0	ns	2-4
t_{PHZ} t_{PLZ}	Output disable time $\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR	0.5 0.5		5.5 5.5			0.5 0.5	5.5 5.5	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		54ABT $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW A_n, APAR to LEA or B_n, BPAR to LEB					2.0 1.5		ns	2-6
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW A_n, APAR to LEA or B_n, BPAR to LEB					1.5 1.0		ns	2-6
$t_W(H)$	Pulse Width, HIGH LEA or LEB					3.0		ns	2-3

Extended AC Electrical Characteristics (PLCC package)

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF, 9 Outputs Switching (Note 4)			74ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 250$ pF, 9 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency								MHz	
t_{PLH} t_{PHL}	Propagation Delay A_n, APAR to B_n, BPAR								ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to BPAR, APAR								ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$								ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$								ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay ODD/EVEN to APAR, BPAR								ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$								ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay SEL to APAR, BPAR								ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay LEA, LEB to B_n, A_n								ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay LEA, LEB to BPAR, APAR								ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$								ns	2-3, 5
t_{PZH} t_{PZL}	Output enable time $\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR								ns	2-4
t_{PHZ} t_{PLZ}	Output disable time $\overline{GBA}$ or $\overline{GAB}$ to A_n, APAR or B_n, BPAR				(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (PLCC package) (Note 3)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 9 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 9 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.3	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.8	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	3.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	3.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	3.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

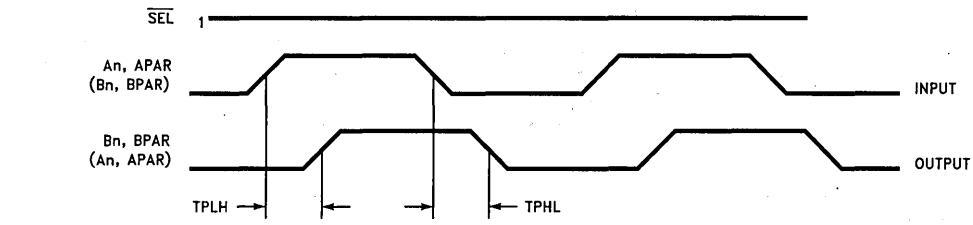
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Pin Capacitance	5.0	pF	$V_{CC} = 0V$
$C_{I/O}$ (Note 1)	Output Capacitance	11.0	pF	$V_{CC} = 5.0V$

Note 1: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Path



A_n, APAR → B_n, BPAR
(B_n, BPAR → A_n, APAR)

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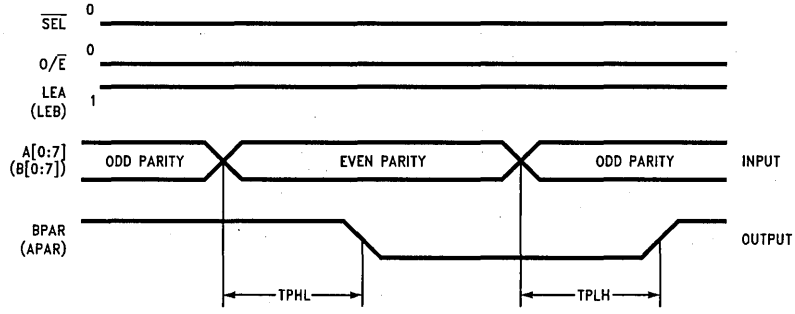
FIGURE 3



A_n → BPAR
(B_n → APAR)

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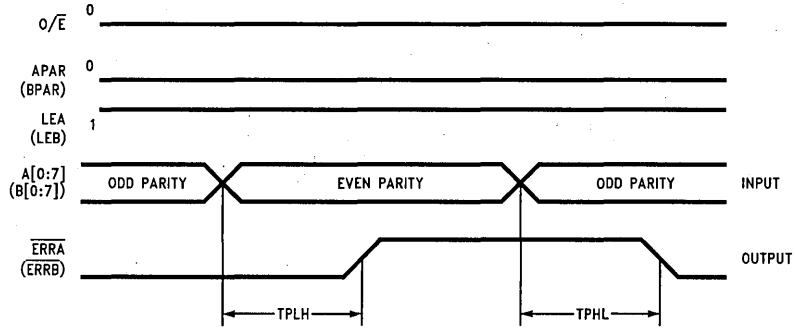
FIGURE 4



A_n → $\overline{ERRA}$
(B_n → $\overline{ERRB}$)

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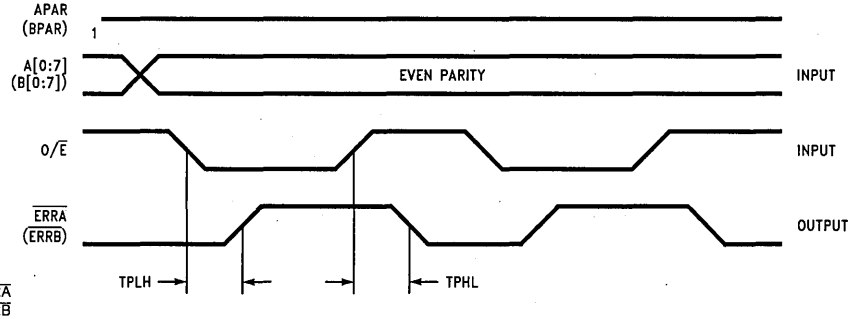
FIGURE 5



O/$\overline{E}$ → $\overline{ERRA}$
O/$\overline{E}$ → $\overline{ERRB}$

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FIGURE 6

AC Path (Continued)

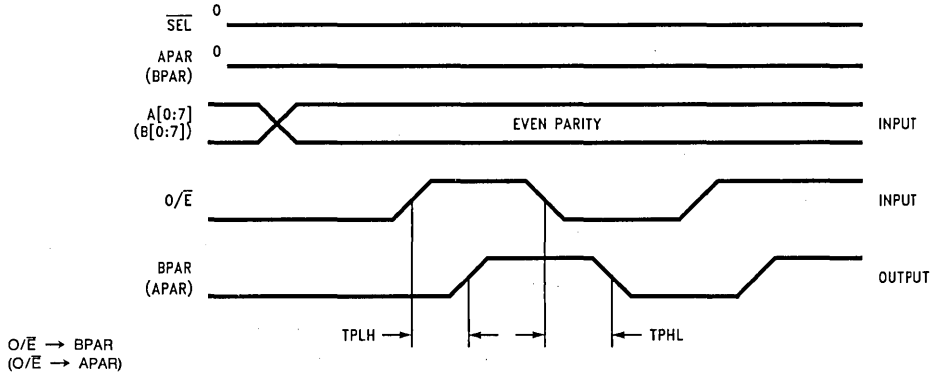

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FIGURE 7

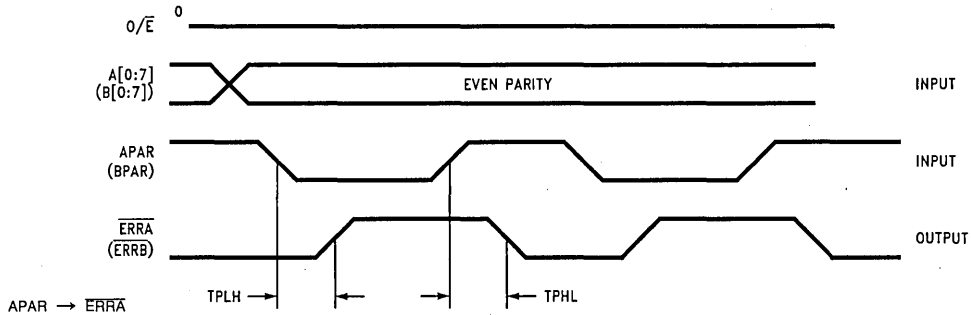

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FIGURE 8

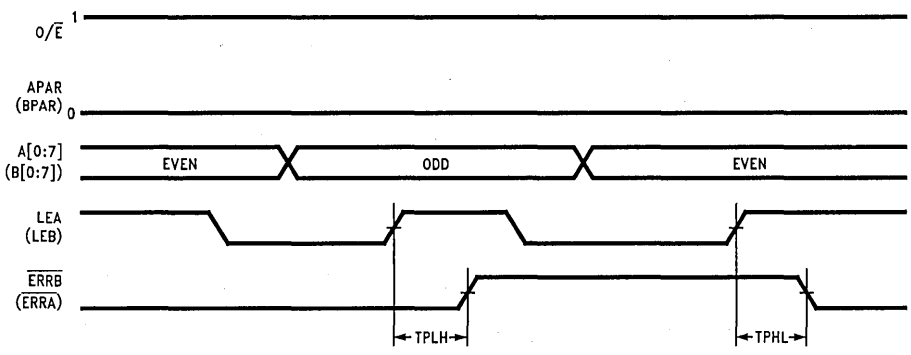

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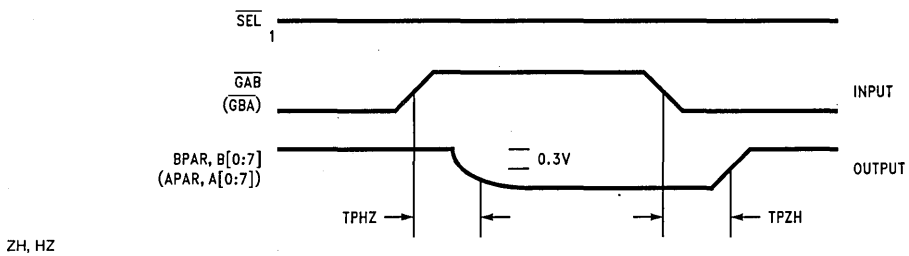
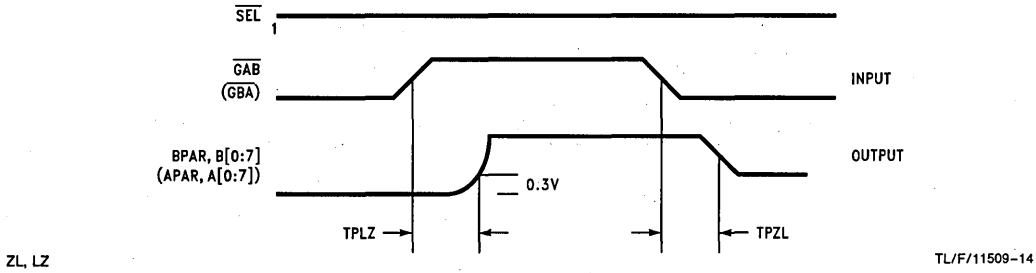
FIGURE 9



TL/F/11509–13

FIGURE 10

AC Path (Continued)



ZL, LZ

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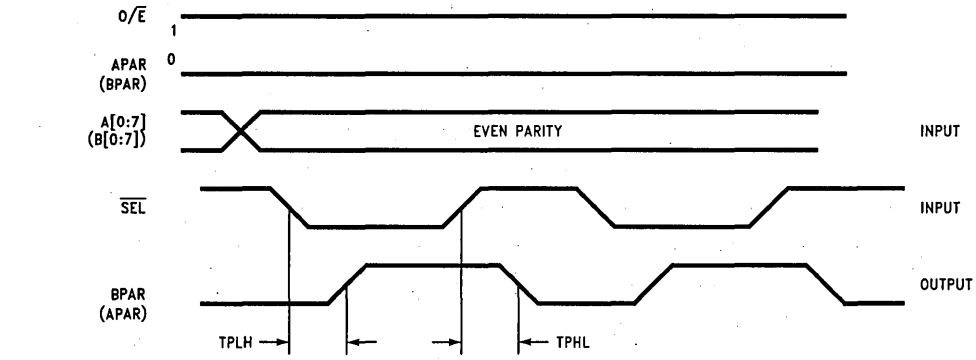
FIGURE 11



SEL → BPAR
(SEL → APAR)

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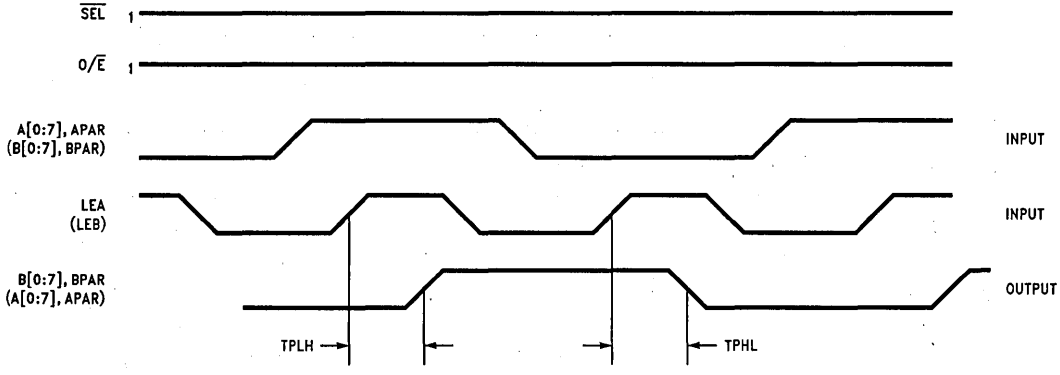
FIGURE 12



LEA → BPAR, B[0:7]
(LEB → APAR, A[0:7])

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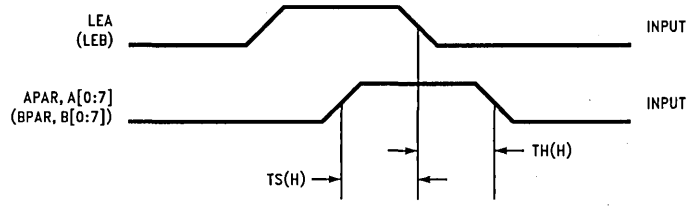
FIGURE 13

AC Path (Continued)



TS(H), TH(H)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

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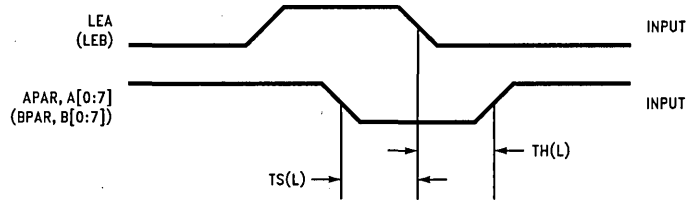
FIGURE 14



TS(L), TH(L)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

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FIGURE 15

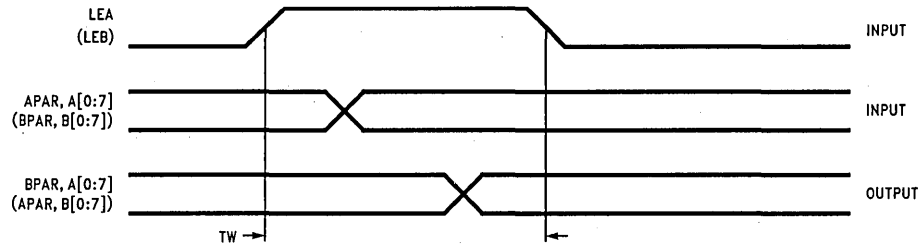

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FIGURE 16

National Semiconductor

PRELIMINARY

54ABT/74ABT2244C Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The 'ABT2244C is an octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

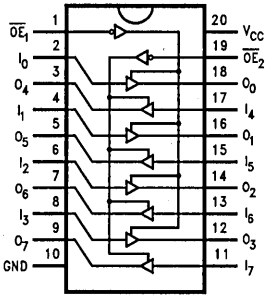
Features

- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneously switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code: See Section 11

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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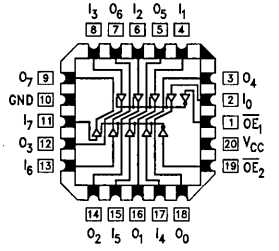
Pin Assignment for LCC



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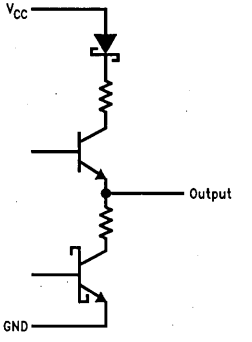
Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active Low)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Table

$\overline{OE}_1$	I_{0-3}	O_{0-3}	$\overline{OE}_2$	I_{4-7}	O_{4-7}
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Schematic of Each Output



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT2244C Min	ABT2244C Typ	ABT2244C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.8	V	Min	I_{OL} = 12 mA
		74ABT			0.8	V	Min	I_{OL} = 15 mA
I_{IH}	Input HIGH Current				5 5	μA	Max	V_{IN} = 2.7V V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5 −5	μA	Max	V_{IN} = 0.5V V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}n$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled Outputs TRI-STATE® Outputs TRI-STATE			2.5 2.5 50	mA mA μA	Max	V_I = V_{CC} − 2.1V Enable Input V_I = V_{CC} − 2.1V Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.1	mA/MHz	Max	Outputs Open $\overline{OE}n$ = GND (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions $C_L = 50\ pF, R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.5	0.8	V	5.0	$T_A = 25°C$ (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.5	−0.3		V	5.0	$T_A = 25°C$ (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.7	3.1		V	5.0	$T_A = 25°C$ (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	$T_A = 25°C$ (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	$T_A = 25°C$ (Note 2)

Note 1: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP package) : See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50\ pF$			54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 50\ pF$		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation	1.0	2.2	3.6			1.0	3.6	ns	2-3, 5
t_{PHL}	Delay Data to Outputs	1.0	2.9	4.1			1.0	4.1	ns	2-3, 5
t_{PZH}	Output Enable	1.5	3.7	6.0			1.5	6.0	ns	2-4
t_{PZL}	Time	1.5	4.3	6.5			1.5	6.5		
t_{PHZ}	Output Disable	1.0	3.5	6.0			1.0	6.0	ns	2-4
t_{PLZ}	Time	1.0	3.7	5.6			1.0	5.6		

Extended AC Electrical Characteristics (SOIC package) : See Section 2 for Waveforms

Symbol	Parameter	74ABT $-40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 50\ pF$, 8 Outputs Switching (Note 4)			74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 250\ pF$, 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 250\ pF$, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH}	Propagation Delay	1.5		6.0	1.5	6.0	2.5	8.5	ns	2-3, 5
t_{PHL}	Data to Outputs	1.5		6.0	1.5	10.0	2.5	11.0		
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.5	2.5	10.0	ns	2-4
t_{PZL}		1.5		7.0	2.5	11.0	2.5	12.5		
t_{PHZ}	Output Disable Time	1.0		5.6	(Note 7)		(Note 7)		ns	2-4
t_{PLZ}		1.0		5.6						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (SOIC package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.3	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.8	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	5.0	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	5.0	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	5.0	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

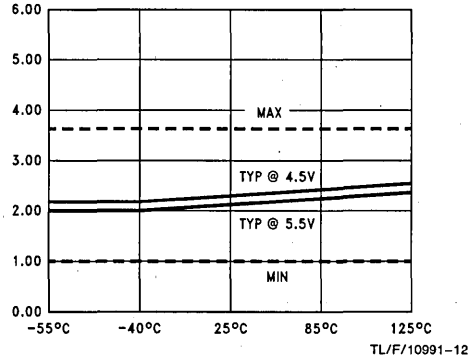
Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Typical Performance Characteristics

T_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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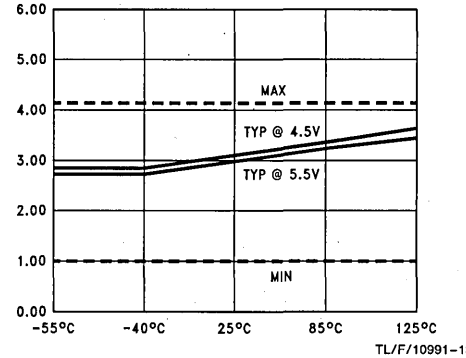
T_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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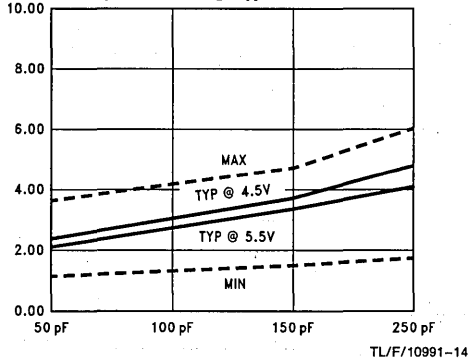
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

T_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



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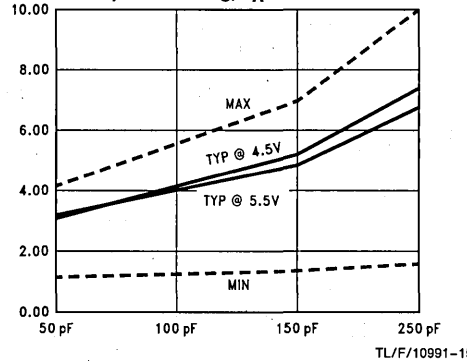
T_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



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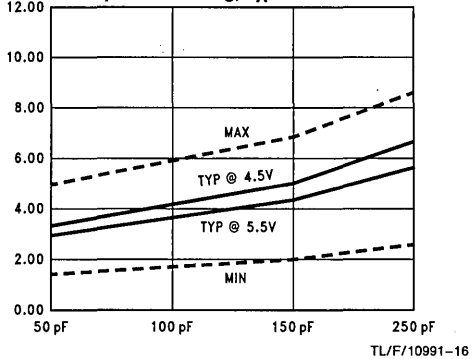
T_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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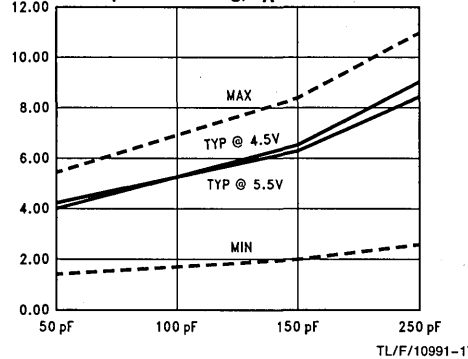
T_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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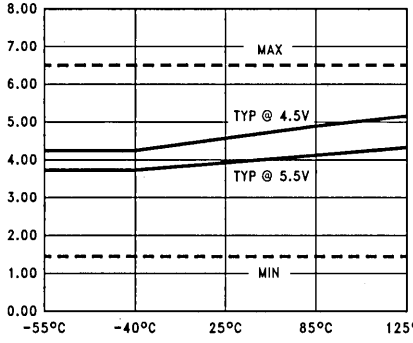
Typical Performance Characteristics (Continued)

T_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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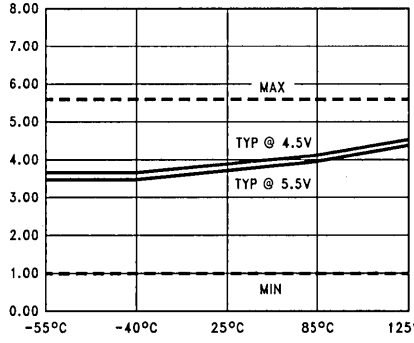
T_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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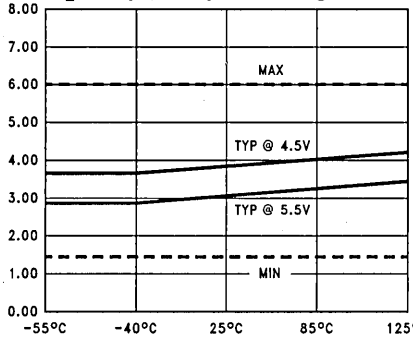
T_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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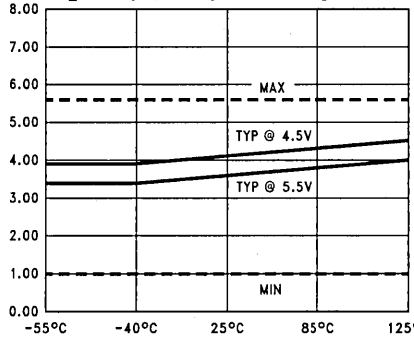
T_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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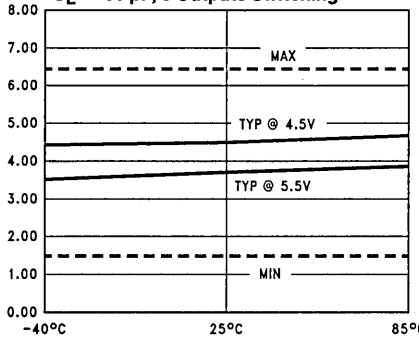
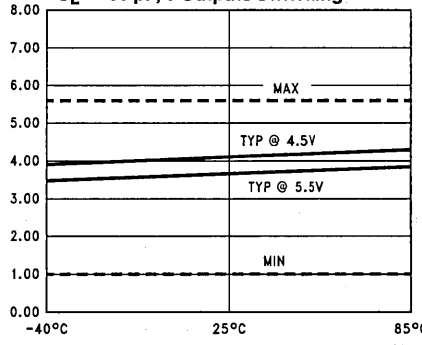
T_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



TL/F/10991–22

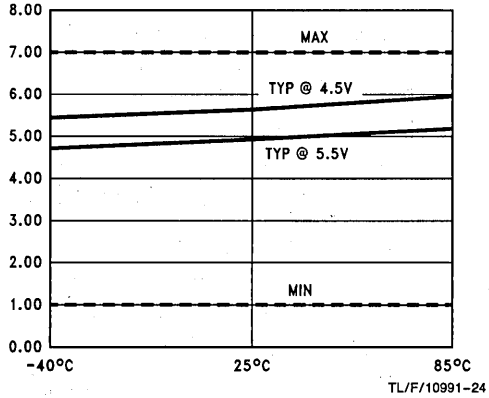
T_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



TL/F/10991–23

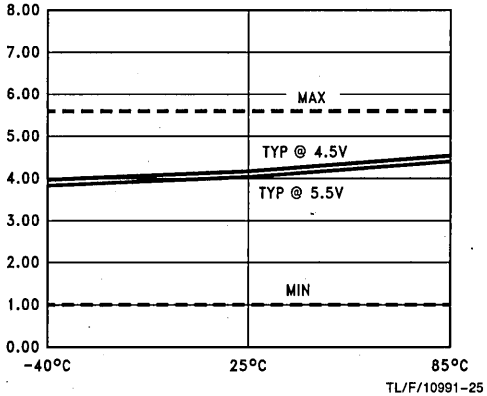
Typical Performance Characteristics (Continued)

T_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



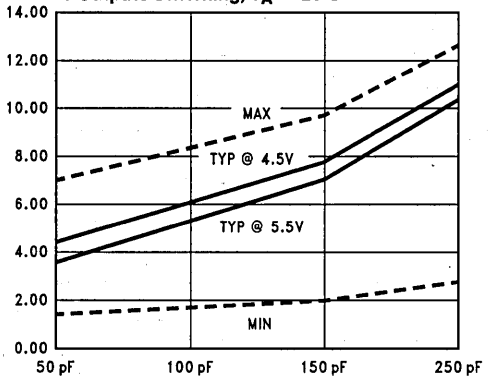
TL/F/10991–24

T_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



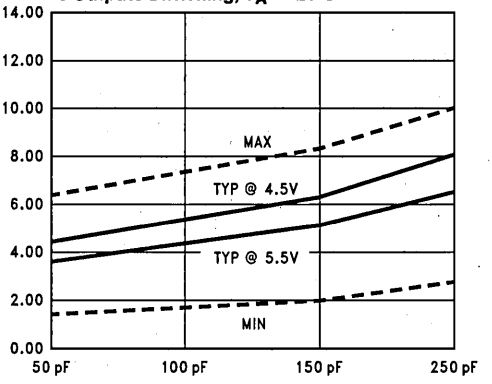
TL/F/10991–25

T_{PZL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



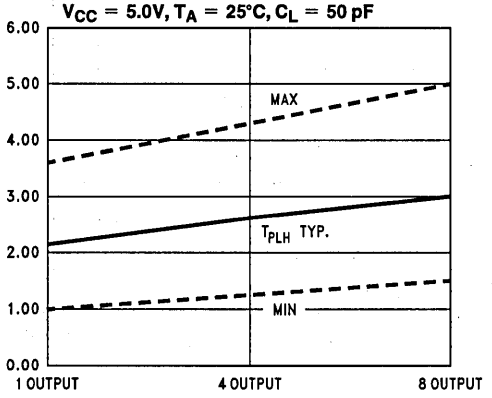
TL/F/10991–26

T_{PZH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



TL/F/10991–27

T_{PLH} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



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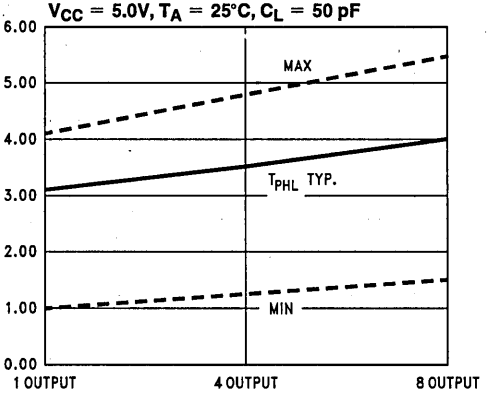
T_{PHL} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



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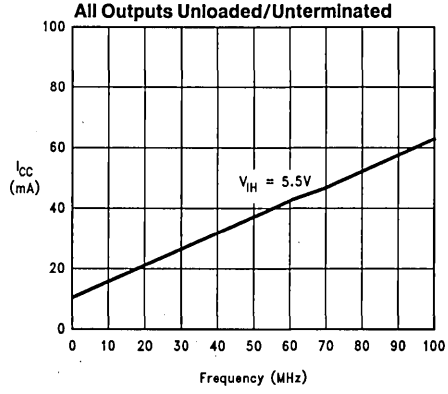
Typical Performance Characteristics (Continued)

I_{CC} vs Frequency, Average, T_A = 25°C, All Outputs Unloaded/Unterminated



TL/F/10991–30

National Semiconductor

54ABT/74ABT2541C Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The 'ABT2541C is an octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers. Functionally identical to the 'ABT541C.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

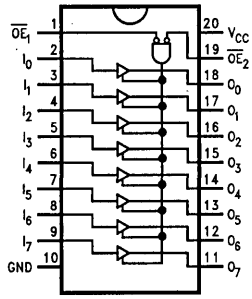
Features

- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneously switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code: See Section 11

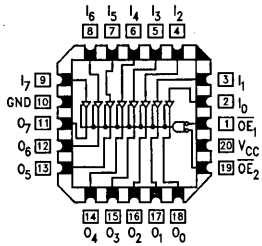
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/11502–1

Pin Assignment for LCC



TL/F/11502–2

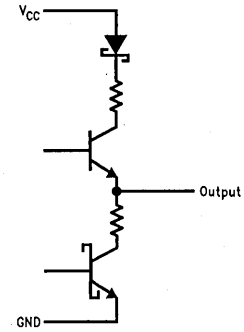
Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active Low)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	ABT541C
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level L = LOW Voltage Level
X = Immaterial Z = High Impedance

Schematic of Each Output



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT2541C Min	ABT2541C Typ	ABT2541C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.8	V	Min	I_{OL} = 12 mA
		74ABT			0.8			I_{OL} = 15 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}_n$ = V_{CC}; All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE®			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.1	mA/MHz	Max	Outputs Open $\overline{OE}_n$ = GND (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8 bit toggling, I_{CCD} < 0.8 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	0.8	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.5	−0.4		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.7	3.1		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.4		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP package) : See Section 2

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V-5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V-5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	1.0	2.3	3.6			1.0	3.6	ns	2-3, 5
t_{PHL}	Data to Outputs	1.0	3.3	4.1			1.0	4.1		2-3, 5
t_{PZH}	Output Enable Time	1.5	3.7	6.0			1.5	6.0	ns	2-4
t_{PZL}		1.5	4.3	6.5			1.5	6.5		
t_{PHZ}	Output Disable Time	1.0	3.5	6.0			1.0	6.0	ns	2-4
t_{PLZ}		1.0	3.7	5.6			1.0	5.6		

Extended AC Electrical Characteristics (SOIC package) : See Section 2

Symbol	Parameter	74ABT −40°C to +85°C, V_{CC} = 4.5V-5.5V, C_L = 50 pF, 8 Outputs Switching (Note 4)			74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V-5.5V, C_L = 250 pF, 1 Output Switching (Note 5)		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V-5.5V, C_L = 250 pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.5	ns	2-3, 5
t_{PHL}	Data to Outputs	1.5		5.5	1.5	10.0	2.5	11.0		
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.5	2.5	9.5	ns	2-4
t_{PZL}		1.5		7.0	2.5	11.0	2.5	12.5		
t_{PHZ}	Output Disable Time	1.0		6.0	(Note 7)		(Note 7)		ns	2-4
t_{PLZ}		1.0		6.0						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew (SOIC package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.3	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.8	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	5.0	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	5.0	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	5.0	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

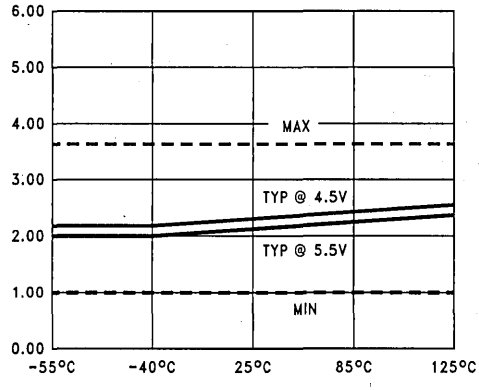
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz; per MIL-STD-883B, Method 3012.

t_{PLH} vs. Temperature (T_A)
$C_L = 50$ pF, 1 Output Switching



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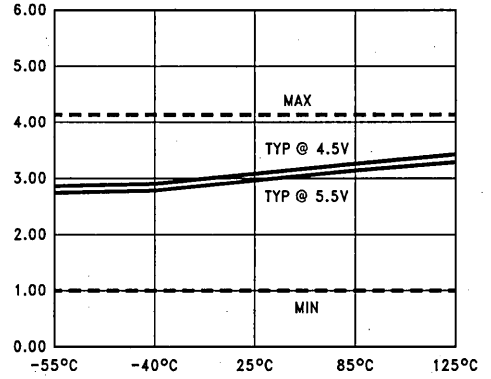
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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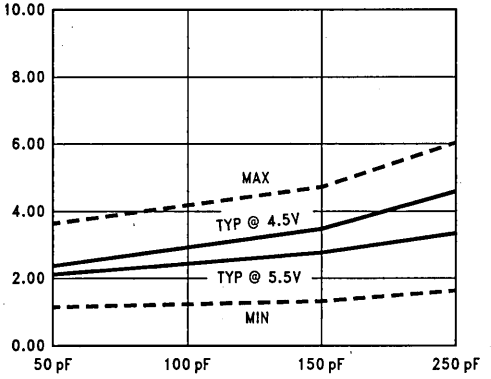
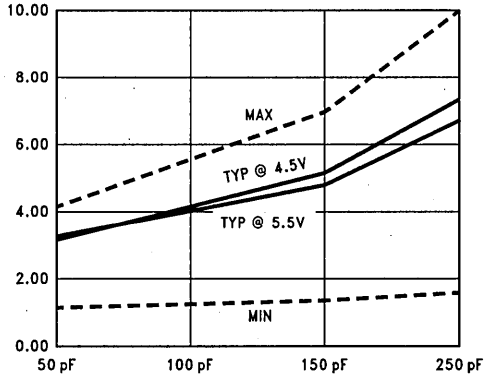
t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



TL/F/11502–14

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



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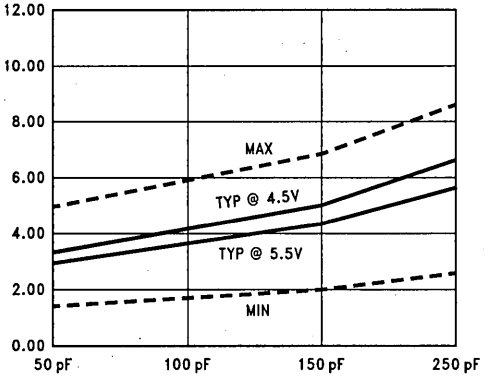
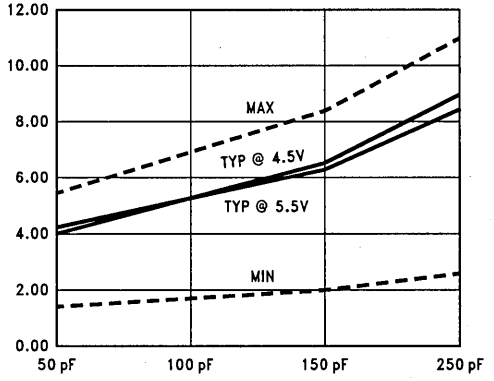
t_{PLH} vs Load Capacitance
8 Outputs Switching,
T_A = −40°C to 85°C



TL/F/11502–16

t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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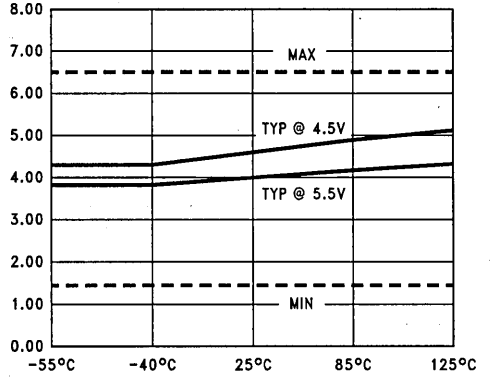
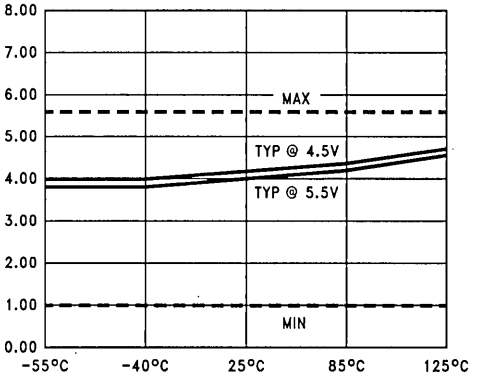
t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



TL/F/11502–18

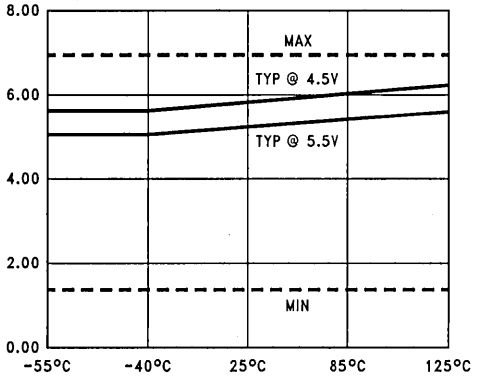
Dashed lines represent design characteristics, for specified guarantees refer to AC Characteristics Table.

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



TL/F/11502–19

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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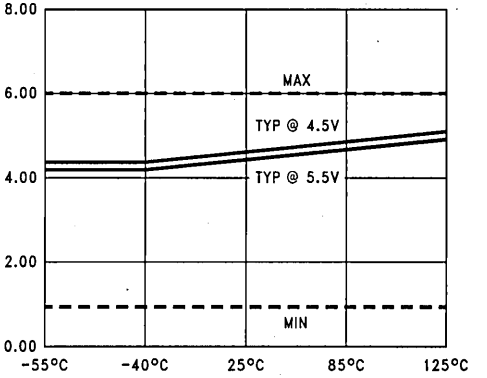
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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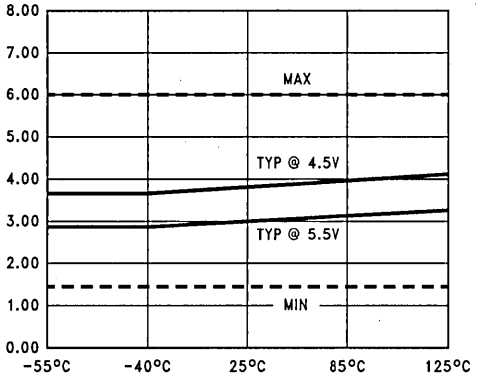
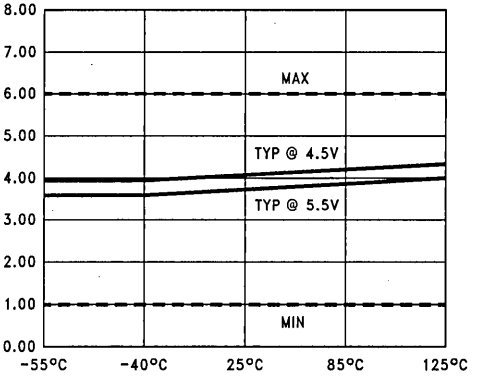
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



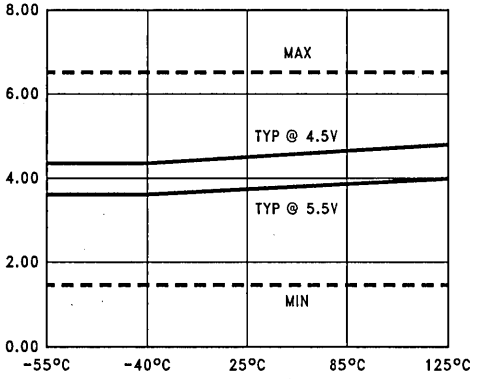
TL/F/11502–22

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



TL/F/11502–23

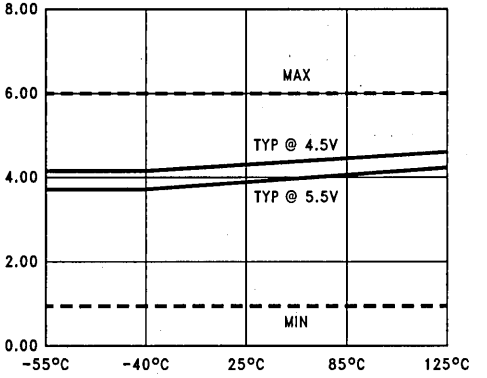
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



TL/F/11502–24

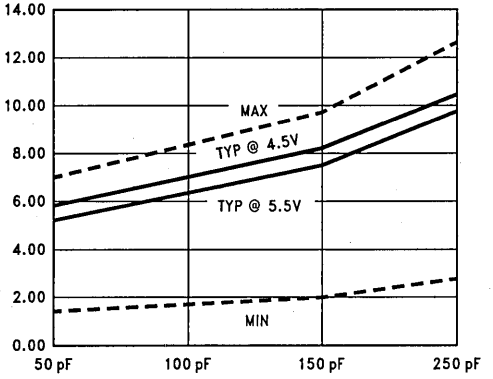
Dashed lines represent design characteristics, for specified guarantees refer to AC Characteristics Table.

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



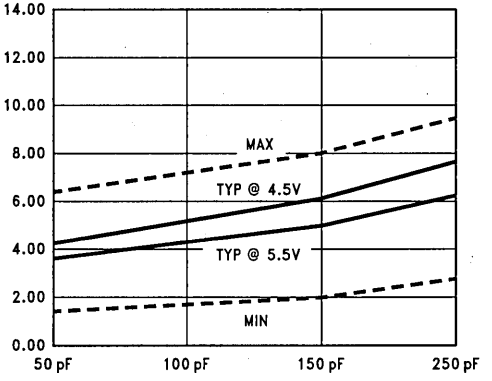
TL/F/11502–25

t_{PZL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



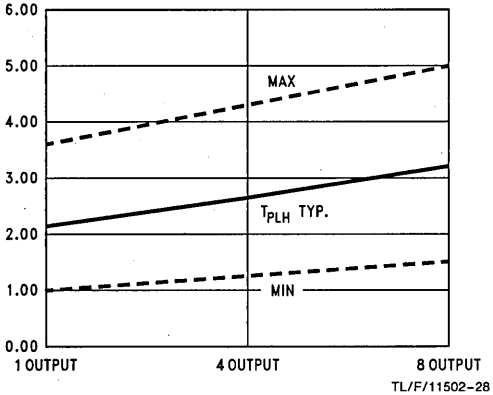
TL/F/11502–26

t_{PZH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



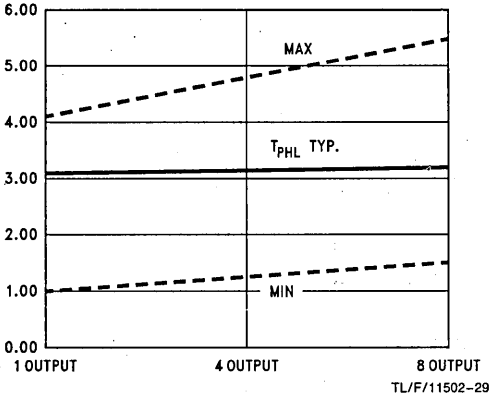
TL/F/11502–27

t_{PLH} vs Number Outputs Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



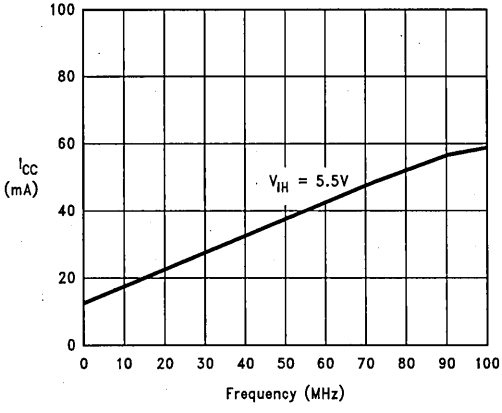
TL/F/11502–28

t_{PHL} vs Number Outputs Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



TL/F/11502–29

I_{CC} vs Frequency, Average, T_A = 25°C
All outputs unloaded/unterminated



TL/F/11502–30

Dashed lines represent design characteristics, for specified guarantees refer to AC Characteristics Table.

National Semiconductor

54ABT/74ABT2952C
8-Bit Registered Transceiver

General Description

The 'ABT2952C is an 8-bit registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The output pins are guaranteed to source 32 mA (24 mA mil.) and to sink 64 mA (48 mA mil).

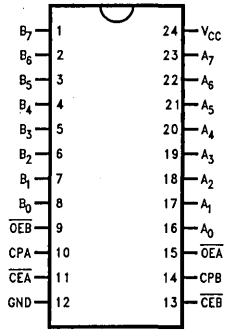
Features

- Separate clock, clock enable and TRI-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code: See Section 11

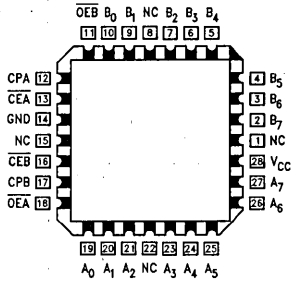
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/10969–3

Pin Assignment for LCC



TL/F/10969–4

Pin Descriptions

Pin Names	Description
A_0–A_7	A-Register Inputs/B-Register TRI-STATE Outputs
B_0–B_7	B-Register Inputs/A-Register TRI-STATE Outputs
$\overline{OEA}$	Output Enable A-Register
CPA	A-Register Clock
$\overline{CEA}$	A-Register Clock Enable
$\overline{OEB}$	Output Enable B-Register
CPB	B-Register Clock
$\overline{CEB}$	B-Register Clock Enable

Pin Descriptions (Continued)

Output Control

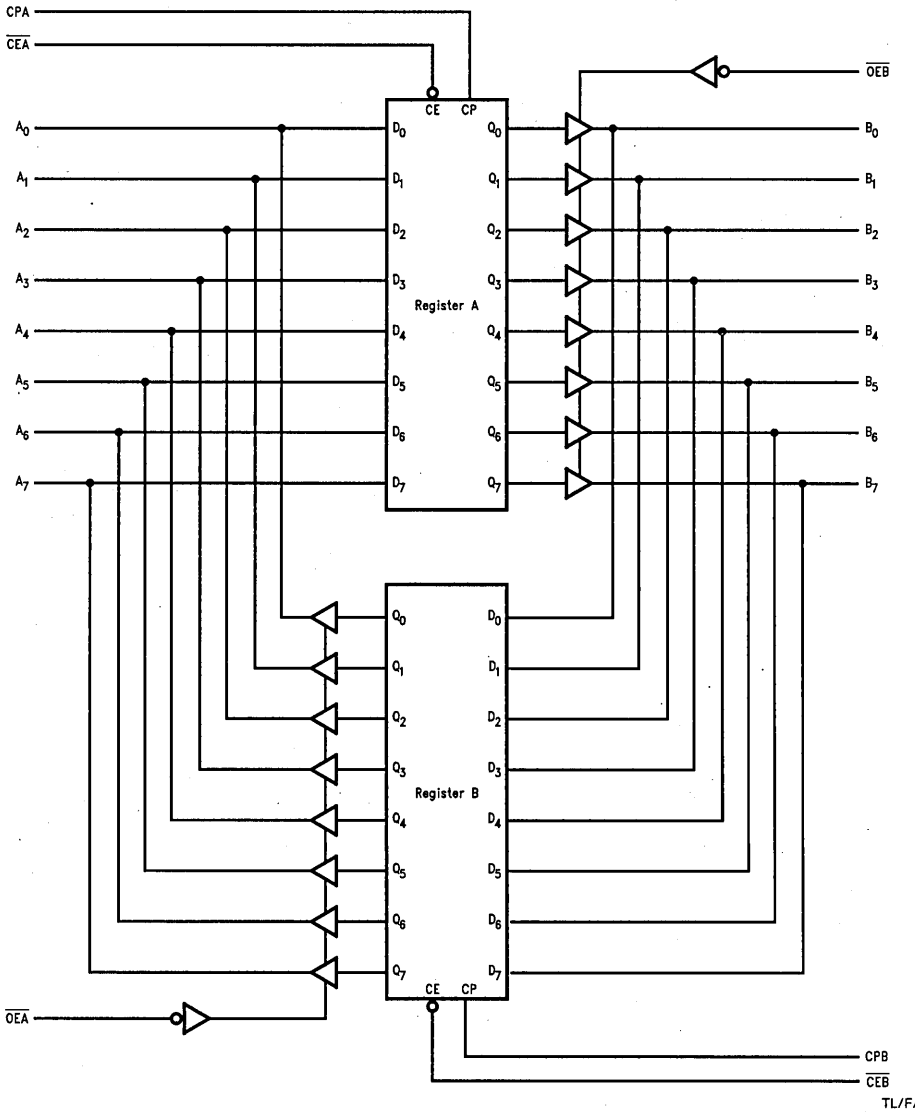
$\overline{OE}$	Internal Q	Output 'ABT2952C	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↗	L	H	

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT2952C Min	ABT2952C Typ	ABT2952C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA (A_n, B_n)
	54ABT	2.0					I_{OH} = −24 mA (A_n, B_n)
	74ABT	2.0					I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage 54ABT			0.55	V	Min	I_{OL} = 48 mA (A_n, B_n)
	74ABT			0.55			I_{OL} = 64 mA (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V or V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V or 0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			250	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	μA	Max	Outputs TRI-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V; All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open $\overline{OEA}$ or $\overline{OEB}$ = GND, Non-I/O = GND or V_{CC} One Bit toggling, 50% duty cycle (Note 1)

Note 1: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	0.8	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−1.0		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms (SOIC and SSOP Package)

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	200					200		MHz	
t_{PLH} t_{PHL}	Propagation Delay CPA or CPB to A_n or B_n	1.5 1.5	3.4 3.6	5.3 5.3			1.5 1.5	5.3 5.3	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5 1.5	3.2 3.5	5.5 5.5			1.5 1.5	5.5 5.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5 1.5	3.6 3.2	6.0 6.0			1.5 1.5	6.0 6.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF		54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n to CPA or CPB	2.5 2.5				2.5 2.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n to CPA or CPB	1.5 1.5				1.5 1.5		ns	2-6
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	2.5 2.5				2.5 2.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	1.5 1.5				1.5 1.5		ns	2-6
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0				3.0 3.0		ns	2-3

Extended AC Electrical Characteristics: See Section 2 (SOIC package)

Symbol	Parameter	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 5)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Progagation Delay	1.5	6.0	2.0	8.0	2.5	10.5	ns	2-4
t_{PHL}	CPA or CPB to A_n or B_n	1.5	6.0	2.0	8.0	2.5	10.5		
t_{PZH}	Output Enable Time	1.5	6.0	2.0	8.0	2.5	11.5	ns	2-4
t_{PZL}	$\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5	6.0	2.0	8.0	2.5	11.5		
t_{PHZ}	Output Disable Time	1.5	6.0	(Note 7)		(Note 7)		ns	2-4
t_{PZL}	$\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5	6.0						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in plce of the 50 pF load capacitors in the standard AC load. This specificaiton pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (SOIC package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	1.5	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	2.0	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	4.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.1	4.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	5.0	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

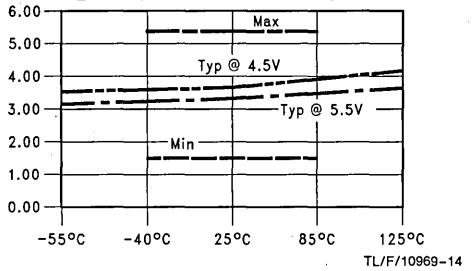
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0V (Non I/O Pins)
$C_{I/O}$ (Note 1)	Output Capacitance	11	pF	V_{CC} = 5.0V (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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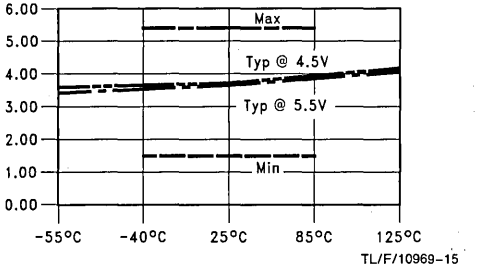
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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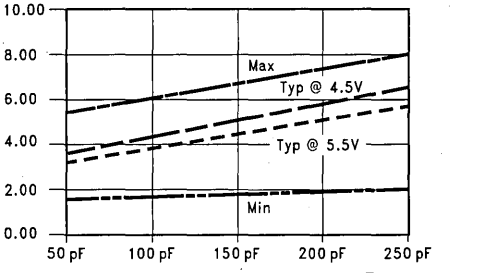
t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



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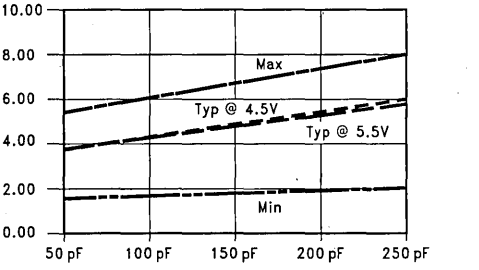
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



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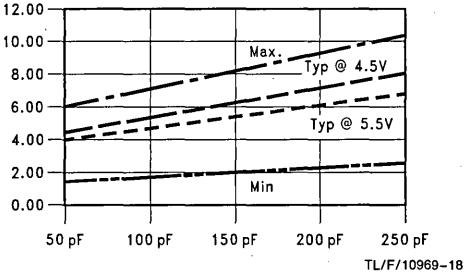
t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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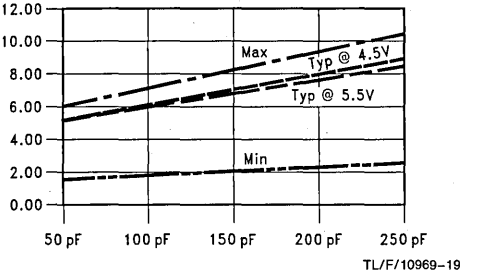
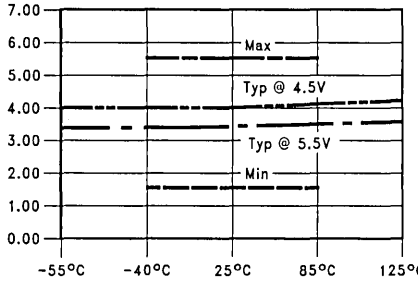
t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



TL/F/10969–19

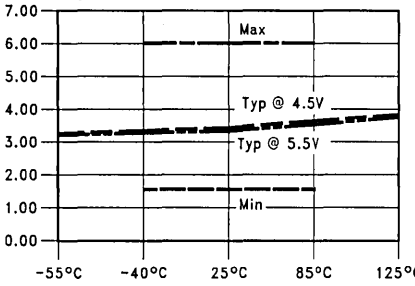
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



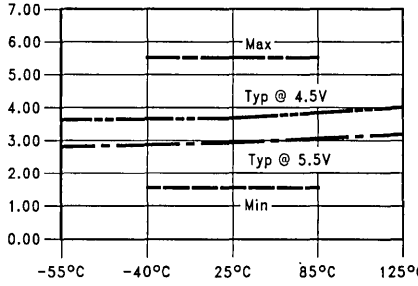
TL/F/10969-20

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



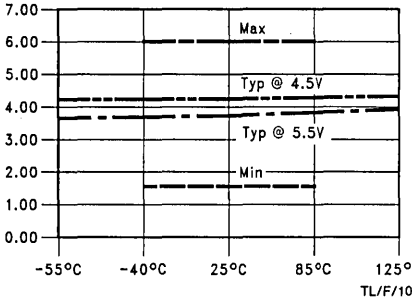
TL/F/10969-21

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



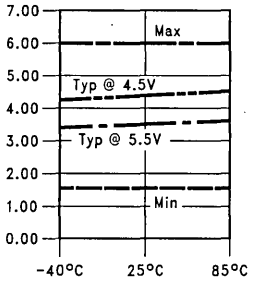
TL/F/10969-22

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



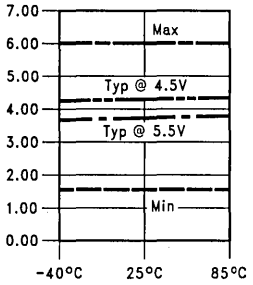
TL/F/10969-23

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



TL/F/10969-24

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching

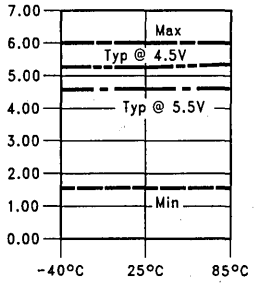


TL/F/10969-25

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

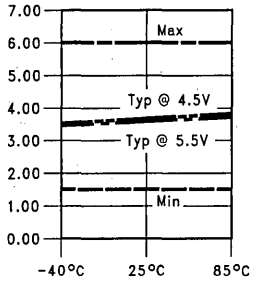
5

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



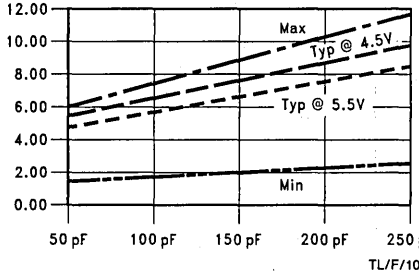
TL/F/10969–26

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



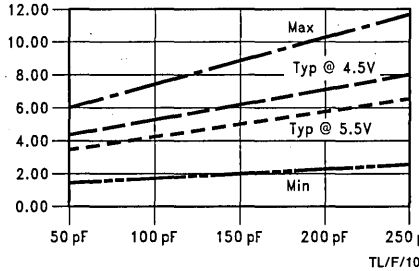
TL/F/10969–27

t_{PZL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



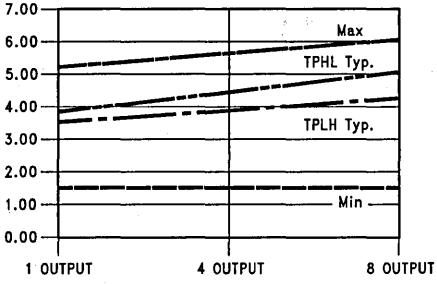
TL/F/10969–28

t_{PZH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



TL/F/10969–29

t_{PLH} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



TL/F/10969–30

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

National Semiconductor

54ABT/74ABT16244C 16-Bit Buffer/ Line Driver with TRI-STATE® Outputs

General Description

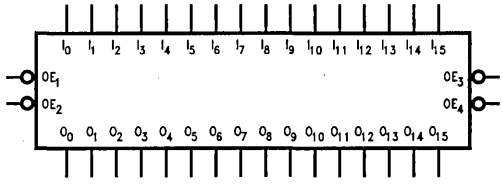
The 'ABT16244C contains sixteen non-inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/ receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

Features

- Separate control logic for each nibble
- 16-bit version of the 'ABT244C
- Outputs sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Ordering Code: See Section 11

Logic Symbol



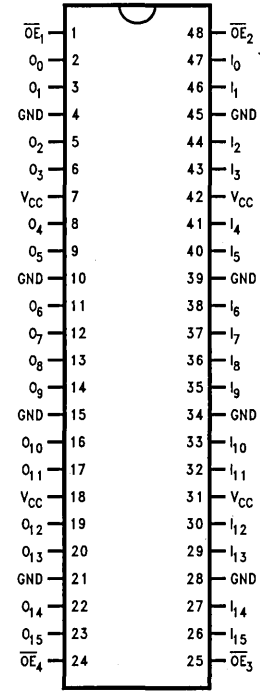
TL/F/10985–1

Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

Connection Diagram

SSOP



TL/F/10985–2

5

Functional Description

The 'ABT16244C contains sixteen non-inverting buffers with TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

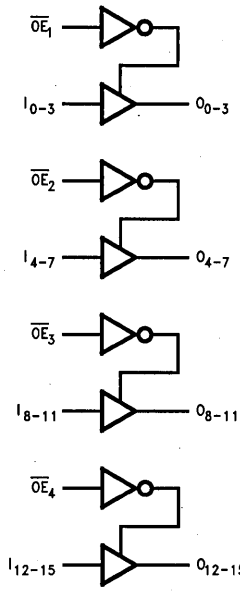
Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT16244C Min	ABT16244C Typ	ABT16244C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V All Other Pins GND
I_{CCH}	Power Supply Current				100	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				100	μA	Max	$\overline{OE}_n$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 1)	No Load			0.1	mA/ MHz	Max	Outputs Open, $\overline{OE}_n$ = GND One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed but not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT16244C			Units	V_{CC}	Conditions C_L = 50 pF R_L = 500Ω
		Min	Typ	Max			
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.4	0.7	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.3	−1.0		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.7	3.0		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.4		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C V_{CC} = +5V C_L = 50 pF			54ABT T_A = −55°C to +125°C V_{CC} = 4.5V-5.5V C_L = 50 pF		74ABT T_A = −40°C to +85°C V_{CC} = 4.5V-5.5V C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation	1.0	2.3	3.9			1.0	3.9	ns	2-3, 5
t_{PHL}	Delay Data to Outputs	1.0	2.7	3.9			1.0	3.9		2-3, 5
t_{PZH}	Output Enable	1.5	3.5	6.3			1.5	6.3	ns	2-4
t_{PZL}	Time	1.5	3.5	6.3			1.5	6.3		
t_{PHZ}	Output Disable	1.0	4.2	6.7			1.0	6.7	ns	2-4
t_{PLZ}	Time	1.0	3.2	6.7			1.0	6.7		

Extended AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ABT −40°C to +85°C V_{CC} = 4.5V-5.5V C_L = 50 pF 16 Outputs Switching (Note 4)			74ABT T_A = −40°C to +85°C V_{CC} = 4.5V-5.5V C_L = 250 pF 1 Output Switching (Note 5)		74ABT T_A = −40°C to +85°C V_{CC} = 4.5V-5.5V C_L = 250 pF 16 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.0	ns	2-3, 5
t_{PHL}	Data to Outputs	1.5		5.3	1.5	6.0	2.5	8.0		
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.8	2.5	9.5	ns	2-4
t_{PZL}		1.5		6.5	2.5	7.8	2.5	8.5		
t_{PHZ}	Output Disable Time	1.0		6.7	(Note 7)		(Note 7)		ns	2-4
t_{PLZ}		1.0		6.7						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 16 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 16 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	1.5	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.5	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	1.5	1.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	1.7	2.0	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	2.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guarantood but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

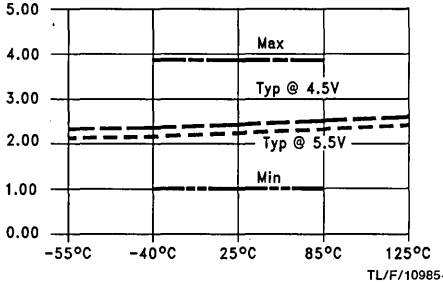
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 5.0V$
C_{OUT} (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz; per MIL STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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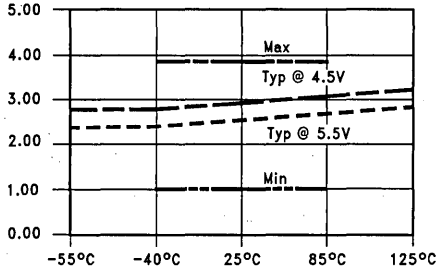
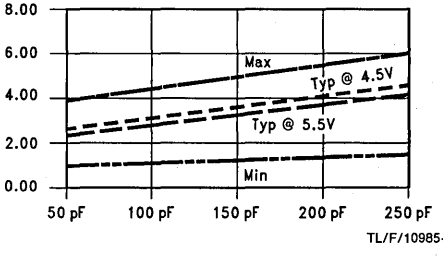
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



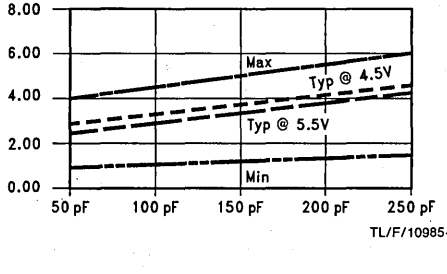
TL/F/10985–13

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



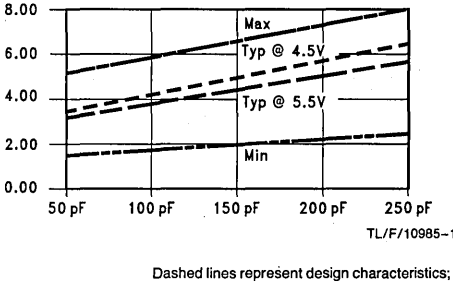
TL/F/10985–14

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



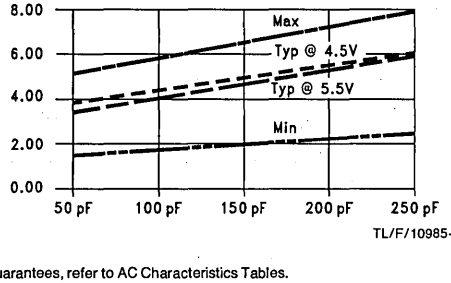
TL/F/10985–15

t_{PLH} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



TL/F/10985–16

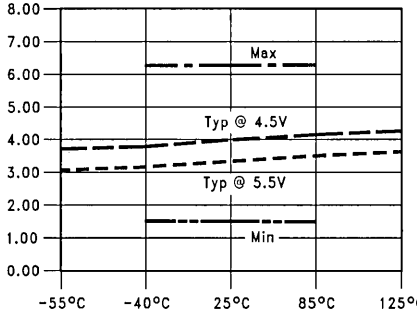
t_{PHL} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



TL/F/10985–17

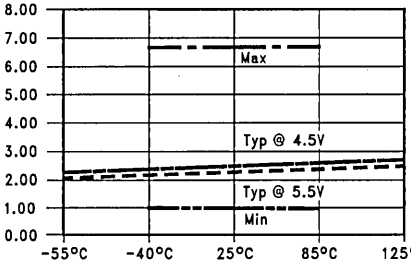
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



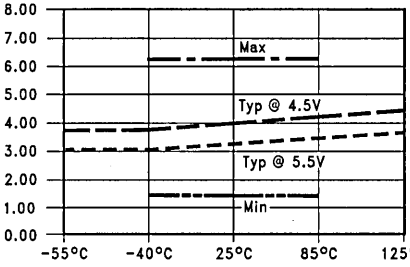
TL/F/10985–18

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



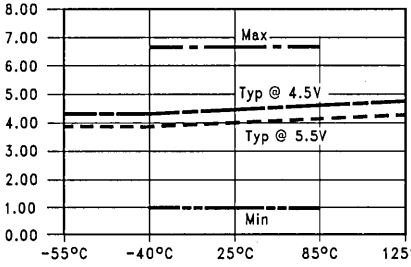
TL/F/10985–19

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



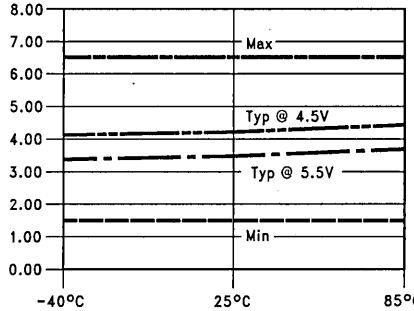
TL/F/10985–20

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



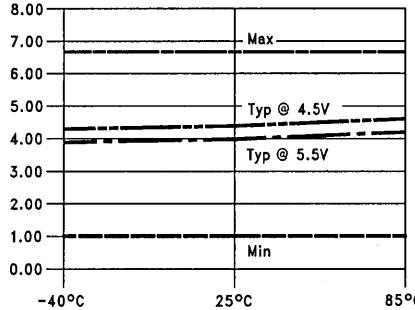
TL/F/10985–21

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



TL/F/10985–22

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching

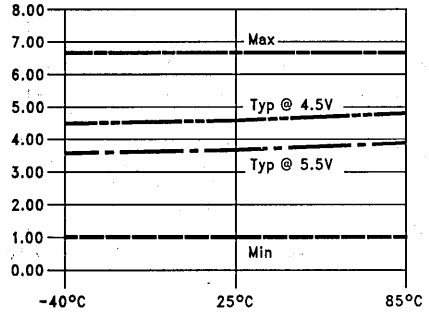


TL/F/10985–23

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

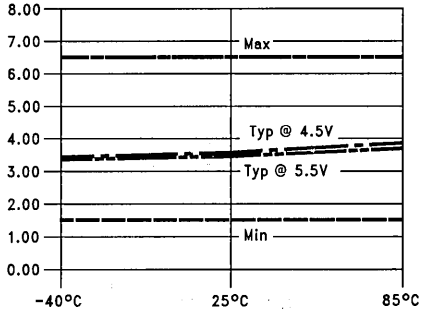
5

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



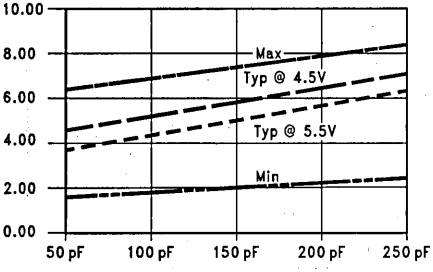
TL/F/10985-24

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



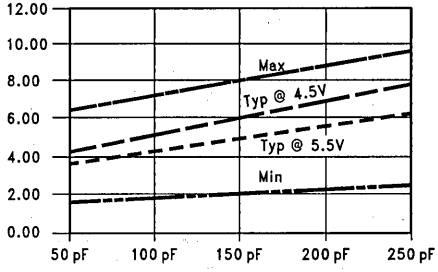
TL/F/10985-25

t_{PZL} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



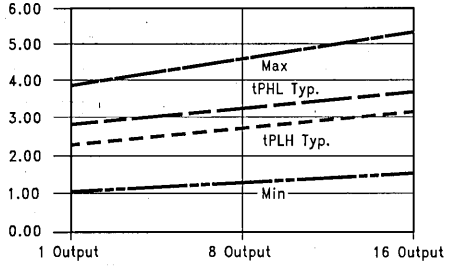
TL/F/10985-26

t_{PZH} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



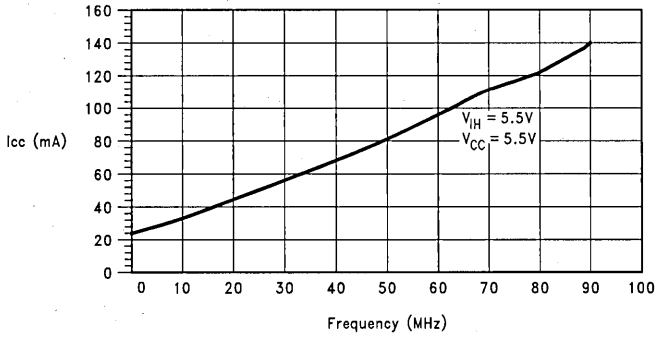
TL/F/10985-27

t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



TL/F/10985-28

I_{CC} vs Frequency Average,
T_A = 25°C, V_{CC} = 5.5V



TL/F/10985-29

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

National Semiconductor

54ABT/74ABT16245C
16-Bit Transceiver with TRI-STATE® Outputs

General Description

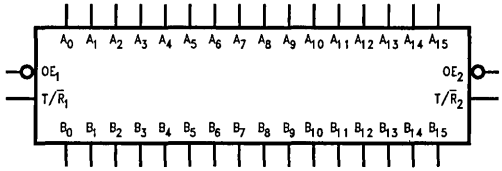
The 'ABT16245C contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

Features

- Bidirectional non-inverting buffers
- Separate control logic for each byte
- 16-bit version of the 'ABT245C
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Ordering Code: See Section 11

Logic Symbol

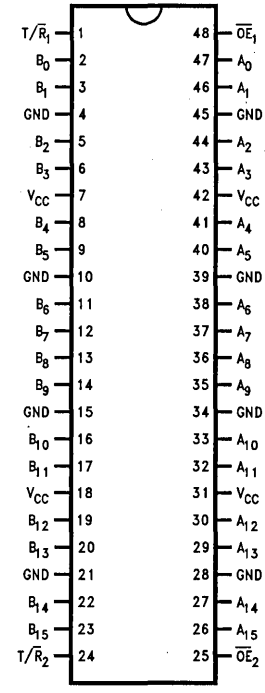


TL/F/10986–1

Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/Outputs
B_0–B_{15}	Side B Inputs/Outputs

Connection Diagram



TL/F/10986–2

Functional Description

The 'ABT16245C contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

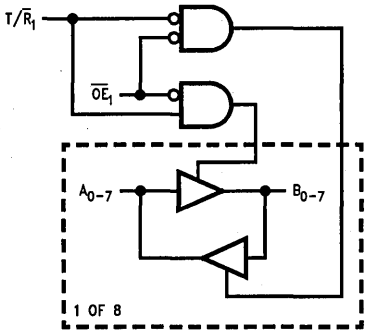
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

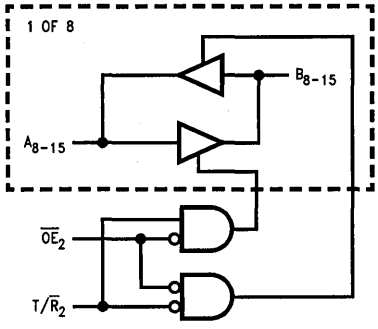
Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams



TL/F/10986–3



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT16245C Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA ($\overline{OE}_n$, T/$\overline{R}_n$)
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.4			V	Min	I_{OH} = −3 mA (A_n, B_n)
		54ABT	2.0			V	Min	I_{OH} = −12 mA (A_n, B_n)
		74ABT	2.0			V	Min	I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	54ABT 74ABT			0.55 0.55	V	Min	I_{OL} = 48 mA (A_n, B_n) I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input HIGH Current				5 5	μA	Max	V_{IN} = 2.7V ($\overline{OE}_n$, T/$\overline{R}_n$) V_{IN} = V_{CC} ($\overline{OE}_n$, T/$\overline{R}_n$)
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V ($\overline{OE}_n$, T/$\overline{R}_n$)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−5 −5	μA	Max	V_{IN} = 0.5V ($\overline{OE}_n$, T/$\overline{R}_n$) V_{IN} = 0.0V ($\overline{OE}_n$, T/$\overline{R}_n$)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA ($\overline{OE}_n$, T/$\overline{R}_n$) All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V (A_n, B_n)
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.50V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current				100	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				100	μA	Max	$\overline{OE}_n$ = V_{CC}, T/$\overline{R}_n$ = GND or V_{CC} All others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled Outputs TRI-STATE Outputs TRI-STATE			2.5 2.5 50	mA mA μA	Max	V_I = V_{CC} − 2.1V $\overline{OE}_n$, T/$\overline{R}_n$ V_I = V_{CC} − 2.1V Data Input V_I = V_{CC} − 2.1V All others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load			0.1	mA/MHz	Max	Outputs Open $\overline{OE}_n$ = GND, T/$\overline{R}_n$ = GND or V_{CC} One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed, but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF; R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.5	0.9	V	5.0	T_A = 25°C (Note 2)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.4	−1.0		V	5.0	T_A = 25°C (Note 2)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 4)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.4		V	5.0	T_A = 25°C (Note 3)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 3)

Note 2: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 3: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 4: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation	1.0	2.4	3.9			1.0	3.9	ns	2-3, 5
t_{PHL}	Delay Data to Outputs	1.0	2.8	3.9			1.0	3.9	ns	2-3, 5
t_{PZH}	Output Enable	1.5	3.6	6.3			1.5	6.3	ns	2-4
t_{PZL}	Time	1.5	3.7	6.3			1.5	6.3	ns	2-4
t_{PHZ}	Output Disable	1.0	4.6	6.9			1.0	6.9	ns	2-4
t_{PLZ}	Time	1.0	3.7	6.9			1.0	6.9	ns	2-4

Extended AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF, 16 Outputs Switching (Note 4)			74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 1 Output Switching (Note 5)		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 16 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.0	ns	2-3, 5
t_{PHL}	Data to Outputs	1.5		5.3	1.5	6.0	2.5	8.0	ns	2-3, 5
t_{PZH}	Output Enable Time	1.5		6.5	2.5	8.2	2.5	10.0	ns	2-4
t_{PZL}		1.5		6.5	2.5	8.2	2.5	9.0	ns	2-4
t_{PHZ}	Output Disable	1.0		6.9	(Note 7)		(Note 7)		ns	2-4
t_{PLZ}	Time	1.0		6.9					ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: TRI-STATE delay are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 16 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 16 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	1.5	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.3	1.5	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	1.5	2.0	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	1.7	2.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	3.0	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

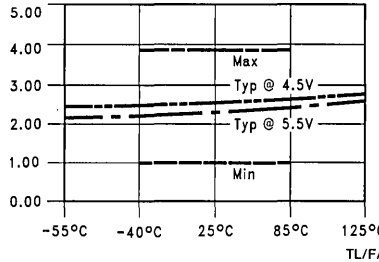
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0.0V$ ($\overline{OE}_n$, $T/\overline{R}_n$)
$C_{I/O}$ (Note 1)	Output Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n)

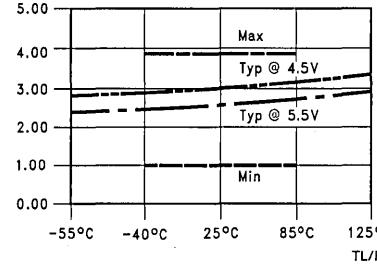
Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
$C_L = 50$ pF, 1 Output Switching



TL/F/10986–13

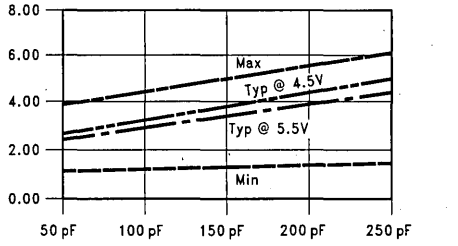
t_{PHL} vs Temperature (T_A)
$C_L = 50$ pF, 1 Output Switching



TL/F/10986–14

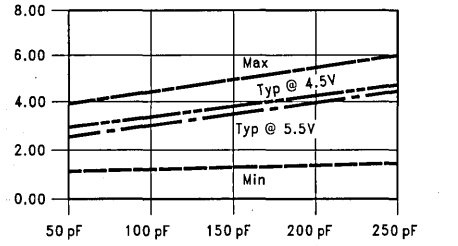
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



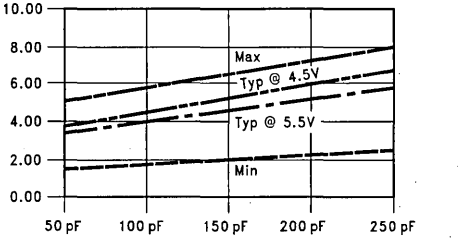
TL/F/10986–15

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



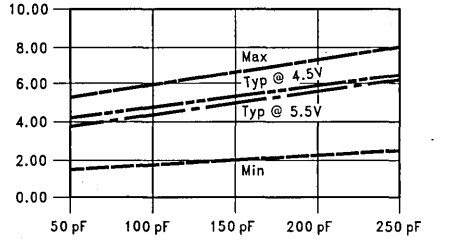
TL/F/10986–16

t_{PLH} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



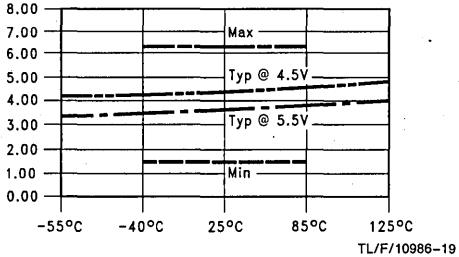
TL/F/10986–17

t_{PHL} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



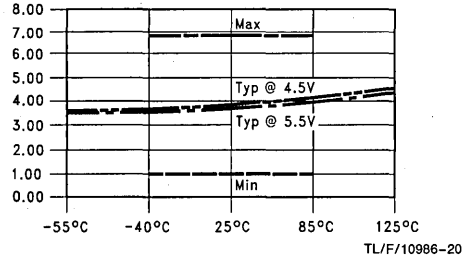
TL/F/10986–18

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



TL/F/10986–19

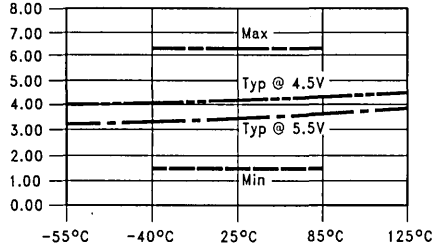
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



TL/F/10986–20

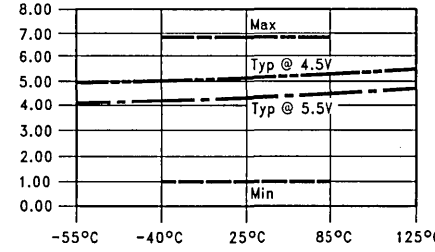
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



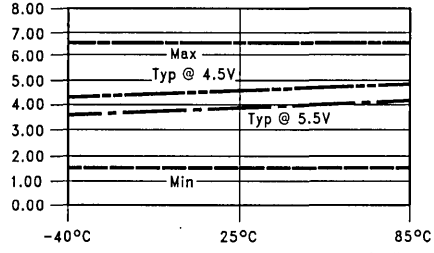
TL/F/10986-21

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



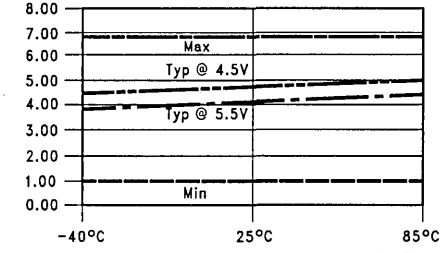
TL/F/10986-22

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



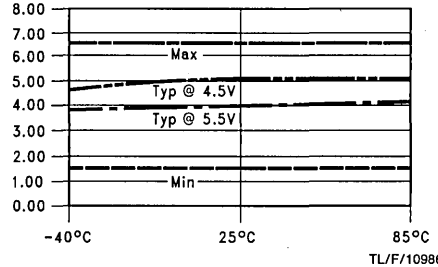
TL/F/10986-23

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



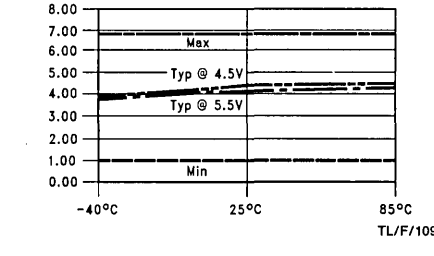
TL/F/10986-24

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



TL/F/10986-25

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching

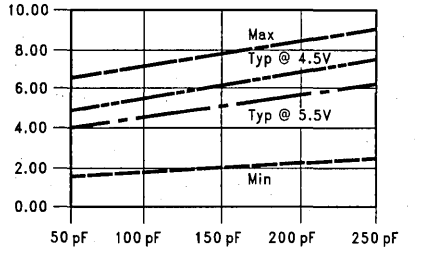


TL/F/10986-26

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

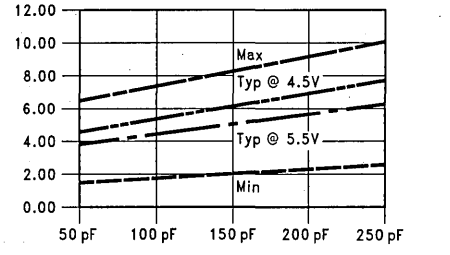
5

t_{PZL} vs Load Capacitance
16 Outputs Switching T_A = 25°C



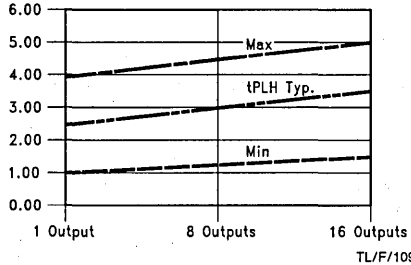
TL/F/10986–27

t_{PZH} vs Load Capacitance
16 Outputs Switching T_A = 25°C



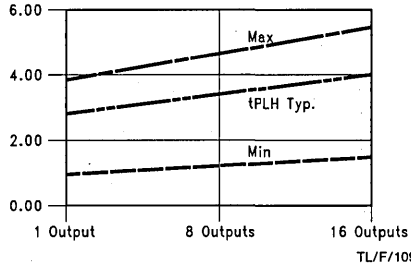
TL/F/10986–28

t_{PLH} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



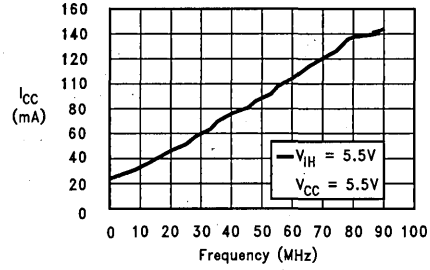
TL/F/10986–29

t_{PHL} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



TL/F/10986–30

I_{CC} vs Frequency
Average, T_A = 25°C, V_{CC} = 5.5V
All Outputs Unloaded/Unterminated;
16 Outputs Switching In-Phase at 50% Duty Cycle



TL/F/10986–31

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

National Semiconductor

PRELIMINARY

54ABT/74ABT16500C 18-Bit Universal Bus Transceivers with TRI-STATE® Outputs

General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$ inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CLKAB}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CLKAB}$. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. The output enables are complementary (OEAB is active high and $\overline{OEBA}$ is active low).

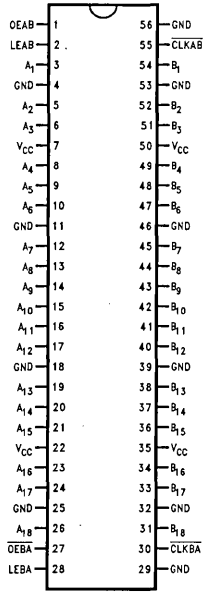
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Features

- Combines D-Type latches and D-Type flip-flops for operation in transparent, latched, or clocked mode
- Flow-through architecture optimizes PCB layout
- Guaranteed latch-up
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Ordering Code: See Section 11

Connection Diagram



TL/F/11581–1

Function Table†

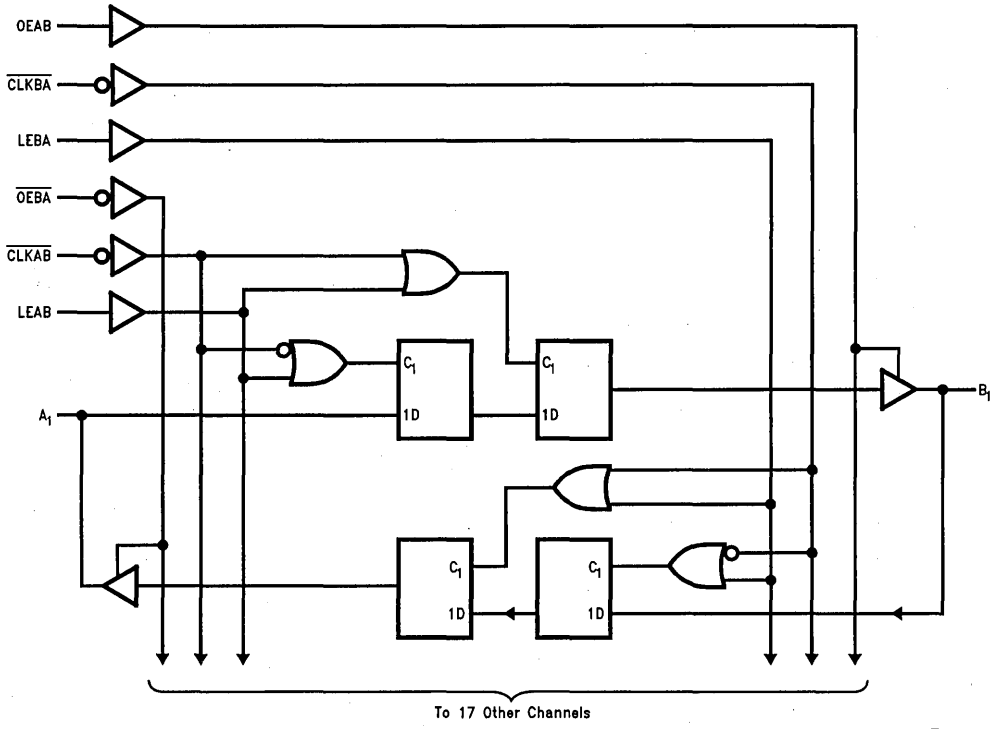
Inputs				Output
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

Logic Diagram



TL/F/11581–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
Output Clamp Current	−50 mA
Max. Power Dissipation @ T_A = 55°C (in still air)	1W
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT16500C Min	ABT16500C Typ	ABT16500C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA; V_{CC} = 4.5V
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA; V_{CC} = 4.5V
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA; V_{CC} = 4.5V
		74ABT			0.55			I_{OL} = 64 mA; V_{CC} = 4.5V
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				100	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				68	μA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				100	μA	Max	$\overline{OE}_n$ = V_{CC}, All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input				2.5	mA	Max	V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 1)	No Load			0.18	mA/MHz	Max	Outputs Open $\overline{OE}_n$ = GND One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed, but not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF; R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}			0.8	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.0			V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5			V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0			V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage			0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	150					150		MHz	
t_{PLH}	Propagation Delay A or B to B or A	1.1		3.6			1.1	4.0	ns	2-3, 5
t_{PHL}		1.0		3.9			1.0	4.6		
t_{PLH}	Propagation Delay LEAB or LEBA to B or A	1.0		4.7			1.0	5.3	ns	2-3, 5
t_{PHL}		1.0		4.7			1.0	5.0		
t_{PLH}	Propagation Delay $\overline{CLKAB}$ or $\overline{CLKBA}$ to B or A	1.0		4.4			1.0	5.3	ns	2-3, 5
t_{PHL}		1.0		4.3			1.0	5.0		
t_{PZH}	Propagation Delay OEAB or $\overline{OEBA}$ to B or A	1.0		4.1			1.0	4.8	ns	2-4
t_{PZL}		2.5		5.7			2.5	6.6		
t_{PHZ}	Propagation Delay OEAB or $\overline{OEBA}$ to B or A	1.5		5.2			1.5	6.2	ns	2-4
t_{PLZ}		1.4		4.7			1.4	5.4		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABTC $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50$ pF		54ABTC $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, A to $\overline{CLKAB}$	4.5 4.5				4.5 4.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, A to $\overline{CLKAB}$	0 0				0 0		ns	2-6
$t_s(H)$ $t_s(L)$	Setup Time, B to $\overline{CLKBA}$	4.0 4.0				4.0 4.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, B to $\overline{CLKBA}$	0 0				0 0		ns	2-6
$t_s(H)$ $t_s(L)$	Setup Time, A to LEAB or B to LEBA, $\overline{CLK}$ High	1.5 1.5				1.5 1.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, A to LEAB or B to LEBA, $\overline{CLK}$ High	1.5 1.5				1.5 1.5		ns	2-6
$t_s(H)$ $t_s(L)$	Setup Time, A to LEAB or B to LEBA, $\overline{CLK}$ Low	4.5 4.5				4.5 4.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, A to LEAB or B to LEBA, $\overline{CLK}$ Low	1.5 1.5				1.5 1.5		ns	2-6
$t_w(H)$ $t_w(L)$	Pulse Width, LEAB or LEBA, High	3.3 3.3				3.3 3.3		ns	2-3
$t_w(H)$ $t_w(L)$	Pulse Width, $\overline{CLKAB}$ or $\overline{CLKBA}$, High or Low	3.3 3.3				3.3 3.3		ns	2-3

Extended AC Electrical Characteristics : See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 18 Outputs Switching (Note 4)			74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 18 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Outputs	1.0 1.0		5.0 5.3	1.5 1.5	6.0 6.0	2.5 2.5	8.0 8.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.0 2.5		6.5 6.5	2.5 2.5	8.2 8.2	2.5 2.5	10.0 9.0	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5		6.7 6.9	(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 18 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 18 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	2.0	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.5	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	1.5	5.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	1.7	5.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	5.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0V$
C_{OUT} (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012.

National Semiconductor

PRELIMINARY

54ABT/74ABT16652C
16-Bit Transceiver/Register with TRI-STATE® Outputs

General Description

The 'ABT16652C consists of sixteen bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Separate control logic for each byte
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

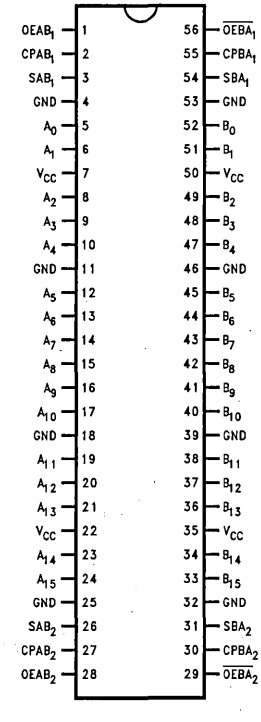
Ordering Code: See Section 11

Pin Descriptions

Pin Names	Description
A_0–A_{16}	Data Register A Inputs/ TRI-STATE Outputs
B_0–B_{16}	Data Register B Inputs/ TRI-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
$OEAB_n$, $\overline{OEBA}_n$	Output Enable Inputs

Connection Diagram

Pin Assignment for SSOP



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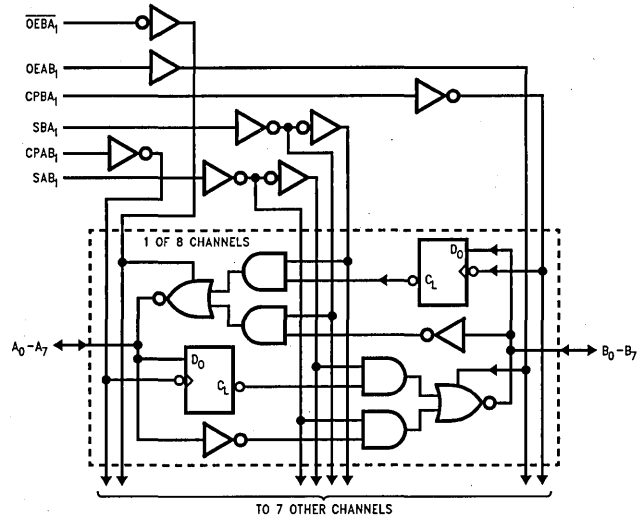
Logic Diagrams



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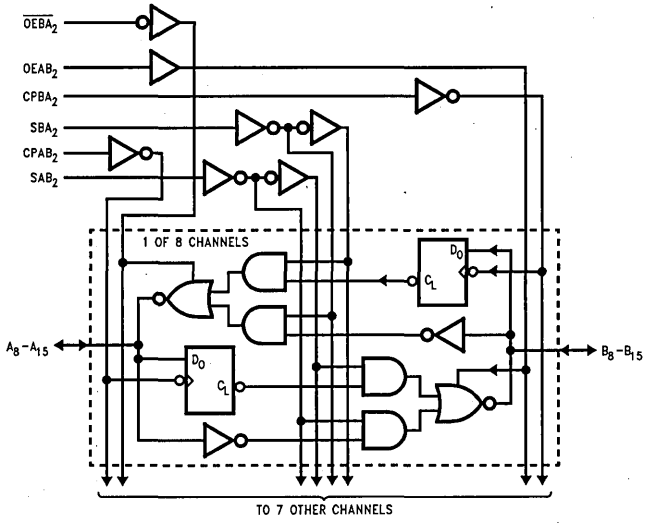

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Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

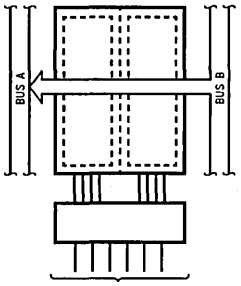
The select (SAB_n, SBA_n) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the 'ABT16652C.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs ($CPAB_n$, $CPBA_n$) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling $OEAB_n$ and $\overline{OEBA}_n$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Functional Description (Continued)

Note A: Real-Time Transfer Bus B to Bus A



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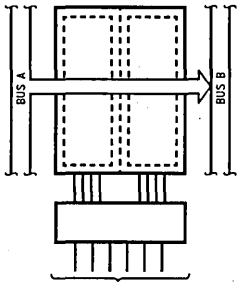
$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
L	L	X	X	X	L

Note B: Real-Time Transfer Bus A to Bus B



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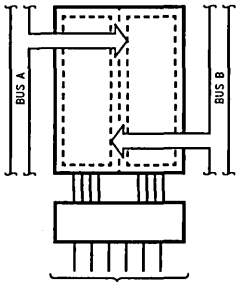
$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
H	H	X	X	L	X

Note C: Storage



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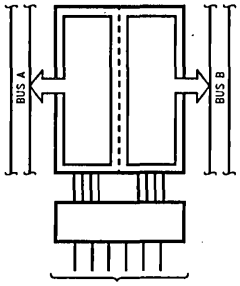
$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
X	H	↗	X	X	X
L	X	X	↗	X	X
L	H	↗	↗	X	X

Note D: Transfer Storage Data to A or B



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$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
H	L	H or L	H or L	H	X

FIGURE 1

Inputs						Inputs/Outputs (Note 1)		Operating Mode
$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8–15) and #2 control pins.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT16652C			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH 54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA, (A_n, B_n)
	Voltage 54ABT	2.0					I_{OH} = −24 mA, (A_n, B_n)
	74ABT	2.0					I_{OH} = −32 mA, (A_n, B_n)
V_{OL}	Output LOW 54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n)
	Voltage 74ABT			0.55			I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V or V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V or 0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $OEAB_n$ = GND and $\overline{OEBA}_n$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $OEAB_n$ = GND and $\overline{OEBA}_n$ = 2.0V

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT16652C			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			100	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			100	μA	Max	Outputs TRI-STATE; All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 1)			0.18	mA/MHz	Max	Outputs Open $OEAB_n$ and $\overline{OEBA}_n$ = GND Non-I/O = GND or V_{CC} One bit toggling, 50% duty cycle

Note 1: Guaranteed, but not tested.

DC Electrical Characteristics (SSOP package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	1.0	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.8		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.0	3.0		V	5.0	T_A = 25° (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	0.8		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SSOP package): See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF		54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	4.9			1.5	4.9	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	4.5			1.5	4.5	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay SBA_n or SAB_n to A_n to B_n	1.5	5.0			1.5	5.0	ns	2-3, 5
t_{PZH} t_{PZL}	Enable Time $\overline{OEBA}_n$ or $OEAB_n$ to A_n or B_n	1.5	5.5			1.5	5.5	ns	2-4
t_{PHZ} t_{PLZ}	Disable Time $\overline{OEBA}_n$ or $OEAB_n$ to A_n or B_n	1.5	6.0			1.5	6.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency		200						MHz	
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW Bus to Clock	1.5					1.5		ns	2-6
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW Bus to Clock	1.0					1.0		ns	2-6
$t_W(H)$ $t_W(L)$	Pulse Width, HIGH or LOW	3.0					3.0		ns	2-3

Extended AC Electrical Characteristics (SSOP package): See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 16 Outputs Switching (Note 4)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 16 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Progagation Delay Clock to Bus	1.5 1.5	5.5 5.5	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns	2-3, 5
t_{PLH} t_{PHL}	Progagation Delay Bus to Bus	1.5 1.5	6.0 6.0	2.0 2.0	7.0 7.0	2.5 2.5	9.5 9.5	ns	2-3, 5
t_{PLH} t_{PHL}	Progagation Delay SBA or SAB to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}_n$ or $OEAB_N$ to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	8.0 8.0	2.5 2.5	11.5 11.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.5 1.5	6.0 6.0	(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (SSOP Package) (Note 3)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 16 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 16 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.5	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	2.0	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	4.0		2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	4.0	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	4.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions (T_A = 25°C)
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0V (non I/O pins)
$C_{I/O}$ (Note 1)	I/O Capacitance	11.0	pF	V_{CC} = 5.0V (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

PRELIMINARY

54ABT/74ABT162244C 16-Bit Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The 'ABT162244C contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

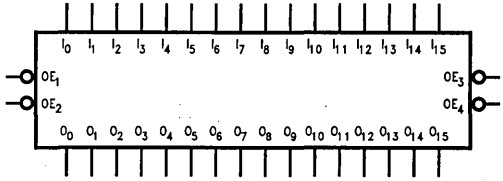
The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

- Separate control logic for each nibble
- 16-bit version of the 'ABT2244C
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latch protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Ordering Code: See Section 11

Logic Symbol



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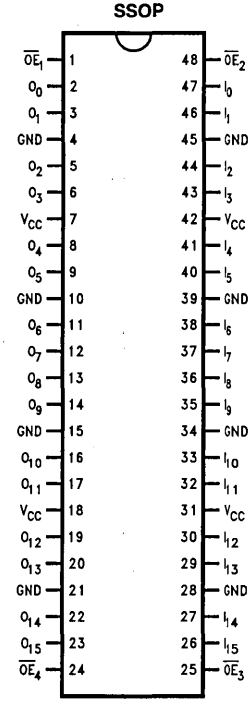
Connection Diagram



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Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

Preliminary Data.
National Semiconductor reserves the right to make changes at any time without notice.

5

Functional Description

The 'ABT162244C contains sixteen non-inverting buffers with TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

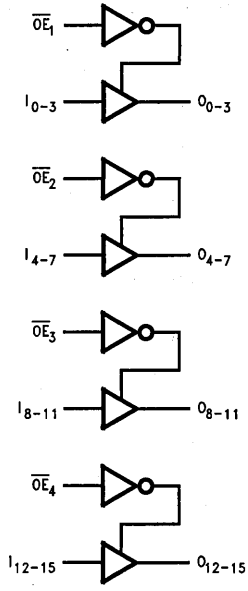
Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams



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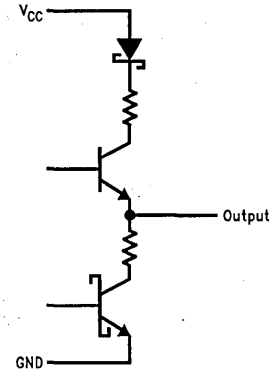
Schematic of each Output



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT162244C Min	ABT162244C Typ	ABT162244C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.8	V	Min	I_{OL} = 15 mA
		74ABT			0.8			I_{OL} = 15 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				100	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				100	μA	Max	$\overline{OE}_n$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 1)	No Load			0.1	mA/ MHz	Max	Outputs Open $\overline{OE}_n$ = GND One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed, but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF; R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.4	0.6	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.7	−1.0		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.7	3.0		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.4		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation	1.0	2.3	3.9			1.0	3.9	ns	2-3, 5
t_{PHL}	Delay Data to Outputs	1.0	3.2	4.4			1.0	4.4		
t_{PZH}	Output	1.5	3.5	6.3			1.5	6.3	ns	2-4
t_{PZL}	Enable Time	1.5	4.0	6.9			1.5	6.9		
t_{PHZ}	Output	1.0	4.2	6.7			1.0	6.7	ns	2-4
t_{PLZ}	Disable Time	1.0	4.2	6.7			1.0	6.7		

Extended AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF, 16 Outputs Switching (Note 4)			74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 1 Output Switching (Note 5)		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 16 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.0	ns	2-3, 5
t_{PHL}	Data to Outputs	1.5		5.5	1.5	10.0	2.5	11.0		
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.9	2.5	9.5	ns	2-4
t_{PZL}		1.5		7.0	2.5	12.2	2.5	12.5		
t_{PHZ}	Output	1.0		6.7	(Note 7)		(Note 7)		ns	2-4
t_{PLZ}	Disable Time	1.0		6.7						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 16 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 16 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	2.0	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.5	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	1.5	5.5	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	1.7	5.5	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	5.5	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0V$
C_{OUT}(Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012.

Section 6

Integrated Bus Function (IBF) Family

Section 6 Contents

National Semiconductor

PRELIMINARY

74ABT3284
18-Bit Synchronous Datapath Multiplexer

General Description

The 74ABT3284 is a synchronous datapath buffer designed to transmit four 9-bit bytes of data onto one or two 9-bit bytes in 2:1 or 4:1 multiplexed configurations. The device supports bidirectional data transfer in transparent or registered modes. A data byte from any one of the six ports can be stored during transparent operation for later recall. Data input to any port may also be read back to itself for byte manipulation or system self-diagnostic purposes.

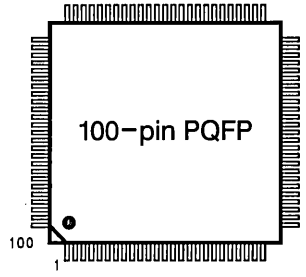
The 74ABT3284 is useful for interleaving data in memory applications or for use in bus-to-bus communications where variations in data word length or construction are required.

Features

- Advanced BiCMOS™ technology provides high speed at low power consumption
- 18-bit 2:1 or 9-bit 4:1 multiplexed modes
- Registered or transparent datapath operation
- Output enables and select lines have the option of being synchronized for pipelined operation
- Independent input, output register and control synchronizing clocks insure maximum timing flexibility
- Independent control signals insure functional flexibility
- Guaranteed output skew
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Ordering Code: See Section 11

Connection Diagram



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Pin Assignment

Pin		Pin		Pin		Pin		Pin	
1	Mode_SO	21	$XSEL_1$	41	GND	61	Y_6	81	D_5
2	CP_AX	22	LDAO	42	B_2	62	Y_5	82	D_4
3	OEC	23	LDAI	43	B_3	63	Y_4	83	D_3
4	LDCI	24	OEA	44	B_4	64	Y_3	84	D_2
5	LDCO	25	V_{CC}	45	B_5	65	Y_2	85	GND
6	SA_2X_1	26	V_{CC}	46	GND	66	GND	86	D_1
7	SA_2X_0	27	A_8	47	B_6	67	Y_1	87	D_0
8	X_0	28	A_7	48	B_7	68	Y_0	88	V_{CC}
9	X_1	29	A_6	49	B_8	69	LDDO	89	C_0
10	GND	30	GND	50	V_{CC}	70	LDDI	90	C_1
11	X_2	31	A_5	51	CP_IN	71	ASEL1	91	GND
12	X_3	32	A_4	52	OEB	72	ASEL0	92	C_2
13	X_4	33	A_3	53	LDBI	73	OED	93	C_3
14	X_5	34	A_2	54	LDBO	74	CP_XA	94	C_4
15	X_6	35	GND	55	Mode_W	75	Mode_SC	95	C_5
16	GND	36	A_1	56	YSEL	76	V_{CC}	96	GND
17	X_7	37	A_0	57	OEY	77	D_8	97	C_6
18	X_8	38	V_{CC}	58	Y_8	78	D_7	98	C_7
19	OEX	39	B_0	59	Y_7	79	D_6	99	C_8
20	$XSEL_0$	40	B_1	60	GND	80	GND	100	V_{CC}

Logic Diagrams

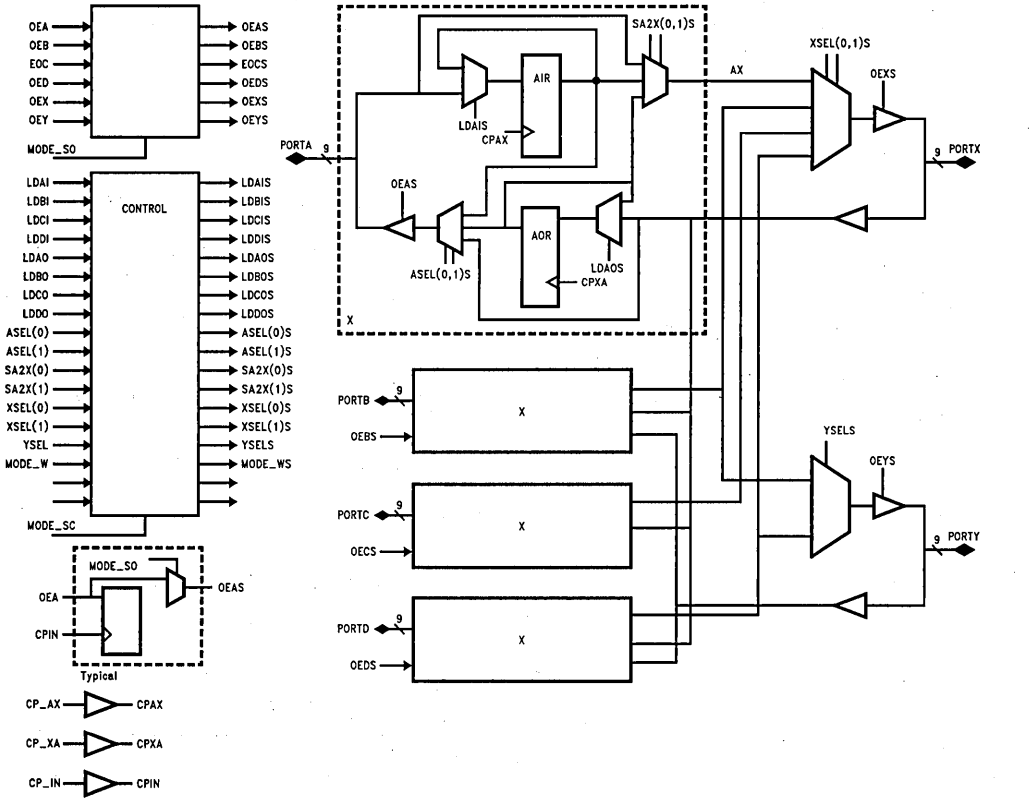

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FIGURE 1. 18-Bit Synchronous Datapath Multiplexer

Logic Diagrams (Continued)

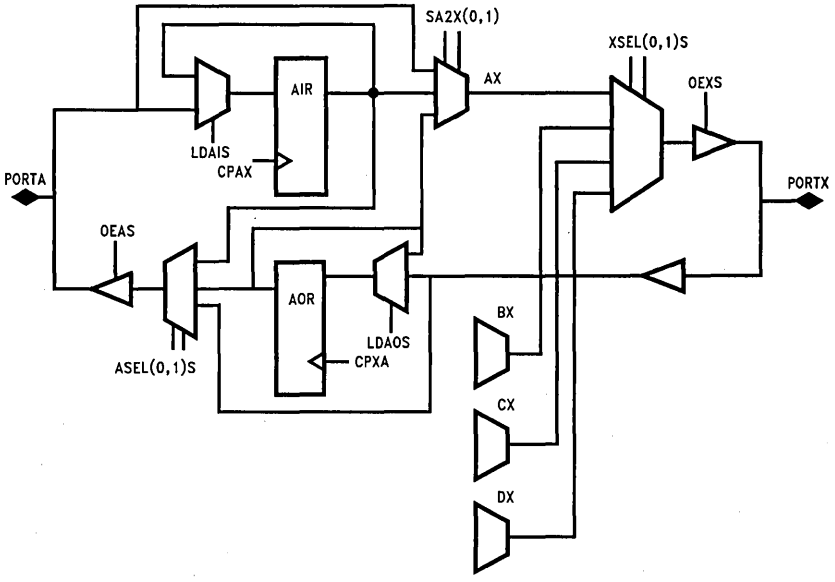

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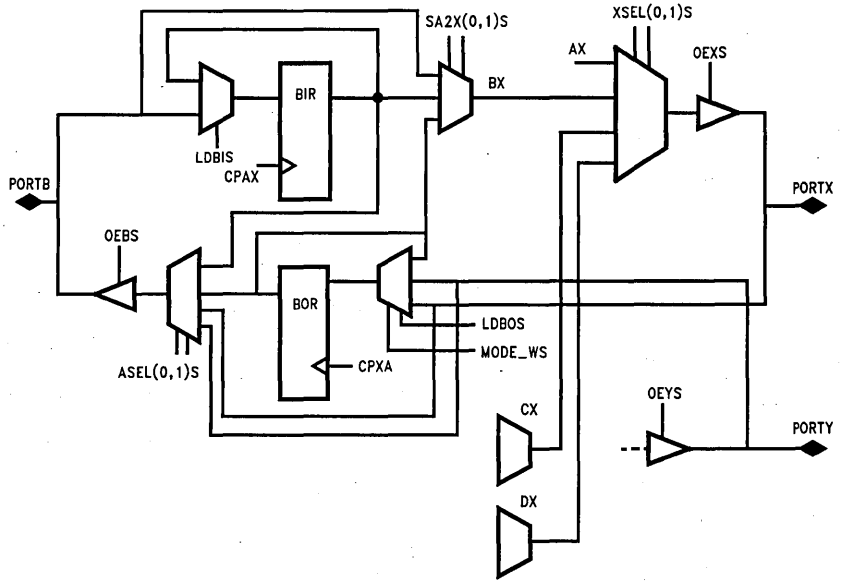
FIGURE 2. Synchronous Bus Multiplexer A-X Datapath



C and D ports are configured similarly to the B port.

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FIGURE 3. Synchronous Bus Multiplexer B PORT Datapath

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to +5.5V
in the HIGH STATE	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT3284			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.5 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −32 mA (Note 3)
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA (Note 4)
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V Control Inputs
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n, C_n, D_n, X_n, Y_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V Control Inputs
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA Control Inputs All Data Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current			50	μA	0–5.5	V_{OUT} = 2.7V (A_n, B_n, C_n, D_n, X_n, Y_n) All Output Enables = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−50	μA	0–5.5	V_{OUT} = 0.5V (A_n, B_n, C_n, D_n, X_n, Y_n) All Output Enables = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0.0V (A_n, B_n, C_n, D_n, X_n, Y_n)
I_{CEX}	Output High Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n, C_n, D_n, X_n, Y_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.5V (A_n, B_n, C_n, D_n, X_n, Y_n)
I_{CCH}	Power Supply Current			3	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			140	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			250	μA	Max	Output Enables = V_{CC}; All Others at GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_{IN} = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load			0.18	mA/MHz	Max	Outputs Open Output Enables = GND One Bit Toggling, 50% Duty Cycle

Note 3: Up to 18 outputs can each source 32 mA continuously, or any combination of outputs can source up to a total of 324 mA. For example, 36 outputs can continuously each source 16 mA.

Note 4: Up to 18 outputs can each sink 64 mA continuously, or any combination of outputs can sink up to a total of 648 mA. For example, 36 outputs can continuously each sink 32 mA.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.0	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.8		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.7	0.9	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Max Operating Frequency			200		200	MHz	
t_{PHL} t_{PLH}	Propagation Delay Clock Data Register to A, B, C, D, X, or Y			6.0		6.0	ns	2-3, 5
t_{PHL} t_{PLH}	Propagation Delay Clock Select Register to A, B, C, D, X, or Y (Note 1)			6.0		6.0	ns	2-3, 5
t_{PHL} t_{PLH}	Propagation Delay A, B, C, D, X, or Y Data Inputs to A, B, C, D, X, or Y Outputs (Note 1)			5.0		5.0	ns	2-3, 5
t_{PHL} t_{PLH}	Propagation Delay Select Inputs (without clocking) to A, B, C, D, X, or Y Outputs (Note 1)			5.0		5.0	ns	2-3, 5
t_{PHL} t_{PLH}	Propagation Delay CLKA at Select Inputs to A, B, C, D, X, or Y Outputs (Note 1)			6.0		6.0	ns	2-3, 5
t_{PZL} t_{PZH}	$\overline{OE}$ (unclocked) to A, B, C, D, X, or Y Outputs (Note 1)						ns	2-4

Note 1: Maximum 18 outputs switching simultaneously.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_s (H) t_s (L)	Setup Time High or Low A, B, C, D, X, and Y Inputs	3			3		ns	2-6
t_h (H) t_h (L)	Hold Time High or Low A, B, C, D, X, and Y Inputs	0			0		ns	2-6
t_s (H) t_s (L)	Setup Time High or Low Control Inputs	3			3		ns	2-6
t_h (H) t_h (L)	Hold Time High or Low Control Inputs	0			0		ns	2-6
t_w (L)	Pulse Width, Low	4			4		ns	2-3

Skew (SOIC Package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 18 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 18 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	TBD	TBD	ns	2-15
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	TBD	TBD	ns	2-15
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	TBD	TBD	ns	2-16
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	TBD	TBD	ns	2-19
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	TBD	TBD	ns	2-22

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$ Control Inputs
$C_{I/O}$ (Note 1)	I/O Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n, C_n, D_n, X_n, Y_n)

Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

74ACTQ3283T 32-Bit Latchable Transceiver with Parity Generator/Parity Checker and Byte Multiplexing with TRI-STATE® Outputs

General Description

The 'ACTQ3283T is a 32-bit latchable transceiver with parity checker/generator. The device can operate as a transceiver generating parity in the A-B direction and checking it in the B-A direction. It can be used to multiplex between data bytes, and provides an easy interface between 32-bit and 8- or 16-bit data busses. It has a guaranteed current sink/source capacity of 24 mA, and features reduced voltage swing outputs to improve output noise and EMI crosstalk.

The 'ACTQ3283T features independent latch enables for the B side, and a 32-bit latch enable for the A side. Each byte is selectable separately for complete byte-wide multiplex control.

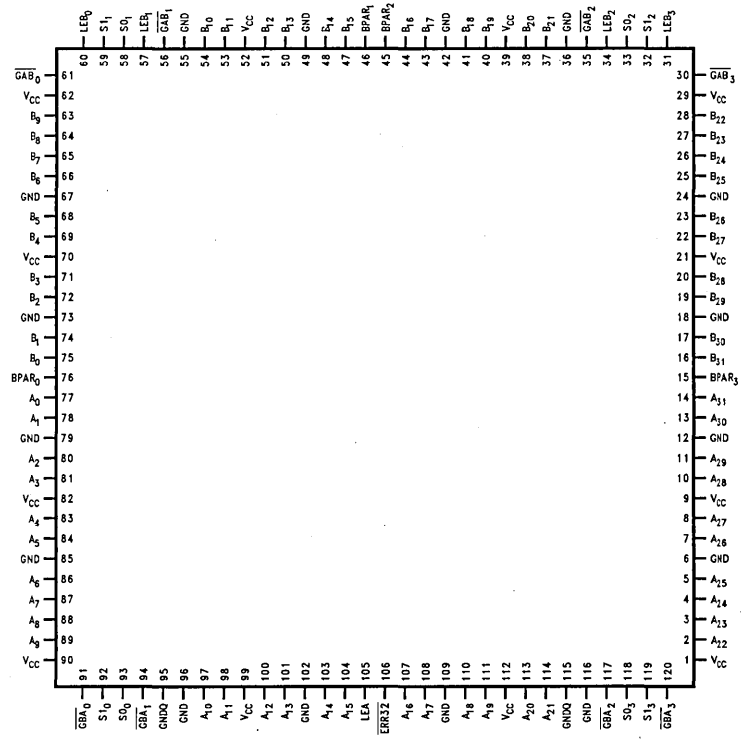
Features

- Utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control for superior performance
- Reduced voltage swing outputs for lower EMI
- Latchable transceiver with 24 mA source/sink capability
- Even parity generation in A-B direction and 32-bit parity check in B-A direction
- Fully selectable byte multiplexing allows byte swapping, byte copying, and 32-bit to 8-bit/16-bit multiplexing
- Separate control logic for each byte

Ordering Code: See Section 11

Connection Diagram

Pin Assignment for PQFP



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Functional Description

The 'ACTQ3283T can operate in transparent or latched modes, with complete byte multiplexing selectable at every byte. For the following descriptions data byte will be referred to as A_n or B_n, the n refers to 0–3 thus representing bytes A_0, A_1, A_2 or A_3.

— Byte A_n to B_n (Feedthrough mode), LEA is held HIGH to put latch in transparent mode. Parity is generated for each byte and select pins $S0_n$ and $S1_n$ select which data byte (A_0–A_3) is fed through.

— Byte B_n to A_n (Feedthrough mode), LEB_n is held HIGH to put latch in transparent mode. Parity is checked for each byte and $\overline{ERR32}$ goes LOW if there is one or more parity errors. Select pins $S0_n$ and $S1_n$ select which data byte (B_0–B_3) is fed through.

— Independent Latch enables LEA, LEB_0, LEB_1, LEB_2 and LEB_3 provide means of latching data at the A bus or at any byte (B_0–B_3) on the B bus. Select pins $S0_n$ and $S1_n$ select which data byte output. See function table and select table for further information.

Pin Description

Pin Names	Description
A_0–A_7	A_0 Byte Inputs/Outputs
A_8–A_{15}	A_1 Byte Inputs/Outputs
A_{16}–A_{23}	A_2 Byte Inputs/Outputs
A_{24}–A_{31}	A_3 Byte Inputs/Outputs
B_0–B_7	B_0 Byte Inputs/Outputs
B_8–B_{15}	B_1 Byte Inputs/Outputs
B_{16}–B_{23}	B_2 Byte Inputs/Outputs
B_{24}–B_{31}	B_3 Byte Inputs/Outputs
$\overline{GAB_0}$–$\overline{GAB_3}$	Output Enable for Byte B_0–B_3, Organized Byte Wide, Active LOW
$\overline{GBA_0}$–$\overline{GBA_3}$	Output Enable for Byte A_0–A_3, Organized Byte Wide, Active LOW
LEA	Latch Enable for A_0, A_1, A_2 and A_3. HIGH for Transparent mode.
LEB_0–LEB_3	Latch Enable for B_0–B_3 Organized byte wide. HIGH for Transparent mode.
$S0_0$–$S0_3$	Select Pins for Byte Multiplexing, Organized by Byte.
$S1_0$–$S1_3$	
$BPAR_0$–$BPAR_3$	Parity bit input/output, one per byte B side only. LOW for EVEN parity.
$\overline{ERR32}$	32-bit parity error, generated by bytes B_0–B_3 and $BPAR_0$–$BPAR_3$. LOW indicates parity error on ONE or MORE of B side bytes.

Select Table

Inputs		Operation
$S1_n$	$S0_n$	
0	0	Byte 0 Data Selected
0	1	Byte 1 Data Selected
1	0	Byte 2 Data Selected
1	1	Byte 3 Data Selected

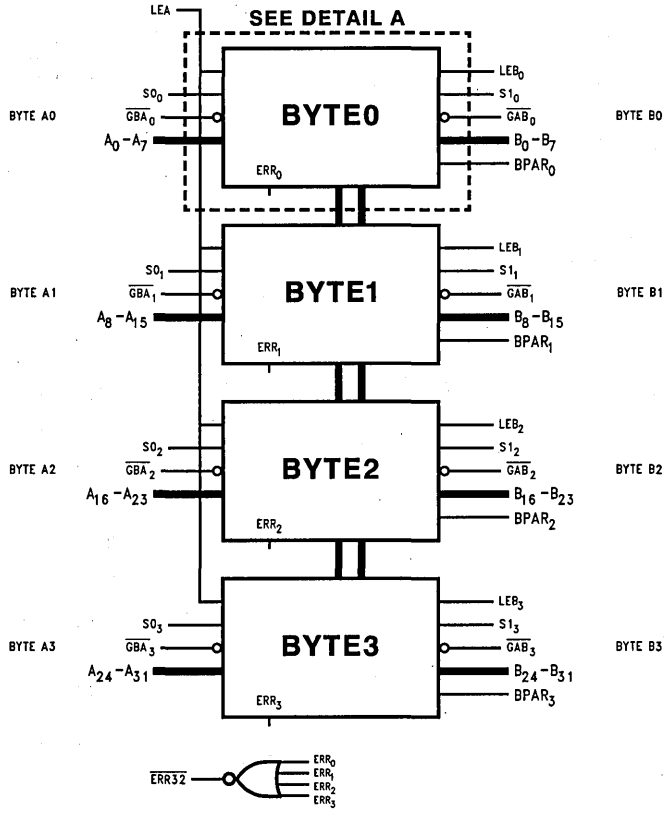
Select pins for the 'ACTQ3283T are organized by byte, and allow for complete byte multiplexing of data. Two control pins S0 and S1 are available for each byte, and the data is selected as described in the Select Tabe for both the A–B and B–A direction.

Function Table

Inputs						Operation
$\overline{GAB}_n$	$\overline{GBA}_n$	LEA	LEB_n	$S1_n$	$S0_n$	
H	H	X	X	X	X	Busses A_n and B_n are in TRI-STATE
L	H	H	X	L	L	Data on bus A_0 is fed through to B_n Parity $BPAR_n$ is generated from A_0
L	H	H	X	L	H	Data on bus A_1 is fed through to B_n Parity $BPAR_n$ is generated from A_1
L	H	H	X	H	L	Data on bus A_2 is fed through to B_n Parity $BPAR_n$ is generated from A_2
L	H	H	X	H	H	Data on bus A_3 is fed through to B_n Parity $BPAR_n$ is generated from A_3
H	L	X	H	L	L	Data on bus B_0 is fed through to A_n Parity is checked by B_n and $BPAR_n$ $\overline{ERR32}$ is pulled LOW on parity ERROR
H	L	X	H	L	H	Data on bus B_1 is fed through to A_n Parity is checked by B_n and $BPAR_n$ $\overline{ERR32}$ is pulled LOW on parity ERROR
H	L	X	H	H	L	Data on bus B_2 is fed through to A_n Parity is checked by B_n and $BPAR_n$ $\overline{ERR32}$ is pulled LOW on parity ERROR
H	L	X	H	H	H	Data on bus B_3 is fed through to A_n Parity is checked by B_n and BPARn $\overline{ERR32}$ is pulled LOW on parity ERROR
L	H	L	X	X	X	Data on bus A is latched and output on B_n based on the select signals
H	L	X	L	X	X	Data on bus B_n is latched and output on A_n based on the select signals

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
A_n – indicates byte A_0, A_1, A_2 or A_3
B_n – indicates byte B_0, B_1, B_2 or B_3
A_0 – indicates byte 0, or pins A_0–A_7

Logic Diagrams



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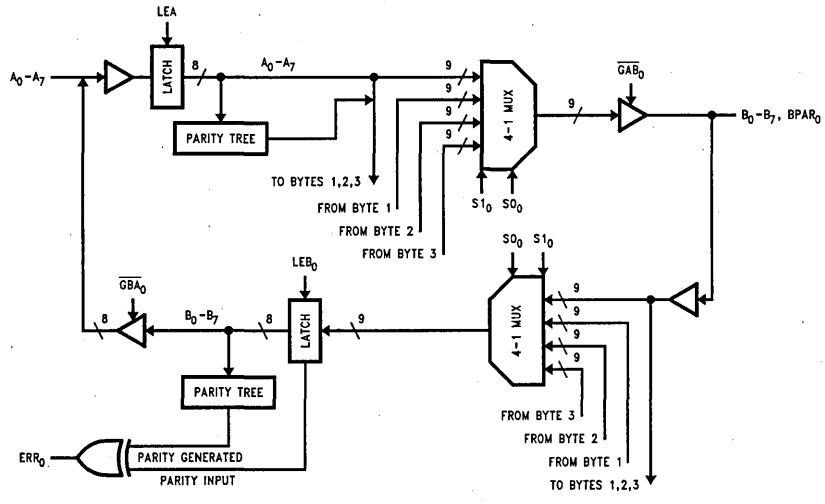
Detail A



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
Junction Temperature PQFP	+140°C
Storage Temperature	−65°C to +150°C
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC}) 'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A) 74ACTQ	−40°C to +85°C
Minimum Input Edge Rate dV/dt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ +25°C		74ACTQ −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{OH}
V_{IL}	Maximum Low Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{OH}
V_{OH}	Minimum High Output Voltage	4.5 5.5		3.15 3.85	3.15 3.85	V	I_{OUT} = −50 μA
		4.5 5.5		2.0 2.0	2.0 2.0	V	V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} − 2.1V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			63	mA	V_{OLD} = 0.8V Max
I_{OHD}					−40	mA	V_{OHD} = 2.0V Min
I_{OZT}	Max I/O Leakage Current	5.5		±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH}

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ +25°C		74ACTQ −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.7	1.2		V	*Figures 9, 10* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.7	−1.2		V	*Figures 9, 10* (Notes 2, 3)
V_{OHP}	Maximum Overshoot	5.0	V_{OH} + 0.6	V_{OH} + 1.2		V	*Figures 9, 10* (Notes 1, 3)
V_{OHV}	Minimum V_{CC} Droop	5.0	V_{OH} − 0.3	V_{OH} − 0.7		V	*Figures 9, 10* (Notes 1, 3)
V_{IHD}	Minimum High Dynamic Input Voltage Level	5.0	1.7	2.0		V	(Notes 1, 4)
V_{ILD}	Maximum Low Dynamic Input Voltage Level	5.0	1.2	0.8		V	(Notes 1, 4)

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V ('ACTQ). Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ +25°C 50 pF			74ACTQ −40°C to +85°C 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A to B	5.0	3.5	7.6	9.7	3.5	10.8	ns	1
t_{PLH} t_{PHL}	Propagation Delay B to A	5.0	3.5	8.9	11.2	3.5	12.5	ns	1
t_{PLH} t_{PHL}	Propagation Delay A to $BPAR_n$	5.0	4.5	9.6	12.1	4.5	13.6	ns	3
t_{PLH} t_{PHL}	Propagation Delay B to $\overline{ERR32}$	5.0	5.0	12.0	14.8	5.0	16.7	ns	4
t_{PLH} t_{PHL}	Propagation Delay $BPAR_n$ to $\overline{ERR32}$	5.0	3.5	10.5	13.2	3.5	14.8	ns	4
t_{PLH} t_{PHL}	Propagation Delay LEA to B_n	5.0	4.5	8.8	10.9	4.5	12.1	ns	2
t_{PLH} t_{PHL}	Propagation Delay LEA to $BPAR_n$	5.0	5.0	10.6	13.1	5.0	14.7	ns	2
t_{PLH} t_{PHL}	Propagation Delay LEB_n to A_n	5.0	4.5	8.7	10.9	4.5	12.3	ns	2
t_{PLH} t_{PHL}	Propagation Delay $S0/S1_n$ to A_n	5.0	4.5	9.3	11.6	4.5	12.9	ns	5
t_{PLH} t_{PHL}	Propagation Delay $S0/S1_n$ to B_n $S0/S1_n$ to BPARn	5.0	3.5	8.6	10.9	3.5	12.1	ns	5
t_{PZL} t_{PZH}	Enable Time	5.0	2.5	7.6	9.8	2.5	10.8	ns	6, 7
t_{PLZ} t_{PHZ}	Disable Time	5.0	1.0	4.5	6.6	1.0	7.2	ns	6, 7

*Voltage range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACTQ Typical $T_A = +25°C$	74ACTQ Commercial $T_A = -40°C$ to $+85°C$	Units
t_s	Setup Time A_n to LEA	5.0	1.0	3.0	ns
t_s	Setup Time B_n, $BPAR_n$ to LEB_n	5.0	1.0	3.0	ns
t_h	Hold Time A_n to LEA	5.0	1.0	1.5	ns
t_h	Hold Time B_n, $BPAR_n$ to LEB_n	5.0	1.0	1.5	ns
t_w	Min Pulse Width LEA	5.0	1.5	4.0	ns
t_w	Min Pulse Width LEB_n	5.0	1.5	4.0	ns

*Voltage range 5.0 is 5.0V ±0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	74ACTQ T_A = Com, V_{CC} = Com, C_L = 50 pF, 32 Outputs Switching (Note 1)		74ACTQ $T_A = -40°C$ to $+85°C$, V_{CC} = Com, C_L = 250 pF (Note 2) 1 Output Switching		74ACTQ $T_A = -40°C$ to $+85°C$, V_{CC} = Com, C_L = 250 pF (Notes 1, 2) 32 Outputs Switching		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A to B	4.5	11.8	5.0	14.5	6.0	15.5	ns
t_{PLH} t_{PHL}	Propagation Delay B to A	5.0	13.0	5.0	15.0	6.0	16.0	ns
t_{PLH} t_{PHL}	Propagation Delay A to $BPAR_n$	5.5	14.5	6.0	17.0	7.0	19.0	ns
t_{PLH} t_{PHL}	Propagation Delay B to $\overline{ERR32}$	6.0	17.5	7.0	19.5	8.0	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay $BPAR_n$ to $\overline{ERR32}$	4.5	15.5	5.0	17.5	6.0	19.5	ns
t_{PLH} t_{PHL}	Propagation Delay LEA to B_n	5.0	13.0	6.0	15.5	7.0	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay LEA to $BPAR_n$	6.0	15.5	6.5	18.5	7.5	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay LEB_n to A_n	5.0	14.0	5.5	16.0	7.0	18.0	ns
t_{PLH} t_{PHL}	Propagation Delay $S0_n/S1_n$ to A_n	6.0	17.0	7.0	20.0	8.0	21.0	ns
t_{PLH} t_{PHL}	Propagation Delay $S0_n/S1_n$ to B_n $S0_n/S1_n$ to $BPAR_n$	5.0	13.0	5.5	16.5	6.0	18.0	ns
t_{PZL} t_{PZH}	Enable Time			(Note 3)				ns
t_{PLZ} t_{PHZ}	Disable Time			(Note 4)				ns

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (il.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 3: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 4: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	7.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	62	pF	V_{CC} = 5.0V

AC Path

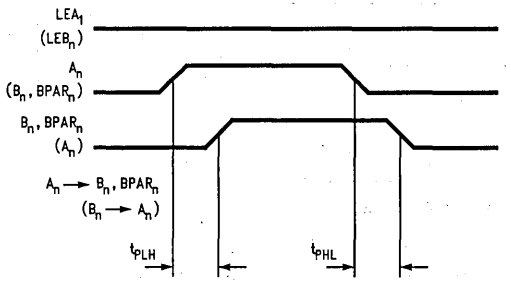

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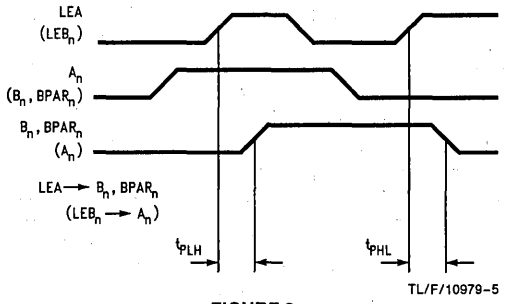
FIGURE 1



TL/F/10979-5

FIGURE 2

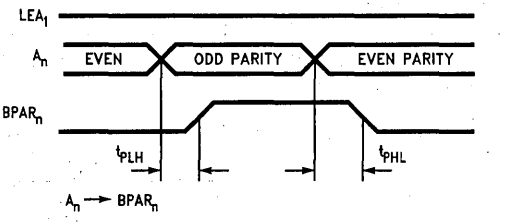


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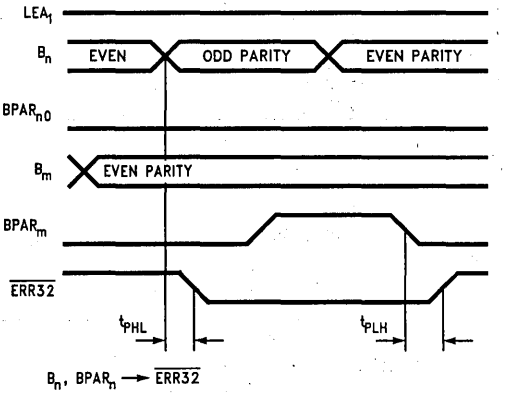
FIGURE 3



TL/F/10979-7

FIGURE 4

AC Path (Continued)

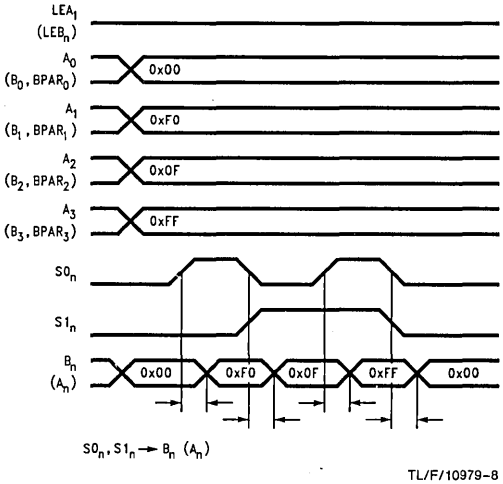


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FIGURE 5. 32-Bit to 8-Bit Multiplexing

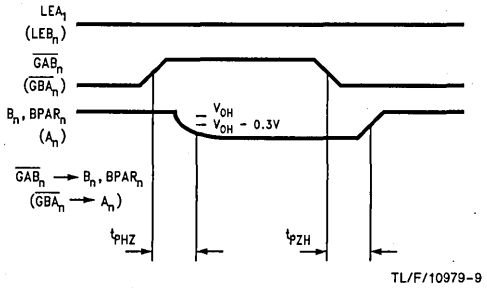

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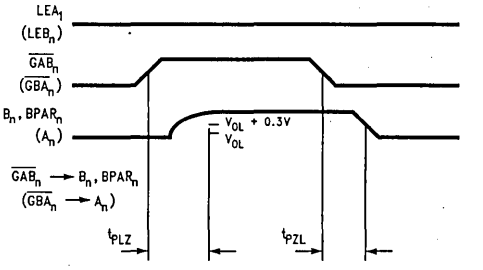
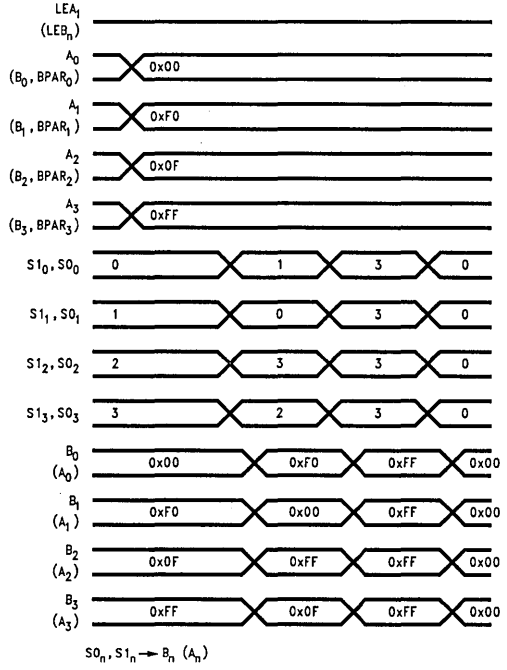
FIGURE 6



TL/F/10979-10

FIGURE 7



TL/F/10979-11

FIGURE 8. Byte Swapping and Byte Copying

Application 1: 32-Bit or 2/16-Bit Data Buffer and Parity Generate/Check

Detailed Pin Description

The following is a table that relates the pin names of the discrete implementation to the 'ACTQ3283T. Also listed are the number of pins, the type of each pin and the function performed.

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type*	Function
A_0–A_7 A_8–A_{15} A_{16}–A_{23} A_{24}–A_{31}	A_{00}–A_{07} A_{08}–A_{15} A_{16}–A_{23} A_{24}–A_{31}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from A bus to B bus the signal associations are: A_0–A_7 B_0–B_7 A_8–A_{15} B_8–B_{15} A_{16}–A_{23} B_{16}–B_{23} A_{24}–A_{31} B_{24}–B_{31}
B_0–B_7 B_8–B_{15} B_{16}–B_{23} B_{24}–B_{31}	B_{00}–B_{07} B_{08}–B_{15} B_{16}–B_{23} B_{24}–B_{31}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from B bus to A bus the signal associations are: B_0–B_7 A_0–A_7 B_8–B_{15} A_8–A_{15} B_{16}–B_{23} A_{16}–A_{23} B_{24}–B_{31} A_{24}–A_{31}
$BPAR_0$–$BPAR_3$	$BPAR_0$–$BPAR_3$	4	I/O	When data is transferred from the A side to the B side each parity bit will be generated to perform even parity for each byte. Data transferred from the B side to the A side will provide the parity bit which will be checked internally.
$\overline{GAB}_0$–$\overline{GAB}_3$	$\overline{EN}_0$–$\overline{EN}_3$ T/$\overline{R}$ (L) T/$\overline{R}$ (H)	4	I	A output enables. When this signal is low the data on the A side, latched or active will be output to the B side. Signal associations are: $\overline{GAB}_0$ A_0–A_7 B_0–B_7 $\overline{GAB}_1$ A_8–A_{15} B_8–B_{15} $\overline{GAB}_2$ A_{16}–A_{23} B_{16}–B_{23} $\overline{GAB}_3$ A_{24}–A_{31} B_{24}–B_{31}

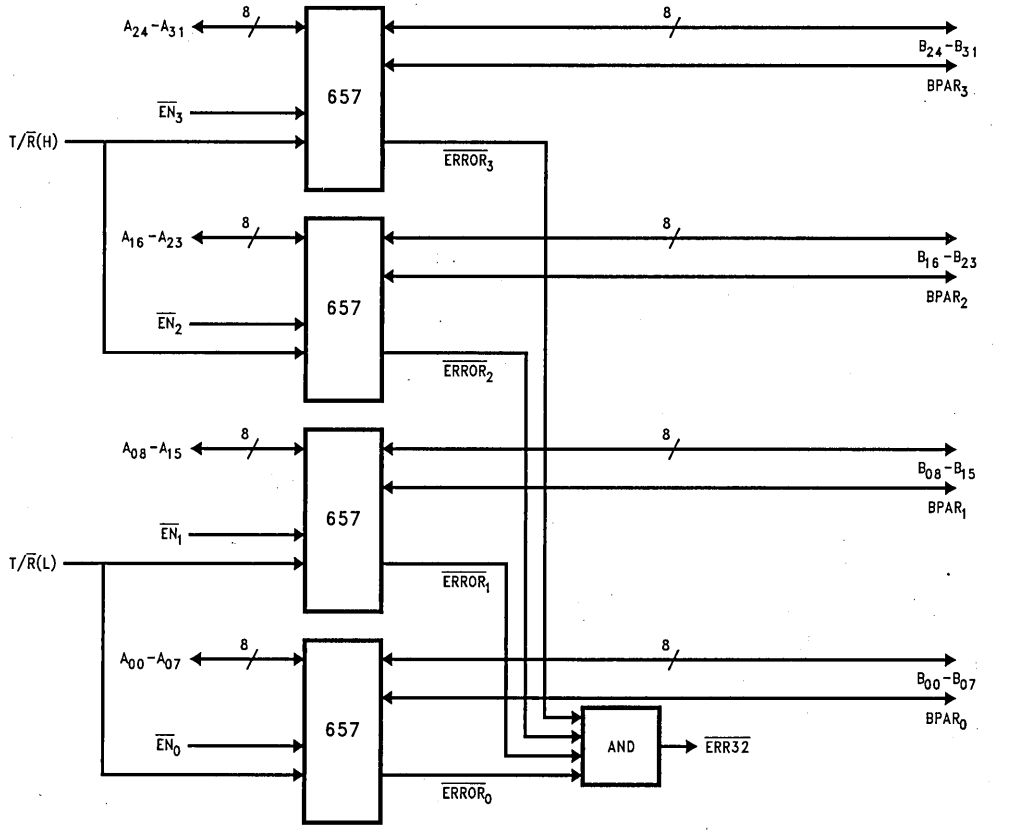
*I = Input, O = Output

Application 1: 32-Bit or 2/16-Bit Data Buffer and Parity Generate/Check
(Continued)

Detailed Pin Description (Continued)

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
$\overline{GBA}_0$–$\overline{GBA}_3$	$\overline{EN}_0$–$\overline{EN}_3$ T/$\overline{R}$ (L) T/$\overline{R}$ (H)	4	I	B output enables. When this signal is low the data on the B side, latched or active will be output to the A side. Signal associations are: $\overline{GAB}_0$ B_0–B_7 A_0–A_7 $\overline{GAB}_1$ B_8–B_{15} A_8–A_{15} $\overline{GAB}_2$ B_{16}–B_{23} A_{16}–A_{23} $\overline{GAB}_3$ B_{24}–B_{31} A_{24}–A_{31}
$\overline{ERR32}$	$\overline{ERR32}$	1	O	This pin indicates if any one or more bytes had a parity error.

Application 1: 32-Bit or 2/16-Bit Data Buffer and Parity Generate/Check



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Application 2: 16-Bit Data and 16-Bit Address Buffer

Detailed Pin Description

The following is a table that relates the pin names of the discrete implementation to the 'ACTQ3283T. Also listed are the number of pins, the type of each pin and the function performed.

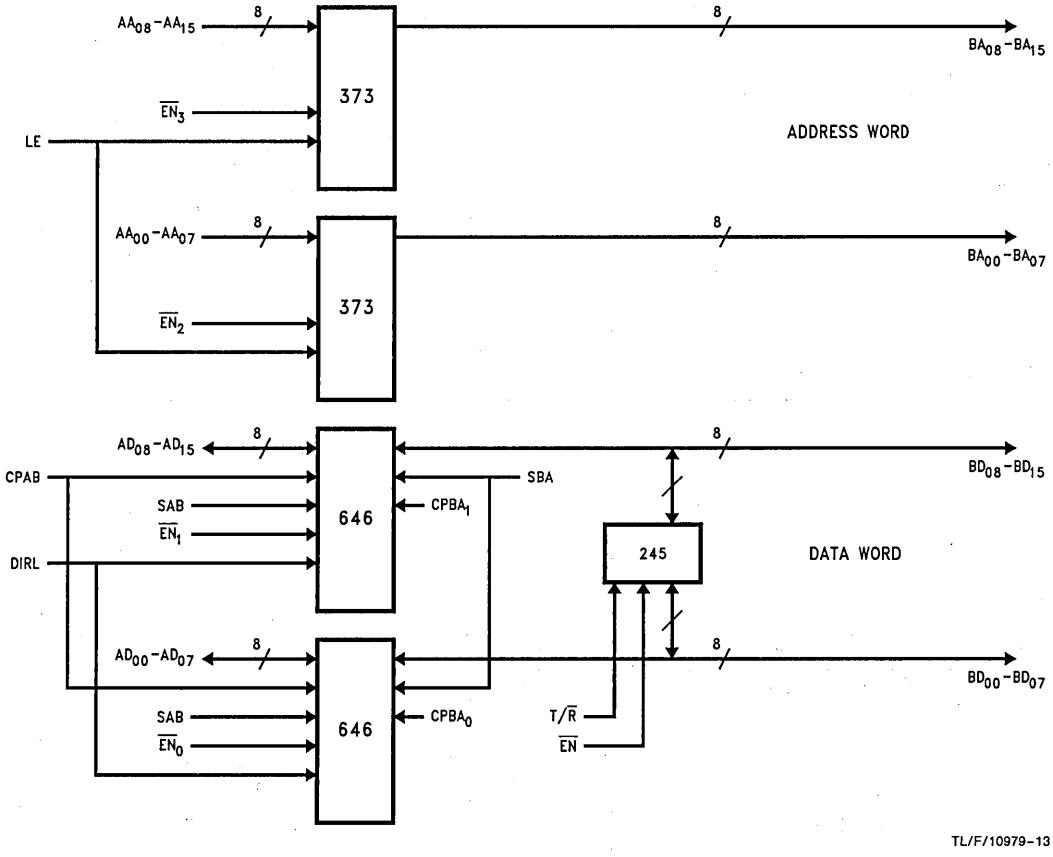
'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
A_0–A_7 A_8–A_{15} A_{16}–A_{23} A_{24}–A_{31}	AD_{00}–AD_{07} AD_{08}–AD_{15} AA_{00}–AA_{07} AA_{08}–AA_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from A bus to B bus the signal associations are: A_0–A_7 B_0–B_7 A_8–A_{15} B_8–B_{15} A_{16}–A_{23} B_{16}–B_{23} A_{24}–A_{31} B_{24}–B_{31}
B_0–B_7 B_8–B_{15} B_{16}–B_{23} B_{24}–B_{31}	BD_{00}–BD_{07} BD_{08}–BD_{15} BA_{16}–BA_{23} BA_{24}–BA_{31}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from B bus to A bus the signal associations are: B_0–B_7 A_0–A_7 B_8–B_{15} A_8–A_{15} B_{16}–B_{23} A_{16}–A_{23} B_{24}–B_{31} A_{24}–A_{31}
$BPAR_0$–$BPAR_3$	$BPAR_0$–$BPAR_3$	4	I/O	Each BPAR pin should be tied to V_{CC} through a suitable resistor if parity is not used.
$\overline{GAB}_0$–$\overline{GAB}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL	4	I	A output enables. When this signal is low the data on the A side, latched or active will be output to the B side. Signal associations are: $\overline{GAB}_0$ A_0–A_7 B_0–B_7 $\overline{GAB}_1$ A_8–A_{15} B_8–B_{15} $\overline{GAB}_2$ A_{16}–A_{23} B_{16}–B_{23} $\overline{GAB}_3$ A_{24}–A_{31} B_{24}–B_{31}
$\overline{GBA}_0$–$\overline{GBA}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL	4	I	B output enables. When this signal is low the data on the B side, latched or active will be output to the A side. Signal associations are: $\overline{GBA}_0$ B_0–B_7 to A_0–A_7 $\overline{GBA}_1$ B_8–B_{15} to A_8–A_{15} $\overline{GBA}_2$ Tied high for this app. $\overline{GBA}_3$ Tied high for this app.
LEA	LE CPAB	1	I	Will latch in the address and data.
LEB_0–LEB_3	$CPBA_0$ $CPBA_1$	4	I	Individual B byte latch enable. When in high state, B data is transparent and if in low state, B data is latched LEB_0 H or L LEB_1 H or L LEB_2 Low for this app. LEB_3 Low for this app.

Application 2: 16-Bit Data and 16-Bit Address Buffer (Continued)

Detailed Pin Description (Continued)

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
$S0_0$–$S0_3$ $S1_0$–$S1_3$	T/$\overline{R}$ (245) $\overline{EN}$ (245)	8	I	These pins allow byte multiplexing, organized by byte, Each byte may be directed to any other byte by setting S0, S1 in a binary fashion to select the stimulus. For this application: $S1_0$=L $S0_0$=L B_0 selected at B_0 $S1_0$=L $S0_0$=H B_1 selected at B_0 $S1_1$=L $S0_1$=L B_0 selected at B_1 $S1_1$=L $S0_1$=H B_1 selected at B_1 $S1_2$=H $S0_2$=L B_2 selected at B_2 $S1_2$=H $S0_3$=H B_3 selected at B_3
N/A	SAB SBA			Select of active byte or latched byte not available.

Application 2: 16-Bit Data and 16-Bit Address Buffer (Continued)



Application 3: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer

Detailed Pin Description

The following is a table that relates the pin names of the discrete implementation to the 'ACTQ3283T. Also listed are the number of pins, the type of each pin and the function performed.

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
A_0–A_7 A_8–A_{15} A_{16}–A_{23} A_{24}–A_{31}	AD_{00}–A_{07} AD_{08}–A_{15} AA_{00}–A_{07} AA_{08}–A_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from A bus to B bus the signal associations are: A_0–A_7 B_0–B_7 A_8–A_{15} B_8–B_{15} A_{16}–A_{23} B_{16}–B_{23} A_{24}–A_{31} B_{24}–B_{31}
B_0–B_7 B_8–B_{15} B_{16}–B_{23} B_{24}–B_{31}	BD_{00}–B_{07} BD_{08}–B_{15} BA_{00}–B_{07} BA_{08}–B_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from B bus to A bus the signal associations are: B_0–B_7 A_0–A_7 B_8–B_{15} A_8–A_{15} B_{16}–B_{23} A_{16}–A_{23} B_{24}–B_{31} A_{24}–A_{31}
$BPAR_0$–$BPAR_3$	$BPAR_0$–$BPAR_3$	4	I/O	Each BPAR pin should be tied to V_{CC} through a suitable resistor if parity is not used.
$\overline{GAB}_0$–$\overline{GAB}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL DIRH	4	I	A output enables. When this signal is low the data on the A side, latched or active will be output to the B side. Signal associations are: $\overline{GAB}_0$ A_0–A_7 to B_0–B_7 $\overline{GAB}_1$ A_8–A_{15} to B_8–B_{15} $\overline{GAB}_2$ A_{16}–A_{23} to B_{16}–B_{23} $\overline{GAB}_3$ A_{24}–A_{31} to B_{24}–B_{31}
$\overline{GBA}_0$–$\overline{GBA}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL DIRH	4	I	B output enables. When this signal is low the data on the B side, latched or active will be output to the A side. Signal associations are: $\overline{GBA}_0$ B_0–B_7 to A_0–A_7 $\overline{GBA}_1$ B_8–B_{15} to A_8–A_{15} $\overline{GBA}_2$ B_{16}–B_{23} to A_{16}–A_{23} $\overline{GBA}_3$ B_{24}–B_{31} to A_{24}–A_{31}
LEA	CPBA	1	I	Will latch in the 32-bit A bus.
LEB_0–LEB_3	$CPBA_0$ $CPBA_1$ $CPBA_2$ $CPBA_3$	4	I	Individual B byte latch enable. When in high state, B data is transparent and in low state B data is latched. LEB_0 H or L LEB_1 H or L LEB_2 H or L LEB_3 H or L

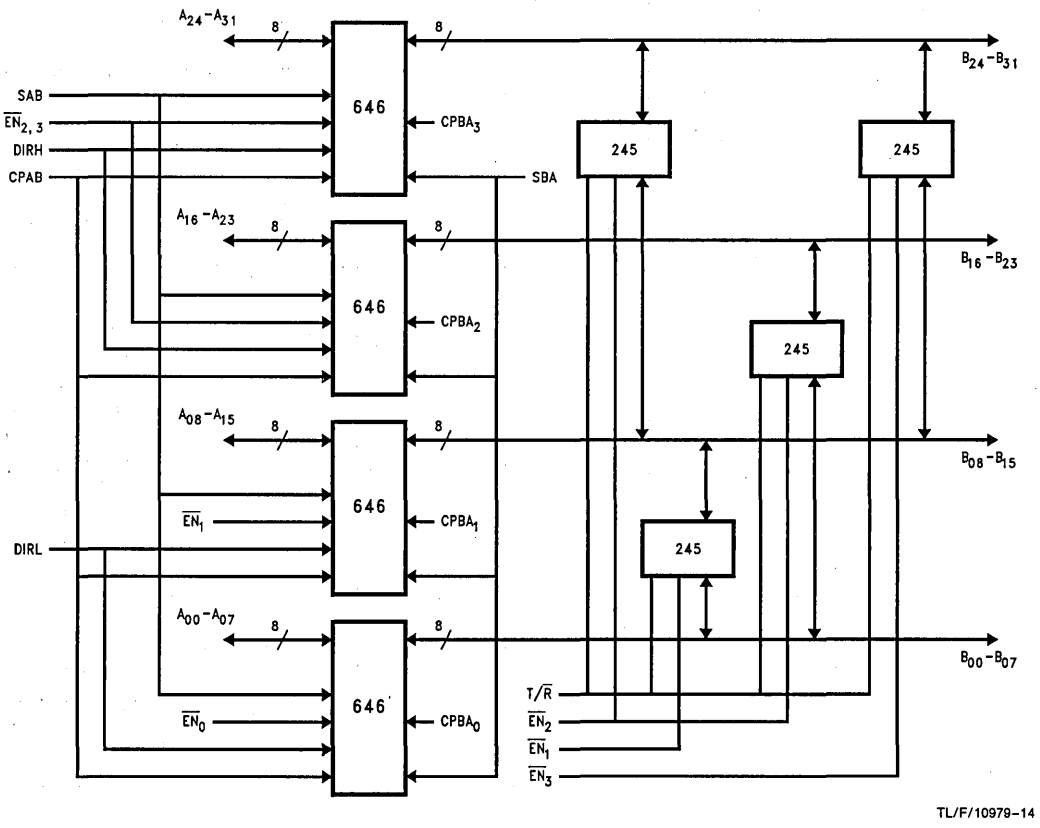
Application 3: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer
(Continued)

Detailed Pin Description (Continued)

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
$S0_0$–$S0_3$ $S1_0$–$S1_3$	T/$\overline{R}$ (245) $\overline{EN}_1$ (245) $\overline{EN}_2$ (245) $\overline{EN}_3$ (245)	8	I	These pins allow byte multiplexing, organized by byte. Each byte may be directed to any other byte by setting S0, S1 in a binary fashion to select the stimulus. For this application: $S1_0$=L $S0_0$=L A_0 selected at B_0 B_0 selected at A_0 $S1_0$=L $S0_0$=H A_1 selected at B_0 B_1 selected at A_0 $S1_0$=H $S0_0$=L A_2 selected at B_0 B_2 selected at A_0 $S1_0$=H $S0_0$=H A_3 selected at B_0 B_3 selected at A_0 $S1_1$=L $S0_1$=L A_0 selected at B_1 B_0 selected at A_1 $S1_1$=L $S0_1$=L A_1 selected at B_1 B_1 selected at A_1 $S1_1$=H $S0_1$=H A_3 selected at B_1 B_3 selected at A_1 $S1_2$=L $S0_2$=L A_0 selected at B_2 B_0 selected at A_2 $S1_2$=H $S0_2$=L A_2 selected at B_2 B_2 selected at A_2 $S1_3$=L $S0_3$=L A_0 selected at B_3 B_0 selected at A_3 $S1_3$=L $S0_3$=H A_1 selected at B_3 B_1 selected at A_3 $S1_3$=H $S0_3$=H A_3 selected at B_3 B_3 selected at A_3

Application 3: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer
(Continued)

Application 3: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer



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Application 4: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer with Parity Generator (A to B)/Check (B to A)

Detailed Pin Description

The following is a table that relates the pin names of the discrete implementation to the 'ACTQ3283T. Also listed are the number of pins, the type of each pin and the function performed.

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
A_0–A_7 A_8–A_{15} A_{16}–A_{23} A_{24}–A_{31}	AD_{00}–A_{07} AD_{08}–A_{15} AA_{00}–A_{07} AA_{08}–A_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from A bus to B bus the signal associations are: A_0–A_7 B_0–B_7 A_8–A_{15} B_8–B_{15} A_{16}–A_{23} B_{16}–B_{23} A_{24}–A_{31} B_{24}–B_{31}
B_0–B_7 B_8–B_{15} B_{16}–B_{23} B_{24}–B_{31}	BD_{00}–BD_{07} BD_{08}–BD_{15} BA_{00}–BA_{07} BA_{08}–BA_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from B bus to A bus the signal associations are: B_0–7 A_0–7 B_8–15 A_8–15 B_{16}–23 A_{16}–23 B_{24}–31 A_{24}–31
$BPAR_0$–$BPAR_3$	$BPAR_0$–$BPAR_3$	4	I/O	When the A side data is received a parity bit is generated for each byte and output on the B bus when active. When data is input on the B bus the parity bit is an input which is checked against an internally generated parity bit. $BPAR_0$ Byte 0 $BPAR_1$ Byte 1 $BPAR_2$ Byte 2 $BPAR_3$ Byte 3
$\overline{GAB}_0$–$\overline{GAB}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL DIRH	4	I	A output enables. When this signal is low the data on the A side, latched or active will be output to the B side. Signal associations are: $\overline{GAB}_0$ A_0–A_7 to B_0–B_7 $\overline{GAB}_1$ A_8–A_{15} to B_8–B_{15} $\overline{GAB}_2$ A_{16}–A_{23} to B_{16}–B_{23} $\overline{GAB}_3$ A_{24}–A_{31} to B_{24}–B_{31}
$\overline{GBA}_0$–$\overline{GBA}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL DIRH	4	I	B output enables. When this signal is low the data on the B side, latched or active will be output to the A side. Signal associations are: $\overline{GBA}_0$ B_0–B_7 to A_0–A_7 $\overline{GBA}_1$ B_8–B_{15} to A_8–A_{15} $\overline{GBA}_2$ B_{16}–B_{23} to A_{16}–A_{23} $\overline{GBA}_3$ B_{24}–B_{31} to A_{24}–A_{31}

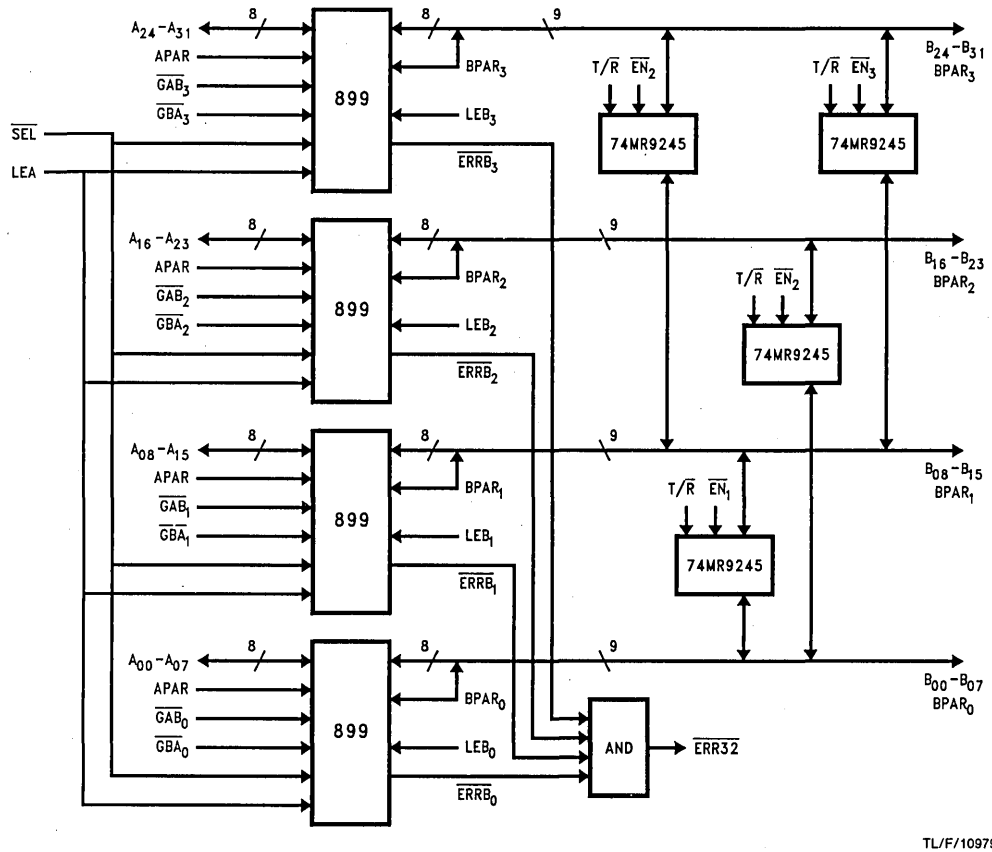
Application 4: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer with Parity Generator (A to B)/Check (B to A) (Continued)

Detailed Pin Description (Continued)

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
LEA	CPAB	1	I	Will latch in the 32-bit A bus.
$\overline{ERR32}$	$\overline{ERR32}$	1	O	Signal that indicates an error in one or more of the bytes.
LEB_0–LEB_3	$CPBA_0$ $CPBA_1$ $CPBA_2$ $CPBA_3$	4	I	Individual B byte latch enable. When in high state B data is transparent and when in low state B data is latched. LEB_0 H or L LEB_1 H or L LEB_2 H or L LEB_3 H or L
$S0_0$–$S0_3$ $S1_0$–$S1_3$	$T/\overline{R}$ (245) $\overline{EN}_1$ (245) $\overline{EN}_2$ (245) $\overline{EN}_3$ (245)	8	I	These pins allow byte multiplexing, organized by byte, Each byte may be directed to any other byte by setting S0, S1 in a binary fashion to select the stimulus. For this application: $S1_0$=L $S0_0$=L A_0 selected at B_0 B_0 selected at A_0 $S1_0$=L $S0_0$=H A_1 selected at B_0 B_1 selected at A_0 $S1_0$=H $S0_0$=L A_2 selected at B_0 B_2 selected at A_0 $S1_0$=H $S0_0$=H A_3 selected at B_0 B_3 selected at A_0 $S1_1$=L $S0_1$=L A_0 selected at B_1 B_0 selected at A_1 $S1_1$=L $S0_1$=L A_1 selected at B_1 B_1 selected at A_1 $S1_1$=H $S0_1$=H A_3 selected at B_1 B_3 selected at A_1 $S1_2$=L $S0_2$=L A_0 selected at B_2 B_0 selected at A_2 $S1_2$=L $S0_2$=L A_2 selected at B_2 B_2 selected at A_2 $S1_3$=L $S0_3$=L A_0 selected at B_3 B_0 selected at A_3 $S1_3$=L $S0_3$=H A_1 selected at B_3 B_1 selected at A_3 $S1_3$=H $S0_3$=H A_3 selected at B_3 B_3 selected at A_3

Application 4: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer with Parity Generator (A to B)/Check (B to A) (Continued)

Application 4: DWORD to WORD to BYTE Transfer with Parity



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/ = 1 byte

\ = 1 byte + 1 parity bit

6

National Semiconductor

74FR900
9-Bit, 3-Port Latchable Datapath Multiplexer

General Description

The 'FR900 is a data bus multiplexer routing any of three 9-bit ports to any other one of the three ports. Readback of data latched from any port onto itself is also possible. The 'FR900 maintains separate control of all latch-enable, output enable and select inputs for maximum flexibility. PINV allows inversion of the data from the C_B to A_B or B_B path. This is useful for control of the parity bit in systems diagnostics.

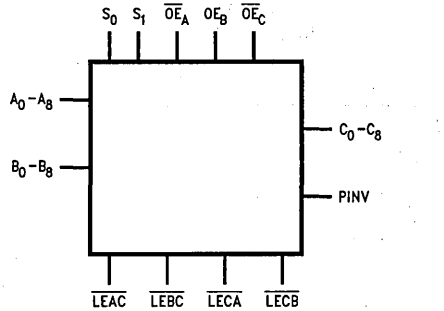
National's 74FR25900 includes 25Ω resistors in series with port A and B outputs. Resistors minimize undershoot and ringing which may damage or corrupt sensitive device inputs driven by these ports.

Features

- 9-bit data ports for systems carrying parity bits
- Readback capability for system self checks.
- Independent control lines for maximum flexibility
- Guaranteed multiple output switching and 250 pF load delays
- Outputs optimized for dynamic bus drive capability
- PINV parity control facilitates system diagnostics
- FR25900 resistor option for driving MOS inputs such as DRAM arrays
- Guaranteed 4000V ESD protection

Ordering Code: See Section 11

Logic Symbol



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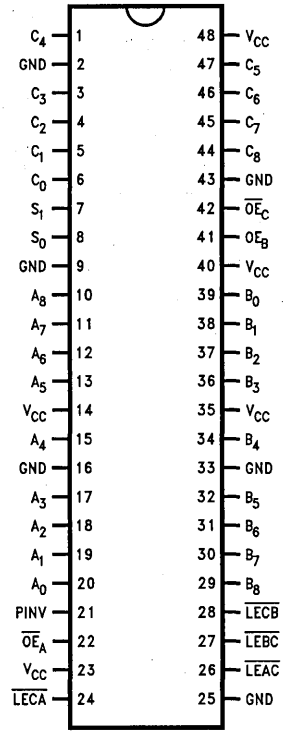
Connection Diagram

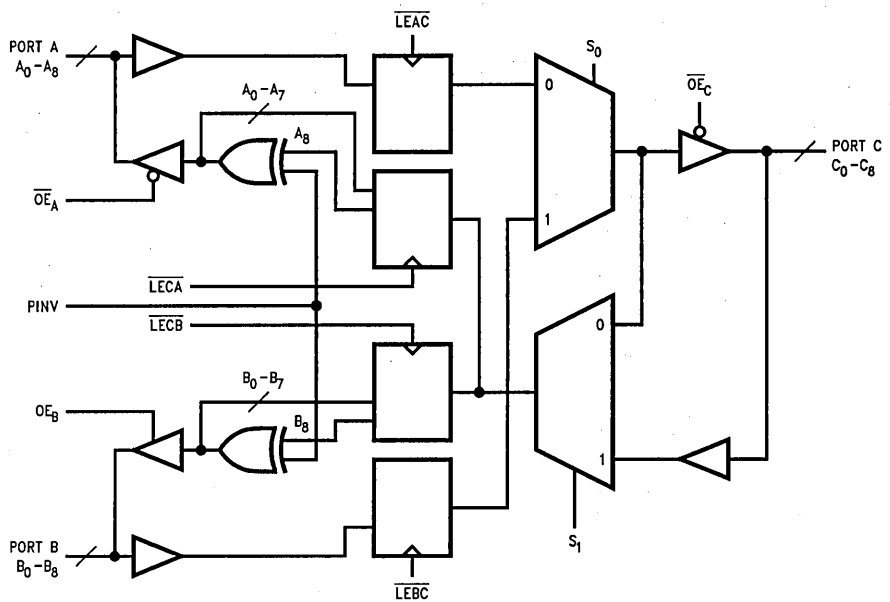


TL/F/10990–2

Pin Description

Pin Names	Description
LExx	Latch Enable Inputs
OE_x	Output Enable Inputs
PINV	Parity Invert Input
S_0, S_1	Select Inputs
A_0–A_8	Port A Inputs or TRI-STATE® Outputs
B_0–B_8	Port B Inputs or TRI-STATE® Outputs
C_0–C_8	Port C Inputs or TRI-STATE® Outputs

Logic Diagram



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Functional Description

The 'FR900 allows 9-bit data to be transferred from any of three 9-bit I/O ports to either of the two remaining I/O ports. The device employs latches in all paths for either transparent or synchronous operation. Readback capability from any port to itself is also possible.

Data transfer within the 'FR900 is controlled through use of the select (S_0 and S_1) and output-enable ($\overline{OE}_A$, OE_B and $\overline{OE}_C$) inputs as described in Table I. Additional control is available by use of the latch-enable inputs ($\overline{LEAC}$, $\overline{LECA}$, $\overline{LEBC}$, $\overline{LECB}$) allowing either synchronous or transparent transfers (see Table II). Table I indicates several readback conditions. By latching data on a given port and initiating the readback control configuration, previous data may be read for system verification or diagnostics. This mode may be useful in implementing system diagnostics.

Table I. Datapath Control

Inputs					Function
S_0	S_1	$\overline{OE}_A$	OE_B	$\overline{OE}_C$	
L	X	H	L	L	Port A to Port C
L	L	H	H	H	Port A to Port B
L	O	H	H	L	Port A to B+C
H	L	L	L	H	Port B to Port A
H	X	H	L	L	Port B to Port C
H	O	L	L	L	Port B to A+C
X	H	L	L	H	Port C to Port A
X	H	H	H	H	Port C to Port B
X	H	L	H	H	Port C to A+B
X	X	H	L	H	Outputs Disabled
L	L	L	X	X	(Readback to A)*
L	H	L	X	L	(Readback to A or C)*
H	L	X	H	X	(Readback to B)*
H	H	X	H	L	(Readback to B or C)*

*Readback operation in latched mode only. Transparent operation could result in unpredictable results.

Data at the port to be readback must be latched prior to enabling the outputs on that port. If this is not done, a closed data loop will result causing possible data integrity problems. Note that the A and B ports allow readback without affecting any other port. Port C, however, requires interruption of either port A or B to complete its readback path.

PINV controls inversion of the C_8 bit. A low on PINV allows C_8 data to pass unaltered. A high causes inversion of the data. See Table III. This feature allows forcing of parity errors for use in system diagnostics. This is particularly helpful in Intel '486 processor designs as the '486 does not provide odd/even parity selection internally.

Table II. Latch-Enable Control

LEXX	Input	Output
L	L	L
L	H	H
H	X	Q_0

Table III. PINV Control

PINV	C_8	A_8 or B_8
L	L	L
L	H	H
H	L	H
H	H	L

Key:

L = Low Voltage

H = High Voltage Level

Q_0 = Output state prior to LEXX low to high transition

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in High State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in Low State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74FR			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input High Voltage	2.0			V		Recognized High Signal
V_{IL}	Input Low Voltage			0.8	V		Recognized Low Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output High Voltage	2.4			V	Min	I_{OH} = −3 mA (A_n, B_n, C_n)
		2.0			V	Min	I_{OH} = −15 mA (A_n, B_n, C_n)
V_{OL}	Output Low Voltage			0.50	V	Min	I_{OL} = 24 mA (A_n, B_n, C_n)
I_{IH}	Input High Current			5	μA	Max	V_{IN} = 2.7V (Control Inputs)
I_{BVI}	Input High Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Control Inputs)
I_{BVIT}	Input High Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n, C_n)
I_{IL}	Input Low Current			−150	μA	Max	V_{IN} = 0.5V (Control Inputs)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, All Other Pins Grounded
I_{OD}	Output Circuit Leakage Test			3.75	V	0.0	V_{IOD} = 150 mV, All Other Pins Grounded
$I_{IH} + I_{OZH}$	Output Leakage Current			25	μA	Max	V_{OUT} = 2.7V (A_n, B_n, C_n)
$I_{IIL} + I_{OZL}$	Output Leakage Current			−150	μA	Max	V_{OUT} = 0.5V (A_n, B_n, C_n)
I_{OS}	Output Short Circuit Current	−100		−225	mA	Max	V_{OUT} = 0.0V (A_n, B_n, C_n)
I_{CEX}	Output High Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n, C_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V (A_n, B_n, C_n)
I_{CCH}	Power Supply Current		115	150	mA	Max	All Outputs High*
I_{CCL}	Power Supply Current		170	200	mA	Max	All Outputs Low*
I_{CCZ}	Power Supply Current		147	175	mA	Max	Outputs in TRI-STATE

*2 ports active only

AC Electrical Characteristics: See Section 8 for waveforms and load configurations

Symbol	Parameter	74FR $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74FR $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_n C_n to A_n or B_n	2.0	4.2	7.0	2.0	7.0	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay C_8 to A_8 or B_8 (PINV High)	2.5	4.8	7.5	2.5	7.5	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n, B_n to A_n	4.5	6.4	10.0	4.5	10.0	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAC}$ to C_n, $\overline{LEBC}$ to C_n	4.5	6.8	10.0	4.5	10.0	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LECA}$ to A_n, $\overline{LECB}$ to B_n	3.0	6.0	9.5	3.0	9.5	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay S_0 to C_n	3.0	6.0	10.0	3.0	10.0	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay S_1 to A_n or B_n	3.5	6.5	11.0	3.5	11.0	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay PINV to A_8 or B_8	2.0	5.0	9.0	2.0	9.0	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time A_n, C_n	2.0	4.0	6.5	2.0	6.5	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time A_n, C_n	1.5	4.0	6.0	1.5	6.0	ns	8-5
t_{PZH} t_{PZL}	Output Enable Time B_n	2.0	5.0	7.0	2.0	7.0	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time B_n	2.0	5.0	7.0	2.0	7.0	ns	8-5

AC Operating Requirements: See Section 8 for waveforms and load configurations

Symbol	Parameter	74FR $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74FR $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, High or Low A_n to $\overline{LEAC}$, B_n to $\overline{LEBC}$	4.0	2.0		4.0		ns	8-6
$t_h(H)$ $t_h(L)$	Hold Time, High or Low A_n to $\overline{LEAC}$, B_n to $\overline{LEBC}$	1.0	−2.0		1.0		ns	8-6
$t_s(H)$ $t_s(L)$	Setup Time, High or Low C_n to $\overline{LECA}$ or $\overline{LECB}$	3.0	1.0		3.0		ns	8-6
$t_h(H)$ $t_h(L)$	Hold Time, High or Low C_n to $\overline{LECA}$ or $\overline{LECB}$	1.0	−1.0		1.0		ns	8-6
$t_w(H)$	$\overline{LE}$ Pulse Width Low	8.0	4.0		8.0		ns	8-4

Extended AC Electrical Characteristics: See Section 8 for waveforms and load configurations

Symbol	Parameter	74FR T_A = Comm V_{CC} = Comm C_L = 50 pF Nine Outputs Switching (Note 1)		74FR T_A = Comm V_{CC} = Comm C_L = 250 pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_n C_n to A_n or B_n	2.0	9.0	2.5	10.5	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay C_8 to A_8 or B_8 (PINV High)	N.A.	N.A.	3.5	11.0	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n, B_n to A_n	4.5	12.0	5.5	13.5	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAC}$ to C_n, $\overline{LEBC}$ to C_n	4.5	12.0	5.5	13.5	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LECA}$ to A_n, $\overline{LECB}$ to B_n	3.0	11.5	4.0	13.5	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay S_0 to C_n	3.0	11.0	3.0	14.0	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay S_1 to A_n or B_n	3.5	12.0	4.5	15.0	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay PINV to A_8 or B_8	N.A.	N.A.	2.5	12.0	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time A_n, C_n	2.0	8.0			ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time A_n, C_n	1.5	6.0			ns	8-5
t_{PZH} t_{PZL}	Output Enable Time B_n	2.0	8.0			ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time B_n	2.0	7.0			ns	8-5

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all low-to-high, high-to-low, TRI-STATE-to-high, etc.

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors standard AC load. This specification pertains to single output switching only.

Note: N.A. = Not Applicable

National Semiconductor

74FR25900
9-Bit, 3-Port Latchable Datapath Multiplexer with 25Ω Output Series Resistors

General Description

The 'FR25900 is a data bus multiplexer routing any of three 9-bit ports to any other one of the three ports. Readback of data latched from any port onto itself is also possible. The 'FR25900 maintains separate control of all latch-enable, output enable and select inputs for maximum flexibility. PINV allows inversion of the data from the C_8 to A_8 or B_8 path. This is useful for control of the parity bit in systems diagnostics.

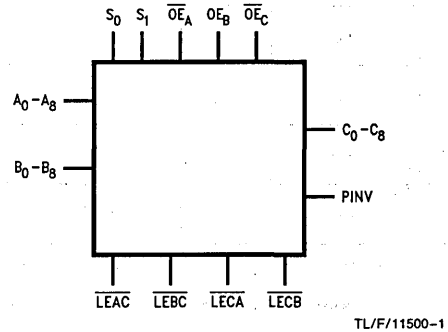
This device includes 25Ω resistors in series with port A and B outputs. Resistors minimize undershoot and ringing which may damage or corrupt sensitive device inputs driven by these ports.

Features

- 25Ω series resistors in the port A and B outputs eliminate the need for external resistors when driving MOS inputs such as DRAM arrays
- 9-bit data ports for systems carrying parity bits
- Readback capability for system self checks.
- Independent control lines for maximum flexibility
- Guaranteed multiple output switching and 250 pF load delays
- Outputs optimized for dynamic bus drive capability
- PINV parity control facilitates system diagnostics
- 'FR900 option available without output series resistors

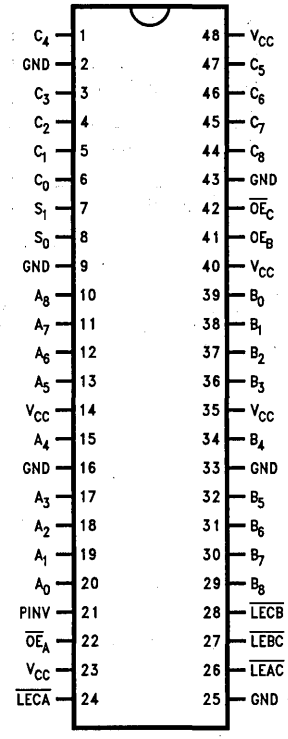
Ordering Code: See Section 11

Logic Symbol



TL/F/11500–1

Connection Diagram

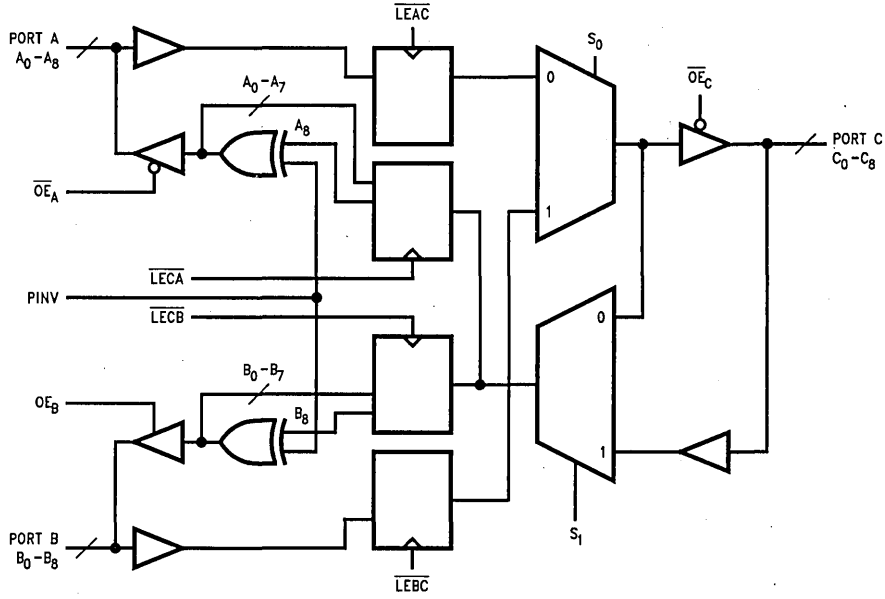


TL/F/11500–2

Pin Description

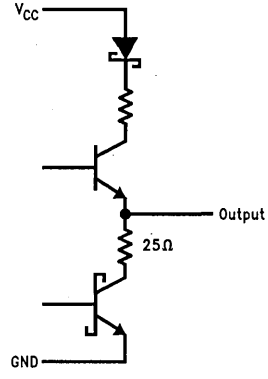
Pin Names	Description
LExx	Latch Enable Inputs
OE_x	Output Enable Inputs
PINV	Parity Invert Input
S_0, S_1	Select Inputs
A_0–A_8	Port A Inputs or TRI-STATE® Outputs
B_0–B_8	Port B Inputs or TRI-STATE® Outputs
C_0–C_8	Port C Inputs or TRI-STATE® Outputs

Logic Diagram



TL/F/11500–3

Schematic of A and B Port Outputs



TL/F/11500–4

Functional Description

The 'FR25900 allows 9-bit data to be transferred from any of three 9-bit I/O ports to either of the two remaining I/O ports. The device employs latches in all paths for either transparent or synchronous operation. Readback capability from any port to itself is also possible.

Data transfer within the 'FR25900 is controlled through use of the select (S_0 and S_1) and output-enable ($\overline{OE}_A$, OE_B and $\overline{OE}_C$) inputs as described in Table I. Additional control is available by use of the latch-enable inputs ($\overline{LEAC}$, $\overline{LECA}$, $\overline{LEBC}$, $\overline{LECB}$) allowing either synchronous or transparent transfers (see Table II). Table I indicates several readback conditions. By latching data on a given port and initiating the readback control configuration, previous data may be read for system verification or diagnostics. This mode may be useful in implementing system diagnostics.

Table I. Datapath Control

Inputs					Function
S_0	S_1	$\overline{OE}_A$	OE_B	$\overline{OE}_C$	
L	X	H	L	L	Port A to Port C
L	L	H	H	H	Port A to Port B
L	O	H	H	L	Port A to B+C
H	L	L	L	H	Port B to Port A
H	X	H	L	L	Port B to Port C
H	O	L	L	L	Port B to A+C
X	H	L	L	H	Port C to Port A
X	H	H	H	H	Port C to Port B
X	H	L	H	H	Port C to A+B
X	X	H	L	H	Outputs Disabled
L	L	L	X	X	(Readback to A)*
L	H	L	X	L	(Readback to A or C)*
H	L	X	H	X	(Readback to B)*
H	H	X	H	L	(Readback to B or C)*

*Readback operation in latched mode only. Transparent operation could result in unpredictable results.

Data at the port to be readback must be latched prior to enabling the outputs on that port. If this is not done, a closed data loop will result causing possible data integrity problems. Note that the A and B ports allow readback without affecting any other port. Port C, however, requires interruption of either port A or B to complete its readback path.

PINV controls inversion of the C_8 bit. A low on PINV allows C_8 data to pass unaltered. A high causes inversion of the data. See Table III. This feature allows forcing of parity errors for use in system diagnostics. This is particularly helpful in Intel '486 processor designs as the '486 does not provide odd/even parity selection internally.

Table II. Latch-Enable Control

LEXX	Input	Output
L	L	L
L	H	H
H	X	Q_0

Table III. PINV Control

PINV	C_8	A_8 or B_8
L	L	L
L	H	H
H	L	H
H	H	L

Key:

L = Low Voltage

H = High Voltage Level

Q_0 = Output state prior to LEXX low to high transition

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in High State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in Low State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74FR			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input High Voltage	2.0			V		Recognized High Signal
V_{IL}	Input Low Voltage			0.8	V		Recognized Low Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output High Voltage	2.4			V	Min	I_{OH} = −3 mA (A_n, B_n, C_n)
		2.0			V	Min	I_{OH} = −15 mA (A_n, B_n, C_n)
V_{OL}	Output Low Voltage			0.50	V	Min	I_{OL} = 1 mA (A_n, B_n)
				0.75	V	Min	I_{OL} = 12 mA (A_n, B_n)
				0.50	V	Min	I_{OL} = 24 mA (C_n)
I_{IH}	Input High Current			5	μA	Max	V_{IN} = 2.7V (Control Inputs)
I_{BVI}	Input High Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Control Inputs)
I_{BVIT}	Input High Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n, C_n)
I_{IL}	Input Low Current			−150	μA	Max	V_{IN} = 0.5V (Control Inputs)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, All Other Pins Grounded
I_{OD}	Output Circuit Leakage Test			3.75	V	0.0	V_{IOD} = 150 mV, All Other Pins Grounded
$I_{IH} + I_{OZH}$	Output Leakage Current			25	μA	Max	V_{OUT} = 2.7V (A_n, B_n, C_n)
$I_{IIL} + I_{OZL}$	Output Leakage Current			−150	μA	Max	V_{OUT} = 0.5V (A_n, B_n, C_n)
I_{OS}	Output Short Circuit Current	−100		−225	mA	Max	V_{OUT} = 0.0V (A_n, B_n, C_n)
I_{CEX}	Output High Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n, C_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V (A_n, B_n, C_n)
I_{CCH}	Power Supply Current		115	150	mA	Max	All Outputs High*
I_{CCL}	Power Supply Current		170	200	mA	Max	All Outputs Low*
I_{CCZ}	Power Supply Current		147	175	mA	Max	Outputs in TRI-STATE

*2 ports active only

AC Electrical Characteristics: See Section 2 for waveforms and load configurations

Symbol	Parameter	74FR $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74FR $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_n C_n to A_n or B_n	2.0	4.7	7.5	2.0	7.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay C_8 to A_8 or B_8 (PINV High)	2.5	4.8	7.5	2.5	7.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n, B_n to A_n	4.5	7.0	11.5	4.5	11.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAC}$ to C_n, $\overline{LEBC}$ to C_n	4.5	6.8	10.0	4.5	10.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LECA}$ to A_n, $\overline{LECB}$ to B_n	3.5	6.0	10.0	3.5	10.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay S_0 to C_n	3.0	6.0	10.0	3.0	10.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay S_1 to A_n or B_n	4.0	7.0	11.5	4.0	11.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay PINV to A_8 or B_8	2.5	5.5	9.5	2.5	9.5	ns	2-3
t_{PZH} t_{PZL}	Output Enable Time C_n	1.5	4.0	6.5	1.5	6.5	ns	2-5
t_{PHZ} t_{PLZ}	Output Disable Time C_n	1.5	4.0	6.0	1.5	6.0	ns	2-5
t_{PZH} t_{PZL}	Output Enable Time A_n, B_n	1.5	6.0	8.0	1.5	8.0	ns	2-5
t_{PHZ} t_{PLZ}	Output Disable Time A_n, B_n	1.5	5.0	7.0	1.5	7.0	ns	2-5

AC Operating Requirements: See Section 2 for waveforms and load configurations

Symbol	Parameter	74FR $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74FR $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, High or Low A_n to $\overline{LEAC}$, B_n to $\overline{LEBC}$	4.5	2.5		4.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, High or Low A_n to $\overline{LEAC}$, B_n to $\overline{LEBC}$	1.0	−1.5		1.0		ns	2-6
$t_s(H)$ $t_s(L)$	Setup Time, High or Low C_n to $\overline{LECA}$ or $\overline{LECB}$	3.0	1.0		3.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, High or Low C_n to $\overline{LECA}$ or $\overline{LECB}$	1.0	−1.0		1.0		ns	2-6
$t_w(H)$	$\overline{LE}$ Pulse Width Low	8.0	4.0		8.0		ns	2-4

Extended AC Electrical Characteristics: See Section 2 for waveforms and load configurations

Symbol	Parameter	74FR T_A = Comm V_{CC} = Comm C_L = 50 pF Nine Outputs Switching (Note 1)		74FR T_A = Comm V_{CC} = Comm C_L = 250 pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_n C_n to A_n or B_n	2.0	11.5	4.0	12.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay C_8 to A_8 or B_8 (PINV High)	N.A.	N.A.	5.5	13.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n, B_n to A_n	4.5	16.0	6.0	16.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAC}$ to C_n, $\overline{LEBC}$ to C_n	4.5	13.0	5.5	13.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LECA}$ to A_n, $\overline{LECB}$ to B_n	3.5	11.5	5.5	14.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay S_0 to C_n	3.0	11.0	3.0	14.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay S_1 to A_n or B_n	4.0	16.5	6.5	16.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay PINV to A_8 or B_8	N.A.	N.A.	4.5	14.5	ns	2-3
t_{PZH} t_{PZL}	Output Enable Time C_n	1.5	8.0			ns	2-5
t_{PHZ} t_{PLZ}	Output Disable Time C_n	1.5	6.0			ns	2-5
t_{PZH} t_{PZL}	Output Enable Time A_n, B_n	1.5	8.0			ns	2-5
t_{PHZ} t_{PLZ}	Output Disable Time A_n, B_n	1.5	7.0			ns	2-5

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all low-to-high, high-to-low, TRI-STATE-to-high, etc.

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors standard AC load. This specification pertains to single output switching only.

Note: N.A. = Not Applicable

Section 7

BCT Description and Family Characteristics

Section 7 Contents

National Semiconductor

BCT Description and Family Characteristics

National now offers BCT BiCMOS logic for bus driving and interfacing in the highest performance systems.

The role of logic is evolving. In traditional logic families, hundreds of SSI/MSI/LSI building block functions enabled engineers to design entire computers from discrete logic ICs. Dramatic technological breakthroughs are changing this environment. Many system designs have migrated from implementations based on general purpose logic to VLSI-based ASICs and dedicated-function VLSI, shifting the role of logic toward bus and timing support functions.

With greater emphasis on bus interface functions (such as buffers, transceivers, and clock drivers), system designers require the ability and flexibility to select logic products that provide the appropriate speed, power, noise, reliability, supply assurance, and cost that's best for the task at hand. System designers often use a combination of several logic families that will contribute the best set of characteristics for optimum system performance. In other instances, logic devices are being designed for circuit functions that are not efficiently performed by larger VLSI components.

For highest performance applications (30 MHz to 66 MHz range), National's new BCT logic together with FASTr™ (see note) fill the need for faster and more effective bus-interface functions. Offering very high speed, BCT is recommended where lower system power takes precedence over speed. FASTr is particularly attractive in applications where absolute speed is the primary concern. Complimentary technologies, the combination is ideal for high-performance bus and clock distribution applications in personal/desktop computers, PC LAN servers, PC peripherals, workstations, telecommunication switches/multiplexers, fiber optic equipment, and automatic test equipment (ATE).

BCT Minimizes Power Consumption While Improving Performance

While National's BCT line of BiCMOS logic is pin and functionally compatible with the competitive BCT line, it also offers the added features of lower power consumption as well as a number of additional guaranteed specifications. As shown below, competitive BCT products consume more power than NSC's BCT.

With a source-current capability of 15 mA and a sink-current capability of 64 mA, BCT devices are designed for driving heavily loaded busses.

More Specifications for Tighter System Timing

NSC guarantees more AC specifications than competitive BCT products, including multiple output switching (MOS) delay, 250 pF AC delay, and output skew. All are key in helping system designers tighten timing guardbands. Using these guaranteed values rather than *rule of thumb,* designers obtain greater precision in the propagation delay budget.

Worst-Case Power Consumption Comparison: National's 'BCT240 vs. Competitive 'BCT240

Parameter	National's BCT (Guaranteed)	Competitive BCT (Guaranteed)
I_{CCH}	18 mA	31 mA
I_{CCL}	69 mA	71 mA
I_{CCZ}	9 mA	9 mA

Note: NSC's FASTr logic is an enhanced version of FAST®. FASTr is the highest speed bus driving/interfacing TTL logic.

Guaranteed National 74BCT240 Specifications (V_{CC} = 4.5V to 5.5V)

Data to Outputs	
T_{PLH}	0.5 ns to 5.6 ns
T_{PHL}	0.4 ns to 4.0 ns
Output Enable Time	
T_{PZH}	1.0 ns to 8.8 ns
T_{PZL}	1.0 ns to 10.5 ns
Output Disable Time	
T_{PHZ}	1.0 ns to 8.1 ns
T_{PLZ}	1.0 ns to 9.5 ns
Power Supply Current	
I_{CCH}	18 mA
I_{CCL}	69 mA
I_{CCZ}	9 mA

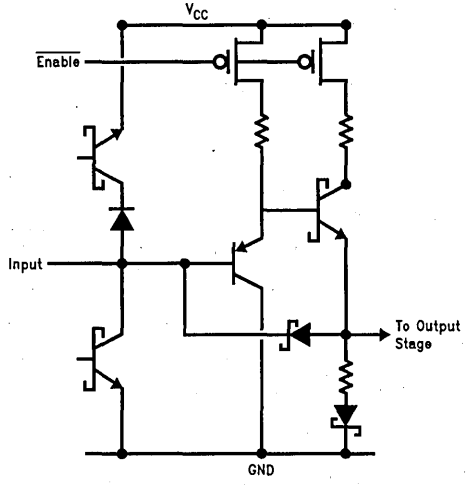
Because systems are requiring ever increasing clock rates, National offers BCT devices with a guaranteed output skew specifications. Devices having tight skew specifications improve timing efficiency in critical timing paths such as those for clock distribution. Many of National's advanced logic devices guarantee less than 1 ns critical path output skew. (See *Figure 1* for typical BCT input and output circuits.)

Beyond use in new system designs, BCT logic is ideal in bipolar-based systems that have marginal power problems. Replacing the bipolar logic with BCT may resolve existing power issues (refer to *Figure 2*). BCT logic offers system advantages where:

- Typical propagation delays of 2 ns–3 ns are required
- Power is a concern
- Percentage of TRI-STATE® times are high
- Low noise levels are major criteria
- Where hot insertion may be an issue

More Specifications for Tighter System Timing (Continued)

Typical Input Circuit



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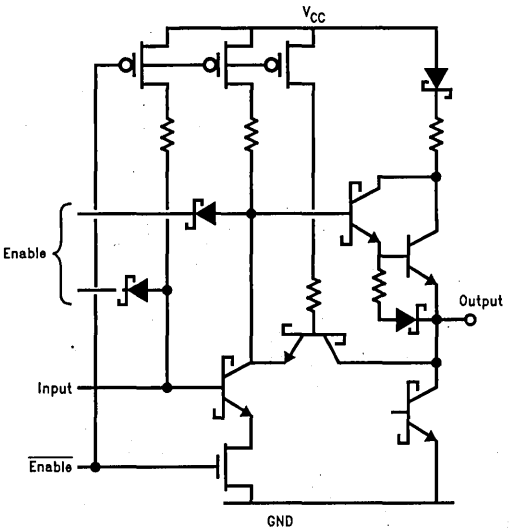
Typical Output Circuit



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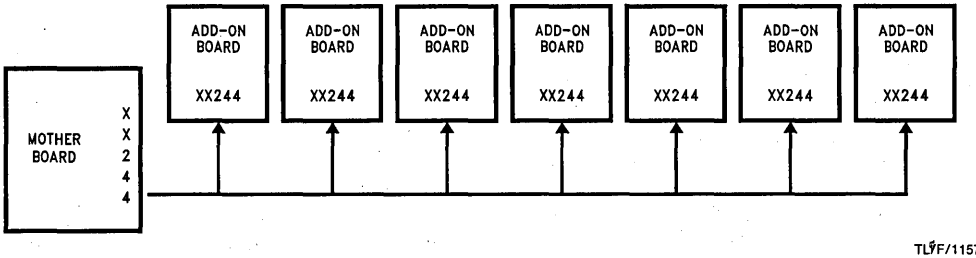
Note: These diagrams represent typical input/output circuits and do not necessarily model the entire actual circuits.

FIGURE 1. Typical BiCMOS Circuits



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X No. of Boards = 8 (2 Active at Any One Time)

	BCT244	ALS244	AS244	F244
I_{CCH}	38	15	34	60
I_{CCL}	66	24	90	90
I_{CC} Active (50% duty cycle)	52	19	62	75
I_{CC} Two Active Boards	104	39	124	150
I_{CCZ}	10	27	54	90
(X-2) I_{CCZ}	60	162	324	540
I_{CC} Total	164	201	448	690
Prop Delay	5.5	10	6.2	6.5
% of BCT I_{CC}	**X**	**122%**	**273%**	**421%**
% of BCT Prop Delay	**X**	**182%**	**113%**	**118%**

FIGURE 2. National's BCT Devices Compare Favorably with Competitive Solutions

Guarantees for Power Down and Hot Insertion

Power down and hot insertion are areas of logic design that are receiving added attention.

National's BCT guarantees high impedance when powered down (specified by I_{ZZ}). This specification guarantees that a TRI-STATE device will not load down a bus to which it is attached when powered down—a very important consideration in applications where power is a concern.

NSC 74BCT240 Compared With the Competition

DC Parameter	Guaranteed by NSC	Guaranteed by Competition
Improvements:		
I_{CCH}	18 mA	31 mA
I_{CCL}	69 mA	71 mA
I_{IH}	5 μA	20 μA
I_L	−250 μA	−1 mA
I_{OZH}	20 μA	50 μA
I_{OZL}	−20 μA	−50 μA
Additional Specifications:		
I_{ZZ}	100 μA	
V_{ID}	4.75V	
I_{CEX}	50 μA	
Latchup	500 mA	
Electrostatic Discharge	4,000V (10,000V typical)	

For example, laptops often use a sleep mode for power conservation. If a device does not have high impedance in a powered down situation, sleep mode can only occur by stopping the clock. Both NSC's BCT and FASTr guarantee high impedance in power down. By nature of their technology, products with CMOS inputs or outputs have difficulties with high impedance in power down capability.

Also featured with BCT and FASTr logic families is hot insertion capability. This allows boards to be pulled from or inserted into systems that are powered up.

National's BCT V_{ID} specification guarantees that a high resistance short will not occur across the input diode. This specification combined with guaranteed ESD and latchup protection indicate NSC's BCT hot insertion capability. Devices with CMOS inputs or outputs have difficulty with hot insertion capability. As with power down, hot insertion is more familiar to designers of bipolar systems than those designing CMOS systems.

National is the only BiCMOS logic supplier to guarantee both high impedance in power down and hot insertion capability reliability features.

To further enhance this hot insertion capability, National's BCT and FASTr products guarantee extremely high ESD and latchup specifications, enabling these devics to tolerate high voltages and current transients on all pins.

Using National's Complimentary High-Performance Bus Logic Families

BCT and FASTr fill the need for the faster bus-interface functions required by many of today's most demanding applications. Implemented on different silicon technologies (BiCMOS and bipolar), their power and noise attributes define their market applications.

- BCT is best suited where very high performance is required and active duty cycles are relatively low. Most of today's high-performance data buses for non-portable equipment are excellent candidates. An application with a lower enable duty cycle can realize substantial power savings by using BCT, such as a data bus to main memory. Designers who need to minimize their system's noise sensitivity—ground bounce, undershoot, ringing, crosstalk—and require fast switching speed at the interface would choose BCT logic.
- FASTr and BCT compliment each other as part of a total system solution. Both lines consist of logic functions that interface high-performance buses. Their TTL I/O characteristics closely match one another. Process technology and circuit design are similar. The two product types can sit side by side on a circuit board, enabling optimum speed/power performance. (Refer to *Figure 3:* FASTr and BCT Used Together to Optimize a Cache Motherboard.)

Using National's Complimentary High-Performance Bus Logic Families
(Continued)

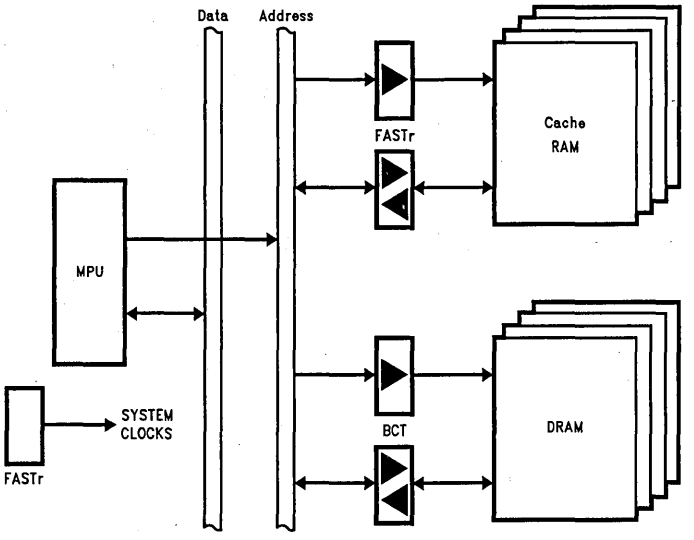

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FIGURE 3. FASTr and BCT Used Together to Optimize a Cache Motherboard

BCT Features and Benefits

FEATURE	BENEFITS
8-bit products are pin-for-pin compatible (function, part number, pinout) with standard 74 input/output logic levels	Allows easy upgrades in existing designs; designers are fully accustomed with nomenclature for easy design
Drop-in replacement for TI BCT	Second source with additional specifications
Guaranteed specifications for: • Pin-to-pin skew; 50 pF multiple output switching T_{PD} = 8 outputs switching T_{PD} = 250 pF capacitive load • ESD immunity (4,000V minimum)* • Latchup immunity	System designers have added tools to get the most from their high-performance designs
Very high speed	Higher incoming PPM quality parts; reduces walking wounded for less field failures; increases quality and reliability
Power dissipation less than FAST; noise performance similar to FAST	Minimum delay degradation in capacitive and transmission line environments; reduces noise and optimizes performance
Available in PDIP and SOIC	Allows higher preformance systems Even lower power for power-sensitive applications Industry-standard packaging

***Note:** ESD 2,000 minimum for 'BCT125 and 'BCT573.

Section 8

BCT Ratings, Specifications and Waveforms

Section 8 Contents

National Semiconductor

BiCMOS Ratings, Specifications and Waveforms

Glossary

Currents—Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specifed as absolute values.

I_{CC} Supply Current—The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst-case operation.

I_{IH} Input HIGH Current—The current flowing into an input when a specified HIGH voltage is applied.

I_{IL} Input LOW Current—The current flowing out of an input when a specified LOW voltage is applied.

I_{OH} Output HIGH Current—The current flowing out of the output when it is in the HIGH state. For a turned-off open-collector output with a specified HIGH output voltage applied, the I_{OH} is the leakage current.

I_{OL} Output LOW Current—The current flowing into an output when it is in the LOW state.

I_{OS} Output Short Circuit Current—The current flowing out of a HIGH-state output when that output is short circuited to ground (or other specified potential).

I_{OZH} Output OFF Current HIGH—The current flowing into a disabled TRI-STATE® output with a specified HIGH output voltage applied.

I_{OZL} Output OFF Current LOW—The current flowing out of a disabled TRI-STATE output with a specified LOW output voltage applied.

Voltages—All voltages are referenced to the ground pin. Negative voltage limits are specified as absolute values (i.e., $-10.0V$ is greater than $-1.0V$).

V_{CC} Supply Voltage—The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

V_{CD} (Max) Input Clamp Diode Voltage—The most negative voltage at an input when a specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode, intended to clamp negative ringing at the input terminal.

V_{IH} Input HIGH Voltage—The range of input voltages that represents a logic HIGH in the system.

V_{IH} (Min) Minimum Input HIGH Voltage—The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} Input LOW Voltage—The range of input voltages that represent a logic LOW in the system

V_{IL} (Max) Maximum Input LOW Voltage—The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

V_{OH} (Min) Output HIGH Voltage—The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

V_{OL} (Max) Output LOW Voltage—The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.

AC Switching Parameters

f_{max} Toggle Frequency/Operating Frequency—The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} Propagation Delay Time—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation Delay Time—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_w Pulse Width—The time between 1.5V amplitude points on the leading and trailing edges of a pulse.

t_h Hold Time—The interval immediately following the active transition of the timing pulse (usually the clock pulse) of following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s Setup Time—The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} Output Disable Time (of a TRI-STATE Output) from HIGH Level—The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} Output Disable Time (of a TRI-STATE Output) from LOW Level—The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

AC Switching Parameter (Continued)

t_{PZH} Output Enable Time (of a TRI-STATE Output) to a HIGH Level—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} Output Enable Time (of a TRI-STATE Output) to a LOW Level—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW level.

AC Loading and Waveforms

Figure 1 shows the AC loading circuit used in characterizing and specifying propagation delays of all BCT devices, unless otherwise specified in the data sheet of a specific device. The use of this load, which differs somewhat from previous practice, provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance, and implied the use of high impedance, high frequency scope probes. BCT circuits changed to 50 pF of capacitance allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the loading to be expected in average applications and thus gives the designer more useful delay figures. The net effect of the change in AC load is to increase the observed propagation delay by an average of about 1 ns.

The 500Ω resistor to ground, in *Figure 1*, acts as a ballast, to slightly load the totem-pole pull-up and limit the quiescent HIGH-state voltage to about +3.5V. Otherwise, an output would rise quickly to about +3.5V but then continue to rise very slowly to about +4.4V. On the subsequent HIGH-to-LOW transition the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the LOW state. Perhaps more importantly, the 500Ω resistor to ground can be a high frequency passive probe for a sampling scope, which costs much less than the equivalent high impedance probe. Alternatively, the 500Ω load to ground can simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Also shown in *Figure 1* is a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with open-collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establish a quiescent HIGH level of +3.5V, which correlates with the HIGH level discussed in the preceding paragraph.

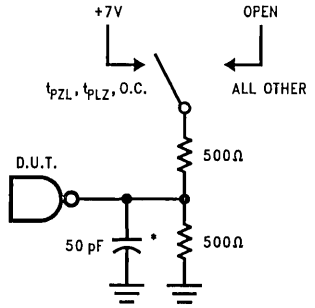
Figure 5 shows that the Disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., LOW for t_{PLZ} or HIGH for t_{PHZ}), compared to a ΔV of 0.5V used in previous practice. This change enhances the repeatability of measurements and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the rising or falling waveform is RC-controlled, the first 0.3V of change is more linear than the first 0.5V and is less susceptible to external influences. More importantly, perhaps, from the system designer's point of view, a ΔV of 0.3V is adequate to ensure that a device output has turned OFF; measuring to a ΔV of 0.5V merely exaggerates the apparent Disable time and thus penalizes system performance, since the designer must use the Enable and Disable times to devise worst-case timing signals to ensure that the output of one device is disabled before that of another device is enabled.

Figure 2 describes the input signal voltages recommended for use when testing BCT circuits. The AC input signal levels follow industry convention of V_{IN} switching 0 to 3 volts. DC low input levels are typically 0 to V_{IL}, and high input levels are typically V_{IH} to V_{CC}. Input thresholds are guaranteed during V_{OL} and V_{OH} tests. High level noise immunity is the difference between V_{OH} and V_{IH}. Low level noise immunity is the difference between V_{IL} and V_{OL}. Noise-free V_{IH} or V_{IL} levels should not induce a switch on the appropriate output of the BCT device. When testing in an automatic test environment, extreme caution should be taken to ensure that input levels plus noise do not go into the transition region.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5 ns and signal swing of 0V to +3.0V. Rise and fall times ≤ 1 ns should be used for testing f_{max} or pulse width. A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Precautions should be taken to prevent damage to devices by electrostatic charge. Static charge tends to accumulate on insulated surfaces, such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to BCT devices it may be necessary for individuals to wear a grounded wrist strap when handling devices.

AC Loading and Waveforms (Continued)



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*Includes jig and probe capacitance

FIGURE 1. Test Load

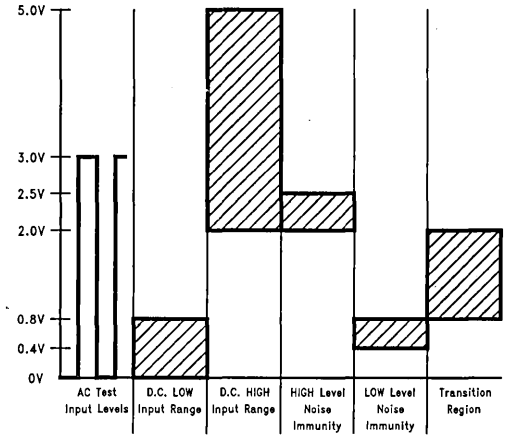

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FIGURE 2. Test Input Signal Levels

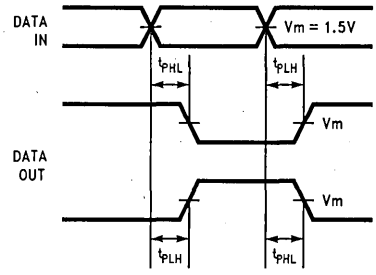

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FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

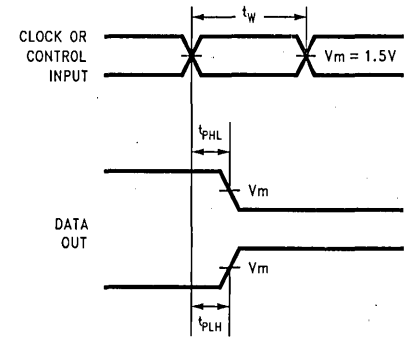

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FIGURE 4. Propagation Delay, Pulse Width Waveforms

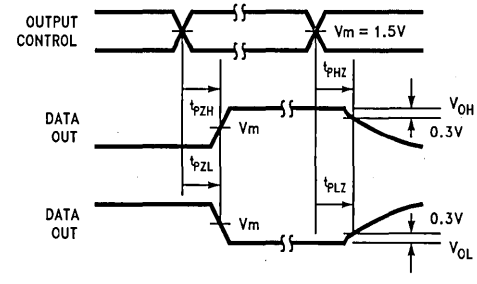

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FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

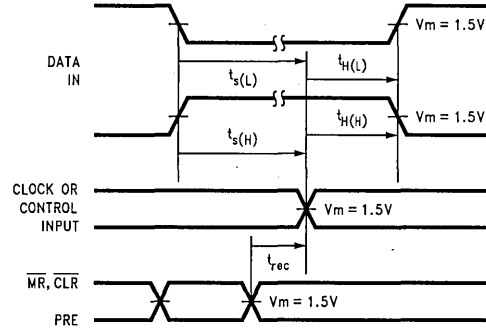

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FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

BCT Family DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA, Non I/O Pins
V_{OH}	Output HIGH Voltage	2.5			V	Min	I_{OH} = −1 mA, Standard or TRI-STATE Outputs
		2.4					I_{OH} = −3 mA, TRI-STATE or Buffer/Line Driver Outputs
		2.0					I_{OH} = −15 mA, Buffer/Line Driver Outputs
V_{OL}	Output LOW Voltage			0.5	V	Min	I_{OL} = 24 mA, TRI-STATE Outputs
				0.55			I_{OL} = 64 mA, Buffer/Line Driver Outputs
I_{IL}	Input LOW Current				mA	Max	V_{IN} = 0.5V, Non I/O Pins
I_{IH}	Input HIGH Current			5.0	μA	Max	V_{IN} = 2.7 V, Non I/O Pins
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V_{IN} = 7.0 V
I_{BVIT}	Input HIGH Current Breakdown (i/o)			100	μA	Max	V_{IN} = 5.5 V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, All Other Pins Grounded
I_{OZH}	Output Leakage Current				μA	Max	V_{OUT} = 2.7V, TRI-STATE Outputs, Non I/O
I_{OZL}	Output Leakage Current				μA	Max	V_{OUT} = 0.5V, TRI-STATE Outputs, Non I/O
I_{IH} + I_{OZH}	Output Leakage Current				μA	Max	$V_{I/O}$ = 2.7V, I/O Pins
I_{IL} + I_{OZL}	Output Leakage Current				μA	Max	$V_{I/O}$ = 0.5V, I/O Pins
I_{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V_{OUT} = 0V, Standard or TRI-STATE Outputs
		−100		−225	mA	Max	V_{OUT} = 0V, Buffer/Line Driver Outputs
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V TRI-STATE Outputs
I_{CCH}	Power Supply Current				mA	Max	V_{OUT} = HIGH
I_{CCL}	Power Supply Current				mA	Max	V_{OUT} = LOW
I_{CCZ}	Power Supply Current				mA	Max	V_{OUT} = HIGH Z

Skew Definitions and Test Philosophy

Test Philosophy

Minimizing output skew is a key design criteria in today's high-speed clocking schemes. National has incorporated new skew specifications into the BCT family of devices. National's test philosophy is to fully test guarantee all the available skew specifications in order to help clock designers optimize their clock budgets.

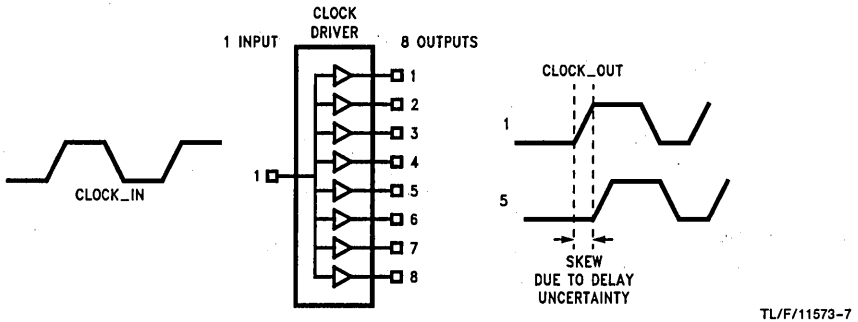
This section provides general definitions and examples of skew and then discusses National's BCT bench performance methods and examples.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s).

Example:

If signal appears at out #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.



TL/F/11573–7

FIGURE 7. Clock Output Skew

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device, duty cycle and device-to-device delay differences.

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

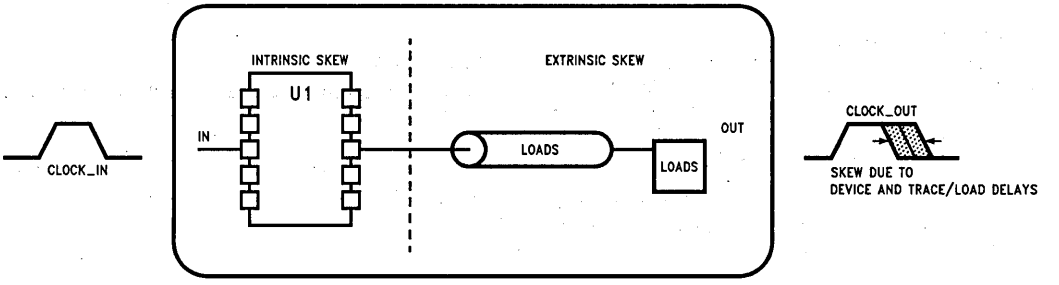


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FIGURE 8. Sources of Clock Skew

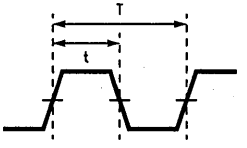
Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles
Total system skew budget = 10% of clock cycle = 2 ns* → 2 ns
If extrinsic skew = 1 ns → − 1 ns
Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design *Rule of thumb.*

CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is *High* or *Low* in a given clock cycle.



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Duty Cycle = t/T * 100%

FIGURE 9. Duty Cycle Calculation

Clock Signal

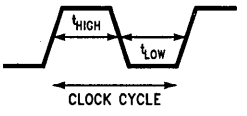

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FIGURE 10. Clock Cycle

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.

Clock + Skew

TL/F/11573–11

FIGURE 11. Clock Skew

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE I

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle		
50 MHz	0 ns	10 ns	10 ns	50/50%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%		
50 MHz	1 ns	11 ns	9 ns	55/45%		
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{PS} (Pin Skew or Transition Skew)

t_{PS}, describes opposite edge skews, i.e., the difference between the delay of the low-to-high transition and the high-to-low transition on the same pin. This parameter is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. Ideally this number needs to be 0 ns. Effectively, 0 ns means that there is no degradation of the input signal's Duty Cycle.

Many of today's microprocessors require a minimum of a 45:55 percent Duty Cycle. System clock designers typically achieve this in one of two ways. The first method is with an expensive crystal oscillator which meets the 45:55 percent Duty Cycle requirement. An alternative approach is to use a less expensive crystal oscillator and implement a divide by two function. Some microprocessors have addressed this by internally performing the divide by two.

Since Duty Cycle is defined as a percentage, the room for error becomes tighter as the system clock frequency increases. For example in a 25 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 4 ns (t_{PLH} of 18 ns and t_{PLH} of 22 ns) and still meet the Duty Cycle requirement. However for a 50 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 2 ns (t_{PLH} of 9 ns and t_{PHL} of 11 ns) and still meet the Duty Cycle requirement. This analysis assumes a perfect 50:50 percent Duty Cycle input signal.

Definition

t_{PS} (Pin Skew or Transition Skew):

$t_{PS} = |t_{PHL} - t_{PLH}|$

Both high-to-low and low-to-high propagation delays are measured at each output pin across the given device.

Example: A 33 MHz, 50/50% duty cycle input signal would be degraded by 2.6% due to a t_{PS} = 0.8 ns. (See Table and Illustration below.)

Note: Output symmetry degradation also depends on input duty cycle.

Example

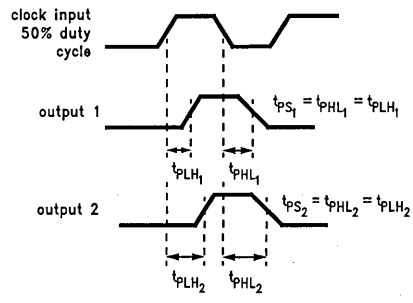

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FIGURE 12. t_{PS}

TABLE II. Duty Cycle Degradation of 33 MHz

f (MHz)	Input			Device	Output			% Δ DC Input to Output
	DC Input	t_{IN} (ns)	T_{IN} (ns)	t_{PS} (ns)	t_{OUT} (ns)	T_{OUT} (ns)	DC Output	
33	**50%/50%**	15.15/15.15	30.3	**0.8**	14.35/15.95	30.3	47.4%/52.6%	**2.6%**
	45%/55%	13.6/16.6	30.3	**1.5**	12.1/18.1	30.3	39.9%/60.1%	**5.1%**

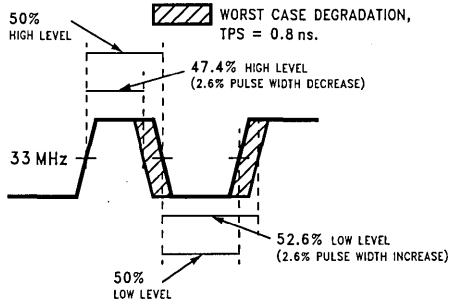

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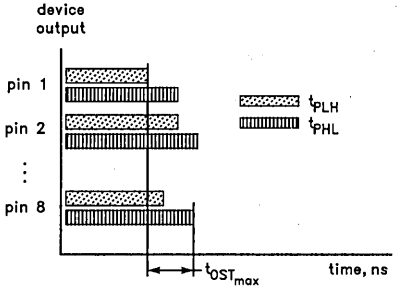
FIGURE 13. Pulse Width Degradation

8

Definition of Parameters (Continued)

t_{OST} (Opposite Edge Skew)

t_{OST} defines the difference between the fastest and the slowest of both transitions within a given chip. Given a specific system with two components, one being positive-edge triggered and one being negative-edge triggered, t_{OST} helps to calculate the required delay elements if synchronization of the positive- and negative-clock edges is required.



TL/F/11573–14

FIGURE 14. t_{OST}

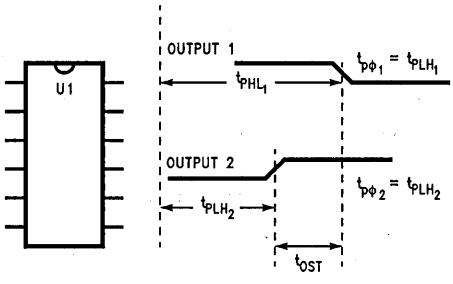
Definition

t_{OST} (Opposite Edge Skew):

$t_{OST} = |t_{P\phi m} - t_{P\phi n}|$

where ϕ is any edge transition (high-to-low or low-to-high) measured between any two outputs (m or n) within any given device.

Example



TL/F/11573–15

FIGURE 15. t_{OST}

Definition of Parameters (Continued)

t_{PV} (Part Variation Skew)

t_{PV} illustrates the distribution of propagation delays between the outputs of any two devices.

Part-to-part skew, t_{PV}, becomes a critical parameter as the driving scheme becomes more complicated. This usually applies to higher-end systems which go from single clock drivers to distributed clock trees to increase fanout (shown below). In a distributed clock tree, part-to-part skew between U2 and U3 must be minimized to optimize system clock frequency. In the case of the clock tree, the total skew becomes a function of $t_{OSLH/HL}$ of U1 plus t_{PV} of U2 and U3.

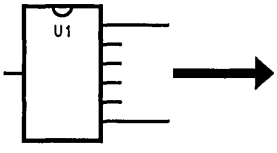


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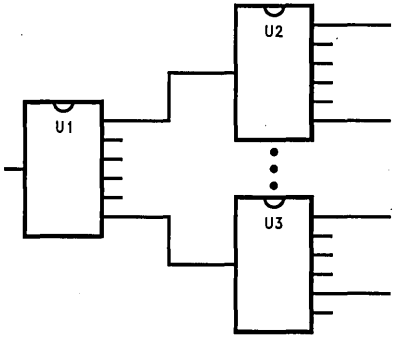
FIGURE 16. Clock Distribution

Case 1: Single Clock Driver

Total Skew = Pin-to-Pin Skew U1
= t_{OSLH} or t_{OSHL} of U1



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Case 2: Distributed Clock Tree

Total Skew (U2, U3) = Pin-to-Pin Skew (U1) + Part-to-Part Skew (U2, U3)

Definition

t_{PV} (Part Variation Skew):

$t_{PV} = |t_{P\phi u,v} - t_{P\phi x,y}|$

where ϕ is any edge transition (high-to-low or low-to-high) measured from the outputs of any two devices.

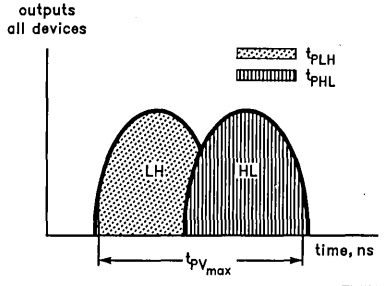

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FIGURE 17. t_{PV}

Example

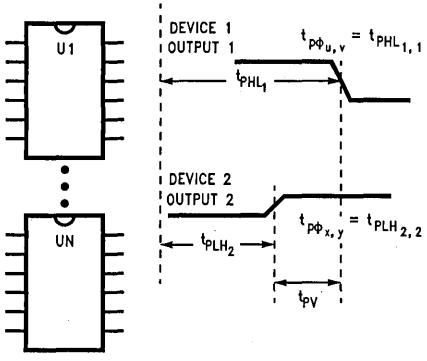

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FIGURE 18. t_{PV}

The skew specifications offered on National's BCT products were chosen based on system performance demands. The parameters t_{OSHL}, t_{OSLH}, t_{OST}, t_{PS}, and t_{PV} each relate to a specific system requirement which helps designers compensate for pin-to-pin skew, duty cycle degradation, and part-to-part variation.

8

Definition of Parameters (Continued)

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

$t_{OSHL} = |t_{PHL_{MAX}} - t_{PHL_{MIN}}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLH_{MAX}} - t_{PLH_{MIN}}|$

Propagation delays are measured across the outputs of any given device.

Example

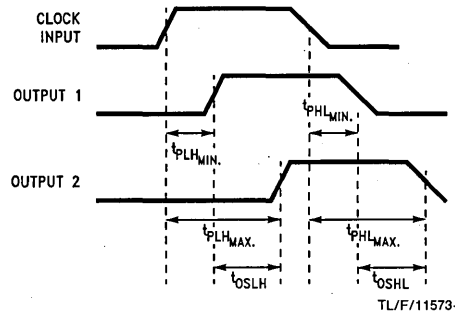

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FIGURE 19. t_{OSLH}, t_{OSHL}

Section 9

BCT Process Characteristics

Section 9 Contents

National Semiconductor

BiCMOS Process Characteristics

A BiCMOS technology has been developed using well-characterized stand-alone bipolar and CMOS processes. Combining CMOS and bipolar circuitry on a single chip has resulted in speed/power advantages that would be difficult and more expensive to achieve in either separate technology. Using 16 masks, this BiCMOS technology is cost effective, manufacturable, and highly suitable for advanced logic designs.

Process Description

The process starts with a standard bipolar front end: P substrate, N buried layer, P buried layer, N-epitaxy, and oxide isolation. The N buried layer provides a collector region for the bipolar device and a retrograde N-well for the PMOS device. The P buried layer is implanted for a retrograde NMOS P-well and channel stop rings for the NPN. These buried layers minimize well and collector resistance, provide latchup suppression, and assist in increasing field threshold and punch-through voltages.

Incorporated into this front end is an intrinsic gettering cycle optimized to create a 10μ–15μ denuded zone. Precipitate-induced stacking faults act as gettering sites for bulk and surface metallics.

1.3μ of N-type epitaxy is grown to support both the CMOS and bipolar devices. Epi oxidation and CVD nitride deposition is accomplished before the active device regions are photo-defined. The nitride and epi oxide are left on all device regions while the field areas receive a silicon etch of 7400Å. 14500Å of isolation oxide is grown to electrically isolate all active devices. The CVD nitride and epi oxide are then stripped and the bird's heads are planarized using an etchback technique. With the device islands created and an implant of phosphrous to the buried collector, the major CMOS steps can now be undertaken. This begins with a second layer of CVD nitride.

A mask step is used to define the field oxidation for the CMOS devices. The field oxidation frames the active CMOS device inside the isolation oxide, while the nitride cap prevents active area oxidation. On the bipolar devices, the field oxidation does not occur because of a complete overlapping of nitride.

Next, a single mask is used to remove nitride from the CMOS device area and to define a V_t adjust implant. A 250Å gate oxidation is followed by polysilicon deposition and photo definition of the gate.

The drawn gate width is 2.5μ and the resulting Leff is 1.8μ. The reduction of the gate can be attributed to the poly overetch and source/drain side diffusion. *Figure 1* shows the bipolar NPN, PMOS, and NMOS devices from left to right, respectively. The NPN is covered with CVD nitride and the CMOS devices have gate oxide under the polysilicon. A cap oxide is grown as a protection layer to the polysilicon during the source and drain implants.

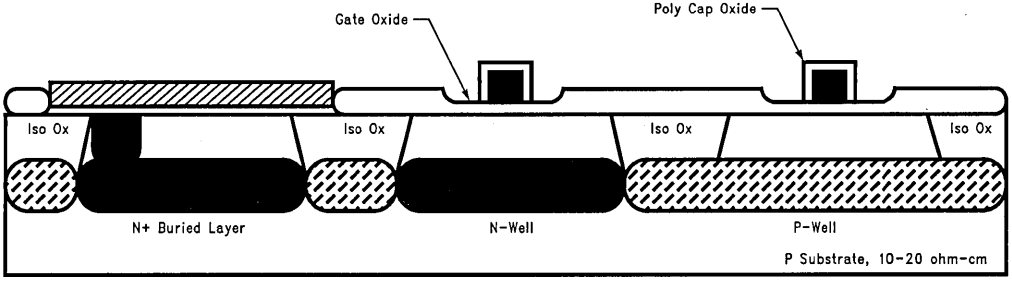

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FIGURE 1. BiCMOS Device Cross-Section

Process Description (Continued)

The bipolar and CMOS final implants follow: P− base, N+ and P+ source/drain. The N+ implant sets the N+ source and drain on the NMOS, as well as the emitter for the bipolar NPN. Anneals are performed after the N+ and P+ source/drain implants.

LTO is used for the CMOS contact film. 3-micron contacts are opened on the source, drain, and gate pad contact areas as well as a frame around the bipolar devices. An LTO etch has been developed that meets the required selectivity to silicon, thermal oxide, doped LTO, and CVD nitride. All contacts receive a platinum silicidation to reduce the contact resistance and allow formation of Schottky diodes.

The interconnect of this technology uses a Ti/W barrier with two layers of Al/Cu. Interconnect planarization is accomplished with spin-on-glass followed by an etch-back. LPCVD oxide completes the inner-layer dielectric. *Figure 2* shows the final process cross section without the metal layers.

Device Characteristics

Table I shows bipolar NPN device characteristics. Beta is stable over four decades of collector current.

TABLE I. BiCMOS Device Results: Bipolar

Emitter Size Microns (as processed)		2.5 x 3.5
Beta	DC Current Gain	75–170
BV_{CBO}	Collector-Base Breakdown	16.0V
BV_{CEO}	Collector-Emitter Breakdown	7.5V
BV_{CES}	C-E with Common Base	12.0V
BV_{EBO}	Emitter-Base Breakdown	5.0V
BV_{ECO}	Emitter-Collector Breakdown	2.5V
BV_{BS}	Base-Substrate Breakdown	16.0V
BV_{CS}	Collector-Subsubstrate Breakdown	15.0V
V_{EARLY}	Forward Early Voltage	28.0V
Rebase	Extrinsic Base Sheet Res.	625Ω/sq
Rpbase	Instrinsic Base Sheet Res.	18000Ω/sq
F_t	Transistor Cut-Off Frequency	8.25 GHz
C_{JE}	Emitter-Base Capacitance	31 fF
C_{JC}	Base-Collector Capacitance	30 fF
C_{JS}	Collector-Substrate Capacitance	68 fF

The I_{CEO} leakage across 1000 transistors in parallel is in the nanoamp range, a direct result of clean process conditions and the intrinsic gettering that maintains that cleanliness.

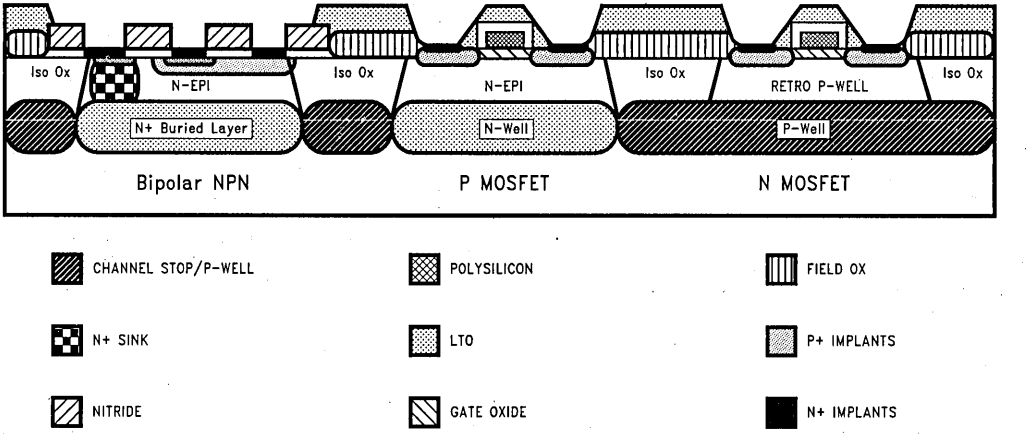

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FIGURE 2. BICMOS Device Cross-Section

Device Characteristics (Continued)

CMOS characteristics are shown in Table II. With drawn 2.5 micron gates and 250 angstroms of gate oxide, the resultant Leff's are 1.8, nominal for both the NMOS and PMOS. Threshold voltages are matched at 0.8V. *Figures 3* and *4* show the I_{DS} vs. V_{DS} family of curves for a PMOS and NMOS, respectively. Channel size is 50 x 2.5, as drawn, for both devices.

TABLE II. BiCMOS Device Results:

CMOS		
Gate Size	Drawn	2.5 μm
Gate Oxide	Thickness	250A
PMOS		
Leff	Effective Gate Length	1.8 μm
V_t	Threshold Voltage	−0.80V
BVDSS	Drain-Source Breakdown	−12.0V min.
IDSS	Saturated Drain Current	4.5 mA*
ISUB	Subthreshold Current	115 mV/dec
BVGOX	Gate Oxide Breakdown	20.0V
NMOS		
Leff	Effective Gate Length	1.8 μm
V_t	Threshold Voltage	0.80V
BVDSS	Drain-Source Breakdown	10.0V min.
IDSS	Saturated Drain Current	9.5 mA*
ISUB	Subthreshold Current	103 mV/dec
BVGOX	Gate Oxide Breakdown	20.0V

*Measured with 5V on Source and Gate

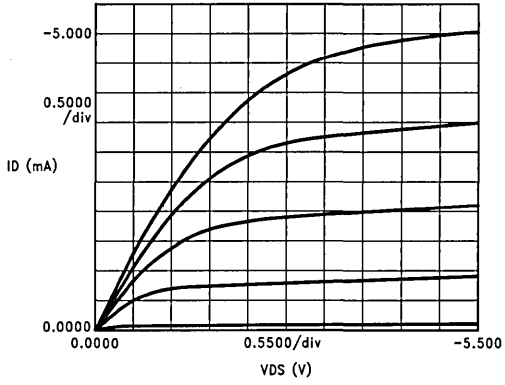

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FIGURE 3. BiCMOS PMOS Device: Forward Characteristics

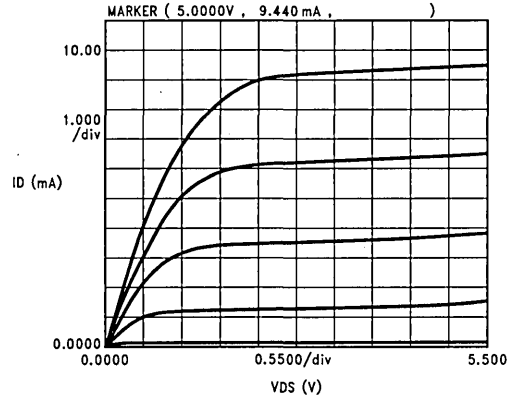

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FIGURE 4. BiCMOS NMOS Device: Forward Characteristics

Manufacturability

Reduced process steps have been achieved with implants that serve more than one device requirement. A single implant is used to set the P-well and the channel stop. The N-well and N+ collector are done with a single implant as are the N+ source/drain and emitter. Mask steps have been kept to a minimum for a merged technology: 16 masks total.

The BiCMOS process meets stringent SPC (Statistical Process Control) requirements established by the manufacturing facility prior to the technology's transfer to the manufacturing organization. Sensitivity analysis has been undertaken to show response to processing excursions, both typical and atypical. All in-line process measurements show normal distributions within established control limits.

Conclusion

A high-performance BiCMOS technology has been demonstrated that is manufacturable and reliable. The device characteristics make this a process that will support advanced logic designs.

References

1. J. Eldredge, C. Joyce, R. Wilkins, *FSTLSI Process Verification Report,* Internal Document.
2. S. Park, *FACT Process Verification Report,* Internal Document.
3. S. Irving, *FAST LSI Model Report,* Internal Report.
4. S. Irving, *1.5 Micron FACT Model Report,* Internal Report.

Section 10

BCT Datasheets

Section 10 Contents

National Semiconductor

74BCT125
Quad Buffer with TRI-STATE® Outputs

General Description

The 'BCT125 is a quad buffer with TRI-STATE outputs designed to be employed as a memory and address driver or bus-oriented transmitter/receiver. Each output is disabled by its own associated $\overline{A}$.

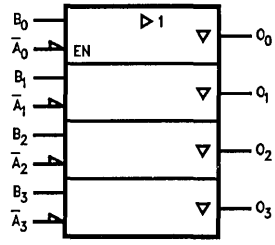
Features

- TRI-STATE outputs drive bus lines or buffer memory address registers
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 2000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbol

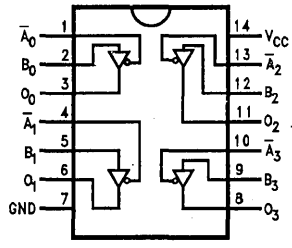
IEEE/IEC



TL/F/10946–1

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10946–2

Pin Names	Description
$\overline{A}_n$, B_n	Inputs
O_n	Outputs

Function Table

Inputs		Output
$\overline{A}_n$	B_n	O
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−50	μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			100 20	μA	0V–2.7V 2.7V–5.5V	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	0V–5.5V	V_{OUT} = 0.5V
I_{OZ}	Output Leakage Current			±100 ±20	μA	0V–2.7V 2.4V–0V	$\overline{A}_n$ = 0.8V, V_{OUT} = 0.5V or 2.7V (Power Up) $\overline{A}_n$ = 0.8V, V_{OUT} = 0.5V or 2.7V (Power Down)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA (All Other Pins Grounded)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		8	20	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		18	30	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		6	12	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74BCT $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	1.6 2.7	3.6 6.3	5.2 7.5	1.6 2.7	5.7 7.7	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	3.4 5.0	6.5 7.8	9.0 10.4	3.4 5.0	10.3 11.0	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	3.0 2.8	5.4 6.0	7.4 7.9	3.0 2.8	8.6 8.6	ns	8-5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.6		0.75	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.4		0.5	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			3.5		3.7	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			3.8		4.0	ns	

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$ 4 Outputs Switching (Note 3)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ 1 Output Switching (Note 4)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ 4 Outputs Switching (Notes 3, 4)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	3.0 3.0	6.5 8.5	3.0 3.0	8.0 10.0	4.0 4.0	9.0 11.5	ns	8-3
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		0.8		1.2		1.3	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output		0.6		0.8		0.9	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output		3.8		4.4		4.8	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output		4.0		4.8		4.9	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Control Inputs	4.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	9.0	pF	V_{CC} = 5.0V

National Semiconductor

74BCT240
Octal Buffer/ Line Driver with TRI-STATE® Outputs

General Description

The 'BCT240 is an inverting octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/ receiver.

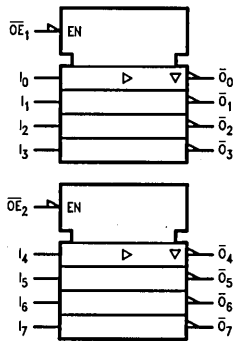
Features

- Inverting buffers
- Low I_{CCZ} through BiCMOS techniques
- TRI-STATE outputs drive bus lines
- Output sink capability of 64 mA, source capability of 15 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed 500 mA minimum latchup protection
- Non destructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbol

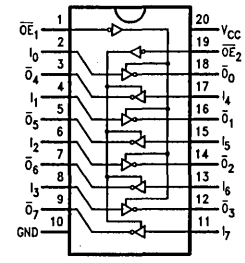
IEEE/IEC



TL/F/10881–2

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10881–1

Truth Table

$\overline{OE}_1$	I_{0-3}	$\overline{O}_{0-3}$	$\overline{OE}_2$	I_{4-7}	$\overline{O}_{4-7}$
H	X	Z	H	X	Z
L	L	H	L	L	H
L	H	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active LOW)
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-off State in the High State	−0.5V to +5.5V −0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source or Sink Current	±500 mA

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		9.8	18	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		44.0	69	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		2.5	9	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.5 0.4	3.0 2.0	4.8 3.5	0.5 0.4	5.6 4.0	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	1.0 1.0	5.0 6.3	7.9 9.4	1.0 1.0	8.8 10.5	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	1.0 1.0	4.6 6.0	6.8 8.1	1.0 1.0	8.1 9.5	ns	8-5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			1.0		1.7	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			1.3		2.3	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			2.5		4.3	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			2.8		5.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 50$ pF, 8 Outputs Switching (Note 1)		74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 250$ pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	3.0 1.5	7.0 6.5	3.0 1.5	7.7 5.0	ns	8-3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	9.0	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT2240
Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The 'BCT2240 is an inverting octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, or bus-oriented transmitters/receivers.

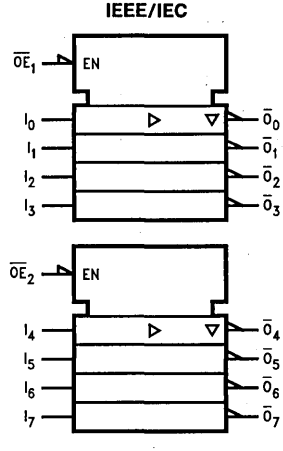
The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

- 25Ω series resistors in outputs eliminate the need for external resistors
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed 500 mA minimum latchup protection
- Hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

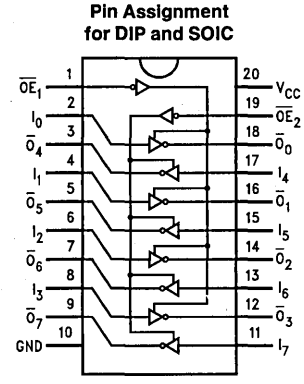
Ordering Code: See Section 11

Logic Symbol



TL/F/10894–1

Connection Diagram



TL/F/10894–2

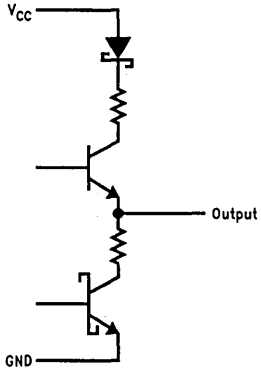
Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Outptut Enable Input (Active LOW)
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Table

$\overline{OE}_1$	I_{0-3}	$\overline{O}_{0-3}$	$\overline{OE}_2$	I_{4-7}	$\overline{O}_{4-7}$
H	X	Z	H	X	Z
L	L	H	L	L	H
L	H	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Schematic of Each Output



TL/F/10894–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source or Sink Current	±500 mA

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54BCT/74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.5 0.8	V	Min	I_{OL} = 3 mA I_{OL} = 15 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		8.3	18	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		42.3	69	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		6.6	8	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.5 0.5	2.6 2.4	4.8 4.0	0.5 0.5	5.7 4.4	ns	8–3
t_{PZH} t_{PZL}	Output Enable Time	2.6 4.3	5.0 7.0	8.2 10.9	2.6 4.3	9.3 12.4	ns	8–5
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.2	4.4 6.6	7.1 8.5	2.0 2.2	8.7 10.6	ns	8–5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.3		0.4	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.4		0.5	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			0.7		1.5	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			1.0		2.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: Progagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 50$ pF, 8 Outputs Switching (Note 1)		74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 250$ pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	3.5 2.5	7.0 5.0	3.0 3.5	7.5 7.8	ns	8–3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	8.8	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	13.6	pF	V_{CC} = 5.0V

National Semiconductor

74BCT241
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

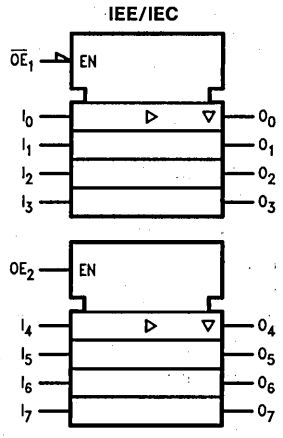
The 'BCT241 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

Features

- Non-inverting buffers
- Low I_{CCZ} through BiCMOS techniques
- TRI-STATE outputs drive bus lines
- Output sink capability of 64 mA, source capability of 15 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed 500 mA minimum latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

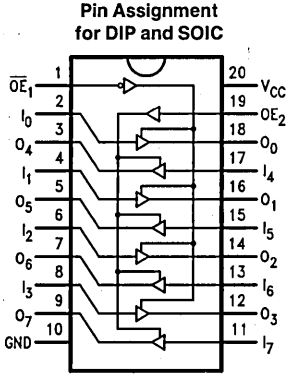
Ordering Code: See Section 11

Logic Symbol



TL/F/10698–2

Connection Diagram



TL/F/10698–1

Truth Table

$\overline{OE}_1$	I_{0-3}	O_{0-3}	OE_2	I_{4-7}	O_{4-7}
H	X	Z	L	X	Z
L	H	H	H	H	H
L	L	L	H	L	L

Pin Names	Description
$\overline{OE}_1$	Output Enable Input (Active Low)
OE_2	Output Enable Input (Active High)
I_0–I_7	Inputs
O_0–O_7	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source or Sink Current	±500 mA

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		23	40	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		41	65	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		6	10	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.5 1.0		4.5 5.4	0.5 1.0	4.9 5.9	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	1.0 1.0		7.8 8.6	1.0 1.0	8.7 9.4	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	1.0 1.0		6.8 8.1	1.0 1.0	8.1 9.9	ns	8-5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.8		1.2	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.9		1.0	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			1.5		2.0	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			2.5		3.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC} from device to device. This specification is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$ 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	3.0 1.5	5.5 6.5	3.0 1.5	8.2 8.5	ns	8-3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 2: These specifications guaranteed but not tested. The limits represent propagation delay swith 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	13.0	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT2241
Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The 'BCT2241 is an octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers.

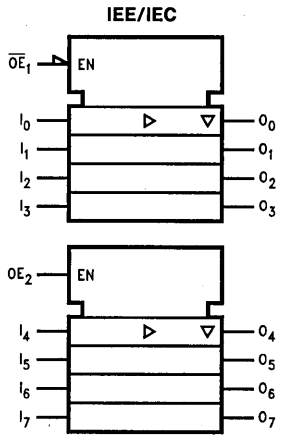
The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

- 25Ω series resistors in outputs eliminate the need for external resistors
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

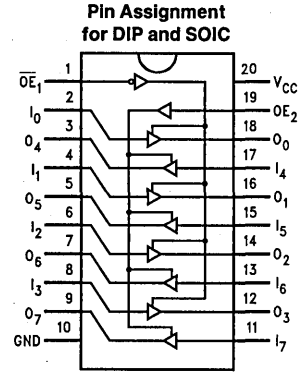
Ordering Code: See Section 11

Logic Symbol



TL/F/10895–1

Connection Diagram



TL/F/10895–2

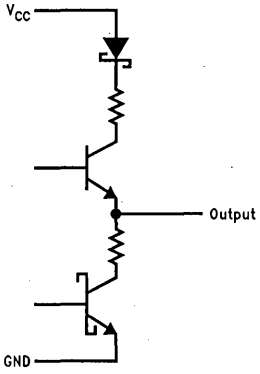
Pin Names	Description
$\overline{OE}_1$	Output Enable Input (Active Low)
OE_2	Output Enable Input (Active High)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Table

$\overline{OE}_1$	I_{0-3}	O_{0-3}	OE_2	I_{4-7}	O_{4-7}
H	X	Z	L	X	Z
L	H	H	H	H	H
L	L	L	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Schematic of Each Output



TL/F/10895–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55 0.8	V	Min	I_{OL} = 3 mA I_{OL} = 15 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		23	35	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		40	60	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		6	10	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $V_{CC} = Com$ $V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.1 2.0	3.0 3.8	4.4 6.6	1.1 2.0	4.9 6.9	ns	8–3
t_{PZH} t_{PZL}	Output Enable Time	2.7 4.1	5.9 6.8	7.8 9.4	2.7 4.1	8.9 10.3	ns	8–5
t_{PHZ} t_{PLZ}	Output Disable Time	1.7 1.7	4.0 5.2	7.2 9.5	1.7 1.7	8.7 11.3	ns	8–5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			1.0		1.2	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.9		1.1	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			2.0		3.3	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			3.0		4.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specificaton is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.5 3.0	6.0 7.0	3.6 3.6	7.0 10.0	ns	8–3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	8	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	11	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT244
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

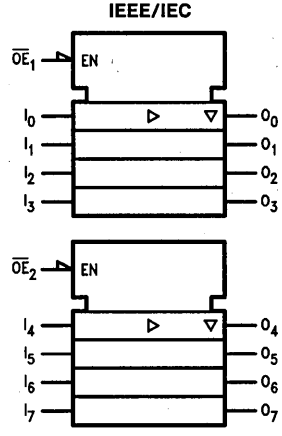
The 'BCT244 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

Features

- Non-inverting buffers
- Low I_{CCZ} through BiCMOS techniques
- TRI-STATE outputs drive bus lines
- Output sink capability of 64 mA
- Source capability of 15 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

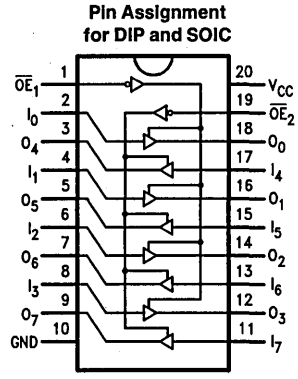
Ordering Code: See Section 11

Logic Symbol



TL/F/10699–2

Connection Diagram



TL/F/10699–1

Truth Table

$\overline{OE}_1$	I_{0-3}	O_{0-3}	$\overline{OE}_2$	I_{4-7}	O_{4-7}
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active Low)
I_0–I_7	Inputs
O_0–O_7	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source or Sink Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		22	38	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		41	66	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		5	10	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	54/74BCT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.2 1.7	2.8 3.2	4.4 5.0	0.7 1.4	5.0 5.5	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	6.0 6.2	7.8 8.1	2.0 2.0	8.7 8.9	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	1.0 1.0	3.8 5.8	6.7 7.8	1.0 1.0	7.7 7.8	ns	8-5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.75		1.0	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.70		1.0	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			3.8		4.5	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			3.8		4.8	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 50$ pF, 8 Outputs Switching (Note 1)		74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 250$ pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	3.0 3.0	6.5 6.0	3.0 3.0	7.7 6.7	ns	8-3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 2: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	11	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT2244
Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The 'BCT2244 is an octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers.

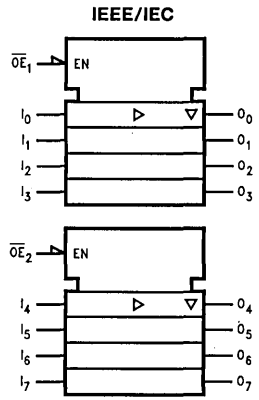
The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

- 25Ω series resistors in outputs eliminate the need for external resistors
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

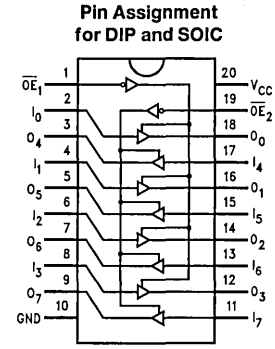
Ordering Code: See Section 11

Logic Symbol



TL/F/10896–1

Connection Diagram



TL/F/10896–2

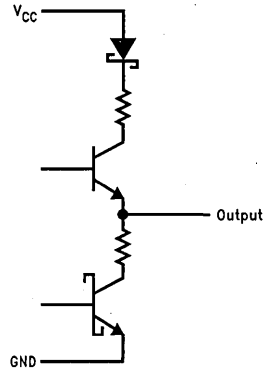
Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active Low)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Table

$\overline{OE}_1$	I_{0-3}	O_{0-3}	$\overline{OE}_2$	I_{4-7}	O_{4-7}
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Schematic of Each Output



TL/F/10896–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55 0.8	V	Min	I_{OL} = 3 mA I_{OL} = 15 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		23	34	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		40	60	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		5.6	10	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.5 1.6	3 3.7	4.4 6.3	0.5 1.6	4.9 6.7	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	2.4 3.9	6.1 7.1	7.7 9.4	2.4 3.9	8.7 10.4	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	1.7 2.8	4 6	6.9 8.3	1.7 2.8	7.8 9.8	ns	8-5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			1.8		2.8	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew HL Data to Output			1.0		1.2	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			2.9		3.3	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			3.5		3.9	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}, from device to device. This specification is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 3.0	5.4 7.2	3.0 3.0	7.0 9.5	ns	8-3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	11	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT245
Octal Bidirectional Transceiver with TRI-STATE® Outputs

General Description

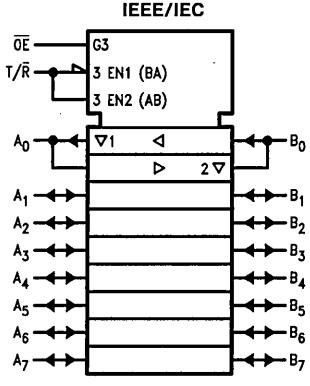
The 'BCT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA (48 mA Mil) at the B port. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in a high impedance state.

Features

- Non-inverting buffers
- Bidirectional data path
- Low I_{CCZ} through BiCMOS techniques
- TRI-STATE outputs drive bus lines
- Output sink capability of 64 mA
- Source capability of 15 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

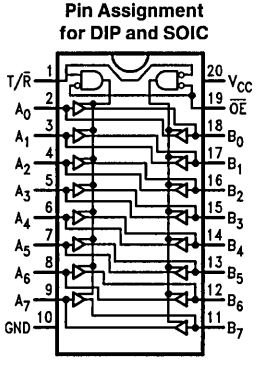
Ordering Code: See Section 11

Logic Symbol



TL/F/10700–3

Connection Diagram



TL/F/10700–2

Truth Table

Inputs		Output
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active Low)
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Inputs or TRI-STATE Outputs
B_0–B_7	Inputs or TRI-STATE Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.5 2.4 2.0			V	Min	I_{OH} = −1 mA (An) I_{OH} = −3 mA (An, Bn) I_{OH} = −15 mA (Bn)
V_{OL}	Output LOW Voltage			0.5 0.55	V	Min	I_{OL} = 24 mA (An) I_{OL} = 64 mA (Bn)
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V ($\overline{OE}$, T/$\overline{R}$)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V ($\overline{OE}$, T/$\overline{R}$)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (An, Bn)
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V ($\overline{OE}$, T/$\overline{R}$)
I_{OS}	Output Short-Circuit Current	−100 −60		−225 −150	mA mA	Max Max	V_{OUT} = 0V (Bn) V_{OUT} = 0V (An)
I_{IH}+ I_{OZH}	Output Leakage Current			25	μA	Max	V_{OUT} = 2.7V (An, Bn)
I_{IL}+ I_{OZL}	Output Leakage Current			−150	μA	Max	V_{OUT} = 0.5V (An, Bn)
I_{CEX}	Output High Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (An, Bn)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V(An, Bn)
I_{CCH}	Power Supply Current		19.4	40	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		42.5	70	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		10	15	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0 1.5	2.7 2.9	6.0 6.6	1.0 1.5	7.0 7.0	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5	6.6 5.8	9.4 10.2	1.5 1.5	10.9 11.6	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	1.5 1.5	3.9 3.4	8.3 7.8	1.5 1.5	9.3 9.1	ns	8-5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			1.2		1.3	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.9		1.0	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			1.8		2.2	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			4.6		5.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 2.0	8.0 8.0	3.0 3.0	9.0 9.0	ns	8-3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	11.2	pF	$V_{CC} = 5.0V$ ($\overline{OE}$, T/$\overline{R}$)
$C_{I/O}$	Input/Output Pin Capacitance	10.2	pF	$V_{CC} = 5.0V$ (An, Bn)

National Semiconductor

74BCT373
Octal Transparent Latch with TRI-STATE® Outputs

General Description

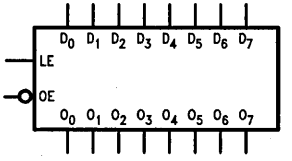
The 'BCT373 consists of eight latches with TRI-STATE outputs for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Features

- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})
- Guaranteed 4000V minimum ESD protection
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed latchup protection
- Low I_{CCZ} through BiCMOS techniques

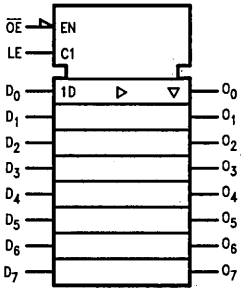
Ordering Code: See Section 11

Logic Symbols



TL/F/10877–3

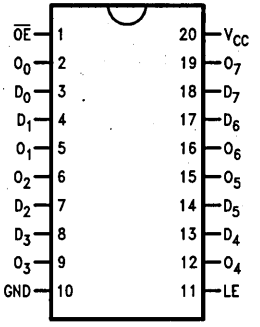
IEEE/IEC



TL/F/10877–1

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10877–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Latch Outputs

Functional Description

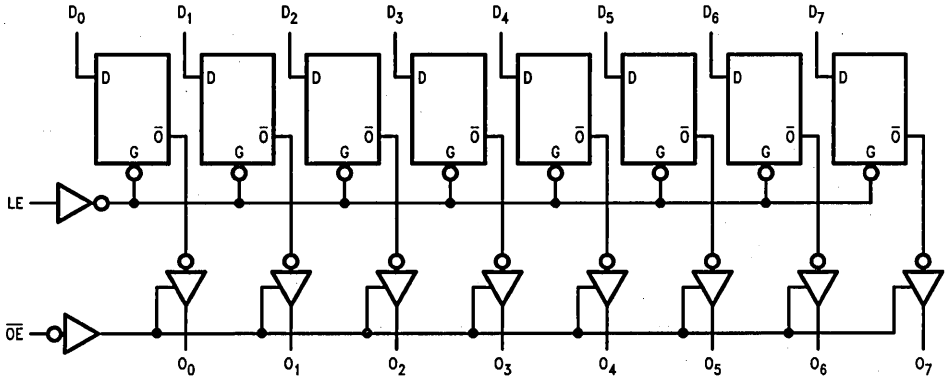
The 'BCT373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Output
LE	$\overline{OE}$	D_n	O_n
H	L	H	H
H	L	L	L
L	L	X	O_n (no change)
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance State

Logic Diagram



TL/F/10877–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			8	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			30	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			10	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 2.0		9.3 11.6	2.0 1.5	9.3 11.6	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	2.0 2.0		10.3 9.3	2.0 2.0	10.3 9.3	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0		11.8 11.8	2.0 2.0	11.8 11.8	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0		6.9 6.1	2.0 2.0	6.9 6.1	ns	8-5

AC Electrical Characteristics: See Section 8 for Waveforms

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to LE	5.9 5.9		5.9 5.9		ns	8-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to LE	1.5 1.5		1.5 1.5			
$t_w(H)$	LE Pulse Width, HIGH	3.0		3.0		ns	8-4

Extended AC Electrical Characteristics: See Section 8

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF 8 Outputs Switching (Note 3)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF (Note 4)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 2.0	10.5 13.0	2.0 2.0	11.8 14.0	ns	8-3

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	5	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	8	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT374
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

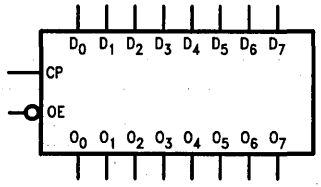
The 'BCT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed 4000V minimum ESD protection
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

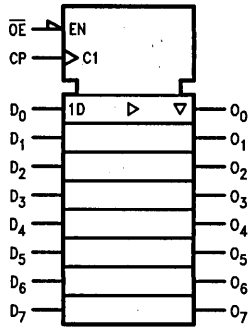
Ordering Code: See Section 11

Logic Symbols



TL/F/10878–1

IEEE/IEC

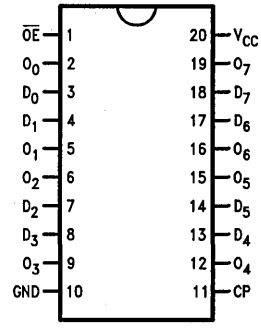


TL/F/10878–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Outputs

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10878–2

Functional Description

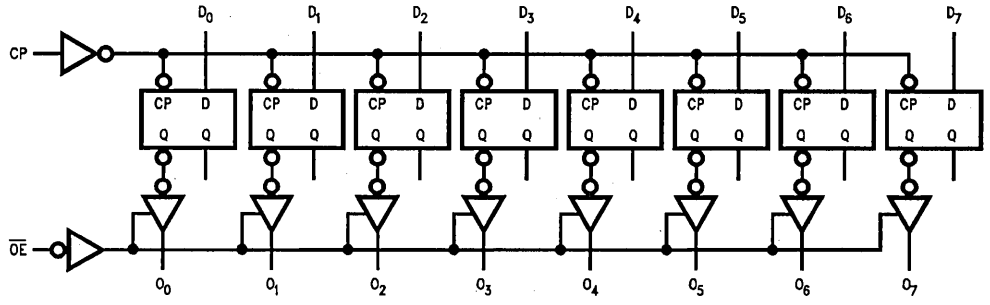
The 'BCT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Internal Register	Output
D_n	CP	$\overline{OE}$		O_n
H	↗	L	H	H
L	↗	L	L	L
X	X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/10878–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			8	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			30	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			10	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	70	130		70		MHz	8-1
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0 2.0	5.4 4.3	9.1 7.0	2.0 2.0	9.1 7.0	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	8.0 9.0	12.0 12.0	2.0 2.0	12.0 12.0	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.2 4.2	6.8 6.8	2.0 2.0	6.8 6.8	ns	8-5

AC Operating Requirements: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	7.5 7.5		7.5 7.5		ns	8-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	0 0		0 0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 11.5		4.0 11.5		ns	8-4

Extended AC Electrical Characteristics

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF 1 Output Switching (Note 2)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF 8 Outputs Switching (Notes 1, 2)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0 2.0	10.2 10.2	3.0 3.0	12.0 12.0	4.0 4.0	15.0 15.0	ns	8-3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	9.0	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT541
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'BCT541 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. This device is functionally similar to the 'BCT244 but has a broadside pinout.

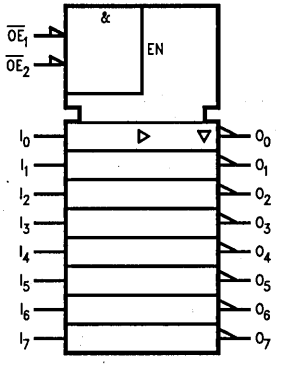
Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Low I_{CCZ} through BiCMOS techniques
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbol

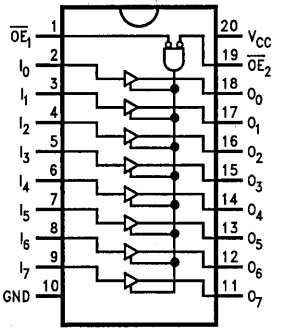
IEE/IEC



TL/F/10989–1

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10989–2

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Input (Active LOW)
I_n	Inputs
O_n	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
Over Voltage Latchup	V_{CC} +4.5V
DC Latchup Source Current	500 mA
DC Latchup Source Current ($\overline{OE}$)	30 mA

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current		−250		μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{OZ}	Output Leakage Current			±100 ±20	μA		
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			40	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			72	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			7	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.7 2.7	2.9 3.9	5.3 6.5	1.7 2.7	5.3 6.5	ns	8–3
t_{PZH} t_{PZL}	Output Enable Time	4.4 3.9	6.9 6.0	12.0 10.4	4.4 3.9	12.0 10.4	ns	8–5
t_{PHZ} t_{PLZ}	Output Disable Time	1.8 1.5	3.7 3.3	6.2 5.4	1.8 1.5	6.2 5.4	ns	8–5

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$ 8 Outputs Switching (Note 3)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ 1 Output Switching (Note 4)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ 8 Outputs Switching (Notes 3, 4)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.5 4.5	5.0 6.5	5.0 5.5	6.5 7.0	6.0 7.0	9.0 10.0	ns	8–3
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		1.0				1.3	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output		1.2				1.3	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output		3.4				4.0	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output		3.5				4.1	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delay swith 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	13.0	pF	V_{CC} = 5.0V

National Semiconductor

74BCT543
Octal Registered Transceiver

General Description

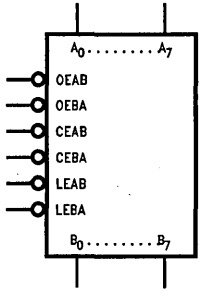
The 'BCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA while the B outputs are rated for 64 mA.

Features

- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA
- B outputs sink 64 mA
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbols



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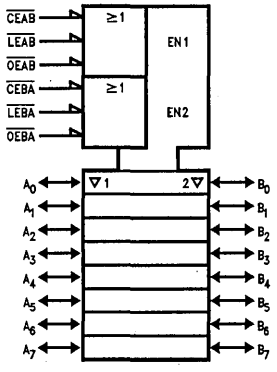
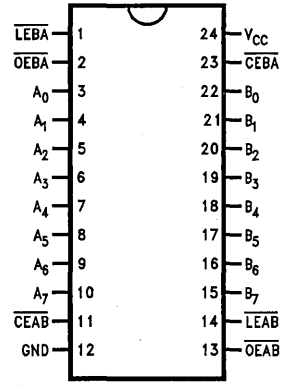
IEEE/IEC



TL/F/10948–4

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10948–2

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

Functional Description

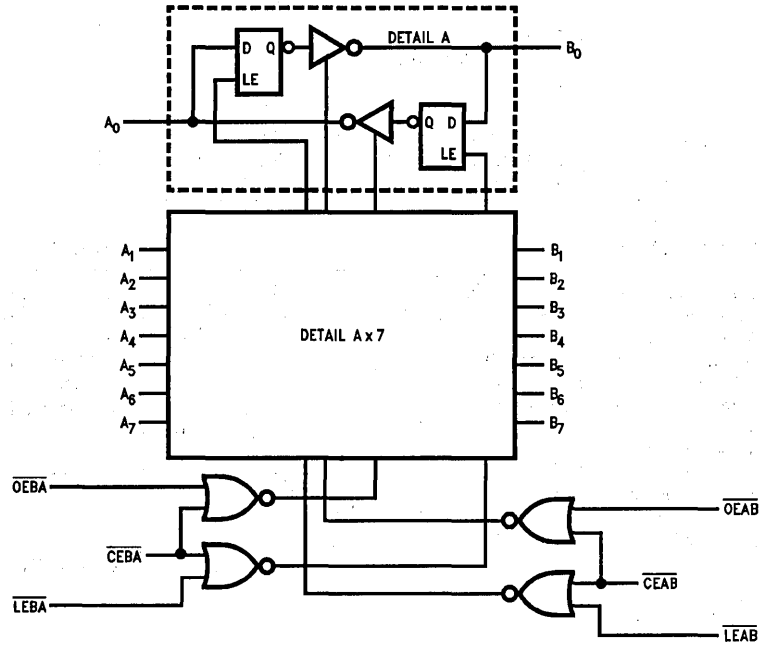
The 'BCT543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or take data from B_0–B_7, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Logic Diagram



TL/F/10948–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V_{IN} = 7.0V ($\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)
I_{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded

DC Electrical Characteristics (Continued)

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{IL}	Input LOW Current			−0.6 −1.2	mA	Max	V_{IN} = 0.5V ($\overline{OEAB}$, $\overline{OEBA}$) V_{IN} = 0.5V ($\overline{CEAB}$, $\overline{CEBA}$)
$I_{IH} + I_{OZH}$	Output Leakage Current			70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
$I_{IL} + I_{OZL}$	Output Leakage Current			−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current	−60 −100		−150 −225	mA	Max	V_{OUT} = 0V (A_n) V_{OUT} = 0V (B_n)
I_{ZZ}	Bus Drainage Test			500	μA	0.0V	V_{OUT} = 5.25V (A_n, B_n)
I_{CCH}	Power Supply Current			15	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			71	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			15	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT T_A = +25°C V_{CC} = +5.0V C_L = 50 pF			74BCT T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	2.0 2.0		8.8 9.6	2.0 2.0	8.8 9.6	ns	8–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ or $\overline{LEAB}$ to A_n or B_n	2.0 2.0		12.9 12.7	2.0 2.0	12.9 12.7	ns	8–3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.0 1.0		12.5 14.5	1.0 1.0	12.5 14.5	ns	8–5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.0 1.0		8.1 7.2	1.0 1.0	8.1 7.2		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.8		0.8	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.8		0.8	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			3.8		3.8	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			4.0		4.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device.

AC Operating Requirements: See Section 8 for Waveforms

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT T_A, V_{CC} = Com		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	4.5 3.0		4.5 3.5		ns	8–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	1.5 3.0		1.5 3.5			
$t_w(L)$	Latch Enable, B to A Pulse Width, LOW	7.0		7.0		ns	8–4

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT T_A = Com V_{CC} = Com C_L = 50 pF 8 Outputs Switching (Note 3)		74BCT T_A = Com V_{CC} = Com C_L = 250 pF (Note 4)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	3.0 3.0	9.8 10.6	3.0 3.0	9.8 10.6	ns	8–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n	3.0 3.0	13.4 13.2	3.0 3.0	13.9 13.7	ns	8–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to B_n	4.5 4.5	13.0 13.0	4.5 4.5	13.5 13.5	ns	8–3

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Control Inputs	6	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	11	pF	V_{CC} = 5.0V

National Semiconductor

74BCT573
Octal D Latch with TRI-STATE® Outputs

General Description

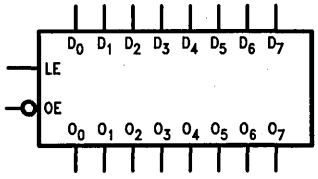
The 'BCT573 consists of eight latches with TRI-STATE outputs for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. This device is functionally identical to the "BCT373 but has a broadside pinout.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to the 'BCT373
- TRI-STATE outputs for bus interfacing
- Guaranteed 2000V minimum ESD protection
- Guaranteed multiple output switching specifications
- Guaranteed 500 mA minimum latchup protection
- Low I_{CCZ} through BiCMOS techniques
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbol



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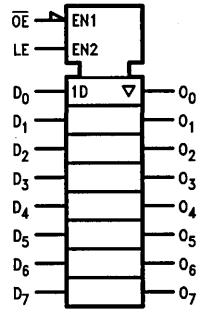
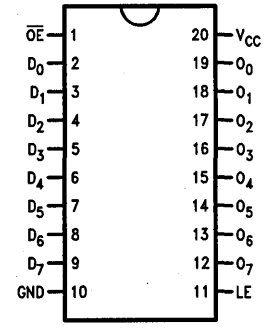
IEEE/IEC



TL/F/10879–3

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10879–2

Functional Description

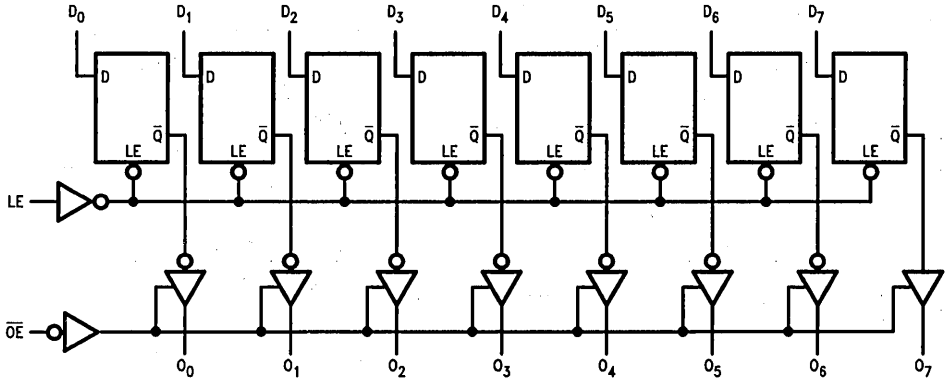
The 'BCT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfer with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
O_0 = Value stored from previous clock cycle

Logic Diagram



TL/F/10879–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			20	μA	0V–5.5V	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	0V–5.5V	V_{OUT} = 0.5V
I_{OZ}	Output Leakage Current			±20	μA	0V–2.0V 1.8V–0V	$\overline{OE}$ = 2.0V, V_{OUT} = 0.5V or 2.7V (Power Up) $\overline{OE}$ = 2.0V, V_{OUT} = 0.5V or 2.7V (Power Down)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		8	12	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		29	48	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		6	8	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 3.5	4.0 7.4	8.4 10.5	2.0 3.5	8.4 10.5	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	3.0 3.0	6.8 5.7	8.9 8.3	3.0 3.0	8.9 8.3	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	3.7 3.7	6.1 6.5	10.0 10.0	3.7 3.7	10.0 10.0	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	2.2 2.2	4.8 4.8	7.0 7.0	2.2 2.2	7.0 7.0	ns	8-5

AC Operating Requirements: See Section 8 for Waveforms

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to LE	1.0 1.0		1.0 1.0		ns	8-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to LE	4.0 4.0		4.0 4.0		ns	
$t_w(H)$	LE Pulse Width, HIGH	4.0		4.0		ns	8-4

Extended AC Electrical Characteristics

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF 1 Output Switching (Note 2)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF 8 Outputs Switching (Notes 1, 2)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 3.5	10.0 13.0	3.0 4.0	9.5 13.0	4.0 6.0	12.0 16.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	4.0 4.0	10.0 9.5	4.0 4.0	12.0 10.0	6.0 6.0	14.5 13.0	ns

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameteer	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	10.0	pF	V_{CC} = 5.0V

National Semiconductor

74BCT574
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'BCT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

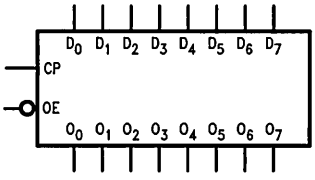
This device is functionally identical to the 'BCT374 but has a broadside pinout.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to the 'BCT374
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection
- Guaranteed multiple output switching specifications
- Guaranteed 500 mA minimum latchup protection
- Low I_{CCZ} through BiCMOS techniques
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbols



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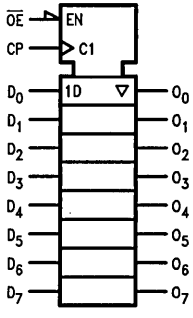
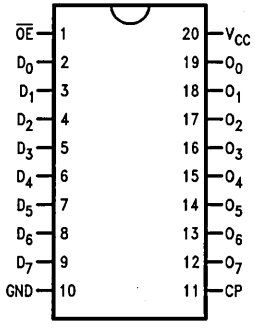
IEEE/IEC



TL/F/10880–3

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10880–2

Functional Description

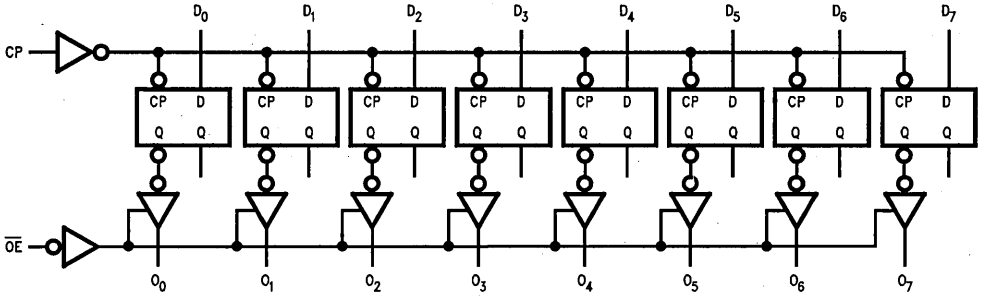
The 'BCT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Internal Register	Output
D_n	CP	$\overline{OE}$		O_n
H	⌐‾	L	H	H
L	⌐‾	L	L	L
X	X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐‾ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/10880–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			20	μA	0V–5.5V	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	0V–5.5V	V_{OUT} = 0.5V
I_{OZ}	Output Leakage Current			±20	μA	0V–2.0V 1.6V–0V	$\overline{OE}$ = 2.0V, V_{OUT} = 0.5V or 2.7V (Power Up) $\overline{OE}$ = 2.0V, V_{OUT} = 0.5V or 2.7V (Power Down)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		8	12	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		30	48	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		6	8	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	77			77		MHz	8–1
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.8 2.8	6.5 5.5	9.4 8.9	2.8 2.8	9.4 8.9	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	3.7 3.7	6.0 6.5	9.5 9.5	3.7 3.7	9.5 9.5	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	1.3 1.3	4.5 4.5	7.5 6.9	1.3 1.3	7.5 6.9	ns	8-5

AC Operating Requirements: See Section 8 for Waveforms

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	4.5 6.0		4.6 6.0		ns	8–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	0.0 0.0		0.0 0.0		ns	
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.5 5.5		5.5 5.5		ns	8–4

Extended AC Electrical Characteristics

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$ 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ 1 Output Switching (Note 2)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ 8 Outputs Switching (Notes 1, 2)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	4.0 4.0	10 9.5	6.0 5.0	12.0 9.5	7.0 6.0	15.0 12.0	ns	8–3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	10.0	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT646
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

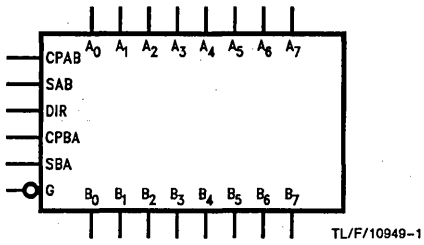
This device consists of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

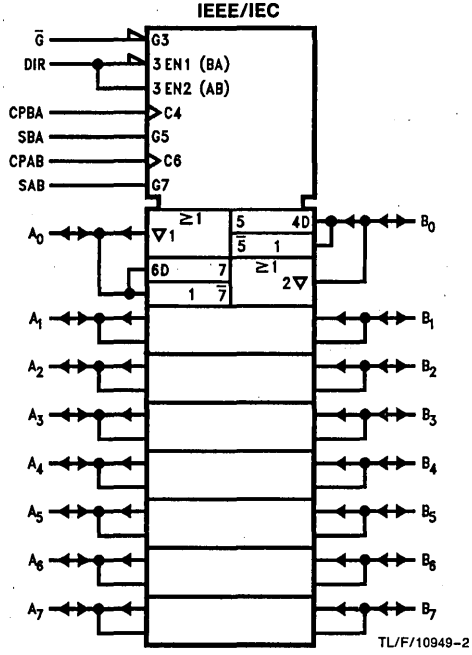
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Low I_{CCZ} through BiCMOS techniques
- TRI-STATE outputs drive bus lines
- Output sink capability of 64 mA, source capability of 15 mA
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed 500 mA minimum latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbols



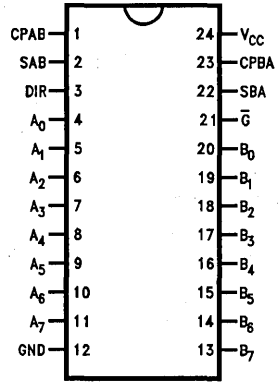
TL/F/10949–1



TL/F/10949–2

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10949–3

Pin Names	Description
A_0–A_7	Data Register A Inputs/TRI-STATE Outputs
B_0–B_7	Data Register B Inputs/TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

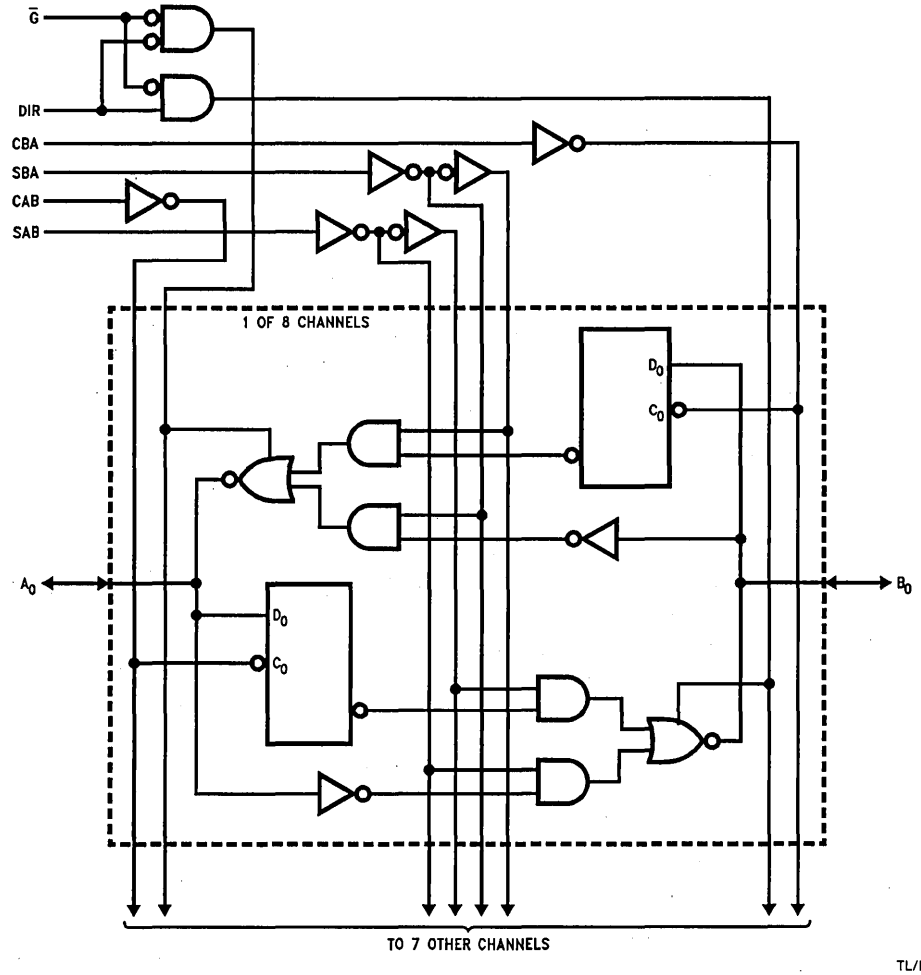
Function Table

Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock A_n Data into A Register
H	X	X	↑	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↑	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↑	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR Inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
↑ = LOW-to-HIGH Transition

Logic Diagram



TL/F/10949–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = − 3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5.0	μA	Max	V_{IN} = 2.7V (Non I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V_{IN} = 7.0V (Non I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V (Non I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current			−225	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		15	22	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		40	49	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		16	22	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	83	165		83		MHz	8-1
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.8 2.8	5.9 5.9	8.8 8.8	2.8 2.8	9.9 9.9	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.4 2.4	4.6 5.8	7.5 9.2	2.4 2.4	8.9 9.8	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	3.0 3.0	6.6 6.6	11.0 11.0	3.0 3.0	11.3 11.3	ns	8-3
t_{PZH} t_{PZL}	Enable Time $\overline{G}$ to A or B	4.0 4.6	8.0 8.8	12.9 13.9	4.0 4.6	13.2 14.4	ns	8-5
t_{PHZ} t_{PLZ}	Disable Time $\overline{G}$ to A or B	2.0 2.0	4.0 5.0	8.8 8.8	2.0 2.0	8.8 8.8	ns	8-5
t_{PZH} t_{PZL}	Enable Time DIR to A or B	4.0 4.0	8.0 9.0	14.4 14.4	4.0 4.0	14.4 14.4	ns	8-5
t_{PHZ} t_{PLZ}	Disable Time DIR to A or B	2.0 2.0	5.0 6.0	11.1 11.1	2.0 2.0	11.1 11.1	ns	8-5

AC Operating Requirements: See Section 8 for Waveforms

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Max	Min		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW Bus to Clock	5.0 5.0		5.0 5.0		ns	8-6
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW Bus to Clock	1.0 1.0		1.0 1.0		ns	8-6
$t_W(H)$ $t_W(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0		5.0 5.0		ns	8-4

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT T_A = Com, V_{CC} = Com, C_L = 50 pF, 8 Outputs Switching (Note 1)		74BCT T_A = Com, V_{CC} = Com, C_L = 250 pF, 1 Output Switching (Note 2)		74BCT T_A = Com, V_{CC} = Com, C_L = 250 pF, 8 Outputs Switching (Notes 1, 2)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.5	10.5	4.0	12.0	4.0	15.6	ns	8–5
t_{PHL}	Clock to Bus	3.5	10.5	4.0	12.0	4.0	15.6		
t_{PLH}	Propagation Delay	3.5	10.5	4.0	11.0	4.0	15.0	ns	8–5
t_{PHL}	Bus to Bus	3.5	10.5	4.0	11.0	4.0	15.0		
t_{PLH}	Propagation Delay	3.5	12.5	4.0	14.2	4.0	18.1	ns	8–5
t_{PHL}	SBA or SAB to A or B	3.5	12.5	4.0	14.2	4.0	18.1		

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	6.2	pF	V_{CC} = 5.0V (Control Inputs)
$C_{I/O}$	Input/Output Pin Capacitance	12.8	pF	V_{CC} = 5.0V (An, Bn)

National Semiconductor

74BCT652
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

This device consists of a bus transceiver circuit with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

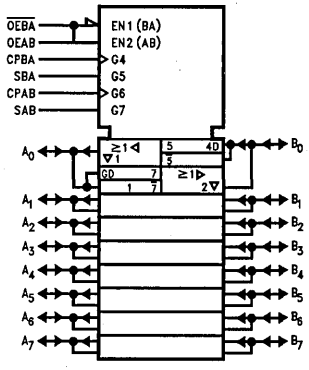
Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})
- TRI-STATE® outputs drive bus lines

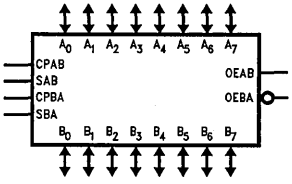
Ordering Code: See Section 11

Logic Symbols

IEEE/IEC



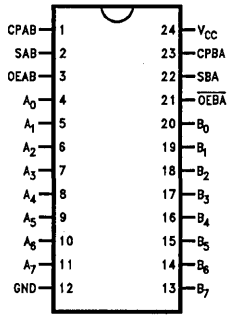
TL/F/10950–1



TL/F/10950–3

Connection Diagram

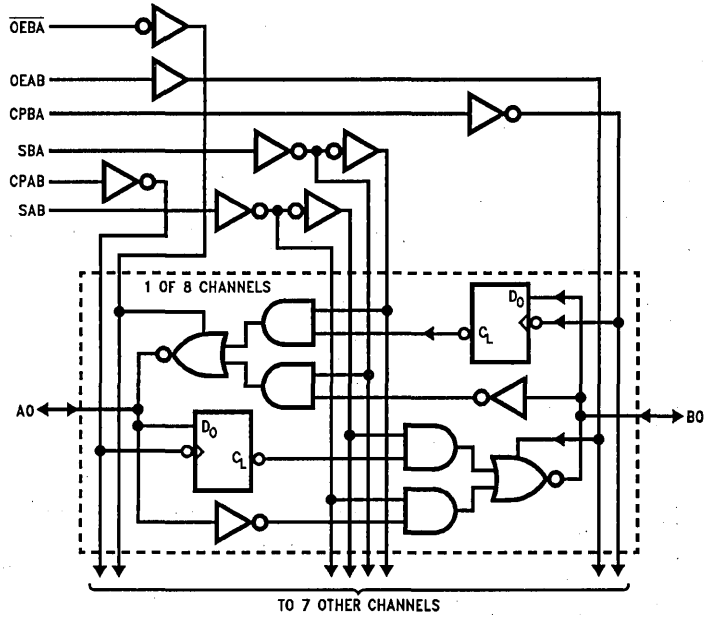
Pin Assignment
DIP and SOIC



TL/F/10950–2

Pin Names	Description
A_0–A_7, B_0–B_7	A and B Inputs/ TRI-STATE® Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

Logic Diagram



TL/F/10950–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

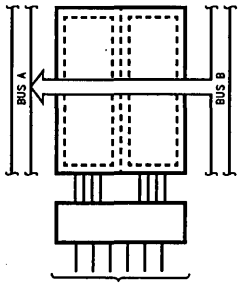
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with this device.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

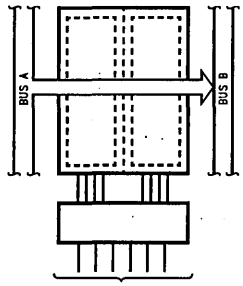
Note A: Real-Time Transfer Bus B to Bus A



TL/F/10950–6

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

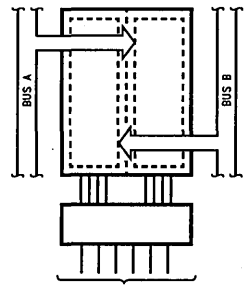
Note B: Real-Time Transfer Bus A to Bus B



TL/F/10950–7

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

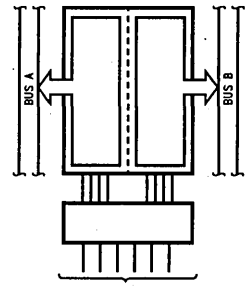
Note C: Storage



TL/F/10950–8

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↗	X	X	X
L	X	X	↗	X	X
L	H	↗	↗	X	X

Note D: Transfer Storage Data to A or B



TL/F/10950–9

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	X

FIGURE 1

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	**$\overline{OEBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**	**A_0 thru A_7**	**B_0 thru B_7**	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5.0	μA	Max	V_{IN} = 2.7V (Non I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V_{IN} = 7.0V (Non I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V (Non I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current			−225	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V (A_n, B_n)
I_{CCH}	Power Supply Current		15	22	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		40	49	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		15	22	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74BCT $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Max. Clock Frequency	90	172		90		MHz	8–1
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.8 2.8	5.9 5.1	8.8 8.8	2.8 2.8	9.9 9.9	ns	8–3
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.7 2.4	4.6 5.8	7.5 9.2	1.7 2.4	8.9 9.8	ns	8–3
t_{PLH} t_{PHL}	Propagation Delay SBA to A or SAB to B	3.0 2.4	7.0 6.6	11.0 11.0	3.0 2.4	11.3 11.3	ns	8–3
t_{PZH} t_{PZL}	Enable Time *OEBA to A	2.5 3.2	5.5 6.3	8.9 10.1	2.5 3.2	10.6 10.6	ns	8–5
t_{PHZ} t_{PLZ}	Disable Time *OEBA to A	1.8 2.4	5.4 5.4	8.6 8.6	1.8 2.4	9.5 9.5		
t_{PZH} t_{PZL}	Enable Time OEAB to B	1.5 2.3	4.6 5.2	7.1 8.1	1.5 2.3	8.1 8.1		
t_{PHZ} t_{PLZ}	Disable Time OEAB to B	2.2 2.2	5.2 5.2	9.1 8.0	2.2 2.2	9.1 8.0	ns	8–5

AC Operating Requirements: See Section 8 for Waveforms

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW, Bus to Clock	5.0 5.0		5.0 5.0		ns	8–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW, Bus to Clock	1.0 1.0		1.0 1.0		ns	8–6
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0		5.0 5.0		ns	8–4

Extended AC Electrical Characteristics

Symbol	Parameter	74BCT T_A = Com V_{CC} = Com C_L = 50 pF 8 Outputs Switching (Note 1)		74BCT T_A = Com V_{CC} = Com C_L = 250 pF 1 Output Switching (Note 2)		74BCT T_A = Com V_{CC} = Com C_L = 250 pF 8 Outputs Switching (Notes 1, 2)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2.8	10.5	3.0	12.0	4.0	15.6	ns
t_{PHL}	Clock to Bus	2.8	10.5	3.0	12.0	4.0	15.6	
t_{PLH}	Propagation Delay	2.0	9.5	2.5	10.9	4.0	15.0	ns
t_{PHL}	Bus to Bus	3.0	11.0	3.0	11.5	4.0	15.0	
t_{PLH}	Propagation Delay							
t_{PHL}	SBA to A or	3.0	12.5	3.0	14.2	4.0	18.1	ns
	SAB to B	3.0	12.5	3.0	14.2	4.0	18.1	

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitor the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	6.0	pF	V_{CC} = 5.0V (Control Inputs)
$C_{I/O}$	Input/Output Pin Capacitance	12.5	pF	V_{CC} = 5.0V (A_n, B_n)

National Semiconductor

74BCT2952
8-Bit Registered Transceiver

General Description

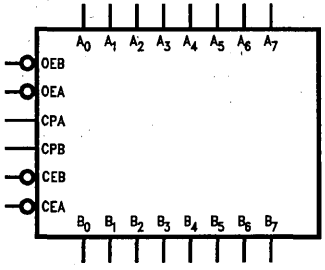
The 'BCT2952 is an 8-bit registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The output pins are guaranteed to sink 64 mA.

Features

- Separate clock, clock enable and TRI-STATE output enable provided for each register
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbols



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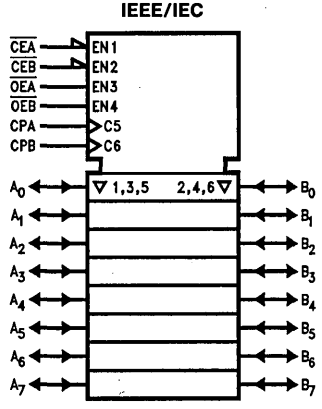

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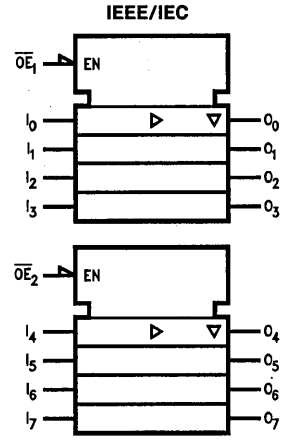
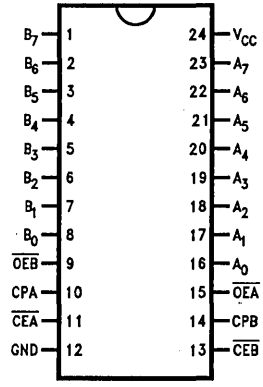


TL/F/10947–3

Connection Diagram

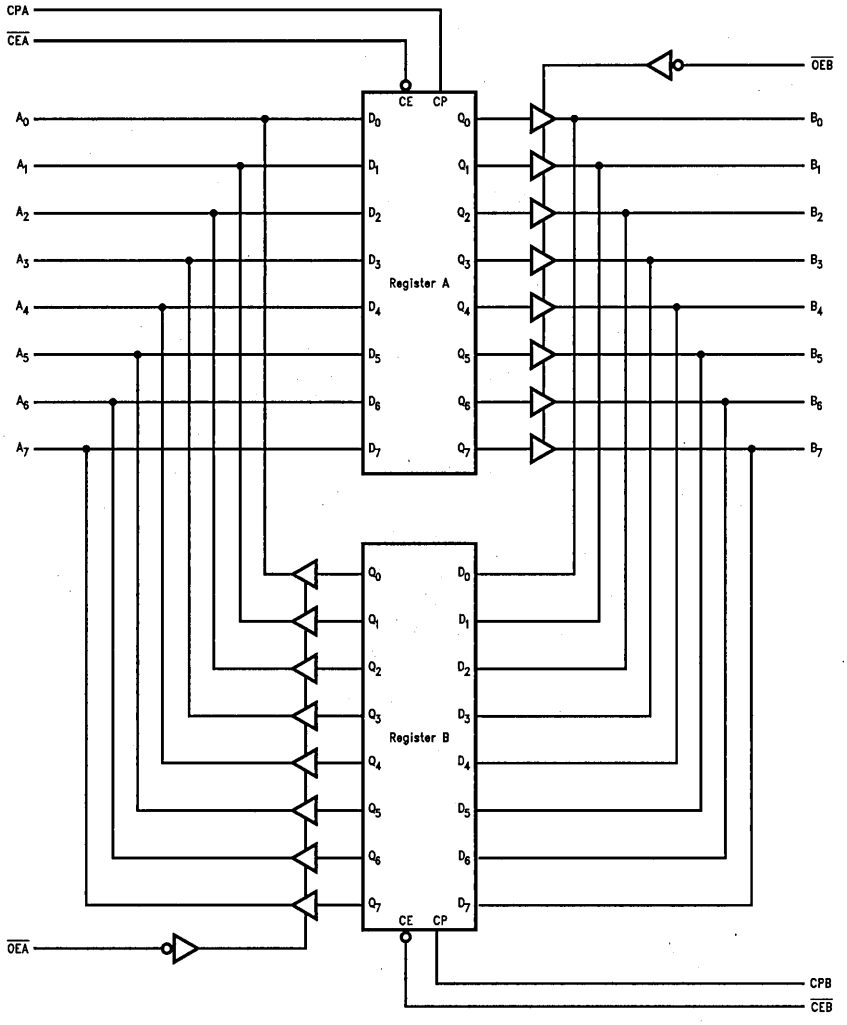
Pin Assignment for DIP and SOIC



TL/F/10947–4

Pin Names	Description
A_0–A_7	A-Register Inputs/B-Register TRI-STATE Outputs
B_0–B_7	B Register Inputs/A-Register TRI-STATE Outputs
$\overline{OEA}$	Output Enable A-Register
CPA	A-Register Clock
$\overline{CEA}$	A-Register Clock Enable
$\overline{OEB}$	Output Enable B-Register
CPB	B-Register Clock
$\overline{CEB}$	B-Register Clock Enable

Block Diagram



TL/F/10947–6

Output Control

OE	Internal Q	Y-Output	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	CE		
X	X	H	NC	Hold Data
L	⌐	L	L	Load Data
H	⌐	L	H	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5.0	μA	Max	V_{IN} = 2.7V (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−250	mA	Max	V_{IN} = 0.5V (Non-I/O Pins)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{IH} + I_{OZH}	Output Leakage Current			70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current			−225	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V (A_n, B_n)
I_{CCH}	Power Supply Current		15	22	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		40	49	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		15	22	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for waveforms and configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A, V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	90	130		90		MHz	8-1
t_{PLH} t_{PHL}	Propagation Delay CPA or CPB to A_n or B_n	2.9 2.9	5.5 5.0	8.1 8.1	2.9 2.9	8.1 8.1	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	3.4 4.0	5.6 6.6	8.9 10.3	3.4 4.0	8.9 10.3	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.1 2.9	4.4 5.6	7.4 8.5	2.1 2.9	7.4 8.5	ns	8-5

AC Operating Requirements: See Section 8 for waveforms and configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n to CPA or CPB	5.5 5.5		5.5 5.5		ns	8-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n to CPA or CPB	0.0 0.0		0.0 0.0		ns	8-6
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CBP	7.7 7.7		7.7 7.7		ns	8-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	0.0 0.0		0.0 0.0		ns	8-6
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	4.0 4.0		4.0 4.0		ns	8-4

Extended AC Electrical Characteristics

Symbol	Parameter	74BCT T_A = Com V_{CC} = Com C_L = 50 pF 8 Outputs Switching (Note 1)		74BCT T_A = Com V_{CC} = Com C_L = 250 pF 1 Output Switching (Note 2)		74BCT T_A = Com V_{CC} = Com C_L = 250 pF 8 Outputs Switching (Notes 1, 2)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	8.5	3.0	10.5	4.0	14.0	ns	8-3
t_{PHL}	CPA or CPB to A_n or B_n	3.0	8.5	3.0	10.5	4.0	14.0		

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	6.8	pF	V_{CC} = 5.0V (Control Inputs)
$C_{I/O}$	Input/Output Pin Capacitance	13.0	pF	V_{CC} = 5.0V (A_n, B_n)

National Semiconductor

74BCT827B
10-Bit Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'BCT827B 10-bit buffer and line driver provides high performance bus interface buffering for wide data/address paths or buses carrying parity. This device is designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

The 'BCT827B is a functional and pin compatible replacement for the TI 'BCT29827B.

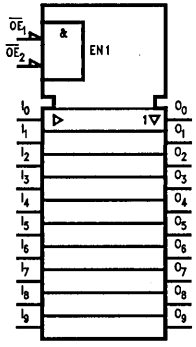
Features

- Non-inverting buffers
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbol

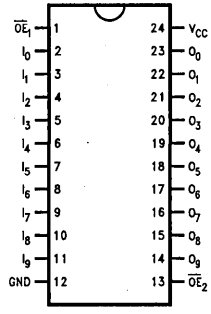
IEEE/IEC



TL/F/10918–1

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10918–2

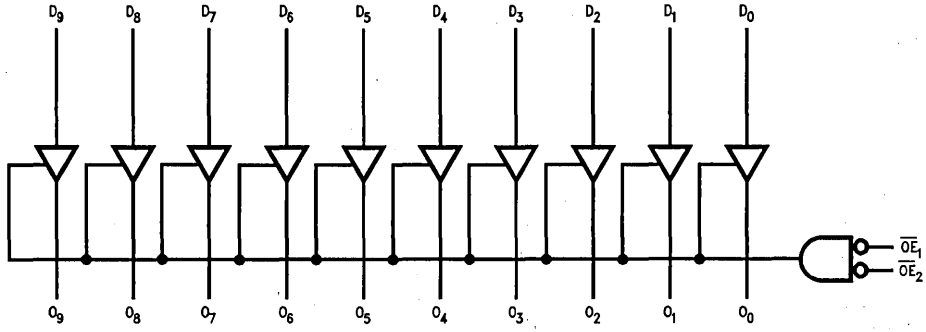
Truth Table

$\overline{OE}_n$	I_n	O_n
L	H	H
L	L	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active LOW)
I_0–I_7	Inputs
O_0–O_7	Outputs

Logic Diagram



TL/F/10918–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
Junction Temperature Under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −24 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−200	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−250	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		10.8	15	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		33.4	40	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		4	6	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0 2.0	2.7 4.6	5.3 7.3	1.0 1.5	5.5 7.5	ns	8–3
t_{PZH} t_{PZL}	Output Enable Time	4.0 4.0	8.4 7.1	11.0 11.0	4.0 4.0	12.0 12.0	ns	8–5
t_{PHZ} t_{PLZ}	Output Disable Time	1.0 1.0	4.3 5.0	7.6 7.6	1.0 1.0	8.4 8.4	ns	8–5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.8		0.8	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.7		1.0	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			4.0		6.0	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			4.0		5.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 4.0	6.5 9.5	3.5 4.5	7.5 9.5	ns	8–3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	15.0	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT2827C
10-Bit Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

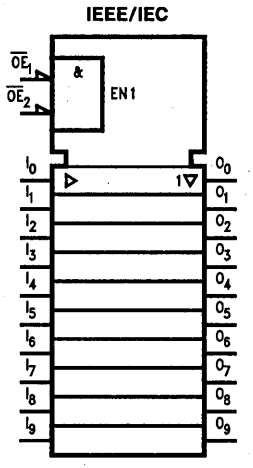
The 'BCT2827C 10-bit buffer and line driver provides high performance bus interface buffering for wide data/address paths or buses carrying parity. This device is designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers or bus-oriented transmitters/receivers. The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

- 25Ω series resistors in outputs eliminate the need for external resistors
- Non-inverting buffers
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

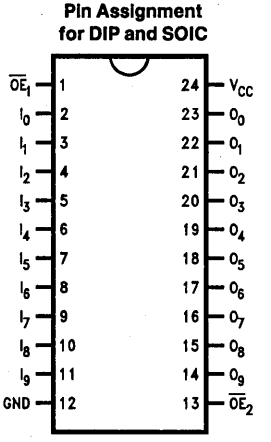
Ordering Code: See Section 11

Logic Symbol



TL/F/10916–1

Connection Diagram



TL/F/10916–2

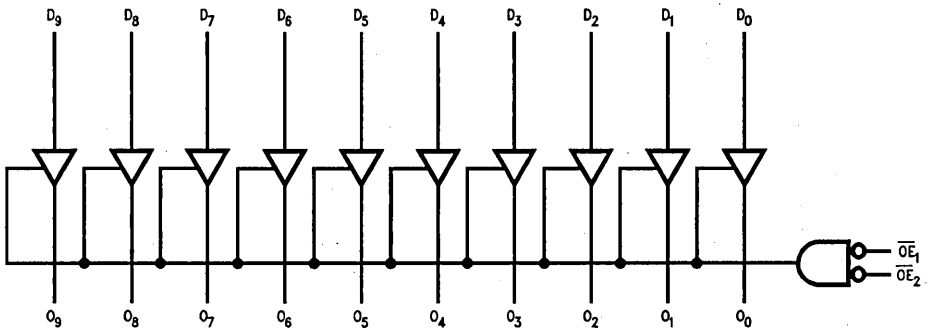
Truth Table

$\overline{OE}_n$	I_n	O_n
L	H	H
L	L	L
H	X	Z

H = HIGH Voltage Level
X = Immaterial
L = LOW Voltage Level
Z = High Impedance

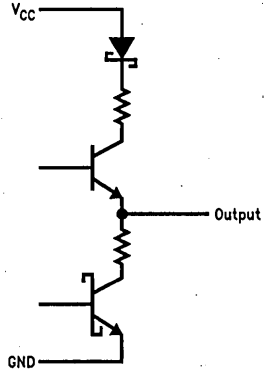
Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active LOW)
I_0–I_7	Inputs
O_0–O_7	Outputs

Logic Diagram



TL/F/10916–4

Schematic of Each Output



TL/F/10916–5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output In LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.5 0.8	V	Min	I_{OL} = 3 mA I_{OL} = 15 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−200	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		10.8	15	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		33	40	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		4	6	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.9 2.0	2.7 5.2	5.2 7.2	0.9 2.0	6.0 7.8	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	4.0 5.0	7.6 7.8	11.0 11.0	4.0 5.0	11.5 11.5	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.3 6.1	8.5 8.5	2.0 2.0	10.0 10.0	ns	8-5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.5		0.6	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.5		0.6	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			5.0		5.0	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			5.0		5.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$ 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5 4.5	7.0 10.0	3.0 6.0	7.0 11.5	ns	8-3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	15.0	pF	$V_{CC} = 5.0V$

National Semiconductor

74BCT2828A
10-Bit Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

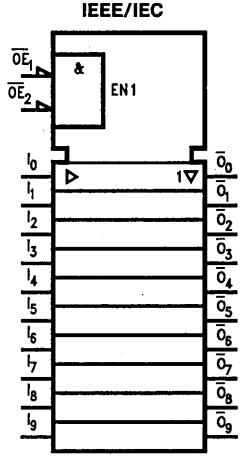
The 'BCT2828A 10-bit buffer and line driver provides high performance bus interface buffering for wide data/address paths or buses carrying parity. This device is designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers or bus-oriented transmitters/receivers. The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

- 25Ω series resistors in outputs eliminate the need for external resistors
- Inverting buffers
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

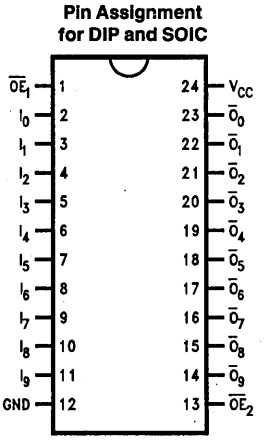
Ordering Code: See Section 11

Logic Symbol



TL/F/10917–1

Connection Diagram



TL/F/10917–2

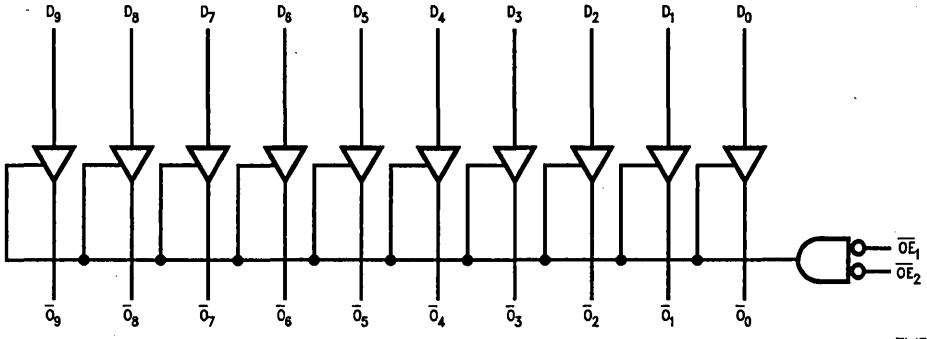
Truth Table

$\overline{OE}_n$	I_n	$\overline{O}_n$
L	H	L
L	L	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

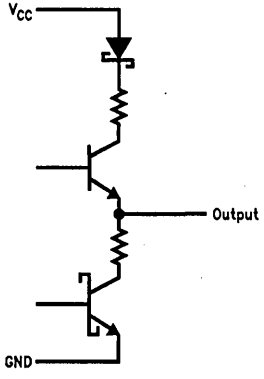
Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active LOW)
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Logic Diagram



TL/F/10917–4

Schematic of Each Output



TL/F/10917–5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State in the High State	−0.5V to +5.5V −0.5V to V_{CC}
Current Applied to Output In LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54BCT/74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.5 0.8	V	Min	I_{OL} = 3 mA I_{OL} = 15 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−200	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		5.6	10	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		31	38	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		4.0	6	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0 1.0	2.7 2.7	7.0 7.0	1.07 1.0	8.0 8.0	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	2.5 5.0	5.4 8.0	10.0 12.0	2.5 5.0	10.5 12.5	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.2 5.0	8.5 8.5	2.0 2.0	10.0 10.0	ns	8-5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.5		0.6	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.8		0.9	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			3.0		3.0	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			5.0		5.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF 8 Outputs Switching (Note 1)		74BCT $T_A = Comm$ $V_{CC} = Comm$ $C_L = 250$ pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5 2.5	8.5 8.5	3.0 4.0	8.5 9.0	ns	8-3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	15.0	pF	$V_{CC} = 5.0V$

Section 11

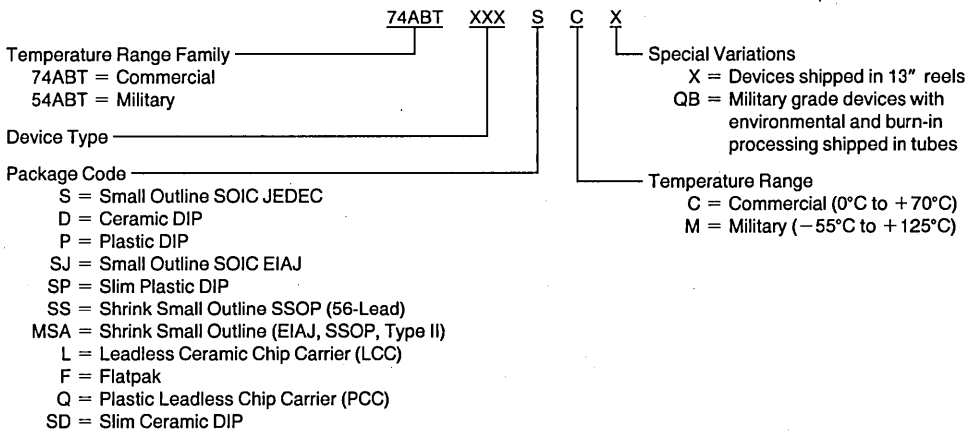
Ordering Information and Physical Dimensions

Section 11 Contents

ABTC Advanced BiCMOS Technology

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

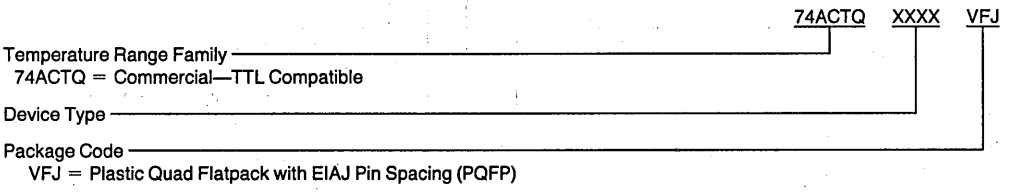


Integrated Bus Function (IBF) Family

Ordering Information

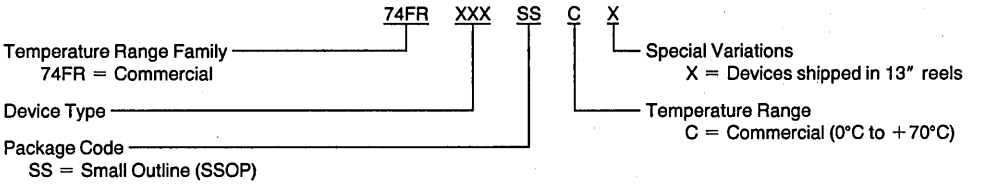
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

ACTQ3283T:



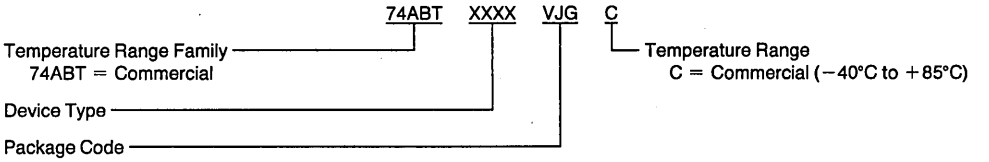
FR900 and FR25900:

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



ABT3284:

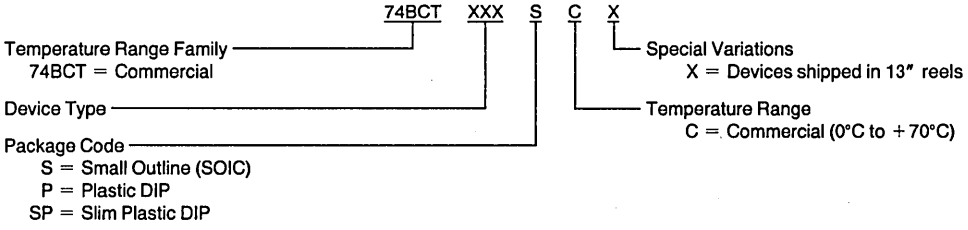
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



BCT BiCMOS Technology

Ordering Information

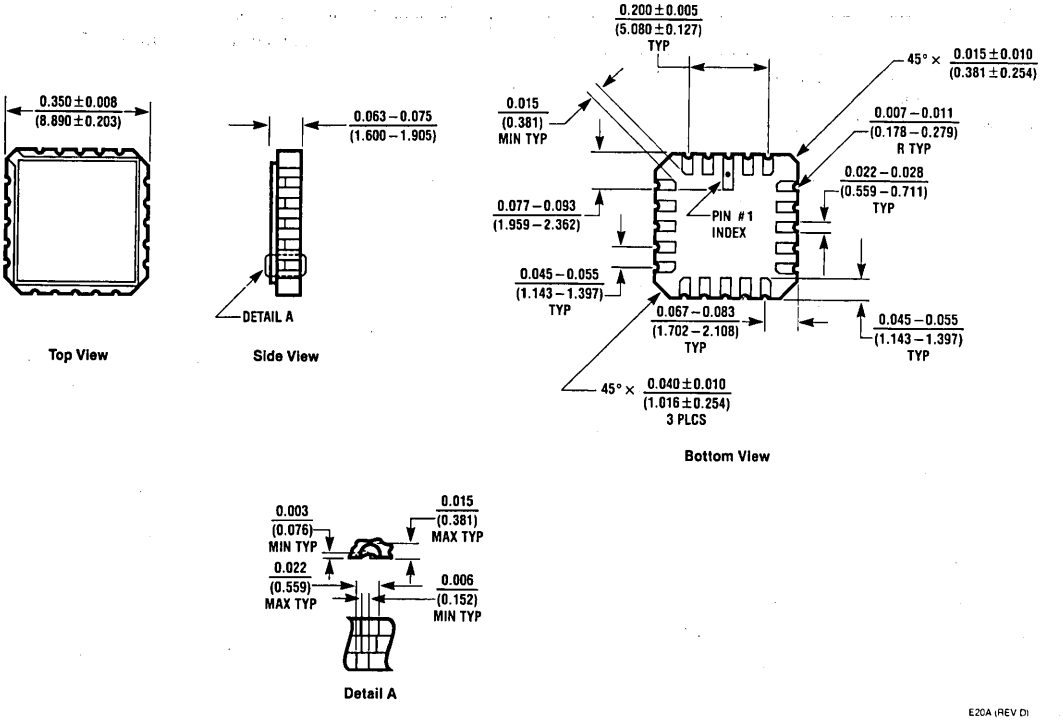
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



National Semiconductor

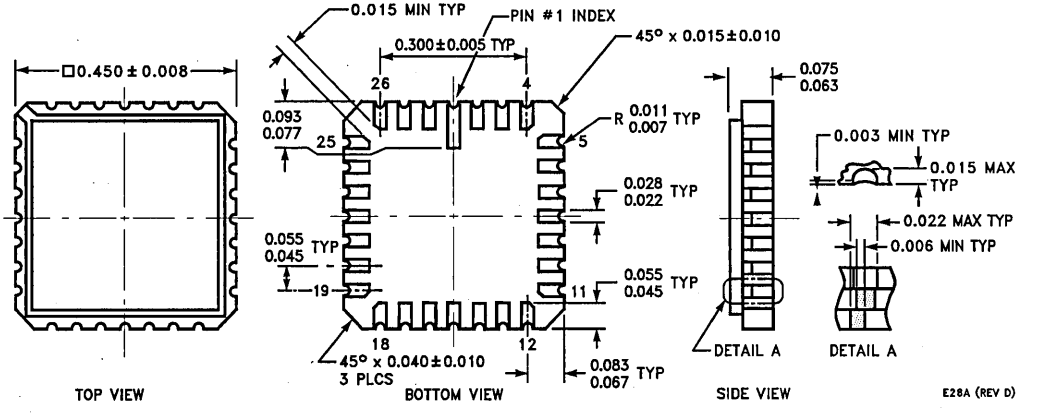
All dimensions are in inches (millimeters)

20 Lead Ceramic Leadless Chip Carrier, Type C (LCC)
NS Package Number E20A



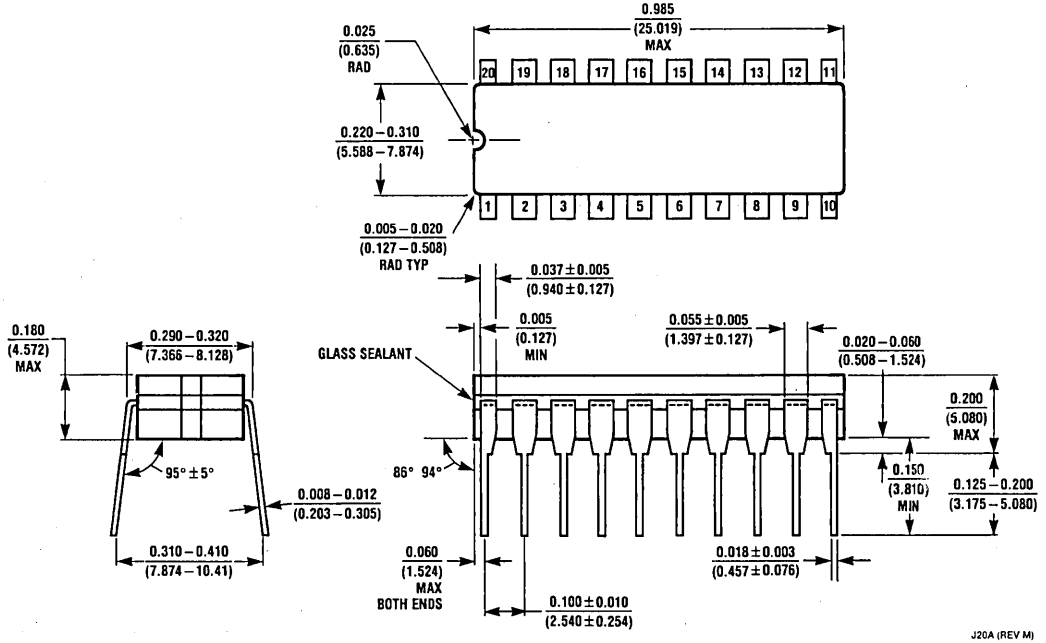
E20A (REV D)

28 Lead Ceramic Leadless Chip Carrier, Type C (LCC)
NS Package Number E28A



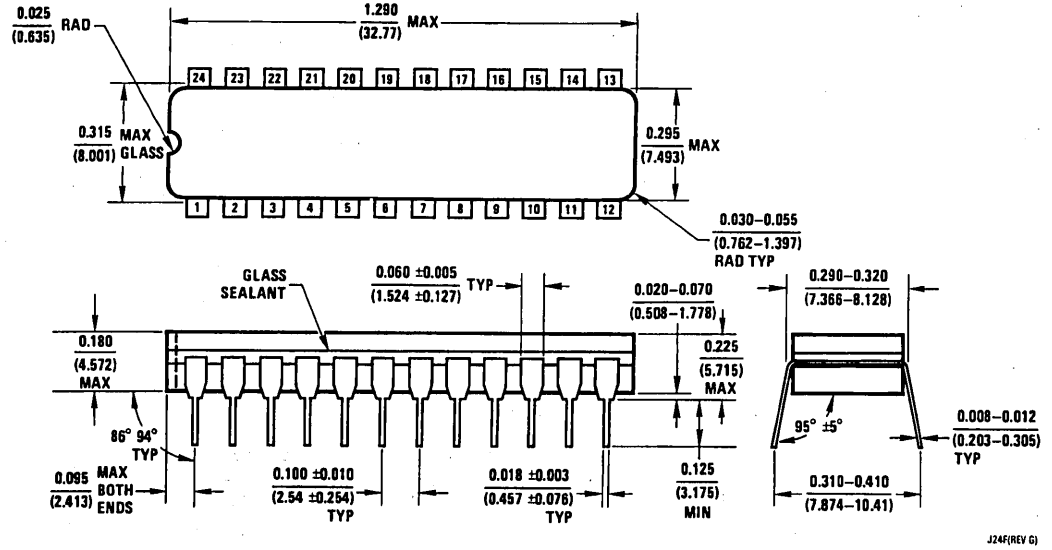
E28A (REV D)

20 Lead Ceramic Dual-in-Line Package (D)
NS Package Number J20A



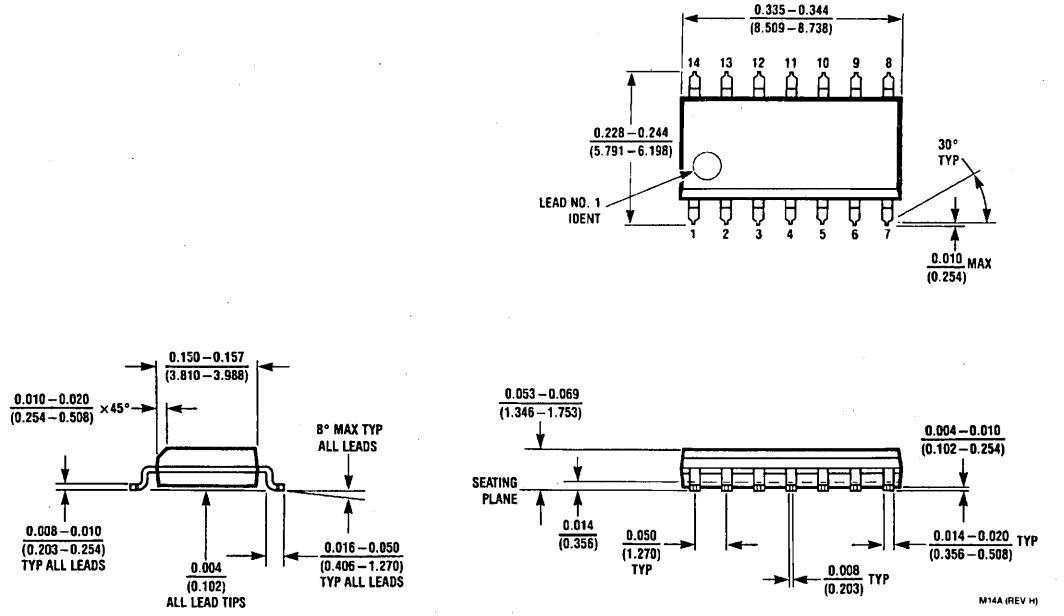
J20A (REV M)

24 Lead (0.300" Wide) Ceramic Dual-in-Line Package (D)
NS Package Number J24F

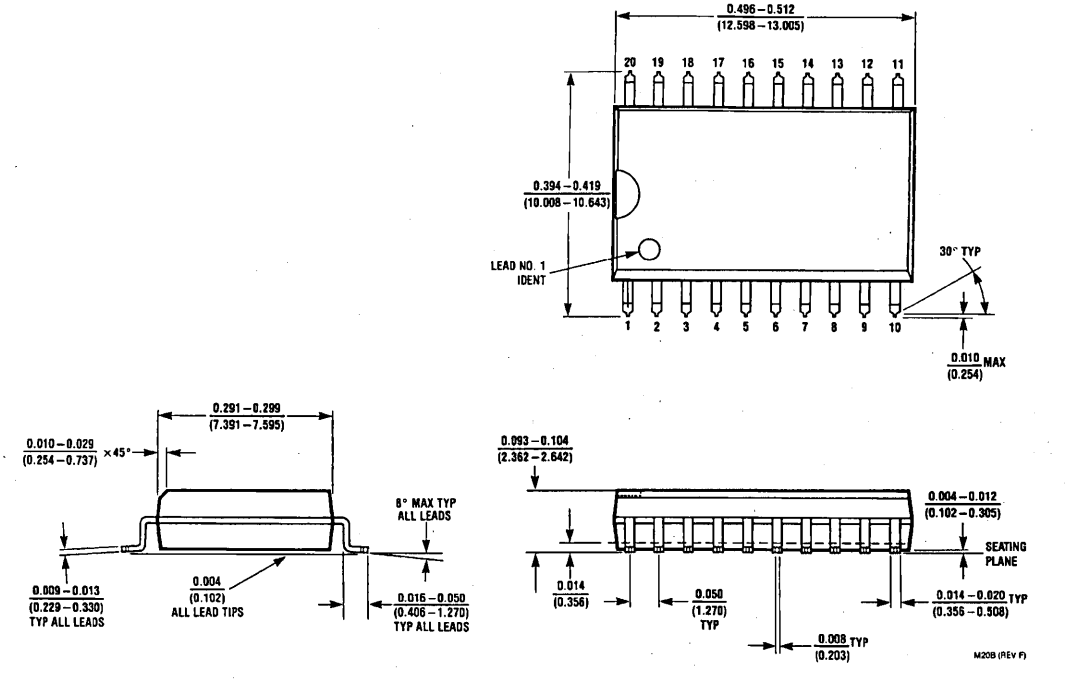


J24F(REV G)

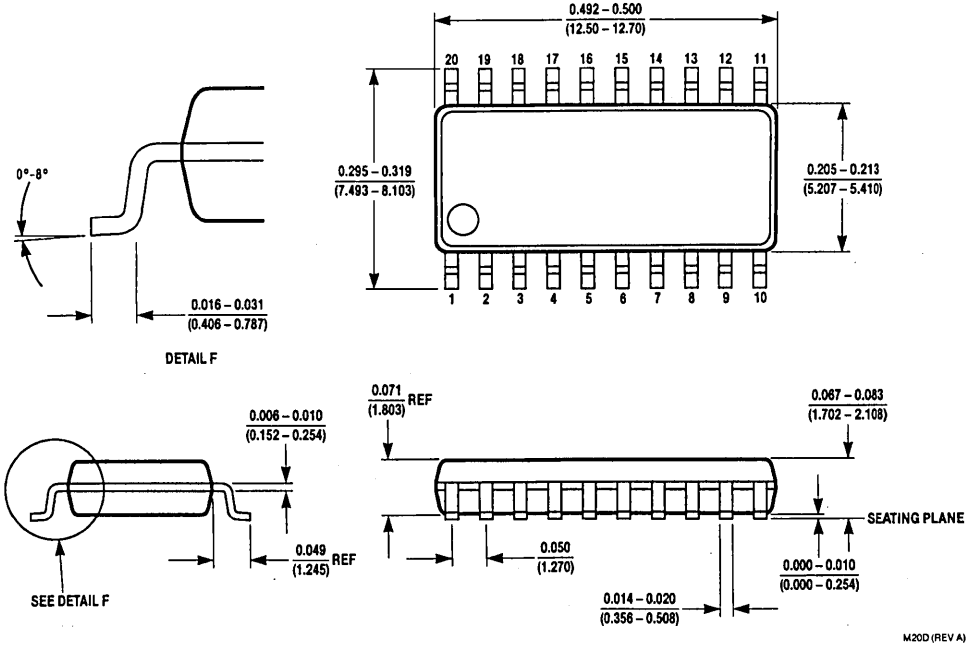
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M14A



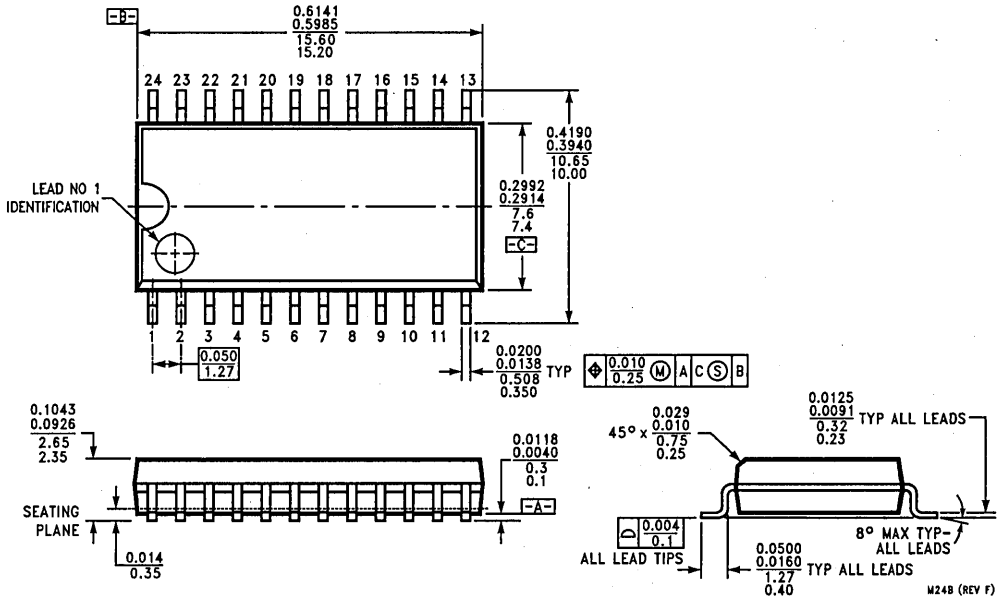
20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B



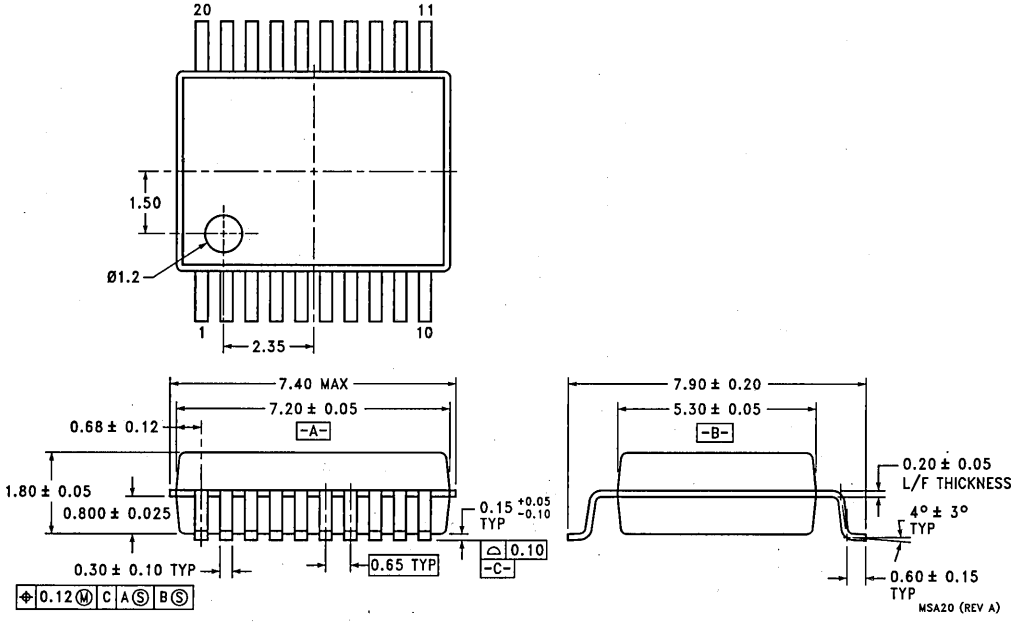
20 Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M20D



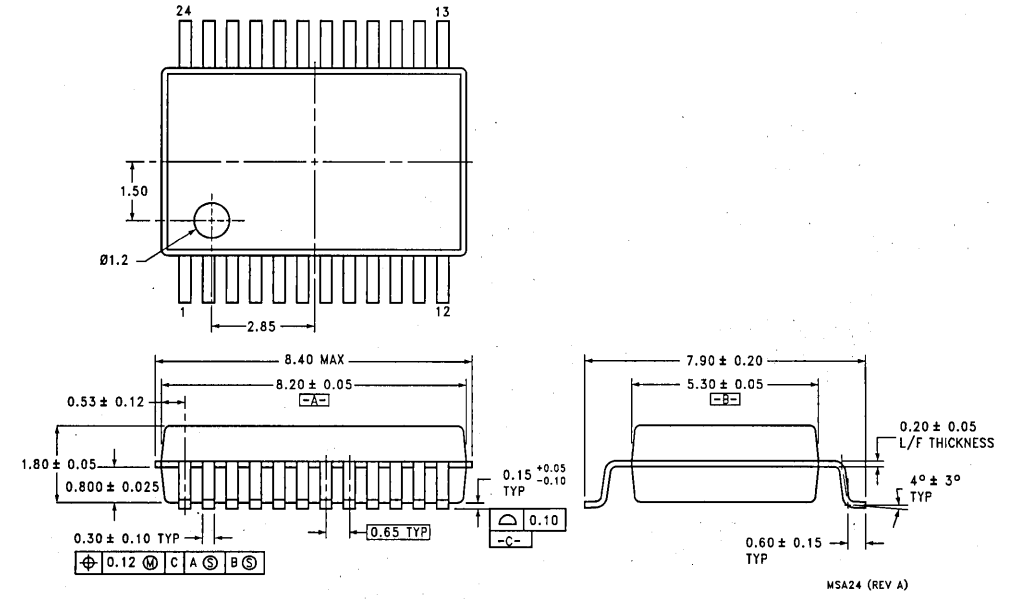
24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M24B



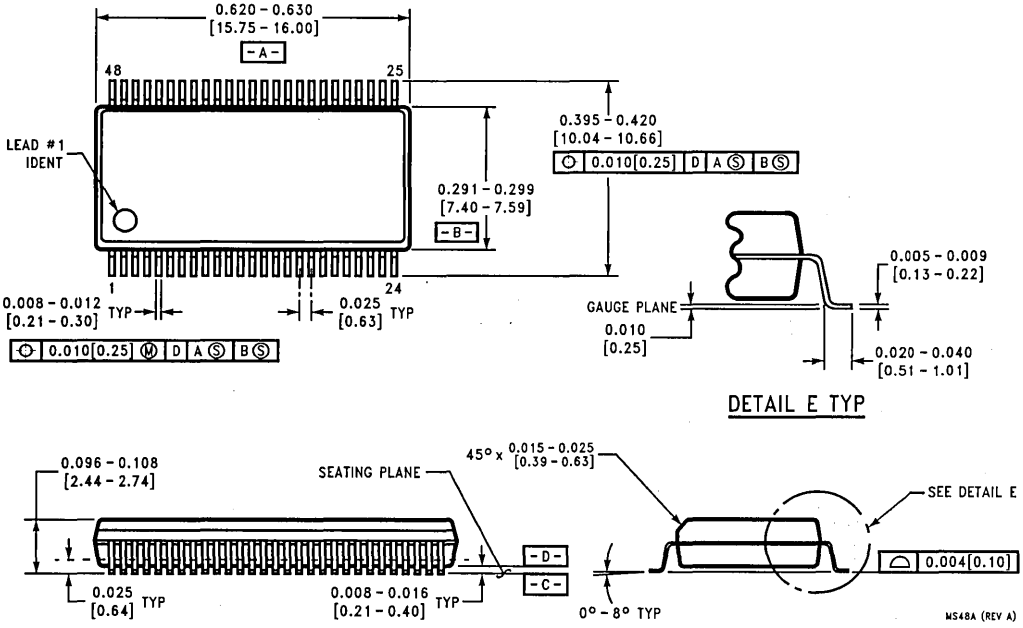
20 Lead Molded Shrink Small Outline Package, EIAJ, Type II (MSA)
NS Package Number MSA20



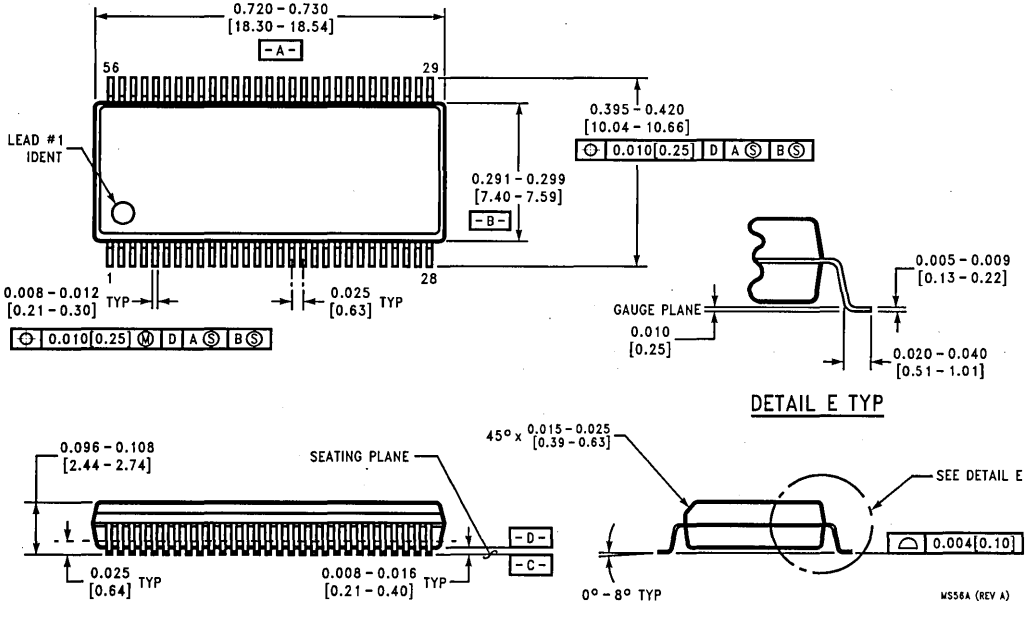
24 Lead Molded Shrink Small Outline Package, EIAJ, Type II (MSA)
NS Package Number MSA24



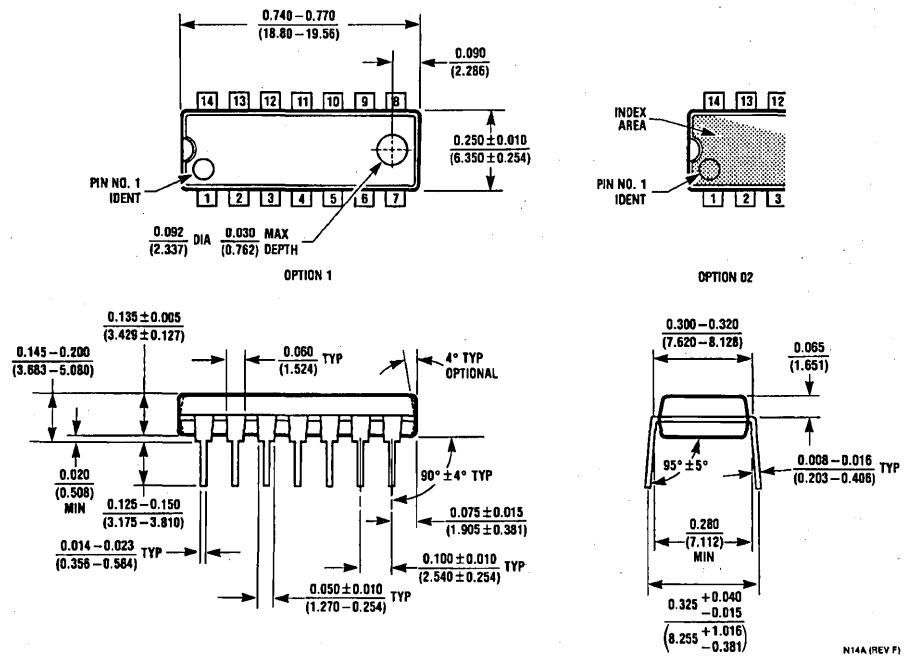
48 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC (S)
NS Package Number MS48A



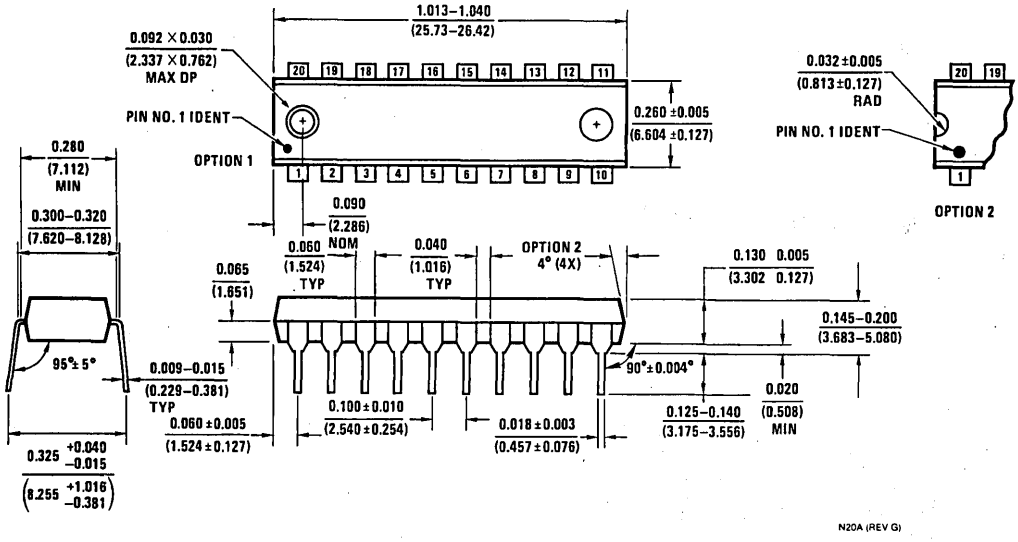
56 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC (SS)
NS Package Number MS56A



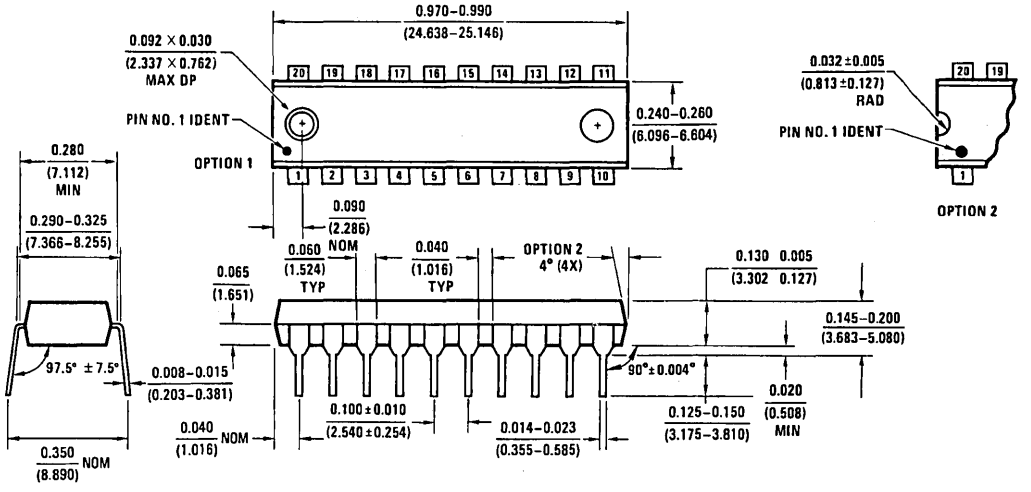
14 Lead (0.300" Wide) Molded Dual-in-Line Package (P)
NS Package Number N14A



20 Lead (0.300" Wide) Molded Dual-in-Line Package (P)
NS Package Number N20A

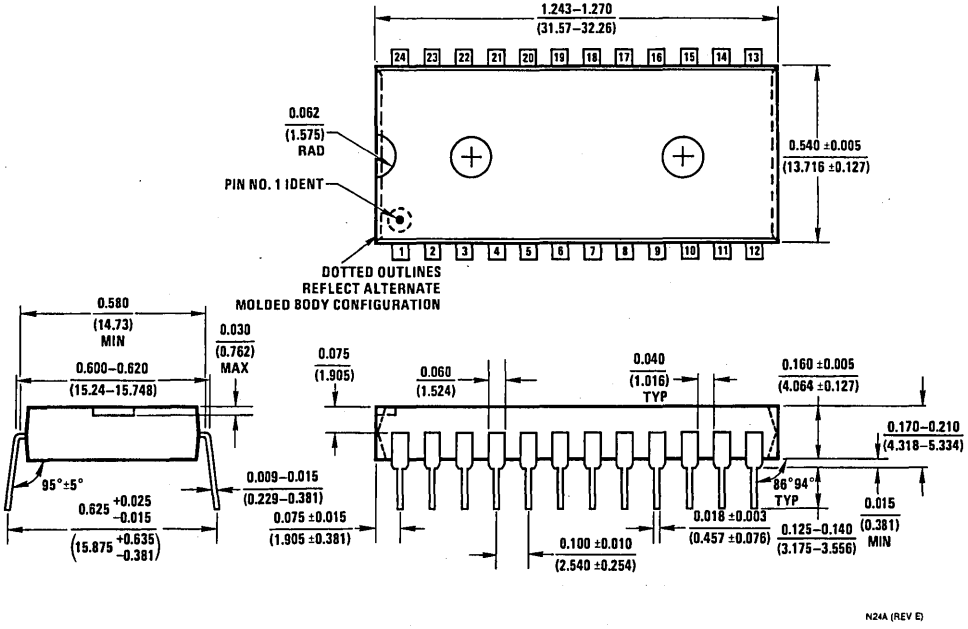


20 Lead (0.300" Wide) Molded Dual-in-Line Package (P)
NS Package Number N20B



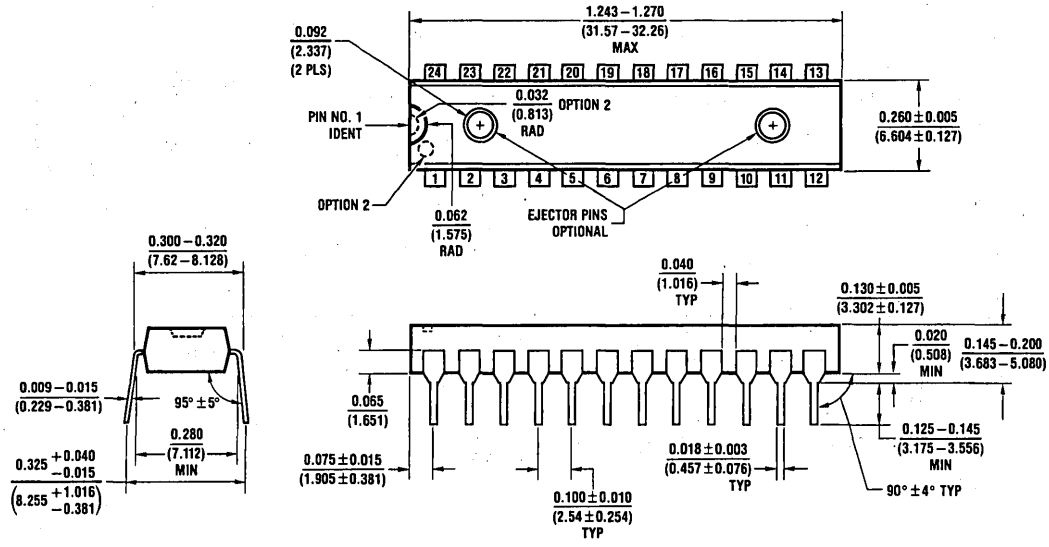
N20B (REV A)

24 Lead (0.600" Wide) Molded Dual-in-Line Package (P)
NS Package Number N24A



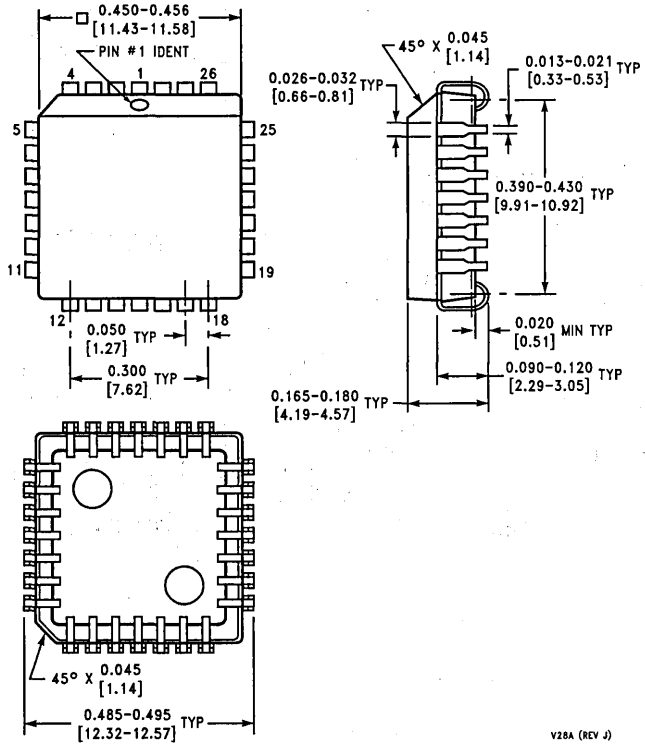
N24A (REV E)

24 Lead (0.300" Wide) Molded Dual-in-Line Package (P)
NS Package Number N24C



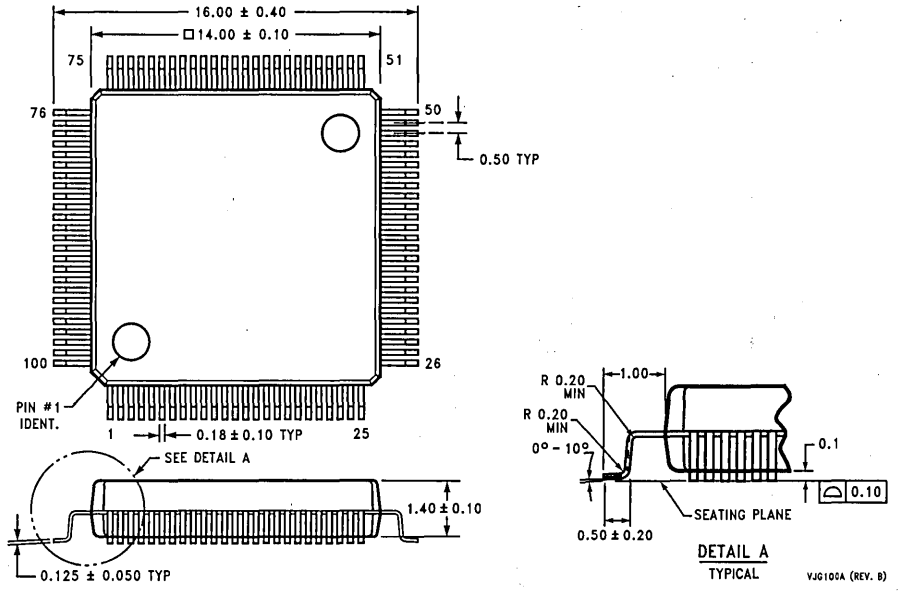
N24C (REV F)

28 Lead Molded Plastic Leaded Chip Carrier (Q)
NS Package Number V28A

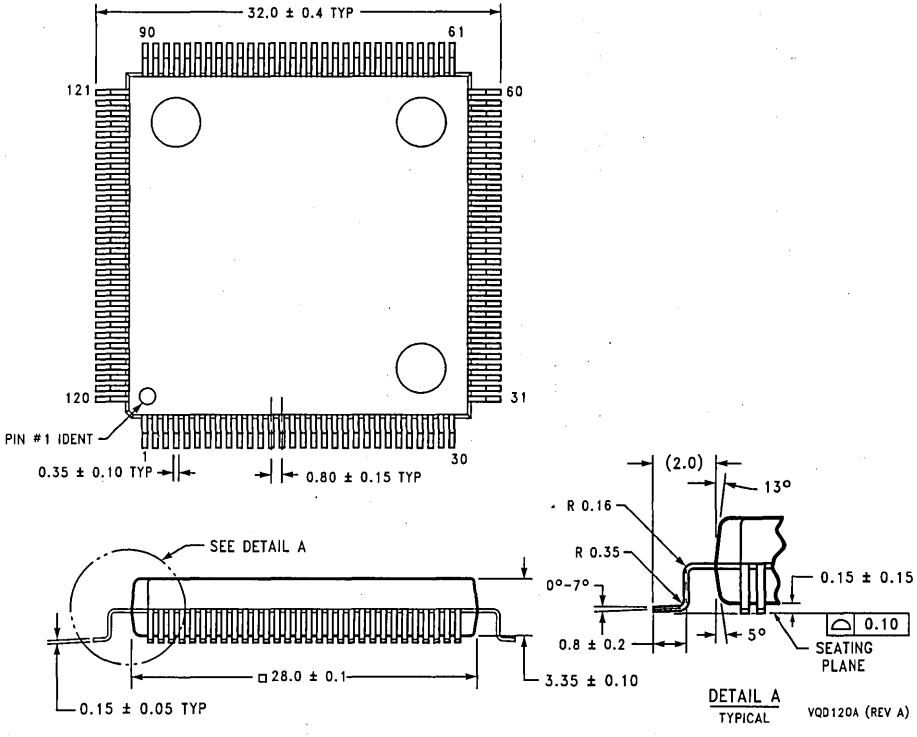


V28A (REV J)

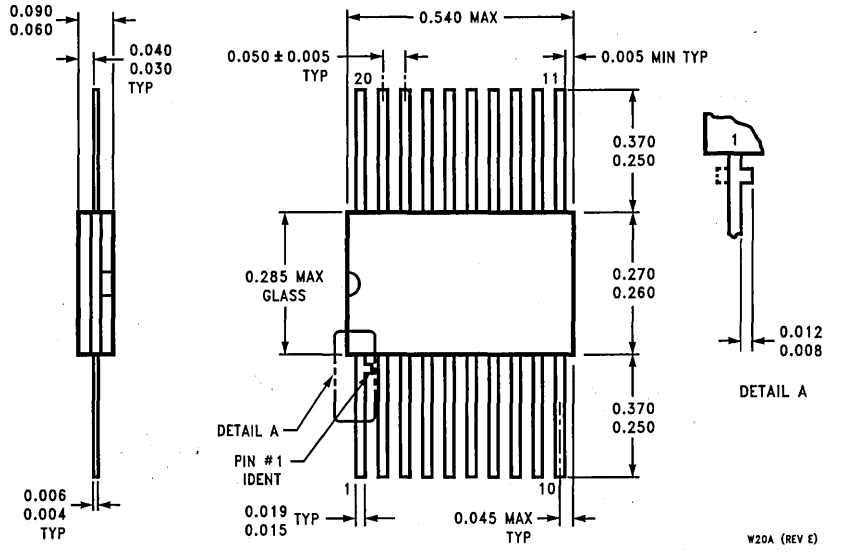
100 Lead (14mm x 14mm) Molded Plastic Quad Flat Package, JEDEC (F)
NS Package Number VJG100A



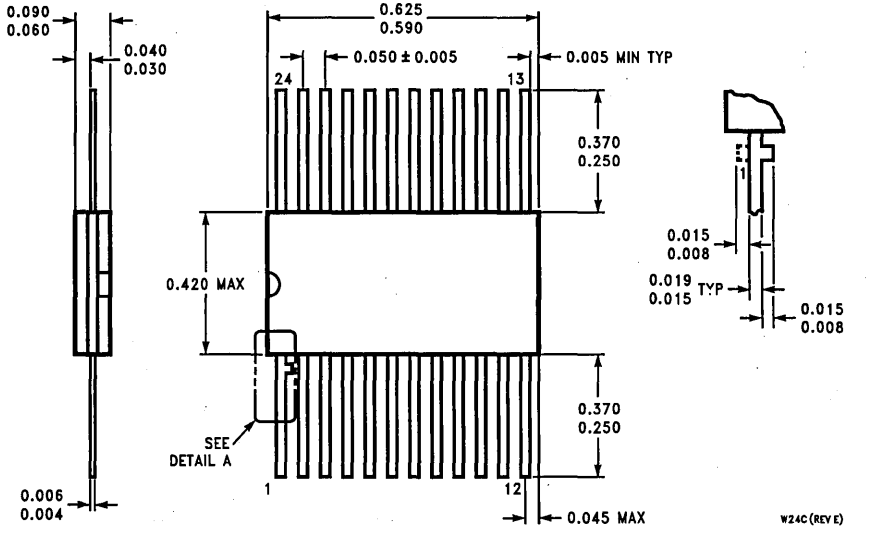
120 Lead Plastic Quad Flatpack (F)
NS Package Number VQD120A



20 Lead Cerpack (F)
NS Package Number W20A



24 Lead Cerpack (F)
NS Package Number W24C



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54/74ACTQ3283 32-Bit Latchable Transceiver with Parity Generator/Checker and Byte Multiplexing
54/74ABTCXXX • 74BCTXXX

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Microprocessor Applications

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