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National Semiconductor

Clock Generation and Support (CGS™) Design Databook

CLOCK GENERATION AND SUPPORT

DATABOOK

1994 Edition

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Clock Generation & Support (CGS™) Family

Introduction

National Semiconductor has developed this handbook to help customers with the design of high-speed clock applications. It contains complete and comprehensive device performance data to assist designers and component engineers in their unique clock distribution applications. Included are skew performance specifications developed by National Semiconductor and discussion of the significance of these specifications as they relate to the end system. Also shown are the Clock Generation and Support (CGS) product's typical and maximum specifications and product functionality and additional characterization data such as power vs frequency, skew performance for unbalanced loads, and derating curves which show the skew performance for balanced output loads across frequency and load. A discussion on clock modeling and its importance in system design along with the required information for modeling is also provided. Finally, criteria for selection is presented with data sheets for National's currently available CGS products.

Clock Generation and Support has become one of the key design areas enabling today's CISC and RISC based systems to obtain maximum operating frequencies. The primary goal of the system clock is to deliver a clock signal to each component's input pins which meets the system's requirements for: signal skew; acceptable waveshape (rise and fall time, overshoot, undershoot, voltage swings), and stability (cycle-to-cycle). The components of clock skew include both intrinsic skew (pin-to-pin skew within a single chip) and extrinsic skew (clock skew generated from trace routing and loading).

National's CGS product strategy is to develop devices to meet customer needs for high speed clock generation and support applications. What CGS offers today is a series of optimal solutions for clock distribution applications requiring devices with high fanout and with guaranteed skew specifications.

For any additional information on device performance or future product availability please contact the National Customer Response Center at 1-800-CRC-9959 or your local sales office.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Alpha-Numeric Index (Continued)

Device	V_{CC}	Frequency (MHz)	T_{OS} (pS)	No. of Outputs	T_{RISE}/T_{FALL}	Technology	Grade	Package
LOW SKEW CLOCK BUFFERS/DRIVERS								
CGS74CT2524	4.5–5.5	100	450	1/4	1.5/1.5	TTL/CMOS	Com/Ind	8 Pin M,N
CGS74LCT2524	3.0–3.6	45	450	1/4	1.5/1.5	TTL/CMOS	Com/Ind	8 Pin M,N
CGS74B2525	4.5–5.5	50	1000	1/8	1.9/1.2	TTL	Com/Ind/Mil	14 Pin M,N
CGS74C2525	4.5–5.5/3.0–3.6	50	700	1/8	1.1/1.1	CMOS	Com/Ind/Mil	14 Pin M,N
CGS74CT2525	4.5–5.5/3.0–3.6	50	700	1/8	1.1/1.1	TTL/CMOS	Com/Ind/Mil	14 Pin M,N
CGS74C2526	4.5–5.5/3.0–3.6	50	700	2/8	1.1/1.1	CMOS	Com/Ind/Mil	16 Pin M,N
CGS74CT2526	4.5–5.5/3.0–3.6	50	700	2/8	1.1/1.1	TTL/CMOS	Com/Ind/Mil	16 Pin M,N
CGS74CT2527	4.5–5.5	100	550	1/8	1.1/1.1	TTL/CMOS	Com/Ind	28 Pin V
CGS74B2528	4.5–5.5	80	550	1/10	1.5/1.5	TTL	Com/Ind	16 Pin M,N,V
CGS74B2529	4.5–5.5	80	550	2/10	1.5/1.5	TTL	Com/Ind	16 Pin M,N,V
CGS100P2530	4.5–5.5	70	550	1/10	1.5/1.5	PECL	Com/Ind	28 Pin V
CGS100P2531	4.5–5.5	70	550	2/10	1.5/1.5	PECL	Com/Ind	28 Pin V
CGS74B303	4.5–5.5	110	1000	1/8	2.0/2.0	TTL	Com/Ind	28 Pin V,16 Pin M,N
CGS74B304	4.5–5.5	110	900	1/8	2.0/2.0	TTL	Com/Ind	28 Pin V,16 Pin M,N
CGS74B305	4.5–5.5	130	750	1/8	2.0/2.0	TTL	Com/Ind	28 Pin V,16 Pin M,N
CGS2534	4.75–5.25	100	500	4/16	1.5/1.5	TTL	Com/Ind	28 Pin V
CGS2535	4.5–5.5/3.0–3.6	85	500	4/16	1.5/1.5	TTL/CMOS	Com/Ind	28 Pin V
CGS2536	4.5–5.5/3.0–3.6	85	500	4/16	1.5/1.5	TTL/CMOS	Com/Ind	28 Pin V
CGS2537	4.75–5.25	100	500	4/16	1.5/1.5	TTL	Com/Ind	28 Pin V
100310	ECL	750	75	2/8	0.75/0.75	ECL	Com/Ind	28 Pin Q
100311	ECL	750	75	1/9	0.75/0.75	ECL	Com/Ind	28 Pin Q
100315	ECL	750	75	2/4	0.75/0.75	ECL	Com/Ind	16 Pin F,S
LOW SKEW PLL CLOCK GENERATORS								
CGS74C800/801/802	4.5–5.5	130	500	2/8	1.5/1.5	CMOS	Com/Ind	28 Pin V
CGS74CT800/801/802	4.5–5.5	130	500	2/8	1.5/1.5	TTL/CMOS	Com/Ind	28 Pin V
CGS74LCT800/801/802	3.0–3.6	100	500	2/8	1.5/1.5	TTL/CMOS	Com/Ind	28 Pin V
CGS700	4.5–5.5	160	500	2/9	1.5/1.5	CMOS	Com	28 Pin V
CGS701	4.5–5.5	160	500	2/7	1.5/1.5	CMOS	Com/Ind	28 Pin V
VIDEO CLOCK GENERATORS								
CGS410	4.75–5.25	135	N/A	1/2	4	CMOS	Com	28 Pin V
LM1881	5–12	150 (kHz)	N/A	N/A	N/A	CMOS	Com/Mil	8 Pin M,N
LM1882	4.5–5.5	130	N/A	N/A	N/A	CMOS	Com	20 Pin M,N,L
CRYSTAL CLOCK GENERATORS								
CGS3310-19	4.5–5.5	110	N/A	1/1	1-4 (pgmable)	CMOS	Com/Ind	8 Pin M
CGS3321-22	4.5–5.5	110	N/A	1/1	1-4 (pgmable)	CMOS	Com/Ind	8 Pin M

Note 1: Frequency is maximum MHz.

Note 2: T_{OS} is the maximum LH or HL pin-to-pin skew in picoseconds.

Note 3: T_{RISE} and T_{FALL} numbers are maximum edge rates in picoseconds.

Section 1

Definitions and Test Philosophy

Section 1 Contents

National Semiconductor

Definitions and Test Philosophy

Test Philosophy

Minimizing output skew is a key design criteria in today's high-speed clocking schemes. National has incorporated new skew specifications into the CGS family of devices. National's test philosophy is to fully test guarantee all the available skew specifications in order to help clock designers optimize their clock budgets. In addition to these specifications, National's CGS family also provides extensive bench performance data for skew, rise and fall times, and duty cycle over various output and input conditions in order to provide designers *real-life* performance data.

This section provides general definitions and examples of skew and then discusses National's CGS bench performance methods and examples. The actual performance data can be found in Section 3.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s).

Example:

If signal appears at out #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

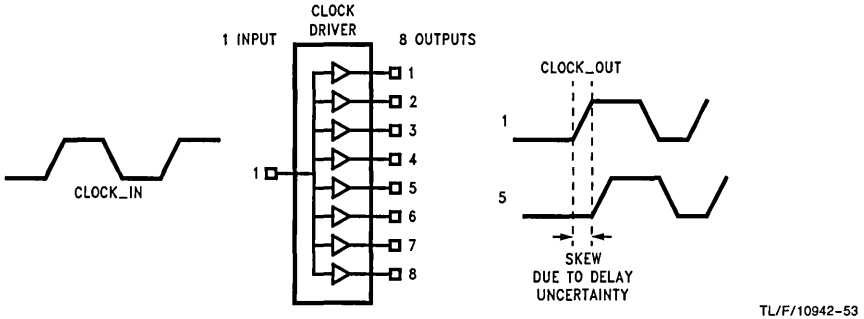

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FIGURE 1-1. Clock Output Skew

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device, duty cycle and device-to-device delay differences.

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

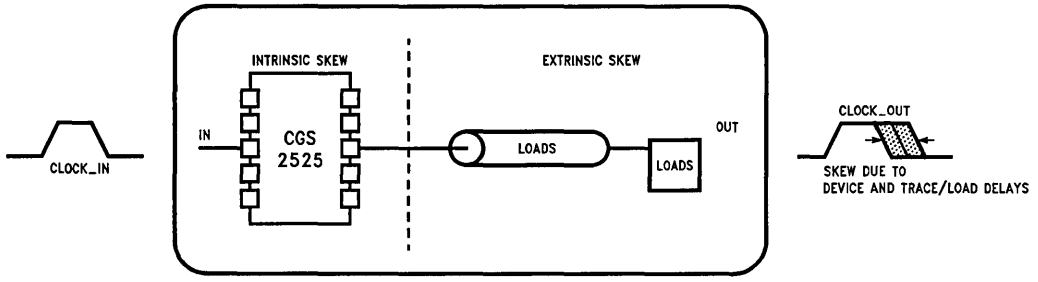

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FIGURE 1-2. Sources of Clock Skew

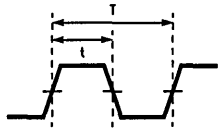
Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles
Total system skew budget = 10% of clock cycle = 2 ns* → 2 ns
If extrinsic skew = 1 ns → − 1 ns
Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design *Rule of thumb.*

CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is *High* or *Low* in a given clock cycle.



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Duty Cycle = t/T * 100%

FIGURE 1-3. Duty Cycle Calculation

Clock Signal

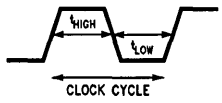

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FIGURE 1-4. Clock Cycle

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.

Clock + Skew

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FIGURE 1-5. Clock Skew

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE 1-I

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle		
50 MHz	0 ns	10 ns	10 ns	50/50%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%		
50 MHz	1 ns	11 ns	9 ns	55/45%		
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

$t_{OSHL} = |t_{PHL_{MAX}} - t_{PHL_{MIN}}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLH_{MAX}} - t_{PLH_{MIN}}|$

Propagation delays are measured across the outputs of any given device.

Example

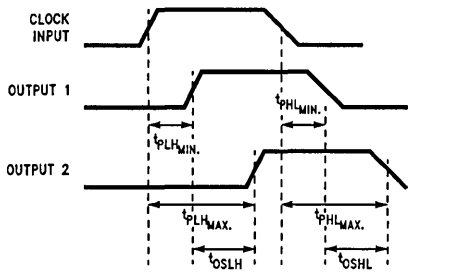

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FIGURE 1-6. t_{OSLH}, t_{OSHL}

TABLE 1-II. Guaranteed Specifications. Useful in applications requiring high fanout drivers with synchronous outputs.

Device	t_{OSHL} or t_{OSLH}	Conditions
CGS74B2525	1 ns	50 pF, 500Ω, 0°C to +70°C, V_{CC} 4.5V to 5.5V
CGS74C2525	700 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
CGS74CT2525	700 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
CGS74C2526	700 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
CGS74CT2526	700 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
100115	75 ps	50Ω, 0°C to +70°C, V_{EE} −4.2V to −4.8V

Definition of Parameters (Continued)

t_{PS} (Pin Skew or Transition Skew)

t_{PS}, describes opposite edge skews, i.e., the difference between the delay of the low-to-high transition and the high-to-low transition on the same pin. This parameter is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. Ideally this number needs to be 0 ns. Effectively, 0 ns means that there is no degradation of the input signal's Duty Cycle.

Many of today's microprocessors require a minimum of a 45:55 percent Duty Cycle. System clock designers typically achieve this in one of two ways. The first method is with an expensive crystal oscillator which meets the 45:55 percent Duty Cycle requirement. An alternative approach is to use a less expensive crystal oscillator and implement a divide by two function. Some microprocessors have addressed this by internally performing the divide by two.

Since Duty Cycle is defined as a percentage, the room for error becomes tighter as the system clock frequency increases. For example in a 25 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 4 ns (t_{PLH} of 18 ns and t_{PLH} of 22 ns) and still meet the Duty Cycle requirement. However for a 50 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 2 ns (t_{PLH} of 9 ns and t_{PHL} of 11 ns) and still meet the Duty Cycle requirement. This analysis assumes a perfect 50:50 percent Duty Cycle input signal.

Definition

t_{PS} (Pin Skew or Transition Skew):

$t_{PS} = |t_{PHL} - t_{PLH}|$

Both high-to-low and low-to-high propagation delays are measured at each output pin across the given device.

Example

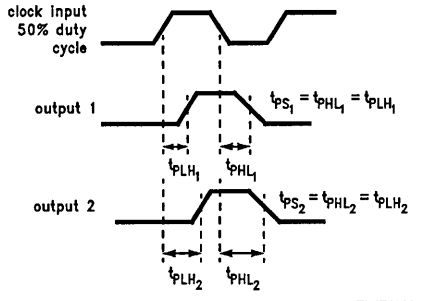

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FIGURE 1-7. t_{PS}

Example: A 33 MHz, 50/50% duty cycle input signal would be degraded by 2.6% due to a t_{PS} = 0.8 ns. (See Table and Illustration below.)

Note: Output symmetry degradation also depends on input duty cycle.

TABLE 1-III. Duty Cycle Degradation of 33 MHz

f (MHz)	Input			Device	Output			% Δ DC Input to Output
	DC Input	t_{IN} (ns)	T_{IN} (ns)	t_{PS} (ns)	t_{OUT} (ns)	T_{OUT} (ns)	DC Output	
33	50%/50%	15.15/15.15	30.3	0.8	14.35/15.95	30.3	47.4%/52.6%	2.6%
	45%/55%	13.6/16.6	30.3	1.5	12.1/18.1	30.3	39.9%/60.1%	5.1%

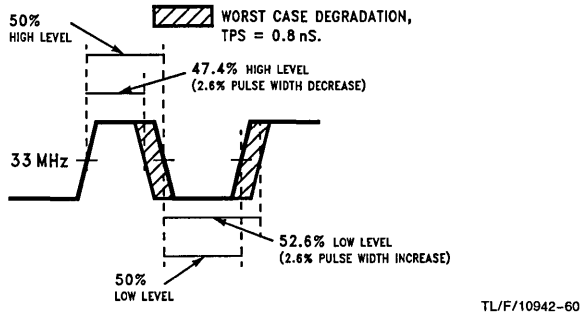

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FIGURE 1-8. Pulse Width Degradation

Definition of Parameters (Continued)

t_{OST} (Opposite Edge Skew)

t_{OST} defines the difference between the fastest and the slowest of both transitions within a given chip. Given a specific system with two components, one being positive-edge triggered and one being negative-edge triggered, t_{OST} helps to calculate the required delay elements if synchronization of the positive- and negative-clock edges is required.

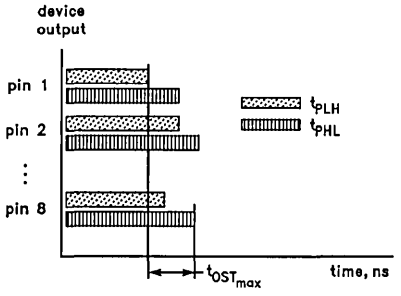

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FIGURE 1-9. t_{OST}

Definition

t_{OST} (Opposite Edge Skew):

$$t_{OST} = |t_{P\varphi m} - t_{P\varphi n}|$$

where φ is any edge transition (high-to-low or low-to-high) measured between any two outputs (m or n) within any given device.

Example

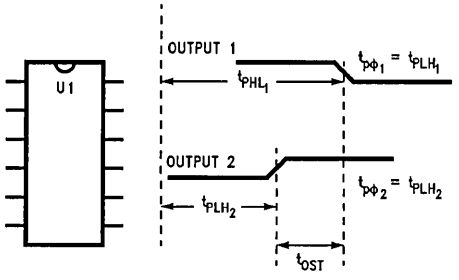

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FIGURE 1-10. t_{OST}

Definition of Parameters (Continued)

t_{PV} (Part Variation Skew)

t_{PV} illustrates the distribution of propagation delays between the outputs of any two devices.

Part-to-part skew, t_{PV}, becomes a critical parameter as the driving scheme becomes more complicated. This usually applies to higher-end systems which go from single clock drivers to distributed clock trees to increase fanout (shown below). In a distributed clock tree, part-to-part skew between U2 and U3 must be minimized to optimize system clock frequency. In the case of the clock tree, the total skew becomes a function of $t_{OSLH/HL}$ of U1 plus t_{PV} of U2 and U3.

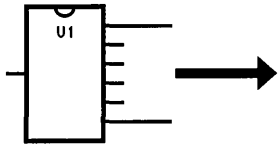

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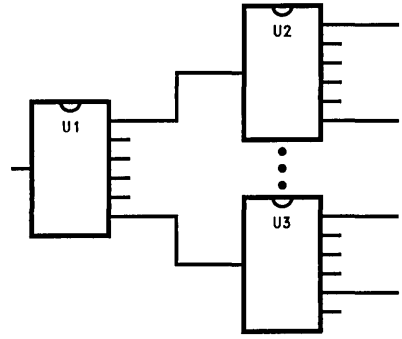
FIGURE 1-11. Clock Distribution

Case 1: Single Clock Driver

Total Skew = Pin-to-Pin Skew U1
= t_{OSLH} or t_{OSHL} of U1



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Case 2: Distributed Clock Tree

Total Skew (U2, U3) = Pin-to-Pin Skew (U1) + Part-to-Part Skew (U2, U3)

Definition

t_{PV} (Part Variation Skew):

$t_{PV} = |t_{P\varphi u,v} - t_{P\varphi x,y}|$

where φ is any edge transition (high-to-low or low-to-high) measured from the outputs of any two devices.

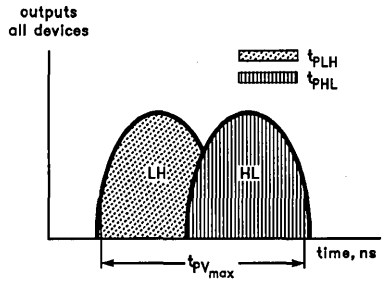

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FIGURE 1-12. t_{PV}

Example

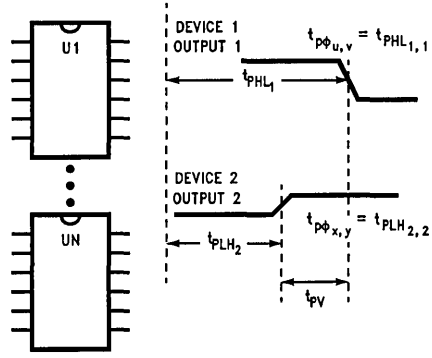

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FIGURE 1-13. t_{PV}

Section 2

Collateral and Support Tools

Section 2 Contents

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High Speed Digital Design Process

Today's high speed digital design process requires board simulation at many different levels before it is fabricated.

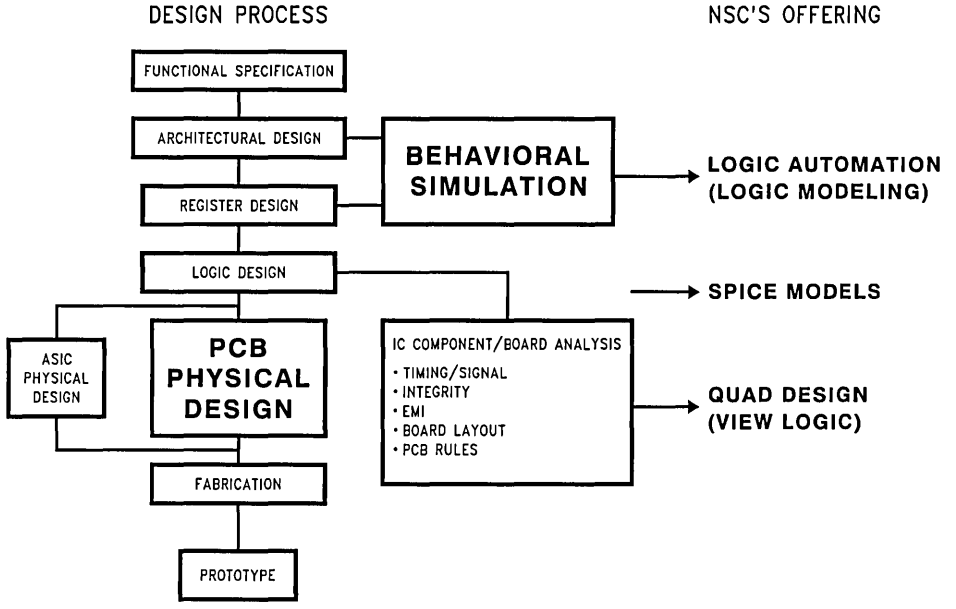
The diagram below depicts such a typical process. Before manufacturing the prototype, in order to save time and money as well as optimizing performance of the system, behavioral along with signal integrity simulations need to be performed along the design process.

These simulations become more important as operating frequencies and board densities increase. At higher frequencies, timing budgets are reduced while at the same time signal transition times are shortened.

National's CGS products line, offers behavioral models which are required during the architectural design of boards. In addition to these behavioral models, SPICE models are also available for simulation purposes.

In order to simulate for the integrity of the signals once they leave the device, its I/O characteristics need be combined with that of the board's.

NSC offers behavioral and SPICE along with I/O characteristics of its CGS products for signal integrity simulators such as QUAD Design's XNS and XTK.



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2

National Semiconductor

Clock Modeling
Transmission Line Characteristics (TLC)

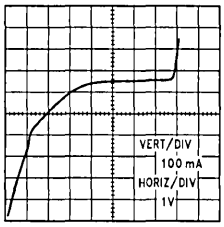
As the speed of the clock signals increases, system designers must account for transmission lines, effects. As a general rule of thumb, if the rise or fall time of any signal is more than twice the propagation delay of the signal's path, the path (trace) behaves as a transmission line. Clocks today operate in the 50 MHz region with the rise and fall time approaching sub-nanosecond transition performance. Also the length of traces is not getting any shorter and the need to distribute the clock to many components at different locations has actually increased. This results in the need to evaluate and simulate the board for transmission line and crosstalk effects caused in high frequency.

Many simulation tools are available today and each has a unique set of information required to perform simulation. Given a set of conditions and characteristics, most of these tools simulate the effects of transmission lines and crosstalk on any path. They usually require information such as the driver's and receiver's input and output characteristics along with information from PC board manufacturers regarding the board's layout and impedance characteristics.

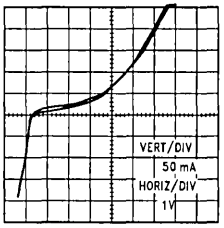
In order to create a model for the driver one must know how the driver behaves as its medium changes. This is how parameters such as t_{RISE}, t_{FALL} along with the output impedance change when board parameters such as length and/or the line's impedance change. For this reason many simulators require models of the drivers and receivers. These models can be obtained either from the manufacturer or can be measured. t_{RISE} and t_{FALL} times can be measured from plots of the output driving purely resistive loads. I-V plots (i.e., plots of V_{OH}/I_{OH} and V_{OL}/I_{OL}) can be extrapolated from the load lines and the effective impedance of the output. The output's pin capacitance is also needed since it adds to the total load.

Following are the I-V plots for CGS devices. The load lines can be obtained by calculating the slopes of V_{OH} and V_{OL}, while t_{RISE}/t_{FALL} graphs are needed for transmission line simulation.

V_{OL} CGS74CT2524



V_{OH} CGS74CT2524



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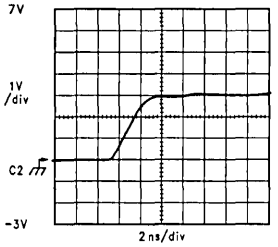
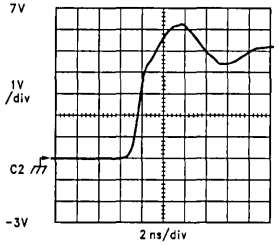
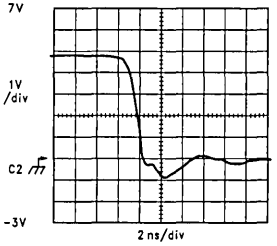


CGS74CT2524 Rise Time



CGS74CT2524 Fall Time



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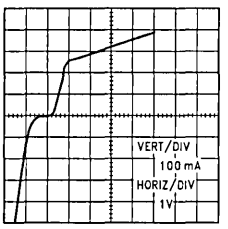
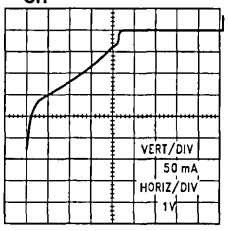


V_{OH} CGS74B2525



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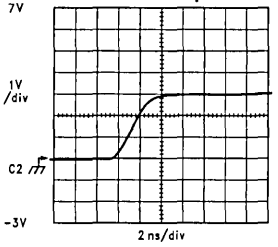

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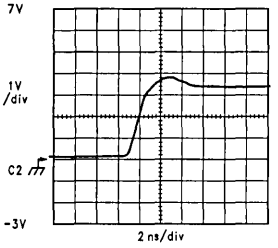

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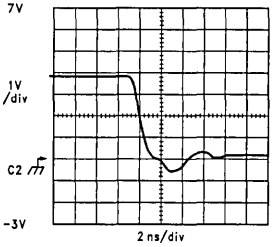

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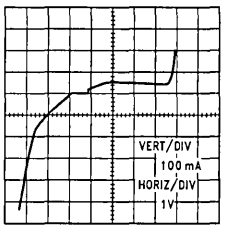

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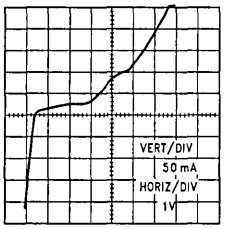

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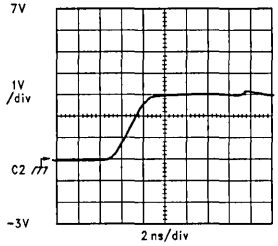
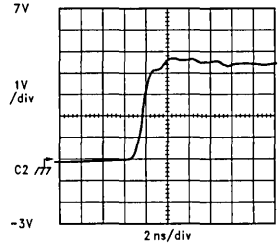
2

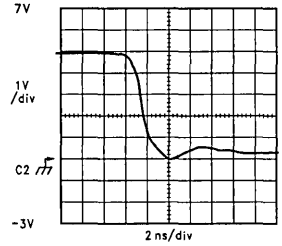
CGS74C2525/C2526 Input



CGS74C2525/C2526 Rise Time



CGS74C2525/C2526 Fall Time



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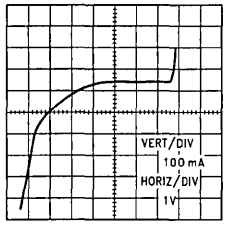

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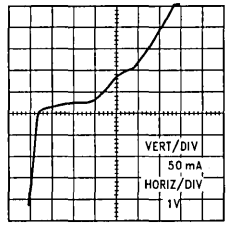

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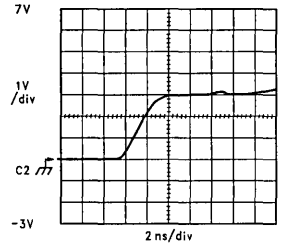

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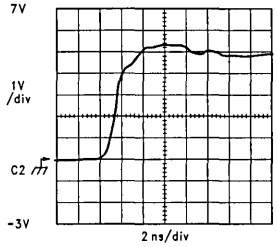
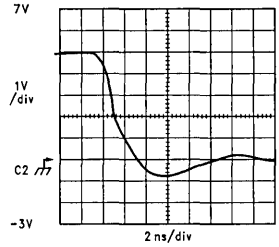


CGS74CT2525/CT2526 Fall Time



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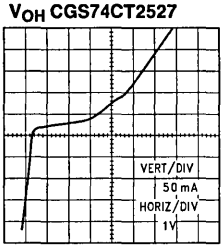

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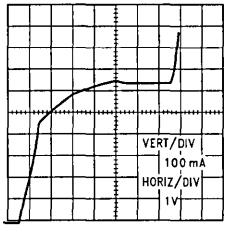

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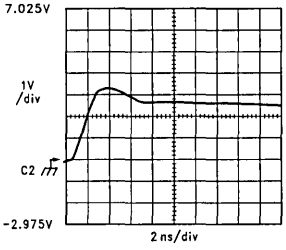
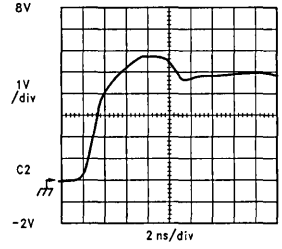
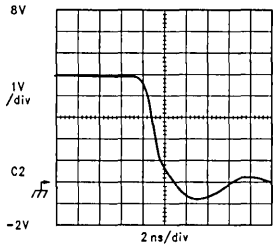


CGS74CT2527 Rise Time



TL/F/11922–2

CGS74CT2527
Fall Time



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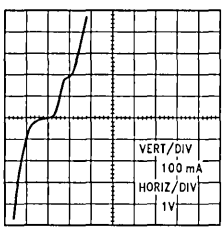
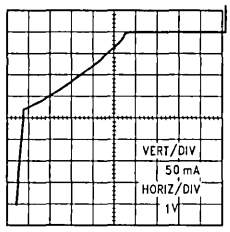


V_{OH} CGS74B2528/B2529



CGSB2528/B2529
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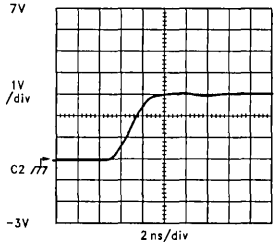
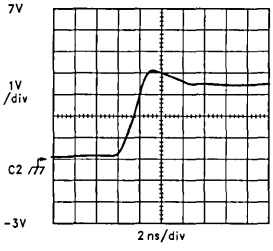


CGSB2528/B2529
Rise Time



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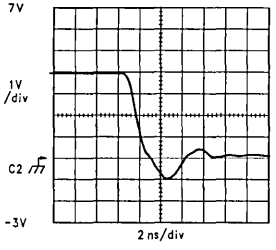
Fall Time



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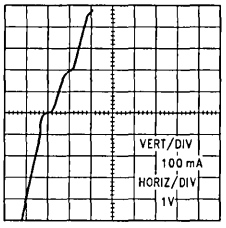

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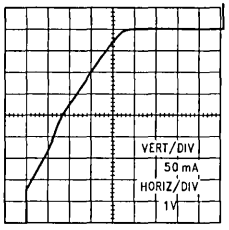

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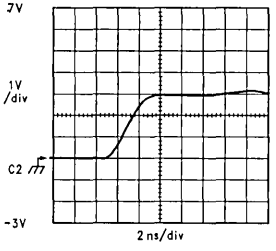

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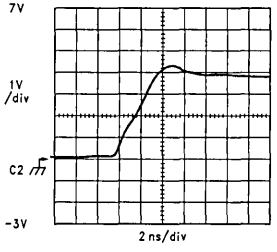
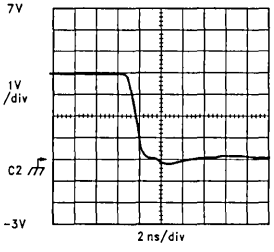
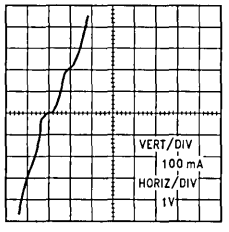
Rise Time



CGS74B303
Fall Time

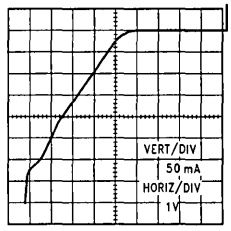


V_{OL} CGS74B304



TL/F/11922–3

V_{OH} CGS74B304



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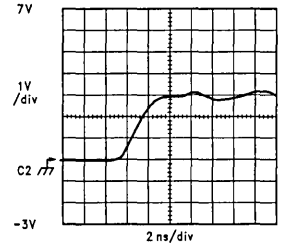
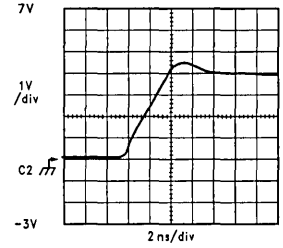
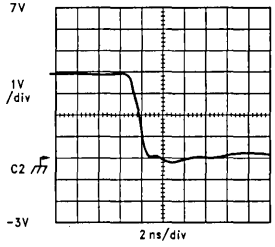


CGS74B304 Rise Time



CGS74B304 Fall Time



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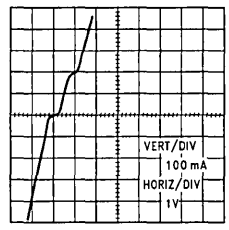

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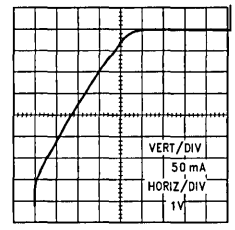

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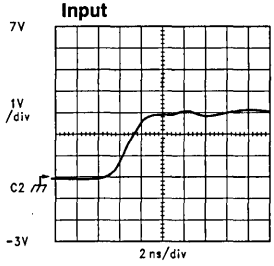

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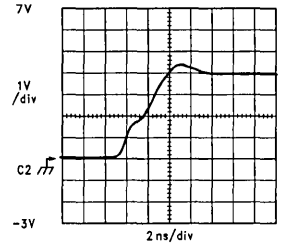

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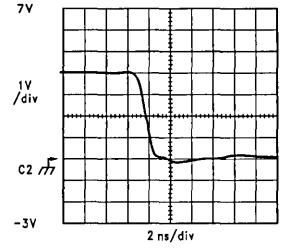
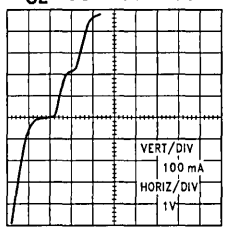
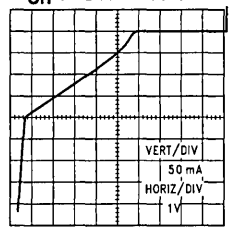


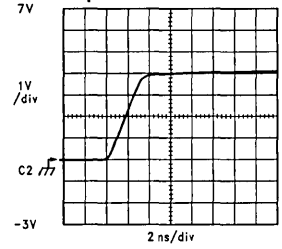
V_{OL} CGS100P2530/31



V_{OH} CGS100P2530/31

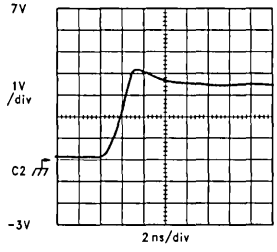


CGS100P2530/P2531 Input

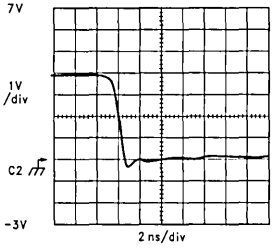


TL/F/11922–4

CGS100P2530/P2531
Rise Time



CGS100P2530/P2531
Fall Time



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Section 3

CGS Product Overview

Section 3 Contents

National Semiconductor

Clock Generation and Support (CGS™) Product Family Overview

Clock generation is a key area in today's designs of high speed CISC and RISC based computers. The primary goal of the system clock is to deliver a clock signal to each component while meeting the system's requirements for skew, acceptable wave shapes (rise, fall, overshoot, undershoot, etc.), as well as stability. At the same time these signals were to avoid timing violations such as setup and hold while minimizing the radiated E.M.I.

This primer presents an overview of NSC's offering in the CGS product line and some of the possible applications of each product individually.

1.0 Clock Buffers and Inverters

Clock drivers of the past needed to deliver and distribute the clock signal across the board (sometimes over the backplane to other boards) on a system. However, due to increased speeds and tightening of the timing budgets, a new breed of clock drivers is needed to perform such clocking functions.

The most simple type of these clock drivers requires new specifications that can allow the system designer to allow for skew (edge variation) on the systems. These skew specifications are needed to accomplish design requirements such as synchronization of different components, large fan-out distributions, duty cycle control or even clocking heavily loaded memory or address buses.

For a detailed list of some of these specifications refer to the Definition and Test Philosophy section at the beginning of this book as well as individual data sheets.

The diagram below represents a typical skew problem that is associated with today's systems.

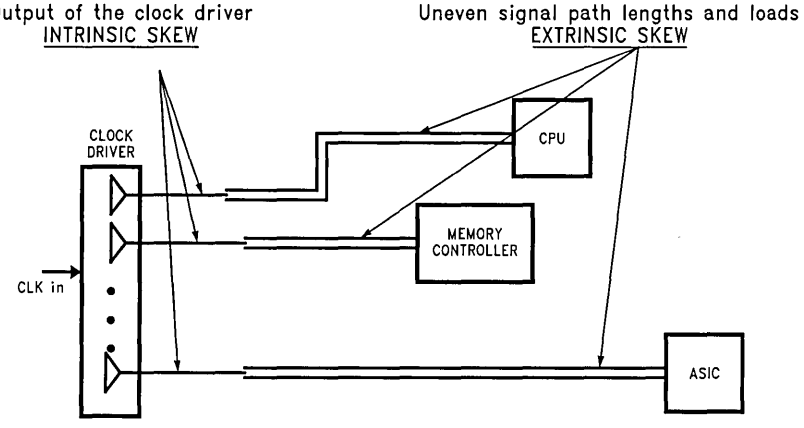
With skew being defined as the difference in signal propagation delay, extrinsic skew, at large, remains a board design issue. There are many ways to minimize, if not eliminate, extrinsic skew. The most common method is the proper routing of the clock signal across the board and or backplane. However, intrinsic skew needs to be addressed during component level design. Among the popular methods to minimize the intrinsic skew are:

- Dedicated 1-input to N-output clock drivers with matched propagation delays
- Common circuits to the last stage, symmetric circuitry and package layout

In addition to the methods above the selected technology for the clock driver has a direct impact on the performance as well as the specifications of each device.

The table below reflects a summary of the available technologies along with their typical pin-to-pin common edge skew performances:

Technology	Design Skew
TTL	200 ps–300 ps
CMOS	200 ps–300 ps
ECL	10 ps–50 ps
PECL-TTL	100 ps–300 ps
BCT	100 ps–200 ps



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1.0 Clock Buffers and Inverters (Continued)

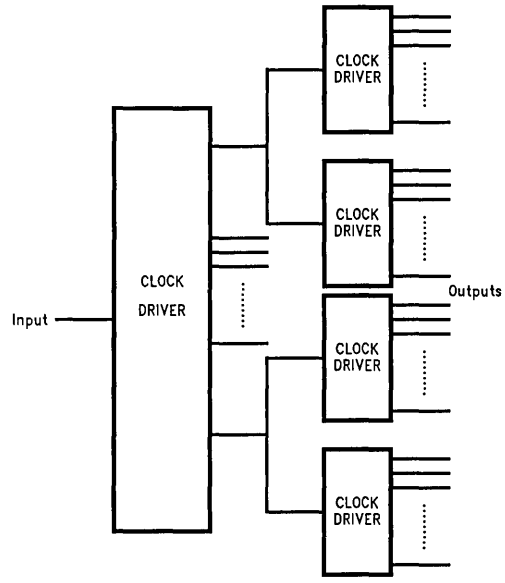
These clock drivers and buffers have a wide range of applications, among which clock distribution is the most common application. These drivers, i.e. CGS2524, 2525, 2526, 2527, 2528 are ideal for applications which require distribution and delivery of high speed clock signal to other components using different configurations such as the one below (Clock Trees).

CPU-Memory Sub-systems often require a large clock/data distribution tree. This will require synchronization at each stage which needs to be accomplished by tight propagation delay windows (T_{PD} Min–Max) as well as low part-to-part skew.

In addition to a large fanout requirement, sometimes it is necessary to provide an additional input as the clocking source. This multiplexed input can serve many purposes such as a test clock during power-up diagnostics where the system can be tested at different frequencies without disabling the main system clock. It also can be used for fault tolerant conditions where it becomes possible to continue the operation of the system if one of the system clocks is disrupted. CGS2530, which is a 1–10 TTL min-skew clock driver as well as CGS2531, have incorporated this additional input feature.

Many of today's processors require highly symmetric input clock duty cycle. For this purpose CGS303-4-5 devices have been designed. These divide-by-two clock drivers provide highly symmetric output clock signals with their inputs at relatively loose duty cycle as shown below. (Refer to data sheets for actual skew specifications.)

Clock Tree



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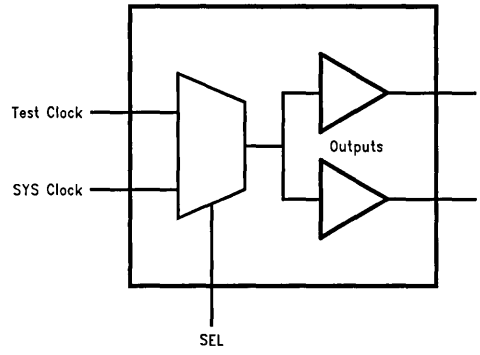
Dual Input Clock Drivers



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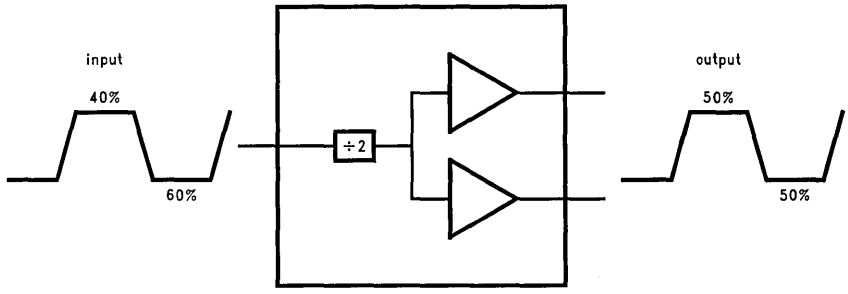
Divide-by-2 Clock Driver



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1.0 Clock Buffers and Inverters (Continued)

MEMORY ARRAY DRIVERS

In order to minimize the total load on the address bus, quite often memory arrays are being driven by buffers while having the inputs of the buffers tied together. Although this practice was feasible in the conventional memory designs, in today's high speed, large bus width designs which require address fetching at higher speeds, this technique produces many undesired results such as cross-talk and over/undershoot.

CGS2534/35/36 Memory Array Drivers were designed specifically to address these application issues on high speed, large memory arrays systems.

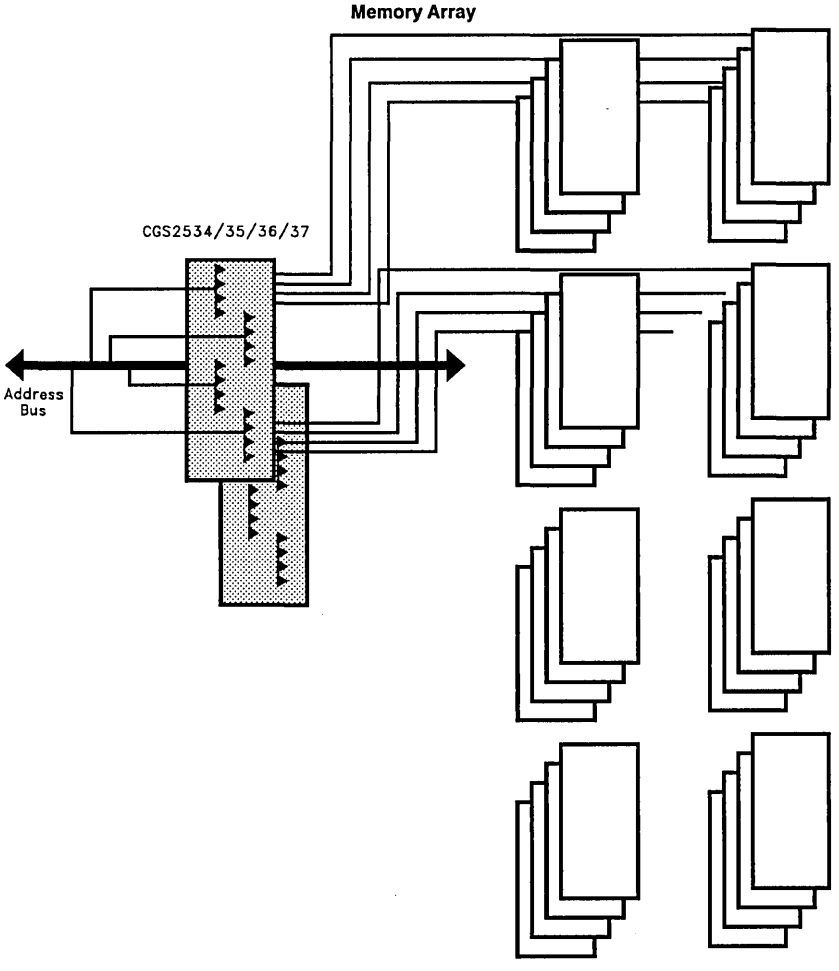
These drivers are optimized to drive large loads, with sub 4 ns propagation delays. These drivers produce less noise while reducing the total capacitive loading on the address bus by having only four inputs tied together. This helps to minimize the overshoot and undershoot by having only four outputs being switched simultaneously.

Also this larger fan-out helps to save board space since for every one of these MAD drivers, two conventional buffers were typically being used.

Another feature associated with these clock drivers is a 250 ps–500 ps pin-to-pin skew specification. The minimum skew specification allows high speed memory system designers to optimize the performance of their memory subsystem by operating at higher frequencies without having concerns about output-to-output (bank-to-bank) synchronization problems which are associated with driving high capacitive loads.

The following diagram depicts a "2534/35/36/37", a memory subsystem operating at high speed with large memory capacity. The address bus is common to both the memory and the CPU and I/Os.

These MAD drivers can operate beyond 150 MHz, and are also available in 3V–5V TTL/CMOS versions with symmetric 24 mA I_{OH}/I_{OL} current drives.



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2.0 Clock Generators

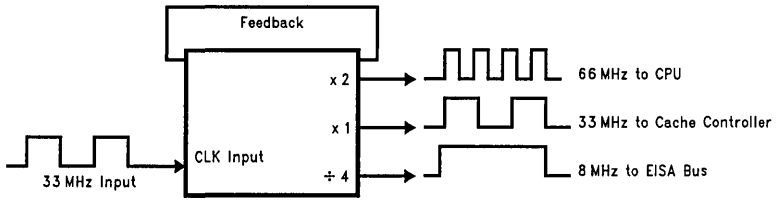
Clock buffers and drivers offer an inexpensive solution for clock distribution for a given design however, there are many drawbacks in using drivers alone.

Due to the variations in propagation delays from buffer to buffer, there will be an accumulation of skew as the buffers are cascaded to increase the fanouts required for large clock trees. In addition to this skew accumulation, since there are no feedback paths, the task of synchronization becomes more difficult since designers need to compensate for uneven trace lengths or any load unbalances across the outputs.

For these reasons it is often required to use phase lock loops for distributing the clock signals. The feedback path that is needed to synchronize the output's phase with the reference input signal, can be taken from one of the outputs that has the same characteristics as the other drivers.

Another benefit that is associated with this implementation is generation of multiple frequencies. This is due to the internal voltage controlled oscillator that is required for phase lock loop designs. These VCOs can be designed to operate at higher frequencies which will allow generation of multiple frequencies on the same chip.

In addition to better synchronization and lowering the number of oscillators required for multi-frequency designs, tighter duty cycle control can be achieved. By designing the VCO's to operate at twice the highest frequency required, a simple divide by two can result in 50% duty cycle for the outputs. This makes the output's duty cycle independent of the input source or the reference signals duty cycle.



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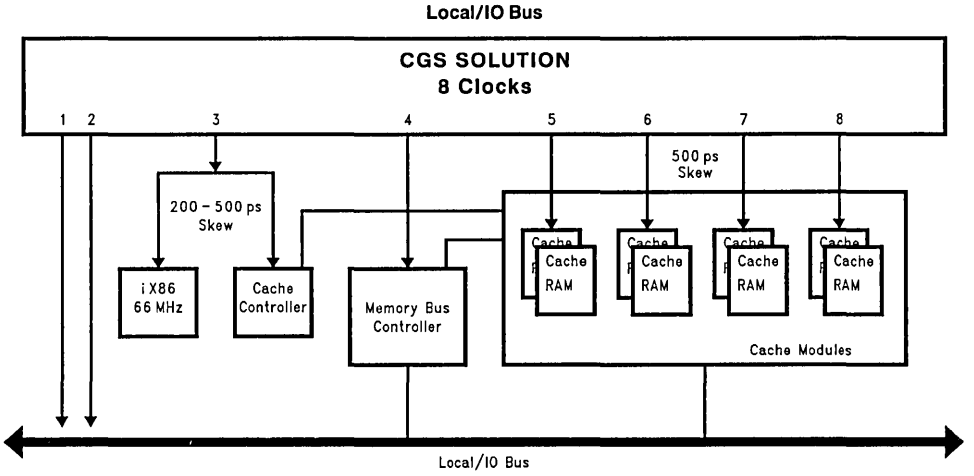
2.0 Clock Generators (Continued)

The following diagram shows one such usage. Many of today's personal computers require clock generators which are capable of generating outputs at multiple frequencies which are synchronous to each other.

As shown in the diagram, for a fully synchronous i586 design, the CPU and cache controller need to be operating at twice the speed of the SRAMs and other peripherals. For these systems the CGS product line offers low skew phase lock loop clock drivers along with low skew buffers to ease the design task by providing high fanout generators and buffers that have all the outputs operating at the same speed.

For those designs that the cache controller does not need to run at the same operating speed as the CPU, CGS solutions provided in the following table, offer flexibility and a lower total chip count for generating the required clock signals.



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	CPU	Memory Bus	CGS Solutions	Features
Fully Synchronous System: • Clock Buffers • PLL Clock Buffers	66 MHz	66 MHz	CGS74B2528 CGS74CT2527	500 ps Pin Skew 1 ns Part Skew 10 Outputs
			CGS801	500 ps Pin Skew Internal PLL 8 Outputs
Divided Synchronous System: • PLL Clock Generators	66 MHz	33 MHz	CGS800	500 ps Pin Skew Internal PLL x2, x1, /2
			CGS802	500 ps Pin Skew Internal PLL x2, x1, /2, /3, /4

2.0 Clock Generators (Continued)

BOARD-TO-BOARD DISTRIBUTION

Quite often clock signals need to be carried over the back plane onto other boards. These boards at the same time need to be synchronized with each other as such is the case for many multiprocessor systems.

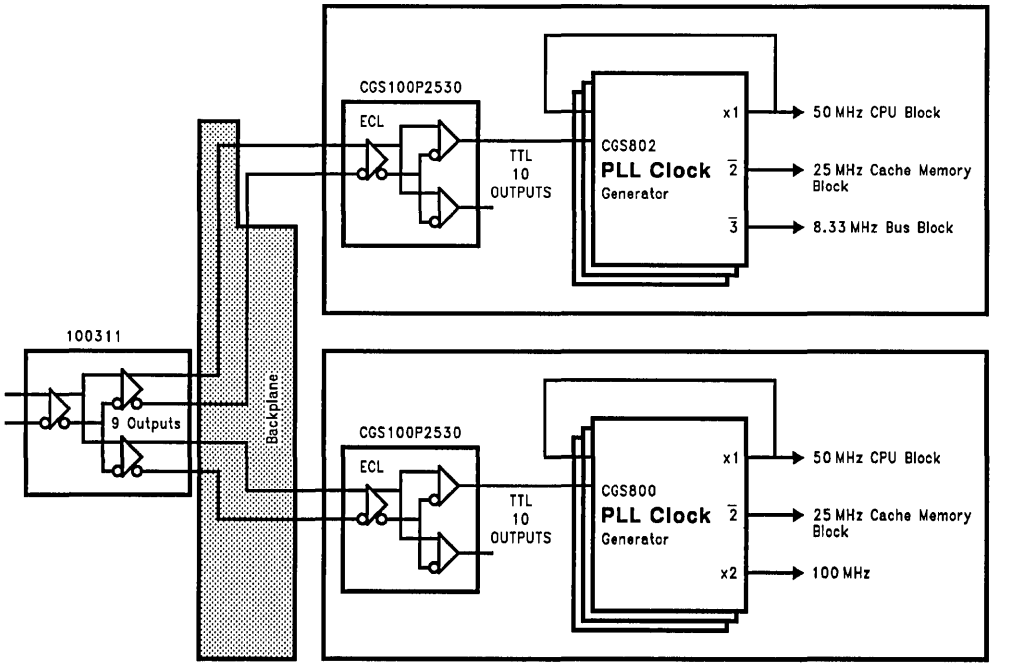
By offering ECL clock drivers and ECL/PECL to TTL clock drivers, CGS product line offers the flexibility required for such high frequency multi-processing systems.

In addition to these drivers, phase lock loop clock drivers can receive the incoming clock signal and produce higher frequency clock signals which are in phase (synchronized) with its input. This design technique allows full board to board synchronization of CPUs while minimizing the total skew that is associated with distributing clock signals across back planes, traces and vias onto other boards.

The diagram below depicts one such example. The clock signal generated on the mother board can be routed thru the back-plane using ECL technology. While, on the receiving side, the same signal can be translated into TTL using PECL to TTL clock drivers with its output being used as the reference frequency for the phase lock loop clock generator.

This method allows distribution of high frequency signals across impedance discontinuities such as back-planes with minimal signal distortion and degradation. This is due to ECL technology's matched impedance characteristics.

The same signal can be used as a reference frequency for the PLLs which can produce many outputs at different frequencies which are in skew with each other.



3.0 Video Pixel Clock Generator

As system clock frequencies reach 100 MHz and beyond, maintaining control over clock timing becomes very important and difficult. Besides microprocessors, other video circuits such as: RAMDAC, Video graphics processors etc., require precise clock timings. In addition, systems requirements demand that the clock distribution to synchronous systems components have minimal skew (the time difference between signals that are intended to switch simultaneously). The CGS410 is just the right device for video circuits.

The CGS410 is a CMOS programmable clock generator device capable of generating synthesized clock outputs in excess of 120 MHz. The device achieves programmability by serially clocking data into an internal shift register. Upon receiving the last bit of information, the data is automatically transferred and mapped into the internal divider circuits.

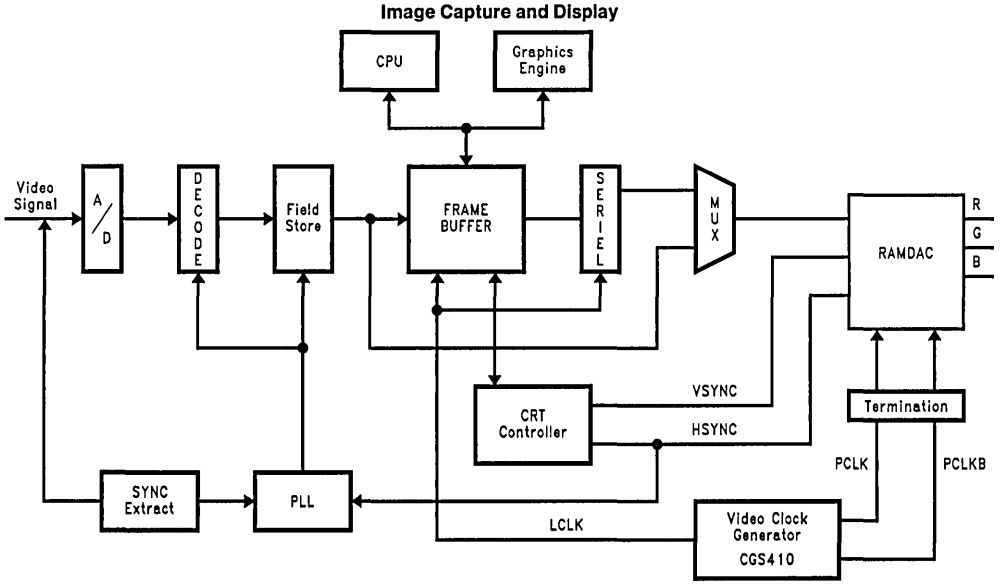
At the heart of the CGS410 is an internal modulated ring oscillator which comprises the VCO. This VCO is different from external VCO implementations because, instead of using an L-C tank ratio to characterize the resonant frequency; an internal time delay through the ring is modulated in direct response to a voltage present on the FREQCTL input. The FREQCTL voltage is the response of the low pass filter driven by the charge pump.

The inherent advantage of running a "ring-oscillator" is its ability to create wide frequency variations as dictated by the gain of the VCO. This is in contrast to the L-C VCO implementations, where the tuning range is much narrower and the VCO gain (generally) much lower.

In order to reduce the internal die noise coupling, specific functions are powered from separate external source and ground return points. These paired pins are: BVDD/BGND, DVDD/DGND, XVCC/XGND, and AVDD/AGND. All pins can be grouped together with little increase in phase noise, with the exception of AVDD/AGND.

What drives the ring-VCO approach is determined by the amount of jitter (instability) present on the VCO output. The jitter can be understood as minute frequency variations present on the VCO output in comparison to an ideal VCO. The jitter is a measure of how much the output clock period varies over time. The CGS410 has extremely low jitter.

CGS410 IN MULTIMEDIA APPLICATION



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The figure above shows the block diagram of a typical video system. The NTSC color signal is converted into digital signal by a video A-to-D converter. The Field storage (memory) contains information on field bits (such as: starting address of the field and the size of the field) which are software configurable. The 3-way frame buffer shown in this example is sophisticated enough so that it can interface with the CPU, graphics processor and CRT controller. The output of the frame buffer is multiplexed with the output of the field store registers and fed to the RAMDAC. The CGS410 is used here to generate the load clock for the frame buffer and the Pixel clock for the RAMDAC. The Load clock for the frame buffer is generated by the CMOS compatible output on the CGS410 and it is programmable in order to produce the lower output frequencies synchronous to Pixel clock. The Pixel clock for the RAMDAC can be derived either from the high frequency differential outputs PCLK and PCLKB on the CGS410 for higher pixel rates (as shown in this figure) or from the single ended, CMOS compatible PCLK output for average pixel rate. Proper termination should be used when using the differential clocks.

4.0 Crystal Clock Generators

THE TOTAL SYSTEM SOLUTION

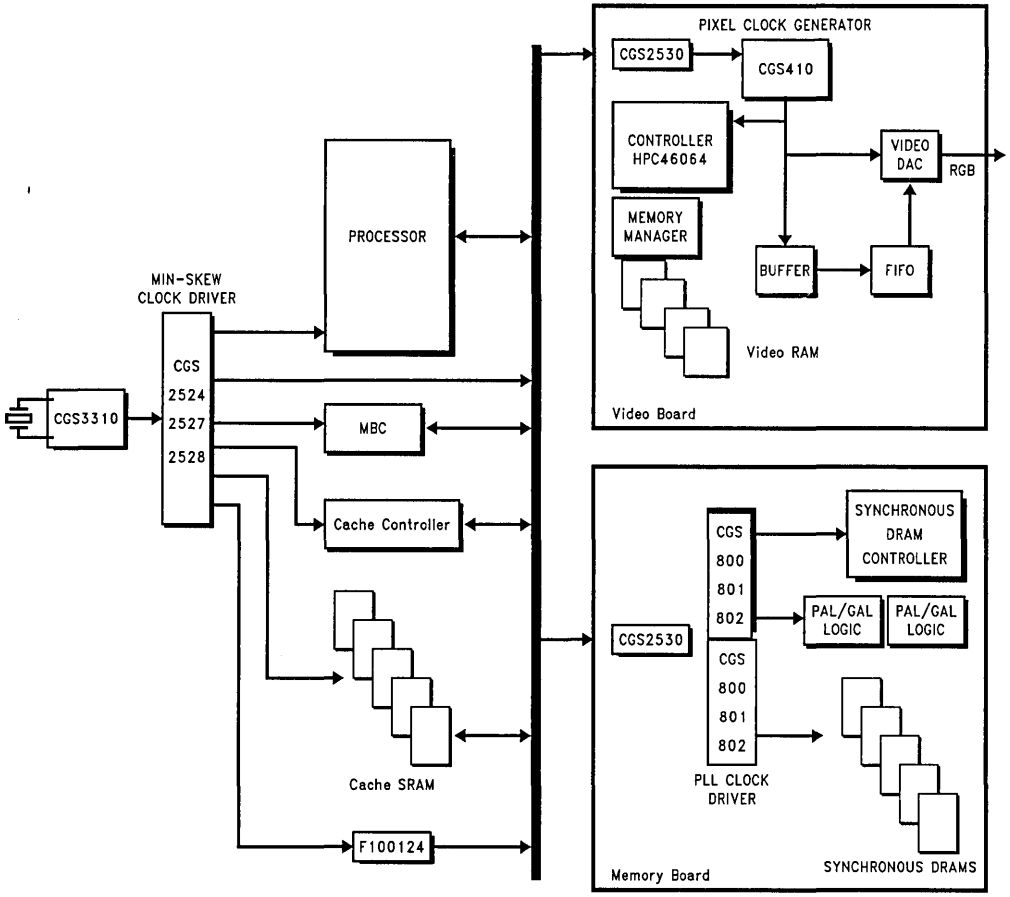
Also offered in the CGS product line are crystal oscillators. These devices require minimum external components since they have already integrated the oscillator and they merely require a crystal as an input source. They can generate clock signals which can be programmed for t_{rise}/t_{fall}/drive/duty cycle and even frequencies.

These products are to complement other products for clock generation and support for providing a total system solution from the crystal oscillators to the generation and distribution of the clock signal.

The block diagram below shows one such solution. The clock signal being generated from the source and being distributed across the back plane to additional modules.

In the application, the clock to the mother board, including the CPU and the memory controller are being supplied with min-skew buffers while at the same time one being translated to ECL.

This needs to be done in order for the signal to be carried over the back-plane to the add-on cards such as the video or the memory boards, where each board either generates or distributes the required signals.



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Section 4

Datasheets

Section 4 Contents

National Semiconductor

CGS74CT2524
1 to 4 Minimum Skew (450 ps) Clock Driver

General Description

These minimum skew clock drivers are designed for Clock Generation and Support (CGS) applications operating at high frequencies. This device guarantees minimum output skew across the outputs of a given device.

Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The '2524 is a minimum skew clock driver with one input driving four outputs, specifically designed for signal generation and clock distribution applications.

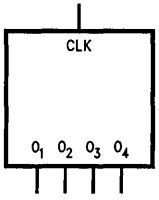
Features

- Guaranteed and tested:
  450 ps pin-to-pin skew
  (t_{OSHL} and t_{OHLH}) M package
- Implemented on National's FACT™ family process
- 1 input to 4 outputs low skew clock distribution
- Symmetric output current drive: 24 mA I_{OH}/I_{OL}
- Industrial temperature of −40°C to +85°C
- 8-pin DIP and SOIC packages
- Low dynamic power consumption above 20 MHz
- Guaranteed 2 kV ESD protection

Ordering Code: See Section 5

Logic Symbol

'2524



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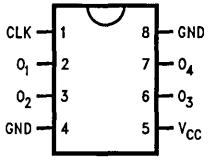
The output pins act as a single entity and will follow the state of the CLK when the clock distribution chip is selected.

Connection Diagrams

Pin Assignment for M and N

'2524



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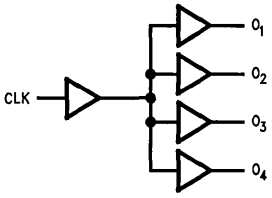
'2524



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Pin Description

Pin Names	Descripton
CLK	Clock Input
O_1–O_4	Outputs

Truth Table

'2524

Inputs	Outputs
CLK	O_1–O_4
L	L
H	H

L = Low Logic Level
H = High Logic Level

4

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})			−0.5 to 7.0V
DC Input Voltage Diode Current (I_{IK})			
$V = -0.5V$			−20 mA
$V = V_{CC} + 0.5V$			+20 mA
DC Input Voltage (V_I)			$-0.5V$ to $V_{CC} + 0.5V$
DC Output Diode (Current) (I_O)			
$V = -0.5V$			−20 mA
$V = V_{CC} + 0.5V$			+20 mA
DC Output Voltage (V_O)			$-0.5V$ to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)			±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})			±50 mA
Storage Temperature (T_{STG})			−65°C to +150°C
Junction Temperature (θ_J)	0	225	500 LFM
	M	167	132	117°C/W
	N	115	79	62°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0 to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

NOTE: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	CGS74CT2524			Units	Conditions
			$T_A = +25°C$	$T_A = -40°C$ to $+85°C$			
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA
		5.5		4.86	4.76		
V_{OL}	Minimum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA
		5.5		0.36	0.44		
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	mA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic Output Current	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Minimum Quiescent Supply Current	5.5		8.0	80	μA	$V_{IN} = V_{CC}$ or GND

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	CT2524 V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω			Units
		Min	Typ	Max	
t_{PLH}	Low-to-High Propagation Delay CK to O_n ('2524)	3.5		9.0	ns
t_{PHL}	High-to-Low Propagation Delay CK to O ('2524)	3.5		9.0	ns

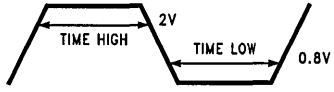
Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	CT2524 V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω					Units
		Package	V_{CC} (V)	Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation*	M	5.0			450	ps
		N				500	
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation*	M	5.0			450	ps
		N				500	
t_{PS}	Maximum Skew Pin (Signal) Transition Variation**	ALL	5.0			1.0	ns
t_{rise} t_{fall}	Rise Time/Fall Time (from 0.8V to 2.0V/2.0V to 0.8V)	ALL	5.0			1.5	ns
F_{max}	Maximum Operating Frequency	ALL			100		MHz

Extended Electrical Characteristics: (66.67 MHz)

CGS74CT2524	T_A = −40 to +85°C, C_L = 50 pF, R_L = 500Ω	Units
Time High	4	ns
Time Low	4	ns



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Time high is measured with outputs at above 2V.
Time low is measured with outputs at below 0.8V.

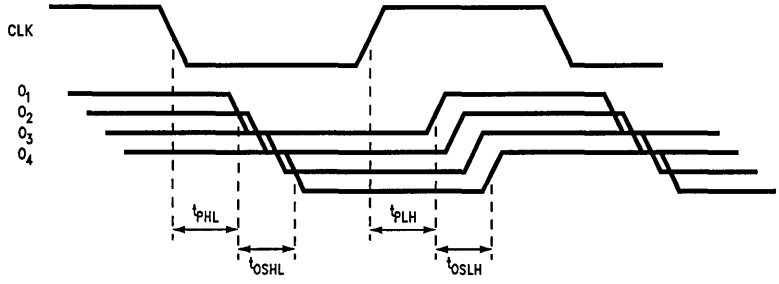
t_{OSHL} and t_{OSLH} parameters for M package are being guaranteed by design at 66.67 MHz until Oct. 1993. Thereafter will be guaranteed by production test.

* Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay from any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH or LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

** Pin transition skews is the absolute difference between High-to-Low and Low-to-High propagation delay measure at a given output pin.

Timing Diagrams

1 to 4 Min-Skew Clock Driver



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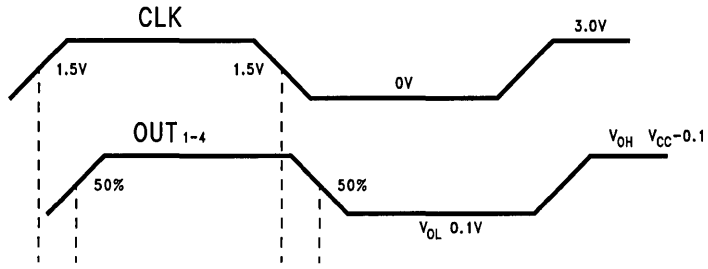

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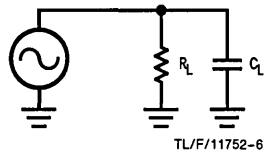
Test Circuit



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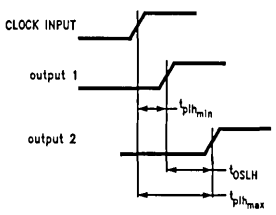
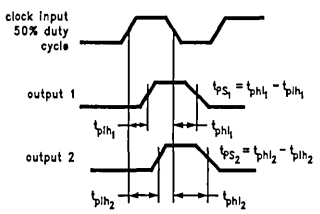
R_L is 500Ω
C_L is 50 pF for all prop delays and skew measurements.

Notes:

- Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.
- Load capacitance includes the test jig.

Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
t_{OSHL}, t_{OSLH} **Common Edge Skew:** Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = \lvert t_{PHL_{max}} - t_{PHL_{min}} \rvert$ Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = \lvert t_{PLH_{max}} - t_{PLH_{min}} \rvert$ Propagation delays are measured across the outputs of any given device.	 **FIGURE A**	• t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/clock operations.
t_{PS} **Pin Skew or Transition Skew:** $t_{PS} = \lvert t_{PHL_i} - t_{PLH_i} \rvert$ Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. T_{PS} is the maximum difference for outputs i = 1 to 8 within a device package.	 **FIGURE B**	• t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).

National Semiconductor

PRELIMINARY

CGS74LCT2524
1 to 4 Minimum Skew (450 ps) 3V Clock Driver

General Description

This minimum skew clock driver is a 3V option of the current '2524 Minimum Skew Clock Driver and is designed for Clock Generation and Support (CGS) applications operating at low voltage, high frequencies. This device guarantees minimum output skew across the outputs of a given device.

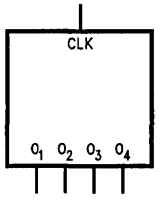
Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The '2524 is a minimum skew clock driver with one input driving four outputs, specifically designed for signal generation and clock distribution applications.

Features

- Ideal for low power/low noise high speed applications
- Guaranteed and tested:
  — 450 ps pin-to-pin skew (T_{OSHL} and T_{OHLH}) M package
- Implemented on National's FACT™ family process
- 1 input to 4 outputs low skew clock distribution
- Symmetric output current drive
  — 24 mA I_{OH}/I_{OL}
- Industrial temperature of −40°C to +85°C
- 8-pin DIP and SOIC packages
- Low dynamic power consumption above 20 MHz
- Guaranteed 2 kV ESD protection

Logic Symbol

'2524



TL/F/11956–1

The output pins act as a single entity and will follow the state of the CLK when the clock distribution chip is selected.

Pin Description

Pin Names	Description
CLK	Clock Input
O1–O4	Outputs

Truth Table

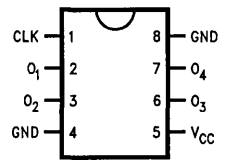
'2524

Inputs CLK	Outputs O1–O4
L	L
H	H

L = Low Logic Level
H = High Logic Level

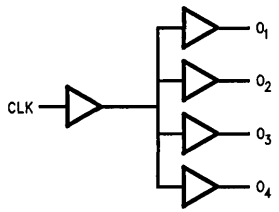
Connection Diagrams

Pin Assignment for M and N
'2524



TL/F/11956–2

'2524



TL/F/11956–3

See NS Package Number M08A and N08E

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})		−0.5V to 7.0V
DC Input Voltage Diode Current (I_{IK})		
$V = -0.5V$		−20 mA
$V = V_{CC} + 0.5V$		+20 mA
DC Input Voltage (V_I)		−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_O)		
$V = -0.5V$		−20 mA
$V = V_{CC} + 0.5V$		+20 mA
DC Output Voltage (V_O)		−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)		±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})		±50 mA
Storage Temperature (T_{STG})		−65°C to +150°C
Junction Temperature (θ_J)		
M Package	0 LFM	167°C/W
	225 LFM	132°C/W
	500 LFM	117°C/W
N Package	0 LFM	115°C/W
	225 LFM	79°C/W
	500 LFM	62°C/W

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Industrial	−40°C to +85°C
Commercial	0°C to +70°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Electrical Characteristics Over recommended operating free air temperature range

Symbol	Parameter	Conditions	V_{CC} (V)	CGS74CT2524			Units
				$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	3.3	1.5	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	3.3	1.5	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OUT} = -50\ \mu A$	3.3	2.99	2.9	2.9	V
		$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -24$ mA	3.3		2.56	2.46	V
V_{OL}	Minimum Low Level Output Voltage	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OUT} = 50\ \mu A$	3.3	0.002	0.1	0.1	V
		$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 24$ mA	3.3		0.36	0.44	V
I_{IN}	Maximum Input Leakage Current	$V_I = V_{CC}$, GND	3.6		±0.1	±1.0	μA
I_{CC_T}	Maximum I_{CC}/Input	$V_I = 2.4V$	3.6			1.0	mA
I_{OLD}	Minimum Dynamic Output Current	$V_{OLD} = 0.8V$ (max)	3.6			36	mA
I_{OHD}		$V_{OHD} = 2.0V$ (min)	3.6			−25	mA
I_{CC}	Minimum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	3.6		2.5	25	μA

AC Electrical Characteristics All typical values are measured at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter	CT2524 V_{CC} = 3.0V to 3.6V, T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω			Units
		Min	Typ	Max	
t_{PLH}	Low-to-High Propagation Delay CK to O_n	3.5		15.0	ns
t_{PHL}	High-to-Low Propagation Delay CK to O	3.5		15.0	ns

Extended AC Electrical Characteristics All typical values are measured at V_{CC} = 3.3V, T_A = 25°C

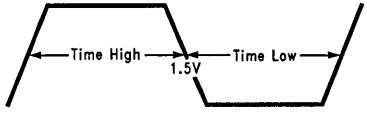
Symbol	Parameter	V_{CC} (V)	CT2524 V_{CC} = 3.0V to 3.6V, T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω			Units
			Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation*					
	M Package	3.3			450	ps
	N Package	3.3			500	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation*					
	M Package	3.3			450	ps
	N Package	3.3			500	ps
t_{PS}	Maximum Skew Pin (Signal) Transition Variation**					
	ALL	3.3			1.0	ns
t_{RISE} t_{FALL}	Rise Time/Fall Time (from 0.8V to 2.0V/2.0V to 0.8V)					
	ALL	3.3			1.5	ns
f_{max}	Maximum Operating Frequency					
	ALL	3.3		45		MHz

*Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

**Pin transition skew is the absolute difference between HIGH-to-LOW and LOW-to-HIGH propagation delay, measured at a given output pin.

Extended Electrical Characteristics (at f_{max})

CGS74LCT2524	T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω	Units
Time High	4	ns
Time Low	4	ns



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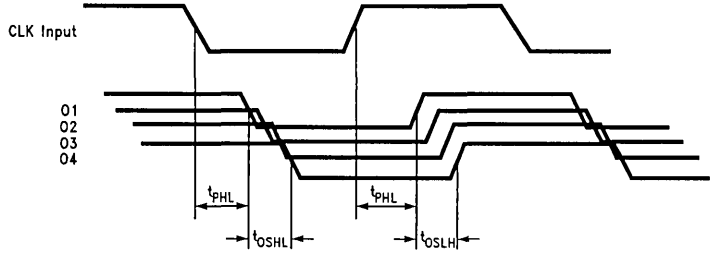
Time high is measured with outputs at above 2V.

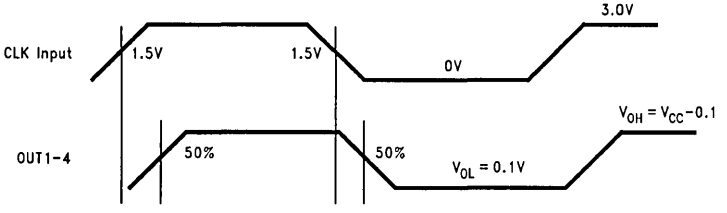
Time low is measured with outputs at below 0.8V.

Extended Electrical Characteristics (at f_{max}) (Continued)

1 to 4 Min-Skew Clock Driver



TL/F/11956-5



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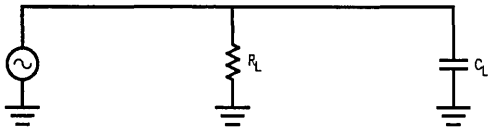
Test Circuit



TL/F/11956-7

R_L is 500Ω

C_L is 50 pF for all propagation delays and skew measurements.

Note 1: Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.

Note 2: Load capacitance includes the test jig.

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CGS74B2525
1-to-8 Minimum Skew Clock Driver

General Description

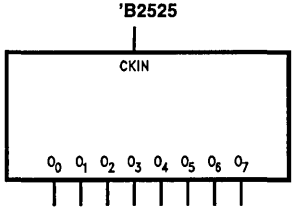
This minimum skew clock driver is designed for Clock Generation and Support (CGS) applications operating well above 20 MHz (33 MHz, 50 MHz). The device guarantees minimum output skew across the outputs of a given device and also from device-to-device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The 'B2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications.

Features

- Clock Generation and Support (CGS) Device—Ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST® LSI process
- 1-to-8 low skew clock distribution
- Sub 1 ns pin-to-pin output skew
- Specifications for device-to-device variation of propagation delay
- Specification for transition skew to meet duty cycle requirements
- Center pin V_{CC} and GND configuration to minimize high speed switching noise
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Ordering Code: See Section 5

Logic Symbol



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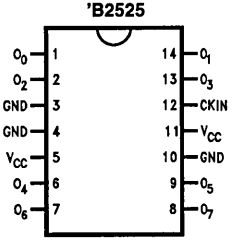
Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10907–2

Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CK_n input will have an active effect on the outputs of the circuit. When SEL = 1, the CK_1 input is selected and when SEL = 0, the CK_0 input is selected. The non-selected CK_n input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK_{IN} or CK_1/CK_0 pins when the ('B2525) clock distribution chip is selected.

Pin Description

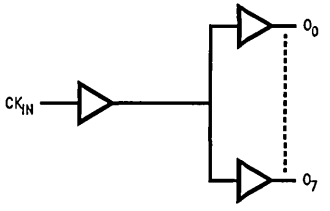
Pin Names	Description
CK_{IN}	Clock Input ('B2525)
O_0–O_7	Outputs

Truth Table

'B2525

Inputs	Outputs
CK_{IN}	O_1–O_7
L	L
H	H

'B2525



TL/F/10907–5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V
Input Voltage (V_I)	7.0V
Operating Free Air Temperature	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
Plastic (N) Package	104 °C/W
JEDEC SOIC (M) Package	120 °C/W

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage—High (V_{IH})	2.0V
Input Voltage—Low (V_{IL})	0.8V
High Level Output Current (I_{OH})	−48 mA
Low Level Output Current (I_{OL})	+64 mA
Free Air Operating Temperature (T_A)	0°C to +70°C

DC Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = −48 mA, V_{CC} = 4.5V		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 64 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IH} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		8	15	mA
			Outputs Low		32	42	mA
C_{IN}	Input Capacitance	V_{CC} = 5V			5		pF

AC Electrical Characteristics

Symbol	Parameter	CGS74B			Units
		V_{CC} = 4.5V to 5.5V R_L = 500Ω, C_L = 50 pF			
		Min	Typ	Max	
t_{PLH}	Propagation Delay	2	2.9	4.8	ns
t_{PHL}	CK to O_n ('2525)	2	3.0	4.8	

Extended AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	CGS74B $R_L = 500\Omega, C_L = 50$ pF, $T_A = 0°C$ to $70°C$			Units
			Min	Typ	Max	
f_{max}	Maximum Operating Frequency	5.0	50			MHz
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.15	1	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.15	1	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation (Note 1)	5.0		0.7	1.5	ns
t_{PV}	Maximum Skew Part-to-Part Variation Skew (Note 2)	5.0			1.75	ns
t_{PS}	Maximum Skew Pin (Signal) Transition Variation (Note 1)	5.0		0.6	1.5	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (from 0.5/2.4V to 2.4/0.5V at 33 MHz, $T_A = 25°C$)	5.0 5.0		1.90 1.15		ns ns

*Voltage Range 5.0 is 5.0V ±0.5V

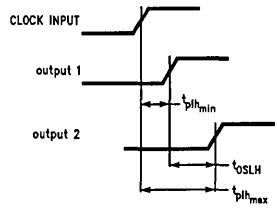
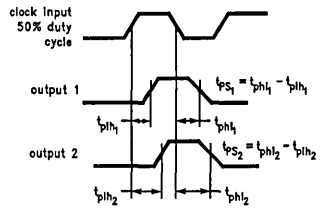
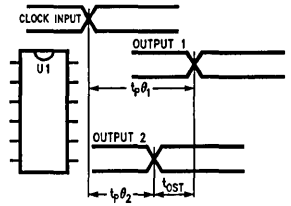
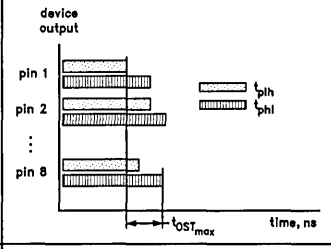
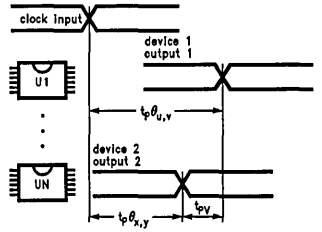
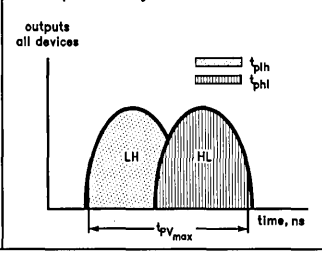
Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

Note 3: 'B2525 is recommended for applications using only the rising edge of the clock while operating at, or below, 50 MHz.

Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
t_{OSHL}, t_{OSLH} **Common Edge Skew:** Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = \lvert t_{PHL_{max}} - t_{PHL_{min}} \rvert$ Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = \lvert t_{PLH_{max}} - t_{PLH_{min}} \rvert$ Propagation delays are measured across the outputs of any given device.	 **FIGURE A**	• t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/clock operations.
t_{PS} **Pin Skew or Transition Skew:** $t_{PS} = \lvert t_{PHL_i} - t_{PLH_i} \rvert$ Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. T_{PS} is the maximum difference for outputs i = 1 to 8 within a device package.	 **FIGURE B**	• t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).
t_{OST} **Opposite Edge Skew:** $t_{OST} = \lvert t_P\theta_m - t_P\theta_n \rvert$ where θ is any edge transition (HIGH-to-LOW or LOW-to-HIGH) measured between any two outputs (m or n) within any given device.	 **FIGURE C**	• t_{OST}, Any Edge Skew • Skew parameter to observe performance distribution of propagation delays across the outputs within any given device. 
t_{PV} **Part Variation Skew:** $t_{PV} = \lvert t_P\theta_{u,v} - t_P\theta_{x,y} \rvert$ where θ is any edge transition (HIGH-to-LOW or LOW-to-HIGH propagation delay) measured from the outputs (v or y) of any two devices (u or x).	 **FIGURE D**	• t_{PV}, Part Variation Skew • Skew parameter to observe performance distribution of propagation delays between the outputs of any two devices. 

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CGS54C/74C2525 • CGS54CT/74CT2525
CGS54C/74C2526 • CGS54CT/74CT2526
1-to-8 Minimum Skew Clock Driver

The CGS 'C/CT2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications. The '2525 is designed to distribute a single clock to eight separate receivers with low skew across all outputs during both the t_{PLH} and t_{PHL} transitions. The '2526 is similar to the '2525 but contains a multiplexed clock input to allow for systems with dual clock speeds or systems where a separate test clock has been implemented.

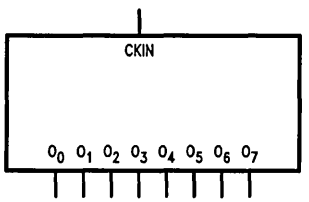
Features

- These CGS devices implement National's FACT™ family
- Ideal for signal generation and clock distribution
- Guaranteed pin to pin and part to part skew
- Multiplexed clock input ('2526)
- Guaranteed 2000V minimum ESD protection
- Symmetric output current drive of 24 mA for I_{OL}/I_{OH}
- 'CT has TTL-compatible inputs
- These products are identical to 74AC/ACT2525 and 2526

Ordering Code: See Section 5

Logic Symbols

'2525



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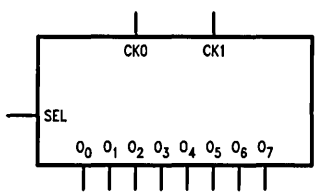
'2526

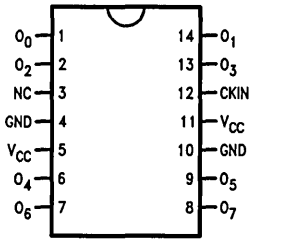


TL/F/10684-2

Connection Diagrams

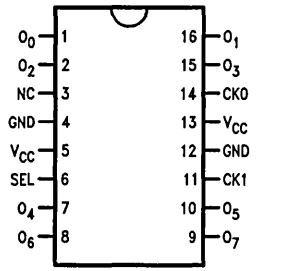
Pin Assignment for DIP, Flatpak and SOIC

'2525



TL/F/10684-3

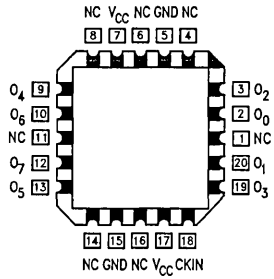
'2526



TL/F/10684-4

Pin Assignment for LCC

'2525



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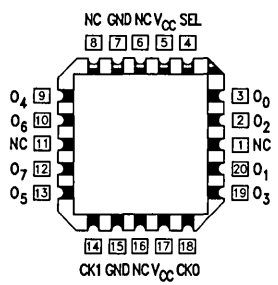
'2526



TL/F/10684-6

Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CK_n input will have an active effect on the outputs of the circuit. When SEL = 1, the CK_1 input is selected and when SEL = 0, the CK_0 input is selected. The non-selected CK_n input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK_{IN} or CK_1/CK_0 pins when either the multiplexed ('2526) or the straight ('2525) clock distribution chip is selected.

Pin Description

Pin Names	Description
CK_{IN}	Clock Input ('2525)
CK_0, CK_1	Clock Inputs ('2526)
O_0–O_7	Outputs
SEL	Clock Select ('2526)

Truth Tables

'2525

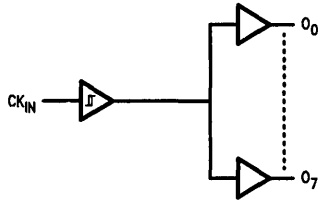
Inputs	Outputs
CK_{IN}	O_1–O_7
L	L
H	H

'2526

Inputs			Outputs
CK_0	CK_1	SEL	O_1–O_7
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

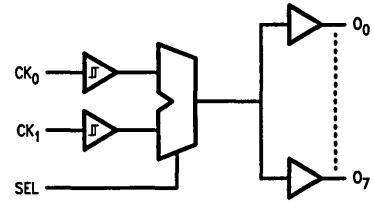
L = Low Voltage Level
H = High Voltage Level
X = Immaterial

'2525



TL/F/10684–7

'2526



TL/F/10684–8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+0.2 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = 0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 MA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of CGS circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'C	2.0V to 6.0V
'CT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
CGS74C/CT	−40°C to +85°C
CGS54C/CT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'C Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'CT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for CGS54C/74C Family Devices

Symbol	Parameter	V_{CC} (V)	CGS74C T_A = +25°C		CGS54C T_A = −55°C to +125°C	CGS74C T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.5[illegible]	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.40	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for CGS54C/74C Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	CGS74C $T_A = +25°C$	CGS54C $T_A = -55°C$ to $+125°C$	CGS74C $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for CGS54C @ 25°C is identical to CGS74C @ 25°C.

DC Electrical Characteristics for CGS54CT/74CT Family Devices

Symbol	Parameter	V_{CC} (V)	CGS74CT $T_A = +25°C$	CGS54CT $T_A = -55°C$ to $+125°C$	CGS74CT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for CGS54CT @ 25°C is identical to CGS74CT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter		V_{CC}* (V)	CGS74C $T_A = +25°C$ $C_L = 50$ pF			CGS54C $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74C $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
				Min	Typ	Max	Min	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay CK to O_n ('2525)		3.3	3.0	6.5	11.0	3.0	11.0	3.0		12.5	ns
			5.0	3.2	5.0	7.8	2.5	8.2	2.9		8.1	
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n ('2526)		3.3	3.0	7.0	13.0			3.0		14.0	ns
			5.0	3.6	5.5	7.8			3.3		8.6	
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2526)		3.3	3.0	8.0	14.0			3.0		15.0	ns
			5.0	4.0	6.5	8.5			3.5		9.5	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		3.3		0.3	1.0		1.5			1.0	ns
			5.0		0.2	0.7		1.0			0.7	
t_{OSLH}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		3.3		0.3	1.0		1.5			1.0	ns
			5.0		0.2	0.7		1.0			0.7	
t_{OST}	Maximum Skew Opposite Edge Output-to-Output (Note 1) Variation		5.0		0.4	1.0		1.5			1.0	ns
								1.0				
t_{PV}	Maximum Skew Part-to-Part Variation (Note 2)	'C2525 'CT2525 'C2526	5.0			3.5		4.0				ns
		'CT2526	5.0			5.0						ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (20% to 80% V_{CC})		5.0			3.0		4.0			3.75	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (0.8V/2.0V and 2.0V/0.8V)				0.9					1.1		ns

*Voltage Range 3.3 is 3.3V ±0.3V

Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the CLK to Q propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	CGS74CT $T_A = +25°C$ $C_L = 50$ pF			CGS54CT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74CT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay CK to O_n ('2525)	5.0	4.6	6.5	9.0			4.0	10.1	ns
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n ('2526)	5.0	5.8	8.5	11.1			5.1	12.4	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC}* (V)	CGS74CT $T_A = +25°C$ $C_L = 50$ pF			CGS54CT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74CT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
				Min	Typ	Max	Min	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2526)		5.0	5.1	8.5	12.4			4.4		14.1	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		5.0		0.2	0.7					0.7	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		5.0		0.2	0.7					0.7	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output (Note 1) Variation		5.0		0.4	1.0					1.0	ns
t_{PV}	Maximum Skew Part-to-Part Variation (Note 2)	AC2525 AC2526	5.0			3.5						ns
		ACT2526	5.0			5.0						ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (20% to 80% V_{CC})		5.0			3.0					3.75	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (0.8V/2.0V and 2.0V/0.8V)				0.9					1.1		ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance ('2525)	820 pF–1.2 x 10^{-18} (f)*	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance ('2526)	820 pF–1.2 x 10^{-18} (f)*	pF	V_{CC} = 5.0V

*f = frequency

Recommended Maximum Power Dissipation (W)

LFPM	T_A = 25°C		T_A = 85°C	
	PDIP	SOIC	PDIP	SOIC
0	1.105	0.858	0.528	0.41
225	1.493	1.055	0.714	0.504
500	1.71	1.210	0.820	0.578

National Semiconductor

CGS74CT2527
1-to-8 Minimum Skew (450 ps) Clock Driver

General Description

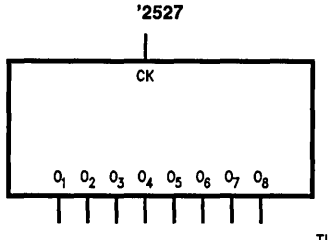
These minimum skew clock drivers are designed for Clock Generation and Support (CGS) applications operating at high frequencies. This device guarantees minimum output skew across the outputs of a given device. The '2527 is a minimum skew clock driver with one input driving eight outputs, specifically designed for clock distribution applications.

Features

- Guaranteed and tested: 450 ps Pin-to-pin skew (t_{OSHL} and t_{OHLH})
- High performance version of existing CGS74CT2525
- Implemented on National's FACT™ family process
- 1 input to 8 outputs low skew clock distribution
- Symmetric output current drive: 24 mA I_{OH}/I_{OL}
- Industrial temperature of −40°C to +85°C
- 28 pin PCC for optimum skew performance
- Guaranteed 2K volts ESD protection

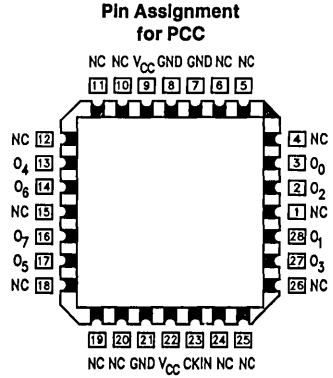
Ordering Code: See Section 5

Logic Symbol



TL/F/10981–2

Connection Diagram



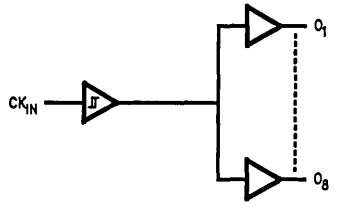
TL/F/10981–3

Functional Description

The output pins act as a single entity and will follow the state of the CK_{IN} when clock distribution chip is selected.

Pin Description

Pin Names	Description
CK_{IN}	Clock Input
O_1–O_8	Outputs



TL/F/10981–4

Truth Table

Inputs	Outputs
CK_{IN}	O_1–O_8
L	L
H	H

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_i = −0.5V	−20 mA
V_i = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_O)	
V_o = 0.5V	−20 mA
V_o = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 MA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature Coeff. (θ_J)	
PCC (0 LFM Air Flow)	71°C/W
PCC (225 LFM Air Flow)	53°C/W
PCC (500 LFM Air Flow)	47°C/W

Note: *Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of CGS circuits outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'CT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for CGS74CT Family Devices

Symbol	Parameter	V_{CC} (V)	CGS74CT T_A = +25°C		CGS74CT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
V_{OL}	Minimum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	mA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Minimum Quiescent Supply Current	5.5		8.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

over Recommended Operating Free Air Temperature Range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

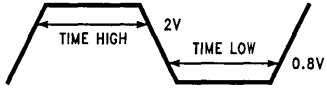
Symbol	Parameter	V_{CC}* (V)	CGS74CT2527						Units
			T_A = +25°C, C_L = 50 pF, R_L = 500Ω			T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω			
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Frequency	5.0					100		MHz
t_{PLH}	Low-to-High Propagation Delay CK to O_n	5.0	3.6		9.5	3.0		10.5	ns
t_{PHL}	High-to-Low Propagation Deay CK to O_n	5.0	3.6		9.5	3.0		10.5	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		150	450		150	450	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		150	450			450	ps
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)				1.5			1.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

Extended Electrical Characteristics: (66.67 MHz)

CGS74CT2527	T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω	Units
Time High*	4	ns
Time Low*	4	ns



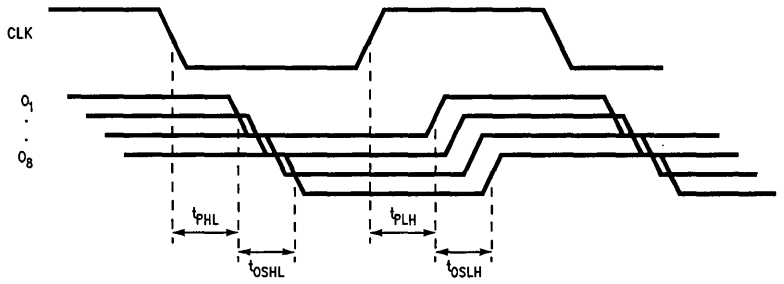
TL/F/10981–11

Time high is measured with outputs at above 2V.

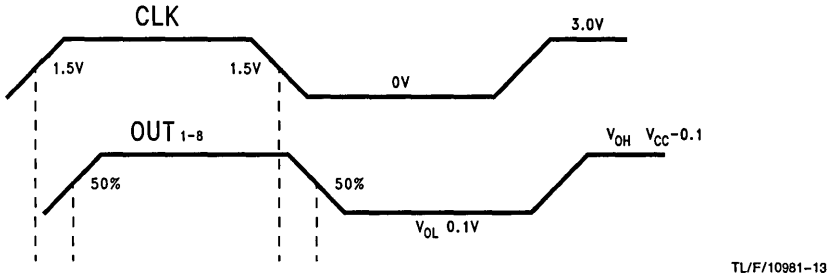
Time low is measured with outputs at below 0.8V.

Extended Electrical Characteristics: (66.67 MHz) (Continued)

1 to 8 Min-Skew Clock Driver

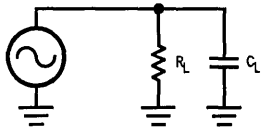


TL/F/10981–12



TL/F/10981–13

Test Circuit



TL/F/10981–14

R_L is 500Ω

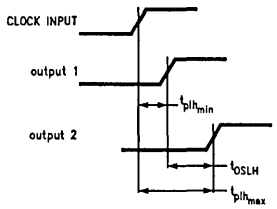
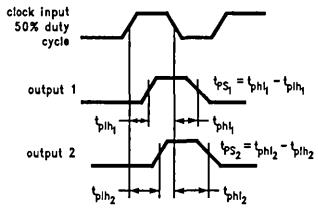
C_L is 50 pF for all prop delays and skew measurements.

Notes:

1. Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.
2. Load capacitance includes the test jig.

Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
t_{OSHL}, t_{OSLH} **Common Edge Skew:** Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = \lvert t_{PHL_{max}} - t_{PHL_{min}} \rvert$ Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = \lvert t_{PLH_{max}} - t_{PLH_{min}} \rvert$ Propagation delays are measured across the outputs of any given device.	 **FIGURE A**	• t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/ clock operations.
t_{PS} **Pin Skew or Transition Skew:** $t_{PS} = \lvert t_{PHL_i} - t_{PLH_i} \rvert$ Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. T_{PS} is the maximum difference for outputs i = 1 to 8 within a device package.	 **FIGURE B**	• t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).

National Semiconductor

CGS64/74B2528 550 ps 1 to 10 Minimum Skew Clock Driver

General Description

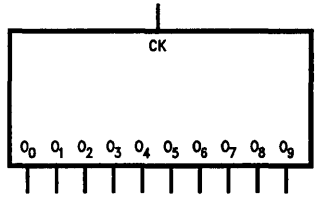
These minimum skew clock drivers are designed for Clock Generation & Support (CGS) applications operating above 50 MHz. This device guarantees minimum output skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The '2528 is a minimum skew clock driver with one input driving ten outputs, specifically designed for signal generation and clock distribution applications.

Features

- Clock Generation & Support (CGS) devices ideal for high frequency signal generation or clock distribution applications
- CGS64/74B version features National's Advanced Bipolar FAST® LSI process
- 1-to-10 low skew clock distribution
- 550 ps pin-to-pin output skew for the PCC package
- Specification for transition skew to meet duty cycle requirements
- 28-pin centered V_{CC} and GND configuration or PLCC to minimize high speed switching noise
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4K volts ESD protection
- Commercial and Industrial temperature availability

Ordering Code: See Section 5

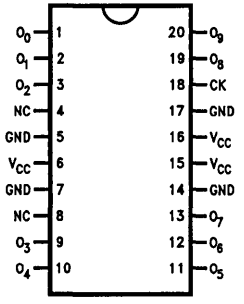
Logic Symbol



TL/F/10984–1

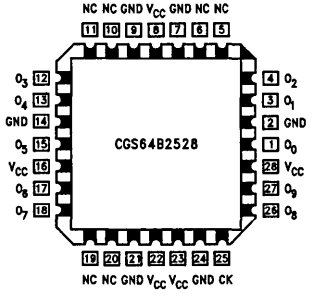
Connection Diagrams

Pin Assignment for DIP and SOIC



TL/F/10984–3

Pin Assignment for LCC



TL/F/10984–5

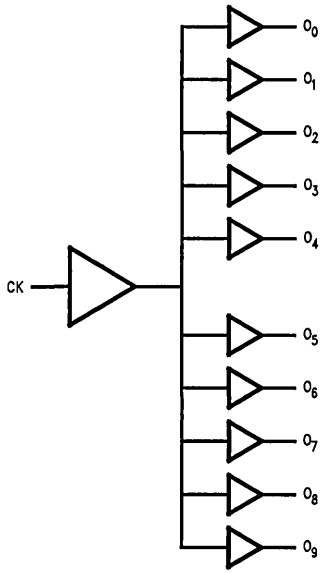
Pin Description

Pin Names	Description
CK	Clock Input ('2528)
O_0–O_9	Outputs

Truth Tables

Inputs	Outputs
CK	**O_0–O_9**
L	L
H	H

L = Low Logic Level
H = High Logic Level
X = Immaterial



TL/F/10984–7

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})		7.0V
Input Voltage (V_I)		7.0V
Operating Temperature	64 Grade	−40°C to +85°C
	74 Grade	0°C to +70°C
Storage Temperature Range		−65°C to +150°C

Typical θ_{JA}	M	N	V	
0 LFM	89	71	64	°C/W
225 LFM	71	57	52	°C/W
500 LFM	63	48	45	°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
High Level Input Voltage (V_{IH})	2V
Low Level Input Voltage (V_{IL})	0.8V
High Level Output Current (I_{OH})	−48 mA
Low Level Output Current (I_{OL})	64 mA
Free Air Operating Temperature 64 (T_A)	−40°C to +85°C
Free Air Operating Temperature 74 (T_A)	−0°C to +70°C

NOTE: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = 48 mA, V_{CC} = 4.5V		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 64 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.5	−0.75	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		24	35	mA
			Outputs Low		45	65	mA
C_{IN}	Input Capacitance	V_{CC} = 5V			5		pF

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω			Units
		Min	Typ	Max	
f_{MAX}	Frequency Maximum		80		MHz
t_{PLH}	Low-to-High Propagation Delay CK to O_n ('2528) M, N	3.0	4.5	7.0	ns
	Low-to-High Propagation Delay CK to O_n ('2528) V	2.5	4.5	6.5	
t_{PHL}	High-to-Low Propagation Delay CK to O_n ('2528) M, N	3.0	4.5	7.0	ns
	High-to-Low Propagation Delay CK to O_n ('2528) V	2.5	4.5	6.5	

Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

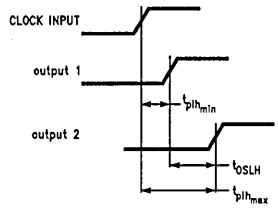
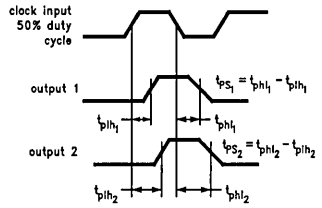
Symbol	Parameter	Package	V_{CC}* (V)	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω			Units
				Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation	N M V	5.0		0.15	800 650 550	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation	N M V	5.0		0.15	800 650 550	ps
t_{PS}	Maximum Skew Pin (Signal) Transition Variation	N M V	5.0		0.6	750 750 850	ps
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)	CGS74	5.0			1.5	ns
		CGS64	5.0			1.75	

*Voltage Range 5.0 is 5.0V ±0.5V

Note: t_{OSHL} and t_{OSLH} parameters are being tested and guaranteed at 1 MHz for V package. In addition V package is guaranteed by design at 66 MHz until Oct. 1993, when it will be fully production tested.

Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
t_{OSHL}, t_{OSLH} **Common Edge Skew:** Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = \lvert t_{PHL_{max}} - t_{PHL_{min}} \rvert$ Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = \lvert t_{PLH_{max}} - t_{PLH_{min}} \rvert$ Propagation delays are measured across the outputs of any given device.	 **FIGURE A**	• t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/clock operations.
t_{PS} **Pin Skew or Transition Skew:** $t_{PS} = \lvert t_{PHL_i} - t_{PLH_i} \rvert$ Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. T_{PS} is the maximum difference for outputs i = 1 8 to within a device package.	 **FIGURE B**	• t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).

National Semiconductor

PRELIMINARY

CGS64/74B2529
550 ps 1 to 10 Minimum Skew Clock Driver

General Description

This minimum skew clock driver is designed for Clock Generation and Support (CGS) applications operating from 33 MHz to 80 MHz. The devices guarantee minimum output skew across the outputs of a given device.

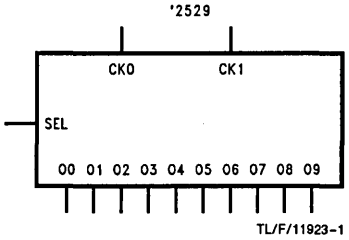
Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The '2529 is a minimum skew clock driver with two selectable inputs driving ten outputs

The SEL pin is used to determine which CKn will have an active effect on the outputs of the circuit. When SEL = 1, the CK1 input is selected and when SEL = 0, the CK0 input is selected. The non-selected CKn input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK inputs.

Features

- Clock Generation and Support (CGS) devices
- Ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST® LSI process
- 1-to-10 low skew clock distribution
- 550 ps pin-to-pin output skew (V package)
- Specification for transition skew to meet duty cycle requirements
- 20-center pin V_{CC} and GND configuration or PLCC to minimize high speed switching noise
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Logic Symbols



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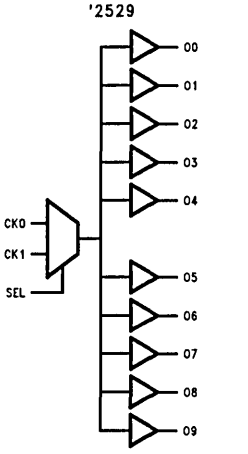

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Pin Description

Pin Names	Description
CK0, CK1	Clock Input ('2529)
O0–O9	Outputs
SEL	Clock Select ('2529)

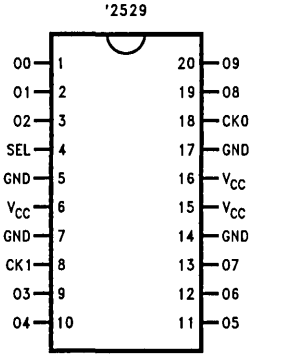
'2529

Inputs			Outputs
CK0	CK1	SEL	O0–O9
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

L = Low Logic Level
H = High Logic Level
X = Immaterial

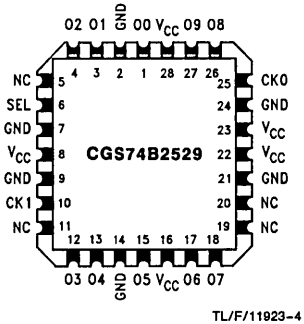
Connection Diagrams

Pin Assignment PDIP and SOIC



TL/F/11923-3

Pin Assignment for PCC



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) 7.0V

Input Voltage (V_I) 7.0V

Operating Temperature

64 Grade −40°C to +85°C

74 Grade 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Typical θ_{JA}

Airflow	M	N	V	
0 LFM	89	71	64	°C/W
225 LFM	71	57	52	°C/W
500 LFM	63	48	45	°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
High Level Input Voltage (V_{IH})	2V
Low Level Input Voltage (V_{IL})	0.8V
High Level Output Current (I_{OH})	−48 mA
Low Level Output Current (I_{OL})	64 mA
Free Air Operating Temperature (T_A)	
64 Grade	−40°C to +85°C
74 Grade	0°C to +70°C

Note: *The Absolule Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating free air temprature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = 48 mA, V_{CC} = 4.5V		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 64 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.5	−0.75	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current '2528	V_{CC} = 5.5V	Outputs High		24	35	mA
			Outputs Low		45	65	mA
C_{IN}	Input Capacitance	V_{CC} = 5.5V			5		pF

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter		V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω			Units
			Min	Typ	Max	
f_{MAX}	Frequency Maximum			80		MHz
t_{PLH}	Low-to-High Propagation Delay CK0,1 to O_n	M, N	3.0	5.5	7.0	ns
	Low-to-High Propagation Delay CK0,1 to O_n	V	2.5	5.5	6.0	
t_{PHL}	High-to-Low Propagation Delay CK0,1 to O_n	M, N	3.0	5.5	7.0	ns
	High-to-Low Propagation Delay CK0,1 to O_n	V	2.5	5.5	6.0	

Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

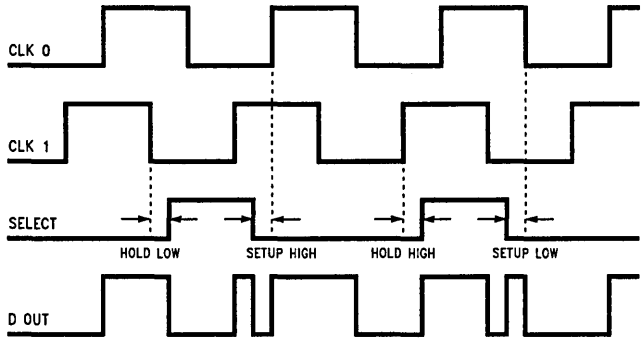
Symbol	Parameter	Package	V_{CC}* (V)	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω			Units
				Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation	N M V	5.0		0.15	800 650 500	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation	N M V	5.0		0.15	800 650 500	ps
t_{PS}	Maximum Skew Pin (Signal) Transition Variation	N M V	5.0		0.6	750 750 850	ps
t_{Set}**	Setup Time High Select to CLK0 or 1 Setup Time Low Select to CLK0 or 1	All	5.0	−2.0 −2.0			ns
t_{Hold}**	Hold Time High Select to CLK0 or 1 Hold Time Low Select to CLK0 or 1	All	5.0	2.0 4.0			ns
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)	CGS74	5.0			1.5	ns
		CGS64	5.0			1.75	

Note: t_{OSHL} and t_{OSLH} parameters are being tested and guaranteed at 1 MHz for V package. In addition, V package is guaranteed by design at 66 MHz until Oct. 1993, when it will be fully production tested.

*Voltage Range 5.0 is 5.0V ±0.5V

**A negative setup time indicates that the correct logic levels may be initiated sometimes after the active transition of the timing pulse.

Timing Diagram for the CGS74/64B2529



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National Semiconductor

CGS74B303 Octal Divide-by-2 Skew Clock Driver

General Description

These minimum skew clock drivers are designed for high frequency Clock Generation and Support (CGS) applications. These devices are ideal for duty cycle recovery applications with internal frequency divide-by-2 circuitry. The devices guarantee minimum output skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems.

Functional Description

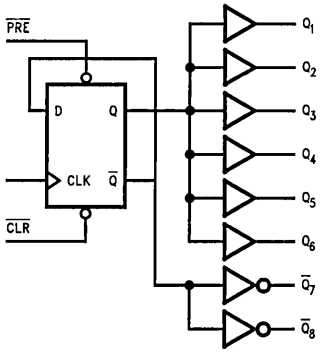
The CGS74B303 contains eight flip-flops designed to have low skew between outputs. The eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set Q and $\overline{Q}$ outputs high or low independent of CLK pin.

Features

- Clock Generation and Support (CGS) Devices ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST™ LSI process
- 1 ns pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- Current sourcing 24 mA and current sinking of 48 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Ordering Code: See Section 5

Logic Diagram



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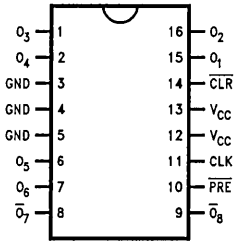
Connection Diagrams

Pin Assignment for DIP and SOIC



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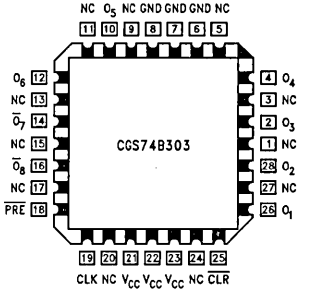
Pin Assignment for 28-Pin PCC



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Pin Description

Pin Names	Description
CLK	Clock Input
O_1–O_8	Outputs
$\overline{PRE}$	Preset
$\overline{CLR}$	Clear

Truth Table

Inputs			Outputs	
$\overline{CLR}$	$\overline{PRE}$	CLK	O_1–O_5	$\overline{O_7}$–$\overline{O_8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	L*	L*
H	H	↑	$\overline{Q}$	Q
H	H	L	Q	$\overline{Q}$

*This state will not persist when $\overline{CLR}$/$\overline{PRE}$ returns to high.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})				7.0V	
Input Voltage (V_I)				7.0V	
Operating Free	74B303		0°C to +70°C		
Air Temperature	64B303		−40°C to +85°C		
Storage Temperature Range			−65°C to +150°C		
Typical θ_{JA}			303/304/305		
Airflow (LFM)	0	225	500		
Plastic (N) Package	95	70	60	°C/W	
Jedec SOIC (M) Package	118	96	86	°C/W	
PCC (V) Package	69	53	45	°C/W	

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
High Level Input Voltage (V_{IH})	2V
Low Level Input Voltage (V_{IL})	0.8V
High Level Output Current (I_{OH})	−24 mA
Low Level Output Current (I_{OL})	48 mA
Free Air Operating Temperature (T_A)	0 to 70°C

NOTE: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics CGS74/64B303/304/305

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V		V_{CC} − 2			V
		I_{OH} = 24 mA, V_{CC} = 4.5V		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 48 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	m A
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.1	−0.50	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current 303	V_{CC} = 5.5V	Outputs High		27	60	mA
			Outputs Low		45	60	mA
I_{CC}	Supply Current 304	V_{CC} = 5.5V	Outputs High		20	30	mA
			Outputs Low		42	55	mA
I_{CC}	Supply Current 305	V_{CC} = 5.5V	Outputs High		35	45	mA
			Outputs Low		42	55	mA
C_{IN}	Input Capacitance	V_{CC} = 5V			5		pF

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter		CGS74B303 V_{CC} = 4.5V to 5.5V, T_A = 0°C to +70°C, C_L = 0 pF–50 pF, R_L = 500Ω			CGS64B303 V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C, C_L = 0 pF–50 pF, R_L = 500Ω			Units
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Input Frequency		110			100			MHz
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n	M, N	4		8	4		8	ns
		V	4		8.5	4		9	
t_{PLH}, t_{PHL}	Propagation Delay PRE/CLR		3		12	3		12	ns
t_{SU}	Set Up Time before CLK		5			5			ns
t_W	CLK HI		4			4			ns
	CLK LO		4			4			
	CLR/PRE		4			4			

Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter		V_{CC}* (V)	CGS74B303 V_{CC} = 4.5V to 5.5V, T_A = 0°C to +70°C, C_L = 0 pF–50 pF, R_L = 500Ω			CGS64B303 V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C, C_L = 0 pF–50 pF, R_L = 500Ω			Units
				Min	Typ	Max	Min	Typ	Max	
t_{OSHL} Q	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.5	1.0		0.5	1.0	ns
t_{OSLH} Q	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.5	1.0		0.5	1.0	ns
t_{OSHL} $\overline{Q}$	Maximum Skew Common Edge	M, N	5.0		0.3	0.6		0.3	0.6	ns
	Output-to-Output Variation (Note 1)	V			0.3	0.75		0.3	0.75	
t_{OSLH} $\overline{Q}$	Maximum Skew Common Edge	M, N	5.0		0.3	0.6		0.3	0.6	ns
	Output-to-Output Variation (Note 1)	V			0.3	0.75		0.3	0.75	
$t_{OSLH/HL}$ Q,$\overline{Q}$	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		1.0	1.6		1.0	1.75	ns
t_{PS} Q	Maximum Skew Pin (Signal) Transition Variation (Note 1)		5.0			1.0			1.2	ns
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) 0 pF–30 pF Loads		5.0		1.1 0.9	2.0 2.0		1.1 0.9	2.0 2.0	ns

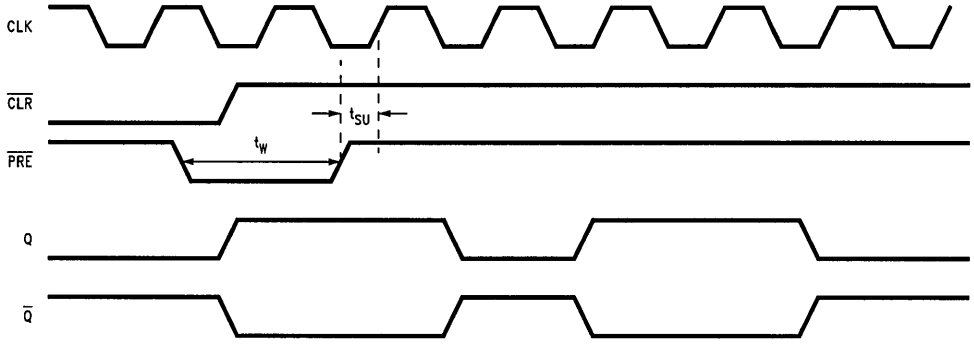
*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

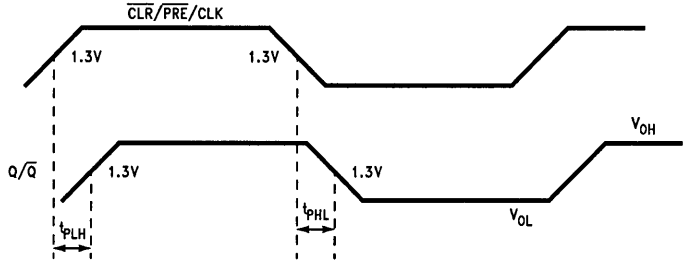
Note 2: This device is sensitive to noise due to the large transient currents which occur during multiple switching of the eight outptus. V_{VV} by-pass capacitor(s), chip types, must be placed as closely as possible to the V_{CC} pin.

Timing Diagrams

Minimum Skew Divide-by-2 Clock Drivers
CGS74B303, CGS74B304, CGS74B305

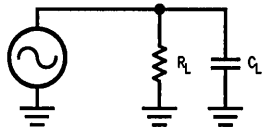


TL/F/10966–4



TL/F/10966–5

Test Circuit



R_L is 500Ω
C_L is 50 pF for all prop delays and skew measurements.
C_L is 30 pF for t_{rise} and t_{fall} measurements.

TL/F/10966–6

Notes:

- Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.
- All input pulses are from 3.5V to 0.3V with rise and fall times of 2.0 ns.
- Load capacitance includes the test jig.

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CGS74B304 Octal Divide-by-2 Skew Clock Driver

General Description

These minimum skew clock drivers are designed for high frequency Clock Generation & Support (CGS) applications. These devices are ideal for duty cycle recovery applications with internal frequency divide-by-2 circuitry. The devices guarantee minimum output skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems.

Functional Description

The CGS74B304 contains eight flip-flops designed to have low skew between outputs. The eight outputs (eight in-phase with CLK) toggle on successive CLK pulses.

$\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set Q and Q outputs high or low independent of CLK pin.

Features

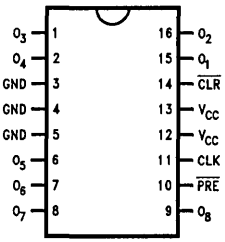
- Clock Generation & Support (CGS) devices ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST™ LSI process
- 900 ps pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- Current sourcing 24 mA and current sinking of 48 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Ordering Code: See Section 5

Connection Diagrams

Pin Assignment for DIP and SOIC

'304



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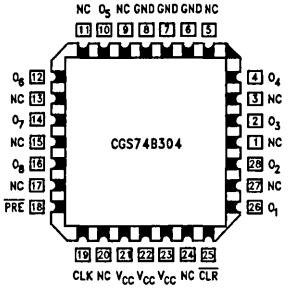
Pin Assignment 28-Pin PCC



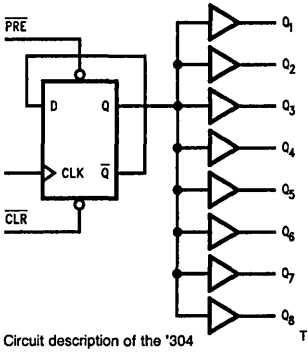
TL/F/11750-2

Pin Description

Pin Names	Description
CLK	Clock Input
O_1–O_8	Outputs
$\overline{PRE}$	Preset
$\overline{CLR}$	Clear

Logic Diagram

CGS74B304



Circuit description of the '304

TL/F/11750-3

Truth Table

CGS74B304

Inputs			Outputs
CLR	PRE	CLK	O_1–O_8
L	H	X	L
H	L	X	H
L	L	X	L*
H	H	↑	$\overline{Q}_0$
H	H	L	Q_0

*This state will not persist when CLR/PRE returns to high.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})		7.0V
Input Voltage (V_I)		7.0V
Operating Free Air Temperature	74B303	0°C to +70°C
	64B303	−40°C to +85°C
Storage Temperature Range		−65°C to +150°C

Typical θ_{JA}			303/304/305	
Airflow (LFM)	0	225	500	°C/W
Plastic (N) Package	95	70	60	°C/W
Jedec SOIC (M) Package	118	96	86	°C/W
PCC (V) Package	69	53	45	°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
High Level Input Voltage (V_{IH})	2V
Low Level Input Voltage (V_{IL})	0.8V
High Level Output Current (I_{OH})	−24 mA
Low Level Output Current (I_{OL})	48 mA
Free Air Operating Temperature (T_A)	0 to 70°C

NOTE: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics CGS74/64B303/304/305

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V		V_{CC} − 2			V
		I_{OH} = 24 mA, V_{CC} = 4.5V		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 48 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.1	−0.50	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current 303	V_{CC} = 5.5V	Outputs High		27	60	mA
			Outputs Low		45	60	mA
I_{CC}	Supply Current 304	V_{CC} = 5.5V	Outputs High		20	30	mA
			Outputs Low		42	55	mA
I_{CC}	Supply Current 305	V_{CC} = 5.5V	Outputs High		35	45	mA
			Outputs Low		42	55	mA
C_{IN}	Input Capacitance	V_{CC} = 5V			5		pF

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	CGS74B304 V_{CC} = 4.5V to 5.5V, T_A = 0°C to +70°C, C_L = 0 pF–50 pF, R_L = 500Ω			CGS64B304 V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C, C_L = 0 pF–50 pF, R_L = 500Ω			Units
		Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Input Frequency	110			100			MHz
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n	4		8.5	4		8.5	ns
t_{PLH}, t_{PHL}	Propagation Delay PRE/CLR	4		11	4		11	ns
t_{SU}	Set Up Time before CLK	5			5			ns
t_W	CLK HI CLK LO CLR/PRE	4 4 4			4 4 4			ns

Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter		V_{CC}* (V)	CGS74B304 T_A = 0°C to +70°C, C_L = 0 pF–50 pF, R_L = 500Ω			CGS64B304 T_A = −40°C to +85°C, C_L = 0 pF–50 pF, R_L = 500Ω			Units
				Min	Typ	Max	Min	Typ	Max	
t_{OSHL} Q	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.5	0.9		0.5	0.9	ns
t_{OSLH} Q	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.5	0.9		0.5	0.9	ns
t_{PS}	Maximum Skew. Pin (Signal) Transition Variation (Note 1)	PDIP	5.0			1.1			1.1	ns
		SOIC	5.0			1.1			1.1	
		PCC	5.0			1.3			1.3	
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) 0 pF–30 pF Loads		5.0		1.1 0.9	2.0 2.0		1.1 0.9	2.0 2.0	ns

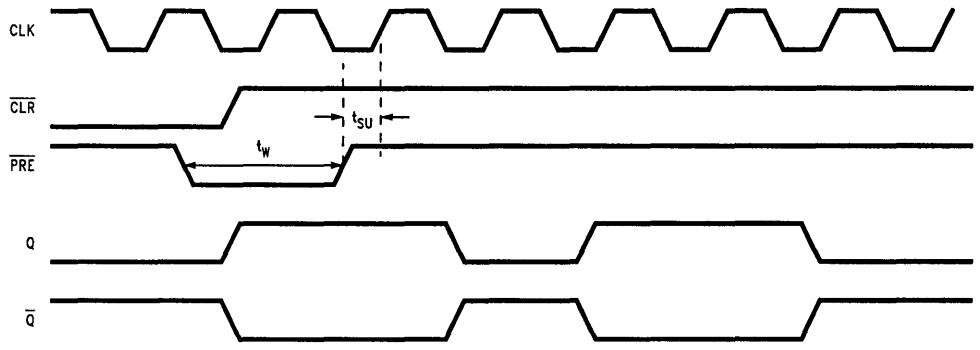
*Voltage Range 5.0 is 5.0V ±0.5V.

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: This device is sensitive to noise due to the large transient currents which occur during multiple switching of the outputs. V_{CC} bypass capacitor(s), chip types, must be placed as closely as possible to the V_{CC} pin.

Timing Diagrams

Minimum Skew Divide-by-2 Clock Drivers
CGS74B303, CGS74B304, CGS74B305



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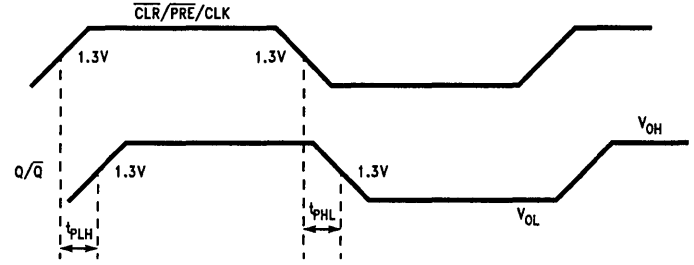

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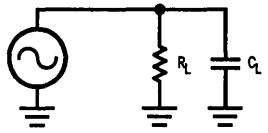
Test Circuit



TL/F/11750–6

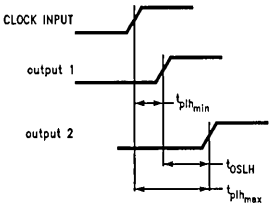
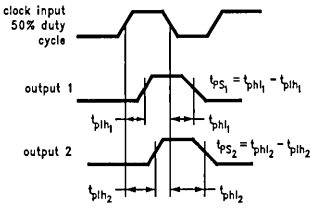
R_L is 500Ω
C_L is 50 pF for all prop delays and skew measurements.
C_L is 30 pF for t_{rise} and t_{fall} measurements.

Notes:

- Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.
- All input pulses are from 3.5V to 0.3V with rise and fall times of 2.0 ns.
- Load capacitance includes the test jig.

Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
t_{OSHL}, t_{OSLH} **Common Edge Skew:** Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = \lvert t_{PHL_{max}} - t_{PHL_{min}} \rvert$ Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = \lvert t_{PLH_{max}} - t_{PLH_{min}} \rvert$ Propagation delays are measured across the outputs of any given device.	 **FIGURE A**	• t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/ clock operations.
t_{PS} **Pin Skew or Transition Skew:** $t_{PS} = \lvert t_{PHL_i} - t_{PLH_i} \rvert$ Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. T_{PS} is the maximum difference for outputs i = 1 to 8 within a device package.	 **FIGURE B**	• t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).

National Semiconductor

CGS74B305
Octal Divide-by-2 Skew Clock Driver

General Description

These minimum skew clock drivers are designed for high frequency Clock Generation & Support (CGS) applications. These devices are ideal for duty cycle recovery applications with internal frequency divide-by-2 circuitry. The devices guarantee minimum output skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems.

Functional Description

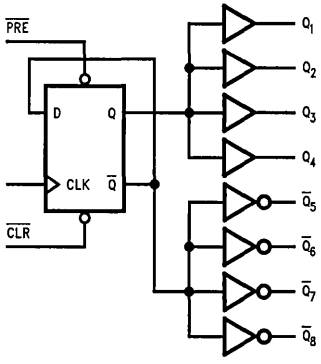
The CGS74B305 contains eight flip-flops designed to have low skew between outputs. The eight outputs (four in-phase with CLK and four out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set Q and Q outputs high or low independent of CLK pin.

Features

- Clock Generation & Support (CGS) devices ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST™ LSI process
- 750 ps pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- Current sourcing 24 mA and current sinking of 48 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Ordering Code: See Section 5

Logic Diagram



Circuit description of the '305 TL/F/11751–3

Pin Description

Pin Names	Description
CLK	Clock Input
O_1–O_8	Outputs
PRE	Preset
CLR	Clear

Truth Table

CGS74B305

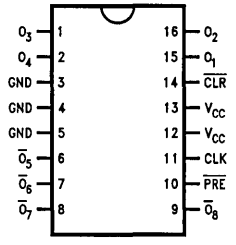
Inputs			Outputs	
CLR	PRE	CLK	O_1–O_4	$\overline{O}_5$–$\overline{O}_8$
L	H	X	L	H
H	L	X	H	L
L	L	X	L*	L*
H	H	↑	$\overline{Q}_0$	Q_0
H	H	L	Q_0	$\overline{Q}_0$

*This state will not persist when CLR/PRE returns to high.

Connection Diagrams

Pin Assignment for DIP and SOIC

'305



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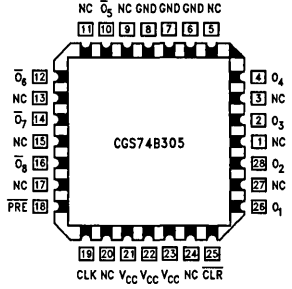
Pin Assignment 28-Pin PCC



TL/F/11751–2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})			7.0V	
Input Voltage (V_I)			7.0V	
Operating Free Air Temperature	74B303		0°C to +70°C	
	64B303		−40°C to +85°C	
Storage Temperature Range			−65°C to +150°C	
Typical θ_{JA}			303/304/305	
Airflow (LFM)	0	225	500	°C/W
Plastic (N) Package	95	70	60	°C/W
Jedec SOIC (M) Package	118	96	86	°C/W
PCC (V) Package	69	53	45	°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
High Level Input Voltage (V_{IH})	2V
Low Level Input Voltage (V_{IL})	0.8V
High Level Output Current (I_{OH})	−24 mA
Low Level Output Current (I_{OL})	−48 mA
Free Air Operating Temperature (T_A)	0°C to 70°C

NOTE: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics CGS74/64B303/304/305

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V		V_{CC} − 2			V
		I_{OH} = 24 mA, V_{CC} = 4.5V		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 48 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	m A
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.1	−0.50	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current 303	V_{CC} = 5.5V	Outputs High		27	60	mA
			Outputs Low		45	60	mA
I_{CC}	Supply Current 304	V_{CC} = 5.5V	Outputs High		20	30	mA
			Outputs Low		42	55	mA
I_{CC}	Supply Current 305	V_{CC} = 5.5V	Outputs High		35	45	mA
			Outputs Low		42	55	mA
C_{IN}	Input Capacitance	V_{CC} = 5V			5		pF

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	CGS74B305 V_{CC} = 4.5V to 5.5V, T_A = 0°C to 70°C, C_L = 0 pF–50 pF, R_L = 500Ω			CGS64B305 V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C, C_L = 0 pF–50 pF, R_L = 500Ω			Units
		Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Input Frequency	130			120			MHz
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n	4		8.5	4		8.5	ns
t_{PLH}, t_{PHL}	Propagation Delay PRE/CLR	4 4		10.5 10.5	4 4		11 11	ns
t_{SU}	Set Up Time before CLK	5			5			ns
t_W	CLK HI CLK LO CLR/PRE	4 4 4			4 4 4			ns

Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter		V_{CC}* (V)	CGS74B305 T_A = 0°C to 70°C, C_L = 0 pF–50 pF, R_L = 500Ω			CGS64B305 T_A = −40°C to +85°C, C_L = 0 pF–50 pF, R_L = 500Ω			Units
				Min	Typ	Max	Min	Typ	Max	
t_{OSHL} Q	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.4	0.75		0.4	0.75	ns
t_{OSLH} Q	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.4	0.75		0.4	0.75	ns
t_{OSHL} $\overline{Q}$	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.4	0.75		0.4	0.75	ns
t_{OSLH} $\overline{Q}$	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.4	0.75		0.4	0.75	ns
$t_{OSLH/HL}$ Q,$\overline{Q}$	Maximum Skew Common Edge Output-to-Output Variation (Note 1)		5.0		0.9	1.45		0.9	1.45	ns
t_{PS}	Maximum Skew Pin (Signal) Transition Variation (Note 1)	PDIP	5.0			1.45			1.45	ns
		SOIC	5.0			1.45			1.45	
		PCC	5.0			1.35			1.35	
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) 0 pF–30 pF Loads		5.0		1.1 0.9	2.0 2.0		1.1 0.9	2.0 2.0	ns

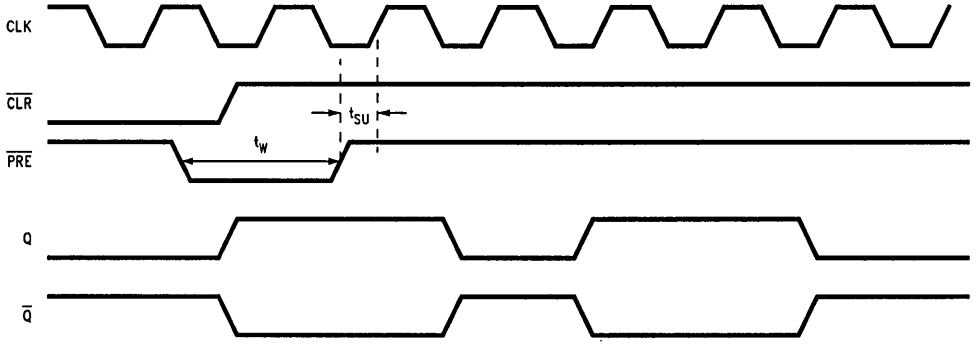
*Voltage Range 5.0 is 5.0V ±0.5V.

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: This device is sensitive to noise due to the large transient currents which occur during multiple switching of the outputs. V_{CC} bypass capacitor(s), chip types, must be placed as closely as possible to the V_{CC} pin.

Timing Diagrams

Minimum Skew Divide-by-2 Clock Drivers
CGS74B303, CGS74B304, CGS74B305



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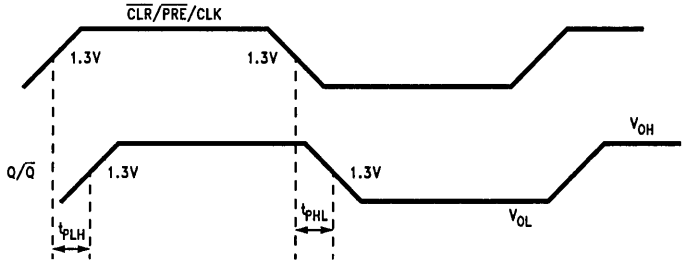

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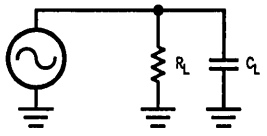
Test Circuit



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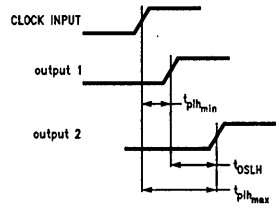
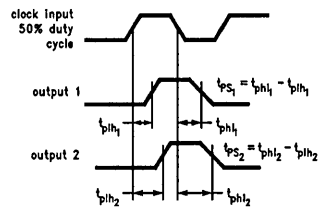
R_L is 500Ω
C_L is 50 pF for all prop delays and skew measurements.
C_L is 30 pF for t_{rise} and t_{fall} measurements.

Notes:

- Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.
- All input pulses are from 3.5V to 0.3V with rise and fall times of 2.0 ns.
- Load capacitance includes the test jig.

Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
t_{OSHL}, t_{OSLH} **Common Edge Skew:** Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = \lvert t_{PHL_{max}} - t_{PHL_{min}} \rvert$ Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = \lvert t_{PLH_{max}} - t_{PLH_{min}} \rvert$ Propagation delays are measured across the outputs of any given device.	 **FIGURE A**	• t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/ clock operations.
t_{PS} **Pin Skew or Transition Skew:** $t_{PS} = \lvert t_{PHL_i} - t_{PLH_i} \rvert$ Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. T_{PS} is the maximum difference for outputs i = 1 to 8 within a device package.	 **FIGURE B**	• t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).

National Semiconductor

CGS100P2530
PECL-TTL 1 to 10 Minimum Skew Clock Driver
CGS100P2531
PECL-TTL 2 to 10 Minimum Skew Clock Driver

General Description

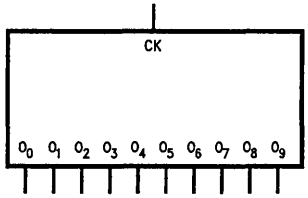
These minimum skew clock drivers are designed for Clock Generation & Support (CGS) applications, particularly for ECL to TTL clock tree distribution schemes. The '2530 and '2531 are single supply devices with guaranteed minimum output skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The '2530 is a minimum skew clock driver with one input driving ten outputs and the '2531 is a selectable two input to 10 outputs, specifically designed for signal generation and clock distribution applications.

Features

- PECL-TTL version of National's CGS74B2528 TTL clock drivers
- Clock Generation & Support (CGS) devices ideal for ECL and TTL clock trees with CGS 100311
- 1-to-10 or 2-to-10 low skew clock distribution
- 550 ps pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- 28-pin PCC to minimize high speed switching noise and for low dynamic power consumption
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Logic Symbols

'2530



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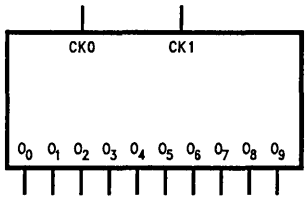
'2531



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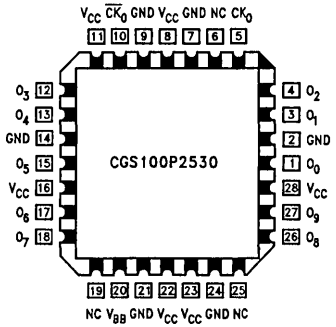
Connection Diagrams

Pin Assignment for LCC



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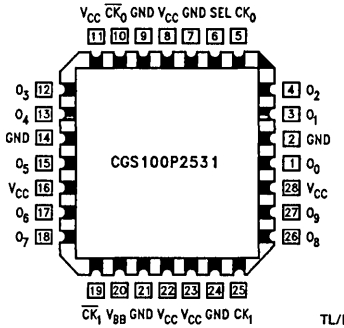

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Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CKn will have an active effect on the outputs of the circuit. When SEL = 1, the CK1 input is selected and when SEL = 0, the CK0 input is selected. The non-selected CKn input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK, CK1/CK0 pins when either the multiplexed ('2531) or the straight ('2530) clock distribution chip is selected.

Pin Description

Pin Names	Description
CK	PECL Differential Clock Input ('2530)
CK0, CK1	PECL Differential Clock Input ('2531)
O_0–O_9	TTL Outputs
SEL	PECL Clock Select ('2531)

Truth Tables

'2530

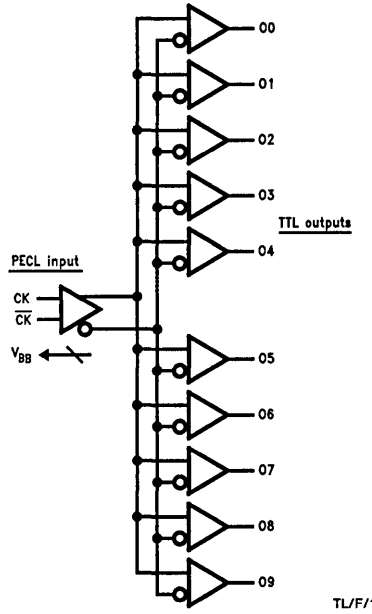
Inputs		Outputs
CK	$\overline{CK}$	O_0–O_9
L	H	L
H	L	H
L	L	U
H	H	U
L	V_{BB}	L*
H	V_{BB}	H*
V_{BB}	X	V_{BB}

L = Low Logic Level
H = High Logic Level
X = Don't Care
U = Undefined
* = Single Ended Operation

'2531

Inputs					Outputs
CK0	$\overline{CK0}$	CK1	$\overline{CK1}$	SEL	O_0–O_9
L	H	X	X	L	L
H	L	X	X	L	H
L	L	X	X	L	U
H	H	X	X	L	U
L	V_{BB}	X	X	L	L*
H	V_{BB}	X	X	L	H*
X	X	L	H	H	L
X	X	H	L	H	H
X	X	L	L	H	U
X	X	H	H	H	U
X	X	L	V_{BB}	H	L*
X	X	H	V_{BB}	H	H*

'2530



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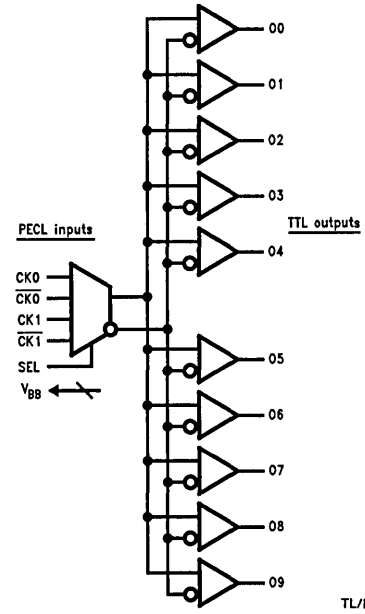
'2531



TL/F/10983–6

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature Plastic	150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
TTL Input Voltage (Note 2)	−0.5V to +7.0V
TTL Input Current (Note 2)	−30 mA to +5.0 mA
V_{BB} Output Current	−5.0 mA to +1.0 mA
ECL Input Potential to GND Pin	−0.5V to V_{CC} +0.5V
Typical θ_{JA}	V Package
0 LFM Airflow	69
225 LFM	53
500 LFM	45
Voltage Applied to Output (with V_{CC} = 0V)	−0.5V to V_{CC}
Current Applied to Output in Low State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V

Recommended Operating Conditions

Operating Free Air Temperature Range	−40°C to +85°C
Supply Voltage	4.5V to 5.5V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage		I_{OH} = −3 mA, V_{CC} = 4.5V	2.4			V
			I_{OH} = 48 mA, V_{CC} = 4.5V	2.0			
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V, I_{OL} = 64 mA		0.375	0.55	V
V_{BB}	Output Reference Voltage		$I_{V_{BB}}$ = −1 mA	V_{CC} − 1.38		V_{CC} − 1.26	V
V_{DIFF}	Input Voltage Differential		Required for Full Output Swing	150			mV
V_{CM}	Common Mode Voltage		High Level	V_{CC} − 1.6		V_{CC} − 0.4	V
V_{IH}	Input High Voltage		Guarantee HIGH Signal for All Inputs	V_{CC} − 1.165		V_{CC} − 0.87	V
V_{IL}	Input Low Voltage		Guarantee HIGH Signal for All Inputs	V_{CC} − 1.83		V_{CC} − 1.475	V
I_{IL}	Low Level Input Current		V_{IN} = V_{IL} (min)	0.50			μA
I_{IH}	High Level Input Current		V_{IN} = V_{IH} (max)			50	μA
I_{CBO}	Input Leakage Current		V_{IN} = 0	−10			μA
I_{CCH}	Supply Current	'2530	V_{CC} = 5.5V			30	mA
		'2531				33	
I_{OS}	Output Current Drive		V_{CC} = 5.5V, V_O = 2.25V	−50		−150	mA
I_{CCL}	Supply Current	'2530	V_{CC} = 5.5V			72	mA
		'2531				75	

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	CGS100P V_{CC} = 4.5V to 5.5V T_A = −40°C to +85°C C_L = 50 pF R_L = 500Ω			Units
		Min	Typ	Max	
f_{MAX}	Frequency Maximum	70			MHz
t_{PLH}	Low-to-High Propagation Delay CK to O_n ('2530)	3.4	5.0	7.0	ns
t_{PHL}	High-to-Low Propagation Delay CK to O_n ('2530)	3.4	5.0	7.0	ns
t_{PLH}, t_{PHL}	Propagation Delay CKn to O_n ('2531)	4.0 4.0	5.0 5.0	8.0 8.0	ns
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2531)	5.0 5.0	5.0 5.0	10.0 10.0	ns

Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

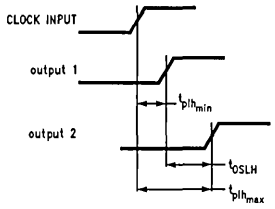
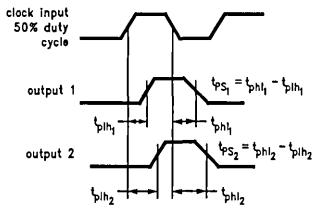
Symbol	Parameter	V_{CC} (V)*	CGS100P T_A = −40°C to +85°C C_L = 50 pF R_L = 500Ω			Units
			Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		150	550	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.5		150	550	ps
t_{PS}	Maximum Skew Pin (Signal) Transition Variation (Note 1)	5.0		0.6	1.1	ns
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)	5.0		1.0	1.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design. See Figures A and B of Parameter Measurement Information.

Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
t_{OSHL}, t_{OSLH} **Common Edge Skew:** Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = \lvert t_{PHL_{max}} - t_{PHL_{min}} \rvert$ Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = \lvert t_{PLH_{max}} - t_{PLH_{min}} \rvert$ Propagation delays are measured across the outputs of any given device.	 **FIGURE A**	• t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/ clock operations.
t_{PS} **Pin Skew or Transition Skew:** $t_{PS} = \lvert t_{PHL_i} - t_{PLH_i} \rvert$ Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. t_{PS} is the maximum difference for outputs i = 1 to 8 within a device package.	 **FIGURE B**	• t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).

National Semiconductor

PRELIMINARY

CGS2534V Commercial/CGS2534TV Industrial Quad Memory Array Clock Drivers

General Description

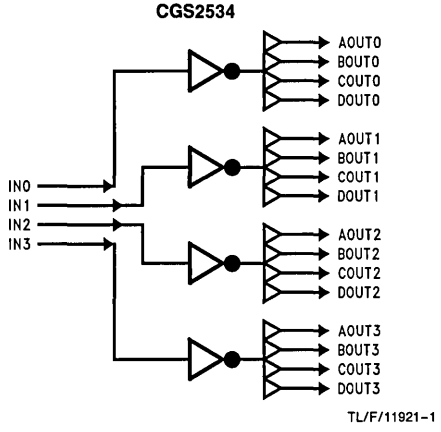
These Clock Generation and Support clock drivers are specifically designed for driving memory arrays requiring large fanouts while operating at high speeds,

CGS2534 is a 4 to 16 inverting driver with TTL compatible I/Os. This device has minimum skew specifications of 500 ps pin-to-pin as well as a 1 ns specification for part-to-part propagation delay variation.

Features

- Guaranteed and tested: 500 ps pin-to-pin skew (t_{OSHL} and t_{OHLH})
- Implemented on National's ABT family process
- Symmetric output current drive: −36/36 mA $I_{OH/IOL}$
- Industrial temperature of −40°C to +85°C
- 28-pin PLCC for optimum skew performance
- Symmetric package orientation
- Large fanout for memory driving applications
- Guaranteed 2 kV ESD protection

Logic Diagram



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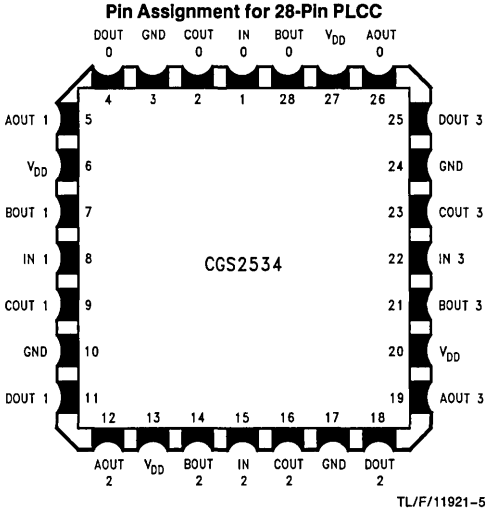
Connection Diagram



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Truth Table

Device	Input	Output
CGS2534	In(0–3)	$\overline{ABCD}$ Out (0–3)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})		7.0V
Input Voltage (V_I)		7.0V
Operating Temperature		
Industrial Grade		−40°C to +85°C
Commercial Grade		0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Typical θ_{JA}	**Airflow**	**V**
	0 LFM	62 °C/W
	225 LFM	43 °C/W
	500 LFM	34 °C/W
	900 LFM	27 °C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.75V to 5.25V
High Level Input Voltage (V_{IH})	2V
Low Level Input Voltage (V_{IL})	0.8V
High Level Output Current (I_{OH})	−36 mA
Low Level Output Current (I_{OL})	36 mA
Free Air Operating Temperature (T_A)	
Industrial	−40°C to +85°C
Commercial	0°C to +70°C

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2.0			V
V_{IK}	Input Clamp Voltage	V_{CC} = 4.75V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −3 mA, V_{CC} = 4.75V	2.4			V
		I_{OH} = −36 mA, V_{CC} = 4.75V	2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 36 mA		0.35	0.44	V
		V_{CC} = 4.75V, I_{OL} = 50 μA		0.1	0.1	
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.25V, V_{IH} = 7V			7	μA
I_{IH}	High Level Input Current	V_{CC} = 5.25V, V_{IH} = 2.7V			5	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.25V, V_{IL} = 0.4V	−5			μA
I_{OS}	Output Drive Current	V_{CC} = 5.25V, V_O = 0V	−100		275	mA
I_{OLD}	Minimum Dynamic Output Current*	V_{CC} = 5.25V, V_{OLD} = 1.65V Max		50	75	mA
I_{CCT}	Maximum I_{CC}/Input	V_{CC} = 5.25V			2.5	mA
I_{CC}	Supply Current '2534 (Quiescent)	V_{CC} = 5.25V			80	μA
C_{IN}	Input Capacitance	V_{CC} = 5V		5		pF

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

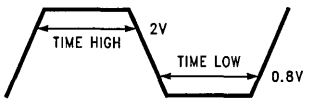
Symbol	Parameter	V_{CC}* (V)	CGS2534						Unit
			T_A = +25°C, C_L = 50 pF, R_L = 500Ω			T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω			
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Frequency Maximum	5.0					100		MHz
t_{PLH}	Low-to-High Propagation Delay CK to O_n	5.0			4.0			4.0	ns
t_{PHL}	High-to-Low Propagation Delay CK to O_n	5.0			4.0			4.0	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0			500			500	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		150	500			500	ps
t_{RISE}, t_{FALL}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)				1.5			1.5	ns
t_{HIGH}	Pulse Width Duration High		4			4			ns
t_{LOW}	Pulse Width Duration Low		4			4			
t_{PVLH}	Part-to-Part Variation of Low-to-High Transitions	5.0			750			750	ps
t_{PVHL}	Part-to-Part Variation of High-to-Low Transitions	5.0			750			750	ps

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

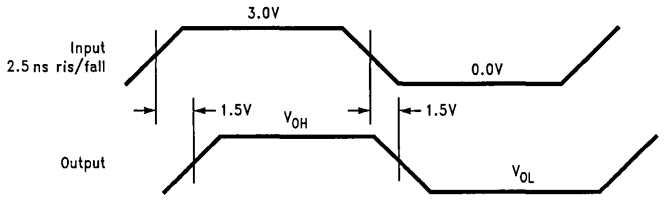
Time high is measured with outputs at 2.0V or above.

Time low is measured with outputs at 0.8V or below.



TL/F/11921–4

Timing information.



TL/F/11921–2

National Semiconductor

PRELIMINARY

CGS2535/36V
Commercial Quad Memory Array Clock Drivers
CGS2535/36TV
Industrial Quad Memory Array Clock Drivers

General Description

These Clock Generation and Support clock drivers are specifically designed for driving memory arrays requiring large fanouts while operating at high speeds.

CGS2535 is a non-inverting 4 to 16 driver with CMOS I/Os. The 2536 option employs the CMOS I/O structure with half of the drivers being inverting and the other half non-inverting while providing divide-by-two banks.

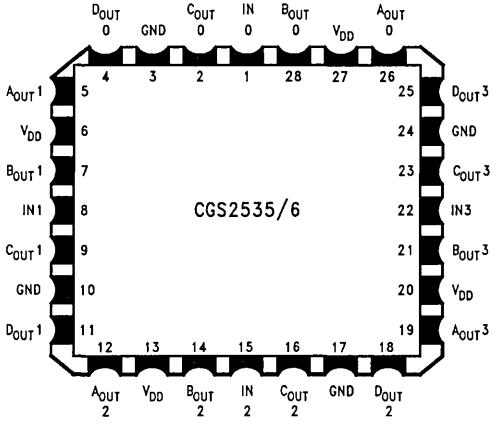
They offer pin-to-pin skew specification that guarantees output skew across a given device.

Features

- Guaranteed and tested:
  — 500 ps pin-to-pin skew (t_{OSHL} and t_{OHLH})
- Implemented on National's ABT family process
- Symmetric output current drive:
  — 24 mA I_{OH}/I_{OL}
- Industrial temperature of −40°C to +85°C
- 28-pin PLCC for optimum skew performance
- 5.5V/3.3V options available
- Symmetric package orientation
- Large fanout for memory driving applications
- Guaranteed 2 kV ESD protection

Connection Diagram

Pin Assignment for 28-Pin PLCC



TL/F/11954-1

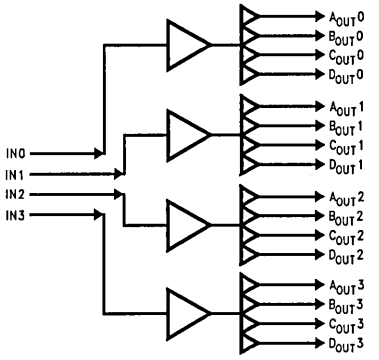
See NS Package Number V28A

Truth Table

Device	Input	Output
CGS2535	In (0–3)	ABCD Out (0–3)
CGS2536	In (0)	ABCD Out (0)
	In (1)	$\overline{ABCD}$ Out (1)
	In (2)	ABCD Out (2) ÷ 2
	In (3)	$\overline{ABCD}$ Out (3) ÷ 2

Logic Diagrams

CGS2535



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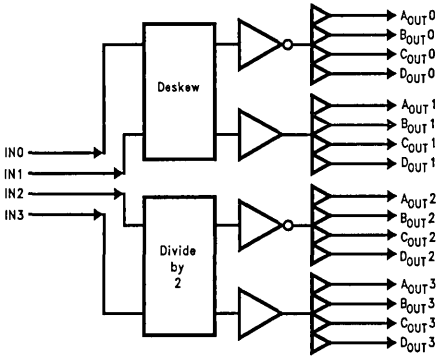
CGS2536



TL/F/11954-3

4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V
Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C

Typical θ_{JA}

Airflow	V Pack
0 LFM	62°C/W
225 LFM	43°C/W
500 LFM	34°C/W
900 LFM	27°C/W

Recommended Operating Conditions

Supply Voltage	
V_{CC}	4.5V to 5.5V
V_{CC}	3.0V to 3.6V
High Level Output Current (I_{OH})	−24 mA
Low Level Output Current (I_{OL})	24 mA
Free Air Operating Temperature	
Industrial	−40°C to + 85°C
Commercial	0°C to + 70°C

Note: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Typ	Max	Units
V_{IH}	Input High Level Voltage		3.3	2.1			V
			4.5	3.15			
			5.5	3.85			
V_{IL}	Input Low Level Voltage		3.3			0.9	V
			4.5			1.35	
			5.5			1.65	
V_{IK}	Input Clamp Voltage	I_I = −18 mA	4.5			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −50 μA	3.3	2.9			V
			4.5	4.4			
			5.5	5.4			
		I_{OH} = −24 mA	3.3	2.46			V
			4.5	3.76			
			5.5	4.76			
V_{OL}	Low Level Output Voltage	I_{OL} = 50 μA	3.3			0.1	V
			4.5			0.1	
			5.5			0.1	
		I_{OL} = 24 mA	3.3			0.44	V
			4.5			0.44	
			5.5			0.44	
I_I	Input Current @ Max Input Voltage	V_{IH} = 7V	5.5	−7		7	μA
		V_{IH} = V_{CC}	3.6	−1		1	μA
I_{IH}	High Level Input Current	V_{IH} = 2.7V	5.5			5	μA
I_{IL}	Low Level Input Current	V_{IL} = 0.4V	5.5	−5			μA
I_{OLD}	Minimum Dynamic Output Current*	V_{OLD} = 1.65V (max)	5.5	75	50		mA
		V_{OLD} = 0.8V (max)	3.6	36			mA
I_{OHD}	Minimum Dynamic Output Current*	V_{OHD} = 3.85V (min)	5.5	−75	−50		mA
		V_{OHD} = 2.0V (min)	3.6	−25			mA
I_{CC}	Supply Current		3.6			25	μA
	'2535/36		5.5			80	
C_{IN}	Input Capacitance		5.0		5		pF

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics (Notes 1, 2, and 3)

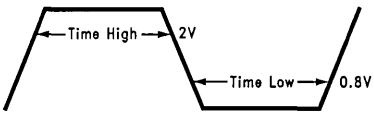
Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter		V_{CC}* (V)	CGS2535/36						Units
				T_A = +25°C, C_L = 50 pF, R_L = 500Ω			T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω			
				Min	Typ	Max	Min	Typ	Max	
f_{max}	Frequency Maximum		3.3 5.5					85		MHz
t_{PLH}	Low to High Propagation Delay CK to On	2535	3.3 5.0			4.5 3.5			4.5 3.5	ns
		2536	3.3 5.0			5.5 4.5			5.5 4.5	
t_{PHL}	High to Low Propagation Delay CK to On	2535	3.3 5.0			4.5 3.5			4.5 3.5	ns
		2536	3.3 5.0			5.5 4.5			5.5 4.5	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	2535	3.3 5.0			500 500			500 500	ps
		2536	3.3 5.0			500 500			500 500	
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	2535	3.3 5.0			500 500			500 500	ps
		2536	3.3 5.0			500 500			500 500	
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)	2535	3.3 5.0			1.5 1.5			1.5 1.5	ns
		2536	3.3 5.0			1.5 1.5			1.5 1.5	
t_{High}	Pulse Width Duration High	2535/6	3.3 5.0	4.0 4.0			4.0 4.0			ns
t_{Low}	Pulse Width Duration Low	2535/6	3.3 5.0	4.0 4.0			4.0 4.0			
t_{PVLH}	Part-to-Part Variation of Low-to-High Transitions	2535	3.3 5.0			1.0 1.0			1.0 1.0	ns
t_{PVHL}	Part-to-Part Variation of High-to-Low Transitions	2535	3.3 5.0			1.0 1.0			1.0 1.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V, 3.3 is 3.3V ±0.3V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Note 2: Time high is measured with outputs which are at 2.0V or above. Time low is measured with outputs which are at 0.8V or below.



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Note 3: The input signal has a rise and fall time transition time of 2.5 ns with high and low values of 3.0V and 0.0V respectively.

National Semiconductor

PRELIMINARY

CGS2537V
Commercial Quad Memory Array Clock Drivers
CGS2537TV
Industrial Quad Memory Array Clock Drivers

General Description

These Clock Generation and Support clock drivers are specifically designed for driving memory arrays requiring large fanouts while operating at high speeds.

CGS2537 is a 4 to 16 inverting driver with TTL compatible I/Os. This device features the same characteristics of CGS2534 with an added series resistor on the output for ease of termination while reducing the undershoot.

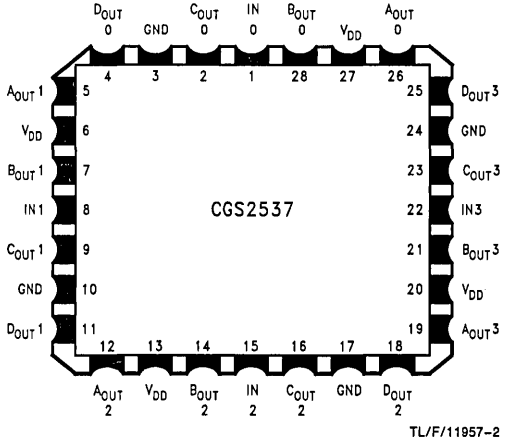
This device has minimum skew specifications of 500 ps pin-to-pin as well as a 1 ns specification for part-to-part propagation delay variation.

Features

- Nominal 8Ω output series resistor
- Guaranteed and tested:
  — 500 ps pin-to-pin skew (T_{OSHL} and T_{OHLH})
- Implemented on National's ABT family process
- Output current drive:
  — −36 mA/+20 mA I_{OH}/I_{OL}
- Industrial temperature of −40°C to +85°C
- 28-pin PLCC for optimum skew performance
- Symmetric package orientation
- Large fanout for memory driving applications
- Guaranteed 2 kV ESD protection

Connection Diagram

Pin Assignment for 28-Pin PLCC

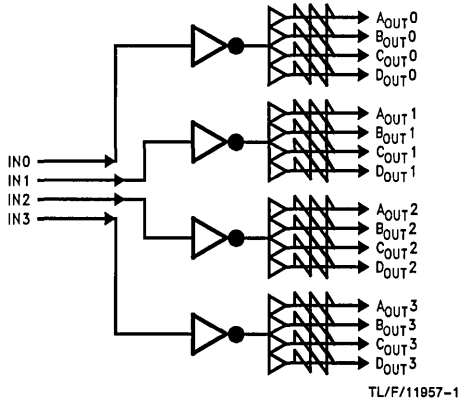


TL/F/11957–2

See NS Package Number V28A

Logic Diagram

CGS2537



TL/F/11957–1

Truth Table

Device	Input	Output
CGS2537	In (0–3)	$\overline{ABCD}$ Out (0–3)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V
Input Voltage (V_I)	7.0V
Storage Temperature Range (T_{stg})	−65°C to +150°C
Typical θ_{JA} Airflow	V Pack
0 LFM	62°C/W
225 LFM	43°C/W
500 LFM	34°C/W
900 LFM	27°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.75V to 5.25V
High Level Input Voltage (V_{IH})	2V
Low Level Input Voltage (V_{IL})	0.8V
High Level Output Current (I_{OH})	−36 mA
Low Level Output Current (I_{OL})	20 mA
Free Air Operating Temperature	
Industrial	−40°C to +85°C
Commercial	0°C to +70°C

Note: The Absolute Maximum Rating are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2.0			V
V_{IK}	Input Clamp Voltage	V_{CC} = 4.75V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −3 mA, V_{CC} = 4.75V	2.4			V
		I_{OH} = −36 mA, V_{CC} = 4.75V	2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 20 mA		0.35	0.5	V
		V_{CC} = 4.75V, I_{OL} = 50 μA		0.1	0.1	
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.25V, V_{IH} = 7V			7	μA
I_{IH}	High Level Input Current	V_{CC} = 5.25V, V_{IH} = 2.7V			5	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.25V, V_{IL} = 0.4V	−5			μA
I_{OS}	Output Drive Current	V_{CC} = 5.25V, V_O = 0V	−100		275	mA
I_{OLD}	Minimum Dynamic Output Current*	V_{CC} = 5.25V, V_{OLD} = 1.65V (max)		50	75	mA
I_{CCT}	Maximum I_{CC}/Input	V_{CC} = 5.25V			3	mA
I_{CC}	Supply Current '2537 (Quiescent)	V_{CC} = 5.25V			80	μA
C_{IN}	Input Capacitance	V_{CC} = 5V		5		pF

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

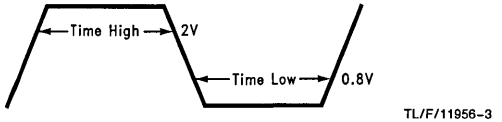
Symbol	Parameter	V_{CC}* (V)	CGS2537						Units
			T_A = +25°C, C_L = 50 pF, R_L = 500Ω			T_A = −40 to +85°C, C_L = 50 pF, R_L = 500Ω			
			Min	Typ	Max	Min	Typ	Max	
f_{max}	Frequency Maximum	5.0					100		MHz
t_{PLH}	Low-to-High Propagation Delay CK to O_n	5.0			4.0			4.0	ns
t_{PHL}	High-to-Low Propagation Delay CK to O_n	5.0			4.5			4.5	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0			500			500	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		150	500			500	ps
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)				1.5			1.5	ns
t_{HIGH}	Pulse Width Duration High		4			4			ns
t_{LOW}	Pulse Width Duration Low		4			4			
t_{PVLH}	Part-to-Part Variation of Low-to-High Transitions	5.0			750			750	ps
t_{PVHL}	Part-to-Part Variation of High-to-Low Transitions	5.0			750			750	ps

*Voltage Range 5.0 is 5.0V ±0.5V

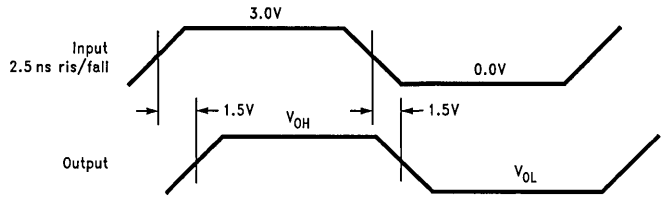
Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Time high is measured with outputs are at 2.0V or above.
Time low is measured with outputs are at 0.8V or below.

Timing Information



TL/F/11956–3



TL/F/11956–4

Memory Array Driving

In order to minimize the total load on the address bus, quite often memory arrays are being driven by buffers while having the inputs of the buffers tied together. Although this practice was feasible in the conventional memory designs, in today's high speed, large buswidth designs which require address fetching at higher speeds, this technique produces many undesired results such as cross-talk and over/undershoot.

CGS2534/35/36/37 Memory Array Drivers were designed specifically to address these application issues on high speed, large memory arrays systems.

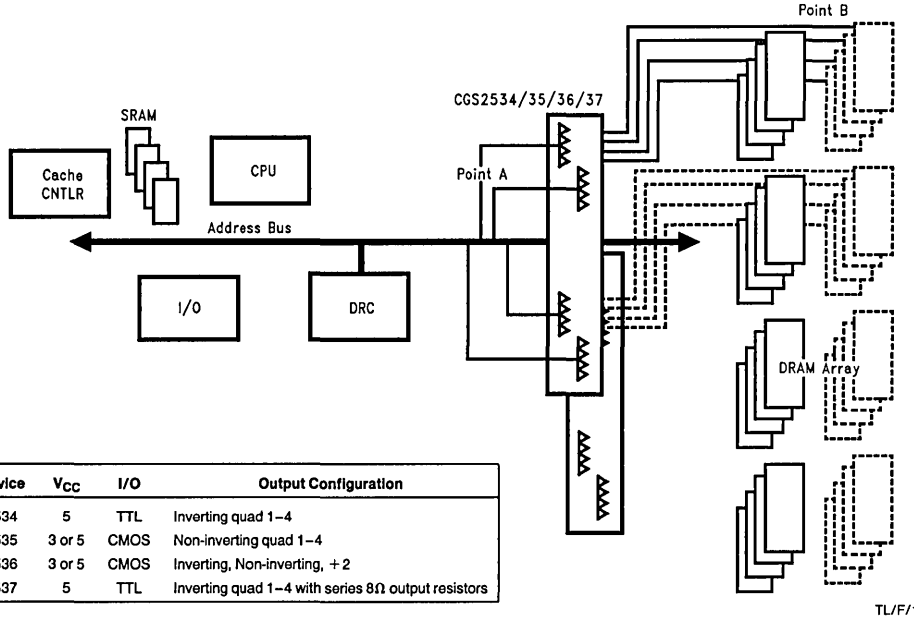
These drivers are optimized to driver large loads, with sub 3 ns propagation delays. These drivers produce less noise while reducing the total capacitive loading on the address bus by having only four inputs tied together (see the diagram below, point A). This helps to minimize the overshoot and undershoot by having only four outputs being switched simultaneously.

Also this larger fan-out helps to save board space since for every one of these MAD drivers, two conventional buffers were typically being used.

Another feature associated with these clock drivers is a 250 ps–500 ps pin-to-pin skew specification. The minimum skew specification allows high speed memory system designers to optimize the performance of their memory subsystem by operating at higher frequencies without having concerns about output-to-output (bank-to-bank) synchronization problem which are associated with driving high capacitive loads (Point B).

The diagram below depicts a "2534/35/36/37" a memory subsystem operating at high speed with large memory capacity. The address bus is common to both the memory and the CPU and I/Os.

These MAD drivers can operate beyond 150 MHz, and are also available in 3V–5V TTL/CMOS versions with symmetric 24 mA I_{OH}/I_{OL} current drive.



Device	V_{CC}	I/O	Output Configuration
2534	5	TTL	Inverting quad 1–4
2535	3 or 5	CMOS	Non-inverting quad 1–4
2536	3 or 5	CMOS	Inverting, Non-inverting, +2
2537	5	TTL	Inverting quad 1–4 with series 8Ω output resistors

TL/F/11957–5

National Semiconductor

100310
Low Skew 2:8 Differential Clock Driver

General Description

The 100310 is a low skew 8-bit differential clock driver which is designed to select between two separate differential clock inputs. The low output to output skew (< 50 ps) is maintained for either clock input. A LOW on the select pin (SEL) selects CLKINA, $\overline{\text{CLKINA}}$ and a HIGH on the SEL pin selects the CLKINB, $\overline{\text{CLKINB}}$ inputs.

The 100310 is ideal for those applications that need the ability to freely select between two clocks, or to maintain the ability to switch to an alternate or backup clock should a problem arise with the primary clock source.

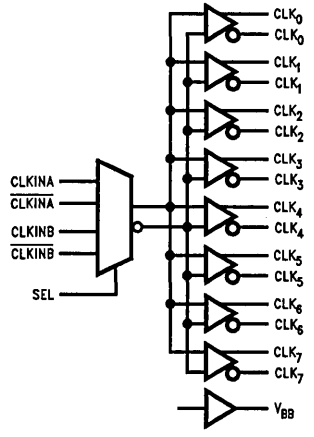
A V_{BB} output is provided for single-ended operation.

Features

- Low output to output skew
- Differential inputs and outputs
- Allows multiplexing between two clock inputs
- Voltage compensated operating range: −4.2V to −5.7V

Ordering Code: See Section 5

Logic Symbol



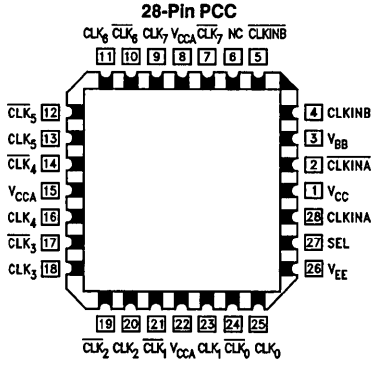
TL/F/10943–1

Pin Names	Description
$CLKIN_n$, $\overline{CLKIN}_n$	Differential Clock Inputs
SEL	Select
CLK_{0-7}, $\overline{CLK}_{0-8}$	Differential Clock Outputs
V_{BB}	V_{BB} Output
NC	No Connect

Truth Table

CLKINA	$\overline{\text{CLKINA}}$	CLKINB	$\overline{\text{CLKINB}}$	SEL	CLK_n	$\overline{CLK}_n$
H	L	X	X	L	H	L
L	H	X	X	L	L	H
X	X	H	L	H	H	L
X	X	L	H	H	L	H

Connection Diagram



TL/F/10943–2

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperture (T_J)	
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −250 μA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Low Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−100		−40	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max Toggle Frequency											
	CLKIN A/B to Q_n	750			750			750			MHz	
	SEL to Q_n	575			575			575			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$ to CLK_n											
	Differential	0.80	0.90	1.00	0.82	0.92	1.02	0.89	1.01	1.09	ns	*Figure 3*
	Single-Ended	0.80	0.96	1.20	0.82	0.98	1.22	0.89	1.06	1.29		
t_{PLH} t_{PHL}	Propagation Delay, SEL to Output	0.75	0.99	1.20	0.80	1.02	1.25	0.85	1.10	1.35	ns	*Figure 2*
t_{PS}	LH-HL Skew		10	30		10	30		10	30	ps	(Notes 1, 4)
t_{OSLH}	Gate-Gate Skew LH		20	30		20	50		20	50		(Notes 2, 4)
t_{OSHL}	Gate-Gate Skew HL		20	50		20	50		20	50		(Notes 2, 4)
t_{OST}	Gate-Gate LH-HL Skew		30	60		30	60		30	60		(Notes 3, 4)
t_S	Setup Time SEL to $CLKIN_n$	300			300			300			ps	
t_H	Setup Time SEL to $CLKIN_n$	0			0			0			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	510	750	275	500	750	275	480	750	ps	*Figure 4*

Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate-to-gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Industrial Version

DC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −250 μA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Low Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	μA	V_{IN} = V_{IH} (Max)	
I_{CBO}	Input Leakage Current	−10		−10		μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−100	−40	−100	−40	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max Toggle Frequency											
	CLKIN A/B to Q_n	750			750			750			MHz	
	SEL to Q_n	575			575			575			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$, to CLK_n											
	Differential	0.78	0.88	0.98	0.82	0.92	1.02	0.89	1.01	1.09	ns	*Figure 3*
	Single-Ended	0.78	0.95	1.18	0.82	0.98	1.22	0.89	1.06	1.29		
t_{PLH} t_{PHL}	Propagation Delay SEL to Output	0.70	0.99	1.20	0.80	1.02	1.25	0.85	1.10	1.35	ns	*Figure 2*
t_{PS}	LH-HL Skew		10	30		10	30		10	30	ps	(Notes 1, 4)
t_{OSLH}	Gate-Gate Skew LH		20	50		20	50		20	50		(Notes 2, 4)
t_{OSHL}	Gate-Gate Skew HL		20	50		20	50		20	50		(Notes 2, 4)
t_{OST}	Gate-Gate LH-HL Skew		30	60		30	60		30	60		(Notes 3, 4)
t_S	Setup Time SEL to $CLKIN_n$	300			300			300			ps	
t_H	Setup Time SEL to $CLKIN_n$	0			0			0			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	510	750	275	500	750	275	480	750	ps	*Figure 4*

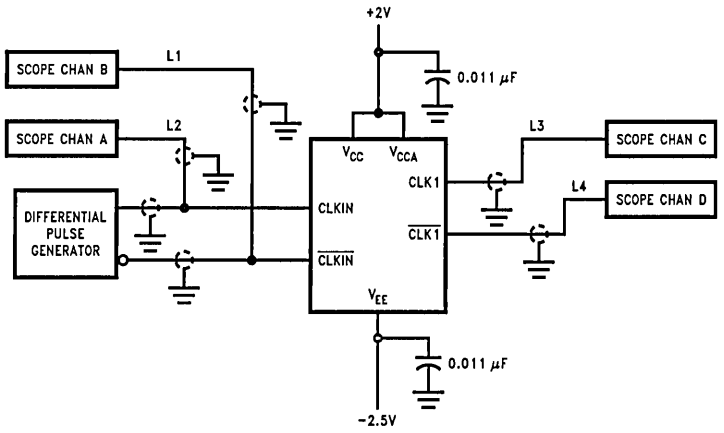
Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate-to-gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Test Circuit



TL/F/10943–3

Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

Note 4: Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit

Switching Waveforms

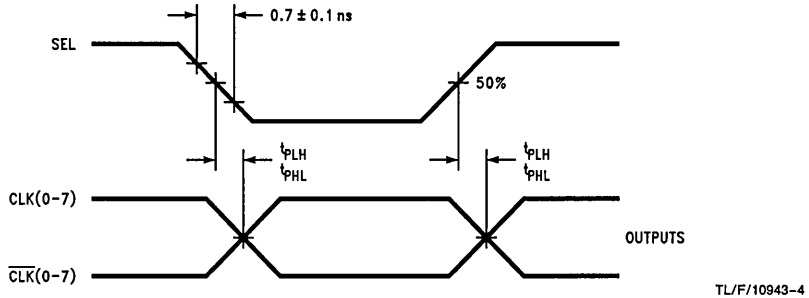


FIGURE 2. Propagation Delay, SEL to Outputs

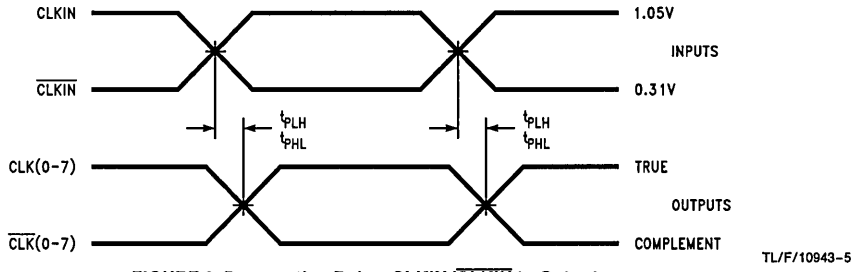


FIGURE 3. Propagation Delay, CLKIN/$\overline{CLKIN}$ to Outputs

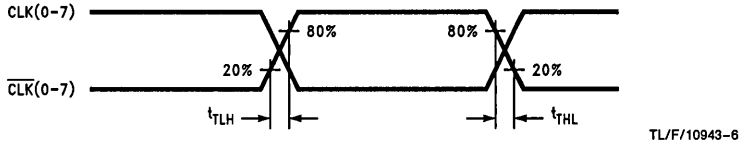


FIGURE 4. Transition Times

National Semiconductor

100311
Low Skew 1:9 Differential Clock Driver

General Description

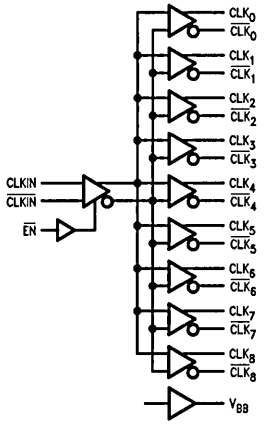
The 100311 contains nine low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input (CLKIN, $\overline{CLKIN}$). If a single-ended input is desired, the V_{BB} output pin may be used to drive the remaining input line. A HIGH on the enable pin ($\overline{EN}$) will force a LOW on all of the CLK_n outputs and a HIGH on all of the $\overline{CLK}_n$ output pins. The 100311 is ideal for distributing a signal throughout a system without worrying about the original signal becoming too corrupted by undesirable delays and skew. The 100311 is pin-for-pin compatible with the Motorola 100E111.

Features

- Low output to output skew
- 2000V ESD protection
- 1:9 low skew clock driver
- Differential inputs and outputs

Ordering Code: See Section 5

Logic Symbol



TL/F/10648–1

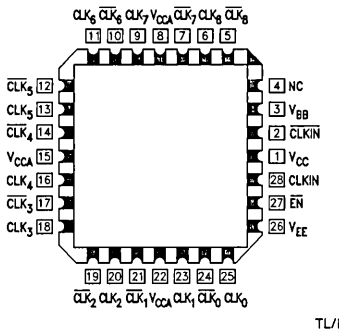
Pin Names	Description
CLKIN, $\overline{CLKIN}$	Differential Clock Inputs
$\overline{EN}$	Enable
CLK_{0-8}, $\overline{CLK}_{0-8}$	Differential Clock Outputs
V_{BB}	V_{BB} Output
NC	No Connect

Truth Table

CLKIN	$\overline{CLKIN}$	$\overline{EN}$	CLK_n	$\overline{CLK}_n$
L	H	L	L	H
H	L	L	H	L
X	X	H	L	H

Connection Diagram

28-Pin PCC



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Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperture (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −300 μA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Low Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$ $\overline{EN}$			 100 250	μA	V_{IN} = V_{IH} (Max)	
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−115		−57	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{max}	Max Toggle Frequency CLKIN to Q_n	750			750			750			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$ to CLK_n											
	Differential	0.75	0.84	0.95	0.75	0.86	0.95	0.84	0.93	1.04	ns	*Figure 3*
	Single-Ended	0.65	0.90	1.05	0.67	0.93	1.17	0.74	1.06	1.24		
t_{PLH} t_{PHL}	Propagation Delay SEL to Output	0.75	1.03	1.20	0.80	1.05	1.25	0.85	1.12	1.35	ns	*Figure 2*
t_{PS}	LH–HL Skew		10	30		10	30		10	30	ps	Notes 1, 4
t_{OSLH}	Gate–Gate Skew LH		20	50		20	50		20	50		Notes 2, 4
t_{OSHL}	Gate–Gate Skew HL		20	50		20	50		20	50		Notes 2, 4
t_{OST}	Gate–Gate LH–HL Skew		30	60		30	60		30	60		Notes 3, 4
t_S	Setup Time EN_n to $CLKIN_n$	250			250			300			ps	
t_H	Hold Time EN_n to $CLKIN_n$	0			0			0			ps	
t_R	Release Time EN_n to $CLKIN_n$	300			300			300			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	500	750	275	480	750	275	460	750	ps	*Figure 4*

Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate-to-gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Note 5: f_{max} = the highest frequency at which output V_{OL}/V_{OH} levels still meet V_{IN} specifications. The F311 will function @ 1 GHz.

Industrial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −300 μA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	

Industrial Version (Continued)

DC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{IL}	Input Low Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)
I_{IH}	Input HIGH Current						V_{IN} = V_{IH} (Max)
	CLKIN, $\overline{CLKIN}$		100		100	μA	
	$\overline{EN}$		250		250		
I_{CBO}	Input Leakage Current	−10		−10		μA	V_{IN} = V_{EE}
I_{EE}	Power Supply Current	−115	−57	−115	−57	mA	Inputs Open
V_{PP}	Minimum Input Swing	150		150		mV	
V_{CMR}	Common Mode Range	V_{CC}−2.0	V_{CC}−0.5	V_{CC}−2.0	V_{CC}−0.5	V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{max}	Max Toggle Frequency CLKIN to Q_n	750			750			750			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$ to CLK_n											
	Differential	0.72	0.81	0.92	0.77	0.86	0.95	0.84	0.93	1.04	ns	*Figure 3*
	Single-Ended	0.62	0.89	1.02	0.67	0.93	1.17	0.74	1.06	1.24		
t_{PLH} t_{PHL}	Propagation Delay SEL to Output	0.70	0.97	1.20	0.80	1.05	1.25	0.85	1.12	1.35	ns	*Figure 2*
t_{PS}	LH−HL Skew		10	30		10	30		10	30	ps	Notes 1, 4
t_{OSLH}	Gate−Gate Skew LH		20	50		20	50		20	50		Notes 2, 4
t_{OSHL}	Gate−Gate Skew HL		20	50		20	50		20	50		Notes 2, 4
t_{OST}	Gate−Gate LH−HL Skew		30	60		30	60		30	60		Notes 3, 4
t_S	Setup Time EN_n to $CLKIN_n$	250			250			300			ps	
t_H	Hold Time EN_n to $CLKIN_n$	0			0			0			ps	
t_R	Release Time EN_n to $CLKIN_n$	300			300			300			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	500	750	275	480	750	275	460	750	ps	*Figure 4*

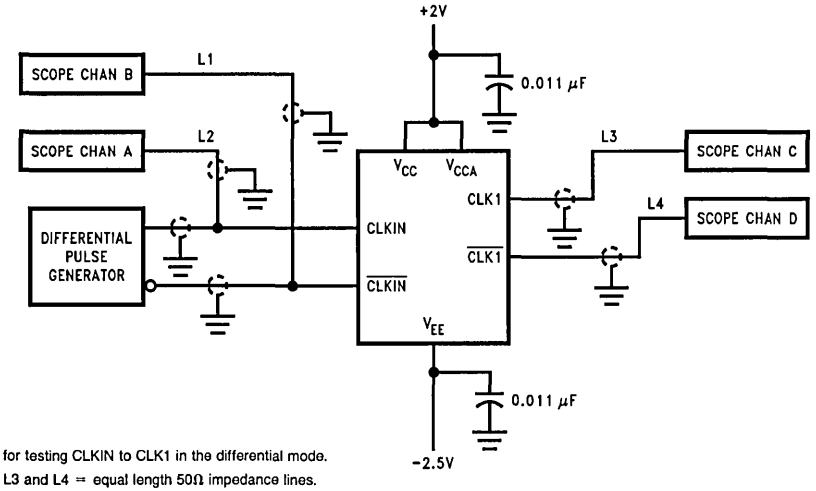
Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Test Circuit



Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

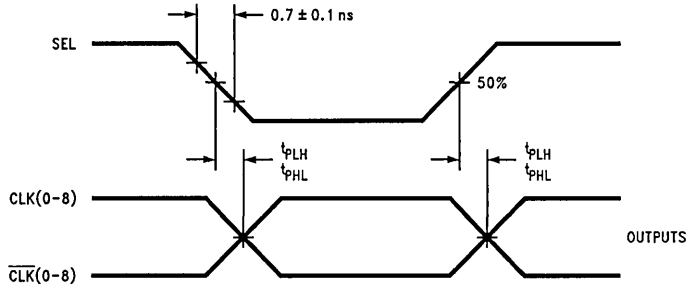
Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤ 3 pF to GND.

Note 4: Scope should have 50Ω input terminator internally.

TL/F/10648-3

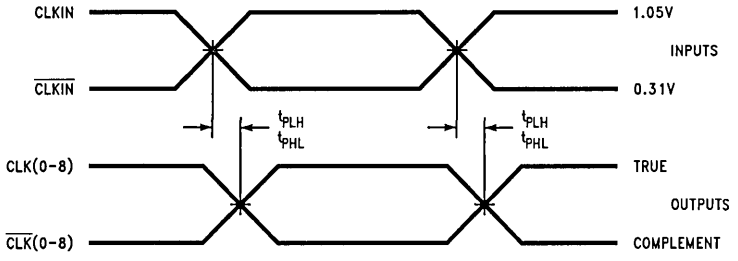
FIGURE 1. AC Test Circuit

Switching Waveforms



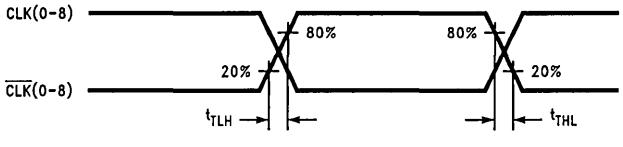
TL/F/10648-4

FIGURE 2. Propagation Delay, $\overline{EN}$ to Outputs



TL/F/10648-5

FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs



TL/F/10648-6

FIGURE 4. Transition Times

National Semiconductor

100315
Low-Skew Quad Clock Driver

General Description

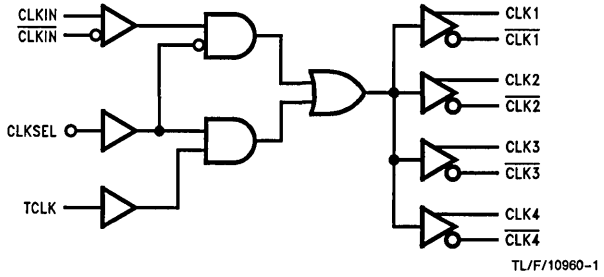
The 100315 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing. The 100315 is a 300 Series redesign of the 100115 clock driver.

Features

- Low output to output skew (≤50 ps)
- Differential inputs and outputs
- Small outline package (SOIC)
- Secondary clock available for system level testing
- 2000V ESD protection
- Voltage compensated operating range: −4.2V to −5.7V
- Military and industrial grades available

Ordering Code: See Section 5

Logic Diagram



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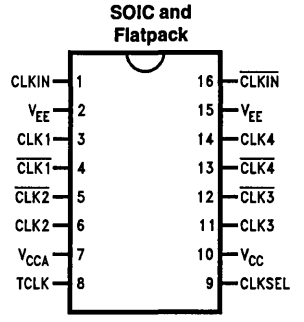
Connection Diagram



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Pin Names	Description
CLKIN, $\overline{\text{CLKIN}}$	Differential Clock Inputs
CLK_{1-4}, $\overline{CLK}_{1-4}$	Differential Clock Outputs
TCLK	Test Clock Input†
CLKSEL	Clock Input Select†

†TCLK and CLKSEL are single-ended inputs, with internal 50 kΩ pulldown resistors.

Truth Table

CLKSEL	CLKIN	$\overline{\text{CLKIN}}$	TCLK	CLK_N	$\overline{CLK}_N$
L	L	H	X	L	H
L	H	L	X	H	L
H	X	X	L	L	H
H	X	X	H	H	L

L = Low Voltage Level
H = High Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Plastic	+150°C
Ceramic	+175°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{CC} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input High Current					V_{IN} = $V_{IH(Max)}$	
	CLKIN, $\overline{CLKIN}$			150	μA		
	TCLK			250	μA		
	CLKSEL			250	μA		
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V	V		
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−67		−35	mA		

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Commercial Version (Continued)

AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	750		750		750		MHz	
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$ Differential Single-Ended	 0.59 0.59	 0.79 0.99	 0.62 0.62	 0.82 1.02	 0.67 0.67	 0.87 1.07	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay, CLKSEL to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.80	1.60	0.80	1.60	0.80	1.60	ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.80	0.30	0.80	0.30	0.80	ns	*Figures 1, 4*
t_{OST} DIFF	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		50		50		50	ps	(Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

DC Electrical Characteristics V_{EE} = −4.2V to −5.7, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{IH}	Single-Ended Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL(Min)}$	

Industrial Version (Continued)

DC Electrical Characteristics V_{EE} = −4.2V to −5.7, V_{CC} = V_{CCA} = GND (Continued)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current						
	CLKIN, $\overline{CLKIN}$		107		107	µA	V_{IN} = $V_{IH\ (Max)}$
	TCLK		300		300	µA	
	CLKSEL		260		260	µA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V		V	
I_{CBO}	Input Leakage Current	−10		−10		µA	V_{IN} = V_{EE}
I_{EE}	Power Supply Current	−70	−30	−70	−30	mA	

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	750		750		750		MHz	
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$								
	Differential	0.59	0.99	0.62	0.82	0.67	0.87	ns	*Figures 1, 3*
	Single-Ended	0.59	0.99	0.62	1.02	0.67	1.07		
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.80	0.30	0.80	0.30	0.80	ns	
t_{OST} DIFF	Maximum Skew Opposite Edge Output-to-Output Variation to Output Path		50		50		50	ps	(Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same package device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Military Version—Preliminary

DC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025		−870	mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830		−1620	mV	0°C to +125°C			
		−1830		−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035			mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085			mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			

Military Version—Preliminary (Continued)

DC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions	Notes
V_{DIFF}	Input Voltage Differential	150			mV	−55°C to +125°C	Required for Full Output Swing	1, 2, 3
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V	−55°C to +125°C		1, 2, 3
V_{IH}	Single-Ended Input High Voltage	−1165		−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Single-Ended Input Low Voltage	−1830		−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$			120	µA	−55°C to +125°C	V_{IN} = $V_{IH(Max)}$	1, 2, 3
	TCLK			350	µA			
	CLKSEL			300	µA			
I_{CBO}	Input Leakage Current	−10			µA	−55°C to +125°C	V_{IN} = V_{EE}	1, 2, 3
I_{EE}	Power Supply Current, Normal	−90		−30	mA	−55°C to +125°C		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.61	0.81	0.61	0.81	0.60	0.83	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns		
$t_{S\,G-G}$	Skew Gate to Gate (Note 5)		100		100		100	ps		4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	0.80	0.30	0.75	0.25	0.75	ns		

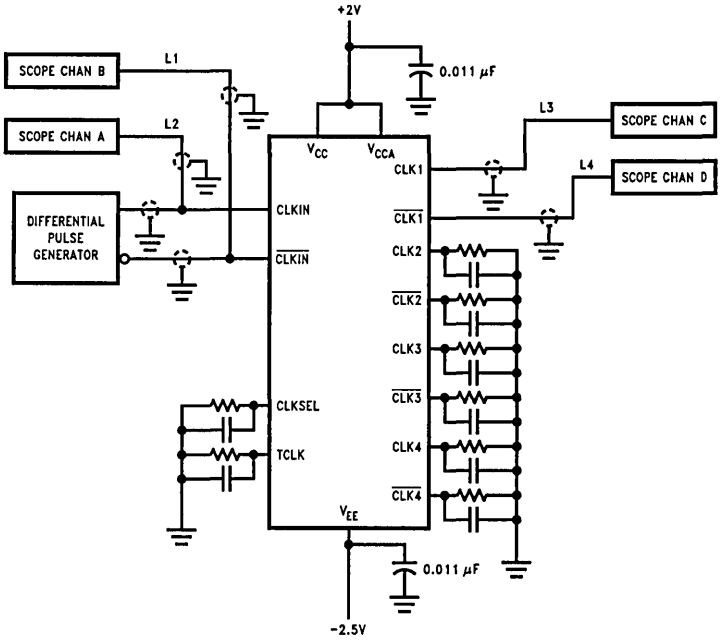
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C, then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Note 5: Maximum output skew for any one device.



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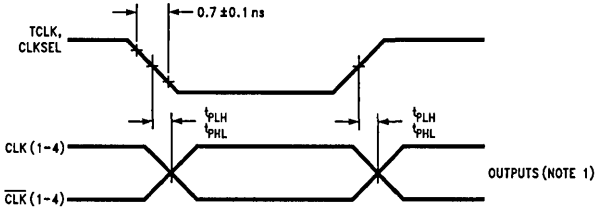
Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

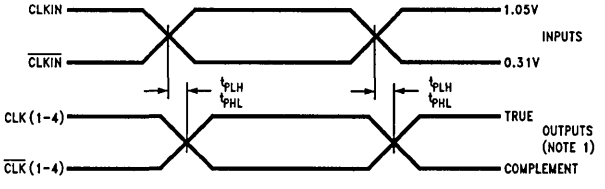
Note 4: Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit



TL/F/10960-4

FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs



TL/F/10960-5

FIGURE 3. Propagation Delay, CLKIN/$\overline{\text{CLKIN}}$ to Outputs

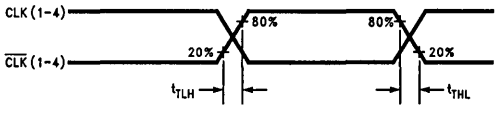


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FIGURE 4. Transition Times

Note 1: The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps.

National Semiconductor

PRELIMINARY

CGS700V
Commercial Low Skew PLL 1 to 9 CMOS Clock Driver

General Description

CGS700 is an off the shelf clock driver specifically designed around the PowerPc™ architecture. It provides low skew outputs which are produced at different frequencies from three fixed input references. The XTALIN input pin is designed to be driven from three distinct crystal oscillators running at 25 MHz, 33 MHz or 40 MHz.

The PLL, using a charge pump and an internal loop filter, multiplies this input frequency to create a maximum output frequency of four times the input.

The device includes a TRI-STATE® control pin to disable the outputs while the PLL is still in lock. This function allows for testing the board without having to wait to acquire the lock once the testing is complete.

Also included, are two EXTSEL and EXTCLK pins to allow testing the chip via an external source. The EXTSEL pin, once set to high, causes the External-Clock_Mux to change its input from the output of the VCO and Counter to the external clock signal provided via EXTCLK input pin. CLK1SEL pin changes the output frequency of the CLK1_0, CLK1_6 outputs. During normal operation, when CLK1SEL pin is high, these outputs are at the same frequency as the input crystal oscillator, while CLK2 and CLK4 outputs are at twice and four times the input frequency respectively.
Once CLK1SEL pin is set to a low logic level, the CLK1 outputs will be at twice the input frequency, the same as the CLK2 output, with CLK4 output still being at four times the input frequency.

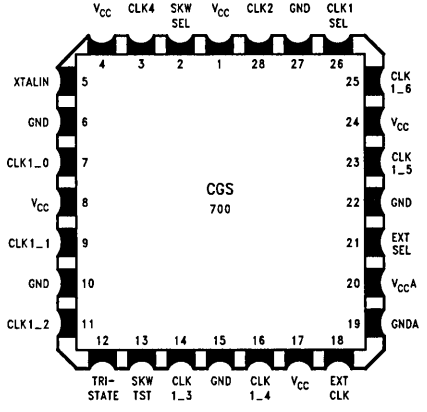
In addition two other pins are added for increasing the test capability. SKWSEL and SKWTST pins allow testing of the counter's output and skew of the output drivers by bypassing the VCO. In this test mode CLK4 frequency is the same as SKWTST input frequency, while CLK2 is ½ and CLK1 frequencies are ¼ respectively (refer to the truth table). In addition CLK1SEL functionality is also true under this test condition

Features

- Guaranteed and tested:
  - 500 ps pin-to-pin skew (t_{OSHL} and t_{OSLH}) on 1X outputs
- Output buffer of nine drivers for large fanout
- 25 MHz–160 MHz output frequency range
- Outputs operating at 4X, 2X, 1X of the reference frequency for multi-frequency bus applications
- Selectable output frequency
- TRI-STATE output control with the PLL is in the lock state
- Internal loop filter to reduce noise and jitter
- Separate analog and digital V_{CC} and Ground pins
- Low frequency test mode by disabling the PLL
- Implemented on National's Core CMOS process
- Symmetric output current drive :
  - +30 mA/−30 mA I_{OL}/I_{OH}
- 28-pin PLCC for optimum skew performance
- Guaranteed 2 kV ESD protection

Connection Diagram

Pin Assignment for PLCC



TL/F/11955–1

See NS Package Number V28A

Pin Description

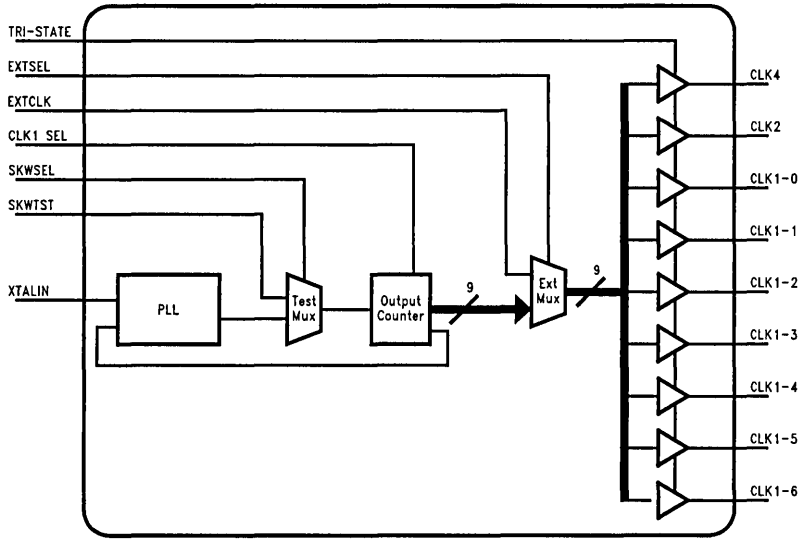
PLCC Package

Pin	Name	Description
1	V_{CC}	Digital V_{CC}
2	SKWSEL	Skew Test Selector Pin
3	CLK4	4X Clock Output
4	V_{CC}	Digital V_{CC}
5	XTALIN	Crystal Oscillator Input
6	GND	Digital Ground
7	CLK1_0	1X Clock Output
8	V_{CC}	Digital V_{CC}
9	CLK1_1	1X Clock Output
10	GND	Digital Ground
11	CLK1_2	1X Clock Output
12	TRI-STATE	Output TRI-STATE Control
13	SKWTST	Skew Testing Pin
14	CLK1_3	1X Clock Output

Pin	Name	Description
15	GND	Digital Ground
16	CLK1_4	1X Clock Output
17	V_{CC}	Digital V_{CC}
18	EXTCLK	External Test Clock
19	GNDA	Analog Ground
20	V_{CC}A	Analog V_{CC}
21	EXTSEL	External Clock Mux Selector
22	GND	Digital Ground
23	CLK1_5	1X Clock Output
24	V_{CC}	Digital V_{CC}
25	CLK1_6	1X Clock Output
26	CLK1SEL	CLK1 Multiplier Selector
27	GND	Digital Ground
28	CLK2	2X Clock Output

Block Diagram

CGS700

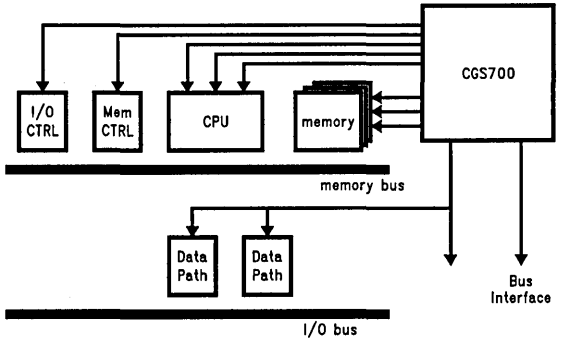


TL/F/11955–2

Truth Table

Input						Output		
CLK1 SEL	EXT SEL	EXT CLK	SKW SEL	SKW TST	TRI-STATE	CLK4	CLK2	CLK1
H	L	X	L	X	H	$4\times f_{IN}$	$2\times f_{IN}$	f_{IN}
L	L	X	L	X	H	$4\times f_{IN}$	$2\times f_{IN}$	$2\times f_{IN}$
X	H	⎍	X	X	H	⎍	⎍	⎍
H	L	X	H	⎍	H	$1\times f_{tst}$	$\frac{1}{2}\times f_{tst}$	$\frac{1}{4}\times f_{tst}$
L	L	X	H	⎍	H	$1\times f_{tst}$	$\frac{1}{2}\times f_{tst}$	$\frac{1}{2}\times f_{tst}$
X	X	X	X	X	L	Z	Z	Z

Typical Application



TL/F/11955–3

CGS700

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage Diode Current (I_{IK})	
V = −0.5V	−20 mA
V = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_O)	
V = −0.5V	−20 mA
V = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±60 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±60 mA
Storage Temperature (T_{stg})	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Static and Dynamic) (Note 2)	1400 mW

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Note 2: Power dissipation is calculated using 49°/W as the thermal coefficient for the PCC package at 225 LFM airflow. The input frequency is assumed @ 33 MHz with CLK4 at 132 MHz and CLK2 and CLK1's being at 66 MHz. In addition the ambient temperature is assumed 70°C.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Input Crystal Frequency	25 MHz to 40 MHz
Operating Temperature (T_A)	0°C to +70°C
External Clock Frequency (EXTCLK Pin)	1 MHz to 10 MHz
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Crystal Input V_{in} from 0.8V to 2.0V	5 ns
All Other Inputs	50 ns

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	V_{CC} (V)	V_{CC} = 4.5V to 5.5V, T_A = 0°C to 70°C			Units
				Min	Typ	Max	
V_{IH}	Minimum Input High Level Voltage		4.5 5.5	2.0 2.0			V
V_{IL}	Maximum Input Low Level Voltage		4.5 5.5			0.8 0.8	V
V_{OH}	Minimum Output High Level Voltage	I_{OUT} = −50 μA	4.5 5.5	4.4 5.4	4.4 5.4		V
		I_{OH} = −30 mA	4.5 5.5	V_{CC} − 0.6 V_{CC} − 0.6			
V_{OL}	Maximum Output High Level Voltage	I_{OUT} = −50 μA	4.5 5.5			0.1 0.1	V
		I_{OL} = 30 mA	4.5 5.5			0.6 0.6	
I_{OH}	High Level Output Current	V_{OH} = V_{CC} − 1.0V	4.5	50	110	170	mA
I_{OL}	Low Level Output Current	V_{OL} = 1.0V	5.5	50	110	170	mA
I_{IN}	Leakage Current	V_{IN} = 0.4V or 4.6V	4.5 5.5	−50		50	μA
C_{IN}	Input Capacitance		4.5 5.5			10	pF
I_{CC}	Quiescent Current (No Load)	V_{IN} = V_{CC}, GND	5.5		15	100	mA
I_{CCT}	I_{CC} per TTL Input	V_{IN} = V_{CC} − 2.1, GND	5.5			2.5	mA

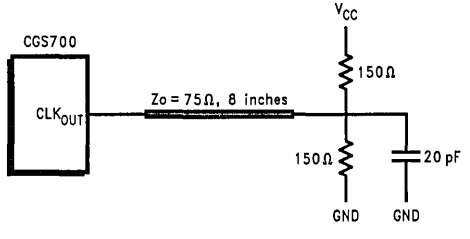
CGS700 (Continued)

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter			V_{CC} = 4.5V to 5.5V T_A = 0°C to 70°C C_L = Circuit 1 R_L = Circuit 1			Units
				Min	Typ	Max	
t_{rise}	Output Rise (Note 1)	CLK4 CLK2 CLK1	0.8V to 2.6V 1.0V to V_{CC} − 1.0V 1.0V to V_{CC} − 1.0V			2.0	ns
t_{fall}	Output Fall (Note 1)	CLK4 CLK2 CLK1	2.6V to 0.8V V_{CC} − 1.0V to 1.0V V_{CC} − 1.0V to 1.0V			2.0	ns
t_{skew}	Maximum Edge- to-Edge Output Skew (Note 2)	+ to + Edges + to + Edges + to + Edges	CLK1 Outputs CLK1 and CLK4 CLK2 and CLK4			500 1000 1000	ps
t_{lock}	Time to Lock the Output to the Synch Input					10.0	ms
t_{cycle}	Output Duty Cycle (Note 3)		CLK1 Outputs CLK2 Output CLK4 Output	40 40 30		60 60 70	%
Jitter	Output Jitter (Note 4)					0.4	ns

Circuit 1. Test Circuit



TL/F/11955–4

Note 1: t_{rise} and t_{fall} are measured at the pin of the device.

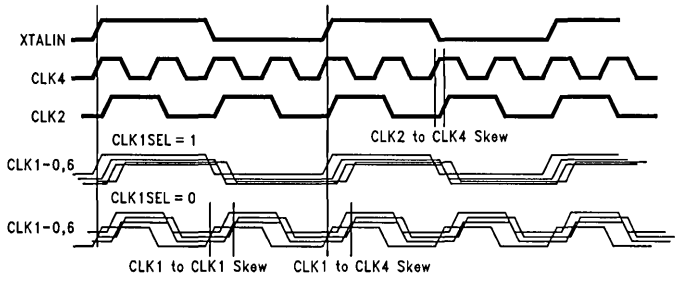
Note 2: Skew is measured at 50% of V_{CC}.

Note 3: Output duty cycle is measured at $V_{DD}/2$.

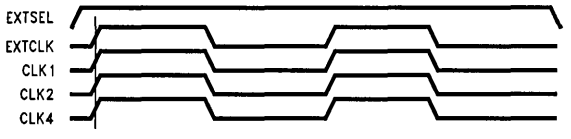
Note 4: Jitter parameter is characterized and is guaranteed by design only. It measures the uncertainty of either the positive or the negative edge compared to its previous cycle. It is also measured at output levels of $V_{CC}/2$. Refer to *Figure 2* for further explanation.

Note 5: The GNDA pins of the 700 must be as free of noise as possible for minimum jitter. Separate analog ground plane is recommended for the PCB. Also the $V_{CC}A$ pin requires extra filtering to further reduce noise. Ferrite beads for filtering and bypass capacitors are suggested for $V_{CC}A$ pin.

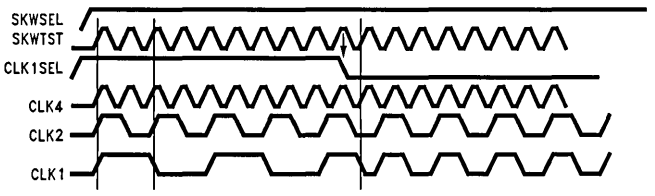
CGS700 (Continued)



TL/F/11955–5

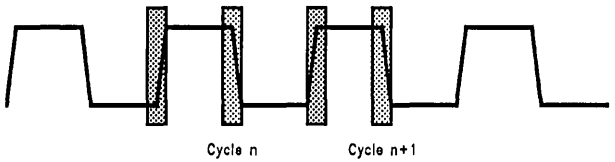


TL/F/11955–6



TL/F/11955–7

FIGURE 1. Waveforms



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P(n) − P(n+1) = ±250 ps for either the rising or falling edge.

FIGURE 2. Jitter

National Semiconductor

PRELIMINARY

CGS701V Commercial/CGS701TV Industrial Low Skew PLL 1 to 8 CMOS Clock Driver

General Description

CGS701 is an off the shelf clock driver specifically designed for today's high speed designs. It provides low skew outputs which are produced at different frequencies from three fixed input references. The XTALIN input pin is designed to be driven from a 15 MHz–50 MHz crystal oscillator.

The PLL, using a charge pump and an internal loop filter, multiplies this input frequency to create a maximum output frequency of four times the input.

The device includes a TRI-STATE® control pin to disable the outputs. This feature allows for low frequency functional testing and debugging.

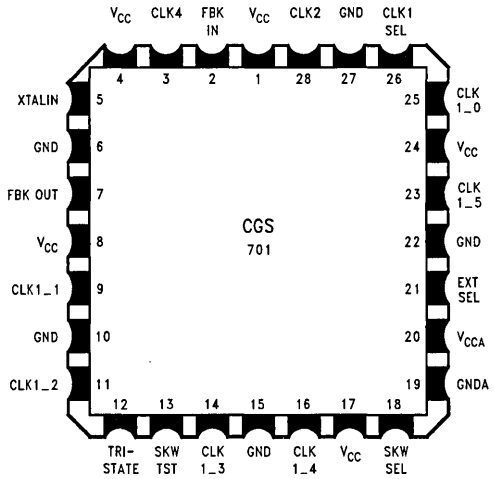
Also included, is an EXTSEL pin to allow testing the chip via an external source. The EXTSEL pin, once set to high, causes the External-Clock_MUX to change its input from the output of the VCO and Counter to the external clock signal provided via SKWTST input pin. (continued)

Features

- Guaranteed and tested:
  500 ps pin-to-pin skew (t_{OSHL} and t_{OSLH}) on 1X outputs. ±500 ps propagation delay
- Output buffer of eight drivers for large fanout
- 25 MHz–160 MHz output frequency range
- Outputs operating at 4X, 2X, 1X of the reference frequency for multifrequency bus applications
- Selectable output frequency
- Internal loop filter to reduce noise and jitter
- Separate analog and digital V_{CC} and ground pins
- Low frequency test mode by disabling the PLL
- Implemented on National's Core CMOS process
- Symmetric output current drive: +30/−30 mA I_{OL}/I_{OH}
- Industrial temperature of −40°C to +85°C
- 28-pin PCC for optimum skew performance
- Guaranteed 2 kV ESD protection

Connection Diagram

Pin Assignment for PLCC



TL/F/11920–1

See NS Package Number V28A

Pin Description

PLCC Package

Pin	Name	Description
1	V_{CC}	Digital V_{CC}
2	FBK IN	Feedback Input Pin
3	CLK4	4X Clock Output
4	V_{CC}	Digital V_{CC}
5	XTALIN	Crystal Oscillator Input
6	GND	Digital Ground
7	FBK OUT	Feedback Output Pin
8	V_{CC}	Digital V_{CC}
9	CLK1_I	1X Clock Output
10	GND	Digital Ground
11	CLK1_2	1X Clock Output
12	TRI-STATE	Output TRI-STATE Control
13	SKWTST	Skew Testing Pin
14	CLK1_3	1X Clock Output
15	GND	Digital Ground
16	CLK1_4	1X Clock Output
17	V_{CC}	Digital V_{CC}
18	SKWSEL	Skew Test Selector Pin
19	GNDA	Analog Ground
20	V_{CCA}	Analog V_{CC}
21	EXTSEL	External Clock MUX Selector
22	GND	Digital Ground
23	CLK1_5	1X Clock Output
24	V_{CC}	Digital V_{CC}
25	CLK1_0	1X Clock Output
26	CLK1SEL	CLK1 Multiplier Selector
27	GND	Digital Ground
28	CLK2	2X Clock Output

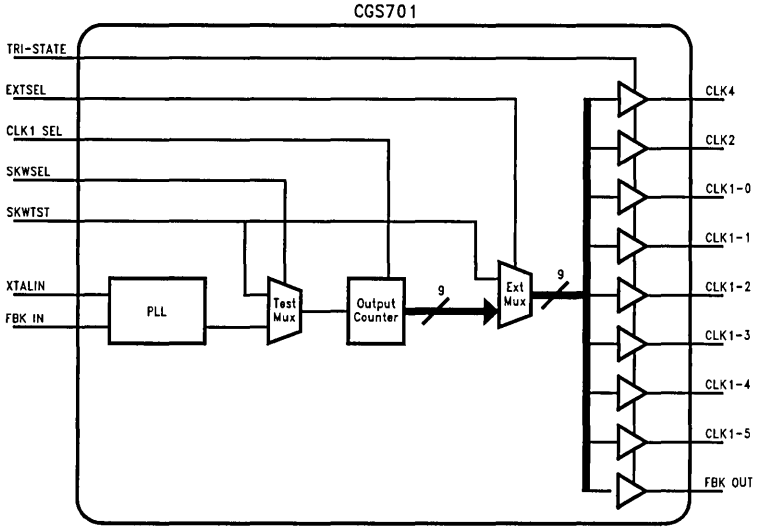
General Description (Continued)

CLK1SEL pin changes the output frequency of the CLK1_0 thru CLK1_5 outputs. During normal operation, when CLK1SEL pin is high, these outputs are at the same frequency as the input crystal oscillator, while CLK2 and CLK4 outputs are at twice and four times the input frequency respectively.

Once CLK1SEL pin is set to a low logic level, the CLK1 outputs will be at twice the input frequency, the same as the CLK2 output, with CLK4 output still being at four times the input frequency.

In addition, another pin is added for increasing the test capability. SKWSEL pin allows testing of the counter's output and skew of the output drivers by bypassing the VCO. In this test mode CLK4 frequency is the same as SKWTST input frequency, while CLK2 is 1/2 and CLK1 frequencies are 1/4 respectively (refer to the Truth Table). In addition CLK1SEL functionality is also true under this test condition.

Block Diagram

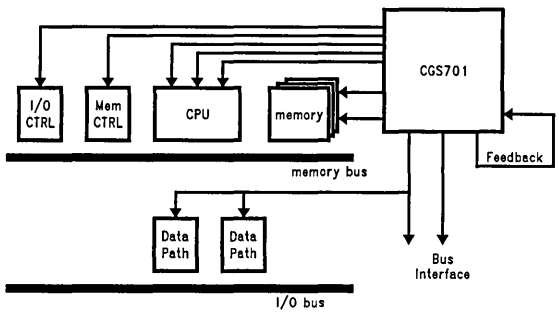


TL/F/11920–2

Truth Table

Input					Output		
CLK1 SEL	EXT SEL	SKW SEL	SKW TST	TRI-STATE	CLK4	CLK2	CLK1
H	L	L	X	H	4 x f in	2 x f in	f in
L	L	L	X	H	4 x f in	2 x f in	2 x f in
X	H	X	⎍	H	⎍	⎍	⎍
H	L	H	⎍	H	1 x f tst	½ x f tst	¼ x f tst
L	L	H	⎍	H	1 x f tst	½ x f tst	½ x f tst
X	X	X	X	L	Z	Z	Z

Typical Application



TL/F/11920–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage Diode Current (I_{IK})	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_O)	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±60 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±60 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Static and Dynamic) (Note 2)	1400 mW

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Input Crystal Frequency	25 MHz–40 MHz
Operating Temperature	
Commercial	0°C to +70°C
Industrial	−40°C to +85°C
External Clock Frequency (EXTCLK Pin)	1 MHz–10 MHz
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Crystal Input V_{IN} from 0.8V to 2.0V	5 ns
All Other Inputs	50 ns

Note 1: The Absolute MAximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Note 2: Power dissipation is calculated using 49°C/W as the thermal coefficient for the PCC package at 225 LFM airflow. The input frequency is assumed at 33 MHz with CLK4 at 132 MHz and CLK2 and CLK1 being at 66 MHz. In addition, the ambient temperature is assumed 70°C.

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	V_{CC}	V_{CC} = 4.5V–5.5V, T = 0°C to 70°C			Units	Conditions
			Min	Typ	Max		
V_{IH}	Minimum Input High Level Voltage	4.5 5.5	2.0 2.0			V	
V_{IL}	Maximum Input Low Level Voltage	4.5 5.5			0.8 0.8	V	
V_{OH}	Minimum Output High Level Voltage	4.5 5.5	4.4 5.4	4.4 5.4		V	I_{OUT} = −50 μA I_{OH} = −30 mA
		4.5 5.5	V_{CC} − 0.6 V_{CC} − 0.6				
V_{OL}	Maximum Output High Level Voltage	4.5 5.5			0.1 0.1	V	I_{OUT} = −50 μA I_{OL} = 30 mA
		4.5 5.5			0.6 0.6		
I_{OH}	High Level Output Current	4.5	50	110	170	mA	$V_{OH} = V_{CC} - 1.0V$
I_{OL}	Low Level Output Current	5.5	50	110	170	mA	V_{OL} = 1.0V
I_{IN}	Leakage Current	4.5 5.5	−50		50.0	μA	V_{IN} = 0.4V or 4.6V
C_{IN}	Input Capacitance	4.5 5.5			10.0	pF	
I_{CC}	Quiescent Current (No Load)	5.5		0.02	0.2	mA	$V_{IN} = V_{CC}$, GND $V_{IN} = V_{CC} - 2.1$, GND
I_{CCT}	I_{CC} per TTL Input	5.5			2.5		

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter				Conditions	V_{CC} = 4.5V–5.5V T = 0°C to +70°C C_L = Circuit 1 R_L = Circuit 1			Units
						Min	Typ	Max	
t_{rise}	Output Rise	CLK4 CLK2 CLK1 All	0.8V to 2.6V 1.0V to V_{CC} − 1.0V 1.0V to V_{CC} − 1.0V 0.8V to 2.0V		(Note 1)			 2.0 1.5	ns
t_{fall}	Output Fall	CLK4 CLK2 CLK1 All	2.6V to 0.8V V_{CC} − 1.0V to 1.0V V_{CC} − 1.0V to 1.0V 0.8V to 2.0V		(Note 1)			 2.0 1.5	ns
t_{SKEW}	Maximum Edge-to-Edge Output Skew		+ to + Edges + to + Edges + to + Edges	CLK1 Outputs CLK1 and CLK4 CLK2 and CLK4	(Note 2)			500 500 500	ps
t_{LOCK}	Time to Lock the Output to the Synch Input							10.0	ms
t_{CYCLE}	Output Duty Cycle			CLK1 Outputs CLK2 Output CLK4 Output	(Note 3)	40 40 30		60 60 70	%
Jitter	Output Jitter				(Note 4)			0.4	ns
t_{PD}	Propogation Delay from XTALIN to FBKOUT				(Notes 6, 2, 4, 5)	−0.5		+0.5	ns

Note 1: t_{rise} and t_{fall} parameters are measured at the pin of the device.

Note 2: Skew is measured at 50% of V_{CC}.

Note 3: Output duty cycle is measured at $V_{DD}/2$.

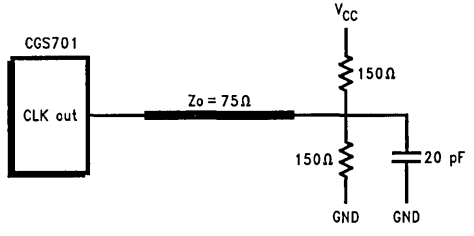
Note 4: Jitter parameter is characterized and is guaranteed by design only. It measures the uncertainty of either the positive or the negative edge compared to its previous cycle. It is also measured at output levels of $V_{CC}/2$. Refer to *Figure 2* for further explanation.

Note 5: Measured from the ref. input to any output pin. The length of the feedback and XTALIN traces will impact this delay time.

Note 6: This parameter includes pin-to-pin skew, cycle to cycle jitter, part-to-part variation as well as propagation delay thru the device.

Note 7: The GNDA pins of the 701 must be as free of noise as possible for minimum jitter. Separate analog ground plane is recommended for the PCB. Also the V_{CCA} pin requires extra filtering to further reduce noise. Ferrite beads for filtering and bypass capacitors are suggested for the V_{CCA} pin.

Circuit 1. Test Circuit



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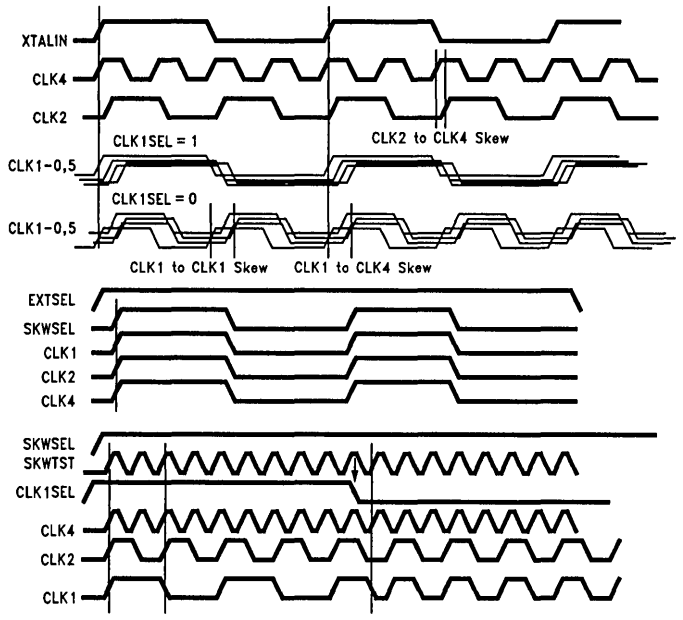
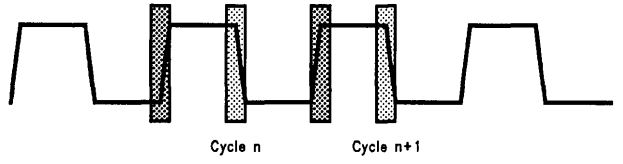
AC Electrical Characteristics (Continued)



TL/F/11920–5

FIGURE 1. Waveforms



TL/F/11920–6

P(n) − P(n+1) = ±250 ps for either the rising or falling edge.

FIGURE 2. Jitter

National Semiconductor

PRELIMINARY

CGS64/74C800/801/802, CGS64/74CT800/801/802, CGS/74LCT800/801/802
Low Skew PLL 1-to-8 CMOS Clock Driver

General Description

These minimum skew clock drivers are designed for Clock Generation and Support (CGS) applications operating at high frequencies utilizing a phase lock loop. The phase lock loop allows for outputs to lock-on to either Synch_0 or Synch_1 inputs, which could be operating at different frequencies. This product is ideal for applications requiring clock synchronization and distribution of either on or off board components.

The PLL uses a counter and a digital to analog convertor for its charge pump and the loop filter and does NOT require any external components for the loop filter. This along with separate analog and digital power rails, helps to minimize the overall sensitivity of the part to noise. The VCO is optimized to operate from 10 MHz up to twice the operating frequency of the 2X output.

The eight outputs, O0–O7, are provided for large fanout applications requiring different phase/frequency clocks. The output buffer of the 800 option includes 5 drivers (O0–O4) with 500 ps skew across either rising or falling edges running at the same frequency as the input. Also included on the 800 option are, O5 which is 180 degrees out of phase output, O6 which is running at twice the input frequency, and O7 an in-phase divide-by-two clock output.

The 801 option has all the output (O0–O7) operating at the same frequency as the input (half the VCO frequency) with a skew of no more than 500 ps.

The 802 option's output buffer consists of two drivers running at twice the input frequency, two drivers at the same frequency, and two drivers at half the input frequency. The last two drivers are operating at 1/4 and 3/2 of the reference frequency (refer to the block diagram).

The Synch_0 and Synch_1 inputs are provided as two different sources for the input reference frequency and can be selected by the REF_SEL pin. These two inputs also can be used for any fault tolerant conditions by being at the same frequency.

The Feedback pin can be used for synchronizing the drivers to any selected output, or for synchronizing the drivers to any external signal.

Also provided is a reset circuitry to actively force the outputs to a low state. This is achieved by the RST pin (active low) which forces all the outputs to low.

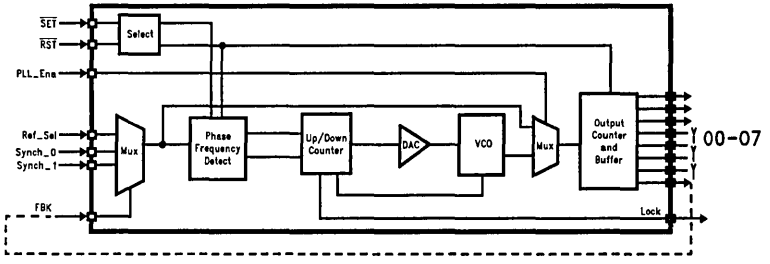
Another available feature is low frequency testing, which can be accomplished by disabling and by-passing the phase lock loop using the PLL_ENA pin. This pin causes the Synch_0 input to control the output counter.

A lock detect circuitry is also provided to determine the lock condition. This pin (LOCK) will remain low until the outputs and Synch inputs are synchronized with the feedback signal. This pin can be used for wait or any interrupt states when the loops steady state phase or frequency lock is lost.

Features

- Guaranteed and tested:
  - 500 ps pin-to-pin skew (T_{OSHL} and T_{OSLH}) on 1X outputs
- Available in 3.3V and 5V options
- Output buffer of eight drivers for large fanout
- 10 MHz to 130 MHz output frequency
- NO LOOP FILTER COMPONENTS required for the PLL
- Motorola's PC88915 functional compatible (800 option)
- Outputs operating at 2X, 1X, 1X (bar), X/2, 3X/2, X/4 of the reference frequency for multi-frequency bus applications
- Two selectable glitch free reference clock available for test or fault tolerant conditions
- Open collector lock pin to enable cascading PLLs by wire-ORing them together
- Low frequency test mode by disabling the PLL
- Phase and frequency lock detect for power-up or interrupt and wait states
- Improved noise sensitivity and jitter performance
- Open drain lock indicator for ease of cascading
- Implemented on National's BCT 1.0 process
- Symmetric output current drive: +24/−24 mA I_{OH}/I_{OL}
- Industrial temperature of −40C to +85C
- 28-pin PCC for optimum skew performance
- Guaranteed 2 kV ESD protection

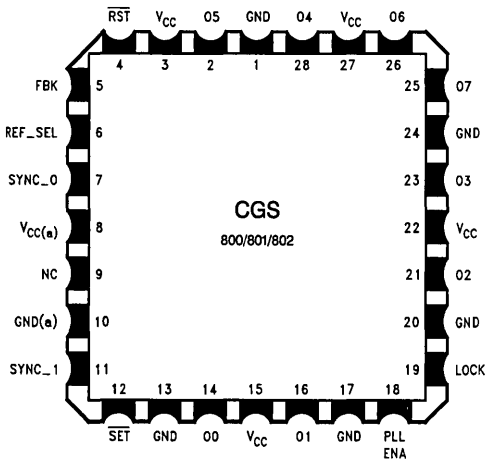
Block Diagram



TL/F/11817–2

Connection Diagram

Pin Assignment for PLCC



TL/F/11817–1

CGS800 Options Output Buffer

Pin Outputs	800	801	802
(14) O0	1X	1X	1X
(16) O1	1X	1X	1X
(21) O2	1X	1X	1X
(23) O3	1X	1X	1X
(28) O4	1X	1X	1/2X
(2) O5	1X (Bar)	1X	1/2X
(26) O6	2X	1X	1/4X
(25) O7	1/2X	1X	3/2X

Truth Table

Input						Output	
PLL ENA	REF SEL	S_0	S_1	SET	RESET	O	LOCK
L	X	X	X	L	L	L	L
L	X	X	X	L	H	L	L
L	X	X	X	H	L	L	L
L	L	⎍	X	H	H	⎍	H*
L	H	X	⎍	H	H	⎍	H*
H	L	⎍	X	H	H	⎍	L
H	H	X	⎍	H	H	⎍	L

*Phase, Frequency Locked State.

Pin Description PLCC Package

Pin	Name	Desciption
1	GND	Digital Ground
2	Output 5	Output
3	V_{CC}	Digital V_{CC}
4	Reset	Reset Active Low (Asynchronous)
5	Feedback	PLL Feed Back Path
6	Input Select	Reference Input Clock Select
7	Input 0	Clock 0 Input
8	Analog V_{CC}	Analog V_{CC}
9	N/C	No Connect
10	GND	Digital Ground
11	Input 1	Clock 1 Input
12	Set	Set Active Low (Asynchronous)
13	Analog GND	Analog Ground
14	Output 0	Output
15	V_{CC}	V_{CC}
16	Output 1	Output
17	GND	Ground
18	PLL Enable	PLL Enable for Test
19	LOCK	Lock
20	GND	Ground
21	Output 2	Output
22	V_{CC}	V_{CC}
23	Output 3	Output
24	GND	Ground
25	Output 7	Output
26	Output 6	Output
27	V_{CC}	V_{CC}
28	Output 4	Output

CGS64/74CT, C800/800/801/802 Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage Diode Current (I_{IK})	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_O)	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +125°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Ind.	−40°C to +85°C
Comm.	0°C to +70°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter		Conditions	V_{CC}	V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C			Units
					Min	Typ	Max	
V_{IH}	Minimum Input High Level Voltage	C800/801/802	V_{OUT} = 0.1V or V_{OUT} = V_{CC} − 0.1V	4.5 5.5	2.1 3.85	1.5 2.75		V
		CT800/801/802		4.5 5.5	2.0 2.0			
V_{IL}	Maximum Input Low Level Voltage	C800/801/802	V_{OUT} = 0.1V or V_{OUT} = V_{CC} − 0.1V	4.5 5.5		1.5 2.75	0.9 1.65	V
		CT800/801/802		4.5 5.5			0.8 0.8	
V_{OH}	Minimum Output High Level Voltage	C800/801/802	I_{OUT} = −50 μA	4.5 5.5	4.4 5.4	4.4 5.4		V
		CT800/801/802		4.5 5.5	4.4 5.4	4.4 5.4		
		C800/801/802	I_{OH} = −24 mA	4.5 5.5	3.7 4.7	3.76 4.76		V
		CT800/801/802		4.5 5.5	3.7 4.7	3.76 4.76		
V_{OL}	Maximum Output Low Level Voltage	C800/801/802	I_{OUT} = −50 μA	4.5 5.5		0.1 0.1	0.1 0.1	V
		CT800/801/802		4.5 5.5		0.1 0.1	0.1 0.1	
		C800/801/802	I_{OL} = 24 mA	4.5 5.5		0.1 0.1	0.44 0.44	V
		CT800/801/802		4.5 5.5		0.1 0.1	0.44 0.44	
I_{IN}	Leakage Current		CT800/801/802 C800/801/802	V_{IN} = V_{CC}, GND	5.5	−1.0		+0.1	μA
I_{CC}	Maximum Supply Current	Analog	CT800/801/802 C800/801/802	V_{IN} = V_{CC}, GND	5.5			50.0 50.0	mA
		Digital	CT800/801/802 C800/801/802		5.5			1.0 1.5	

CGS74LCT, 800/801/802

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage Diode Current (I_{IK})	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_O)	
$V = -0.5V$	−50 mA
$V = V_{CC} + 0.5V$	+50 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +125°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0 to V_{CC}
Operating Temperature (T_A)	−0°C to +70°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V, 3.6V	125 mV/ns

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter		Conditions	V_{CC}	V_{CC} = 3.3V to 3.6V T_A = 0°C to +70°C			Units
					Min	Typ	Max	
V_{IH}	Minimum Input High Level Voltage	LCT800/801/802	V_{OUT} = 0.1V or V_{OUT} = V_{CC} − 0.1V	3.3	2.0			V
V_{IL}	Maximum Input Low Level Voltage	LCT800/801/802	V_{OUT} = 0.1V or V_{OUT} = V_{CC} − 0.1V	3.3			0.8	V
V_{OH}	Minimum Output High Level Voltage	LCT800/801/802	I_{OUT} = −50 μA	3.3	V_{CC} −0.2			V
		LCT800/801/802	I_{OH} = −24 mA	3.3	2.4			V
V_{OL}	Maximum Output Low Level Voltage	LCT800/801/802	I_{OUT} = −50 μA	3.3			0.2	V
		LCT800/801/802	I_{OL} = 24 mA	3.3			0.5	V
I_{IN}	Leakage Current	LCT800/801/802	V_{IN} = V_{CC}, GND	3.6	−1.0		+0.1	μA
I_{CC}	Maximum Supply Current — Analog	LCT800/801/802	V_{IN} = V_{CC}, GND	3.6			50.0 50.0	mA
	Maximum Supply Current — Digital	LCT800/801/802		3.6			1.0 1.5	mA

CGS64/74CT, C800/801/802

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter			V_{CC} = 4.5V to 5.5V T_A = −40°C to +85°C C_L = 50 pF R_L = 500Ω			Units	Notes
				Min	Typ	Max		
t_r	Output Rise	0.8V to 2.0V				1.5	ns	
		0.2 V_{CC} to 0.8 V_{CC}				2.5		
t_f	Output Fall	0.8V to 2.0V				1.5	ns	
		0.2 V_{CC} to 0.8 V_{CC}				2.5		
t_{SKEW}	Maximum Edge-to-Edge Output Skew	+ to + edges − to − edges + to − edges	CGS800			500 500 750	ps	(Note 1)
		All edges	CGS801			500	ps	(Note 2)
		+ to + edges − to − edges + to − edges	CGS802			500 500 750	ps	(Note 3)
$t_{PULSE\ WIDTH}$	Output Pulse Width from Synch_0 or Synch_1 in Test Mode			Period/2 ±0.5		Period/2 ±0.5	ns	
$t_{PROP-DELAY}$	Synch to Feedback Delay Master Set/Reset to Q Master Set to Lock Master Reset to Lock PLL Enable to Lock Synch Loss to Lock			 8 Cycles		0.5 8.0 TBD TBD 5.0 16 Cycles + 10 ns	ns	(Note 4)
t_{LOCK}	Time to Lock the Output to the Synch Input					10.0	ms	(Note 5)
$t_{RECOVERY}$	Reset Recovery to Synch_0/1			9.0			ns	(Note 6)
t_{WIDTH}	Set/Reset Input Pulse Width Synch_0/1 Minimum Pulse Width			5.0 3.0			ns	(Note 7)
t_{CYCLE}	Input Duty Cycle			25%		75%	ns	(Note 8)
f_{max}	Output Operating Frequency			10.0		130.0	MHz	(Note 9)
Jitter	Output Jitter					500	ps	(Note 10)
C_{IN}	Input Capacitance				5.0		pF	
C_{PD}	Power Dissipation Capacitance				50.0		pF	

CGS74LCT800/801/802

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter			V_{CC} = 3.0V to 3.6V T_A = −40°C to +85°C C_L = 50 pF R_L = 500Ω			Units	Notes
				Min	Typ	Max		
t_r	Output Rise	0.8V to 2.0V				1.5	ns	
		0.2 V_{CC} to 0.8 V_{CC}				2.5		
t_f	Output Fall	0.8V to 2.0V				1.5	ns	
		0.2 V_{CC} to 0.8 V_{CC}				2.5		
t_{SKEW}	Maximum Edge-to-Edge Output Skew	+ to + edges − to − edges + to − edges	CGS800			500–750 500–750 750	ps	(Note 1)
		All edges	CGS801			500–750	ps	(Note 2)
		+ to + edges − to − edges + to − edges	CGS802			500–750 500–750 750	ps	(Note 3)
$t_{PULSE\ WIDTH}$	Output Pulse Width from Synch_0 or Synch_1 in Test Mode			Period/2 ±0.5		Period/2 ±0.5	ns	
$t_{PROP-DELAY}$	Synch to Feedback Delay Master Set/Reset to Q Master Set to Lock Master Reset to Lock PLL Enable to Lock Synch Loss to Lock			 8 Cycles		0.5 8.0 TBD 5.0 16 Cycles + 10 ns	ns	(Note 4)
t_{LOCK}	Time to Lock the Output to the Synch Input					10.0	ms	(Note 5)
$t_{RECOVERY}$	Reset Recovery to Synch_0/1			9.0			ns	(Note 6)
t_{WIDTH}	Set/Reset Input Pulse Width Synch_0/1 Minimum Pulse Width			5.0 3.0			ns	(Note 7)
t_{CYCLE}	Input Duty Cycle			25%		75%	ns	(Note 8)
f_{max}	Output Operating Frequency			10.0		100.0	MHz	(Note 9)
Jitter	Output Jitter			−250		+250	ps	(Note 10)
C_{IN}	Input Capacitance				5.0		pF	
C_{PD}	Power Dissipation Capacitance				50.0		pF	

AC Electrical Characteristics (Continued)

Note 1: Skew is measured at 50% of output level. For the case of 800 rising edge to rising edge, reflects output to output skew between Q0–Q4 and the rising output of Q7.

For falling edges it reflects the skew from output to output between Q0–Q4.

Also rising to falling skew reflects the output skew between the positive edges of 2XQ, Q0–Q4 and Q/2 with the negative edge of Q5. See *Figure 1.*

Note 2: For CGS801 skew is measured at the 50% level of the rising or falling edge transitions across outputs from Q0–Q7. See *Figure 2.*

Note 3: Skew is measured at 50% of output level. For the case of 802 rising edge to rising edge, reflects output to output skew between Q0–Q6.

For falling edges it reflects the skew from output to output between Q0 and Q1 or Q2 and Q3 or Q4 and Q5.

Also rising to falling skew reflects the output skew between the positive edges of 2XQ, Q0–Q4 and Q/2 with the negative edge of Q5. See *Figure 3.*

Note 4: Output pulse width is measured at $V_{CC}/2$. This parameter refers to a long term jitter versus period to period jitter and is guaranteed by design only. (Also refer to Note 10.)

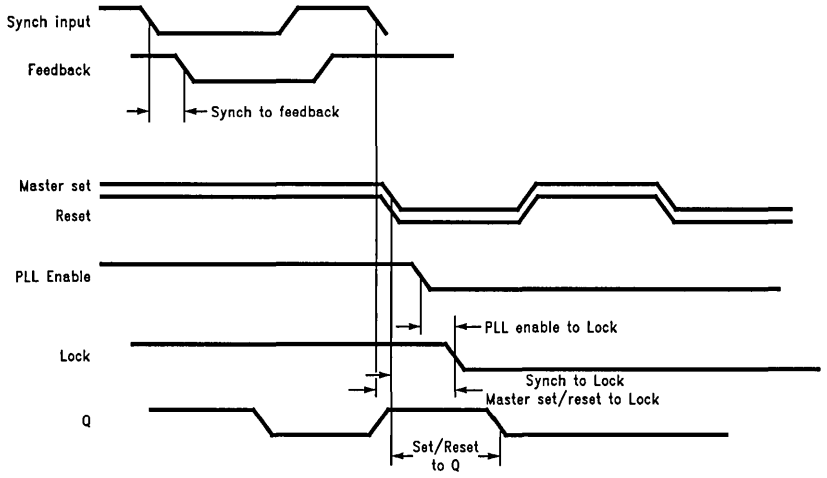
Note 5: Synch to feedback delay measures the delay (hold) required for the feedback to either of the synch inputs.

Master set or Reset propagation delays measures from 50% of the input to 50% of the output levels the amount of time for the output to transition to low state from its locked state.

Master set or Reset to Lock is measured from 50% of the input to 50% of the output. It is the amount of time required for the chip to acknowledge its reset condition via the lock pin.

PLL enable to Lock propagation delay is also measured from 50% of the input to 50% of the output level and it reflects the amount of time again to the lock pin to acknowledge its loss of lock for test chip enabling.

Synch loss to lock is also measured from 50% to 50% of the input/output levels and is the amount of time required for the chip to detect a loss of input signal. It can be used for fault tolerant applications. See figure below.



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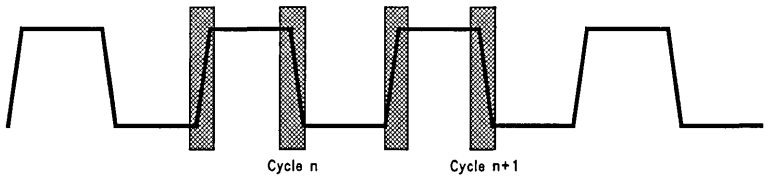
Note 6: Reset recovery time is measured from the rising edge of the reset pin to falling edge of the synch pin.

Note 7: t_{WIDTH} is measured at maximum V_{CC} and at 1.5V input levels.

Note 8: Input duty cycle is twice the reciprocal of the f_{max}. This reflects the maximum duty cycle allowed as an input to these devices. The actual duty cycle is not relevant since the part internally operates on a negative transition and performs a divide-by-two function.

Note 9: f_{max} is the maximum output frequency allowed. It represents the 2X outputs on the 800 and the 802 options, while f_{max} is for the X output on the 801.

Note 10: Jitter parameter is characterized and is guaranteed by design only. It measures the uncertainty of either the positive or the negative edge compared to its previous cycle. It is also measured at output levels of $V_{CC}/2$. Refer to figure below for further explanation.



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P(n) − P(n + 1) = ±250 ps for Either The Rising Or Falling Edge

AC Electrical Characteristics (Continued)

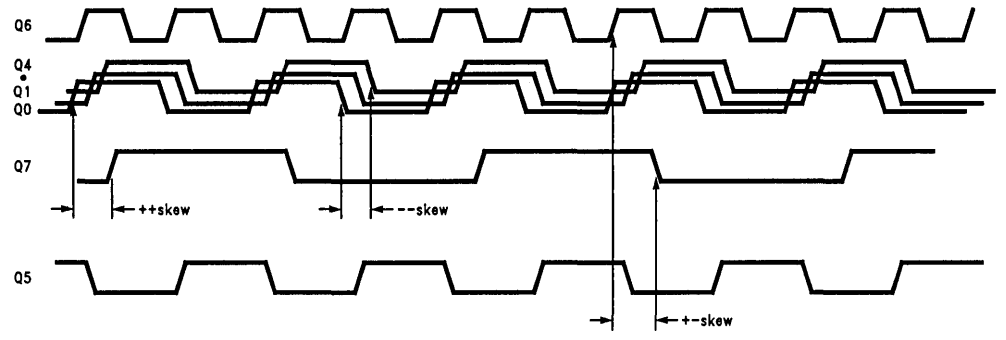

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FIGURE 1. CGS800

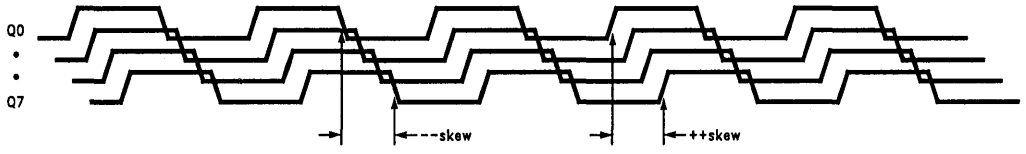

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FIGURE 2. CGS801

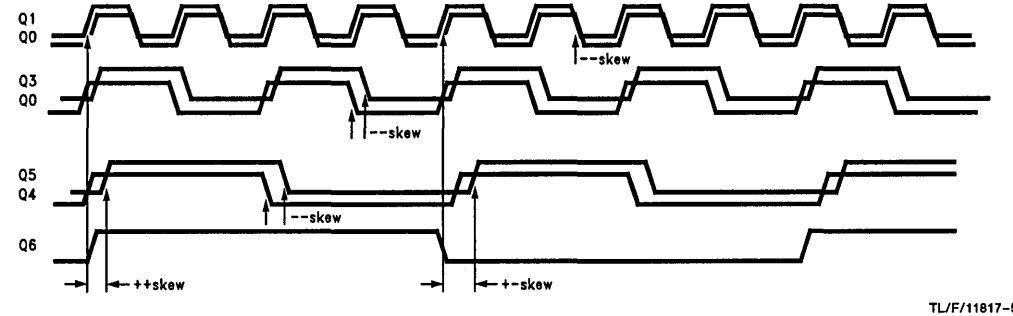

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FIGURE 3. CGS803

Typical Applications

The following represents some of the applications for the CGS800 and it options. In these applications 800/801/802 are used to generate and distribute clock signals for components that need synchronization.

The 802 has a 3/2 output which can be used to generate 50 MHz signals given a source of 33 MHz.

The next example also depicts typical usage for these products. The cache module could be either fully synchronized or non-fully synchronized.

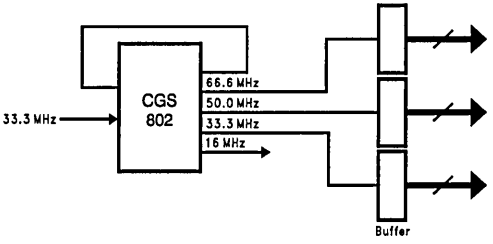
In the latter case the MBC runs at the same frequency as the CPU and so do the cache controller as well as the SRAMs. This can be achieved by providing a 1 to n clock driver/buffer to fanout the required input clock signals across the module. For the non-fully synchronized case, since the MBC and SRAMs as well as the controller are running at half the frequency of the CPU, the required buffer can be eliminated since the 800 and its options provide enough outputs to drive the required components.

Also another ideal application for these products are clock distribution across backplanes. Since these products include a digital PLL, the noise sensitivity is relatively less than their analog counterparts. This enables transmission of the required signal at half the frequency across the backplane. The outputs then can be synchronized together given a feedback reference signal.

The total skew for all the above applications must be calculated by adding the pin-to-pin skew of the 800 series to the part-to-part and the pin-to-pin of any required buffers.

$$t_{SKEW\,(tot)} = t_{OSHL/HL(PLL)} + (t_{pv} + t_{OSHL/HL})\,(Buffer)$$

Also to ensure jitter free operation of the PLL clock drivers, both ground and V_{CC} chokes must be used along with a bypass capacitor between the analog ground plane and the board power plane. A capacitor of 0.1 μF is recommended for bypassing, while the inductor size depends on the frequency of the operation as well as the induced noise frequency(ies) from both the power and the analog planes.



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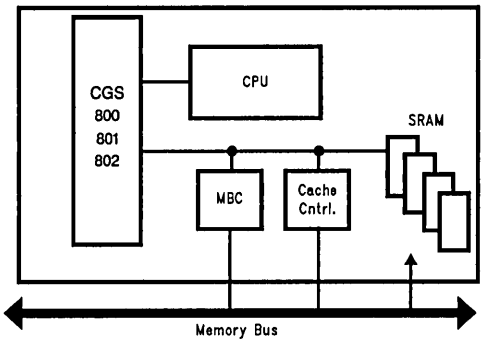

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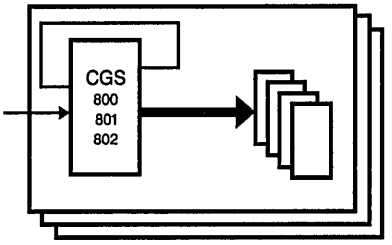

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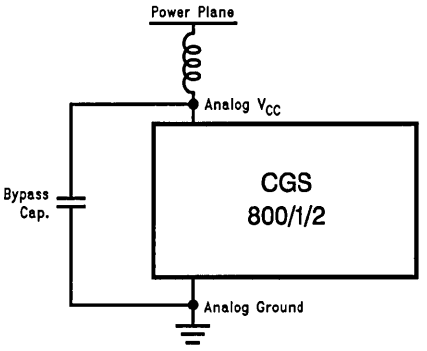

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4

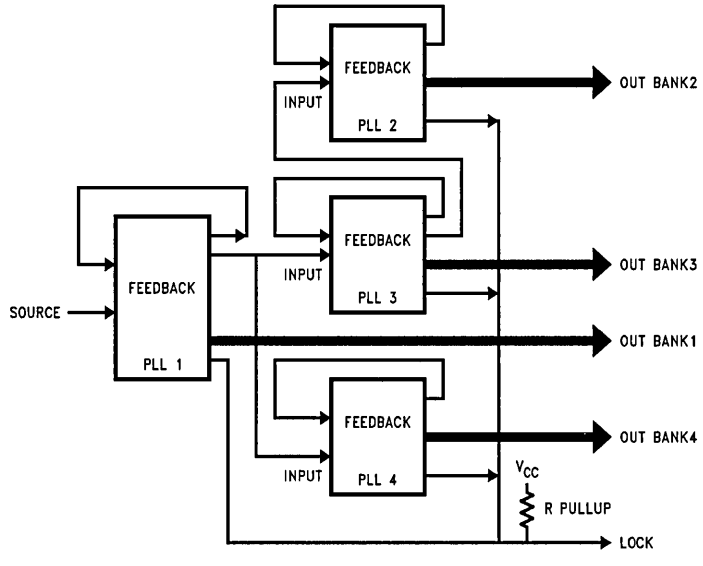
Applications Requiring Cascading Phase Lock Loops

Due to the accumulation of noise, it is not recommended to cascade phase lock loops. However cascading phase lock loops can be beneficial in large clock trees due to the elimination of part to part skew.

CGS800 series clock drivers are less sensitive to noise since they do not require any external components for the loop filter. Additionally the lock indicator being an open drain output, allows this pin to be wired-OR to enable the system to achieve lock state once all the PLLs have acquired a lock on the frequency.

In the diagram below one such application is depicted. The source frequency is the incoming signal. This signal which is often generated from a crystal oscillator is the base frequency of the system. The PLL1, while generating a bank of outputs, bank 1, has also generated the source input signals for PLLs 3 and 4. While PLL3's outputs have generated the reference input frequency for the PLL2.

In the diagram below one such application is depicted. The source frequency is the incoming signal. This signal which is often generated from a crystal oscillator is the base frequency of the system. The PLL1, while generating a bank of outputs, bank 1, has also generated the source input signals for PLLs 3 and 4. While PLL3's outputs have generated the reference input frequency for the PLL2.



TL/F/11817–12

National Semiconductor

CGS410
Programmable Video Pixel Clock Generator

General Description

The CGS410 is a programmable clock generator which produces a variable frequency clock output for use in graphics, disk drives and clock synchronizing applications. The CGS410 produces output clocks in CMOS and differential formats. The user is able to program the differential output levels to best suit the levels of the interfacing device. A common configuration allows PCLK to emulate positive ECL logic levels, eliminating the need for TTL to ECL translation.

The CGS410 is referenced off the XTLIN input which can be configured for either external crystal or external oscillator support. All internal frequency generation is referenced from the XTLIN input. The CGS410 can also be driven by EXTCLK as desired. EXTCLK may serve as the source from a fixed clock (for passthru mode), or as an external VCO input.

The CGS410 contains three internal user-selectable low pass filters (LPFs). A fourth option allows for the use of an external LPF configuration. Use of the internal filters greatly simplifies layout, reduces board real estate, and minimizes part count. A programmable polarity charge pump allows the user to optimize the optional external LPF circuitry.

The primary loop structure of the CGS410 consists of programmable N and R dividers. Both are contiguous; N can be any value between 2 and 16383, and R can be any value between 1 and 1023. Additional dividers of the internal VCO allow individual programmability for the PCLK, CMOS_PCLK, and LCLK outputs.

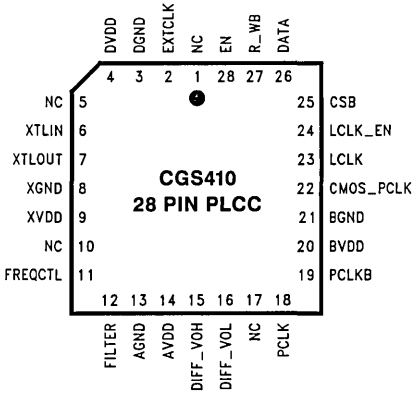
An additional advantage of the CGS410 is its ability to perform smooth, glitch-free clock output changes as the user selects passthru clock sources or changes the VCO frequency. A real-time synchronous load clock enable (LCLK_EN) control input allows for the enabling and disabling of the LCLK output. This is suitable for applications which require the removal of an active LCLK during the blanking portion of a screen refresh.

On power-up the XTLIN frequency is internally divided by two and routed to the PCLK outputs, providing a known power-up output frequency with a 50% duty cycle. The CGS410 is programmed by a serial stream of data. A serial bit read can verify the contents of the register.

Features

- Fully programmable frequency generator
- Provides frequencies to 135 MHz
- Configurable high-speed complementary clock outputs
- CMOS output clocks
- Glitch-free transitions for clock changes
- Powers up in a known state
- Single supply (+5V) operation
- Low current draw, ideal for battery applications
- Read/write control register
- Internal VCO and loop filters

Connection Diagram



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Important Note: This device is sensitive to noise on certain pins, especially FREQCTL, FILTER, AVDD, and AGND. Special care must be taken with board layout for optimum performance.

Table of Contents

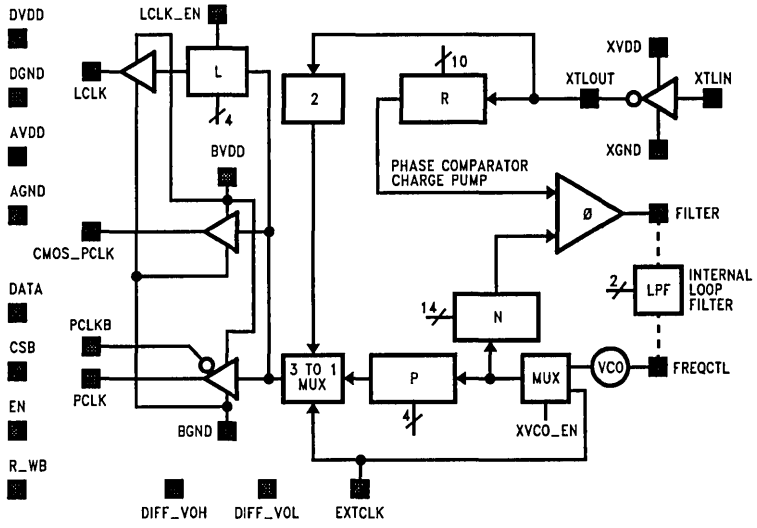
LIST OF FIGURES

1.0 Functional Description

The CMOS clock outputs are generated by a phase lock loop (PLL). The internal voltage controlled oscillator (VCO) derives a reference frequency from the crystal input (XTLIN) and produces a synthesized output. A programmable 1 to 16 divider and a passthru mux are positioned between the VCO and clock outputs, allowing a wide range of output frequencies without having to band switch the VCO. A load clock (LCLK) is also available. A synchronous LCLK control simplifies system frame buffer design.

With the CGS410 programmed to run in internal LPF mode, no external low pass filter components are required. There are three internal filters. If an external loop filter is desired, or if precise LPF parameters are required, the CGS410 can be programmed to use the external filter pin. The external filter requires two capacitors and one resistor. No external devices such as inductors or varactors are necessary. Frequency configuration is programmed through the internal N, R, P, and L dividers and the 3-to-1 MUX.

CGS410 Block Diagram



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2.0 Pin Definitions

Symbol	Pin	I/O	Function
AGND	13	S	**Analog Ground.** This pin serves as the return for the analog circuitry. AGND should also serve as the external filter return reference as sourced by FILTER. AGND should be well referenced to DGND.
AVDD	14	S	**Analog VDD.** This pin sources the internal VCO, internal loop filter, and charge pump. Due to the sensitive nature of this pin, special care should be taken to filter out noise for best performance. AVDD should track DVDD to within ±5%.
BGND	21	S	**Buffer Ground.** Output buffer supply return. This serves as the return for the CMOS_PCLK and LCLK outputs. Best output performance is obtained when the CMOS_PCLK and LCLK reception devices are referenced to BGND.
BVDD	20	S	**Buffer VDD.** This positive power supply input sources LCLK, CMOS_ PCLK and the differential PCLK output pair. Care must be taken to properly bypass this input with BGND.
CMOS_PCLK	22	O	**CMOS PCLK Output.** This single-ended output is typically used to drive devices which require CMOS input characteristics.
CSB	25	I	**Clock for Serial Data Input and Output.** This input is TTL compatible edge sensitive. In the serial read or write operation, the falling edge latches the R_WB and EN states. The rising edge completes the shift and transfer operation.
DATA	26	I/O	**Data Input/Output.** This is a bi-directional I/O pin used to transfer data in and out of the CGS410 in a serial fashion. Data must be valid when each bit is clocked on the rising edge of the CSB input. DATA is TTL compatible for input mode; CMOS compatible for output mode.
DGND	3	S	**Digital Ground.** This pin serves as the return path for the internal CGS410 counter circuitry. This input should be well referenced to BGND.

2.0 Pin Definitions (Continued)

Symbol	Pin	I/O	Function
DIFF_VOH	15	O	**Differential High Voltage Load.** This output is connected to a load network which is ten times the value of the load network connected to the differential PCLK pins.
DIFF_VOL	16	O	**Differential Low Voltage Load.** This output is connected to a load network which is ten times the value of the load network connected to the differential PCLK pins.
DVDD	4	S	**Digital VDD.** This pin serves as the source for the internal CGS410 counter circuitry. This input should be well referenced to BVDD and bypassed to DGND.
EN	28	I	**An Active-High, Level-Sensitive TTL Compatible Input.** This input is sampled on the falling edge of CSB, EN high allows data to be transferred to the shadow register in the write mode or to the shift register in the read mode.
EXTCLK	2	I	**External Clock.** When the internal multiplexer is set to EXTCLK mode, the crystal and phase-locked loop are bypassed, and this TTL compatible input will drive the PCLK outputs and the L divider input. If the external VCO mode is invoked, EXTCLK drives the P and N dividers. When this input is not selected, it should be driven to a high or low to avoid oscillations.
FILTER	12	O	**Filter Output.** This current source output is driven from the internal charge pump. This output is left floating in applications where only the internal low pass filters are used. FILTER is used for applications which require passive or active external LPF networks. For passive LPF networks, this output should be connected directly to FREQCTL input and the LPF network (see *Figure 3-7*).
FREQCTL	11	I	**Frequency Control.** FREQCTL is the VCO voltage control input. When in external loop filter mode, the voltage present on this input determines the VCO frequency. For applications which require only the internal filters, this input is left unconnected. This input is used for applications which require external networks for loop filtering. The input voltage range should not exceed AVDD, and not go below the AGND reference.
LCLK	23	O	**Load Clock Output.** This CMOS compatible, non-gated output is typically used in video applications which require a programmable clock to produce lower output frequencies synchronous to PCLK. Typically, this is used to clock video shift registers or RAMDACs.
LCLK_EN	24	I	**Load Clock Enable.** This synchronous active high TTL compatible input selects whether the LCLK output is disabled or enabled. A HIGH level enables the LCLK output pin, while a LOW disables activity on the LCLK. In the disabled state LCLK is driven high or low depending on the logic state of the L counter when disabled. Refer to the LCLK_EN timing specification.
PCLK	18	O	**Differential PCLK Output.** This high speed output is configured to drive a host of devices requiring differential clock inputs. Output voltage swing is defined by the differential level control bit (Bit 1).
PCLKB	19	O	**Differential PCLK Output.** This high speed output is configured to drive a host of devices requiring differential clock inputs. Output voltage swing is defined by the differential level control bit (Bit 1).
R_WB	27	I	**Read/Write Select.** R_WB is a level sensitive TTL compatible input. When writing values to the chip, the R_WB would be sampled low on the falling edge of CSB. Conversely, when reading values, the R_WB would be sampled high on the falling edge of CSB.
XGND	8	S	**Crystal Ground.** This pin serves as the ground return for the internal oscillator circuitry. All external oscillator support, be it active or passive, should be tied to XGND for best performance.
XTLIN	6	I	**Crystal Input.** XTLIN is designed to operate with crystal, oscillator or ceramic resonator input. For crystal input applications, the crystal should be the fundamental parallel mode type. See the applications diagrams for more information.
XTLOUT	7	O	**Crystal Output.** This output is used as the Pierce Oscillator output for use with parallel mode crystals. An external resistor between XTLOUT and XTLIN will bias this stage to approximately XVDD/2. This output is left floating for applications which directly drive the XTLIN.
XVDD	9	S	**Crystal VDD.** This positive power supply input sources the internal oscillator circuitry. All external oscillator support, be it active or passive, should be referenced to XVDD for best performance. This supply input must track DVDD to within 5%.

3.0 Circuit Operation

The CGS410 programmable clock generator uses a crystal oscillator as a frequency reference to generate clock signals for video applications such as display systems or disk drive constant density recording. The reference may come from any source as long as input specifications are maintained. Both single-ended (CMOS) and differential clock outputs are generated. Both clock outputs are synchronized to simplify system timing. A unique combination of internal functions (such as the VCO, the crystal oscillator, a phase comparator, various programmable counters, and a readable 47-bit serial control register) allows for versatility and ease of design.

3.1 INTERNAL VCO OPERATION

No external VCO inductor or capacitor components are required for operation, simplifying PC board layout requirements. P counter programmability is contiguous from 1 to 16, although a 50% duty cycle will be created only if the P modulus is an even number, or if the P modulus is 1.

3.1.1 VCO Tuning Characteristics

The CGS410 VCO requires an input voltage to set the proper operating frequency. The input voltage is the direct result of charge sourced or sinked off the LPF network. The function of the LPF is to convert the charge to voltage (see "Loop Filter Characteristics"). The VCO requires the input voltage to be set in the linear portion of the input range. The VCO output frequency is a function of the VCO gain (F_{VCO}) and the range of the input voltage.

Normal, or linear VCO operation will place the input voltage range from AVDD/3 (the lowest frequency response) to approximately AVDD − 1.5V (the highest frequency response). The linear operating range is illustrated in *Figure 3-1* with VCO output frequency (F_{VCO}) expressed as a voltage filter input (V_{FILTER}).

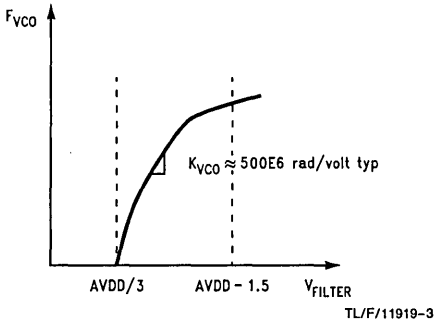

FIGURE 3-1. Linear Operating Range

Applying an input voltage beyond the intended range will force the VCO to rail high or low. Input voltages which exceed AVDD, or go negative with respect to AGND, can damage the CGS410.

3.2 CRYSTAL OSCILLATOR OPERATION

The XTLIN and XTLOUT pins are used in conjunction with an external crystal, two capacitors, and two resistors to form an external oscillator tank circuit. The crystal should be a fundamental parallel mode type. XTLOUT serves as the driving source to the crystal. Consideration should be given to avoiding crystal overdrive situations. XTLOUT should show an output waveform well within the XVDD and XGND boundary conditions. The elements forming the crystal tank should be low-leakage devices. Capacitor values (per crystal leg) will typically fall within the range of 10 pF–40 pF.

The crystal oscillator divide-by-2 output may be directed to appear at the clock outputs depending on the state of the 3 to 1 MUX. On power up, both differential and CMOS_PCLK outputs will reflect half the oscillator frequency input. The XTLIN pin can be driven from a variety of sources, including ECL, TTL, or CMOS logic. Attach a coupling capacitor into the XTLIN pin when using a TTL or small-signal source (such as ECL). Please see application diagrams for details. The CGS410 may be used to genlock to an external clock source.

3.3 PHASE COMPARATOR OPERATION

The phase comparator compares the difference in clock edges between the internal N and R counter outputs. The difference results as either a charge source (pump-up), or charge sink (pump-down). The amount of charge is directly proportional to the phase difference (see *Figure 3-2*). The phase comparator controls the VCO by comparing the phase of a derived signal from a known accurate reference source such as a crystal or an external reference signal. In genlocking situations, the reference source may be a constant stream of pulses such as an external HSYNC.

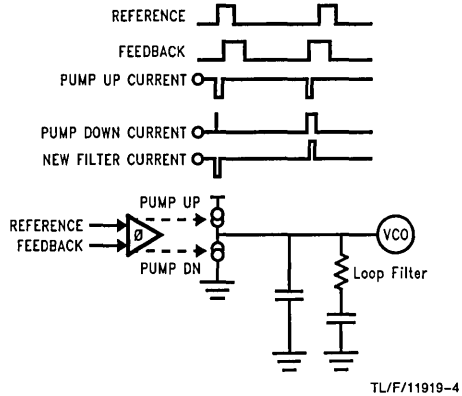

FIGURE 3-2. Phase Comparator/Charge Pump

The VCO-derived signal is divided by N, and applied to one phase comparator input. The R divider output serves as the other phase comparator reference input. The comparator functions as a three-state machine: providing a pump-up state when R leads N, and a pump-down state when N leads R. This situation exists only when there is a difference between the two input edges. The VCO frequency is then increased or decreased in the closed loop system. At all other times, the phase comparator is in a tri-state condition.

The direction and amount of charge on the FILTER pin is proportional to the difference in the phase comparator input edges. The charge flow is made up of correction pulses. The resulting correction pulses are converted to a voltage as dictated by the LPF network. Selection of LPF components characterizes the resulting voltage and phase response.

3.0 Circuit Operation (Continued)

The CGS410 allows the user to select the quantity of charge pump current and its direction. Specifying the direction of charge flow is useful in situations where an external filter and/or VCO is incorporated. See the applications section for an example. In situations where external networks lack the charge sensitivity, the amount of charge can be increased at the user's discretion.

3.4 PROGRAMMABLE DIVIDER OPERATION

The CGS410 has four internal dividers (R, N, P, and L) which are programmed serially via the internal control register.

The R (reference) divider provides a reference frequency from either a crystal or an externally generated clock source. The divisor range is contiguous and varies from 1 to 1023. The modulus selected is the direct binary equivalent loaded in the serial control register at bit locations 24–33.

The internal N divider provides a means of locking the VCO with a constant tuning resolution that is independent of the pixel system. Its contiguous modulus range is 2 to 16383.

The P (postscaling) divider provides a means of generating an output over a wide frequency range from a VCO which has a fixed frequency range. The modulus selections of the P divider range from 1–16 inclusive. The modulus of this divider is programmed with serial control register bits 16–19. The PCLK outputs are square when the P modulus is 1, 2, 4, 6, 8, 10, 12, 14, or 16. If the P modulus is 3, 5, 7, 9, 11, 13, or 15, the PCLK outputs are low one less count than it is high. For example, dividing by modulus 5 would result in three counts high and two counts low.

The L (load) divider provides a means of generating a load clock by dividing the PCLK by a modulus ranging from 1–16 inclusive. The modulus of the load divider is programmed with serial control register bits 20–23. The L clock output is derived from the output of the internal MUX, so whichever output is selected by the mux will be divided by L. The L clock can be asynchronously disabled/enabled by a serial bit. The LCLK outputs are square when the L modulus is 1, 2, 4, 6, 8, 10, 12, 14, or 16. If the L modulus is 3, 5, 7, 9, 11, 13, or 15, the LCLK is high one less count than it is low. For example, dividing by modulus 5 would result in three counts low and two counts high.

3.5 CONTROL REGISTER OPERATION

The CGS410 serial control register consists of 47 bits, each of which control various internal functions as described later in the section "Structure of the Internal Serial Control Register". All bit locations are RAM based, and are volatile during power cycling operations. The CGS410 contains an internal shadow register which directly reflects that of the serial shift register. The contents of the shadow register program the CGS410 parameters. The shadow register allows the user to write a stream of data to the serial shift register, then, for the last bit do a write followed by a transfer operation. The transferring operation allows all parameters to be loaded into the respective target registers in a single clock cycle. This ensures that changes in clocking parameters take place in a uniform manner.

Read operations are performed in the opposite sequence from that of write. Here, data is transferred from the shadow register to the serial shift register on the first bit, and serially shifted out thereafter.

Performing transfer operations is up to the discretion of the system programmer. In many instances the system may only require partial diagnostic information from the internal registers, and hence avoid a full serial transfer. This is easily accomplished by transferring the data, then shifting only that portion required for the task. The sequence can easily be repeated without adverse affects on the shadow register. Bear in mind that the first data bit written will be the first bit read-out.

3.5.1 System Loading Sequence

All system access to the CGS410 takes place relative to the rising or falling edge of CSB. EN and R_WB must be stable and in the desired state prior to the falling edge of CSB, while data must be present, or sampled by the system CPU during the rising edge of CSB.

Serial write operations consist of setting both ENable and R_WB low for the first N-1 bits. Transfer of serial data to the latch register occurs when writing the N^{th} (last) bit. On the last bit-write bus cycle, set EN high. The CGS410 will shift in the last bit then perform a transfer to the shadow register. Once the transfer takes place the PLL will immediately begin to lock to the new values.

Serial read operations consist of setting ENable low and R_WB high for all bits. However, if the programmer wishes to refresh the data in the serial shift register, a transfer operation is performed when reading the first bit. On the first bit read bus cycle, set EN high. The CGS410 will transfer all data in the shadow resister to the shift register then shift out the first valid data bit. Note that the contents of the shadow register are unchanged by the read transfer with no effect on the CGS410 internal parameters or output clocks.

The rest of the serial read operation consists of shifting data bits 2–47. Each bit becomes valid at the DATA pin after CSB goes low and then shifts on the positive edge of CSB.

3.5.2 Structure of the Internal Serial Control Register

The following describes the bit structure of the Control Register. Where applicable, all programmable registers values are loaded with the LSB first.

Serial Bit 1

Differential Level control. This bit sets an internal bias level to provide differential "large" (bit 1 high) or "small" (bit 0 low) signal swing. On power-up this bit is low (small signal swing).

3.0 Circuit Operation (Continued)

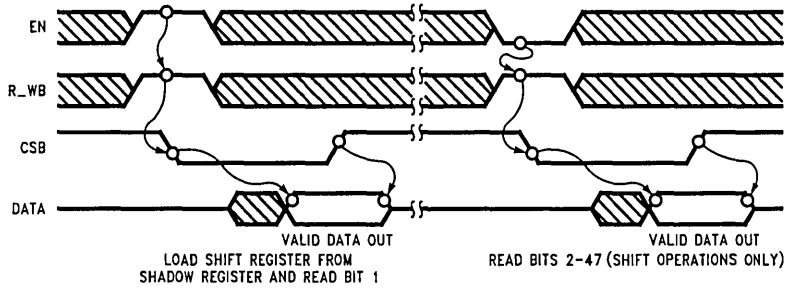

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FIGURE 3-3. Control Register Read Operations

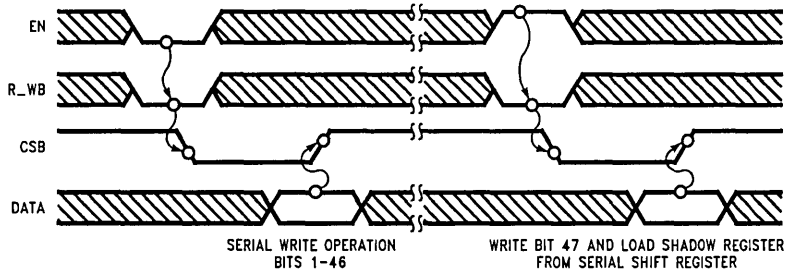

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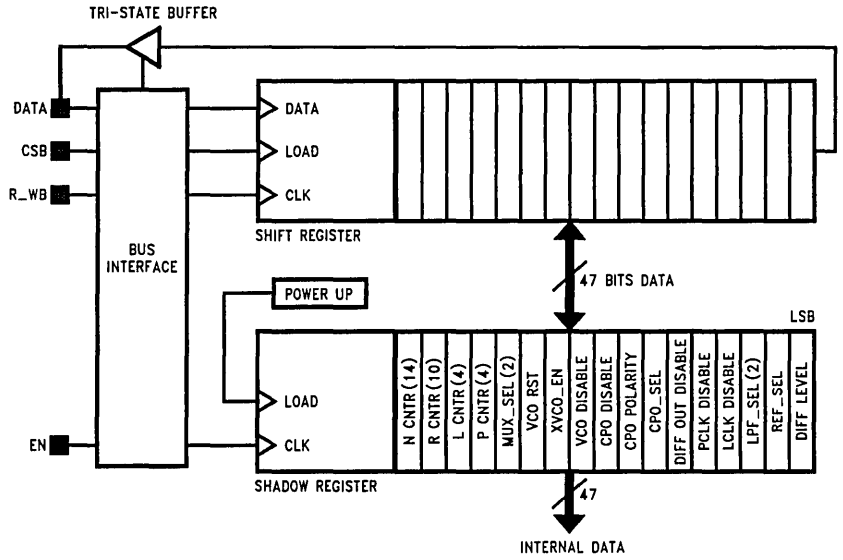
FIGURE 3-4. Control Register Write Operations



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(Simplified functional representation only)

FIGURE 3-5. Control Register Architecture

3.0 Circuit Operation (Continued)

Serial Bit 2

Reference Select. A logic low configures XTLIN and XTLOUT for crystal mode. A logic high configures for EXTREF. On power-up this bit is low (crystal mode).

Serial Bits 3, 4

Loop Filter Select. LSB is loaded first. Bit values are mapped by the following:

Bit 4	Bit 3	
0	O	External Mode
0	1	500 kHz Reference
1	0	1.5 MHz Reference
1	1	5 MHz Reference

External mode selected on power-up.

Serial Bit 5

Load Clock (LCLK) Disable. A logic low enables LCLK. A logic high freezes the LCLK output low and disables the L counter. Note that this is different from the effects of the L clock enable pin, which is a synchronous disable and which only disables the output (leaving the counter operational). LCLK is enabled on power-up.

Serial Bit 6

PCLK Disable. A logic low enables CMOS_PCLK output. A logic high freezes CMOS_PCLK low. CMOS_PCLK is enabled on power-up.

Serial Bit 7

Differential (DIFF) Out Disable. A logic low enables Differential Output. A logic high causes both differential outputs to be driven below 400 mV. DIFF out is enabled on power-up.

Serial Bit 8

Charge Pump Output (CPO) Select. A logic low forces a 25 μA current pump. A logic high forces a 75 μA current pump. There is a 25 μA current pump on power-up.

Serial Bit 9

Charge Pump Output (CPO) Polarity. A logic low forces a "normal" output response, i.e., the charge pump sinks current when the feedback signal (N counter output) leads the reference signal (R counter output). A logic high forces an inverted response. CPO polarity is in normal mode on power-up.

Serial Bit 10

Charge Pump (CPO) Disable. A logic low enables charge pump activity. A logic high Tri-States CPO activity. CPO is enabled on power-up.

Serial Bit 11

Voltage Controlled Oscillator (VCO) Disable. A logic low enables VCO operation. A logic high disables VCO activity. VCO is enabled on power-up.

Serial Bit 12

External VCO Enable (XVCO_EN). A logic high enables the external VCO path. This bit is disabled on power-up.

Serial Bit 13

Voltage Control Oscillator (VCO) Reset. A logic high resets the VCO. This means that the charge pump output is clamped to AGND to guarantee that the loop filter is discharged. VCO reset is high (enabled) on power-up. A logic low places the VCO in normal operating mode. In order for the PLL to lock, this bit must be returned low after power-up.

Serial Bits 14, 15

Internal clock MUX_SEL. LSB (bit 14) is loaded first. This MUX selects which clock signal is passed to the clock outputs. Bit values are mapped by the following:

Bit 15	Bit 14	
0	0	XTAL/2 Mode
0	1	P Counter Mode (Internal PLL)
1	0	External Clock Mode (Passthru)
1	1	XVCO Mode

XVCO mode (1,1) is used in conjunction with bit 12, XVCO_EN to allow an external VCO to drive the N and P counters via the EXTCLK input pin. The XTAL/2 mode is selected on power-up.

Serial Bits 16–19

P counter modulus select. LSB bit 16 is loaded first. The P modulus range is 1–16 continuous. Serial bits 16–19 are loaded with the desired modulus value − 1 (i.e., 0–15). P counter divides by modulus 4 on power-up.

Serial Bits 20–23

L counter modulus select. LSB bit 20 is loaded first. The L modulus range is 1–16 continuous. Serial bits 20–23 are loaded with the desired modulus value − 1 (i.e., 0–15). L counter divides by modulus 4 on power-up.

Serial Bits 24–33

R counter modulus. LSB (bit 24) is loaded first. The R counter divides continuously by the binary value loaded. Modulus range is 1–1023 inclusive. R is initialized at 20 on power-up. Loading R = 0 is undefined.

Serial Bits 34–47

N counter modulus. LSB (bit 34) is loaded first. The N counter divides by the binary value loaded. Modulus range is 2–16383 inclusive. N is initialized at 120 on power-up. Loading N = 0 or N = 1 is undefined.

3.5.3 Power-Up Conditions

At power-up the control register bits are set to provide initial operating conditions as follows:

1. All clock outputs are active.
2. The differential PCLK and CMOS_PCLK outputs function at a rate of XTAL/2. The LCLK functions at a rate of XTAL/8.
3. The status of the internal register reflects the following:
   N = 120
   R = 20
   P = 4 (bits 16–19 = 3)
   L = 4 (bits 20–23 = 3)
4. All other programmable bits are low, except VCO_RPST which is set high.

3.0 Circuit Operation (Continued)

Note that with VCO_PST high, the charge pump output voltage is clamped to AGND. This condition will prevent the PLL from locking. *Proper VCO lock operation will require the user to reset this bit.*

3.6 LOOP FILTER CHARACTERISTICS

The function of the low pass filter (LPF) is to transform the CPO charge output into a DC voltage seen on the VCO input. A variety of LPF configurations exist. This particular architecture is suited towards a C/RC type of configuration. *Figure 3-7* shows such an architecture. The desired Bode plot of gain and phase is shown in *Figure 3-6* with 20 dB/decade slope at ω_0 for stability at unity gain.

Capacitor C_2 governs the PLL's ability to reject instantaneous bit jitter. This represents the high frequency pole. R_1 and C_1 determine the low frequency zero. When R_1, C_1 and C_2 values are properly calculated, ω_0 will fall in the −20 dB/decade flattened response and will help track out the 1/f noise inherent in the VCO. An added benefit is that the LPF phase response is symmetrical at this frequency. Increasing or decreasing C_2 will move the high frequency pole up or down, likewise with the R_1 and C_1 combination. Converging and expanding the pole pairs will result in a underdamped or overdamped filter. Resistive component R_1 directiy affects this response.

Loop filter components can vary somewhat to conform to the given application requirements. Underdamping the loop response causes decreased loop stability (ultimately resulting in loop oscillation), but will decrease lock time, an advantage in applications where lock time is critical. On the other hand, overdamping the filter response leads to decreased phase noise while increasing the loop lock time.

Generally, setting C_2 at $1/10^{th}$ to $1/50^{th}$ the value of C_1 will provide reasonable loop response.

Selecting the appropriate loop filter depends on the frequency at the phase comparator. The most effective filtering ranges for the three internal filters are:

Loop Filter 1: 0.3 MHz–1.0 MHz (80 < N < 500)

Loop Filter 2: 1.0 MHz–3.0 MHz (30 < N < 80)

Loop Filter 3: 3.0 MHz–6.0 MHz (15 < N < 30)

Best performance (lowest phase noise) is obtained by programming F_{REF} to fall somewhere in the middle of any of these frequency ranges.

3.6.1 Loop Filter Calculations

Several constraints need to be known in order to determine the external loop filter components for external loop filter operation: the loop divide ratio (N), the phase comparator gain (K_p), the VCO gain (K_o) the loop bandwidth (ω_o), and the phase margin (F).

The constants for the CGS410 are as follows:

K_o = 500E6 rad/v

K_p = 4 μA/rad when CPO SEL (bit 8) = 0
12 μA/rad when CPO SEL (bit 8) = 1

The variable parameters for the CGS410 are as follows:

N = N counter modulus

R = R counter modulus

f_{XTAL} = frequency at XTLIN pin (in Hz)

N is equal to the VCO frequency divided by the frequency input at F_{REF}. The loop bandwidth (ω_o) is recommended to be about $1/30^{th}$ of the F_{REF} frequency (times 2π radians). Most users will find the following set of equations give good loop filter values for frequency synthesis applications:

$R_1 = (0.23 \bullet N \bullet f_{XTAL})/(K_p \bullet K_o \bullet R)$

$C_1 = (68.4 \bullet K_p \bullet K_o \bullet R^2)/(N \bullet f_{XTAL}^2)$

$C_2 = C_1/20$

The following equations can be used for different cutoff frequencies and phase margins.

For F = 57 degrees phase margin:

$R_1 = (1.1 \bullet N \bullet \omega_o)/(K_p \bullet K_o)$

$C_1 = (3 \bullet K_p \bullet K_o)/(N \bullet \omega_o^2)$

$C_2 = (0.15 \bullet K_p \bullet K_o)/(N \bullet \omega_o^2)$ ($1/20^{th}$ C_1 value)

For a phase margin other than 57 degrees:

$R_1 = (\text{Cosec } F + 1) \bullet (N \bullet \omega_o)/(2 \bullet K_p \bullet K_o)$

$C_1 = (\text{Tan } F) \bullet (2 \bullet K_p \bullet K_o)/(N \bullet \omega_o^2)$

$C_2 = (\text{Sec } F - \text{Tan } F) \bullet (K_p \bullet K_o)/(N \bullet \omega_o^2)$

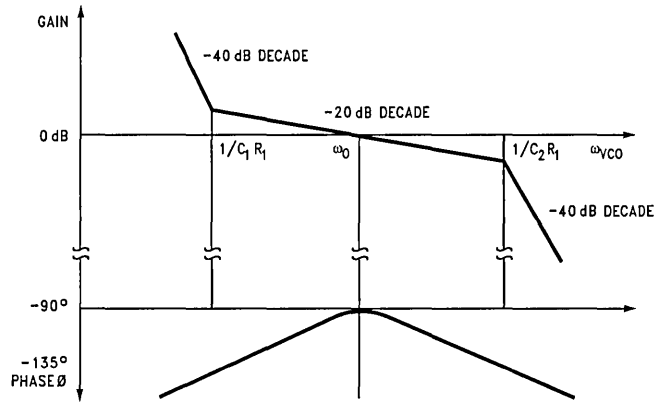

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FIGURE 3-6. Bode Plot of Loop Filter Response

3.0 Circuit Operation (Continued)

The values R_1, C_1 and C_2 refer to the following filter configuration:

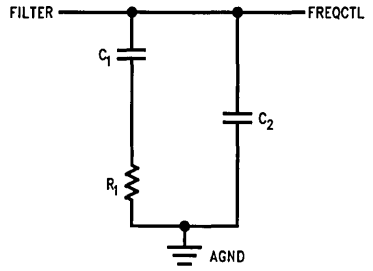

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FIGURE 3-7. External Low Pass Filter

The above equations refer to the low pass filter loop response associated with a single phase comparator reference frequency. In many situations the CGS410 will be required to generate many output frequencies. Best performance is obtained by matching the filter to the required frequency. This may require different LPF component values for each configuration. In most instances, selection of any of the CGS410's three internal filters will satisfy the LPF requirements. A fourth option allows the use of an external configuration.

When generating a wide range of output frequencies, a phase margin of approximately 60 degrees should be maintained for a theoretically stable system. In practice, wide variation is possible. Note that the equations expressed above are functions of only N, ω_o, K_p and K_o. PCLK output frequency is NOT included. Since the CGS410 allows the use of an external loop filter as well as three internal filters, there should always exist a configuration of counter values that will produce a quality clock output without the need to externally switch loop filter values.

3.7 CLOCK DEGLITCHING CONSIDERATIONS

The CGS410's automatic deglitching function ensures that the clock output pulse width will be no shorter than the briefest clock high or low time currently programmed. Deglitching the clock outputs allows the system to maintain proper state throughout the clock change cycle.

When the user loads the shadow register with a code that changes the state of serial bits 14 through 19 (the P counter modulus or the internal clock MUX select), the deglitching process is automatically initiated. The PCLK outputs are temporarily frozen and then are restarted several PCLK periods later synchronous to the new output frequency.

3.8 CONFIGURABLE DIFFERENTIAL OUTPUT BUFFERS

For proper operation, a 10:1 resistive relationship will exist between the DIFF_VOH/VOL pin loads and the PCLK differential loads. Adhering to this relationship will provide the correct voltage drive at the PCLK differential outputs.

3.9 TERMINATION CONSIDERATIONS

Each differential PCLK output serves as a current source to a resistive termination network. The termination network matches the characteristic impedance as seen by the PCLK system trace. Proper network component selection also biases the differential output stage to maintain the proper V_{OH} and V_{OL} values. The most common network uses a resistive pull-up/pull-down combination (see *Figure 3-9*). The combination of the resistive devices provides a DC Thevenin equivalent with a specified voltage output and load resistance.

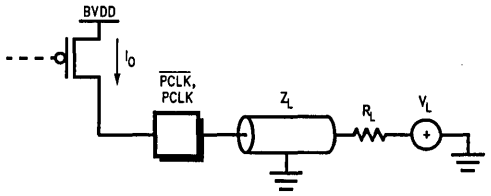

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FIGURE 3-8. Termination

Figure 3-8 illustrates the electrical model for driving the differential PCLK outputs down a transmission line. It terminates in a Thevenin equivalent consisting of a resistance (R_L) and a source voltage (V_L). Modulating the output driver gate modulates the output PMOS source current (I_O). The combination of source current and load resistance results in an output voltage. For properly terminated systems, the characteristic impedance of the signal line (Z_L) should closely approximate the effective R_L. When using a Thevenin equivalent circuit (see *Figure 3-8*), the effective R_L is described as the open circuit voltage divided by the short circuit current:

$$R_L = V_{OC}/I_{SC} = (R_1 \bullet R_2)/(R_1 + R_2)$$

In addition to maintaining the proper resistance, the resistors must be selected to provide the proper V_L for the circuit. The resistors should be selected such that V_{OL} can be reached. V_{OL} is the most important parameter. The following rule will apply:

$VL < V_{OL}$, where typically V_L = is 150 mV–500 mV below the V_{OL}.

V_L is calculated as the open circuit voltage:

$$V_L = V_{OC} = BVDD \bullet R_2/(R_1 + R_2)$$

In all the equations, the output PMOS source current (I_O) should never exceed 21 mA.

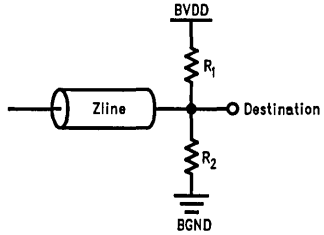

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FIGURE 3-9. Pull-Up/Pull-Down DC Termination

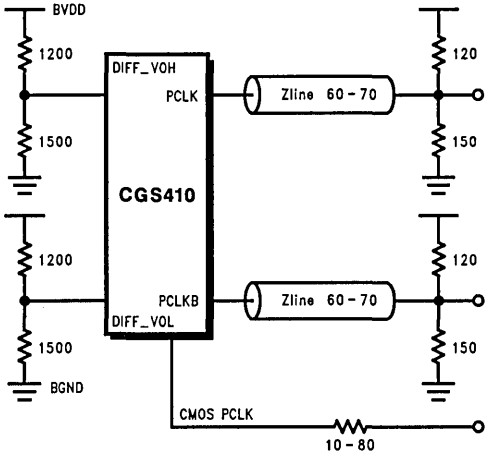
Figure 3-10 illustrates a typical termination that will assume the V_{OH} and V_{OL} requirements are met without overdriving the CGS410 outputs. The value of V_{OL} must meet the requirements of the destination device. For positive ECL logic,

3.0 Circuit Operation (Continued)

the resistive termination is normally set to provide a voltage of 3V. This is readily accomplished with R_1 = 220 and R_2 = 330. With the control register differential level (bit 1) equal to 0, the output V_{OL} = BVDD * 0.642V or 3.21V at BVDD = 5V. The V_{OH} is typically BVDD * 0.824V or 4.12V at BVDD = 5V. In this example,

$$I_{O(MAX)} = (V_{OH} - V_L)/R_L$$
$$= (4.12 - 3)/132$$
$$= 9.5\ mA$$

Generation of V_{OH} requires the maximum I_O. Since the CGS410 can provide up to 21 mA of output source for V_{OH}, this is well within driving specifications.



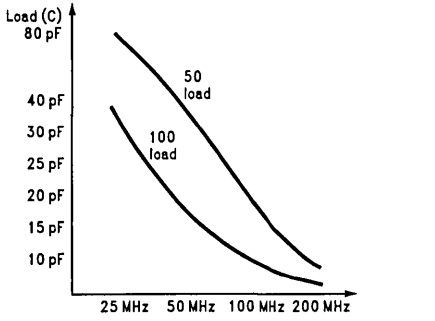
TL/F/11919-12

FIGURE 3-10. Typical Termination (Bit 1 = 0)

Other factors which influence the differential output response include the characteristic impedance of the line (Z_L) and capacitive loads. The characteristic impedance of the "stripline" connecting the CGS410 output to the destination device input should match the Thevenin equivalent of the line termination to assure maximum power transfer, glitch-free clock outputs and reduced EMI.

Capacitive loading will affect the rise and fall times of the output waveform. The current required is: i C V/T.

Figure 3-11 indicates typical loading parameters used for driving differential output capacitive loads for frequencies from 25 MHz to 200 MHz with a 1V differential voltage swing. In addition, the resulting graph bases the voltage slew rate (v/t) for 1/10 of the operating frequency period. The graph illustrates the fact that as the output frequency and capacitance increase, the amount of source current must also increase to maintain reasonable slew rates.



TL/F/11919-13

FIGURE 3-11. PCLK/PCLKB Load vs. Frequency

CMOS_PCLK drive requirements vary greatly from those of the PCLK differential counterparts because the output buffer size and the output impedance are higher. Best performance is usually obtained by placing a series resistor on the output and then driving to the receiving device. Selection of the resistor is best obtained on an empirical basis. Normally, resistor sizes starting in the 10Ω–80Ω range provide a good start. *Figure 3-10* shows a typical termination scheme for 60–70 board impedance.

3.10 SYSTEM INTERFACE CONSIDERATIONS

The CGS410 data bus can be managed by a wide variety of controllers. If a serial data source is not available from the controller, external serializing circuitry, or slight bus modification may be required.

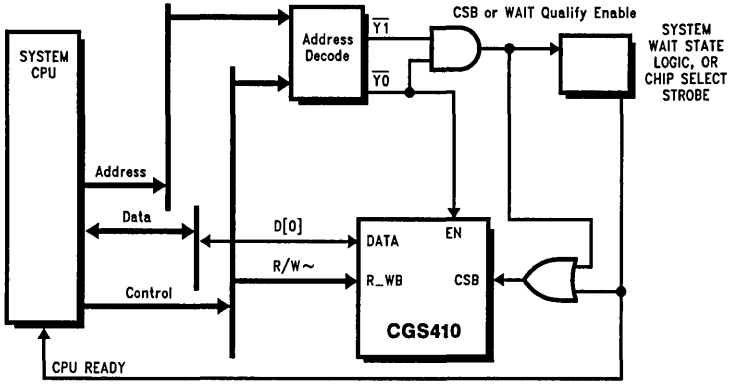
Figure 3-12 illustrates a generic hardware system implementation where the CGS410 control signals are qualified through a memory map. In this example, the CGS410 is mapped into two address locations. This particular mapping scheme allows:

1) typical read/write operations to execute through one mapped port,
2) transfer operations to execute through the second mapped port (see Figure 3-12).

Depending on the system configuration, CGS410 control signals such as R_WB may be connected directly to a qualified CPU strobe R/W~. In this example, the system bus data line zero D[0] serves as the DATA port of the CGS410. The control signal EN may be derived from address decode select logic, and can maintain any state during non-CGS410 accesses.

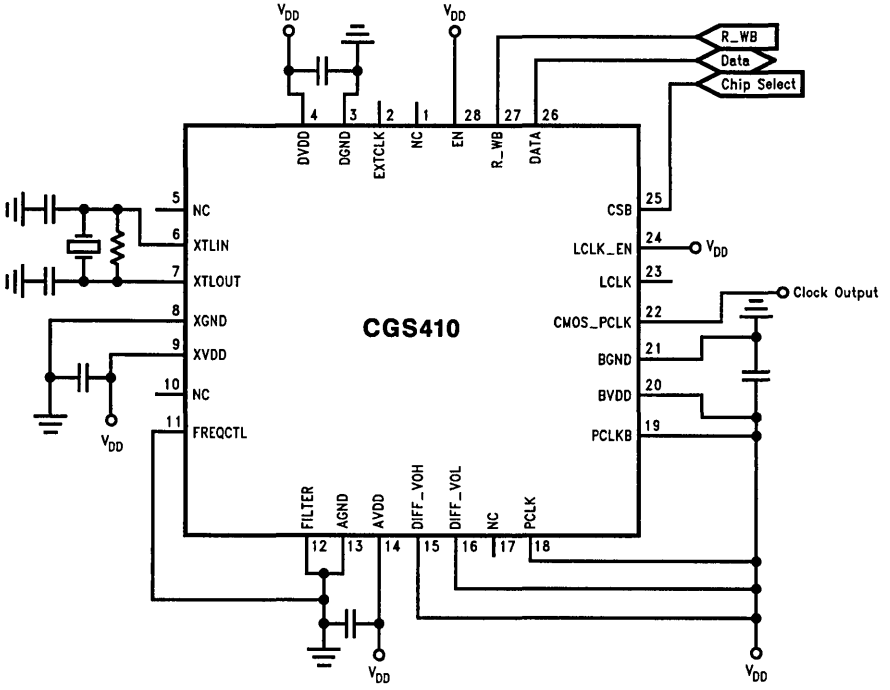
The control signal CSB requires the greatest attention because it is the CGS410's clocking agent. Care must be taken to ensure that no activity takes place on this input during non-CGS410 accesses. Note that when this input is strobed, all control and data present at the CGS410 must conform to the respective rising and falling edges of this signal as specified in the timing diagrams in this data sheet. CSB may be generated from a variety of system sources. A qualified CPU WAIT may serve as one source. Other timing requirements may need a timing generator (such as a two-state machine) to generate CSB.

3.0 Circuit Operation (Continued)



TL/F/11919–14

FIGURE 3-12. Serial Interface Example



TL/F/11919–15

FIGURE 3-13. Minimum Cost, <80 MHz CGS410 Implementation

3.11 APPLICATIONS

Many applications exist which can use the synthesized clock capability of the CGS410. Because of the CMOS nature of the device, it can maintain high frequency clock rates while consuming little current. This allows use of the CGS410 in battery powered systems.

Application requirements for the CGS410 are largely dictated by the user. *Figure 3-13* illustrates a low cost implementation. Pulling the PCLK outputs to BVDD will turn the outputs off. In this configuration, DIFF_VOH and DIFF_VOL are also tied to BVDD. CMOS_PCLK serves as the frequency output source. Note also that all LCLK, EXTCLK, FILTER and crystal functions can be modified to address the needs of the application.

Figure 3-14 shows the common clock drive requirements for a video-based system. The CGS410 provides all clocking sources. LCLK provides a synchronized low-frequency submultiple of PCLK for driving the RAMDAC load data requirements. In addition, LCLK can easily be used to drive the respective frame buffer array which clocks the display data. The Load Clock Enable (LCLK_EN) can be used to disable load clock pulses during screen blanking intervals.

3.0 Circuit Operation (Continued)

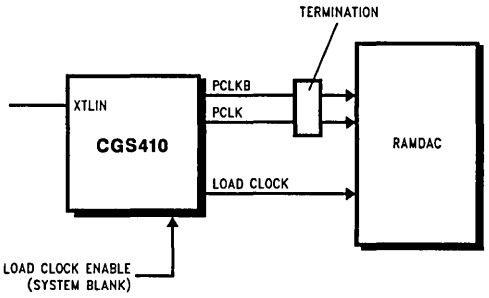


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FIGURE 3-14. Common Video Application

Genlock applications allow one system to synchronize its clocking system to an external source of clocking pulses. In most instances, the external source is asynchronous to the receiving system. In this example *(Figure 3-15)*, the XTLIN is driven from an external HSYNC source. Care must be taken to ensure that the respective V_{OH} and V_{OL} levels of HSYNC always fall within the XTLIN required input levels. Additional modification of HSYNC may be necessary to ensure that no over or under shoot conditions occur. The HSYNC frequency input is then passed to the internal R (or reference) divider. R is normally set to a divide by one in these applications. The PLL is referenced to and locks on the incoming HSYNC. This configuration requires that an HSYNC signal is always present to ensure that the loop will remain locked. XTLIN is negative edge triggered.

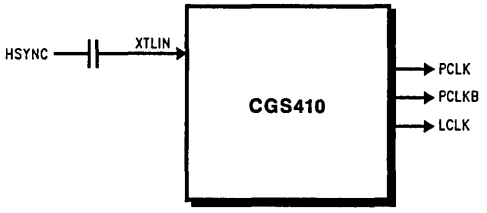

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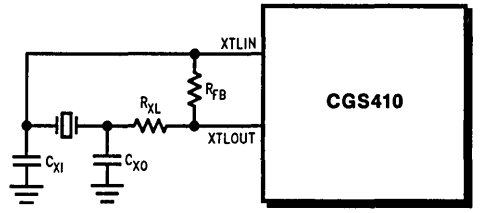
FIGURE 3-15. Primary Loop GENLOCK Configuration

Figure 3-16 shows the Pierce Oscillator configuration when using an external crystal. The feedback resistor placed between XTLIN and XTLOUT biases the input. The additional resistor in the diagram serves to limit the amount of power dissipated by the crystal. This value is based upon crystal drive specifications. In most circumstances this resistor is not required. The two capacitors off the crystal leg serve to form the crystal tank. These components, combined with the electrical function of the crystal, form the additional 180 degree phase shift required for oscillation.

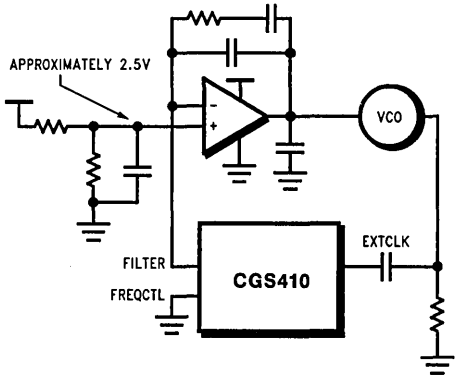


TL/F/11919–18

FIGURE 3-16. Crystal Configuration

Component values depend on the crystal manufacturer specifications. C_{XI} and C_{XO} will typically range from 10 pF to 30 pF. Resistor R_{XL} limits the amount of current flow into the external crystal tank R_{XL} is usually between 100Ω and 600Ω. In many instances this component may be eliminated. The feedback resistor (R_{FB}) biases the internal inverter so proper oscillation can take place. Recommended values are from 10k to 100k.

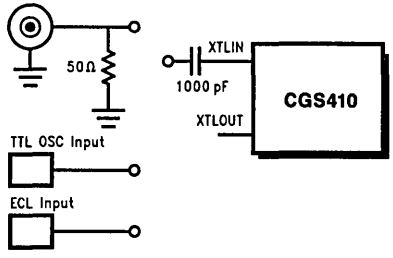
In systems where the lowest possible phase noise is required, a high-Q, external VCO may be implemented. An example is illustrated in *Figure 3-17.* Here the CGS410 provides the phase comparison, the first stage charge pump output, and the user programmable divider circuitry. In these types of configurations, EXTCLK can be driven with a small sinusoidal input. EXTCLK is capacitively coupled, while the VCO is DC terminated. An external OP-AMP such as National Semiconductor's LM324 provides the additional VCO voltage input range required. In this example, the OP-AMP is biased by the resistor divider. In most instances, the voltage present on the OP-AMP "+" input is half the OP-AMP source voltage. The OP-AMP feedback consists of a C/RC network which provides the voltage input characteristics of the VCO.



TL/F/11919–19

FIGURE 3-17. CGS410 Using an External Loop Filter and VCO

The designer may drive the CGS410 XTLIN in a variety of configurations. In most instances XTLIN is capacitively coupled to remove any DC effects from the source. Typical capacitor values will vary depending on the frequency and desired waveform at the XTLIN input. In most instances this value ranges from several hundred pF up to approximately 0.01f (See *Figure 3-18*).



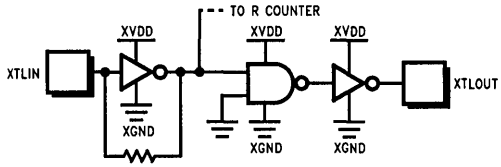
TL/F/11919–20

FIGURE 3-18. External XTLIN Drive Options

3.0 Circuit Operation (Continued)

3.12 INPUT/OUTPUT STRUCTURES

XTLIN/XTLOUT
(REF_SEL = 1)



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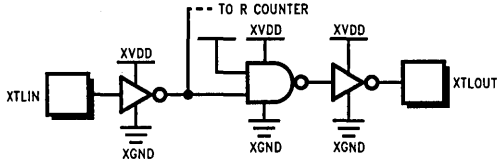
XTLIN/XTLOUT
(REF_SEL = 0)



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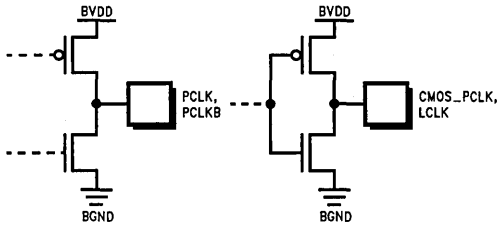

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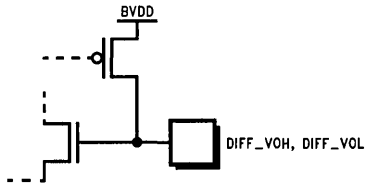

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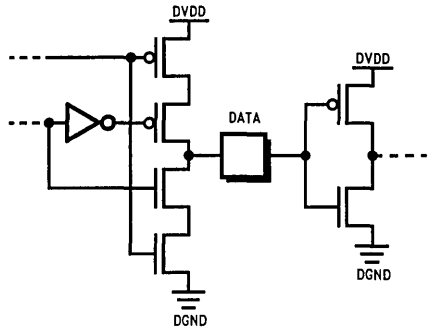

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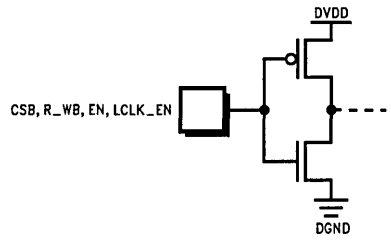

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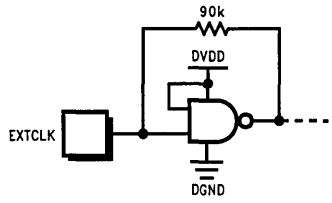

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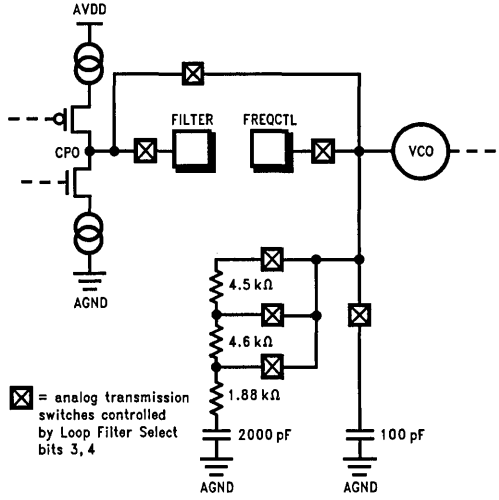

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4.0 Device Specifications

4.1 ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +6.3V
DC Input Voltage (V_{IN})	−1.5V to V_{DD} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{DD} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	+20 mA
DC Output Current, per pin (I_{DD})	+35 mA
DC V_{DD} or GND Current, per Pin (I_{DD})	+70 mA
Storage Temperature Range (T_{STG})	−165°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

4.2 RECOMMENDED OPERATING CONDITIONS

	Min	Max	Units
Supply Voltage (V_{DD})	4.75	5.25	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{DD}	V
Operating Temperature Range (T_A)	0	70	°C
VCO Frequency (f_{VCO})	65	135	MHz
Crystal Frequency (f_{XTL}) (Note 3)		35	MHz
Differential PCLK Frequency (f_{PCLK})		135	MHz
CMOS PCLK Frequency (f_{CMOS})		65	MHz
LCLK Frequency (f_{LCLK})		65	MHz

Note 3: Crystal should be parallel mode, fundamental type. This specification also applies to externally driven references.

4.3 DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5%, unless otherwise specified

Symbol	Parameter	Pin Name	Conditions	Min	Typ	Max	Units
V_{IH}	Minimum High Level Input Voltage	CSB, EXTCLK, DATA, EN, LCLK__EN, R__WB		2.0			V
		XTLIN	XVDD = 5.0V	3.5			V
V_{IL}	Minimum Low Level Input Voltage	CSB, EXTCLK, DATA, EN, LCLK__EN, R__WB				0.8	V
		XTLIN	XVDD = 5.0V			1.5	V
V_{OH}	Minimum High Level Output Voltage	DIFF V_{OH}	DIFF Level Bit = 0(1)		BVDD • 0.824		V
			DIFF Level Bit = 1(1)		BVDD • 0.825		V
		XTLOUT	I_{OH} = −400 μA	XVDD − 0.3			V
		DATA	I_{OH} = 6 mA	DVDD − 0.5			V
		CMOS__PCLK, LCLK	I_{OH} = 2 mA	BVDD − 0.3			V
V_{OL}	Maximum Low Level Output Voltage	DIFF__V_{OL}	DIFF Level Bit = 0(1)		BVDD • 0.642		V
			DIFF Level Bit = 1(2)		BVDD • 0.490		V
		XTLOUT	I_{OL} = 400 μA			0.3	V
		DATA	I_{OL} = 6 mA			0.5	V
		CMOS__PCLK, LCLK	I_{OL} = 2 mA			0.3	V
$V_{O(DIFF)}$	Output Voltage Swing PCLK, PCLKB		DIFF Level Bit = 0(3)		0.900		V
			DIFF Level Bit = 1(3)		1.650		V
I_{IN}	Maximum Input Current	CSB, DATA, EN, LCLK__EN, R__WB	V_{IN} = V_{DD} or GND, V_{IH} or V_{IL}			10	μA
		EXTCLK			100		μA
		XTLIN, FREQCTL	REF__SEL = 0		0.1	1.0	μA
I_{OZ}	Maximum Output TRI-STATE® Leakage Current	FILTER			0.1	1.0	μA
I_{SOURCE}	Charge Pump Source Current	FILTER	CPO__SEL = 0(4)	−15	−25	−35	μA
			CPO__SEL = 1(4)	−50	−75	−120	μA

4.0 Device Specifications (Continued)

4.3 DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5%, unless otherwise specified (Continued)

Symbol	Parameter	Pin Name	Conditions	Min	Typ	Max	Units
I_{SINK}	Charge Pump Sink Current	FILTER	CPO_SEL = 0(4)	15	25	35	µA
			CPO_SEL = 1(4)	50	75	120	µA
I_{DD}	Maximum Supply Current	DVDD, BVDD, XVDD, and AVDD	V_{DD} = 5.25V(5)		45		mA

Note 1: 50 Load to BVDD − 2V

Note 2: 50 Load to BVDD − 3V

Note 3: BVDD = 5.0V

Note 4: AVDD = 5.0V

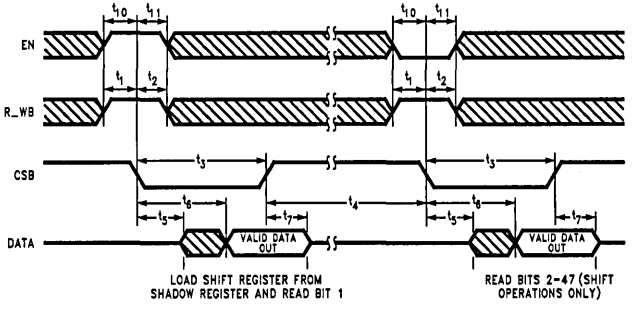
Note 5: PCLK and PCLKB terminated with 50 to BVDD − 2V
DIFF_VOH and DIFF_VOL terminated with 500 to BVDD − 2V
DIFF Level (Bit 0) = 0

4.4 AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_1	R_WB Setup to CSB Falling Edge		0			ns
t_2	R_WB Hold from CSB Falling Edge		10			ns
t_3	CSB low time (while writing data)		TBD	10		ns
t_4	CSB high time (while writing data)		TBD	10		ns
t_5	CSB asserted to Read Data Bus Driven (Note 1)		8			ns
t_6	CSB Asserted to Valid Read Data (Note 1)				40	ns
t_7	CSB Negated to Read Data TRI-STATE				15	ns
t_8	Write Data Setup to CSB Rising Edge		15			ns
t_9	Write Data hold from CSB rising edge		0			ns
t_{10}	EN Setup to CSB Falling Edge		0			ns
t_{11}	EN Hold from CSB Falling Edge		10			ns
t_{12}	LCLK_EN Setup to LCLK Rising Edge			6		ns
t_{13}	LCLK_EN Hold from LCLK Rising Edge			−4		ns
t_{14}	Skew from CMOS PLCK Rising Edge to LCLK Rising Edge			4		ns
t_{15}	Skew from CMOS PLCK Rising Edge to LCLK Falling Edge			5		ns
t_{16}	Skew from DIFF PCLK Rising Edge to LCLK Rising Edge			3		ns
t_{17}	Skew from DIFF PCLK rising edge to LCLK falling edge			4		ns

Note 1: C_L = 50 pF on DATA pin.

4.5 TIMING ISSUES



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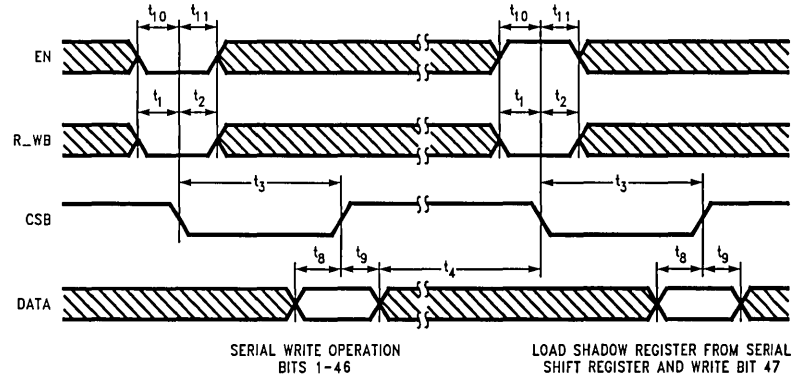
Note: In the system read cycle EN, R_WB and CSB are measured at 1.3V threshold voltage. DATA is a CMOS compatible output.

FIGURE 4-1. System Read Timing Specification

4.0 Device Specifications



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Note: In the system write cycle EN, R_WB and CSB are measured at 1.3V threshold voltage. DATA is a TTL compatible input.

FIGURE 4-2. System Write Timing Specification

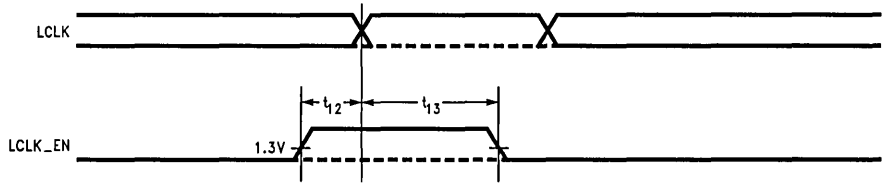

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FIGURE 4-3. LCLK_EN Timing Specification

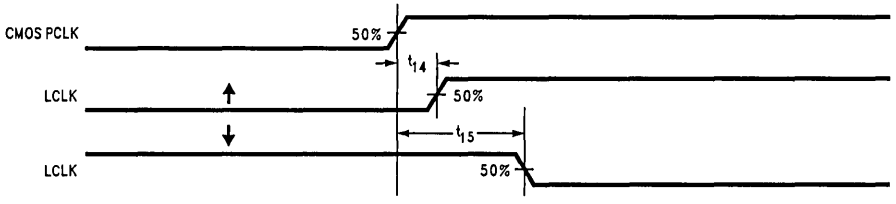

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FIGURE 4-4. CMOS PCLK Output Skew Timing Specification

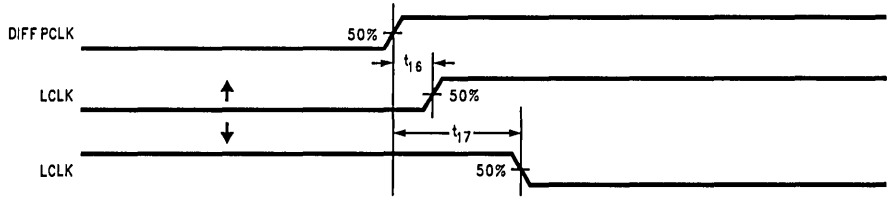

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FIGURE 4-5. DIFF PCLK Output Skew Timing Specification

National Semiconductor

LM1881 Video Sync Separator

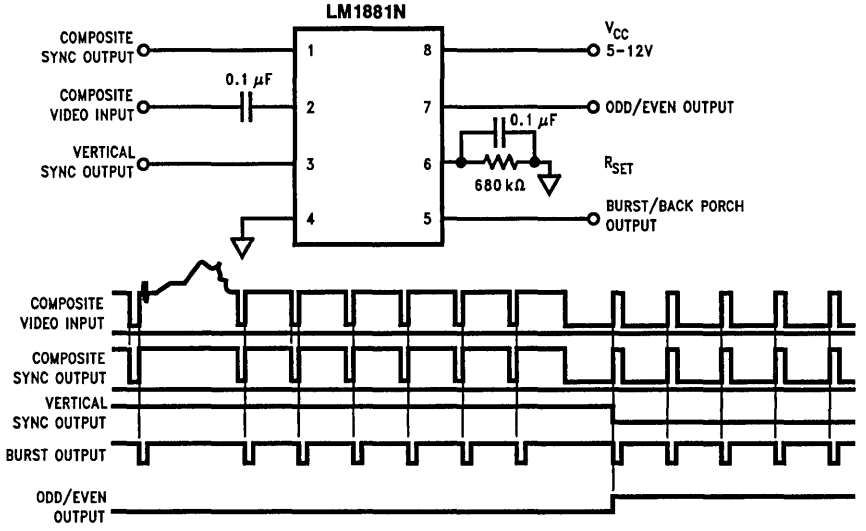
General Description

The LM1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL*, and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

Features

- AC coupled composite input signal
- >10 kΩ input resistance
- <10 mA power supply drain current
- Composite sync and vertical outputs
- Odd/even field output
- Burst gate/back porch output
- Horizontal scan rates to 150 kHz
- Edge triggered vertical output
- Default triggered vertical output for non-standard video signal (video games-home computers)

Connection Diagram



TL/H/9150-1

Order Number LM1881M or LM1881N
See NS Package Number M08A or N08E

*PAL in this datasheet refers to European broadcast TV standard "Phase Alternating Line", and not to Programmable Array Logic.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	13.2V
Input Voltage	3 Vpp (V_{CC} = 5V) 6 Vpp (V_{CC} ≥ 8V)
Output Sink Currents; Pins 1, 3, 5	5 mA
Output Sink Current; Pin 7	2 mA
Package Dissipation (Note 1)	1100 mW
Operating Temperature Range	0°C − 70°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility (Note 2)	2 kV
Soldering Information	
Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

V_{CC} = 5V; Rset = 680 kΩ; T_A = 25°C; Unless otherwise specified

Parameter	Conditions		Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Units (Limits)
Supply Current	Outputs at Logic 1	V_{CC} = 5V V_{CC} = 12V	5.2 5.5	10 12		mAmax mAmax
DC Input Voltage	Pin 2		1.5	1.3 1.8		Vmin Vmax
Input Threshold Voltage	Note 5		70	55 85		mVmin mVmax
Input Discharge Current	Pin 2; V_{IN} = 2V		11	6 16		μAmin μAmax
Input Clamp Charge Current	Pin 2; V_{IN} = 1V		0.8	0.2		mAmin
R_{SET} Pin Reference Voltage	Pin 6; Note 6		1.22	1.10 1.35		Vmin Vmax
Composite Sync. & Vertical Outputs	I_{OUT} = 40 μA; Logic 1	V_{CC} = 5V V_{CC} = 12V	4.5	4.0 11.0		Vmin Vmin
	I_{OUT} = 1.6 mA Logic 1	V_{CC} = 5V V_{CC} = 12V	3.6	2.4 10.0		Vmin Vmin
Burst Gate & Odd/Even Outputs	I_{OUT} = 40 μA; Logic 1	V_{CC} = 5V V_{CC} = 12V	4.5	4.0 11.0		Vmin Vmin
Composite Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 1		0.2	0.8		Vmax
Vertical Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 3		0.2	0.8		Vmax
Burst Gate Output	I_{OUT} = −1.6 mA; Logic 0; Pin 5		0.2	0.8		Vmax
Odd/Even Output	I_{OUT} = −1.6 mA; Logic 0; Pin 7		0.2	0.8		Vmax
Vertical Sync Width			230	190 300		μsmin μsmax
Burst Gate Width	2.7 kΩ from Pin 5 to V_{CC}		4	2.5 4.7		μsmin μsmax
Vertical Default Time	Note 7		65	32 90		μsmin μsmax

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 110° C/W, junction to ambient.

Note 2: ESD susceptibility test uses the "human body model, 100 pF discharged through a 1.5 kΩ resistor".

Note 3: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 4: Tested Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

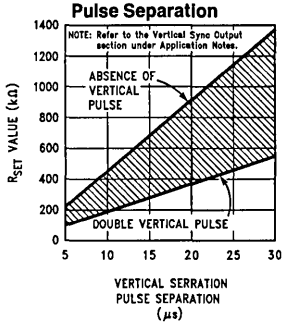
Note 5: Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.

Note 6: Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5, and 7) to the R_{SET} pin (Pin 6).

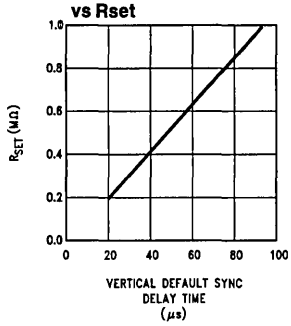
Note 7: Delay time between the start of vertical sync (at input) and the vertical output pulse.

Typical Performance Characteristics

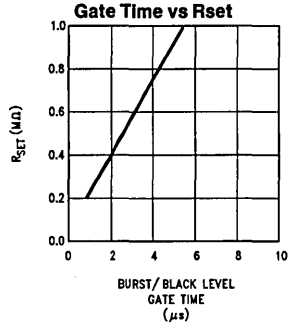
R_{set} Value Selection vs Vertical Serration Pulse Separation



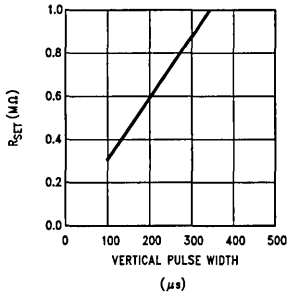
Vertical Default Sync Delay Time vs Rset



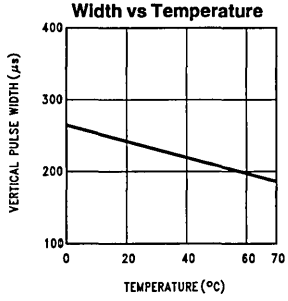
Burst/Black Level Gate Time vs Rset



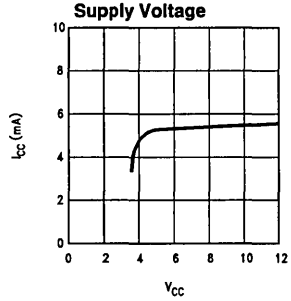
Vertical Pulse Width vs Rset



Vertical Pulse Width vs Temperature



Supply Current vs Supply Voltage



TL/H/9150-2

Application Notes

The LM1881 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5V (p-p) to 2V (p-p) can be accommodated. The LM1881 operates from a single supply voltage between 5V DC and 12V DC. The only required external components beside power supply and set current decoupling are the input coupling capacitor and a single resistor that sets internal current levels, allowing the LM1881 to be adjusted for source signals with line scan frequencies differing from 15.734 kHz. Four major sync signals are available from the I/C: composite sync including both horizontal and vertical scan timing information; a vertical sync pulse; a burst gate or back porch clamp pulse; and an odd/even output. The odd/even output level identifies which video field of an interlaced video source is present at the input. The outputs from the LM1881 can be used to gen-lock video camera/VTR signals with graphics sources, provide identification of video fields for memory storage, recover suppressed or contaminated sync signals, and provide timing references for the extraction of coded or uncoded data on specific video scan lines.

To better understand the LM1881 timing information and the type of signals that are used, refer to *Figure 2(a–e)* which shows a portion of the composite video signal from the end of one field through the beginning of the next field.

COMPOSITE SYNC OUTPUT

The composite sync output, *Figure 2(b)*, is simply a reproduction of the signal waveform below the composite video black level, with the video completely removed. This is obtained by clamping the video signal sync tips to 1.5V DC at Pin 2 and using a comparator threshold set just above this voltage to strip the sync signal, which is then buffered out to Pin 1. The threshold separation from the clamped sync tip is nominally 70 mV which means that for the minimum input level of 0.5V (p-p), the clipping level is close to the halfway point on the sync pulse amplitude (shown by the dashed line on *Figure 2(a)*). This threshold separation is independent of the signal amplitude, therefore, for a 2V (p-p) input the clipping level occurs at 11% of the sync pulse amplitude. The charging current for the input coupling capacitor is 0.8 mA, whereas the discharge current is only 11 μA, typically. This allows relatively small capacitor values to be used—0.1 μF is generally recommended.

Normally the signal source for the LM1881 is assumed to be clean and relatively noise-free, but some sources may have excessive video peaking, causing high frequency video and chroma components to extend below the black level reference. Some video discs keep the chroma burst pulse present throughout the vertical blanking period so that the burst actually appears on the sync tips for three line periods instead of at black level. A clean composite sync signal can be generated from these sources by filtering the input signal. When the source impedance is low, typically 75Ω, a 620Ω resistor in series with the source and a 510 pF capacitor to ground will form a low pass filter with a corner frequency of 500 kHz. This bandwidth is more than sufficient to pass the sync pulse portion of the waveform; however, any subcarrier content in the signal will be attenuated by almost 18 dB, effectively taking it below the comparator threshold. Filtering will also help if the source is contaminated with thermal noise. The output waveforms will become delayed from between 40 ns to as much as 200 ns due to this filter. This much delay will not usually be significant but it does contribute to the sync delay produced by any additional signal processing. Since the original video may also undergo processing, the need for time delay correction will depend on the total system, not just the sync stripper.

VERTICAL SYNC OUTPUT

A vertical sync output is derived by internally integrating the composite sync waveform *(Figure 3)*. To understand the generation of the vertical sync pulse, refer to the lower left hand section *Figure 3*. Note that there are two comparators in the section. One comparator has an internally generated voltage reference called V_1 going to one of its inputs. The other comparator has an internally generated voltage reference called V_2 going to one of its inputs. Both comparators have a common input at their noninverting input coming from the internal integrator. The internal integrator is used for integrating the composite sync signal. This signal comes from the input side of the composite sync buffer and are **positive** going sync pulses. The capacitor to the integrator is internal to the LM1881. The capacitor charge current is set by the value of the external resistor R_{set}. The output of the integrator is going to be at a low voltage during the normal horizontal lines because the integrator has a very short time to charge the capacitor, which is during the horizontal sync period. The equalization pulses will keep the output voltage of the integrator at about the same level, below the V_1. During the vertical sync period the narrow going positive pulses shown in *Figure 2* is called the serration pulse. The wide negative portion of the vertical sync period is called the vertical sync pulse. At the start of the vertical sync period, before the first Serration pulse occurs, the integrator now charges the capacitor to a much higher voltage. At the first serration pulse the integrator output should be between V_1 and V_2. This would give a high level at the output of the comparator with V_1 as one of its inputs. This high is clocked into the "D" flip-flop by the falling edge of the serration pulse (remember the sync signal is inverted in this section of the LM1881). The "Q" output of the "D" flip-flop goes through the OR gate, and sets the R/S flip-flop. The output of the R/S flip-flop enables the internal oscillator and also clocks the ODD/EVEN "D" flip-flop. The ODD/EVEN field pulse operation is covered in the next section. The output of the oscillator goes to a divide by 8 circuit, thus resetting the R/S flip-flop after 8 cycles of the oscillator. The frequency of the oscillator is established by the internal capacitor going to the oscillator and the external R_{set}. The "$\overline{Q}$" output of the R/S flip-flop goes to pin 3 and is the actual vertical sync output of the LM1881. By clocking the "D" flip-flop at the start of the first serration pulse means that the vertical sync output pulse starts at this point in time and lasts for eight cycles of the internal oscillator as shown in *Figure 2*.

How R_{set} affects the integrator and the internal oscillator is shown under the Typical Performance Characteristics. The first graph is "R_{set} Value Selection vs Vertical Serration Pulse Separation". For this graph to be valid, the vertical sync pulse should last for at least 85% of the horizontal half line (47% of a full horizontal line). A vertical sync pulse from any standard should meet this requirement; both NTSC and PAL do meet this requirement (the serration pulse is the remainder of the period, 10% to 15% of the horizontal

Application Notes (Continued)

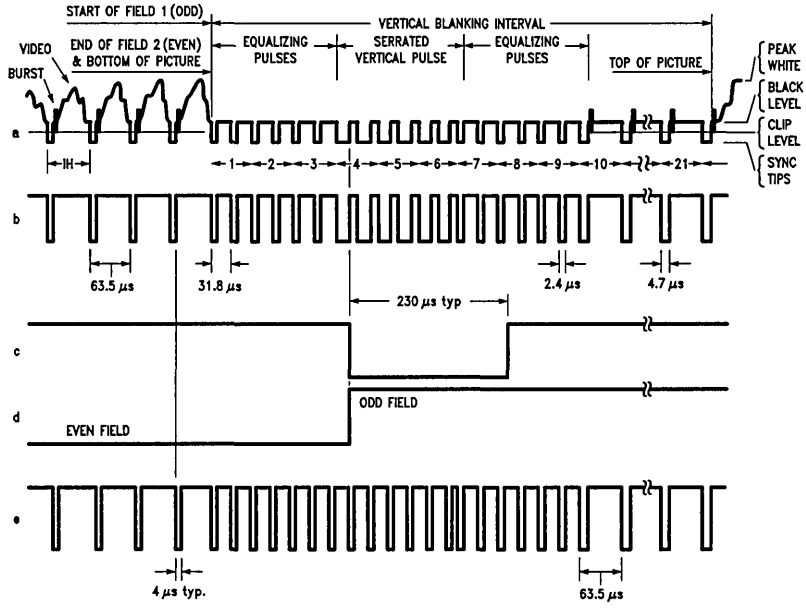


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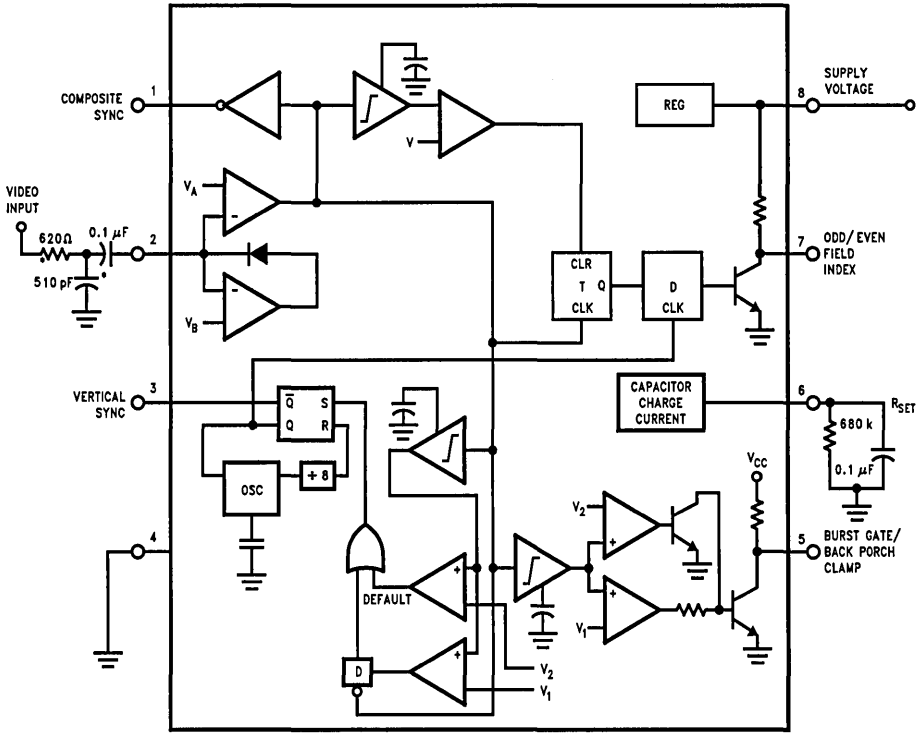
FIGURE 2. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp



*Components Optional, See Text

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FIGURE 3

Application Notes (Continued)

half line). Remember this pulse is a positive pulse at the integrator but negative in *Figure 2*. This graph shows how long it takes the integrator to charge its internal capacitor above V_1.

WITH R_{set} too large the charging current of the integrator will be too small to charge the capacitor above V_1, thus there will be no vertical synch output pulse. As mentioned above, R_{set} also sets the frequency of the internal oscillator. If the oscillator runs too fast its eight cycles will be shorter than the vertical sync portion of the composite sync. Under this condition another vertical sync pulse can be generated on one of the later serration pulses after the divide by 8 circuit resets the R/S flip-flop. The first graph also shows the minimum R_{set} necessary to prevent a double vertical pulse, assuming that the serration pulses last for only three full horizontal line periods (six serration pulses for NTSC). The actual pulse width of the vertical sync pulse is shown in the "Vertical Pulse Width vs R_{set}" graph. Using NTSC as an example, lets see how these two graphs relate to each other. The Horizontal line is 64 μs long, or 32 μs for a horizontal half line. Now round this off to 30 μs. In the "R_{set} Value Selection vs Vertical Serration Pulse Separation" graph the minimum resistor value for 30 μs serration pulse separation is about 550 kΩ. Going to the "Vertical Pulse Width vs R_{set}" graph one can see that 550 kΩ gives a vertical pulse width of about 180 μs, the total time for the vertical sync period of NTSC (3 horizontal lines). A 550 kΩ will set the internal oscillator to a frequency such that eight cycles gives a time of 180 μs, just long enough to prevent a double vertical sync pulse at the vertical sync output of the LM1881.

The LM1881 also generates a default vertical sync pulse when the vertical sync period is unusually long and has no serration pulses. With a very long vertical sync time the integrator has time to charge its internal capacitor above the voltage level V_2. Since there is no falling edge at the end of a serration pulse to clock the "D" flip-flop, the only high signal going to the OR gate is from the default comparator when output of the integrator reaches V_2. At this time the R/S flip-flop is toggled by the default comparator, starting the vertical sync pulse at pin 3 of the LM1881. If the default vertical sync period ends before the end of the input vertical sync period, then the falling edge of the vertical sync (positive pulse at the "D" flip-flop) will clock the high output from the comparator with V_1 as a reference input. This will retrigger the oscillator, generating a second vertical sync output pulse. The "Vertical Default Sync Delay Time vs R_{set}" graph shows the relationship between the R_{set} value and the delay time from the start of the vertical sync period before the default vertical sync pulse is generated. Using the NTSC example again the smallest resistor for R_{set} is 500 kΩ. The vertical default time delay is about 50 μs, much longer than the 30 μs serration pulse spacing.

A common question is how can one calculate the required R_{set} with a video timing standard that has no serration pulses during the vertical blanking. If the default vertical sync is to be used this is a very easy task. Use the "Vertical Default Sync Delay Time vs R_{set}" graph to select the necessary R_{set} to give the desired delay time for the vertical sync output signal. If a second pulse is undesirable, then check the "Vertical Pulse Width vs R_{set}" graph to make sure the vertical output pulse will extend beyond the end of the input vertical sync period. In most systems the end of the vertical sync period may be very accurate. In this case the preferred design may be to start the vertical sync pulse at the end of the vertical sync period, similar to starting the vertical sync pulse after the first serration pulse. A VGA standard is to be used as an example to show how this is done. In this standard a horizontal line is 32 μs long. The vertical sync period is two horizontal lines long, or 64 μs. The vertical default sync delay time **must be longer** than the vertical sync period of 64 μs. In this case R_{set} must be larger than 680 kΩ. R_{set} must still be small enough for the output of the integrator to reach V_1 before the end of the vertical period of the input pulse. The first graph can be used to confirm that R_{set} is small enough for the integrator. Instead of using the vertical serration pulse separation, use the actual pulse width of the vertical sync period, or 64 μs in this example. This graph is linear, meaning that a value as large as 2.7 MΩ can be used for R_{set} (twice the value as the maximum at 30 μs). Due to leakage currents it is advisable to keep the value of R_{set} under 2.0 MΩ. In this example a value of 1.0 MΩ is selected, well above the minimum of 680 kΩ. With this value for R_{set} the pulse width of the vertical sync output pulse of the LM1881 is about 340 μs.

ODD/EVEN FIELD PULSE

An unusual feature of LM1881 is an output level from Pin 7 that identifies the video field present at the input to the LM1881. This can be useful in frame memory storage applications or in extracting test signals that occur only in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—i.e., at the bottom of the picture. This is called the "odd field" or "field 1". The "even field" or "field 2" has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. *Figure 2(a)* shows the end of the even field and the start of the odd field.

To detect the odd/even fields the LM1881 again integrates the composite sync waveform *(Figure 3)*. A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flipflop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this

Application Notes (Continued)

threshold from being reached and the Q output of the flip-flop is toggled with each equalizing pulse. Since the half line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd/even field index is generated. Pin 7 remains low during the even field and high during the odd field.

BURST/BACKPORCH OUTPUT PULSE

In a composite video signal, the chroma burst is located on the backporch of the horizontal blanking period. This period, approximately 4.8 μs long, is also the black level reference for the subsequent video scan line. The LM1881 generates a pulse at Pin 5 that can be used either to retrieve the chroma burst from the composite video signal (thus providing a subcarrier synchronizing signal) or as a clamp for the DC restoration of the video waveform. This output is obtained simply by charging an internal capacitor starting on the trailing edge of the horizontal sync pulses. Simultaneously the output of Pin 5 is pulled low and held until the capacitor charge circuit times out—4 μs later. A shorter output burst gate pulse can be derived by differentiating the burst output using a series C-R network. This may be necessary in applications which require high horizontal scan rates in combination with normal (60–120 Hz) vertical scan rates.

APPLICATIONS

Apart from extracting a composite sync signal free of video information, the LM1881 outputs allow a number of interesting applications to be developed. As mentioned above, the burst gate/backporch clamp pulse allows DC restoration of the original video waveform for display or remodulation on an R.F. carrier, and retrieval of the color burst for color synchronization and decoding into R.G.B. components. For frame memory storage applications, the odd/even field level allows identification of the appropriate field ensuring the correct read or write sequence. The vertical pulse output is particularly useful since it begins at a precise time—the rising edge of the first vertical serration in the sync waveform. This means that individual lines within the vertical blanking period (or anywhere in the active scan line period) can easily be extracted by counting the required number of transitions in the composite sync waveform following the start of the vertical output pulse.

The vertical blanking interval is proving popular as a means to transmit data which will not appear on a normal T.V. receiver screen. Data can be inserted beginning with line 10 (the first horizontal scan line on which the color burst appears) through to line 21. Usually lines 10 through 13 are not used which leaves lines 14 through 21 for inserting signals, which may be different from field to field. In the U.S., line 19 is normally reserved for a vertical interval reference signal (VIRS) and line 21 is reserved for closed caption data for the hearing impaired. The remaining lines are used in a number of ways. Lines 17 and 18 are frequently used during studio processing to add and delete vertical interval test signals (VITS) while lines 14 through 18 and line 20 can be used for Videotex/Teletext data. Several institutions are proposing to transmit financial data on line 17 and cable systems use the available lines in the vertical interval to send decoding data for descrambler terminals.

Since the vertical output pulse from the LM1881 coincides with the leading edge of the first vertical serration, sixteen positive or negative transitions later will be the start of line 14 in either field. At this point simple counters can be used to select the desired line(s) for insertion or deletion of data.

VIDEO LINE SELECTOR

The circuit in *Figure 4* puts out a single video line according to the binary coded information applied to line select bits b0–b7. A line is selected by adding two to the desired line number, converting to a binary equivalent and applying the result to the line select inputs. The falling edge of the LM1881's vertical pulse is used to load the appropriate number into the counters (MM74C193N) and to set a start count latch using two NAND gates. Composite sync transitions are counted using the borrow out of the desired number of counters. The final borrow out pulse is used to turn on the analog switch (CD4066BC) during the desired line. The falling edge of this signal also resets the start count latch, thereby terminating the counting.

The circuit, as shown, will provide a single line output for each field in an interlaced video system (television) or a single line output in each frame for a non-interlaced video system (computer monitor). When a particular line in only one field of an interlaced video signal is desired, the odd/even field index output must be used instead of the vertical output pulse (invert the field index output to select the odd field). A single counter is needed for selecting lines 3 to 14; two counters are needed for selecting lines 15 to 253; and three counters will work for up to 2046 lines. An output buffer is required to drive low impedance loads.

MULTIPLE CONTIGUOUS VIDEO LINE SELECTOR WITH BLACK LEVEL RESTORATION

The circuit in *Figure 5* will select a number of adjoining lines starting with the line selected as in the previous example. Additional counters can be added as described previously for either higher starting line numbers or an increased number of contiguous output lines. The back porch pulse output of the LM1881 is used to gate the video input's black level through a low pass filter (10 kΩ, 10 μF) providing black level restoration at the video output when the output selected line(s) is not being gated through.

Typical Applications

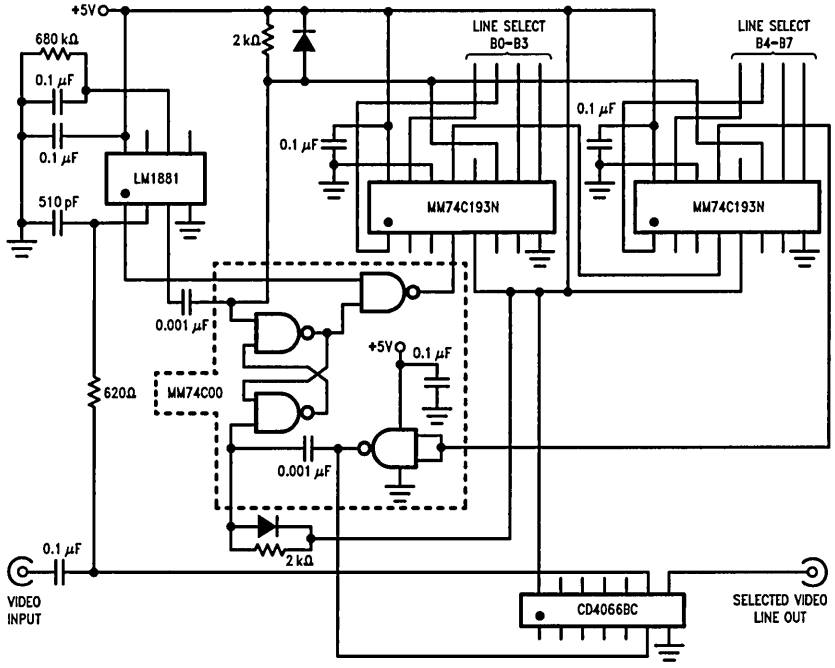

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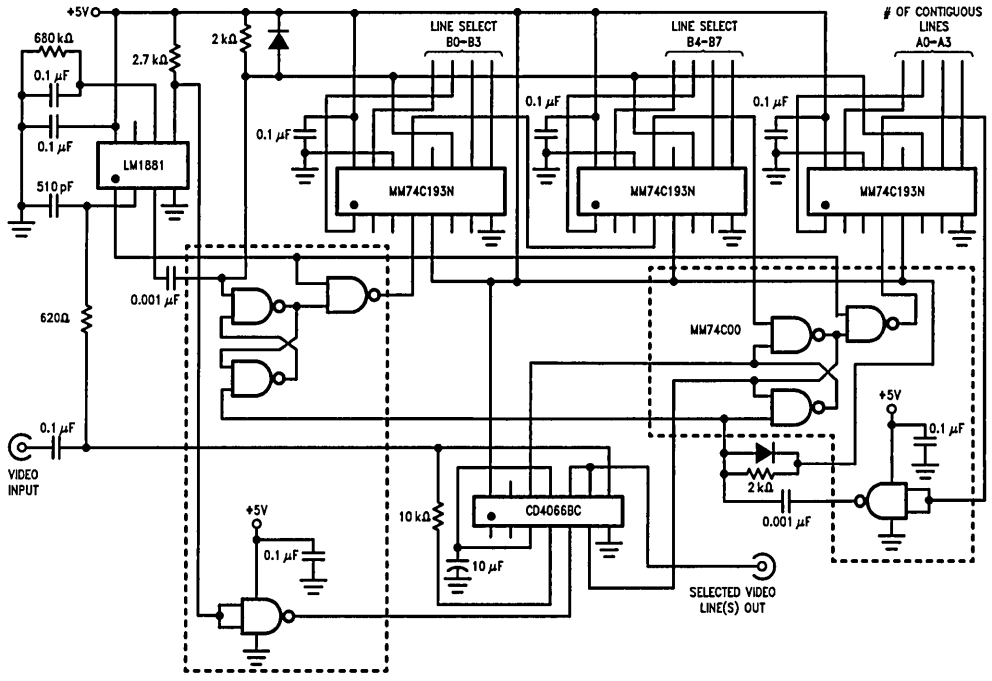
FIGURE 4. Video Line Selector



TL/H/9150–6

FIGURE 5. Multiple Contiguous Video Line Selector With Black Level Restoration

National Semiconductor

54ACT/74ACT715•LM1882
54ACT/74ACT715-R•LM1882-R
Programmable Video Sync Generator

General Description

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R are 20-pin TTL-input compatible devices capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The devices are capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal or vertical gating pulses, cursor position or vertical interrupt signal.

These devices make no assumptions concerning the system architecture. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

The 'ACT715/LM1882 is mask programmed to default to a Clock Disable state. Bit 10 of the Status Register, Register 0, defaults to a logic "0". This facilitates (re)programming before operation.

The 'ACT715-R/LM1882-R is the same as the 'ACT715/LM1882 in all respects except that the 'ACT715-R/LM1882-R is mask programmed to default to a Clock Enabled state. Bit 10 of the Status Register defaults to a logic "1". Although completely (re)programmable, the 'ACT715-R/LM1882-R version is better suited for applications using the default 14.31818 MHz RS-170 register values. This feature allows power-up directly into operation, following a single CLEAR pulse.

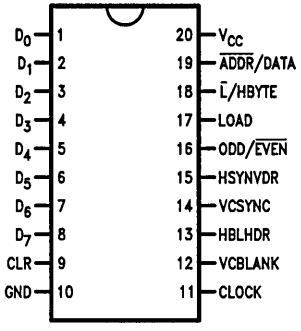
Features

- Maximum Input Clock Frequency > 130 MHz
- Interlaced and non-interlaced formats available
- Separate or composite horizontal and vertical Sync and Blank signals available
- Complete control of pulse width via register programming
- All inputs are TTL compatible
- 8 mA drive on all outputs
- Default RS170/NTSC values mask programmed into registers
- 4 KV minimum ESD immunity
- 'ACT715-R/LM1882-R is mask programmed to default to a Clock Enable state for easier start-up into 14.31818 MHz RS170 timing

Ordering Code: See Section 5

Connection Diagrams

Pin Assignment for DIP and SOIC



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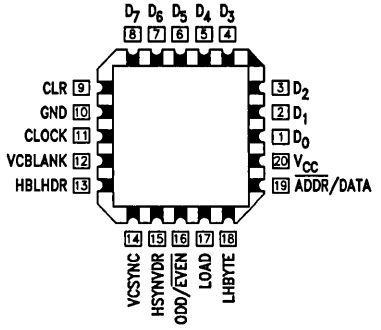
Order Number LM1882CN or LM1882CM
For Default RS-170, Order Number LM1882-RCN or LM1882-RCM

Pin Assignment for LCC



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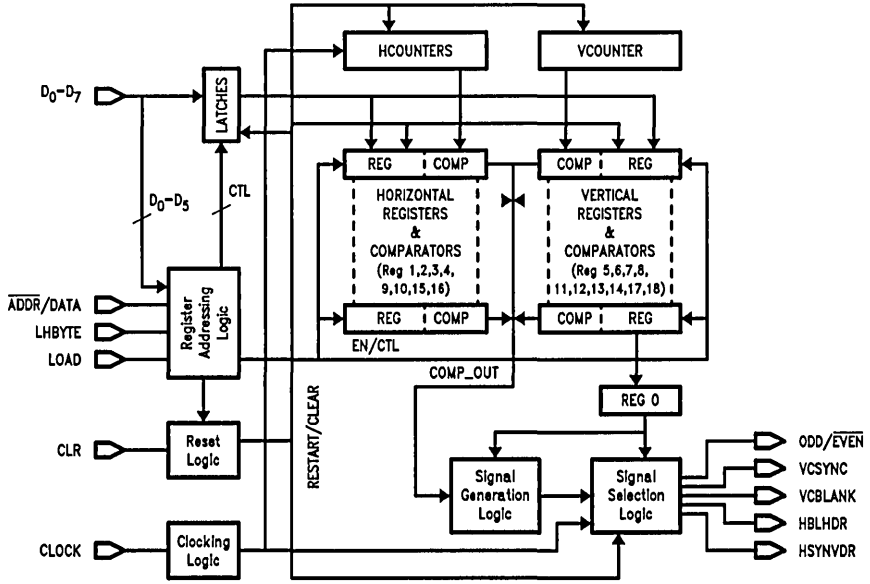
Logic Block Diagram



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Pin Description

There are a Total of 13 inputs and 5 outputs on the 'ACT715/LM1882.

Data Inputs D0–D7: The Data Input pins connect to the Address Register and the Data Input Register.

ADDR/DATA: The ADDR/DATA signal is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus.

L/HBYTE: The L/HBYTE signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the Data Registers. A 1 on this pin when an ADDR/DATA is a 0 enables Auto-Load Mode.

LOAD: The LOAD control pin loads data into the Address or Data Registers on the rising edge. ADDR/DATA and L/HBYTE data is loaded into the device on the falling edge of the LOAD. The LOAD pin has been implemented as a Schmitt trigger input for better noise immunity.

CLOCK: System CLOCK input from which all timing is derived. The clock pin has been implemented as a Schmitt trigger for better noise immunity. The CLOCK and the LOAD signal are asynchronous and independent. Output state changes occur on the falling edge of CLOCK.

CLR: The CLEAR pin is an asynchronous input that initializes the device when it is HIGH. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators and registers. The CLEAR pin has been implemented as a Schmitt trigger for better noise immunity. A CLEAR pulse should be asserted by the user immediately after power-up to ensure proper initialization of the registers—even if the user plans to (re)program the device.

Note: A CLEAR pulse will disable the CLOCK on the 'ACT715/LM1882 and will enable the CLOCK on the 'ACT715-R/LM1882-R.

ODD/EVEN: Output that identifies if display is in odd (HIGH) or even (LOW) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation this output is always HIGH. Data can be serially scanned out on this pin during Scan Mode.

VCSYNC: Outputs Vertical or Composite Sync signal based on value of the Status Register. Equalization and Serration pulses will (if enabled) be output on the VCSYNC signal in composite mode only.

VCBLANK: Outputs Vertical or Composite Blanking signal based on value of the Status Register.

HBLHDR: Outputs Horizontal Blanking signal, Horizontal Gating signal or Cursor Position based on value of the Status Register.

HSYNVDR: Outputs Horizontal Sync signal, Vertical Gating signal or Vertical Interrupt signal based on value of Status Register.

Register Description

All of the data registers are 12 bits wide. Width's of all pulses are defined by specifying the start count and end count of all pulses. Horizontal pulses are specified with-respect-to the number of clock pulses per line and vertical pulses are specified with-respect-to the number of lines per frame.

REG0—STATUS REGISTER

The Status Register controls the mode of operation, the signals that are output and the polarity of these outputs. The default value for the Status Register is 0 (000 Hex) for the 'ACT715/LM1882 and is "512" (200 Hex) for the 'ACT715-R/LM1882-R.

Register Description (Continued)

Bits 0–2

B_2	B_1	B_0	VCBLANK	VCSYNC	HBLHDR	HSYNVDR
0	0	0	CBLANK	CSYNC	HGATE	VGATE
(DEFAULT)						
0	0	1	VBLANK	CSYNC	HBLANK	VGATE
0	1	0	CBLANK	VSYNC	HGATE	HSYNC
0	1	1	VBLANK	VSYNC	HBLANK	HSYNC
1	0	0	CBLANK	CSYNC	CURSOR	VINT
1	0	1	VBLANK	CSYNC	HBLANK	VINT
1	1	0	CBLANK	VSYNC	CURSOR	HSYNC
1	1	1	VBLANK	VSYNC	HBLANK	HSYNC

Bits 3–4

B_4	B_3	Mode of Operation
0	0	Interlaced Double Serration and
(DEFAULT)		Equalization
0	1	Non Interlaced Double Serration
1	0	Illegal State
1	1	Non Interlaced Single Serration and Equalization

Double Equalization and Serration mode will output equalization and serration pulses at twice the HSYNC frequency (i.e., 2 equalization or serration pulses for every HSYNC pulse). Single Equalization and Serration mode will output an equalization or serration pulse for every HSYNC pulse. In Interlaced mode equalization and serration pulses will be output during the VBLANK period of every odd and even field. Interlaced Single Equalization and Serration mode is not possible with this part.

Bits 5–8

Bits 5 through 8 control the polarity of the outputs. A value of zero in these bit locations indicates an output pulse active LOW. A value of 1 indicates an active HIGH pulse.

B5— VCBLANK Polarity

B6— VCSYNC Polarity

B7— HBLHDR Polarity

B8— HSYNVDR Polarity

Bits 9–11

Bits 9 through 11 enable several different features of the device.

B9— Enable Equalization/Serration Pulses (0)
Disable Equalization/Serration Pulses (1)

B10— Disable System Clock (0)
Enable System Clock (1)

Default values for B10 are "0" in the 'ACT715/LM1882 and "1" in the 'ACT715-R/LM1882-R.

B11— Disable Counter Test Mode (0)
Enable Counter Test Mode (1)

This bit is not intended for the user but is for internal testing only.

HORIZONTAL INTERVAL REGISTERS

The Horizontal Interval Registers determine the number of clock cycles per line and the characteristics of the Horizontal Sync and Blank pulses.

REG1— Horizontal Front Porch

REG2— Horizontal Sync Pulse End Time

REG3— Horizontal Blanking Width

REG4— Horizontal Interval Width # of Clocks per Line

VERTICAL INTERVAL REGISTERS

The Vertical Interval Registers determine the number of lines per frame, and the characteristics of the Vertical Blank and Sync Pulses.

REG5— Vertical Front Porch

REG6— Vertical Sync Pulse End Time

REG7— Vertical Blanking Width

REG8— Vertical Interval Width # of Lines per Frame

EQUALIZATION AND SERRATION PULSE SPECIFICATION REGISTERS

These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.

REG 9— Equalization Pulse Width End Time

REG10— Serration Pulse Width End Time

REG11— Equalization/Serration Pulse Vertical Interval Start Time

REG12— Equalization/Serration Pulse Vertical Interval End Time

VERTICAL INTERRUPT SPECIFICATION REGISTERS

These Registers determine the width of the Vertical Interrupt signal if used.

REG13— Vertical Interrupt Activate Time

REG14— Vertical Interrupt Deactivate Time

CURSOR LOCATION REGISTERS

These 4 registers determine the cursor position location, or they generate separate Horizontal and Vertical Gating signals.

REG15— Horizontal Cursor Position Start Time

REG16— Horizontal Cursor Position End Time

REG17— Vertical Cursor Position Start Time

REG18— Vertical Cursor Position End Time

Signal Specification

HORIZONTAL SYNC AND BLANK SPECIFICATIONS

All horizontal signals are defined by a start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. All values of the horizontal timing registers are referenced to the falling edge of the Horizontal Blank signal (see *Figure 1*). Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Horizontal Blank reference pulse, edges referenced to this first Horizontal edge are n + 1 CLOCKs away, where "n" is the width of the timing in question. Registers 1, 2, and 3 are programmed in this manner. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This

Signal Specification (Continued)

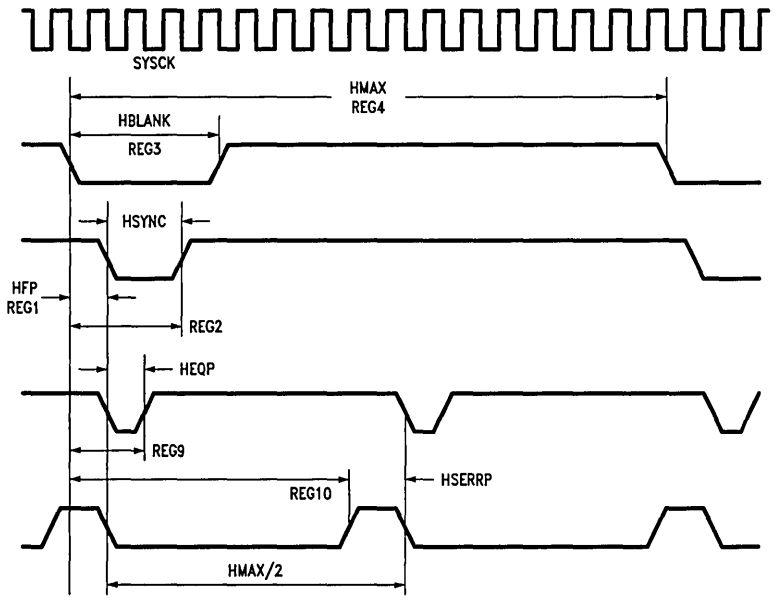

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FIGURE 1. Horizontal Waveform Specification

limitation is imposed because during interlace operation this value is internally divided by 2 in order to generate serration and equalization pulses at 2 × the horizontal frequency. Horizontal signals will change on the falling edge of the CLOCK signal. Signal specifications are shown below.

Horizontal Period (HPER) = REG(4) × ckper

Horizontal Blanking Width = [REG(3) − 1] × ckper

Horizontal Sync Width = [REG(2) − REG(1)] × ckper

Horizontal Front Porch = [REG(1) − 1] × ckper

VERTICAL SYNC AND BLANK SPECIFICATION

All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the Vertical Registers in terms of lines per field. Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Vertical Blank (first Horizontal Blank) reference pulse, edges referenced to this first edge are n + 1 lines away, where "n" is the width of the timing in question. Registers 5, 6, and 7 are programmed in this manner. Also, in the interlaced mode, vertical timing is based on half-lines. Therefore registers 5, 6, and 7 must contain a value twice the total horizontal (odd and even) plus 1 (as described above). In non-interlaced mode, all vertical timing is based on whole-lines. Register 8 is always based on whole-lines and does not add 1 for the first clock. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical Blank will change on the leading edge of HBLANK. Vertical Sync will change on the leading edge of HSYNC. (See *Figure 2A.*)

Vertical Frame Period (VPER) = REG(8) × hper

Vertical Field Period (VPER/n) = REG(8) × hper/n

Vertical Blanking Width = [REG(7) − 1] × hper/n

Vertical Syncing Width = [REG(6) − REG(5)] × hper/n

Vertical Front Porch = [REG(5) − 1] × hper/n

where n = 1 for noninterlaced
n = 2 for interlaced

COMPOSITE SYNC AND BLANK SPECIFICATION

Composite Sync and Blank signals are created by logically ANDing (ORing) the active LOW (HIGH) signals of the corresponding vertical and horizontal components of these signals. The Composite Sync signal may also include serration and/or equalization pulses. The Serration pulse interval occurs in place of the Vertical Sync interval. Equalization pulses occur preceding and/or following the Serration pulses. The width and location of these pulses can be programmed through the registers shown below. (See *Figure 2B.*)

Horizontal Equalization PW = [REG(9) − REG(1)] × ckper
REG 9 = (HFP) + (HEQP) + 1

Horizontal Serration PW = [REG(4)/n + REG(1) − REG(10)] × ckper
REG 10 = (HFP) + (HPER/2) − (HSERR) + 1

Where n = 1 for noninterlaced single serration/equalization
n = 2 for noninterlaced double serration/equalization
n = 2 for interlaced operation

Signal Specification (Continued)

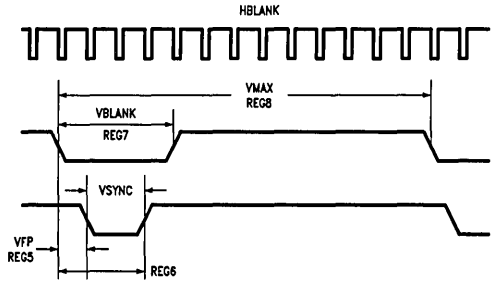

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FIGURE 2A. Vertical Waveform Specification

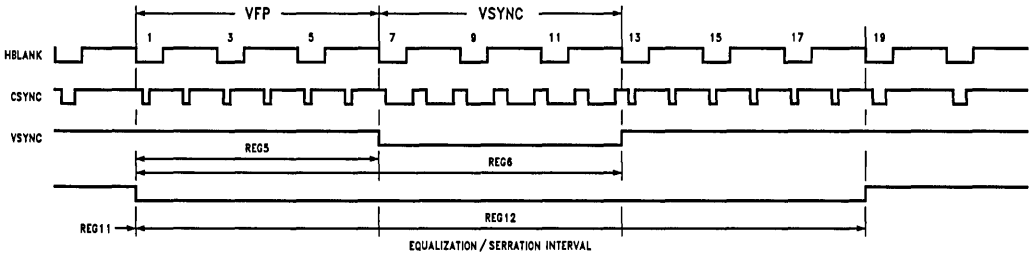

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FIGURE 2B. Equalization/Serration Interval Programming

HORIZONTAL AND VERTICAL GATING SIGNALS

Horizontal Drive and Vertical Drive outputs can be utilized as general purpose Gating Signals. Horizontal and Vertical Gating Signals are available for use when Composite Sync and Blank signals are selected and the value of Bit 2 of the Status Register is 0. The Vertical Gating signal will change in the same manner as that specified for the Vertical Blank.

Horizontal Gating Signal Width = [REG(16) − REG(15)] × ckper

Vertical Gating Signal Width = [REG(18) − REG(17)] × hper

CURSOR POSITION AND VERTICAL INTERRUPT

The Cursor Position and Vertical Interrupt signal are available when Composite Sync and Blank signals are selected and Bit 2 of the Status Register is set to the value of 1. The Cursor Position generates a single pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active LOW (HIGH) signals specified by the registers used for generating Horizontal and Vertical Gating signals. The Vertical Interrupt signal generates a pulse during the vertical interval specified. The Vertical Interrupt signal will change in the same manner as that specified for the Vertical Blanking signal.

Horizontal Cursor Width = [REG(16) − REG(15)] × ckper

Vertical Cursor Width = [REG(18) − REG(17)] × hper

Vertical Interrupt Width = [REG(14) − REG(13)] × hper

Addressing Logic

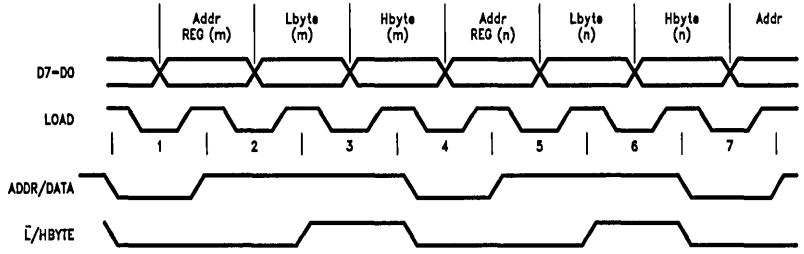
The register addressing logic is composed of two blocks of logic. The first is the address register and counter (ADDRCNTR), and the second is the address decode (ADDRDEC).

ADDRCNTR LOGIC

Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 load cycles (19 address and 38 data cycles). Auto Addressing requires that only the initial register value be specified. The Auto Load sequence would require only 39 load cycles to completely program all registers (1 address and 38 data cycles). In the auto load sequence the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the time the High Byte is written the address counter is incremented by 1. The counter has been implemented to loop on the initial value loaded into the address register. For example: If a value of 0 was written into the address register then the counter would count from 0 to 18 before resetting back to 0. If a value of 15 was written into the address register then the counter would count from 15 to 18 before looping back to 15. If a value greater than or equal to 18 is placed into the address register the counter will continuously loop on this value. Auto addressing is initiated on the falling edge of LOAD when ADDRDATA is 0 and LHBYTE is 1. Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDRDATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto Incrementing is disabled on the falling edge of LOAD after ADDRDATA and LHBYTE goes low.

Manual Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Manual Addressing	Load Address m
2	Enable Lbyte Data Load	Load Lbyte m
3	Enable Hbyte Data Load	Load Hbyte m
4	Enable Manual Addressing	Load Address n
5	Enable Lbyte Data Load	Load Lbyte n
6	Enable Hbyte Data Load	Load Hbyte n



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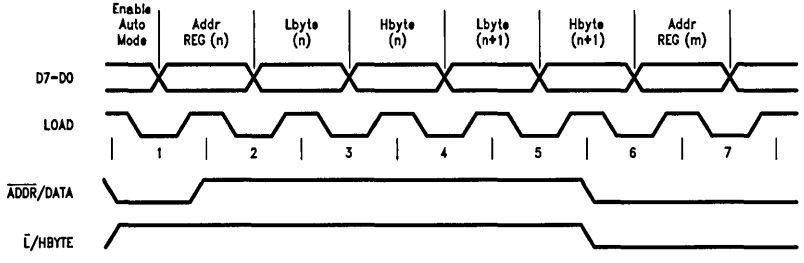
Auto Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Auto Addressing	Load Start Address n
2	Enable Lbyte Data Load	Load Lbyte (n)
3	Enable Hbyte Data Load	Load Hbyte (n); Inc Counter
4	Enable Lbyte Data Load	Load Lbyte (n+1)
5	Enable Hbyte Data Load	Load Hbyte (n+1); Inc Counter
6	Enable Manual Addressing	Load Address



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Addressing Logic (Continued)

ADDRDEC LOGIC

The ADDRDEC logic decodes the current address and generates the enable signal for the appropriate register. The enable values for the registers and counters change on the falling edge of LOAD. Two types of ADDRDEC logic is enabled by 2 pair of addresses, Addresses 22 or 54 (Vectored Restart logic) and Addresses 23 or 55 (Vectored Clear logic). Loading these addresses will enable the appropriate logic and put the part into either a Restart (all counter registers are reinitialized with preprogrammed data) or Clear (all registers are cleared to zero) state. Reloading the same ADDRDEC address will not cause any change in the state of the part. The outputs during these states are frozen and the internal CLOCK is disabled. Clocking the part during a Vectored Restart or Vectored Clear state will have no effect on the part. To resume operation in the new state, or disable the Vectored Restart or Vectored Clear state, another non-ADDRDEC address must be loaded. Operation will begin in the new state on the rising edge of the non-ADDRDEC load pulse. It is recommended that an unused address be loaded following an ADDRDEC operation to prevent data registers from accidentally being corrupted. The following Addresses are used by the device.

Address 0	Status Register REG0
Address 1–18	Data Registers REG1–REG18
Address 19–21	Unused
Address 22/54	Restart Vector (Restarts Device)
Address 23/55	Clear Vector (Zeros All Registers)
Address 24–31	Unused
Address 32–50	Register Scan Addresses
Address 51–53	Counter Scan Addresses
Address 56–63	Unused

At any given time only one register at most is selected. It is possible to have no registers selected.

VECTORED RESTART ADDRESS

The function of addresses 22 (16H) or 54 (36H) are similar to that of the CLR pin except that the preprogramming of the registers is not affected. It is recommended but not required that this address is read after the initial device configuration load sequence. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.

VECTORED CLEAR ADDRESS

Addresses 23 (17H) or 55 (37H) is used to clear all registers to zero simultaneously. This function may be desirable to use prior to loading new data into the Data or Status Registers. This address is read into the device in a similar fashion as all of the other registers. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.

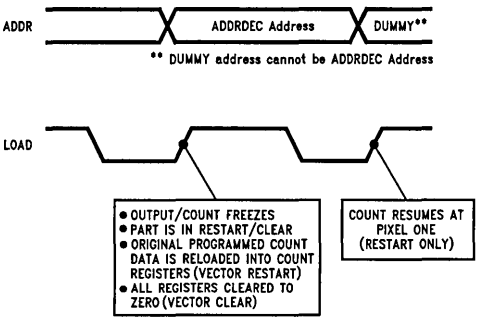

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FIGURE 3. ADDRDEC Timing

GEN LOCKING

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R is designed for master SYNC and BLANK signal generation. However, the devices can be synchronized (slaved) to an external timing signal in a limited sense. Using Vectored Restart, the user can reset the counting sequence to a given location, the beginning, at a given time, the rising edge of the LOAD that removes Vector Restart. At this time the next CLOCK pulse will be CLOCK 1 and the count will restart at the beginning of the first odd line.

Preconditioning the part during normal operation, before the desired synchronizing pulse, is necesasry. However, since LOAD and CLOCK are asynchronous and independent, this is possible without interruption or data and performance corruption. If the defaulted 14.31818 MHz RS-170 values are being used, preconditioning and restarting can be minimized by using the CLEAR pulse instead of the Vectored Restart operation. The 'ACT715-R/LM1882-R is better suited for this application because it eliminates the need to program a 1 into Bit 10 of the Status Register to enable the CLOCK. Gen Locking to another count location other than the very beginning or separate horizontal/vertical resetting is not possible with the 'ACT715/LM1882 nor the 'ACT715-R/LM1882-R.

SCAN MODE LOGIC

A scan mode is available in the ACT715/LM1882 that allows the user to non-destructively verify the contents of the registers. Scan mode is invoked through reading a scan address into the address register. The scan address of a given register is defined by the Data register address + 32. The internal Clocking signal is disabled when a scan address is read. Disabling the clock freezes the device in it's present state. Data can then be serially scanned out of the data registers through the ODD/EVEN Pin. The LSB will be scanned out first. Since each register is 12 bits wide, completely scanning out data of the addressed register will require 12 CLOCK pulses. More than 12 CLOCK pulses on the same register will only cause the MSB to repeat on the output. Re-scanning the same register will require that register to be reloaded. The value of the two horizontal counters and 1 vertical counter can also be scanned out by using address numbers 51–53. Note that before the part will scan out the data, the LOAD signal must be brought back HIGH.

Addressing Logic (Continued)

Normal device operation can be resumed by loading in a non-scan address. As the scanning of the registers is a non-destructive scan, the device will resume correct operation from the point at which it was halted.

RS170 Default Register Values

The tables below show the values programmed for the RS170 Format (using a 14.31818 MHz clock signal) and how they compare against the actual EIA RS170 Specifications. The default signals that will be output are CSYNC, CBLANK, HDRIVE and VDRIVE. The device initially starts at the beginning of the odd field of interlace. All signals have active low pulses and the clock is disabled at power up. Registers 13 and 14 are not involved in the actual signal information. If the Vertical Interrupt was selected so that a pulse indicating the active lines would be output.

Reg	D Value H		Register Description
REG0	0	000	Status Register (715/LM1882)
REG0	1024	400	Status Register (715-R/LM1882-R)
REG1	23	017	HFP End Time
REG2	91	05B	HSYNC Pulse End Time
REG3	157	09D	HBLANK Pulse End Time
REG4	910	38E	Total Horizontal Clocks
REG5	7	007	VFP End Time
REG6	13	00D	VSYNC Pulse End Time
REG7	41	029	VBLANK Pulse End Time
REG8	525	20D	Total Vertical Lines
REG9	57	039	Equalization Pulse End Time
REG10	410	19A	Serration Pulse Start Time
REG11	1	001	Pulse Interval Start Time
REG12	19	013	Pulse Interval End Time
REG13	41	029	Vertical Interrupt Activate Time
REG14	526	20E	Vertical Interrupt Deactivate Time
REG15	911	38F	Horizontal Drive Start Time
REG16	92	05C	Horizontal Drive End Time
REG17	1	001	Vertical Drive Start Time
REG18	21	015	Vertical Drive End Time

	Rate	Period
Input Clock	14.31818 MHz	69.841 ns
Line Rate	15.73426 kHz	63.556 μs
Field Rate	59.94 Hz	16.683 ms
Frame Rate	29.97 Hz	33.367 ms

RS170 Horizontal Data

Signal	Width	μs	%H	Specification (μs)
HFP	22 Clocks	1.536		1.5 ±0.1
HSYNC Width	68 Clocks	4.749	7.47	4.7 ±0.1
HBLANK Width	156 Clocks	10.895	17.15	10.9 ±0.2
HDRIVE Width	91 Clocks	6.356	10.00	0.1H ±0.005H
HEQP Width	34 Clocks	2.375	3.74	2.3 ±0.1
HSERR Width	68 Clocks	4.749	7.47	4.7 ±0.1
HPER iod	910 Clocks	63.556	100	

RS170 Vertical Data

VFP	3 Lines	190.67		6 EQP Pulses
VSYNC Width	3 Lines	190.67		6 Serration Pulses
VBLANK Width	20 Lines	1271.12	7.62	0.075V ± 0.005V
VDRIVE Width	11.0 Lines	699.12	4.20	0.04V ± 0.006V
VEQP Intrvl	9 Lines		3.63	9 Lines/Field
VPERiod (field)	262.5 Lines	16.683 ms		16.683 ms/Field
VPERiod (frame)	525 Lines	33.367 ms		33.367 ms/Frame

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source or Sink Current (I_O) ±15 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±20 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Junction Temperature (T_J)
- Ceramic 175°C
- Plastic 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC}) 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74ACT −40°C to +85°C
- 54ACT −55°C to +125°C

Minimum Input Edge Rate ($\Delta V/\Delta t$)
- V_{IN} from 0.8V to 2.0V
- V_{CC} @ 4.5V, 5.5V 125 mV/ns

DC Characteristics For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF		54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4	5.4	V	
		4.5		3.86	3.7	3.76	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		4.86	4.7	4.76	V	$I_{OH} = -8$ mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1	0.1	V	
		4.5		0.36	0.5	0.44	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		0.36	0.5	0.44	V	$I_{OH} = +8$ mA
I_{OLD}	Minimum Dynamic Output Current	5.5			32.0	32.0	mA	$V_{OLD} = 1.65V$
I_{OHD}	Minimum Dynamic Output Current	5.5			−32.0	−32.0	mA	$V_{OHD} = 3.85V$
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CC}	Supply Current Quiescent	5.5		8.0	160	80	μA	$V_{IN} = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1V$

*All outputs loaded; thresholds on input associated with input under test.

Note 1: Test Load 50 pF, 500Ω to Ground.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$ $C_L = 50$ pF			54ACT/LM1882 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT/LM1882 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAXI}	Interlaced f_{MAX} (HMAX/2 is ODD)	5.0	170	190		130		150		MHz
f_{MAX}	Non-Interlaced f_{MAX} (HMAX/2 is EVEN)	5.0	190	220		145		175		MHz
t_{PLH1} t_{PHL1}	Clock to Any Output	5.0	4.0	13.0	15.5	3.5	19.5	3.5	18.5	ns
t_{PLH2} t_{PHL2}	Clock to ODDEVEN (Scan Mode)	5.0	4.5	15.0	17.0	3.5	22.0	3.5	20.5	ns
t_{PLH3}	Load to Outputs	5.0	4.0	11.5	16.0	3.0	20.0	3.0	19.5	ns

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$		54ACT/LM1882 $T_A = -55°C$ to $+125°C$	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units
			Typ	Guaranteed Minimums			
	Control Setup Time						
t_{sc}	ADDR/DATA to LOAD−	5.0	3.0	4.0	4.5	4.5	ns
t_{sc}	L/HBYTE to LOAD−		3.0	4.0	4.5	4.5	ns
	Data Setup Time						
t_{sd}	D7–D0 to LOAD+	5.0	2.0	4.0	4.5	4.5	ns
	Control Hold Time						
t_{hc}	LOAD− to ADDR/DATA	5.0	0	1.0	1.0	1.0	ns
	LOAD− to L/HBYTE		0	1.0	1.0	1.0	ns
	Data Hold Time						
t_{hd}	LOAD+ to D7–D0	5.0	1.0	2.0	2.0	2.0	ns
t_{rec}	LOAD+ to CLK (Note 1)	5.0	5.5	7.0	8.0	8.0	ns
	Load Pulse Width						
t_{wld-}	LOW	5.0	3.0	5.5	5.5	5.5	ns
t_{wld+}	HIGH	5.0	3.0	5.0	7.5	7.5	ns
t_{wclr}	CLR Pulse Width HIGH	5.0	5.5	6.5	9.5	9.5	ns
t_{wck}	CLOCK Pulse Width (HIGH or LOW)	5.0	2.5	3.0	4.0	3.5	ns

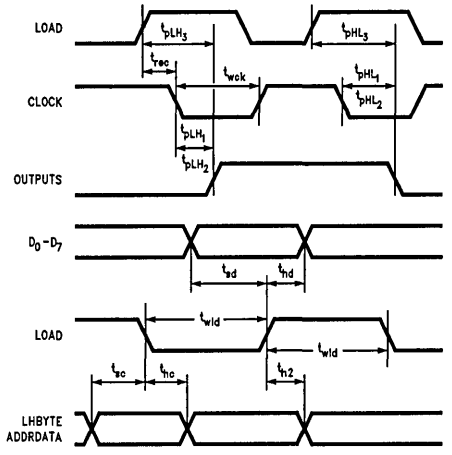
Note 1: Removal of Vectored Reset or Restart to Clock.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	17.0	pF	$V_{CC} = 5.0V$

4

AC Operating Requirements (Continued)



TL/F/10137–6

FIGURE 4. AC Specifications

Additional Applications Information

POWERING UP

The 'ACT715/LM1882 default value for Bit 10 of the Status Register is 0. This means that when the CLEAR pulse is applied and the registers are initialized by loading the default values the CLOCK is disabled. Before operation can begin, Bit 10 must be changed to a 1 to enable CLOCK. If the default values are needed (no other programming is required) then *Figure 5* illustrates a hardwired solution to facilitate the enabling of the CLOCK after power-up. Should control signals be difficult to obtain, *Figure 6* illustrates a possible solution to automatically enable the CLOCK upon power-up. Use of the 'ACT715-R/LM1882-R eliminates the need for most of this circuitry. Modifications of the *Figure 6* circuit can be made to obtain the lone CLEAR pulse still needed upon power-up.

Note that, although during a Vectored Restart none of the preprogrammed registers are affected, some signals are affected for the duration of one frame only. These signals are the Horizontal and Vertical Drive signals. After a Vectored Restart the beginning of these signals will occur at the first CLK. The end of the signals will occur as programmed. At the completion of the first frame, the signals will resume to their programmed start and end time.

PREPROGRAMMING "ON-THE-FLY"

Although the 'ACT715/LM1882 and 'ACT715-R/LM1882-R are completely programmable, certain limitations must be set as to when and how the parts can be reprogrammed. Care must be taken when reprogramming any End Time registers to a new value that is lower than the current value. Should the reprogramming occur when the counters are at a count after the new value but before the old value, then the counters will continue to count up to 4096 before rolling over.

For this reason one of the following two precautions are recommended when reprogramming "on-the-fly". The first recommendation is to reprogram horizontal values during the horizontal blank interval only and/or vertical values during the vertical blank interval only. Since this would require delicate timing requirements the second recommendation may be more appropriate.

The second recommendation is to program a Vectored Restart as the final step of reprogramming. This will ensure that all registers are set to the newly programmed values and that all counters restart at the first CLK position. This will avoid overrunning the counter end times and will maintain the video integrity.

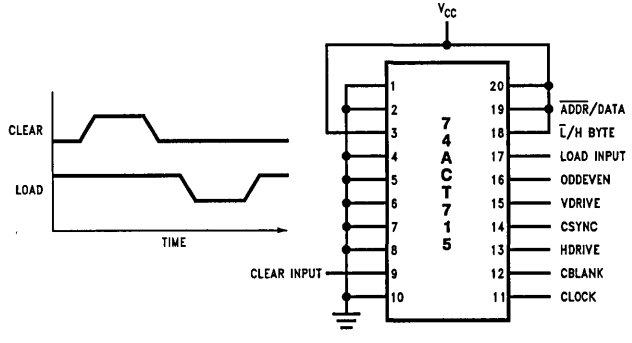


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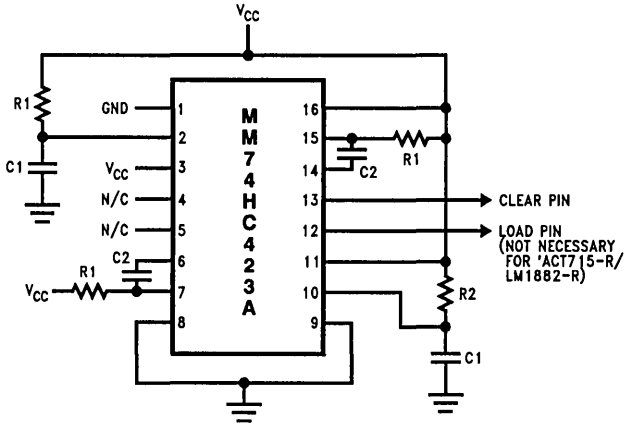
FIGURE 5. Default RS170 Hardwire Configuration

Additional Applications Information (Continued)



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Note: A 74HC221A may be substituted for the 74HC423A Pin 6 and Pin 14 must be hardwired to GND

Components

R1: 4.7k C1: 10 μF
R2: 10k C2: 50 pF

FIGURE 6. Circuit for Clear and Load Pulse Generation

National Semiconductor

PRELIMINARY

CMOS Crystal Clock Generators CGS3311/CGS3312/CGS3313/CGS3314/CGS3315/ CGS3316/CGS3317/CGS3318/CGS3319

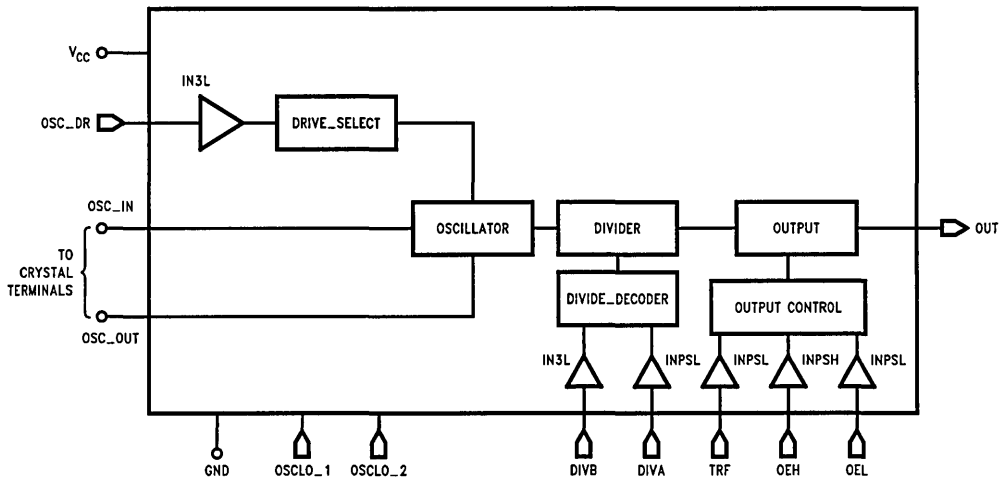
General Description

These devices are designed for Clock Generation and Support (CGS™) applications up to 110 MHz. The CGS331x series of devices are crystal controlled CMOS oscillators requiring a minimum of external components. The 331x devices provide selectable output divide ratio (and selectable crystal drive level). The circuit is designed to operate over a wide frequency range using fundamental model or overtone crystals.

Features

- National's CGS™ family of devices for high frequency clock source applications
- Crystal frequency operation range: fundamental: 10 MHz to 100 MHz typical 3rd or 5th overtone: 10 MHz to 85 MHz
- Programmable oscillator drive
- Selectable fast output edge rates
- Output symmetry circuit to adjust 50% duty cycle point between CMOS and TTL levels
- Output current drive of 48 mA for I_{OL}/I_{OH}
- FACT™ CMOS output levels
- Output has high speed short circuit protection
- Basic oscillator type: Pierce
- Hysteresis inputs to improve noise margin

Block Diagrams

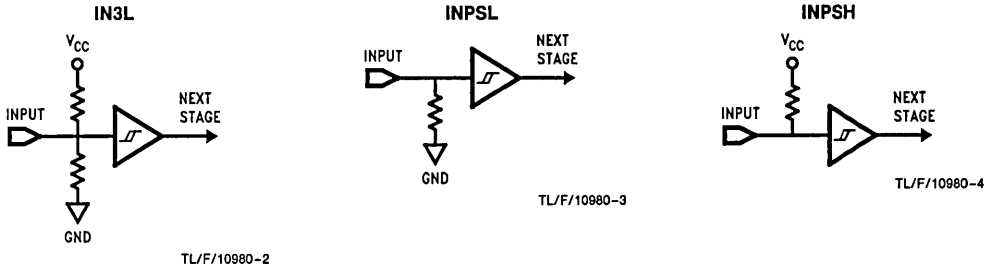


TL/F/10980–1

Note: Pin numbers vary for each device

Block Diagrams (Continued)

Input Drivers

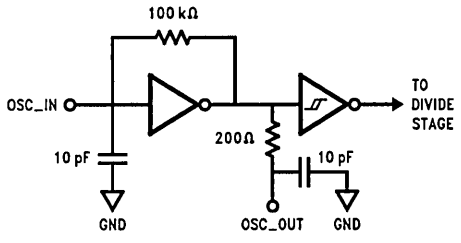


TL/F/10980–2

TL/F/10980–3

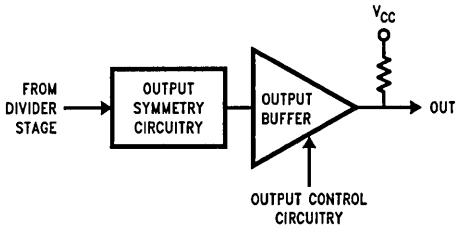
TL/F/10980–4

Oscillator Stage



TL/F/10980–5

Output Stage



TL/F/10980–6

Functional Description

Summary of Device Options

Device	Divide	Enable	Drive	Output Rise/ Fall Time (ns)
3311	1, 2, 4	OEH	L, M, H	2, 4
3312	1, 2, 4	OEH	H	2, 4
3313	8, 16, 32	OEH	H	4
3314	8, 16, 32	OEH	L, M, H	4
3315	1, 2, 4	OEL	H	1, 2
3316	4	OEH	H	4
3317	32	OEH	H	4
3318	1, 2, 4	OEH	H	1, 2
3319	1, 2, 4	OEL	L, M, H	2, 4

Each drive has one output with the choices of selecting frequency divide, output enable, crystal drive and output rise and fall time. Crystal drive options are:

L = Low Drive
M = Medium Drive
H = High Drive

Pin Descriptions

Note: Pin out varies for each device.

OSC_IN Input to Oscillator Inverter. The output of the crystal would be connected here.

OSC_OUT Resistive Buffered Output of the Oscillator Inverter

OSC_DR 3 Level input pin that selects Oscillator Drive Level

DIVA Input used to select Binary Divide-by Option. This pin has CMOS compatible input levels.

DIVB 3 Level input used to select Binary Divide-by value.

OEH Active High TRI-STATE® enable pin. This pin pulls to a high value when left floating and TRI-STATEs the output when forced low. This pin has TTL compatible input levels.

OEL Active Low TRI-STATE enable pin. This pin pulls to a low value when left floating and TRI-STATES the output when forced high. This pin has TTL compatible input levels.

TRF Rise and Fall time override pin. Available only for die form.

OUT This pin is the main clock output on the device.

OSCLO_1 The Oscillator Low pin is the ground for the Oscillator.

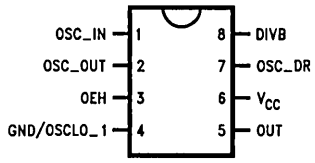
OSCLO_2 This pin is the same signal as OSCLO_1. It has been provided as an alternate connection for OSCLO_1 for hybrid assemblies.

V_{CC} The power pin for the chip.

GND The ground pin for all sections of the circuitry except the oscillator and oscillator related circuitry.

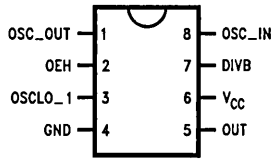
Connection Diagrams

Pin Assignment for SOIC



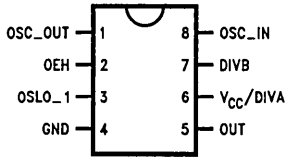
TL/F/10980–7

(A) 3311



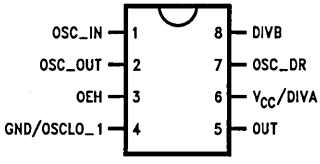
TL/F/10980–8

(B) 3312



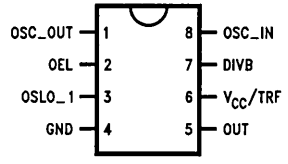
TL/F/10980–9

(C) 3313



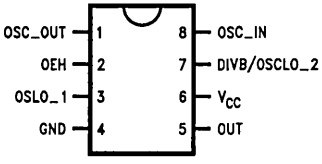
TL/F/10980–10

(D) 3314



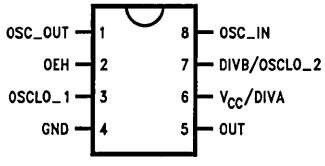
TL/F/10980–11

(E) 3315



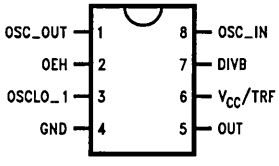
TL/F/10980–12

(F) 3316



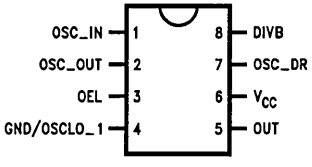
TL/F/10980–13

(G) 3317



TL/F/10980–14

(H) 3318



TL/F/10980–15

(I) 3319

Truth Tables

Division Selection

DIVB	DIVA	OEL	OEH	Divider Output
F	0/F	X	X	Divide-by 1
1	0/F	0	1	Divide-by 2
0	0/F	0	1	Divide-by 4
F	1	0	1	Divide-by 8
1	1	0	1	Divide-by 16
0	1	0	1	Divide-by 32
X	X	1	X	Output Reset High at Re-enable
X	X	X	0	Output Reset High at Re-enable

Note: Actual value of the floating OSC__DR and DIVB input is $V_{CC/2}$

Rise and Fall Time Selection

OSC__DR	DIV	TRF	Rise/Fall Time (ns)
F	N	0/F	2
F	N	1	less than 2
F	Y	0/F	4
F	Y	1	2
0, 1	X	0/F	4
0, 1	X	1	2

Drive Selection

OSC__DR	Drive
0	Low
1	Medium
F	High

Note: Where "F" indicates floating the input.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage Diode Current (I_{IK})	± 9mA
DC Input Voltage (V_I)	−0.5V to 7.0V
DC Output Diode Current (I_{OK})	±20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±70 mA
Storage Temperature (T_{STG})	−55°C to +150°C
Junction Temperature (T_J) SOIC	140°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC} V
Operating Temperature (T_A)	−40°C to +85°C

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	CGS3311 to 3319							Units	Conditions
			T_A = +25°C		T_A = −40°C to +85°C		T_A = −55°C to +125°C				
			Typ	Guaranteed Limits							
				Min	Max	Min	Max	Min	Max		
$V_{IH_{TTL}}$	Minimum High Level Input Voltage. TTL Level Inputs (OEH, OEL)	4.5 5.5		2.0 2.0		2.0 2.0				V	
$V_{IL_{TTL}}$	Maximum Low Level Input Voltage. TTL Level Inputs (OEH, OEL)	4.5 5.5			0.8 0.8		0.8 0.8			V	
$V_{IH_{CMOS}}$	Minimum High Level Input Voltage. CMOS Level Inputs (DIVA)	4.5 5.5		3.15 3.85		3.15 3.85				V	
$V_{IL_{CMOS}}$	Maximum Low Level Input Voltage. CMOS Level Inputs (DIVA)	4.5 5.5			1.35 1.65		1.35 1.65			V	
V_{IN3L_H}	Minimum Logic 1 Input for Three Level Input (DIVB, OSC_DR)	4.5 5.5		4.05 4.95		4.05 4.95				V	
$V_{IN3L\_1/2}$	Minimum Logic 1/2 Input for Three Level Input (DIVB, OSC_DR)	4.5 5.5		1.8 2.2	2.7 3.3	1.8 2.2	2.7 3.3			V	
V_{IN3L_L}	Maximum Logic 0 Input Level Three Level Input (DIVB, OSC_DR)	4.5 5.5			0.45 0.45		0.45 0.45			V	
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.40 5.40		4.40 5.40				V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86		3.76 4.76					I_{OH} = −48 mA V_{IN} = V_{IH} or V_{IH}

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	CGS3311 to 3319							Units	Conditions
			T_A = +25°C			T_A = −40°C to +85°C		T_A = −55°C to +125°C			
			Typ	Guaranteed Limits							
				Min	Max	Min	Max	Min	Max		
V_{OL}	Minimum Low Level Output Voltage	4.5	0.001		0.1		0.1			V	I_{OUT} = 50 μA
		5.5	0.001		0.1		0.1				
		4.5			0.44		0.44				I_{OL} = +48 mA V_{IN} = V_{IL} or V_{IH}
		5.5			0.44		0.44				
$I_{IH_{RES}}$	Input Current for Pins DIVB, OSC_DR, and DIVA (Input is Logic High)	5.5		220	360	200	380			μA	V_{IN} = 5.5V
$I_{IL_{RES}}$	Input Current for Pins DIVB, OSC_DR, and DIVA (Input is Logic Low)	5.5		−220	−360	−200	−380			μA	V_{IN} = 0.0V
$I_{IH_{ENAB}}$	Input Current for Enable Pin OEL	5.5		90	160	85	175			μA	V_{IN} = 5.5V
$I_{IL_{ENAB}}$	Input Current for Enable pin OEH	5.5		−90	−160	−85	−175			μA	V_{IN} = 0.0V
$I_{IH_{OSC}}$	Input Current for OSC_IN pin (Indicates Bias Resistance)	5.5		20	100	20	125			μA	V_{IN} = 5.5V
$I_{IL_{OSC}}$	Input Current for OSC_IN pin (Indicates Bias Resistance)	5.5		−20	−100	−20	−125			μA	V_{IN} = 0.0V
I_{OZH}	Output Disabled Current (Output High)	4.5			3.0		5.0			μA	V_{OUT} = V_{CC}
		5.5			3.0		5.0				
I_{OZL}	Output Disabled Current (Output Low)	4.5			−140		−150			μA	V_{OUT} = 0.0V
		5.5			−170		−180				
I_{OLD}	Minimum Dynamic Output Current	5.5		75		75				mA	V_{OLD} = 1.65V
I_{OHD}	Minimum Dynamic Output Current	5.5		−75		−75				mA	V_{OHD} = 3.85V
$I_{CC_{OSC\_L}}$	Additional I_{CC} with OSC_IN Floating. Low Drive Mode	4.5		0.6		0.6				mA	OSC_IN = Float
		5.5			6.5		6.5				
$I_{CC_{OSC\_M}}$	Additional I_{CC} with OSC_IN Floating. Low Drive Mode	4.5		1.7		1.7				mA	OSC_IN = Float
		5.5			12.4		12.4				
$I_{CC_{OSC\_H}}$	Additional I_{CC} with OSC_IN Floating. Low Drive Mode	4.5		5.5		5.5				mA	OSC_IN = Float
		5.5			31.5		31.5				
I_{CC_T}	Additional Maximum I_{CC} per Input (OEH, OEL Pins)	5.5			1.5		1.5			mA	V_{IN} = V_{CC} − 2.1V
$I_{CC_{3L}}$	Additional Maximum I_{CC} per Input (DIVB, OSC_DR Inputs)	5.5			1.5		1.5			mA	DIVB, OSC_DR Inputs Equal to $V_{CC/2}$

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	V_{CC}* (V)	CGS331X						Units
			T_A = −40°C to +85°C, C_L = 50 pF			T_A = −55°C to +125°C, C_L = 50 pF			
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Frequency Maximum	5.0	100						MHz
t_{PZH}	Output High Enable Time	5.0	1.0		31.5				ns
t_{PZL}	Output Low Enable Time	5.0	1.0		28.0				ns
t_{PHZ}	Output High Disable Time	5.0	1.0		21.5				ns
t_{PLZ}	Output Low Disable Time	5.0	1.0		16.0				ns
t_{rise}, t_{fall}	Rise/Fall Time 30 pF, 20% to 80%)	5.0		4.0					ns

* Voltage Range 5.0 is 5.0V ± 0.5V

4

National Semiconductor

CGS3321/CGS3322
CMOS Crystal Clock Generators

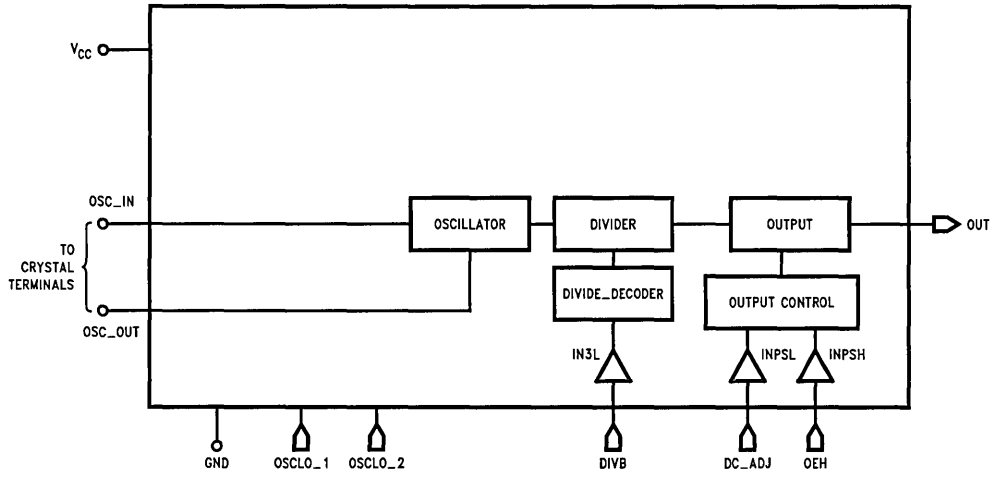
General Description

These devices are designed for Clock Generation and Support (CGS™) applications up to 110 MHz. The CGS332x series of devices are crystal controlled CMOS oscillators requiring a minimum of external ccomponents. The 332x devices provide selectable output divide ratio. The circuit is designed to operate over a wide frequency range using fundamental mode or overtone crystals.

Features

- National's CGS family of devices for high frequency clock source applications
- Crystal frequency operation range:
  fundamental: 10 MHz to 110 MHz typical
  3rd or 5th overtone: 10 MHz to 95 MHz
- 1000V ESD protection on OSC_IN and OSC_OUT pins. 2000V ESD protection on all other pins
- Output current drive of 48 mA for I_{OL}/I_{OH}
- FACT™ CMOS output levels
- Output has high speed short circuit protection
- Intended for Pierce oscillator applications
- Hysteresis inputs to improve noise margin
- CGS3321 has duty cycle adjust
- CGS3322 has 1, 2, 4 divide ratio

Block Diagrams

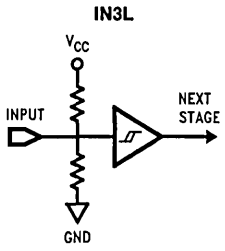


TL/F/11503–1

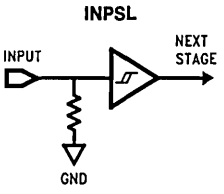
Note: Pin numbers vary for each device.

Block Diagrams (Continued)

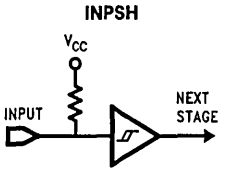
Input Drivers



TL/F/11503–2

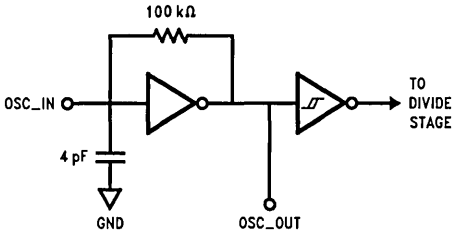


TL/F/11503–3



TL/F/11503–4

Oscillator Stage



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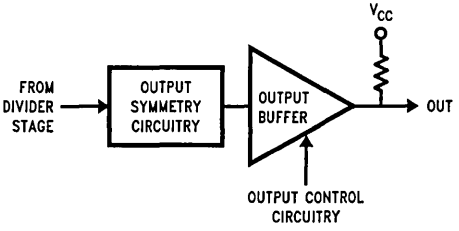
Output Stage



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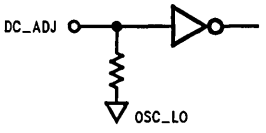


TL/F/11503–9

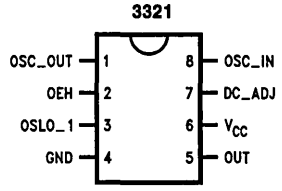
Pin Descriptions

OSC_IN	Input to Oscillator Inverter. The output of the crystal would be connected here.
OSC_OUT	Buffered Output of the Oscillator Inverter
DIVB	(CGS3322 only) 3-Level input used to select Binary Divide-by value of output frequency.
DC_ADJ	(CGS3321 only) Active high input that controls output duty cycle. Logic high level will delay the HL transition edge approximately 0.3 ns.
OEH	Active High TRI-STATE® enable pin. This pin pulls to a high value when left floating and TRI-STATEs the output when forced low. This pin has TTL compatible input levels.
OUT	This pin is the main clock output on the device.
OSCLO_1	The Oscillator Low pin is the ground for the Oscillator.
V_{CC}	The power pin for the chip.
GND	The ground pin for all sections of the circuitry except the oscillator and oscillator related circuitry.

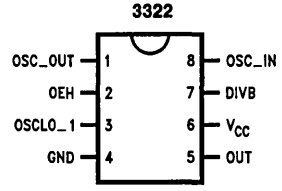
Note: Pin out varies for each device.

Connection Diagrams

Pin Assignment for SOIC



TL/F/11503–7



TL/F/11503–8

Truth Table

Division Selection

DIVB	OEH	Divider Output
F	X	Divide-by 1
1	1	Divide-by 2
0	1	Divide-by 4

Note: Actual value of the floating DIVB input is $V_{CC/2}$.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage Diode Current (I_{IK})	± 9 mA
DC Input Voltage (V_I)	−0.5V to 7.0V
DC Output Diode Current (I_{OK})	±20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±70 mA
Storage Temperature (T_{STG})	−55°C to +150°C
Junction Temperature (T_J) SOIC	140°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC} V
Operating Temperature (T_A)	−40°C to +85°C

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	CGS3321/3322							Units	Conditions
			T_A = +25°C			T_A = −40°C to +85°C		T_A = −55°C to +125°C			
			Typ	Guaranteed Limits							
				Min	Max	Min	Max	Min	Max		
$V_{IH_{TTL}}$	Minimum High Level Input Voltage. TTL Level Inputs (OEH, OEL)	4.5 5.5		2.0 2.0		2.0 2.0				V	
$V_{IL_{TTL}}$	Maximum Low Level Input Voltage. TTL Level Inputs (OEH, OEL)	4.5 5.5			0.8 0.8		0.8 0.8			V	
$V_{IH_{CMOS}}$	Minimum High Level Input Voltage. CMOS Level Inputs (DC_ADJ)	4.5 5.5		3.15 3.85		3.15 3.85				V	
$V_{IL_{CMOS}}$	Maximum Low Level Input Voltage. CMOS Level Inputs (DC_ADJ)	4.5 5.5			1.35 1.65		1.35 1.65			V	
V_{IN3L_H}	Minimum Logic 1 Input for Three Level Input (DIVB)	4.5 5.5		4.05 4.95		4.05 4.95				V	
$V_{IN3L\_1/2}$	Minimum Logic 1/2 Input for Three Level Input (DIVB)	4.5 5.5		1.8 2.2	2.7 3.3	1.8 2.2	2.7 3.3			V	
V_{IN3L_L}	Maximum Logic 0 Input Level Three Level Input (DIVB)	4.5 5.5			0.45 0.45		0.45 0.45			V	
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.40 5.40		4.40 5.40				V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86		3.76 4.76					I_{OH} = −48 mA V_{IN} = V_{IH} or V_{IL}

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	CGS3321/3322							Units	Conditions
			T_A = +25°C			T_A = −40°C to +85°C		T_A = −55°C to +125°C			
			Typ	Guaranteed Limits							
				Min	Max	Min	Max	Min	Max		
V_{OL}	Minimum Low Level Output Voltage	4.5 5.5	0.001 0.001		0.1 0.1		0.1 0.1			V	I_{OUT} = 50 μA
		4.5 5.5			0.44 0.44		0.44 0.44				I_{OL} = +48 mA V_{IN} = V_{IL} or V_{IH}
I_{IHRES}	Input Current for Pins DIVB	5.5		220	360	200	380			μA	V_{IN} = 5.5V
I_{ILRES}	Input Current for Pins DIVB	5.5		−220	−360	−200	−380			μA	V_{IN} = 0.0V
I_{IHENAB}	Input Current for Enable Pin OEL	5.5		90	160	85	175			μA	V_{IN} = 5.5V
I_{ILENAB}	Input Current for Enable pin OEH	5.5		−90	−160	−85	−175			μA	V_{IN} = 0.0V
I_{IHOSC}	Input Current for OSC_IN pin (Indicates Bias Resistance)	5.5		20	100	20	125			μA	V_{IN} = 5.5V
I_{ILOSC}	Input Current for OSC_IN pin (Indicates Bias Resistance)	5.5		−20	−100	−20	−125			μA	V_{IN} = 0.0V
I_{OZH}	Output Disabled Current (Output High)	4.5 5.5			3.0 3.0		5.0 5.0			μA	V_{OUT} = V_{CC}
I_{OZL}	Output Disabled Current (Output Low)	4.5 5.5			−140 −170		−150 −180			μA	V_{OUT} = 0.0V
I_{OLD}	Minimum Dynamic Output Current	5.5		75		75				mA	V_{OLD} = 1.65V
I_{OHD}	Minimum Dynamic Output Current	5.5		−75		−75				mA	V_{OHD} = 3.85V
I_{CC_T}	Additional Maximum I_{CC} per Input (OEH, OEL Pins)	5.5			1.5		1.5			mA	V_{IN} = V_{CC} − 2.1V
$I_{CC_{3L}}$	Additional Maximum I_{CC} per Input (DIVB)	5.5			1.5		1.5			mA	DIVB Inputs Equal to $V_{CC/2}$

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	V_{CC}* (V)	CGS332X						Units
			T_A = −40°C to +85°C, C_L = 50 pF			T_A = −55°C to +125°C, C_L = 50 pF			
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Frequency Maximum	5.0	95	110					MHz
t_{PZH}	Output High Enable Time	5.0	1.0		31.5				ns
t_{PZL}	Output Low Enable Time	5.0	1.0		28.0				ns
t_{PHZ}	Output High Disable Time	5.0	1.0		21.5				ns
t_{PLZ}	Output Low Disable Time	5.0	1.0		16.0				ns
t_{rise}, t_{fall}	Rise/Fall Time (30 pF, 20% to 80%)	5.0		1.0					ns

*Voltage Range 5.0 is 5.0V ± 0.5V.

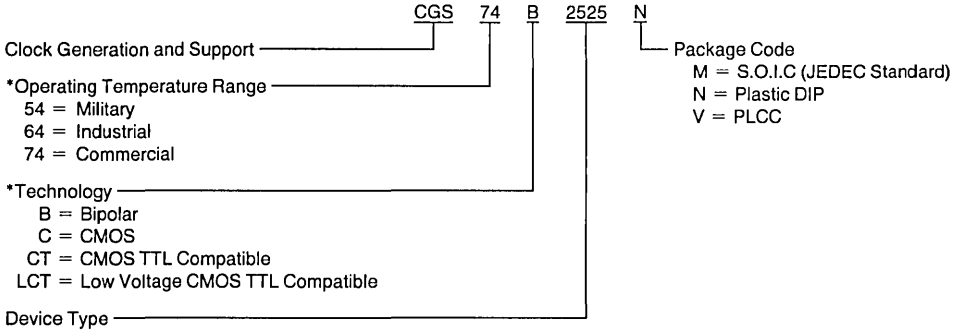
Section 5

Physical Dimensions

Section 5 Contents

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows for Bipolar, CMOS and CMOS TTL compatible CGS parts:



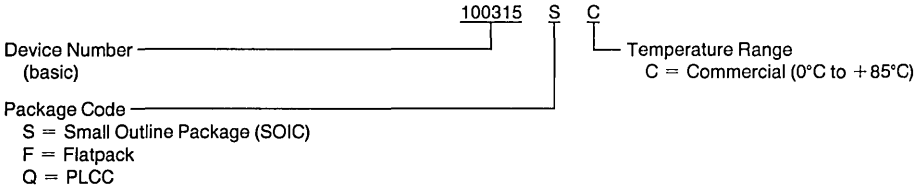
*Optional

Temperature Information

	Technology	Temperature Range†		
		74-Grade	64-Grade	54-Grade
TTL/CMOS	Bipolar	0°C to 70°C	−40°C to +85°C	−55°C to +125°C
	CMOS	−40°C to +85°C	N/A	−55°C to +125°C
	CMOS/TTL Compatible	−40°C to +85°C	N/A	−55°C to +125°C
	BiCMOS	0°C to +70°C	−40°C to +85°C	−55°C to +125°C

†Typically, 64- and 74-grade are commercial products; and 54-grade may or may not be Mil/Aero product.

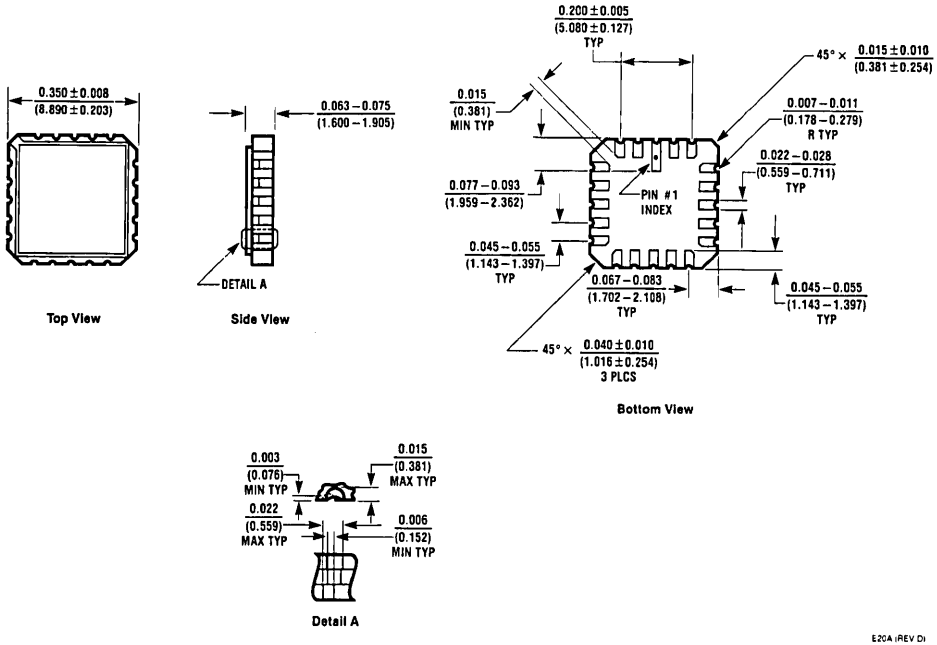
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows for ECL compatible CGS parts:



National Semiconductor

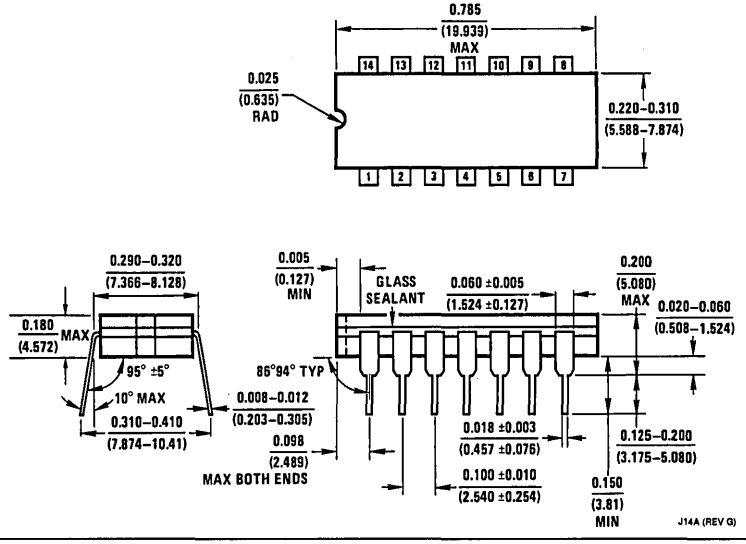
All dimensions are in inches (millimeters)

20 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E20A



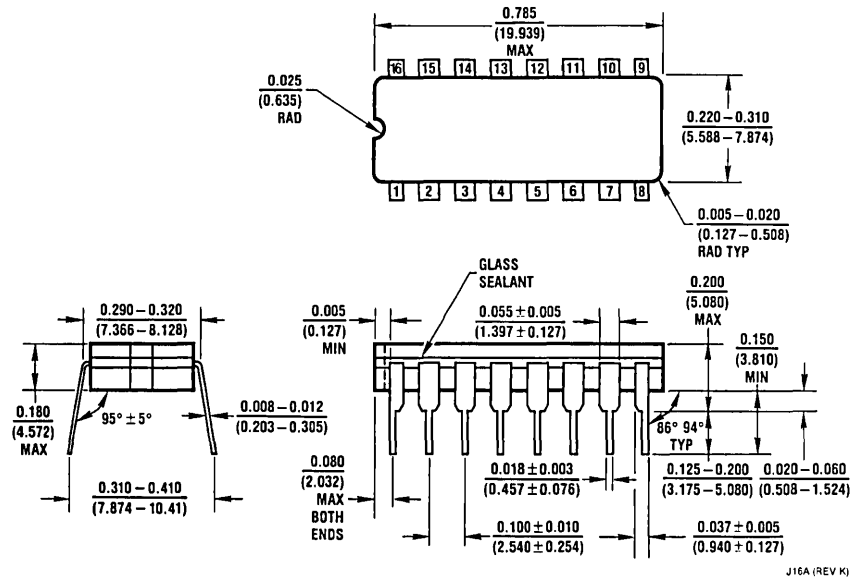
E20A (REV D)

14 Lead Ceramic Dual-in-Line Package
NS Package Number J14A



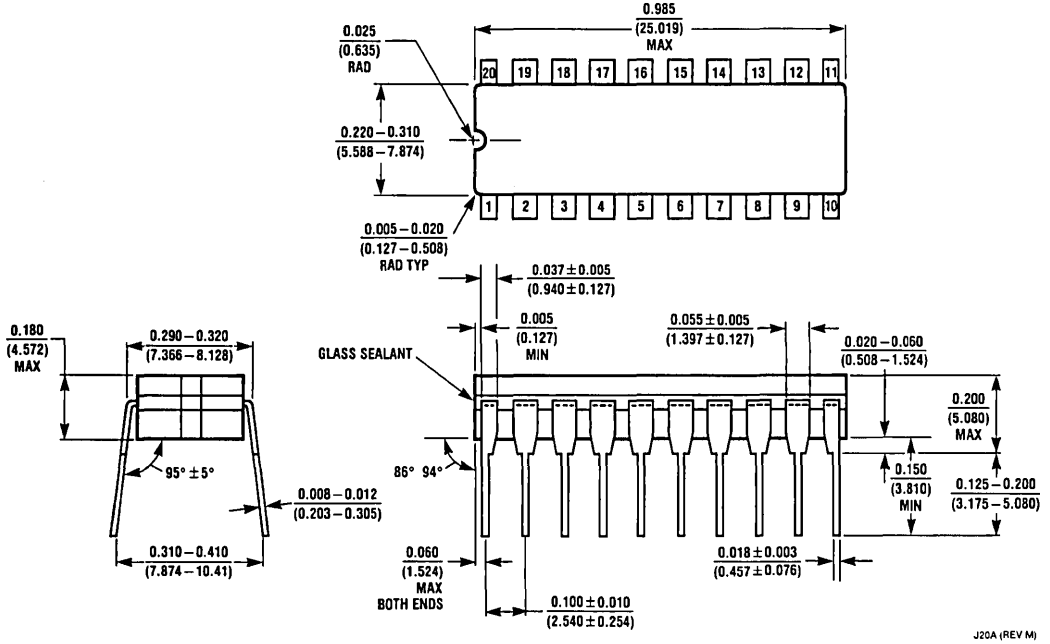
J14A (REV G)

16 Lead Ceramic Dual-in-Line Package
NS Package Number J16A



J16A (REV K)

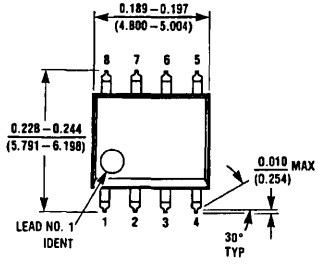
20 Lead Ceramic Dual-in-Line Package
NS Package Number J20A

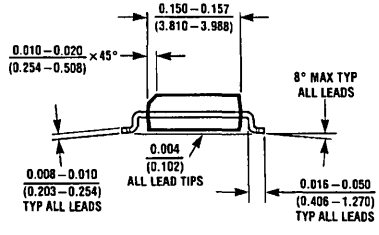


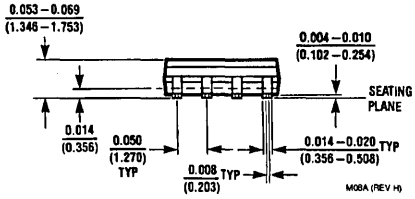
J20A (REV M)

5

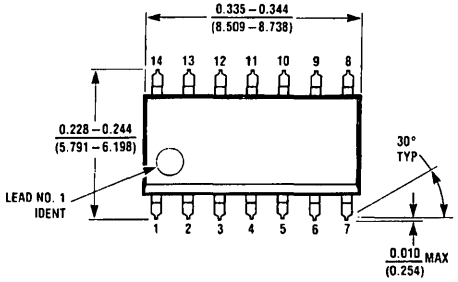
8 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M08A

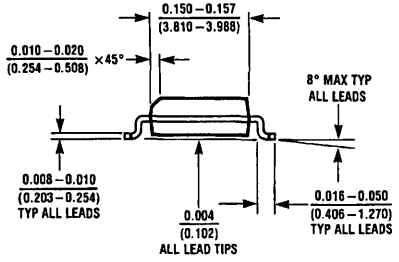


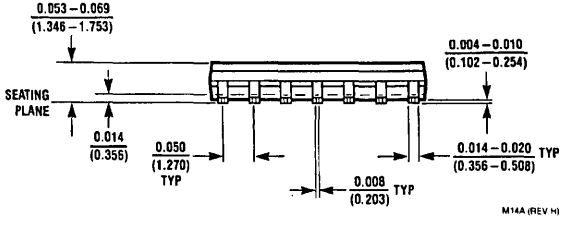




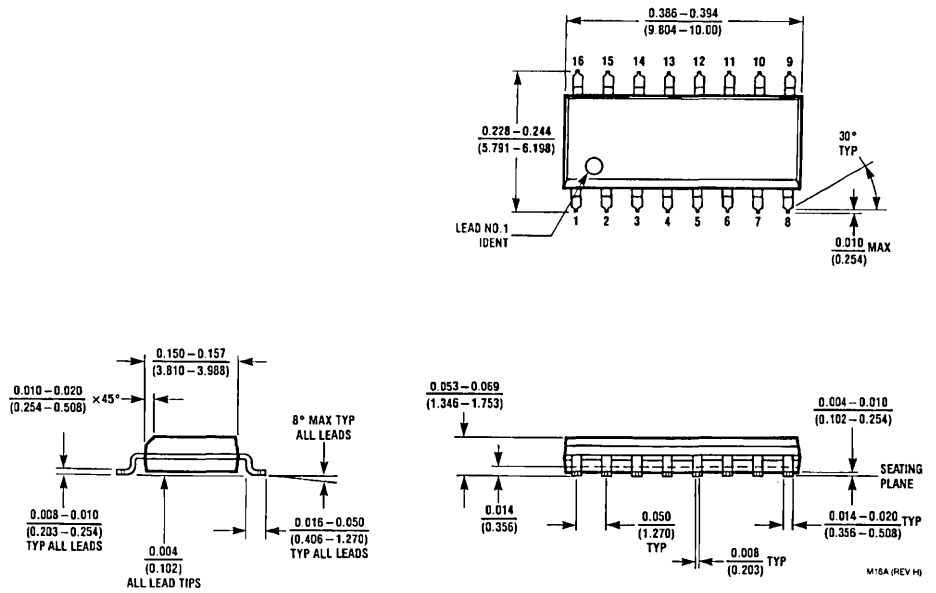
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14A



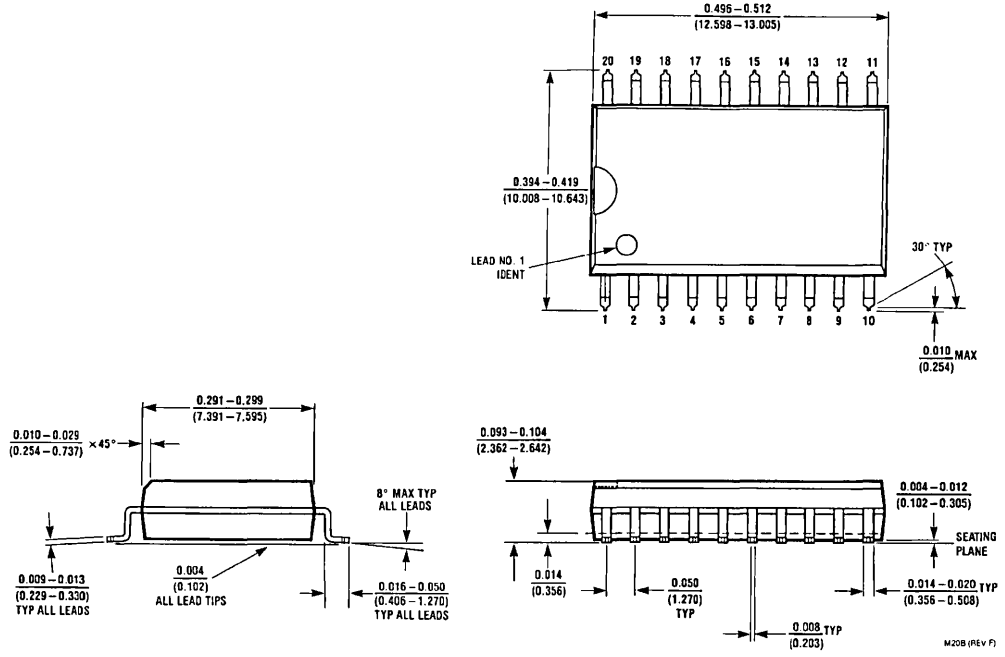




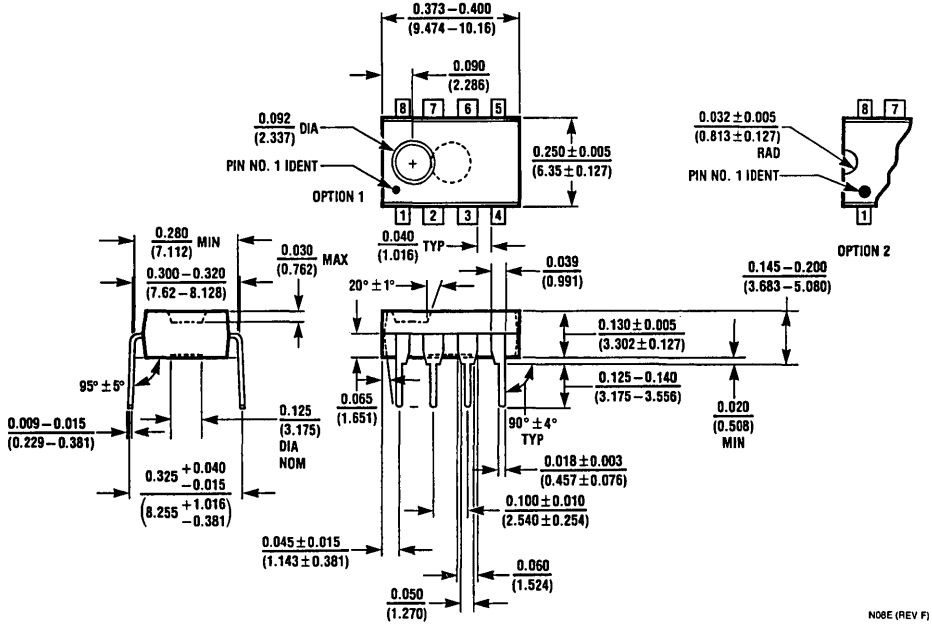
16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A



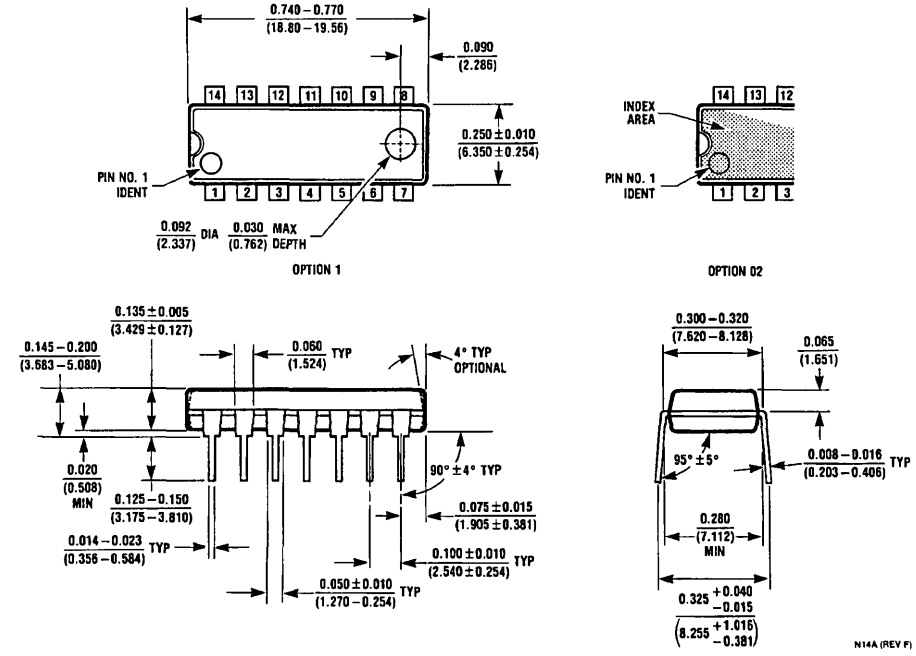
20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B



8 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N08E



14 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N14A



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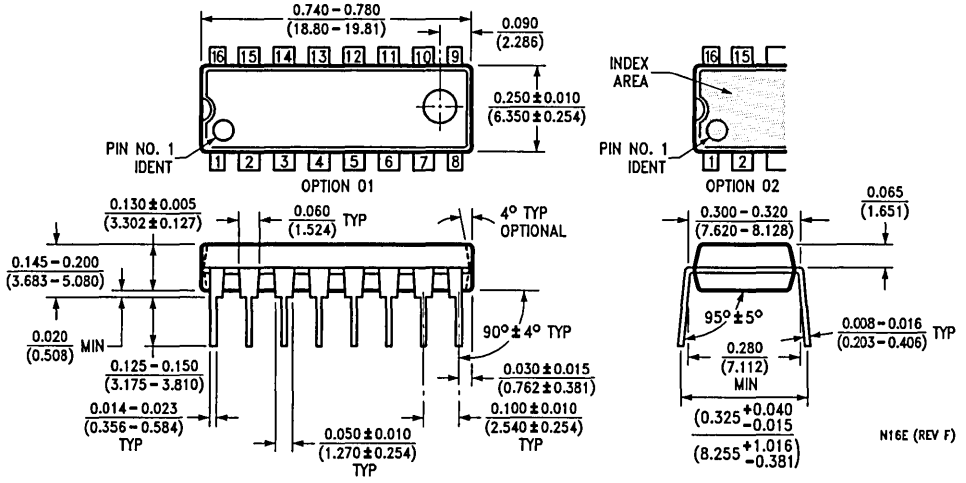
NS Package Number N16E



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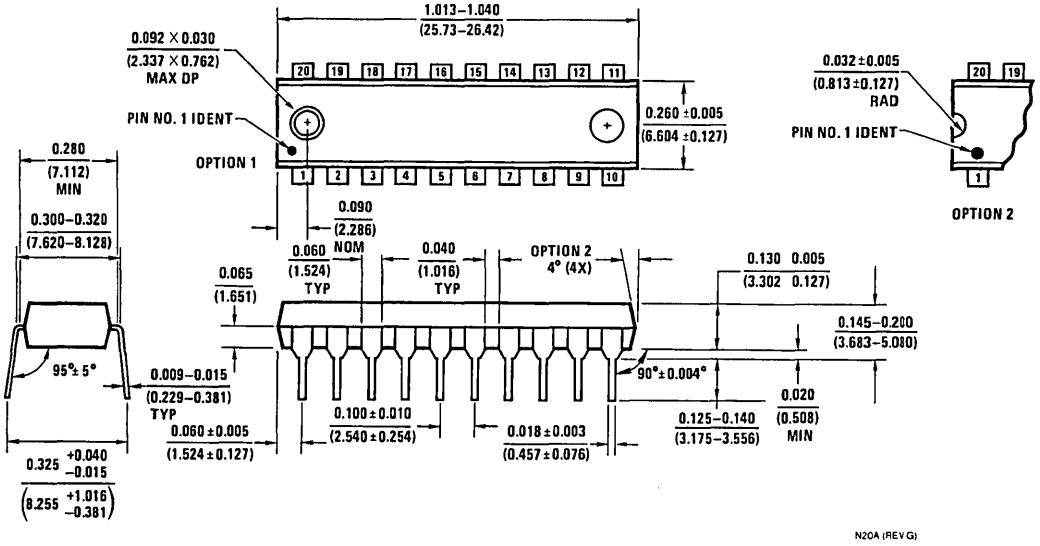
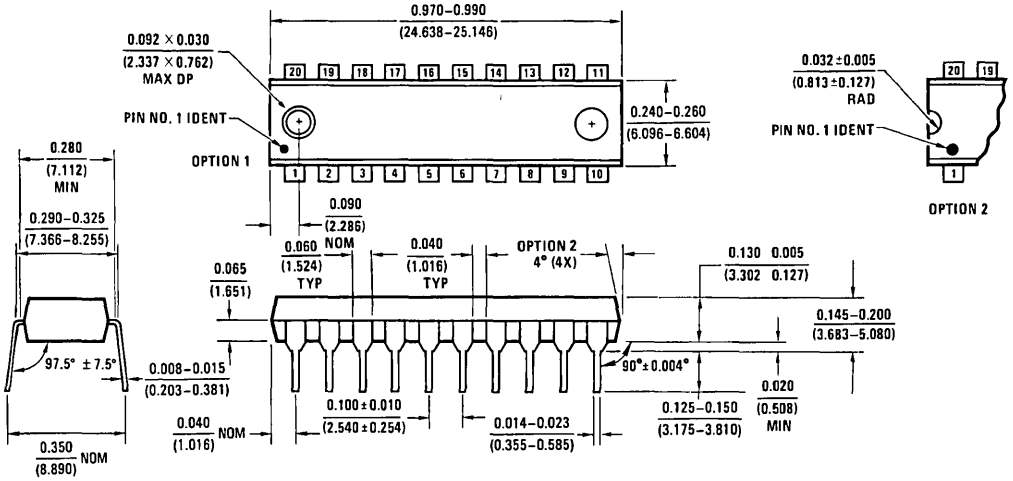
NS Package Number N20A

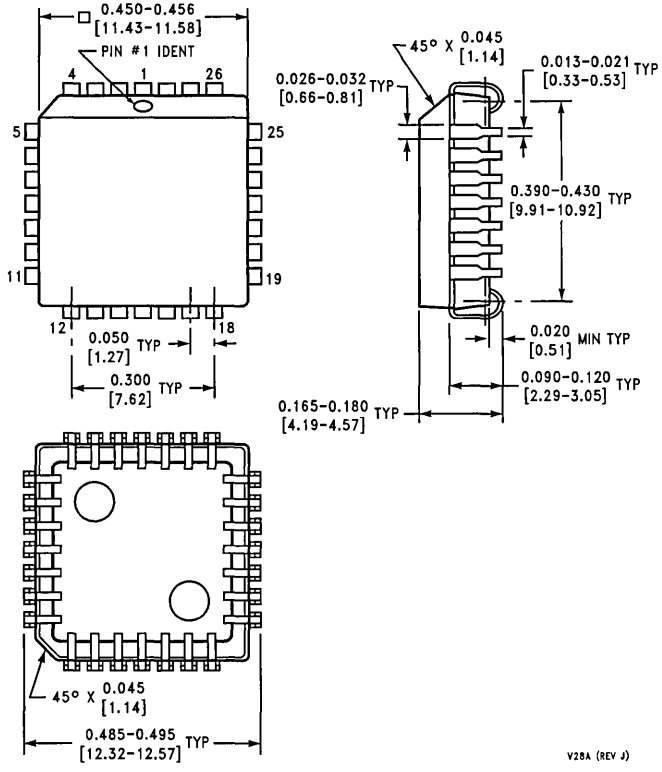


20 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N20B



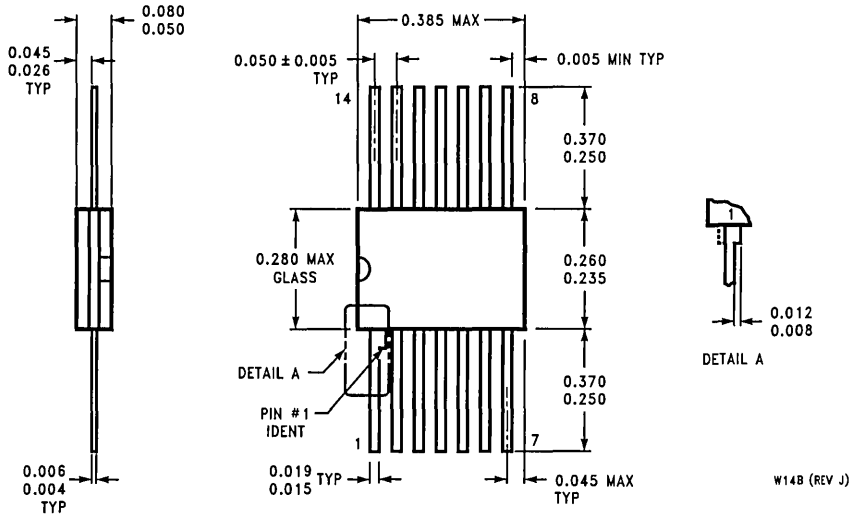
N20B (REV A)

28 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V28A

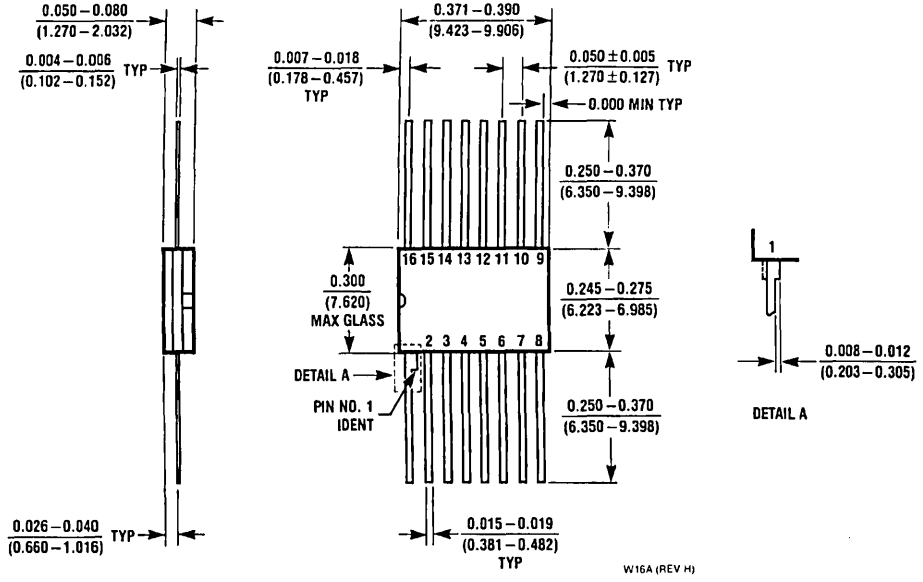


V28A (REV J)

14 Lead Cerpack
NS Package Number W14B



16 Lead Cerpack
NS Package Number W16A



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2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090

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ABTC Applications and Design Considerations • Quality and Reliability • Integrated Bus Function (IBF) Introduction
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54/74ACTQ3283 32-Bit Latchable Transceiver with Parity Generator/Checker and Byte Multiplexing
54/74ABTCXXX • 74BCTXXX

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MM54HCT/MM74HCT • CD4XXX • MM54CXXX/MM74CXXX • Surface Mount

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Crystal Clock Generators

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Bipolar PNP Transistors • JFET Transistors • Surface Mount Products • Pro-Electron Series
Consumer Series • Power Components • Transistor Datasheets • Process Characteristics

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Microprocessor Applications

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F100K ECL LOGIC DATABOOK & DESIGN GUIDE—1992

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Design Guide • Circuit Basics • Logic Design • Transmission Line Concepts • System Considerations
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Quality Assurance and Reliability • Application Notes

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Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA/B

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Circuit Characteristics • Ratings, Specifications and Waveforms • Design Considerations • 54F/74FXXX

FAST® APPLICATIONS HANDBOOK—1990

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Contains application information on the FAST family: Introduction • Multiplexers • Decoders • Encoders
Operators • FIFOs • Counters • TTL Small Scale Integration • Line Driving and System Design
FAST Characteristics and Testing • Packaging Characteristics

HIGH-PERFORMANCE BUS INTERFACE DESIGNER'S GUIDE—1992

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High Performance TTL Bus Drivers • PI-Bus • Futurebus+/BTL Reference

IBM DATA COMMUNICATIONS HANDBOOK—1992

IBM Data Communications • Application Notes

INTERFACE: LINE DRIVERS AND RECEIVERS DATABOOK—1992

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Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

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PROGRAMMABLE LOGIC DEVICE DATABOOK AND DESIGN GUIDE—1993

Product Line Overview • Datasheets • Design Guide: Designing with PLDs • PLD Design Methodology
PLD Design Development Tools • Fabrication of Programmable Logic • Application Examples

REAL TIME CLOCK HANDBOOK—1993

3-Volt Low Voltage Real Time Clocks • Real Time Clocks and Timer Clock Peripherals • Application Notes

RELIABILITY HANDBOOK—1987

Reliability and the Die • Internal Construction • Finished Package • MIL-STD-883 • MIL-M-38510
The Specification Development Process • Reliability and the Hybrid Device • VLSI/VHSIC Devices
Radiation Environment • Electrostatic Discharge • Discrete Device • Standardization
Quality Assurance and Reliability Engineering • Reliability and Documentation • Commercial Grade Device
European Reliability Programs • Reliability and the Cost of Semiconductor Ownership
Reliability Testing at National Semiconductor • The Total Military/Aerospace Standardization Program
883B/RETS™ Products • MILS/RETS™ Products • 883/RETS™ Hybrids • MIL-M-38510 Class B Products
Radiation Hardened Technology • Wafer Fabrication • Semiconductor Assembly and Packaging
Semiconductor Packages • Glossary of Terms • Key Government Agencies • AN/ Numbers and Acronyms
Bibliography • MIL-M-38510 and DESC Drawing Cross Listing

SCAN™ DATABOOK—1993

Evolution of IEEE 1149.1 Standard • SCAN Buffers • System Test Products • Other IEEE 1149.1 Devices

TELECOMMUNICATIONS—1992

COMBO and SLIC Devices • ISDN • Digital Loop Devices • Analog Telephone Components • Software
Application Notes

VHC/VHCT ADVANCED CMOS LOGIC DATABOOK—1993

This databook introduces National's Very High Speed CMOS (VHC) and Very High Speed TTL Compatible CMOS (VHCT) designs. The databook includes Description and Family Characteristics • Ratings, Specifications and Waveforms Design Considerations and Product Datasheets. The topics discussed are the advantages of VHC/VHCT AC Performance, Low Noise Characteristics and Improved Interface Capabilities.

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