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DP8492VF Integrated Read Channel

General Description

The DP8492 Hard Disk Data Path Electronics integrated circuit incorporates a pulse/servo detector, a data synchronizer, a frequency synthesizer and write precompensation circuitry onto a single chip, providing a near complete serial data channel solution for mass storage systems (excepting encoder/decoder (ENDEC), and read/write preamplifier). The chip receives data from the read preamplifier, peak detects the read pulses for both data and embedded servo information and resynchronizes the data. The chip operates at data rates from 7.5 Mbit/sec to 33 Mbit/sec and is specifically designed to address multiple data rates by the incorporation of multiplexed pulse detector filters, variable equalization (or variable bandwidth) and a complete frequency synthesizer. A four-bank, on-chip control register allows the user to configure general chip functions. At V_{CC} power-up, the chip self-configures by presetting all bits within the control register to a predetermined operating set-up. Independent ("selective") power-down control for all three major blocks within the chip is provided via the control register, allowing unused functions to be shut down for power reduction while needed portions remain operative. No control register information is lost during selective power-down. Ten power and ground pins are provided to isolate major functional blocks and allow for independent V_{CC} filtering, thus enhancing noise immunity. The circuit is fabricated with a bipolar/CMOS process well suited to high-performance analog, digital and combined analog/digital functions.

The pulse detector section employs user-programmable equalization (pulse slimming) and has connections for two independent external filters to allow multiple data rate selection. The filters may be configured either for peaking (pulse slimming) or variable bandwidth. Digitally-controlled current-injection equalization is employed, requiring no additional external components. Four gated servo detectors are incorporated for recovery of quadrature embedded servo information. A proprietary, self-timing gating qualification technique enhances off-track noise rejection. A pattern-insensitive, fast responding AGC (with HOLD function) allows rapid head-switch settling and embedded servo normalization. A delayed, programmable, low impedance switch at the pulse detector input offers rapid recovery from write mode. Programmable delay (4 steps) in the qualification channel provides additional baseline noise rejection.

The data synchronizer incorporates zero-phase start (ZPS) and a digitally controlled window strobe function which allows 1 ns step increments about the window center. The VCO is fully integrated, requiring no external components, and provides a wide dynamic range. Data windowing is based on precise VCO duty cycle symmetry (in contrast to delay line based centering). An internal silicon delay line, used to establish the phase detector retrace angle, can derive its delay reference from either the synchronizer or synthesizer VCO period. The charge pump output and VCO input are provided as separate pins, allowing ample design flexibility in the external loop filter. Frequency lock may be employed if desired within the synchronization field. Charge pump (phase detector) gain may be selected to remain constant or to vary either by a factor of two or four and can be set to switch at the internal detection of lock or manually as instructed via the CPGAIN pin and the control register.

An on-chip frequency synthesizer, capable of producing a number of frequencies from a single external reference source, generates synchronizer reference. The synthesizer frequency selection is controlled via a user programmable, 10-bit control word within the control register. The user has full control over both the input divider and feedback divider programming. All blocks within the synthesizer, excepting the RC loop filter, are fully integrated. The loop filter resides external to the chip giving the user full control over the PLL's dynamics.

The synthesizer was incorporated as an extension of previous Read Channel products to further simplify customer applications in several areas. In a single data rate application, the synthesizer allows the user to use a Crystal Oscillator with a different frequency from that of the code rate. This will enable the user to choose a less expensive or more readily available crystal, especially when operating at very high code rates. For tape drive applications, the synthesizer allows the drive employing it to be backward compatible with previous designs operating at different data rates.

A write precompensation circuit is included which provides independent control of early and late precompensation settings to accommodate the asymmetrical pulses generated by thin-film and metal-in-gap (MIG) heads.

The DP8492 is available in an 80 pin PQFP package. The DP8492VF operates off of a single +5V supply.

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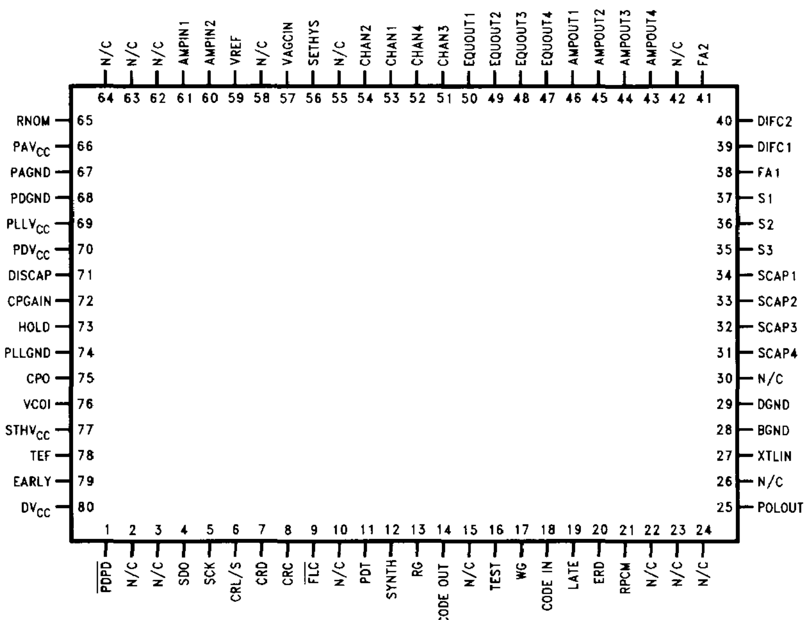
Features

- NRZ data rates up to 33 Mbit/sec
- Precompensation data rate to 25 Mbit/sec
- Single, +5V power supply
- Directly addresses multiple data rate requirements
  — Dual-filter pulse detector for band selection
  — Fully integrated frequency synthesizer
- TTL compatible inputs and outputs
- Partitioned power-down control and separate power control pin for the pulse detector/servo
- Variable equalization (pulse slimming) or variable bandwidth requiring no additional external components
- Programmable-delay impedance switch (clamp) at pulse detector input
- Self-timing qualification channel for increased immunity to off-track noise
- Pattern-insensitive, fast AGC for rapid head-switch settling and embedded servo normalization
- Four gated detectors for quadrature embedded servo detection
- Built-in AGC hold for embedded servo
- Programmable qualification channel delay
- Dual-gain data synchronizer PLL requiring no external high-frequency elements, data rate setting components, external adjustments or precision components
- Digitally controlled synchronizer window strobing
- Zero-phase start synchronizer lock acquisition
- Two-port synchronizer PLL filtering
- Delay line tracking select—Synthesizer or synchronizer
- Frequency lock option for 2T or 3T synchronization field (preamble)
- Write data precompensation with separate control of early and late shift magnitudes

Connection Diagram



TL/F/11709–1

FIGURE 1. DP8492 Pinout for PQFP (80-Lead)
Order Number DP8492VF
See NS Package Number VF80A

Pin Descriptions

PQFP	Description
POWER SUPPLY AND GROUND PINS	
66	Pulse Detector Analog V_{CC} (PAV_{CC}) 5V +5%, −10%
67	Pulse Detector Analog Ground (PAGND)
68	Pulse Detector Digital Ground (PDGND)
69	Synchronizer PLL Analog V_{CC} ($PLLV_{CC}$) 5V +5%, −10%
70	Pulse Detector V_{CC} (PDV_{CC}) 5V +5%, −10%
74	Synchronizer and Synthesizer PLL Analog Ground (PLLGND)
77	Synthesizer PLL Analog V_{CC} ($STHV_{CC}$) 5V +5%, −10%
80	PLL Digital V_{CC} (DV_{CC}) 5V +5%, −10%
28	Input/Output Buffer Ground (BGND)
29	PLL Digital Ground (DGND)
TTL LEVEL LOGIC PINS	
72	**CHARGE PUMP GAIN (CPGAIN):** Selects gain of charge pump.
73	**COAST/AGC HOLD (HOLD):** Freezes the pulse detector AGC level for the reading of the servo burst. Also disables phase comparisons within the Synchronizer (read mode only), allowing the PLL to coast.
79	**EARLY:** Selects or de-selects early write precompensation. A logic high state selects the code out pulse output to shift early by an amount determined by the control register setting and an external RC circuit. A logical low state selects no early precompensation.
1	**$\overline{\text{PULSE DETECTOR POWER DOWN}}$ ($\overline{\text{PDPD}}$):** When held at a logical low state, this pin selectively powers down the pulse detector/servo section.
4	**SYNC DATA OUTPUT (SDO):** Resynchronized data directly from the synchronizing PLL block.
5	**MULTIPLEXED SYNC CLOCK OUTPUT (SCK):** Selects either synchronizer or synthesizer clock signal. The synchronizer clock is selected during Read mode while the synthesizer clock is selected during non-read mode. Multiplexing is done without glitches.
6	**CONTROL REGISTER LATCH/$\overline{\text{SHIFT}}$ (CRL/$\overline{\text{S}}$):** A logical low state allows the CONTROL REGISTER CLOCK to shift data into the control register via the CONTROL REGISTER DATA input. A logical high state latches the data into the addressed bank of latches and issues the information to the appropriate circuitry.
7	**CONTROL REGISTER DATA (CRD):** Control register data input.
8	**CONTROL REGISTER CLOCK (CRC):** Positive-edge-active control register clock input.
9	**$\overline{\text{FREQUENCY LOCK CONTROL}}$ ($\overline{\text{FLC}}$):** Selects or de-selects the frequency lock function during a read operation. This pin has no effect with READ GATE deasserted. Frequency lock is automatically employed for the full duration of the time READ GATE is deasserted regardless of the level of the $\overline{\text{FLC}}$ input. With READ GATE at a logical high state and $\overline{\text{FLC}}$ at a logical low state the PLL is forced to lock to the pattern frequency selected in the control register. When $\overline{\text{FLC}}$ is at a logical high state the frequency lock action is terminated and the PLL employs a pulse gate to accommodate random disk data patterns. There are no setup or hold timing restrictions on $\overline{\text{FLC}}$ assertion or deassertion.
11	**PREAMBLE DETECTED (PDT):** Issues a logical high state following the assertion of READ GATE, the completion of the zero phase start sequence and the detection of approximately 16 sequential pulses of 2T or 3T period preamble. Following preamble detection the output remains latched until READ GATE is deasserted. The PREAMBLE DETECTED output will be at a logical low state whenever READ GATE is inactive.
12	**SYNTHESIZER REFERENCE OUTPUT (SYNTH):** Continuous reference signal from the frequency synthesizer. At V_{CC} power-up, this pin is in the inactive state (a logical low state) and can be enabled via the control register. The output frequency will be the same as the media code clock rate.
13	**READ GATE (RG):** A mode control input from the controller, active high for a read operation. There are no set-up or hold timing restrictions on READ GATE assertion or deassertion.

Pin Descriptions (Continued)

PQFP	Description
14	**CODE OUT:** Precompensated encoded data to be written to the disk. The sense of the output can be selectively inverted to allow the active edge to be either the positive or negative transition, determined via a bit in he control register. The default at V_{CC} power-up is positive-edge-active.
16	**TEST PIN:** This pin is used for production test. Make no connection to this pin.
17	**WRITE GATE (WG):** Write mode control input, active high (logical one). Pulse detector inputs AMPIN1 and AMPIN2 (see below) are held in a low impedance state when WG is at a logical high state. There are no set-up or hold timing requirements for the assertion or deassertion of WRITE GATE.
18	**CODE INPUT (CODE IN):** Input to the write precompensation circuit.
19	**LATE:** Selects or deselects late write precompensation. A logical high state selects the pulse output to shift late by an amount set in the control register and external RC circuit. A logical low state selects no late precompensation.
20	**ENCODED READ DATA (ERD):** Bidirectional pin which can be selected via the control register to 1) remain inactive at a logical-low state (V_{CC} power-up default condition), 2) issue raw pulsed data (post pulse detector) as an output, or 3) admit pulsed data to the synchronizer as an input. The pulsed data is always internally issued to the synchronizer unless the input mode is selected.
25	**POLARITY OUTPUT (POLOUT):** This open-collector TTL signal is the output of the comparator with hysteresis. The logical polarity of this signal corresponds to the polarity of the signal at the channel input pins.
27	**CRYSTAL IN (XTLIN):** Synthesizer reference frequency input; for connection of a crystal (future option), or for direct TTL input of a reference frequency source. Duty cycle is not critical.

PQFP	Description
35–37	**SERVO #3–#1 (S3, S2, S1):** When the AGC HOLD pin is at a logical high state, these TTL input pins control the gating action of the gated servo peak detectors. These pins are configured in gray code to select one of four servo channels. When the AGC HOLD is at a logical low state, these pins select the discharge of the servo channels and the operating mode of the AGC. The AGC can be made to operate in a fast or a slow mode. The mode of the AGC can be changed on the fly using these pins.
ANALOG SIGNAL PINS	
51–54	**TIMING/GATING CHANNEL INPUT/SERVO INPUT (CHAN3, CHAN4, CHAN1, CHAN2):** Multiplexed inputs from the external channel filters to the differentiator, AGC amplifier, servo channel and qualification channel. CHAN1 and CHAN2 are connected to the output of channel filter A, CHAN3 and CHAN4 are connected to the output of channel filter B. These inputs are switched by the control register to select the appropriate channel filter for multiple data rates.
56	**SET HYSTERESIS (SETHYS):** The voltage at this pin determines the amount of hysteresis for the hysteresis comparator. This level should be set high enough to eliminate noise which might occur in the shoulder region between pulses.
57	**AGC VOLTAGE INPUT (VAGCIN):** The voltage at this pin controls the gain of the gain controlled amplifier.
59	**REFERENCE VOLTAGE (VREF):** Reference voltage input to the AGC circuit for controlling the peak-to-peak signal swing at the channel input pins.
60, 61	**AMPLIFIER INPUT 1/AMPLIFIER INPUT 2 (AMPIN2, AMPIN1):** Preamplified, analog, coded data signal read from the disk. These pins go to a low impedance state when WG is at a logical high state and remain low impedance for either 1.7 μs or 3.4 μs (programmable) after WG is deasserted.

Pin Descriptions (Continued)

PQFP	Description
65	**$R_{NOMINAL}$ (RNOM):** Synchronizer charge pump current setting resistor pin, internally biased to ½ V_{CC}. A resistor is connected from this pin to ground.
71	**DISCHARGE CAPACITOR (DISCAP):** A parallel RC combination tied from this pin to ground sets the minimum operational frequency and decay characteristics of the AGC. The voltage at this pin can also be used for dynamic hysteresis.
75	**CHARGE PUMP OUTPUT (CPO):** Output from the synchronizer PLL charge pump; connected to the external loop filter input.
76	**VOLTAGE CONTROLLED OSCILLATOR INPUT (VCOI):** Input to the voltage control block for the synchronizer VCO; connected to the external loop filter output.
78	**TIMING EXTRACTOR FILTER (TEF):** Filter node for the synthesizer PLL. An external resistor and capacitor loop filter is tied in series between this pin and ground.
21	**$R_{PRECOMPENSATION}$ (RPCM):** RC timing node for write data precompensation. From this pin, a resistor is tied to V_{CC} and a capacitor is tied to ground.
31	**SERVO CAPACITOR 4 (SCAP4):** Connection point for the peak detector capacitor for the embedded servo gated detector. The DC level on this capacitor represents the amplitude of one of four servo bursts. **NOTE:** When the "Output Internal Signals" mode is selected through the control register, the signal on this pin becomes the output of the selectable delay block.
32	**SERVO CAPACITOR 3 (SCAP3):** (see SCAP4 definition) **NOTE:** When the "Output Internal Signals" mode is selected through the control register, the signal on this pin becomes the output of the time channel zero cross detector.
33	**SERVO CAPACITOR 2 (SCAP2):** (see SCAP4 definition) **NOTE:** When the "Output Internal Signals" mode is selected through the control register, the signal on this pin becomes one of the differential outputs from the differentiator.
34	**SERVO CAPACITOR 1 (SCAP1):** (see SCAP4 definition) **NOTE:** When the "Output Internal Signals" mode is selected through the control register, the signal on this pin becomes one of the differential outputs from the differentiator.
38, 41	**FILTERED ANALOG PINS (FA1, FA2):** Buffered channel input signal after the channel input switches.
39, 40	**DIFFERENTIATOR CAPACITOR (DIFC1, DIFC2):** Connection points for differentiator components (typically a resistor, capacitor and inductor).
43–46	**GAIN CONTROLLED AMPLIFIER OUTPUTS 1–4 (AMPOUT4, AMPOUT3, AMPOUT2, AMPOUT1):** These are two pair of complimentary, open collector (current source) outputs from the gain controlled amplifier, for connection to the inputs of two external channel filters (for zoned data recording applications); AMPOUT1 and AMPOUT2 are connected to channel Filter A and AMPOUT3 and AMPOUT4 are connected to channel Filter B. Each filter's output must be externally terminated with a resistor connected to the +5V supply.
47–50	**EQUALIZATION AMPLIFIER OUTPUTS 1–4 (EQUOUT4, EQUOUT3, EQUOUT2, EQUOUT1):** These are two pair of complimentary, open collector (current source) outputs from the gain controlled amplifier which provide controlled, out of phase, current injection into the channel filters for pulse slimming purposes. When connected in-phase, they provide variable bandwidth. EQUOUT1 and EQUOUT2 are connected to channel Filter A and EQUOUT3 and EQUOUT4 are connected to channel Filter B, just after the first inductor in each. The signal current in EQUOUT1 and EQUOUT3 is in phase with the signal current in AMPOUT2 and AMPOUT4.

Pin Descriptions (Continued)

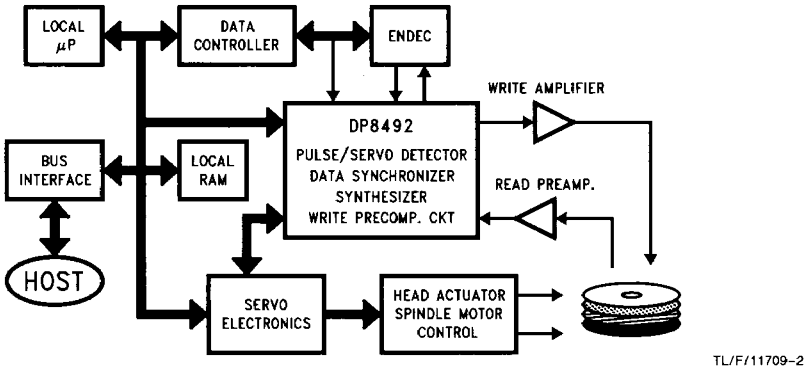


FIGURE 2. DP8492 in a Typical Disk Drive System

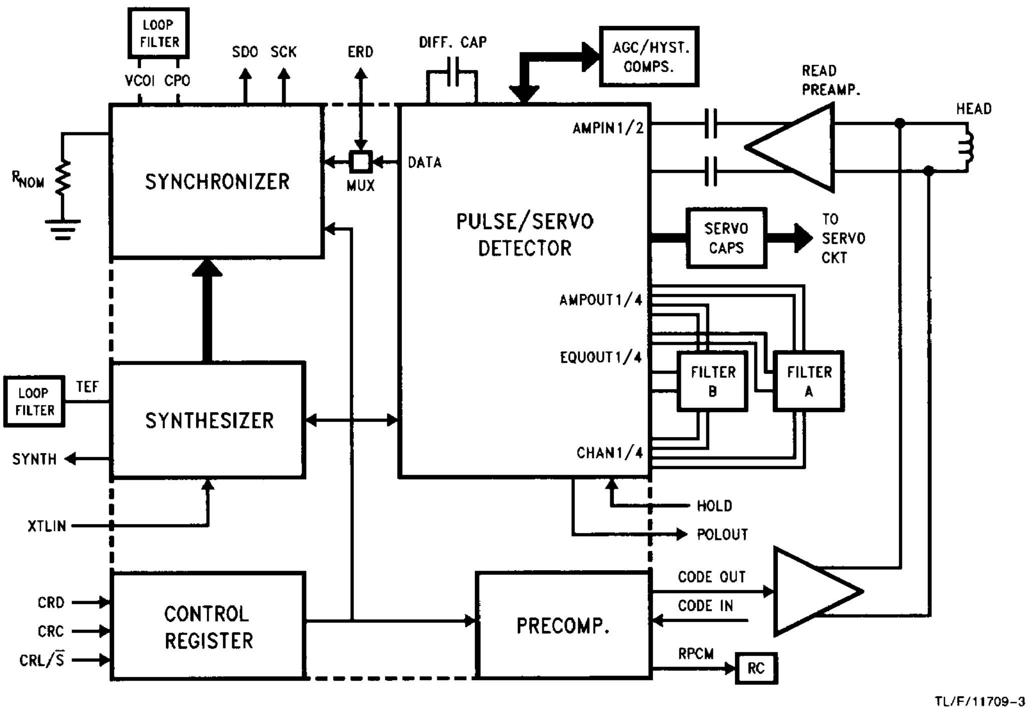


FIGURE 3. DP8492 General Block Diagram

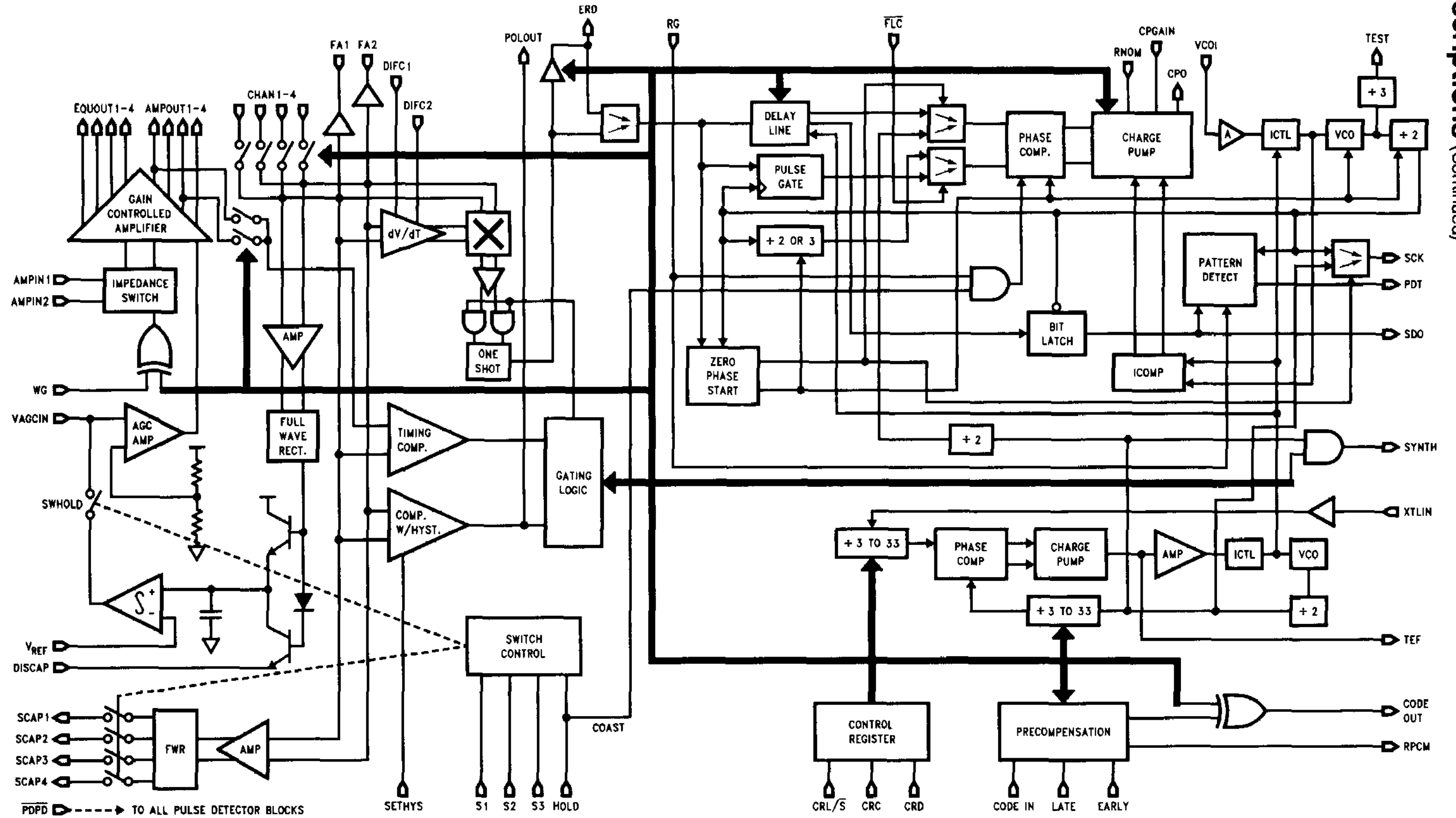


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FIGURE 4. DP8492 Block Diagram

Control Register

The control register (CR) is comprised of a 20-bit serial shift register (18 data bits and two address bits) and four banks of latches (see *Figure 5*). The latches are segmented into four subsections, three of which are 18 bits in length and one which is 4 bits in length, to allow the user to load/reload subsets of control bits without having to reenter the entire contents of 58 bits. Information is strobed into the shift register via the CONTROL REGISTER DATA (CRD) input on the positive edge of CONTROL REGISTER CLOCK (CRC) input with the CONTROL REGISTER LATCH/$\overline{\text{SHIFT}}$ (CRL/$\overline{\text{S}}$) pin at a logical low state, and is parallel-transmitted to one of the four latch banks when CRL/$\overline{\text{S}}$ is taken to a logical high state. Bit positions 2 through 19 contain the control information; the last two bits shifted into the shift register (positions 0 and 1) are the two address bits which call out which of the four latch banks is to be loaded. Table I lists CR bit names and describes their functions. (Note: POR indicates the Power-On-Reset state forced when V_{CC} is first applied. Selective power-down and re-powering will not reset CR bits into these states.)

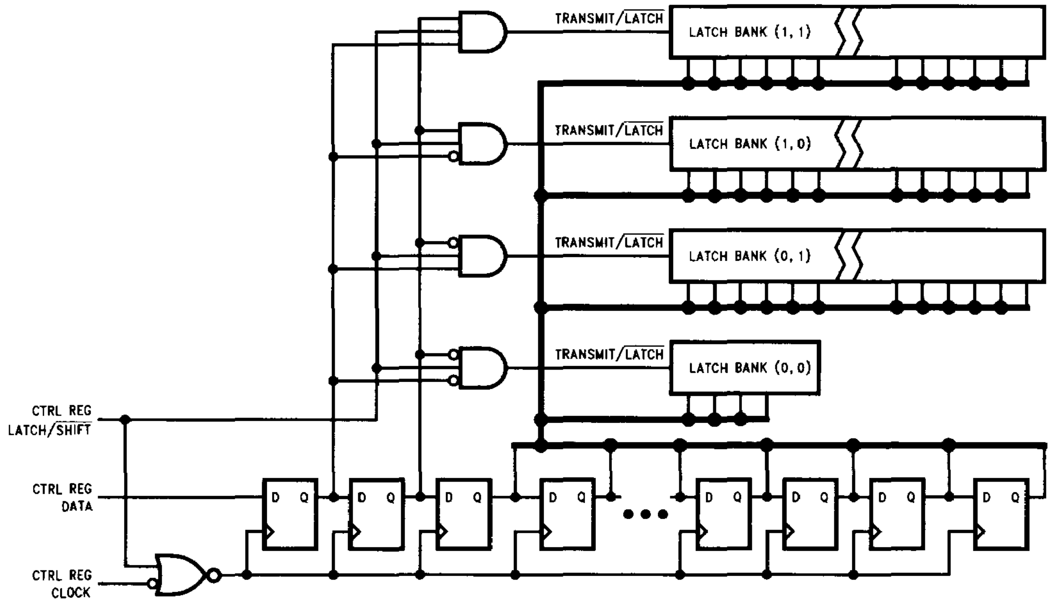

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FIGURE 5. Control Register Block Diagram

TABLE I. Control Register Bit Definitions

Bit	Name	POR	Block	Function
BANK (0, 0)				
0	ADDR0 = 0			Address LSB = 0
1	ADDR1 = 0			Address MSB = 0
2	STR_Sign	0	SYNC	Strobe Sign Bit (0 = Positive, 1 = Negative)
3	STR_0	0	SYNC	Strobe LSB
4	STR_1	0	SYNC	Strobe Intermediate Bit
5	STR_2	0	SYNC	Strobe MSB
BANK (0, 1)				
0	ADDR0 = 1			Address LSB = 1
1	ADDR1 = 0			Address MSB = 0
2	EQ_0	0	PD	Equalization Select 0 (MSB)
3	EQ_1	0	PD	Equalization Select 1
4	EQ_2	0	PD	Equalization Select 2
5	EQ_3	0	PD	Equalization Select 3 (LSB)
6	SW_BAND	0	PD	Select AMP/EQ/CHAN 1 & 2 (3 & 4 if Logical High State)
7	GATE_DEL_1	0	PD	Gating Channel Delay Select 1 (LSB)
8	GATE_DEL_2	0	PD	Gating Channel Delay Select 2 (MSB)
9	HALF~	1	PD	Reduce AMPOUT/EQUOUT Current 50% (Active Low)

Control Register (Continued)

TABLE I. Control Register Bit Definitions (Continued)

Bit	Name	POR	Block	Function
BANK (0, 1) (Continued)				
10	PDATA0	1	SYNTH	Feedback Divider Programming LSB
11	PDATA1	0	SYNTH	Feedback Divider Programming
12	PDATA2	0	SYNTH	Feedback Divider Programming — Division N_{fb} = Binary Value of Control Word + 2
13	PDATA3	0	SYNTH	Feedback Divider Programming
14	PDATA4	0	SYNTH	Feedback Divider Programming MSB
15	PDATA5	1	SYNTH	Input Divider Programming LSB
16	PDATA6	0	SYNTH	Input Divider Programming
17	PDATA7	0	SYNTH	Input Divider Programming — Division N_{in} = Binary Value of Control Word + 2
18	PDATA8	0	SYNTH	Input Divider Programming
19	PDATA9	0	SYNTH	Input Divider Programming MSB
BANK (1, 0)				
0	ADDR0 = 0			Address LSB = 0
1	ADDR1 = 1			Address MSB = 1
2	PWRDWN_WRT	0	PD	Power-Down PD in Write Mode only (1 = Power-Down)
3	PD_PWR_DN~	1	PD	Selective Power-Down (0 = Power-Down)
4	STH_PWR_DN	0	SYNTH	Selective Power-Down (1 = Power-Down)
5	PRE_PWR_DN	0	PRECOMP	Selective Power-Down (1 = Power-Down)
6	EQU_OFF~	1	PD	Disables EQ, Reduces Power (0 = Lower Power, Must Use with HALF~ = 0)
7	PRECOMP_0	0	PRECOMP	Precompensation Control 0, Early
8	PRECOMP_1	0	PRECOMP	Precompensation Control 1, Early
9	PRECOMP_2	0	PRECOMP	Precompensation Control 2, Early
10	PRECOMP_3	0	PRECOMP	Precompensation Control 3, Late
11	PRECOMP_4	0	PRECOMP	Precompensation Control 4, Late
12	PRECOMP_5	0	PRECOMP	Precompensation Control 5, Late
13	SYNC_PWR_DN	0	SYNC	Selective Power-Down (1 = Power-Down)
14	—	—	—	N/A
15	STH_SEL	1	SYNTH	Enable Synthesizer (0 = Bypass)
16	DELAYSEL	0	SYNC	Reference Delay Line to Sync
17	ENSTHO	0	SYNTH	Enables SYNTH Output
18	—	—	—	N/A
19	SLOW	0	PD	Selects 3.4 μs Delay on AMPIN Clamp (1.7 μs if Low)
BANK (1, 1)				
0	ADDR0 = 1			Address LSB = 1
1	ADDR1 = 1			Address MSB = 1
2	BAND_ON_HOLD	0	PD	Switch Bands at HOLD De-assertion
3	DIS_SGQ_CH~	1	PD	Disable Self-Timing Qualification. Chan. (Active Low)
4	OUT_INT_SIG	0	PD	Output Internal Signals
5	—	1	—	N/A (Must be Set to 1)
6	CPGAIN0	1	SYNC	See Table III. Sec. 4.2
7	CPGAIN1	0	SYNC	See Table III. Sec. 4.2
8	CPGAIN2	1	SYNC	See Table III. Sec. 4.2
9	EN_PDOUT	0	SYNC	Enable ERD as Pulse Detector Output
10	SELXERD	0	SYNC	Enable ERD as Data Input
11	TEST	0	PD	Enable Test Mode
12	—	—	—	N/A
13	—	—	—	N/A
14	—	—	—	N/A
15	PREAM_3T	1	SYNC	Selects 3T Preamble (2T if Low) for Frequency Lock
16	INV_WG	0	PD	Selects Polarity of Write Gate (Hi = Inverted WG)
17	INV CODE	0	PRECOMP	Inverts CODE OUT Output
18	FIX_GAIN_1	0	PD	Fixed-Gain Select (Gain = 8 in Full Power Mode)
19	FIX_GAIN_2	0	PD	Fixed-Gain Select (Gain = 4 in Full Power Mode)

Functional Block Descriptions

PULSE DETECTOR DESCRIPTION

The purpose of the pulse detector is to convert the timing information contained in the analog peaks of the disk waveform to a digital signal whose leading edge accurately represents the time position of the peaks. The output of the pulse detector feeds the input to the data synchronizer section and/or is available at the ERD pin (control register option).

Raw disk data from the output of an external read preamplifier is capacitively coupled to the input of the DP8492's gain controlled amplifier (AMPIN1, AMPIN2). These inputs are switched to low impedance when the WRITE GATE input pin is at a logical high state and stay at a low impedance for either 1.7 μs or 3.4 μs after WRITE GATE is returned to a logical low state. The amount of delay is programmable via the control register. During this time any DC offsets accumulated across the input coupling capacitors during the write mode are removed. Also during the write mode, the AGC voltage is held fixed and the input signal to the amplifier is blocked. DC offsets at the output of the amplifier are the same for read or write modes.

The gain controlled amplifier accepts signals in the range of 20 mV to 200 mV peak-to-peak differential and produces a constant 500 mV peak-to-peak differential signal at the channel input pins. The amplifier output current is designed to drive either a 68Ω or 130Ω termination which is selected through the control register. Selecting the higher valued termination resistance reduces the amount of power dissipated in the amplifier output stage but may only be practical at lower data rates.

The gain controlled amplifier supports variable pulse slimming using a technique of injecting out-of-phase current into internal nodes of the channel filter. This technique does not require any additional external components. The amount of pulse slimming is controlled in 16 steps up to a maximum peaking of 10 dB which is selected by the control register. Pulse slimming is supported independently for both channel filters.

Should pulse slimming not be required, the power consumption of the amplifier output stage can be significantly reduced via two bits of the control register. Both the HALF~ bit [bank (0,1) bit 9] and the EQU_OFF~ bit [bank (1,0) bit 6] need to be at a logical low levels to select this reduced power mode. In this lower power mode the amplifier output will drive no lower than a 130Ω termination.

If desired, the equalization ports may instead be connected in-phase at the filter, resulting in a variable bandwidth configuration as an alternative to variable equalization. With this technique, a variable bandwidth over a 1.5 to 1 range is achievable (see *Figure 6*).

The gain of the amplifier is controlled by a fast equal attack, equal decay, pattern insensitive, exponential responding, automatic gain controlled (AGC) amplifier circuit. The AGC allows for fast settling within 3 μs for a 50% change in input signal level. The exponential response of the AGC allows the settling time to be independent of the input signal level. The response is pattern-insensitive because charging or discharging is allowed only in the presence of a signal and thus large shoulder regions will not cause the AGC voltage to droop. A high impedance MOS AGC input pin allows for an AGC hold function with very little leakage of the AGC capacitors' charge.

The input amplifier may be operated in a fixed gain mode where the AGC has no effect on the gain. This mode is selected via two bits of the control register. Three fixed gains (4, 8 or 12) can be selected. To select a fixed gain of 4, bit FIX_GAIN_1 [bank (1,1) bit 18] is set to a logical low state and bit FIX_GAIN_2 [bank (1,1) bit 19] is set to a logical high state. To select a fixed gain of 8, bit FIX_GAIN_1 is set to a logical high state and bit FIX_GAIN_2 is set to a logical low state. To select a fixed gain of 12, both FIX_GAIN_1 and FIX_GAIN 2 bits are set to logical high states.

The differentiator extracts the timing information from the peaks of the disk signal. The timing of the peaks is preserved in the zero crossing of the signal at the differentiator output. A zero cross detector is used in conjunction with the qualification channel to provide noise free, encoded data pulses to the data synchronizer. Fully differential circuits are used throughout the pulse detector to minimize pulse pairing.

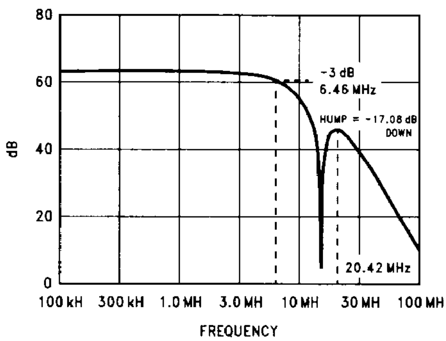
The qualification channel has been designed using a proprietary technique to improve the rejection of off-track noise. Off-track noise is characterized as false peaks that can interfere with the detection of the true peaks and cause soft errors.

A programmable delay (controlled via the control register) has been added in the qualification channel to allow up to 33 ns of delay in approximately 11 ns steps. This delay is added to the qualification signal to add skew with respect to the zero cross detector output from the differentiator. This delay allows for a close alignment of the signals in the qualification and the time channel paths, important for proper noise rejection.

The pulse detector output pulse width is internally fixed to approximately 15 ns, independent of data rate.

Four gated peak detectors are used to detect quadrature embedded servo bursts. When gated on, the peak detector charges an external capacitor to a DC level proportional to the amplitude of the servo burst. The output voltage range of these detectors is large enough for 7 bits of resolution.

Equiripple Error Filter—0.05° Error—10 MHz BW



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Step 5: Ia = 10.48 Ii = 4.0

−3 dB = 6.46 MHz

FIGURE 6. Magnitude Response Variable Bandwidth Configuration

Functional Block Descriptions (Continued)

The gating and discharge of the servo capacitors is controlled by three TTL level logic pins (S1, S2 and S3). The servo channel is designed for very low servo offsets and good gain linearity.

Additional control register features pertinent to the pulse detector include the ability to selectively power-down the pulse detector block or allow the pulse detector to power-down when in write mode. Powering-down the pulse detector in write mode will not power-down the gain controlled amplifier, the amplifier input clamp, amplifier input biasing or channel input biasing. This allows for fast recovery when the pulse detector is returned to read mode.

A mode is also available in which the timing of the channel filter selection and channel input switching is controlled by the AGC HOLD toggling from a low to a logical high state and back to a low logical state. In this way, band switching can be made to occur immediately after an embedded servo sector passes the head, minimizing the settling time after a band switch and allowing the read channel and filters to be completely settled prior to the next embedded servo sector. If this mode is not selected, band switching will occur whenever the control register is instructed to switch bands.

By setting the control register bit OUT_INT_SIG [bank (1, 1) bit 4] to a high logical level, certain selected internal signals are routed to the four servo output pins as observation points. These signals include the fully differential analog output of the differentiator (SCAP1 and SCAP2 pins), the output of the zero cross detector at the differentiator output (SCAP3 pin), and the delayed qualification signal (SCAP4 pin). This mode is useful for the system designer while optimizing the implementation of the pulse detector. This mode would not normally be selected in a production drive as it precludes the operation of these pins for embedded servo.

SYNCHRONIZER DESCRIPTION

The DP8492 data synchronizer consists of a phase-locked loop (PLL) employing a delay line, a pulse gate, a phase-frequency comparator, an analog charge pump, an external passive loop filter, a voltage controlled oscillator, and assorted logic. The synchronizer extracts the code-rate clock from the peak-detected disk data, generates bit frames (windows) for bit capture, and reissues phase-stabilized data. The synchronization window (with strobe setting at nominal, M = 0 position) is centered about the ERD pulses via the 50% duty cycle of the VCO and the time-averaging action of the PLL.

The synchronizer incorporates a zero-phase start (ZPS) block to minimize the phase step seen at the beginning of a lock sequence. Prior to the beginning of a read operation, the synchronizer PLL is locked to the output of the synthesizer to maintain the VCO frequency at the current code rate.

Following READ GATE assertion and the completion of two subsequent VCO cycles, the ZPS block then freezes the synchronizer VCO and restarts it coincidentally with the second data bit following the VCO pause. If frequency lock is employed (READ GATE pin at a high logical level and FREQUENCY LOCK CONTROL (FLC~) pin at a low logical level), a divider is incorporated in the VCO feedback path corresponding to the 2T or 3T sync field being used; the divider is dropped out and the Pulse Gate enabled, once the FLC~ input is taken to a high logical level (see National Semiconductor Mass Storage Handbook, Application Note AN-414, for a discussion of frequency lock). If frequency lock is not employed, the Pulse Gate becomes active immediately at the end of the zero-phase start sequence. At the deassertion of READ GATE, ZPS is again employed, though the accuracy of VCO restart phase alignment is less stringent than when entering a read operation.

The synchronizer provides two pins for PLL filtering purposes, CHARGE PUMP OUTPUT (CPO) and VCO INPUT (VCOI), permitting the use of high-order, two-port filters for optimization of PLL lock characteristics and bit jitter rejection. The VCO control input is buffered by an amplifier with a MOS input device for very high input impedance and negligible bias current. For basic applications, CPO and VCOI may be tied together (single-node) and a simple lead-lag, C||(R + C) filter tied between these pins and ground. PLL filter recommendations for the single-node configuration supplied within this data sheet may be used for device evaluation and basic applications; however, they are general in nature—best performance will be achieved if the Customer optimizes the filter design for the requirements of the specific system involved.

The synchronizer may be selectively powered-down at the user's option via a single bit in the control register; however, this should be done only during a non-read operation, or a discontinuity (glitch) may occur at the SCK output. No control register information is lost during selective power-down. When selective power-down occurs within the synchronizer, an idle-biasing circuit is activated at the CPO pin which will keep the filter voltage at 2 times V_{BE} (approximately 1.5V) above ground potential in order to minimize lock recovery time at re-enabling of power. When selective re-powering occurs, as when V_{CC} power-up occurs, all synchronizer logic is set into the non-read mode and the CPO idle-bias circuit is disabled.

Input/Output Port Control

The ENCODED READ DATA (ERD) pin may be configured via the control register to allow access to the raw (peak detected) data path. The ERD pin is a bidirectional pin which can 1) remain inactive (low; default V_{CC} power-up state) with the pulse detector output passing data internally to the synchronizer input, 2) issue pulse detector output data while the data remains internally transmitted to the synchronizer, or 3) act as an input to the synchronizer with the pulse detector output disabled.

In addition, a special test mode is entered when both port control bits are taken to a logical high state; this allows for two of the control register input pins to change function and act as excitation sources (substitute VCO signals) for clocking internal logic circuitry in the synchronizer and synthesizer (see Control Register Description). When the TEST mode is activated, the VCOs are stopped, the CRD input is redirected to act as a clock source for the synchronizer and the CRC pin as a clock source for the synthesizer. Further information regarding the test mode will be furnished at the Customer's request; contact National Semiconductor Mass Storage Marketing Group or Mass Storage Applications Group.

Synchronizer I/O pin configuration is described in Table II. Note that the cryptic control bit names are general in nature and assigned for convenience; they do not apply literally to all port selection cases.

Functional Block Descriptions (Continued)

TABLE II. Synchronizer I/O Pin Control Truth Table

Control Register Bits Bank (1, 1)		I/O Port Mode	
(10) SELXERD	(9) EN_PDOUT	ERD	TEST MODE
0	0	Hi-Z	Off
0	1	Output	Off
1	0	Input	Off
1	1	Input	On

The synchronizer Pulse Gate is partitioned into two sections; the SYNC DATA Bit Latch and the VCO Gate (see *Figure 7*). The Bit Latch, operating independently of VCO Gate, generates the data synchronization window at the code clock rate based on the 50% duty cycle of the synchronizer VCO clock. 50% duty cycle symmetry in the VCO (or Code) clock is produced by division of a 2X oscillator signal by a differential ECL toggle flip flop. This symmetry-based technique eliminates reliance on the absolute value of the delay line for nominal window centering (see section on Window Strobing). The on-chip silicon delay line is employed in conjunction with the VCO Gate to align the phase detector window (retrace angle). The delay magnitude, one-half of the period of the VCO clock, will track either the synthesizer or the synchronizer VCO as selected via the control register. The synthesizer VCO is selected as the delay reference automatically at V_{CC} power-up. Synchronizer-derived delay reference may be useful in applications where precise delay tracking of data rate variations (e.g., in tape drive systems) is desired. With either selection, the delay tracks data rate variations automatically, and because it is referenced to an external frequency source, it is insensitive to external component tolerance, supply voltage, temperature, and IC process variations.

The synchronizer employs a digital phase comparator (non-harmonic frequency discriminator) which, when frequency lock is enabled, will force the frequency of the VCO toward the frequency of the reference input regardless of the magnitude of the frequency difference. The function of the phase comparator circuit can be represented in the simplified form of *Figure 8*. The AND reset path has sufficient delay added to eliminate any "dead-zone" in the phase detector transfer function. The DP8492 also provides an AGC

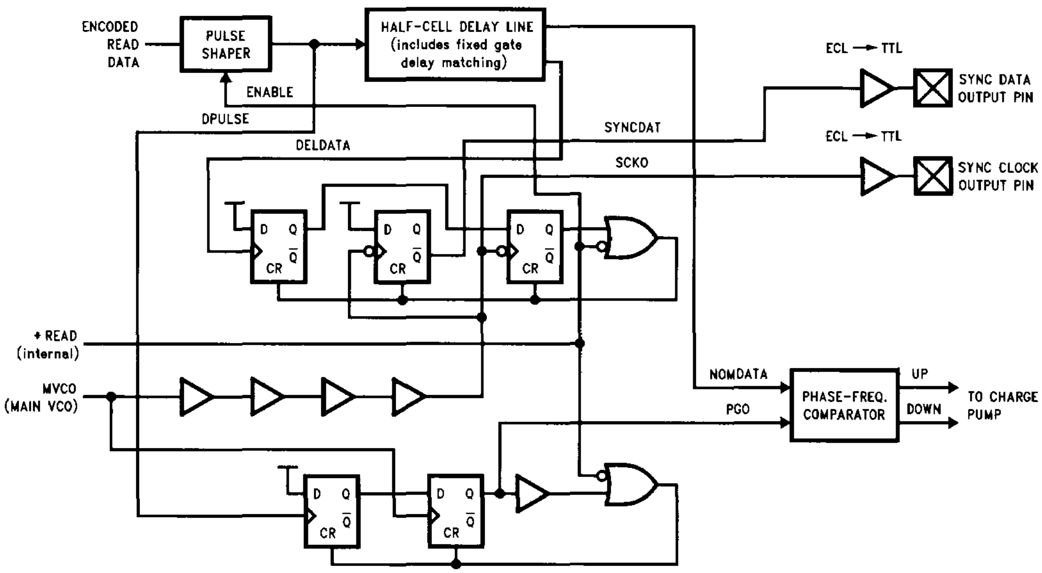

FIGURE 7. Pulse Gate and SYNC DATA/CLK Ports (Logic is ECL except in/out ports)

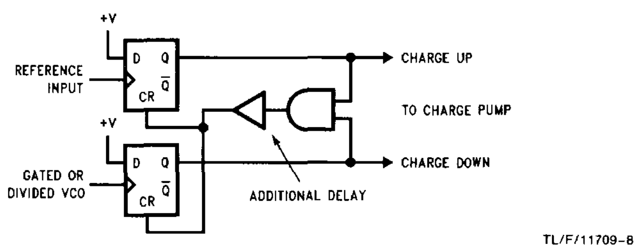

FIGURE 8. Simplified Digital Phase—Freq. Comparator

Functional Block Descriptions (Continued)

HOLD/COAST control input, operable only during the read mode, which serves both to freeze the AGC level in the pulse detector and to clear the phase comparator, disabling charge pump action. This function is made available to allow the PLL to be set to free-run, undisturbed, during servo bursts or while a detectable defect is being read from the media. External data controller circuitry is responsible for the detection of the servo burst or defect and for issuing the HOLD command to the DP8492.

The charge pump is a digitally gated, bidirectional current source with selectable gain whose current flow is regulated by the digital phase comparator circuit. The net current at the CHARGE PUMP OUTPUT (CPO) pin reflects the magnitude and sign of the phase error seen at the input of the phase comparator. The transfer function from the phase comparator input to the charge pump output has a sawtooth characteristic from $-\pi$ to $+\pi$ in phase (harmonic) mode, or monotonically extends to the operating limit of the VCO in frequency (non-harmonic) mode. The CPO pin is connected externally to a passive component network whose impedance translates the aggregate charge pump current into a voltage for the VCO INPUT while providing a low-pass filter function for the PLL. The matched sourcing and sinking current generators' operating currents are set via the R_{NOM} pin, which is connected to an external resistor whose opposite terminal is connected to ground. The R_{NOM} pin will self-bias to ½ V_{CC}. Charge pump gain can be made to self-attenuate at the assertion of an internal lock detect signal by a selectable factor (1, 2 or 4). If the internal lock detect signal has been selected for gain control, the attenuation will be removed at the deassertion of READ GATE. The charge pump gain options are selected via the control register and are described in Table III. The charge pump gain can be also controlled by the CPGAIN pin. If the appropriate code is entered into the control register, the CPGAIN pin will chose high gain at a logical low level and low gain at a logical high level. Note that the bit names are general and assigned for convenience; they do not apply literally to all CP gain cases. "CP Gain" refers to the absolute value of amplification of current between the R_{NOM} pin and the CHARGE PUMP OUTPUT (CPO) when either sourcing or sinking action is gated-on. It is recommended the charge pump operating current be kept as high as practical (using the minimum R_{NOM} value and selecting the higher values of programmable CP gain). This minimizes the resulting impedance of the loop filter for any given application, maximizing environmental noise immunity.

The charge pump has a gain peaking characteristic around the zero phase error point, as shown in *Figure 9.* The peak is approximately 1.9 times the nominal gain (charge pump gain becomes $1.9 \times K1 \times V_{CC}/2R_{NOM}$) and should be taken into account in the calculation of loop filter components and loop dynamics. K1 is the programmable gain factor of 1, 2, or 4 in the charge pump.

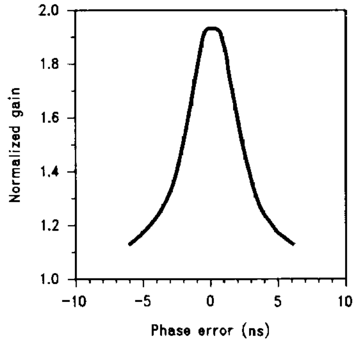

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FIGURE 9. Charge Pump Gain vs Phase Error

The synchronizer VCO is a fully integrated oscillator (no external components) whose frequency is an exponential function of the voltage at the VCOI pin. The VCO block contains a 2X oscillator (two times the media code clock rate) which is divided by two by differential ECL logic in order to produce the necessary 50% duty cycle 1.5F (code rate) VCO waveform for window generation. The exponential VCO transfer characteristic produces a VCO gain which is directly proportional to data rate—while at any single operating frequency the VCO gain characteristic closely approximates linear behavior (see 1988 ISSCC Digest of

TABLE III. Charge Pump Gain Control Truth Table

Control Register Bits, Bank (1, 1)			CPGAIN Pin	Lock Detected (internal)	CP Gain
(Bit 8) CPGAIN2	(Bit 7) CPGAIN1	(Bit 6) CPGAIN0			
0	0	0	X	X	4
0	0	1	X	X	4
0	1	0	X	X	2
0	1	1	X	X	1
1	0	0	X	0	4
1	0	0	X	1	2
1	0	1	X	0	4
1	0	1	X	1	1
1	1	0	0	X	4
1	1	0	1	X	2
1	1	1	0	X	4
1	1	1	1	X	1

Functional Block Descriptions (Continued)

Technical Papers, "A 33 Mb/s Data Synchronizing Phase-Locked Loop," for a discussion of an exponential gain VCO in data recovery applications). The data rate dependency of loop gain causes the PLL bandwidth to track zoned data recording data rate variations (BW varies with the square root of the gain).

The synchronizer VCO is constrained at all times to operate within a frequency swing of approximately ±50% of the synthesizer's operating frequency. Internal frequency detector/comparator circuitry senses when the 50% boundary is overrun and forces the charge pump to move the synchronizer VCO back toward the SYNTH frequency until the 50% constraint is again satisfied—thus preventing VCO runaway in the event of loss of lock or during extended periods where ENCODED READ DATA is not present. Additionally, this technique causes the filter node voltage to behave as if a soft voltage clamp were present at the CHARGE PUMP OUTPUT, preventing the control voltage from drifting outside of its operating range and extending lock recovery time.

The synchronizer VCO Control block employs a positive-sense feed-forward bias signal derived from the synthesizer which forces the VCOI pin to remain at a relevantly constant voltage independent of data rate. This can give the misleading impression that a very high synchronizer VCO gain exists if the synchronizer VCO is varied coincidentally with the synthesizer VCO. Gain of the synchronizer VCO must only be measured with the synthesizer frequency held constant in order to prevent the bias normalization circuitry from effecting the VCOI bias point.

The SCK pin is provided so that an external ENDEC can use the VCO clock from either the synchronizer (read mode) or synthesizer (non-read mode). The multiplexer switches from synthesizer VCO to synchronizer VCO only after ZPS occurs when entering the read mode and, when exiting the read mode, switches back to the synthesizer VCO prior to the occurrence of ZPS. All multiplexing is done with no glitches.

Eleven position window strobing (nominal position and 5 steps on either side of center) is available via the control register. Strobing on either side of nominal is achieved via a proprietary delay line technique (patent pending) which modulates the window position without any disturbance of the PLL's phase equilibrium or movement of the retrace angle. In addition, strobe response is immediate, requiring no settling time. The first two positions on either side of nominal ($M = -1, -2, +1$, or $+2$) are fixed-delay steps of approximately 1 ns each (see AC Electrical Characteristics Table), intended for fine-stepping functions such as window deskewing. All remaining steps (-3 through -5 and $+3$ through $+5$) are equal and dependent on data rate, each step being one sixteenth (6.25%) of the window width.

SYNTHESIZER DESCRIPTION

The synthesizer block is a phase-locked loop with programmable dividers at its input port and in its feedback path. A single, external node (Timing Extractor Filter, or TEF) is provided for passive components for the synthesizer PLL filter. The resulting synthesized output, F_{SYNTH}, is the code rate clock used for encoding and as a reference signal for the synchronizer during the non-read mode. The frequency of F_{SYNTH} is the reference input frequency multiplied by the modulus of the feedback divider and divided by the modulus of the input divider:

$$F_{SYNTH} = F_{REF} \times N_{FEEDBACK} / N_{INPUT}$$

The input divider modulus N_{INPUT} (N_{IN}) is set via control register Bank 01, bits 15–19 (LSB–MSB, resp.), and feedback modulus $N_{FEEDBACK}$ (N_{FB}) is set via control register Bank 01, bits 10–14 (LSB–MSB, resp.). The value of each N modulus is equal to the binary value of its 5-bit control word PLUS 2. This gives each divider a division range of 3 to 33.

N_{INPUT} (N_{IN}) = [Binary value of control register Bank 01, bits 15–19] + 2

$N_{FEEDBACK}$ (N_{FB}) = [Binary value of control register Bank 01, bits 10–14] + 2

A zero value control word (all bits low) for either divider is *not allowed* (divider operation stops). At V_{CC} power-up, the divider control words are both automatically set to 00001, and thus the ratio N_{FB}/N_{IN} is $(1 + 2)/(1 + 2) = (3)/(3)$, or unity.

TABLE IV. Window Strobe Control Truth Table

Control Register Bits, Bank (0, 0)				Typical Window Shift
STR_2	STR_1	STR_0	STR_SIGN	
1	0	1	1	$-(0.188)t_{VCO} - 2$ ns
1	0	0	1	$-(0.125)t_{VCO} - 2$ ns
0	1	1	1	$-(0.062)t_{VCO} - 2$ ns
0	1	0	1	−1.2 ns
0	0	1	1	−0.6 ns
0	0	0	1	None
0	0	0	0	None
0	0	1	0	+0.6 ns
0	1	0	0	+1.2 ns
0	1	1	0	$(0.062)t_{VCO} + 1.2$ ns
1	0	0	0	$(0.125)t_{VCO} + 1.2$ ns
1	0	1	0	$(0.188)t_{VCO} + 1.2$ ns

Note: Strobe selections not shown in Table IV are invalid and should not be used. If an invalid state is inadvertently entered, SDO will become indeterminate, though PLL lock (phase comparator activity) will not be affected.

Functional Block Descriptions (Continued)

The synthesizer may be selectively powered-down via a single bit in the control register, if desired. No control register data is lost during selective power-down. When selective power-down occurs, an idle-bias circuit is activated at the TEF pin which keeps the filter voltage at a typical operating bias of 2 times V_{BE} (approximately 1.5V) above ground potential in order to minimize lock recovery time at reapplication of power.

Note: The synchronizer derives its reference signal, VCO normalization bias and (optionally) its delay line control from the synthesizer; thus the synthesizer must be powered-on for the synchronizer to operate properly. If the synthesizer is powered-down, the synchronizer should be as well.

For systems which require a synthesized master clock, the SYNTH output is made available. The frequency of the SYNTH output will be equal to the recorded media code rate. Should the SYNTH output be employed as a system clock, care should be taken, as with all switching outputs on the DP8492, to minimize capacitive loading (use an external buffer/driver for multiple fan-out applications). The standard, default V_{CC} power-up condition for the SYNTH output pin is the disabled mode (logic-low state) to minimize switching noise. This output should always be left disabled if not needed.

WRITE PRECOMPENSATION CIRCUIT DESCRIPTION

Write data precompensation (optional) is performed via the EARLY and LATE control inputs, by a user-programmable amount. Precompensation timing range is set by an external RC circuit and can be modulated at any time by a six-bit control word in the Control Register. For each step the typical amount of time offset is $t = 8\% \times RC$ where R and C are the external components and the value of C includes stray capacitances at the RPCM pin. Early and late shift controls are independent of one another, each having three control bits and seven displacement steps, including "none" (precompensation enabled, no shift). Independent early/late shift control is intended to allow compensation for the asymmetrical intersymbol interaction characteristic of thin film and metal-in-gap heads.

The leading edge of the CODE OUT output pulse represents the precompensated code bit, and is selectable to be either positive-going or negative-going (i.e., may be inverted via the Control Register).

Note: The leading edge and trailing edge of the CODE OUT output do NOT have a fixed relationship (pulse width will vary with precompensation); thus the trailing edge must NOT be used as the active edge.

The precompensation circuitry may be fully bypassed (and the external RC net omitted if precompensation is not used) by setting Control Register bits PRECOMP—3 through PRECOMP—5 to the low state (default V_{CC} power-up state is low for all precomp CR bits).

TABLE V. Precompensation Truth Table

Control Register Bits, Bank (1, 0)								
Late Shift Control			Early Shift Control			Typical Precompensation Amount		
PRECOMP_5 (12)	PRECOMP_4 (11)	PRECOMP_3 (10)	PRECOMP_2 (9)	PRECOMP_1 (8)	PRECOMP_0 (7)	EARLY	LATE	BYPASS
0	0	0	X	X	X	N/A	N/A	Yes
0	0	1	0	0	1	None	None	No
0	1	0	0	1	0	8%RC	8%RC	No
0	1	1	0	1	1	16%RC	16%RC	No
1	0	0	1	0	0	24%RC	24%RC	No
1	0	1	1	0	1	32%RC	32%RC	No
1	1	0	1	1	0	40%RC	40%RC	No
1	1	1	1	1	1	48%RC	48%RC	No

DC and AC Device Specifications

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
TTL Input Maximum Voltage	7V
Maximum Output Voltage	7V
Maximum Input Current (Note 3)	2 mA
ESD Susceptibility (Note 1)	1500V

General Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5.0	5.25	V
T_A	Operation Ambient Temperature		0		70	°C
T_S	Storage Temperature		−65		150	°C
I_{OH}	High Logic Level Output Current For TTL Type Outputs	Code & Synth Pins			−2000	μA
		Others			−400	μA
I_{OL}	Low Logic Level Output Current For TTL Type Outputs	Code & Synth Pins			20	mA
		Others			8	mA
V_{IH}	High Logic Level Input Voltage		2			V
V_{IL}	Low Logic Level Input Voltage				0.8	V
C_{LOAD}	Capacitive Load On Any TTL Output				15	pF
f_{NRZ}	NRZ Transfer Rate Operating Frequency		7.5		33	Mb/s
f_{VCO}	Synchronizer VCO Operating Frequency		11.25		50	MHz
f_{STH}	Synthesizer VCO Operating Frequency		11.25		50	MHz
f_{XTL}	Crystal Input Frequency Maximum				30	MHz
f_{PCMP}	Maximum Data Rate for Precompensation				25	Mb/s
f_{PDT}	Maximum Data Rate for Preamble Detection				40	Mb/s
$t_{PW(XTL)}$	Width of XTLIN Pulse (High or Low)		12			ns
$t_{PW(ERD)}$	Width of ERD Input Pulse (High or Low)		12			ns
$t_{PW(CRL/\overline{S})}$	Width of CRL/$\overline{S}$ Pulse (High or Low) (Note 2)		40			ns
$t_{SU(CRD)}$	CRD Setup Time with respect to CRC (Note 2)		5			ns
$t_{H(CRD)}$	CRD Hold Time with respect to CRC (Note 2)		20			ns
$t_{H(CRL/\overline{S})}$	CRL/$\overline{S}$ Hold Time with respect to CRC (Note 2)		25			ns
$t_{PW(CRC)}$	CRC Pulse Width (Positive or Negative) (Note 2)		30			ns
I_{RNOM}	R_{NOM} Pin Current		−45		−265	μA
$t_{SU(EARLY)}$	EARLY Setup Time with respect to CODE IN (Note 4)			15 ns−0.4 RC		ns
$t_{H(EARLY)}$	EARLY Hold Time with respect to CODE IN			TBD		ns
$t_{SU(LATE)}$	LATE Setup Time with respect to CODE IN			TBD		ns
$t_{H(LATE)}$	LATE Hold Time with respect to CODE IN (Note 4)			6 ns+1.2 RC		ns
R_{RPCM}	Resistor Value at RPCM pin		512			Ω
t_{CODE}	Min CODE IN pulse spacing, positive edge to positive edge			2.4 RC+40		ns
$t_{WCI(POS)}$	Min CODE IN pulse width, positive pulse			1.1 RC+13		ns
$t_{WCI(NEG)}$	Min CODE IN pulse width, negative pulse			15		ns

Note 1: Human body model is used. (120 pF through 1.5 kΩ)

Note 2: Parameter guaranteed by design or correlation data. No outgoing test are performed.

Note 3: This specification applies to analog pins only. Limit may be overridden by individual pin specification.

Note 4: $t_{SU(EARLY)}$ and $t_{H(LATE)}$ timing requirements should be used to decide signal timing for both EARLY and LATE inputs. RC = RPCM × CPCM.

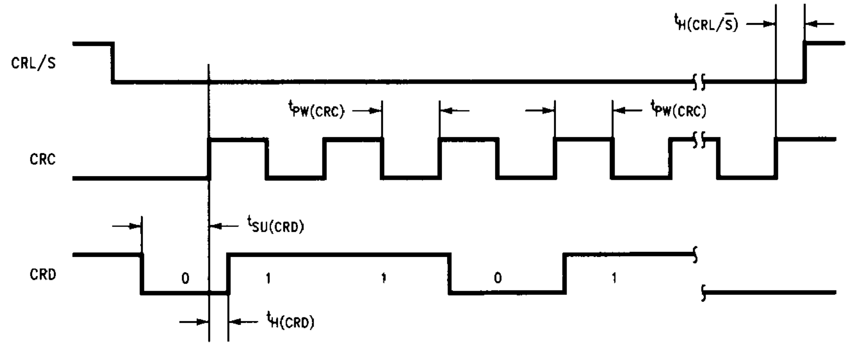

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FIGURE 10. MICROWIRE™ Compatible Control Register Serial Load Timing Diagram

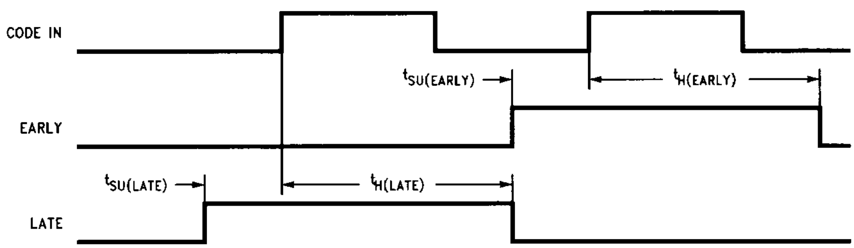

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FIGURE 10.5. EARLY/LATE Precompensation Timing Diagram

General DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Logic Level Output Voltage	V_{CC} = Min, I_{OH} = Max	$V_{CC}-2$	$V_{CC}-1.6$		V
V_{OL}	Low Logic Level Output Voltage	V_{CC} = Min, I_{OL} = Max			0.5	V
I_{IH}	High Logic Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Logic Level Input Current	V_{CC} = Max, V_I = 0.4V			−200	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.125V (Note 1)	−12		−110	mA
I_{CPO}	Charge Pump Output Current	(Notes 2 & 6)	$0.8K_1I_{IN}$		$1.2K_1I_{IN}$	
$I_{CPO\text{-}OFF}$	Charge Pump Output Inactive Current	(Note 2)	−0.8		0.8	μA
I_{TEF}	TEF Output Current (Absolute Value)	1V < V_{TEF} < 2.5V	300	500	900	μA
$I_{TEF\text{-}OFF}$	TEF Output Inactive Current	1V < V_{TEF} < 2.5V	−2		2	μA
I_{VCOI}	VCOI Current	1V < V_{VCOI} < 2.5V	−0.05		0.05	μA
V_{RNOM}	Voltage at R_{NOM} Pin	−265 μA < I_{RNOM} < −45 μA	0.45 V_{CC}		0.55 V_{CC}	V
$V_{CPO(PD)}$	CPO Voltage with Synchronizer Powered Down	−5 μA < I_{CPO} < 5 μA	0.9	1.5	2.1	V
$V_{TEF(PD)}$	TEF Voltage with Synthesizer Powered Down	−5 μA < I_{TEF} < 5 μA	0.9	1.5	2.1	V
$I_{CCR(FP)}$	Supply Current with Full Power Amplifier Output in the Read Mode	V(WG) = 0.3V, All Sections Powered on and Pulse Detector Amp. Full Power Mode Selected			215	mA
$I_{CCW(FP)}$	Supply Current with Full Power Amplifier Output in the Write Mode	V(WG) = 4V, All Sections Powered on and Pulse Detector Amp. Full Power Mode Selected			230	mA
$I_{CC(HP)}$	Supply Current with Half Power Amplifier Output	V(WG) = 0.3V, All Sections Powered on and Pulse Detector Amp. Half Power Mode Selected			200	mA
$I_{CC(EO)}$	Supply Current with Equalization Off	V(WG) = 0.3V, All Sections Powered On (Note 3)			175	mA
$I_{CC(PDW)}$	Supply Current when Powered Down in the Write Mode	V(WG) = 4V, All Sections Powered On (Note 4)			175	mA
$I_{CC(FPD)}$	Supply Current when in Full Power Down Mode	V(WG) = 0.3V, Power Down All Sections of the Chip Via Control Register			130	mA
$I_{CC(PD)}$	Pulse Detector Supply Current with All Other Sections Powered Down	V(WG) = 0.3V (Note 5)			116	mA

Note 1: V_O = 2.125V produces a current closely approximating one half of the true short circuit current, I_{OS}.

Note 2: K1 is the selected charge pump gain constant (1, 2, or 4), I_{IN} = I_{RNOM}, 1V < V_{CPO} < 2.5V. This specification together with $V_{(RNOM)}$ specification result in the following $I_{(CPO)}$ dependance on V_{CC} and $R_{(NOM)}$.

$[(0.36(K1)(V_{CC}))/R_{(NOM)}] < I_{(CPO)} < [(0.66(K1)(V_{CC}))/R(NOM)]$

Note 3: Pulse detector equalization circuitry is turned off by simultaneously programming half power mode and equalization off modes through the control register.

Note 4: Power down in write mode selected through the control register.

Note 5: Power down all sections except the pulse detector and select full power mode for the pulse detector via the control register.

Note 6: I_{CPO} also exhibits variation as a function of phase error.

Pulse Detector DC Electrical Characteristics

Symbol	Circuit Block	Parameter	Conditions	Min	Typ	Max	Units
Z_{IN-AL}	GCA	Amplifier Input Impedance (AMPIN1/AMPIN2)	Nonwrite Mode (Note 1)	1.5	2.1	2.8	kΩ
$Gm_{A(MAX-SO)}$	GCA	Max Amplifier Transconductance—Step 0	$V_{(VAGCIN)}$ = 1V (Notes 2 & 3) All Power Modes	332	485		mA/V
$Gm_{A(MIN-SO)}$	GCA	Min Amplifier Transconductance—Step 0	V(VAGCIN) = 4V (Notes 2 & 3) All Power Modes			5	mA/V
$Gm_{A(FG1-SO)}$	GCA	Amplifier Transconductance in Fixed Gain Mode 1 and Step 0	Control Register Programmed for Fixed Gain Mode 1 (Notes 2 & 3)	70	125	200	mA/V
$Gm_{A(FG2-SO)}$	GCA	Amplifier Transconductance in Fixed Gain Mode 2 and Step 0	Control Register Programmed for Fixed Gain Mode 2 (Notes 2 & 3)	40	70	120	mA/V
$Gm_{A(FG12-SO)}$	GCA	Amplifier Transconductance in Fixed Gain Both Mode 1 & 2 on and Step 0	Control Register Programmed for Fixed Gain Mode 1 & 2 (Notes 2 & 3)	110	187	290	mA/V
$\%Gm_A$	GCA	Max % of Additional Transconductance for Amplifier	(Notes 3 & 4)	148	190	247	%
$\%Gm_E$	EQUAL	Max % of Additional Transconductance for Equalizer	(Notes 5 & 6)	148	190	247	%
K1	GCA & EQUAL	Ratio of Equalization Gain to Amplifier Gain for Pulse Slimming Step 1	(Notes 3, 5 & 7)	0.09	0.12	0.15	
K2	GCA & EQUAL	Ratio of Equalization Gain to Amplifier Gain for Pulse Slimming Step 2	(Notes 3, 5 & 8)	0.17	0.21	0.25	
K4	GCA & Equal	Ratio of Equalization Gain to Amplifier Gain for Pulse Slimming Step 4	(Notes 3, 5 & 9)	0.3	0.33	0.39	
K8	GCA & EQUAL	Ratio of Equalization Gain to Amplifier Gain for Pulse Slimming Step 8	(Notes 3, 5 & 10)	0.39	0.50	0.57	
K15	GCA & EQUAL	Ratio of Equalization Gain to Amplifier Gain for Pulse Slimming Step 15	(Notes 3, 5 & 11)	611	665	726	
V_{Aob}	GCA	Amplifier Output DC Bias Level Operating Range	(Notes 3, 12 & 30)	1.4	1.9		V
V_{Eob}	EQUAL	Equalization Output DC Bias Level Operating Range	(Notes 5, 13 & 30)	1.4	1.9		V
$I_{Aob(FP)}$	GCA	Amplifier Output DC Bias Current, Full Power Mode	Full Power Mode (Notes 31, 32, 3 & 14)	1.9	2.65	3.2	mA/V
$I_{Eob(FP)}$	EQUAL	Equalization Output DC Bias Current, Full Power Mode	Full Power Mode (Notes 31, 32, 5 & 14)	1.3	1.76	2.3	mA/V
$I_{Aob(HP)}$	GCA	Amplifier Output DC Bias Current, Half Power Mode	Half Power Mode (Notes 31, 32, 3 & 14)	0.95	1.3	1.75	mA/V
$I_{Eob(HP)}$	EQUAL	Equalization Output DC Bias Current, Half Power Mode	Half Power Mode (Notes 31, 32, 5 & 14)	0.65	0.89	1.15	mA/V
$I_{Aob(EO)}$	GCA	Amplifier Output DC Bias Current, Equalization Off	Half Power Mode (Notes 31, 32, 3 & 14)		0.32	0.4	mA/V
$V_{th(AGC)}$	AGC	AGC Threshold Voltage	VREF = 0.5V, I(DISCAP) = 10 μA, V(VAGCIN) = 2.5V (Note 15)	375	440	507	mV_{pp}
$Gm_{AGC(FAST)}$	AGC	AGC Transconductance in Fast Mode	V(VAGCIN) = 2.5V, I(DISCAP) = −10 μA (Note 16)	1.1	1.6	2.2	mA/V
$Gm_{AGC(SLOW)}$	AGC	AGC Transconductance in Slow Mode	V(VAGCIN) = 2.5V, I(DISCAP) = 10 μA (Note 17)	200	302	400	μA/V

Pulse Detector DC Electrical Characteristics (Continued)

Symbol	Circuit Block	Parameter	Conditions	Min	Typ	Max	Units
$-I_{AGC(SLEW)F}$	AGC	AGC Slew Current in Fast Mode (Flowing out of Pin)	|V(CHAN1)−V(CHAN2)| = 0.5V, V(VAGCIN) = 2.5V (Note 18)	−170	−240	−310	μA
$I_{AGC(SLEW)F}$	AGC	AGC Slew Current in Fast Mode (Flowing into Pin)	|V(CHAN1)−V(CHAN2)| = 0V, V(VAGCIN) = 2.5V (Note 18)	170	240	310	μA
$-I_{AGC(SLEW)S}$	AGC	AGC Slew Current in Slow Mode (Flowing out of Pin)	|V(CHAN1)−V(CHAN2)| = 0.5V, V(VAGCIN) = 2.5V (Note 19)	−55	−108	−170	μA
$I_{AGC(SLEW)S}$	AGC	AGC Slew Current in Slow Mode (Flowing into Pin)	|V(CHAN1)−V(CHAN2)| = 0V, V(VAGCIN) = 2.5V (Note 19)	120	168	230	μA
FSBP	AGC	Fast Slew Break Point for AGC	V(VACGIN) = 2.5V, I(DISCAP) = −10 μA (Note 20)	25	37	50	%
V_{DISCAP}	AGC	Discharge Capacitor Voltage	I(DISCAP) = −10 μA Measurement made at VthAGC	1.15	1.5	1.85	V
$I_{LEAK(AGC)H}$	AGC	AGC Leakage Current in AGC Hold Mode	HOLD = High, V(VAGCIN) = 2.5V (Note 21)		0.02	0.07	μA
$I_{LEAK(AGC)W}$	AGC	AGC Leakage Current in Write Mode	Pulse Detector Placed in Write Mode V(VAGCIN) = 2.5V (Note 21)		0.02	0.07	μA
$I_{LEAK(AGC)PD}$	AGC	AGC Leakage Current in Full Power Down	Pulse Detector is Powered Downed V(VAGCIN) = 2.5V (Note 21)		0.01	0.07	μA
$Z_{IN(AL)W}$	AMP CLAMP	Amplifier Input Impedance in Write Mode	(Note 22)		30	80	Ω
$I_{clamp(sink)}$	AMP CLAMP	Amplifier Input Clamp Sink Current	(Note 23)	18	20		mA
$I_{clamp(source)}$	AMP CLAMP	Amplifier Input Clamp Source Current	(Note 24)	−18	−20		mA
$Z_{IN(CH)}$	CHAN INPUTS	Channel Input Impedance	(Note 22)	2.4	3.5	6.5	kΩ
$V_{th(HYST)}$	CHAN INPUTS	Hysteresis Comparator Threshold Voltage	Connect 1 kΩ resistor from V_{CC} to POLOUT Pin (Note 25)	0.128	0.150	0.174	V_{PP}
H/R	CHAN INPUTS	Ratio of the Hysteresis Threshold to the AGC Threshold	See Conditions for Vth(HYST) and Vth(AGC)	0.25	0.30	0.35	
I_{SETHYS}	CHAN INPUTS	Set Hysteresis Input Bias Current	V(SETHYS) = 0.3V	−50	−25		μA
I_{VREF}	CHAN INPUTS	VREF Input Bias Current	V(VREF) = 0.5V	−50	−25		μA
I_{DIFC}	CHAN INPUTS	Differentiator Bias Current	V(DIFC2) = 4V or V(DIFC1) = 4V	1.6	1.9		mA
$Z_{SCAP(DIS)}$	SERVO	SCAP Pin Discharge Impedance	V(HOLD) = 0.3V, V(S2) = 4V, V(SCAP 1 thru 4) = 2V (Note 25A)	0.73	1.1	1.4	kΩ
$Av_{QT(gd)}$	SERVO	Servo Channel Gain for Quarter Track Mispositioning	V(HOLD) = 4V (Notes 26 & 26A)	5	5.4	5.8	V/V
$V_{INTERCEPT}$	SERVO	Servo Channel Output Voltage for 0 Vpp Input	V(HOLD) = 4V (Notes 26 & 26B)	14	18.6	22	%
GL_{gd}	SERVO	Gated Detector Gain Linearity	V(HOLD) = 4V (Notes 26, 27 & 27A)		0.23	1	%
VOS_{gd}	SERVO	Gated Detector Output Voltage Offset	V(HOLD) = 4V (Note 28)		2	10	mV
IL_{gd}	SERVO	Gated Detector Leakage Current	V(S1) = V(S2) = V(S3) = 0.3V, V(HOLD) = 4V (Note 29)		0.02	0.07	μA

Pulse Detector DC Electrical Characteristics (Continued)

Note 1: The input pin consists of two resistors tied to a voltage source. This is the resistance of each resistor.

Note 2: Transconductance is measured differentially. Pulse slimming step 0 programmed.

Note 3: AMPOUT1, AMPOUT2, AMPOUT3 and AMPOUT4 pins are measured.

Note 4: Transconductance is measured differentially. Gm is first measured for pulse slimming step 0 at the amplifier output = Gm0a. Gm is measured again but for pulse slimming step 15 at the amplifier output = Gm15a. % GmA = 100(Gm15a-Gm0a)/Gm0a.

Note 5: EQOUT1, EQOUT2, EQOUT3 and EQOUT4 pins are measured.

Note 6: Transconductance is measured differentially. Gm is first measured for pulse slimming step 0 at the amplifier output = Gm0a. Gm is measured again but for pulse slimming step 15 at the equalization output = $Gm15_E$. $\%Gm_E$ = $100(Gm15_E)/Gm0_A$.

Note 7: Transconductance is measured differentially at both the equalization (Gm_E) and amplifier (Gm_A) outputs for pulse slimming step 1. K1 = Gm_E/Gm_A.

Note 8: Transconductance is measured differentiallly at both the equalization (Gm_E) and amplifier (Gm_A) outputs for pulse slimming step 2. K2 = Gm_E/Gm_A.

Note 9: Transconductance is measured differentially at both the equalization (Gm_E) and amplifier (Gm_A) outputs for pulse slimming step 4. K4 = Gm_E/Gm_A.

Note 10: Transconductance is measured differentially at both the equalization (Gm_E) and amplifier (Gm_A) outputs for pulse slimming step 8. K8 = Gm_E/Gm_A.

Note 11: Transconductance is measured differentially at both the equalization (Gm_E) and amplifier (Gm_A) outputs for pulse slimming step 15. K15 = Gm_E/Gm_A.

Note 12: The DC bias voltage level (Vbias) at AMPOUT pins (AMPOUT1, AMPOUT2, AMPOUT3 and AMPOUT4) is reduced until a 2% change in output current is measured. V(Aob) = V_{CC} −Vbias.

Note 13: The DC bias voltage level (Vbias) at EQOUT pins (EQOUT1, EQOUT2, EQOUT3 and EQOUT4) is reduced until a 2% change in output current is measured. V(Eob) = V_{CC} −Vbias.

Note 14: The amplifier input pins (AMPIN1 & AMPIN2) are shorted together. Since the DC bias current is V_{CC} dependent, the specification is expressed as a transconductance. The transconductance is given by the average DC bias current output per pin divided by V_{CC}. The specification is for each pin.

Note 15: The AGC threshold voltage is defined as the equivalent differential peak to peak AC voltage swing across the channel input pins (CHAN1, CHAN2, CHAN3 & CHAN4) that causes the current at VAGCIN pin to equal zero.

Note 16: Channel inputs (CHAN1 and CHAN2) are set at Vth(AGC) + 10 mV and fast AGC mode is selected. Transconductance is measured from the channel inputs (CHAN1 and CHAN2) to the current at the VAGCIN pin. The measurement is made at Vth(AGC). GmAGC(fast) = |I(VAGCIN)/10mV|.

Note 17: Slow AGC mode is selected. The transconductance is measured from channel inputs (CHAN1 & CHAN2) to the current output of the VAGCIN pin. The measurement is made at Vth(AGC). GmAGC(slow) = |I(VAGCIN)/(V(CHAN1)−V(CHAN2))−(½)Vth(AGC)|.

Note 18: Fast AGC mode is selected. Iagc(slew)F is measured at the VAGCIN pin. I(DISCAP) = −10 μA.

Note 19: Slow AGC mode is selected. Iagc(slew)S is measured at the VAGCIN pin. I(DISCAP) = −10 μA.

Note 20: Fast AGC mode is selected. The Fast Slew Break Point (FSBP) is defined as a positive or negative percentage of the AGC threshold voltage (Vthagc). The break point is that voltage above and below Vthagc where the GmAGC(FAST) abruptly increases. The FSBP only occurs for the fast AGC mode. This point is found by increasing or decreasing the differential voltage at the channel inputs (CHAN1 and CHAN2) above and below the AGC threshold, while monitoring the transconductance at the VAGCIN pin. The break point occurs when this transconductance increases by at least 20% above GmAGC(FAST).

Note 21: Measure current into or out of VAGCIN pin for both V(CHAN1)−V(CHAN2) = 0 and V(CHAN1)−V(CHAN2) = 0.5V.

Note 22: The input can be modeled as two resistors tied to a voltage source. This is the resistance of each resistor.

Note 23: The common mode voltage a AMPIN1 and AMPIN2 pins is measured for no current into these pins. Current is the forced into either AMPIN1 or AMPIN2 (not both simultaneously) until the volltage on the pin rises by 1 volt.

Note 24: The common mode voltage a AMPIN1 and AMPIN2 pins is measured for no current out of these pins. Current is the pulled out of either AMPIN1 or AMPIN2 (not both simultaneously) until the voltage on the pin falls by 1 volt.

Note 25: The hysteresis comparator threshold is defined as the minimum differential AC signal across the channel inputs (CHAN1 & CHAN2 or CHAN3 & CHAN4) which causes the voltage on the POLOUT pin to change state. V(SETHYS) = 0.37V.

Note 25A: SCAP1, SCAP2, SCAP3 and SCAP4 pins are measured.

Note 26: S1, S2 and S3 pins are at an appropriate level to gate on the channel under test. Pull 10 μA from each SCAP pin (SCAP1, SCAP2, SCAP3 and SCAP4).

VoQTH = The servo output voltage from pins SCAP1, SCAP2, SCAP3, SCAP4 with the channel input level set to simulate the read head mispositioned by one quarter of a track in a direction towards the servo burst (i.e. larger amplitude). This is done by setting Vci = |V(CHAN1)−V(CHAN2)| = 187.5 mV = QTH and measuring the voltage on pins SCAP1, SCAP2, SCAP3, SCAP4.

VoQTL = The servo output voltage from pins SCAP1, SCAP2, SCAP3, SCAP4 with the channel input level set to simulate the read head mispositioned by one quarter of a track in a direction away from the servo burst (i.e. smaller amplitude). This is done by setting V_{CI} = |V(CHAN1)−V(CHAN2) | = 62.5 mV = QTL and measuring the voltage on pins SCAP1, SCAP2, SCAP3, SCAP4.

Note 26A: Av(QT(gd)) = (VoQTH−VoQTL)/(QTH−QTL).

Note 26B: V(intercept) is expressed as a percentage of V_{CC}.

Note 27: S1, S2, and S3 pins are at an appropriate level to gate on the channel under test. Pull 10 μA from each SCAP pin (SCAP1, SCAP2, SCAP3 and SCAP4).

VoETH = The servo output voltage from pins SCAP1, SCAP2, SCAP3, SCAP4 with the channel input level set to simulate the read head mispositioned by one quarter of a track in a direction towards the servo burst (i.e. larger amplitude). This is done by setting Vci = | V(CHAN1)−V(CHAN2) | = 156.25 mV = ETH and measuring the voltage on pins SCAP, SCAP2, SCAP3, SCAP4.

VoETL = The servo output voltage from pins SCAP1, SCAP2, SCAP3, SCAP4 with the channel input level set to simulate the read head mispositioned by one quarter of a track in a direction away from the servo burst (i.e. smaller amplitude). This is done by setting Vci = | V(CHAN!)−V(CHAN2) | = 93.75 mV = ETL and measuring the voltage on pins SCAP1, SCAP2, SCAP3, SCAP4.

Note 27A: GL(gd) = 100|[(|VoETH−VoETL|/|VoQTH−VoQTL|)-0.5]/0.5|.

Note 28: Set the voltage at S1, S2 and S3 pins to gate on the channel under test. Pull 19 μA from each SCAP pin (SCAP1, SCAP2, SCAP3, SCAP4). Force |V(CHAN1)−V(CHAN2) | = 125 mV. Measure the voltage at each gated detector output (SCAP1, SCAP2, SCAP3, SCAP4) Vosgd = ±| Max. difference voltage between (SCAP1−SCAP2) and (SCAP3−SCAP4) |.

Note 29: V(CHAN1)−V(CHAN2) = 0.5V. Force 3V on each of the gated detector output pins (SCAP1, SCAP2, SCAP3, SCAP4) and measure the current into or out of the pin.

Note 30: Minimum specification is worst case at low supply voltage, and high temperature.

Note 31: Maximum specification is worst case at high supply voltage, and high temperature.

Note 32: Minimum specification is worst case at low supply voltage, and cold temperature.

Pulse Detector AC Electrical Characteristics (Note 1)

Symbol	From Input (2)	To Output (2)	Parameter	Conditions	Min	Typ	Max	Units
$t_{recov(s)}$	WG ↓	ERD ↑	Recovery Time from Write Mode with Short Mode Programmed	Enable ERD for Pulse Detector Output Via Control Register	1.3	1.9	2.6	μs
$t_{recov(l)}$	WG ↓	ERD ↑	Recovery Time from Write Mode with Long Mode Programmed	Enable ERD for Pulse Detector Output Via Control Register	2.6	3	4.5	μs
$t_{recov(PDPD)}$	$\overline{PDPD}$ ↑	ERD ↑	Recovery Time from Full Power Down of Pulse Detector	Enable ERD for Pulse Detector Output Via Control Register (Note 12)		10	25	μs
t_{charge}	S1 to S3	SCAP1–SCAP4	Gated Detector Charge Time	(Note 3)		2	4	μs
$t_{discharge}$	S1 to S3	SCAP1–SCAP4	Gated Detector Discharge Time	(Note 4)		2.6	4.2	μs
t_{on}	S1 to S3	SCAP1–SCAP4	Gated Detector Turn On Time	(Note 5)	10	20	50	ns
t_{off}	S1 to S3	SCAP1–SCAP4	Gated Detector Turn Off Time	(Note 6)	15	28	40	ns
t_{pw}	ERD ↑	ERD ↓	Encoded Read Data Output Pulse Width	Enable ERD for Pulse Detector Output Via Control Register	10		34	ns
t_{GTO}	SCAP4 ↑	SCAP3 ↑	Gate to Time Channel Delay, Delay Step 0	V(SETHYS) = 0.1V, (Note 7) F = 5 MHz	65	77	89	ns
t_{DS}	SCAP4 ↑	SCAP3 ↑	Programmable Channel Delay, Delay Step Size	(Note 8)	7	11	15	ns
t_{STQC}	SCAP4 ↑	SCAP3 ↑	Self Timing Qualification Channel Delay	V(SETHYS) = −0.1V, (Note 9)	8	17	25	ns
t_{pp}	ERD		Pulse Pairing	f = 2.5 MHz and f = 5 MHz V(AMPIN) = 60 MV pp Differential (Note 10)		0.25	1	ns
V_{stqc}	SCAP4 ↑	SCAP3 ↑	Max DC Amplifier Output Level for Self Timing Qual Channel Operation	V_{CC} = 5V (Note 11)	3.7	4.5		V

Note 1: All parameters are specified for the following conditions unless otherwise stated. The device uses the components described in the AC test setup diagram. Parameters are guaranteed over the recommended operating temperature and supply range from operating conditions table. V(REF) = 0.5V. V(SETHYS) = 0.3V. V(RG) = 0.3V. f = 2.5 MHz. Control register is set at the initial power up conditions.

Note 2: The symbol (up arrow) indicates the rising edge of the pulse is used as reference. The symbol (down arrow) indicates the falling edge of the pulse is used as reference.

Note 3: Close SW1, SW2, SW3 and SW4. With all external capacitors to SCAP pins (SCAP1 thru SCAP4) discharged, measure the time from servo channel enable pins (S1, S2 and S3) to 90% of the rising edge of the selected servo channel output.

Note 4: Close SW1, SW2, SW3 and SW4. With all external capacitors to SCAP pins (SCAP1 thru SCAP4) charged, measure the time from servo channel enable pins (S1, S2 and S3) to 90% of the falling edge of the selected servo channel output.

Note 5: Open SW1, SW2, SW3 and SW4. Pull 1 mA from each of the SCAP pins (SCAP1 thru SCAP4). Measure the time from the selection of each servo channel (S1, S2, S3) to the voltage on the selected servo output (SCAP1 thru SCAP4) when it increases by 0.1V.

Note 6: Open SW1, SW2, SW3 and SW4. Pull 1 μA from each of the SCAP pins (SCAP1 thru SCAP4). Measure the time from the sellection of each servo channel (S1, S2, S3) to the voltage on the deselected servo output (SCAP1 thru SCAP4) when it decreases by 0.1V.

Note 7: Disable the self timing qualification channel, enable internal pulse detector signals and program the gate channel delay step 0 through the control register. tGTO includes time contributions from the test frequency and delay introduced by the external differentiator components. The test frequency contribution is the amount of time from the zero crossing at the base line to the peak (which for a 5 MHz signal is 100 ns). The theoretical delay introduced by the differentiator components, shown in the AC test setup diagram, at this frequency is__ns. Consequently, the raw gate to channel delay can be found by subtracting off these external contributions to the delay.

Note 8: Disable the self timing qualification channel and enable internal pulse detector signals through the control register. Measure the time from the rising edge of SCAP4 pin to the rising edge of SCAP3 pin as the programmable gate channel delay step is changed. tDS = the incremental delay change per step.

Note 9: Select the 10 Mbit/s filter, enable internal pulse detector signals, and program gate channel delay step 0 through the control register.

Note 10: Enable pulse detector output at ERD via the control register. The 7.5 MHz pulse pairing measurement is made with the 20 Mbit/s channel filter in full power mode.

Note 11: Increase the DC amplifier output level until tSTQC changes by 2 ns. Vstgc is this DC level.

Note 12: Pulse detector is initially powered down for 1 ms prior to powering on.

Synchronizer and Synthesizer AC Electrical Characteristics

Symbol	Func. Block	Parameter	Conditions	Min	Typ	Max	Units
$t_{T\text{-}SYNC}$	Synch.	Synchronizer Half Window Loss	13.3 Mb/s, Strobe M = 0		0.8	4	ns
			33 Mb/s, Strobe M = 0			2.7	
$\theta_{LIN\text{-}PH}$	Synch.	Phase Detector Retrace Angle	Phase Lock (Notes 4, 6)		$\pm\pi$		rad
$K_{VCO\text{-}SYNC}$	Synch.	Synchronizer VCO Gain (Note 1)	25°C Ambient	$0.4\ \omega_0$	$0.57\ \omega_0$	$0.74\ \omega_0$	rad/Vs
t_{SD0}	Synch.	SCK Neg. Edge to SD Neg. Edge		0		12	ns
t_{SD1}	Synch.	SCK Neg. Edge to SD Pos. Edge		0		12	ns
t_{ZPSR}	Synch.	Zero-Phase Start Accuracy	Entering READ Mode (Note 4)		3		ns
$f_{AUTORANGE}$	Synch.	VCO Self-Limit w.r.t. f_{SYNTH}	(Note 4)		± 50		%
t_{SFIX}	Synch.	Strobe per Step Size, −2 to +2			0.6		ns
t_{SVAR}	Synch.	Strobe per Step Size, −2 to −5, 2 to 5	(Note 2)		0.0625xTvco		ns
$t_{PW\text{-}SCK}$	Synch.	SCK Output Pulse Width	(Note 5)	Tw − 5	Tw	Tw + 5	ns
$t_{ERD\text{-}SDO}$	Synch.	Delay, ERD Pos. Edge to SDO Pos. Edge	(Note 3)		TBD		ns
$t_{-3\ dB-KVCO}$	Synch.	VCO Control Block −3 dB Rolloff	(Note 4)		16		MHz
$t_{-3\ dB\text{-}CP}$	Synch.	Charge Pump Block − 3 dB Rolloff	(Note 4)		16		MHz
t_{PWSTH}	Synth.	Synthesizer Output Pulse Width	(Note 5)	$T_W - 2$	T_W	$T_W + 2$	ns
$K_{VCO\text{-}SYNTH}$	Synth.	Synthesizer VCO Gain	(Notes 1 and 5) 25°C Ambient	$1.4\ \omega_0$	$2.0\ \omega_0$	$2.6\ \omega_0$	rad/Vs
$f_{-3\ dB\text{-}KSTH}$	Synth.	VCO Control Block −3 dB Rolloff	(Note 4)		15		MHz

Note 1: ω_0 is the operating frequency of the synchronizer VCO. This parameter is specified at 25°C ambient only. K_{VCO} varies inversely with absolute (Kelvin) temperature; K_{VCO} (T) $\approx$ K_{VCO} (25°C) $\times$ 298/T, where T is in degrees Kelvin.

Note 2: T(VCO) is the period of the VCO selected as delay line reference, either the synthesizer or synchronizer VCO. The period is equal to the code rate clock period.

Note 3: Add to this value the data rate dependent delay line term TBD%xT(VCO): Note 2 also applies.

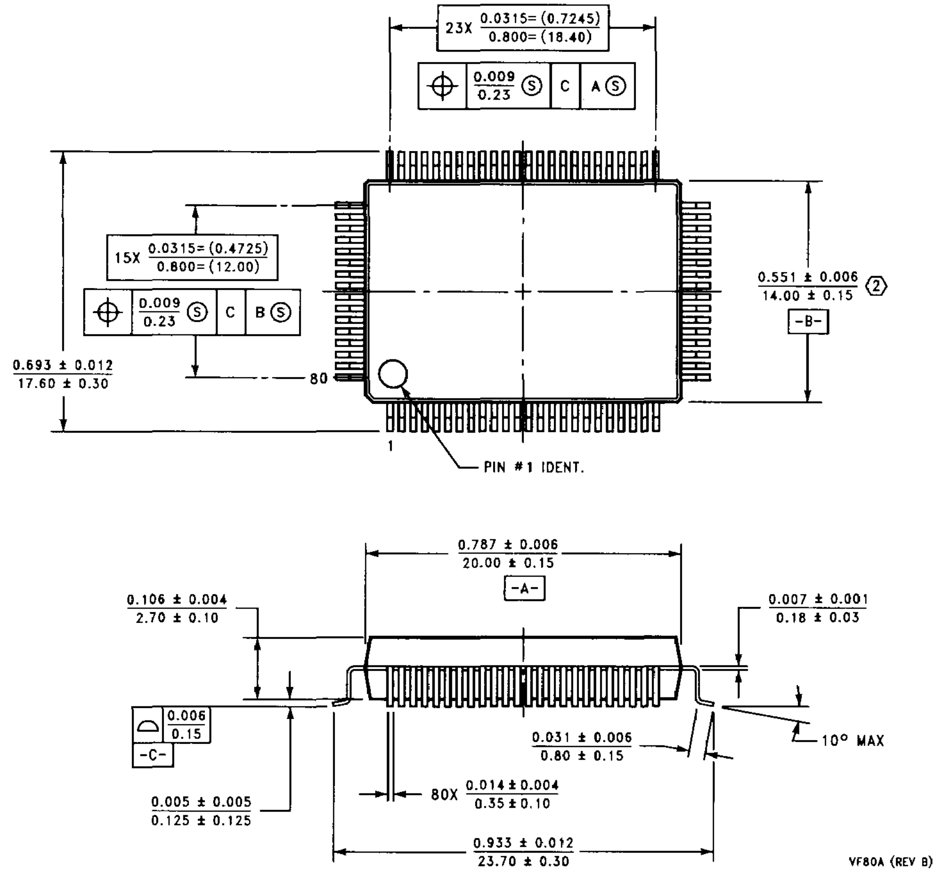
Note 4: Parameter guaranteed by design or correlation to characterization data. No outgoing tests are performed.

Note 5: Tw = 0.5X respective clock period.

Note 6: The parameter is measured w.r.t. code rate clock period.

Physical Dimensions inches (millimeters)

Lit. # 103080



Plastic Quad Flat Package (VF)
Order Number DP8492VF
NS Package Number VF80A

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