OTI-031

IBM PS/2® MODEL 30-COMPATIBLE SYSTEM CONTROLLER

FEATURES

- Supports 8086 or V30 CPU speed at 8 MHz or 10 MHz with zero wait state using 150 ns DRAMs
- Generates programmable fast and normal timing for PC memory
- Provides either DRAM or SRAM control
- Supports up to 8M bytes of expanded memory
- Supports 256K or 1M bit DRAMs on EMS memory
- Arbitrates the system bus among the CPU, DMA, math coprocessor, and DRAM memory refresh cycle
- Provides four channels of 8 MHz DMA as well as burst mode
- RAM pin available to select static or dynamic memory interface
- Power down mode

DESCRIPTION

The OTI-031 provides the PS/2 Model 30-compatible system with the dual speed control, 8 MHz or 10 MHz, necessary to operate the system at peak performance. The device also controls memory, I/O, parity, address paths, data paths as well as handling four channels of direct memory access. The OTI-031 is available from Oak Technology, Inc. in an industry-standard plastic 100-pin flatpack.

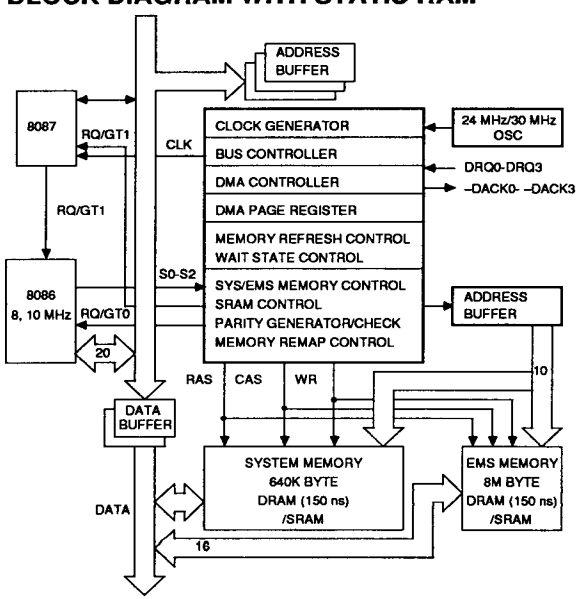
The CMOS OTI-031 is the System Controller device in the four-chip VLSI PS/2 Model 30-compatible chip set. The other three devices are the OTI-032 I/O Controller, the OTI-033 Floppy Disk Controller and Data Separator, and the OTI-034 Address/Data Buffer Drivers.

The chip set integrates logic and functions on PS/2 Model 30-compatible systems to the point of reducing the printed circuit board device count by half, when memories are excluded. Further, while offering complete compatibility with the PS/2 Model 30-compatible system, the OTI chip set improves system performance by allowing 10 MHz operation with no "wait states" (using 150 ns DRAMS), supports an additional 8M-bytes of memory using EMS (Expanded Memory Specification) 4.0, and controls system speed as necessary for optimum performance.

The chip can be brought to a power-down mode to conserve power dissipation and can be entered into only when the RAM pin is tied low. The chip can then be programmed into power-down mode through several registers and can be woke up from power-down mode by an external interrupt.

The OTI-037 VGA, Video Graphics Controller, and OTI-036 Color Palette can also be used in the PS/2 Model 30-compatible system and provides high resolution graphics of 800 x 600 elements with 16 colors. Graphic capabilities of this resol-ution are usually found only on more expensive systems.

BLOCK DIAGRAM WITH STATIC RAM



ORDER INFORMATION

Part Number	Package
OTI-031	Plastic Flatpack

Notes: Operating temperature range is 0°C to +70°C.
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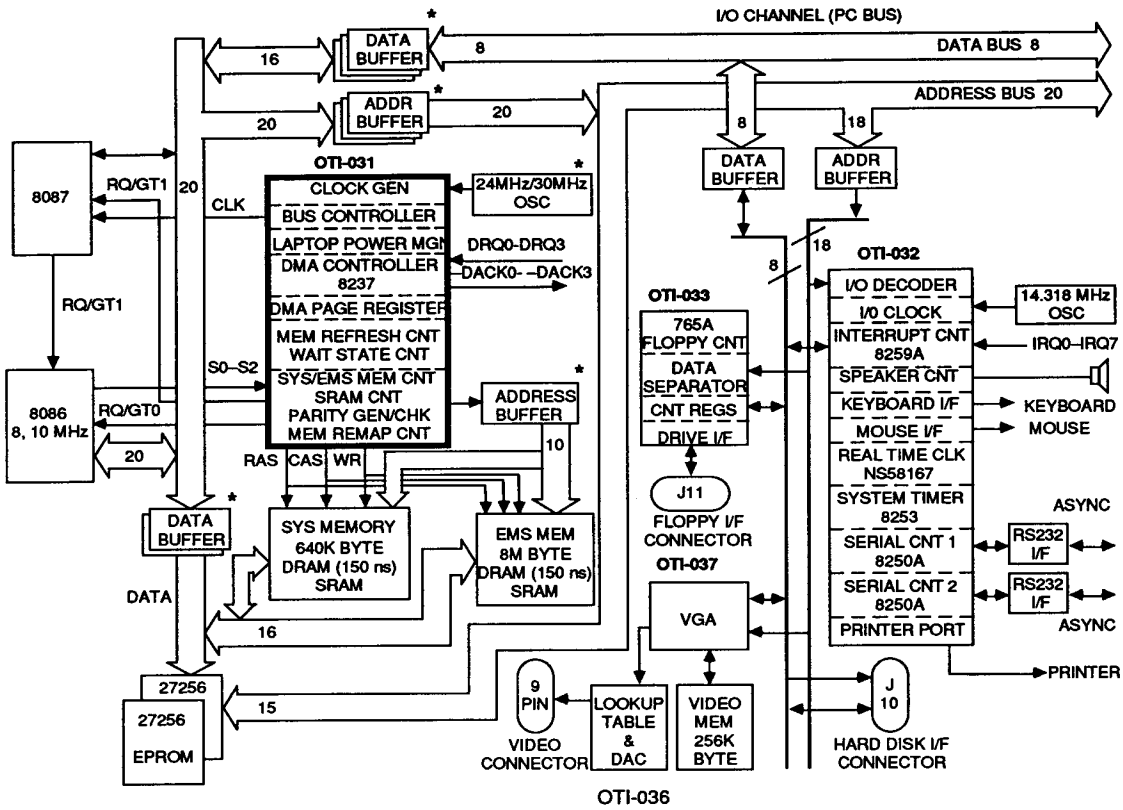
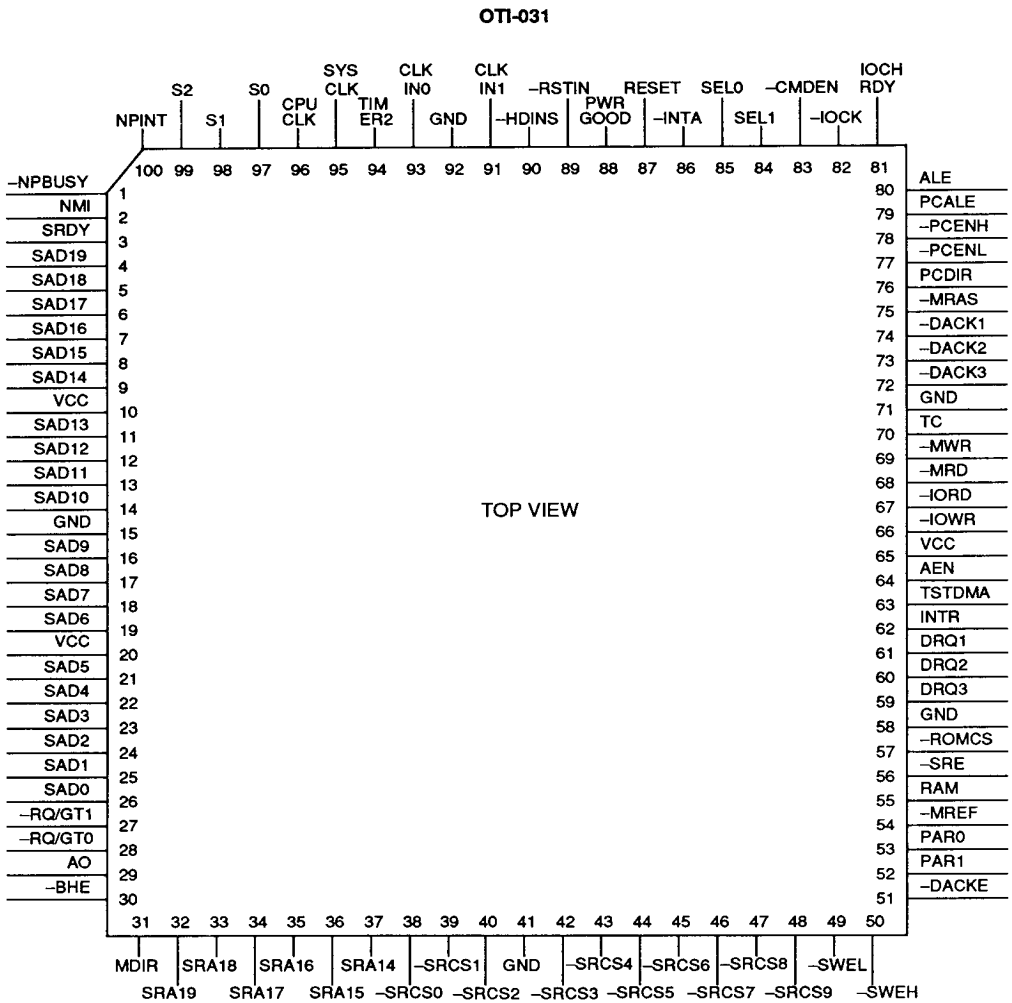
PS/2 MODEL 30-COMPATIBLE SYSTEM DIAGRAM

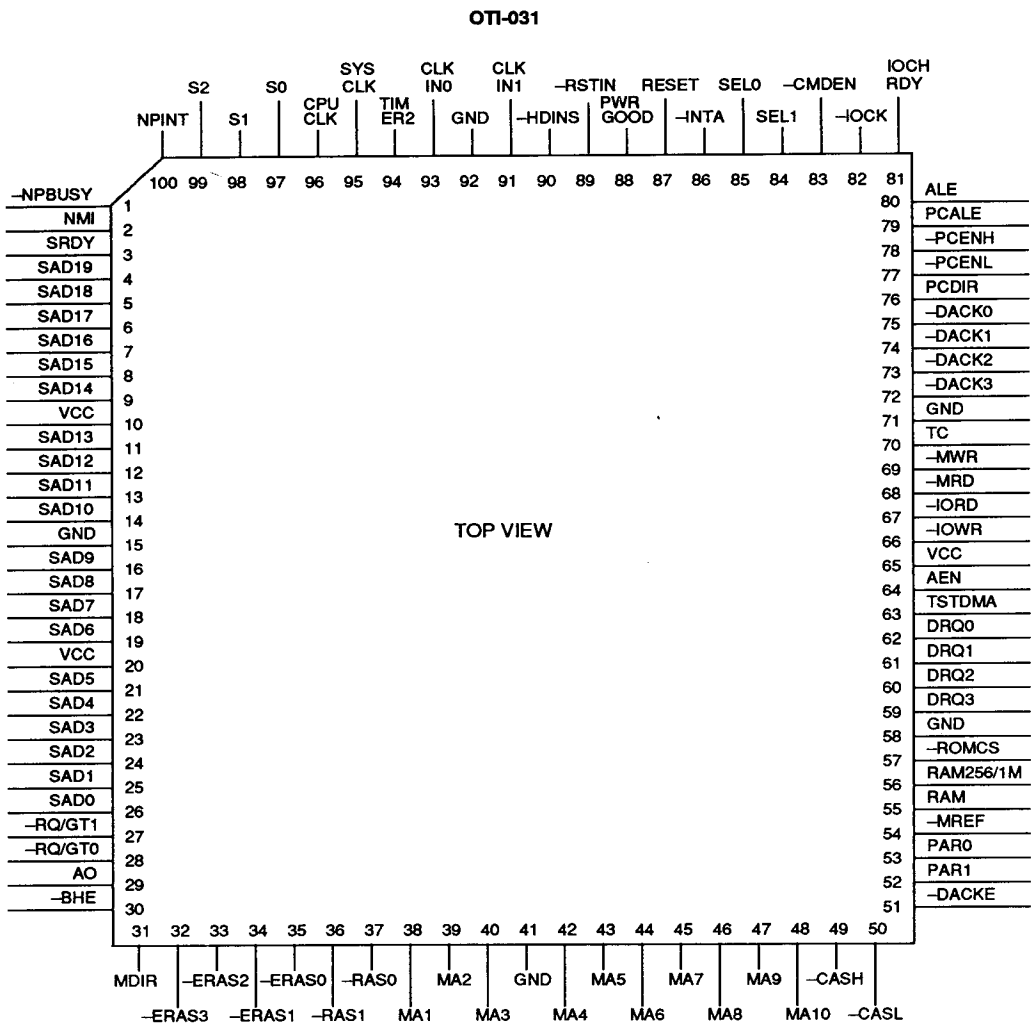


* OTI-034 contains these functional blocks.

PIN DIAGRAM [When pin 55 (RAM) is tied low.]



PIN DIAGRAM [When pin 55 (RAM) is tied high.]



SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to low.]

Signal Name	Pin Number	Signal Type	Signal Description
–NPBUSY	1	I	Busy - Is an active low signal connected directly to the –BUSY signal of 8087 which is normally connected to the –TEST signal of the 8086 CPU. It is examined by the bus arbitrator logic internally to the OTI-031.
NMI	2	O	Non Maskable Interrupt - Is an active high signal to the CPU that there is an error caused by one of the following: - memory parity error, - I/O channel check signaled from the PC bus, - 8087 interrupts (an unmasked exception has occurred).
SRDY	3	O	System Ready - This is an active high signal that acknowledges the CPU or 8087 at t3 or tW before t4 time that the data transfer for either memory or I/O is complete.
SAD19-SAD16	4-7	I/O	Address Bus - These lines are the four most significant address lines for memory operation. They are input lines during the time the CPU or 8087 is in control. The chip starts driving these lines during the DMA address time.
SAD15-SAD0	8,9,11-14, 16-19, 21-26	I/O	Address and Data Bus - These lines are time multiplexed addresses and data bus corresponding to the AD15-ADO of 8086 and 8087 bus. OTI-031 monitors these lines during the time the CPU or 8087 is in control of the bus. It will begin to drive these lines during the DMA address time.
–RQ/GT1	27	I/O	Request Grant Channel 1 - Is an active low pulse signal connected directly to –RQ/GT1 of 8087. This signal is used by the chip to request the bus from 8087. If 8087 hasn't controlled tha bus at that time, the request will relay through –RQ/GT0 of 8087 that is connected to –RQ/GT1 of the CPU.
–RQ/GT0	28	I/O	Request Grant Channel 0 - Is an active low pulse signal connected directly to –RQ/GT0 of the CPU. This signal is used by the chip to request the bus from the CPU if there is no 8087, otherwise it is inactive.
A0	29	O	Address Line 0 - Is the latched version of address 0. It is used along with –BHE signal to distinguish the 8/16 bit and odd/even byte operation.
–BHE	30	I/O	Byte High Enable - This is an active low signal used to enable data on to the most significant half of the data bus (D15-D8). It is an input line during the time the CPU or 8087 is in control. The chip starts driving this signal during the DMA time.
MDIR	31	O	Memory Direction - Is the status signal to memory write enable of memory devices and also the data direction transceiver between the CPU and system memory bus.
SRA16-SRA19	35-32	O	SRAM Address Bits 16-19 - If RAM is low, they are SRAM address decoders for Expanded Memory option. The combination of SRA16-SRA19 is capable of selecting 32K X 8 SRAM organized as a word wide for the total of 960K bytes. Expanded memory is not selected if SRA16-SRA19 are 1111.
SRA14, SRA15	37, 36	O	SRAM Address Bits 14, 15 - If RAM is low, they are the two most significant addresses of the 32K X 8 SRAM.

–BHE	A0	Operation
0	0	Word (D15-D0)
0	1	Odd Byte (D15-D8)
1	0	Even Byte (D7-D0)
1	1	Not Used

SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to low.] (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SRCS0- –SRCS9	38-40, 42-48	O	Static RAM Chip Select Bits 0-9 - If RAM is low, they are Static RAM Memory Chip Selects (active low signals). Each signal selects two banks of 32K X 8 type SRAM for a total of 640K bytes of memory.
–SWEH, –SWEL	50, 49	O	SRAM Write Enable (High & Low) - If RAM is low, they are active low write enable signals for SRAM: - –SWEH for odd byte. - –SWEL for even byte.
–DACKE	51	O	DACK Enable - Is an active low control signal to enable either –DACK2 or –DACK3 to on-board floppy and hard disk controllers respectively. This is a condition signal based on the content of Chip Select Control Port 0065 (hex).
PAR0, PAR1	53, 52	I/O	Parity Bits 0-1 - Are the memory (odd type) parity bits for even and odd bytes of memory bank. Each parity bit is generated and written during the memory write operation. Each parity bit is checked and reported on an error to the system at the end of the memory cycle. PAR0 is the memory parity bit for even byte. PAR1 is the memory parity bit for odd byte.
–MREF	54	O	Memory Refresh - Is an active low signal indication of the refresh cycle. It is inhibited when RAM is low.
RAM	55	I	RAM Select - Is an input signal to tell the chip of the memory type used in the system: - RAM = low = Static RAM - RAM = high = Dynamic RAM
–SRE	56	O	SRAM Read Enable - If RAM is low, it is an active low read enable signal for SRAM memory.
–ROMCS	57	O	ROM Chip Select - Is an active low signal used to enable the ROM BIOS to output data on to the data bus.
DRQ1-DRQ3	61-59	I	DMA Request Bits 1-3 - Are the asynchronous active high signal channel request inputs used by peripheral devices to obtain DMA service. –DACK will acknowledge the recognition of DRQ signals. These signals are compatible to the DRQ signals of 8237.
INTR	62	I	Interrupt Signal - Is a positive edge signal to release the system from an idle state for power saving management.
TSTDMA	63	I	Test DMA Function - This signal is used for testing purposes of the internal circuit.

Signal	Memory Space
–SRCS0	00000 - 0FFFF
–SRCS1	10000 - 1FFFF
–SRCS2	20000 - 2FFFF
–SRCS3	30000 - 3FFFF
–SRCS4	40000 - 4FFFF
–SRCS5	50000 - 5FFFF
–SRCS6	60000 - 6FFFF
–SRCS7	70000 - 7FFFF
–SRCS8	80000 - 8FFFF
–SRCS9	90000 - 9FFFF

SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to low.] (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
AEN	64	O	Address Enable - Is the active high signal during the DMA cycle to de-gate the I/O devices from the I/O channel to allow DMA transfers to take place.
–IOWR	66	O	I/O Write Command - Is the active low command to instruct the I/O device to read the data present on the data bus.
–IORD	67	O	I/O Read Command - Is the active low command to instruct the I/O device to drive its data on to the data bus.
–MRD	68	O	Memory Read Command - Is the active low signal to instruct the memory to drive its data on to the data bus.
–MWR	69	O	Memory Write Command - Is the active low command to instruct the memory to store the data present on the data bus.
TC	70	O	Terminal Count - Is an active high pulse signal when the terminal for any DMA channel is reached. It can be driven from I/O channel to terminate the current operation of DMA cycle.
–DACK1- –DACK3	74-72	O	DMA Acknowledge Bits 1-3 - Are the active low signals to notify the individual peripherals when one has been granted a DMA cycle. These signals are compatible to the DACK signals of 8237.
–MRAS	75	O	Memory Signal Timing - Is an active low control signal to indicate the system memory cycle.
PCDIR	76	O	PC Data Bus Direction - Is the status signal to the data transceiver between the CPU and PC data bus: - high means the CPU drives the PC data bus (write cycle), - low means the PC drives the CPU data bus (read cycle).
–PCENL	77	O	PC Data Byte Low Bus Enable - Is the active low control signal to enable the data buffer (D7-D0) between CPU and PC data bus.
–PCENH	78	O	PC Data Byte High Bus Enable - Is the active low control signal to enable the data buffer (D15-D8) between CPU and PC data bus.
PCALE	79	O	PC Address Latch Enable - Is an active high pulse active during t1 of any bus cycle. It is similar to the ALE signal except that this signal is active high throughout the DMA cycle.
ALE	80	O	Address Latch Enable - Is an active high pulse active during t1 of any bus cycle including DMA, and memory refresh cycle. The address should be latched using the ALE falling edge.
IOCHRDY	81	I	I/O Channel Ready - Is an active high ready signal from an I/O channel. Pulling low in active by a memory or I/O device to lengthen memory or I/O cycles. For every system clock cycle this signal is inactive, one wait state is added.
–IOCK	82	I	I/O Channel Check - Is the active low pulse signal for at least two system clock durations to indicate an uncorrectable error on the I/O channel. This signal causes the NMI, if NMI is enabled.
–CMDEN	83	O	Command Enable - Is the active low control signal to enable or disable the command buffer going to the I/O channel bus (PC Bus). It is used to prevent the bus contention between the I/O devices that shares the same address space resided in the X bus and in the I/O channel bus.
SEL0,SEL1	85, 84	O	Select Function (0-1) - These are the special select status signal decoders for address range, and an on-board video memory space are active at the current cycle:

SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to low.] (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description

SEL1	SEL0	Function
0	0	Nothing Selected
0	1	A15-A10 = 0 (I/O)
1	0	On-board Video ROM
1	1	On-board Video RAM

See more details in MEMORY 7 I/O DECODER 7 BUFFER CONTROL Section.

–INTA	86	O	Interrupt Acknowledge - This pin is an active low signal used to enable interrupt controller's interrupt-vector data on to the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
RESET	87	O	Reset - Is an active high signal synchronized to the system clock to reset the CPU and system. Its timing characteristics are determined by –RSTIN signal.
PWRGOOD	88	I	Power Good - Is an active high signal (TTL level of 2.4 to 5.25 Vdc during normal operation, or an inactive level of 0.0 to 0.4 Vdc) coming from a power supply to indicate that power is stable. The signal is inactive if an undervoltage condition occurs. The PWRGOOD signal has a turn on delay that is between 100 ms and 500 ms. This line can sink 2 mA or source 100 µA.
–RSTIN	89	I	Reset Input - Is an active low signal which is used to generate RESET signal. The OTI-031 provides a Schmitt trigger input so that an RC connection can be used to establish the power on reset of proper duration.
–HDINS	90	I	Hard Disk Installed - Is the status signal that the hard disk is installed on the system. This is present to I/O port 62 bit 2.
CLKIN1	91	I	Clock Input 1 - Is the 30 MHz TTL clock input with 40/60% duty cycle. It is used for system clock at CPU running at 10 MHz. It should be pulled up high if there is no clock source to this pin.
CLKIN0	93	I	Clock Input 0 - Is the 24 MHz TTL clock input with 40/60% duty cycle. It is used for the system clock at CPU running at 8 MHz, internal DMA control, and memory refresh time.
TIMER2	94	I	Timer2 Status - Is the status signal on the 8253 Timer Channel 2 which comes from OTI-032. This is present to I/O port 62 bit 5.
SYSCLK	95	O	System Clock - Is the MOS driven clock signal to the CPU and system. It has a 33% duty cycle (67-low, 33-high).
CPUCLK	96	O	CPU Clock - Is a MOS driven clock signal to 8086 or NEC V30 CPU. The clock duty cycle can be selected through a special register. The default duty cycle of CPU clock is 33%.
S2-S0	99-97	I	System Status - These signals are used to decode different CPU or 8087 operations.

S2-S0	Operation
000	Interrupt Acknowledge
001	I/O Read
010	I/O Write
011	Halt
100	Memory Read (fetch)
101	Memory Read (data)
110	Memory Write
111	Passive

SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to low.] (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
NPINT	100	I	8087 Numerical Processor Interrupt - An active high signal that indicates that an unmasked exception has occurred during numeric instruction execution when 8087 interrupt is enabled.
VCC	65, 20, 10		Power: +5 V
GND	92, 71, 41, 58, 15		Ground

SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to high.]

Signal Name	Pin Number	Signal Type	Signal Description
–NPBUSY	1	I	Busy - Is an active low signal connected directly to the –BUSY signal of 8087 which is normally connected to the –TEST signal of the 8086 CPU. It is examined by the bus arbitrator logic internally to the OTI-031.
NMI	2	O	Non Maskable Interrupt - Is an active high signal to the CPU that there is an error caused by one of the following: - memory parity error, - I/O channel check signaled from the PC bus, - 8087 interrupts (an unmasked exception has occurred).
SRDY	3	O	System Ready - This is an active high signal that acknowledges the CPU or 8087 at t3 or tW before t4 time that the data transfer for either memory or I/O is complete.
SAD19-SAD16	4-7	I/O	Address Bus - These lines are the four most significant address lines for memory operation. They are input lines during the time CPU or 8087 is in control. The chip starts driving these lines during the DMA address time.
SAD15–SAD0	8, 9, 11-14 16-19 21-26	I/O	Address and Data Bus - These lines are time multiplexed address and data bus corresponding to the AD15-ADO of 8086 and 8087 bus. OTI-031 monitors these lines while the CPU or 8087 is in control of the bus. It will begin to drive these lines during the DMA address time.
–RQ/GT1	27	I/O	Request Grant Channel 1 - Is an active low pulse signal connected directly to –RQ/GT1 of 8087. This signal is used by the chip to request the bus from 8087. If 8087 hasn't controlled the bus at that time, the request will relay through –RQ/GT0 of 8087 that is connected to– RQ/GT1 of CPU.
–RQ/GT0	28	I/O	Request Grant Channel 0 - Is connected directly to –RQ/GT0 of the CPU. This signal is used by the chip to request the bus from the CPU if there is no 8087. Otherwise, it is inactive.
A0	29	O	Address Line 0 - Is the latched version of address 0. It is used along with –BHE signal to extinguish the 8/16 bit and odd/even byte operation.
–BHE	30	I/O	Byte High Enable - This is an active low signal used to enable data on to the most significant half of the data bus (D15-D8). It is an input line during the time CPU or 8087 is in control. The chip starts driving this signal during the DMA time.

–BHE	A0	Operation
0	0	Word (D15-D0)
0	1	Odd Byte (D15-D8)
1	0	Even Byte (D7-D0)
1	1	Not Used

SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to high.] (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MDIR	31	O	Memory Direction - Is the status signal to memory write enable of memory devices and also the data direction transceiver between the CPU and system memory bus.
–ERAS0- –ERAS3	35-32	O	EMS Row Address Strobe Bits 0-3 - If RAM is high, they are active low –RAS signals for Expanded Memory option to the system:
–RAS0- –RAS1	37, 36	O	Row Address Strobe Bits 0-1 - If RAM is high, they are the active low control signals to the 640K byte DRAM system memory to inform the memory that row address is present on the address bus. –RAS0 is for the first 128K bank and –RAS1 is for the next 512K bank of memory.
MA1-MA10	38-40, 42-48	O	Memory Address Bit 1-10 - If RAM is high, it is the time multiplex memory address for 1M memory type (for 256K memory type MA10 is not used.) During the memory cycle, MA1-MA10 is the row address output until one unit time delay is elapsed, the MA1-MA10 will start outputting the column address.
–CASH- –CASL	49 ,50	O	Column Address Strobe (High & Low) - If RAM is high, they are active low control signals to the on-board DRAM system & EMS memory to inform them that column address is present on the address bus: - –CASH for odd byte [D(15-18)], - –CASL for even byte [D(7-0)].
–DACKE	51	O	DACK Enable - Is an active low control signal to enable either –DACK2 or –DACK3 to on-board floppy and hard disk controllers respectively. This is a condition signal based on the content of Chip Select Control Port 0065 (hex).
PAR0-PAR1	53, 52	I/O	Parity Bits 0-1 - Are the memory (odd type) parity bits for even and odd bytes of memory bank. Each parity bit is generated and written during the memory write operation. Each parity bit is checked and reported on an error to the system at the end of the memory read cycle. PAR0 is memory parity bit for even byte. PAR1 is the memory parity bit for odd byte.
–MREF	54	O	Memory Refresh - Is the active low signal indication of the refresh cycle. It is inhibited when RAM is low.
RAM	55	I	RAM Select - Is an input signal to tell the chip of the memory type used in the system: - RAM = low = Static RAM, - RAM = high = Dynamic RAM.
RAM256/1M	56	I	256K or 1M - If RAM is high, it is the signal to inform the chip of the memory type used in expanded memory: - low means 1M type, - high means 256K type.

	Pin	Odd	Even
–ERAS0	35	256K (1M)	256K (1M)
–ERAS1	34	256K (1M)	256K (1M)
–ERAS2	33	256K (1M)	256K (1M)
–ERAS3	32	256K (1M)	256K (1M)

SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to high.] (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–ROMCS	57	O	Rom Chip Select - Is an active low signal used to enable the ROM BIOS to output data on to the data bus.
DRQ0-DRQ3	62-59	I	DMA Request Bits 0-3 - Are the asynchronous active high channel request inputs used by peripheral devices to obtain DMA service. –DACK will acknowledge the recognition of DRQ signals. These signals are compatible to the DRQ signals of 8237.
TSTDMA	63	I	Test DMA Function - This signal is used for testing purposes of the internal circuit of the DMA controller only.
AEN	64	O	Address Enable - Is an active high signal during the DMA cycle to disable the I/O devices from the I/O channel to allow DMA transfers to take place.
–IOWR	66	O	I/O Write Command - Is the active low command to instruct the I/O device to read the data present on the data bus.
–IORD	67	O	I/O Read Command - Is the active low command to instruct the I/O device to drive its data on to the data bus.
–MRD	68	O	Memory Read Command - Is the active low command to instruct the memory to drive its data on to the data bus.
–MWR	69	O	Memory Write Command - Is the active low command to instruct the memory to store the data present on the data bus.
TC	70	O	Terminal Count - Is an active high pulse signal when the terminal for any DMA channel is reached. It can be driven from I/O channel to terminate the current operation of DMA cycle.
–DACK0- –DACK3	75-72	O	DMA Acknowledge Bits 0-3 - Are active low signals to notify the individual peripherals when one has been granted a DMA cycle. These signals are compatible to the DACK signals of 8237.
PCDIR	76	O	PC Data Bus Direction - Is the status signal to the data transceiver between the CPU and PC data bus: - high means the CPU drives the PC data bus (write cycle), - low means the PC drives the CPU data bus (read cycle).
–PCENL	77	O	PC Data Byte Low Bus Enable - Is the active low control signal to enable the data buffer (D7-D0) between CPU and PC data bus.
–PCENH	78	O	PC Data Byte High Bus Enable - Is the active low control signal to enable the data buffer (D15-D8) between CPU and PC data bus.
PCALE	79	O	PC Address Latch Enable - Is a high pulse active during t1 of any bus cycle. It is similar to ALE signal except that this signal is active high throughout the DMA cycle.
ALE	80	O	Address Latch Enable - Is an active high pulse active during t1 of any bus cycle including DMA, and Memory refresh cycle. The address should be latched using the ALE falling edge.
IOCHRDY	81	I	I/O Channel Ready - Is an active high ready signal from an I/O channel. Pulling low inactive by a memory or I/O device to lengthen memory or I/O cycles. For every system clock cycle this signal is inactive, one wait state is added.
–IOCK	82	I	I/O Channel Check - Is the active low pulse signal for at least two system clock duration to indicate an uncorrectable error on the I/O channel. This signal causes the NMI, if NMI is enabled.

SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to high.] (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–CMDEN	83	O	Command Enable - Is the active low control signal to enable or disable the command buffer going to the I/O channel bus (PC bus). It is used to prevent the bus contention between the I/O devices that shares the same address space resided in the X bus and in the I/O channel bus.
SEL0, SEL1	85, 84	O	Select Function Bits 0-1 - These are the special select status signal decoders for address range, and an on-board video memory space are active at current cycle: SEL1 / SEL0 / Function 0 / 0 / Nothing Selected 0 / 1 / A15-A10 = 0 (I/O) 1 / 0 / On-board Video ROM 1 / 1 / On-board Video RAM See more details in MEMORY 7 I/O DECODER 7 BUFFER CONTROL Section.
–INTA	86	O	Interrupt Acknowledge - This pin is an active low signal used to enable interrupt controller's interrupt-vector data on to the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
RESET	87	O	Reset - Is an active high signal synchronized to the system clock to reset the CPU and system. Its timing characteristics are determined by –RSTIN signal.
PWRGOOD	88	I	Power Good - Is an active high signal (TTL level of 2.4 to 5.25 Vdc during normal operation, or an inactive level of 0.0 to 0.4 Vdc) coming from a power supply to indicate that power is stable. The signal is inactive if an undervoltage condition occurs. The PWRGOOD signal has a turn on delay that is between 100 ms and 500 ms. This line can sink 2 mA or source 100 μA.
–RSTIN	89	I	Reset Input - Is an active low signal which is used to generate the RESET signal. The OTI-031 provides a Schmitt trigger input so that an RC connection can be used to establish the power on reset of proper duration.
–HDINS	90	I	Hard Disk Installed - Is the status signal that the hard disk is installed on the system. This is present to I/O port 62 bit 2.
CLKIN1	91	I	Clock Input 1 - Is the 30 MHz TTL clock input with 40/60% duty cycle. It is used for system clock at CPU running at 10 MHz. It should be pulled up high if there is no clock source to this pin.
CLKIN0	93	I	Clock Input 0 - Is the 24 MHz TTL clock input with 40/60% duty cycle. It is used for the system clock at CPU running at 8 MHz, internal DMA control, and memory refresh time.
TIMER2	94	I	Timer2 Status - Is the status signal on the 8253 Timer Channel 2 which comes from OTI-032. This is present to I/O port 62 bit 5.
SYSCLK	95	O	System Clock - Is the MOS driven clock signal to the CPU and system. It has a 33% duty cycle (67-low, 33-high).
CPUCLK	96	O	CPU Clock - Is a MOS driven clock signal to 8086 or NEC V30 CPU. The clock duty cycle can be selected through a special register. The default duty cycle of the CPU clock is 33%.
S2-S0	99-97	I	System Status -These signals are used to decode different CPU or 8087 operations.

SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to high.] (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
			S2-S0 / Operation: 000 Interrupt Acknowledge; 001 I/O Read; 010 I/O Write; 011 Halt; 100 Memory Read (fetch); 101 Memory Read (data); 110 Memory Write; 111 Passive
NPINT	100	I	8087 Numerical Procesor Interrupt - An active high signal that indicates that an unmasked exception has occurred during numeric instruction execution when 8087 interrupt is enabled.
VCC	65, 20, 10		Power: +5 V
GND	92, 71, 58 41, 15		Ground

DESCRIPTION

SYSTEM MEMORY AND I/O MAP

The 8086/V30 supports 16 bit operations with 20 bit addressing to directly access up to 1M byte of memory space. The system memory and an On-board Expanded Memory (if it's enabled) are byte and/or word accessible. Memory is mapped in Table 1.

MEMORY CONTROL UNIT

OTI-031 offers either Dynamic or Static RAM memory control unit depending on the RAM input signal with zero wait state for 150 ns access of memory.

If "RAM" pin is strapped high (to VCC), OTI-031 will resume on-board DRAM memory control. It supports 640K bytes of system memory using 64K X 4 DRAM for the first 128K bytes and 256K X 1 DRAM for the next 512K bytes of memory. In addition to 640K bytes, OTI-031 also supports full specification of EMS 4.0 which makes the multi-tasking possible. The EMS logic will support memory either 256K or 1M byte of memory type depending on where RAM 256/1M input signal is strapped. The EMS logic will control on-board memory up to 2M bytes if 256K type of memory is used or up to 8M bytes if 1M type is desired (see RAM 256/1M input definition in OTI-031Pin Description).

If "RAM" pin is strapped low (to Ground), OTI-031 will resume on-board SRAM memory control. It supports 640K bytes of system memory using 32K X 8 type of SRAM. It also supports an EMS SRAM up to 960K (1M minus 64K) bytes of 32K X 8 type memory. It provides 4-bit address selects [SRA(16-19)] that can select one out of 16 bank of memory (64K bytes each). However, if EMS SRAM is not accessed, SRA(16-19) will be all 1's. Hence, only 15 possible ways are used.

The function of Memory Control Units have the following five functions:

1. System Memory Control
2. EMS Control
3. Memory Request Control
4. Memory Parity Check and Generator
5. Memory Address Generator

SYSTEM MEMORY CONTROL

FOR DRAM CONTROL: The system memory control generates system RAS signals to the 640K of read/write memory:

- –RAS0 is for the first 128K of memory,
- –RAS1 is for the next 512K of memory.

FOR SRAM CONTROL: The system memory control generates 10 SRAM chip selects [–SRCS(0-9)] and read/write control signals (–SRE, –SWEH, –SWEL):

TABLE 1. FUNCTIONS

Hex Address	Description
00000 - 1FFFF	128K byte: 1st bank #1 (640K System Memory)
20000 - 2FFFF	64K byte: 2nd bank #2 (640K System Memory)
30000 - 3FFFF	64K byte: 2nd bank #3 (640K System Memory)
40000 - 4FFFF	64K byte: 2nd bank #4 (640K System Memory)
50000 - 5FFFF	64K byte: 2nd bank #5 (640K System Memory)
60000 - 6FFFF	64K byte: 2nd bank #6 (640K System Memory)
70000 - 7FFFF	64K byte: 2nd bank #7 (640K System Memory)
80000 - 8FFFF	64K byte: 2nd bank #8 (640K System Memory)
90000 - 9FFFF	64K byte: 2nd bank #9 (640K System Memory)
A0000 - BFFFF	64K byte: Video Buffer
C0000 - EFFFF	192K byte: Reserved for BIOS on I/O Channel.
F0000 - FFFFF	64K byte: System ROM

TABLE 2. MEMORY

Signal	Memory Space
–SRCS0	00000 - 0FFFF
–SRCS1	10000 - 1FFFF
–SRCS2	20000 - 2FFFF
–SRCS3	30000 - 3FFFF
–SRCS4	40000 - 4FFFF
–SRCS5	50000 - 5FFFF
–SRCS6	60000 - 6FFFF
–SRCS7	70000 - 7FFFF
–SRCS8	80000 - 8FFFF
–SRCS9	90000 - 9FFFF

The system memory control has ability to allocate the system memory through the Planar RAM Control Register Port 006B. If the first bank (128K bytes of memory) is not installed or bad, the system can map the second bank (next 512K bytes of memory) over. Also, each block of 64K bytes of second bank (except the first 128K bytes) can be enabled or disabled so that the system can reallocate the memory between the system memory and expanded one.

If MAP/UNMAP– bit 0 of the Planar RAM register is 0,– RAS0 or –SRCS(0-1) will be active at the memory space of 00000 - 1FFFF (128K bytes), and –RAS1 or –SRCS(2-9) will be active at the memory space of 20000 - 9FFFF (512K byte) for 640K bytes of system memory total.

If MAP/UNMAP– bit 0 is 1, the physical memory bank 0 is disabled [–RAS0 or –SRCS(0-1)], and the physical memory of second bank [–RAS1 or –SRCS(8-9)], i.e. second bank #8 and #9 (80000 - 9FFFF) will be allocated to the memory space of 00000 -FFFF. Thus, –RAS1 or –SRCS(2-9) will be active at the memory space of 00000 - 7FFFF for 512K bytes of system memory total.

The format of the Planar RAM Control/ Status Register is:

Planar RAM Control Register: I/O Port 006B (hex) R/W:

Bit	Function
7	Parity Check Pointer 1 = Lower 128K failed 0 = Upper 512K failed
6	DIS/EN– RAM, 90000 - 9FFFF
5	DIS/EN– RAM, 80000 - 8FFFF
4	DIS/EN– RAM, 70000 - 7FFFF
3	DIS/EN– RAM, 60000 - 6FFFF
2	DIS/EN– RAM, 50000 - 5FFFF
1	DIS/EN– RAM, 40000 - 4FFFF
0	MAP/UNMAP– Low Memory

At power on or reset, this port is 00.

If the EMS memory happens to be selected at the system memory space, –RAS0 and –RAS1 or –SRCS(0-9) will be blocked. Both –RAS0 and –RAS1 will be asserted during the refresh. Refresh function is inhibited if "RAM" is low.

Bit 7 of Planar RAM Control Register will be set (1) or clear (0) according to the recent parity bit error:

- If the present memory read cycle is the first 128K memory and caused a parity error, bit 7 will be set.
- If the present memory read cycle is the next 512K memory and caused a parity error, bit 7 will be clear.
- If there is no parity error, bit 7 will remain unchanged.
- Writing a 1 to bit 7 of this port will reset this bit. Writing a 0 to this bit has no effect.

EMS CONTROL

The EMS Control consists of EMS Current Map, EMS Alternate Map, and the EMS RAS generator.

MEMORY REFRESH CONTROL CYCLE

Memory Refresh Timer generates the request every 15.6 µs to the Refresh Controller. Once the Refresh Controller grants the cycle (–MREF is asserted), it outputs the ALE, PCALE, –MRD signals. The minimum refresh cycle is five system clocks for system running at 8 MHz or six system clocks for system running at 10 MHz.

Memory Refresh Address Generator drives all 20 address lines through the CPU bus during memory refresh cycle time (–MREF is low). Address 0-8 is outputed from a 9-bit binary counter (which will increment the count at the end of the cycle), address 9-19 is driving low during the memory refresh cycle.

DMA CONTROL

DMA Control consists of two blocks:

- 8237 DMA Control
- DMA Page Register

8237 DMA CONTROL

8237 DMA Control is a four channel DMA operating at 8 MHz used to support byte (8-bits) transfer operation between memory and peripherals capable of doing the DMA request and transferring data such as Floppy Controller. Its function is equivalent to the 8237 DMA chip. The DMA channels are assigned as shown in Table 3.

Each channel can transfer data throughout the 1M byte system address space in 64K bytes per block at a time. The following figure shows address generation for the DMA channels.

Source	DMA Page Registers	Controller
Address	A19 ◄——► A16	A15 ◄► A0

Note: The addressing signal, 'byte high enable' (–BHE), is generated by inverting address line A0.

Three DMA channels (1, 2, 3) are available on the I/O channel. The 8237 DMA controller command code addresses are shown in Table 2.

DMA PAGE REGISTER

DMA Page Register can be accessed through the 8-bit I/O ports. These ports can be read or write, however, only data bits 0-4 are significant. Table 5 shows the address for the page register.

Addresses for all DMA channels do not increase or decrease through page boundaries (64K bytes).

TABLE 3. CHANNELS

Channel	Assignment
Channel0: DRQ0	Reserved
Channel1: DRQ1	Not Used
Channel2: DRQ2	Diskette
Channel3: DRQ3	Fixed Disk

TABLE 4. PAGE REGISTER

Page Register	I/O Address (In hex)
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082

TABLE 5. REGISTER FUNCTIONS

I/O Address (In hex)	Register Function
0000	Channel 0 Base and Current Address Register
0001	Channel 0 Base and Current Word Count
0002	Channel 1 Base and Current Address Register
0003	Channel 1 Base and Current Word Count
0004	Channel 2 Base and Current Address Register
0005	Channel 2 Base and Current Word Count
0006	Channel 3 Base and Current Address Register
0007	Channel 3 Base and Current Word Count
0008	Read Status Register/Write Command Register
0009	Write Request Register
000A	Write Single Mask Register Bit
000B	Write Mode Register
000C	Clear Byte Pointer Flip-Flop
000D	Read Temporary Register/Write Master Clear
000E	Clear Mask Register
000F	Write All Mask Register Bits

SYSTEM I/O MAP

I/O Address	Function	OTI-031 Respond	OTI-032 Respond	PC Bus Respond
0000 - 000F	DMA Controller	R/W	None	None
0010 - 001F	System Control and Status Group 1	R/W	W	None
0020 - 0021	Interrupt Control	None	R/W	None
0030 - 003F	Reserved	None	None	None
0040 -0043	System Timer	None	None	None
0044 - 005F	Reserved	None	None	None
0060	System Data Port	None	R/W	None
0061	System Control	W	R/W	None
0062	System Status	R	None	None
0063	Reserved	W	R/W	None
0064	Reserved	None	None	None
0065	Chip Select Control	W	R/W	None
0066 - 006A	Reserved	None	R/W	None
006B	Planar RAM Control	R/W	None	None
006C - 006F	Reserved	None	None	None
0070 - 0080	Reserved	None	None	None
0081 - 0087	DMA Page Register	R/W	None	None
0088 - 009F	Reserved	None	None	None
00A0 - 00AF	Reserved	W	R/W	None
00B0 - 00BF	Real Time Clock	None	R/W	None
00C0 - 00CF	Reserved	None	None	None
00D0 - 00DF	System Control and Status Group 2	None	R/W	None
00E0 - 00EF	Real Time Clock	None	R/W	None
00F0 - 00FF	Reserved	None	none	None
02F8-02FF	Serial Comm. Control 2	None	R/W	R/W
0320 - 032F	Fixed Disk Control	None	R/W*	R/W
0378 - 037A	Parallel Port	None	R/W*	R/W
03B0 - 03DF	Video System	On-Board Decoder	None	R/W
03F0 - 03F7	Floppy Disk Control	None	R/W*	R/W
03F8 - 03FF	Serial Comm. Control 1	None	R/W*	R/W

***Note:** The peripheral is built in OTI-032 and OTI-033. It can be enabled or disabled through Chip Select Control Register Port.

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
tCYC	SYSCLK, CPUCLK Cycle Time	100		ns	
tDCY0	CLKIN0 Cycle Time	42		ns	24 MHz
tDCY1	CLKIN1 Cycle Time	33		ns	30 MHz
tSCLKH	SYSCLK High Time	33		ns	33% Duty Cycle
tSCLKL	SYSCLK Low Time	60		ns	33% Duty Cycle
tCCLKH	CPUCLK High Time	33		ns	33% Duty Cycle
		47		ns	50% Duty Cycle
tCCLKL	CPUCLK Low Time	60		ns	33% Duty Cycle
		47		ns	50% Duty Cycle
tCMD	SYSCLK to Command		25	ns	
tALEH	SYSCLK Low to ALE, PCALE High		42	ns	
tALEL	SYSCLK High to ALE, PCALE Low		30	ns	
tSRDY	SYSCLK to SRDY		35	ns	
tADR	SYSCLK Low to Address on I/O Channel		75	ns	
tDARV	Data Valid before t4 during Read	25		ns	
tDARF	Data Invalid after End of t3 during Read		5	ns	
tDAWS	Data Setup Time from End of t1 during Write		75	ns	
tDAWH	Data Hold Time to t4 SYSCLK High during Write	35		ns	
tMAR	Memory Row Address Valid from SYSCLK Low		100	ns	
tMAC	Memory Column Address Valid from SYSCLK Low		43	ns	
tRAS	SYSCLK to –RAS		20	ns	
tCAS	SYSCLK to –CAS		20	ns	
tMDR	Memory Data Valid from –RAS		155	ns	
tMDC	Memory Data Valid from –CAS		75	ns	
tMDV	Memory Data Valid before t4	20		ns	
tMDF	Memory Data Invalid after –CAS		20	ns	
tMDS	Memory Data Valid after SYSCLK Low during Write		75	ns	
tMDH	Memory Data Hold Time after –Cas	20		ns	
tRQ	Request/Grant from SYSCLK Low		25	ns	
tREF	Refresh after SYSCLK Low		40	ns	
tRFP	PCALE after SYSCLK High during Refresh		30	ns	
tRADR	Memory Refresh Address after PCALE		25	ns	
tDRQS	DRQ Setup Time before –RQ/GT Request		2 TCYC	ns	
tDRQH	DRQ Hold Time after –DACK	0		ns	
tDPAH	PCALE High from –RQ/GT Grant		30	ns	

AC CHARACTERISTICS: (Cont.)

Symbol	Parameter	Min	Max	Unit	Condition
tDPAH	PCALE High from –RQ/GT Grant		30	ns	
tDPAL	PCALE Low from End of DMA Command		2 1/2 TDCY +35	ns	
tAENH	AEN High from –RQ/GT Grant		1/2 TDCY +35	ns	TDCY=DMA Cycle Time Min 125 ns
tAENL	AEN Low from End of DMA Command		2 1/2 TDCY +35	ns	
tDACL	–DACK Low from AEN		3 TDCY +70	ns	
tDACH	–DACK High from End of DMA Command		1/2 TDCY +40	ns	
tDADR	DMA Address Valid from AEN		3 TDCY +30	ns	
tDMAR	–MRD, –IORD Active from AEN		3 1/2 TDCY +35	ns	
tDMAW	–MWR, –IOWR Active from –MRD, –IORD		2 TDCY	ns	
tDWID	–MWR, –IOWR Command Width	4 TDCY		ns	
tDRID	–MRD, –IORD Command Width	6 TDCY		ns	
tDMRQ	End of DMA Command to –RQ/GT Release		2 TDCY	ns	

MAXIMUM OUTPUT CAPACITANCE LOADING

Pinout	Capacitance Loading (pF)
CPUCLK	20
SYSCLK	20
RESET	200
–INTA	15
SEL0	30
SEL1	30
–CMDEN	15
ALE	20
PCALE	15
–PCENH	15
–PCENL	15
PCDIR	20
–DACK3- –DACK0	200
TC	15
–MWR	25

Pinout	Capacitance Loading (pF)
–MRD	25
–IORD	25
–IOWR	25
AEN	200
–ROMCS	20
–MREF	200
PAR0	100
PAR1	100
–DACKE	15
–CASL	45
–CASH	45
MA1-MA10	20
–RAS0	20
–RAS1	20
–ERAS0	20

Pinout	Capacitance Loading (pF)
–ERAS1	20
–ERAS2	20
–ERAS3	20
MDIR	15
–BHE	15
A0	15
–RQ/GT0	20
–RQ/GT1	20
SAD19-SAD0	40
SRDY	35
NMI	20

TIMING CHARACTERISTICS

FIGURE 1. READ CYCLE TIMING DIAGRAM FOR I/O CHANNEL

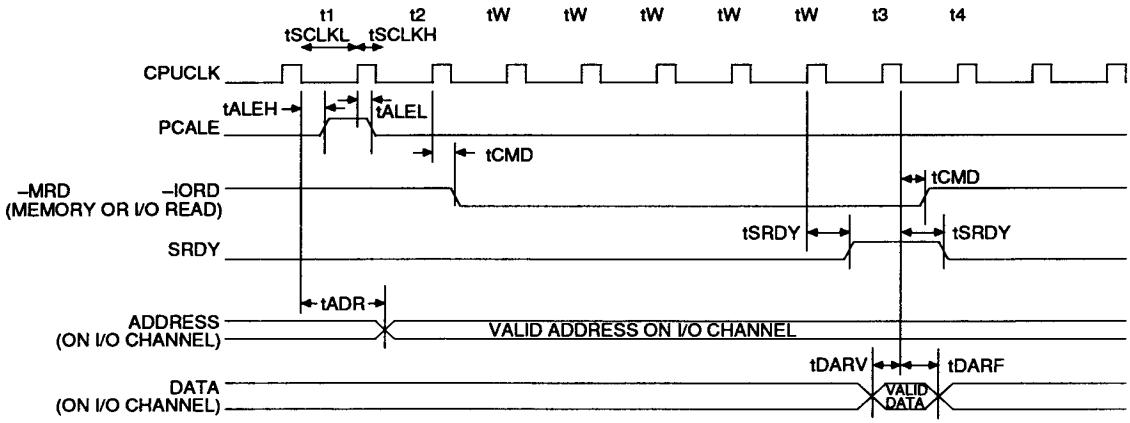


FIGURE 2. WRITE CYCLE TIMING DIAGRAM FOR I/O CHANNEL

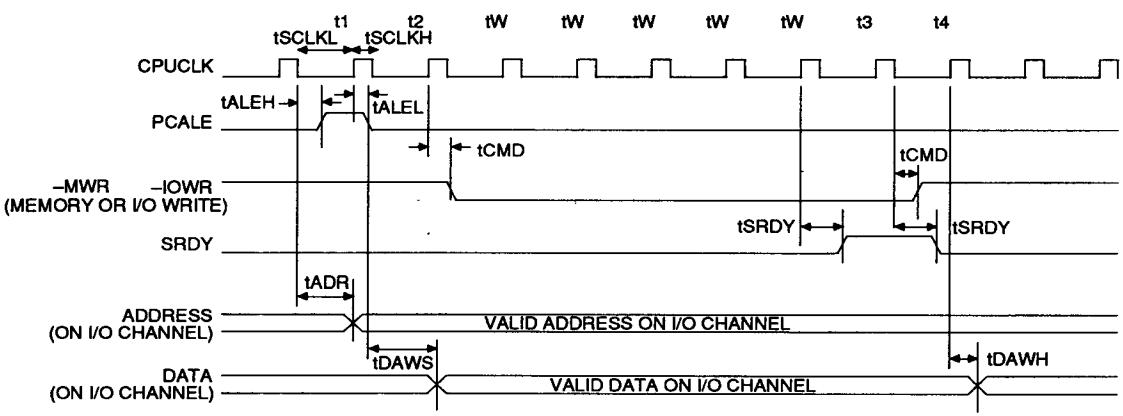


FIGURE 3. READ CYCLE TIMING DIAGRAM FOR ON-BOARD MEMORY (0 WAIT, 150 NS DRAM)

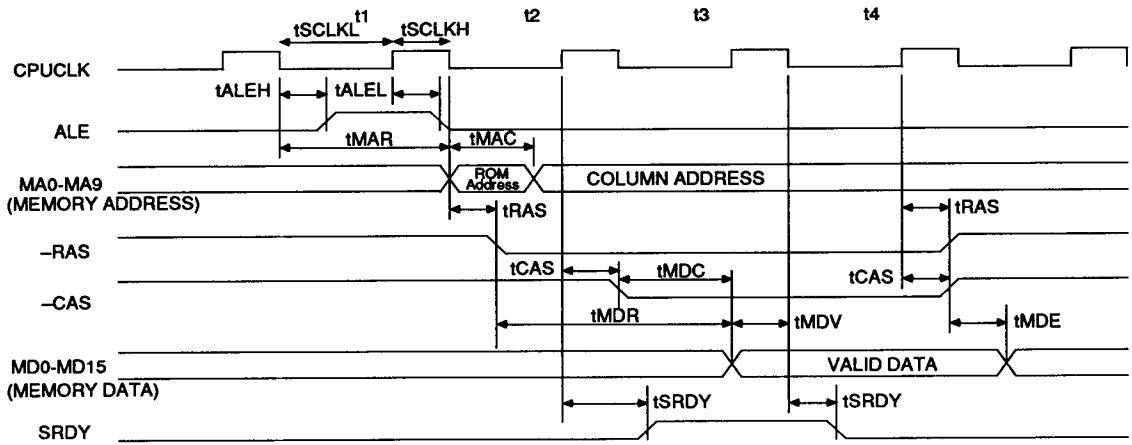


FIGURE 4. WRITE CYCLE TIMING DIAGRAM FOR ON-BOARD MEMORY (0 WAIT, 150 NS DRAM)

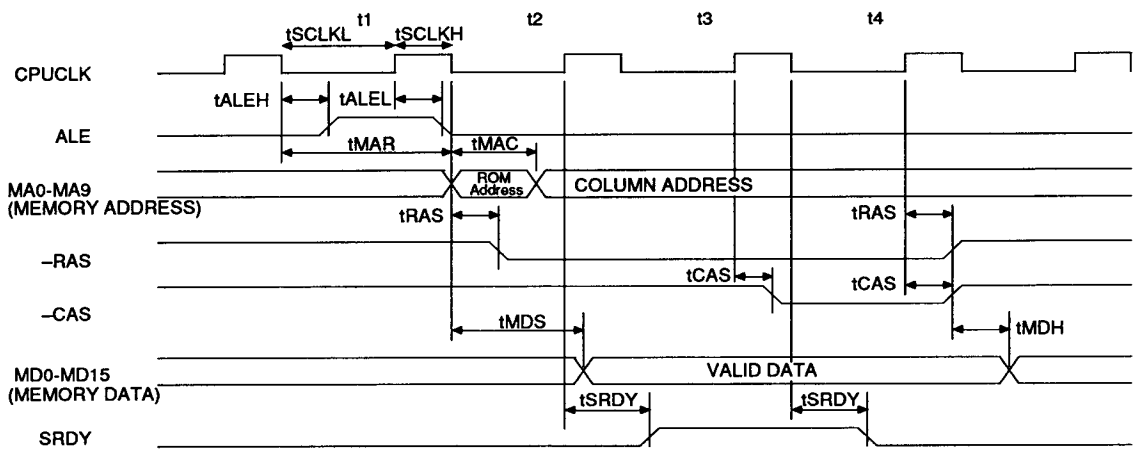


FIGURE 5. MEMORY REFRESH CYCLE TIMING DIAGRAM

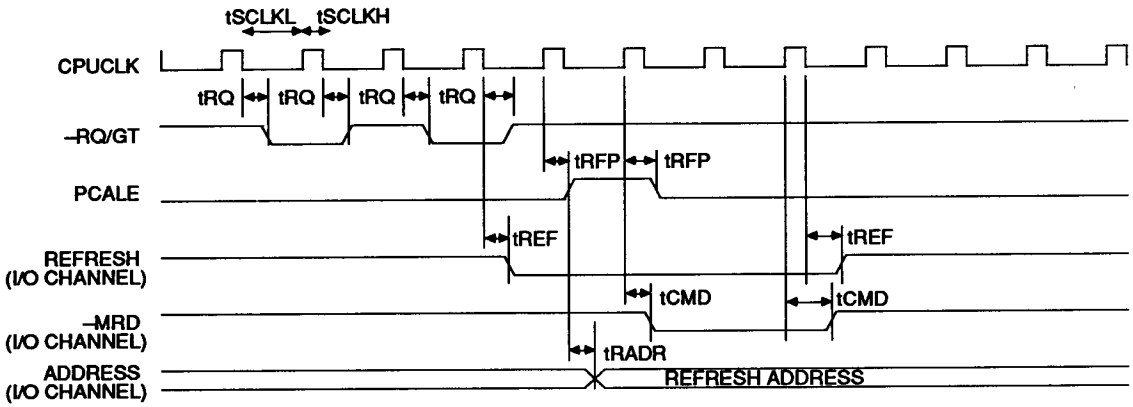
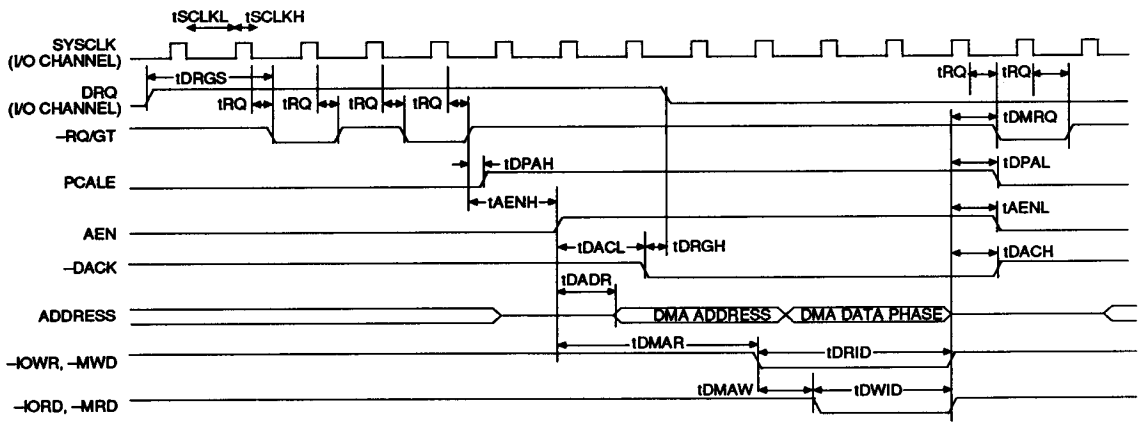


FIGURE 6. DMA TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0V
Applied Input Voltage	–0.5 V to +7.0 V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = 400 µA
VOL	Output Low Voltage		0.45	V	IOL = 20 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 16 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 10 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 8 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 2 mA, Note 1
VIH	Input High Voltage	2.0	VCC + 0.5	V	TTL
VIL	Input Low Voltage	–0.5	0.8	V	TTL
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILI	Input Leakage Current	–10	10	µA	
OLI	Output Leakage Current	–10	10	µA	
ICC	Operating Supply Current (OTI-031) Operating Supply Current (OTI-032)		250 40	mA mA	VIN = VCC or GND VCC = 5.25V Outputs Grounded

DC CHARACTERISTICS (Cont.)

Note 1: Output Current Driving Capabilities (IOL).

IOL	VL82C031 Pins	VL82C032 Pins
20 mA	RESET –DACK1- –DACK3 AEN –MREF	–LED PD0-PD7
16 mA		J1DATA J2DATA J1CLK J2CLK
10 mA		–INIT –STROBE -SELIN -AUTOFD
8 mA	PAR0 PAR1	XD7-XD0 KEYLOCK -SELHDK
4 mA	CPUCLK SYSCLK MDIR –ERAS3 –ERAS2 –ERAS1 –ERAS0 –RAS1 –RAS0 –CASH –CASL MA1-MA10 SAD0-SAD19 A0 ALE –DACK0 –MWR –MRD –IOWR –IORD RAM256/1M –ROMCS	INTR SPKOUT -FLPCS -XBFRD -TXD1 -TXD2 -DTR1 -DTR2 -RTS1 -RTS2
2 mA	–INTA SEL0 SEL1 –CMDEN NMI SRDY –RQ/GT0 –RQ/GT1 –BHE PCALE –PCENH –PCENL PCDIR TC –DACKE	–XBUFRD DRVTYPE -PRE –RD3F0 –RD3F1 TIMEROUT2

NOTE 2: REAL TIME CLOCK DC CHARACTERISTICS

ICC1 for VDDRTC = 4 µA maximum
Operating Voltage = 3.0-6.0 V
Standby Voltage = 2.0 V minimum (for battery backup)