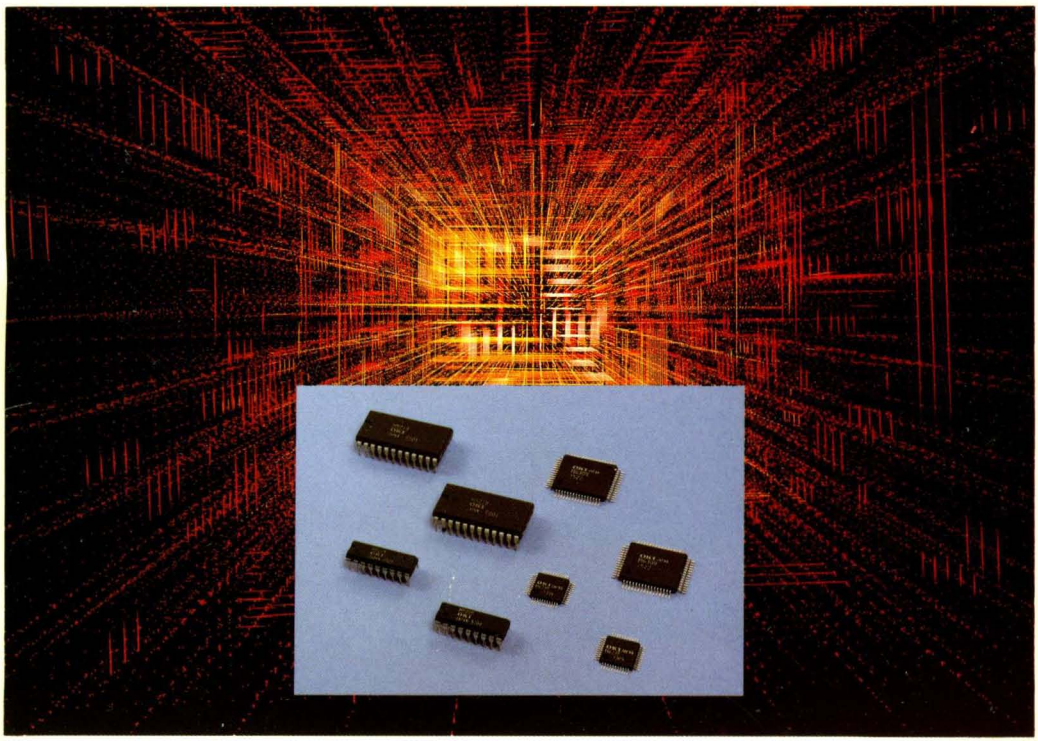
OKI

OKI VOICE SYNTHESIS LSI DATA BOOK



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INTRODUCTION

■ The Voice Synthesis LSI

In regular tape recorders where sound is stored as analog signals on magnetic tape, the subsequent amplification of those signals to drive a speaker is referred to as sound "reproduction". It cannot be called sound "synthesis". If the amount of information stored (which is 100% in the above tape recorder) is reduced, the amount of storage medium (memory) can also be reduced for greater economy. Where the amount of information is reduced (compressed) on the basis of a certain principle, the restoration of the original sound is called "synthesis".

■ Voice Synthesis Methods

Voice synthesis methods can be divided into three major types:- waveform encoding, parametric synthesis, and synthesis by rule. Each type is briefly outlined below.

(1) Waveform coding methods
This type includes differential PCM (DPCM), adaptive delta modulation (ADM), and adaptive differential PCM (ADPCM). The original sound wave amplitude is sampled at fixed intervals, digitized, and the volume of data then reduced on the basis of the principles mentioned above.

(2) Parametric synthesis methods
Characteristic information included in voice waveforms is extracted as parameters for synthesizing purposes. The PARCOR method is a typical example.
In this method where models of the human vocalization mechanism are used, voiced and voiceless consonant sounds are discriminated, and voiced sound pitch and amplitude data is extracted together with filter characteristic of vocal tract. Voice synthesis is then achieved by passing this data to hardware consisting of digital filter circuits etc.

(3) Synthesis by rule method
This synthesis method is an ideal method where groups of phonemes expressed by small quantities of data are skillfully linked together to reproduce any desired words.
However, since further elucidation of linguistic laws taking intonation, accents, and length sounds into consideration is required to achieve a highly natural voice, this method must still be considered to be in the research stage.

■ Basic ADPCM Method

Oki voice synthesis LSIs are based on adaptive differential PCM (ADPCM) which is an improved form of the DPCM method. The PCM and ADPCM methods are described below.

(1) Pulse code modulation (PCM)
Voice waveforms and other analog data can be PCM encoded (into digital data) by sampling and quantization in S&H (sample and hold) and AD converter stages. The S/N ratio in this case is determined by the following expression

$$(N - 1) \times 6 \text{ dB}$$

where N is the number of output bits from the AD converter assuming that the maximum waveform amplitude is equivalent to full scale in the converter. For example, if the sampling frequency is 8 kHz and the number of AD converter output bits is 12, the required amount of data (number of bits) per second is

$$8 \text{ kHz} \times 12 \text{ bits} = 96\text{K bits/sec}$$

This is called the bit rate. The S/N ratio is this case is obtained as

$$(12 - 1) \times 6 = 66 \text{ dB}$$

(2) Adaptive Differential PCM
The ADPCM method was devised as a means of reducing the bit rate without sacrificing the S/N ratio too much. In this method, the amount of data is reduced by quantizing and encoding the differential (dn) between adjacent signal samples. A feature of this method is the ability to make adaptive changes to the quantization width $\triangle n$ when quantizing the differential dn. (In the DPCM method, the quantization width is fixed.) In other words, $\triangle n$ is enlarged when the differential dn is large, and reduced when dn is small.

(3) ADPCM analysis
If the input at the nth sampling point is Xn, and the waveform reproduction value at the (n-1)th sampling point is $\hat{X}n-1$, the differential dn between the two is

$$dn = Xn - \hat{X}n-1 \qquad \text{(Differential calculation)}$$

This is then encoded by the quantization width $\triangle n$ at the present point of time (the nth point of time).

$$Ln = dn/\triangle n \qquad \text{(Encoding: Ln = ADPCM data)}$$

And if this is then quantized and the waveform subsequently reproduced,

$$qn = (Ln + 1/2)\triangle n \qquad \text{(Quantization)}$$

$$\hat{X}n = \hat{X}n-1 + qn \qquad \text{(Reproduction)}$$

The quantization width for the next (n+1)th item of data is then changed from $\triangle n$ to $\triangle n+1$.

$\triangle n+1 = \triangle n \cdot M(Ln)$ (Quantization width change)
(where M(Ln) is the Ln function format)

The quantization width is thus determined according to the previously accumulated data.

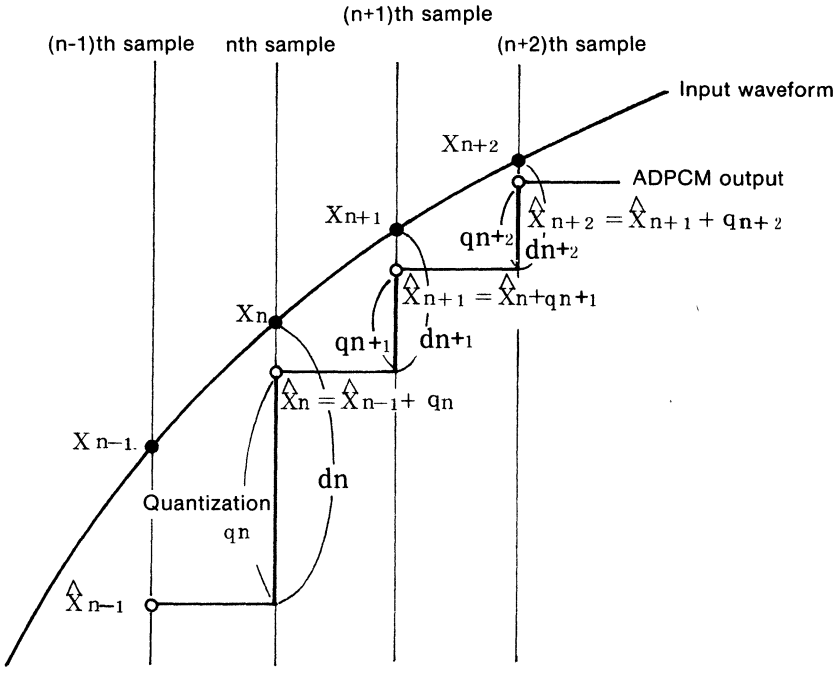


Fig. 1 ADPCM method computation process

(4) ADPCM data
The ADPCM data Ln is expressed as M bits of data including the polarity bit. For example, a 4-bit expression is given as

$$Ln = \{B_3, B_2, B_1, B_0\}$$

where B_3 (polarity bit) indicates the polarity of the (begin-ind)differential dn,
B_2 (MSB) indicates the presence of a $4\triangle n$ digit in the changed portion,
B_1 (2SB) indicates the presence of a $2\triangle n$ digit in the changed portion, and
B_0 (LSB) indicates the presence of a $\triangle n$ digit in the changed portion.

(5) ADPCM reproduction
ADPCM reproduction can be expressed as part of the ADPCM analysis. The reproduction for the nth ADPCM input data Ln is given as

$$qn = (Ln + 1/2)\triangle n \quad \text{(Quantization)}$$
$$= (-1 \times B_3)\,(4\triangle nB_2 + 2\triangle nB_1 + \triangle nB_0 + \tfrac{1}{2}\triangle n)$$
$$\hat{X}n = \hat{X}n\text{-}1 + qn \quad \text{(Reproduction)}$$

And $\triangle n+1$ is calculated for the (n+1)th item of ADPCM data.

$$\triangle n+1 = \triangle n \cdot M(Ln)$$

In other words, in addition to serving as data used for calculating new PCM values for previously set quantization widths, the ADPCM code also serves as the data for calculating the quantization width to be set next. Furthermore, if

Xn is set to 12 bits, and
Ln is set to 4 bits,

the quantity of ADPCM encoded data is compressed by 4/12.

Note: The 1/2 element in
quantization $qn = (Ln + 1/2)\triangle n$
serves as a means of linear equalization for changed polarity.

■ Oki ADPCM Types

Although the ADPCM method is the basic method adopted by Oki, a few modifications have been made, and two analysis/synthesis methods are now in use. These are outline briefly below.

(1) Straight ADPCM: This is the basic unmodified ADPCM method where the quality of sound is better than the two methods described below. This method is also suitable for sound effects.

(2) Compressed ADPCM: The compressed ADPCM method is the straight ADPCM method subject to unvoice elimination processing[Note 1] and waveform repetition processing[Note 2]. The bit rate, therefore, can be reduced to 1/3 of the straight ADPCM bit rate. Furthermore, the degree of data compression can be changed for each word.

Note 1. Unvoice elimination processing:
Extensive reduction of unvoice interval data by replacing unvoice intervals (which exceed a certain length) with unvoice data.

Note 2. Waveform repetition processing:
Data volume reduced by repeating a single item of waveform data in voiced waveforms such as vowels which are repeated periodically.

■ Features of Oki Voice Synthesis LSIs

The major features of Oki voice synthesis LSIs are summarized below.

(1) Quality and object of synthesis
   (i) Good quality sound with high degree of naturalness
   (ii) Synthesis of sound effects, musical instruments, and animal sounds also possible

(2) Hardware
   (i) Easy to handle built-in ROM 1-chip devices prepared for application in simple sets
   (ii) Range of voice synthesis LSIs with varying built-in ROM sizes to meet diversified market needs
   (iii) Low power requirements due to CMOS with low fundamental oscillating frequency — ideal also for battery operated applications

(3) Software
   (i) Simple and precise analysis for broader range of user selected sounds
   (ii) Comprehensive range of analytical tools to enable synthesis to be executed by user

Because of the fine quality of sound achieved in a wide range of applications, Oki voice synthesis LSIs are used by a great many users in many different applications.

PRODUCT LINE-UP

Functions and Specifications \ Device		5205	5218	6295	5248	6243	6212	6258		6308	6309
								Stand-alone	MPU interface		
ADPCM Method	Straight	○	○	○	○	○	○	○		○	○
	Compressed	—	—	—	—	○	○	—		—	—
ADPCM Bit Length	3 bit	○	○	—	○	—	○	○		—	—
	4 bit	○	○	○	—	○	—	○		○	○
Oscillation Frequency (Hz)		384 ~ 738K	384 ~ 768M	1 ~ 5M	10 ~ 50K	30 ~ 132K	30 ~ 132K	4 ~ 8 M		4 ~ 6 M	4 ~ 6 M
Maximum Vocalization Time		Determined by external connections	Determubed by external connections	*1 90 sec	*1 3 sec	*2 20 sec	*2 40 sec	Determined external connections		Determined external connections	Determined external connections
Maximum Number of Vocalized Words		Determined by external connections	Determined by external connections	127	7	124	124	7	Determined by external connections	4	4
Analytical Functions		—	○	—	—	—	—	○		○	○
Built-in ROM (Kbits)		—	—	—	48	192	288	—		—	—
Built-in DA Converter		Voltage type	Voltage type	Voltage type	Voltage type	Current type	Voltage type	Voltage type		Voltage type	Voltage type
Built-in AD Converter		—	—	—	—	—	—	○		○	○
External Memory Interface		—	—	○	—	—	—	○		○	○
Input Interface	SW Input	—	—	—	○	○	○	○	—	○	○
	Microcomputer Control	○	○	○	○	○	○	○		○	○
DA Output	A class	○	○	○	—	○	○	○		○	○
	B class	—	—	—	○	○	○	—		—	—
MSC1161 Connection		—	—	—	—	○	○	—		—	—
Power Supply Voltage (V)		5	5	5	3	3 or 5	3 or 5	5		5	5
Power Consumption (in standby mode)		4 mA (−)	4 mA (−)	5 mA (−)	0.5 mA (1.0 μA) (0.5μA)	Note 3 0.5 mA (0.5μA)	Note 3 0.5 mA	4 mA (−)		10 mA (−)	10 mA (1.0μA)
Package Shape		18 DIP	24 DIP 32 flat	44 flat	18-DIP 24 flat chip	40-DIP 44, 60 flat chip	40-DIP 44, 60 flat chip	60 flat	40-DIP 44 flat	44 flat	60 flat
Remarks		—	—	External ROM	ROM code device	ROM code device	ROM code device	—		—	—

Note: *1 Applicable when f_{SAMPLE} = 5.5 kHz
*2 Applicable when f_{SAMPLE} = 8.2 kHz compressed ADPCM
*3 Applicable when power supply voltage is 3 V

COMPARATIVE FUNCTIONS BLOCK DIAGRAM

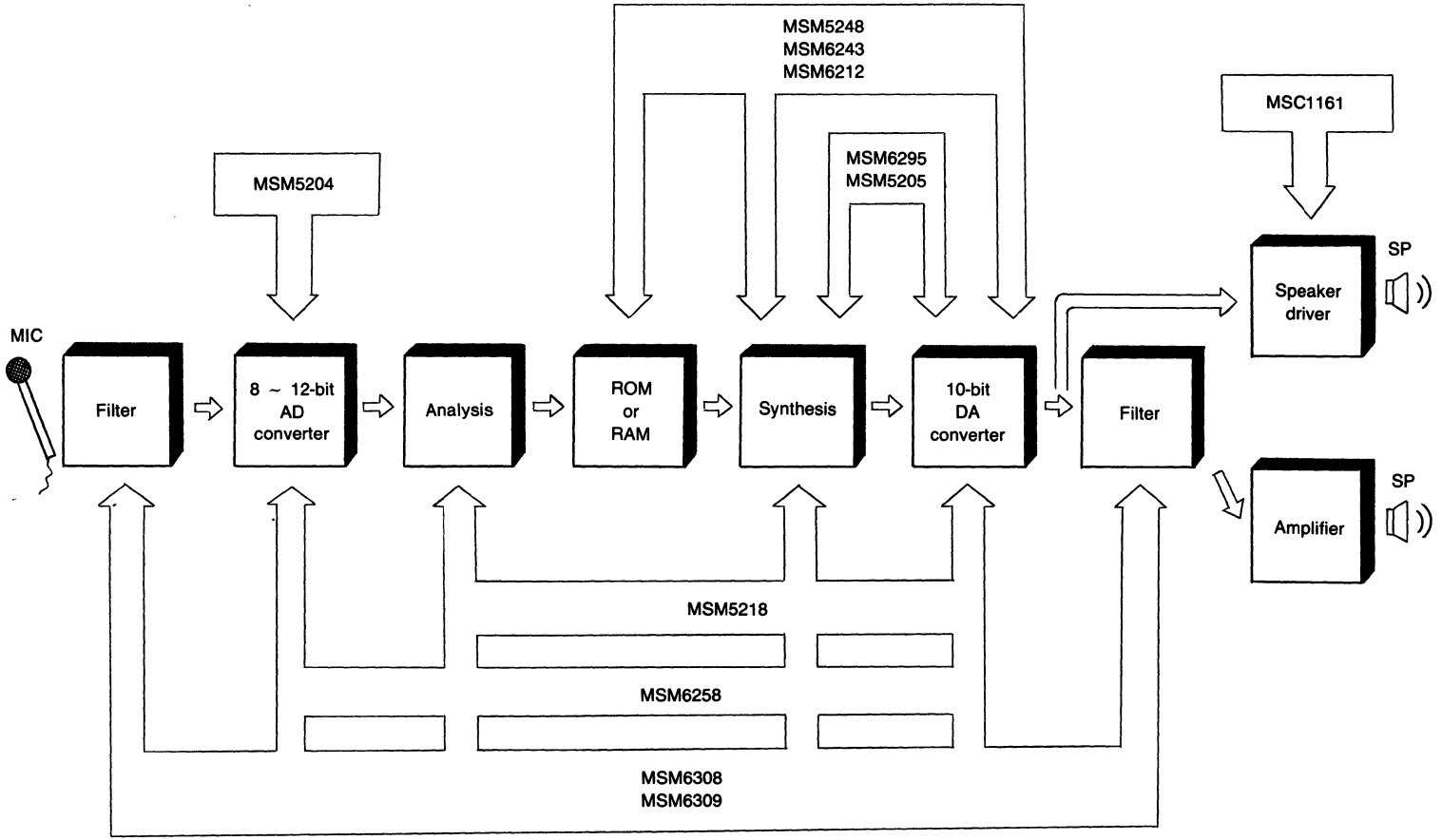


Fig. 2

PACKAGING

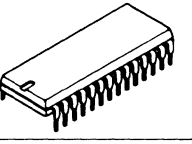
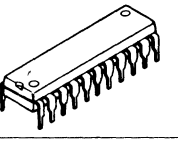
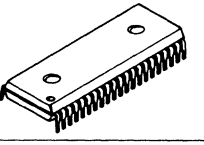
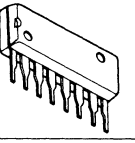
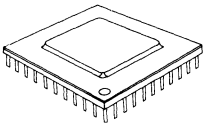
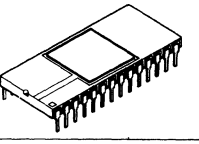
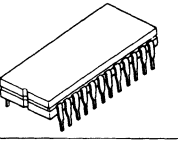
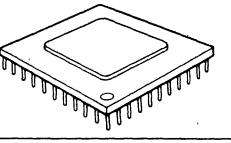
Packaging / Device	Chip	Plastic DIP (RS)			Plastic Flat (GS)			
		18 pin	24 pin	40 pin	24 pin	32 pin	44 pin	60 pin
MSM5205		○						
MSM5218			○			○		
MSM6295							○	
MSM5248	○	○			○			
MSM6243	○			○			○	○
MSM6212	○			○			○	○
MSM6258V				○			○	
MSM6258								○
MSM6308							○	
MSM6309								○
MSC1161	○	○			○			

Oki's Package Types

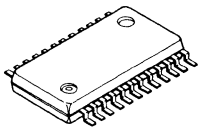
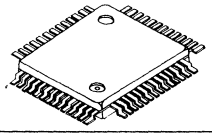
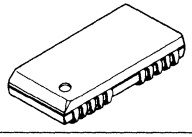
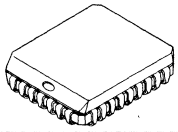
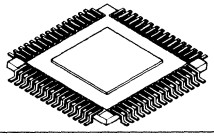
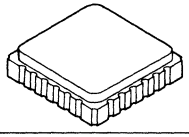
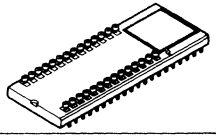
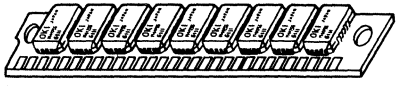
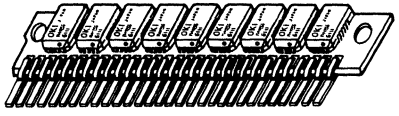
Below are Oki's IC package types and features.

Through-hole and surface-mount IC package types are described as a function of the board mounting method.

PACKAGE TYPES

Type		Package Types			Package Symbol	Pin Count
Through Hole	Plastic	DIP	Standard		RS	8,14,16,18,22,24,28,40,42,48
			Skinny		RS	20,22
			Shrink		SS	42,64
		SIP			RS	8
		PGA			–	*1 88,120,132,176,208
	Ceramic	Standard DIP			AS	14,16,18,22,24,28,40,42,48
		Cer DIP			AS	8,14,16,18,22,24,28,40
		PGA			AS	72,88,120,132,176,208

* 1. In development

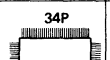
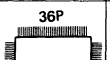
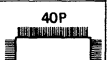
Type	Package Type				Package Symbol	Pin Count
Surface Mount	Plastic	FP	SOP		MS	8, 16, 24, 32
			QFP		GS	*2 *3 *4 24, 32, 44, 56(S), 56(L), 60, 64, 80, 88, 100 128, 136, 144, 160
		PLCC	SOJ		JS	26
			PLCC		JS	18, 20, 22, 28, 32, 44, 68, 84
	Ceramic	QFP			FS	42, 60, 64, 80
		CC			ES	14, 24, 28, 44
Special Packages	Piggyback				VS	40, 42
	SIMM				YS	30
	SIMP				KS	30

*2 Two types of packages are available, thin type and heat-resistant type (with vent hole).

*3 Lead Pins of 24- or 32-pin plastic FPs are in two directions.

*4 (S) and (L) differ in pin pitch and outside dimensions.

For each type of Oki flat pack, the material it is made from, its outline and its pin count are shown here.

Material	Pin Pitch (mm) \ Pin Count	8	16	24	32	42	44	56	60	64	80	88	100	128	136	144	160
Plastic	1.27	 4P (4P×2)	 8P (8P×2)	●  12P (12P×2)	—	—	—	—	—	—	—	—	—	—	—	—	—
	1.00	—	—	—	●  16P (16P×2)	—	—	●  14P (14P×4)	●  14P 16P (14P×2 16P×2)	●  13P 19P (13P×2 19P×2)	—	—	—	—	—	—	—
	0.80	—	—	—	—	—	●  11P (11P×4)	—	—	—	●  16P 24P (16P×2 24P×2)	—	—	 32P 32P (32P×4)	—	—	—
	0.65	—	—	—	—	—	—	●  14P (14P×4)	—	—	—	●  18P 26P (18P×2 26P×2)	●  20P 30P (20P×2 30P×2)	—	 34P 34P (34P×4)	 36P 36P (36P×4)	 40P 40P (40P×4)
Ceramic	1.27	—	—	—	—	 10P 11P (10P×2 11P×2)	—	—	 15P (15P×4)	 16P (16P×4)	 20P (20P×4)	—	—	—	—	—	—

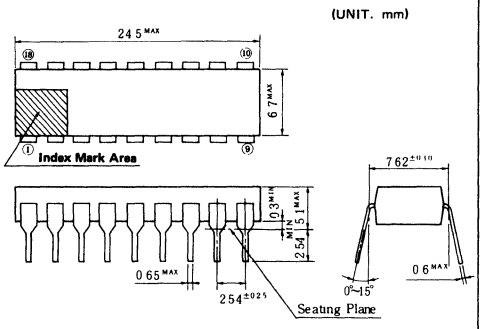
●: Two type of packages are available, thin type and heat-resistant type (with vent hole), which shall be used depending upon board assembly method.

PACKAGE OUTLINES AND DIMENSIONS

• PLASTIC STANDARD DIP

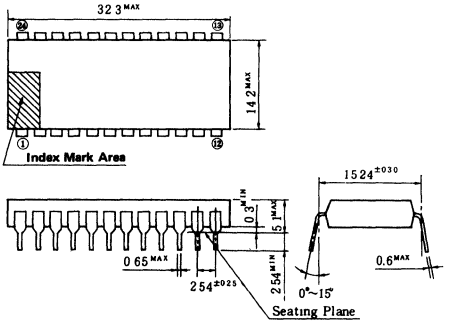
18PIN

(UNIT. mm)



24PIN

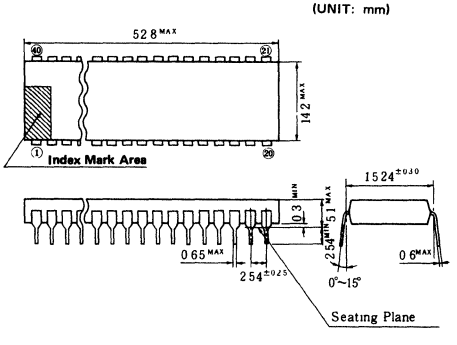
(UNIT: mm)



• PLASTIC QFP

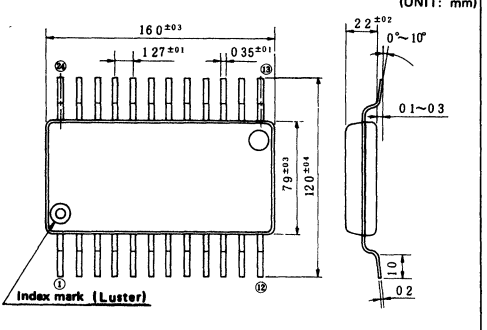
40PIN

(UNIT: mm)



24PIN

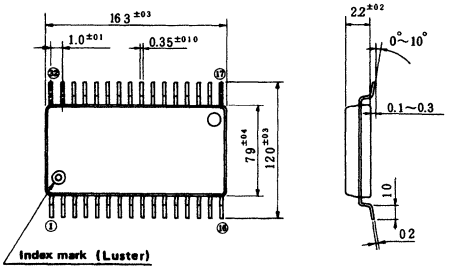
(UNIT: mm)



- **PLASTIC QFP**

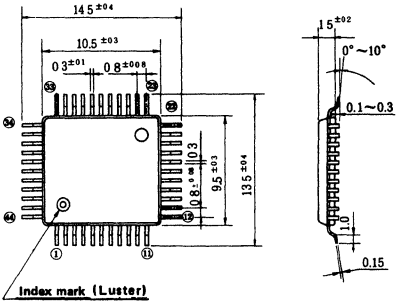
32PIN

(UNIT. mm)



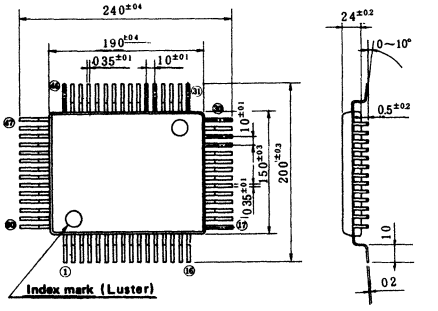
44PIN

(UNIT· mm)



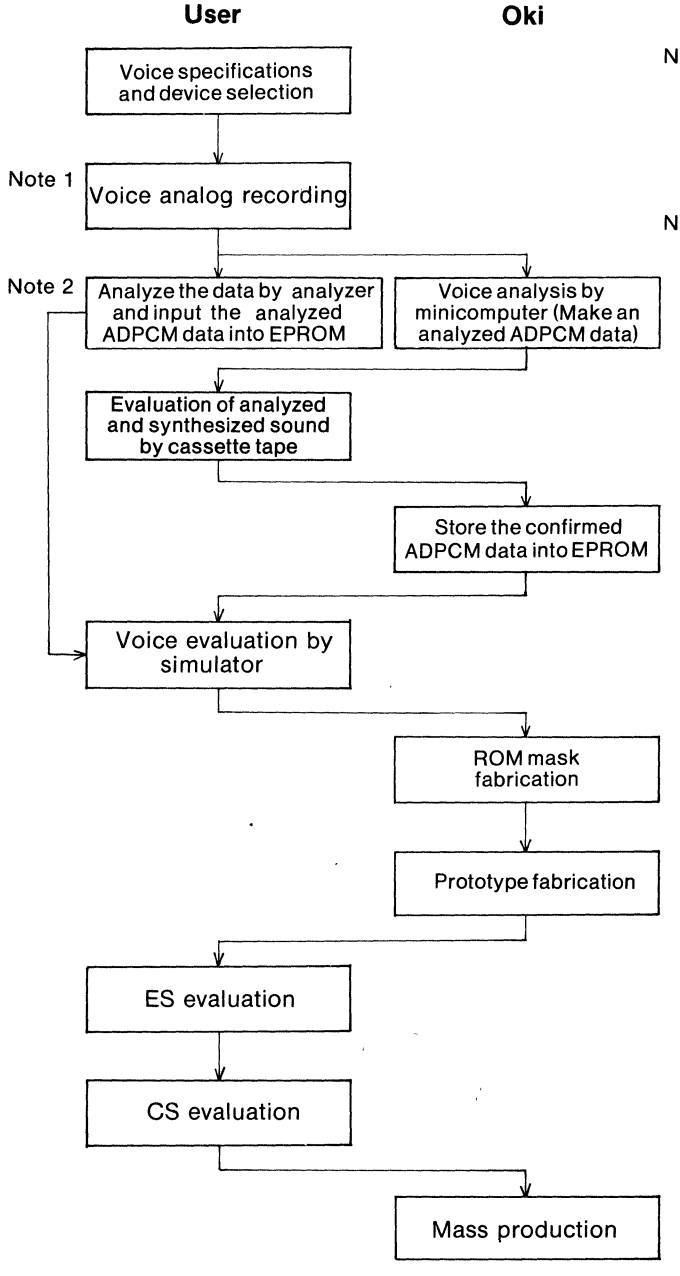
60PIN

(UNIT mm)



USEFUL INFORMATION

BUILT-IN ROM VOICE SYNTHESIS LSI DEVELOPMENT FLOWCHARTS (MSM5248, MSM6243, and MSM6212)



Note 1. Record the source sound on an open-reel tape deck. Recording assistance and studio/announcer can also be arranged where required.

Note 2. The voice analysis flowchart is divided into two paths as indicated. Where analysis is to be performed by the user, suitable ADPCM data can be readily generated by analyzer.

Fig. 3

USER ANALYSIS SUPPORT TOOLS

■ **OSA-1 (OKI Speech Analyzer)**

OSA-1 enables user to make a straight/compressed ADPCM data for MSM6243 and MSM6212 instantanuously by inputting the voice from the line input via microphone or tape deck player. OSA-1 also can output the analyzed ADPCM data. The analyzed data can be stored into the EPROM by connecting OSA-1 via RS232C interface.

The OSA-1 enables the user himself to change the degree of compression voice analysis purposes, thereby enabling sounds preferred by the user to be generated.

Furthermore, if EPROMs generated with the OSA-1 are used together with a simulator (described later) the quality of the sound when the LSI is formed can be evaluated. OSA-1 is available to users on a loan basis.

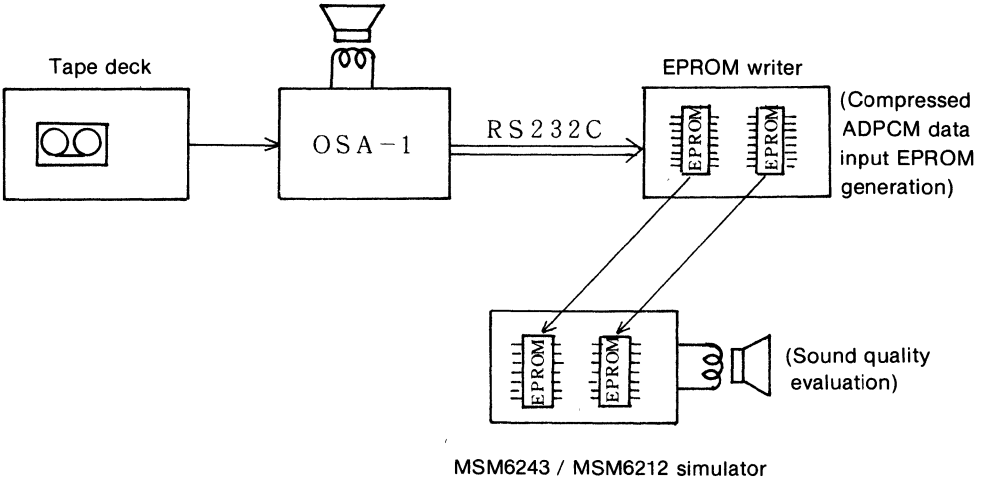


Fig. 4 Voice analysis and evaluation block diagram where OSA-1 is used

■ Speech Analyzer

The speech analyzer set using MSM5218RS is used to make an ADPCM data on real-time basis by inputting voice from microphone or tape deck player etc. Analyzed data is stored in a built-in RAM, and can be written into an EPROM by a built-in EPROM writer.

This EPROM can be used as the voice simulator's data or as ROM data for MSM5248 etc. For further details, please contact

Nihon Denso Kogyo Co., Ltd.
3-14-19 Shibaura, Minato-ku,
Tokyo, Japan TEL. (03) 452-2351

■ MSM5248 Simulator

The MSM5248 simulator has the same functions as the MSM5248. When the EPROM, in which the analyzed data is stored, is mounted on this simulator, this simulator can synthesize the same quality voice data as that of MSM5248.

■ MSM6243 Simulator, MSM6212 Simulator

When the EPROM, in which the analyzed data by using OSA-1 is stored, is mounted on the simulator these simulators can synthesize the same quality voice data as that of MSM6243, MSM6212 respectively.

DATA SHEET

OKI semiconductor

MSM5205

ADPCM SPEECH SYNTHESIS IC

GENERAL DESCRIPTION

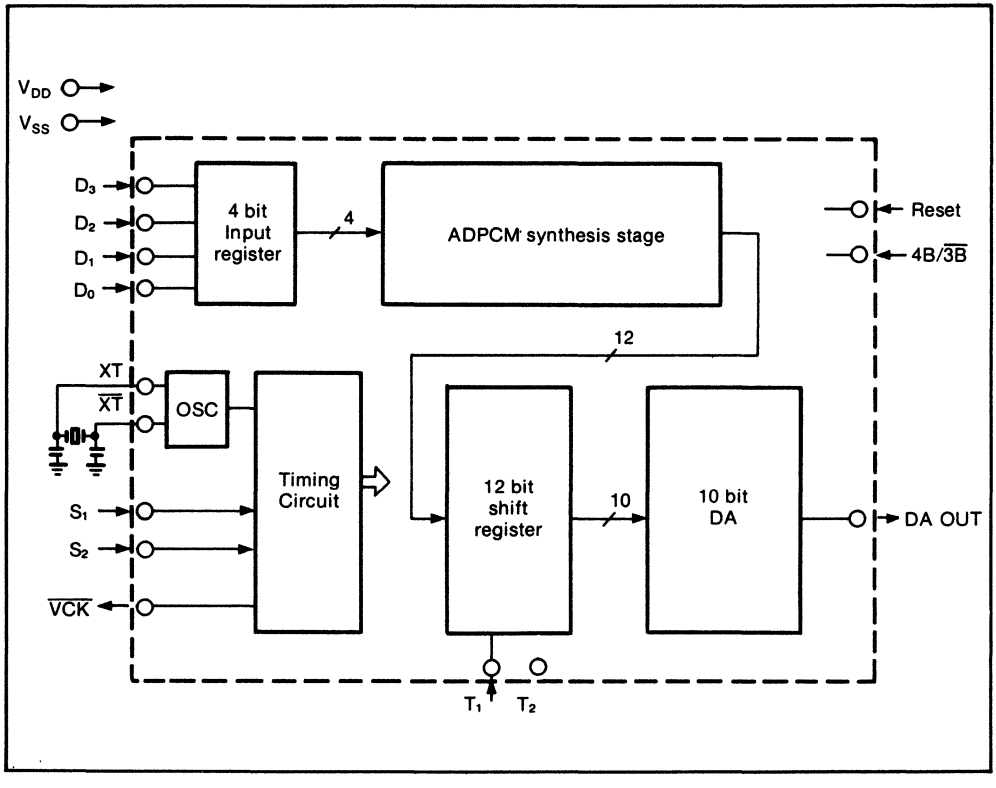
The MSM5205 is a speech synthesis integrated circuit which accepts Adaptive Differential Pulse Code Modulation (ADPCM) data. The circuit consists of synthesis stage which expands the 3- or 4-bit ADPCM data to 12-bit Pulse Code Modulation (PCM) data and a D/A stage which reproduces analog signals from the PCM data.

The MSM5205 is fabricated using Oki's advanced CMOS process which enables low power consumption. The single power supply requirement and its availability in 18-pin molded DIP allow the MSM5205 to be ideally suited for various applications.

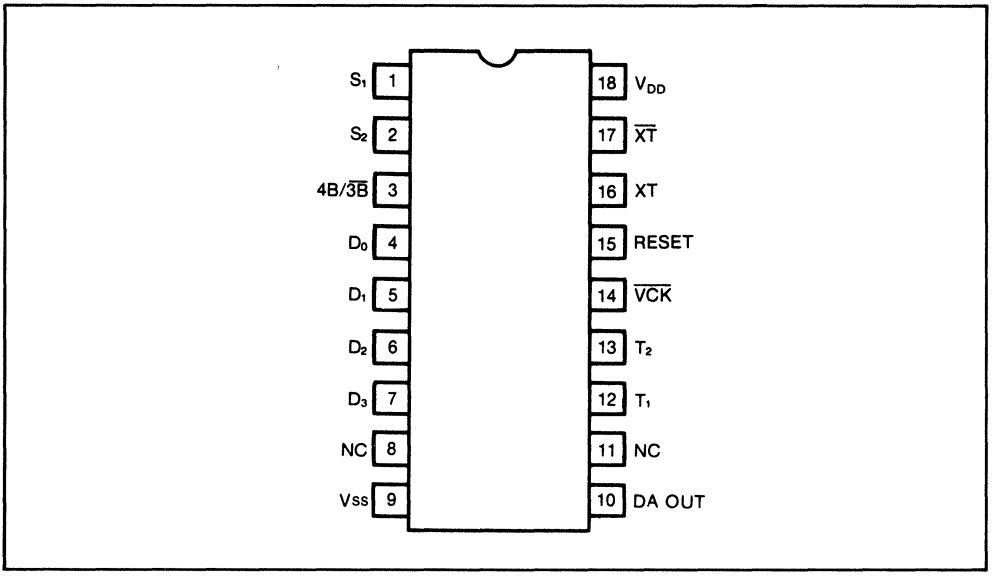
FEATURES

- 3 or 4 bit ADPCM system
- 12 to 32 kb/sec with INT $\overline{VCK}$
- On-chip 10-bit D/A converter
- Low power consumption (10 mW typical)
- Single +5V supply
- Wide operating temperature (Ta = -30°C to +70°C)
- 18-pin molded DIP

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	Ta = 25° C	-0.3 to +7.0	V
Input voltae	V_{IN}	Ta = 25° C	-0.3 to V_{DD}	V
Power dissipation	P_D	Ta = 25° C	200 max	mW
Storage temperature	Tstg	—	-55 to +150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device raliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	—	+3 to +6	V
Operating temperature	Top	—	-30 to +70	°C

D.C./A.C. CHARACTERISTICS

(V_{DD} = 5V ± 5%; Ta = -30° C to +70° C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	All inputs except T_1, T_2	4.2	—	V_{DD}+.3	V
Input Low Voltage	V_{IL}	All inputs except T_1, T_2	V_{SS}—.3	—	0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	—	—	1	μA
Input Low Current	I_{IL}	V_{IN} = 0V	—	—	-1	μA
Output High Current	I_{OH}	$\overline{VCK}$ pin: Vo = 4.2V	-50	—	—	μA
Output High Current	I_{OL}	$\overline{VCK}$ pin: Vo = 0.4V	+50	—	—	μA
Oscillator Frequency	f_{OSC}	Specified Oscillator	—	384	768	kHz
Operating Current	I_{DD}	f_{OSC} = 384 kHz V_{DD} = 5V	—	2	4	mA
D/A Accuracy (Internal 10-bit D/A)	V_E	Full Scale; V_{DD} = 5V	—	±4	—	LSB
DA_{OUT} Output Impedance	V_{OR}		—	100	—	KΩ

PIN DESCRIPTION

Pin Name	Terminal Number	I/O
S_1	1	I
S_2	2	I

These inputs select the sampling frequency according to Figure 1.

4B/$\overline{3B}$	3	O

Specifies whether 3-bit or 4-bit ADPCM data is to be processed.

D_0	4	I
D_1	5	I
D_2	6	I
D_3	7	I

ADPCM data inputs. For 3-bit ADPCM data, D_0 input is not used and should be connected to ground.

V_{SS}	9	I

Ground (0 V)

DA_{OUT}	10	O

Output for synthesized analog signal. Peak-to-peak swing is proportional to V_{DD}. Typical connection scheme is shown Figure 2.

PIN DESCRIPTION (continued)

T_1	12	I
T_2	13	I

IC test pins used at the factory for testing purposes only. During normal operations, T_1 is grounded and T_2 is left open.

Pin Name	Terminal Number	I/O
$\overline{VCK}$	14	O

This pin outputs a signal whose frequency is equal to the sampling frequency selected by the S_1, S_2 inputs. See note *1.

RESET	15	I

An active high input which initializes the internal circuitry. Internally, the reset pulse is synchronized with the $\overline{VCK}$ signal. To be effective, it must be true for at least twice $\overline{VCK}$ time.

XT	16	I/O
$\overline{XT}$	17	I/O

Oscillator input and output for a 384 kHz crystal or ceramic resonator (Figure 3).

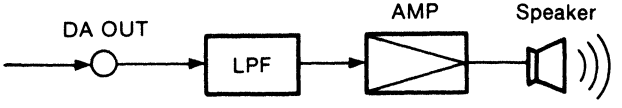
V_{DD}	18	I

Power supply pin (Typical +5 V)

S1	S2	Sampling Frequency
L	L	4 kHz (384 kHz/96)
L	H	6 kHz (384 kHz/64)
H	L	8 kHz (384 kHz/48)
H	H	Prohibited See Note *1

Note: *1 The 384 kHz oscillator must be used whether 4 kHz, 6 kHz, 8 kHz.

Figure 1 Functional table



Cut off frequency fc of LPF should be related to the selected sampling frequency f sample by,

$$fc = f\ sample/2 \times 0.85$$

Sound quality is strongly dependent on the sharpness of the low pass filter.

*If the 5205 is sent a stream of ADPCM data that causes greater than full scale output, the D/A output will wrap around: +5 0.0 +5.

Figure 2

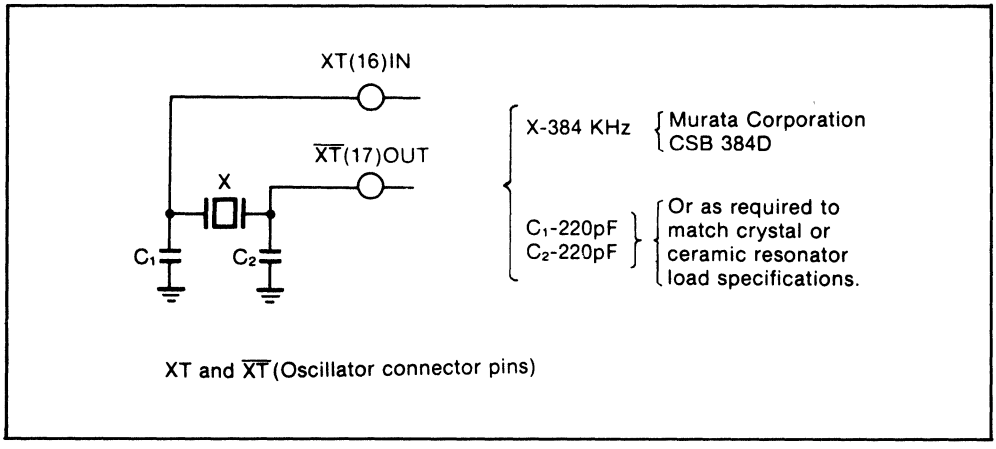


Figure 3

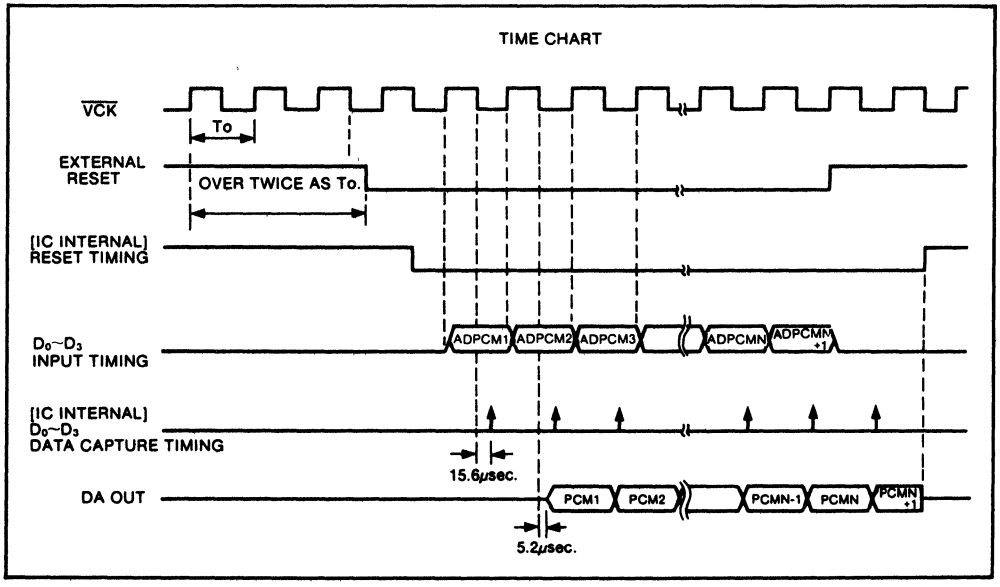


Figure 4

DISTINCTION BETWEEN MSM 5218 AND MSM5205

Both Synthesis stages (MSM5218 and MSM5205) work with the same method. However, with the exception that MSM5218 is equipped with an overflow protection.
In other words, when all 12 PCM bits become '1' any further exceeding analog input would cause a data overflow which is catched and re-routed as the MSB in case of MSM5218.
MSM5205 returns to 'all bits zero' when a data overflow sets in.
Therefore, the DA output of MSM5205 is distorted badly.

When MSM5218 is being used to generate ADPCM data for playback on MSM5205, the peak to peak input level to the A to D converter should be limited to 80% of the converters maximum input range. The use of an automatic gain control (AGC) amplifier or a hard limiter is recommended.

TYPICAL APPLICATION

MSM5205 to Centronics Interface Circuits (f_{SAMPLE} = 8kHz)

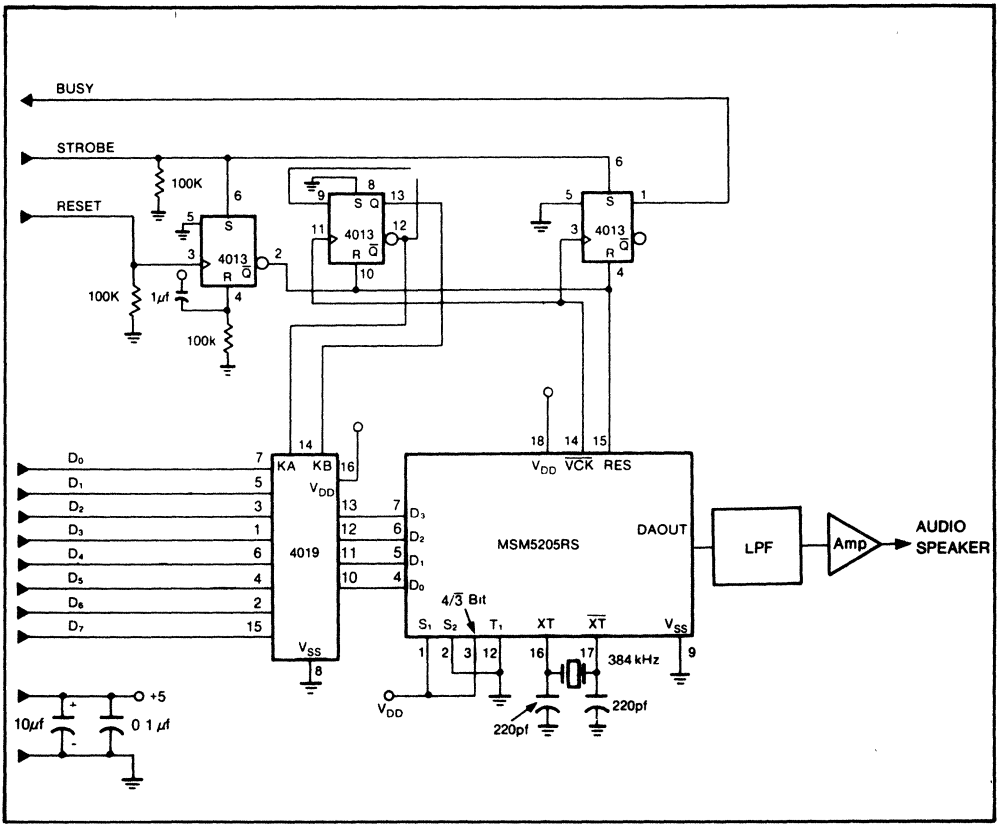


Figure 5

MSM5205 to Centronics Timing Diagram

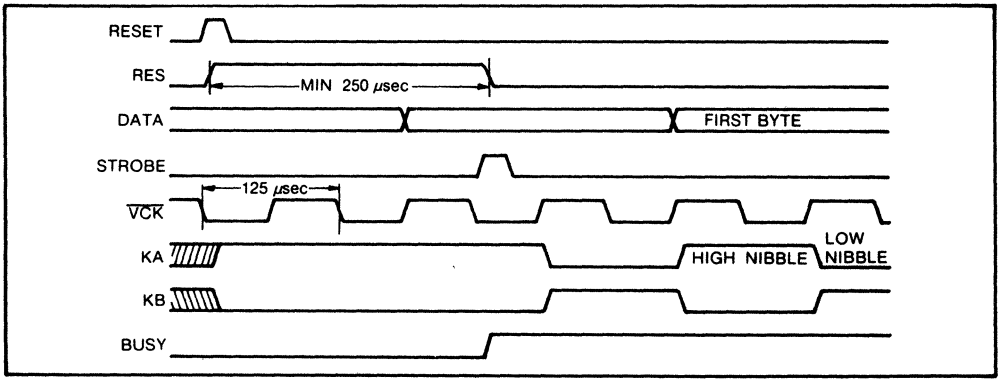


Figure 6

MSM5218

ADPCM SPEECH ANALYSIS/SYNTHESIS IC

GENERAL DESCRIPTION

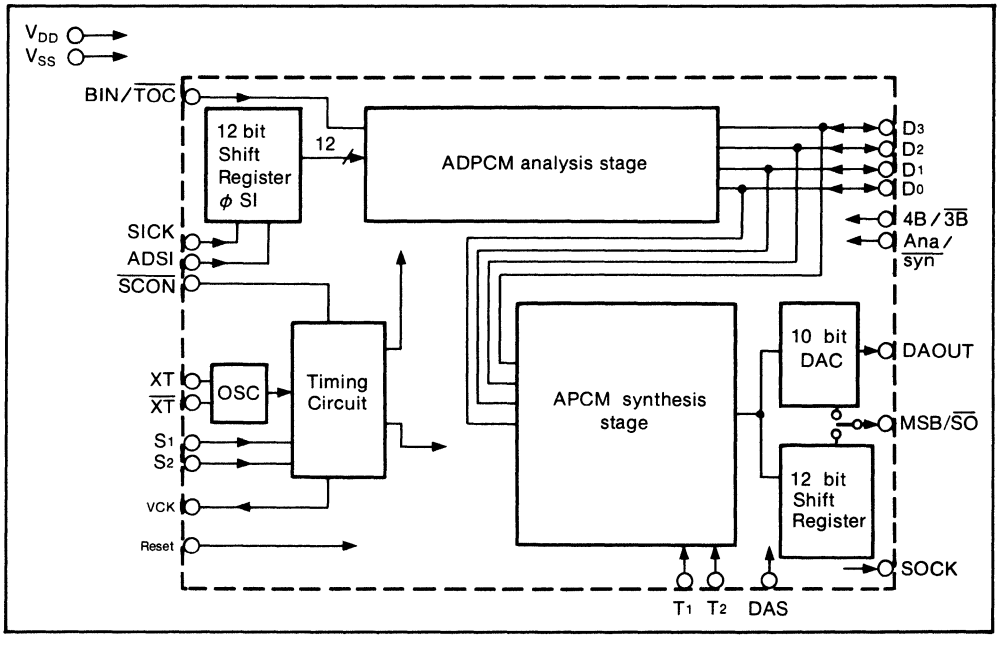
The MSM5218 is a complete speech analysis/synthesis LSI featuring the Adaptive Differential Pulse Code Modulation (ADPCM) method of data compression. The MSM5218 contains an analysis stage where serial PCM data is compressed to 3- or 4-bit parallel ADPCM data. In addition, a synthesis stage synthesizes PCM data from ADPCM data. This PCM data can be output directly or routed to the internal 10-bit DAC for analog signal output.

In addition to simplifying speech analysis and simulation, this circuit enables users to develop their own speech analysis and synthesis systems.

FEATURES

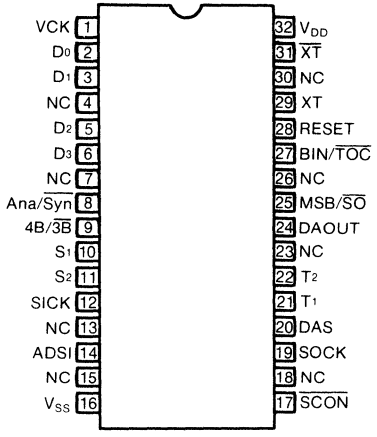
- One-chip speech analyzer/synthesizer
- 3- or 4-bit ADPCM system
- ADPCM data compatible with Oki's synthesis LSI MSM5205RS
- Single power supply
- Variable sampling frequency (4 kHz, 6 kHz, 8 kHz)
- Low power consumption CMOS process (15 mW typical)
- Built-in 10-bit D/A converted for analog output
- Handshaking signals provided for synchronous operation with an external A/D converter.
- 24 pin plastic DIP, 32 pin plastic flat.

FUNCTIONAL BLOCK DIAGRAM

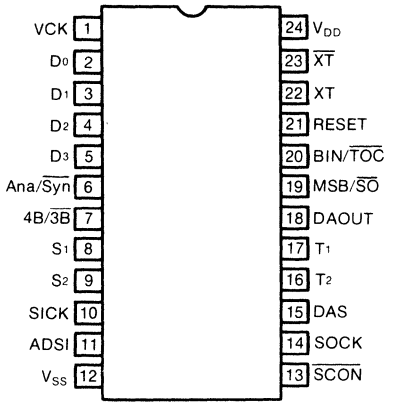


PIN CONFIGURATION

(Top View) 24 Lead Plastic DIP



(Top View) 32 Lead Plastic Flat Package



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	Ta = 25°C	-0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	-0.3 to V_{DD}	V
Power dissipation	P_D	Ta = 25°C	200 max	mW
Storage temperature	Tstg	—	-55 to +150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may after device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	—	+3 to +6	V
Operating temperature	Top	—	-30 to +70	°C

D.C./A.C. CHARACTERISTICS

(V_{DD} = 5V ± 5%, Ta = −30°C to +70°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	All input except T_1, T_2	4.2	—	—	V
Input Low Voltage	V_{IL}	All inputs except T_1, T_2	—	—	0.8	V
Input High Current(1)	I_{IH}	$V_{IN} = V_{DD}$	—	—	1	μA
Input Low Current	I_{IL}	V_{IN} = 0V	—	—	-1	μA
Output High Current	I_{OH}	$\overline{SCON}$, VCK, SOCK, MSB/$\overline{SO}$, D0~D3 Vo = 4.2V	-50	—	—	μA
Output Low Current	I_{OL}	$\overline{SCON}$, VCK SOCK, MSB/$\overline{SO}$, D0 ~ D3 Vo = 0.4V	50	—	—	μA
Oscillator Frequency	f_{OSC}	Specified Oscillator	—	384	768	kHz
Operating Current Operating Current	I_{DD} I_{DD}	f_{VCK} = 8 kHz f_{VCK} = 16 kHz	— —	3 6	6 12	mA mA
DA. OUT Output Impedance	V_{OR}		100	—	kΩ	
D/A Accuracy (Internal 10-bit D/A)	V_E	Full Scale V_{DD} = +5V	—	±4	—	LSB
SICK Clock Frequency	f_{SICK}		—	—	500	kHz
Input High current (2)	I_{IH2}	$V_{IN} = V_{DD}$ Note 1	20	—	400	μA

Note1: Applicable for Reset

PIN DESCRIPTION

Pin Name	Terminal Number		I/O
	24 DIP	32 FLT	
V_{CK}	1	1	O

This pin outputs a signal whose frequency is equal to the sampling frequency selected by S1, S2 inputs.

D_0	2	2	I/O
D_1	3	3	I/O
D_2	4	5	I/O
D_3	5	6	I/O

Data I/O port for the ADPCM data. For 3-bit ADPCM data, D_0 input is not used.

ANA/$\overline{SYN}$	6	8	I/O

Analyze/synthesize function selector. Controls data I/O port direction. When high, data I/O are outputs and simultaneous analysis and synthesis occur. When low, data I/O are inputs and no analysis occurs.

4B/$\overline{3B}$	7	9	O

Specifies whether 3-bit or 4-bit ADPCM data is to be used. High = 4-bit.

S_1	8	10	I
S_2	9	11	I

These inputs select the sampling frequency according to figure 1.

SICK	10	12	I

Clock input for clocking in serial PCM data from an external ADC into the internal 12-bit shift resister.

ADSI	11	14	I

Serial PCM data input.

V_{SS}	12	16	I

Ground (0V)

$\overline{SCON}$	13	17	O

Output which signals the start of conversion.

SOCK	14	19	O

When serial PCM data output mode is selected (DAS = H), this pin provides a 192 kHz signal which is synchronized with the output of the serial PCM data through the MSB/$\overline{SO}$ pin. Each bit of the 12-bit PCM data will be valid before the positive edge of this 192 kHz signal.

DAS	15	20	O

Selector for analog signal output (DAS = L), or serial PCM data output (DAS = H).

Pin Name	Terminal Number		I/O
	24 DPI	32 FLT	
T1	17	21	I
T2	16	22	I

IC test pins used at factory for testing purposes only. During normal operation, T1 is grounded and T2 is left open.

DAOUT	18	24	O

Analog signal output pin.

MSB/$\overline{SO}$	19	25	O

MSB/serial data output pin — MSB of the data in the internal 10-bit DAC will appear at this pin if analog signal output mode (DAS = L) is selected. When serial PCM data output mode is selected (DAS = H), serial PCM data can be clocked out of this pin.

BIN/$\overline{TOC}$	20	27	I

Specifies whether the input serial PCM data is in binary or 2's complement form.

RESET	21	28	I

An active high input which initializes the MSM5218RS internal circuitry. To be effective, must be held true for at least one VCK time.

XT	22	29	I
$\overline{XT}$	23	31	I

Oscillator inputs for a 384 kHz crystal or ceramic resonator (Figure 2).

V_{DD}	24	32	I

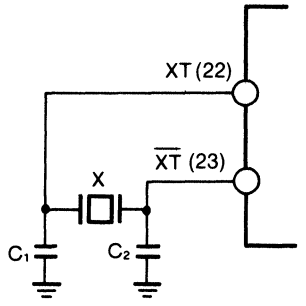
Power supply pin. (typical +5V)

S1	S2	Sampling Frequency
L	L	4 kHz (384 kHz/96)
L	H	6 kHz (384 kHz/64)
H	L	8 kHz (384 kHz/48)
H	H	Prohibited

Note: The 384 kHz oscillator must be used whether 4 kHz, 6 kHz, 8 kHz.

With 384 kHz oscillator. Other oscillator frequencies are possible and will proportionately modity the sample rate.

Figure 1



X-384 KHz

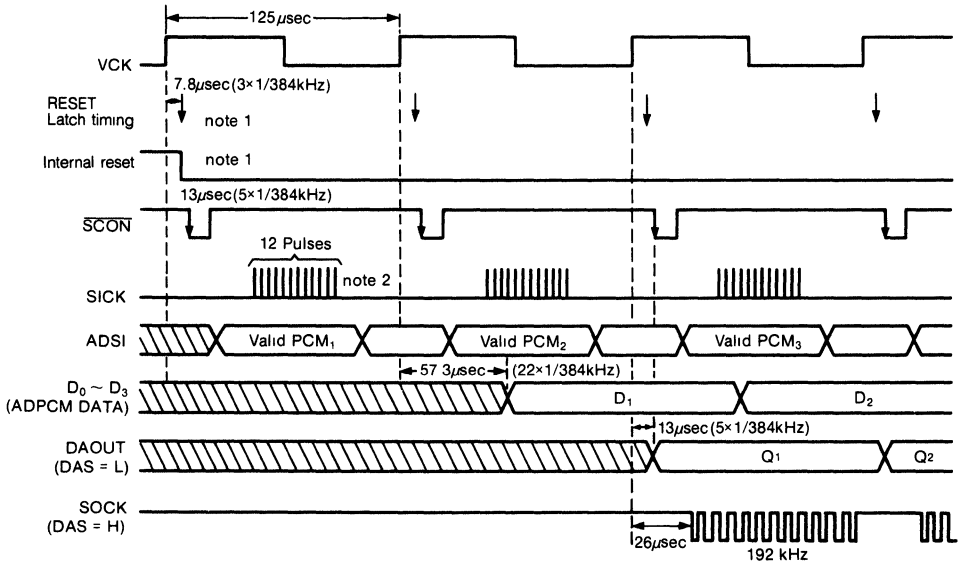
C_1-220pF
C_2-220pF

Murata Corporation
CSB 384P
Or as required to match crystal or ceramic resonator load specifications.

XT and $\overline{XT}$ (Oscillator connector pins)

Figure 2

ANALYSIS WITH SIMULTANEOUS SYNTHESIS (f_{SAMPLE} = 8kHz)

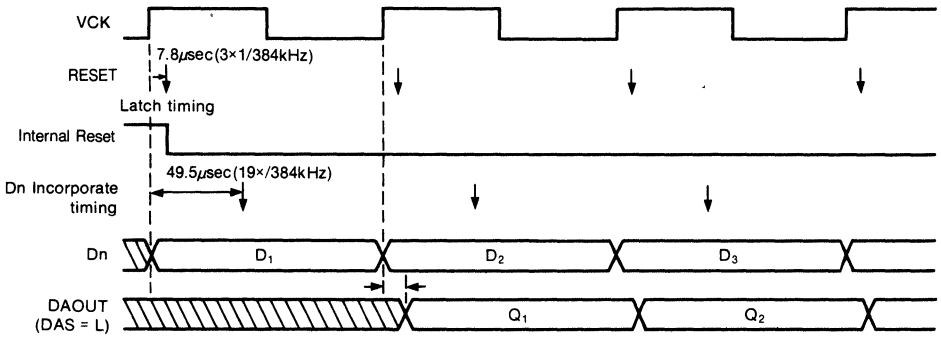


Note 1: The state of the RESET input is strobed into the internal reset latch by the reset latch timing pulse. Analysis begins on the H to L transition of internal reset

Note 2: Up to 12 bits of PCM data may be strobed into the device by SICK. If more than 12 SICK pulses occur in a given VCK cycle, only the last 12 are regarded as valid. The cycle of SICK pulses must be completed before the next SCON- pulse.

PCMn: nth input PCM data (12 bits)

SYNTHESIS ONLY (f_{SAMPLE} = 8kHz)



Dn: nth ADPCM data.

Qn: Analog output corresponding to input nth ADPCM data.

Figure 3

BLOCK DIAGRAM - ANALYZER

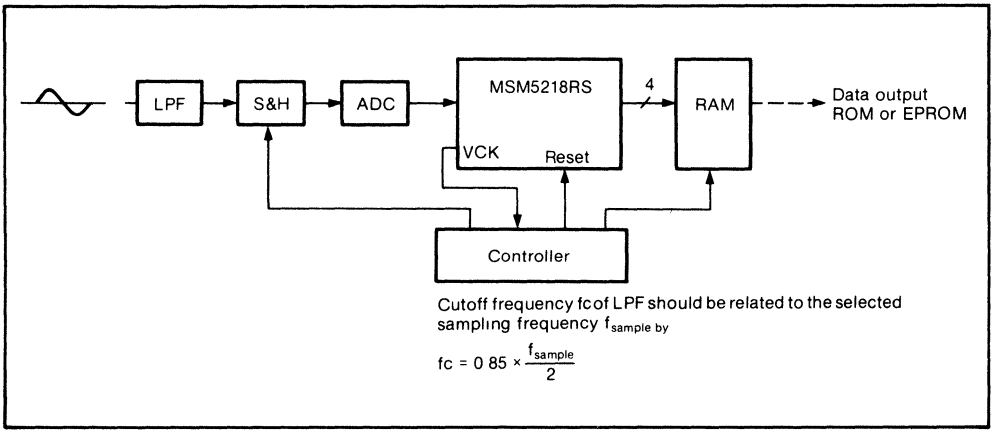


Figure 4

BLOCK DIAGRAM - SYNTHESIZER

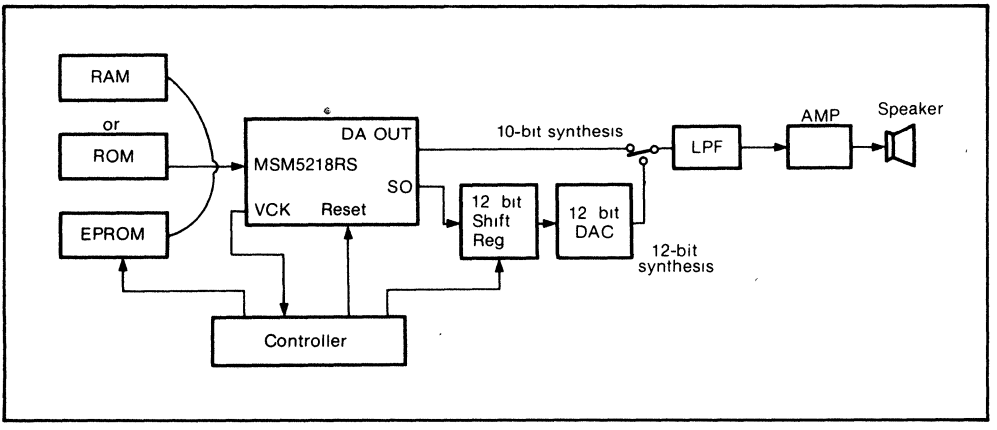


Figure 5

DISTINCTION BETWEEN MSM5218 AND MSM5205

Both Synthesis stages (MSM5218 and MSM5205) work with the same method. However, with the exception that MSM5218 is equipped with an overflow protection.
In other words, when all 12 PCM bits become '1' any further exceeding analog input would cause a data overflow which is catched and re-routed as the MSB in case of MSM5218.
MSM5205 returns to 'all bits zero' when a data overflow sets in.
Therefore, the DA output of MSM5205 is distorted badly.

When MSM5218 is being used to generate ADPCM data for playback on MSM5205, the peak to peak input level to the A to D converter should be limited to 80% of the converters maximum input range. The use of an automatic gain control (AGC) amplifier or a hard limiter is recommended.

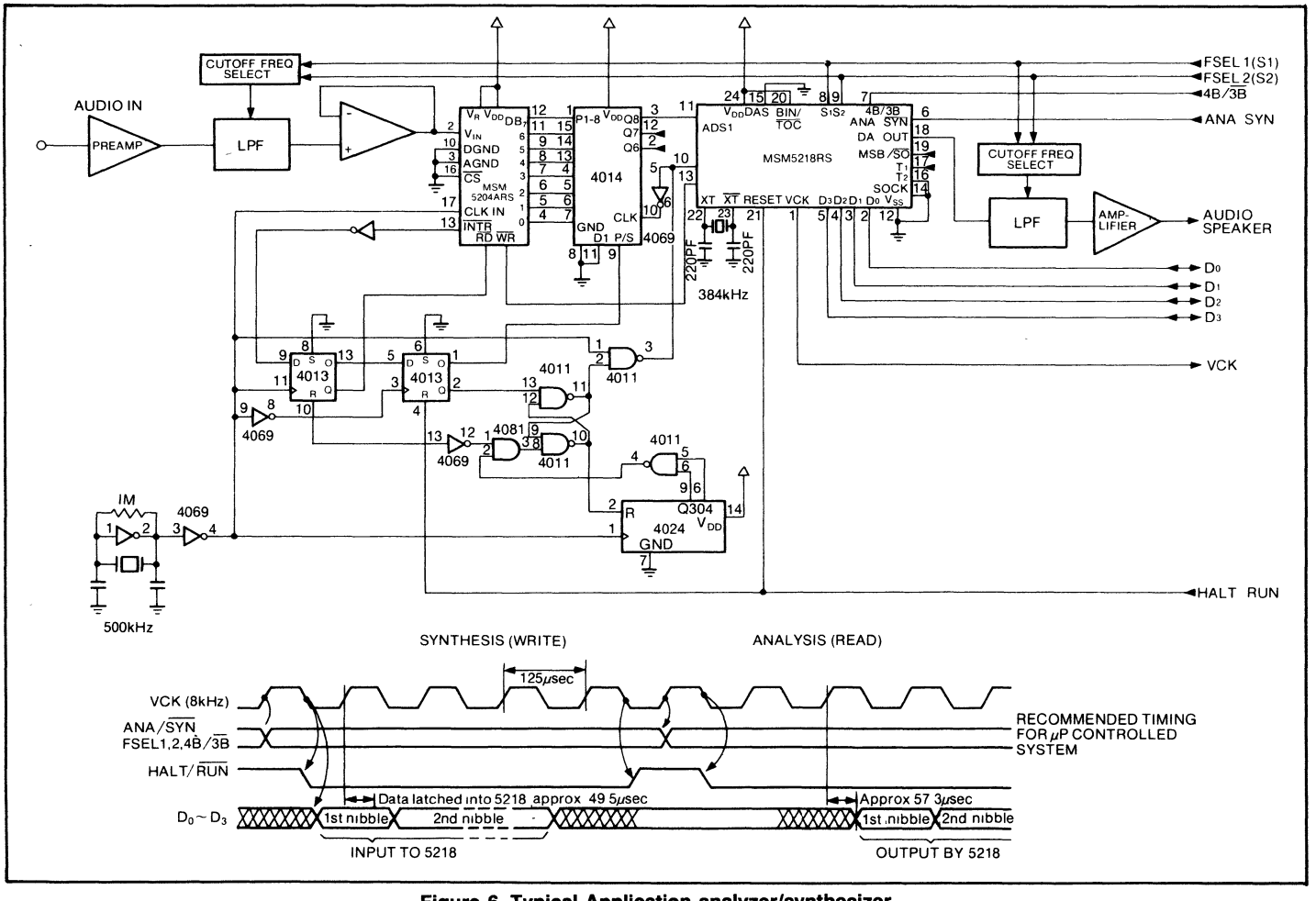


Figure 6 Typical Application analyzer/synthesizer

OKI semiconductor

MSM6295

4-CHANNEL ADPCM VOICE SYNTHESIS LSI

GENERAL DESCRIPTION

The Oki MSM6295 is a 4-channel ADPCM voice synthesis LSI which is fabricated using Oki's low power CMOS silicon gate technology.

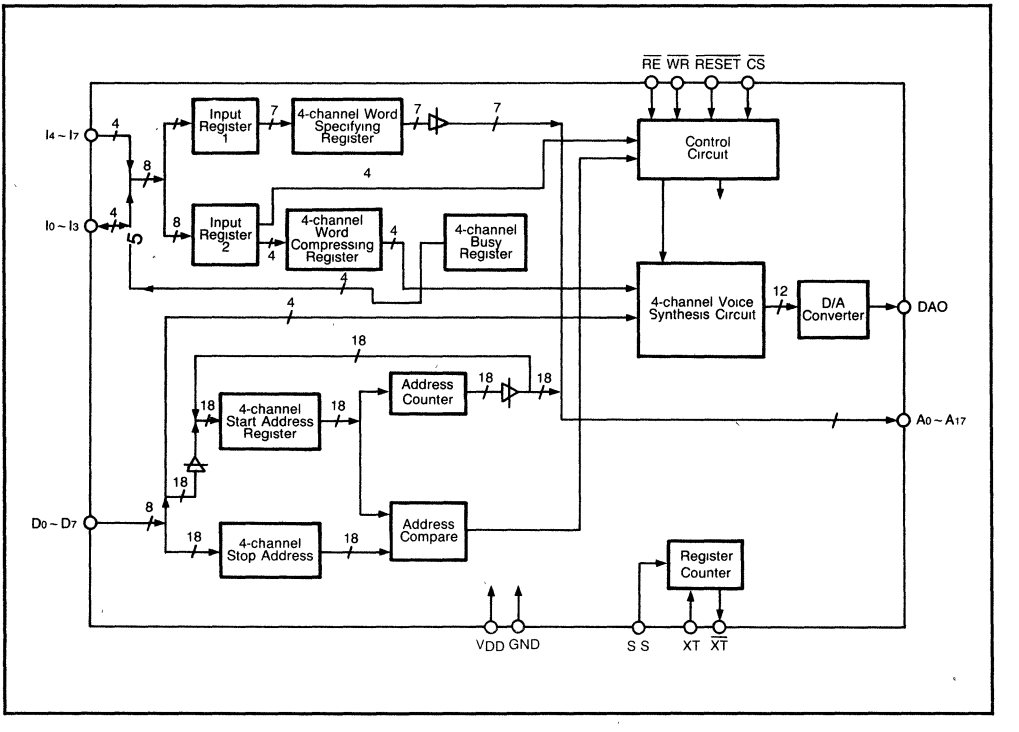
The MSM6295 can access an external ROM, where speech or sound effect data is stored. The maximum size ROM is 256K bytes.

The MSM6295 has a 4-channel synthesis stage which allows the simultaneous playback of four different channels. So, it is quite useful to have a voice with BGM effect, instrumental sound, echo etc.

FEATURES

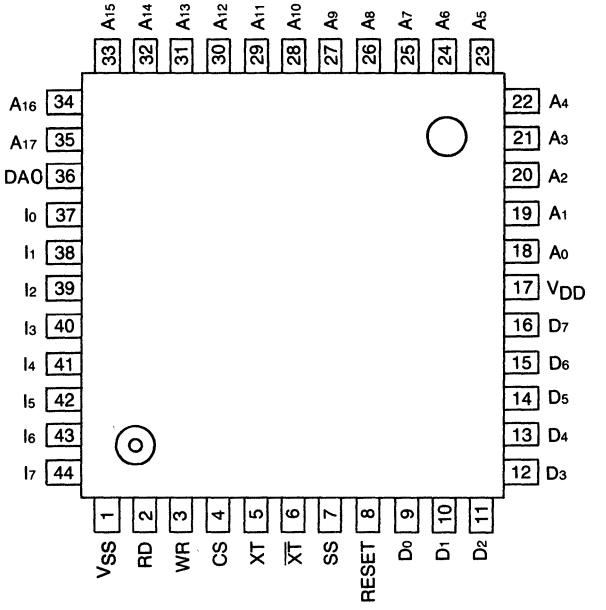
- Oki straight ADPCM algorithm
- Number of bits/sample: 4
- 18 address lines for external ROM
- 8-bit control bus for mode setting
- External memory capacity 2M-bit
- Interface with common CPU and MPU
- Clock frequency: 1 MHz and 4 MHz
- Sampling frequency: 6.4 kHz and 8 kHz (@ 1 MHz clock)
  25.6 kHz and 32 kHz (@ 4 MHz clock)
- Number of words: 127 maximum
- Vocalization time: 60 sec maximum (@ 8 kHz, straight)
- Built-in DA converter: 12-bit
- DA output format: A class
- Voice level reduction on each channel: −3 dB ~ −24 dB (8 steps) −3 dB/step
- Low power CMOS process
- 3 V or 5 V single power supply
- 44 pin plastic flat package

BLOCK DIAGRAM



PIN CONFIGURATION

44 pin Flat Package



PIN DESCRIPTION

Pin Symbol	Pin No.	I/O	Function
I0	37	I/O	Data bus and condition output These terminals are inputs of phrase specification. Maximum number of phrases is 127. Also, I0 ~ I3 terminals are outputs of operating state, busy state, for 1 ~ 4 channel.
I1	38	I/O	
I2	39	I/O	
I3	40	I/O	
I4	41	I	
I5	42	I	
I6	43	I	
I7	44	I	
$\overline{WR}$	3	I	Writing input Write the data on the data bus of I0 ~ I7. The data is written by the setting-up of $\overline{WR}$.
$\overline{RD}$	2	I	Reading out input Output busy state of 1 ~ 4 channel on the data bus of I0 ~ I3. "L" level or "H" level is output while RD is "L". When it becomes "H", busy state is output.

PIN DESCRIPTION (continued)

<table>
<tr><th>Pin Symbol</th><th>Pin No.</th><th>I/O</th><th>Function</th></tr>
<tr><td>$\overline{CS}$</td><td>4</td><td>I</td><td>Chip selection input
Input "L" level either when $\overline{WR}$ signal is input or when $\overline{RD}$ signal is input.</td></tr>
<tr><td>$\overline{RESET}$</td><td>8</td><td>I</td><td>Reset input
Reset condition is available by inputting "L" level. All functions are suspended during reset.</td></tr>
<tr><td>A_0
~
A_{17}</td><td>18
~
35</td><td>I
~
I</td><td>Address output
These terminals are to addresses the external ROM in which original voice data is stored.</td></tr>
<tr><td>D_0
~
D_7</td><td>9
~
16</td><td>I
~
I</td><td>Input of original voice data
Input the data from external ROM which stores original voice data.</td></tr>
<tr><td>SS</td><td>7</td><td>I</td><td>Sampling input
Selecting sampling frequency.
When oscillation frequency is 1.18 MHz or 4.13 MHz, following choices are available by inputting "H" level or "L" level into SS.
<table>
<tr><th></th><th>SS="H"</th><th>SS="L"</th></tr>
<tr><td>Oscillation frequency 1.18 MHz</td><td>8 kHz</td><td>6.4 kHz</td></tr>
<tr><td>Oscillation frequency 4.13 MHz</td><td>32 kHz</td><td>25.6 kHz</td></tr>
</table></td></tr>
<tr><td>DA_0</td><td>36</td><td>O</td><td>Voice synthesis output
Voice synthesized analog signal is output from this terminal.</td></tr>
<tr><td>XT</td><td>5</td><td>I</td><td>Crystal oscillator connector terminal.</td></tr>
<tr><td>$\overline{XT}$</td><td>6</td><td>O</td><td>Same as above</td></tr>
<tr><td>V_{DD}</td><td>17</td><td>I</td><td>Power supply terminal</td></tr>
<tr><td>V_{SS}</td><td>1</td><td>I</td><td>Ground</td></tr>
</table>

FUNCTION EXPLANATION

1. Phrase Specification

Phrases are specified and read into the 2 byte data which is made up of $I_0 \sim I_7$ data bus. The phrases specification data are latched when $\overline{WR}$ goes high while $\overline{CS}$ keeps low (L).
Format of phrase specification input is as follows.

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
1 Byte	1	Phrase specification data						
2 Byte	Channel specification				Reduction specification			

As shown in the above chart, I_7 of the first 1 byte data is 1. $I_0 \sim I_6$ of the first 1 byte data specifies the phrase. Phrase specification data has a selection of 127 phrases which corresponds to 0000001 ~ 1111111. The phrase specification data is equivalent to $A_3 \sim A_9$ address outputs, and specify both start and stop address which are stored in the external out ROM.

CORRESPONDENSE BETWEEN PHRASE SPECIFICATION DATA AND ROM ADDRESS

Phrase specification data	—	I_6	I_5	I_4	I_3	I_2	I_1	I_0	—	—	—
External ROM address	$A_{17} \sim A_{10}$	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Specification Not Valid	0 ~ 0	0	0	0	0	0	0	0	0	0	0
Phrase 1	0 ~ 0	0	0	0	0	0	0	1	0	0	0
Phrase 2	0 ~ 0	0	0	0	0	0	1	0	0	0	0
Phrase 3	0 ~ 0	0	0	0	0	0	1	1	0	0	0
Phrase 127	0 ~	1	1	1	1	1	1	1	0	0	0

* Phrases cannot be specified with all 0s.

The second byte of data specifies the synthesis operation channel as well as channel specific reduction of playback synthesis sound. As to the format of channel specification, please refer to the following chart for channel specification format.

CHANNEL SPECIFICATION

Channel	I_7	I_6	I_5	I_4
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	1	0	0	0

It is impossible to specify multiple channels at the same time. For example, it is impossible to specify channel 1 and channel 3 simultaneously.

REDUCTION SPECIFICATION

All 0 is considered as 0 dB, the analyzed sound itself. The reduction is made through 8 levels from about −3 dB to −24 dB with the steps of about −3 dB. As to the format for reduction, please refer to the following chart.

REDUCTION SPECIFICATION

Reduction rate	I_3	I_2	I_1	I_0
0 dB	0	0	0	0
− 3.2 dB	0	0	0	1
− 6.0 dB	0	0	1	0
− 9.2 dB	0	0	1	1
−12.0 dB	0	1	0	0
−14.5 dB	0	1	0	1
−18.0 dB	0	1	1	0
−20.5 dB	0	1	1	1
−24.0 dB	1	0	0	0

2. Channel Voice Synthesis Suspension

Voice synthesis operation of any channel can be suspended. Its data consists of 1 byte of data. To suspend a channel, make I_7 = 0. And I_3 ~ I_6 represent the channel which should be suspended.

Suspended channel	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
1	0	0	0	0	1	X	X	X
2	0	0	0	1	0	X	X	X
3	0	0	1	0	0	X	X	X
4	0	1	0	0	0	X	X	X

Channel suspension occurs even if multiple channels are specified. For example, if I_3 ~ I_6 are all 1, channels 1 ~ 4 are suspended simultaneously.

3. Data ROM

1. ADDRESS DATA

This specifies start and stop address of ADPCM sound source data. One sound address data consists of 8 bytes. The first 3 bytes show start address while the last 3 bytes show stop address. The other 2 bytes are empty.
By specifying the first address in which the start address is stored, the sound source which should be synthesized is selected.

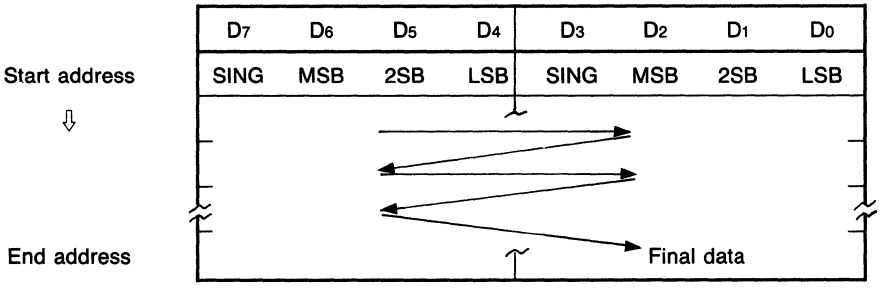
Address 0	SA_1
1	SA_2
2	SA_3
3	EA_1
4	EA_2
5	EA_3
6	EMPTY
7	EMPTY

Start address (SA_1 ~ SA_3) and stop addresses (EA_1 ~ EA_3) are stored according to the chart shown below.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_1, EA_1	0	0	0	0	0	0	A_{17}	A_{16}
SA_2, EA_2	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
SA_3, EA_3	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

2. ADPCM SOUND SOURCE DATA

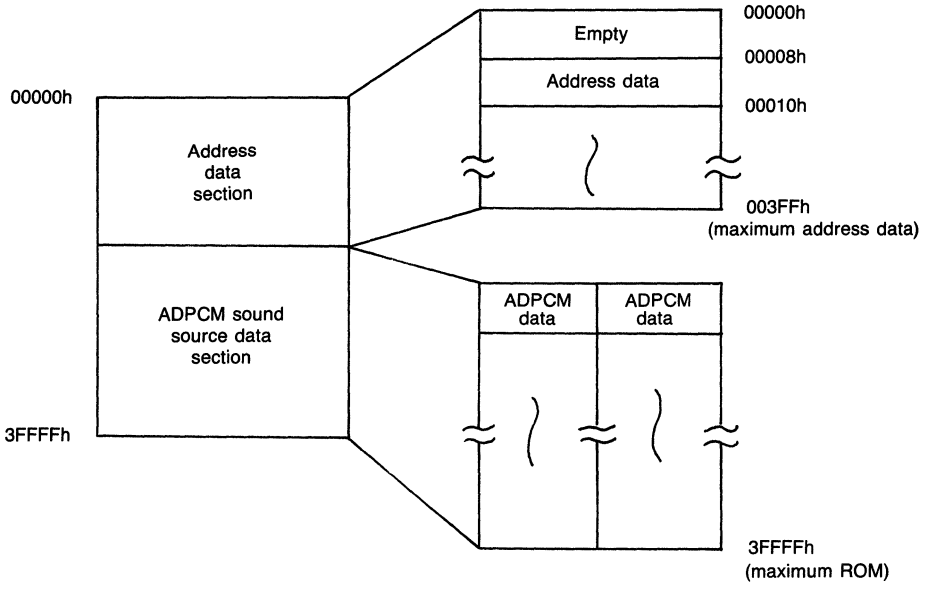
ADPCM sound source data consists of 1 sample for every 4 bits. So, 1 byte stores data of 2 samples. Data arrangement proceeds from higher rank bits (D_4 ~ D_7) to lower rank bits (D_0 ~ D_3). The construction of sound source data should always be ended with lower rank bit. So, construct it with even number of samples.



Sound source data is compatible with the data which is analyzed by MSM5218 or MSM6258. In addition, the data which is analyzed by analyzer is usable, too.

3. STRUCTURE OF SOUND SOURCE DATA ROM

Following chart shows the memory map of the sound source data ROM.



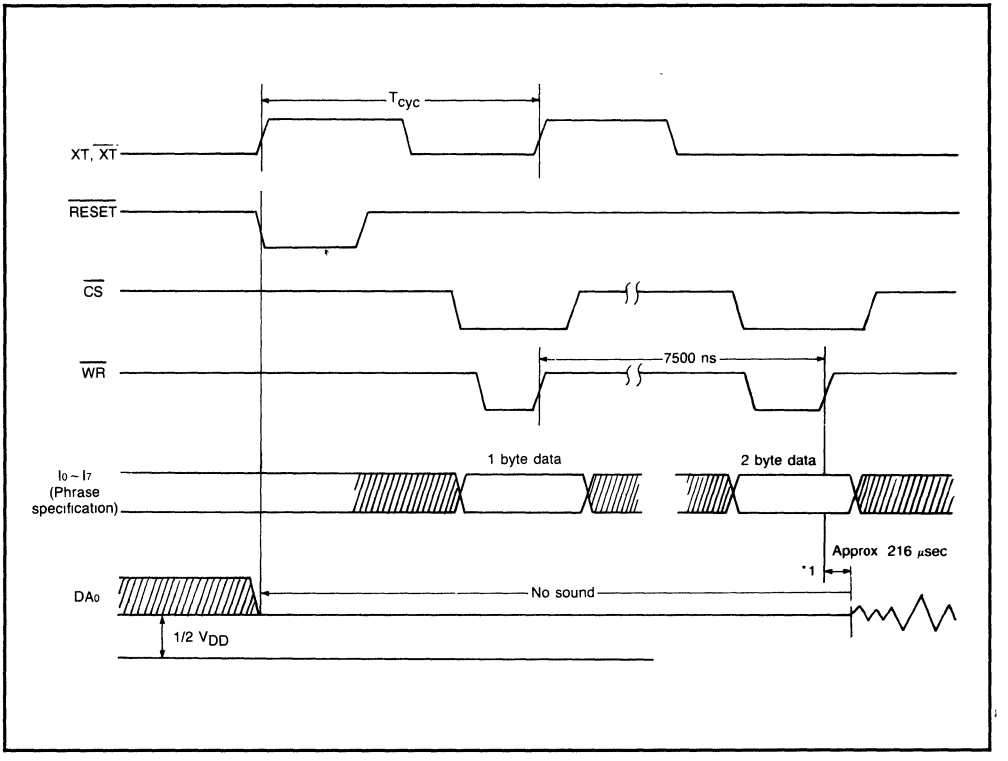
When the maximum 127 phrases are selected in address data section, the data is written up to ROM address 003FFh.
When 1 phrase is selected, address data is written from ROM address 00008h to 0000Fh, and the rest is used as the ADPCM data section.

FUNCTIONAL DESCRIPTION

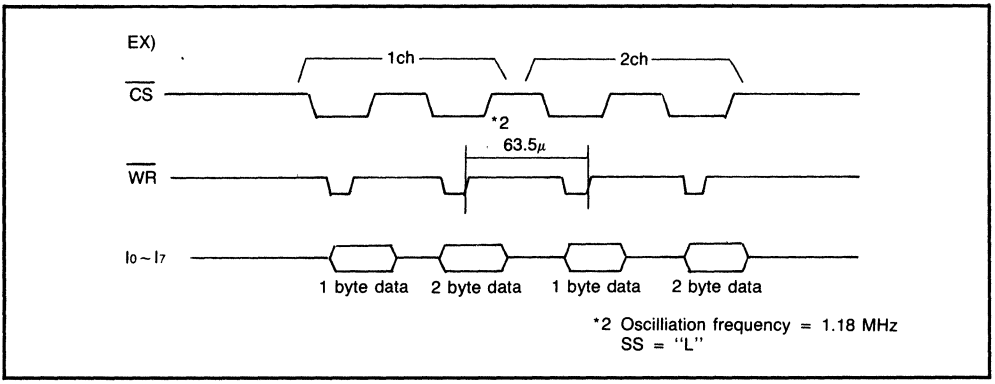
1. Phrase Specifying Input

This procedure is to input phrase specifying data onto the data bus input $I_0 \sim I_7$. The data is latched inside when $\overline{WR}$ goes "L" to "H" while $\overline{CS}$ remains "L".

Voice synthesis operation does not start till the second byte is fully latched.



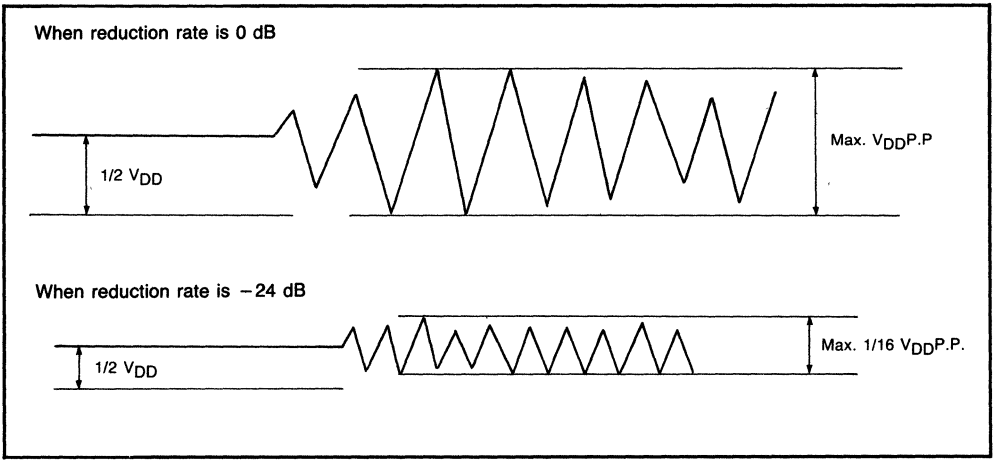
Phrase specifying input is from channel 1 to channel 4 continuously. *1 An interval of 15 Tcyc (max.) is needed between phrases.



Voice synthesis operation can be started from any channel, 1 to 4. The arrangement of each channel is of no concern.

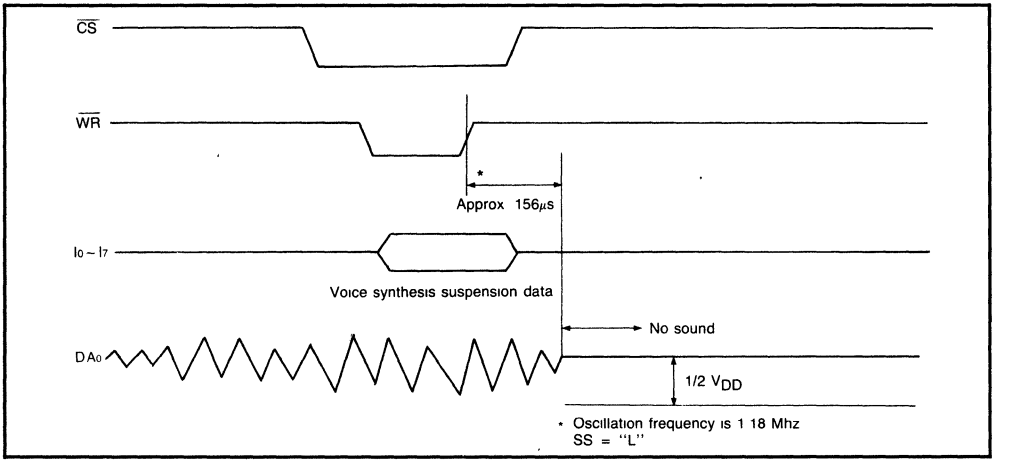
2. Reduction of Synthesized Sound

This procedure is made by the second byte of phrase specifying data. Considering all 0 data of I_0 ~ I_3 as 0 dB, synthesized sound is reduced between approx. −3 dB and −24 dB with the steps of −3 dB.



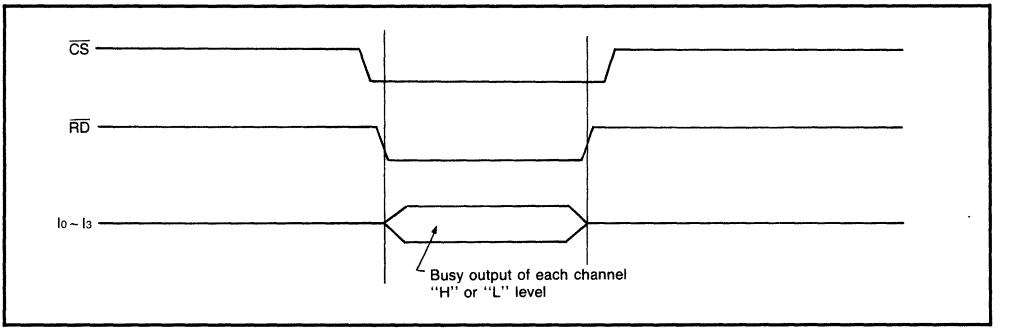
3. Channel Voice Synthesis Suspension

This is accomplished by inputting synthesis suspension data onto data bus input $I_3 \sim I_7$. The data is latched inside when $\overline{WR}$ goes from "L" to "H" while $\overline{CS}$ remains active (L). Since synthesis suspension data is 1 byte data, synthesis operation is suspended right after $\overline{WR}$ is input. Multiple channels can be specified. Therefore it is possible to make suspended channels 1 ~ 4 simultaneously.



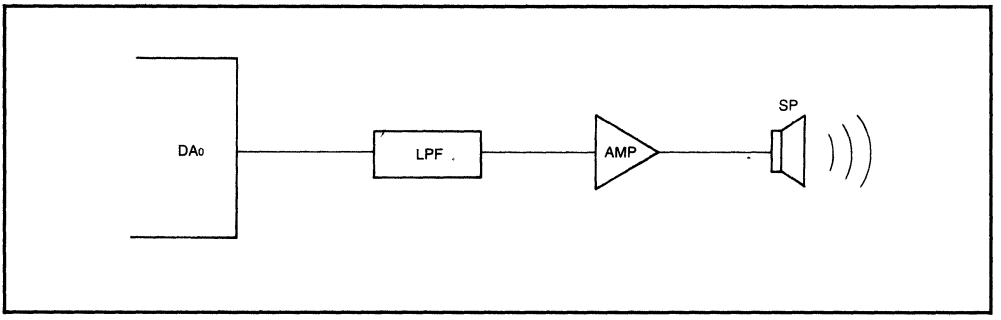
4. Reading-out of Busy State

While $\overline{CS}$ is "L" and $\overline{RD}$ is "L", each operation state, busy state of channels 1 ~ 4 is output on $I_0 \sim I_3$. "H" is output during the operation.



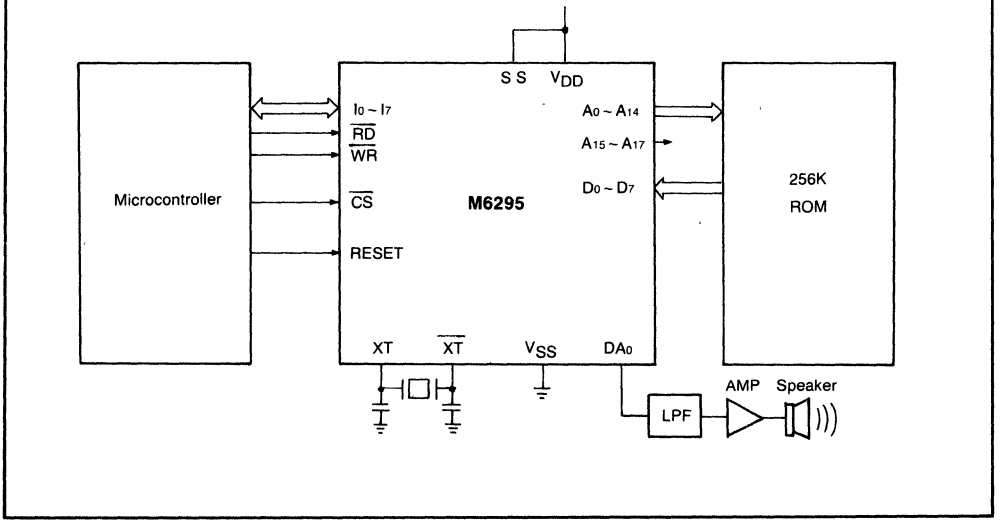
5. Output of Voice Synthesized Sound

MSM6295 has a 12 bit A class (voltage type) DA converter on chip. So, analog signal is available from DA_0 terminal.
DA_0 turns approx. 1/2 V_{DD} (when no sound is output) right after power supply is on. This terminal outputs the amplitude of max. V_{DD}p.p.
To output sound connects LPF and AMP to DA_0 terminal.



APPLICATION CIRCUIT

Interface with Microcontroller



MSM5248

48K BIT ROM ADPCM VOICE SYNTHESIZER

GENERAL DESCRIPTION

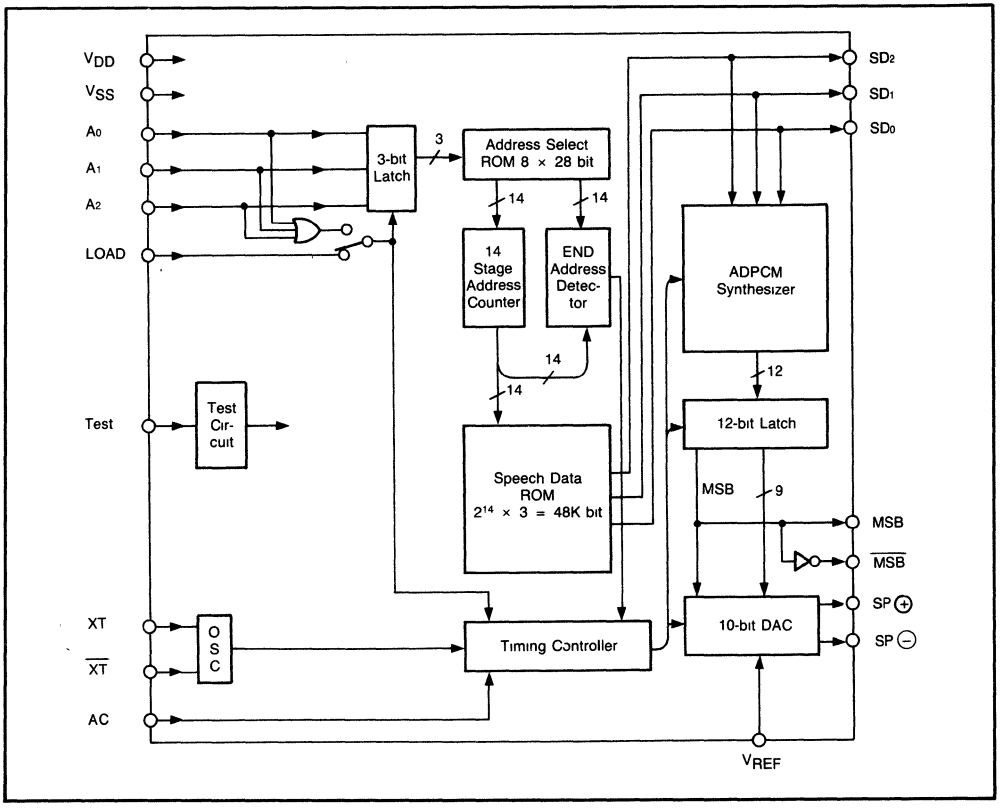
The MSM5248 is an ADPCM voice synthesizer LSI using the CMOS technology process. Its internal circuit consists of the voice synthesis stage, the ROM which stores the speech data, 10-bit D/A converter and the control circuit. It can be used in the variety of systems by connecting with the speaker via the simple interface.

The sampling frequency, etc. can be optionally selected by the user.

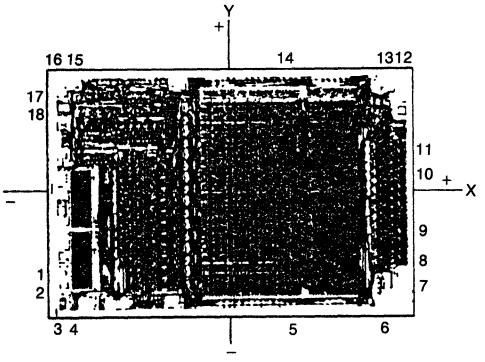
FEATURES

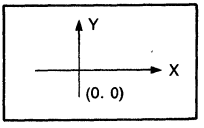
- COMS single chip
- 48K bit ROM for the user's program
- Single power supply: 3 V
- Low power consumption: 0.2 mA (typical)
- Maximum number of words: 7 words
- Maximum length of speech: 3 sec (Sampling frequency: 5.46 kHz)
- Built-in 10-bit D/A converter
- 32.768 kHz crystal oscillation
- Chip form, 18-pin plastic DIP or 24-pin flat package available

BLOCK DIAGRAM



PAD LAYOUT





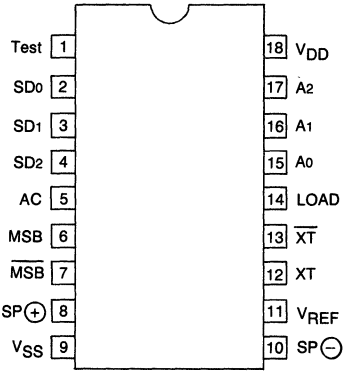
Note: • Chip size: 5.2 mm × 3.48 mm
• Pad size: 110 µm × 110 µm min

PAD LOCATION

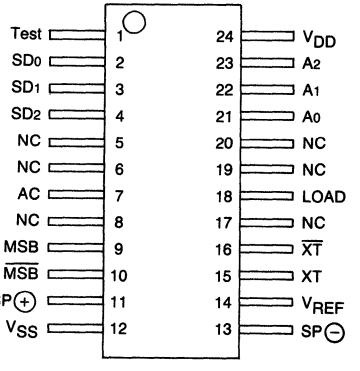
Pad No.	Symbol	Position	
		X	Y
1	TEST	−2445	−1197
2	SD_0	−2445	−1377
3	SD_1	−2445	−1585
4	SD_2	−2265	−1585
5	AC	893	−1585
6	MSB	2143	−1585
7	$\overline{MSB}$	2445	−1289
8	SP ⊕	2445	−987
9	V_{SS}	2445	−511
10	SP ⊖	2445	221
11	V_{REF}	2445	567
12	XT	2445	1585
13	$\overline{XT}$	2265	1585
14	LOAD	789	1585
15	A_0	−2265	1585
16	A_1	−2445	1585
17	A_2	−2445	1317
18	V_{DD}	−2445	1137

PIN CONFIGURATION

(Top View) 18 Lead Plastic DIP



(Top View) 24 Lead Plastic Flat Package



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings **Table 1** (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Limit	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +3.6	V
Input Voltage	V_I		−0.3 to V_{DD}	V
Power Dissipation	P_D		200 max	mW
Storage Temperature	Tstg	—	−55 to +150	°C

Operating Range **Table 2**

Parameter	Symbol	Conditions	Limit	Unit
Supply Voltage	V_{DD}	—	+2.4 to +3.6	V
Operating Temperature	Top	—	−10 to +60	°C
External Reference Resistor	R_{REF}	Applicable for V_{REF}	Min 100	kΩ

DC Characteristics **Table 3** (V_{DD} = 3.1 V, V_{SS} = 0 V, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
"H" Input Voltage	V_{IH}	—	2.5	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Input Voltage *1	I_{IH}	V_{IH} = 3.1 V	—	—	1	µA
"L" Input Voltage	I_{IL}	V_{IL} = 0 V	—	—	−1	µA
"H" Input Voltage *2	I_{IH1}	V_{IH1} = 3.1 V	7	—	200	µA
"H" Output Voltage *3	I_{OH}	V_{OH} = 2.5 V	−0.1	—	—	mA
"L" Output Voltage *3	I_{OL}	V_{OL} = 0.5 V	0.1	—	—	mA
Power Consumption (1)	I_{DD1}	Active	—	0.2	1.0	mA
Power Consumption (2)	I_{DD2}	Standby (no oscillation)	—	—	1	µA
Power Consumption (3)	I_{DD3}	Standby (oscillation)	—	10	20	µA
DA Synk Current *4	I_{SYNK}	Note 1	260	400	600	µA
DA Accuracy *4	I_E	Note 2	0.75 × 1	1	1.25 × 1	µA

Notes: *1 Applicable for A_0, A_1, A_2, when pull down resistor is not provided.
*2 Applicable for LOAD, AC and A_0, A_1 and A_2 when pull down resistor is applied.
*3 Applicable for MSB, MSB.
*4 Applicable for SP ⊕, SP ⊖.

Table 4
(Value of resistor V_{REF} is 2 MΩ)

MSB									LSB	Pin
0	1	1	1	1	1	1	1	1	1	SP ⊕
1	0	0	0	0	0	0	0	0	0	SP ⊖

Note 1: Lower 2 bit in output of 12 bit latch is disregarded, and data with 10 bit is input to D/A converter.
The characteristics indicates the value of the pin SP ⊕ and SP ⊖ when the value as shown below is input to D/A converter.

Table 5

Actual Measurement Value	Input Data to 10-bit D/A Converter										
I_1 =	MSB									LSB	Pin
	0	0	0	0	0	0	1	0	0	0	SP ⊕
I_0 =	MSB									LSB	Pin
	0	0	0	0	0	0	0	1	0	0	SP ⊖

Note 2: $0.75 \times 2I_0 < I_1 < 1.25 \times 2I_0$
This Formula is applied on following condition.

AC Characteristics
(V_{DD} = +2.4 to +3.6 V, Ta = −10 to +60°C)

Table 6
(Timing Chart)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Oscillator Frequency	f_{OSC}	—	32	32.768	35	kHz
AC Input Pulse Width	t_{ACW}	—	10	—	—	μs
Load Input Pulse Width	t_{LW}	—	65	—	—	μs
D/A Output Delay Time	t_{LO}	$f_{(OSC)}$ = 32.768 kHz	—	—	305	μs
Full-address Zero Interval	t_{OW}		2	—	—	μs

PIN DESCRIPTION

Pin Name	Terminal Number			I/O
	CHIP	18 DIP	24 FLT	
A_0	15	15	21	I
A_1	16	16	22	
A_2	17	17	23	I

Address selection input
Maximum 7 words or 3 words are determined according to A_0, A_1, and A_2 H/L combinations ~, except that $A_0 = A_1 = A_2$ = "L" is prohibited for users because of the test code for LSI.

LSI operation starting method is selected by masking option, too.
① One method is to apply appointed pulse to either A_0, A_1 or A_2.
② The other method is to apply load pulse to LOAD pin after determining A_0, A_1 or A_2.

When the voice starting method ① is selected, repeated operation or one time operation is selected by masking option. (See timing chart)

Existence of pull-down resistor of A_0, A_1 and A_2 is selected by masking option.

Starting method of IC with A_0 to A_2 pins.

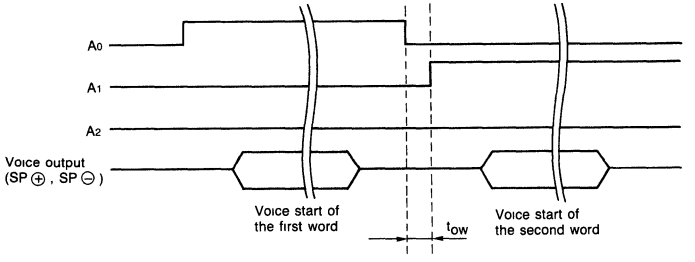


Figure 1

IC is activated by setting only one of A_1 to A_2 pins in "H" level. When switching to the voice start of another word, be sure to set full-address "L" interval (t_{ow}). The maximum number of words in three in case this starting method is selected.

LOAD	14	14	18	I

Pulse input pin for LSI starting
LOAD pin is a pulse input pin for voice start. Load pin is pulled down inside.

- When the voice is started by either A_0, A_1 or A_2, LOAD pin should be used as open.
- Either repeated operation or one time operation is selected by masking option. (See timing chart)

PIN DESCRIPTION (Continued)

Pin Name	Terminal Number			I/O
	CHIP	18 DIP	24 FLT	
XT	12	12	15	I
$\overline{XT}$	13	13	16	I

Pins for crystal
Either external clock input or crystal oscillation can be selected by masking option.

- External clock input

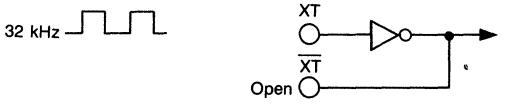


Figure 2

- Crystal oscillation

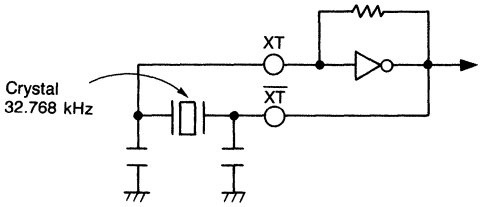


Figure 3

AC	5	5	7	I

All clear input pin
All functions of LSI are stopped by input of "H" level voltage to AC pin, and status of LSI turns to stand-by. AC pin is pulled down inside.
The built-in P.O.R. (Power on reset) function is designated by masking option.

V_{REF}	11	11	14	I

This pin is an input pin for the constant-current control of low impedance D/A converter.
The volume of speaker can be controlled by external resistor (variable) whose value is more than 100 kΩ.

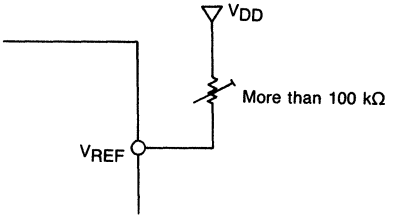


Figure 4

PIN DESCRIPTION (Continued)

Pin Name	Terminal Number			I/O
	CHIP	18 DIP	24 FLT	
SP ⊕	8	8	11	O
SP ⊖	10	10	13	

These are output pins for 10-bit D/A converter (low impedance type). When LSI is at standby, SP ⊕ and SP ⊖ turn to high impedance.

MSB	6	6	9	O
$\overline{\text{MSB}}$	7	7	10	O

These are output pins for the most significatiant bit signal and the inverted signal.

TEST	1	1	1	I
SD_0	2	2	2	O
SD_1	3	3	3	O
SD_2	4	4	4	O

As test pin is pulled down, this pin should open.
SD_0, SD_1, SD_2 are 3-bit ADPCM data output pins, these pins should be open.

V_{SS}	9	9	12	I

This is a ground input pin.

V_{DD}	18	18	24	I

This is a supply voltage input pin.

TIMING CHART

REPEATED OPERATION

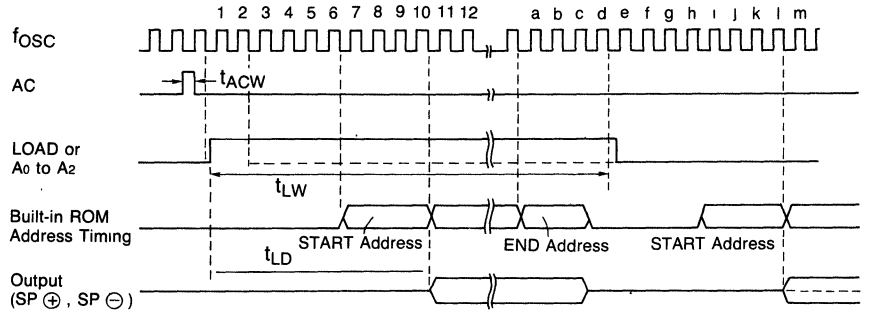


Figure 5

ONE TIME OPERATION

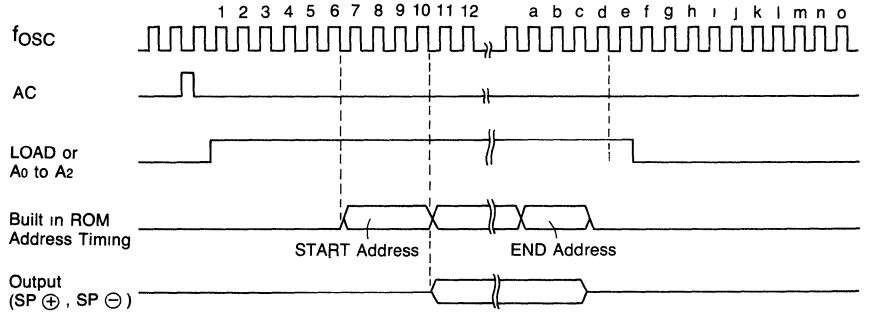


Figure 6

TYPICAL APPLICATION CIRCUIT

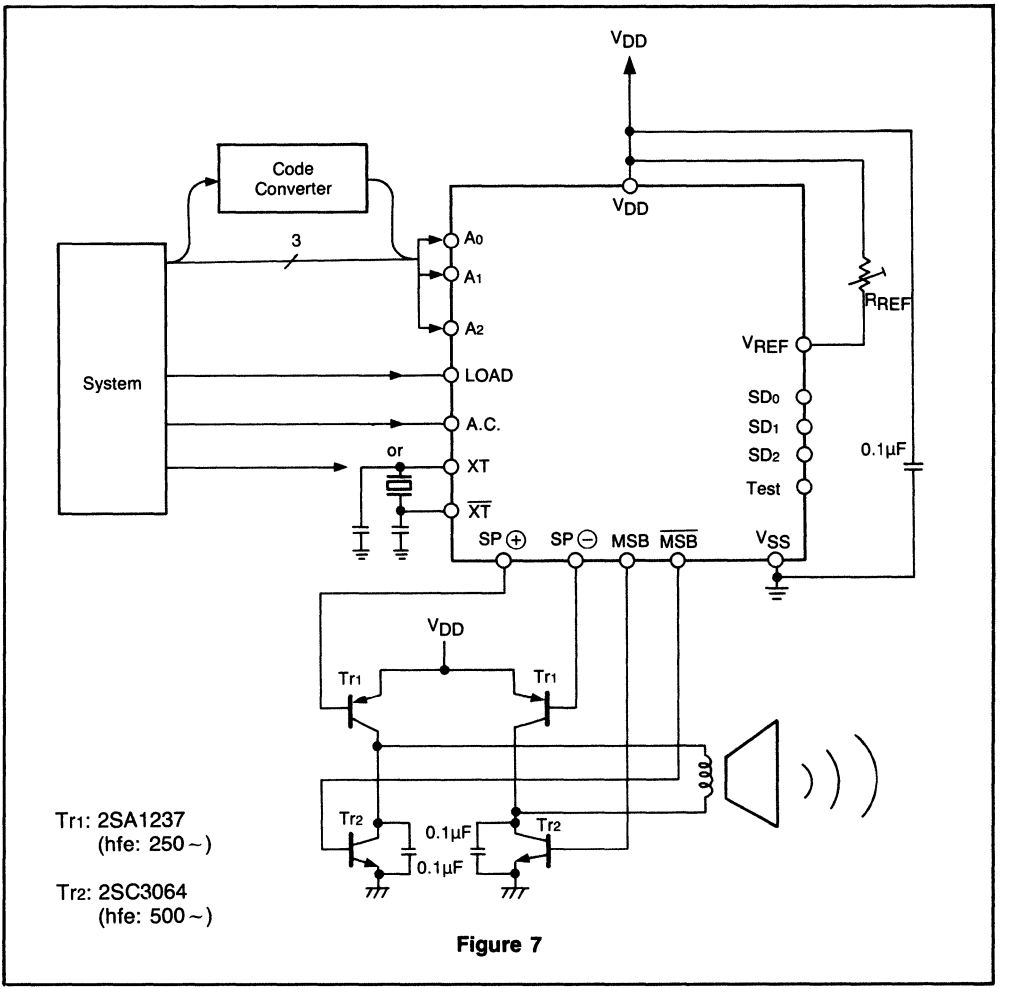


Figure 7

Combination in MSM5248 and MSM5041 (Melody chip)
This circuit is applied to Voice & Melody card and Toy, etc.

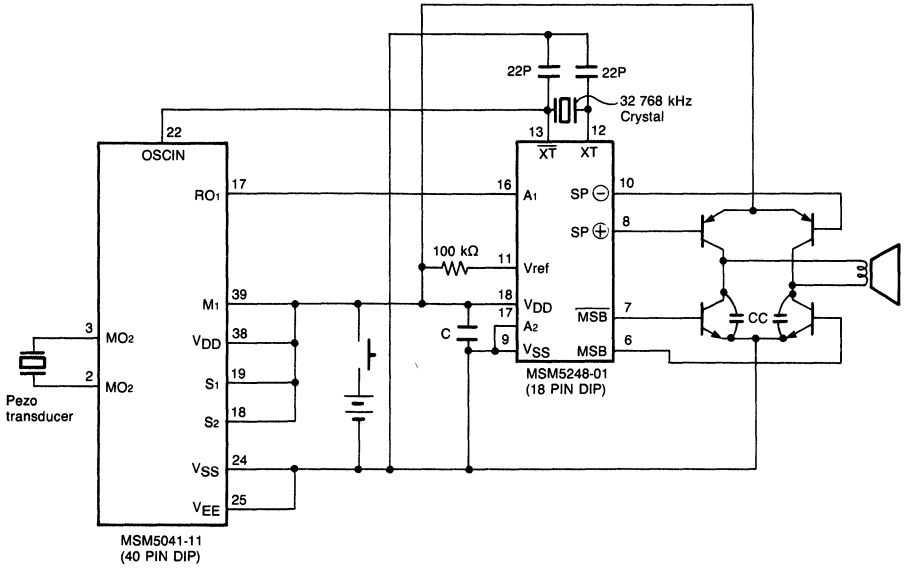


Figure 8

OPTION LIST

Table 7

No.	Items	Selection		
1	Package	Chip	18p DIP	24p FLAT
2	Sampling frequency	8.19 kHz	5.46 kHz	
OP-1	Pull-down for A_0	Yes	No	
OP-2	Pull-down for A_1	Yes	No	
OP-3	Pull-down for A_2	Yes	No	
OP-7	Anti-chattering when A_0—A_2 of starting method is selected.	Yes	No	
OP-9	Oscillation	X'tal	External clock	
OP-10, 11	Starting method of LSI	A_0—A_2	LOAD	
OP-12	One time or repeatable	One time	Repeatable	
OP-14	Power on reset	Yes	No	

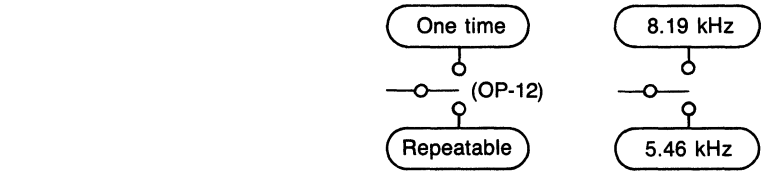


Figure 9

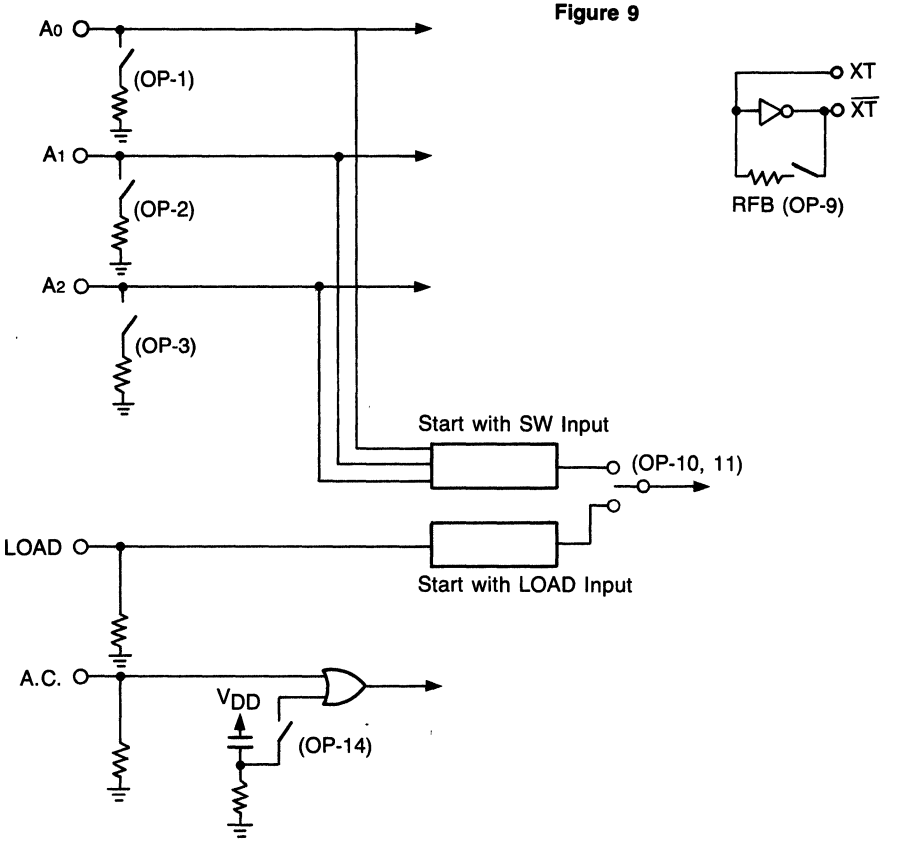


Figure 10

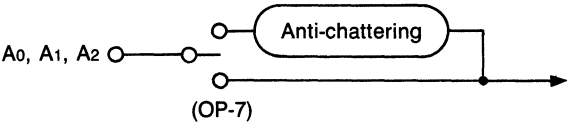


Figure 11

STANDARD VERSION LIST

Type No.	Contents	Selection		
		A_0	A_1	A_2
MSM5248-01	"Happy Birthday"	L	H	L
MSM5248-04	Fanfare Sound	H	L	L
MSM5248-05	"Merry Christmas & a Happy New Year"	H	L	L
	"Merry Christmas"	L	H	L

OPTION LIST OF STANDARD VERSION

MSM5248-01

No.	Items	Selection		
1	Package	Chip	18p DIP	24p FLAT
2	Sampling frequency	8.19 kHz		
OP-1	Pull-down for A_0	Yes		
OP-2	Pull-down for A_1	No		
OP-3	Pull-down for A_2	No		
OP-7	Anti-chattering when A_0—A_2 of starting method is selected.	Yes		
OP-9	Oscillation	X'tal		
OP-10, 11	Starting method of LSI	A_0—A_2		
OP-12	One time or repeatable	One time		
OP-14	Power on reset	Yes		

MSM5248-04

No.	Items	Selection		
1	Package	Chip	18p DIP	24p FLAT
2	Sampling frequency	8.19 kHz		
OP-1	Pull-down for A_0	No		
OP-2	Pull-down for A_1	Yes		
OP-3	Pull-down for A_2	Yes		
OP-7	Anti-chattering when A_0—A_2 of starting method is selected.	Yes		
OP-9	Oscillation	X'tal		
OP-10, 11	Starting method of LSI	LOAD		
OP-12	One time or repeatable	Repeatable		
OP-14	Power on reset	Yes		

MSM5248-05

No.	Items	Selection		
1	package	Chip	18p DIP	24p FLAT
2	Sampling frequency	8.19 kHz		
OP-1	Pull-down for A_0	No		
OP-2	Pull-down for A_1	No		
OP-3	Pull-down for A_2	Yes		
OP-7	Anti-chattering when A_0—A_2 of starting method is selected.	Yes		
OP-9	Oscillation	X'tal		
OP-10, 11	Starting method of LSI	A_0—A_2		
OP-12	One time or repeatable	One time		
OP-14	Power on reset	Yes		

MSM6243

SPEECH SYNTHESIS LSI WITH 192 KBIT ROM

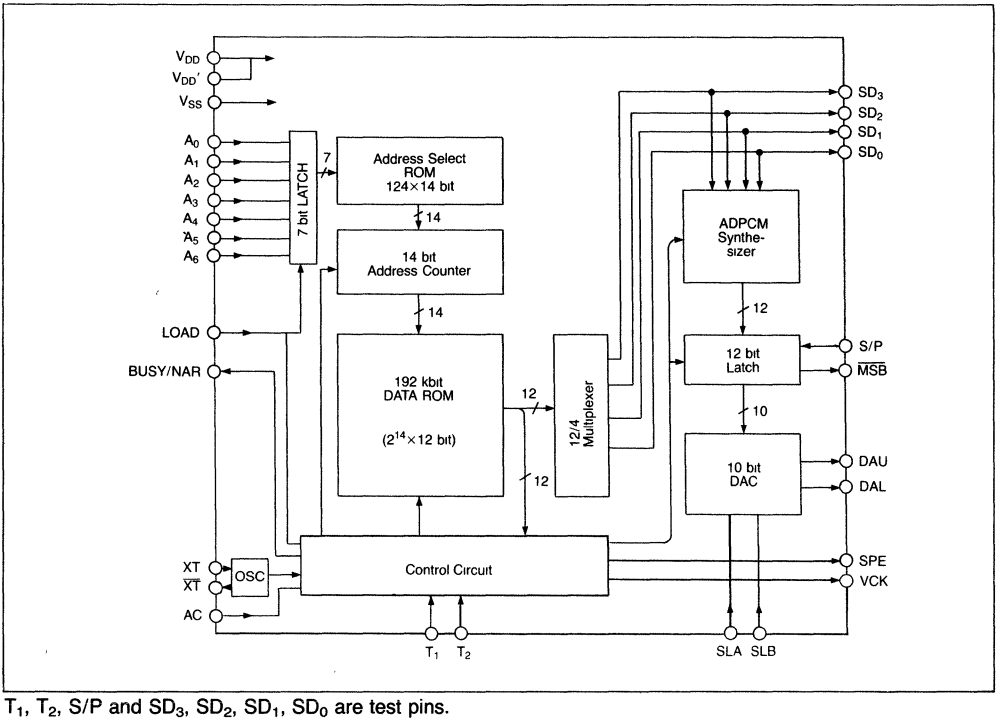
GENERAL DESCRIPTION

The Oki MSM6243 is a single-chip, CMOS, speech synthesis LSI for ADPCM systems. It contains 192k bits of speech data ROM storage. This IC has an input interface, a timing generation circuit, and a 10 bit DA converter. Therefore, voice output systems may be constructed easily by connecting the voice output circuit consisting of a simple input circuit, filter, amplifier, and speaker to the chip.

FEATURES

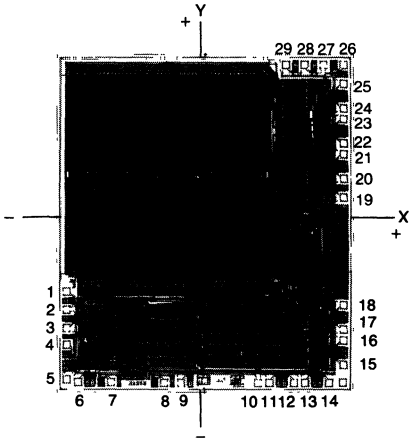
- CMOS single chip
- Low power consumption
- Custom ROM
- Selection of supply voltage: 3V system or 5V system.
- ADPCM bit length: 4 bits
- Maximum word number: 124 words
- Maximum speaking time: 20 seconds (compressed ADPCM)
- Selection of class A or class B analogue output is possible.
- Built-in 10 bit DA converter
- Oscillator frequency: 30 to 132 kHz (5V system).
- Chip, 40 pins plastic DIP, 44 pins or 60 pins plastic flat package. 2 types of plastic flat package are provided depending on terminal pin bending or not bending.
  - Terminal pin not bending
    - MSM6243-XXGS
  - Terminal pin bending
    - MSM6243-XXGS-K
  - When placing an order, specify the type.
- Word selection through an internal random number circuit is possible (maximum 32 words).

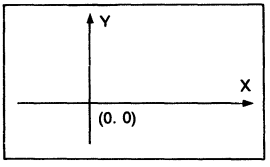
BLOCK DIAGRAM



T_1, T_2, S/P and SD_3, SD_2, SD_1, SD_0 are test pins.

PAD LAYOUT





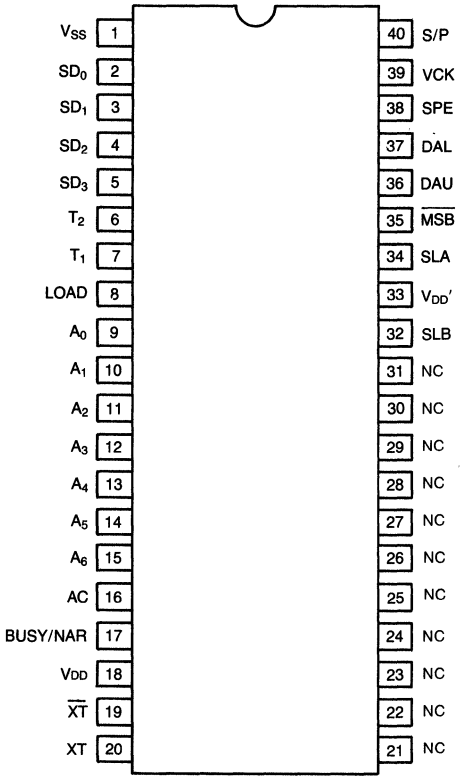
Note: • Chip size: 4.91 mm × 5.57 mm
• Chip thickness: 350 ± 30 μm

PAD LOCATION

Pad No.	Symbol	Position	
		X	Y
1	SLB	−2300	−1125
2	V_{DD}'	−2300	−1425
3	SLA	−2300	−1725
4	$\overline{MSB}$	−2300	−2000
5	DAU	−2300	−2570
6	DAL	−2110	−2615
7	SPE	−1560	−2615
8	VCK	−675	−2625
9	S/P	−395	−2625
10	V_{SS}	885	−2625
11	SD_0	1075	−2625
12	SD_1	1480	−2625
13	SD_2	1660	−2625
14	SD_3	2060	−2625
15	T_2	2295	−2325
16	T_1	2295	−1925
17	LOAD	2295	−1745
18	A_0	2295	−1345
19	A_1	2295	440
20	A_2	2295	745
21	A_3	2295	1145
22	A_4	2295	1325
23	A_5	2295	1730
24	A_6	2295	1910
25	AC	2295	2310
26	BUSY/NAR	2295	2625
27	V_{DD}	1965	2625
28	$\overline{XT}$	1650	2625
29	XT	1345	2625

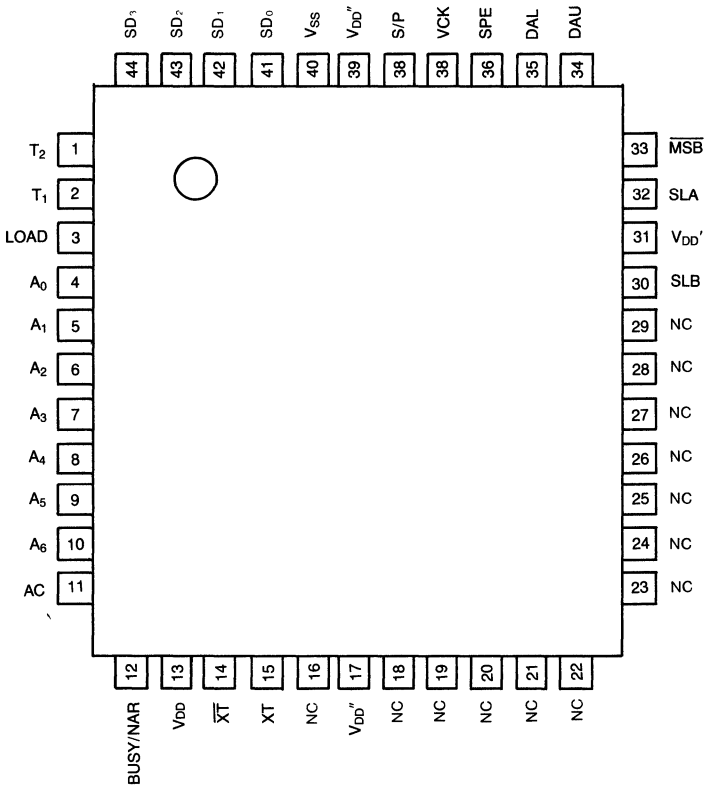
PIN CONFIGURATION

(Top View) 40 Lead Plastic DIP



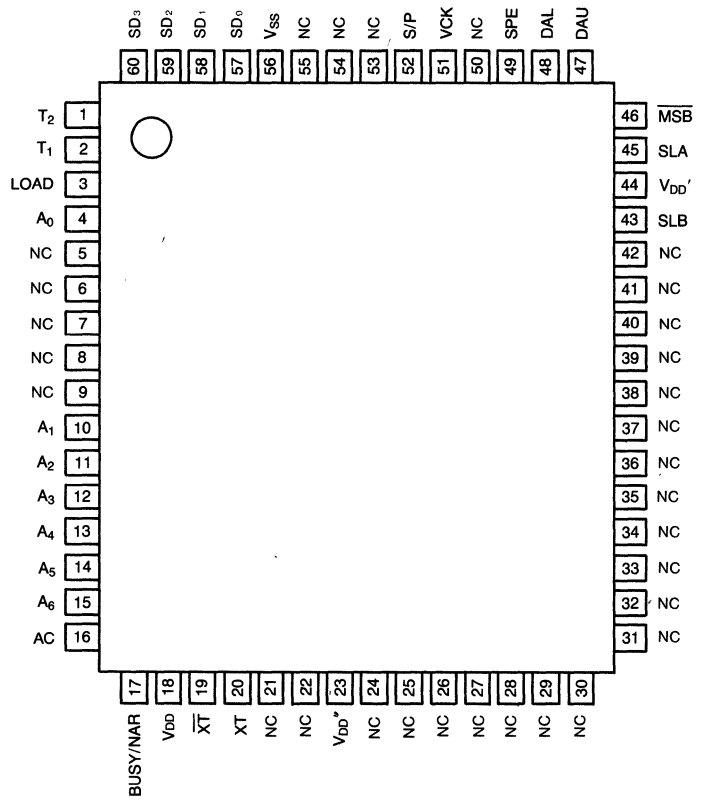
Note: This pinout applies to the MSM6243-XXRS.

(Top View) 44 Lead Plastic Flat Package



Note 1. This pinout applies to the MSM6243-XXGS and -XXGS-K.
Note 2. Since 17 and 39 pin (V_{DD}'') is substrate continuity, short-circuits with V_{DD} and V_{DD}' in the outside.

(Top View) 60 Load Plastic Flat Package



Note 1. This pinout applies to the MSM6243-XXGS and -XXGS-K.
Note 2. Connect pin 23 (V_{DD}'') with V_{DD} and V_{DD}' externally. This pin is conducted to the substrate.

ELECTRICAL CHARACTERISTICS

3V System (V_{DD} = 3.1V TYP)

- **Absolute maximum rating**

(V_{SS} = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ +5.0	V
Input Voltage	V_I		−0.3 ~ V_{DD}	V
Storage Temperature	T_{stg}	—	−55 ~ +150	°C

- **Operating range**

(V_{SS} = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}	—	+2.4 ~ 3.6	V
Operating Temperature	T_{op}	—	−10 ~ +60	°C
DAU, DAL Output Level	V_{DD}	No-load	0 ~ V_{DD}	V

- **DC characteristics**

(V_{DD} = 3.1V, V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	2.6	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Input Current*1	I_{IH1}	V_{IH} = 3.1V	—	0.01	0.5	μA
"H" Input Current*2	I_{IH2}	V_{IH} = 3.1V	10	—	150	μA
"L" Input Current	I_{IL}	V_{IL} = 0V	—	−0.01	−0.5	μA
"H" Output Current	I_{OH}	V_{OH} = 2.7V	−200	—	—	μA
"L" Output Current	I_{OL}	V_{OL} = 0.4V	200	—	—	μA
Operating Power Consumption	I_{DD1}	—	—	0.1	0.5	mA
Standby Power Consumption	I_{DD2}	Class B output selection and oscillation stop.	—	0.01	0.5	μA
Power Consumption*3 in the case of oscillation	I_{DD3}	Standby and class B output selection.	—	4	30	μA
DA Output Precision	$\lvert V_E \rvert$	No-load and class A output selection.	—	—	100	mV
DA Output Impedance	V_{OR}	—	—	50	—	kΩ

Notes:

*1. This applies to the AC, LOAD and A_0 to A_6 pins.

*2. This applies to the input pin except AC, LOAD and A_0 to A_6 pins.
For SLA, and SLB pins, this applies in the case of AC input "H". (In the case of AC input "L", this conforms to Note 1.)

*3. This applies when R_{FB} exists and f_{OSC} = 32.768 kHz.

5V System (V_{DD} = 5.0V TYP)

- **Absolute maximum rating** (V_{SS} = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ +7.0	V
Input Voltage	V_I		−0.3 ~ V_{DD}	V
Storage Temperature	T_{stg}	—	−55 ~ +150	°C

- **Operating range** (V_{SS} = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}	—	+4.5 ~ +5.5	V
Operating Temperature	T_{OP}	—	−30 ~ +70	°C
DAU, DAL Output Level	V_{OD}	No-load	0 ~ V_{DD}	V

- **DC characteristics** (V_{DD} = 3.1V, V_{SS} = 0V, Ta = −30~+70°)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Input Current*1	I_{IH1}	V_{IH} = 5.0V	—	—	1	μA
"H" Input Current*2	I_{IH2}	V_{IH} = 5.0V	20	—	400	μA
"L" Input Current	I_{IL}	V_{IL} = 0V	—	—	−1	μA
"H" Output Current	I_{OH}	V_{OH} = 4.6V	−1	—	—	mA
"L" Output Current	I_{OL}	V_{OL} = 0.4V	1	—	—	mA
Operating Power Consumption	I_{DD1}	—		0.2	0.7	mA
Standby Power Consumption	I_{DD2}	Class B output selection and oscillation stop.	—	0.01	10	μA
Power Consumption*3 in the case of oscillation	I_{DD3}	Standby and class B output selection.	—	15	100	μA
DA Output Precision	$\|V_E\|$	No-load and class A output selection	—	—	130	mV
DA Output Impedance	V_{OR}	—	—	60	—	kΩ

Notes:

*1. This applies to the AC, LOAD and A_0 to A_6 pins.

*2. This applies to the input pin except AC, LOAD and A_0 to A_6 pins.
For the pins of SLA and SLB, this applies in the case of AC input "H". (In the case of AC input "L", this conforms to Note 1.)

*3. This applies when R_{FB} exists and f_{OSC} = 32.768 kHz.

AC CHARACTERISTICS

(V_{DD} = +2.4 to +5.5V are common for 3V system and 5V systems.
Ta = −30 to +70°C, f_{osc} = 32.768 kHz.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillator frequency (1)	f_{OSC1}	3V system	30	32.768	35	kHz
Oscillator frequency (2)	f_{OSC2}	5V system	30	32.768	120	kHz
Oscillator duty-cycle	f_{duty}	—	40	50	60	%
LOAD input*1 pulse width	t_L	In the case of f_{sample} = 8.19 kHz and CPU interface	1	—	40	μS
AC input pulse width	$t_{W(AC)}$	—	1	—	—	μS
Sampling frequency (1)	f_{S1}	$f_{OSC}/4$	—	8.192	—	kHz
Sampling frequency (2)	f_{S2}	$f_{OSC}/5$	—	6.554	—	kHz
Sampling frequency (3)	f_{S3}	$f_{OSC}/8$	—	4.096	—	kHz
NAR minimum "H" level width	t_{MN}	In the case of f_{S1} selection	1	—	—	μS
Hold time for LOAD	t_H	In the case of f_{S1} selection	1	—	—	μS

*1. $t_{L(MAX)}$ in the case of SW input interface is equal to the speaking time of a specified word.

PIN DESCRIPTION

Pin Name	Terminal Number				I/O
	CHIP	40 DIP	44 FLT	60 FLT	
AC	25	16	11	16	I

All clear
LSI comes to standby state by "H" input, and SLA and SLB pins are pulled down to "L" level. Since this pin is started by LOAD input, pulse input can be used.
In this LSI, since power on clear circuit is not built-in, apply AC pulse when power is turned on.

A_0	18	9	4	5	I
A_1	19	10	5	10	I
A_2	20	11	6	11	I
A_3	21	12	7	12	I
A_4	22	13	8	13	I
A_5	23	14	9	14	I
A_6	24	15	10	15	I

Address
These pins are used to specify the speaking word code.
Speaking word code is latched into inside by the LOAD pulse rise.

LOAD	17	8	3	3	I

Speaking word code is latched into inside by the LOAD pulse rise.
When the system is reset by previously applied AC signal, the system reset is cancelled in the case of LOAD pulse rise, and LSI is started. And when NAR output mentioned later is in the "H" level, LOAD signal comes to effective.

BUSY/NAR	26	17	12	17	O

Next address request
BUSY/NAR can be switched in an LSI, and an either of them may be specified on the occasion of order. In the case of NAR use, LOAD input comes to effective with "H" level, and in the case of BUSY use, LOAD input comes to effective with "L" level.

XT	29	20	15	20	I

Crystal
This is crystal input pin for internal clock oscillation.
This also becomes input pin when an external clock is used.

$\overline{XT}$	28	19	14	19	I

This is crystal input pin for internal clock oscillation.

DAU	5	36	34	47	O
DAL	6	37	35	48	O

DA upper, DA lower
The output of 10 bits DA converter is connected to these pins directly. Since output impedance of these pins are great and LPF is not built in, connect the LPF through a low impedance output buffer outside.
In the selection of class A mode, output pin is only DAU.

PIN DESCRIPTION (Continued)

Pin Name	Terminal Number				I/O
	CHIP	40 DIP	44 FLT	60 FLT	
SLA	3	34	32	45	I
SLB	1	32	30	43	I

Selecter A, selecter B
Switchover of DA converter output condition to class A mode or class B mode.

SLA	SLB	Mode	Output Pin
Open (L)	Open (L)	Class B × 2	DAU, DAL
V_{DD} (H)	Open (L)	Class B × 1	Same as above
Open (L)	V_{DD} (H)	Class B × 4	Same as above
V_{DD} (H)	V_{DD} (H)	Class A	DAU

$\overline{MSB}$	4	35	33	46	I/O

In the case of class B mode, this pin becomes as follows:
- In the case of MSB = "L" output, DAU output is effective.
- In the case of MSB = "H" output, DAL output is effective.

In the case of class A mode, this pin becomes as follows:
- In the case of MSB = "L" output, DAU output value is $V_{DD}/2$ or more.
- In the case of MSB = "H" output, DAU output value becomes $V_{DD}/2$ or less.

In the case of internal circuit test, this pin is used as input pin.

SPE	7	38	36	49	I/O

Speaker enable
In the case of "H" level output, DA output is effective. In the case of internal circuit test, this pin is used as input pin.

VCK	8	39	38	51	O

Voice clock
Sampling frequency is output through this pin.

SD_0	11	2	41	57	I/O
SD_1	12	3	42	58	I/O
SD_2	13	4	43	59	I/O
SD_3	14	5	44	60	I/O

These pins are used for internal circuit test. These pins carry out I/O of 4 bits ADPCM data. Usually, set them to open.

S/P	9	40	38	52	I

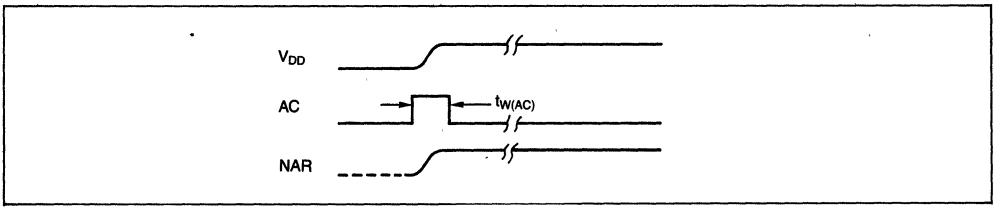
Serial/parallel
These pins are used for internal circuit test. Usually, set them to GND level.

T_1	16	7	2	2	I
T_2	15	6	1	1	

Test
These pins are used for internal circuit test. Usually, set them to GND level

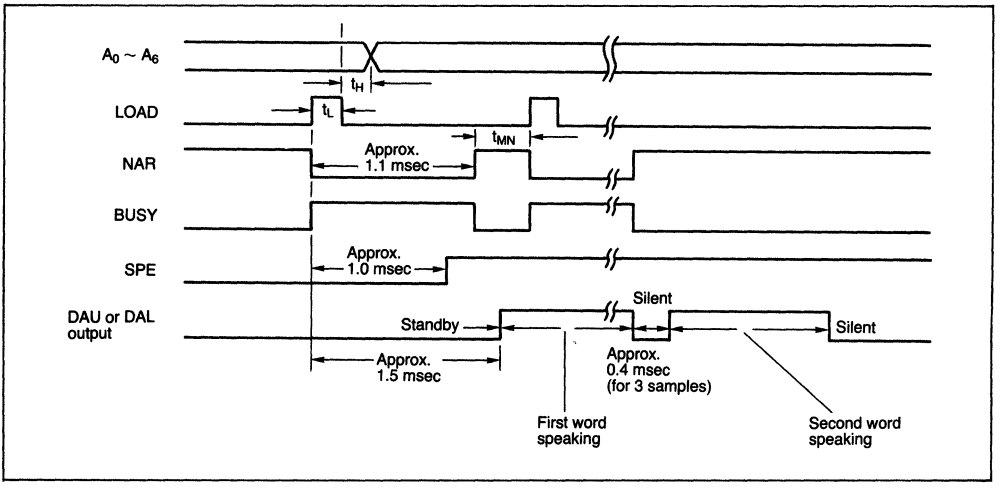
TIMING CHART

Power On

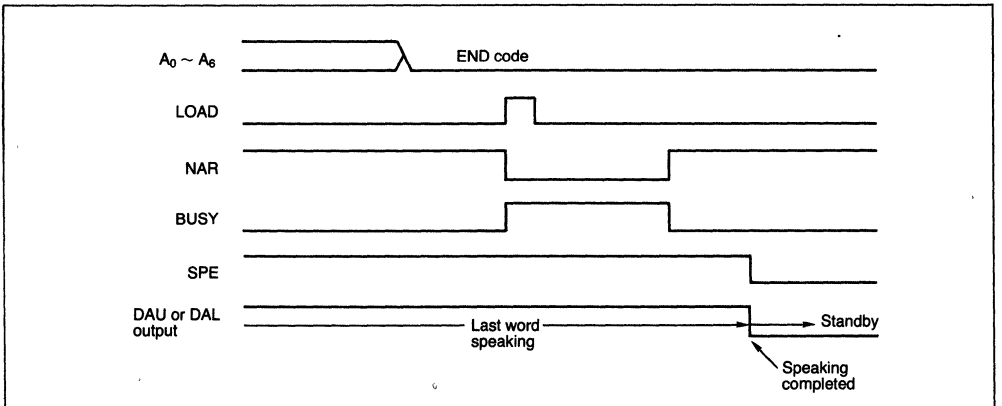


LSI Start and No Operation (Standby)

1. Start in the case of CPU interface



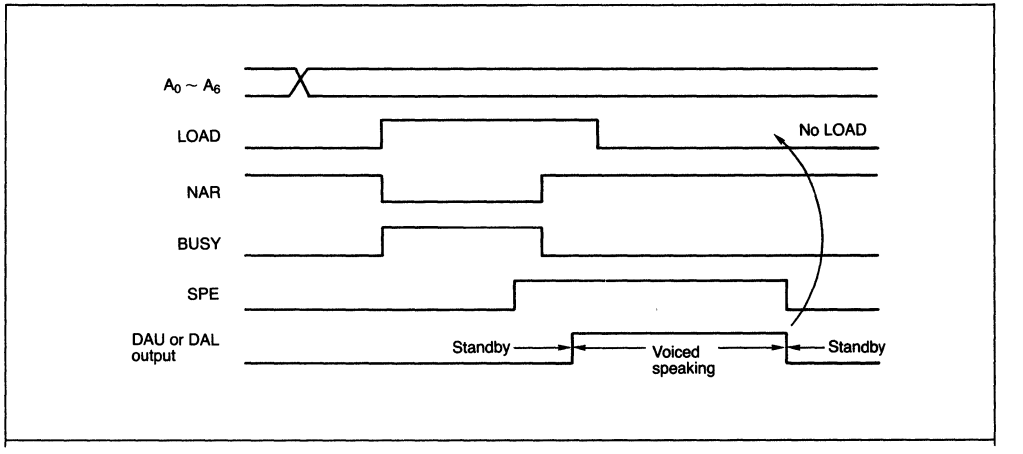
2. Transfer to standby in the case of CPU interface



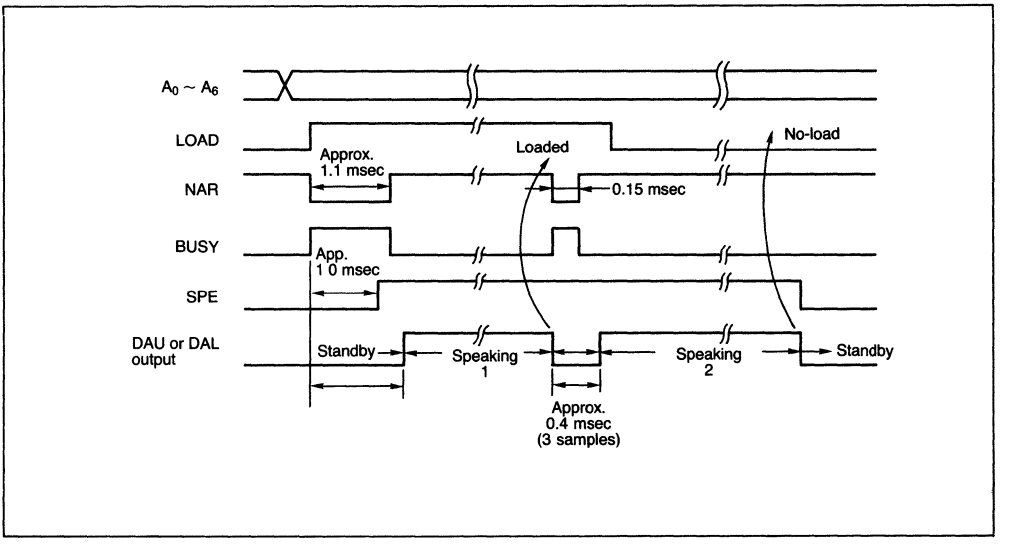
When END code (A_0 to A_6 = "L") is accompanied with LOAD, LSI comes to the same state as standby because of AC input.

Start of SW input interface and standby

1. Single word speaking



2. Repetition of word speaking



FUNCTIONAL DESCRIPTION

Speaking Word Code Specification
User can specify word codes set by $A_0 \sim A_6$ and can select either CPU interface or SW input interface.

1. CPU interface
In this case, user specified words are maximum 124 words. For A_0 to A_6, the following 3 codes, "1111111", "0111111", "1011111", are test codes, and the code "0000000" is an END code, therefore, these 4 codes can not be used.

The procedure up to the LSI operation start is as follows:
Input A_0 to A_6 → LOAD pulse apply → latched inside, also LSI operation starts simultaneously.

LOAD pulse is effective when NAR output is "H".

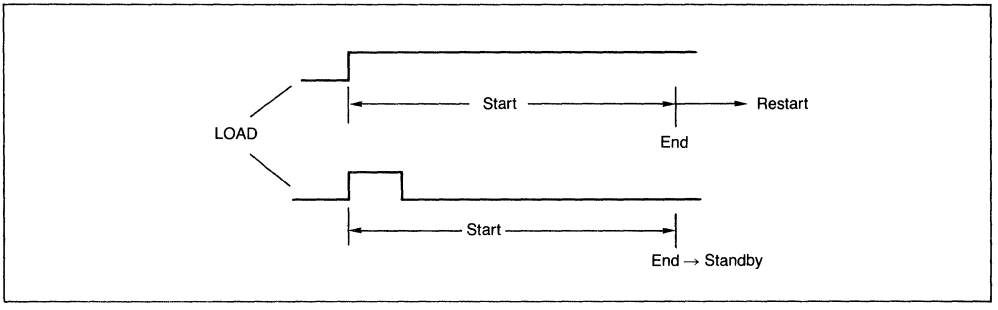
2. SW input interface
By the reason described in clause 9.1.1. CPU interface, number of words is set to maximum 124 words with combination of A_0 to A_6.

After the code is set by A_0 to A_6, when "H" level LOAD input is switched by push switch, etc., the specified word starts speaking. (From standby to operation state).

When speaking of the specified word is completed, if the LOAD input is set being "H" as it is, repeat speaking of the same word, and if the LOAD input turns to "L", LSI moves to standby state automatically.

Therefore, for example, so far the push switch is being pushed as it is, speaking of the same word is repeated. When the push switch is released, the repetition is stopped at the same time of the speaking ends.

To make speaking of different words continuously, change the codes of A_0 to A_6 before the first word speaking comes to end, and keep the LOAD in "H" state.



Sampling Frequency Specification
An user can specify available sampling frequency for each word when ordering.

Relation between sampling frequency and oscillator frequency is as follows:

In the case of $f_{(OSC)} = 32.768$ kHz

Selection 1. $\dfrac{32.768 \text{ kHz}}{4} \fallingdotseq 8.2$ kHz

Selection 2. $\dfrac{32.768 \text{ kHz}}{5} \fallingdotseq 6.55$ kHz

Selection 3. $\dfrac{32.768 \text{ kHz}}{8} \fallingdotseq 4.1$ kHz

Straight ADPCM and Compressed ADPCM

1. Straight ADPCM

Features of the straight ADPCM are as follows:

1) ADPCM bit length ..... Fixed in 4 bits.
2) Deletion of silent component is possible.
3) High bit rate, high tone quality.
4) Suitable for a sound effect

Bit rate (B·R) example:

f_{SAMPLE} = 8.2 kHz
ADPCM bit length = 4 bits
Deleted silent data ≒ 1/5 (voice)
B·R ≒ 8.2×4×4/5 ≒ 26.3 kbits/sec

2. Compressed ADPCM

Features of the compressed ADPCM are as follows:

1) ADPCM bit length ..... Fixed in 4 bits
2) Deletion of data by repeated detection of speech waveform.
3) Deletion of silent component is possible.
4) Low bit rate
5) Mainly applies to speech.

Bit rate example:

f_{SAMPLE} = 8.2 kHz
ADPCM bit length = 4 bits
Number of average waveform repetition = 3 (deleted data = 2/3)
Deleted silent data ≒ 1/5
B·R ≒ 8.2×4×1/3×4/5 ≒ 8.8 kbits/sec

Sampling Frequency and Band

1. Simple relation between sampling frequency and band

$f_{SAMPLE} \times 1/2 = f_{BAND(UL)}$

Here, $f_{BAND(UL)}$ means upper limit of the band.

f_{SAMPLE}	f_{BAND}	Characteristics
8.2 kHz	DC ~ 4.1 kHz	Clear comprehending almost all tones of voice.
6.55 kHz	DC ~ 3.2 kHz	High tone female voice sounds usual.
4.1 kHz	DC ~ 2.0 kHz	Both male and female voices sound nasal and unclear.

2. Relation between sampling frequency and LPF (Low Pass Filter) is as follows:

$f_{SAMPLE} \times 1/2 = f_C$ (cut-off frequency of ideal filter)

Practically, according to the skirt characteristics of filter, f_C shall be designed to be lower than the above mentioned equation. That is, the band will be further narrowed according to filter characteristics.

As an example, the f_C and skirt characteristics of filter used for speech analysis by OKI are shown as follows.

f_{SAMPLE}	f_C	Skirt character	f_{BAND}
8.2 kHz	3.4 kHz	−48 dB/oct	Dc ~ 3.4 kHz
5.55 kHz	2.7 kHz	−48 dB/oct	DC ~ 2.7 kHz
4.1 kHz	1.7 kHz	−48 dB/oct	DC ~ 1.7 kHz

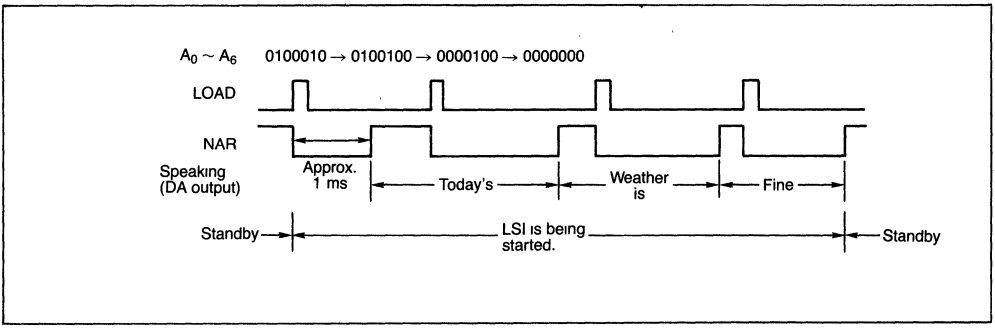
Precautions in Use

1. Relation between LOAD and NAR

A LOAD pulse input is effective when NAR output is "H" state, and at the LOAD pulse rise NAR output transfers to "L" state which will be held till the completion of the former word speaking.

Therefore, use of NAR output is capable of speaking smoothly of the sentence composed of some words.

Example:	"Today's"	"Weather is"	"Fine"	"END"
Corresponding codes by A_0 to A_6	0100010	0100100	0000100	0000000



2. Internal random number circuit

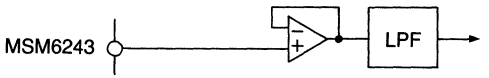
Use of internal random number circuit may be specified on the occasion of order, but the specification prohibits external code input by $A_0 \sim A_6$ and maximum word number is limited to 32 words.

3. Analog output (DAU, DAL)

The output of 10 bits DA converter is connected to DAU and DAL pins directly.

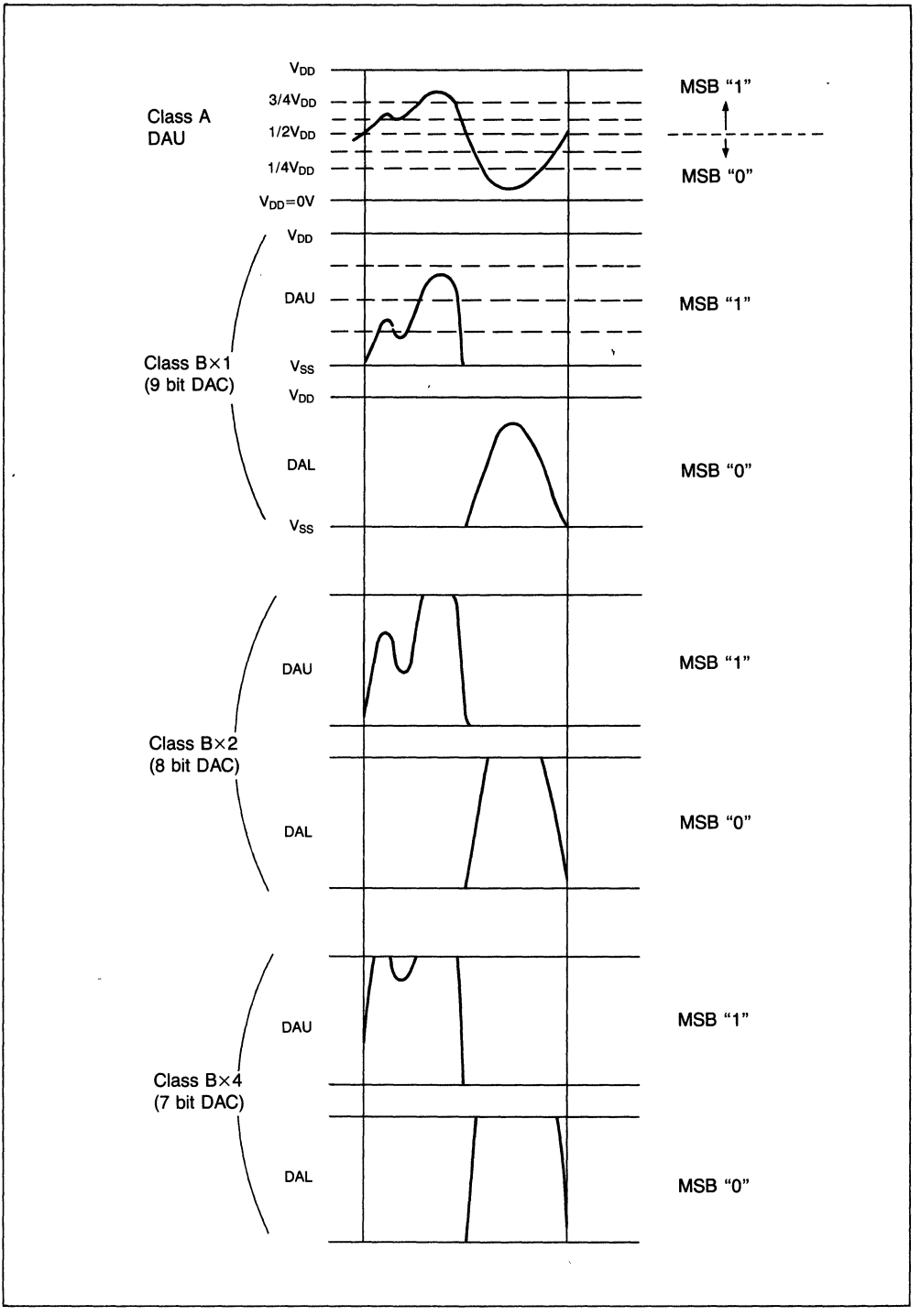
Since this output impedance is great and LPF is not built-in, it is necessary to connect outside LPF through the low impedance output buffer.

Circuit example:



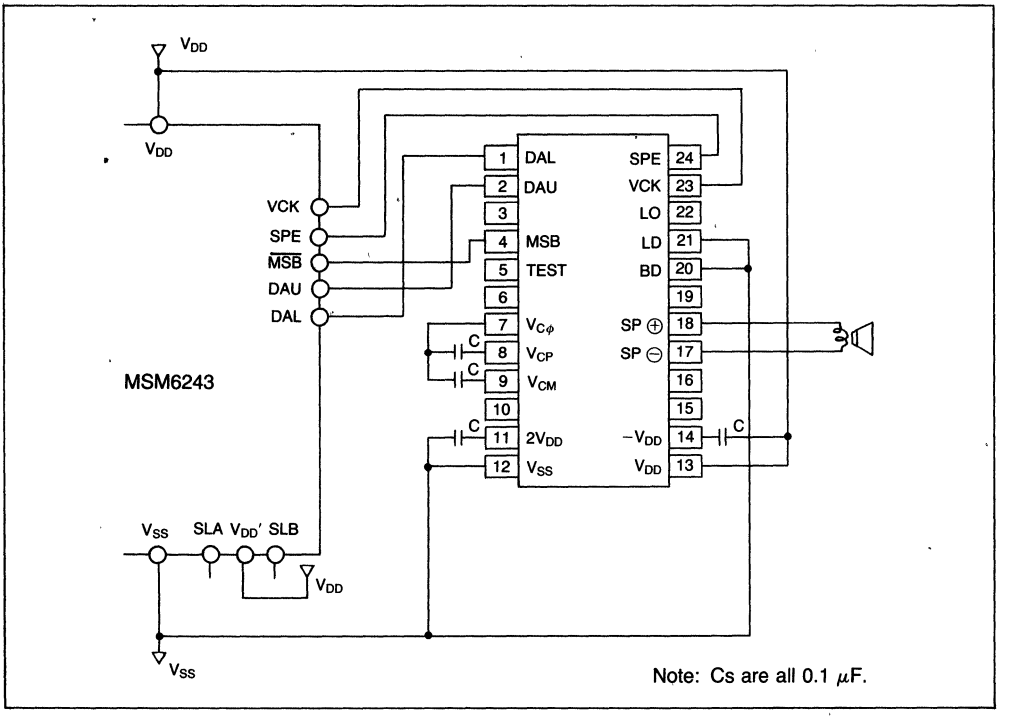
For output status, the following modes of class A and class B are obtained by 2 pins of SLA and SLB.

SLA	SLB	Mode	Output pin
Open (L)	Open (L)	Class B×2	DAU, DAL
V_{DD} (H)	Open (L)	Class B×1	Same as above
Open (L)	V_{DD} (H)	Class B×4	Same as above
V_{DD} (H)	V_{DD} (H)	Class A	DAU

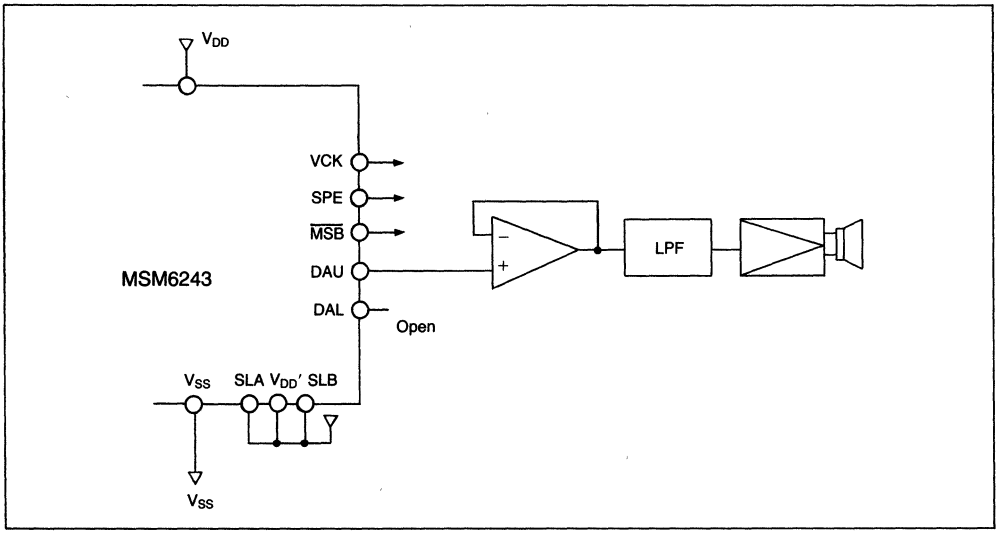

Class A
DAU
V_{DD}
$3/4V_{DD}$
$1/2V_{DD}$
$1/4V_{DD}$
$V_{DD}=0V$
MSB "1"
MSB "0"
Class B×1
(9 bit DAC)
V_{DD}
DAU
V_{SS}
V_{DD}
DAL
V_{SS}
MSB "1"
MSB "0"
Class B×2
(8 bit DAC)
DAU
DAL
MSB "1"
MSB "0"
Class B×4
(7 bit DAC)
DAU
DAL
MSB "1"
MSB "0"

EXAMPLE OF OUTPUT INTERFACE

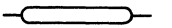
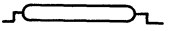
- In the case of class B use, output interface is connected with MSC1161GS (provided, for only 3V system)



- Output of class A

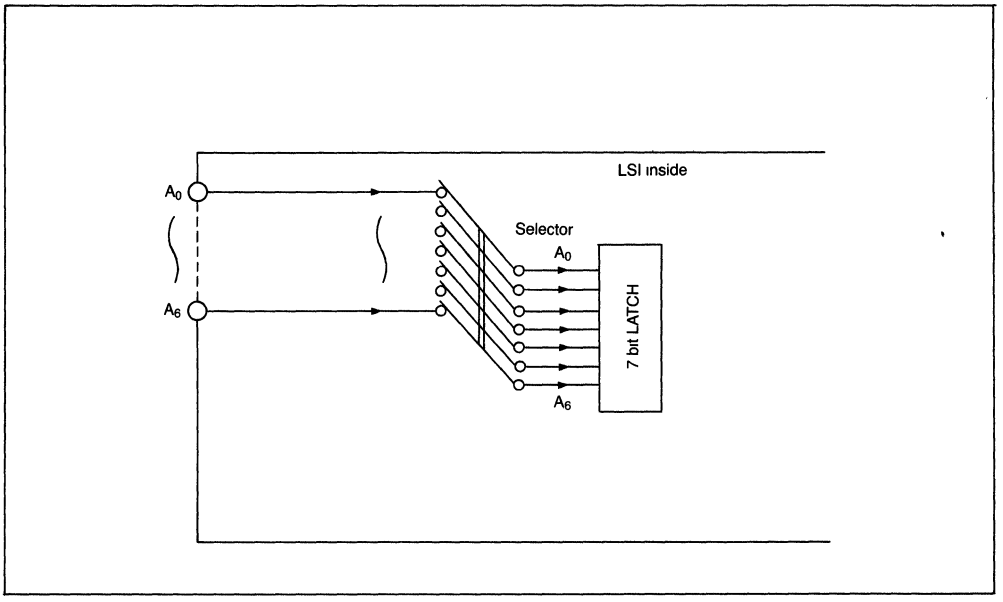


USER SPECIFIED PARAMETER

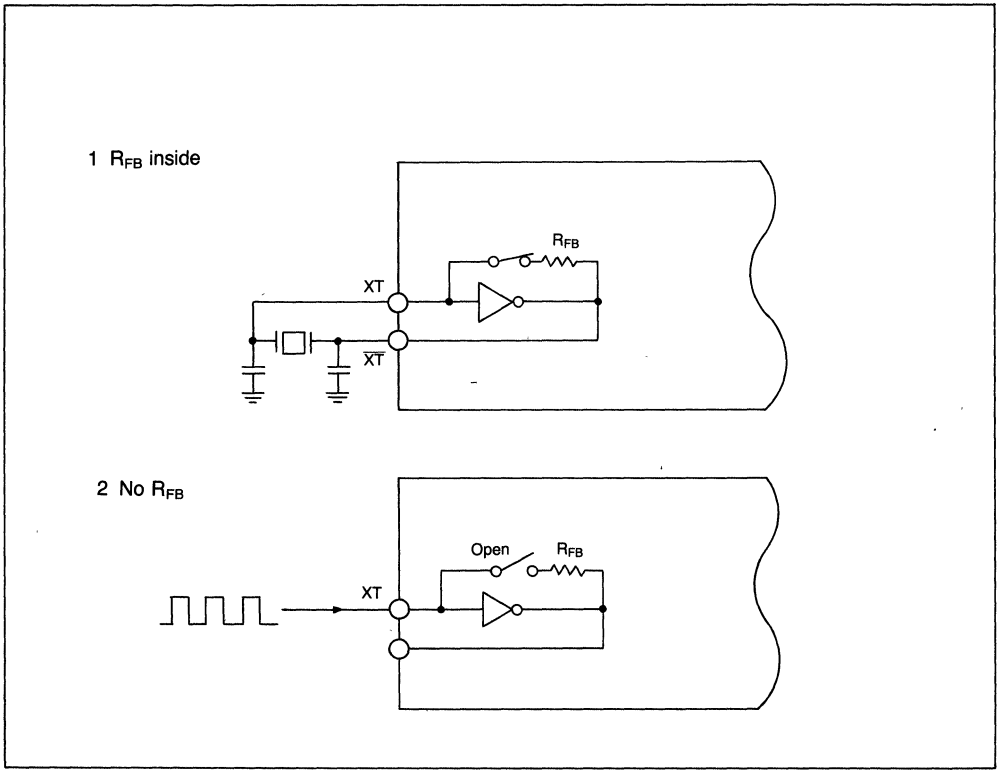
No.	Item	User specification				Remarks
1	Shipping form	Chip	DIP (40 pin)	Flat (60 pin) GS	Flat (60 pin) GS-K	Pin without bending for GS  Pin bending for GS-K  Package side view
2	Supply voltage	3V system (2.4 ~ 3.6V)		5V system (4.5 ~ 5.5V)		
3	Operational temperature	___°C ~ ___°C				
4	Interface condition	SW input interface		CPU input interface		
5	BUSY/NAR	BUSY		NAR		
6	Word code input	External		Internal random number		Refer to circuit 1.
7	Oscillator	32.768 kHz		Other than 32.768 kHz		In the case other than 32.768 kHz, specify the oscillator frequency in the range of 30 to 132 kHz.
8	Sampling frequency	8.2 kHz (1/4)	6.55 kHz (1/5)	4.1 kHz (1/8)		When oscillator frequency is other than 32.768 kHz, specify dividing ratio within a parenthesis.
9	R_{FB} of internal oscillation circuit	Exists		Not exists		Exists → Connect the resonator to XT and XT. Not exists → Apply external clock to TX. Refer to circuit 2.
10	Specification of correspondence between speaking word and word code (A_0 to A_6)	Specify		Not specify		When specified, attach corresponsing table with this paper When not specified, OKI decides it.
11	Editing of speaking words	Editing		No editing		In the case of editing, attach an example sentence with this paper. Ex. 3 o'clock 10 minutes

Note 1. For parameters of No. 4, 5, 6, 8, 9, 10, and 11, corresponds with ROM mask.
Note 2. When an user creates a voice data, never write the voice data in 256 words×126 bits (3 kbits) from the top.

Circuit 1. The following chart shows simple circuit when the word is specified.



Circuit 2. The following charts show the interface examples for XT and $\overline{XT}$.



OKI semiconductor

MSM6212

ADPCM 288K ROM VOICE SYNTHESIZER

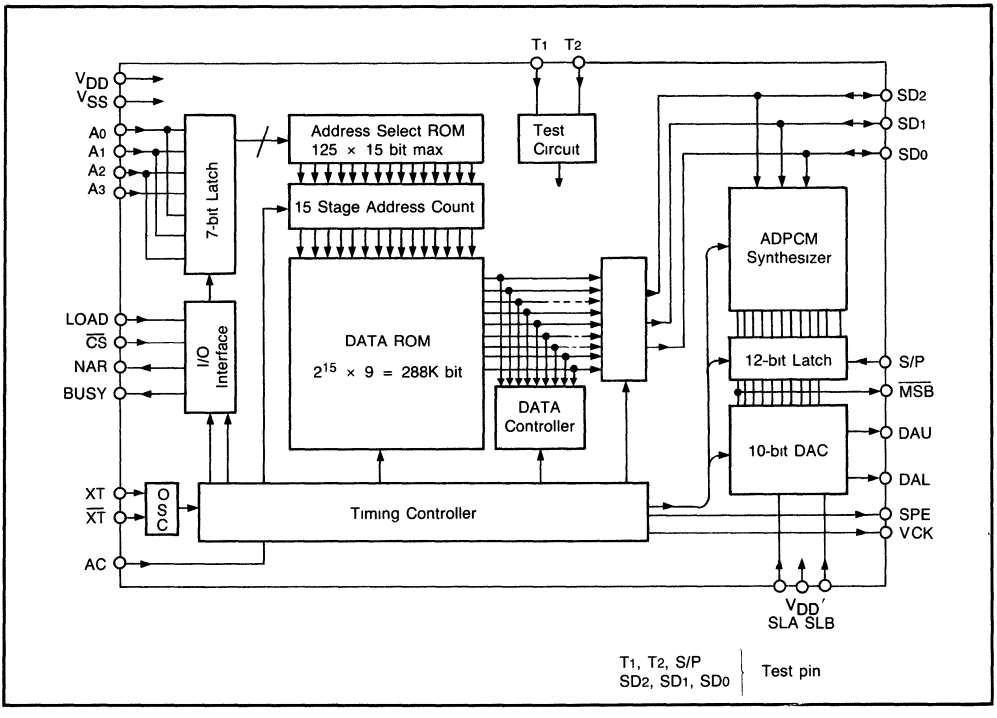
GENERAL DESCRIPTION

MSM6212 is a single-chip ADPCM speech synthesizer incorporating 288K bits ROM to store speech data. In addition to ROM and speech synthesizer circuits, MSM6212 contains an input interface, timing generator circuit and a 10-bit DA converter. Therefore it is possible to configurate a speech output system easily merely by connecting a simple circuit to the speech output consisting of a filter, an amplifier and a speaker.

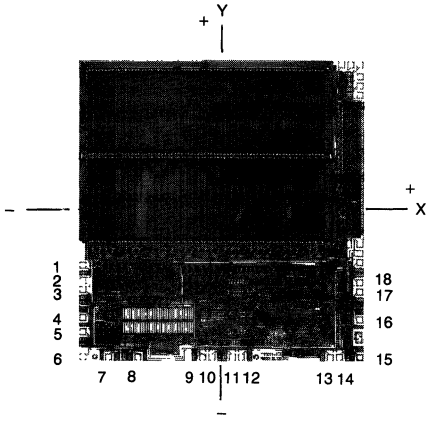
FEATURES

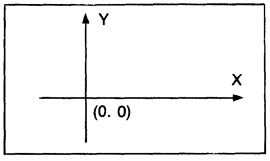
- Low power consumption
- On-chip 288K ROM
- 2 power supply selectable: 3 V or 5 V systems
- Maximum No. of syllable words: 124 words
- Maximum speaking time: 40 sec (compressed ADPCM)
- Class A and Class B analog outputs selectable
- Built-in 10-bit DA converter
- Oscillator frequency: 32,768 kHz
- Available in 40 pin plastic DIP, 60 pin plastic flat package, or die form.

BLOCK DIAGRAM



PAD LAYOUT





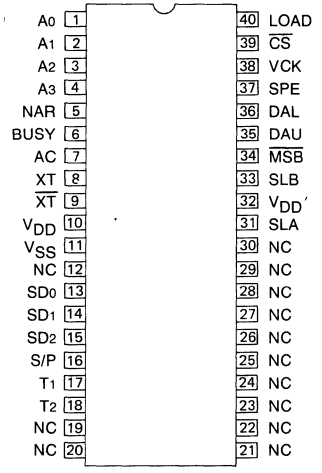
Note: • Chip size: 5.7 mm × 6.0 mm

PAD LOCATION

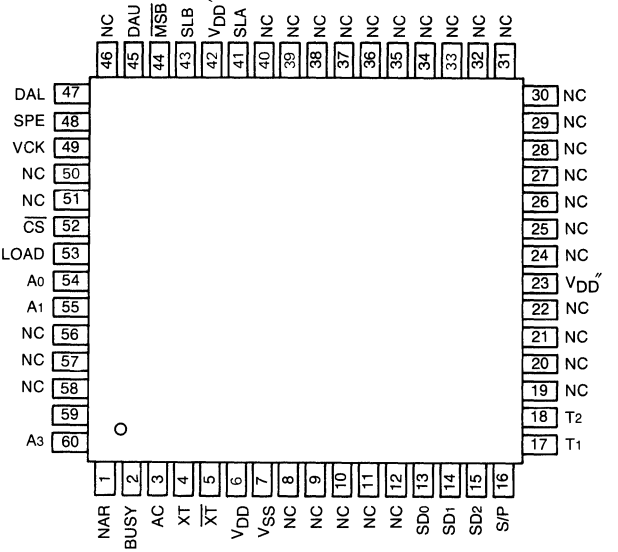
Pad No.	Symbol	Position	
		X	Y
1	SLA	−2699	−1063
2	V_{DD}'	−2699	−1365
3	SLB	−2699	−1545
4	$\overline{MSB}$	−2699	−2091
5	DAU	−2699	−2363
6	DAL	−2699	−2849
7	SPE	−2199	−2849
8	VCK	−1635	−2849
9	$\overline{CS}$	−381	−2849
10	LOAD	−201	−2849
11	A_0	201	−2849
12	A_1	381	−2849
13	A_2	2121	−2849
14	A_3	2301	−2849
15	NAR	2699	−2849
16	BUSY	2699	−2123
17	AC	2699	−1577
18	XT	2699	−1397
19	$\overline{XT}$	2699	−995
20	V_{DD}	2699	−815
21	V_{SS}	2699	−635
22	SD_0	2699	2263
23	SD_1	2699	2443
24	SD_2	2699	2623
25	S/P	2699	2849
26	T_1	2519	2849
27	T_2	2339	2849

PIN CONFIGURATION

(Top View)
40 Lead Plastic DIP
(MSM6212RS)



(Top View)
60 Lead Plastic Flat Package (MSM6212GS)



Note: Connect pin 23 (V_{DD}") with V_{DD} and V_{DD}' externally since this pin is conducted to the substrate.

ELECTRICAL CHARACTERISTICS

3 V System (V_{DD} = 3.1 V Typ)

Absolute Maximum Rating (V_{SS} = 0 V)

Item	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +3.6	V
Input Voltage	V_I		−0.3 to V_{DD}	V
Storage Temperature	Tstg	—	−55 to +150	°C

Recommended Operating Range (V_{SS} = 0 V)

Item	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	—	+2.4 to +3.6	V
Operating Temperature	Top	—	−10 to +60	°C
DAU and DAL Output Level	V_{OD}	No load	0 to V_{DD}	V

DC Characteristics (V_{DD} = 3.1 V, V_{SS} = 0 V, Ta = 25°C)

Item	Symbol	Conditions	Min	Typ	Max	Unit
"H" Input Voltage	V_{IH}	—	2.5	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Input Current *1	I_{IH1}	V_{IH} = 3.1 V	—	—	1	μA
"H" Input Current *2	I_{IH2}	V_{IH} = 3.1 V	10	—	150	μA
"L" Input Current	I_{IL}	V_{IL} = 0 V	—	—	−1	μA
"H" Output Current	I_{OH}	V_{OH} = 2.7 V	−50	—	—	μA
"L" Output Current	I_{OL}	V_{OL} = 0.4 V	50	—	—	μA
Operating Current Consumption	I_{DD1}	—	—	0.1	0.5	mA
Standby current Consumption	I_{DD2}	When selecting class "B" output	—	0.01	0.5	μA
DA Output Accuracy	$\|V_E\|$	No Load	—	—	100	mV
DA Output Impedance	V_{OR}	—	—	170	—	kΩ

Notes: *1 Applied to AC, LOAD and A_0 to A_3 terminals
*2 Applied to input terminals other than the above.
However, terminals SLA and SLB are applied when AC input is set to "H" (Conform to Note 1 when AC input is set to "L").

5 V System (V_{DD} = 5.0 V Typ)

Absolute Maximum Rating (V_{SS} = 0 V)

Item	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +5.5	V
Input Voltage	V_I		−0.3 to V_{DD}	V
Storage Temperature	Tstg	—	−55 to +150	°C

Recommended Operating Range (V_{SS} = 0 V)

Item	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	—	+4.5 to +5.5	V
Operating Temperature	Top	—	−30 to +70	°C
DAU and DAL Output Level	V_{OD}	No load	0 to V_{DD}	V

DC Characteristics (V_{DD} = 5.0 V, V_{SS} = 0 V, Ta = −30 to +70°C)

Item	Symbol	Conditions	Min	Typ	Max	Unit
"H" Input Voltage	V_{IH}	—	4.0	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	1.0	V
"H" Input Current *1	I_{IH1}	V_{IH} = 5.0 V	—	—	1	µA
"H" Input Current *2	I_{IH2}	V_{IH} = 5.0 V	40	—	400	µA
"L" Input Current	I_{IL}	V_{IL} = 0 V	—	—	−1	µA
"H" Output Current	I_{OH}	V_{OH} = 4.6 V	−1	—	—	mA
"L" Output Current	I_{OL}	V_{OL} = 0.4 V	1	—	—	mA
Operating Current Consumption	I_{DD1}	—	—	0.2	0.7	mA
Standby current Consumption	I_{DD2}	—	—	30	100	µA
DA Output Accuracy	$\lvert V_E \rvert$	No Load	—	—	130	mV
DA Output Impedance	V_{OR}	—	—	150	—	kΩ

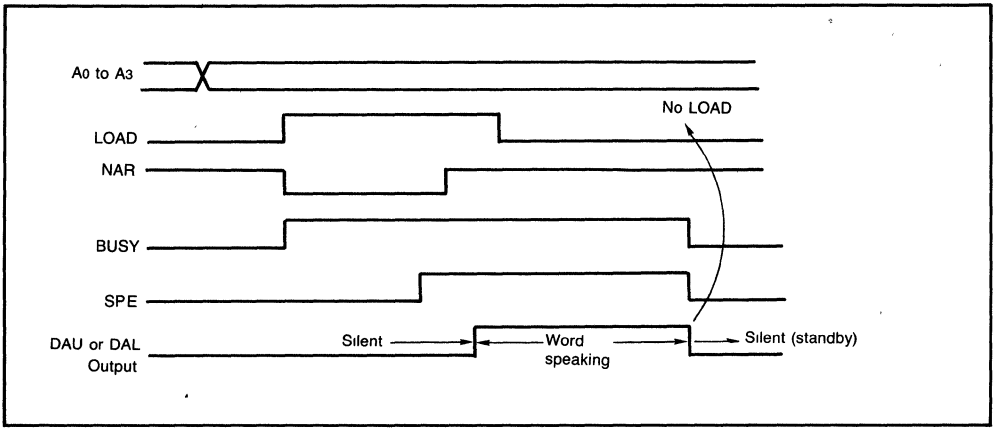
Notes: *1 Applied to AC, LOAD and A_0 to A_3 terminals
*2 Applied to input terminals other than the above. However, terminals SLA and SLB are applied when AC input is set to "H" AC power.
(Conform to Note 1 when AC input is set to "L").

AC Characteristics (Common to V_{DD} = +2.4, +5.5 V, 3 V system and 5 V system)
Ta = −30 to +70°C $f_{(OSC)}$ = 32.768 kHz

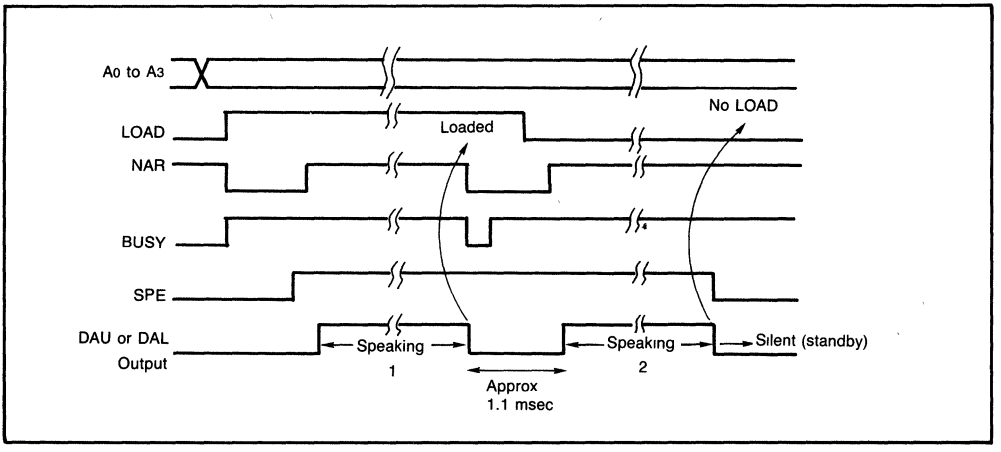
Item	Symbol	Conditions	Min	Typ	Max	Unit
Original oscillation frequency (1)	$f_{(OSC1)}$	3 V system	30	32.768	35	kHz
Original oscillation frequency (2)	$f_{(OSC2)}$	5 V system	30	32.768	65	kHz
Original oscillation duty cycle	f_{duty}	—	40	50	60	%
Load Input Pulse Width	t_L	When f sample = 8.19 kHz	1	—	45	µs
AC Input Pulse Width	$t_{W(AC)}$	—	1	—	—	µs
Sampling Frequency (1)	f_{S1}	$f_{(OSC)/4}$	—	8.192	—	kHz
Sampling Frequency (2)	f_{S2}	$f_{(OSC)/5}$	—	6.554	—	kHz
Sampling Frequency (3)	f_{S3}	$f_{(OSC)/8}$	—	4.096	—	kHz
NAR minimum "H" Level Width	t_{MN}	When f_{S1} is selected	1	—	—	µs
Input Change Standby Time	t_A	When f_{S1} is selected	1	—	—	µs
Load Pulse Interval	t_{NL}	When f_{S1} is selected	5	—	1000	µs

ACTUATION AND NON-OPERATION OF SW INPUT INTERFACE

1. Single Speaking



2. Repeated Speaking



PIN DESCRIPTION

Pin Name	Terminal Number			I/O
	CHIP	40 DIP	60 FLT	
LOAD	10	40	53	I

The LOAD pulse can be applied when NAR level (see below) is "H". When LOAD is set to "H", the code at A_0 to A_3 is transferred into the latch.
A single pulse or a pair of pulses switches the LSI from standby mode to active.

NAR	15	5	1	O

Next address request
NAR indicates whether the LOAD pulse (see above) can be applied or not. "H" level enables while an "L" output disable.
NAR outputs a "H" when the speaking of the current addressed word begins and indicates the next address code can be entered.

$\overline{CS}$	9	39	52	I

Chip select
This pin enables the use of multiple LSI's. It is open when a single LSI is used because it has an internal pull-down resister. If "H" is applied to $\overline{CS}$, the LSI is retained in "standby" mode.

BUSY	16	6	2	O

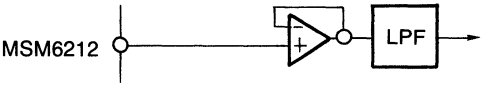
This pin is used for CPU interface, outputting "H" level during the speaking time.

AC	17	7	3	O

All clear
A "H" pulse to this pin stops all internal functions and the LSI switches to standby mode.
No power ON clear circuit is built in the LSI. Therefore, make sure that AC pulse is applied when the power supply is made.

DAU	5	35	45	O
DAL	6	36	47	O

These pins (DAU and DAL) are connected to the output of the 10-bit DA converter. These pins have no built-in LPF because of high output impedance. Use them connected to LPF through the buffer of external low-output impedance.
Example of circuit:

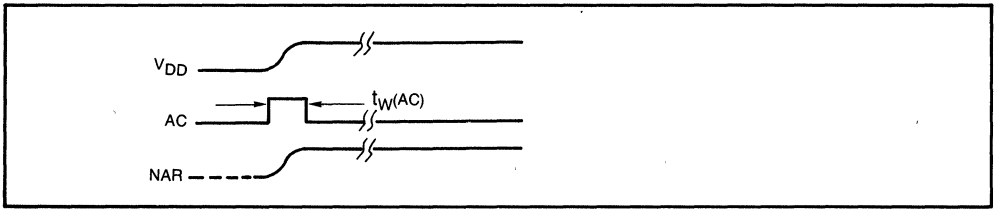


The following class A and class B modes can be obtained from two pins.

SLA	SLB	Mode	Output Pin
Open (L)	Open (L)	Class B × 2	DAU, DAL
V_{DD} (H)	Open (L)	Class B × 1	DAU, DAL
Open (L)	V_{DD}(H)	Class B × 4	DAU, DAL
V_{DD} (H)	V_{DD}(H)	Class A	DAU

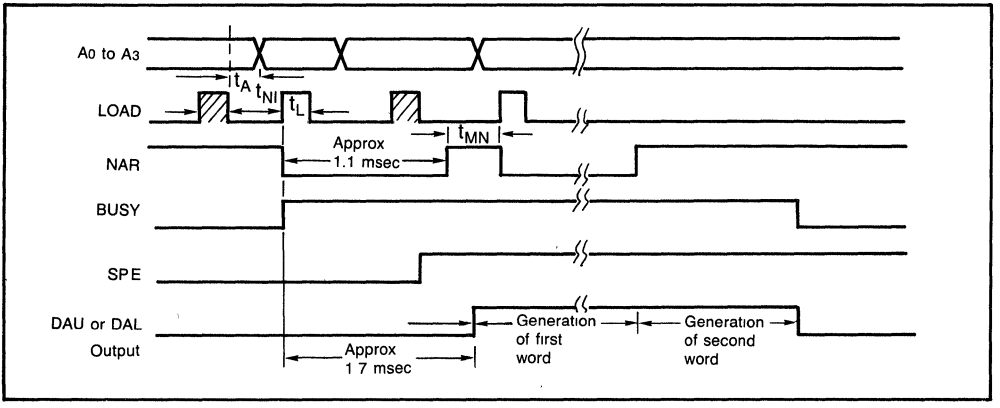
TIMING CHART

1. Power on Sequence

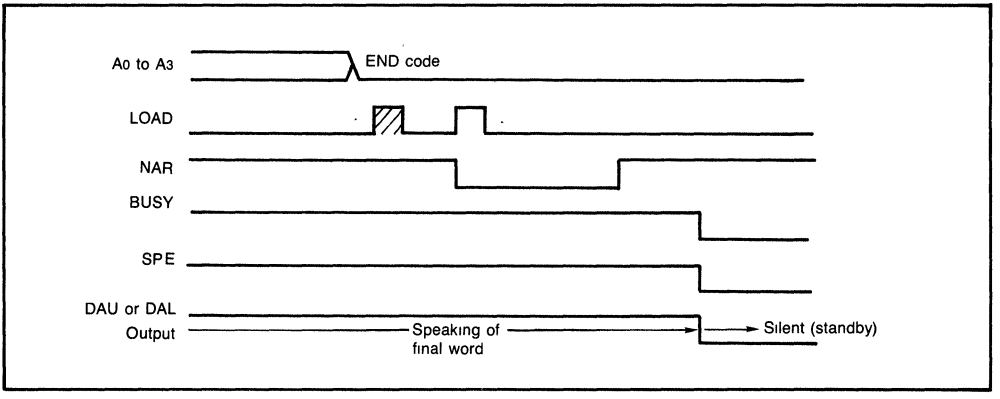


2. LSI Starting and Non-operation (Stand-by)

OPERATING SEQUENCE FOR CPU INTERFACE



FROM OPERATION TO STANDBY IN THE CASE OF CPU INTERFACE



Note: t_A ..... Address hold time
t_{NL} ..... Double LOAD pulse interval
t_L ..... LOAD pulse width
t_{MN} ..... NAR "H" width

FUNCTIONAL DESCRIPTION

DESIGNATION OF SYLLABLE CODES

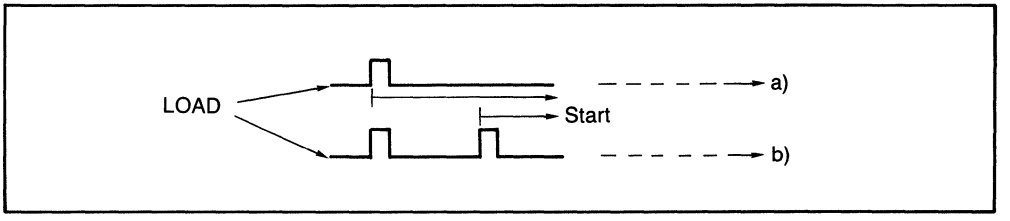
User can designate syllable codes by A_0 to A_3 and can select either CPU interface or simple interface.

1. CPU Interface

In this case, the maximum number of user's designated words (syllables) is 124. All "L"s represent "END" code. A_0 to A_3 and "LOAD" pulse are related to each other as shown below.

a) Single "LOAD" pulse (The max No. of words is 14)
Input A_0 to A_3 → apply "LOAD" pulse → data is latched internally and at the same time, the LSI is actuated.

b) Two "LOAD" pulses (The max No. of words is 124)
Input A_0 to A_3 → apply first "LOAD" pulse → data is latched internally and LSI retains in "STANDBY" status. → Input A_0 to A_2 (A_3 ignored) → apply second "LOAD" pulse → data is latched internally and at the same time, the LSI is actuated.
For the timing of "LOAD" pulse application, apply it when "NAR" output is at "H" level. For the application of "END" code, conform to the above a) and b).



2. Simple Interface

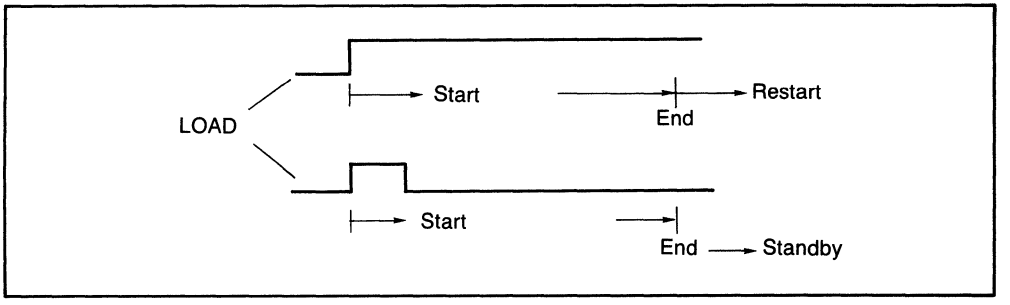
The maximum No. of words is 14. A_0 to A_3 = "H" is a test code.

If "LOAD" input is set at "H" level by means of a push switch after setting of a code by A_0 to A_3, the designated word is spoken (from "Standby" status to "operation" status).

If "LOAD" input is set at "H" level when the speaking of the designated word has ended, the same word is repeated. On the other hand, if "LOAD" input is set at "L" level, LSI is automatically shifted to "STANDBY" status.

Therefore, as long as the push switch continues to be depressed, the same word is repeated. If the push switch is released, the repetition is stopped simultaneous with the ending of speaking.

If the continuous speaking of different words is desired, change codes by A_0 to A_3 and retain "LOAD" input at "H" level, before the speaking of first word is ended.



3. Designation of Sampling Frequency

It is possible for the user to designate the sampling frequency for each word.

The relationship between a sampling frequency and the crystal oscillator frequency is as follows:

When $f_{(OSC)} = 32.768$ kHz

Selection 1 $\quad \frac{32.768\text{ kHz}}{4} = 8.2$ kHz

Selection 2 $\quad \frac{32.768\text{ kHz}}{5} = 6.55$ kHz

Selection 3 $\quad \frac{32.768\text{ kHz}}{8} = 4.1$ kHz

STRAIGHT ADPCM AND COMPRESSED ADPCM

1. Straight ADPCM

The features are enumerated below.

1. Length of ADPCM bits ..... fixed in 3 bits.
2. Deletion of silent component is possible.
3. High bit rate and high tone quality.
4. Suitable to imitation sound.

Example of bit rate

f_{SAMPLE} = 8.2 kHz
Length of ADPCM bits = 3 bits
Deleted silent component ≒ 1/5 (speech)
B•R ≒ 8.2 × 3 × 4/5 ≒ 19.7 kb/sec

2. Compressed ADPCM

The features are enumerated below:

1. Length of ADPCM bits ..... fixed in 3 bits
2. Deletion of data by repeated detection of speech waveform
3. Deletion of silent component is possible.
4. Low bit rate.
5. Mainly applied to speech.

Example of bit rate

f_{SAMPLE} = 8.2 kHz
Length of ADPCM bits = 3 bits
Frequency of average repetition ≒ 3
(Deleted data component of waveform ≒ 1/3)
Deleted silent component ≒ 1/5 (speech)
B•R ≒ 8.2 × 3 × 1/3 × 4/5 ≒ 6.6 kb/sec

SAMPLING FREQUENCY AND BAND WIDTH

1. Simple Relationship between Sampling Frequency and Band Width

$f_{SAMPLE} \times 1/2 = f_{BAND}$ (UL)
Here f_{BAND} (UL) ..... Upper limit of band

f_{SAMPLE}	f_{BAND}	Quality
8.2 kHz	DC to 4.1 kHz	Clear maximum intelligibility
6.55 kHz	DC to 3.2 kHz	Female speech of high tone sounds nasal
4.1 kHz	DC to 2.0 kHz	Unclear both male and female speeches sound nasal

2. The Relationship between a Sampling Frequency and LPF (low pass filter)

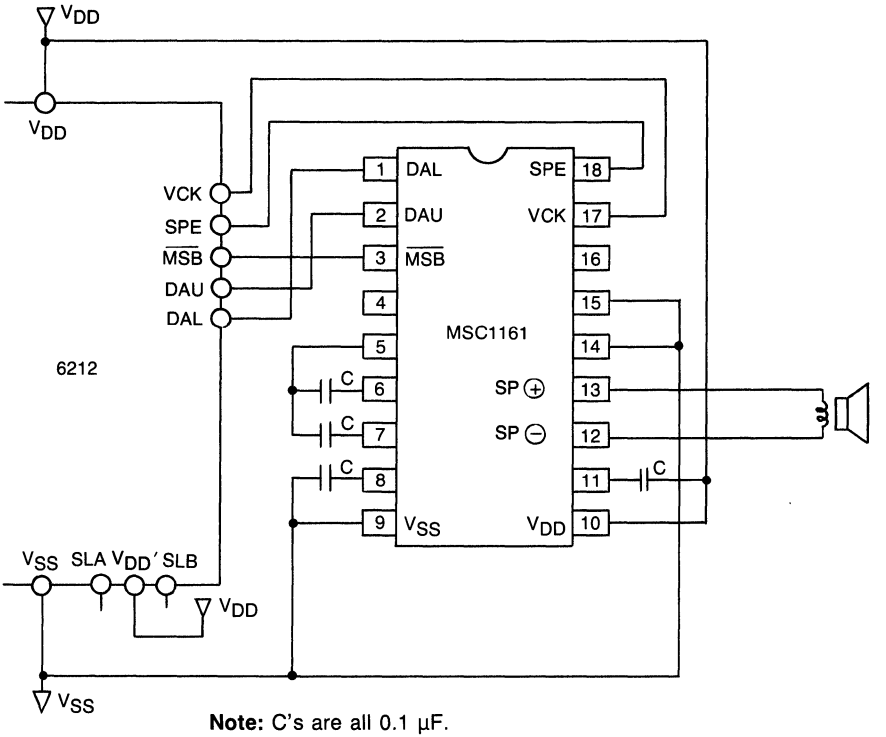
The relationship between a sampling frequency and LPF (low pass filter) is $f_{SAMPLE} \times 1/2 = f_C$ (cutoff frequency of ideal filter). However, realistically it is necessary to design "f_C" to be lower than the above equation according to the skirt characteristics of filter. That is, the band will be further narrowed according to filter characteristics.

As an example, the f_C and skirt characteristics of L.P.F. used for speech analysis by Oki are shown as follows.

f_{SAMPLE}	f_C	Skirt Characteristics	f_{BAND}
8.2 kHz	3.4 kHz	−48 dB/oct	DC to 3.4 kHz
6.55 kHz	2.7 kHz	−48 dB/oct	DC to 2.7 kHz
4.1 kHz	1.7 kHz	−48 dB/oct	DC to 1.7 kHz

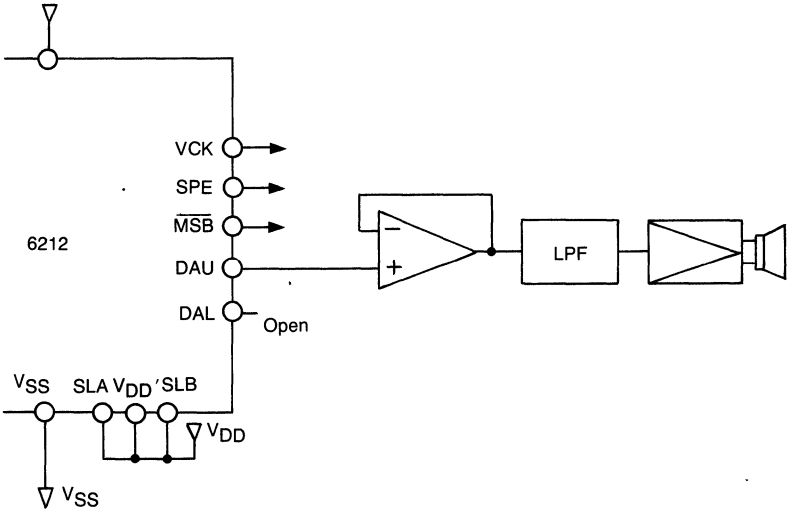
EXAMPLE OF OUTPUT INTERFACE

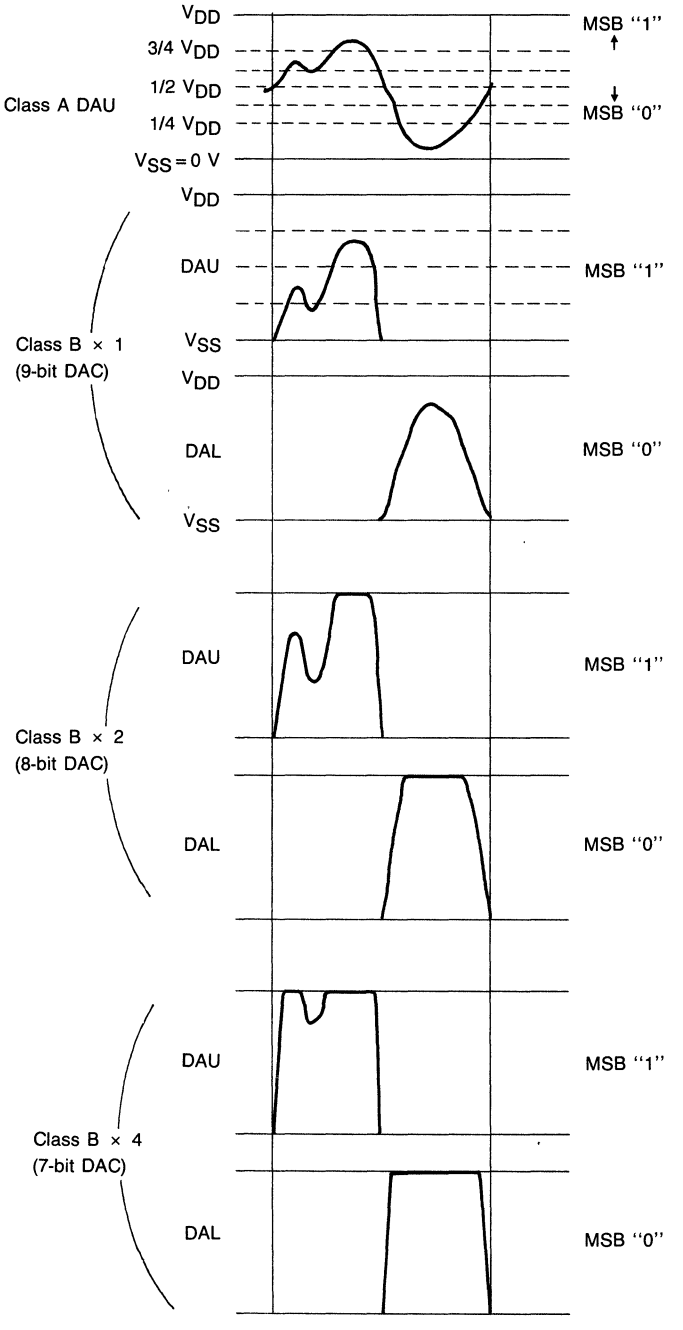
When connected to MSC1161 for Class B (for 3 V system only)



Note: C's are all 0.1 µF.

Class A Output





(An abbreviated name of the type is sometimes used as an indication representing an actual product)

Preliminary

OKI semiconductor

MSM6308

ADPCM SPEECH PROCESSOR FOR SOLID STATE RECORDER DRAM INTERFACE

GENERAL DESCRIPTION

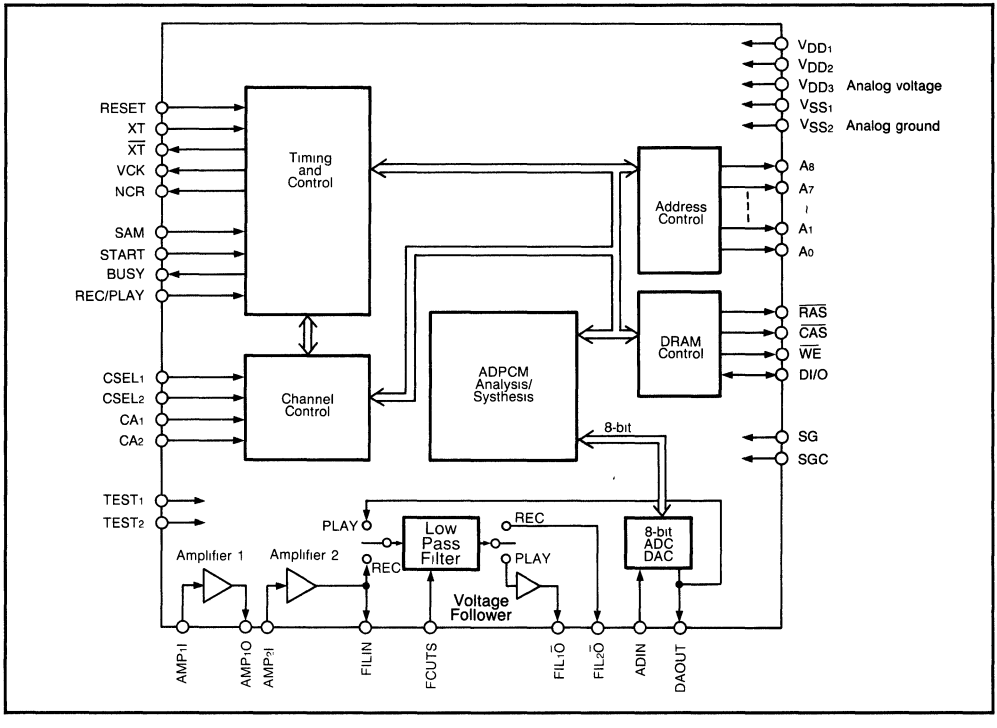
The Oki MSM6308 is a ADPCM speech processor LSI for solid state recording which is manufactured using Oki's low power CMOS silicon gate technology. A maximum of 256K Dynamic RAM is used to store the ADPCM data.

The MSM6308 has internal LPF and amplifier for a microphone. So, by connecting microphone, speaker, speaker driving amplifier and 256K DRAM, recording and playback of voice can be implemented in the same manner as a tape recorder.

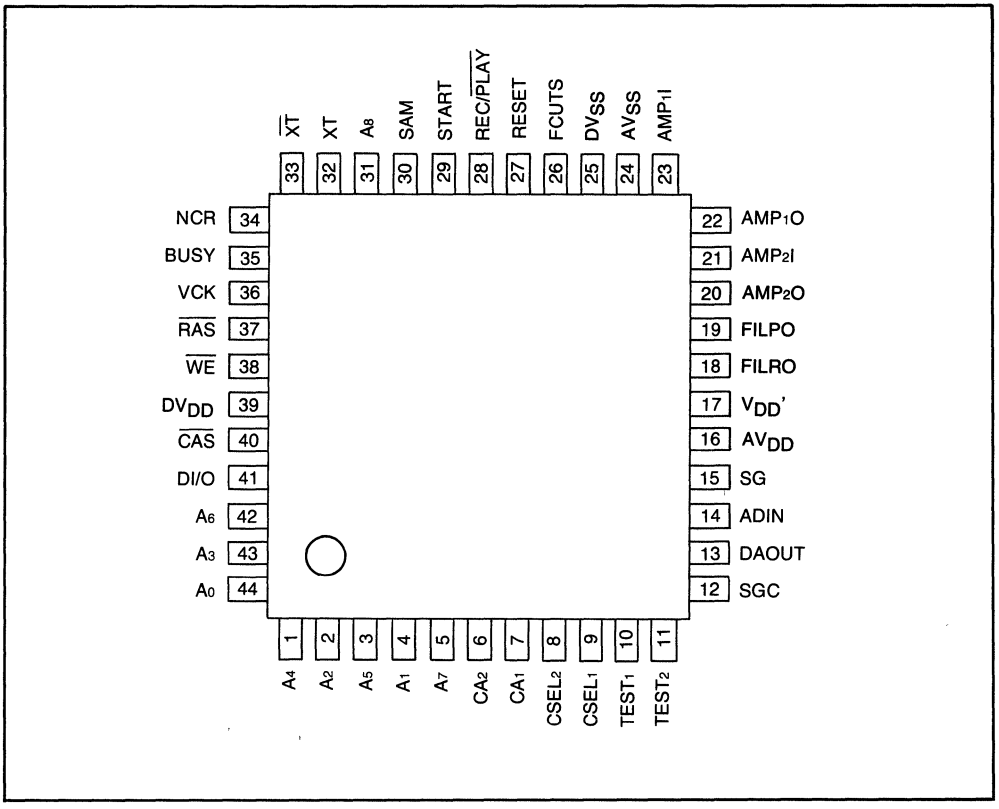
FEATURES

- 4-bit ADPCM algorithm
- Built-in 8-bit AD converter
- Built-in 8-bit DA converter
- Amplifier for microphone on chip
- LPF (Low Pass Filter) on chip
- 256K DRAM direct drive capability
- Oscillation frequency: 4 MHz ~ 6 MHz
- Sampling frequency: 4 kHz, 8 kHz (@ 4 MHz)
- Recording phrase: 1, 2, 4 selectable
- Vocalization time: 16 sec. maximum (@ 4 kHz)
- Supply voltage: +5 V
- 44 pin plastic flat package

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(V_{SS1} = V_{SS2} = 0V)

Parameter	Symbol	Conditions	Value	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to 7.0	V
Input Voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{stg}	—	−55 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS1} = V_{SS2} = 0V	+4.0 to +6.0	V
Operating Temperature	T_{op}	—	−40 to +85	°C
Oscillation Frequency	f_{osc}	—	4.0 to 6.0	MHz

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 $V_{SS1} = V_{SS2}$ = 0V TA = −30 to 70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
"H" Input Voltage *1	V_{IH}	—	3.6	—	—	V
"H" Input Voltage *1	V_{IH}	—	$0.8 \times V_{DD}$	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	$I_{OH} = -40\mu A$	4.2	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
"H" Input Current *3	I_{IH1}	$I_{IH} = V_{DD}$	1	—	100	μA
"H" Input Current *4	I_{IH2}	$I_{IH} = V_{DD}$	—	—	10	μA
"L" Input Current	I_{IL}	$V_{IL} = V_{SS}$	−10	—	—	μA

Note: *1 Apply to input terminals except XT
*2 Apply to XT terminal
*3 Apply to start terminal
*4 Apply to terminal without pull down resistors

PIN DESCRIPTION

Pin Symbol	Pin No.	I/O	Function
DV_{DD}	39	I	Digital power supply terminal
V_{DD}'	17	I	Digital power supply terminal
AV_{DD}	16	I	Analog power supply terminal
DV_{SS}	25	I	Digital ground terminal
AV_{SS}	24	I	Analog ground terminal
SG	15	I	Signal ground terminal Connect condenser for stabilization
SGC	12	I	Connect condenser for stabilization
$AMP_{1}I$	23	I	Input terminal for amplifier 1
$AMP_{1}O$	22	O	Output terminal for amplifier 1

PIN DESCRIPTION (continued)

Pin Symbol	Pin No.	I/O	Function
AMP_{2I}	21	O	Input terminal for amplifier 2
AMP_{2O}	20	O	Output terminal for amplifier 2 This terminal is connected to built-in LPF.
ADIN	14	I	Voice input terminal
DAOUT	13	O	Output of DA converter This terminal is connected to built-in LPF.
FILPO	19	O	Output of LPF Synthesized sound is output from this terminal.
FILRO	18	O	Output of LPF Analyzed sound is output from this terminal. Connect this terminal to ADIN
RESET	27	I	By inputting "H" level, the inside of the circuit returns to the early stage.
REC/$\overline{PLAY}$	28	I	Selection terminal for recording or playback "H" = recording
START	29	I	By inputting "H" level, recording or playback is started.
BUSY	35	O	This terminal outputs "H" level while recording or playback.
$CSEL_1$	9	I	Terminal for selecting number of recording words
$CSEL_2$	8	I	Same as above
CA_1	7	I	Terminal for specifying channels when selecting 2 words or 4 words
CA_2	6	I	Terminal for specifying channels when selecting 4 words
SAM	30	I	Terminal for determining the sampling frequency
D I/O	41	I/O	Input/output terminal for 4 bit ADPCM data
A_0	44	O	Address terminals of 256K DRAM
A_1	4	O	
A_2	2	O	
A_3	43	O	
A_4	1	O	
A_5	3	O	
A_6	42	O	
A_7	5	O	
A_8	31	O	
$\overline{RAS}$	37	O	Row address strobe for a 256K DRAM
$\overline{CAS}$	40	O	Column address strobe for a 256K DRAM
$\overline{WE}$	38	O	Write enable signal to the DRAM device

PIN DESCRIPTION (continued)

Pin Symbol	Pin No.	I/O	Function
XT	32	I	Crystal oscilliator connector terminal
$\overline{XT}$	33	O	Same as above
VCK	36	O	Outputs sampling frequency
NCR	34	O	This terminal is used when playbacks contents of different channels continuously.
F_{CUTS}	26	I	Terminal for selecting the cut-off frequency of the built-in LPF
TEST 1	10	I	Terminal for inhouse testing
TEST 2	11	I	Same as above

FUNCTIONAL DESCRIPTION

The number of recording words of MSM6308 is selectable either a single word, 2 words or 4 words. When selecting 1 word, the maximum memory capacity will be 256K bits. When selecting 2 words, 128K bits are allocated to each channel. When selecting 4 words, 64K bit are allocated to each channel. So each recording length is limited depending on the capacity of each DRAM.

1. Selection of the Number of Recording Words and the Way to Specify Channel ($CSEL_1$, $CSEL_2$, CA_1, CA_2)

$CSEL_1$	$CSEL_2$	Number of Words	CA_1	CA_2	Channel	Capacitance of Channel
L	—	4	L L H H	L H L H	CH1 CH2 CH3 CH4	64K bit
H	L	2	— —	L H	CH1 CH2	128K bit
H	H	1	—	—	CH1	256K bit

2. How to Select the Sampling Frequency (SAM)

Following is the relationship between oscillation frequency and sampling frequency.

SAM	L	H
f_{samp}	$f_{osc}/1024$ (4 kHz)*	$f_{osc}/512$ (8 kHz)*

* When oscillation frequency is 4.096 kHz.

3. How to Select the Cut-off Frequency of LPF

The cut-off frequency of LPF is controlled by F_{CUTS} terminal. Please refer to the following chart.

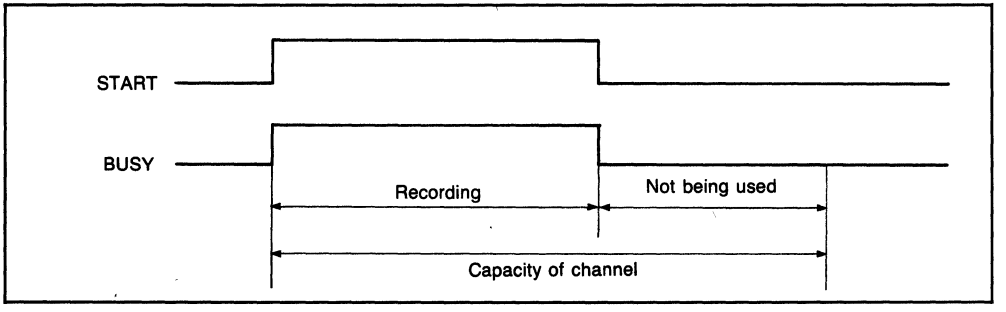
Voice Sampling		F_{CUTS}	
SAM	VCK (Hz)	"H"	"L"
L	4 K	2.3 K	1.95 K
H	8 K	3.8 K	2.9 K

When oscillation frequency is 4.096 kHz.

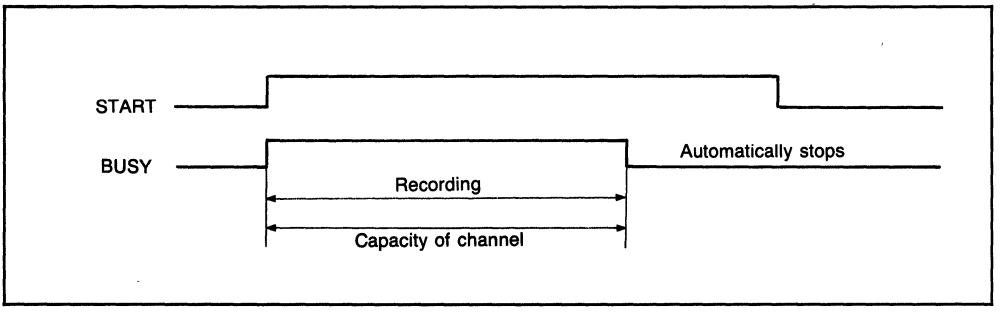
4. Function of REC/PLAY and Start Terminals

RECORDING

1. REC/$\overline{\text{PLAY}}$ = "H" When Recording Using Partial Memory Capacity of the Channel

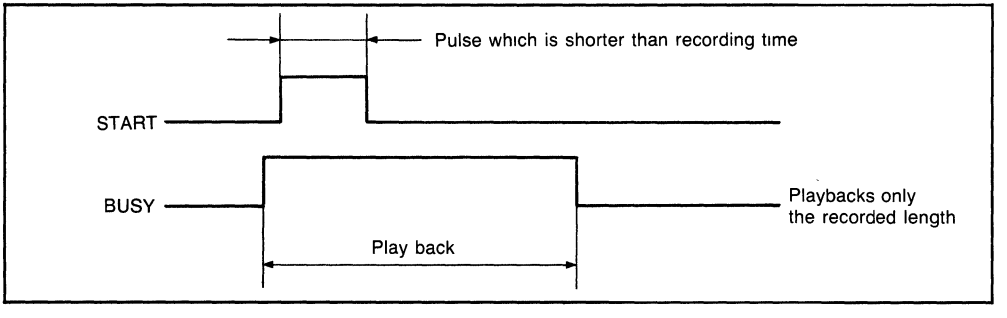


2. REC/$\overline{\text{PLAY}}$ = "H" When Recording Using Entire Memory Capacity of the Channel

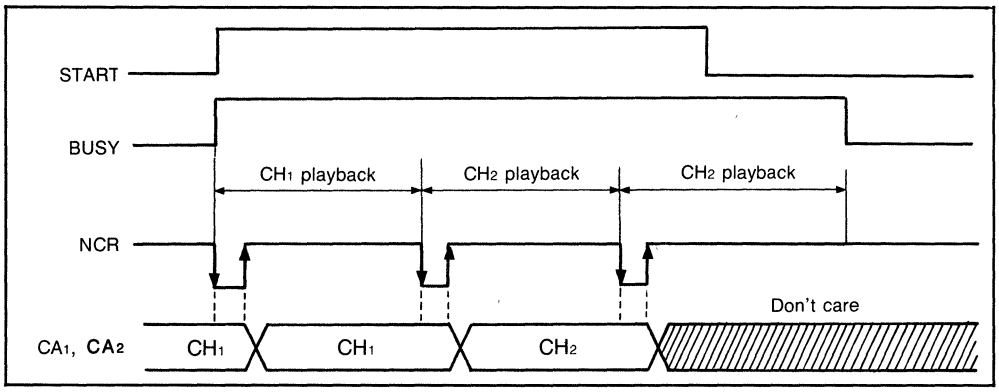


PLAYBACK

3. REC/$\overline{\text{PLAY}}$ = "L" to Playback the Recorded Contents Once



4. REC/$\overline{\text{PLAY}}$ = "L" to Playback the Recorded Content Repeatedly and Continuously



Continuous playback and repeated playback are acheived by maintaining Start terminal at "H" level. Writing to channel is done when NCR goes low, or when starts playinh back each word. So chennels will be changed, if "START" is high, when NCR goes from low to high.

5. Interval of Recording Time

As described up to now, by maintaning REC/$\overline{\text{PLAY}}$ terminal high, recording is achieved for the length of time of Start terminal is high. Recording time could be longer because the interval of recording time is for 4K bit.
The interval of recording time can be figured out by the following formula.

(The interval of recording time) = 4K bit/(bit rate [Kbit/sec])[sec]

EXAMPLE

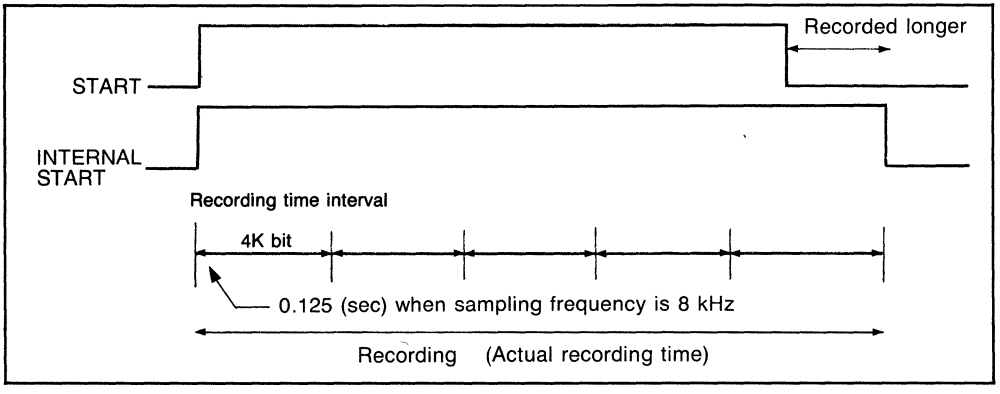
When sampling frequency is 8 kHz, bit rate is

4 bit × 8 kHz = 32K bit/sec.

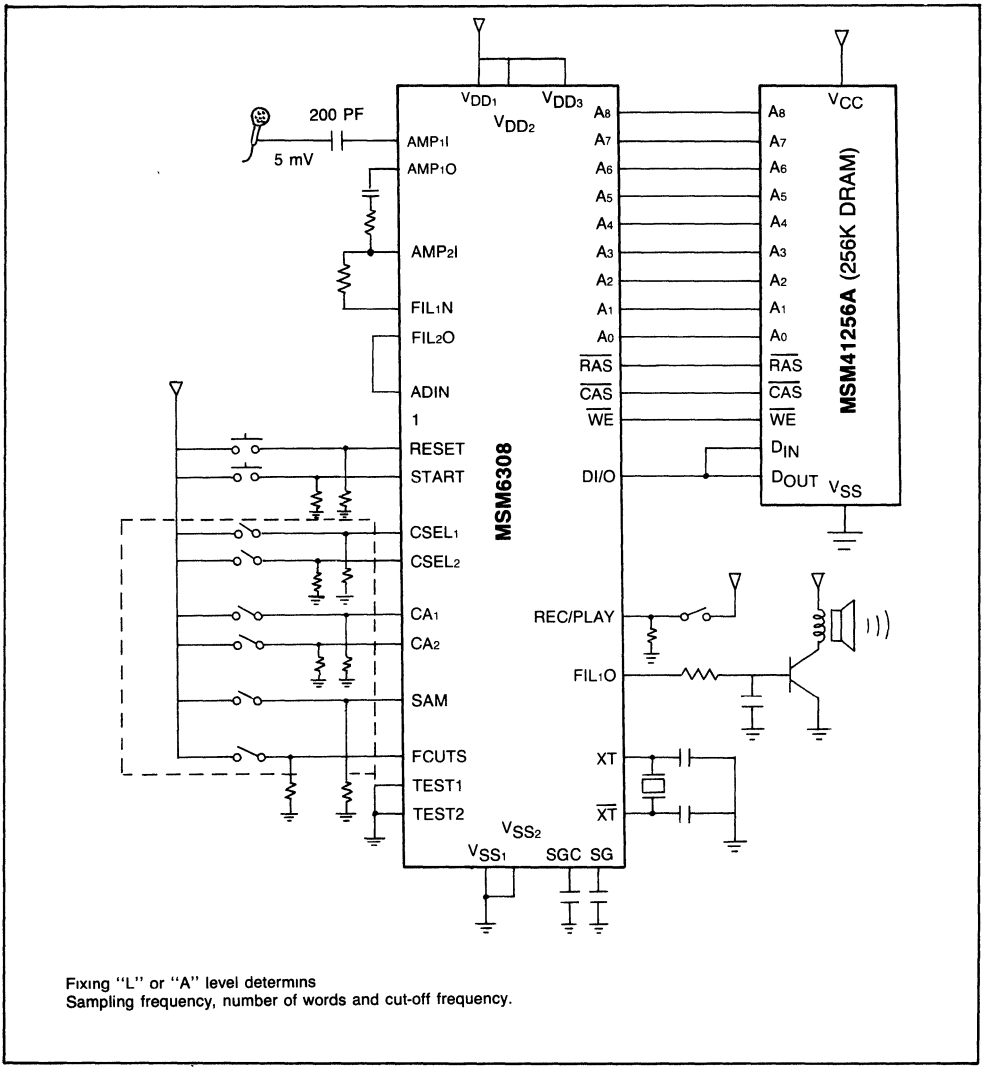
The interval of recording time is

4 bit/32K bit/sec = 0.125 (sec)

So, the recording time becomes a maximum of 0.125 msec.



APPLICATION CIRCUIT



Fixing "L" or "A" level determins
Sampling frequency, number of words and cut-off frequency.

OKI semiconductor

MSM6309

ADPCM SPEECH PROCESSOR FOR SOLID STATE RECORDER SRAM INTERFACE

GENERAL DESCRIPTION

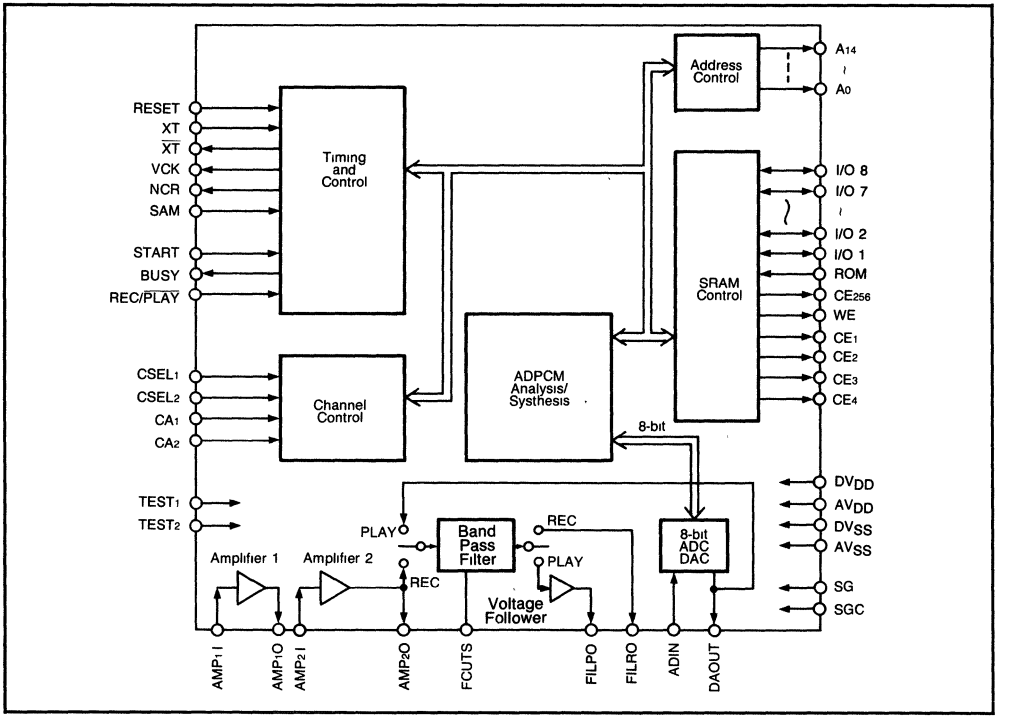
The Oki MSM6309 is a ADPCM speech processor LSI for solid state recording which is manufactured using Oki's low power CMOS silicon gate technology. 64K or 256K static RAM is used to store the ADPCM data.

The MSM6309 has internal LPF and amplifier for microphone. So, by connecting the microphone, speaker, speaker driving amplifier and SRAM, recording and playback of voice can be easily implemented in the same manner as a tape recorder.

FEATURES

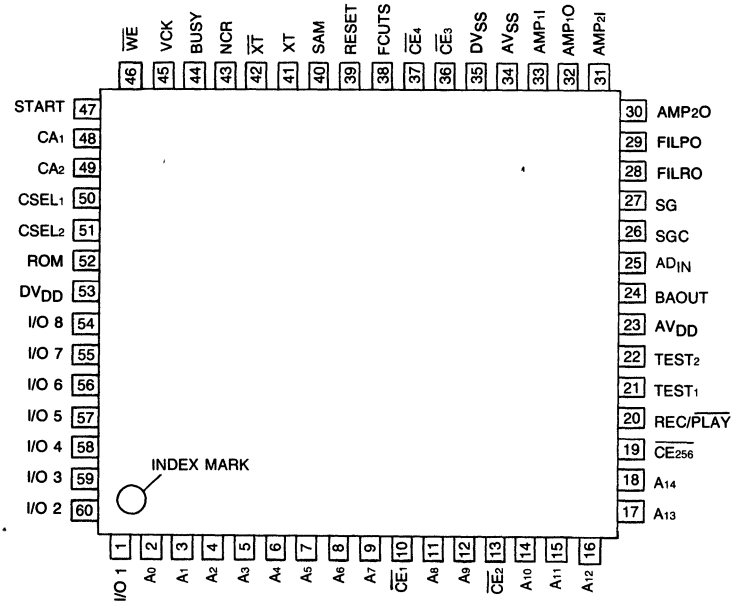
- 4-bit ADPCM algorithm
- Built-in 8-bit AD converter
- Built-in 8-bit DA converter
- Amplifier for microphone on chip
- LPF (Low Pass Filter) on chip
- Direct drive capability for SRAM: 64K 4 pcs
  or 256K
  1 pce
- Oscillation frequency: 4 MHz ~ 6 MHz
- Sampling frequency: 4 kHz, 8 kHz
  (@ 4 MHz)
- Recording phrase: 1, 2, 4 selectable
- Vocalization time: 16 sec maximum
  (@ 4 kHz)
- Supply voltage: +5 V
- 60 pin plastic flat package and

BLOCK DIAGRAM



PIN CONFIGURATION

60 pin Flat Package



ABSOLUTE MAXIMUM RATINGS

(V_{SS1} = V_{SS2} = 0V)

Parameter	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to 7.0	V
Input Voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{stg}	—	−55 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS1} = V_{SS2} = 0V	+3.5 to +6.0	V
Operating Temperature	T_{op}	—	−40 to +85	°C
Oscillation Frequency	f_{osc}	—	4.0 to 6.0	MHz

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V_{SS1} = V_{SS2} = 0V Ta = −40 ~ 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
"H" Input Voltage *1	V_{IH}	—	3.6	—	—	V
"H" Input Voltage *2	V_{IH}	—	0.8 × V_{DD}	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = −40μA	4.2	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
"H" Input Current	I_{IH1}	V_{IH} = V_{DD}	20	—	400	μA
"L" Input Current	I_{IL}	V_{IL} = V_{SS}	−10	—	—	μA

Note: *1 Apply to input terminals except XT
*2 Apply to XT terminal

PIN DESCRIPTION

Pin Symbol	Pin No.	I/O	Function
DV_{DD}	53	I	Degital power supply terminal
AV_{DD}	23	I	Analog power supply terminal
DV_{SS}	35	I	Degital ground terminal
AV_{SS}	34	I	Analog ground terminal
SG	27	I	Signal ground terminal Connect condenser for stabilization
SGC	26	I	Connect condenser for stabilization of SG
$AMP_{1}I$	33	I	Input terminal for amplifier 1
$AMP_{1}O$	32	O	Output terminal for amplifier 1
$AMP_{2}I$	31	I	Input terminal for amplifier 2
$AMP_{2}O$	30	O	Output terminal for amplifier 2 This terminal is connected to built-in LPF.
AD_{IN}	25	I	Voice input terminal
DA_{OUT}	24	O	Output of DA converter This terminal is connected to built-in LPF.
FILPO	29	O	Output of LPF Synthesized sound is output from this terminal.
FILRO	28	O	Output of LPF Analized sound, original sound is output from this terminal
RESET	39	I	By inputting "H" level, the inside of the circuit returns to the early stage, viz. stand-by stage
REC/$\overline{PLAY}$	20	I	Selection terminal for recording or playback "H" = recording
START	47	I	By inputting "H" level, recording or playback is started
BUSY	44	O	This terminal outputs "H" level during recording or playback
$CSEL_{1}$	50	I	Terminal for selecting number of recording phrase
$CSEL_{2}$	51	I	Same as above
CA_{1}	48	I	Terminal for specifying channels when selecting 2 phrases or 4 phrases
CA_{2}	49	I	Terminal for specifying channels when selecting 4 phrases
SAM	40	I	Terminal for determining the sampling frequency

PIN DESCRIPTION (continued)

Pin Symbol	Pin No.	I/O	Function
I/O 1	1	I/O	Input/output terminal for 4-bit ADPCM data
I/O 2	60	I/O	
I/O 3	59	I/O	
I/O 4	58	I/O	
I/O 5	57	I/O	
I/O 6	56	I/O	
I/O 7	55	I/O	
I/O 8	54	I/O	
A_0	2	O	Address terminals of SRAM
A_1	3	O	
A_2	4	O	
A_3	5	O	
A_4	6	O	
A_5	7	O	
A_6	8	O	
A_7	9	O	
A_8	11	O	
A_9	12	O	
A_{10}	14	O	
A_{11}	15	O	
A_{12}	16	O	
A_{13}	17	O	
A_{14}	18	O	
$\overline{CE_1}$	10	O	Control terminals for external 64K SRAM
$\overline{CE_2}$	13	O	
$\overline{CE_3}$	36	O	
$\overline{CE_4}$	37	O	
$\overline{CE_{256}}$	19	O	Control terminals for external 256K SRAM
$\overline{WE}$	46	O	Write enable signal to the SRAM device
ROM	52	I	Make "H" level when EPROM is equipped externally
XT	41	I	Crystal oscillator connector terminal
$\overline{XT}$	42	O	Same as above
VCK	45	O	Outputs sampling frequency
NCR	43	O	This terminal is used when playbacks contents of different channels continuously
F_{CUTS}	38	I	Terminal for selecting the cut-off frequency of the built-in LPF
TEST 1	21	I	Terminal for inhouse testing
TEST 2	22	I	Same as above

FUNCTIONAL DESCRIPTION

The number of recording words of MSM6309 is selectable either 1 word, 2 words or 4 words. When selecting 1 word, the maximum memory capacitance will be 256K bit. When selecting 2 words, each 128K bit is allocated to each channel. When selecting 4 words, each 64K bit is allocated to each channel. So each recording length is limited according to the capacitance of each SRAM.

1. Selection of the Number of Recording Words and the Way to Specify Channel ($CSEL_1$, $CSEL_2$, CA_1, CA_2)

$CSEL_2$	$CSEL_1$	Number of Words	CA_2	CA_1	Channel	Capacitance of Channel
L	—	4	L L H H	L H L H	CH_1 CH_2 CH_3 CH_4	64K bit
H	L	2	— —	L H	CH_1 CH_2	128K bit
H	H	1	—	—	CH_1	256K bit

2. How to Select the Sampling Frequency (SAM)

Following is the relationship between oscillation frequency and sampling frequency.

SAM	L	H
f_{samp}	$f_{osc}/1024$ (4 kHz)*	$f_{osc}/512$ (8 kHz)*

* When oscillation frequency is 4.096 kHz.

3. How to Select the Cut-off Frequency of LPF

The cut-off frequency of LPF is controlled by F_{CUTS} terminal. Please refer to the following chart.

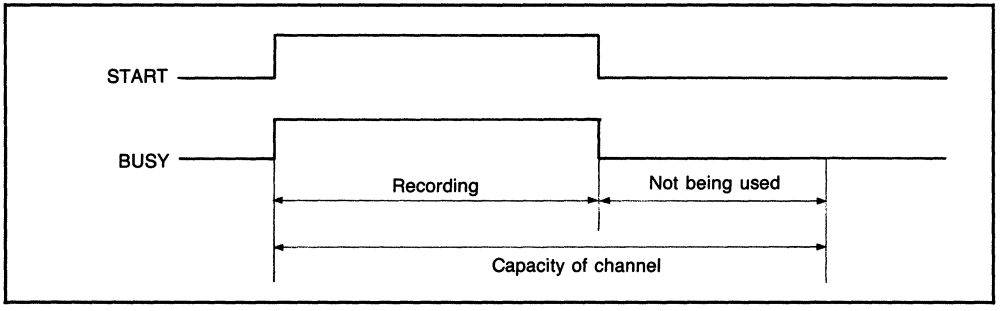
Voice Sampling		F_{CUTS}	
SAM	VCK (Hz)	"H"	"L"
L	4 K	2.3 K	1.95 K
H	8 K	3.8 K	2.9 K

When oscillation frequency is 4.096 kHz.

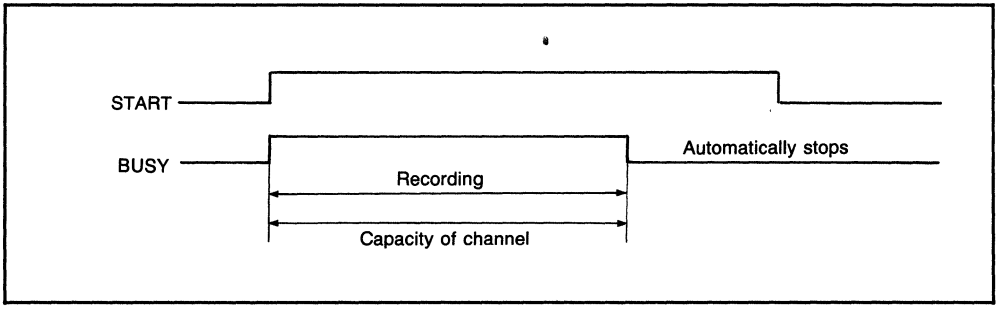
4. Function of REC/$\overline{\text{PLAY}}$ and Start Terminals

RECORDING

1. REC/$\overline{\text{PLAY}}$ = "H" When Recording Using Partial Memory Capacity of the Channel

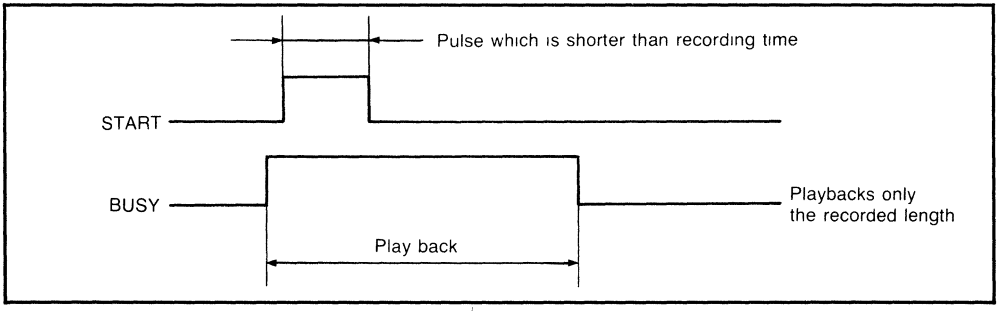


2. REC/$\overline{\text{PLAY}}$ = "H" When Recording Using Entire Memory Capacity of the Channel

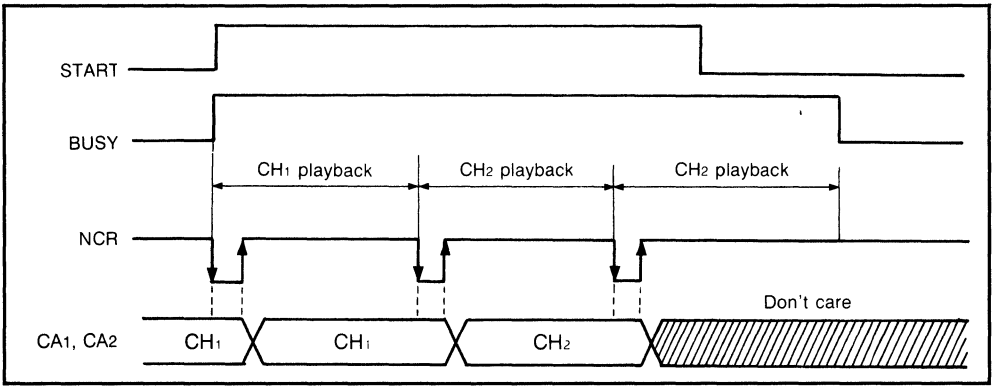


PLAYBACK

3. REC/$\overline{\text{PLAY}}$ = "L" to Playback the Recorded Contents Once



4. REC/$\overline{\text{PLAY}}$ = "L" to Playback the Recorded Content Repeatedly and Continuously



Continuous playback and repeated playback are made by maintaining start terminal at "H" level. Writing channel is done when NCR falls down, or the time when starts playbacking each word. So, changing channel is made by turning it with the time when NCR stands up.

5. Interval of Recording Time

As described up to now, by maintaning REC/$\overline{\text{PLAY}}$ terminal high, recording is made for the length of time the start terminal is high. Strictly speaking, recording time could be longer by the reason of the fact that the interval of recording time is for 4K bits.
The interval of recording time can be figured out by the following formula.

(The step of recording time) = 4K bit/(bit rate [K bit/sec])[sec]

EXAMPLE

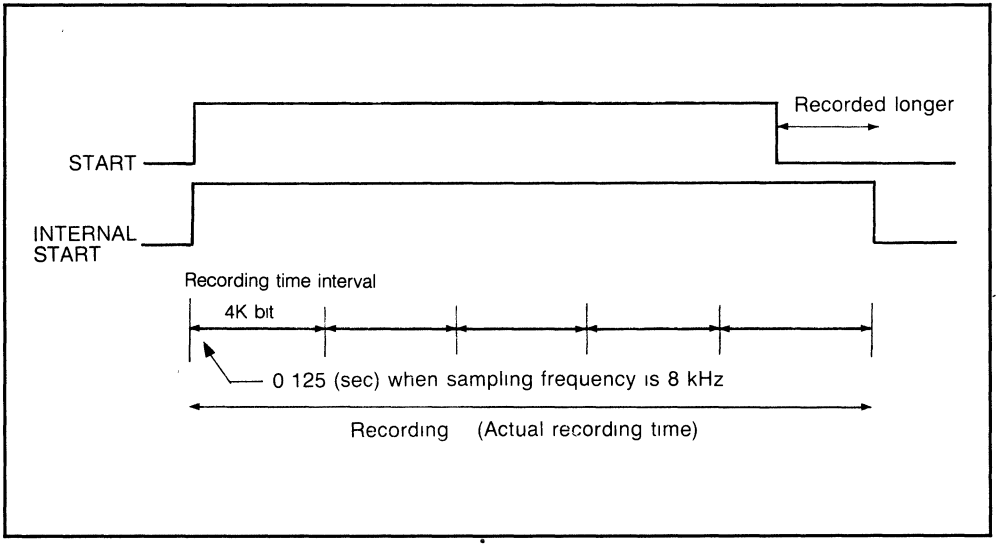
When sampling frequency is 8 kHz, bit rate is

4 bit × 8 kHz = 32K bit/sec.

The step of recording time is

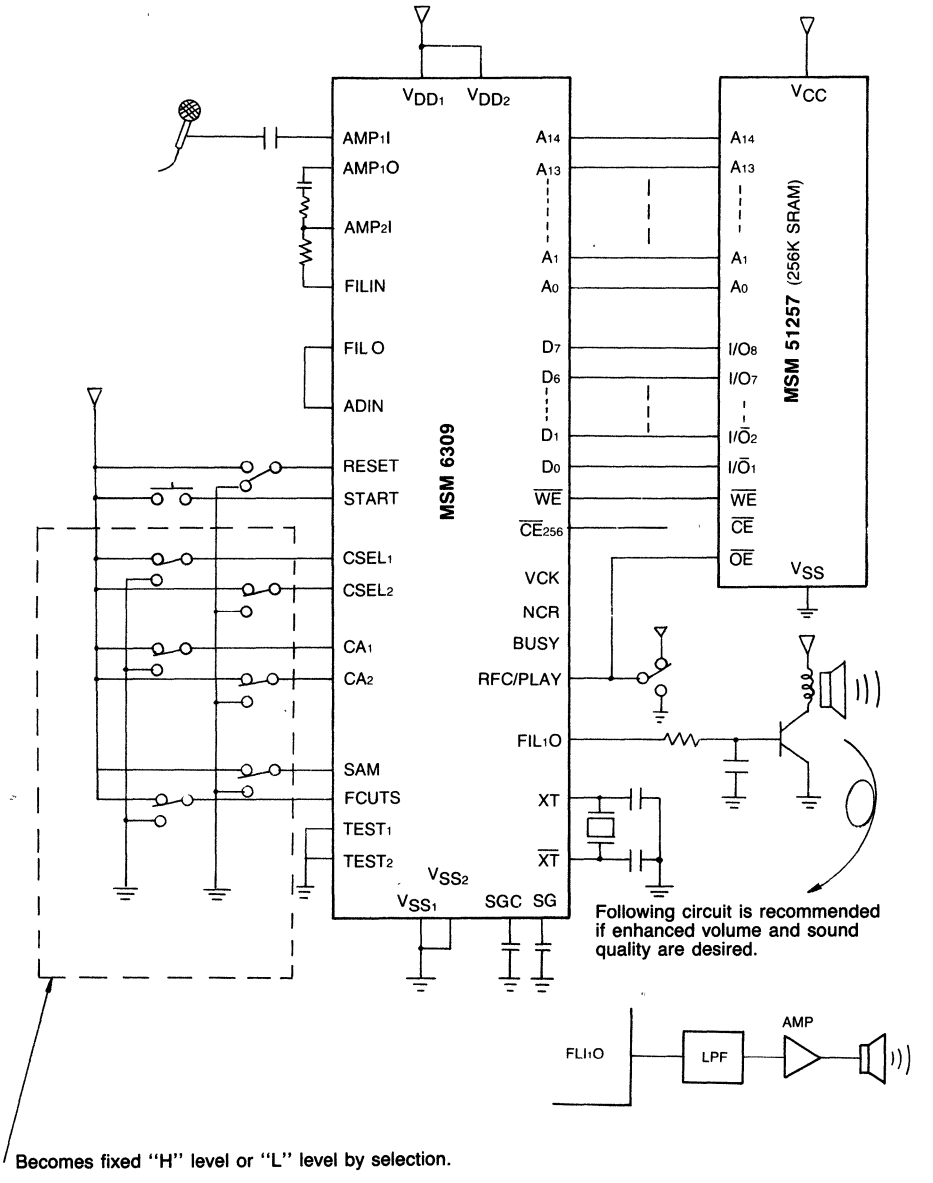
4 bit/32K bit/sec = 0.125 (sec)

So, the recording time becomes 0.125 msec longer at most.



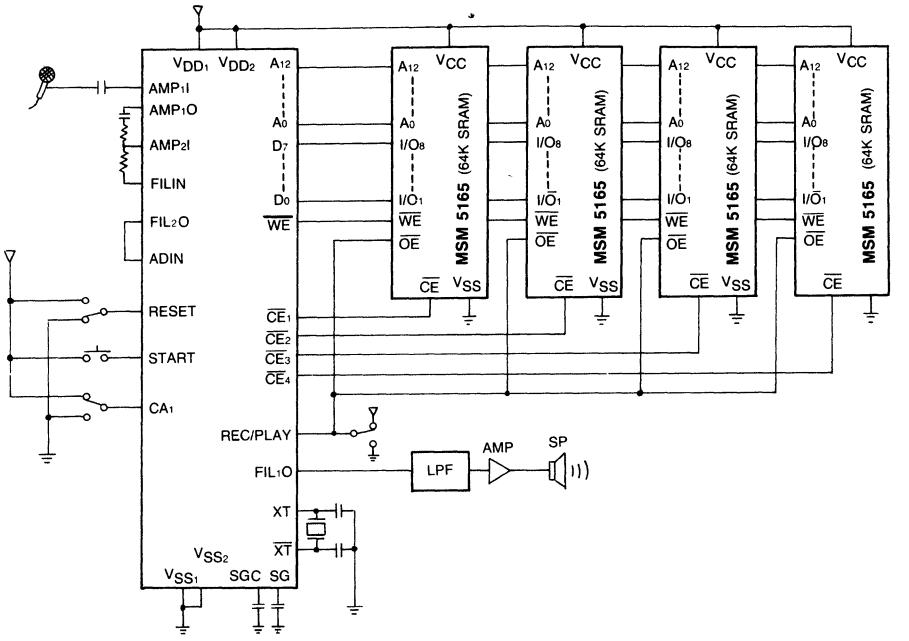
APPLICATION CIRCUIT I

Interface with a single 256K SRAM



APPLICATION CIRCUIT II

Interface with 4 64K SRAMs



MSM6258/MSM6258V

ADPCM SPEECH PROCESSOR FOR SOLID STATE RECORDER

GENERAL DESCRIPTION

The MSM6258 is a complex and highly integrated ADPCM speech processor, implemented in CMOS technology for low power consumption. The integrated AD and DA converters make the chip more self-contained, relieving the need of an external conversion circuitry. The device comprises internally a DRAM controller permitting the use of DRAMs alternatively to SRAMs and ROMs to store speech data. In other words, less periphery, thus less system vulnarability. A voice detector circuit and a phrase select provision are succesfully added features for more performance.

The ADPCM analysis and synthesis block is identical to the popular OKI MSM5218, that is, the bit overflow protection is included in the interest of improved reproduction quality. The device is offered in two basic versions, each of which comes in two package types. One is the version designed to be interfaced with an 8-bit CPU like the OKI MSM80C85, and comes in a 40-pin DIP or in a 44-pin flat package; the other operates as a stand-alone solution that includes 19 pin-programmable output lines for memory addressing and chip select in a 60-pin flat package or in a 68-pin PLCC, respectively, to permit fully surface mount implementation.

MSM6258 accepts 4 to 8MHz master clocks, out of which two sets of sampling frequencies can be derived. Additionally, the ADPCM bit number is pin-selectable between three or four bits per sample. When using 256k or 1Mb DRAMs, the maximum I/O time is approximately 17 minutes at a bit-rate of 16kbit/s, while 256k SRAMs offer a little more than a minute of speech, both in their maximum memory configurations. At the higher bit-rates, 21.2 and 32 kb/s, the I/O times are reduced proportionally.

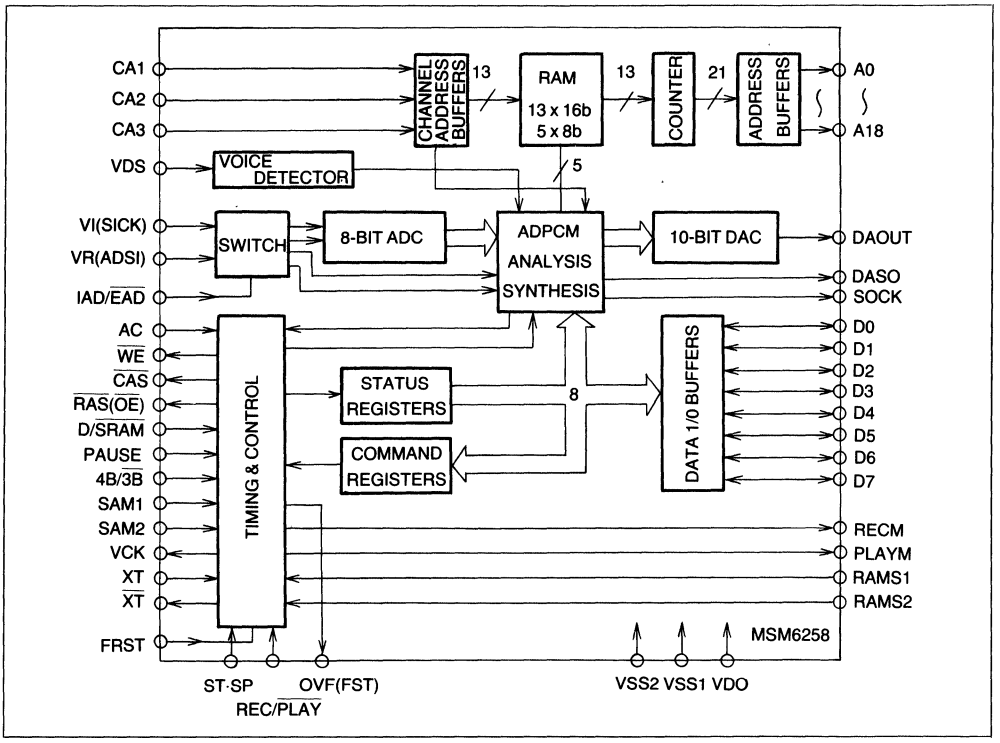
In case of DRAMs, the OKI MSC2304 (2-Megabit module) or MSC2305 (4-Megabit module) are recommendable for space and cost saving benefits and in the interest of simplified handling. In the external mode, the built-in 8-bit ADC is looped in that a separate ADC can be connected to MSM6258, while the accuracy may be between 8 to 12 bits for 'recording' speech. When the playback mode is set, the internal 10-bit DAC will be disabled to permit the connection of an external device at 10 to 12 bits of resolution.

FEATURES

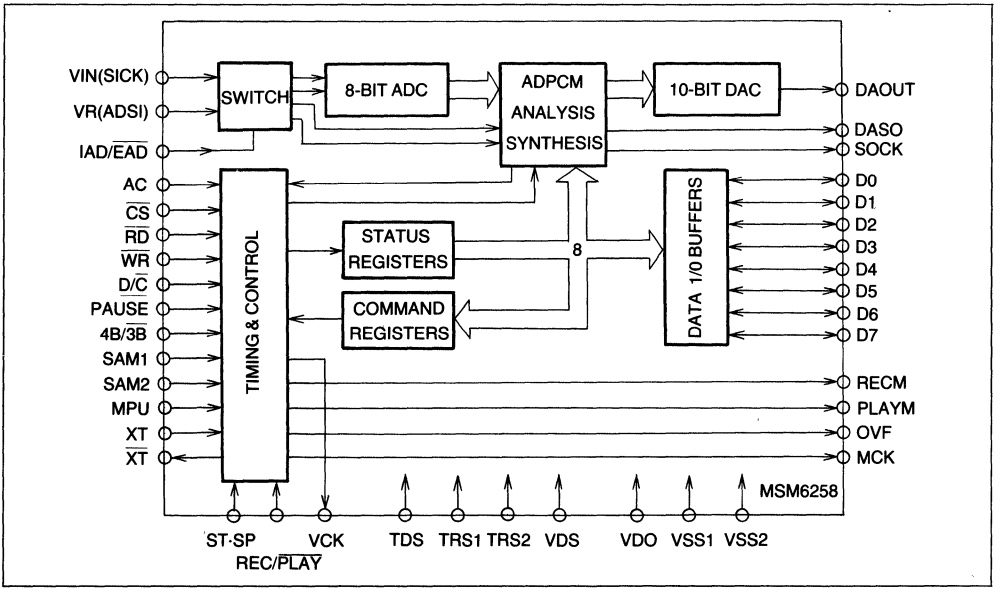
- On chip analog I/O circuits: 8-bit ADC and 10-bit DAC
- ADC and DAC can be looped to connect external devices
- External conversion from 8 to 12 bits
- Analog or PCM data input
- Analog or PCM data output
- Selectable voice detector function
- On-chip complex memory timing & control
- SRAM interface: 64 to 256kbit (128kbyte max)
- Power-down mode possible with SRAM interface
- DRAM interface: 64K to 1Mbit (2Mbyte max)
- Internal DRAM controller/refresh circuit
- Playback from programmed EPROMs
- Master clock 4 to 8MHz (typically 4.096MHz)
- Sampling frequencies 4.0, 5.3, and 8.0kHz @4.096MHz clock
- Selectable ADPCM bit numbers: 3 or 4-bit
- Recording and playback monitor outputs
- Momentary pause function during recording and playback
- 7 phrase channels with individual length
- Two versions: For stand-alone operation
  For CPU interface (8-bit)
- Four packaging options for flexible device mounting
- Single power supply +5Volts (10%)
- Current comsumption: 4mA (@4.096MHz)
  10uA during standby
  (SRAM interface)
- Operational temperature −40 to +85°C (Stand-alone version)
- Operational temperature −40 to +85°C (MPU I/F version)
- Stand-alone version
  60 pin plastic FLAT
  68 pin PLCC (upon request only)
- MPU interface version
  44 pin plastic FLAT
  40 pin plastic DIP

BLOCK DIAGRAMS

A. STAND-ALONE VERSION



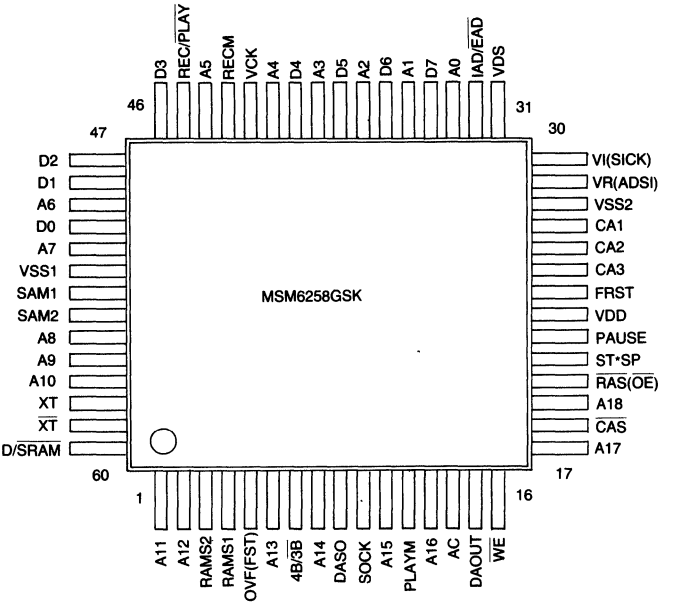
B. MPU INTERFACE VERSION



PIN CONFIGURATION

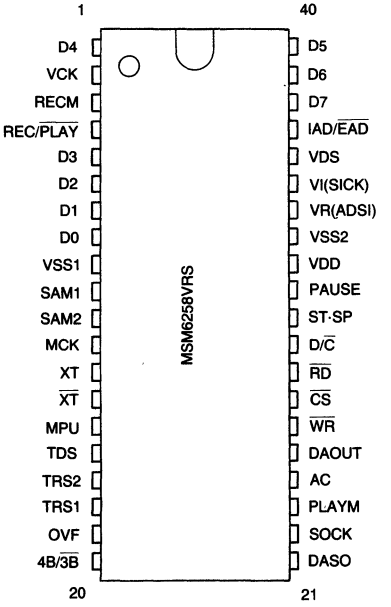
Stand-Alone version MSM6258GSK (GS-K)

60-LEAD PLASTIC FLAT PACKAGE (bottom)



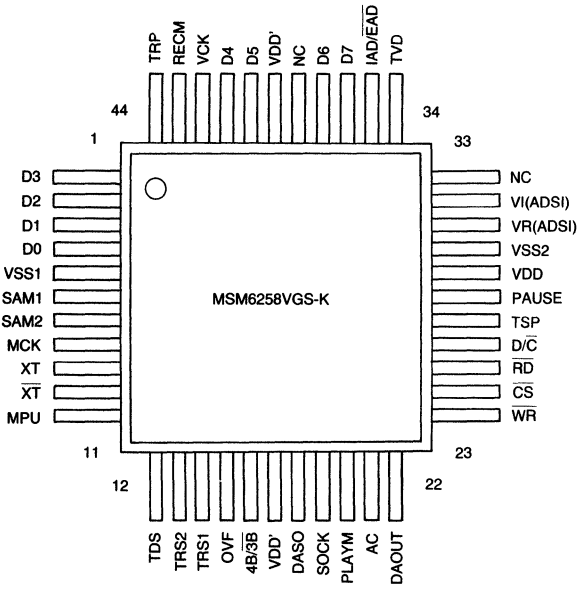
MPU interface version MSM6258VRS

40-LEAD PLASTIC DUAL-IN-LINE PACKAGE (top)



MPU interface version MSM6258VGS (GS-K)

44-LEAD PLASTIC FLAT PACKAGE (top)



Note: Since 17, 39 pin (VDD') is substrate continuity, short-circuits with VDD in the outside.

ABSOLUTE MAXIMUM RATINGS

STAND-ALONE & MPU interface version

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 to 7.0	Volts
Input voltage	V_I	Ta = 25°C	−0.3 to VDD+0.3	Volts
Storage temperature	T_{stg}	—/—	−55 to +150°C	deg C
Maximum permissable loss	P_d	—/—	1	Watt

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Power supply voltage	V_{DD}	—/—	3.5 to 6.0	Volts
Ambient range	T_{op}	—/—	−40 to +85	deg C
Oscillation frequency	f_{OSC}	—/—	4 to 8	MHz

DC CHARACTERISTICS

(V_{DD} = 5V/10%, Ta = −40 TO +85°C) STAND-ALONE VERSION

(V_{DD} = 5V/10%, Ta = −30 TO +70°C) MPU I/F VERSION

PARAMETER	SYMB	CONDITIONS	MIN	MAX	UNIT
Operating current	I_{DD}	@4MHz		4	mA
Stand by current	I_{DS}	With SRAM, AC = H		10	μA
H input voltage	V_{IH1}			3.6	V
H input voltage (Note 1)	V_{IH2}		0.8 x VDD		V
L input voltage	V_{IL}			0.8	V
H output voltage	V_{OH}	IOH= −40μA	4.2		V
L output voltage	V_{OL}	IOL= 2mA		0.45	V
H input current	I_{IH1}	Without pull down VIH = VDD		10	μA
H input current (Note 2)	I_{IH2}	With pull down VIH = VDD	20	400	μA
L input current	I_{IL}	VIL = OV	−10	5	μA
Output leakage current	I_{LO}	OV < VO < VDD	−10	10	μA
DA-output relative error	V_{DAE}	No-load		40	mV
AD conversion precision	V_{ADE}	VSS1 = VSS2 = OV VR = VDD	−1	40	mV
AD S/N ratio* Int ADC selected	S_{N1}	VR = VDD VSS1 = VSS2 = OV		42	dB
AD S/N ratio* Ext ADC connected	S_{N2}	12-Bit, full scale VSS1 = VSS2 = OV		66	dB
DA output impedance	R_{DA}		12	22	kOhms
VR input impedance	R_{VR}			35typ	kOhms
VR input voltage	V_{VR}		0.9 x VDD	VDD	V
VI input voltage	V_{VI}		0	V_{VR}	V
VI input impedance	R_{VI}		10		kOhms

* S/N = (n − 1) x 6
n = ADC bit number

NOTE 1: Applies to XT
NOTE 2: Applies to ST/SP and PAUSE and MPU

PIN FUNCTIONAL DESCRIPTION

PIN NAME	TERMINAL NUMBER				I/O	LSI VERSION	
	40DIP	44FLT	60FLT	68PLCC		SA	MPU
IAD/$\overline{\text{EAD}}$	37	35	32	62	I	○	○

In the recording (analysis) mode, this pin selects either the internal ADC or an externally connected converter.
"H" = internal, "L" = external.

VI (SICK)	35	32	30	60	I	○	○

If the internal ADC is selected (IAD/$\overline{\text{EAD}}$ = H), the analog signal coming from a pre-amplifier/low pass filter configuration can be input through this terminal.
If an external ADC is selected (IAD/$\overline{\text{EAD}}$ = L), the PCM data clock can be input here.
SICK = [S]erial [I]nput [C]loc[k], as in the case of MSM5218.

VR (ADSI)	34	31	29	59	I	○	○

If the internal ADC is selected (IAD/$\overline{\text{EAD}}$ = H), this pin accepts the reference voltage for the internal converter. Nominally, the reference voltage is VDD. thus derivale from the power supply rail.
In the external ADC mode (IAD/$\overline{\text{EAD}}$ = L), this pin functions as the imput for PCM data.
ADSI = [A]nalogue/[D]igital [S]erial [I]n, as in the case of MSM5218.

SOCK	22	19	10	38	O	○	○

The terminal provides the serial output clock to shift out the PCM data available at DASO.

DASO	21	18	9	37	O	○	○

The recuperated PCM data is output here in the record and the playback (synthesis) mode.
DASO = [D]igital/[A]nalogue [S]erial [O]ut.

DAOUT	25	22	15	43	O	○	○

Voice signal output terminal. DAOUT provides ground level during stand by (AC = H), in order to minimize the current through an eventual transistor amplifier stage. Note, that a "pop" noise appears when the level goes to ground. In case of the SA version, when AC is changed from H to L, DAOUT raises from GND to VDD/2 within 16 msec. In case of the MPU version, when recording or playback is suspended by stop command, this terminal maintains the level when suspended. By start command, recording or playback is started. At the same time this terminal changes 1/2 VDD level. During recording (analysis), this terminal monitors the analog input with a slight delay, being useful to measure with a scope in real time.

PIN FUNCTIONAL DESCRIPTION, continued

PIN NAME	TERMINAL NUMBER				I/O	LSI VERSION	
	40DIP	44FLT	60FLT	68PLCC		SA	MPU
AC	24	21	14	42	I	○	○

A "H" level applied to this pin initializes the entire internal circuitry (reset function), and causes the DAOUT output to return to ground level. MSM 6258 provides power-on reset, setting AC initially H.

SAM1	10	6	53	18	I	○	○
SAM2	11	7	54	19	I	○	○

The logic levels on these two pins determine the sampling frequency as follows:

SAM1	SAM2	SAMPLING FREQUENCY	@fosc = 4.096MHz
L	L	fs1 = fosc/1024	4.0 kHz
H	L	fs2 = fosc/768	5.3 kHz
L	H	fs3 = fosc/512	8.0 kHz
H	H	invalid	invalid

The maximum recording playback times are calculated by:

$$t = \frac{\text{disposable memory capacity [kbit]}}{\text{fsample x ADPCM bit number [kb/s]}} \text{ [sec]}$$

VCK	2	42	42	5	O	○	○

Outputs the sampling frequency (Voice Clock) selected at SAM1 and SAM2 for further control tasks to peripheral circuits, if required. The duty ratio is 50%, while VCK is output during AC = L, when interfaced with DRAMs and the MPU version. When the SA version is interfaced with SRAM, VCK is output during recording and playback and not during standby. During AC = H, VCLK is ϕ.

PLAYM	23	20	12	40	O	○	○

During the activated playback (synthesis) state, this pin outputs an "H" level for the duration of the operation. During recording (analysis), a "L" is provided.

RECM	3	43	43	6	O	○	○

This terminal outputs L, H, or a 2 Hz pulse depending on the state of operation:

1. During playback = L
2. Stand by during recording = L
3. During recording = H
4. During pause or voice detection = 2 Hz pulse

REC/$\overline{\text{PLAY}}$	–	–	45	8	I	○	X

Selects recording (analysis) or playback mode (synthesis). "H" = recording, "L" = playback.

PIN FUNCTIONAL DESCRIPTION, continued

PIN NAME	TERMINAL NUMBER				I/O	LSI VERSION	
	40DIP	44FLT	60FLT	68PLCC		SA	MPU
OVF(FST)	19	15	5	32	O	○	○

1. OVERFLOW INDICATOR. During recording and playback, an H is output if frequency of waveform exceeds 80% of dinamic range.

2. FLAG STATUS INDICATOR. This is a monitor output related to the phrase channels, operable in stand by only. If a selected channel does not contain voice data, an L is output. If data is present, an H is provided. Since the MPU I/F version omits the phrase channels, this function applies to the stand-alone version exclusively.

D/$\overline{\text{SRAM}}$	–	–	60	27	I	○	X

Selects the DRAM or SRAM interface. "H" = DRAM, "L" = SRAM (EPROM).

$\overline{\text{RAS}}$($\overline{\text{OE}}$)	–	–	20	48	O	○	X

This is the Row Address Strobe signal for the DRAM interface (D/$\overline{\text{SRAM}}$ = H), or the Output Enable signal for the SRAM interface (D/$\overline{\text{SRAM}}$ = L).

$\overline{\text{CAS}}$	–	–	18	46	O	○	X

CAS on MSM6258 is output monitor pin for column address strobe timing. Please do not connect the CAS pin of DRAM directly to this pin. Only high order address bits are connected to DRAM CAS signal.

$\overline{\text{WE}}$	–	–	16	44	O	○	X

Provides the Write Enable signal either to the DRAM or to the SRAM memories.

VDS	–	–	31	61	I	○	X

The level at this pin selects or deselects the Voice Detector Function, "H" = on, "L" = off. The voice detector may be compared with an auto-start recording upon detection of a sufficient voice signal level.

FRST	–	–	24	54	I	○	X

Resets the flag of a selected phrase channel when the flag status is H. Only operable during stand by. Also refer to OVF (FST) description.

PIN FUNCTIONAL DESCRIPTION, continued

PIN NAME	TERMINAL NUMBER				I/O	LSI VERSION	
	40DIP	44FLT	60FLT	68PLCC		SA	MPU
D0	8	4	50	15	I/O	○	○
D1	7	3	48	13	I/O	○	○
D2	6	2	47	12	I/O	○	○
D3	5	1	46	10	I/O	○	○
D4	1	41	40	5	I/O	○	○
D5	40	40	38	1	I/O	○	○
D6	39	37	36	66	I/O	○	○
D7	38	36	34	64	I/O	○	○

This bi-directional data bus conveys the ADPCM-coded data to and from the memory. One byte consists of two nibbles in the 4-bit ADPCM data format. Also in case of 3-bit data format two nibbles are presented, but the LSB of each is always externally pulled-down. The MSB of every nibble indicates whether the input waveform is ascending (MSB = 0), or descending (MSB = 1). D0 to D7 output or input a pair of ADPCM nibbles during every sampling period, which is VCK.

The MPU I/F version additionally uses the data bus to call and send command and status data.

ST·SP	–	–	21	50	I	○	X

This is a pulse input commencing START and STOP of either recording or playback. When the LSI is reset, and a pulse applied, recording or playback commerce at the raising edge of this pulse. Any operation is cancelled at the raising edge of another pulse applied to this terminal. In applications, this pin is connected to VDD via a momentary switch. If not, the pulse width should be at least 2usec long. The input is internally pulled-down.

PAUSE	–	–	22	51	I	○	X

When momentarily connected with VDD, the recording or playback operation is temporarily suspended. The input is internally pulled-down.

$\overline{XT}$	14	10	59	25	O	○	○
XT	13	9	58	24	I	○	○

These are the crystal connectors. When the clock is to be applied from an external source, XT is used to input the signal while $\overline{XT}$ remains open.

PIN FUNCTIONAL DESCRIPTION, continued

PIN NAME	TERMINAL NUMBER				I/O	LSI VERSION	
	40DIP	44FLT	60FLT	68PLCC		SA	MPU
RAMS1	–	–	4	31	I	○	X
RAMS2			3	30	I	○	X

In connection with terminal D/S, the logic levels on RAMS1 and RAMS2 (RAM SIZE) determine the type and capacity of the memory chips as follows:

D/$\overline{SRAM}$	RAMS1	RAMS2	MEMORY
H	L	L	64k DRAM (including 41464)
H	H	L	256k DRAM (including 414256)
H	L	H	1Mb DRAM
H	H	H	prohibited
L	L	L	64k SRAM
L	H	L	256k SRAM
L	L	H	A0 TO A18 BINARY
L	H	H	prohibited

4B/$\overline{3B}$	20	16	7	34	I	○	○

The logic levels on this pin determine the ADPCM data format:
"H" = 4-bit ADPCM, "L" = 3-bit ADPCM.

CA1	–	–	27	57	I	○	X
CA2			26	56	I	○	X
CA3			25	55	I	○	X

The address inputs to select the recording and playback phrase channels. Up to 7 channels can be selected, while the code LLL, corresponding to channel 0, is reserved for reading data from EPROMs, or for use of the memory attached without channel separation.
The condition that permits recording on a channel n with FST = L is that the flag of the upper priority channel n-1 is H.
Priorities: CHANNEL 1 > 2 > 3 > 4 > 5 > 6 > 7

CHANNEL	CA1	CA2	CA3
0	L	L	L
1	H	L	L
2	L	H	L
3	H	H	L
4	L	L	H
5	H	L	H
6	L	H	H
7	H	H	H

The MPU I/F version omits the phrase channel provision.

PIN FUNCTIONAL DESCRIPTION, continued

PIN NAME	TERMINAL NUMBER				I/O	LSI VERSION	
	40DIP	44FLT	60FLT	68PLCC		SA	MPU
A0			33	63	O	○	X
A1			35	65	O	○	X
A2			37	67	O	○	X
A3			39	2	O	○	X
A4			41	4	O	○	X
A5			44	7	O	○	X
A6			49	14	O	○	X
A7			51	16	O	○	X
A8			55	20	O	○	X
A9	—	—	56	21	O	○	X
A10			57	23	O	○	X
A11			1	28	O	○	X
A12			2	29	O	○	X
A13			6	33	O	○	X
A14			8	35	O	○	X
A15			11	39	O	○	X
A16			13	41	O	○	X
A17			17	45	O	○	X
A18			19	47	O	○	X

Address outputs to external RAM. Depending on which type of RAM and RAM capacity is used, the bus provides the number of required addresses, while not required lines operate as chip select outputs (Active = 0). In other words, the pins RAMS1 and RAMS2 program the address bus A0 to A18

MEMORY TYPE	ADDRESSES	CHIP SELECT
DRAM 64k	A0 TO A7	A8 TO A18
DRAM 256k	A0 TO A8	A9 TO A16
DRAM 1Mb	A0 TO A9	A10 TO A11
SRAM 64k	A0 TO A12	A13 TO A18
SRAM 256k	A0 TO A14	A15 TO A18

Maximum configuration of memory chips:

MEMORY TYPE	4-BIT ADPCM	3-BIT ADPCM
DRAM 64kx1	11SETS OF 8PCS [88]	11SETS OF 6PCS [66]
DRAM 64kx4	11SETS OF 2PCS [22]	11SETS OF 2PCS [22]
DRAM 256kx1	8SETS OF 8PCS [64]	8SETS OF 6PCS [48]
DRAM 256kX4	8SETS OF 2PCS [16]	8SETS OF 2PCS [16]
DRAM 1Mbx1	2SETS OF 8PCS [16]	2SETS OF 6PCS [12]
SRAM 64k	6 PIECES	6 PIECES
SRAM 256k	4 PIECES	4 PIECES

The MPU I/F version omits the address bus A0 to A18.

PIN FUNCTIONAL DESCRIPTION, continued

PIN NAME	TERMINAL NUMBER				I/O	LSI VERSION	
	40DIP	44FLT	60FLT	68PLCC		SA	MPU
VDD	32	29	23	52	I	○	○

Power supply pin, nominally 5 Volts.

VSS1	9	5	52	17	I	○	○

Digital ground pin, nominally 0 Volts.

VSS2	33	30	28	58	I	○	○

Analog ground pin, nominally 0 Volts.

PIN FUNCTIONAL DESCRIPTION FOR MPU I/F ORIENTED I/Os

PIN NAME	TERMINAL NUMBER				I/O	LSI VERSION	
	40DIP	44FLT	60FLT	68PLCC		SA	MPU
MPU	15	11	–	–	I	X	○

Selects the MPU interface. When H, the internal circuitry is set to communicate with an external CPU. Since the input is internally pulled-down, make sure to apply a H.

$\overline{CS}$	27	23	–	–	I	X	○

A chip select input. When receiving a L, the MSM6258 can communicate with the CPU. When set to H, the data bus goes on high impedance, thus disabling read & write functions.

MCK	12	8	–	–	O	X	○

Synchronization signal to the CPU. During recording and playback, a frequency of fsample/2 is output here.

$\overline{RD}$	28	24	–	46	I	X	○

When this pin is L, the CPU can read the ADPCM coded data or status data of the MSM6258.

$\overline{WR}$	26	25	–	48	I	X	○

At the L to H transition, the CPU can write ADPCM data or command data into the MSM6258.

D/$\overline{C}$	29	26	–	–	I	X	○

When selected H, the data bus provides ADPCM data; when L, command or status data can be accessed.

TDS	16	12			I	X	○
TRS1	17	14			I	X	○
TRS2	18	13	–	–	I	X	○
TSP	30	27			I	X	○
TRP	4	44			I	X	○
TVD	36	34			I	X	○

These are test inputs for factory testing. The three terminals must be grounded during normal operation.

HOW TO CONTROL EXTERNAL ADC & DAC

Internal and external modes are related to signal conversion:

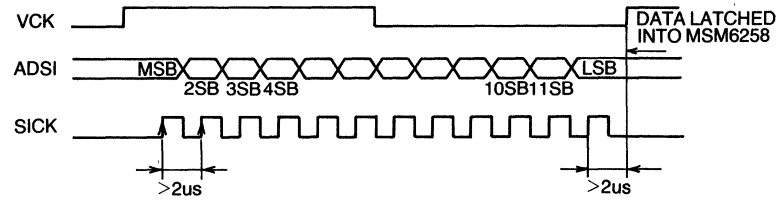
MODE	IAD/$\overline{EAD}$ = H (INTERNAL)	IAD/$\overline{EAD}$ = L (EXTERNAL)
VI(SICK)	VI (Voltage Input)	SICK (Serial Input Clock)
VR(ADSI)	VR (Reference Voltage)	ADSI (Analog/Digital Serial Input)

External DAC

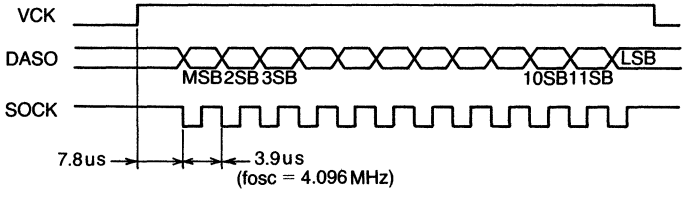
The straight binary (PCM-coded) data is fed into the MSM6258 through terminal ADSI, while the data clock must be applied to SICK. As a result, every bit coming from the external ADC is shifted into the speech chip at the raising edge of every clock-in pulse. In case less than 12 bits are provided, the remaining lower order bits (LSB) must be clocked in as zeros. However, usually an external ADC of more than 8 bits will be employed to boost up the speech quality.

Timing charts (fosc = 4.096MHz)

External Analogue-to-Digital converter



External Digital-to-Analogue Converter



External DAC

During playback, recuperated straight binary PCM coded data is output by terminal DASO, while the data clock is available at SOCK. Every bit of the PCM pulse train is valid upon the falling edge of the clock-out pulses.
The effort that an external DAC involves is worth while only under the condition that an external ADC of a higher resolution than 8 bits is used at the input.
MSM6258 does not accept u-LAW or A-LAW companded PCM data, and also does not satisfy CCITT G.721 recommendation. Therefore, the device cannot fully replace an ADPCM CODEC.

RECORDING INSTRUCTIONS (For Stand-Alone Version)

1. Select the desired sampling frequency at pins SAM1 and SAM2.
2. Set the REC/PLAY pin to "H" to determine the recording mode.
3. Set the phrase select pins CA1 to CA3 in accordance with the channel priority.
4. The flag of the selected channel is output at pin OVF(FST) (Note).
5. Commence recording by pressing the ST·SP momentary button.

NOTE: When the selected channel flag if "H", it is indicated that the channel is already recorded. The available recording time for a new input is identical to the duration of the previous recording length, and ends automatically when the pre-recorded data boundary has been reached, followed by an internal reset.
The ST·SP input has no effect during recording. In other words, the recording operation cannot be suspended intermediately once commenced.

When the selected channel flag is "L", (can also be set to L by applying a H pulse to the input), recording time is freely available until ST·SP is pressed again. However, if the recording merges into another already recorded channel, playback of this intruded channel becomes impossible since its flag is reset (L).

In brief:

	FST=H	FST=L
RECORDING	1	2
PLAYBACK	3	4

1 = The recording time is the same as the previous.
2 = Recording time is variable.
3 = Playback time as previously recorded.
4 = Playback impossible when data from previous channel has merged.

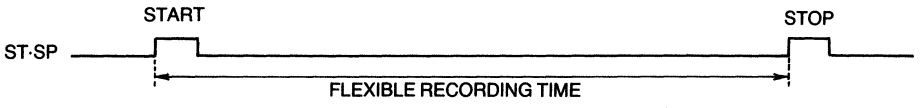
PLAYBACK INSTRUCTIONS

1. Set REC/PLAY to 'L'.
2. Select the desired channel to be reproduced.
3. Make sure that the OVF (FST) pin outputs 'H'. If 'L', playback is not possible (see table above).
4. Input a pulse through ST·SP to commence playback.
5. Playback stops automatically when the time of the recording has elapsed, or can be interrupted any time by another pulse to ST·SP.

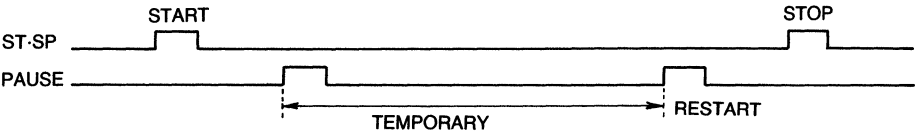
START/STOP/PAUSE TIMINGS

1.) RECORDING (FLAG = L)

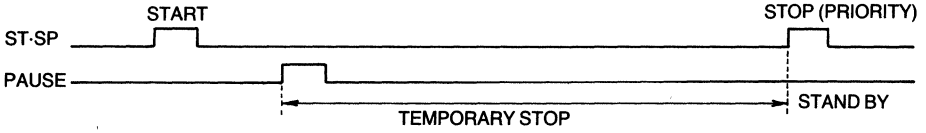
a: START and STOP



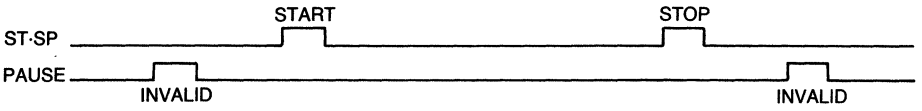
b: TWICE PAUSE DURING OPERATION



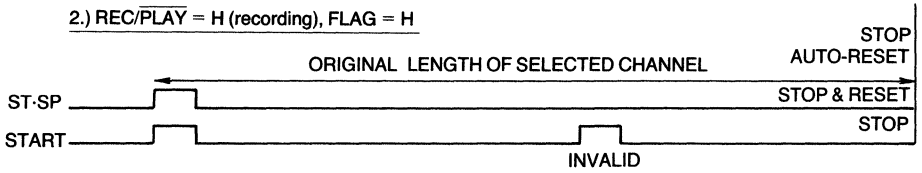
c: ONCE PAUSE DURING OPERATION



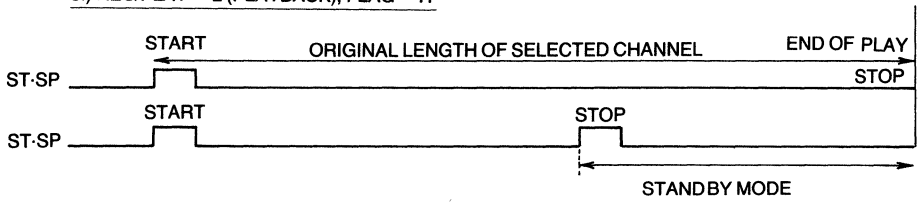
d: PAUSE DURING STAND BY



2.) REC/$\overline{\text{PLAY}}$ = H (recording), FLAG = H



3.) REC/$\overline{\text{PLAY}}$ = L (PLAYBACK), FLAG = H



NOTE: PAUSE timings at 2.) and 3.) are idenfical with 1.) b,c,d.

4) REC/$\overline{\text{PLAY}}$ = L (PLAYBACK), FLAG = L

The LSI is in Stand by condition,
and does not permit playback.

POWER-DOWN REDUCTION MODE

During stand by, the internal oscillation circuit automatically stops the operation and validates the power-saving mode. This mode can be entered under the condition that the SRAM interface is set (D/S = L).When the master clock is 4.096MHz, the start-up period after cancellation of the power-saving mode by a START pulse lasts 20 to 30 ms until the oscillator stabilizes.

HOW TO USE PHRASE CHANNEL "0" (Stand-Alone Version)

[1]. Phrase channel "0" is effective for reading EPROM resident ADPCM coded speech data into the MSM6258. The EPROMs may have been programmed previously by a SAS1A or AW101 development system.
When channel "0" is selected (CA1 to CA3 = L L L), all address outputs from A0 to A18 are initialized to all "0", and commence counting up the binary addresses upon receipt of a pulse to the START input. Condition: RAMS1 = L, RAMS2 = H, D/$\overline{\text{SRAM}}$ = L; refer to pin descriptions. Playback of certain words or word groups can be implemented by external individual control of the CE inputs of the EPROMs. However, this demands adequate editing of speech data prior to writing the EPROMs. In the interest of best reproduction, the MSM6258 should be set at the same sampling rate at which the data was recorded and stored in the memories.
When channel "0" is selected VDS (voice detector) input goes to L.

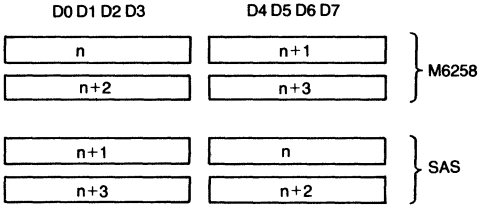
PLAYBACK INSTRUCTIONS:

a. Set "REC/PLAY" to "L".
b. Select channel 0 by setting CA1 to CA3 to "L L L".
c. Make sure that "OVF/FST" output is H, otherwise playback is impossible. If necessary, reset the chip.
d. Apply a pulse to "ST·SP", and playback commences.
e. Suspend playback with another pulse to START/STOP.

[2]. When DRAM or SRAM memories are interfaced with MSM6258, the selection of channel 0 gives the user the totally available memory area without channel separations.

SPEECH DEVELOPMENT SYSTEMS

Right top: SAS1A records, replays, edits speech data, and writes ADPCM coded data into 64 to 128k EPROMs. It also copies written EPROMs. A microphone and a line input are provided.
Right bottom: The latest development system AW101 performs the same functions as SAS1A, but can be linked with a floppy drive, and has a HEX keyboard for comfortable operation. It writes EPROMs from 64k to 512k.



SWITCHING CHARACTERISTICS

MPU I/F VERSION
(VDD =4.5V to 5.5V, Ta = −40 to +85°C, fosc = 4.096MHz, fsample = 8.0kHz)

PARAMETER		SYMB	MIN	TYP	MAX	UNIT
VCK high period	note 1	tVH	–	1/fs x 0.5	–	μs
VCK low period	note 1	tVL	–	1/fs x 0.5	–	us
MCK high period	note 2	tMH	–	39.1	–	μs
MCK low period	note 3	tML	–	210.9	–	μs
VCK raise to MCK raise time	note 2	tVM	–	19.5	–	μs
Set up time in respect to MCK fall (when reading ADPCM data)	note 2	tRMS	15	–	–	μs
Hold time in respect to MCK fall (when reading ADPCM data)	note 2	tRMH	55	–	–	μs
Set up time in respect to MCK fall (when writing ADPCM data)	note 2	tWMS	70	–	–	μs
Hold time in respect to MCK fall (when writing ADPCM data)	note 2	tWMH	2	–	–	μs
RD pulse width		tRR	250	–	–	ns
D/C set up time in respect to $\overline{RD}$ fall		tDCR	50	–		ns
D/C hold time in respect to RD raise		tRDC	100	–	–	ns
CS set up / hold time in respect to $\overline{RD}$		tCR	50	–		ns
Data stabilization time after $\overline{RD}$ fall		tDRE	–	–	200	ns
Data floating time after $\overline{RD}$ raise		tDRF	10	–	200	ns
$\overline{WR}$ pulse width		tWW	250	–	–	ns
D/$\overline{C}$ set up time in respect to WR fall		tDCW	50	–	–	ns
D/$\overline{C}$ hold time in respect to WR raise		tWDC	100	–	–	ns
$\overline{CS}$ set up / hold time in respect to $\overline{WR}$		tCW	50	–	–	ns
Data set up time in respect to $\overline{WR}$ raise		tDWS	100	–	–	ns
Data hold time in respect to $\overline{WR}$ raise		tDWH	150	–	–	ns
AC fall to START command input	note 2	tAS	16	–	–	ms
START command input set up time in respect to VCK raise	note 2	tWVS	4	–	120	us
STOP command input hold time in respect to VCK raise	note 2	tWVP	4	–	120	μs
VCK fall to RECM raise		tVRR	0	–	2	μs
VCK fall to RECM fall		tVRF	0	–	2	μs
AC fall to DAOUT = 1/2VDD	note 2	tDAS	–	15.6	–	ms
START command input to PLAYM raise		tWPR	0	–	4	μs
STOP command input to PLAYM fall	note 2	tWPF	0	–	2	μs
Time from STOP command input to START command input	note 1	tspt	260	—	—	μs

NOTES:

1.) Directly proportional to fsamp

2.) Directly proportional to fosc

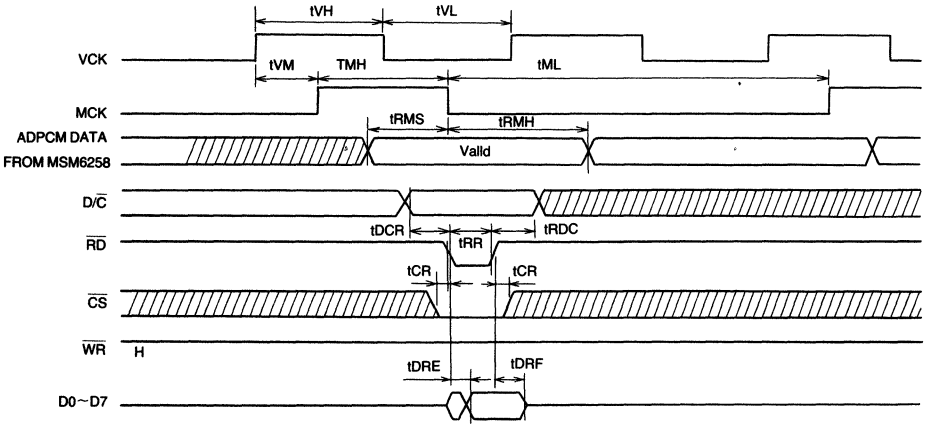
3.) Sampling frequency x 2 − tMH

STAND-ALONE VERSION
(VDD =4.5V to 5.5V, Ta = −40 to +85°C, fosc 4.096MHz, fsample = 8.0kHz)

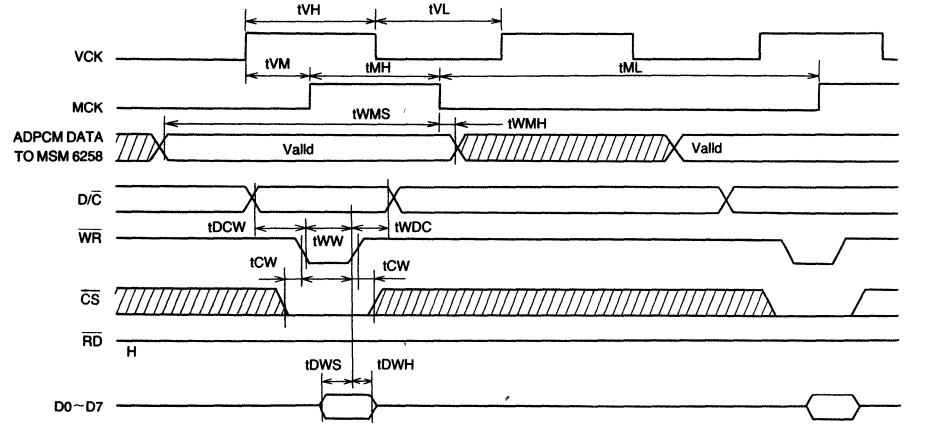
PARAMETER	SYMB	MIN	TYP	MAX	UNIT
AC pulse width	tACP	2.0	–	–	μs
ST·SP pulse width	tSTP	2.0	–	–	μs
PAUSE pulse width	tPAP	2.0	–	–	μs
FRST pulse width	tFRP	2.0	–	–	μs
ST·SP input to RECM raise (DRAM I/F)	tDRR	–	16.3	–	ms
Oscillation start to RECM raise (SRAM)	tSRR	50.2	–	70	ms
Oscillation start to DAOUT active (SRAM)	tXDS	–	40	–	ms
STOP input to RECM fall	tSRF	0	–	32	ms
VSS to 1/2VDD transition time at DAOUT	tDAR	–	16	–	ms
RECM/PLAYM "L" to DAOUT = VSS	tDAF	0	16	32	ms
START pulse input to PLAYM raise	tSPR	0	–	4	μs
STOP pulse input to PLAYM fall	tSPF	0	–	4	μs
PLAYM "L" to next replay START pulse	tPRS	35	–	–	ms

TIMING CHARTS

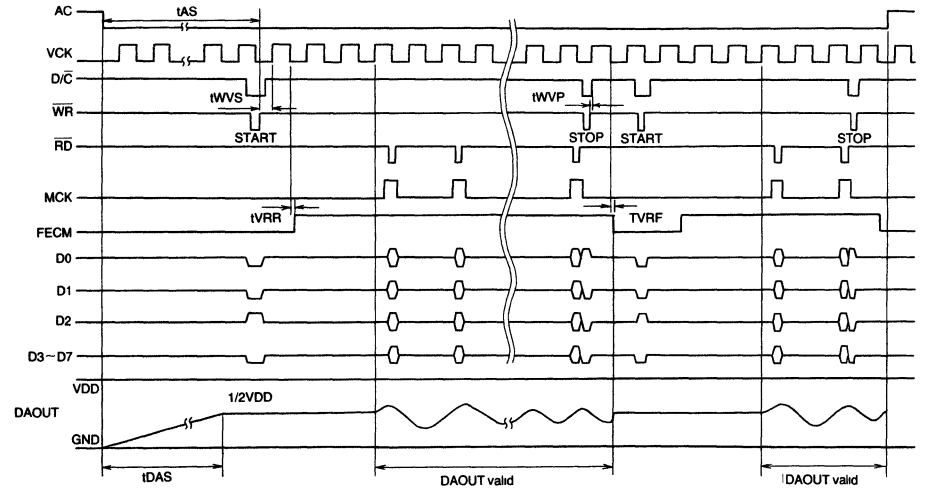
MPU interface version



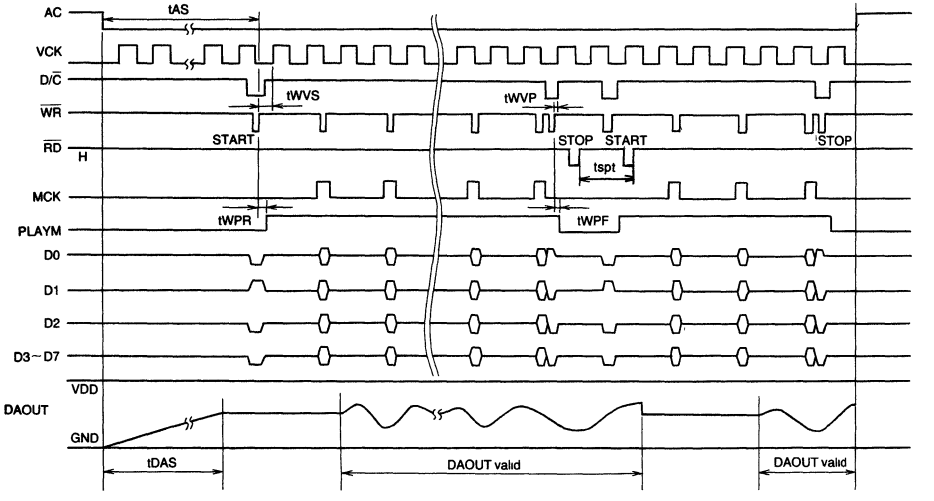
READ TIMING (recording or status data output)



WRITE TIMING (playback or command data input)



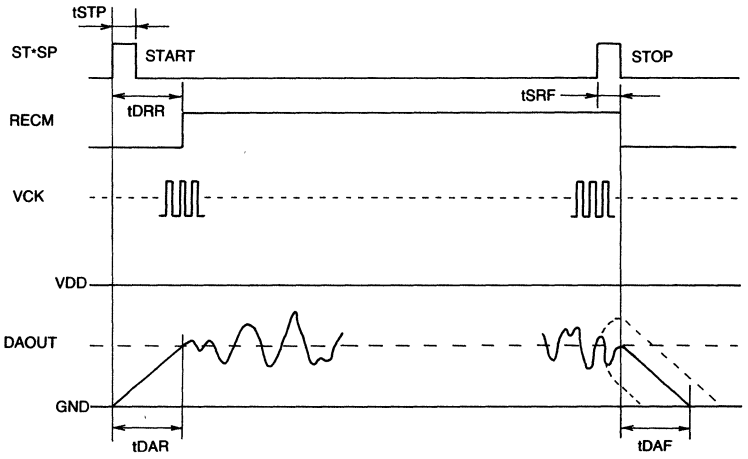
RECORDING TIMING



PLAYBACK TIMING

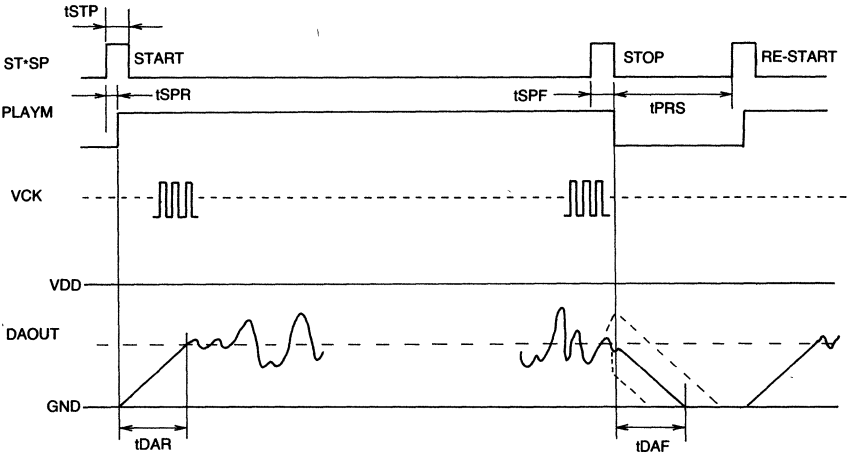
Stand-alone version

1.Recording Timing, DRAM I/F, VDS = "L"

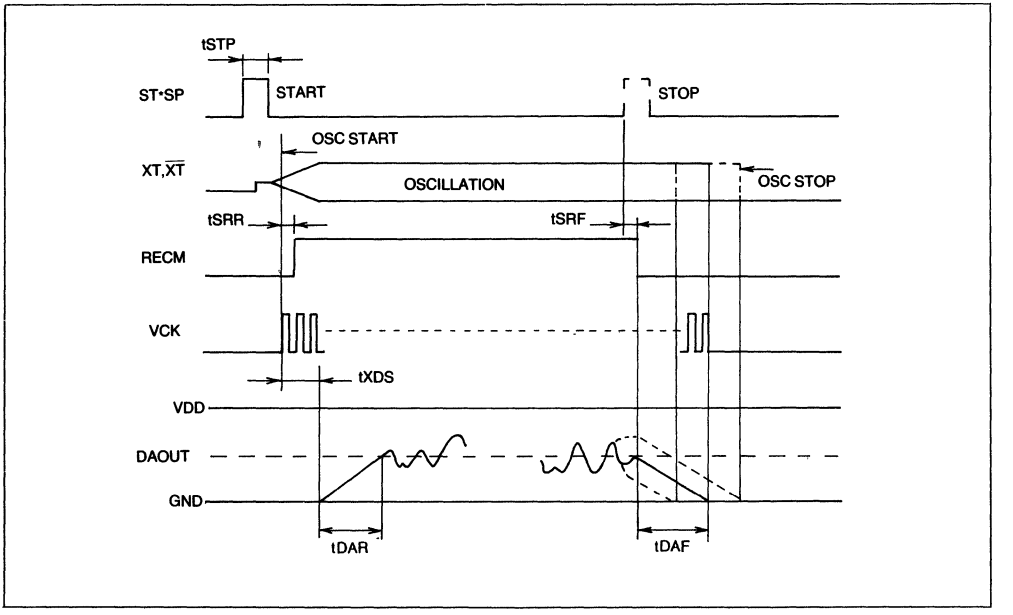


NOTE: When "VDS" is H, the pin RECM outputs a 2-Hz pulse during voice detection.

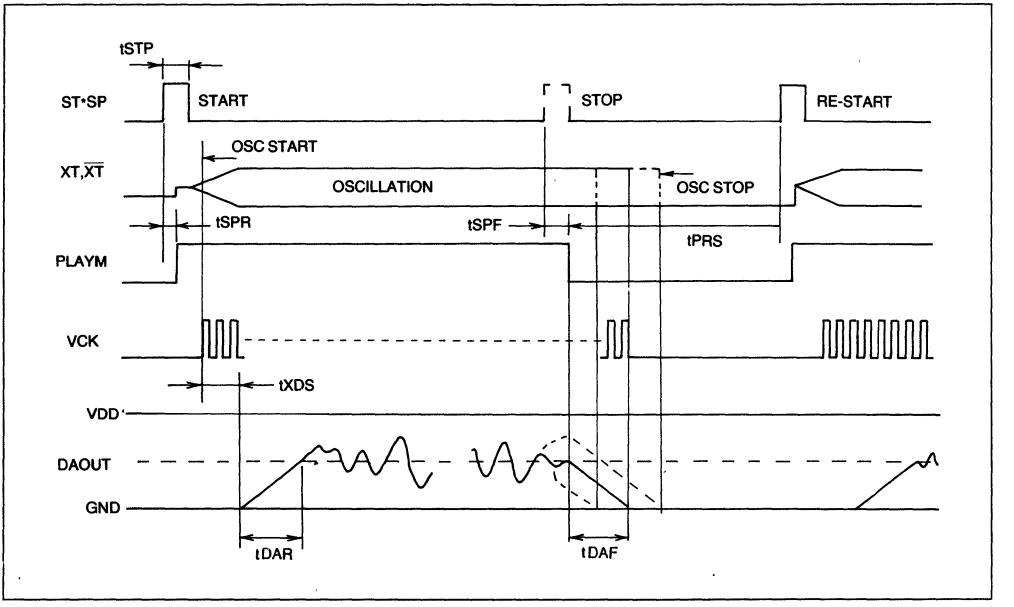
2. Playback Timing (DRAM I/F)



3. Recording Timing, SRAM I/F, VDS = L



4. Playback Timing, SRAM I/F



HOW TO USE THE DATA BUS (MPU I/F Version)

1. The data bus designations are explained by the following table:

$\overline{CS}$	D/$\overline{C}$	RD	$\overline{WR}$	Operation
L	H	L	H	ADPCM data output
L	H	H	L	ADPCM data input
L	L	L	H	Status data output
L	L	H	L	Command data input
H	X	X	X	High impedance

2. ADPCM data composition on the bus:

BUS LINES:	D0	D1	D2	D3	D4	D5	D6	D7
4-BIT ADPCM:	B0n	B1n	B2n	B3n	B0n+1	B1n+1	B2n+1	B3n+1
3-BIT ADPCM:	XX	B0n	B1n	B2n	XX	B0n+1	B1n+1	B2n+1

4-BIT ADPCM
B3 = Sign Bit
B2 = M S B
B1 = 2 S B
B0 = L S B

3-BIT ADPCM
B2 = Sign bit
B1 = M S B
B0 = L S B

Sign bit = 1: Waveform descending
Sign bit = 0: Waveform ascending

3. Command input structure on the data bus:

D0	D1	D2	D3	D4	D5	D6	D7
SP	PLAY ST	REC ST	P4	P3	P2	P1	P0

CONDITION: $\overline{CS}$ = L, D/$\overline{C}$ = L, $\overline{RD}$ = H, $\overline{WR}$ = L

SP: terminates recording or playback
PLAY ST: commences playback
REC ST: commences recording
P0 to P4: set the initialization pointers. (Normaly set to "L")

NOTE: Do not input SP command during PAUSE.

4. Command data direction:

CPU ——command——→ MSM6258

5. Status output structure on the data bus:

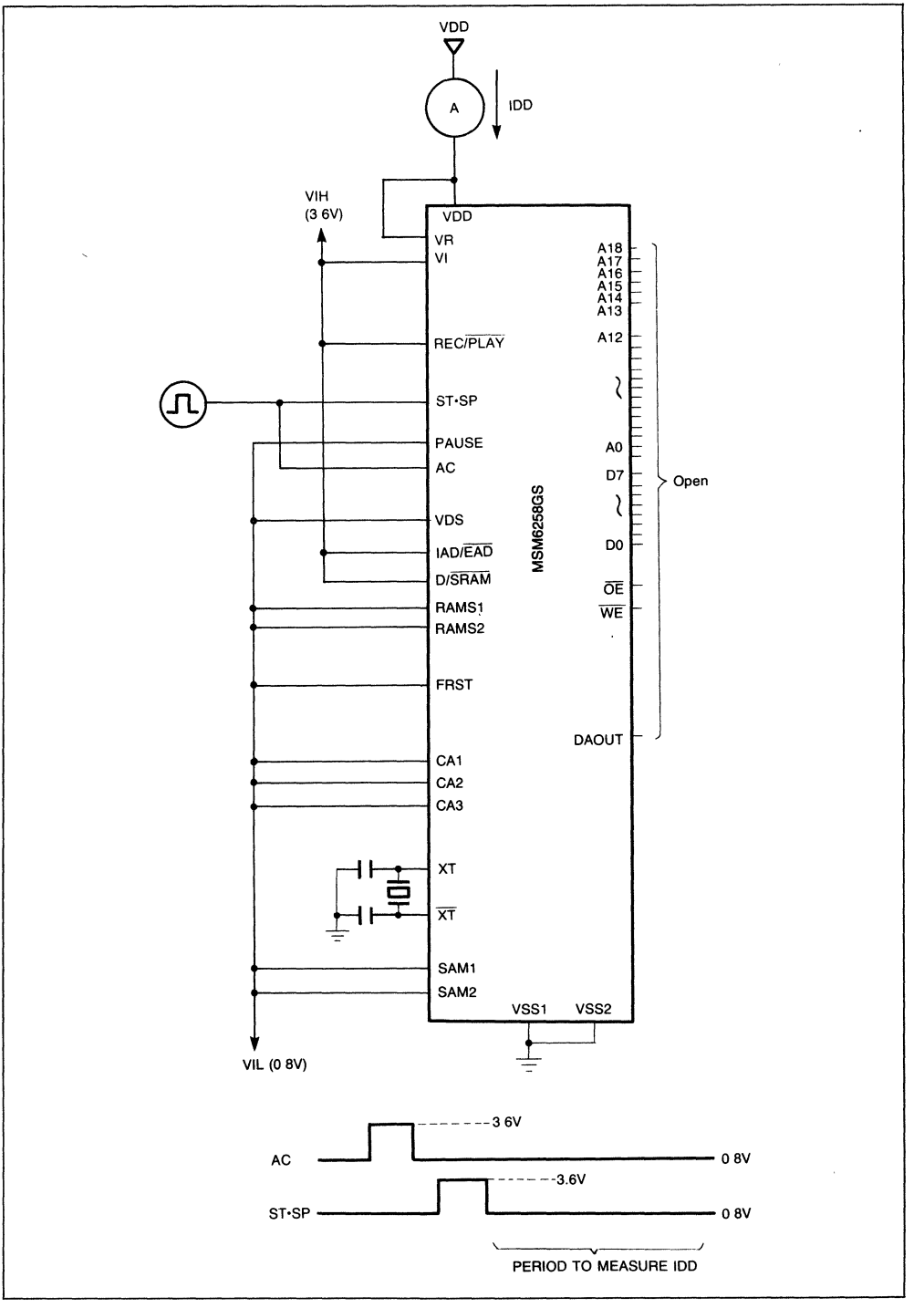
D0	D1	D2	D3	D4	D5	D6	D7
P0	P1	P2	P3	P4	XX	VOICE	REC/ PLAY

CONDITION: $\overline{CS}$ = L, D/$\overline{C}$ = L, $\overline{RD}$ = L, $\overline{WR}$ = L
P0 to P4: set initialization pointers
VOICE: L = mute
H = voice present
REC/PLAY: H = during recording operation
L = during playback operation

6. Status data direction:

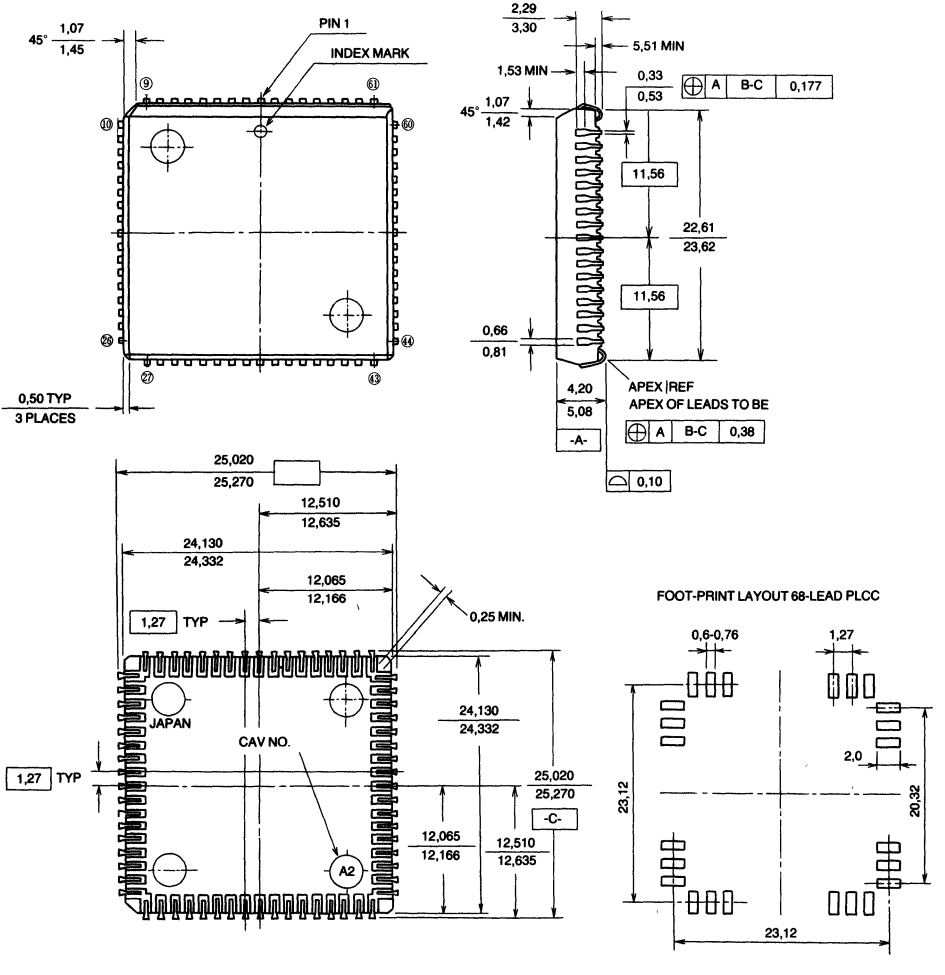
CPU ←——status—— MSM6258

HOW TO MEASURE IDD



PACKAGE DIMENSIONS

68-pin QUAD PLCC (MSM6258JS)



Rth (JA) 53°C/W
Lead frame:Cu|Alloy

ALLDIMENSIONS ARE IN MILLIMETERS MIN. MAX

CONNECTION DIAGRAM AND CONTROL TIMING FOR DRAM

A. How to connect DRAM

The are 5 kinds of DAM's that can be connected to the MSM6258:
64K x 1-bit, 64K x 4-bit, 256K x 1-bit, 256K x 4-bit and 1M x 1-bit.

However plase connect as follows:

Type of ADPCM bit length	Input/Output	X 4-bit DRAM	1-bit DRAM
4-bit	Use pin 8	Every even number	A multiple of 8
3-bit	Use pin 6	—	A multiple of 6

B. DRAM REFRESH — The way to referesh DRAM is by $\overline{RAS}$ only refresh, and so almost all DRAM's can be used with the MSM6258.

The MSM6258 has A0 to A18 address pin and if a specific type of DRAM is selected, upper order address bits (A8 to A11) are used as $\overline{CAS}$ signal. They also play a role of chip select.

DRAM driving timing of selection of 64K DRAM is shown below.
(diagram 1 to 3)

Timing for DRAM memory

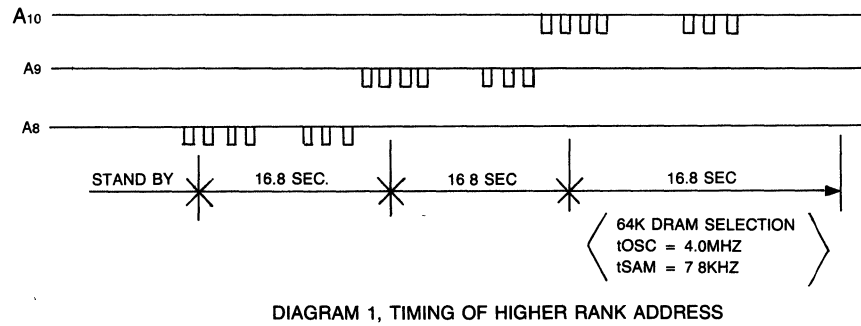


DIAGRAM 1, TIMING OF HIGHER RANK ADDRESS

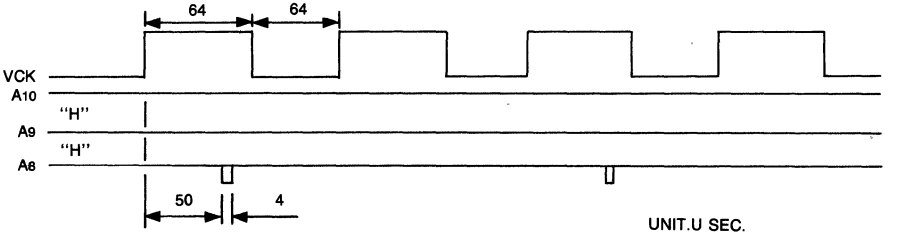


DIAGRAM 2, ENLARGED TIMING OF DIAGRAM 1

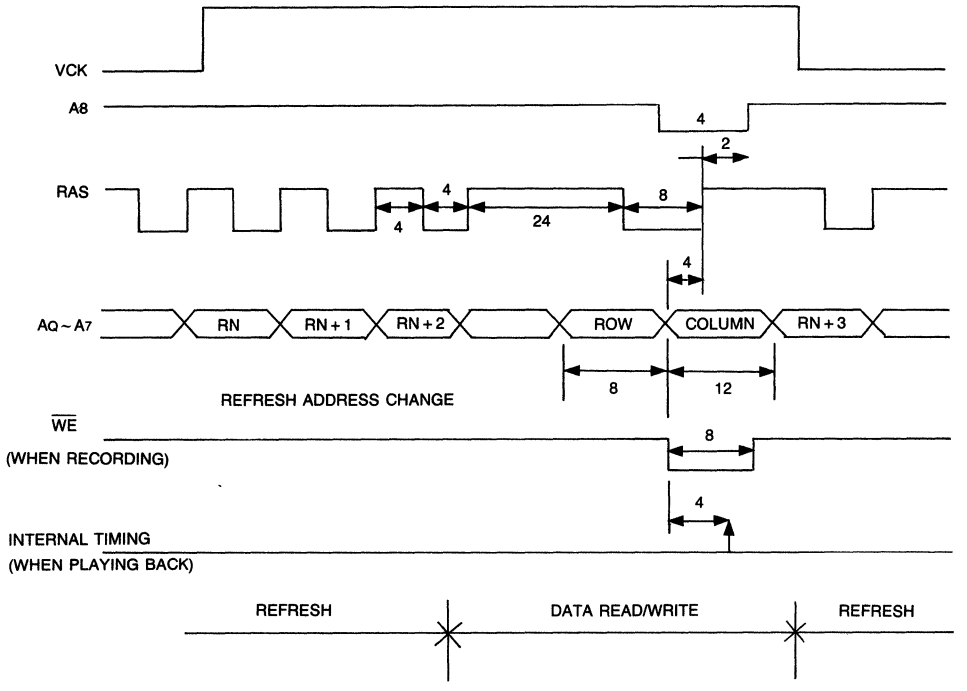


DIAGRAM 3, DATA READ TIMING OF MSM6258

C. RAM selection and DRAM type that can be used.

Following chart shows the combination between DRAM
Type and addresses when D/SRAM terminal is "H" level and DRAM is selected.

RAMS1	RAM2	DRAM Type	Oki's equivalent parts No.	Address Terminal	Chip Select Terminal
L	L	64K × 1-bit	MSM4164	$A_0 \sim A_7$	$A_8 \sim A_{18}$
		64K × 4-bit	MSM41464		
H	L	256K × 1-bit	MSM41256	$A_0 \sim A_8$	$A_9 \sim A_{16}$
		256K × 4-bit	MSM414256		
L	H	1M × 1-bit	MSM411000	$A_0 \sim A_9$	$A_{10} \sim A_{11}$

CONTROL TIMING FOR SRAM

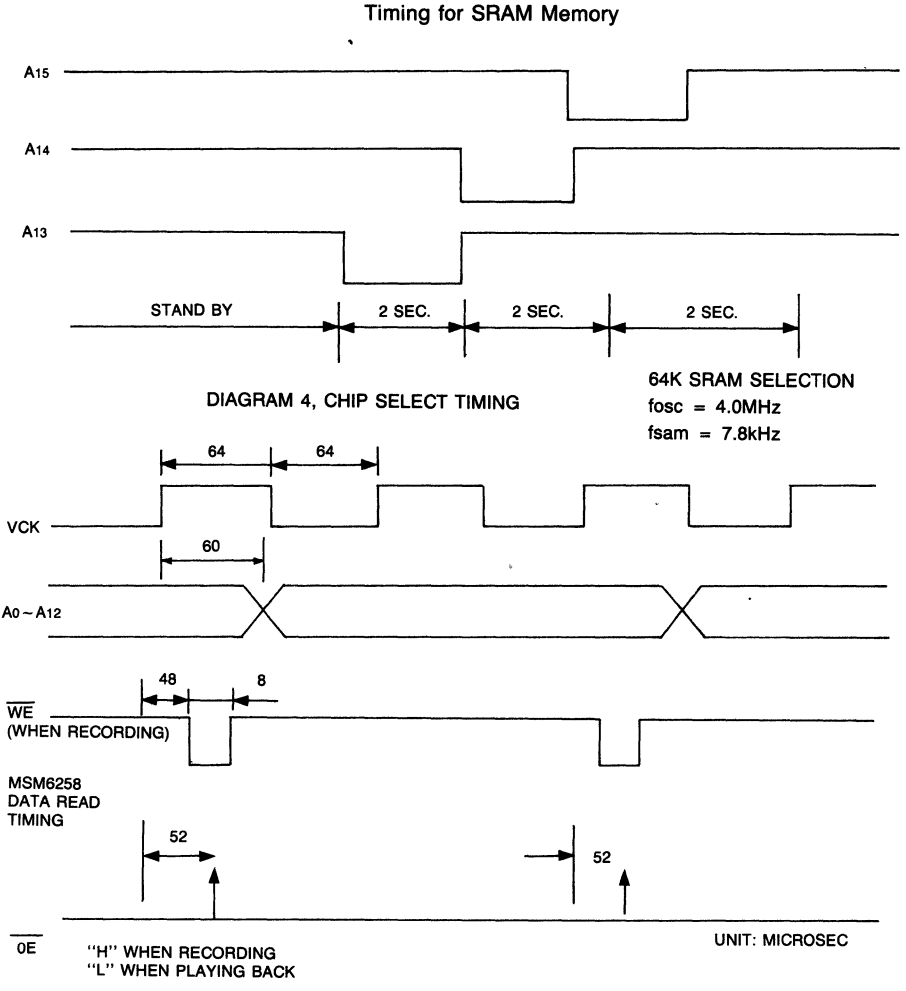


DIAGRAM 4, CHIP SELECT TIMING

DIAGRAM 5, DETAILED TIMING

HOW TO RE-RECORD

MSM6258 has protection function for each recorded channel. So to re-record, and to extend the length of recording, the protection function has to be turned off for each subsequent channels. For example, if CH-1 is to be extended then CH-2 protection flag is cancelled by activating, the "flag reset" pin (FRST = H).

Below is a sequence to record over and change the recording lengths of channel 2-4 after the channel links and lengths had been established. Please note that each channel has an override priority. That is, if CH-2 protection flag is reset and the new length of CH-2 is longer than before, it will extend into CH-3 area even if CH-3 protection flag is set.

1. Select channel 2 and reset the "flag" of channel-2 by "FRST" ((b))
2. Record again on channel 2. At this time, FST is low and so input beginning and ending pulse for ST/SP pin is needed. At this stage, recording time of channel 2 is prolonged, FST signal of channel 3 will automatically be low but at the same time, channel 3 will not be able to be recorded, ((c)).
3. (2) is an example where channel 3 was selected and that it was recorded again so as not to extend into channel-4.
4. (e) is an example where channel 4 is reset and recorded over.

EXAMPLE SHOWING CHANGE OF RECORDING LENGTH

EXTERNAL RAM CAPACITY

(a)

CH.1	2	3	4
FST = "H"	"H"	"H"	"H"

RESET FLAG OF CH.2

(b)

CH.1	2	3	4
FST = "H"	"H"	"H"	"H"

RECORD AGAIN TO CH.2

(c)

CH.1	2	3	4
FST = "H"	"H"	"H"	"H"

RECORD AGAIN TO CH.3

(d)

CH.2	2	3		4
FST = "H"	"H"	"H"		"H"

RESET CH.4 FLAG AND RECORD AGAIN TO CH.4

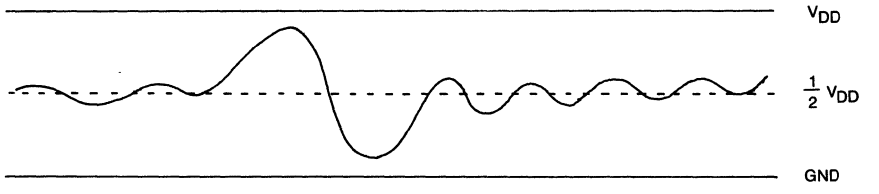
(e)

CH.2	2	3	4
FST = "H"	"H"	"H"	"H"

As shown above, all channels of MSM6258 can be used for external RAM efficiently.

OVF PIN OF MSM6258

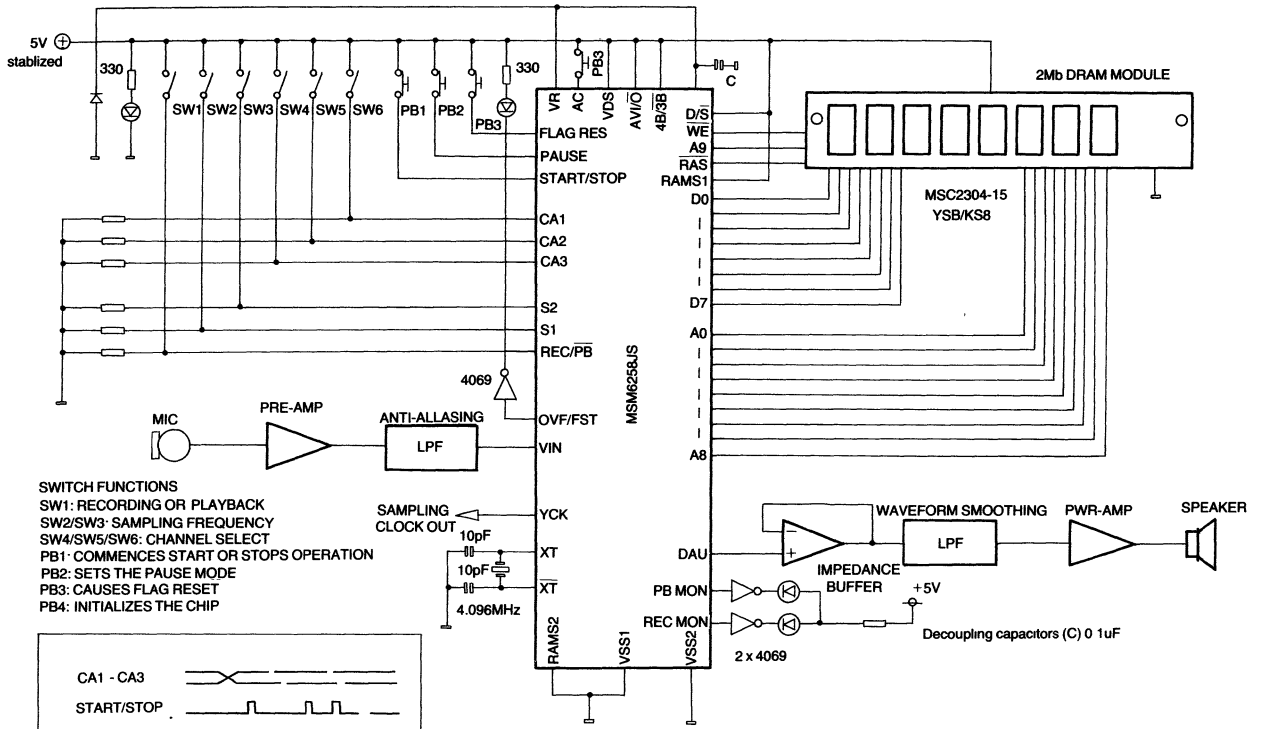
OVF pin of MSM6258 outputs "H" level when input signal exceeds 80% of dynamic range. However, human voice peak has extremely large amplitude as compared with the average, so even if "H" level is outputed from OVF pin, average power of voice is occasionally too small and the playback signal is noisy. Therefore, usage off OVF pin be avoided.



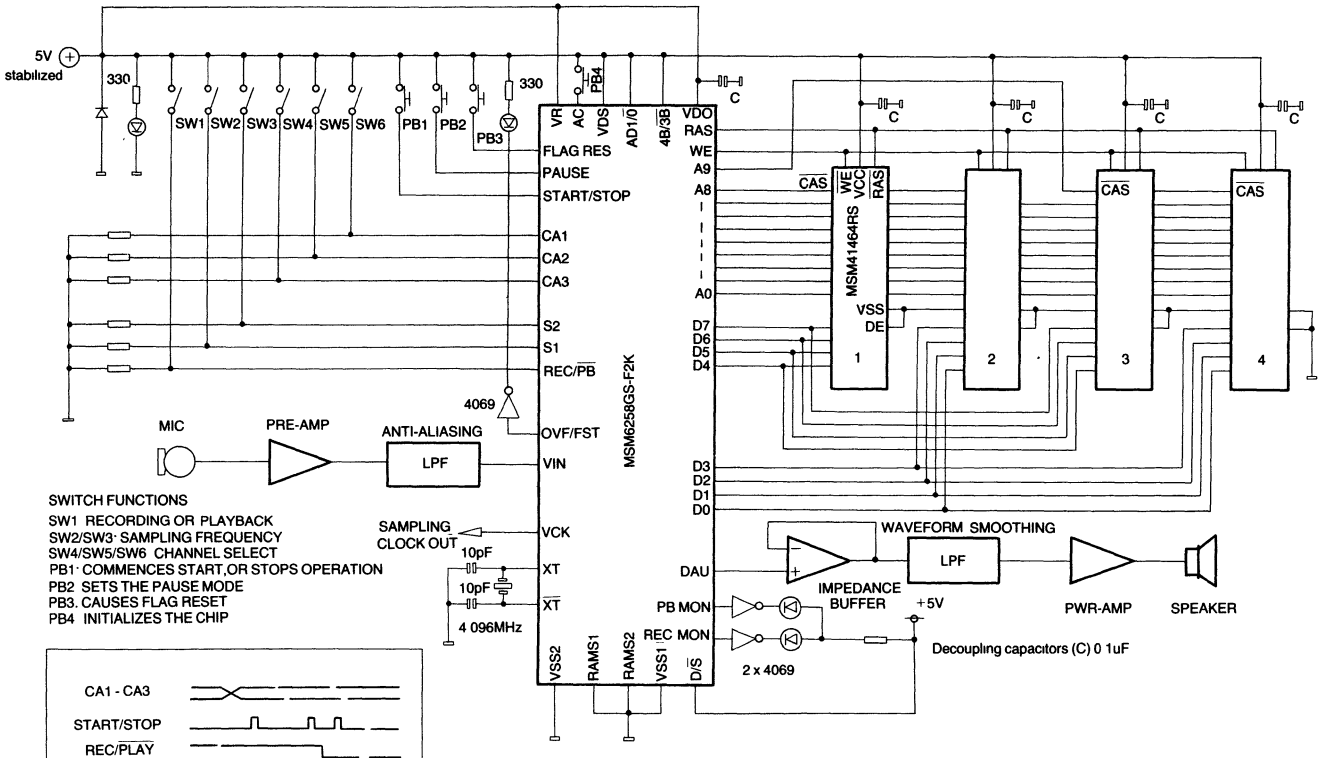
PIN CONNECTION FOR MPU INTERFACE

Following pins Must Be Grounded for MSM6258VRS

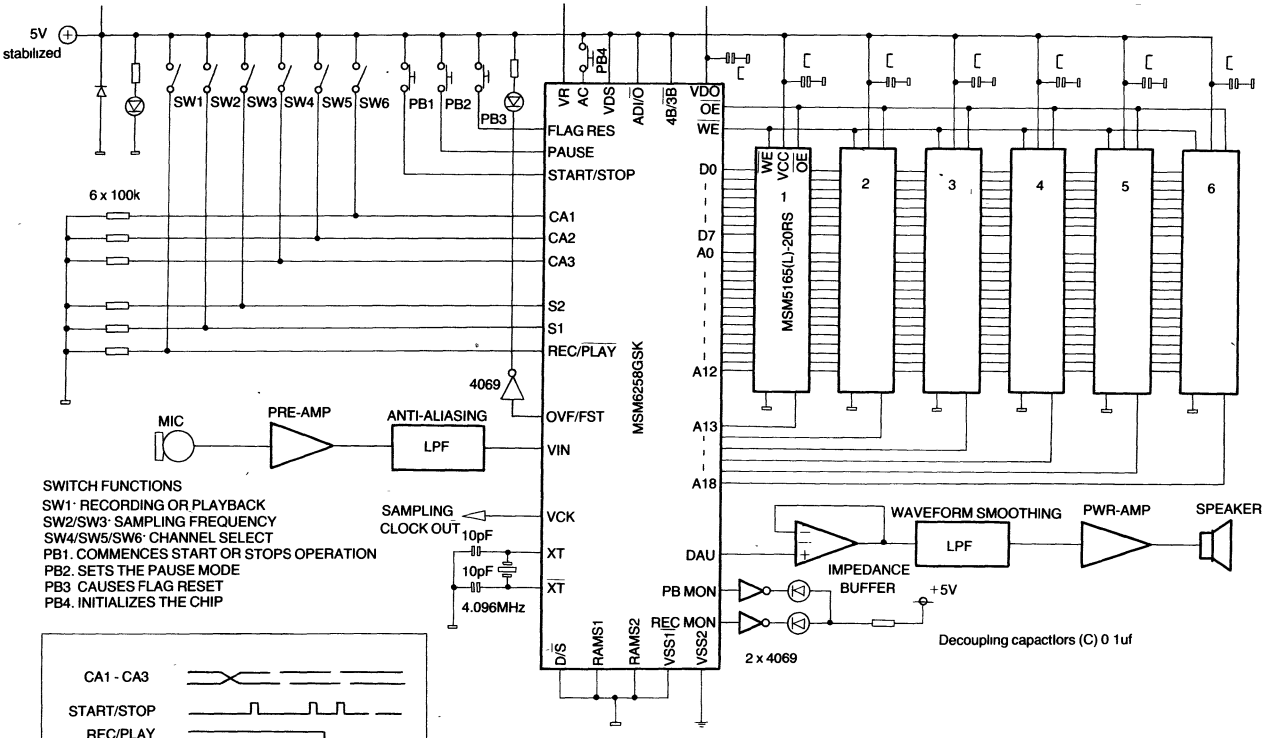
1. ST.SP
2. REC/PLAY
3. VDS
4. TDS
5. TRS1
6. TRS2
7. PAUSE



MSM6258 INTERFACED WITH DRAM MODULE (MINIMUM CONFIGURATION)

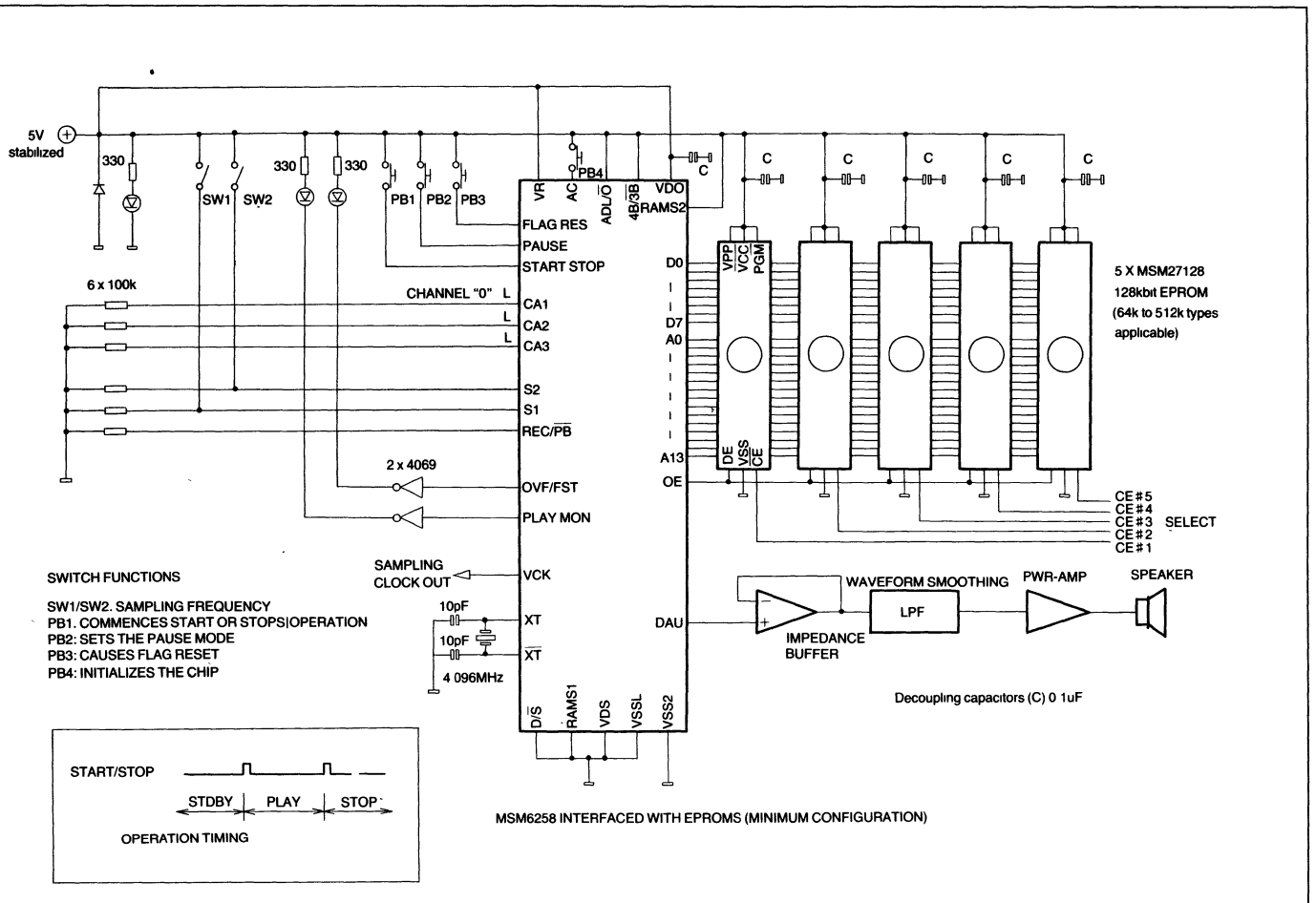


MSM 6258 INTERFACED WITH 64K x 4 DRAM (MINIMUM CONFIGURATION)

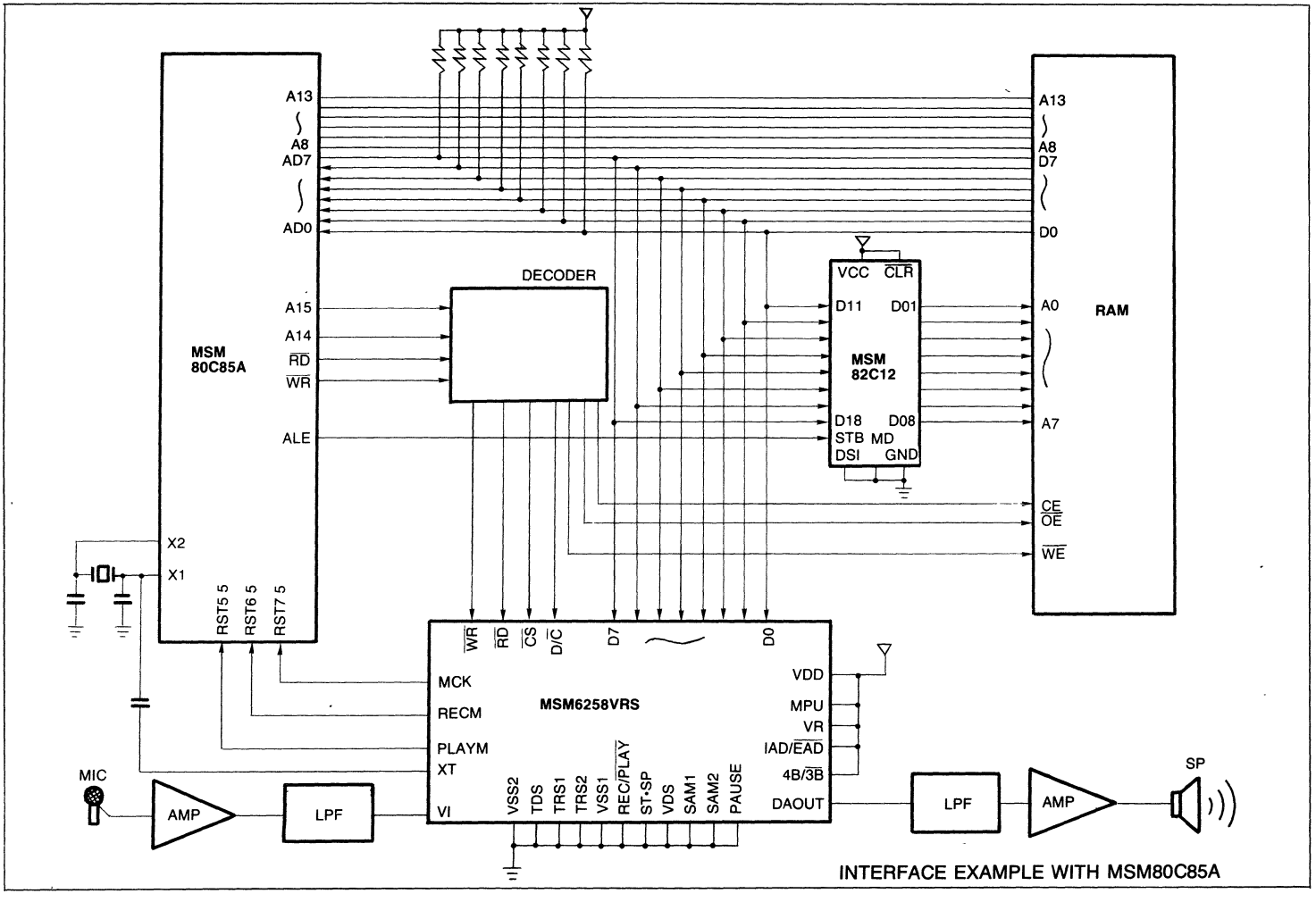


MSM6258 INTERFACED WITH SRAM (Minimum Configuration)

FILE MSM6258GSK



MSM6258 INTERFACED WITH EPROMS (MINIMUM CONFIGURATION)



INTERFACE EXAMPLE WITH MSM80C85A

REMARKS TO THE APPLICATION CIRCUITS

1. All by-pass capacitors (C)0.1uF; should be mounted in close proximity to the relevant IC.

2. If the 4.096 MHz crystal were replaced by an 8MHz type, the sampling frequency adjusted at pins S1 and S2 is proportionately increased up to the possible maximum of fs = 15.6kHz.

3. When various sampling frequencies are to be used, the cut-off frequency of the LPF's must be related individually to fs: fc = fs/2 x 0.85.
   For sampling frequencies up to 8.0 kHz, the hybrid filters, type number ALP3B (fc = 2.6kHz) and ALP4B (fc = 3.5kHz) manufactured by SOSHIN may used.

TIME TABLE for application circuits @fosc = 4.096MHz, 4=Bit ADPCM

S1	S2	fsample	BIT-RATE	TOTAL I/O TIMES OF APPLICATION CIRCUITS			
				SRAM	DRAM x 1	DRAM x 4	EPROM
L	L	4.0kHz	16.0kb/s	23 sec.	128 sec.	64sec.	40 sec.
H	L	5.3kHz	21,2kb/s	18 sec.	97 sec.	48sec.	30 sec.
L	H	8.0kHz	32.0kb/s	12 sec.	64 sec.	32sec.	20 sec.
H	H	invalid	—/—	—/—	—/—	—/—	—/—

4. The analog ground shall be separated from the digital and bonded together at a well chosen system ground position. Use VSS1 and VSS2! The power rail to VDD/VIN (MSM6258) and the memory supply line should as well be separated in the interest of improved noise immunity, especially when using DRAMs. High level and low level signal lines should be located as far from each other as possible.

MSC1161

SPEAKER DIRECT DRIVE AMPLIFIER

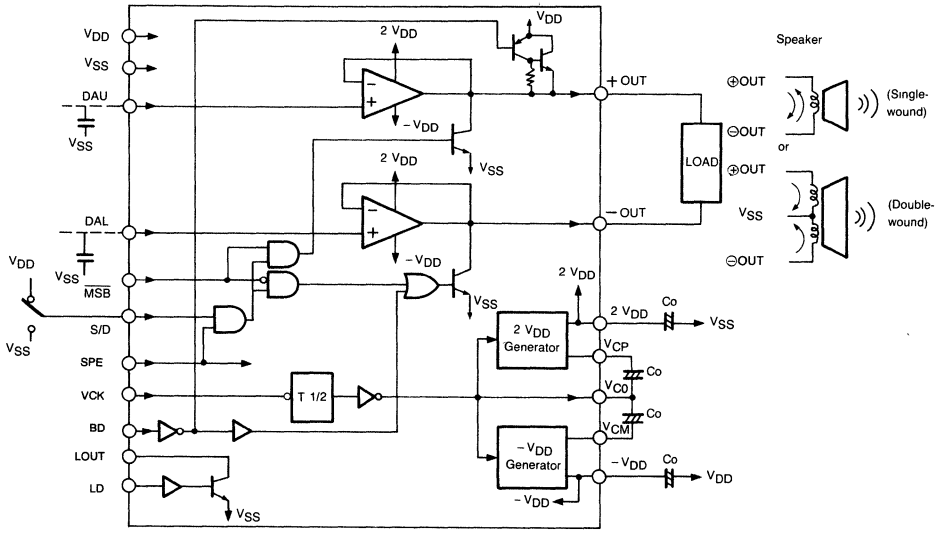
GENERAL DESCRIPTION

MSC1161 is a speaker drive amplifier IC designed specifically for watches and also for similar small system having a limitted space and power supply restriction. This IC is used together with a speech synthesizer LSI. It receives a high impedance analog signal generated from D-A converter section of the voice synthesizer LSI and directly drives a low impedance voice coil of a speaker.

FEATURES

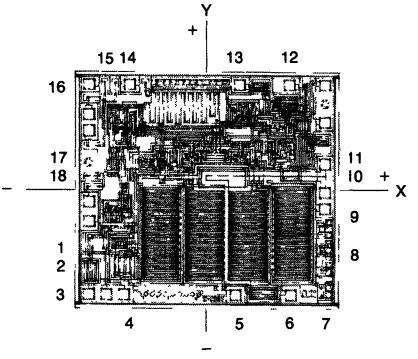
- Driven by a single power supply of +3 V.
- Input impedance higher than 1 MΩ.
- Output impedance lower than 10 Ω.
- Speaker output enable function.
- Two built-in voltage doublers for $-V_{DD}$ and 2 V_{DD}. (Four external capacitors higher than 0.1 µF are required.)
- Bi-CMOS device technology.
- Class B amplification
- Input terminal pins and levels are compatible with those of MSM6202.
- Chip, 18-pin plastic DIP, 24-pin plastic flat

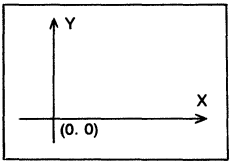
BLOCK DIAGRAM



Co = 0.1 µF or higher.

PAD LAYOUT





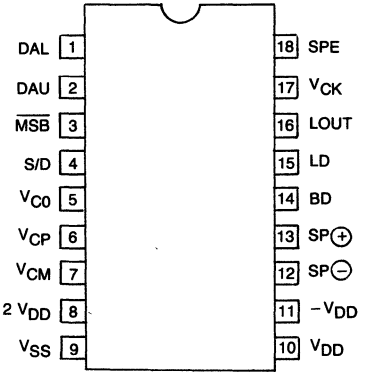
Note: • Chip size: 2.95 mm × 2.65 mm

PAD LOCATION

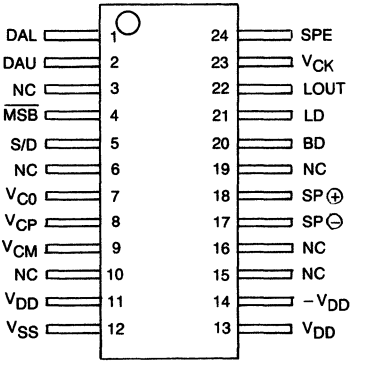
Pad No.	Symbol	Position	
		X	Y
1	DAL	−1325	−655
2	DAU	−1325	−835
3	$\overline{MSB}$	−1325	−1175
4	S/D	−865	−1175
5	V_{C0}	+365	−1175
6	V_{CP}	+925	−1175
7	V_{CM}	+1325	−1175
8	2 V_{DD}	+1325	−755
9	V_{SS}	+1325	−295
10	V_{DD}	+1325	+23
11	$-V_{DD}$	+1325	+203
12	SP⊖	+945	+1173
13	SP⊕	+325	+1173
14	BD	−925	+1173
15	LD	−1125	+1173
16	LOUT	−1325	+1173
17	V_{CK}	−1323	+355
18	SPE	−1323	+133

PIN CONFIGURATION

(Top View) 18 Lead Plastic DIP



(Top View) 24 Lead Plastic Flat Package



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Characteristics	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +5	V
Digital Input Voltage	V_{IND}	Ta = 25°C $\overline{MSB}$, S/D, SPE, VCK, BD, LD	−0.3 to V_{DD}	V
Analog Input Voltage	V_{INA}	Ta = 25°C DAUDAL	−0.3 to V_{DD}	V
Output Current	Iout	Ta = 25°C	0 to 150	mA
Storage Temperature	Tstg	—	−55 to +150	°C
Power Dissipation	P_D	Ta = 25°C	200 max	mW

Operating Ranges

Characteristics	Symbol	Test Conditions	Range	Unit
Power Supply Voltage	V_{DD}	—	+2.4 to +3.3	V
Operating Temperature	Topr	—	−10 to +60	°C
Analog Input Frequency	f_{IN}	—	0 to 8	kHz
Effective Analog Input Voltage	V_{CL}	Load dependent per graphs of Fig. 1 and 2	0 to V_{DD}	V
Output Current	Iout	V_{AIN} = 0 to V_{DD}	0 to 80	mA
VCK Input Frequency	fVCK	—	2 to 8	kHz

DC Characteristics (Ta = −10 to +60°C, V_{DD} = 3.0 V, Typ is at 25°C)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	$\overline{MSB}$, SPE, VCK BD, LD	2.5	—	—	V
Input Low Voltage	V_{IL}	$\overline{MSB}$, SPE, VCK, BD, LD	—	—	0.5	V
Input High Current	I_{IH}	$\overline{MSB}$, SPE, VCK, BD, LD	—	—	1	μA
Input Low Current	I_{IL}	$\overline{MSB}$, SPE, VCK, BD, LD	—	—	−1	μA
Input vs. Output Error Voltage	V_E	$V_{IN} < V_{CL}$ R_L = 100 Ω	—	—	30	mV
Analog Input Current	I_{INA}	$V_{IN} = V_{DD}$	—	—	3	μA
Switching Transistor Serial Resistance	γ_S	—	—	—	10	Ω
ON Output Voltage	V_{OL}	LOUT I_{SINK} = 10 mA	—		0.4	V
OFF Output Leak Current	I_{OR}	LOUT $V_O = V_{DD}$	—		1	μA
Current Consumption 1	I_{DD} (1)	Active at 8 kHz f_{VCK}	—		1	mA
Current Consumption 2	I_{DD} (2)	Standby VCK = SPE = 0 V	—		1	μA

PIN DESCRIPTION

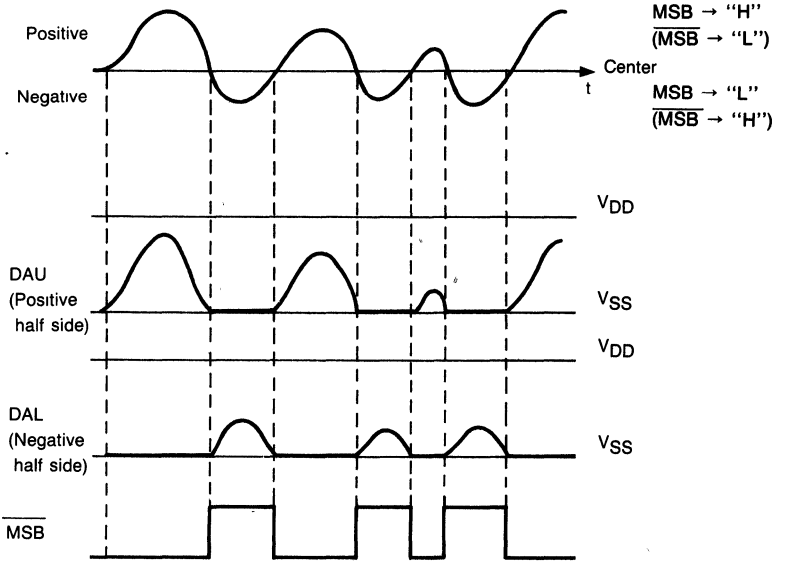
Pin Name	Terminal Number			I/O
	CHIP	18 DIP	24 FLT	
V_{DD}	10	10	13	I
V_{SS}	9	9	12	I

Power supply
In general, a 3 V line is connected to pin V_{DD} and a 0 V line to pin V_{SS}. Note that the power supply current needed is determined in most part by the current flowing through the external load. It should be also noted that the internal impedance of the power supply must be sufficiently smaller than the load impedance.

DAU	2	2	2	O
DAL	1	1	1	O
$\overline{MSB}$	3	3	4	I/O

The former two pins correspond to the positive half wave and negative half wave of the analog signal output of the D-A converter in a speech synthesizer LSI (for example, Oki's MSM6202) respectively. It should be stressed to note that in using any LSI, the V_{DD} and V_{SS} must be in common with the preceding LSI. The DAU means the positive half wave of the output analog signal and the DAL is the negative half wave. The following illustration shows a relationship of the $\overline{MSB}$ pulse with the DAU and DAL waves.

Original Signal



SPE	18	18	24	I

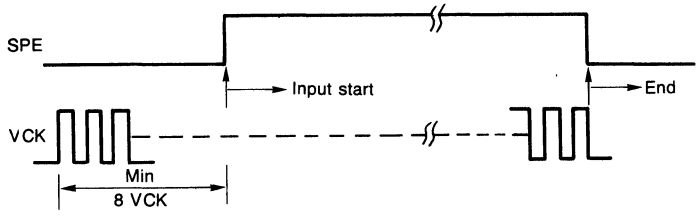
Speaker enable input
Used to make the internal circuit active when voice is produced. This feature is so effective for power saving that the internal circuit is designed to fairly reduce power consumption when no voice is produced. To enable the speaker at all times, make the pin level high by connecting pin SPE to V_{DD} or "H" as shown in the truth table below.

Truth Table

	IC state
High	Active
Low	Standby

Pin Name	Terminal Number			I/O
	CHIP	18 DIP	24 FLT	
VCK	17	17	23	I

Voltage doubler clock input
Has a 2 to 8 kHz pulse input. This input is not needed when no voice is produced. It, however, is required for a period of time for at least eight VCK pulses before starting voice input from the pins DAU and DAL. The reason is that the 2 V_{DD} and $-V_{DD}$ voltages of the internal voltage double circuit should be stabilized previously.



$2V_{DD}$	8	8	11	I
V_{CP}	6	6	8	I
V_{CO}	5	5	7	I
V_{CM}	7	7	9	I
$-V_{DD}$	11	11	14	I

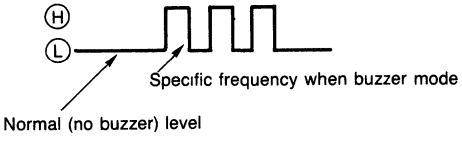
Two voltage doublers
Additional capacitors should be externally connected as shown in the preceding "Block Diagram and 18-Pin Terminal Identification" figure. With a specific frequency input from the pin VCK, a doubled voltage (2 V_{DD}) and negative voltage ($-V_{DD}$) will be obtained. It should be noted that the both voltages are for internal use only.

BD	14	14	20	I

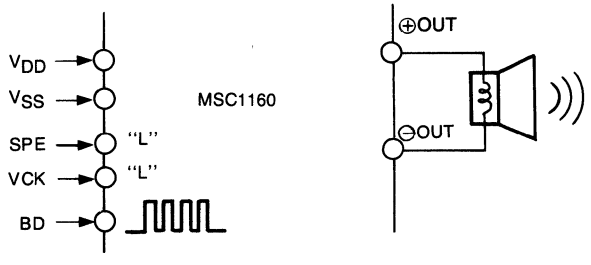
Buzzer drive input
Has a usual square waveform input when no voice is produced, to make the voice speaker sound as a buzzer. For this purpose, should be as follows.

SPE Input: Low (standby state)

BD Input:

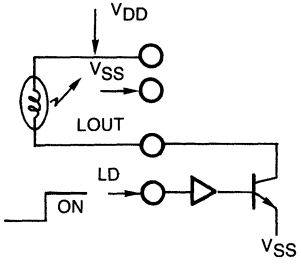


Connection Diagram (for single-wound speaker)



Pin Name	Terminal Number			I/O
	CHIP	18 DIP	24 FLT	
LD	15	15	21	I
LOUT	16	16	22	O

Lamp drive input, lamp drive output
A simple independent lamp drive circuit for watch is built in. If a high signal is applied to pin LD, it turns on the NPN transistor, the open collector of which makes low output signal at pin LOUT, thereby turning on the lamp.

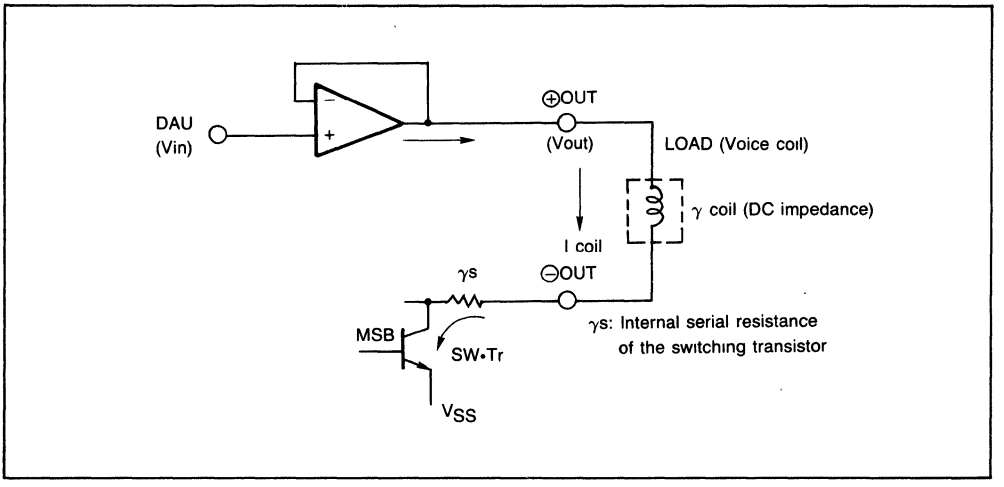


SP ⊕	13	13	18	O
SP ⊖	12	12	17	O
S/D	4	4	5	I

Speaker output single/double wind select
The former two pins are connected to the speaker to directly drive in class B amplification. For a speaker having double-wound voice coil with a center tap, a voltage of V_{SS} is applied to pin S/D as shown in the preceding figure of the "Internal Block Diagram and 18-Pin Terminal Identification". The voltage level to be applied to pin S/D is charted below.

Speaker Used	Voltage Input Level at S/D
Single-wound type	High (or open)
Double-wound type	Low

RELATION BETWEEN INPUT VOLTAGE AND VOICE COIL CURRENT



STEP 1: Relation between Vin and Vout

The class B amplifier shown in the equivalent circuit above can satisfactorily follow up the input signal because its frequency is relatively low.

a. If Vin is lower than V_{DD}

$$Vin = Vout + Voffset \quad \text{..... (1)}$$

where Voffset represents the offset voltage of the amplifier which is lower than 10 mV. In view of the fact that ILSB (input least significant bit level) of Vin (D-A converter output) is 10 mV, the offset voltage, Voffset, can be ignored. (The ILSB is given as ILSB = $2.5\ V/2^8$ = 10 mV.) Hence, Eq. 1 can be regarded as

$$Vin = Vout \quad \text{..... (2)}$$

b. If Vin approaches to V_{DD}

As long as $Vin < V_{CL}$, Eq. 2 can be held. If $V_{CL} \leqq Vin \leqq V_{DD}$, the following relationship is given.

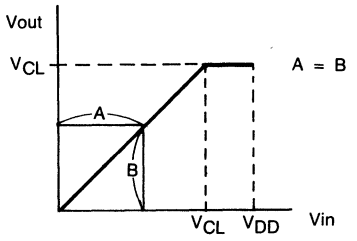
Vin corresponds almost to Vout in the amplification as described in a. If Vin is made to approach V_{DD}, the upper limit of the output voltage, Vout, of the amplifier fixes to the clipped value, V_{CL}. Hence, in the region of $V_{CL} \leqq Vin \leqq V_{DD}$

$$Vout = V_{CL} \quad \text{..... (3)}$$

This equation means that Vout has no relation to Vin.

c. Graphical illustration

The two operational cases, a and b, mentioned above are illustrated in graph below.



d. Relation between V_{DD} and V_{CL}

The clipped voltage, V_{CL}, for a specific power voltage, V_{DD}, can be determined according to the characteristics of the driver elements in the amplifier. The MSC1160 is designed to have such load characteristic lines as in Figs. 1 and 2. According to the load characteristic lines, V_{CL} can be determined uniquely together with Icoil (denoting the current flowing the voice coil) with a serial resistance of the voice coil as part of a parameter. The designer should take the condition for Icoil and Vout in designing the voice coil. The condition will be explained in the following paragraphs.

Step 2: Relation between Vout and Icoil

a. If Vout is lower than V_{CL}, i.e., Vout < V_{CL}

If Vin is rather small, Vout is not clipped by V_{CL} yet. Relationship between Vout and Icoil is given as

$$Icoil = \frac{Vout}{\gamma coil + \gamma s} \quad \text{..... (3)}$$

Where γs is the internal serial resistance of the switching transistor, and $\gamma coil$ is the serial resistance of the voice coil. Since γs is around 5 Ω as the switching transistor characteristic, if $\gamma coil$ can be ignored in comparison with γs, then Eq. 3 can be modified as

$$Icoil = \frac{Vout}{\gamma coil} \quad \text{..... (4)}$$

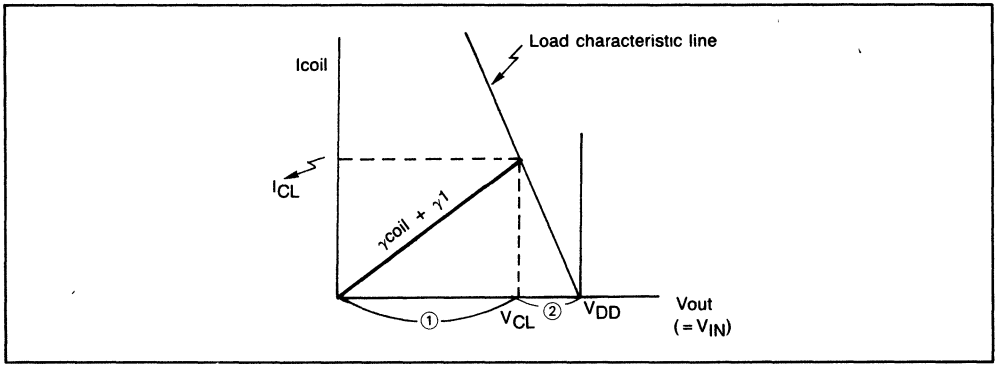
b. If Vout is clipped to V_{CL}, i.e., Vout = V_{CL}

The voice coil current, Icoil, can be given by

$$Icoil = \frac{V_{CL}}{\gamma coil} \quad \text{..... (5)}$$

c. Graphical illustration

The two operational cases, a and b, are shown in Figs. 1 and 2 for obtaining the voice coil current, Icoil. For using the graphs, refer to the illustration below.



Region 1 corresponds to Eq. 3 or 4.

Region 2 is a range where Vout and Icoil are clipped to V_{CL} and I_{CL}.

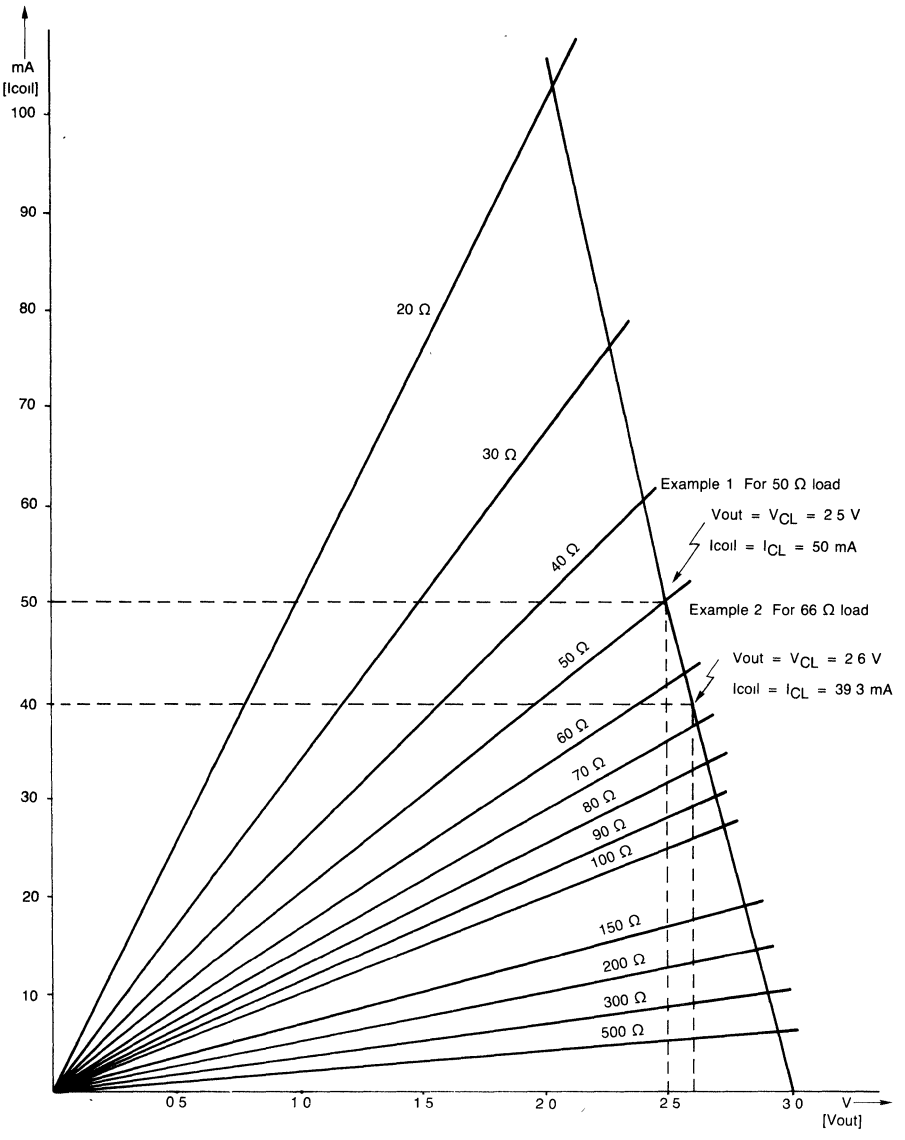


Fig. 1 Determination of Icoil vs. Vout with parameter of γcoil plus γs at 2.4 V of V_{DD}

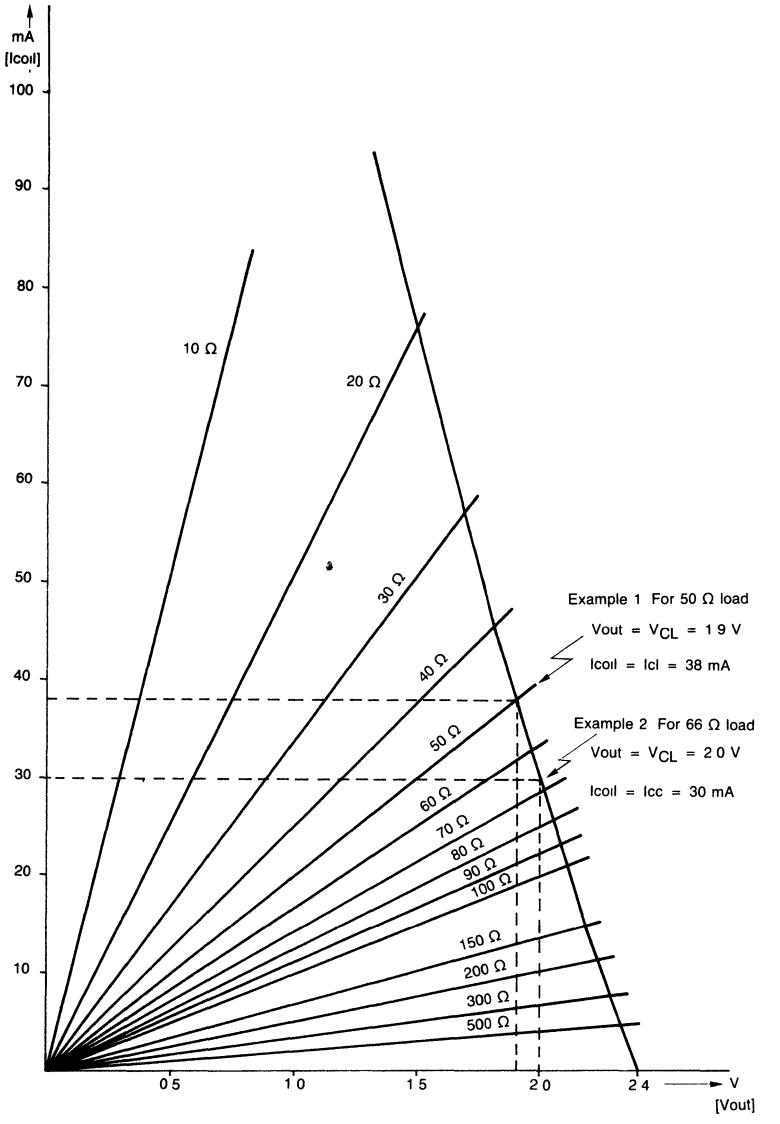
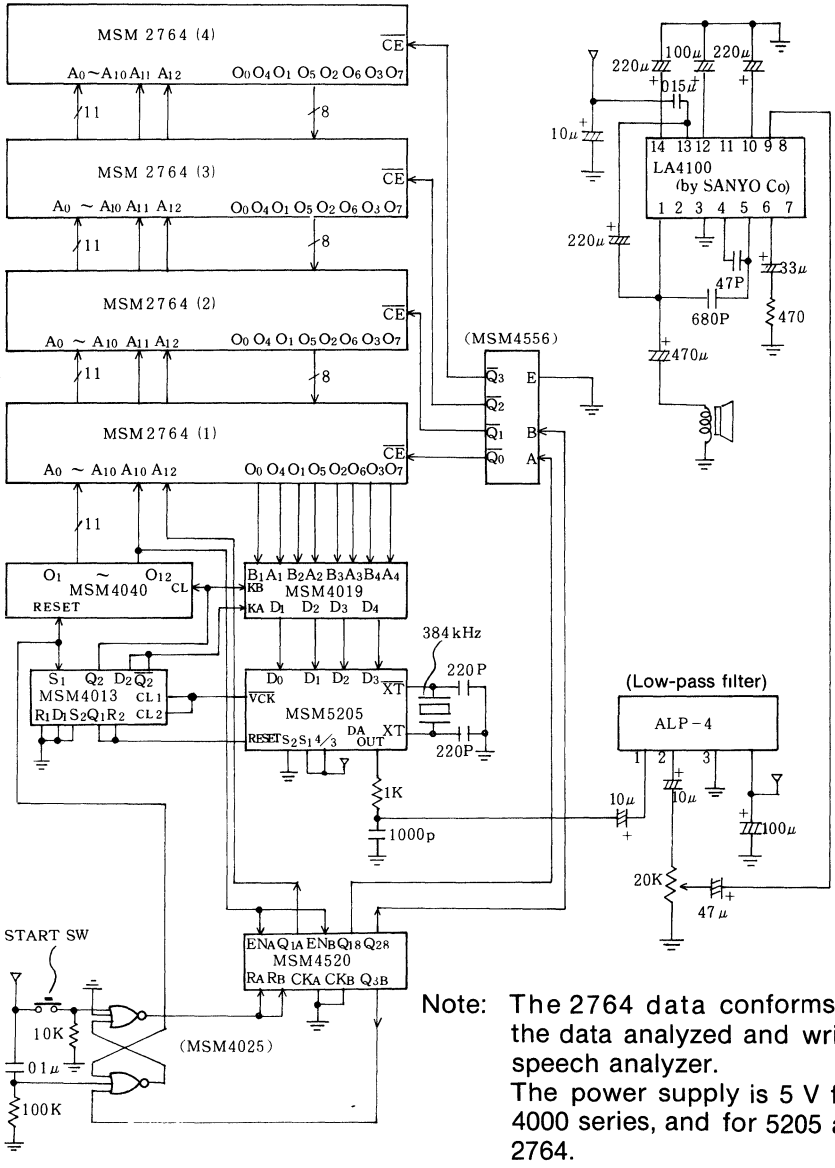


Fig. 2 Determination of Icoil vs. Vout with parameter of γcoil plus γs at 3.0 V of V_{DD}

APPENDIX

■ MSM5205 Voice Synthesis Circuit Example

An example where four 2764 devices are used linked together is shown in Figure 1. The timing chart for this example is provided in Figure 2.



Note: The 2764 data conforms with the data analyzed and written by speech analyzer.
The power supply is 5 V for the 4000 series, and for 5205 and 2764.

Fig. 1 MSM5205 voice synthesis circuit example

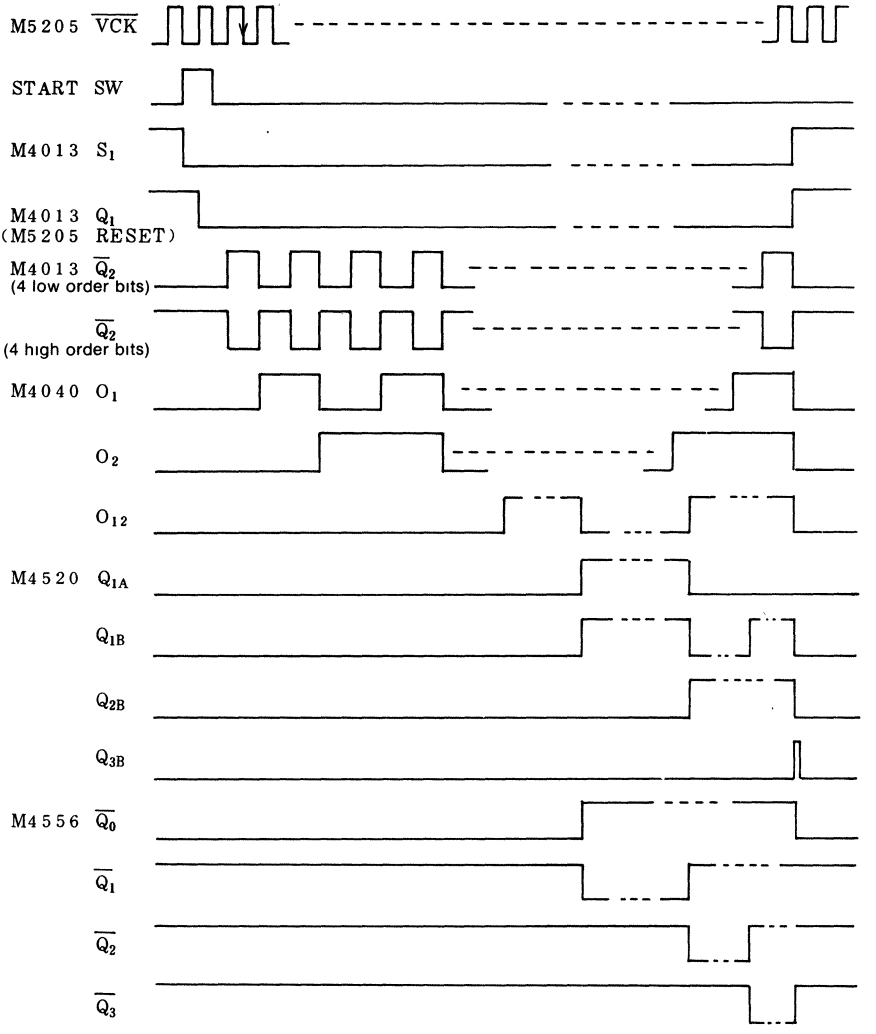


Fig. 2 MSM5205 application circuit example time chart

■ MSM5218 Voice Analysis/Synthesis Circuit Example (When MSM5204 is Used)

An example of an application circuit for voice analysis and synthesis using MSM5218 and MSM5204 is shown in Figure 3. The time charts for these circuits are given in Figures 4 and 5.

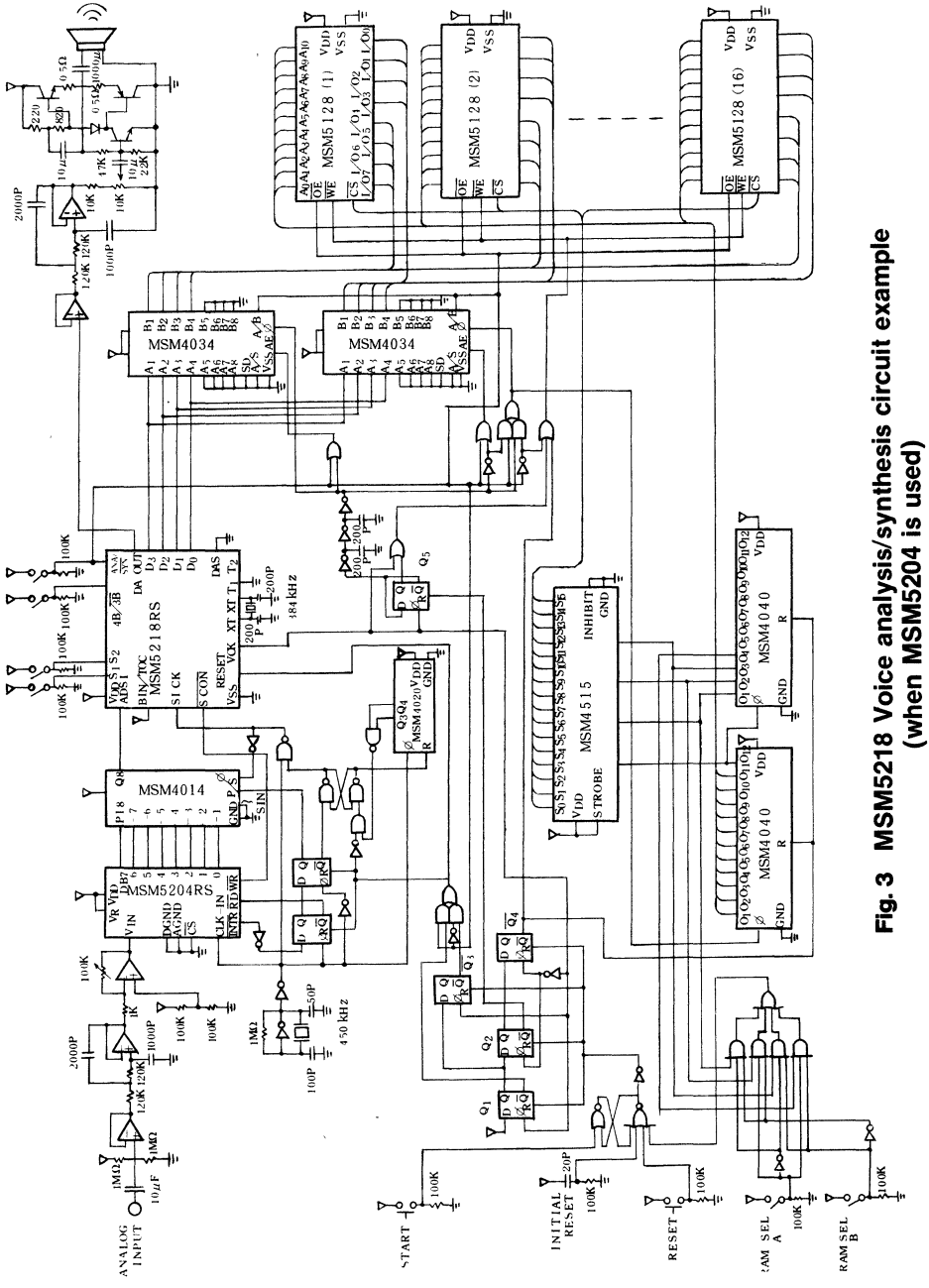


Fig. 3 MSM5218 Voice analysis/synthesis circuit example (when MSM5204 is used)

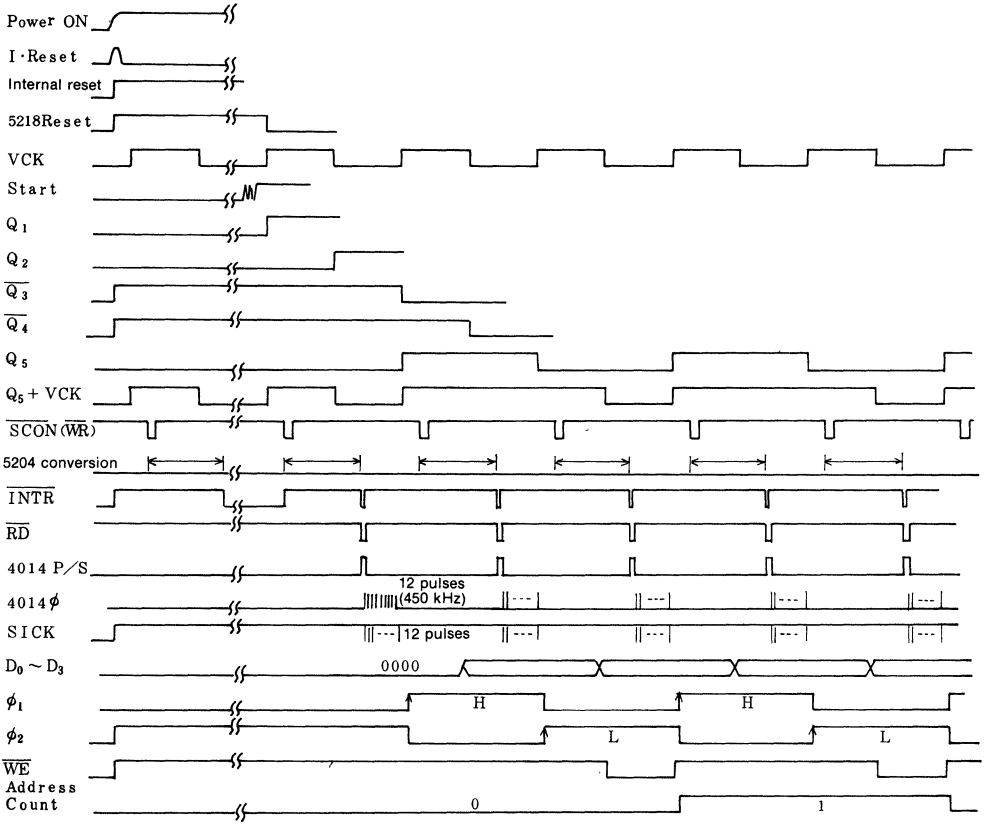


Fig. 4 MSM5218 Voice analysis time chart

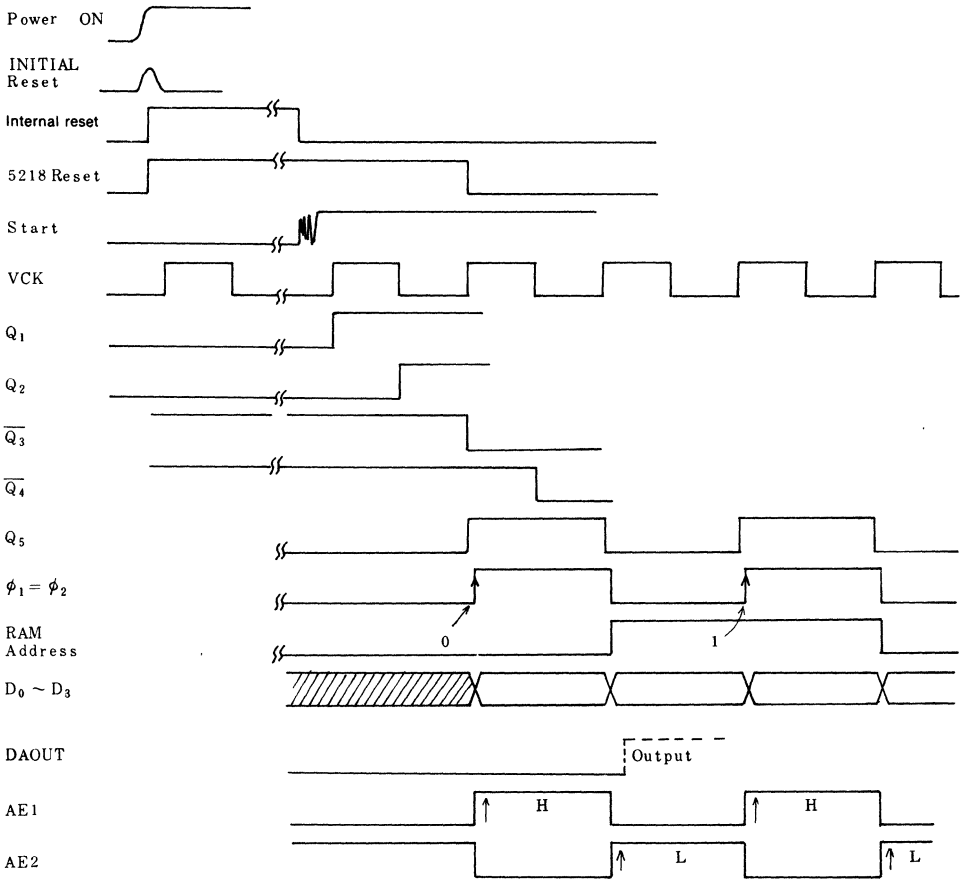


Fig. 5 MSM5218 Voice synthesis time chart

■ MSM5218 Voice Analysis/Synthesis Circuit Example (When 12-bit AD Converter is Used)

An example of an application circuit for voice analysis and synthesis using MSM5218 and a 12-bit AD converter (ADC-80AG is manufactured by *MN Co.) is shown in Figure 6.

The time charts for these circuits are given in Figures 5 and 7.

* Micro Network Corp.

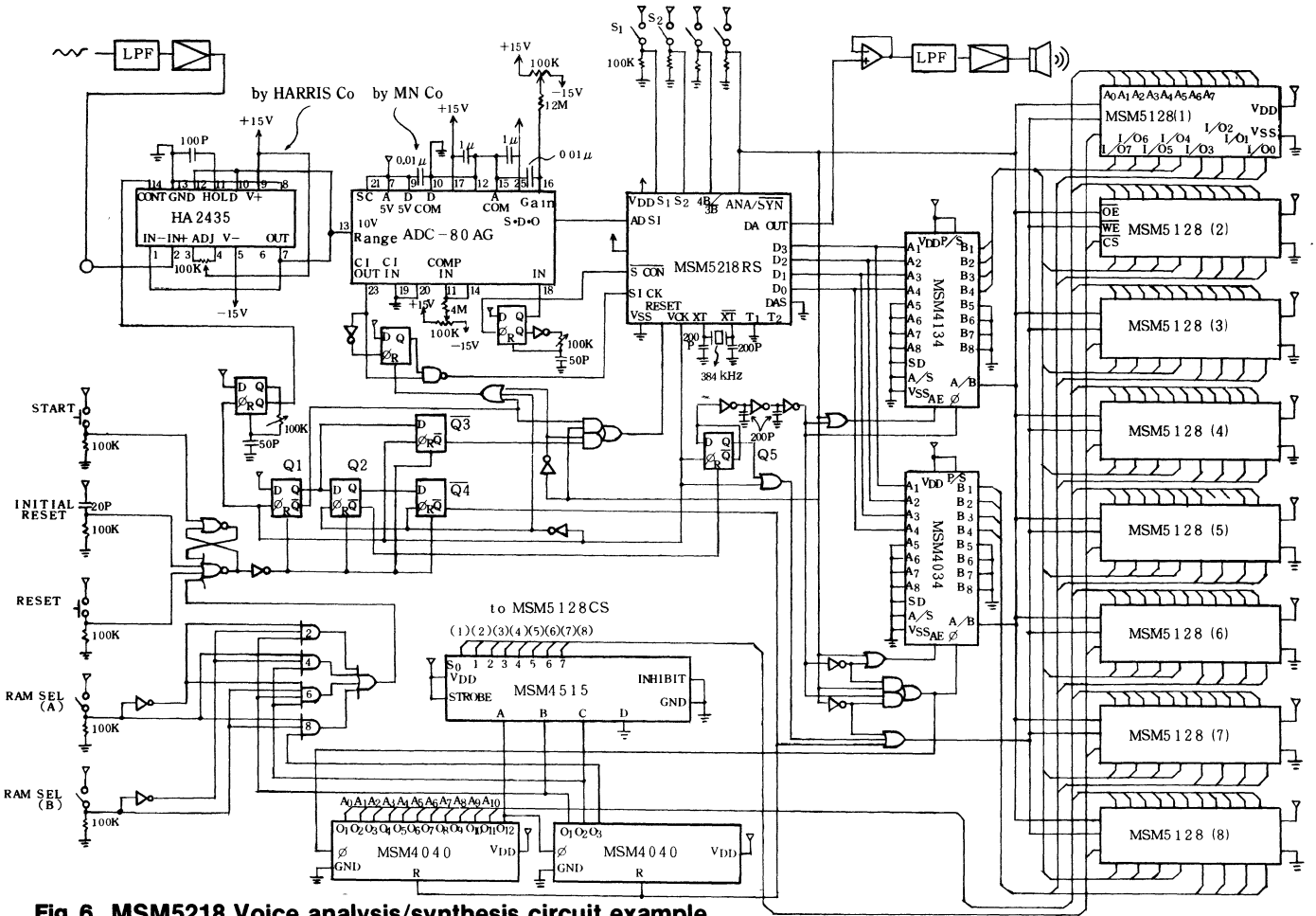


Fig. 6 MSM5218 Voice analysis/synthesis circuit example (when 12-bit AD converter is used)

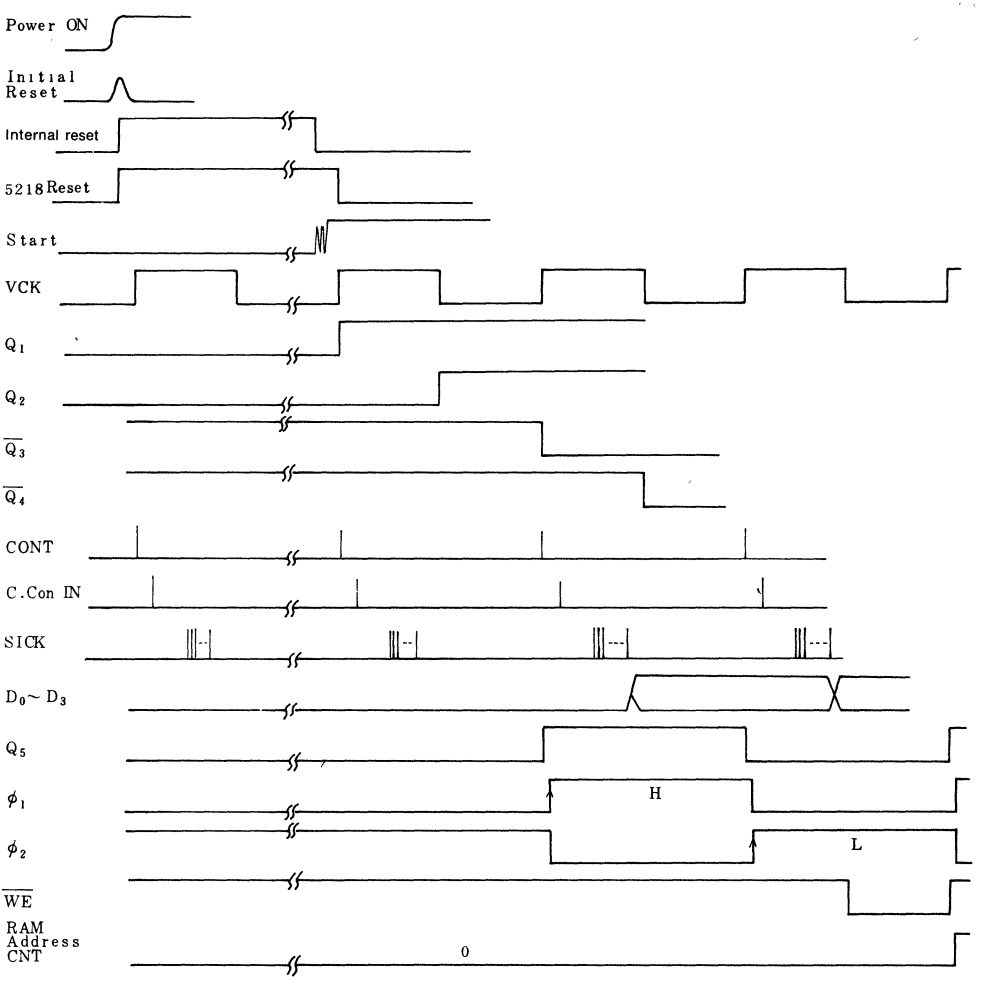
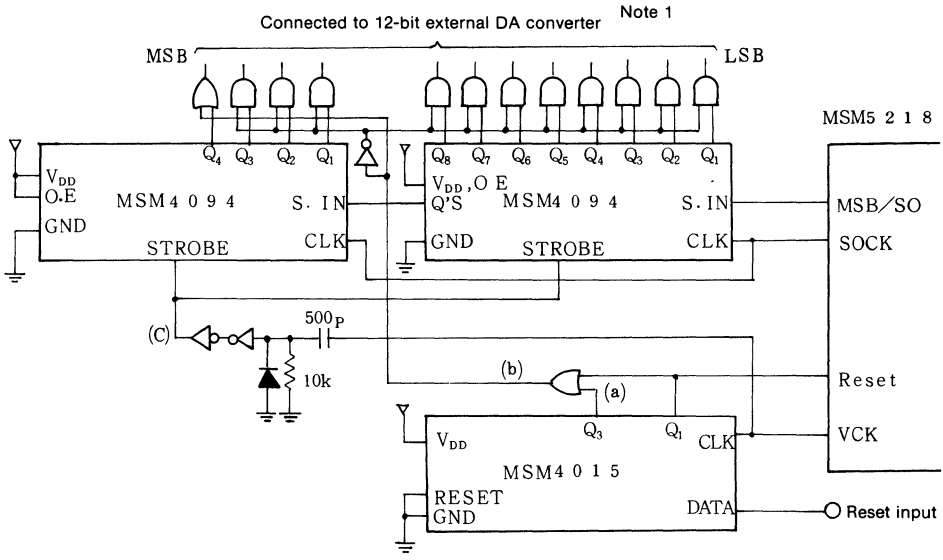


Fig. 7 MSM5218 Voice analysis time chart (when 12-bit AD converter is used)

■ Example of Interface between MSM5218 and an External DA Converter

An example of an interface circuit between MSM5218 and an external DA converter is shown in Figure 8.

The time chart for this circuit is given in Figure 9.



Note 1. The 12-bit output is in regular straight binary code.

Fig. 8 MSM5218 to external DA converter interface example

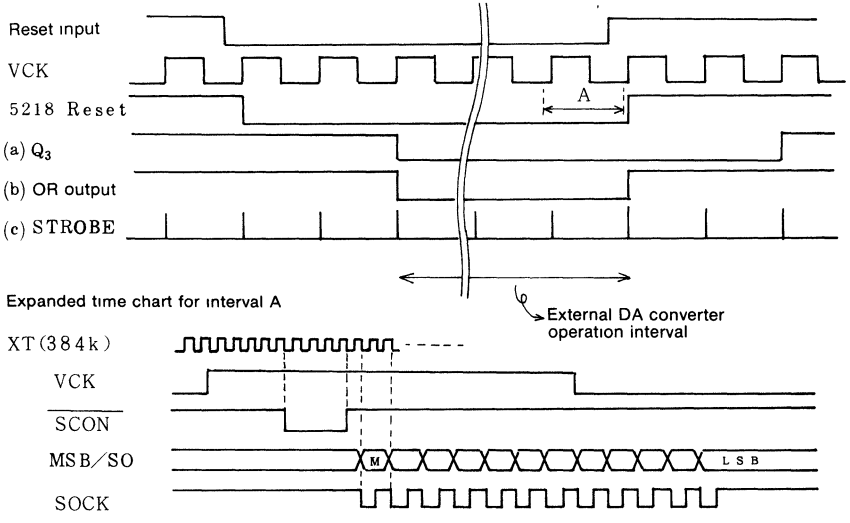


Fig. 9 MSM5218 and external DA converter time chart

■ Example of MSM6258 Application Circuit

An example of an application circuit which MSM6258 is used with six 64K SRAM devices for voice recording and reproduction is shown in Figure 10.

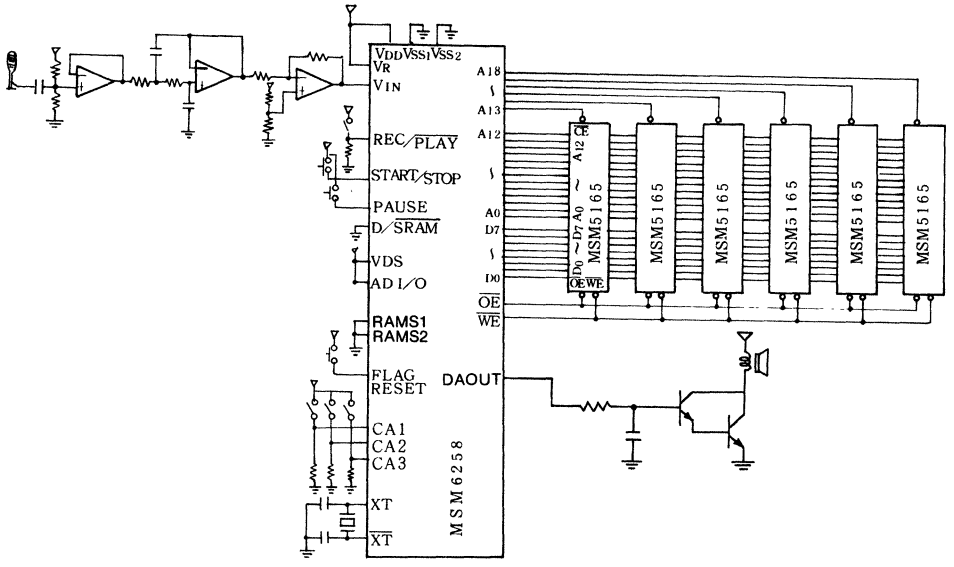


Fig. 10 MSM6258 application circuit example

The time chart for Figure 10 is given in Figure 11.

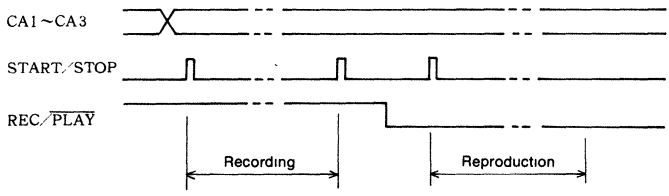


Fig. 11 MSM6258 time chart

■ MSM5248 and LM380N (Power Amplifier) Interface Example

An example of interfacing with LM380N to achieve a high volume output from MSM5248 is outlined in Figure 12.

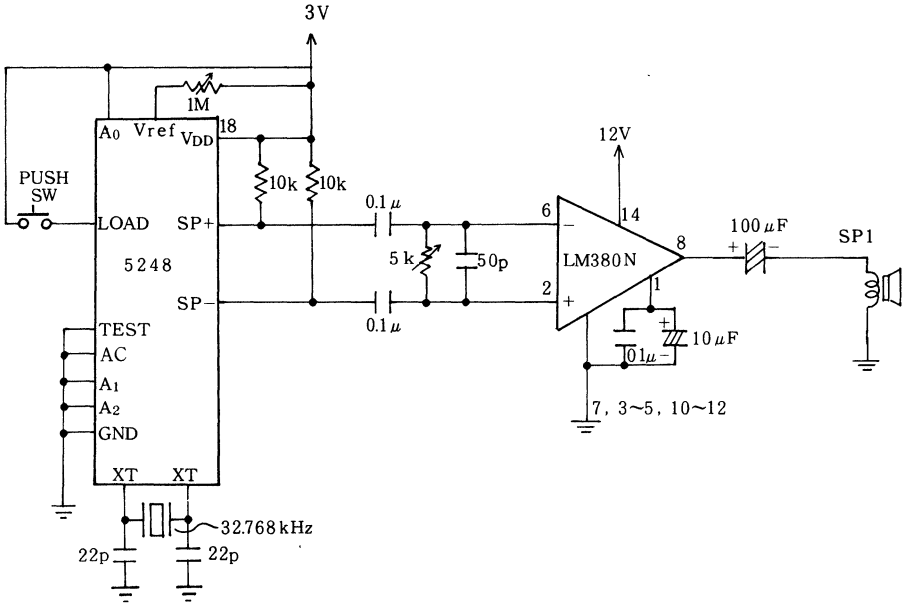
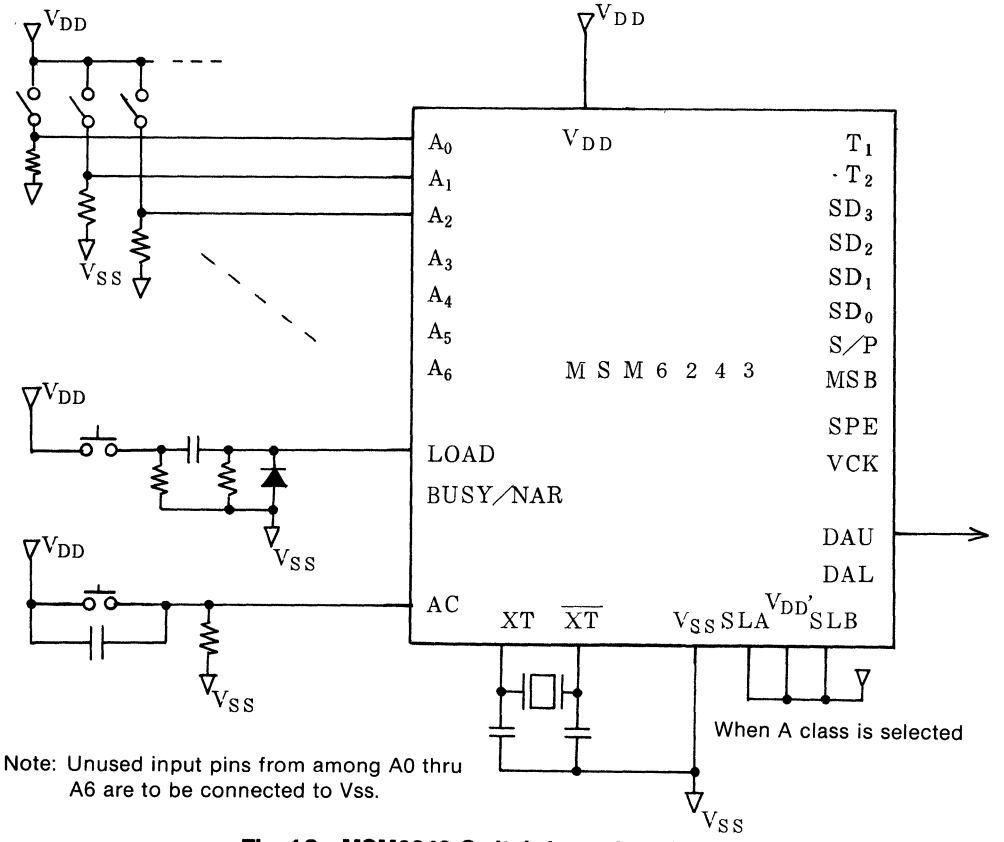


Fig. 12 MSM5248 and LM380 interface example

Note 1. The MSM5248 and LM380N ground pins are connected to a common ground terminal.
2. Use SP and SP- pull-up resistances of about 20 kohm when an external Vref resistance of 500 kohm VR is used.
3. LM380N is manufactured by the National Semiconductor Co.
4. The MSM5248 outlined in Figure 12 shows LOAD input activated with no A0 pull-down resistance.

■ MSM6243 Switch Input Interface Example

An example of MSM6243 switch input interface is shown in Figure 13, and the time chart for repeated vocalization of a single word is shown in Figure 14.



Note: Unused input pins from among A0 thru A6 are to be connected to Vss.

Fig. 13 MSM6243 Switch input interface example

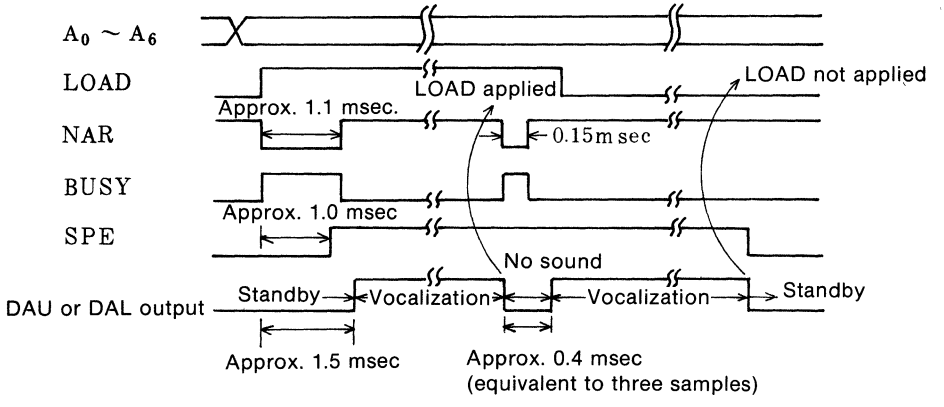
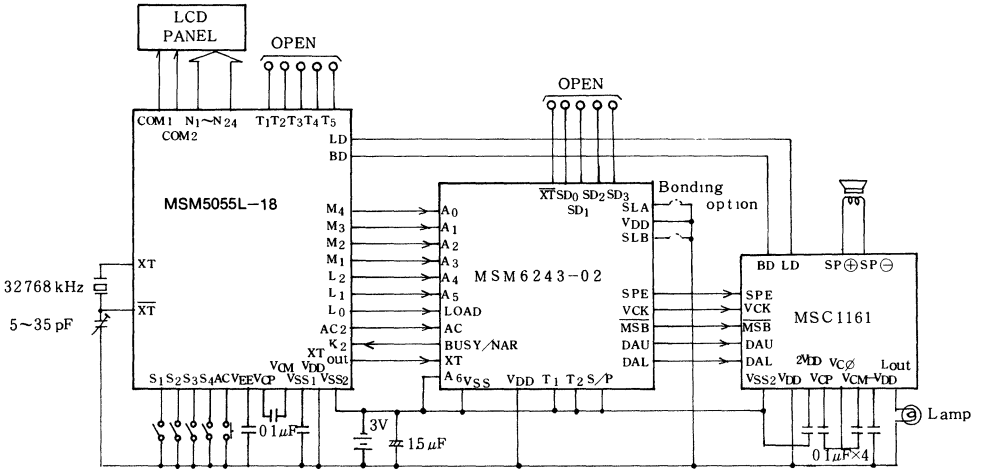


Fig. 14 MSM6243 Switch input timing diagram

■ Example of MSM6243 and MSM5055 (Watch CPU) Interfacing with MSC1161

An example of MSM5055 interfacing when MSM6243 is used in time announcing watches is outlined in Figure 15.



Note: If bonding on chip, make sure that MSC1161 is (begin-ind) isolated from MSM5055 and MSM6243. (See accompanying diagram.)

COB example

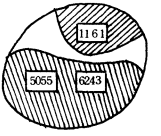


Fig. 15 Example of MSM6243 and MSM5055 interfacing with MSC1161

■ MSM6243 Microcomputer Interface Examples

MSM6243 has been designed with due consideration given to microcomputer interfacing, thereby enabling simple voice editing etc. The method for interfacing MSM6243 to a microcomputer is described here using the well-known Centronics parallel interface as an example.

Normal Centronic interfaces consist of "handshaking" by BUSY and STROBE lines where seven or eight bits of data are passed via the D0~D7 data line for accurate transfer from microcomputer to external device (such as a printer). That is, the microcomputer first places the data to be sent on the $D_0 \sim D_7$ line, and after checking that the external device is not busy (BUSY line at L level), applies positive pulses to the STROBE line. The external device subsequently detects pulses on the STROBE line and proceeds to accept that data. An H level signal is passed to the BUSY line until the external device completes acceptance of the pulses and is prepared to accept the next set of pulses. In this way, a single item of data is transferred, and where necessary the next item of data is transferred in the same way.

MSM6243 is equipped with a LOAD pin and a BUSY/NAR pin (user selectable) which correspond to the above STROBE and BUSY pins. Furthermore, MSM6243 is equipped with $A_0 \sim A_6$ pins which correspond to the above data line. Vocalized syllable codes are applied to the $A_0 \sim A_6$ pins. The microcomputer is notified whether this input code has been enabled or disabled at this time via the BUSY/NAR pin (enabled when H, and disabled when L if NAR has been selected). When enabled, a positive input pulse is applied to the LOAD pin. Upon input of this code, the BUSY/NAR output is switched to L (if NAR has been selected) thereby disabling subsequent input. And almost at the same time, the sound corresponding to that syllable code is vocalized. And if input of the next code during vocalization of that syllable is enabled, the BUSY/NAR output is switched to H (if NAR has been selected) in readiness for input of the next code.

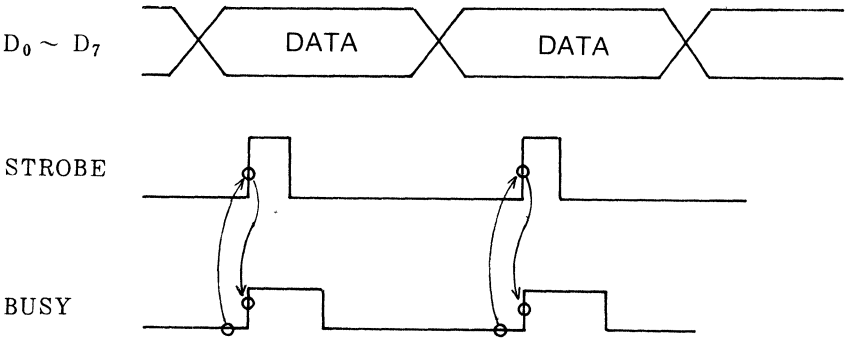


Fig. 16 Centronic interfaces in/out timing

In this way, sounds can be vocalized by MSM6243 in much the same way that characters are printed by a printer. The flow for vocalization of a single syllable code is outlined in Figure 17. And since MSM6243 is equipped with two buffers for storing syllable codes, editing without interrupting syllables is possible.

Single syllable vocalization output routine flowchart Assume that RESET has been cancelled by main routine. Assume that syllable codes are obtained from the main routine.

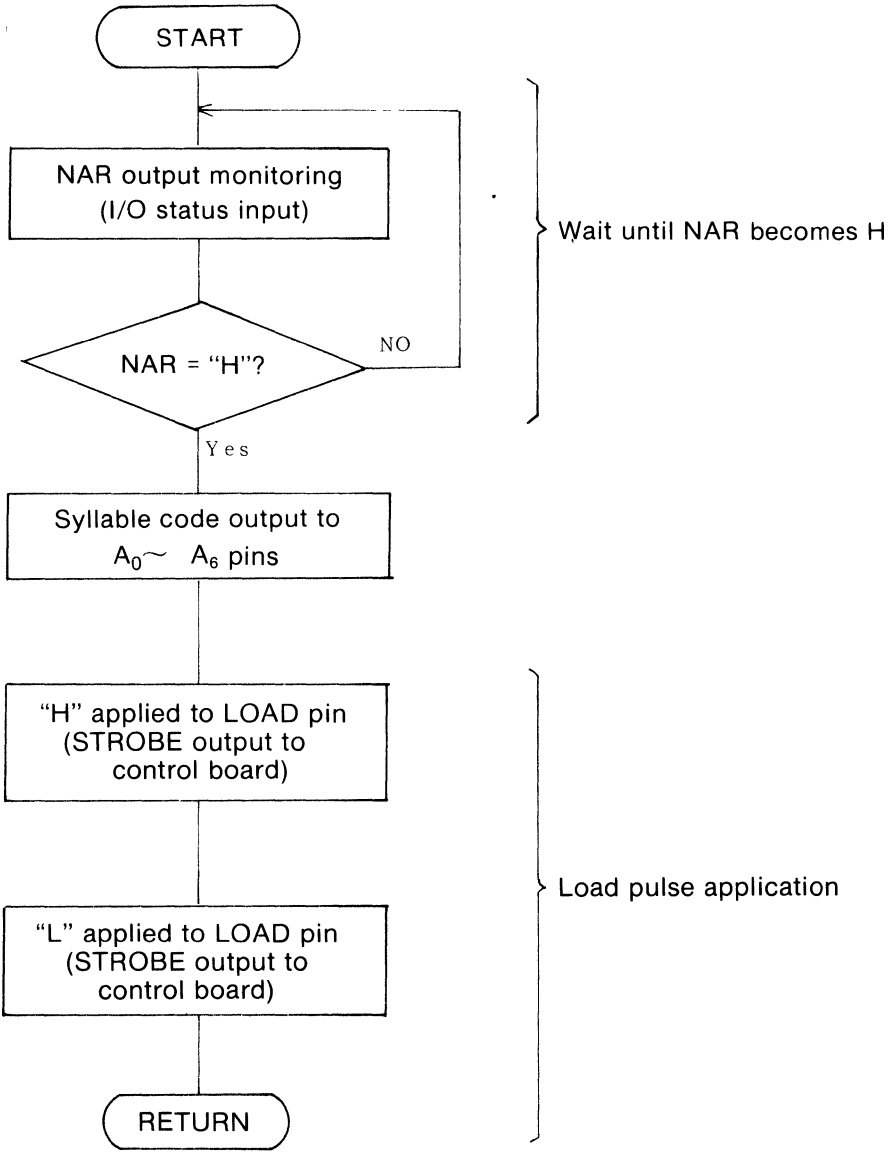


Fig. 17 Single sound output routine flow chart

■ **Example of MSM6212 Interfacing with an OP amp. (Class B Operation)**

An example of MSM6212 interfacing with an OP amp. Used in class B operation is shown in Figures 18 and 20.

1) Example of circuit where the OP amp. ±power supply is used apart from the MSM6212 power supply

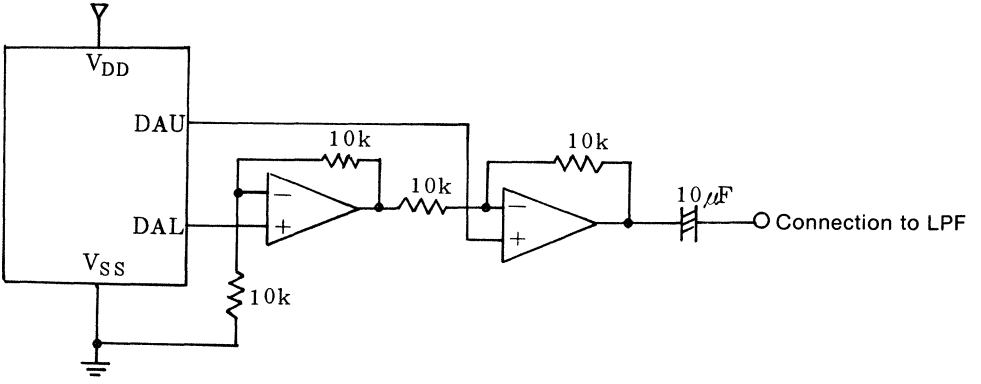


Fig. 18 MSM6212 and OP amplifier interface example 1

2) DAU and DAL output waveforms and the LPF input waveform in the above example

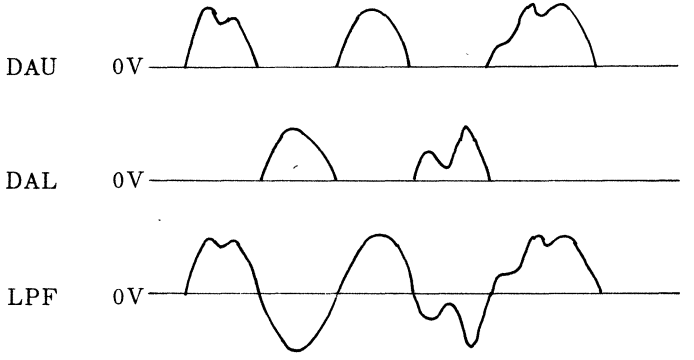


Fig. 19 Class B operation output and input waveforms

3) Example of 5 V single phase power supply circuit for both MSM6212 and OP amp.

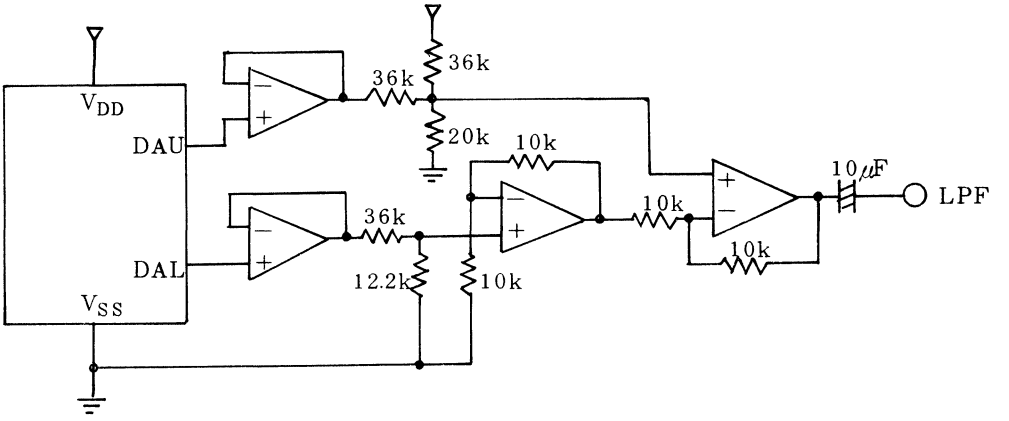


Fig. 20 MSM6212 and OP amp interface example 2

Note: Ensure that the OP amp is operated in this case (begin-end) with an input voltage above 0 V.

■ MSM6212 Switch Input Interface Example

An example of MSM6212 switch input interfacing is shown in Figure 21, and the time chart for repeated vacalization of a single word is shown in Figure 22.

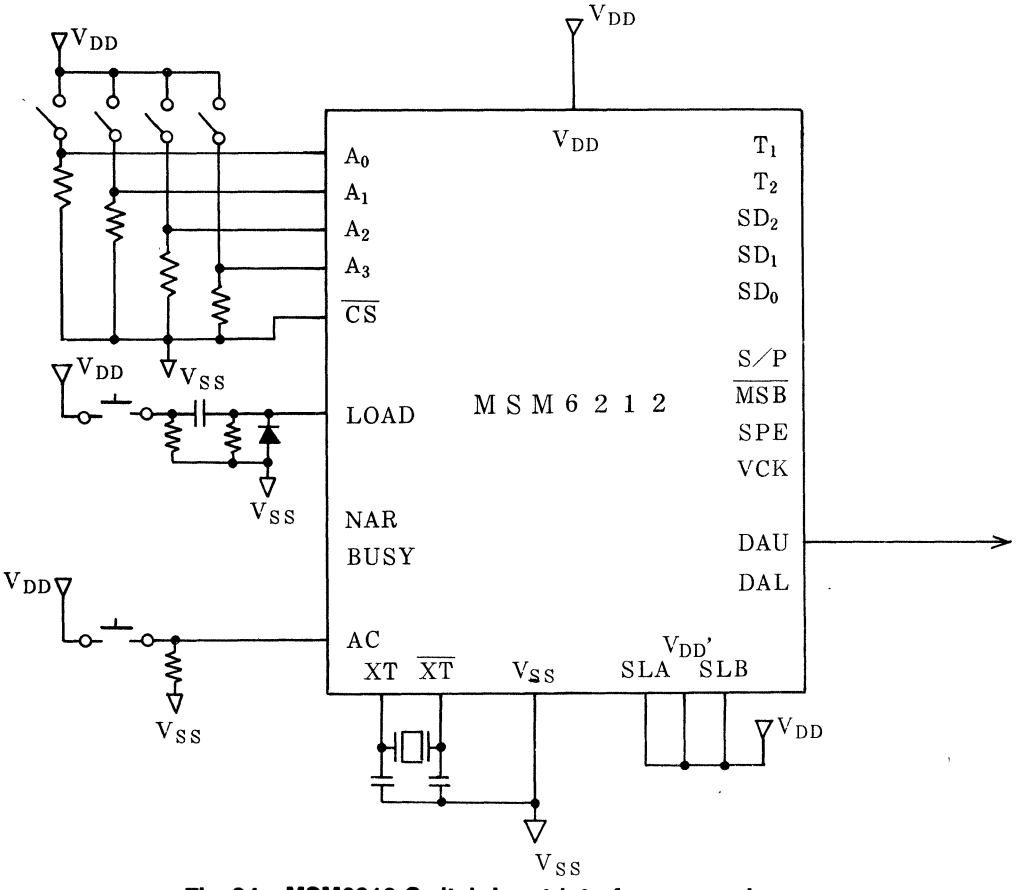


Fig. 21 MSM6212 Switch input interface example

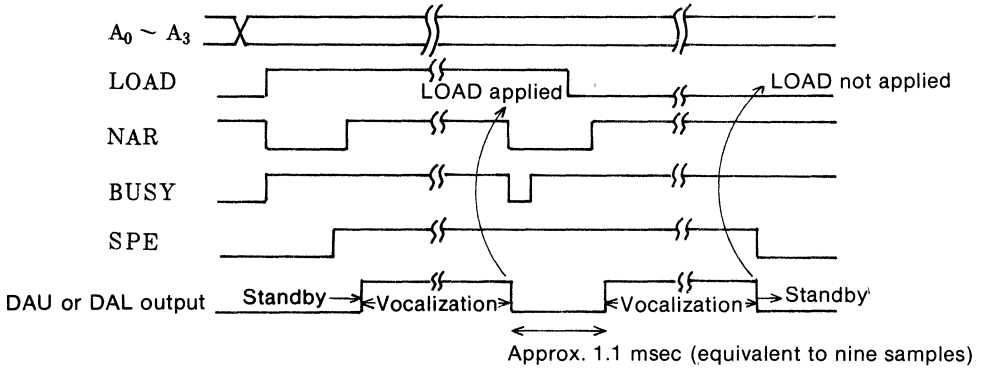
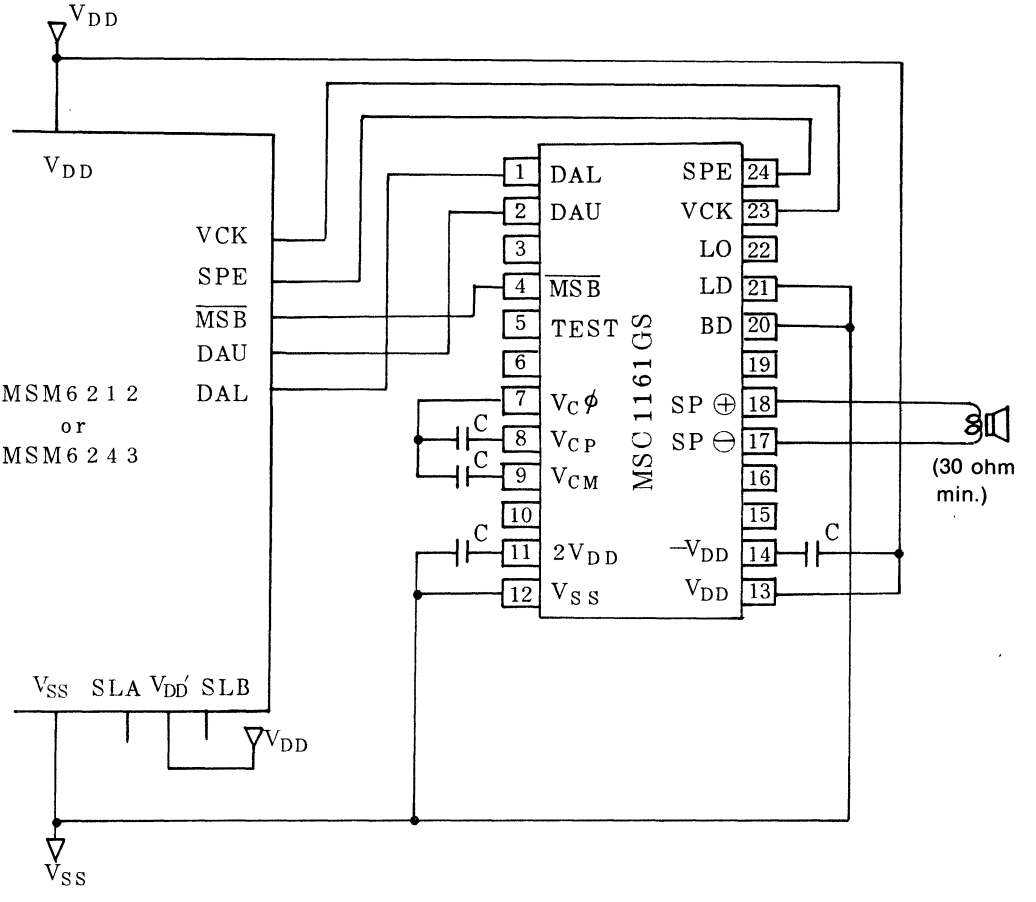


Fig. 22 MSM6243 Switch input timing diagram

■ Example of MSC1161 Interfacing with Voice Synthesis LSI

An example showing how Oki voice synthesis LSIs (MSM6212, MSM6243) are connected to MSC1161 (speaker driver IC) is given in Figure 23. Note that a speaker with mpedance of at least 30 ohms should be used.



Note: All capacitors are 0.1 μF min.

Fig. 23 Example of interface between MSC1161 and voice synthesis LSI

■ Examples of Inexpensive Voice Synthesis LSI Output Circuits

The following circuits are examples of inexpensive voice synthesis LSI systems constructed with fewer components in the output circuit.

(1) MSM5248 output circuit example

An output circuit example is shown in Figure 24, and the waveform of the output from the SP(+) pin is shown in Figure 25. A good degree of clarity is obtained with the waveform shown in Figure 26.

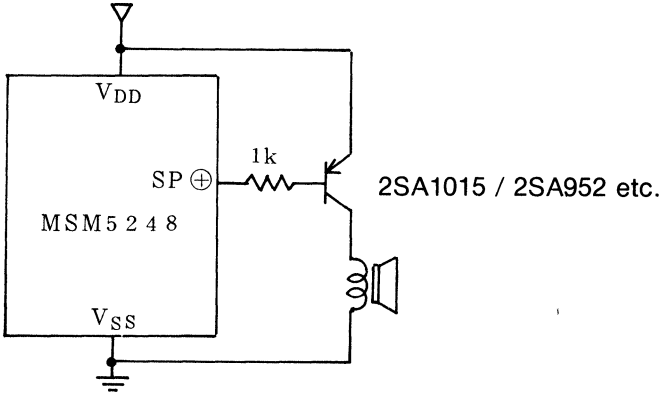


Fig. 24 Output circuit example

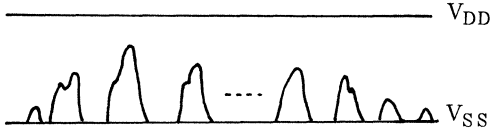


Fig. 25 Output waveform from SP (+)

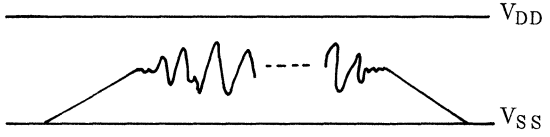


Fig. 26 Output waveform from SP(+) when DA converter accuracy is set to 9 bits

(2) Example of voltage type DA converter output circuit

An MSM6243 output circuit is shown in Figure 27 as a typical example of a voltage type DA converter. The LPF cut-off frequency (see Q10) can be changed by changing resistance and capacitance.

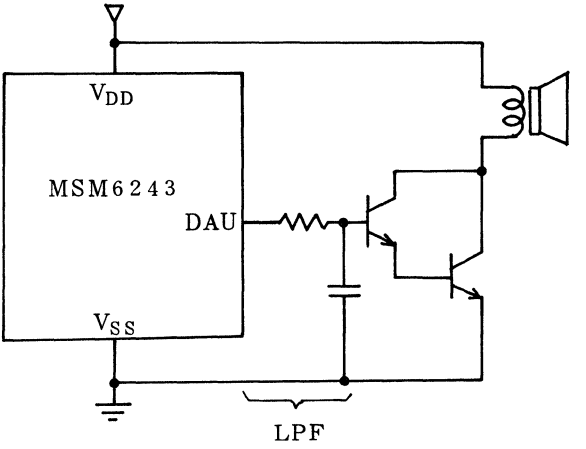


Fig. 27 MSM6243 output circuit example (for class A operation)

(3) Example of interfacing with regular audio amplifiers

An interface example where the speaker is driven by a regular audio amplifier (to achieve volume levels greater than that achieved by MSC1161) is shown in Figure 28. Although the circuit shown here includes a CR type LPF (see Q10), resistance in excess of 500 kohm is to be inserted beteween DAU and the audio amplifier input terminal even if the filter is removed. The reason for this is that the DAU output impedance varies considerably from -50% to +100% of the typical value due to ambient temperature conditions etc. The purpose of the resistance is to protect the audio amplifier output volume level from the effects of these changes.

The audio amplifier used should have a voltage gain of at least 40 dB.

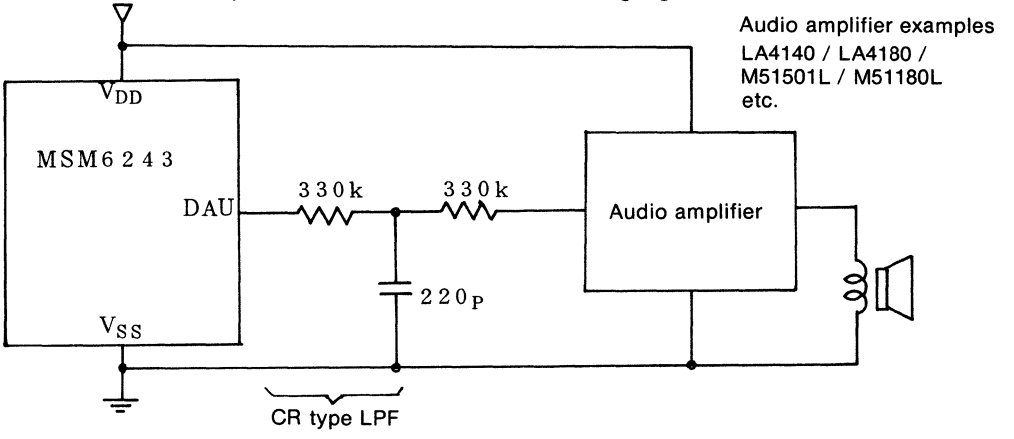


Fig. 28 Example of interfacing with regular audio amplifier

VOICE SYNTHESIS LSI LIBRARY

Apart from custom-order devices for specific user requirements, the following library of general-purpose voice synthesis LSIs (with built-in ROM) is available from Oki. Oki plans to further expand this library, and welcomes suggestions from its customers.

Voice synthesis LSI library (as of August 1987)

Device	Vocalized phrase
MSM5248-01	Happy Birthday (English)
MSM5248-04	Fanfare sound 
MSM5248-05	Merry Christmas And A Happy New Year (English)
MSM5248-09	"Irasshaimase — Arigato gozaimashita" (Japanese) (Welcome — Thank you)
MSM6243-02	Time announcement in Japanese.
MSM6243-21 (under development)	Time announcement in English

Q & A

Q1 What is the relationship between the vocalization time and quality in built-in ROM voice synthesis LSIs ?

A1 Parameters involved in determining vocalization time and quality include the sampling frequency, ADPCM word length, and the degree of data reduction when a compressed ADPCM method is used. These parameters are described below.

(1) Sampling frequency:
The vocalization bandwidth where voice can be synthesized is determined by the sampling frequency. According to the sampling theorem,

$$f_{BAND} = f_{SAMPLE} \times 1/2$$

where f_{BAND} is the upper limit of the frequency passband and f_{SAMPLE} is the sampling frequency
The effective bandwidth (f_{BAND} eff) where the ADPCM method response (see Figures 33 and 34) and the LPF used are considered can be stated as:

$$f_{BAND}\ \text{eff} = f_{SAMPLE} \times 1/2 \times 0.85$$

The hearing evaluation for different f_{SAMPLE} values are listed in Table 1.

Table 1

f_{SAMPLE}	Bandwidth	Hearing evaluation
8.2 kHz	DC ~ 3.49 kHz	Very clear sound including almost all vocalized sounds
6.55 kHz	DC ~ 2.78 kHz	High tone female voices sound as if the nose is blocked up
4.1 kHz	DC ~ 1.78 kHz	Both male and female voices sound as if the nose is blocked up

The "blocked up nose" sound is due to elimination of high frequency components normally included in the human voice. Since high frequency components are prevalent in constants (and in the "i" vowel), the effect is stronger at lower sampling frequencies.
In determining the sampling frequency, it is better to decide the most suitable value after listing to the source voice passed through a LPF.

(2) ADPCM word length:
The ADPCM word length is related to the S/N ratio. The 4-bit ADPCM method is better than the 3-bit ADPCM method by about 6 dB.

(3) Degree of data reduction in compressed ADPCM methods:
The quality of sound varies according to the degree of compression in compressed ADPCM methods. In compressed ADPCM, data can be compressed to 1/3 of the data used in straight ADPCM. Needless to say, the greater the degree of compression, the poorer the quality of sound becomes. The degree of compression is selected according to the intended purpose.

(4) Vocalization duration and quality of sound
An example of the relationship between vocalization duration and the quality of sound as determined by the above parameters when MSM6243 is used is outlined in Figure 29.

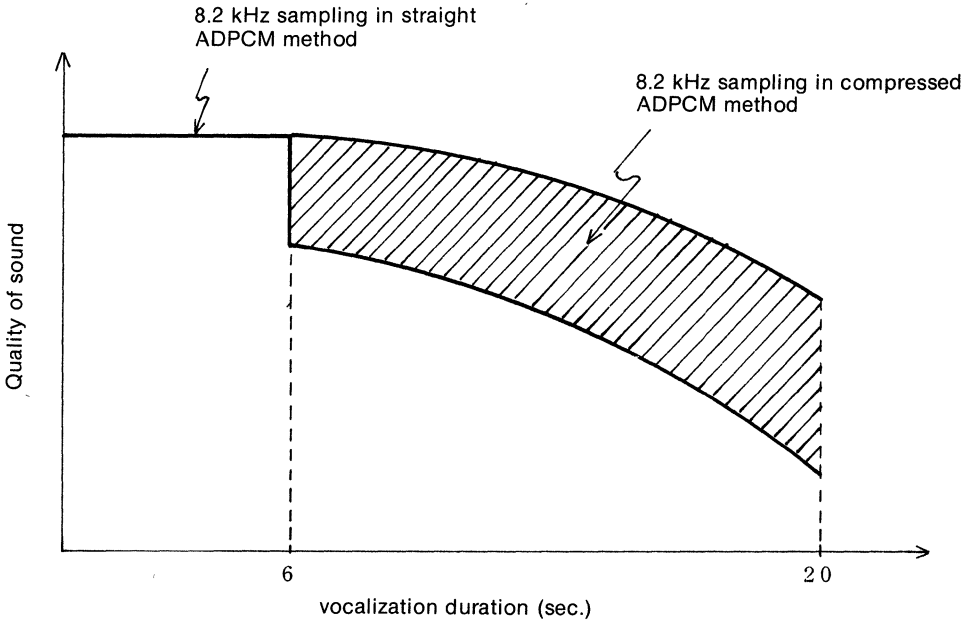


Fig. 29 Relationship between vocalization duration and quality of sound

The quality of sound is depicted as a range in the compressed ADPCM method in Figure 29. This is because the quality of sound is also dependent on the quality of the source sound vocalized statement specifications. And since the quality of sound cannot be expressed in absolute terms, it is shown here in relative terms.

(5) Examples of calculating the vocalization duration:
An example of calculation of the maximum vocalization duration in straight ADPCM for MSM6243 at a sampling frequency of 8.2 kHz is given below.

193,584 [bits] ÷ (8.2 [kHz] x 4 [bits]) = 5.90 [sec.]

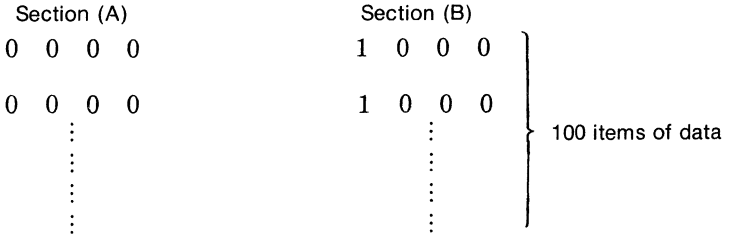
↑ ↑ ↑

Built-in ROM capacity f_{SAMPLE} **ADPCM word length**

The reason why the built-in ROM capacity is not 196,608 bits = 192 kbits x 1,024 bits/kbits is because the user will have a certain amount of area where use is disabled.

Q2 Although there is a certain amount of variation in the precision of the MSM5205 and MSM5218 DA converters, are there any methods for improving the S/N ratio?

A2 Yes. In terms of configuration in the above two DA converters, it is possible for the voice waveform precision to fall in the vicinity of the center waveform. Therefore, the S/N ratio can be improved by displacing the center of the waveform either up or down. This method is particularly effective in improving the S/N ratio for low level signals and in minimizing the residual noise during silent periods (such as the intervals between successive words). In practice, the waveform center can be shifted by adding additional data before or after the current ADPCM data (voice data) as indicated in Figure 30.



(Example where the ADPCM bit length is 4 bits)

Since an offset of about 5 mV per 2 items of data can be obtained in this case, shifts case, shifts of about 250 mV will require input of some 100 items of data.
The shift is upwards in (A), and downwards in (B). The number of data items should be equal in (A) and (B). The output waveform obtained when (A) is added at the start of the voice data and (B) is added at the end is shown in Figure 30.

Note that in since the dynamic range is compressed in the shifted sections, overflow may occur in some cases depending on the data, and this can result in clipping of the output sound. Reduce the sound pressure by about 20% and repeat the analysis. (See Q3 for additional information about overflow.)

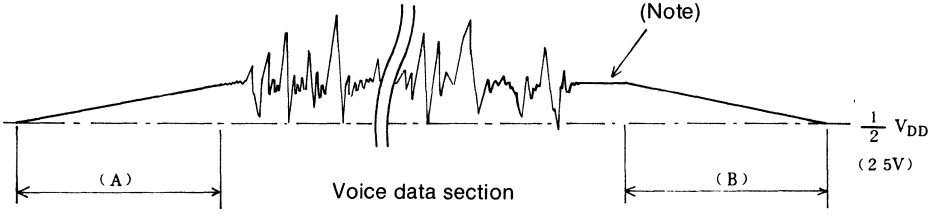


Fig. 30 DA converter output waveform

Note: There must be less voice data immediately prior to section (B). Input of some 20 to 30 msec of silence prior to the beginning of the voice is recommended.

Q3 When ADPCM data analyzed by MSM5218 was used in voice synthesis by MSM5205, noise was generated in the synthesized voice. How can this be overcome? There was no noise in the output from the MSM5218 DAOUT pin.

A3 The analysis must be repeated.
This is because MSM5205 is not equipped with the overflow prevention circuit featured in the MSM5218 internal computing circuits. Although sound synthesized by MSM5218 may be normal, overflow can occur during synthesis by MSM5205 resulting in the generation of noise. In this case, the data must be re-analyzed and the ADPCM data regenerated.
An example of a waveform where overflow has occurred, and a method for avoiding this overflow are outlined below.

(1) Waveforms where overflow occurs
Observation of the MSM5205 DA converter output waveform by oscilloscope shows the occurrence of an overflow.
(see Figure 31).

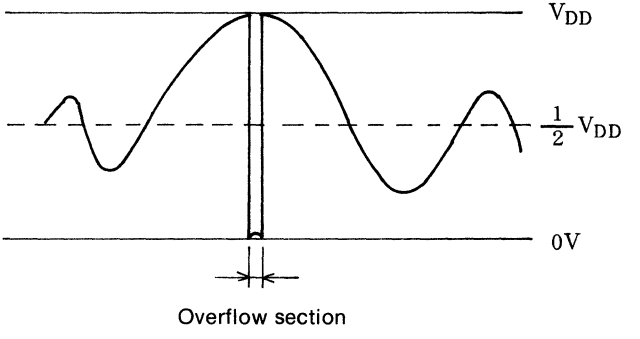


Fig. 31 Output waveform when overflow occurs

(2) Method used to avoid overflow
Even where the input waveform does not exceed the dynamic range when analyzed by MSM5218, output overflow can be generated by internal calculation error. Therefore, even if the input amplitude level reaches a maximum when analyzed by MSM5218, keeping the level within 80% of the dynamic range (see Figure 32) will ensure that no overflow occurs in the MSM5205 output and no noise is generated in the synthesized sound.

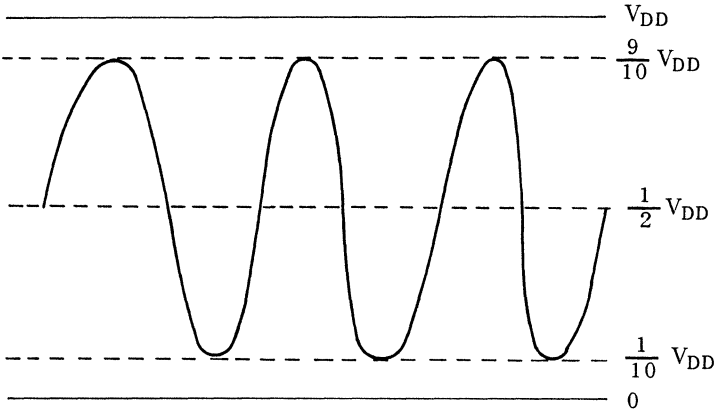


Fig. 32 Waveform with amplitude kept within 80% of the dynamic range

Q4 What kind of frequency response is achieved in the output waveform in respect to Oki ADPCM input waveforms?

A4 The frequency response achieved in output waveforms when sinewave input waveforms are applied is outlined in Figures 33 and 34.
Since these diagrams show the frequency response when 4-bit ADPCM data is used with an 8 kHz sampling frequency, an increase in the sampling frequency will result in a shift of the frequency response to the right.

(1) When input waveform is a 1/2 scale sinewave (1/2VDD Vp-p)

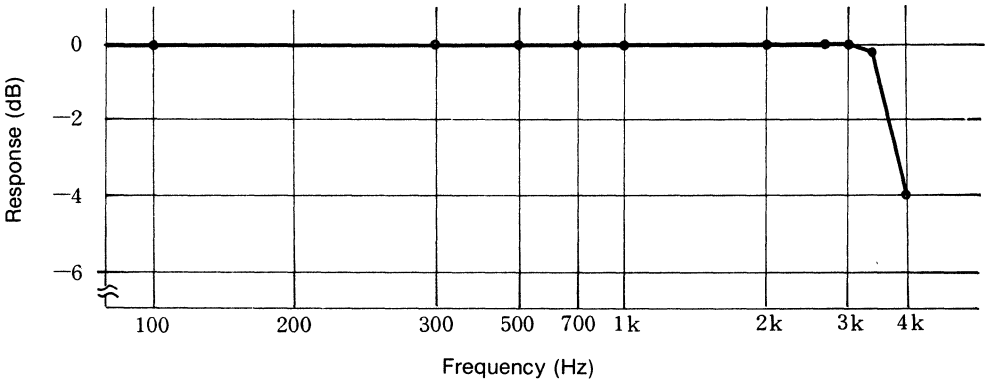


Fig. 33 Oki ADPCM frequency response (1)

(2) When input waveform is a full scale sinewave (VDD Vp-p)

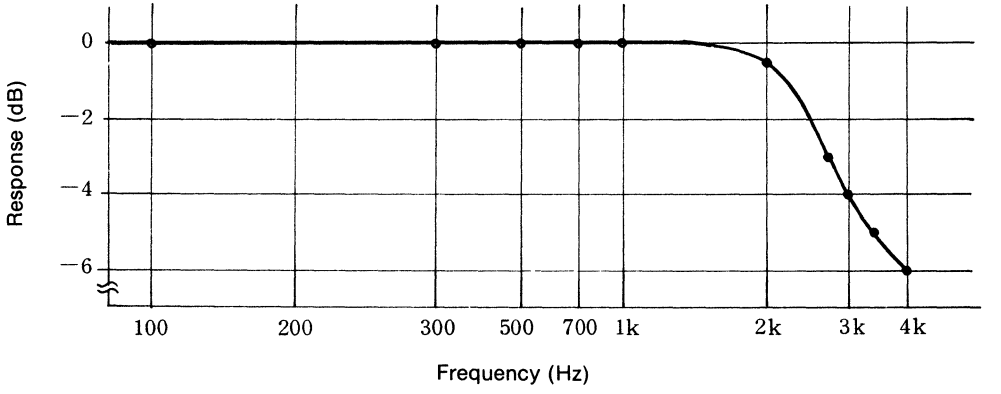


Fig. 34 Oki ADPCM frequency response (2)

Q5 What does it mean to say that the DA converter output from MSM6243 etc is a "class A output" or "class B output"?

A5 MSM6243 and other devices are equipped with two DA converter output pins DAU and DAL. In class A output mode (the normal mode), the output waveform only appears at the DAU pin with the VDD/2 potential at the amplitude center to obtain maximum amplitude for Vss thru VDD. Class B output mode is used in interfacing with MSC1161 (note). The upper half of the waveform above the class A output amplitude center appears at the DAU pin and the lower half of the waveform appears at the DAL pin with the main amplitude direction as the positive direction. The comparative waveforms are shown in Figure 35.

Where class B is multiplied by 1, the amplitude scale is twice the class A level, and likewise class B multiplied by 2 and 4 result in class A multiplied by 4 and 8 respectively.
In waveforms where the VDD level is exceeded, however, the output is clamped at V_{DD}.

Note: The method described in MSM6212 Switch Input Interface Example at page 174.

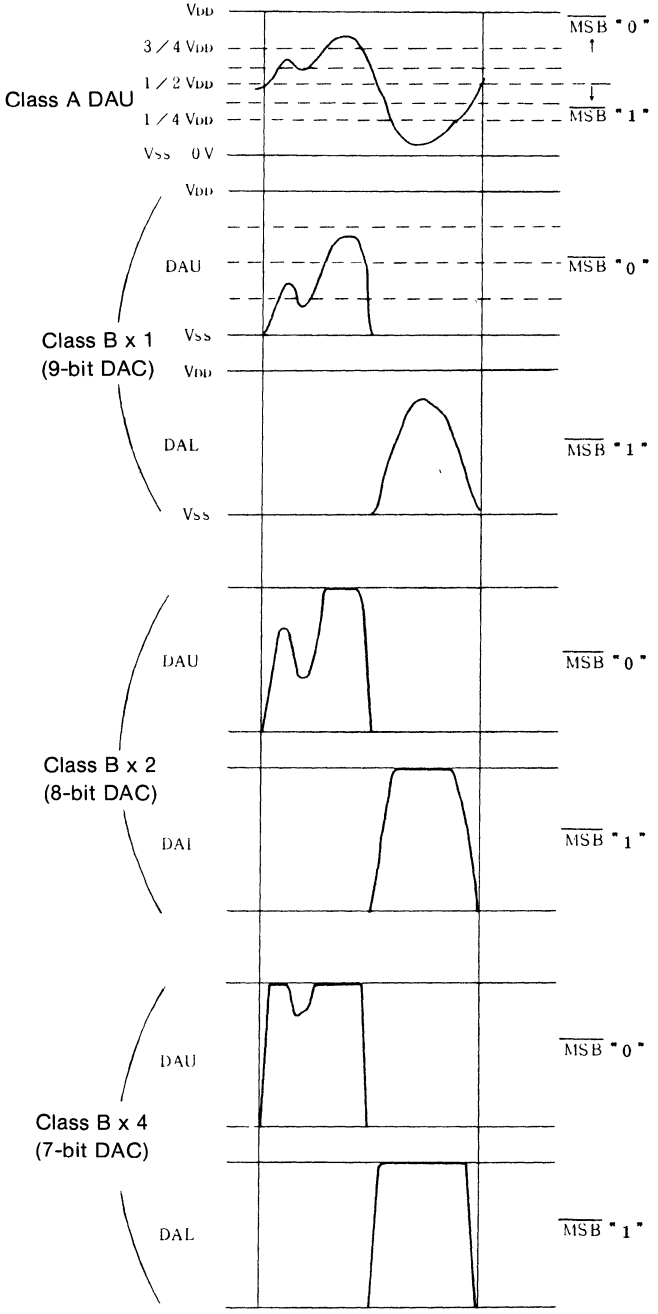


Fig. 35 Comparative waveforms

Q6 What is the best way to form a sinewave with MSM5205?

A6 By input of the following data values. The corresponding output waveforms are also shown. The data used is 4-bit data (in hexadecimal notation).

(1) To obtain an output of 1.5 Vp-p
Use the following input data.

0,0,0,3,3,3,7,F,7,F,4,C,4,C
Then 4,0,9,C,8,1 repeatedly.

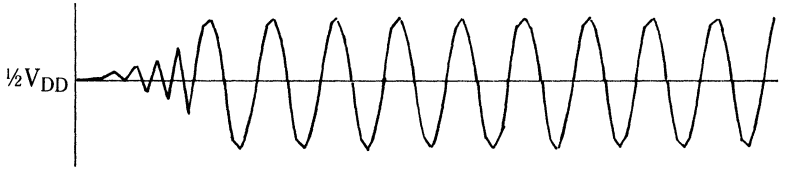


Fig. 36 1.5 Vp-p output

(2) To obtain an output of 0.85 Vp-p
Use the following input data.

0,0,0,B,B,B,7,F,7,F,4,C,0,0
Then 4,0,9,C,8,1 repeatedly.

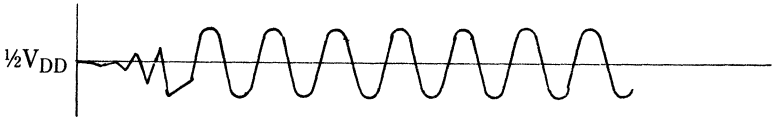


Fig. 37 0.85 Vp-p output

(3) To obtain an output of 2.6 Vp-p
Use the following input data.

0,0,0,0,7,F,7,F,7,F,4,C,0,0
Then 4,0,9,C,8,1 repeatedly.

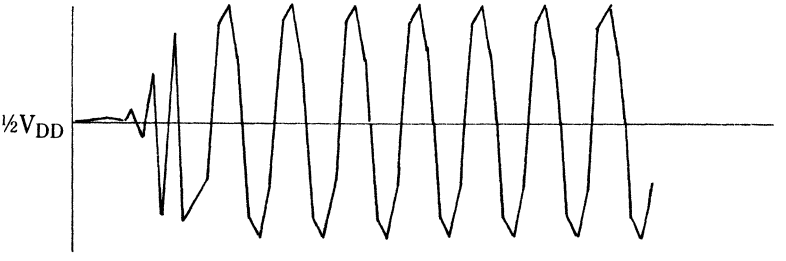


Fig. 38 2.6 Vp-p output

Q7 How should the MSM5205 and MSM5218 reset input timing be best set?

A7 The MSM5205 and MSM5218 reset should be input according to the following timing.

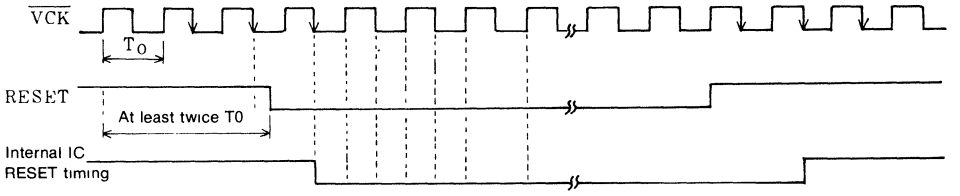


Fig. 39 MSM5205 reset timing

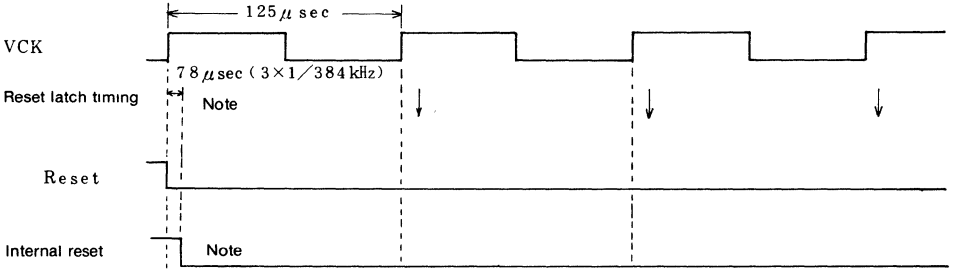


Fig. 40 MSM5218 reset timing (8 kHz sampling example)

Note: The reset signal is latched within the LSI by the reset latch timing. Analysis is commenced by switching the external reset signal from H to L before this timing. Switching is probably best achieved by the leading edge of the VCK signal.

Q8 Why is a low-pass filter required in the voice synthesis output?

A8 Low-pass filters (LPF) are designed to pass only those frequency components below a certain frequency when the input contains a number of different components. Since the voice synthesis output is obtained from a DA converter output, the output waveform is a stepwise waveform as indicated in Figure 41.

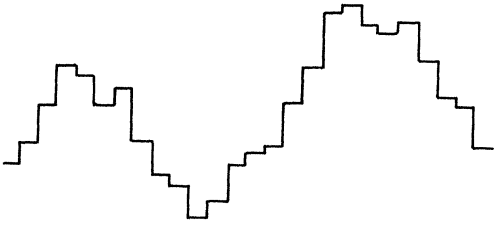


Fig. 41 DA converter voice output waveform

This waveform contains certain high frequency noise components, and since the sampling theorem states that sampling is not effective unless only frequency components below half the sampling frequency are obtained, the unwanted high frequency components are removed by the LPF. The LPF output waveform is as shown in Figure 42.

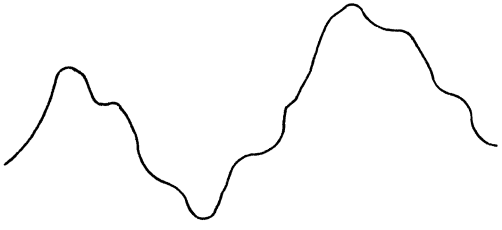


Fig. 42 LPF output waveform

Q9 How is the LPF cut-off frequency best determined?

A9 In an ideal LPF, all frequencies above a certain level are filtered out. In practice, however, frequencies are attenuated at a certain rate (slope) from a particular level. This slope is usually expressed in terms of dB per octave (dB/oct). For example, in a filter with a slope of -12 dB/oct, the output is attenuated by -12 dB (that is, reduced to 1/4) for each octave increase of the frequency (that is, each time the frequency is doubled).

The frequency where the attenuation commences is called the cut-off frequency (note). The best cut-off frequency for any situation will depend on the sampling frequency, the attenuation slope, and the frequency components in the source sound. The usual design criteria is the degree of attenuation (that is, how many dB) at half the sampling frequency (f_{SAM}).

A number of reference values are listed in Table 2. Since the optimum value as determined for the frequency components in the source sound varies considerably, ddit is best to decide on the basis of actual listening.

Table 2 Relationship between filter attenuation characteristics, cut-off frequency, and sampling frequency

Filter attenuation characteristics (dB/oct)	Cut-off frequency	Gain at 0.5 f_{SAM} (dB)	Diagram number
-12	0.3 f_{SAM}	- 8.7	①
-18	0.33 f_{SAM}	-11	—
-24	0.35 f_{SAM}	-12.5	②
-48	0.38 f_{SAM}	-19	—

Although high frequency noise components are attenuated more efficiently when the attenuation characteristics are "sharper", a larger number of structural elements are required, making such a filter uneconomical. The filter frequency response when f_{SAMPLE} is 8 kHz is outlined in Figure 43 for reference purposes.

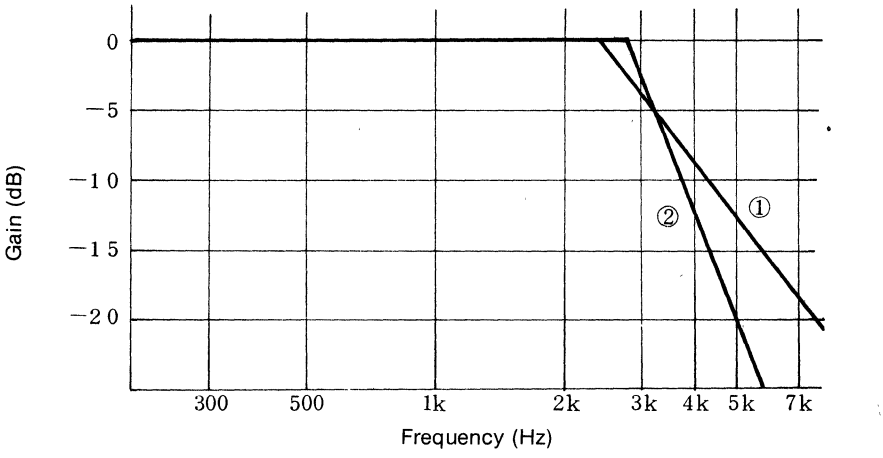


Fig. 43 f_{SAMPLE} 8 kHz filter frequency response

Note: Strictly speaking, the cut-off frequency is not defined as the point where attenuation is commenced. In Butterworth type filters, the cut-off frequency is the "point -3 dB below the overall characteristics", while in Chebyshev type filters it is defined as the "point where the maximum ripple width within the set passband first appears". Where strict adherence to either definition is not required, the cut-off frequency can be assumed to be the point where attenuation is commenced.

Q10 What is the configuration of low-cost filters designed for voice synthesis applications?

A10 The most common types of active filters (filters with active elements) used are the Butterworth, Bessel, and Chebyshev filters. Each type is used for different purposes.
The Butterworth filter puts emphasis on the flatness of the passband and is less strict in terms of attenuation characteristics and transient response performance than the Bessel and Chebyshev filters.
In the LPF used for voice synthesis where the passband attenuation characteristics do not need to be perfectly flat, a Chebyshev filter capable of achieving sharp attenuation characteristics with a small number of component parts should be considered. Chebyshev filters can be designed with suitable ripple width and attenuation characteristics.
Note that if the frequency response of the speaker rolls off at the desired cut-off frequency, the LPF will not be required.

Configuration
A 1-pole RC LPF where no active elements are used is shown in Figure 44, and the corresponding transmission characteristics can be expressed in the following way.

$$F(j\omega) = \frac{\ell_o}{\ell_i} = \frac{1}{1 + i\left(\frac{\omega}{\omega_0}\right)} \quad \cdots\cdots\cdots\cdots \quad (1)$$

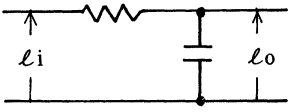


Fig. 44 1-pole RC LPF

where

$$\omega_0 = \frac{1}{CR} \quad (\omega_0 = 2\pi f_0)$$

fo: cut-off frequency

An F(jw) plot is shown in Figure 45.
The frequency response shown in this diagram is cut off at -6 dB/oct above frequency wo where w_0 is the -3 dB value.

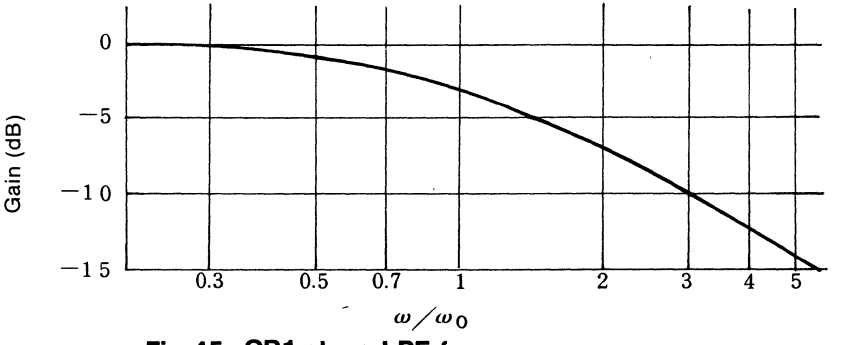


Fig. 45 CR1 stage LPF frequency response

The circuit configuration of a 2nd order Chebyshev filter is shown in Figure 46.

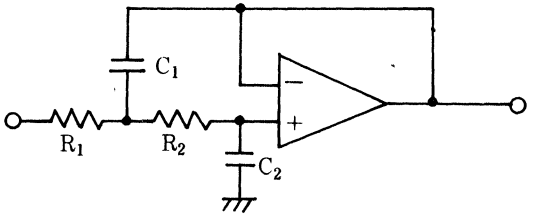


Fig. 46 2nd order Chebyshev type filter

The transmission characteristics for this circuit can be expressed in the following way.

$$F(j\omega) = \frac{\ell_0}{\ell_i} \quad \frac{1}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{1}{Q} \cdot \frac{\omega}{\omega_0}}$$

$$Q = \frac{\sqrt{R_1 C_1 R_2 C_2}}{C_2 (R_1 + R_2)} \qquad \omega_0 = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$$

The active element used in this circuit is assumed to be an OP amplifier voltage follower with a gain of 1.

$$C_1 = \frac{2Q}{\omega_0 R} \qquad C_2 = \frac{1}{2Q\omega_0 R}$$

Higher order Chebyshev filter design

Even numbered higher order filters such as 4th and 6th order filters can be divided into 2nd order elements. And odd numbered higher order filters such as 3rd and 5th order filters can be divided into 2nd order and 1st order (CR1 stage passive filter) elements.

A 4th order filter, for example, can be divided into two 2nd order element stages as shown in Figure 47. And by determining the fn and qn factors in each stage, the filter configuration can be easily achieved.

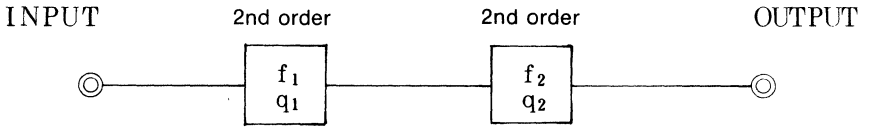


Fig. 47 4th order LPF

The attenuation characteristics of Chebyshev filters can be changed depending on the ripple tolerance within the passband. The fn and qn settings will also vary according to the tolerance.

A list of fn and qn values for Chebyshev filters is given in Table 3 below.

Table 3 Chebyshev LPF and HPF fn and qn values

	Ripple = 0 1 dB		Ripple = 0 2 dB		Ripple = 0.25 dB		Ripple = 0 3 dB		Ripple = 0 5 dB	
	fn	qn	fn	qn	fn	qn	fn	qn	fn	qn
2nd order	1 8204497	0 7673593	1 5351966	0 7966418	1 4539722	0 8092536	1 3911667	0 8210811	1 231418	0 8637210
3rd order	1 2999029 0 9694057	1 3490276 0 5*	1 1889612 0 8146341	1 4595033 0 5*	1 1569921 0 7672227	1 5080264 0 5*	1 1321861 0 7292773	1 5524768 0 5*	1 0688535 0 6254565	1 7061895 0 5*
4th order	1 1532699 0 7892557	2 1829303 0 6188010	1 0948338 0 7011094	2 4350125 0 6458968	1 0779389 0 6744223	2 5361100 0 6572494	1 0648159 0 6532428	2 6279020 0 6677803	1 0312704 0 5970024	2 9405542 0 7051102
5th order	1 0931318 0 7974460 0 5389143	3 2820141 0 9145215 0 5*	1 0570753 0 7472558 0 4614106	3 7068586 1 0009079 0 5*	1 0466301 0 7324054 0 4369509	3 8756825 1 0359319 0 5*	1 0385110 0 7207553 0 4171291	4 0283601 1 0678979 0 5*	1 0177347 0 6904832 0 3623196	4 5449633 1 1778056 0 5*
6th order	1 0627261 0 8344903 0 5131875	4 6329012 1 3315707 0 5994600	1 0382299 0 8030621 0 4603216	5 2689021 1 4917187 0 6259511	1 0311242 0 7938542 0 4440628	5 5204164 1 5556533 0 6370268	1 0255981 0 7866630 0 4310754	5 7474076 1 6135959 0 6472924	1 0114459 0 7681212 0 3962290	6 5128456 1 8103772 0 6836390

The 0 5* in the qn column denotes CR1 stage 1st order

Example

The following example shows how a 5th order Chebyshev filter would actually be designed. A ripple tolerance of 0.5 dB is assumed. The circuit diagram is shown in Figure 48.

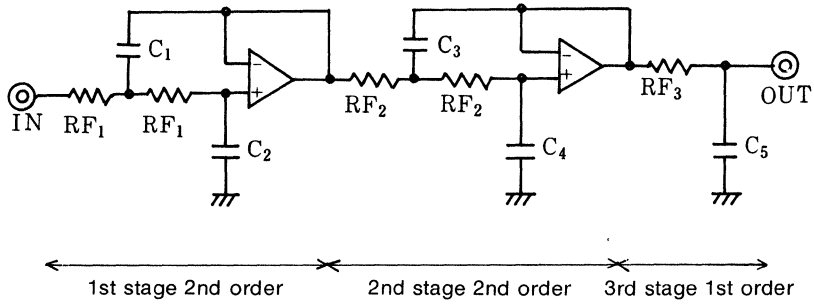


Fig. 48 5th order Chebyshev LPF

The fn and qn values have already been listed in Table 3. Where ripple 0.5 dB for a 5th order filter, the 1st stage 2nd order fn=1.0177347 and qn=4.5449633 the 2nd stage 2nd order fn=0.6904832 and qn=1.1778056 the 3rd stage 1st order fn=0.3623196 and qn=0.5. The constants can thus be calculated using these values. (begin-ind) A cut-off frequency of 2.8 kHz is selected. This value is then substituted in equations introduced earlier for calculating 1st and 2nd order constants.

1st stage 2nd order

Assume R_{F1} = 51 kohm

$$f_0 = 2800 \times 1.0177347 \div 2850\,(\mathrm{Hz})$$

$$C_1 = \frac{2Q}{\omega_0 R_F} = \frac{2qn}{2\pi f_0 R_F} = \frac{2 \times 4.5449633}{2\pi \times 2850 \times 51 \times 10^3} = 9953\,(\mathrm{pF})$$

$$C_2 = \frac{1}{2Q\omega_0 R_F} = \frac{1}{2qn2\pi f_0 R_F} = \frac{1}{2 \times 4.5449633 \times 2\pi \times 2850 \times 51 \times 10^3}$$

$$= 120\,(\mathrm{pF})$$

2nd stage 2nd order

Assume R_{F2} = 56 kohm

$$f_0 = 2800 \times 0.6904832 \div 1933\,(\mathrm{Hz})$$

$$C_3 = \frac{2Q}{\omega_0 R_F} = \frac{2 \times 1.1778056}{2\pi \times 1933 \times 56 \times 10^3} = 3463\,(\mathrm{pF})$$

$$C_4 = \frac{1}{2Q\omega_0 R_F} = \frac{1}{2 \times 1.1778056 \times 2\pi \times 1933 \times 56 \times 10^3} = 624\,(\mathrm{pF})$$

3rd stage 1st order

Assume R_{F3} = 68 kohm

$$f_0 = 2800 \times 0.3623196 \fallingdotseq 1014(\mathrm{Hz})$$

$$C_5 = \frac{1}{\omega_0 R_F} = \frac{1}{2\pi f_0 R_{F3}} = \frac{1}{2\pi \times 1014 \times 68 \times 10^3} = 2308(\mathrm{pF})$$

In this case, the RF value can be changed to approach the value of a real capacitor. If the values of C1 and C2 are increased 1.5 times, RF1 is more or less divided by 1.5. By selecting values which approach capacitor values, the filter constants finally selected are as shown in Figure 49.

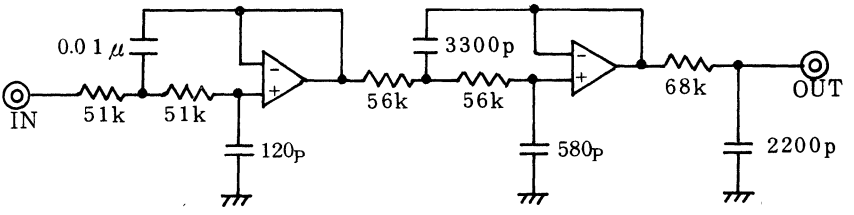


Fig. 49 Designed filter (5th order)

The filter characteristics for this filter can then be plotted. The transmission characteristics for the 1st and 2nd stage 2nd order filter elements can be expressed in the following way.

$$F(j\omega) = \frac{1}{1 - (\frac{\omega}{\omega_0})^2 + j\frac{1}{Q} \cdot \frac{\omega}{\omega_0}}$$

And the transmission characteristics for the 3rd stage 1st order filter element can be expressed by

$$F(j\omega) = \frac{1}{1 + j(\frac{\omega}{\omega_0})}$$

When, for example, w wo in the 1st stage filter,

$$F(j\omega_0) = \frac{1}{1 - (1)^2 + j\frac{1}{Q} \times 1} = -jQ = -4.5449633j$$

If the absolute input/output voltage ratio is expressed in dB,

$$20 \log 4.545 = 13.15 \text{ (dB)}$$

That is, the level is 13.15 dB when the frequency is 2850 Hz. The plot obtained inserting successive values in this equation is shown as a dashed line in Figure 50. And similar plots obtained for the 2nd and 3rd stages are shown as the dot-dash and double-dot-dash lines. The overall characteristics are shown by the full line.
line.
According to the overall characteristics, the use of values approaching actual capacitors gives a maximum ripple of 0.6 dB and a cut-off frequency of about 2.9 kHz.

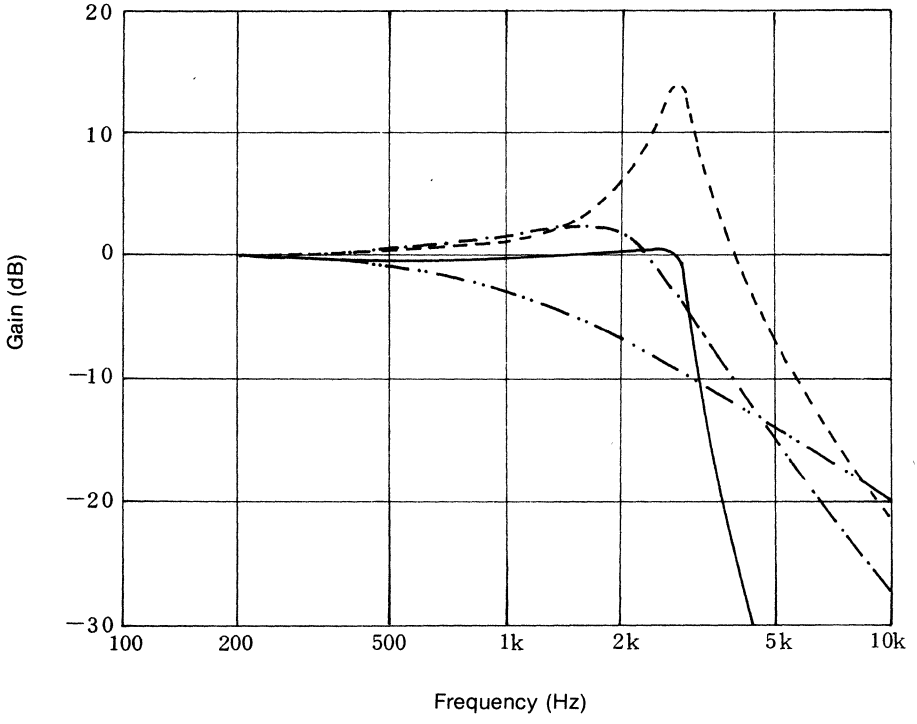


Fig. 50 Frequency response of the designed filter (5th order)

The constants and frequency response for a 3rd order Chebyshev filter designed in the same manner are shown in Figures 51 and 52.
The full line in Figure 52 represents the overall characteristics.
According to these overall characteristics, the use of values approaching actual capacitors gives a maximum ripple of 3 dB and a cut-off frequency of about 2.56 kHz.

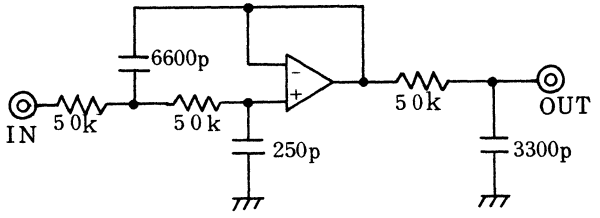


Fig. 51 Designed filter (3rd order)

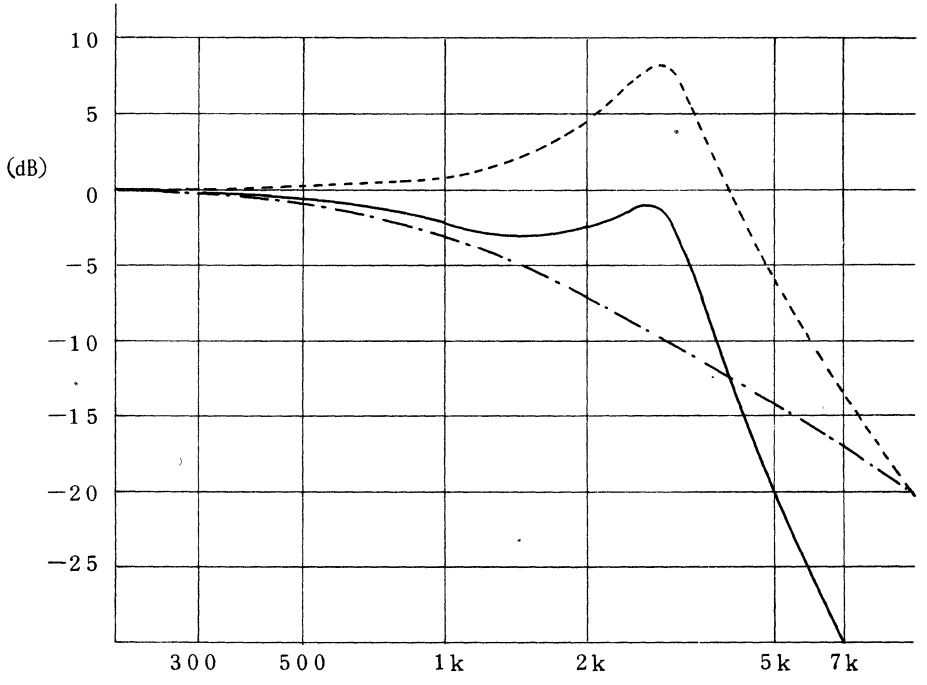


Fig. 52 Designed filter frequency response (3rd order)

Q11 How should the filter be connected where the MSM6243 voice output pin output impedance is 60 kohm (typ)?

A11 An output impedance of 60 kohm is equivalent to connecting 60 kohms to a 0 ohm output impedance pin (ideal constant voltage source).
If ambient temperature fluctuations and manufacturing tolerance spread are considered, this 60 kohm output impedance can vary from -50% to 100%, making filter constant settings impossible.
Hence, it is recommended that a voltage follower be inserted before the filter as shown in Figure 53 to vary the impedance.
(A voltage follower should also be used when MSM5205, MSM5218, MSM6212, MSM6258, and other devices are used.)

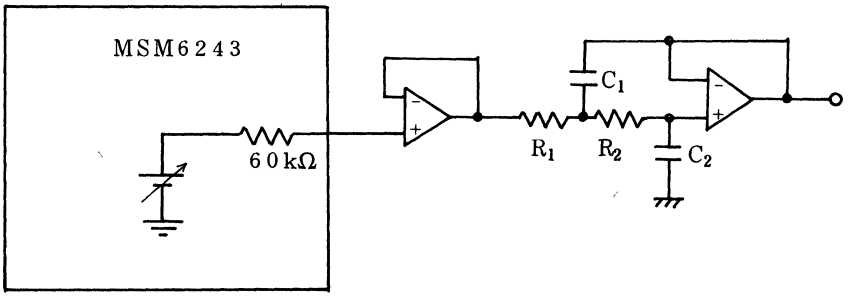


Fig. 53 MSM6243 and filter interface

Q12 Can the MSM5205 voice output be connected directly to an audio amplifier?

A12 **Yes. But note that the amplifier input impedance and allowable input amplitude must be considered.**
With a preamplifier stage input impedance of about 47 kohm, the normal input amplitude is 200 mVp-p. Since the MSM5205 voice output impedance is approximately 100 kohm and the output amplitude about 4 Vp-p (V_{DD} = 5 V when unloaded), a load has to be connected to reduce the amplitude to about 1/20. Likewise with other devices, direct connection to an audio amplifier is enabled by connecting a load to match the output impedance. See Figure 54.

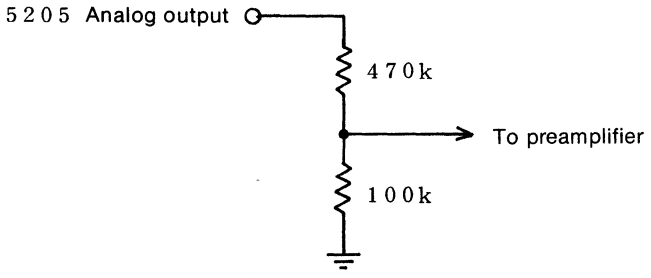


Fig. 54 Audio amplifier connection

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