1.0 Features

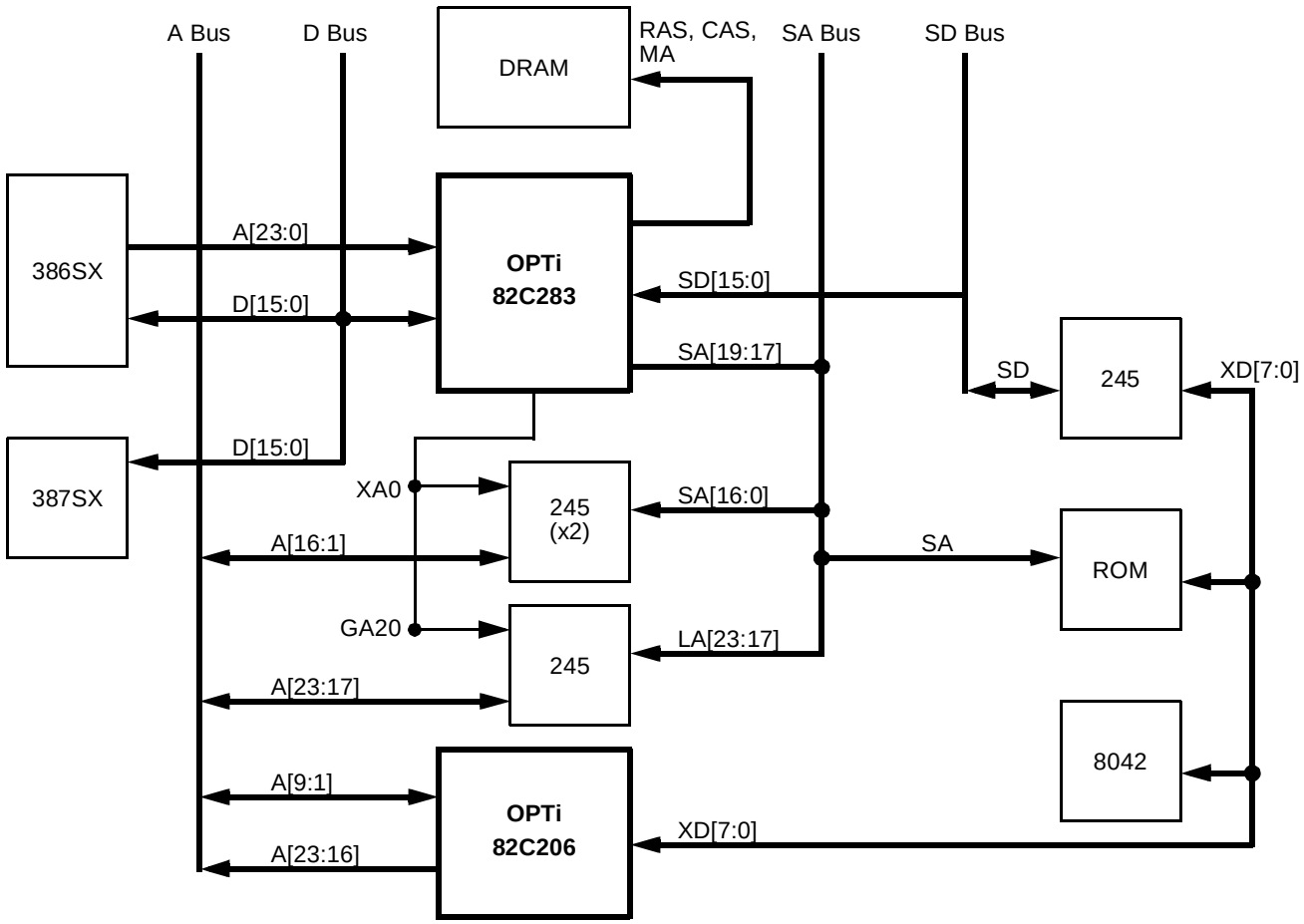
- Flexible DRAM banks configuration
  - Supports 256K, 1M and 4M DRAM
- Block interleave mode operations
  - Block interleaving at a block size of 512 bytes
- BIOS shadow RAM
  - Shadow RAM for system, video and adapter BIOS
- Memory remapping
- Flexible multiplexed DRAM address
- Programmable AT bus clock
- Turbo switch
- 160-pin PQFP (Plastic Quad Flat Pack)

2.0 Overview

The 82C283 is a highly integrated, AT system logic VLSI chip for high-end 386SX/AT systems. It integrates a local memory controller (local memory is on-board memory), AT bus controller, and data bus controller into one chip. It is designed for systems running at 16MHz, 20MHz, 25MHz, and 33MHz*. A high performance, compact 386SX/AT system is readily implemented with the 82C283 and a standard peripheral controller like OPTi's 82C206 or the 82C100 (with Dallas Semiconductor (DS1287).

*Rev. B only

Figure 2-1 System Block Diagram



3.0 Signal Definitions

Figure 3-1 Pin Diagram

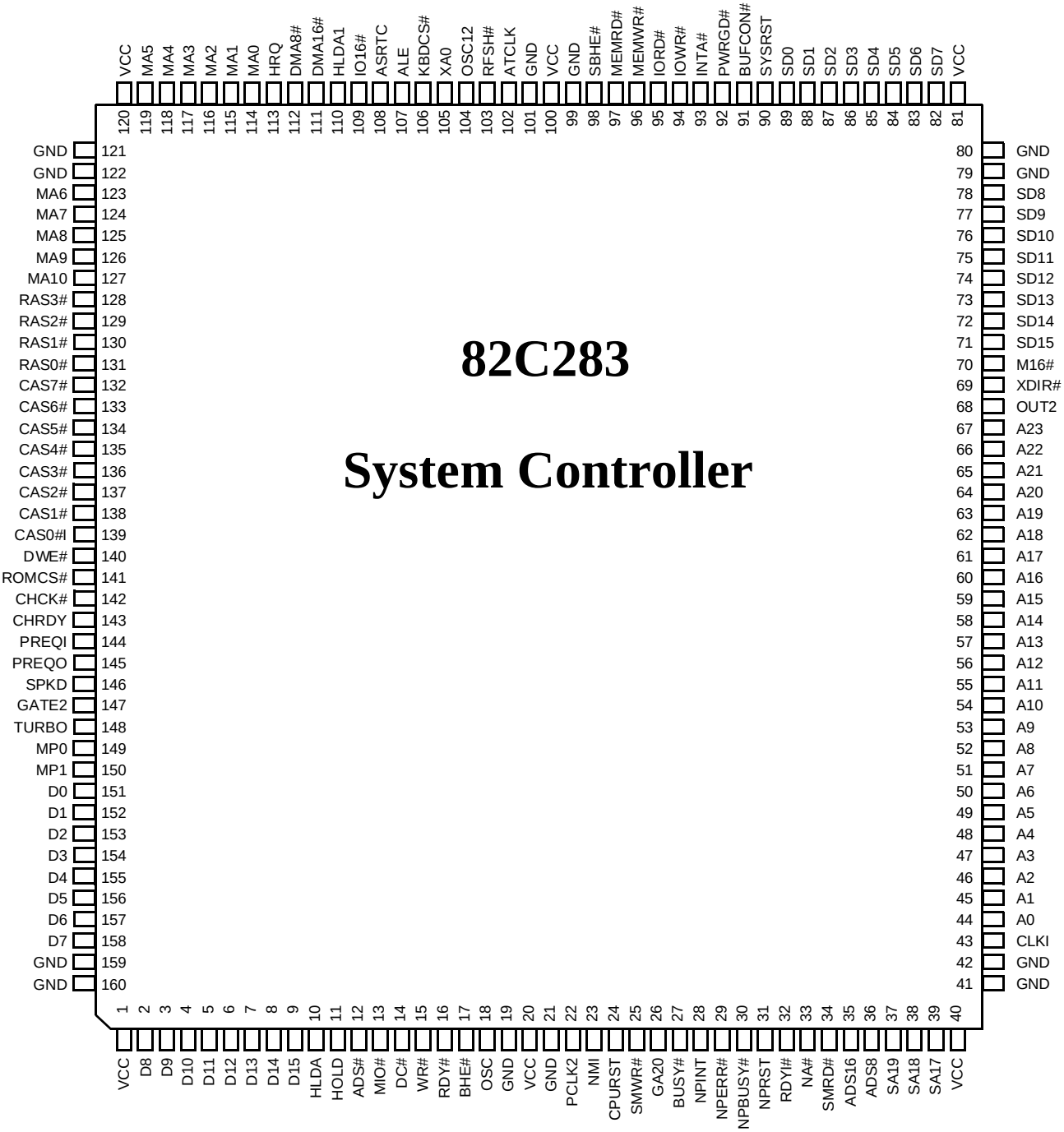


Table 3-1 Numerical Pin Cross-Reference List

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VCC	41	GND	81	VCC	121	GND
2	D8	42	GND	82	SD7	122	GND
3	D9	43	CLKI	83	SD6	123	MA6
4	D10	44	A0	84	SD5	124	MA7
5	D11	45	A1	85	SD4	125	MA8
6	D12	46	A2	86	SD3	126	MA9
7	D13	47	A3	87	SD2	127	MA10
8	D14	48	A4	88	SD1	128	RAS3#
9	D15	49	A5	89	SD0	129	RAS2#
10	HLDA	50	A6	90	SYSRST	130	RAS1#
11	HOLD	51	A7	91	BUFCON#	131	RAS0#
12	ADS#	52	A8	92	PRWGD#	132	CAS7#
13	MIO#	53	A9	93	INTA#	133	CAS6#
14	DC#	54	A10	94	IOWR#	134	CAS5#
15	WR#	55	A11	95	IORD#	135	CAS4#
16	RDY#	56	A12	96	MEMWR#	136	CAS3#
17	BHE#	57	A13	97	MEMRD#	137	CAS2#
18	OSC	58	A14	98	SBHE#	138	CAS1#
19	GND	59	A15	99	GND	139	CAS0#
20	VCC	60	A16	100	VCC	140	DWE#
21	GND	61	A17	101	GND	141	ROMCS#
22	PCLK2	62	A18	102	ATCLK	142	CHCK#
23	NMI	63	A19	103	RFSH#	143	CHRDY
24	CPURST	64	A20	104	OSC12	144	PREQI
25	SMWR#	65	A21	105	XA0	145	PREQO
26	GA20	66	A22	106	KBDCS#	146	SPKD
27	BUSY#	67	A23	107	ALE	147	GATE2
28	NPINT	68	OUT2	108	ASRTC	148	TURBO
29	NPERR#	69	XDIR#	109	IO16#	149	MP0
30	NPBUSY#	70	M16#	110	HLDA1	150	MP1
31	NPRST	71	SD15	111	DMA16#	151	D0
32	RDYI#	72	SD14	112	DMA8#	152	D1
33	NA#	73	SD13	113	HRQ	153	D2
34	SMRD#	74	SD12	114	MA0	154	D3
35	ADS16	75	SD11	115	MA1	155	D4
36	ADS8	76	SD10	116	MA2	156	D5
37	SA19	77	SD9	117	MA3	157	D6
38	SA18	78	SD8	118	MA4	158	D7
39	SA17	79	GND	119	MA5	159	GND
40	VCC	80	GND	120	VCC	160	GND

Table 3-2 Alphabetical Pin Cross Reference List

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	44	CAS7#	132	HLDA1	110	RAS2#	129
A1	45	CHCK#	142	HOLD	11	RAS3#	128
A2	46	CHRDY	143	HRQ	113	RDY#	16
A3	47	CLKI	43	INTA#	93	RDYI#	32
A4	48	CPURST	24	IO16#	109	RFSH#	103
A5	49	D0	151	IORD#	95	ROMCS#	141
A6	50	D1	152	IOWR#	94	SA19	37
A7	51	D2	153	KBDCS#	106	SA18	38
A8	52	D3	154	M16#	70	SA17	39
A9	53	D4	155	MA0	114	SBHE#	98
A10	54	D5	156	MA1	115	SD0	89
A11	55	D6	157	MA2	116	SD1	88
A12	56	D7	158	MA3	117	SD2	87
A13	57	D8	2	MA4	118	SD3	86
A14	58	D9	3	MA5	119	SD4	85
A15	59	D10	4	MA6	123	SD5	84
A16	60	D11	5	MA7	124	SD6	83
A17	61	D12	6	MA8	125	SD7	82
A18	62	D13	7	MA9	126	SD8	78
A19	63	D14	8	MA10	127	SD9	77
A20	64	D15	9	MIO#	13	SD10	76
A21	65	DC#	14	MP0	149	SD11	75
A22	66	DMA8#	112	MP1	150	SD12	74
A23	67	DAM16#	111	MEMRD#	97	SD13	73
ADS#	12	DWE#	140	MEMWR#	96	SD14	72
ADS8	36	GA20	26	NA#	33	SD15	71
ADS16	35	GATE2	147	NMI	23	SMRD#	34
ALE	107	GND	19	NPBUSY#	30	SMWR#	25
ASRTC	108	GND	21	NPERR#	29	SPKD	146
ATCLK	102	GND	41	NPINT	28	SYSRST	90
BHE#	17	GND	42	NPRST	31	TURBO	148
BUFCON#	91	GND	79	OSC	18	VCC	1
BUSY#	27	GND	80	OSC12	104	VCC	20
CAS0#	139	GND	99	OUT2	68	VCC	40
CAS1#	138	GND	101	PCLK2	22	VCC	81
CAS2#	137	GND	121	PREQI	144	VCC	100
CAS3#	136	GND	122	PREQO	145	VCC	120
CAS4#	135	GND	159	PRWGD#	92	WR#	15
CAS5#	134	GND	160	RAS0#	131	XDIR#	69
CAS6#	133	HLDA	10	RAS1#	130	XA0	105

3.1 Signal Descriptions

3.1.1 Clock and Reset Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
CLKI	43	I	CLK2 input from oscillator.
PCLK2	22	I/O	CLK2 output to 386SX and 387SX. (Bidirectional output is always enabled.)
OSC12	104	O	1.19MHz output.
OSC	18	I	14.31818MHz oscillator input.

3.1.2 CPU Control and Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
A[23:17]	67:61	I	CPU Address Bus: Address lines 23 through 17 and 7 through 0.
A[16:8]	60:52	I/O	CPU Address Bus: Address lines 16 through 8. These signals are inputs except during DMA cycles. A[16:9] become outputs and convey DMA address 16-9 for 16-bit DMA cycles. A[15:8] become outputs and convey DMA address 15-8 for 8-bit DMA cycles. A[10:9] are outputs during refresh.
A[7:0]	51:44	I/O	CPU Address Bus: Address lines 7 through 0. These inputs become outputs during refresh.
D[15:0]	9:2, 158:151	I/O	Data bus to/from the CPU.
MP[1:0]	150, 149	I/O	Local DRAM parity bits 1 and 0.
RDYI#	32	I	Ready input from coprocessor Ready.
RDY#	16	O	Ready output to the CPU to terminate the current cycle.
NA#	33	O	CPU next address control signal.
CPURST	24	O	CPU reset signal.
NMI	23	O	Non-maskable interrupt.
WR#	15	I	Write or Read is a bus cycle definition pin that distinguishes write cycles from reads cycles.
DC#	14	I	Data or Control is a bus cycle definition pin that distinguishes data cycles from control cycles.
MIO#	13	I	Memory or I/O is a bus cycle definition pin that distinguishes memory cycles from input/output cycles.
ADS#	12	I	Address status from the 386SX.
HOLD	11	O	Hold request to the 386SX
HLDA	10	I	Hold acknowledge from the 286SX.
BHE#	17	I/O	Byte high enable from the CPU. It is an input during CPU cycles and an output during non-CPU cycles.

Signal Descriptions (Cont.)

3.1.3 DRAM Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
RAS[3:0]#	128:131	O	Local DRAM row address strobe signals.
CAS[7:0]#	132:139	I	Local DRAM column address strobe signals.
MA[10:0]	127:123, 119:114	O	Multiplexed row and column address bits 10 through 0.
RFSH#	103	I/O	Refresh cycle indication signal.
DWE#	140	O	DRAM write/read control signal.

3.1.4 AT Bus Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
ALE	107	T	At bus address latch enable. This signal is tristated during master cycles.
XA0	105	I/O	System board latched address bit 0. This signal is an output for CPU, refresh, or 16-bit DMA cycles and an input for 8-bit DMA or master cycles.
ATCLK	102	O	AT system clock, ATCLK = CLK2/6 (default), ATCLK can be set to CLK2/4 by programming the internal registers.
SBHE#	98	I/O	System byte high enable to/from the AT bus. SBHE# is an input during master cycles.
MEMRD#	97	I/O	Memory read command signal.
MEMWR#	96	I/O	Memory write command signal.
IORD#	95	I/O	I/O read command signal.
IOWR#	94	I/O	I/O write command signal.
CHRDY	143	I	I/O channel ready signal from the AT channel.
IO16#	109	I	I/O data size 16 indication from AT channel.
M16#	70	I/O	Memory data size 16 indication from the AT channel.
CHCK#	142	I	Channel Check signal from the AT channel.
SA[19:17]	37:39	O	System address lines 19 through 17. Tristated during master cycles.
SMRD#	34	O	AT memory read command to memory below 1MB.
SMWR#	25	O	AT memory write command to memory below 1MB
SD[15:0]	71:78, 82:89	I/O	System data bus lines 15 through 0. These signals are connected to AT data bus directly.

Signal Descriptions (Cont.)

3.1.5 DMA Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
DMA8#	112	I	8-bit DMA transfer indication.
DMA16#	111	I	16-bit DMA transfer indication.
HRQ	113	I	Hold request from the 82C206 IPC.
HLDA1	110	O	Hold acknowledge 1 indicates a CPU HLDA was caused by HRQ, not by a refresh request.
ADS8	36	I	8-bit DMA transfer address strobe.
ADS16	35	I	16-bit DMA transfer address strobe.

3.1.6 Miscellaneous Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
KBDCS#	106	O	I/O Port 60 and 64 Address decode. It is de-activated during DMA cycles.
TURBO	148	I	Turbo switch control. CPUCLK2 = ATCLK2 if TURBO pin is low when turbo switch function is enabled.
GATE2	147	O	Timer 2 enable signal.
SPKD	146	O	Speaker output.
INTA#	93	O	Interrupt acknowledge cycle indication.
PWRGD#	92	I	Power bad indication.
SYSRST	90	O	System reset signal.
ROMCS#	141	O	BIOS ROM output enable signal
GA20	26	I/O	Gate Address 20. It is an input from master card during master cycles. Connected to AT bus LA20 indirectly through a buffer.
XDIR#	69	O	XD bus to/from SD bus direction control.
ASRTC	108	O	Address strobe for real-time clock.
BUFCON#	91	O	Buffer control signal. BUFCON# goes low during a master and non-refresh cycle.
OUT2	68	I	Timer 2 output.

3.1.7 Numeric Coprocessor Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
NPBUSY#	30	I	Numeric coprocessor busy signal.
NPERR#	29	I	Numeric coprocessor error signal.
NPRST	31	O	Numeric coprocessor reset.

Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
NPINT	28	O	Interrupt request 13 for 387SX exception.
BUSY#	27	O	Numeric coprocessor busy and error status to CPU busy input.
PREQO	145	O	Connected to the 386SX PREQ input.
PREQI	144	I	Connected to the 387SX PREQ output.

3.1.8 Power and Ground Pins

Signal Name	Pin No.	Signal Type	Signal Description
VCC	1, 20, 40, 81, 100, 120	I	Power connection: +5.0V
GND	19, 21, 41, 42, 79, 80, 99, 101, 121, 122, 159, 160	I	Ground connection

4.0 Functional Description

The following sub-sections will explain the various cycles, features, and operations of the 82C283.

4.1 Local Memory Controller

The 82C283 memory controller has the following features:

- Flexible DRAM banks configuration - The 82C283 supports 256K, 1M, and 4M size DRAM. Total memory can be up to 16MB. Twelve memory configurations are supported as shown in Table 4-1.
- Block interleave mode operations - Depending on the memory configuration, the local memory controller unit performs block interleaving at a block size of 512 bytes using 256K, 1M or 4M DRAMs.
- BIOS shadow RAM - The local memory controller can shadow RAM for system BIOS, video BIOS, and adapter BIOS.
  - 0F0000h-0FFFFFh is system BIOS area and can be programmed to be:
    - Read during AT ROM cycles; written during local memory cycles (default).
    - Read during local memory cycles with no writes allowed (write-protected).
  - 0C000h-0EFFFFh contains twelve 16KB blocks, each programmable:
    - Read from AT bus; write to AT bus (default).
    - Read from AT bus; write to local memory.
    - Read from local memory; write to local memory.
    - Read from local memory and write protected.
- Memory remapping - If shadow RAM is not used at memory area 0D0000h-0EFFFFh, remapping is possible. Then, local memory areas 0A0000h-0BFFFFh and 0D0000h-0EFFFFh (each 128K bytes) are mapped to the top of total memory. Memory areas 0F0000h-0FFFFFh (system BIOS) and 0C0000h-0CFFFFh (video BIOS) are reserved for shadow RAM.
- Flexible multiplexed DRAM address - Table 4-2 shows how DRAM address lines are multiplexed when different size DRAM are used.

Table 4-1 DRAM Banks Configurations

Bank 0	Bank 1	Bank 2	Bank 3	Total
256K	256K			1M
256K	256K	256K	256K	2M
1M				2M
256K	256K	1M		3M
1M	1M			4M
256K	256K	1M	1M	5M
1M	1M	1M		6M
1M	1M	1M	1M	8M
256K	256K	4M		9M
1M	4M			10M
1M	1M	4M		12M
4M	4M			16M
4M*				8M

*Rev. B only

Table 4-2 Address to MA Mapping

Memory Address	256K		1M		4M	
	Col	Row	Col	Row	Col	Row
0	1	11	1	20	1	20
1	2	12	2	11	2	22
2	3	13	3	12	3	12
3	4	14	4	13	4	13
4	5	15	5	14	5	14
5	6	16	6	15	6	15
6	7	17	7	16	7	16
7	8	18	8	17	8	17
8	10	19	10	18	10	18
9			9	19	9	19
10					11	21

4.2 AT Bus Controller

The AT bus controller handles all of the AT bus operations and DMA/refresh arbitration. The controller has the following features:

- Programmable AT bus clock - The AT bus clock, ATCLK, is selectable from either CLK2/6 (default) or CLK2/4.
- Turbo switch - The 82C283 has a turbo switch feature allowing users to change the system clock speed. Setting Register 14h, bit 1 high (to 1), enables the turbo function, whereupon the 82C283 TURBO pin selects the system clock speed as follows:
  - A low on the TURBO pin causes the CPU to run at the current at bus speed (either CLK2/6 or CLK2/4).
  - A high on the TURBO pin causes the CPU to run at 16, 20 or 25MHz.
  - If the keyboard controlled turbo switching is desired, the TURBO pin should be kept low and the turbo configuration bit should be toggled.

4.3 SX/AT System Operation

The detailed operation of an 82C283-based SX/AT system design is described in the following sub-sections.

4.3.1 Reset

The power supply's power good (PWRGD#) signal initializes the system when PWRGD# goes low. The 82C283 forces CPURST, NPRST high and SYSRST# low, then negates these signals 128 CLK2 cycles after PWRGD# goes high.

4.3.2 Local DRAM Interfaces

Local memory (DRAM) is located on the CPU local data bus. The CPU reads data directly from local memory. Local memory latches CPU write data on the leading edge of CAS#. The memory controller asserts M16# when external master cards read local memory, and asserts DWE# when they write local memory.

For parity control, the memory controller reads the requested byte(s) and checks parity; during local memory writes, the data bus control unit generates parity, to be stored in local memory.

4.3.3 System BIOS ROM

If the system BIOS ROM is not shadowed, ROM cycles are treated as AT cycles. 8-bit BIOS ROM resides on the XD bus and 16-bit BIOS ROM on the SD bus. With 16-bit ROM, ROMCS# is connected to M16# through an open collector (a driver such as a 7407), allowing the 82C283 to determine the width of the ROM data path by monitoring M16#.

4.3.4 I/O Ports Located on the XD Bus

XDIR# controls the direction of I/O ports on the XD bus. Not that I/O ports 0F0h-0FFh are reserved for the coprocessor.

4.3.5 Refresh Cycles

The AT bus controller arbitrates between the 82C206 hold request (HRQ) and the 82C283 refresh request, to determine who receives bus control when the CPU relinquishes it. The bus controller grants refresh requests once every 15.9µs (regular refresh) or once every 63.6µs (slow refresh). During refresh, the AT bus controller asserts RFSH# and MEMRD# and generates the refresh address.

4.3.6 DMA Cycles

HRQ initiates a DMA/master transfer. When the 82C283 selects DMA (via the HRQ input) over the refresh request, after the CPU acknowledges by asserting HLDA, then the 82C283 sends HLDA1 to the 82C206 to acknowledge the request. The 82C206 asserts DMA16# and activates ADS16# to start 16-bit DMA transfers, or asserts DMA8# and activates ADS8# to start 8-bit DMA transfers.

5.0 Configuration Registers

There are seven Configuration Registers inside the 82C283. An indexing scheme is used to access all of these registers. Port 22h is used as the Index Register and Port 24h is the Data Register. Each access to a Configuration Register consists of a write to Port 22h, specifying the desired register in the data byte, followed by a read or write to Port 24h with the actual register data. The index resets after every access; therefore every data access (via Port 24h) must be preceded by a write to Port 22h, even if the same register is being accessed on consecutive occasions. All reserved bits are set to zero by default.

Table 5-1 DRAM Configuration Register - Index 10h

Bit(s)	Type	Default	Function
7	RO	0	82C283 revision number: 0 = Revision A 1 = Revision B
6	R/W	0	Revision A: Reserved - Must always = 0. Revision B: 0 = Non-pipelined 1 = Pipelined
5	R/W	1	Local DRAM read cycle wait state: 0 = Zero wait state 1 = One wait state
4	R/W	1	Local DRAM write cycle wait state: 0 = Zero wait state 1 = One wait state
3:0	R/W	1111	Local DRAM memory configuration:

Bits	Bank 0	Bank 1	Bank 2	Bank 3	Total
1111	256K	256K			1M
0001	256K	256K	256K	256K	2M
0010	256K	256K	1M		3M
0011	256K	256K	1M	1M	5M
0100	256K	256K	4M		9M
0101					2M
0110	1M	1M			4M
0111	1M	1M	1M		6M
1000	1M	1M	1M	1M	8M
1001	1M	4M			10M
1010	1M	1M	4M		12M
1011	4M	4M			16M
1100*	4M				8M

*Rev. B Only

Table 5-2 Shadow RAM Control Register - Index 11h

Bit(s)	Type	Default	Function
7	R/W	1	Shadow RAM enable for system BIOS ROM at F0000h-FFFFFh: 0 = Read only from shadow RAM 1 = Reads go to ROM and writes go to shadow RAM
6	R/W	1	Adaptor ROM located at E0000h-EFFFFh: 0 = All accesses are to system board ROM, shadow RAM is disabled 1 = Shadow RAM is selectively enabled in 16KB blocks by CFG register 12h; other accesses are AT bus cycles.
5	R/W	1	ROM located at D0000h-DFFFFh: 0 = All accesses are on AT bus and shadow RAM is disabled 1 = Shadow RAM is selectively enabled in 16KB blocks by CFG register 12h; other accesses are AT bus cycles.
4	R/W	1	ROM located at C0000h-CFFFFh: 0 = All accesses are on AT bus and shadow RAM is disabled 1 = Shadow RAM is selectively enabled in 16KB blocks by CFG register 13h; other accesses are AT bus cycles.
3	R/W	0	Shadow RAM copy enable control for C0000h-EFFFFh: 0 = Write to AT bus 1 = Write to local DRAM
2:0	R/W	000	Shadow RAM AT X0000h-XFFFFh read/write status: 0 = Read/write 1 = Read only (While shadow RAM is being loaded, this bit must be set to 0; after shadow RAM is loaded, setting this bit to 1 write-protects shadow RAM.) Bit 2 = E0000h -EFFFFh Bit 1 = D0000h-DFFFFh Bit 0 = C0000h-CFFFFh

Table 5-3 Shadow RAM Control Register - Index 12h

Bit(s)	Type	Default	Function
7:0	R/W	0000 0000	This register selectively enables shadow RAM in 16KB blocks from D0000h-EFFFFh. This and the Shadow RAM Register (Index 11h) implement full system selective shadowing. Shadow RAM for XX000h-XXFFFh segments: 0 = Disable 1 = Enable Bit 7 = EC000h-EFFFFh Bit 3 = DC000h-DFFFFh Bit 6 = E8000h-EBFFFh Bit 2 = D8000h-D8FFFh Bit 5 = E4000h-E7000h Bit 1 = D4000h-D7FFFh Bit 4 = E0000h-E3FFFh Bit 0 = D0000h-D3FFFh

Table 5-4 Shadow RAM Control Register - Index 13h

Bit(s)	Type	Default	Function
7:4	R/W	0000	Shadow RAM for CX000h-CXFFFh segments: 0 = Disable 1 = Enable Bit 7 = CC000h-CFFFFh Bit 5 = C4000h-C7000h Bit 6 = C8000h-CBFFFh Bit 4 = C0000h-C3FFFh
3:0	R/W	0000	Remap address for unused shadow RAM. Remaps A0000h-BFFFFh and D0000h-EFFFFh if not used for shadowing. Bits 3 through 0 correspond to Address 23 through 20.

A23	A22	A21	A20	Remap Address
0	0	0	0	No mapping
0	0	0	1	1MB
0	0	1	0	2MB
0	0	1	1	3MB
0	1	0	0	4MB
0	1	0	1	5MB
0	1	1	0	6MB
0	1	1	1	7MB
1	0	0	0	8MB
1	0	0	1	9MB
1	0	1	0	10MB
1	0	1	1	11MB
1	1	0	0	12MB
1	1	0	1	13MB
1	1	1	0	14MB
1	1	1	1	15MB

Table 5-5 Miscellaneous Control Register - Index 14h

Bit(s)	Type	Default	Function
7	R/W	0	Zenith mode: Setting this bit to 1 will turn on the Zenith mode which allows F0000h-F0FFFh to be written while write-protect is on.
6	R/W	0	Keyboard reset control: If active, a halt instruction must be executed before the 82C283 generates a CPU reset from the keyboard reset.
5	R/W	0	Master byte swap enable.
4	R/W	0	Rev. A: Reserved - Must be programmed to 0. Rev. B: 0 = ATCLK set with Register 14h, bit 0 (Default) 1 = ATCLK = CLK/8 for 33MHz operation
3:	R/W	0	Rev. A: Reserved - Must be programmed to 0. Rev. B: 0 = Disable on-board parity errors (main DRAM) (Default) 1 = Enable on-board parity errors (main DRAM)
2	R/W	0	Slow refresh mode: The 82C283 refresh request is generated internally every 15.9µs. Setting this bit to a 0 will cause a refresh request to occur every 63.6µs.
1	R/W	0	Turbo switch function: Turning on this bit enables the turbo switch function.
0	R/W	0	AT clock select: 0 = ATCLK2 = CPUCLK2/6 1 = ATCLK2 = CPUCLK2/4

5.1 AT Compatible Registers

5.1.1 I/O Port 61h (Port B)

The 82C283 provides access to Port B, I/O Port address 61h defined for the PC/AT as shown in Table 5-6.

At power-on, the NMI is disabled. However, it can be enabled or disabled by writing to I/O Port 70h with data bit 7 equal to zero or one, respectively. An NMI occurs when NMI is enabled. If bits 3 or 2 are enabled, an IOCHCK or PCK occurs.

Table 5-6 Port 61h (Port B)

Bit(s)	Type	Function
7	R	System Parity Check: This bit indicates that an on-board RAM parity error has occurred. It can only be set if bit 2 (Parity Check Enable) = 0. This bit should be cleared by writing a 1 to bit 2.
6	R	I/O Channel Check: This bit indicates that a peripheral device is reporting an error. It can only be set if bit 3 (I/O Channel Check Enable) = 0. This bit should be cleared by writing a 1 to bit 3.
5	R	Timer OUT2 Detect: This bit indicates the current state of the OUT2 signal from the on-board timer.
4	R	Refresh Detect: This bit is tied to a toggle flip-flop which is clocked by REFRESH. It toggles the opposite state every time a refresh cycle occurs.
3	R/W	I/O Channel Check Enable: When this bit is set low, it allows an NMI to be generated if the IOCHCK# input is pulled low. Otherwise, the IOCHCK# input is ignored and can not generate an NMI. 0 = Enable 1 = Disable
2	R/W	Parity Check Enable: When this bit is set low, it allows parity errors from on-board RAM memory to cause an NMI. When high, on-board RAM parity errors will not cause an NMI.
1	R/W	Speaker Output Enable: This bit is gated with the output of Counter 2 from the on-board timer. When this bit is high, it allows the OUT2 frequency to be passed out on the SPKR pin. When low, the SPKR output is forced low. 0 = Enable 1 = Disable
0	R/W	Timer 2 Gate: This bit goes to the GATE2 input of the on-board timer to enable Counter 2 to produce a speaker frequency. 0 = Enable 1 = Disable

6.0 Maximum Ratings

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	Supply Voltage	-0.5	6.5	V
VI	Input Voltage	-0.5	VCC + 0.5	V
VO	Output Voltage	-0.5	VCC + 0.5	V
TOP	Operating Temperature	0	+70	°C
TSTG	Storage Temperature	-40	+125	°C

6.2 DC Characteristics

VCC = 5.0V ±5%, TA = 0°C to +70°C

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.0	VCC + 0.3	V	
VOL	Output Low Voltage		0.45	V	IOL = 3.0mA all pins except: IOL = 6.0mA for Group A IOL = 12.0mA for Group B
VOH	Output High Voltage	2.4		V	IOL = -1.6mA all pins except: IOL = -3.2mA for Group A IOL = -3.2mA for Group B
IIL	Input Leakage Current	-10	10	µA	VIN = VCC
IOZ	Tristate Leakage Current	-10	10	µA	
CIN	Input Capacitance		10	pF	
COUT	Output Capacitance		10	pF	
ICC (20MHz)	Power Supply Current		50	mA	

Group A Pins: D[15:0], MP[1:0], RDYO#, ATCLK, MA[9:0], RAS[3:0]#, CAS[7:0]#
Group B Pins; PCLK2, SD[15:0], RFSH#, SA[19:17], SMRD#, SMWR#

6.3 AC Characteristics - 16/20/25MHz

Symbol	Parameter	Min	Max	Unit	Condition
t1	RDYI# setup time to CLK2↑	13		ns	
t2	RDYI# hold time to CLK2↑	12		ns	
t3	CPURST active delay from CLK2↑	0	17	ns	
t4	CPURST Inactive delay from CLK2↑	5	12	ns	
t5	RST4 active delay from CLK2↑	0	17	ns	
t6	RST4 active delay from CLK2↑	0	17	ns	
t7*	NPRST active delay from CLK2↑	0	17	ns	30 pF load
t8*	NPRST inactive delay from CLK2↑	5	12	ns	30 pF load

Symbol	Parameter	Min	Max	Unit	Condition
t11	BUSY# active delay from NPBUSY#		20	ns	
t12	BUSY# inactive delay from NPBUSY#		20	ns	
t13	NPERR# setup time to NPBUSY#	5		ns	
t14	NPRST active delay from IOW#		32	ns	
t15	NPRST inactive delay from IOW# inactive		32	ns	

Symbol	Parameter	Min	Max	Unit	Condition
t41	SD[15:0] setup time to IORD# (MEMRD#)	22		ns	
t42	SD[15:0] hold time from IORD# (MEMRD#)	3		ns	
t43	SD[15:8] active delay from SD[7:0] valid	2	24	ns	
t44	SD[15:8] inactive delay from SD[7:0] invalid	2	24	ns	
t45	NMI active delay from CHCK# active		25	ns	
t46	SD[15:0] active delay from D[15:0] valid	2	25	ns	
t47	SD[15:0] inactive delay from D[15:0] invalid	2	25	ns	
t48	MP[1:0] active delay from D[15:0] valid	2	27	ns	
t49	MP[1:0] inactive delay from D[15:0] invalid	2	27	ns	
t50	D[15:0] active delay from SD[15:0] valid	2	25	ns	
t51	D[15:0] inactive delay from SD[15:0] invalid				
t52	D[15:0] active delay from SD[15:0] valid	2	27	ns	
t53	D[15:0] inactive delay from SD[15:0] invalid	2	27	ns	

Symbol	Parameter	Min	Max	Unit	Condition
t54	ALE active delay from ATCLK↑	0	15	ns	
t55	ALE inactive delay from ATCLK↑	0	15	ns	

AC Characteristics - 16/20/25MHz (Cont.)

Symbol	Parameter	Min	Max	Unit	Condition
t56	Command active delay from ATCLK↑	0	15	ns	
t57	Command inactive delay from ATCLK↑	0	15	ns	
t60	CHRDY setup time to ATCLK	15		ns	
t61	CHRDY hold time from ATCLK	5		ns	
t62	HOLD active delay from ATCLK	0	20	ns	
t63	HOLD inactive delay from ATCLK	0	20	ns	
t64	RFSH# active delay from ATCLK↑	0	20	ns	
t65	RFSH# inactive delay from ATCLK↑	0	20	ns	
t66	MEMRD# active delay from ATCLK↑	0	20	ns	
t67	MEMRD# inactive delay from ATCLK↑	0	22	ns	
t68	HRQ setup time to ATCLK↑	15		ns	
t69	HRQ hold time to ATCLK↑	20		ns	
t70	HLDA1 active delay from HLDA active	0	20	ns	
t71	HLDA1 inactive delay from HLDA inactive	0	20	ns	

Symbol	Parameter	Min	Max	Unit	Condition
t80	RAS# active delay from XMEMW# (XMEMR#) active	0	22	ns	
t81	RAS# inactive delay from XMEMW# (XMEMR#) inactive	0	22	ns	
t82	MA[10:0] active delay from RAS# active	0	22	ns	
t83	CAS# active delay from XMEMW# (XMEMR#) active	20	40	ns	
t84	CAS# inactive delay from XMEMW# (XMEMR#) inactive	20	40	ns	
t85	DWE# active delay from XMEMW# (XMEMR#) active	20	40	ns	
t86	DWE# inactive delay from XMEMW# (XMEMR#) inactive	20	40	ns	

Symbol	Parameter	Min	Max	Unit	Condition
t90	CAS# active delay from CLK2↑	5	20	ns	
t91	CAS# inactive delay from CLK2↑	5	20	ns	
t92	RDY# active delay from CLK2↑	4	20	ns	
t93	RDY# inactive delay from CLK2↑	4	20	ns	
t98	RAS# active delay from CLK2↑	5	21	ns	
t99	RAS# inactive delay from CLK2↑	5	21	ns	
t100	MA[10:0] active delay from CLK2↑	5	21	ns	
t101	DWE# active delay from CLK2↑	5	20	ns	
t102	DWE# inactive delay from CLK2↓	5	20	ns	

AC Characteristics - 16/20/25MHz (Cont.)

Symbol	Parameter	Min	Max	Unit	Condition
	CLK2 period	20		ns	
	CLK2 high time	8		ns	
	CLK2 low time	8		ns	
	CLK2 fall time		4	ns	
	CLK2 rise time		4	ns	

All AC specifications are relative to the CLK2 rising/falling edge crossing the 2.0V level. All other signals are relative to their rising/falling edge crossing 1.5V level.

Notes: 1. ↑ means rising edge.
2. ↓ means falling edge.
3. Loading capacitance is 50pf unless otherwise noted.

6.4 AC Timing Waveforms

Figure 6-1 Reset Timing

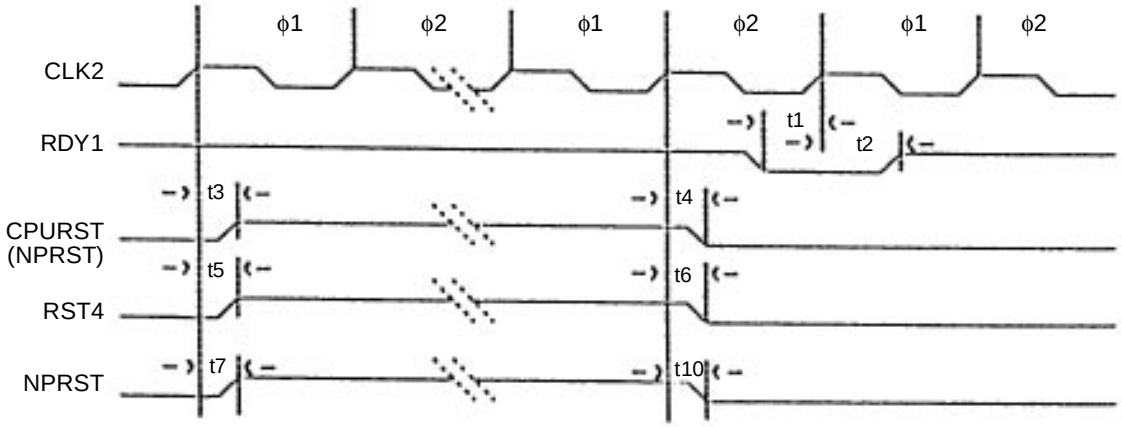


Figure 6-2 Numeric Processor Reset Timing

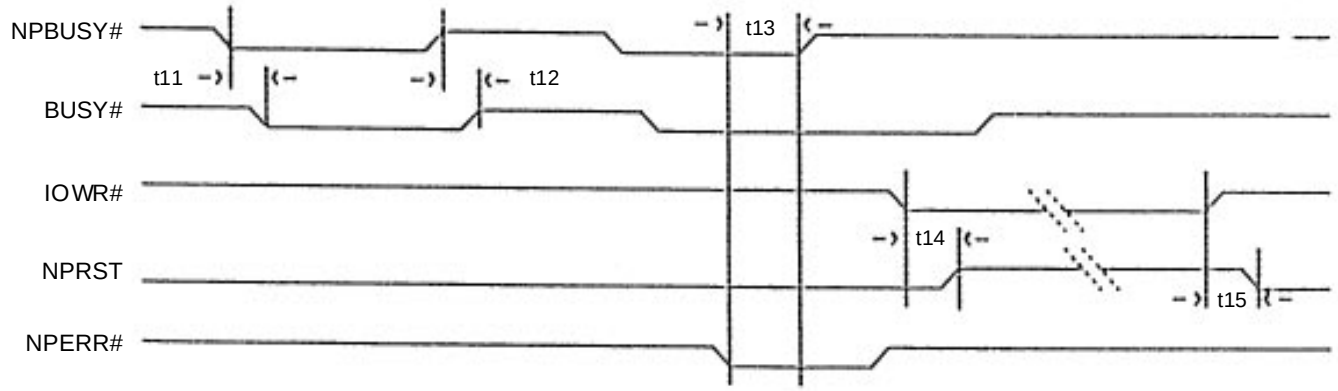


Figure 6-3 Data Setup and Hold Time for IORD# or MEMRD#

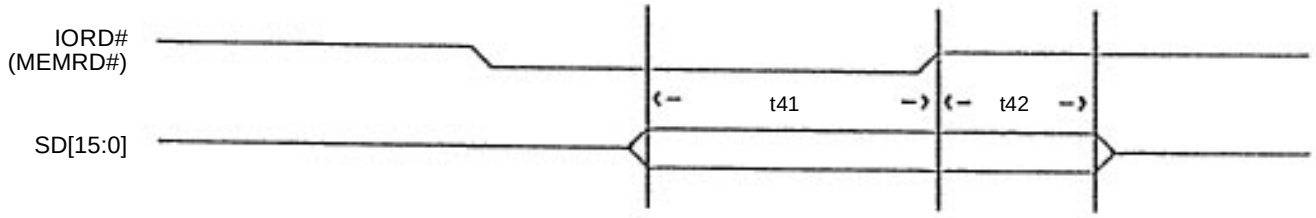


Figure 6-4 Data Valid and Invalid Delay between SD[15:8] and SD[7:0]

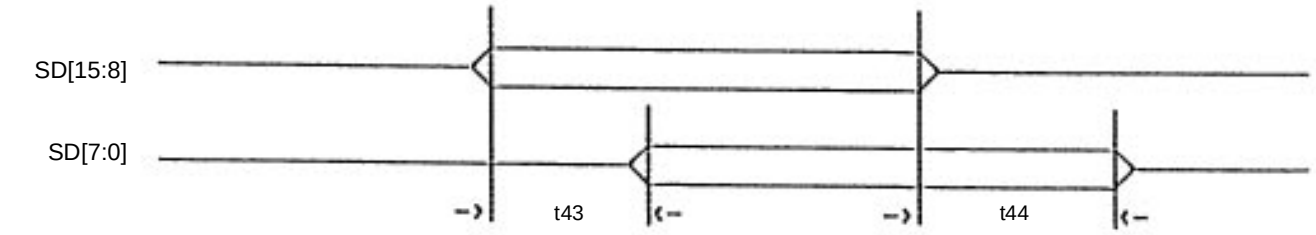


Figure 6-5 NMI Valid Delay related to CHCK#]

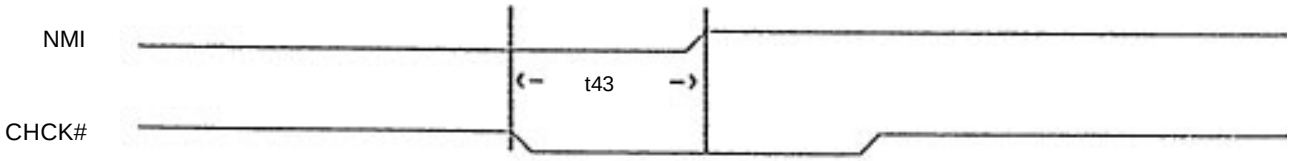
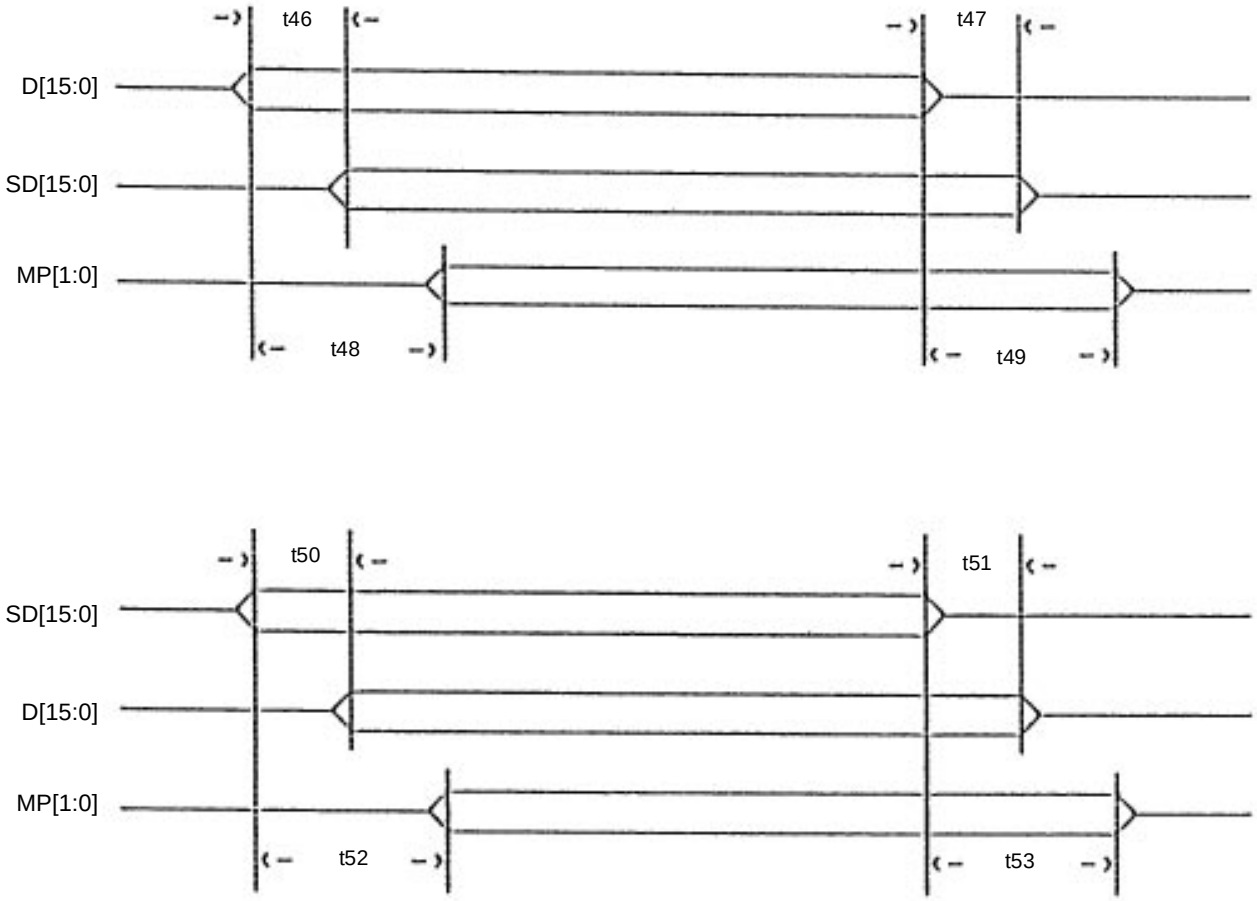
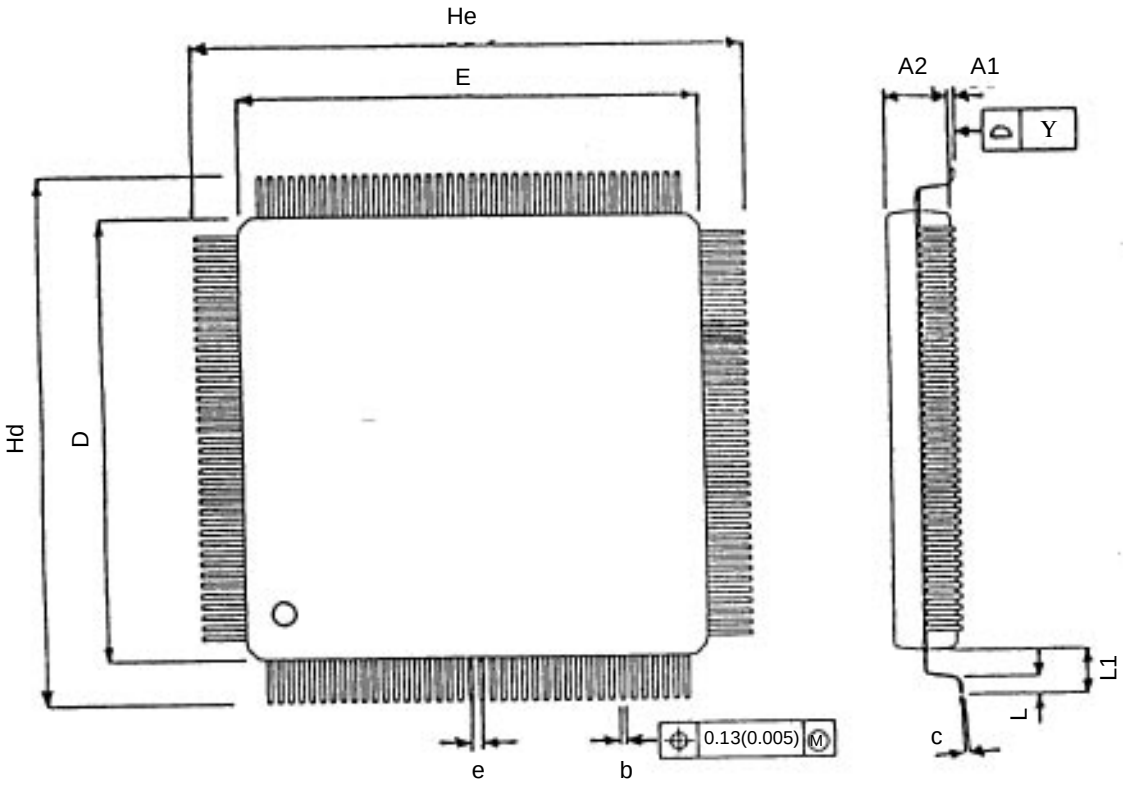


Figure 6-6 SD[15:0] to D[15:0] and MP[1:0] Valid and Invalid Delay



7.0 Mechanical Package Outline

Figure 7-1 160-Pin Plastic Quad Flat Pack (PQFP)



Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A1	0.05	0.25	0.50	0.002	0.010	0.020
A2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.65			0.026	
Hd	31.65	31.90	32.15	1.246	1.256	1.266
He	31.65	31.90	32.15	1.246	1.256	1.266
L	0.65	0.80	0.95	0.025	0.031	0.037
L1		1.95			0.077	
Y			0.08			0.003
θ	0		10	0		10