OPTi-DXBB PC/AT Chipset (82C497)

PRELIMINARY

82C497 DATA BOOK

Version 1.2
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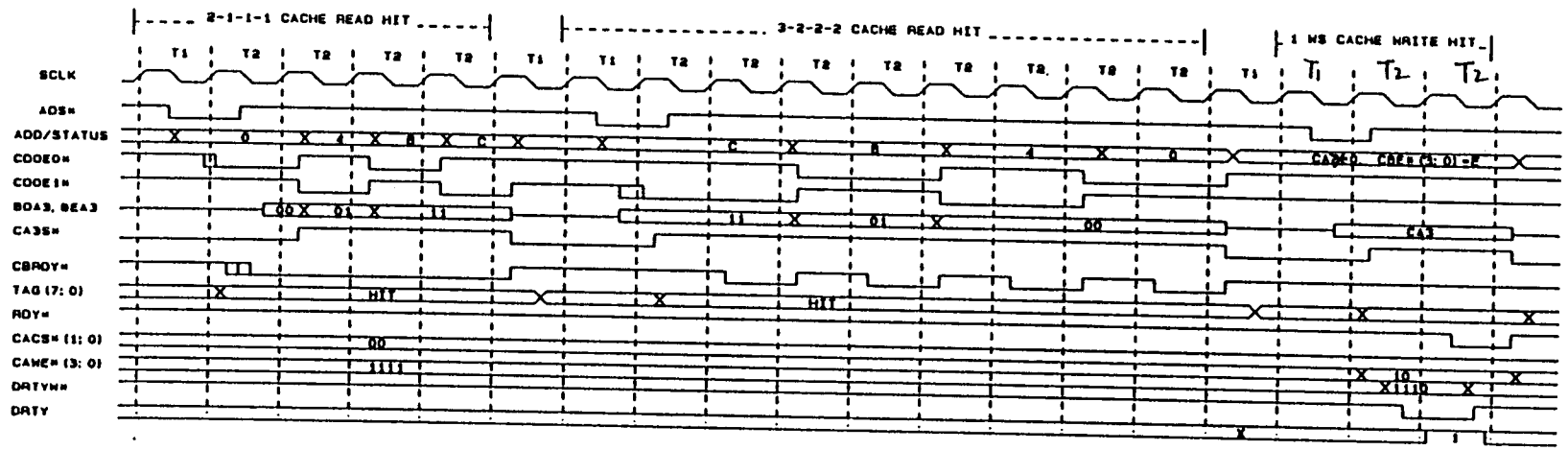

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1.0 FEATURES

* 386 and 486 CPU interface
* Isolates the CPU bus from Local bus, more reliable system operation at high speed
* Asynchronous handshaking between CPU bus and Local bus; fixed base-board speed with upgradeable CPU card speed
* Direct map write back cache with one level write buffer and 16-byte line size
* Programmable 2-1-1-1,3-1-1-1,2-2-2-2 or 3-2-2-2 burst read cycle
* Programmable cache write hit 0 or 1 wait state
* Optional Dirty bit
* Supports 32K - 256K cache size for 386 cache system
* Support 64K - 512K cache size for 486 cache system
* Provides TAG and Dirty RAM test capability
* Built-in TAG auto-invalidation circuitry
* Two programmable non-cacheable regions
* Option for write-protected, cacheable Video BIOS
* Cacheable AT bus memory space
* 8042 emulation for fast CPU-reset and gateA20 generation
* 1X clock source support for systems from 16 MHZ to 50 MHZ
* 160-pin plastic quad flat package

OPTi DXBB System Diagram

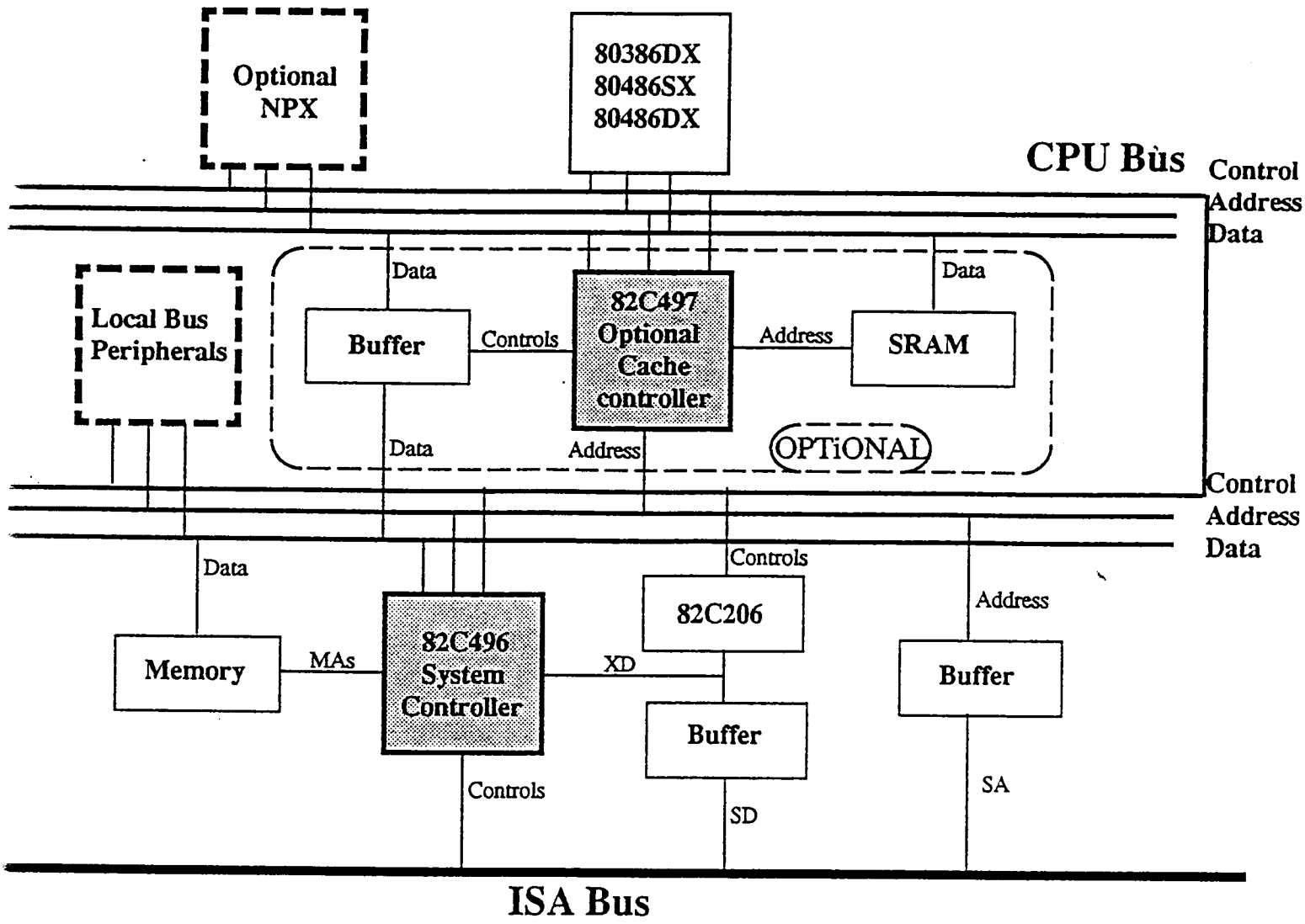


Figure1

2.0 INTRODUCTION

The OPTi 82C497 is a Direct Mapped Write Back cache controller with one level write buffer that is an optional part of the DXBB (Building Block) Chip set. The DXBB also contains the 82C496 and the 82C206, which form the heart of the system. The 82C497 is added to the DXBB chip set for cache based systems.

The OPTi 82C496 offers an upgradable CPU module base-board solution for the 80386 or the 80486 PC/AT system. By swapping the CPU module, the vendor can configure the 82C496 driven base-board into various 32-bit AT systems – 386 or 486 CPU, with cache or without cache and rated at 16MHz-50MHz.

For the Non-Cache systems, the CPU interfaces directly with the 82C496 and the local devices, like the local VGA controller or the local hard disk adaptor.

For cache based systems the 82C497 (the cache controller) sits between the CPU and the 82C496 and the local devices. All the high frequency signals are isolated by the 82C497. This allows the base-board to run at a fixed speed (25 or 33MHz) – while the CPU and the Cache can run synchronously at any determined rated speed. This provides a reliable upgrade method for the CPU modules.

82496 SYSTEM

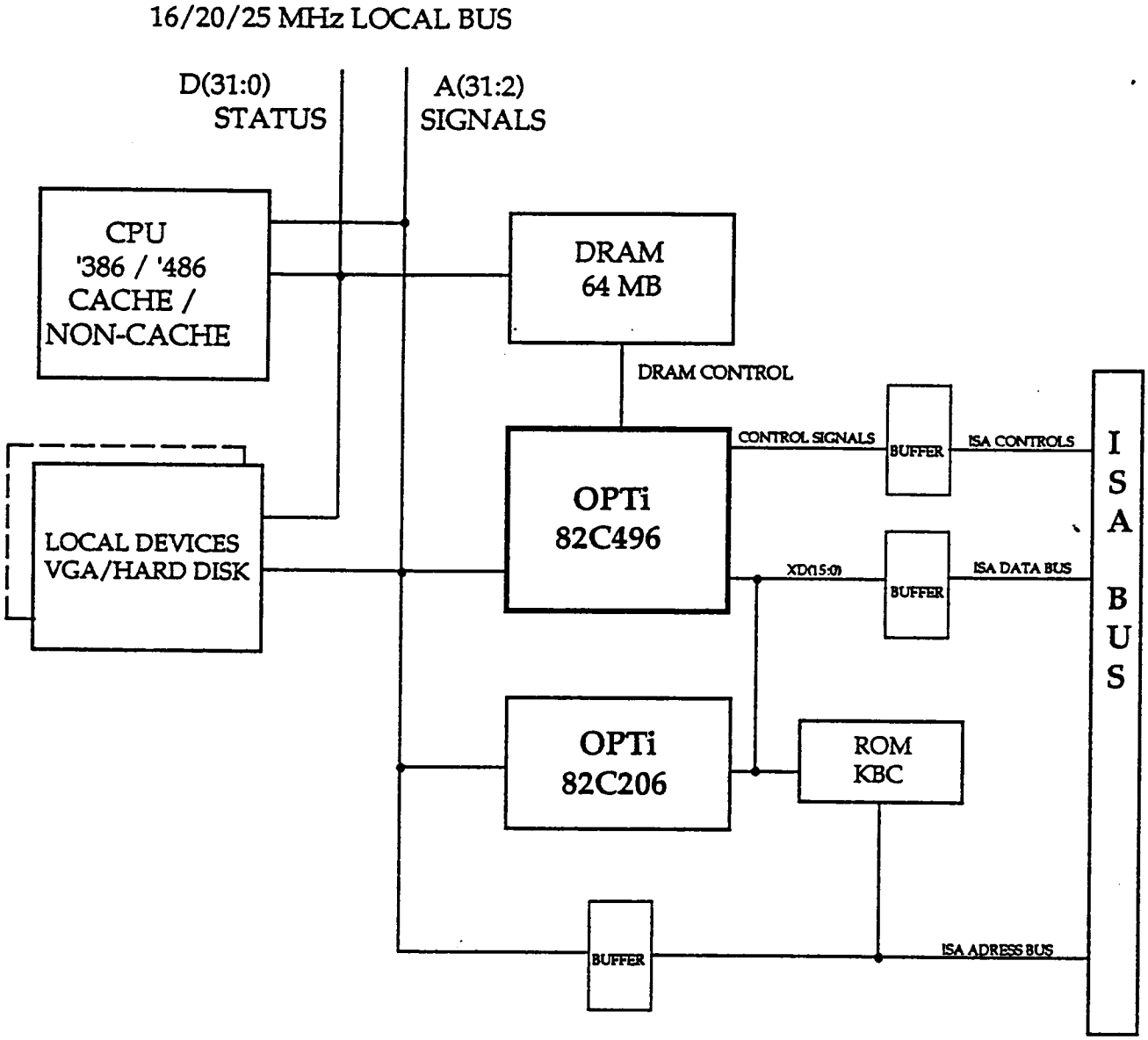


FIGURE 2A

82497 SYSTEM

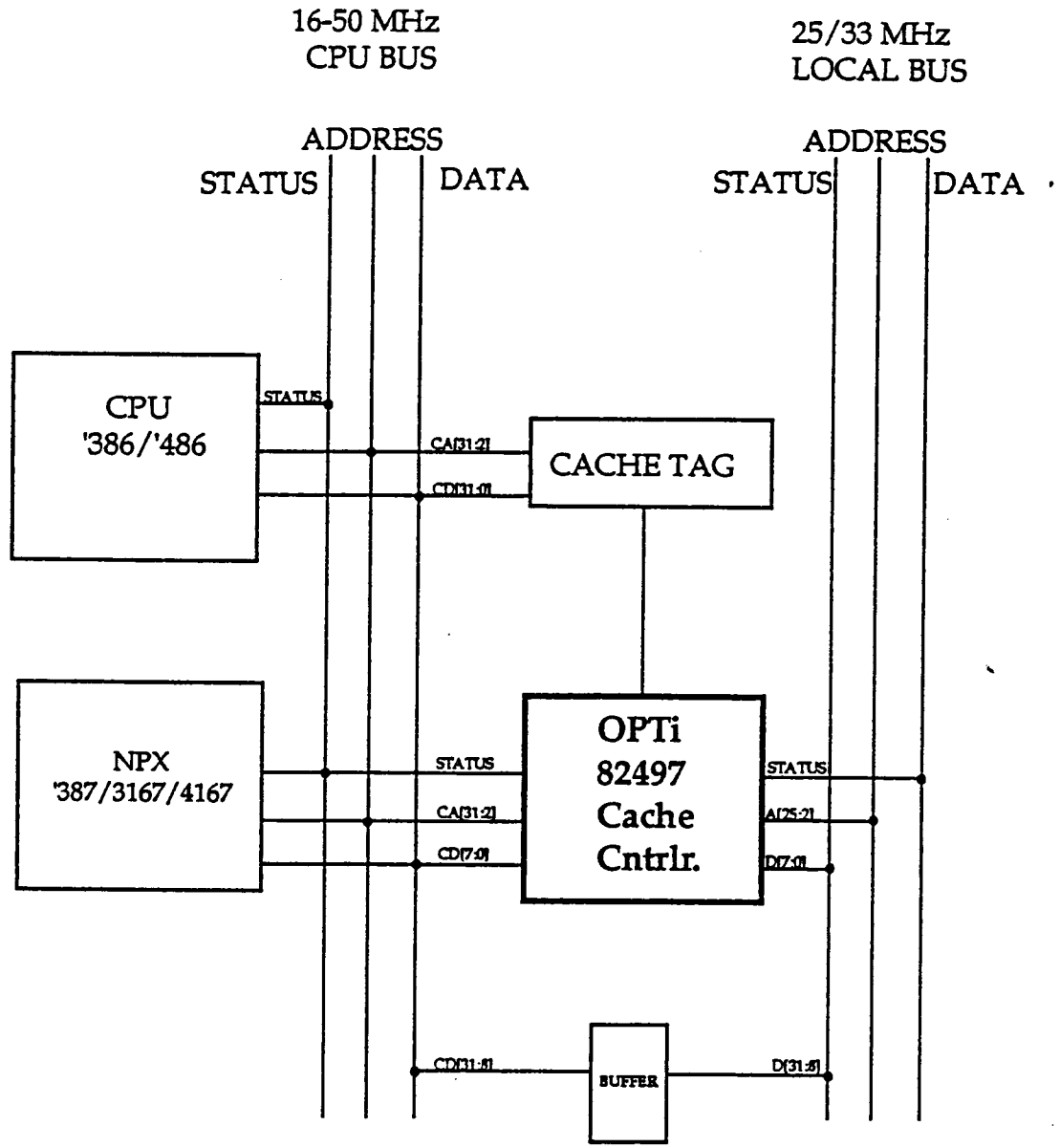


FIGURE 2B

3.0 DESCRIPTION

The 82C497 is a direct write back cache control unit with one-level of write buffers and a 16 byte line size. The cache controller can support cache sizes from 32K to 512K with a cacheable address range of upto 64M. There is a programmable option of 2-1-1-1, 3-1-1-1, 2-2-2-2 or 3-2-2-2 burst read cycles and a cache write hit of 0 or 1 wait state. The 82C497 also provides asynchronous handshaking between the CPU bus and the local bus to enable a fixed base-board speed with variable CPU unit speeds. The controller also supports the Dirty bit option and has TAG and Dirty RAM test capability.

The 82C497 consists of six functional blocks: 1) CPU interface 2) Local Bus Interface 3) Cache control logic 4) Reset generation and Keyboard emulation logic 5) Data & Address Latches 6) Programmable Registers.

3.1 CPU Interface

The CPU interface monitors and relays the particular cycles to the related control units and returns the READY signal back to the CPU when the cycle is completed.

1. Numeric Co-Processor (NPX) cycles

The NPX being installed or not determines the way the '497 treats the NPX cycles. If the NPX is not installed, the '497 treats any NPX cycle as an AT cycle. If the NPX is installed, the '497 will not take any action, when the CPU accessess any of the NPX address spaces, except re-synchronizing the NPX READY before sending it back to the CPU.

2. Cache cycles

The cache hit cycle is handled by the cache control logic. The cache read miss cycle is also turned over to the cache control logic, after the external cache is filled from the DRAM on the Local bus. The CPU status signals including ADS# do not go to the Local bus if there is a cache hit cycle.

82C497 BLOCK DIAGRAM

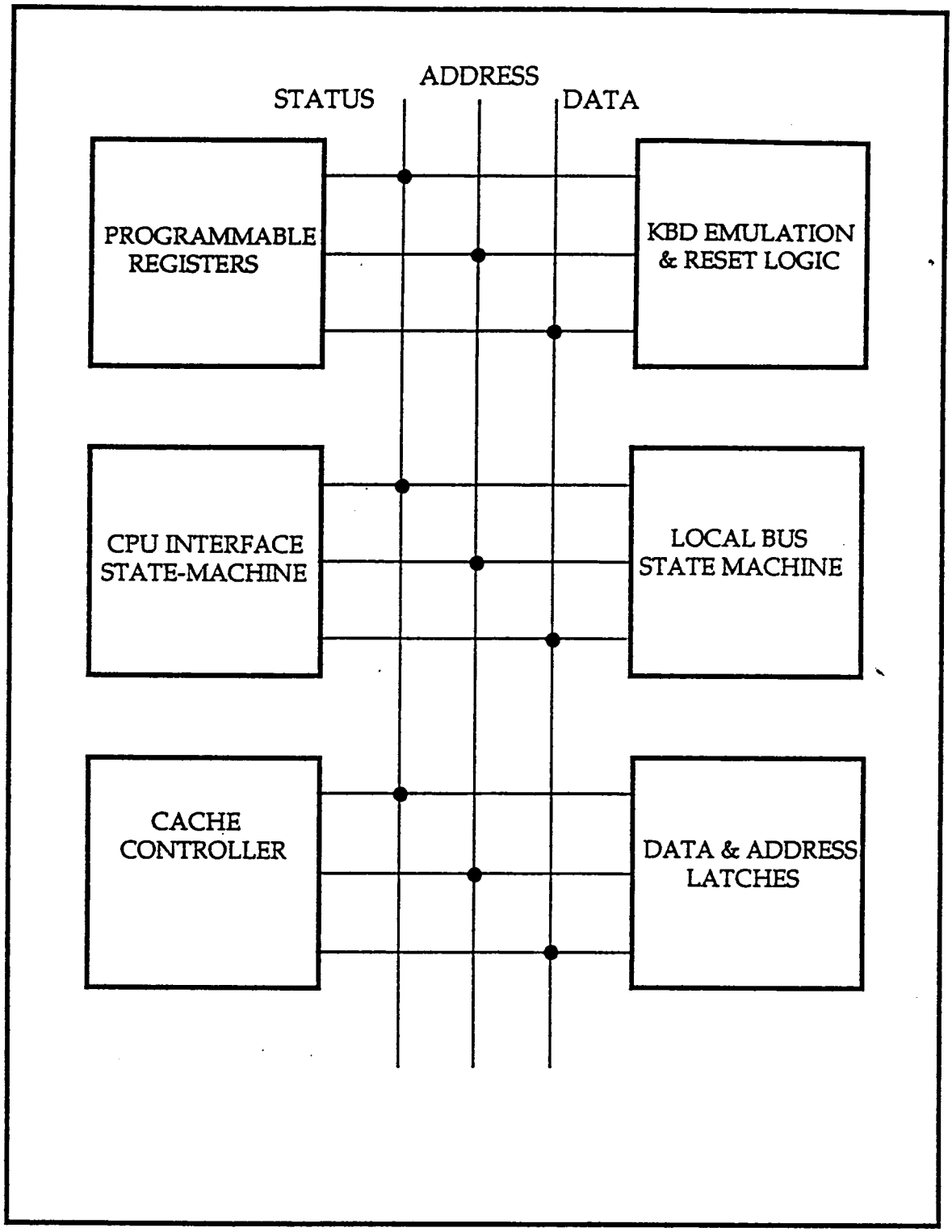


FIGURE 3A

3. Special cycles

The special cycles – such as SHUT DOWN and HALT cycles are handled by the Special cycle handling logic. This logic converts the CPU status signals MIO, DC and WR signals automatically based on the processor mode being 386 or 486. The special cycles NEVER go the Local bus.

4. All other CPU cycles

All other CPU cycles, like:

- non-cacheable cycles
- cache miss cycles
- IO cycles
- INTA cycles

are transferred to the local bus interfaces unit.

5. Write cycles

The 82C497 has one level deep write buffer. The write cycle is terminated upon the determination that the Local bus is not busy.

3.2 Cache Control Unit

The 82C497 contains Tag comparator circuitry. The Tag comparator compares the CPU address and the Tag RAM inputs. The comparator asserts the internal HIT# signal when the address location points to a current cache entry. Simultaneously, the comparator determines whether the current cycle's address is cacheable or not by comparing it with the pre-defined non-cacheable address space. All the non-cacheable address cycles are passed to the Local bus. The cache control logic handles the cache hit cycle and the cache read miss cycle, after the Local bus line fill is finished.

The possible cache cycles are:

1. Cache read hit

The 82C497 enables the cache memory output enable and terminates the cycle when BLST# is activated.

2. Cache write hit

The 82C497 asserts DRTYWE# for dirty RAM and CAWE#(3:0) for cache memory. The accessed cache line is specified as a dirty line.

3. Cache read miss (not dirty)

The cache controller does not need to update DRAM with the cache's current data, since the accessed cache line is not stale. The cache control unit asserts the TAGWE*, updating the TAG RAM with new line address, and asserts CAWE*(3:0) while the local bus cache line fill is going on.

4. Cache read miss (dirty)

The cache controller updates the DRAM with data from cache line address which will be overwritten. The controller writes the 16-byte line from the cache to the DRAM, then reads the new line from the DRAM into the cache memory.

The cache memory can be configured as one or two banks. The cache control unit performs two-way double-word interleave for the two banks cache configuration. This allows for looser cache memory timing requirements.

The following tables show the cache size supported by the 82C497, with the corresponding tag RAM address bits, tag RAM size, cache RAM address bits, cache RAM size, and cacheable main memory size.

486 mode:

Cache size (KB)	Tag field Address Tag RAM size	Cache RAM addr. Cache RAMs	Cacheable Memory(MB)
64	A23-A16 4K X 9	A15-A4 8 8K X 8	16
128	A24-A17 8K X 9	A16-A4 4 32K X 8	32
256	A25-A18 2 8K X 9	A17-A4 8 32K X 8	64
512	A25-A19 32K X 9	A18-A4 4 512K X 8	64

386 mode:

Cache size (KB)	Tag field Address Tag RAM size	Cache RAM addr. Cache RAMs	Cacheable Memory(MB)
32	A22-A15 2K X 9	A15-A4 4 8K X 8	8
64	A23-A16 8K X 9	A15-A4 8 8K X 8	16
128	A24-A17 2 8K X 9	A16-A4 4 32K X 8	32
256	A25-A18 32K X 9	A17-A4 8 32K X 8	64

3.3 Local Bus Interface

The local bus interface unit emulates most CPU control and status signals. The CPU's data and address lines, also, are manipulated to respond to the cycle's requirements.

MODE	R/C	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
256K PM	ROW	-	-	A19	A18	A17	A16	A15	A9	A13	A12	A11
	COL			A10	A14	A8	A7	A6	A5	A4	A3	A2
256K IL	ROW	-	-	A19	A18	A17	A16	A15	A9	A13	A12	A20
	COL			A11	A14	A8	A7	A6	A5	A4	A3	A2
1M PM	ROW	-	A21	A19	A18	A17	A16	A15	A9	A13	A12	A20
	COL		A11	A10	A14	A8	A7	A6	A5	A4	A3	A2
1M IL	ROW	-	A21	A19	A18	A17	A16	A15	A9	A13	A22	A20
	COL		A12	A11	A14	A8	A7	A6	A5	A4	A3	A2
4M PM	ROW	A23	A21	A19	A18	A17	A16	A15	A9	A13	A22	A20
	COL	A12	A11	A10	A14	A8	A7	A6	A5	A4	A3	A2
4M IL	ROW	A23	A21	A19	A18	A17	A16	A15	A9	A24	A22	A20
	COL	A13	A12	A11	A14	A8	A7	A6	A5	A4	A3	A2

Table 3 Address Map PM: Page Mode IL: Block Interleave

The local bus controller sends out MADS#, after it recieves the cycle start request from the CPU interface unit. It then waits for the return ofready from the local bus. The 82C497 latches all the CPU signals if the write cycle passes to the local bus. The read data is also latched before being sent to the CPU.

The 82C497 converts a read miss (not dirty) cycle into four local bus cycles. Four MADS# signals are sent out and four ready signals monitored. For the 486 system, four more CPU states, minimum, are required to read the data from the external cache and sent to the CPU.

The read miss (dirty) cycle needs eight local bus cycles to complete. Four for writing stale data back to DRAM and the other four for updating the external cache. The WR# and A23-A15 will be transformed correctly during the write back process.

Since the 82C497 provides one level of write buffer, the write cycle is processed concurrently with the CPU cycle. The consequent local bus cycle can not start until the write cycle is completed. The CPU is put onto a wait-state during this process.

3.4 Clock Signals

The 82C497 has three clock sources:

1. MCLK

MCLK is the clock from the local bus, used to synchronize the local bus state. It is a single phase clock and has a normal frequency of25MHZ or 33MHZ. The single phase clock interface with the local bus provides higher reliability as compared to the double frequency clock approach.

2. CLK

The 82C497 uses CLK to synchronize the CPU states when interfacing with the '386 or '486. For the 486 system, CLK has the same clock source as the 486 clock input. For the 386 system, CLK represents the 386's SYSCLK, inverted (SYSCLKB).

3. CLK2

The CLK2 input is used to maintain the clock phase between '386 and 82C497 by controlling the CPU reset timing. For the 486 system, CLK2 is simply connected to CLK.

'386: The Oscillator X provides a double frequency clock which is sent to the 82C496 in the double(pin 2) and single(pin 183) frequency format. The single frequency clock is also sent to the 82C497(pin 51).

Oscillator Y generates a double frequency clock that is sent to the CPU. The 82C497 also gets the double frequency clock(pin 159) and the single frequency clock(pin 2).

'486: The Oscillator X provides a double frequency clock which is sent to the 82C496 in the double(pin 2) and single(pin 183) frequency format. The single frequency clock is also sent to the 82C497(pin 51).

Oscillator Y needs to send two single frequency clocks to the 82C497(pins 2 and 159). This can be achieved by generating a double frequency clock and dividing by 2(for inventory and backward compatibility sake) or generating the single frequency clock to begin with. The single frequency clock is also sent to the CPU.

CLOCKING SCHEME

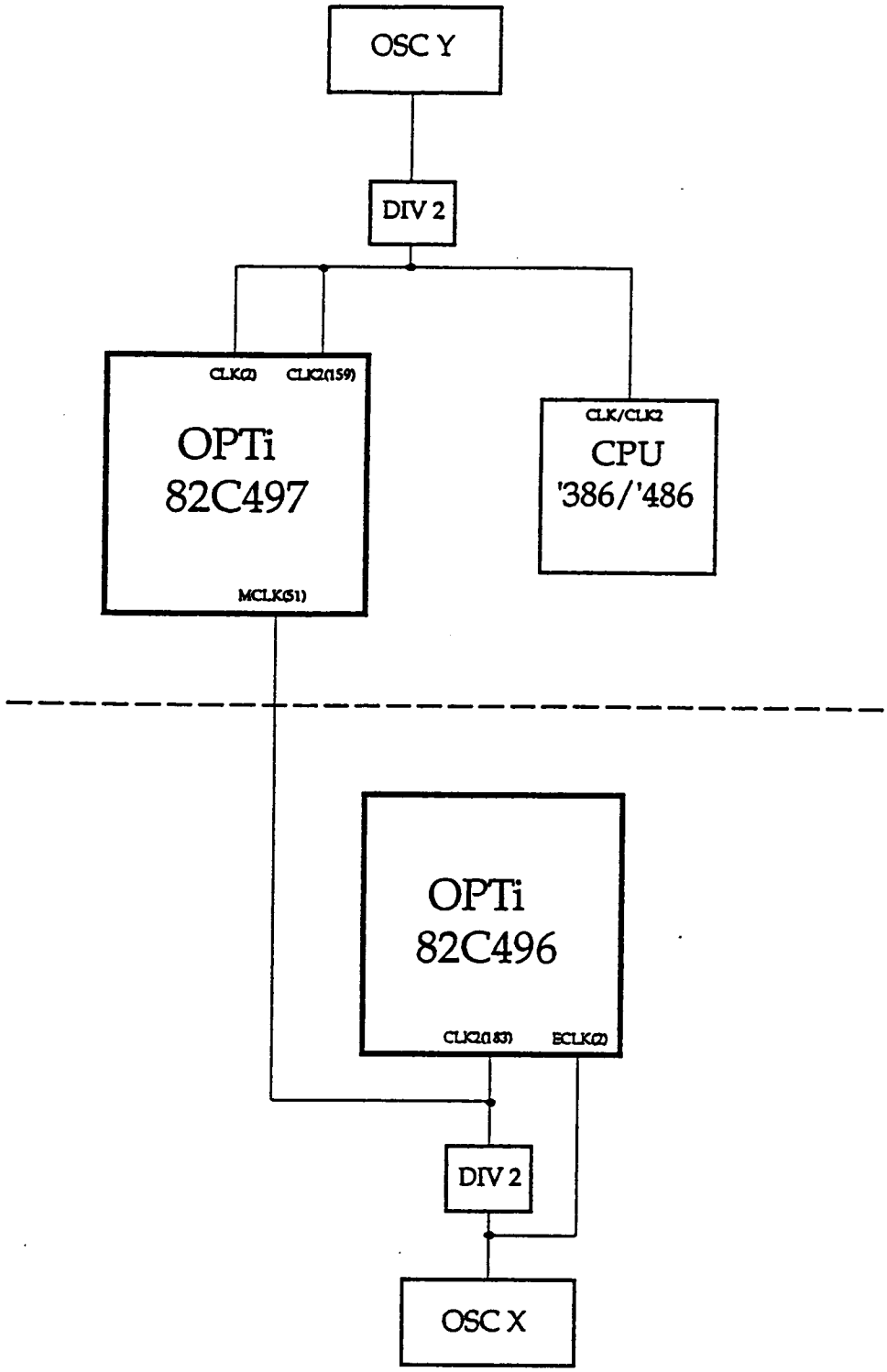


FIGURE 3B

3.5 Reset Signals Generation

The 82C497 generates the CPU reset signal based on the following situations:

1. Power on reset: by monitoring the system reset input from the 82C496.

2. Warm reset: evoked by CPU reset request through keyboard reset emulation.

3. Shut down: when a shut down instruction is executed.

When configured to interface with 387, the 82C497 asserts the NPRST signal if:

1. CPURST is activated, or
2. an IO write to F1 hex is issued.

3.6 Keyboard GATEA20 and Reset Emulation

The 82C497 emulates the keyboard's GATEA20 and Reset generation.

1. GATEA20

The cache controller intercepts the GATEA20 setting/resetting instruction by monitoring IO write cycle to the port 64 hex with D1 command, then accepting data bit 1 from the, next, IO port 60 hex write cycle.

The 82C497 converts the CA20 to A20 which goes to the local bus and AT bus according to the GATEA20's condition.

2. Keyboard Reset

The keyboard reset is emulated by monitoring the IO write cycle port 64 hex with FE command. The CPU reset will not start until a HALT instruction follows if bit 7 of the index 36h is enabled, otherwisw, the CPU reset is generated right after the cycle I/O write is completed.

4.0 82C497 PINS

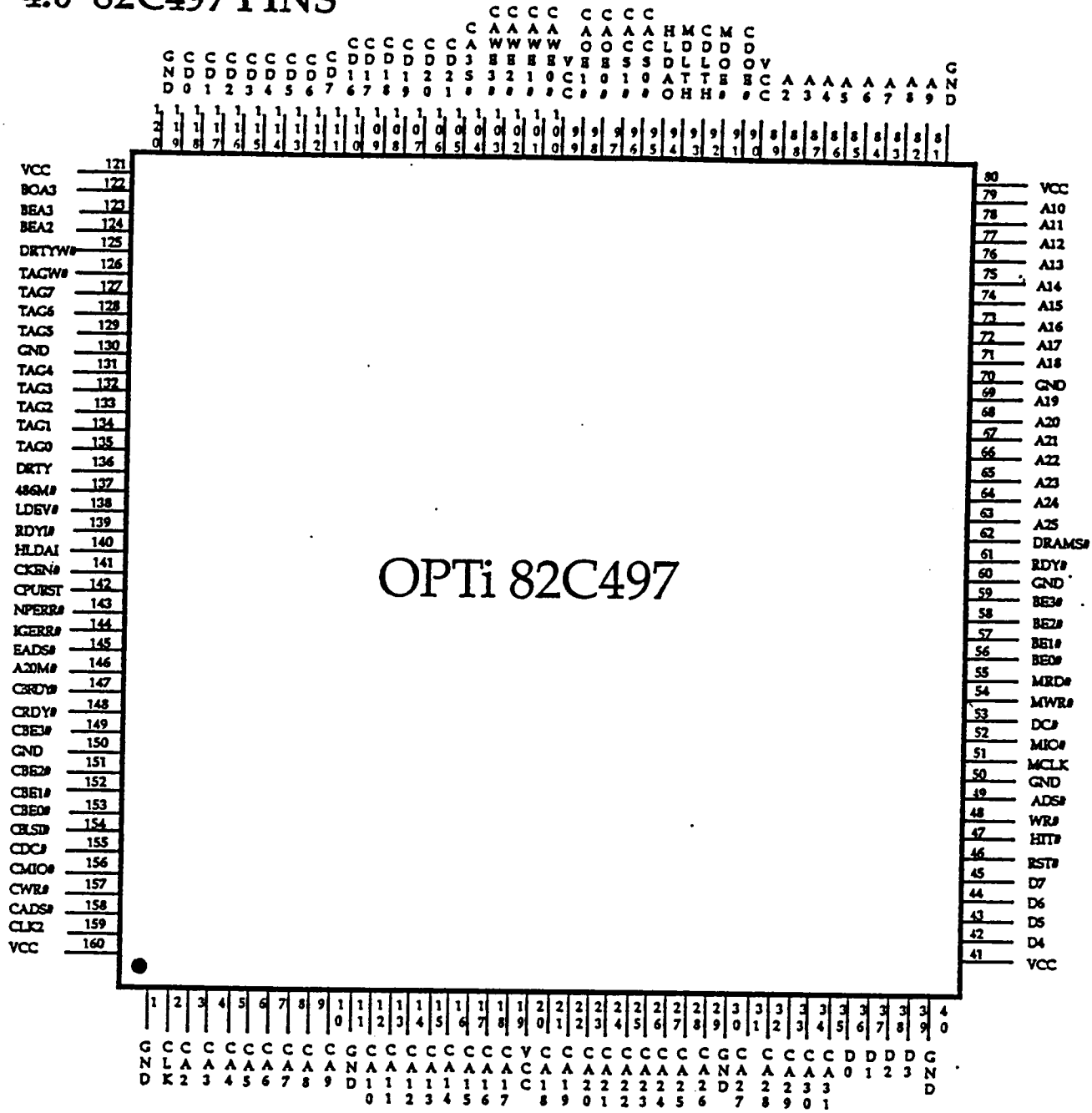


Figure 4

4.1 PIN CROSS REFERENCE LIST

#	Type	Pin Name	#	Type	Pin Name	#	Type	Pin Name
1	I	GROUND	56	B	BSD#	111	I	CD16
2	I	CLK	57	B	BSI#	112	B	CD7
3	B	CA2	58	B	BS2#	113	B	CD6
4	B	CA3	59	B	BS3#	114	B	CD5
5	B	CA4	60	I	GROUND	115	B	CD4
6	B	CA5	61	I	RDY#	116	B	CD3
7	B	CA6	62	O	DRAMS#	117	B	CD2
8	B	CA7	63	B	A25	118	B	CD1
9	B	CA8	64	B	A24	119	B	CD0
10	B	CA9	65	B	A23	120	I	GROUND
11	I	GROUND	66	B	A22	121	I	VCC
12	B	CA10	67	B	A21	122	O	BOA3
13	B	CA11	68	B	A20	123	O	BEA3
14	B	CA12	69	B	A19	124	O	BEA2
15	B	CA13	70	I	GROUND	125	O	DRTYW#
16	B	CA14	71	B	A18	126	O	TAGW#
17	B	CA15	72	B	A17	127	B	TAG7
18	B	CA16	73	B	A16	128	B	TAG6
19	B	CA17	74	B	A15	129	B	TAG5
20	I	VCC	75	B	A14	130	I	GROUND
21	B	CA18	76	B	A13	131	B	TAG4
22	B	CA19	77	B	A12	132	B	TAG3
23	B	CA20	78	B	A11	133	B	TAG2
24	B	CA21	79	B	A10	134	B	TAG1
25	B	CA22	80	I	VCC	135	B	TAG0
26	B	CA23	81	I	GROUND	136	B	DRTY
27	B	CA24	82	B	A9	137	I	486M#:
28	B	CA25	83	B	A8	138	B	LDEV#:
29	B	CA26	84	B	A7	139	I	RDYI#:
30	I	GROUND	85	B	A6	140	I	HOLDAI
31	B	CA27	86	B	A5	141	O	CKEN#
32	B	CA28	87	B	A4	142	O	CPURST
33	B	CA29	88	B	A3	143	I	NPERR#
34	B	CA30	89	B	A2	144	O	IGERR#
35	B	CA31	90	I	VCC	145	O	EADS#
36	I	D0	91	O	CDOE#	146	O	A20M#
37	I	D1	92	O	MDOE#	147	O	CBRDY#
38	I	D2	93	O	CDLTH	148	O	CRDY#
39	I	D3	94	O	MDLTH	149	I	CBE3#
40	I	GROUND	95	O	HLDAO	150	I	GROUND
41	I	VCC	96	O	CACS0#	151	I	CBE2#
42	I	D4	97	O	CACS1#	152	I	CBE1#
43	I	D5	98	O	CAOE0#	153	I	CBE0#
44	I	D6	99	O	CAOE1#	154	I	CBLST#
45	I	D7	100	I	VCC	155	I	CDC#
46	I	RST#	101	O	CAWE0#	156	I	CMIO#
47	O	HIT#	102	O	CAWE1#	157	I	CWR#
48	TO	WR#	103	O	CAWE2#	158	I	CADS#
49	TO	ADS#	104	O	CAWE3#	159	I	CLK2
50	I	GROUND	105	O	CA3S#	160	I	VCC
51	I	MCLK	106	I	CD21	-	-	-
52	TO	MIO#	107	I	CD20	-	-	-
53	TO	DC#	108	I	CD19	-	-	-
54	I	MWR#	109	I	CD18	-	-	-
55	I	MRD#	110	I	CD17	-	-	-

4.3 PIN DESCRIPTION 82C497

CPU Interface Signals:

SYMBOL	PIN	TYPE	DESCRIPTION
			CPU INTERFACE
486M#	137	I	486 Mode selected when tied LOW. 386 Mode selected when HIGH.
A20M#	146	O	Address line 20 masked-out control for the '486.
CA(31:2)	35-31, 29-21, 19-12, 10-3	B	CPU address lines 31 to 2.Input during regular operation(default). Become outputs during Non-CPU cycles. During Non-CPU cycles, CA(23:2)reflect A(23:2) values and CA(31:24) are pulled LOW.
CADS#	158	I	CPU address strobe input.
CBE(3:0)#	149, 151-153	I	CPU byte enables 3 to 0.
CBLST#	154	I	Burst Last (CBLST#) input during '486 mode.
CBRDY#	147	O	Burst ready to the '486.
CD(21:16)	106-111	I	CPU data line 21 to 16. Selects Index registers.
CD(7:0)	112-119	B	CPU data lines 7 to 0. Input during normal operation. They are output, only, during the local bus read cycles.
CDC#	155	I	CPU data or control cycle status.

SYMBOL	PIN	TYPE	DESCRIPTION
			CO-PROCESSOR INTERFACE
IGERR# (NPRST)	144	O	In the '486 mode, this pin controls the 486's IGNNE#, ignore, numeric error, pin. In the '386 mode, this pin is directly connected to the '387's reset pin.
LDEV#	138	B	CPU Local bus device cycle indication pin. It is sampled by the end of the first T2. For non-CPU cycles it is decoded from address and qualified by the command signals.
NPERR#	143	I	Numerical processor error indication; used to : 1. Sample if the '387 exists. 2. Control the IGERR# generation.
RDYI#	139	I	CPU bus device ready input. It is re-synchronized by the 82C497 and then sent to the CPU through RDY# pin.
			LOCAL BUS INTERFACE
A(25:2)	63-69, 71-79, 82-89	B	Local bus address lines 25 to 2. These pins are output during the CPU cycles but become input during the non-CPU cycles.
ADS#	49	TO	Cycle start indication for the local bus.
BE(3:0)#	59-56	B	Local bus byte enables 3 to 0. These are outputs during CPU cycles. They become inputs during non-CPU cycles.
D(7:0)	45-42, 39-36	I	Local bus data lines 7 to 0.
DC#	53	TO	Local bus data/control status pin.

SYMBOL	PIN	TYPE	DESCRIPTION
			CPU INTERFACE (CONTINUED)
CKEN#	141	O	Handshake pin for the '486 pin KEN#. Asserted, both, at the beginning and the end of the cache line fill. The processor KEN# is ignored during write cycles.
CLK	2	I	Single phase clock input. It has the same source as the '486 clock input in the '486 mode. It is the inverted SYSCLK in the '386 mode.
CLK2	159	I	CLK2 controls the reset timingwhen operating in the '386 mode. It is directly tied to the SCLK signal in the '486 mode.
CMIO#	156	I	CPU Memory/IO cycle access indication signal.
CPURST	142	O	CPU Reset signal.
CRDY#	148	O	CPU Ready signal.
CWR#	157	I	CPU Read or Write sysle status signal.
EADS# (ERR#)	145	O	In the '486 mode, this pin is used by the '486 for bus snooping during the non-CPU cycles. In the '386 mode, this pin is connected directly to the ERROR# pin.
HOLDAI	140	I	Hold acknowledge input from the CPU.
MRD#	55	I	Command memory read signal. This signal will be used to access the SRAM during the DMA/Master cycles.
MWR#	54	I	Command memory write signal. This signal will be used to access the SRAM during the DMA/Master cycles.

SYMBOL	PIN	TYPE	DESCRIPTION
			LOCAL BUS INTERFACE(CONTINUED)
DRAMS#	62	O	CA31-CA26 all low decode to the Local bus.
HIT#	47	O	Cache hit indication signal. The 82C496 will not respond to the current memory access when it monitors this signal to be active during the non-CPU cycles.
HLDAO	95	O	Hold acknowledge to the local bus.
MCLK	51	I	Local bus operating clock. It is used to synchronize the phase.
MIO#	52	TO	Local bus Memory/IO cycle status signal.
RDY#	61	I	Local bus cycle completion signal.
RST#	46	I	System reset. Power up reset signal.
WR#	48	TO	Local bus write/read cycle status.
			BUFFER CONTROL SIGNALS
CDLTH	93	O	CPU data bus latch control signal. The LOW to HIGH transition latches CD(31:0) to D(31:0) data path.
CDOE#	91	O	Output enable control siganls for the buffers from CD(31:0) to D(31:0).
MDLTH	94	O	Local data bus latch control signal. The LOW to HIGH transition latches D(31:0) to CD(31:0) data path.

SYMBOL	PIN	TYPE	DESCRIPTION
			BUFFER CONTROL SIGNALS(CONTINUED)
MDOE#	92	O	Output enable control siganls for the buffers from D(31:0) to CD(31:0).
			CACHE INTERFACE
BEA2	124	O	One of the EVEN bank cache memory address line 2 sources. It is connected to a tri-stated CA2 buffer's output which is controlled by CA3S#.
BEA3	123	O	One of the EVEN bank cache memory address line 3 sources. It is connected to a tri-stated CA3 buffer's output which is controlled by CA3S#.
BOA3	122	O	One of the ODD bank cache memory address line 3 sources. It is connected to a tri-stated CA3 buffer's output which is controlled by CA3S#.
CA3S#	105	O	Cache memory address line 3 source selection pin. CA3 selected when this signal is LOW, otherwise BEA3 or BOA3 is selected. The selection is changed from CA3 to BEA3 or BOA3 at the end of the first T2.
CACS0#	96	O	Even bank cache memory chip select control signal.
CACS1#	97	O	Odd bank cache memory chip select control signal.
CAOE0#	98	O	Even bank cache memory output enable control signal.
CAOE1#	99	O	Odd bank cache memory output enable control signal.

SYMBOL	PIN	TYPE	DESCRIPTION
			CACHE INTERFACE(CONTINUED)
CAWE(3:0)#	104-101	O	Cache memory write enable control signals for the bytes 3 to 0.
DRTY	136	B	Data bit for the DIRTY RAM. It is an input pin, normally. It becomes an output pin when DRTYW# is activated.
DRTYW#	125	O	Dirty RAM write enable control signal. A cache write hit will set the dirty bit for the currently accessed cache line.
TAG(7:0)	127-129, 131-135	B	Data bits for the TAG RAM. They are inputs in normal conditions. They become outputs whenever TAGW# is activated.
TAGW#	126	O	Tag RAM write enable control signal.A cache read miss cycle will update the valid TAG of the accessed cache line.
			MISCELLANEOUS SIGNALS
VCC	20,41, 80,90, 100,121 160	I	+5 POWER.
GROUND	1,11,30 40,50, 60,70, 81,120, 130,150	I	GROUND.

5.0 82C497 Register Description

There are nine configuration registers inside the 82C497. An indexing scheme is used to access all the registers of 82C496/82C497 chipset. Port 22 hex is the index register and port 24 hex is the data register. EVERY data access must be preceded by a write to port 22 hex, even if the same register is being accessed.

Index Register:34h
(Write only; duplicated in the 82C496)

BIT	FUNCTION	DEFAULT
7-1	RESERVED	-
0	Video BIOS at C000h-C8000h 1 = "Cacheable" 0 = "Non-Cacheable"	0

Index Register:36h
(Write only; duplicated in the 82C496)

BIT	FUNCTION	DEFAULT
7	RESERVED	-
6	When Keyboard Reset active; Wait for HALT instruction before generating CPURST 1 = "Enable" 0 = "Disable"	1
5	RESERVED	-
4	All memory Non-Cacheable, Always. 1 = "Always Non-Cacheable" 0 = "Disable"	0
3-0	RESERVED	-

Index Register:37h
(Read/Write; duplicated in the 82C496)

BIT	FUNCTION	DEFAULT
7	RESERVED	-
6-4	Size of Non-Cacheable memory block 1: 000 = 64K 001 = 128K 010 = 256K 011 = 512K 100 = 2M 101 = 4M 110 = 8M 111 = DISABLE	111
3-2	RESERVED	-
1-0	Address bits A25 and A24 of the non-cacheable memory block 1. These two bits are always valid, no matter what the size of the non-cacheable block.	xx

Index Register:38h
(Read/Write; duplicated in the 82C496)

BIT	FUNCTION	DEFAULT
7-0	Address bits A23-A16 of Non-Cacheable memory block 1	xxxxxxxx
	Valid starting address bits versus the non-cacheable block size:	

Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	D
256K	V	V	V	V	V	V	D	D
512K	V	V	V	V	V	D	D	D
2M	V	V	V	D	D	D	D	D
4M	V	V	D	D	D	D	D	D
4M	V	D	D	D	D	D	D	D

V=VALID D=DON'T CARE

Index Register:39h
(Read/Write; duplicated in the 82C496)

BIT	FUNCTION	DEFAULT
7	RESERVED	-
6-4	Size of Non-Cacheable memory block 2: 000 = 64K 001 = 128K 010 = 256K 011 = 512K 100 = 2M 101 = 4M 110 = 8M 111 = DISABLE	111
3-2	RESERVED	-
1-0	Address bits A25 and A24 of the non-cacheable memory block 2. These two bits are always valid, no matter what the size of the non-cacheable block.	xx

Index Register:3Ah
(Read/Write; duplicated in the 82C496)

BIT	FUNCTION	DEFAULT
7-0	Address bits A23-A16 of Non-Cacheable memory block 2.	xxxxxxxx
	Valid starting address bits versus the non-cacheable block size:	

Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	D
256K	V	V	V	V	V	V	D	D
512K	V	V	V	V	V	D	D	D
2M	V	V	V	D	D	D	D	D
4M	V	V	D	D	D	D	D	D
4M	V	D	D	D	D	D	D	D

V=VALID D=DON'T CARE

Index Register:3Bh
(Read/Write)

BIT	FUNCTION	DEFAULT
7-6	Cache controller operating mode setting: 00:Cache disable;Any memory read invalidates tag 01:Cache enable 10:Cache disable;Any memory read writes 3Ch and 3Dh index register contents to tag 11:Cache disable;Any memory read, readsthe tag into 3Bh and 3Ch index registers.	00
5-4	Cache size selection: SEL. '386 '486 00 32K 64K 01 64K 128K 10 128K 256K 11 256K 512K	00
3	RESERVED	-
2	Cache read hit 1st cycle wait state selection: '0' = 3-1-1-1 or 3-2-2-2 cycle '1' = 2-1-1-1 or 2-2-2-2 cycle	0
1	Cache write hit wait state selection: '0' = 1 wait state '1' = 0 wait state(386 mode only)	0
0	Burst cycle wait states: '0' = 3-1-1-1 or 2-1-1-1 cycle '1' = 3-2-2-2 or 2-2-2-2 cycle	0

Index Register:3Ch
(Read/Write)

BIT	FUNCTION	DEFAULT
7	Post write function selection: '1' = enable '0' = disable	1
6-1	RESERVED	-
0	Working register to test dirty bit	x

Index Register:3Dh
(Read/Write)

BIT	FUNCTION	DEFAULT
7-0	Working registers to test the TAG bits	xxxxxxxx

6.0 SPECIFICATIONS

6.1 82C497 33/40/50 MHz DC Characteristics
(TA=0C to 70C, Vcc=5V+/- 5%)

Symbol	Description	Min	Max	Units
VIL	Input low voltage	-0.3	0.8	V
VIH	Input high voltage	2.0	Vcc+0.3	V
VOL	Output low voltage IOL=3.0 mA all pins except IOL=6.0 mA all group A IOL=12.0 mA all group B	-	0.45	V
VOH	Output high voltage IOH=-1.6 mA all pins except IOH=-3.2 mA all group A IOH=-6.4 mA all group B	2.4	-	V
IIL	Input leakage current, VIN=Vcc 0V < VIN <Vcc	-10	10	uA
IOZ	Tristate leakage current 0.45V < Vout < Vcc	-	10	uA
CIN	Input Capacitance	-	12	pF
COUT	Ouput Capacitance	-	12	pF
CIO	I/O Capacitance	-	12	pF
ICC	Power supply current @ 33 MHz	-	50	mA

Group A pins:

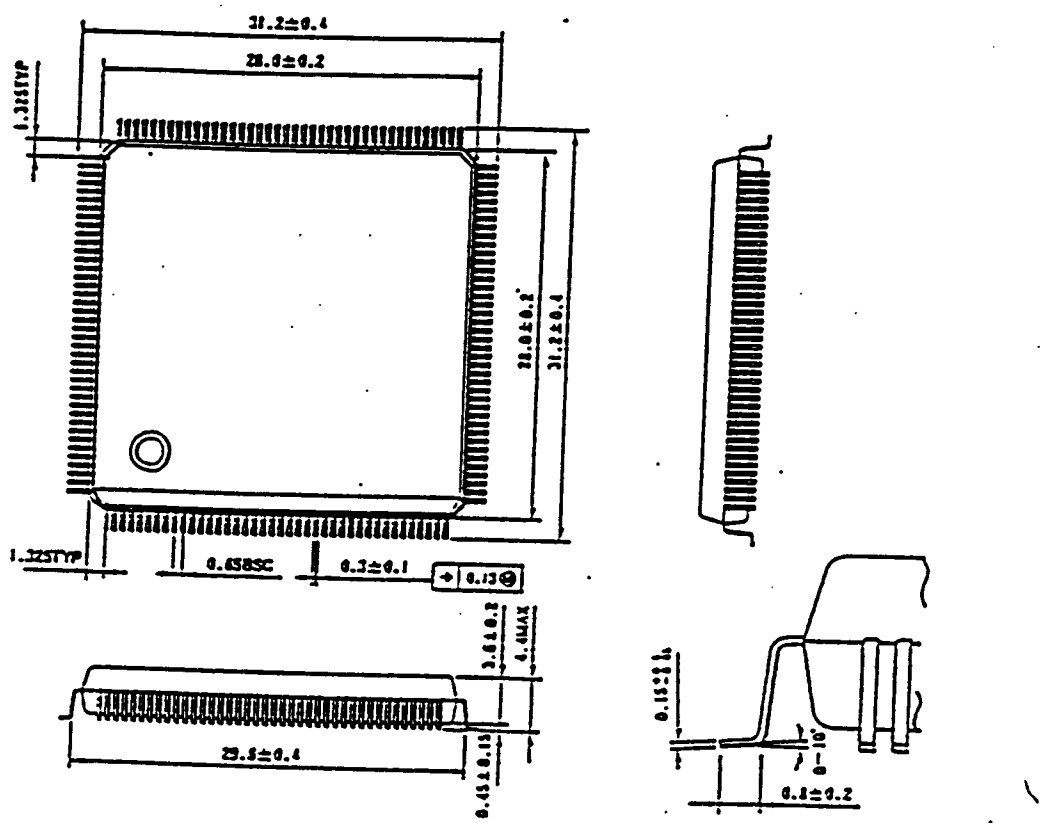
Group B pins:

6.2 Absolute Maximum Ratings

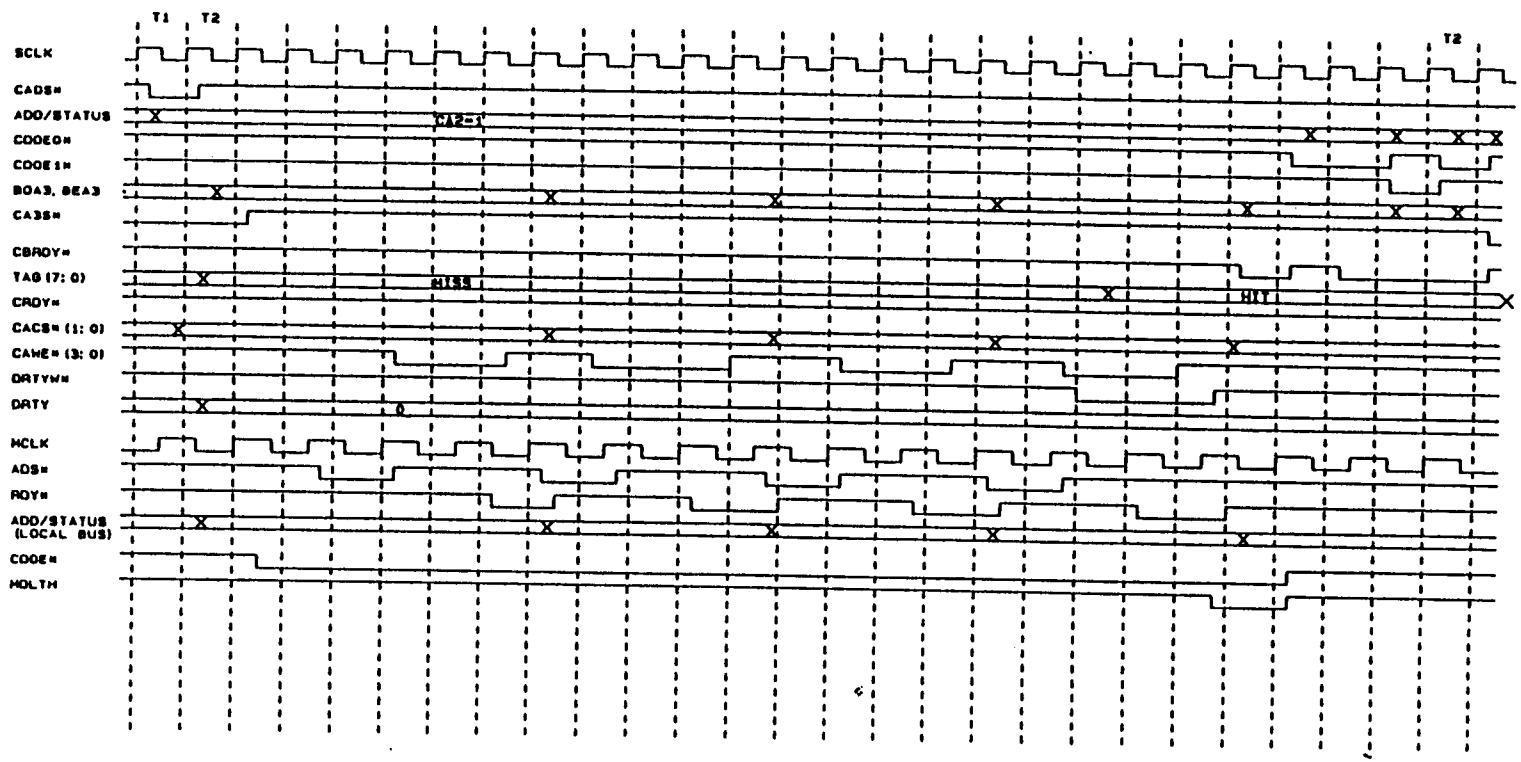
Symbol	Description	Min	Max	Units
VCC	Supply voltage	-0.5	6.5	V
VI	Input voltage	-0.5	Vcc+0.5	V
VO	Output voltage	-0.5	Vcc+0.5	V
TOP	Operating temperature	0	70	C
TSTG	Storage temperature	-40	125	C

6.5 Package Information and Ordering

QFP160-P-2828(160-Pin Plastic Flat Package)



2ND CACHE READ MISS NOT DIRTY CYCLE



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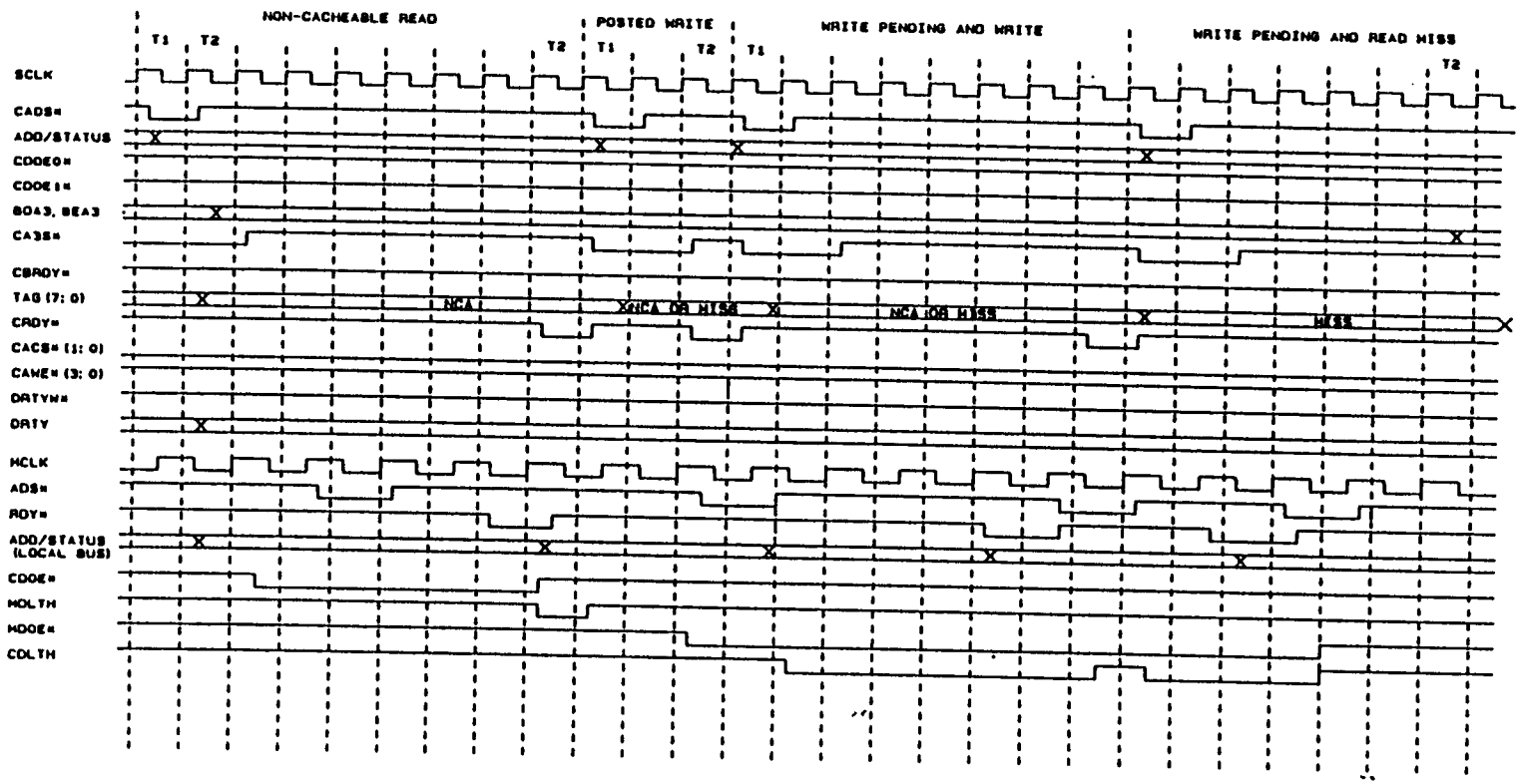

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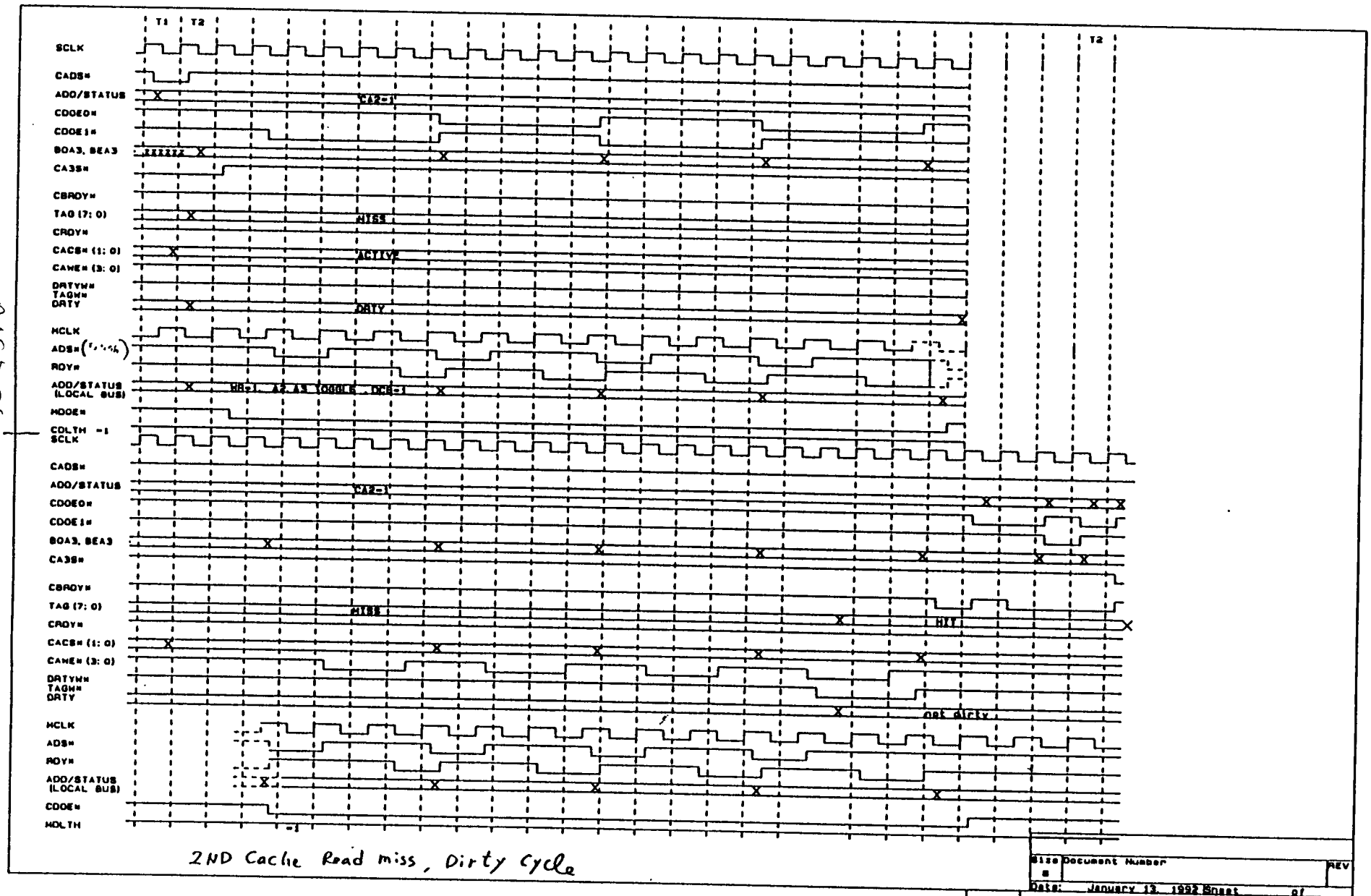

2ND Cache Read miss, Dirty Cycle

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