PHILIPS

FAST TTL Logic series

IC15 1986

PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Book IC15 1986

FAST TTL Logic series

FAST TTL LOGIC SERIES

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons**

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T8 **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers and infrared detectors**

T15 **Dry reed switches**

T16 **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8a **Light-emitting diodes**

S8b **Devices for optoelectronics**
Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave transistors**

S12 **Surface acoustic wave devices**

S13 **Semiconductor sensors**

***S14** **Liquid Crystal Displays**

*To be issued shortly.

INTEGRATED CIRCUITS (PURPLE SERIES)

The NEW SERIES of handbooks is now completed. With effect from the publication date of this handbook the "N" in the handbook code number will be deleted.
Handbooks to be replaced during 1986 are shown below.

The purple series of handbooks comprises:

IC01	**Radio, audio and associated systems** Bipolar, MOS	new issue 1986 IC01N 1985
IC02a/b	**Video and associated systems** Bipolar, MOS	new issue 1986 IC02Na/b 1985
IC03	**Integrated circuits for telephony** Bipolar, MOS	new issue 1986 IC03N 1985
IC04	**HE4000B logic family** CMOS	new issue 1986 IC4 1983
IC05N	**HE4000B logic family — uncased ICs** CMOS	published 1984
IC06N	**High-speed CMOS; PC74HC/HCT/HCU** Logic family	published 1986
IC08	**ECL 10K and 100K logic families**	New issue 1986 IC08N 1984
IC09N	**TTL logic series**	published 1986
IC10	**Memories** MOS, TTL, ECL	new issue 1986 IC7 1982
IC11N	**Linear LSI**	published 1985
Supplement to IC11N	**Linear LSI**	published 1986
IC12	**I²C-bus compatible ICs**	not yet issued
IC13	**Semi-custom** Programmable Logic Devices (PLD)	new issue 1986 IC13N 1985
IC14N	**Microprocessors, microcontrollers and peripherals** Bipolar, MOS	published 1985
IC15	**FAST TTL logic series**	new issue 1986 IC15N 1985
IC16	**CMOS integrated circuits for clocks and watches**	first issue 1986
IC17	**Integrated Services Digital Networks (ISDN)**	not yet issued
IC18	**Microprocessors and peripherals**	new issue 1986*

* The Microprocessors were included in handbook IC14N 1985, so IC18 will replace that part of IC14N.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C2	Television tuners, coaxial aerial input assemblies, surface acoustic wave filters
C3	Loudspeakers
C4	Ferroxcube potcores, square cores and cross cores
C5	Ferroxcube for power, audio/video and accelerators
C6	Synchronous motors and gearboxes
C7	Variable capacitors
C8	Variable mains transformers
C9	Piezoelectric quartz devices
C11	Varistors, thermistors and sensors
C12	Potentiometers, encoders and switches
C13	Fixed resistors
C14	Electrolytic and solid capacitors
C15	Ceramic capacitors
C16	Permanent magnet materials
C17	Stepping motors and associated electronics
C18	Direct current motors
C19	Piezoelectric ceramics
C20	Wire-wound components for TVs and monitors
C22	Film capacitors

GENERAL CONTENTS

Preface

Signetics would like to thank you for your interest in our FAST product line. Because of its wide customer acceptance, FAST has become the preferred high-performance logic family of the 80's. We are proud to participate in and contribute to the dynamic growth of this product family.

Each data sheet contained in this manual is designed to stand alone and reflect the latest DC and AC specifications for a particular product. Several changes differentiate these data sheets from previous ones. First, all reference to military product has been deleted, specifically, to reflect recent government requirements imposed by Revision C of MIL-STD 883, including the general provisions of Paragraph 1.2. Specifications for military-grade FAST products are available in the latest Military Products Data Manual available from your nearest Signetics Sales Office, sales representative, or authorized distributor. Second, each commercial 74F product is specified over a 10% V_{CC} range, for both AC and DC parameters. Additionally, DC specifications for V_{OH} and V_{OL} are provided over the 5% V_{CC} range.

This 1986 FAST Data Manual consolidates 1984 Volumes 1 and 2, updates a large number of data sheets which were previously "preview" or "preliminary", and adds many newly defined products.

Other features of this data manual include:

- Updated Availability and Functional Cross-Reference Guides
- An expanded Circuit Characteristics Section
- A User's Guide
- Selected Application Notes
- An expanded chapter on Surface Mounted Devices (SMD) and an Application Note on Thermal Considerations in SMD
- A new section on package outlines

New FAST part types are being released continuously. As you see new product announcements, please contact your nearest Signetics Sales Office, sales representative, or authorized distributor for the latest technical information.

In addition to FAST, Signetics Standard Products Division offers the industry's broadest line of commercially available Logic Products, spanning a wide speed/power spectrum from 100K/10K ECL to 74HC/HCT CMOS, including industry standard families such as 4000 Series CMOS, 74, 74LS, 74S, 8T, and 8200 Logic. Information on these product lines is also available from your nearest Signetics Sales Office, sales representative, or authorized distributor.

Signetics Standard Products Division — Logic Products

TM FAST is a trademark of Fairchild Semiconductor Corporation

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Logic Products

Product Status

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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74F FAST TTL
Introduction

Logic Products

THE HIGH-SPEED LOGIC OF THE '80s

Product Description

Signetics has combined advanced oxide-isolated fabrication techniques with standard TTL functions to create a new family designed for the '80s. The high operating speeds of FAST can push system operating speeds into areas previously reserved for 10K ECL, but with simple TTL design rules and single 5V power supplies. Low input loading allows the user to mix LS, ALS, and HCMOS in the same system without the need for translators and restrictive fanout requirements.

FAST circuits are pin-for-pin replacements for 74S types, but offer dissipation 3-4 times lower and higher operating speeds. Existing systems can achive much lower power and improved performance by replaceing the 74S types with the corresponding FAST devices.

The input structure provides better noise immunity because of higher thresholds, while the oxide-isolation and new circuit techniques create devices that have less variaton with temperature or supply voltage than existing TTL logic families. Signetics guarantees all AC parameters under realistic system conditions – across the supply voltage spread and the temperature range, and with heavy 50pF output loads.

The use of high-capacitance PNP inputs has been avoided, and clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unsued inputs to be tied directly to V_{CC} without pull-up resistors.

Multiple sources and a complete family of powerful circuits combine to make Signetics FAST the logic choice of the '80s.

FEATURES

- **3ns propagation delays**
- **4mW/gate power dissipation**
- **Guaranteed AC performance over temperature and extended V_{CC} Range: 5V ± 10%**
- **High impedance NPN base input structure on many types for reduced bus loading in LOW state (I_{IL} = 20μA)**
- **Standard TTL functions and pinouts**
- **Replacement for "S" types...1/4 the power**
- **Designer's choice for new system designs**

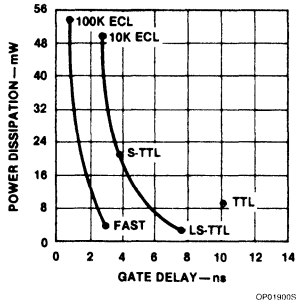


Figure 1. The Speed/Power Spectrum

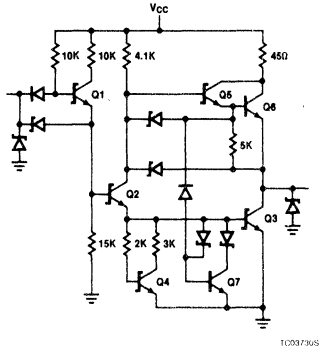


Figure 2. Basic FAST Gate

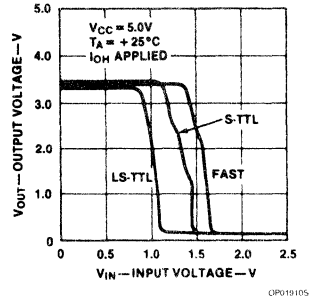
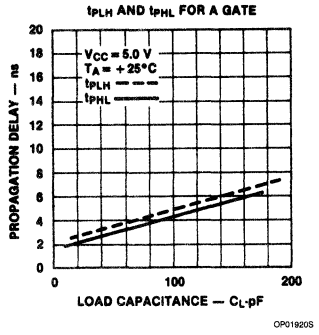
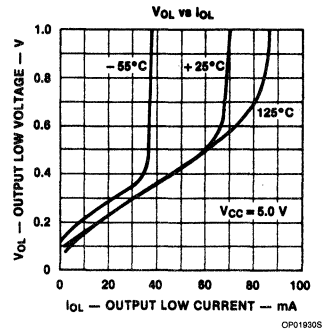


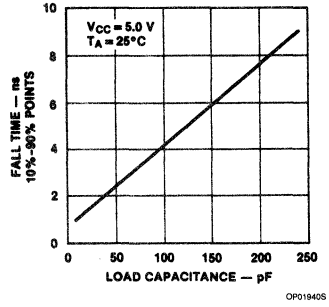
Figure 3. Transfer Functions At Room Temperature



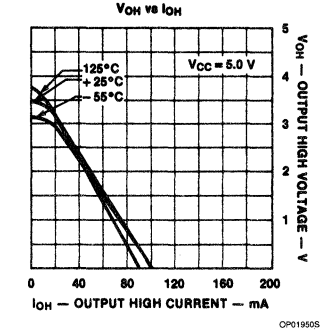
'F00
Figure 4. Propagation Delay VS Load Capacitance



'F00
Figure 5. Output LOW Characteristics



'F00
Figure 6. Fall Time VS Load Capacitance



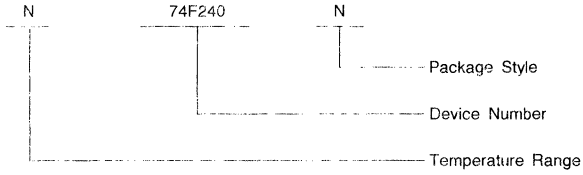
'F00
Figure 7. Output HIGH Characteristics

Ordering Information

Signetics commercial FAST products are generally available in both standard dual-in-line and surface mounted options. The ordering code specifies temperature range, device number, and package style as shown below. For commercial product, the standard temperature range is 0-70°C. Available package options are shown on individual data sheets in the "Ordering Code" block. For surface mounted devices the S.O. plastic dual-in-line package is supplied up to and including 28 pins. Above 28 pins, the plastic leaded chip carrier is utilized.

A wide variety of functions and package options is available for military products. Information on military products is available from the nearest Signetics sales office, sales representative, or authorized distributor. The Signetics Military Products Data Manual contains specifications, package, and ordering information for all military-grade products.

ORDERING CODE EXAMPLES



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
N = Commercial Range 0°C to 70°C	74FXXX	N = Plastic DIP D = Plastic S.O. DIP (surface mounted) A = Plastic Leaded Chip Carrier
S = Military Range −55°C to 125°C	See Military Products Data Manual	

Signetics

Logic Products

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Logic Products

DEVICE	DESCRIPTION	AVAILABILITY
74F00	Quad 2-Input NAND Gate	A
74F02	Quad 2-Input NOR Gate	A
74F04	Hex Inverter	A
74F08	Quad 2-Input AND GATE	A
74F10	Triple 3-Input NAND Gate	A
74F11	Triple 3-Input AND Gate	A
74F13	Dual 4-Input NAND Schmitt Trigger	A
74F14	Hex Schmitt Trigger	A
74F20	Dual 4-Input NAND Gate	A
74F27	Triple 3-Input NOR Gate	A
74F30	8-Input NAND Gate	A
74F32	Quad 2-Input OR Gate	A
74F37	Quad 2-Input NAND Buffer	A
74F38	Quad 2-Input NAND Buffer, OC	A
74F40	Dual 4-Input NAND Buffer	A
74F51	Dual 2-Wide 3-Input, 2-Wide 2-Input AND-OR Invert Gate	A
74F64	4-2-3-2 Input AND/OR Invert Gate	A
74F74	Dual D-Type Flip-Flop	A
74F83	4-Bit Binary Adder with Fast Carry	1H 86
74F85	4-Bit Magnitude Comparator	A
74F86	Quad 2-Input Exclusive-OR Gate	A
74F109	Dual JK Flip-Flop	A
74F112	Dual JK Flip-Flop	1H 86
74F113	Dual JK Flip-Flop	1H 86
74F114	Dual JK Flip-Flop	1H 86
74F125	Quad Buffer, 3-State	A
74F126	Quad Buffer, 3-State	A
74F132	Quad 2-Input NAND Schmitt Trigger	A
74F138	1-of-8 Decoder/Demultiplexer	A
74F139	Dual 1-of-4 Decoder/Demultiplexer	A
74F148	8-Bit Priority Encoder	A
74F151	8-Input Multiplexer	A
74F153	Dual 4-Input Multiplexer	A
74F157	Quad 2-Input Multiplexer	A
74F158	Quad 2-Input Multiplexer	A
74F160A	BCD Decade Counter, Asynch Reset	1H 86
74F161A	4-Bit Binary Counter, Asynch Reset	A
74F162A	BCD Decade Counter, Synch Reset	1H 86
74F163A	4-Bit Binary Counter, Synch Reset	A
74F164	8-Bit SIPO Shift Register	1H 86
74F166	8-Bit Serial/Parallel-In/Serial-Out Shift Register	A
74F168	4-Bit Up/Down Decade Counter (3-State)	1H 86
74F169	4-Bit Up/Down Binary Counter (3-State)	1H 86
74F174	Hex D-Flip-Flop with Common Master Reset	A
74F175	Quad D Flip-Flop with Common Master Reset	A
74F181	4-Bit Arithmetic Logic Unit	A
74F182	Carry Lookahead Generator	A
74F189	4-Bit Random Access Memory (3-State)	2H 86
74F190	Up/Down Decade Counter	1H 86
74F191	Up/Down Binary Counter	1H 86
74F192	Up/Down Decade Counter	1H 86
74F193	Up/Down Binary Counter	1H 86
74F194	4-Bit Bidirectional Universal Shift Register	A
74F195	4-Bit Parallel Access Shift Register	A
74F198	8-Bit Bidirectional Universal Shift Register	1H 86
74F199	8-Bit Parallel-Access Shift Register	1H 86
74F240	Octal Inverting Bus/Line Driver (3-State)	A
74F241	Octal Bus/Line Driver (3-State)	A
74F242	Quad Bus Transceiver (3-State)	A
74F243	Quad Bus Transceiver (3-State)	A
74F244	Quad Bus/Line Driver (3-State)	A
74F245	Octal Bus Transceiver (3-State)	A
74F251	8-Input Multiplexer (3-State)	A
74F253	Dual 4-Input Multiplexer (3-State)	A
74F256	Dual 4-Bit Addressable Latch	A
74F257	Quad 2-Input Multiplexer (3-State)	A
74F258	Quad 2-Input Multiplexer (3-State)	A
74F259	8-Bit Addressable Latch	A
74F260	Dual 5-Input NOR Gate	A

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DEVICE	DESCRIPTION	AVAILA-BILITY
74F269	8-Bit Up/Down Counter (3-State)	A
74F273	Octal D Flip-Flop	A
74F280A	9-Bit Parity Generator/Checker	A
74F283	4-Bit Adder	A
74F298	Quad 2-Input Multiplexer	A
74F299	Octal Shift/Storage Register (3-State)	A
74F322	Octal Shift/Storage Register (3-State)	1H 86
74F323	Octal Shift/Storage Register (3-State)	1H 86
74F350	4-Bit Shifter (3-State)	A
74F352	Dual 4-Input Multiplexer (Inverted '153)	A
74F353	Dual 4-Input Multiplexer (Inverted '253)	A
74F365	Hex Buffer with Common Enable (3-State)	A
74F366	Hex Inverter with Common Enable (3-State)	A
74F367	Hex Buffer, 4-Bit and 2-Bit (3-State)	A
74F368	Hex Inverter, 4-Bit and 2-Bit (3-State)	A
74F373	Octal D Latch (3-State)	A
74F374	Octal D Flip-Flop (3-State)	A
74F377	Octal D-Type Flip-Flop with Enable	A
74F378	Hex D Flip-Flop with Enable	A
74F379	Quad D Flip-Flop with Enable	A
74F381	4-Bit Arithmetic Logic Unit	A
74F382	4-Bit Arithmetic Logic Unit	A
74F384	8-Bit Serial/Parallel Two's Complement Multiplier	2H 86
74F385	Quad Serial Adder/Subtractor	2H 86
74F395	4-Bit Cascadable Shift Register (3-State)	A
74F398	4-Bit Flip-Flop, True and Complement Outputs	A
74F399	4-Bit Flip-Flop, True and Complement Outputs	A
74F412	Multi-Mode Buffered Latch (3-State)	1H 86
74F432	Octal Multi-Mode Buffered Latch	1H 86
74F455	Octal Buffer w/Parity Generator Checker	A
74F456	Octal Buffer w/Parity Generator Checker	A
74F521	Octal Comparator	A
74F524	8-Bit Register Comparator (OC)	1H 86
74F533	Inverting Octal D Latch (3-State)	A
74F534	Inverting Octal D Flip-Flop (3-State)	A
74F537	1-of-10 Decoder, 3-State	1H 86
74F538	1-of-8 Decoder, 3-State	1H 86

DEVICE	DESCRIPTION	AVAILA-BILITY
74F539	Dual 1-of-4 Decoder, 3-State	1H 86
74F540	Octal Inverting Buffer, 3-State	A
74F541	Octal Buffer, 3-State	A
74F543	Octal Transparent Bidirectional Latch	1H 86
74F544	Octal Transparent Bidirectional Latch	1H 86
74F545	Octal Bus Transceiver (3-State)	A
74F547	Octal Decoder/DeMUX w/Address Latches and Acknowledge	1H 86
74F548	Octal Decoder/DeMUX w/Acknowledge	1H 86
74F563	Octal D Latch, 3-State	1H 86
74F564	Octal D Flip-Flop, 3-State	1H 86
74F568	4-Bit Binary Up/Down Counter (3-State)	1H 86
74F569	4-Bit Decade Up/Down Counter (3-State)	1H 86
74F573	Octal D Latch, 3-State	1H 86
74F574	Octal D Flip-Flop, 3-State	1H 86
74F579	8-Bit Up/Down Counter, Common I/O (3-State)	A
74F588	GPIB Compatible Octal Transceiver	A
74F595	8-Bit Shift Register with Output Latch	1H 86
74F597	8-Bit Shift Register with Input Latch	1H 86
74F598	8-Bit Shift Register with Input Latch	1H 86
74F604	Dual 8-Bit Latch (3-State)	A
74F605	Dual 8-Bit Latch (OC)	A
74F620	Octal Bus Transceiver (3-State)	A
74F621	Octal Bus Transceiver (3-State)	A
74F622	Octal Bus Transceiver (OC)	A
74F623	Octal Bus Transceiver (3-State)	A
74F630	Memory Error Detector/Corrector (3-State)	2H 86
74F631	Memory Error Detector/Corrector (OC)	2H 86
74F640	Octal Bus Transceiver, Inverting, (3-State)	A
74F641	Octal Bus Transceiver, OC	A
74F642	Octal Bus Transceiver, Inverting, OC	A
74F646	Octal Bus Transceiver and Register (3-State)	1H 86
74F647	Octal Bus Transceiver and Register (OC)	1H 86
74F648	Octal Bus Transceiver and Register (3-State)	1H 86
74F649	Octal Bus Transceiver and Register (OC)	1H 86
74F651	Octal Bus Transceiver and Register, Inverting, 3-State	2H 86
74F652	Octal Bus Transceiver and Register, Non-Inverting, 3-State	2H 86

Availability Guide

DEVICE	DESCRIPTION	AVAILABILITY
74F653	Octal Bus Transceiver and Register, Inverting, OC	2H 86
74F654	Octal Bus Transceiver and Register, Non-Inverting, OC	2H 86
74F655A	Octal Inverting Buffer with Parity Generator-Checker (3-State)	A
74F656A	Octal Buffer with Parity Generator-Checker (3-State)	A
74F657	Octal Bus Transceiver with Parity Generator-Checker (3-State)	A
74F673	16-Bit Serial-In/Parallel-Out Shift Register (3-State)	1H 86
74F674	16-Bit Parallel-In/Serial-Out Shift Register (3-State)	1H 86
74F675	16-Bit Serial-In/Parallel-Out Shift Register with SO Capability	1H 86
74F676	16-Bit Parallel-In/Serial-Out Shift Register with SO Capability	1H 86
74F764	Dual Port RAM Controller with Latch	2H 86
74F765	Dual Port RAM Controller without Latch	2H 86
74F779	8-Bit Counter (3-State)	A
74F784	8-Bit Serial/Parallel Multiplier (with Adder/Subtractor)	2H 86
74F821	10-Bit Register, Non-Inverting	2H 86
74F822	10-Bit Register, Inverting	2H 86
74F823	9-Bit Register, Non-Inverting	2H 86
74F824	9-Bit Register, Inverting	2H 86
74F825	8-Bit Register, Non-Inverting	2H 86
74F826	8-Bit Register, Inverting	2H 86
74F827	10-Bit Buffer, Non-Inverting	2H 86

DEVICE	DESCRIPTION	AVAILABILITY
74F828	10-Bit Buffer, Inverting	2H 86
74F841	10-Bit Latch, Non-Inverting	2H 86
74F842	10-Bit Latch, Inverting	2H 86
74F843	9-Bit Latch, Non-Inverting	2H 86
74F844	9-Bit Latch, Inverting	2H 86
74F845	8-Bit Latch, Non-Inverting	2H 86
74F846	8-Bit Latch, Inverting	2H 86
74F861	10-Bit Transceiver, Non-Inverting	2H 86
74F862	10-Bit Transceiver, Inverting	2H 86
74F881	Arithmetic Logic Unit/Function Generator	1H 86
74F882	32-Bit Lookahead Carry Generator	1H 86
74F1240	Octal Buffer, 3-State	A
74F1241	Octal Buffer, 3-State	A
74F1242	Quad Transceiver, Inverting, 3-State	A
74F1243	Quad Transceiver, 3-State	A
74F1244	Octal Buffer, 3-State	A
74F1245	Octal Bus Transceiver, 3-State	1H 86
74F3037	Quad 2-Input 30Ω Transmission Line Driver	A
74F3038	Quad 2-Input Driver, Non-Inverting, OC	A
74F3040	Dual 4-Input 30Ω Transmission Line Driver	A
74F30240	Octal Driver, Inverting, OC	1H 86
74F30244	Octal Driver, Non-Inverting, OC	1H 86
74F30245	Octal Transceiver, Non-Inverting, OC	1H 86
74F30640	Octal Transceiver, Inverting, OC	1H 86

FAST ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F — N	
Plastic SO[1]	N74F — D	
Ceramic DIP		S54F — F
Ceramic LLCC[2]		S54F — G

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. LLCC is ceramic surface-mounted leadless chip carrier.

Signetics

Function Selection Guide

Logic Products

GATES

FUNCTION	DEVICE NUMBER
Inverters	
Hex Inverter	74F04
Hex Inverter Schmitt Trigger	74F14
NAND	
Quad 2-Input	74F00
Triple 3-Input	74F10
Dual 4-Input, Schmitt Trigger	74F13
Dual 4-Input	74F20
8-Input	74F30
Quad 2-Input, Schmitt Trigger	74F132
AND	
Quad 2-Input	74F08
Triple 3-Input	74F11
NOR	
Quad 2-Input	74F02
Triple 3-Input	74F27
Dual 5-Input	74F260
OR	
Quad 2-Input	74F32
Exclusive-OR	
Quad	74F86
Combination Gates	
Dual 2-Wide, 2-Input AND-OR-Invert	74F51
4-2-3-2 Input AND-OR-Invert	74F64

DUAL FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	CLEAR
D	74F74	↑	LOW	LOW
JK	74F109	↑	LOW	LOW
JK	74F112	↓	LOW	LOW
JK	74F113	↓	LOW	
JK	74F114	↓	LOW	LOW

MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NUMBER	RESET LEVEL	CLOCK EDGE	OUTPUT
Quad D	74F175	LOW	↑	True Comp
Quad D with Enable	74F379		↑	True Comp
Hex D	74F174	LOW	↑	True
Hex D with Enable	74F378		↑	True
Octal D	74F273	LOW	↑	True
Octal D, 3-State	74F374		↑	True
Octal D, 3-State	74F534		↑	Comp
Octal D with Enable	74F377		↑	True
Octal D, 3-State	74F564		↑	Comp
Octal D, 3-State	74F574		↑	True

Function Selection Guide

OTHER REGISTERS, REGISTER FILES

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK
Quad 2 Port	74F298	4 × 2		2D (mux)	⌐
Quad 2 Port	74F398	4 × 2		2D (mux)	⌐
Quad 2 Port	74F399	4 × 2		2D (mux)	⌐
10-Bit, Non-Inverting	74F821	10		2D	⌐
10-Bit, Inverting	74F822	10		2D	⌐
9-Bit, Non-Inverting	74F823	9		2D	⌐
9-Bit, Inverting	74F824	9		2D	⌐
8-Bit, Non-Inverting	74F825	8		2D	⌐
8-Bit, Inverting	74F826	8		2D	⌐

LATCHES

FUNCTION	DEVICE NUMBER	COMMON CLEAR (LEVEL)	ENABLE INPUT (LEVEL)	OUTPUT
Dual 4-Bit Addressable	74F256	LOW	1(L)	True
Dual 4-Bit Addressable	74F259	LOW	1(H)	True
Dual 8-Bit	74F604			True
Dual 8-Bit	74F605			True
Octal, 3-State	74F373		1(H)	True
Octal Inverting, 3-State	74F533		1(H)	Comp
Octal Transparent, Bidirectional	74F543		4(L)	True
Octal Transparent, Bidirectional	74F544		4(L)	Comp
Octal Transparent, Inverting, 3-State	74F563		1(H)	Comp
Octal Transparent, 3-State	74F573		1(H)	True
Multi-Mode Buffered, 3-State	74F412	LOW	1(L), 2(H)	True
Multimode Buffered	74F432	LOW		Comp
10-Bit, Non-Inverting	74F841		1(H)	True
10-Bit, Inverting	74F842		1(H)	Comp
9-Bit, Non-Inverting	74F843	LOW	1(H)	True
9-Bit, Inverting	74F844	LOW	1(H)	Comp
8-Bit, Non-Inverting	74F845	LOW	1(H)	True
8-Bit, Inverting	74F846	LOW	1(H)	Comp

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ENABLE INPUT (LEVEL)	SELECT INPUTS	OUTPUT
Quad 2-Input	74F157	1(L)	1	True
Quad 2-Input	74F158	1(L)	1	True
Quad 2-Input, 3-State	74F257		1	True
Quad 2-Input, 3-State	74F258		1	Comp
Dual 4-Input	74F153	2(L)	2	True Comp
Dual 4-Input	74F352	2	2	Comp
Dual 4-Input, 3-State	74F253		2	True
Dual 4-Input, 3-State	74F353	2	2	Comp
8-Input	74F151	1(L)	3	True Comp
8-Input, 3-State	74F251		1	True Comp

DECODER/DEMULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE LEVEL	OUTPUT LEVEL
Dual 1-of-4	74F139	2 + 2	1(L) + 1(L)	4(L) + 4(L)
Dual 1-of-4	74F539	2 + 2	1(L) + 1(L)	4(H) + 4(H)
1-of-8	74F138	3	2(L), 1(H)	8(L)
1-of-8	74F538	3	2(L), 2(H)	8(H)
1-of-10	74F537	4	1(L), 1(H)	10(H)
Octal, with Address Latches and Acknowledge	74F547	3	1(L), 2(H)	8(L)
Octal with Acknowledge	74F548	3	2(L), 2(H)	8(L)

Function Selection Guide

BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad 2-Input NAND Buffer	74F37	Comp
Quad 2-Input NAND Buffer, OC	74F38	Comp
Dual 4-Input NAND Buffer	74F40	Comp
Quad 2-Input NAND Transmission Line Driver	74F3037	Comp
Quad 2-Input Transmission Line Driver	74F3038	True
Dual 4-Input NAND Transmission Line Driver	74F3040	Comp
Octal Transmission Line Driver	74F30240	Comp
Octal Transmission Line Driver	74F30244	True
Octal Transmission Line Driver	74F30245	True
Octal Transmission Line Driver	74F30640	Comp
Octal Transceiver	74F621	True
Octal Transceiver	74F623	True
Octal Transceiver	74F641	True
Octal Transceiver	74F642	Comp
Octal Transceiver and Registers	74F647	True
Octal Transceiver and Registers	74F649	Comp
Octal Transceiver and Registers	74F653	Comp
Octal Transceiver and Registers	74F654	True

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK
Serial-In/Parallel-Out	74F164	8	D_{sa}, D_{sb}		⎍
Serial-In/Parallel-Out Output Latch, 3-State	74F595	8	D_s		⎍
Serial-In/Serial-Out/Parallel-Out, 3-State	74F673	16	SI/O		⎏
Serial-In/Serial-Out/Parallel-Out	74F675	16	D		⎍⎏
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F195	4	J,K	4D	⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F598	8	D_{s0}, D_{s1}	8 I/O	⎍
Serial-In/Parallel-In/Serial-Out	74F674	16	SI/O	SI/O, 16D	⎏
Serial-In/Parallel-In/Serial-Out	74F676	16	SI	16D	⎍
Serial-In/Parallel-In/Parallel-Out Shift Right, 3-State	74F395	4	D_s	4D	⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F322	8	D_0, D_1	8 I/O	⎍
Serial-In/Parallel-In/Parallel-Out	74F194	4	D_{sr}, D_{sl}	4D	⎍
Serial-In/Parallel-In/Parallel-Out, Bidirectional	74F198	8	D_{sr}, D_{sl}	8D	⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F299	8	D_{s0}, D_{s7}	8 I/O	⎍
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F323	8	D_{s0}, D_{s7}	8 I/O	⎍
Parallel-In/Serial-Out Input Latch	74F597	8	D_s	8D	⎍
Parallel-In/Parallel-Out, 3-State	74F350	4	$I_{-3} - I_{+3}$	4Y	
Parallel-In/Parallel-Out, 3-State	74F604	16		$A_1 - A_8$, $B_1 - B_8$	⎍
Parallel-In/Parallel-Out, OC	74F605	16		$A_1 - A_8$, $B_1 - B_8$	⎍
Parallel-In/Parallel-Out, True and Complement Output	74F398	8	S	$I_{0a} - I_{0d}$, $I_{1a} - I_{1d}$	⎍
Parallel-In/Parallel-Out	74F399	8	S	$I_{0a} - I_{0d}$, $I_{1a} - I_{1d}$	⎍

Function Selection Guide

COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PARALLEL ENTRY	PRESETTABLE	CLOCK EDGE
Synchronous	74F160A	10	S	X	⌐
Synchronous	74F161A	16	S	X	⌐
Synchronous	74F162A	10	S	X	⌐
Synchronous	74F163A	16	S	X	⌐
Up/Down	74F168	10	S	X	⌐
Up/Down	74F169	16	S	X	⌐
Up/Down	74F190	10	A	X	⌐
Up/Down	74F191	16	A	X	⌐
Up/Down	74F192	10	A	X	⌐
Up/Down	74F193	16	A	X	⌐
Up/Down	74F269	8	S	X	⌐
Up/Down, 3-State	74F568	10	S	X	⌐
Up/Down, 3-State	74F569	16	S	X	⌐
Up/Down	74F579	8	S (I/O)	X	⌐
Up/Down, 3-State Multiplexed	74F779	8	S (I/O)	X	⌐

THREE-STATE BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Buffer	74F125	True
Quad Buffer	74F126	True
Quad Bus Transceiver	74F242	Comp
Quad Bus Transceiver	74F243	True
Quad Bus Transceiver	74F1242	Comp
Quad Bus Transceiver	74F1243	True
Hex Buffer	74F365	True
Hex Inverter	74F366	Comp
Hex Buffer, 4-Bit and 2-Bit	74F367	True
Hex Inverter, 4-Bit and 2-Bit	74F368	Comp
Octal Buffer	74F240	Comp
Octal Buffer	74F241	True
Octal Buffer	74F244	True
Octal Buffer	74F1240	Comp
Octal Buffer	74F1241	True
Octal Buffer	74F1244	True
Octal Buffer with Parity	74F455	Comp
Octal Buffer with Parity	74F456	True
Octal Buffer with Parity	74F655A	Comp
Octal Buffer with Parity	74F656A	True
Octal Driver	74F540	Comp
Octal Driver	74F541	True
Octal Transceiver	74F245	True
Octal Transceiver	74F545	True
Octal Transceiver with IEEE-488 Termination Resistors	74F588	True
Octal Transceiver	74F620	Comp
Octal Transceiver	74F622	Comp
Octal Transceiver	74F640	Comp
Octal Transceiver	74F651	Comp
Octal Transceiver	74F652	True
Octal Transceiver with Parity	74F657	True
Octal Transceiver/Register	74F646	True
Octal Transceiver/Register	74F648	Comp
Octal Transceiver	74F1245	True
10-Bit Buffer	74F827	True
10-Bit Buffer	74F828	Comp
10-Bit Transceiver	74F861	True
10-Bit Transceiver	74F862	Comp

Function Selection Guide

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	INPUT ENABLE (LEVEL)	INPUT/OUTPUT (LEVEL)
8-to-3	74F148	LOW	Active-LOW

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit ALU	74F181
4-Bit ALU	74F381
4-Bit ALU with Overflow Output for Two's Complement	74F382
ALU/Function Generator	74F881
4-Bit Binary Full Adder with Ripple Carry	74F83
4-Bit Binary Full Adder with FAST Carry	74F283
Lookahead Carry Generator	74F182
Lookahead Carry Generator	74F882
Quad Serial Adder/Subtractor	74F385

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Comparator	74F85
8-Bit Comparator	74F521
8-Bit Register Comparator	74F524

PARITY

FUNCTION	DEVICE NUMBER
9-Bit Odd/Even Parity Generator/Checker	74F280A

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
16-Bit Error Detection	74F630
16-Bit Error Detection/Correction Circuit	74F631
64-Bit RAM	74F189
8-Bit Serial Multiplier with Adder/Subtractor	74F784
Dual Port RAM Controller with Refresh	74F764
Dual Port RAM Controller without Latch	74F765
8-Bit Serial/Parallel Two's Complement Multiplier	74F384
2-Bit Serial/Parallel (with Adder/Subtractor)	74F784

Signetics

Logic Products

Section 2
Quality And Reliability

SIGNETICS LOGIC PRODUCTS QUALITY

Signetics has put together a winning process for manufacturing Logic Products. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The products produced in the Standard Products Division must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 A/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to ensure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from −55°C to +125°C and at +10% supply voltage.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 – QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of Logic products, samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: T_J = 150°C, 1000 hours, static biased or dynamic operation, as appropriate (worst case bias configuration is chosen)
- High Temperature Storage: T_J = 150°C, 1000 hours
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static biased
- Temperature Cycling (Air-to-Air): −65°C to +150°C, 1000 cycles

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15psig, 121°C, 100% saturated steam) and 300 cycles of thermal shock (−65°C to +150°C)

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Quality And Reliability

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the corporate SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, *lower cost of ownership.*

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals, inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues. For example, in 1978 a program to reduce electrically defective units for a major automotive manufacturer improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100PPM (parts per million), down from an industry practice of 10,000PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, from a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality (see Figure 1).

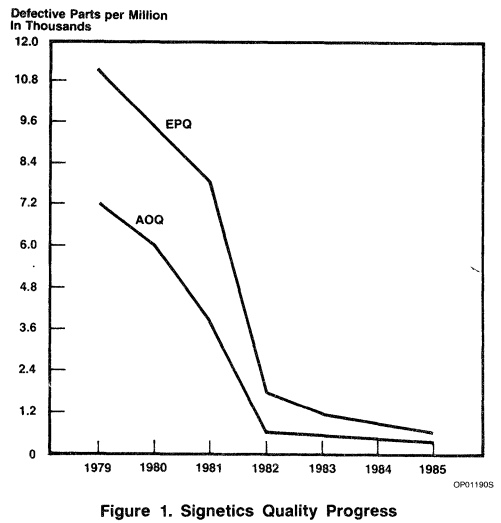


Figure 1. Signetics Quality Progress

Quality And Reliability

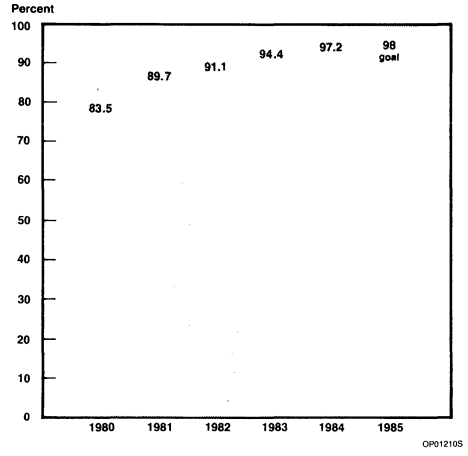


Figure 3. Lot Acceptance Rate from Signetics Vendors

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed upon price (see Figure 2).

ONGOING QUALITY PROGRAM

The quality improvement program at Signetics is based on "Do it Right the First Time". The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by all technical and administrative functions equally.

This program extends into every area of the company, and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" – ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent.

Quality And Reliability

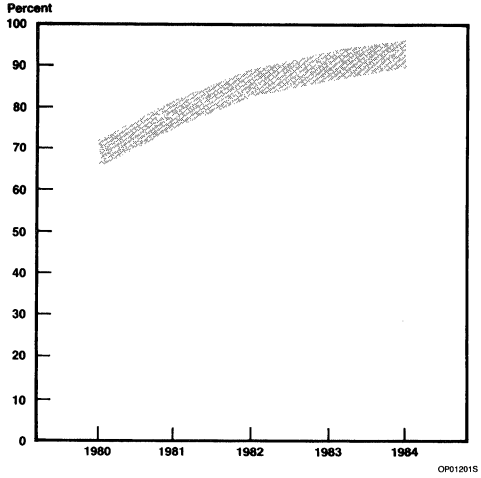


Figure 2. Performance to Schedule On-Time Delivery

Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

MATERIAL WAIVERS

1985 – 0
1984 – 0
1983 – 0
1982 – 2
1981 – 134

Higher incoming quality material ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities – failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers. Or, write on your letter-head directly to the corporate director of quality at the corporate address shown at the back of this manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

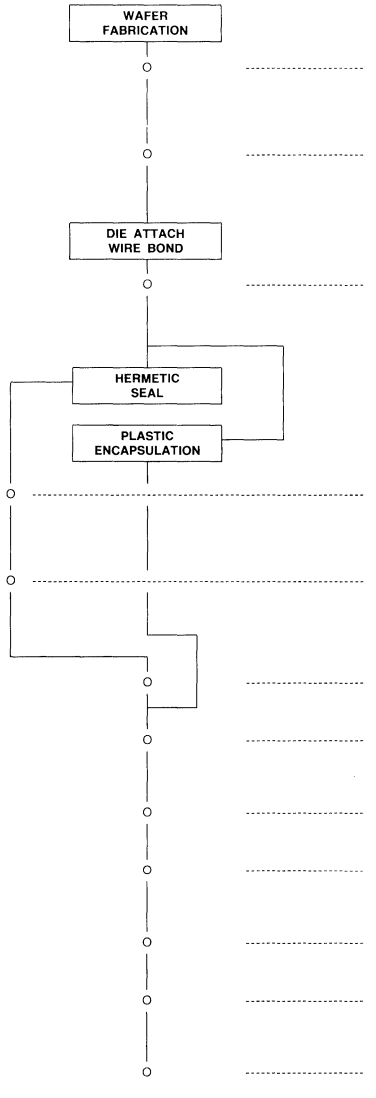
This team work with you will allow us to achieve our mutual goal of improved product quality.

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the quality improvement program. During the development of the program many profound changes were made. Figure 4, *Logic Products Generic Process Flow*, shows the result. Key changes included such things as implementing 100% temperature testing on all products as well as upgrading test handlers to insure 100% positive binning. Some of the other changes and additions were to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading Quality supplier of Logic products. These achievements have also led to our participation in several Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

Quality And Reliability



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

STABILIZATION BAKE PRECONDITIONING

Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance. Hermetic devices are baked to ensure the elimination of any remaining cavity moisture.

TEMPERATURE CYCLING

Using MIL-STD-883 Method 1010.1 Condition C devices are cycled from cold to hot temperatures imposing a very severe stress which weakens loose bonds and package seals without degrading good devices. A loosened bond is later detected during 100% electrical tests.

SEAL TESTS

Hermetic package seal integrity is ensured by 100% gross leak testing.

100% ELECTRICAL TEST

Every device is tested for functional and AC/DC parameters at high temperature with guard bands to assure performance to data sheet limits.

BURN IN (SUPR II LEVEL B OPTION)

Devices are burned in for 21 hours at 155°C maximum junction temperature.

SYMBOL

Devices are marked with the Signetics logo, device number and date code or custom symbol per individual specification requirements.

VISUAL

All products are 100% visually inspected per the requirements specified in Signetics or customer documents.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested for functional and AC/DC parameters at 25°C with guard bands to assure performance to data sheet limits.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step guarantees that the specified mechanical and electrical AQL's have been met. Every shipment is sealed and identified by QA personnel.

NOTE: The items on this flowchart do not all happen in the same sequence for all products.

Figure 4. Logic Products Generic Process Flow

Quality And Reliability

As time goes on the drive for a product line that has Zero Defects will grow in intensity. These efforts will provide both Signetics and our customers with the ability to achieve the mutual goal of improved product quality.

The Logic Products Quality Assurance department has monitored PPM progress, which can be seen in Figure 5. We are pleased with the progress that has been made, and expect to achieve even more impressive results as the procedures for accomplishing these tasks are fine tuned.

The real measure of any quality improvement program is the result that our customers see. The meaning of *Quality* is more than just working circuits. It means commitment to *On Time Delivery* at the *Right Place* of the *Right Quantity* of the *Right Product* at the *Agreed Upon Price.*

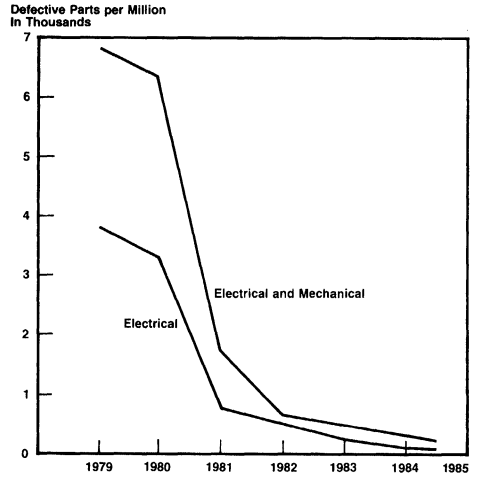


Figure 5. Logic Products AOQ (Average Outgoing Quality)

Signetics

Logic Products

Section 3
Circuit Characteristics

INPUT STRUCTURES

There are six types of input structures that are commonly employed in TTL families: diffusion diode, Schottky diode, multiple emitter, Schottky-diode cluster, PNP, and NPN. Each of these is discussed below. Some of them are not used in FAST circuits for reasons which are discussed.

The diffusion diode input is most often used with FAST circuits. The input diode is labeled as D1 in Figure 1. There can be more than one of them if NAND logic is to be performed. In the oxide-isolated processes these are base collector diffusions. Each input pin also has a Schottky clamp diode D2. This diode is standard for most TTL circuits, and is included to limit negative input voltage excursions that are generally the result of inductive undershoot.

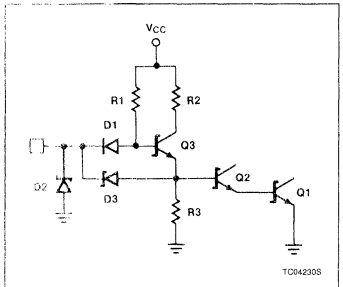


Figure 1. Diode Input

The static diode input function of voltage versus current is shown in Figure 2. If the pin voltage is negative, most of the relatively high negative current flows through the clamp Schottky D2. At 0V the current flows from V_{CC} through R1 and D1 to the pin. Switching from a logic LOW level to a logic HIGH level occurs when the input pin voltage rises high enough to force the current from the D1 path to the Q4 - Q2 - Q1 path. This happens when the base voltage of transistor Q3 is at three base-emitter drops ($3V_{BE}$), and the pin is at $2V_{BE}$, which is the standard FAST threshold switching voltage. At this voltage the input current is very small, just the leakage currents of diodes D1, D3 and clamp diode D2. The current remains at this small, positive value until breakdown voltage is reached.

Transistor Q3 and resistor R2 provide a current gain by increasing the amount of current available to Q2 and Q1 when the pin voltage is high. R3 bleeds current off the base of Q2 to pull it low when the pin voltage is low. D3 speeds up this process during the HIGH-to-LOW pin transition. When the switching transients are over, D3 is reverse biased.

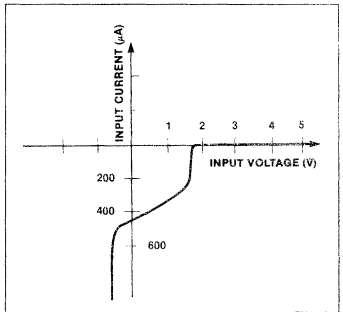


Figure 2. Static Diode Input Function Of Voltage VS Current

The current of Figure 2 is scaled for the case where the pin is required to pull down a single 10KΩ resistor R1 (20μA maximum in the HIGH state and 0.6mA maximum in the LOW state), which is defined as a standard FAST Unit Load (UL). For some parts, pin current can exceed a UL, especially in the logic LOW state. This will happen if the pin must sink the current from more than one R1 resistor, or if the value of R1 is less than 10KΩ, which will be the case if the capacitance at the base of the transistor Q3 is too large for the required switching speed. In this event, the actual number of ULs is listed for each input in the specification sheet for the part. Note that a UL as defined here is less than the normally defined Schottky TTL Unit Load; the correlation is one Schottky Unit Load = 1.67 ULs. This is an important point to remember for fan-in and fan-out calculations in systems that mix FAST with other TTL families.

The Schottky diode input is shown in Figure 3. Its function is much the same as the diffusion diode input, except that the switching threshold voltage is lower by the Schottky diode forward drop, about 500mV. Because a higher threshold voltage is usually advantageous from a noise-margin standpoint in high-speed systems, the Schottky diode input is not normally used with FAST.

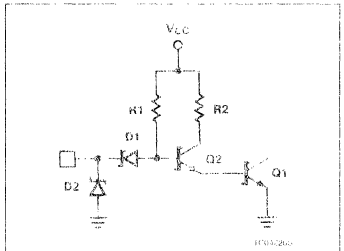


Figure 3. Schottky Diode Input

The multiple-emitter input is shown in Figure 4. Its function is also much the same as the diffusion diode input, but with the base-emitter junction used instead of the base-collector junction. In some respects this is a better choice for high-speed logic, but it has one serious limitation which is the emitter-base breakdown voltage that may be as low as 5V. This low breakdown allows a high input current to flow through the Q2 - Q1 base emitter path which cannot be limited to an acceptable value with a series resistor.

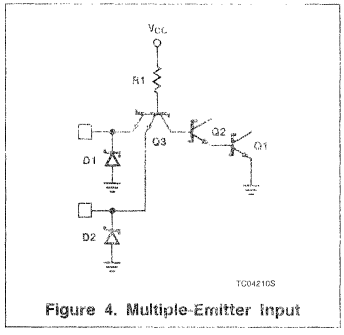


Figure 4. Multiple-Emitter Input

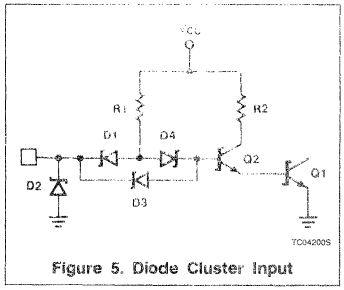


Figure 5. Diode Cluster Input

Circuit Characteristics

The diode cluster input (Figure 5) looks like a multiple-emitter input, except that its breakdown voltage is higher because separate Schottky junctions are used instead of a transistor. It has limited use in FAST circuits.

The PNP input (Figure 6) in various forms has found wide acceptance in low power Schottky logic because it provides a high-impedance input which is desirable in some applications. It has not been used in FAST circuits because the early oxide isolated processes do not provide a fully suitable PNP device. This is not the case now, particularly with new processes aimed at relatively large chips, which may use the PNP input for those applications where input current must be very low for input voltages that may exceed V_{CC}. The PNP transistor Q3 is fabricated with the P-type substrate as the grounded collector, the N-type Epi as the base, and the P-type normal base diffusion as the emitter. The process must be tailored to provide a suitable current gain for this vertical structure and must have provision to remove the considerable substrate current without an appreciable rise in substrate voltage. Q3 functions as an emitter follower for pin voltages low enough to provide an emitter-base forward bias. This occurs at an emitter voltage below the $3V_{BE}$ value provided by the D3 – Q2 – Q1 stack, and gives the desired $2V_{BE}$ pin threshold. At pin voltages above this value, Q3 turns off and the current through R1 is directed to Q2 – Q1 through D3. The Schottky diode D2 speeds up the HIGH to LOW transition if the pin voltage falls more rapidly than the base of Q2; otherwise, D2 is off. In comparison with the NPN input, the PNP input has: 1) lower input current above V_{CC} 2) higher input current above threshold, 3) a slower switching speed, and 4) a larger pin transition current. The first trait may be advantageous in some applications. The last three traits are generally not advantageous.

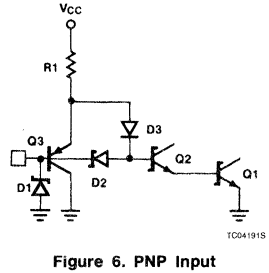


Figure 6. PNP Input

The NPN input is shown with two variations in Figures 7a and 7b. It has limited use in standard TTL circuits, and is used in selected FAST devices, especially where its superior high-impedance input characteristics are useful. A typical plot of static input current versus input voltage is shown in Figure 8. There are some significant differences between this function and that of the diffusion diode input shown in Figure 2, the most important being the much lower input current in the region from 0V to threshold, and the controlled increase of input current above V_{CC}. In Figure 7a Ref 2 is set to $2V_{BE}$ plus one Schottky drop.

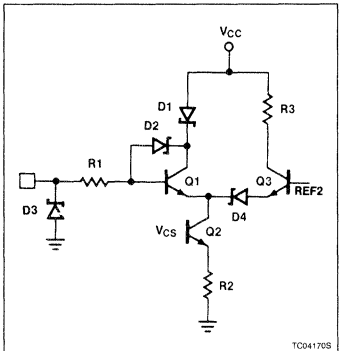


Figure 7a. NPN Input

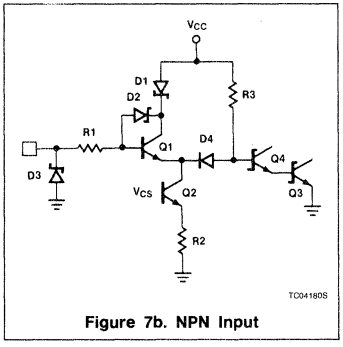


Figure 7b. NPN Input

When the pin voltage is negative, the large negative clamp current is supplied through the clamp Schottky diode D3. For positive voltages, from 0V to the switching threshold of $2V_{BE}$, Q1 is off, and the input current I_{IL} is very small, just the leakage current of Q1, D2, and D3 with low reverse bias. As the input voltage rises above $2V_{BE}$, Q1 turns on and the current that had been flowing through D4 now flows through Q1, and blocking Schottky diode D1 to V_{CC}. The value of this current is determined by the current source transistor Q2 with its base connected to voltage reference V_{CS}, and by the size of the emitter resistor R2. The current is nearly constant within the normal operating range of input voltages, and has a typical value of 0.1mA to 1.0mA. The pin must supply only a small fraction of this bias current, the ratio of Q1 collector current to base current being the bipolar β factor. Typically, I_{IH} base input current is less than 20μA in the voltage range from 0V to V_{CC}. This value is the specification for a standard FAST NPN Unit Load. As in the diode input case, if larger currents are needed to reduce delay times or to provide for multiple-input transistors connected to the same pin, the specification sheet for the particular device will identify the input pins which have NPN ULs larger than one, and will list their values.

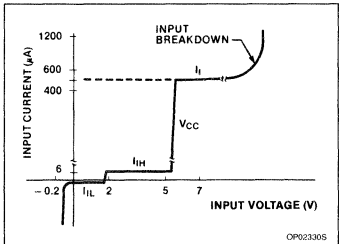


Figure 8. NPN Input Characteristics (Not To Scale)

In normal operation, the pin voltage will be limited in the negative direction by the diode clamp D3, and will be less than V_{CC} in the positive direction. The actual input voltage may exceed V_{CC} for three reasons: there may be inductive overshoot in badly terminated systems; the V_{CC} pin may be floating or grounded; or the input pin may be forced high by electrostatic discharge or incoming inspection testing.

For the inductive overshoot case, when the pin voltage exceeds V_{CC}, part of the Q1 collector current begins to flow from the pin through limiting resistor R1 and Schottky diode D2. The current from V_{CC} through D1 decreases by exactly this amount, since Q2 is a constant current source. As the voltage continues to rise, D1 becomes reverse biased and prevents high currents flowing from the pin into V_{CC}. All the Q2 current flows into the pin through the R1 – D2 – Q1 – Q2 – R2 path to ground. As stated before, this current is typically small, in the range of 0.1mA to 1.0mA, and nearly independent of pin voltage, as shown by the I_I plateau in Figure 8. I_I provides a clamping action to ground for pin voltages in excess of V_{CC}, and this is usually desirable to reduce overshoot.

For the case where V_{CC} is grounded or floating, the input current is nearly zero for positive voltages between zero and approximately 7V. The conducting path through R1 – D2 – Q1 is available, but the current source Q2 will be shut off because, without V_{CC} drive, the Q2 base reference V_{CS} will be at 0V. This is a standard set up for incoming

Circuit Characteristics

inspection. For the incoming inspection testing case where V_{CC} is connected to a 5V source the response is shown in Figure 8. The current remains on the Q2-limited plateau until the pin voltage is high enough to cause non-destructive collector-emitter reach-through of Q2. At this point, input current increases as the pin voltage rises, and R1 functions to limit this current and prevent damage to Q2.

The electrostatic discharge case is similar to the incoming inspection case except that Q2 may be off if the V_{CC} pad is floating, in which case it breaks down at a slightly higher voltage. The NPN input produces reach-through at a relatively low voltage compared with the diode input. The effect of this non-destructive reach-through is to greatly increase the ability of the device to survive electrostatic discharge. The discharge current is passed through the chip at a relatively low power dissipation, and this is shared by elements R1, D2, Q1, Q2 and R2, so that none of them dissipate enough power to do damage. By way of contrast, with a diode input, the clamp Schottky diode breaks down at high voltage with high dissipation in a localized area, and may suffer damage.

Another advantage of the NPN input is its ability to interface on the chip to either a conventional TTL interior design, or to the increasingly popular current-mode interior logic. The conventional TTL interface is shown in Figure 7b. In this case the Q2 current source is designed to provide sufficient current to insure that in the LOW state, with current flowing through the R3 – D4 – Q2 path, the base-emitter stack of Q3 – Q4 is shut off. The $2V_{BE}$ input threshold is set by the forward drops of Q1, D4, Q4 and Q3.

The current-mode logic interface is shown in Figure 7a. The output voltage is the drop across R3, and is referenced to V_{CC} (or some on-chip regulated voltage lower than V_{CC}) as is required for current-mode logic. For this case, voltage reference REF2 is normally fixed at $2V_{BE}$ + 1 Schottky drop to provide a pin threshold voltage of $2V_{BE}$. In fact, REF2 can be tailored to set the switching threshold voltage to any desirable level; it can be set to something other than an integral number of base emitter drops, or it can be designed to reduce the sometimes undesirable temperature variations of input threshold.

INPUT CONSIDERATIONS

Input Resistance

Many standard TTL devices, and the majority of FAST devices available to date, have diode or equivalent input structures with static current functions similar to those shown in Figure 2. At voltages above switching threshold the input junctions are reverse-biased and sink very little current, typically less than a microampere. At voltages below threshold, the inputs supply current to a positive source, and TTL designs accomodate this with a driver that sinks current when its output is positive but low. The maximum current the diode-type input supplies in the LOW state occurs at maximum V_{CC} with a minimum pull-up resistor value (all resistor values can vary due to process inconsistencies). This maximum input current is specified to be less than 600μA for the majority of FAST devices if the input voltage (V_{IN}) is 0.5V. If a driver cannot sink the necessary current for a particular number of loads, the system designer must either add a buffer circuit designed to drive with higher current, or switch to loads that have high impedance NPN inputs. These are available on many Signetics FAST designs, and are specified to have input current less than 20μA over the full switching range from 0V to V_{CC}. Typical input current for the NPN structure at room temperature is less than 1μA below switching threshold voltage, and 3μA above threshold.

Input Capacitance

Input capacitance, measured using a small-signal variation about a static DC operating point, is usually least for the NPN, next lowest for the diode, and highest for the PNP. When one includes the added capacitance of the elements common to each input, such as the pin, pad, bond wire, and clamp Schottky-diode, the percentage difference for total static input capacitance for any of the three types of inputs is not very large.

Dynamic Input Current

In many applications the total current an input pin draws during a switching transition is a more important consideration than its input capacitance. This dynamic input current is often larger than the value of static capacitance would predict because each of the three types of input structure normally includes some sort of speed-up mechanism, usually a "kicker" Schottky diode, connected to an internal node of the circuit. The kickers deliver current, related in a non-linear way to input edge-rates. High dynamic input current does not always equate to fast circuit switching. NPN inputs are usually faster than diode or PNP inputs, but in general have the lowest total dynamic current, followed by the diode input, and then the PNP which is highest. The percentage differences for dynamic current tend to be larger than the respective differences for static capacitance.

Switching Threshold Voltage

The FAST input switching threshold voltage is set quite high for TTL at two base-emitter junction forward-bias drops. FAST input structures have enough gain that the voltage range in which they switch from one state to the other, as shown by a static DC transfer function curve, is completed within about 100mV of the $2V_{BE}$ threshold. For a typical part at room temperature, V_{BE} is about 800mV, and the switching threshold is nominally at 1.6V; the static transfer range uncertainty of about 100mV gives a nominal threshold for solid LOWs and HIGHs of about 1.55V and 1.65V respectively. The FAST threshold voltage was chosen higher than other TTL families to give a larger noise margin with respect to ground, and to be more nearly centered in the region where a FAST output driver stage switches with maximum edge rates, which occurs between about 0.6V and 2.6V.

Because the FAST threshold is set by the base-emitter junction voltage, it is dependent on junction temperature and current density. V_{BE} increases by about 1.2mV for each degree C drop in junction temperature; current density changes by about a decade for a 60mV change in V_{BE}. The total variation due to processing differences, temperature, and current density is about 150mV per junction, or 300mV total change in input threshold to give limits of 1.25V LOW and 1.95V HIGH. The FAST V_{IL} and V_{IH} limits are 0.8V and 2.0V respectively ... a tight spec for V_{IH}.

HYSTERESIS CONSIDERATIONS

The following discussion of hysteresis, DC noise margin, and AC noise immunity in high-speed TTL circuits is reprinted with the permission of Fairchild Camera and Instrument Corporation.

The inclusion of hysteresis circuitry into a logic design has two basic aims: improved DC noise margin and improved AC noise immunity. This is accomplished through the use of negative feedback which changes the input threshold of a device depending on its output state. Figure 9 shows an octal buffer design. Hysteresis is provided by circuitry Q2, Q3, Q4 and associated resistors and diodes. The output state is sensed by the voltage on the collector of Q7. The positive input threshold is established by

$$V_{t+} = V_{BE}(Q10) + V(R7) + V_{BE}(Q5) + V_{BE}(Q1) - V(D2)$$

and the negative input threshold is established by

$$V_{t-} = V_{BE}(Q10) + V(R7) + V_{BE}(Q5) + V_{SAT}(Q2) - V(D2)$$

From this we can see that the input hysteresis is:

$$\Delta IR(R7) + V_{BE}(Q1) - V_{SAT}(Q2)$$

These voltages are, of course, temperature dependent and do not track well. Propagation delay from input to output is typically 3.0ns at 25°C but the propagation delay from input to threshold change is 6.0ns due to the low drive

Circuit Characteristics

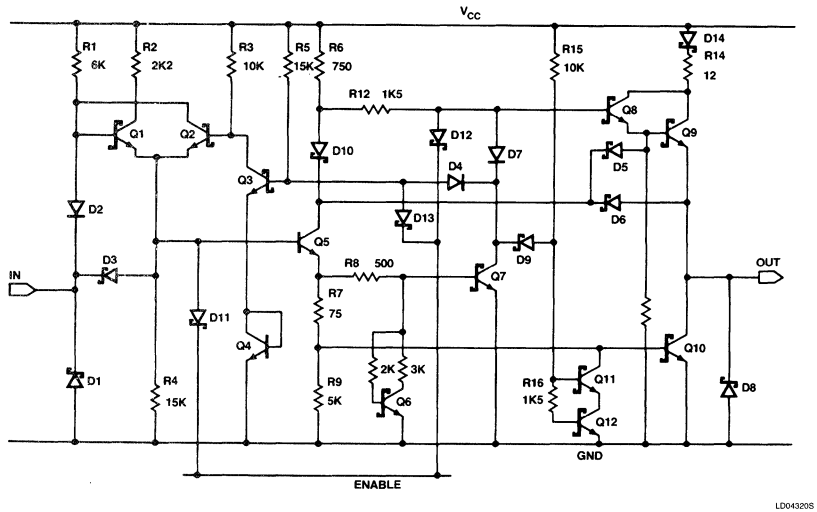


Figure 9. Enable

current levels of the hysteresis circuitry. The effects of this we will see later.

The inclusion of hysteresis circuitry does improve the typical DC noise margin of FAST somewhat. Due to test difficulties, the hysteresis threshold voltages are not specified so the guaranteed DC noise margins are no better than standard FAST inputs. In considering the benefits of improved DC noise margin it is worthwhile to compare various TTL families. As Table demonstrates, the DC noise immunity of a standard FAST gate exceeds that of an LS gate with hysteresis.

Table 1

	'LS00	'LS240	'S00	'F00	
Typical Gate Input Threshold	1.0	1.5	1.3	1.6	Volts
Typical DC Noise Margin*	0.7	1.2	1.0	1.3	Volts

*Logic LOW noise Margin, Typical V_{OL} = 0.3V

Before covering the effects of hysteresis on AC noise immunity, it is important to cover the topic of ground/V_{CC} bounce since it plays an important role in the AC behavior of a logic gate. Ground bounce is a phenomenon where the internal ground of a device differs from that external to the device. It is proportional to output switching edge rate, output load and package inductance. As technology improves propagation delays decrease. For reduced propagation delay to be effective on voltage switched technology (TTL structures) then edge rates must increase. Thus for a given package and load, faster edge rates generate more ground/V_{CC} deviation.

To quantify the situation, take a loaded bus-line driven from part way along the bus. The driver will see two stub lines in parallel which for this example has an effective impedance of 30Ω. A FAST output will switch from 3.4V to 0.4V, a swing of 3.0V, in 2.5 to 3ns. This will result in an output current of 100mA for the duration of the edge transition. All this current must flow in the ground lead of the package. A 20-pin plastic package has a ground/V_{CC} pin inductance of 10nH (a ceramic package ground/V_{CC} inductance is 24nH). The ground pin of the chip will deviate from the external ground by:

$V = Ldl/dt$

For this example L = 10nH, dl = 100mA, and dt = 3ns. So V = 300mV. This voltage will move the chip ground as shown in Figure 10.

The effects of hysteresis and ground bounce on AC noise immunity are best explained through a series of voltage waveforms. Figure 11 shows ideal input and output waveforms. If all signals in a system environment were this clean, there would be little need for hysteresis circuitry. Figure 12 shows an input waveform

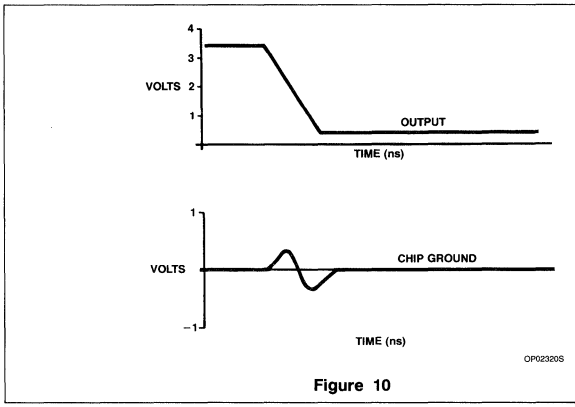


Figure 10

Circuit Characteristics

with a kink in the threshold region caused by a poorly terminated line, and/or poor decoupling at the driver. The double crossing of the input threshold has caused a glitch in the output waveform. Ideally, the incorporation of hysteresis circuitry in a receiver would improve AC noise immunity and prevent the glitched output by changing the input threshold as soon as the output begins to switch. However, Figure 13 shows that the change in input threshold occurs after the output begins to switch.

We now need to consider the effects of ground/V_{CC} bounce. Figure 14 shows the effect of a single output switching on internal threshold and output waveform. Comparing Figures 13 and 14 we see that output waveform distortion is worse. This effect increases with multiple output switching until a limiting factor is reached. This limiting factor is caused by reduction of effective V_{CC} to the chip, giving reduced output drive capability and reduced edge rates. The effective chip V_{CC} self limits at approximately 2.6V. The edge rate to 1.5V can be predicted by the formula

$\Delta t = \Delta IL\ 1/V$

where I = total of all output source and sink currents plus 5mA per output switching,
L = ground or V_{CC} inductance and
V = voltage drop from nominal (i.e. 5 – 2.6 = 2.4V)

There is yet another complexity in the interaction of ground bounce and hysteresis circuitry. It is possible that under the right set of conditions the output waveform can actually oscillate as a result of the internal feedback mechanisms and package inductances. With multiple outputs switching ground bounce can be sufficiently severe that a non-switching input can have its threshold, as referenced to the external ground, cross a high or low input condition and cause its output to glitch. Figure 15 shows this effect when seven of the eight inputs receive the input shown in the upper trace. The center trace shows the output to be expected at the seven switching outputs; the bottom trace shows the effective input threshold against high and low levels. As can be seen, this crosses both high and low input levels and under these circumstances this output would most likely glitch.

Conclusions

DC noise margins for standard FAST input structures equal that of older TTL technologies which incorporate hysteresis circuitry. Further, increasing AC noise margin is inconsistent with other goals in a high-speed TTL family. It is therefore necessary to prevent input waveform distortion in threshold regions through proper circuit design in high performance bus environments.

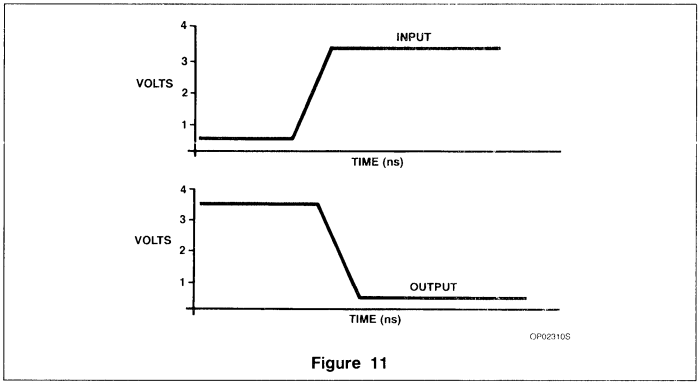


Figure 11

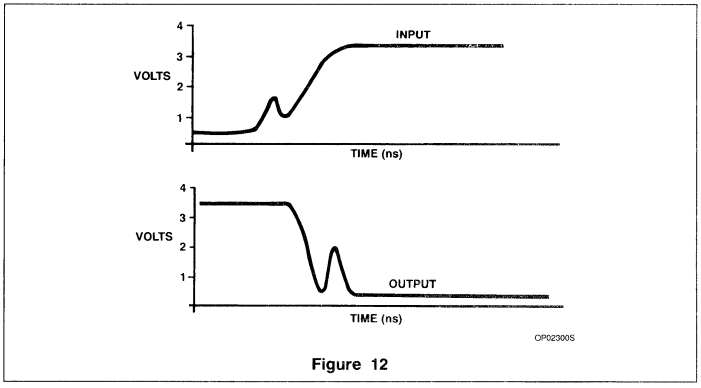


Figure 12

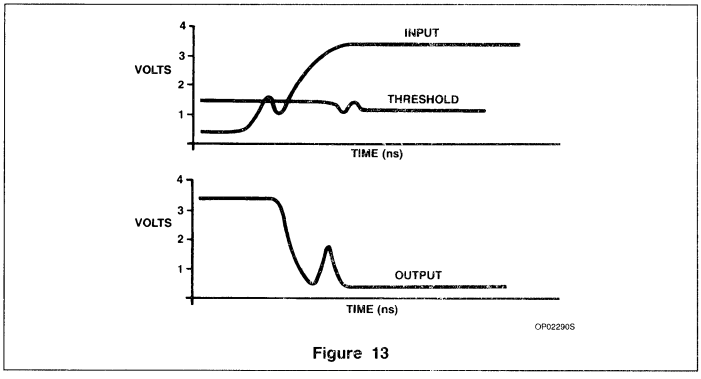


Figure 13

The incorporation of hysteresis circuitry into high performance TTL logic provides few user benefits and can actually create more system problems that it solves. The added circuitry consumes power, slows down logic delays and increases input loading. Input hysteresis is also very difficult to test on high-speed automatic production test equipment, thus adding to product cost.

Because of these disadvantages, Signetics has designed hysteresis only into devices which are specifically designated as Schmitt Triggers. These parts are the 74F13, 74F14,

Circuit Characteristics

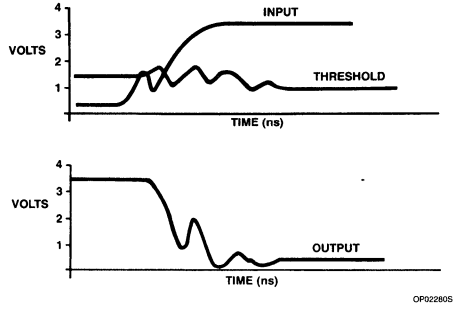


Figure 14

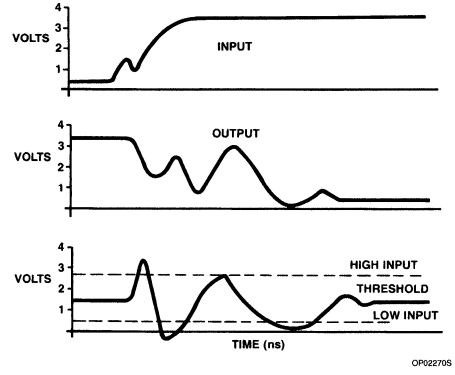


Figure 15

and 74F132. All other part types have eliminated hysteresis as a design feature.

ELECTRO-STATIC DISCHARGE (ESD) CONSIDERATIONS

It is universally true that no bipolar integrated circuit process can provide devices with such high breakdown voltages that they are able to simply stand off ESD without some structure punching through or breaking down. The necessary condition for survival when this occurs is that the energy dissipation in any volume of the chip must be kept low enough that neither the silicon nor the interconnecting metal can melt. This can be accomplished in two ways: the breakdown voltage should be as low as practical, consistent with normal circuit operation, and the energy should be dissipated in as large a volume as is possible. Circuit components that are particularly sensitive to charge damage must be protected by structures that are less fragile. All Signetics FAST parts are designed with these requirements in mind, and although, as a rule of thumb, a sophisticated oxide isolated process used to fabricate these parts tends to be more ESD damage-prone than a junction isolated process, FAST is about as rugged as other TTL families in general. If FAST parts are handled with the same care afforded any other high-technology parts, they will not be damaged.

ESD sources usually fit into one of two categories: people or other objects, that have accumulated static charge may touch the parts; or they generate their own charge, as is the case when a circuit makes sliding contact with an insulator. In the first instance, static voltages tend to be high, over 1000V, and discharge is usually limited by relatively high series resistance. In the second case, voltages are lower, around 200V, but there is very little series resistance to limit discharge current. Both possibilities are simulated with discharge models that are used in the majority of the test set-ups, and parts are designed in a way to improve survival for both ESD conditions.

Experience has shown that inputs of TTL circuits are much more likely to suffer ESD damage than outputs. Since negative voltages are discharged through clamp ground diodes with low chip dissipation, only voltages positive with respect to substrate ground are apt to produce input damage.

Circuits with diode inputs have a positive voltage breakdown in the relatively high range of from 15V to 25V. Schottky diodes connected to an input pin usually break down before junction diodes, and if they are stressed beyond their limits the Schottky diodes usually sustain damage in the corners. A diffusion guard-ring around the diode increases the uniformity of the breakdown, and as a result maximizes the dissipation volume at breakdown and increases the ability of the device to survive ESD. All Signetics FAST circuits have guard-rings on Schottky diodes that connect to input pins.

NPN inputs are designed to have low holdoff voltage for positive voltages in excess of V_{CC}. Under static discharge the input structure forward biases, and the current-source transistor conducts the ESD current to substrate with a relatively low collector-emitter reach-through voltage. The input current for normal operation is low enough that a series limiting resistor can be added; this limits ESD current, especially for the case where the ESD source has no appreciable series resistance itself.

An additional input structure is available for environments where high positive voltages can occur even after a circuit is connected to a PC board. Designed specifically to limit overshoot in transmission line systems, these inputs have a hard clamp to ground at a voltage slightly above V_{CC} Max. Because this clamping action occurs at low voltage, and because the clamp is designed to handle high current, the ESD sensitivity is minimal; the input is as rugged as a standard TTL output.

FLOATING INPUTS

FAST inputs should not be allowed to float. All unused inputs, even those on unused gates, should be tied to a voltage source of relatively low impedance that will get them out of the logic picture and out of trouble. For a LOW input this can be ground, or the output of a permanently low driver. For a HIGH input this can be V_{CC}, protected by a series resistor if circuit damaging voltage spikes are possible in the system, or a permanently high driver.

Properly tied HIGH or LOW, inputs will not pick up enough spurious noise to cause problems. If they are allowed to float, the results can be disastrous. Floating diode inputs usually pull to within a few Mv of $3V_{BE}$

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above ground ... a V_{BE} above threshold. The input voltage will fall about 1V per 0.1mA of current that is capacitively coupled from an adjacent LOW-going pin. Since pin-to-pin input capacitance is in the order of one pF for an IC in a PC environment, an adjacent pin falling at 1.0V/ns couples in about 1.0mA of current, enough to switch the input to a LOW state for as long as the current lasts. The normal FAST circuit response will be to switch, or oscillate. The problem is even worse for high impedance low capacitance NPN or PNP inputs. In this case the static voltage to which they float is determined in part by leakage, and is not predictable.

To reiterate, FAST inputs must not be allowed to float. To do so is to invite serious system problems.

OUTPUT STAGES

The purpose of the output stage is to supply current to a load to force it to a HIGH state or to sink current from the load to force it to a LOW state. The speed at which the load can be switched from one state to the other depends on how much supply current or sink current is available from the output driver. There must be an amount in excess of that which is required to maintain the static load voltage, and it is the excess current that is available to charge or discharge the load capacitance. Most FAST circuits are designed to fit into one of two categories, based on output drive capability; the normal output stage, and the buffer driver which can supply approximately twice as much current.

Both normal drivers and buffers may be 3-State, which means that, in addition to LOW and HIGH states, they can be forced to a high-impedance OFF state as a third possible choice. This allows multiple components to be connected to a bus simultaneously, with only the single-selected device providing actual drive capability.

The basic components of an output stage are shown in Figure 16.

The pull-down driver components sink load currents to force a LOW state at the output pin; the pull-up driver components supply current to force a HIGH state. The control components turn on the selected driver and turn off the nonselected driver in response to the logic input signal. For 3-State parts, the control components turn off both drivers if the 3-State control signal is active. The output Schottky clamp is included to suppress inductive undershoots, and is a part of every FAST circuit. The load requires a static current to keep it in either a logic HIGH or LOW state. The drivers must also charge and discharge the load capacitance C_L, which is generally one of the major factors that influence switching speed.

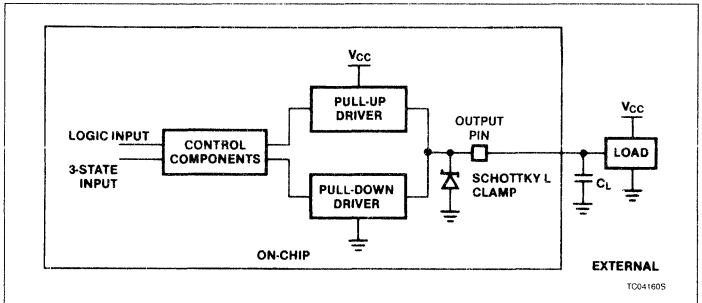

Figure 16. Output Stage Basic Components

Since, to a large extent, they function independently of each other, the pull-up driver, pull-down driver, and control blocks are discussed independently.

PULL-UP DRIVERS

Open Collector

The simplest pull-up driver consists of no more than a fixed pull-up resistor tied to V_{CC}. For this case, the control stage interacts only with the pull-down driver. In the LOW state, this must sink the current from both the pull-up resistor and load. In the HIGH state, the pull-up resistor must supply all of the load current. Most often, the pull-up resistor is not physically part of the integrated circuit chip itself, but is added externally. In this case the only circuit element connected to the output pad (in addition to the ever-present Schottky clamp) is the collector of the pull-down driver transistor, hence the name "open-collector." Parts with this output stage can be tied together for bus applications.

If any of the connected pull-down stages is active, it will pull the bus LOW; only if all of them are off can the external resistor pull the bus HIGH. This action provides a "wired" logical function that is free in the sense that no additional components are required to achieve it. Some open-collector FAST parts also have 3-State inputs that serve to disable output pull-down stages regardless of the action of the normal logic function.

The open-collector output voltage depends on the load, the value of the pull-up resistor, and the voltage to which this is connected. If the resistor value is low, the output will rise to nearly the full value of the pull-up source voltage; in particular, the open-collector output can rise to V_{CC}, a voltage higher than that obtainable with a standard Darlington totem-pole pull-up.

High-drive open-collector parts are ideal as drivers for terminated transmission lines. In this application the line is terminated at the receiving end with a resistor network that provides the proper impedance and an equivalent source voltage of about 3V. The circuit pull-down drive sinks the termination current through the line at relatively low chip power dissipation when it is on. When it is turned off, the line pulls the output high, charging the stray capacitance from an impedance equal to the line characteristic impedance. Since the current is supplied by the line, the chip power dissipation falls. Very fast rise times approaching 1ns can be obtained with this scheme. Rise times, in general, for open-collector outputs are determined by the RC product of the pull-up resistor and the stray capacitance, and are limited only by the ability of the chip to pull the load low.

The list of available Signetics parts designed for low impedance terminated driver applications includes the 74F3037, 74F3038, and 74F3040 which are all available in 20 pin packages with center power pins and multiple V_{CC} and Ground pins to reduce inductance related ground noise to an acceptable level. Octal and open collector options are in design and will be available in 1986 in 24 pin Slim DIP packages.

Standard Darlington

Most FAST pull-up drivers use dual transistors, connected as shown in Figure 17a, with the emitter of the first device Q_b delivering current to the base of the driver Q_a. This configuration is called a Darlington circuit and provides a composite current gain nearly as large as the product of the current gains of Q_b and Q_a.

The major advantage of the Darlington pull up, as compared to the open collector, is that the pin is actively pulled high by the emitter-follower action of Q_a which is capable of supplying large currents to quickly charge output capacitance. Despite the large output current that is available, the drive requirements of Q_b are low, so that the voltage drop

Circuit Characteristics

across R_c is small, and the pad will pull up to a voltage nearly as high as $V_{CC} - 2V_{BE}$.

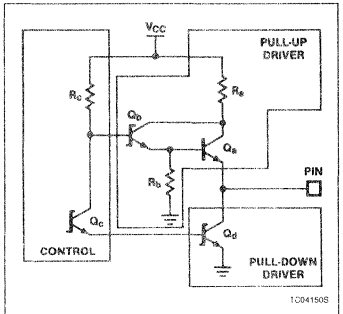

Figure 17a. Basic Darlington Pull-Up

For the case where the pin voltage is high, the phase-splitter transistor Q_c is off, and the base of Q_b is pulled high by resistor R_c. The current which flows through R_c is just sufficient to provide base drive to Q_b. The base voltage of Q_b will be just slightly below V_{CC}, and the output pin voltage will be less than this by the sum of the V_{BE} drops of Q_b and Q_a, both of which are on. Most of the base current for Q_a and the current through pull-down resistor R_b is supplied from V_{CC} through R_a and Q_b. Q_b has a Schottky clamp to prevent saturation when the current through R_a is large. Resistor R_a limits the amount of current flowing from V_{CC} through Q_a to a value small enough that Q_a will not be damaged if the output pin is accidentally grounded for a short period of time. This short circuit output current is called I_{OS}, and its value is approximately the maximum current available to charge the output capacitance at the beginning of a LOW-to-HIGH transition. The minimum current available when the pin has reached the minimum guaranteed high voltage V_{OH} is called output high current (I_{OH}), and is specified to be either 1mA or 3mA, depending on the type of driver. The maximum output voltage that the pull-up driver can achieve occurs at maximum V_{CC}, and at high temperatures with corresponding low values of transistor V_{BE} and high current gain. Conversely, the minimum high voltage occurs at low V_{CC} and low temperatures.

In the LOW state, the pull-down driver Q_d is on and the pin voltage is the Q_d saturation voltage V_{SAT}. Q_c is on and its collector resistor R_c is pulled down to $V_{BE} + V_{SAT}$; the V_{BE} of Q_d, V_{SAT} of Q_c. Q_b is also on, with its emitter at V_{SAT}, and the current through R_b is low. The base-emitter voltage of Q_a is nearly zero and Q_a is off.

The rate at which the pull-up driver can force a LOW-to-HIGH transition depends on a number of factors. The first, and obvious, consideration is that the control components must turn off the pull-down driver very quickly. During the short time that both pull-up and pull-down are on, there is a large feed-through current spike that is wasted as far as switching the load is concerned; it also increases chip power dissipation and produces undesirable voltage spikes in V_{CC} and ground. Assuming the pull-down is off, the LOW-to-HIGH transition speed is governed by: 1) the rate at which R_c can pull-up the base of Q_b; 2) the amount of pin current required to drive the load and charge the load capacitance; 3) the value of R_a; 4) the physical size and current gain of Q_a; and 5) the amount of Q_a base drive current that is lost through R_b to ground. The amount of R_b drive current lost can be reduced by connecting R_b to the output pin instead of ground, and this is done in a number of FAST parts. For this case, the static current through R_b with the pin high is less than if R_b is grounded, but switching feed-through current spike for a HIGH-to-LOW transition may be increased because R_b cannot effectively pull-down the base of Q_a until after the pin voltage falls.

The pin can be driven above its maximum high value by an external pull-up or by positive reflections from a transmission line. When this happens, Q_a and Q_b do not have sufficient base-emitter drive to keep them on. If the pin voltage rises significantly above V_{CC}, Q_a will begin to leak current into V_{CC}. For the case where R_b is tied to the pin instead of ground, the reverse transistor action of Q_a allows a high pin-to-V_{CC} current. This is not usually a problem in normal operation, but should be avoided in system applications where the V_{CC} pin may be intentionally grounded.

3-State

For all 3-State FAST parts, the leakage paths to a grounded V_{CC} pin are blocked with Schottky diodes. A typical 3-State pull-up is shown in Figure 17b. S_a is the series Schottky blocking diode. 3-State Schottkys S_{t1} and S_{t2} serve to simultaneously turn off the pull-up and pull-down drivers. The 3-State control is active when it is pulled low to within V_{SAT} of ground. In this state it sinks all the available drive current for Q_b and Q_c, and pulls their bases down to ($V_{SAT} + V_{Schottky}$), which is essentially one V_{BE}. The voltage drop across R_c is large and 3-State power dissipation is typically high. Q_a and Q_b are off for normal TTL voltage ranges of the output pin; a negative undershoot large enough to drive the pin about one V_{BE} below ground will allow them to turn on and supply current from V_{CC}; this action aids the clamping Schottky diode in preventing the pin voltage from falling lower.

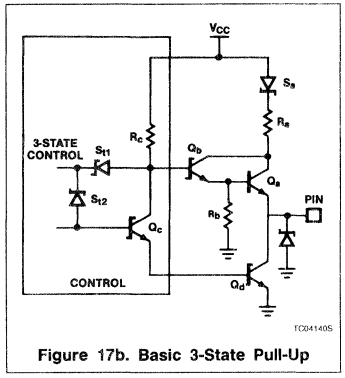

Figure 17b. Basic 3-State Pull-Up

PULL-DOWN DRIVERS

The basic FAST pull-down is shown in Figure 18. Q_d is the pull-down driver transistor, a big Schottky-clamped device capable of sinking large currents. C_d is the stray base-collector capacitance of Q_d and its unavoidable presence has an important effect on the performance of the pull-down driver. Q_c is the Schottky-clamped phase splitter. It functions as a current-limited, low-impedance driver for Q_d when the logic input voltage V_{IN} is high, and as an inverting driver for pull-up Q_b by virtue of the current through R_c when V_{IN} is low and Q_C is off. Z_d is the pull-down impedance network which insures that Q_d is off when V_{IN} is low.

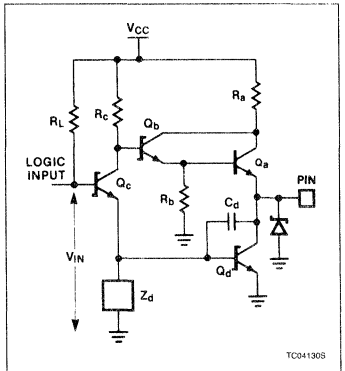

Figure 18. Basic FAST Pull-Down

Switching to the logic LOW state occurs when V_{IN} is larger than the V_{BE} drops of Q_c plus Q_d, both of which are on. Part of the total emitter current available from Q_c comes from R_c, which has a voltage drop of $V_{CC} - V_{BE} - V_{SAT}$. The remainder of the Q_c emitter current is supplied through its base Schottky clamp or by other components not shown in Figure 18 but discussed in the section on

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control components. A portion of the total Q_c emitter current is lost in the pull-down network Z_d; the remainder is available as base current for pull-down driver Q_d. The amount of current Q_d can sink depends on its base drive, its current gain, and its collector voltage. This current is specified on a per-part basis in the data sheets at output low voltage (V_{OL}) of 0.5V. The current which Q_d can sink in the switching range with the pin voltage at 2.5V is called available current (I_{AVL}), and is usually at least 70mA for FAST. The manner in which this current varies as the pin voltage decreases from 2.5V to V_{OL} is not specified as a FAST family parameter, since it is critically dependent on circuit design for a particular part, but is included as a specification for selected parts, especially those tailored to drive transmission lines. Several innovative circuit improvements that increase I_{AVL} by increasing the drive current for Q_d are shown in Figures 19a and 19b. Speed-up Schottky diodes S_{s1} and S_{s2} have been added to the standard pull-down circuit as shown in Figure 19a. Both are reverse-biased and off in the HIGH state, since R_c pulls the collector of Q_c nearly to V_{CC}. Both connect the collector of Q_c to nodes that need to be discharged during a HIGH-to-LOW transition, S_{s1} to the base of Q_a, S_{s2} to the pin. They will conduct if these node voltages are higher than $V_{BE} + V_{SAT} + V_{Schottky}$, or approximately $2V_{BE}$; they are quite effective above $2V_{BE}$. Other networks are available which function down to lower voltages; these are especially useful for transmission line drivers. Figure 19b shows a dynamic kicker that gives an impulse of current which is especially useful in discharging high capacitive loads.

The network of elements labeled Z_d in Figure 18 is the pull-down impedance which insures that Q_d is off when the value of V_{IN} falls below $2V_{BE}$. When the voltage at the base of Q_d is being pulled high by Q_c or low by Z_d, the output pin voltage responds by moving in the opposite direction. This produces a change in voltage across C_d, which is the sum of the base voltage change and the collector voltage change, so the amount of charge required by C_d is magnified by a factor which is larger than unity.

This well-known Miller-effect causes the apparent value of C_d, as perceived by the drivers, to be a factor of about five times larger than the already large physical junction capacitance, all of which means that the drivers Q_c and Z_d need to supply or sink much more current during an output transition than is necessary to maintain static conditions. When static conditions do exist internally in the circuit, noise voltage spikes on the output pin, V_{CC}, or ground can momentarily force the base of Q_d in the direction to produce a serious output glitch, and the drivers must respond quickly to counter this coupled noise.

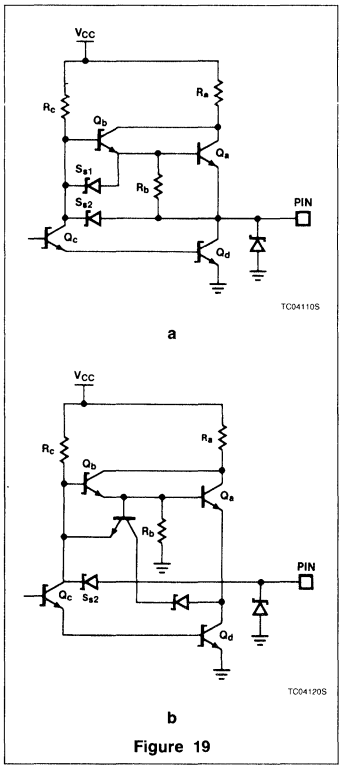

Figure 19

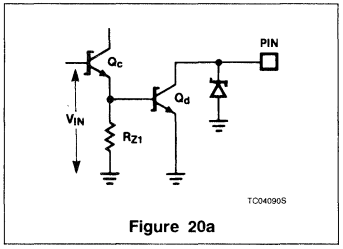

Figure 20a

The simplest Z_d element is a resistor R_{Z1} tied to ground, as shown in Figure 20a. It will pull the base of Q_d all the way down to 0V if V_{IN} is less than one V_{BE}. This provides good immunity to coupled noise, but slows down the HIGH-to-LOW pad transition somewhat because the base of Q_d must rise a full V_{BE} before the output can begin to change. The value of R_{Z1} needs to be relatively large to prevent a serious loss of base drive current when Q_d is on, which makes it easier to capacitively couple voltage spikes to the base of Q_d and, in part, nullifies the good noise immunity the full V_{BE} swing provides.

The addition of a series Schottky diode solves most of the problems. This is shown in Figure 20b. The Q_d base voltage cannot pull below a Schottky drop, so the switching speed is unimpaired. The value of R_{Z2} can be less than R_{Z1} for the same current when the base is high, so the effect of coupled charge is less and the noise margin is acceptable.

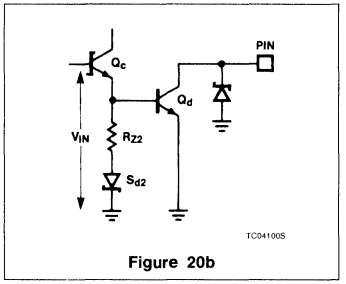

Figure 20b

The circuit of Figure 20c is standard with many TTL families. It pulls the base of Q_d down even less than does $R_{Z2} - S_{d2}$, but it has a relatively high dynamic impedance and is somewhat noise sensitive. It has the advantage that it tends to "square up" the input voltage-to-output voltage transfer function, hence its popular name "squaring circuit." It is frequently used in simple gates where the shape of the transfer function may be important. For more complicated circuits, where there are one or more stages of logic with gain between input and output pins, the squaring ability is pretty much lost; in fact, it is likely that high-gain, multiple-logic-level FAST circuits will oscillate if the input voltage is held at near threshold for any length of time.

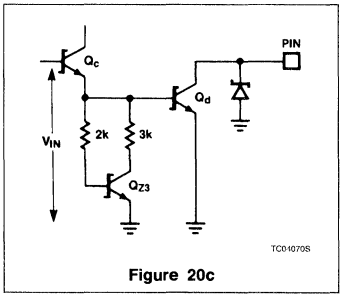

Figure 20c

Figure 20d shows a popular dynamic circuit that is used in conjunction with a resistor or squaring circuit pull-down, and which insures that C_d cannot couple enough charge to the base of Q_d to slow down a LOW-to-HIGH transition. In operation, as the emitter of Q_d rises, charge is coupled through C_{Z4} into the base of Q_{Z4} which turns on and shunts the

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Miller current flowing through C_d to ground. When the transition is finished, the current through C_{Z4} stops and Q_{Z4} turns off. When the HIGH-to-LOW transition of Q_b occurs, C_{Z4} discharges through S_{d4}. Because Q_{Z4} reduces the problems associated with Miller current, the circuit is called a "Miller Killer."

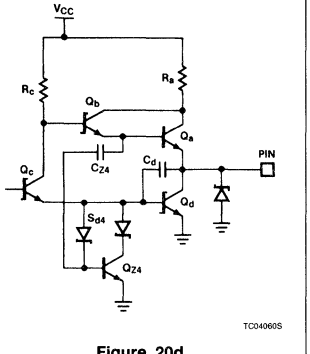


Figure 20d

Figure 20e shows an active pull-down for the base of Q_d. The drive for Q_{Z5} (not shown) must be generated from the same signal that drives the base of Q_c. When Q_c is on, Q_{Z5} must be off and when Q_c is off, Q_{Z5} turns on to hold the base of Q_d low. The impedance is very low, eliminating the capacitive-coupling noise problem.

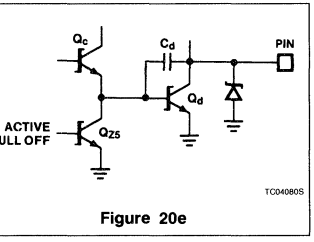


Figure 20e

CONTROL COMPONENTS

This section covers the following topics: 3-State control drivers and special 3-State problems; V_{CC} turn-on current and 3-State glitches during power-up; and noise margin and ground voltage as relates to inputs.

3-State Control Drivers

The normal TTL 3-State scheme is shown in Figure 17b. The 3-State control voltage in the OFF state is high enough that S_{t1} and S_{t2} are reverse-biased; in the active state the control voltage is low, usually V_{sat}, so that the $Q_a - Q_b$ base emitter stack is off, as is the $Q_c - Q_d$ stack. In the 3-State mode, R_c is dissipating maximum power. Blocking Schottky diode S_a prevents current from flowing backwards through Q_a if the V_{CC} pin is grounded; the output pin high voltage can be about 4.5V before there is any significant 3-State leakage current. The only exception to this general rule with FAST is for the diode input transceiver function, where the same pin acts as an input or an output. In this case, the pin supplies one or more normal FAST unit loads of current if it is LOW, and tends to pull to $2V_{BE}$ if it is floating. NPN input transceivers have normal low 3-State leakage.

There are several innovative improvements to the basic 3-State circuit, as shown in Figure 21. The addition of inverter $Q_{c2} - R_{c2}$ with a blocking Schottky S_{c2} allows the addition of feedback diodes S_{s1} and S_{s2} to increase I_{AVL}; S_{c2} cannot be included in series with R_{c1} because its forward voltage drop would lower V_{OH}. 3-State power is not increased, since only one R_{c1} is pulled low. The current through Q_{c2} is available as added base drive to Q_d, so nothing is wasted. An additional transistor may be paralleled with Q_{c1} and Q_{c2} to control an active pull-down version of impedance Z_d which, discussed in a previous section, eliminates the Miller turn-on problem of Q_d.

I_{CC} Considerations

There is no formal family specification that limits the amount of V_{CC} current a FAST circuit may draw during turn-on as V_{CC} rises from zero to 4.5V. However, for most new designs, and especially for circuits that have high I_{CC} requirements, an effort has been made to limit maximum turn-on I_{CC} to 110% of I_{CCmax}. This precaution prevents an undesirable system situation where the V_{CC} power supply is large enough to drive the devices, but can't power them up. The major component of turn-on current is V_{CC} to ground feedthrough of output stages. Unless specific steps are taken to prevent it, the pull-up Darlington turns on if V_{CC} is greater than $2V_{BE}$, and remains on until the on-chip voltage is high enough to set the phase splitter solidly in one or the other of its two states. The solution is to incorporate extra circuit components that will set the phase splitter at voltages nearly as low as $2V_{BE}$, or turn off the top device with a separate 3-State type structure which activates at low V_{CC} voltages and becomes inoperative when V_{CC} is high.

The amount of current that can be fed from an output pin back into a grounded V_{CC} pin, or through the chip to ground for an open V_{CC} pin, depends on the design. Generally, 3-State feedback current is specifically limited to low values which are leakage or breakdown related. Other parts have medium to high current. Those with Darlington pull-downs connected to the output pin conduct the most.

Some 3-State parts, especially selected buffer functions, have additional circuit elements to insure that as they power on they source or sink no appreciable output current, provided that the 3-State control pins are in the active state as V_{CC} rises. This means that V_{CC} can be turned on or off at will in the system to conserve power, and bus voltages will not be affected. Parts with this capability are identified in the specific data sheets.

GROUND VOLTAGE AND OTHER NOISE PROBLEMS

Ground Voltage As A Serious Problem

Excessive ground noise voltage in a system usually produces serious degradation of

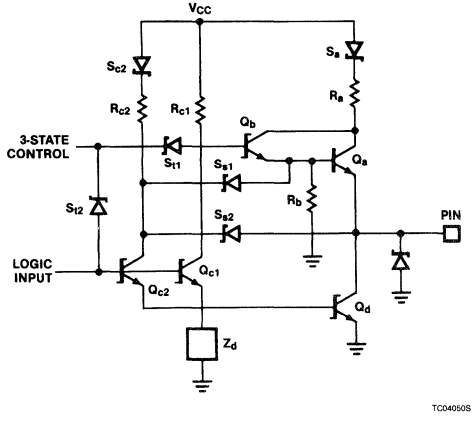


Figure 21. Improved 3-State Circuit

Circuit Characteristics

switching speed. It may also produce unwanted glitches on outputs, or spurious clocks which cause flip-flops to lose data, or relaxation oscillations that completely disrupt a system. It is, without doubt, one of the major causes of logic systems failure ... difficult to accommodate, and difficult to eliminate.

The problem is not unique with FAST, but is greatly aggravated by the high transition rates and large currents for which FAST is designed. Because of this, FAST can optimally replace other TTL families in systems that have been carefully designed at the PC board level. Well planned layout is vital, and multilayer boards with ground and V_{CC} planes are often necessary. Great care must be taken to insure adequate bypassing for V_{CC}. The problems are not trivial, but they can be solved satisfactorily to yield systems whose performance is not exceeded in the TTL world.

Sources Of Ground Noise

Ground lead inductance is the source of most ground noise voltage; it causes a voltage drop proportional to the rate at which the current through it changes.

Inductance is a measure of the amount of energy stored in the magnetic field associated with a current. Low values of inductance imply low energy, which means low voltage required to affect a change in current. As a general rule, inductance decreases as current is allowed to spread out in space, and current interactions decrease. The inductance of a thin wire far removed from the return current path is high; that of a large conductor coaxially encircled by the return path is low. Inductance tends to be proportional to the log of dimensions: a change of a factor of ten in spacing tends to change inductance by only a factor of two. From a logic system viewpoint, ground planes are better than ground traces; wide lines are better than narrow lines; close spacing to planes is good; loops that allow magnetic flux linkages are bad. Wire lengths of fractions of inches count, and sockets with long pins add significant inductance to a PC card.

Ground noise voltage is increased by feedthrough current spikes. These occur when both top and bottom devices of the output totem-pole driver are on simultaneously, and heavy currents are allowed to flow directly from V_{CC} to ground. They can be minimized in one of two ways: drive the devices such that one is turned off before the other can turn on, as is done in the new Signetics 30Ω drivers (74F3037, 74F3038, and 74F3040 are available now and octal versions are due in 1986); or, more commonly, drive them together, but very fast, so the feed-through current can flow for only a short time.

Although most ground noise results from ground inductance, resistance also contributes. Static ground offsets unrelated to rates of current change occur, and add to the total ground voltage. Generally speaking, those measures which reduce ground inductance also reduce ground resistance.

Estimating The Magnitude Of Ground Noise

The accurate modeling of ground noise-related problems in logic design is a complex procedure that requires numerical analysis to determine system currents and voltages as a function of time. This can only be accomplished in a satisfactory manner if one has reasonable electrical models, especially for input stages and output drivers of the integrated circuits used in the system. These data are available on request for many of the FAST logic functions. Signetics is prepared to assist customers in solving the sometimes formidable problems associated with large system simulation.

The following discussion derives the minimum peak-value of ground noise that will occur as an integrated circuit discharges a capacitor through ground lead inductance. It points out the minimum problems that will exist. In the real world, the peak ground voltage will always be larger than the simplest derivation predicts.

The load capacitor C and its discharge path are shown in Figure 22. The capacitor has been previously charged to a positive voltage, and is discharging through pull-down transistor Q_d and lead ground inductance L_g. As the current changes, it develops a ground voltage V_g across L_g that is equal to the product of L_g times the rate at which it changes.

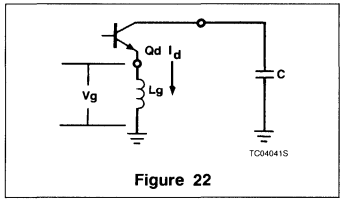


Figure 22

The discharge current I_d will vary with time; starting from zero, it will increase to a maximum value, and then eventually return to zero. There are an infinite number of ways I_d can vary, depending on how the transistor allows charge to flow at any instant in time, but each of the possible current-vs-time discharge curves must define the same area, equal in value to the total charge Q that is removed from the capacitor as its voltage falls by an amount V.

The voltage drop V_g across the inductor at any instant in time will be determined by the slope of the current-vs-time curve, that is, by the rate at which current is changing. The unique curve that has the required area and minimum slope is triangular, as shown in Figure 23. The ground voltage for this case is a square wave as shown in Figure 24. It will be positive while the current is increasing, and negative when the current is decreasing.

The equations of interest in estimating V_g are:

$$\text{Charge} = Q = CV = I_{MAX}\frac{T}{2}$$

$$\text{Ground voltage} = V_g = (\text{triangle slope})(L)$$

$$= \frac{2\ I_{MAX}\ L}{T}$$

Combining the two equations to eliminate I_{MAX} gives:

$$V_g = \frac{4CVL}{T^2}$$

This lower limit of peak ground voltage will always be exceeded in the real world, where ground voltages are usually spikes, not square waves. If a spike is large enough and long enough, the chip will erroneously recognize it as a valid input, and respond either by glitching, slowing down, clocking incorrectly, or oscillating.

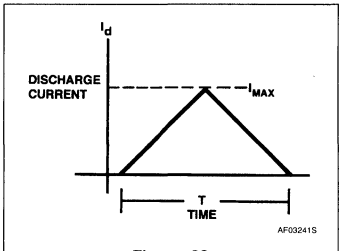


Figure 23

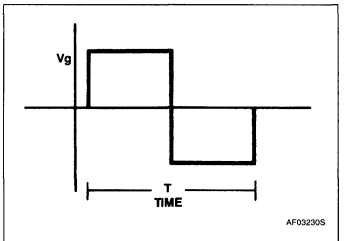


Figure 24

An example using values typical for a FAST circuit in a 16-pin DIP illustrates the potential for trouble. If the circuit discharges one standard FAST load of 50pF in 2ns with a voltage change of 3V through a ground inductance of 10nH, the minimum ground voltage will be:

$$V_g = \frac{4 \times 50 \times 10^{-12} \times 3 \times 10 \times 10^{-9}}{(2 \times 10^{-9})^2}$$

$$= 1.5V$$

Circuit Characteristics

This value is high, and suggests that if transition times are not to be seriously degraded, inductances must be kept as small as possible, and loads must be minimized.

Effects Of Ground Noise On Input Stages

FAST TTL input voltages are referenced to system ground as illustrated in Figure 25 which shows an equivalent input and output stage. The equivalent input circuit is represented by R_{IN} and the four diodes D1 through D4. These components establish an input switching threshold voltage of 2 V_{BE} relative to chip ground. The on-chip voltage V_{IN} must be different from this value by a margin large enough to guarantee a static LOW or HIGH with sufficient overdrive to insure switching speed. The on-chip voltage V_{IN} that is actually available is the difference between the input pin voltage V_{PIN} and the total ground voltage noise V_g. V_g is the sum of the steady state voltage due to ground current flowing through R_g, and the inductive voltage drop across L_g. The inductive voltage is usually the larger of the two, and since it depends on current changes, it will have both positive and negative polarities for each switching cycle. This means that either LOW or HIGH input voltages which are too close to switching threshold will allow the noise margin to be exceeded, and if the ground voltage noise persists long enough, the input will switch erroneously. The result of this depends on the chip function. Combinatorial logic usually slows down or produces output glitches. Latches and flip-flops may be clocked inadvertently, and stored data will be lost. Complex circuits that have multiple outputs may oscillate, particularly if one polarity of ground noise results in a rapid change of ground current that produces the opposite polarity ground noise.

Ground noise adds a dimension of difficulty in measuring input threshold voltage. FAST parts are guaranteed to have input thresholds between the limits 0.8V and 2.0V. A typical method of verifying this is to determine the voltage at which the input actually switches. This requires some care, since the true threshold voltage is masked by any noise voltage contributed by the test system or ground inductance. For accurate results, the input pin voltage should approach the switching threshold slowly and smoothly. At threshold the input will switch. Sensing this point is easy for those circuits where an output also switches, glitches, or oscillates. It is more difficult to determine for those circuits where an input change produces no output change, as is the case, for example, with flip-flops which change state only when clocked. The input switch point for these devices can be inferred by measuring the input current as a function of input voltage. Clocking the part may produce enough ground noise to distort the measurement, even if the output doesn't switch.

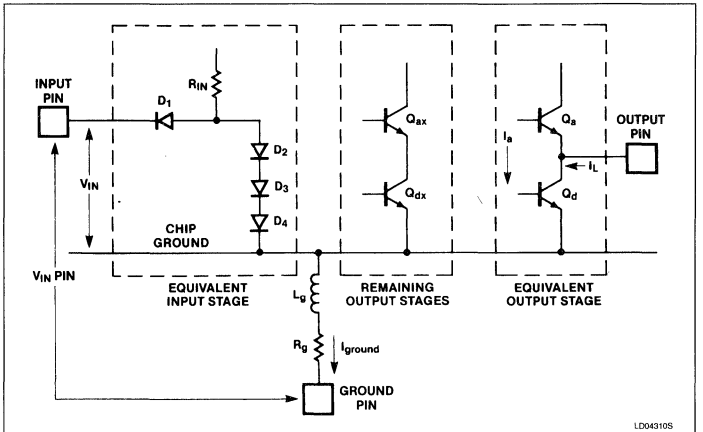


Figure 25. Equivalent Input And Output Stage

Effects Of Ground Noise On Output Stages

The most obvious effect that ground noise has on output stages is to directly change the voltage available to force discharge current through the pull-down device. If the only source of ground voltage is from the particular output of interest, the ground and output pin inductances will always slow down a high-to-low transition. They produce a voltage in opposition to the output pin voltage at the beginning of the discharge when currents tend to be high and voltage changes rapidly. As discharge continues, the available drive decreases, and currents increase less rapidly. Eventually the current begins to fall, and the ground voltage reverses polarity, which tends to limit the rate at which the current decreases. If currents have been high, and the inductances are large, there may be substantial undershoot at the end of the switching cycle which can drive the output pin below ground.

If multiple outputs are switching simultaneously, the total ground noise needs to be considered to determine the result for a particular output. For this case, it can happen that ground noise will, in fact, speed up an output; on the other hand, it may introduce delays that are much larger than those possible with single output switching. This behavior makes it difficult to predict, except on a case by case basis, what the actual effects of multiple output switching will be. Curves of delay vs multiple switching have been published, but these serve only as rough guides to indicate potential problems, and need to be backed up with actual analysis for any particular application.

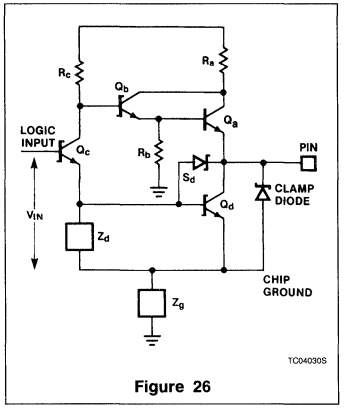


Figure 26

In addition to the direct influence on discharge voltage, excessive ground noise can affect the operation of the control components, and alter both rise and fall times by driving pull-up or pull-down stages incorrectly. One example of this can be understood with reference to Figure 26. The scenario is that the output pin is LOW, but on the verge of switching HIGH, with V_{IN} falling and Q_c ready to turn off. A problem occurs if, at the instant before the pull-up transistor Q_a turns on to pull the output pin high, the voltage from output pin to chip ground falls. This can happen as a result of inductive undershoot driving the output pin down, or by a rise in ground voltage caused by currents completely unrelated to the output of interest. The low output-pin-to-chip-ground voltage pulls down the emitter of Q_c through Schottky clamp

Circuit Characteristics

diode S_d, and if V_{IN} is not low enough to counteract this, Q_c will not turn off. The net result is that R_c cannot rise, and the transition is delayed until the noise voltage from output to ground disappears.

V_{CC} Noise As An Additional Problem

Inductance in the V_{CC} lead produces noise in the on-chip V_{CC} voltage that is entirely analogous to ground voltage. The effects of V_{CC} noise can be nearly as harmful as those produced by ground noise, the only significant difference being the fact that TTL input voltages are referenced to ground instead of V_{CC}.

The first symptom of excessive V_{CC} inductive voltage drop is a change in the edge rate for a low-to-high transition. This will decrease if the on-chip V_{CC} falls, and increase if it rises. If the ground to V_{CC} voltage falls below a minimum value, internal circuit delays or glitches can occur, and functions with flip-flops or other storage elements may lose data. As is the case with excessive ground noise, FAST circuits may break into relaxation oscillation.

Because V_{CC} to ground voltage must remain above a minimum value to avoid logic errors and glitches, it is absolutely vital that V_{CC} to ground bypassing is adequate. This requires low inductance V_{CC} and ground PC traces, and low inductance bypass capacitors. FAST parts are guaranteed to function properly for low V_{CC} of 4.5V. This means that pin voltages must not fall below this value for any appreciable time ... fractions of nanoseconds; V_{CC} system voltage should be close to the maximum guaranteed value for safe system design.

Designing To Reduce The Effects Of Ground Noise

The typical 1.5V minimum value for ground noise, calculated in the preceeding example, points out the possibility of noise-related problems when only one standard 50pF load is being driven by an output stage. Simultaneous switching of more than one such load obviously increases the risk of trouble, and raises the question of how an octal part can work at all. Fortunately, the real world, with careful PC layout, is not usually so grim.

The standard 50pF load is a lot of capacitance, chosen so one can estimate the chip response for a single output switching under conditions that approach worst case. On a modern PC board a wire trace that has 50pF stray capacitance is several feet long and looks like a resistive delay line instead of a lumped capacitor. Extremely fast buffer drivers, with multiple ground and V_{CC} pins brought out on the side of the package, are now available to drive low impedance loads on both PC boards and terminated back planes. These parts are equally useful as buffers to unload circuits that are especially sensitive to ground noise, such as octal latches and flip-flops.

Traces on a PC card must be short to behave like lumped capacitance for an output stage. For this case, a major contributor to driver current is the load presented by the input stages of the driven circuits, and the associated stray capacitance. As previously mentioned, the input current for FAST parts is related to edge rates, and is generally larger than the measured static value of input capacitance would predict. Because of this, the useful fan-out of FAST circuits may be more dependent on ground noise of drivers with heavy capacitive loads than on the amount of current available to a static DC load, which is the guaranteed data sheet value.

Most Signetics' FAST parts are available in surface mount packages, and these have lower ground inductance than the standard DIP parts.

Some of the standard TTL functions have been paralleled with equivalent DIP parts with side pin-out of both ground and V_{CC}. This is accomplished either by rotating the die 90° in the package, or by shifting the ground and V_{CC} bonding pins from their corner locations on the die. The parts are not, of course, pin-for-pin replacements of the equivalent functions, but the ground and V_{CC} inductances are about one-half as large as for the corner-pin parts.

Inductance of output signal pins reduces the rate at which associated ground current can change, and this reduces ground noise voltage without a corresponding reduction of static output voltage. This inductance may be intentionally increased by adding trace length on the PC board; one needs to be careful, and anticipate the increase in output ringing during switching transitions.

In summary, there are many potential problems that one can anticipate in logic systems with fast edge rates. Some of these are dependent on the available components and their respective packages, and the system designer must be certain that the demands made of them are not more than they can handle. A second major consideration is the system layout, especially from the standpoint of ground, V_{CC}, and signal lead inductance. If one is careful with PC design and layout, and chooses components wisely, FAST systems deliver performance second to none in the TTL world.

Signetics

Logic Products

Section 4
FAST User's Guide

INDEX

Signetics

Data Sheet Specification Guide

Logic Products

INTRODUCTION

Signetics' FAST data sheets have been configured for quick usability.

They are self-contained and should require minimum reference to other sections for amplifying information.

All references to military products have been deleted from this manual, specifically, to reflect recent government requirements imposed via Revision C of MIL-STD-883, including the general provisions of paragraph 1.2. Specifications for military-grade FAST products are included in the Military Products Data Manual available from the nearest Signetics Sales Office or Sales Representative.

TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed at the top of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part.

In the case of clocked products, this is sometimes the maximum frequency of operation. In any event, this number is under the operating conditions of $V_{CC} = 5.0V$ and $T_A = 25°C$.

The typical I_{CC} current shown in that same specification block is the average current (in the case of gates, this will be the average of the I_{CCH} and I_{CCL} currents) at $V_{CC} = 5.0V$ and $T_A = 25°C$. It represents the total current through the package, not the current through the individual functions.

LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol," explicitly shows the internal logic (except for complex logic). The other is "Logic Symbol (IEEE/IEC)" as developed by the IEC and IEEE. The International Electrotechnical Commission (IEC) has developed a very powerful symbolic language than can show the relationship of each input of a digital logic circuit to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 817-12) that will consolidate the original work started in the mid-1960's and published in 1972 (Publication 117-15), and the amendments and supplements that have followed. Similarly, for the U.S.A., IEEE Committee SCC 11 has revised the publication IEEE Std 91/ANSI Y32.14-1973.

The updated version IEEE Standard Graphic Symbols for Logic Functions ANSI/IEEE Std 91-1984 (Revision of ANSI/IEEE Std 91-1973 [ANSI Y32.14-1973]) can be ordered through:

IEEE Service Center
445 Hoes Lane
Piscataway, New Jersey 08854
Phone (201) 981-0060

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it ... there is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than −0.5V is applied to the output pin, after that voltage is removed, the part will still be functional and its useful life will not have been shortened.

Input and output voltage specifications in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (−0.5V).

Absolute maximum ratings imply that any transient voltages, currents, and temperatures will not exceed the maximum ratings. Absolute maximum ratings are shown in Table 1.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has a dual purpose. It sets environmental conditions (operating free-air temperature), and it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in these tables. Signetics feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	Standard outputs	40	mA
		3-State outputs	48	mA
		All buffer outputs	128	mA
T_A	Operating free-air temperature range		0 to 70	°C
	Storage temperature range		−65 to +150	°C

with parametric test equipment ... if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by DC Electrical Characteristics table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Thus, V_{IH} and V_{IL} should never be used in testing the functionality of any FAST part type. For these types of tests, input voltages of +4.5V and 0.0V should be used for the HIGH and LOW states, respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" HIGHs and LOWs during functional testing is done primarily to reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet. The situation in a system on a PC board is less severe than in a noisy production environment. Typical recommended operating conditions are shown in Table 2.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during their testing operations conducted under the conditions set forth in the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with V_{CC} = +4.75V, V_{IH} = 0.8V across the temperature range of 0°C to +70°C, and with an output current of I_{OH} = −1.0mA. In this table, one sees the heritage of the original junction-isolated Schottky family ... V_{OL} = 0.5V at I_{OL} = 20mA. This gives the user a guaranteed worst-case LOW-state noise immunity of 0.3V. In the HIGH state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the HIGH state than in the LOW, this is a useful state of affairs. Because the impedance of an output in the HIGH state is generally much higher than in the LOW state, more noise immunity in the HIGH state is needed. This is because the noise source couples noise onto the output connection of the device — that output tries to pull the noise source down by sinking the energy to ground or to V_{CC}, depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective in shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the HIGH state compensates for the higher impedance. The result is a nice balance of sink and drive current capabilities with the optimum amount of noise immunity in both states.

V_{OH} and V_{OL} values may vary depending on whether 5% or 10% V_{CC} swings are specified. The type of output structure — standard, 3-State, or buffer will also affect the value of V_{OH} and V_{OL}. Generally, as the output current and V_{CC} variations increase, the guaranteed minimum V_{OH} decreases and the maximum V_{OL} increases. Signetics specifies and tests V_{OH} and V_{OL} for both 5% and 10% V_{CC} swings.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at a guaranteed minimum input breakdown voltage. The test conditions for I_I vary according to the type of input structure being tested. Diode inputs are tested with V_{CC} = MAX and 7.0V at the input. NPN inputs are tested with V_{CC} = 0.0V and 7.0V at the input. It is necessary to turn V_{CC} off for the NPN input test to measure leakage. Otherwise, the current source is on and the leakage is undetectable. When I_I is being measured on transceiver I/O pins, both V_{CC} and the input voltage are 5.5V. The reduced input voltage is necessary because of the output structure connected to the input structure. Output structures break down sooner than input structures and it is impossible to test the input without testing the output also.

I_{IH} for both Diode and NPN input structures is less than 20μA typically. I_{IL} is less than 20μA for NPN inputs and less than 600μA for Diode inputs. If multiple input structures are tied together in the design, then the input current values also multiply. The fan-out for devices with NPN inputs is 30 times greater than those with Diode inputs. This means the output current sinking ability of the device driving the input to the LOW state could be 30 times less when driving NPN devices.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage	Open collector			4.5	V
I_{OH}	HIGH-level output current	Standard			−1	mA
		3-State			−3	mA
		Buffers			−15	mA
I_{OL}	LOW-level output current	Standard			20	mA
		3-State			24	mA
		Buffers			64	mA
T_A	Operating free-air temperature		0		70	°C

For transceiver I/O pins the outputs are in the HIGH impedance state when the inputs are tested. Therefore, a maximum of 50μA extra leakage is allowed and combined with the I_{IH} and I_{IL} values. These tests are called $I_{IH} + I_{OZH}$ and $I_{IL} + I_{OZL}$ to more accurately describe the true measurement being made.

I_{OZH} is tested with set-up conditions that would put the output in the HIGH state if it were not in the 3-State high impedance condition. I_{OZL} is similar except the set-up condition is for the LOW state.

I_{OH} is tested only on open collector outputs as a leakage test for the lower output transistor structure. Both V_{CC} and V_{OH} are at the same value so that there is not a current path to or from V_{CC} that would mask the leakage.

Short-circuit output current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that specification has totally changed. Originally, I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground, the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally-induced malfunctions could occur after several seconds of sustained test.

Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the LOW state. When the output is switched HIGH, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to its new state of V_{OH}. At the instant the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. We now reach the critical point in our discussion. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μFd of line capacitance tied to the output, a load that is unrealistically high by several orders of magnitude.

The effect of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious — AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through that output state and may cause functional failure or damage to the structure. A test-induced failure may occur if the I_{OS} test time is excessive. As long as the I_{OS} condition is very brief, typically 50ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures might occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging line capacitance. The Signetics data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground an output for too long a time, causing functional failure or damage. DC electrical characteristics are shown in Table 3.

AC ELECTRICAL CHARACTERISTICS

The AC Electrical Characteristics table (see Table 4) contains the guaranteed limits when tested under the conditions set forth in the AC Test Circuits and Waveforms section. In some cases, the test conditions are further defined by the AC set-up requirements (see Table 5) — this is generally the case with counters and flip-flops where set-up and hold times are involved.

All of the AC characteristics are guaranteed with 50pF load capacitance. The reason for choosing 50pF over 15pF as load capacitance is that it allows more leeway in dealing with stray capacitance, and also loads the device during rising or falling output transitions, which more closely resembles the loading to be expected in average applications, thus giving the designer more useful delay figures.

Although the 50pF load capacitance will increase the propagation delay by an average of about 1ns for FAST devices, it will increase several ns for standard Schottky devices.

The load resistor of 500Ω is conveniently specified as both a pull-up and pull-down load resistor.

FAST products are being released in the surface-mounted SO package as a commercial option. Because of the reduced inductance inherent in this package, minimum propagation delays are being derated by 0.2ns. This is reflected by a note at the bottom of Table 4.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER[1]			CONDITIONS[2]	LIMITS[2] Min	Typ[3]	Max	UNITS	V_{CC}[4]
V_{IH}	Input HIGH voltage			Recognized as a HIGH signal over recommended V_{CC} and T_A range	2.0			V	
V_{IL}	Input LOW voltage			Recognized as a LOW signal over recommended V_{CC} and T_A range			0.8	V	
V_{IK} (V_{CD})	Input clamp diode voltage			$I_{IN} = -18mA$			−1.2	V	MIN
V_{OH}	Output HIGH voltage	Std.[5]	±10%	$I_{OH} = -1mA$	2.5	3.4		V	MIN
			±5%	$I_{OH} = -1mA$	2.7	3.4		V	MIN
		3-State	±10%	$I_{OH} = -3mA$	2.4	3.3		V	MIN
			±5%	$I_{OH} = -3mA$	2.7	3.3		V	MIN
		Buffers	±10%	$I_{OH} = -15mA$	2.0	3.1		V	MIN
			±5%	$I_{OH} = -15mA$	2.0	3.1		V	MIN
V_{OL}	Output LOW voltage	Std.[5]	±10%	$I_{OL} = 20mA$		0.35	0.5	V	MIN
			±5%	$I_{OL} = 20mA$		0.35	0.5	V	MIN
		3-State	±10%	$I_{OL} = 24mA$		0.35	0.5	V	MIN
			±5%	$I_{OL} = 24mA$		0.35	0.5	V	MIN
		Buffers	±10%	$I_{OL} = 48mA$		0.35	0.5	V	MIN
			±5%	$I_{OL} = 64mA$		0.40	0.55	V	MIN
I_I	Input HIGH current breakdown test	Diode inputs		$V_{IN} = 7.0V$			100	μA	MAX
		NPN inputs		$V_{IN} = 7.0V$			100	μA	0.0V
		Transceiver I/O pins		$V_{IN} = 5.5V$			1.0	mA	5.5V
I_{IH}	Input HIGH current			$V_{IH} = 2.7V$ (20μA × n HIGH U.L.)			n(20)	μA	MAX
I_{IL}	Input LOW current	Diode inputs		$V_{IL} = 0.5V$ (−0.6mA × n LOW U.L.)			n(−0.6)	mA	MAX
		NPN inputs		$V_{IL} = 0.5V$ (−20μA × n LOW U.L.)			n(−20)	μA	MAX
I_{IH} + I_{OZH}	Input HIGH current (I/O pins)			$V_{IH} = 2.7V$ (20μA × n HIGH U.L.)			n(20) +50	μA	MAX
I_{IL}+ I_{OZL}	Input LOW current (I/O pins)	Diode inputs		$V_{IL} = 0.5V$ (−0.6mA × n LOW U.L.)			n(−0.6)	mA	MAX
		NPN inputs		$V_{IL} = 0.5V$ (−20μA × n LOW U.L.)			n(−20) −50	μA	MAX
I_{OZH}	3-State OFF current HIGH			$V_{OUT} = 2.7V$			50	μA	MAX
I_{OZL}	3-State OFF current LOW			$V_{OUT} = 0.5V$			−50	μA	MAX
I_{OH}	Open-collector output leakage			$V_{OH} = 4.5V$			250	μA	MIN
I_{OS}[6]	Output short-circuit current	Std.[5] 3-State		$V_{OUT} = 0V$	−80		−150	μA	MAX
		Buffer driver		$V_{OUT} = 0V$	−100		−225	μA	MAX

NOTES:

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to $T_A = +25°C$ and $V_{CC} = +5.0V$.
4. MIN and MAX refer to the values listed in the data sheet table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-State outputs.
6. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operation values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} test should be performed last.

AC CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, 'F374	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay Latch enable to output	Waveform 1, 'F373	3.0 2.0	9.0 4.0	11.5 7.0	5.0 3.0	13.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, 'F373	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, 'F374	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH}	Enable time to HIGH level	Waveform 2, 'F373 'F374	2.0 2.0	5.0 9.0	11.0 11.5	2.0 2.0	12.0 12.5	ns
t_{PZL}	Enable time to LOW level	Waveform 3, 'F373 'F374	2.0 2.0	5.6 5.3	7.5 7.5	2.0 2.0	8.5 8.5	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, 'F373 'F374	2.0 2.0	4.5 5.3	6.5 7.0	2.0 2.0	7.5 8.0	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, 'F373 'F374	2.0 2.0	3.8 4.3	5.0 5.5	2.0 2.0	6.0 6.5	ns

NOTE:
Substract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_W(H)$ $t_W(L)$	Latch enable pulse width	Waveform 1, 'F373	6.0 6.0			6.0 6.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, data to latch enable	Waveform 5, 'F373	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, data to latch enable	Waveform 5, 'F373	3.0 3.0			3.0 3.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width	Waveform 6, 'F374	7.0 6.0			7.0 6.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, data to clock	Waveform 7, 'F374	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, data to clock	Waveform 7, 'F374	2.0 2.0			2.0 2.0		ns

TEST CIRCUITS AND WAVEFORMS

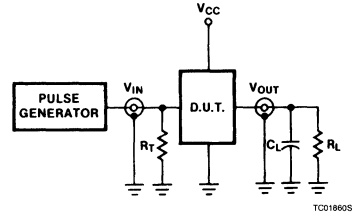
The 500Ω load resistor, R_L to ground, as described in Figure 1, acts as a ballast to slightly load the totem-pole pull-up and limit the quiescent HIGH-state voltage to about +3.5V. Otherwise, an output would rise quickly to about +3.5V, but then continue to rise very slowly up to about +4.4V. On the subsequent HIGH-to-LOW transition, the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the LOW state. Perhaps, more importantly, the 500Ω resistor to ground can be a high-frequency, passive probe for a sampling scope, which costs much less than the equivalent high-impedance probe. Alternatively, the 500Ω load to ground can simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Figure 2, Test Circuit for 3-State Outputs, shows a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with Open-Collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a 3-State output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establish a quiescent HIGH level of +3.5V, which correlates with the HIGH level discussed in the preceding paragraph.

As shown in Figure 3, AC Waveforms for FAST 74F373, 74F374, the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., LOW for t_{PLH}[2] or HIGH for t_{PHL}[2]).

Since the rising or falling waveform is RC-controlled, the 0.3V of change is more linear and is less susceptible to external influences.

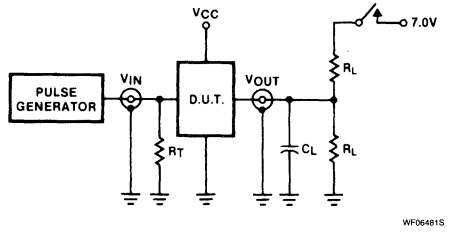
More importantly, from the system designer's point of view, 0.3V is adequate to ensure that a device output has turned OFF. It also gives system designers more realistic delay times to use in calculating minimum cycle times.



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 1. Test Circuit For Totem-Pole Outputs, 74F00



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PLZ}	closed
OC	closed
All other	open

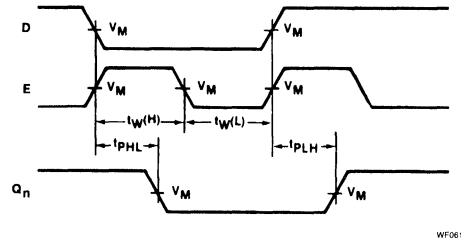
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

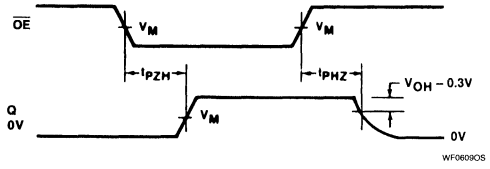
Figure 2. Test Circuit For 3-State And Open-Collector (OC) Outputs

Good, high-frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5ns, and signal swing of 0V to +3.0V, 1.0MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters as set-up time, hold time, recovery time, etc.

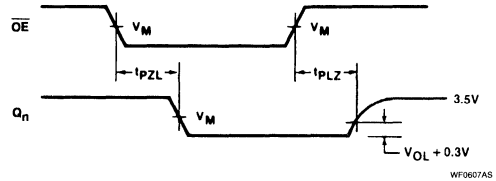
AC WAVEFORMS



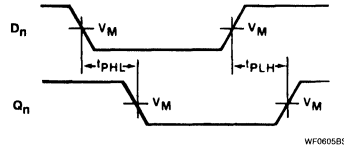
Waveform 1. Latch Enable To Output Delays And Latch Enable Pulse Width



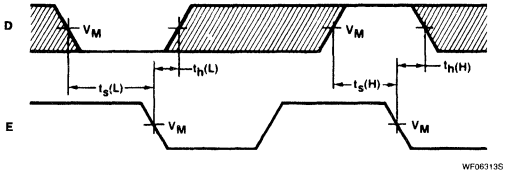
Waveform 2. 3-State Enable Time To HIGH Level And Disable Time From HIGH Level



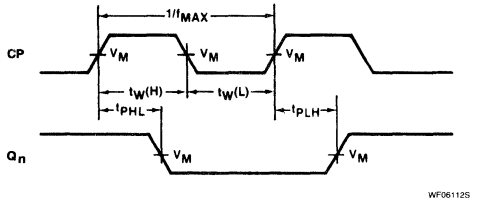
Waveform 3. 3-State Enable Time To LOW Level And Disable Time From LOW Level



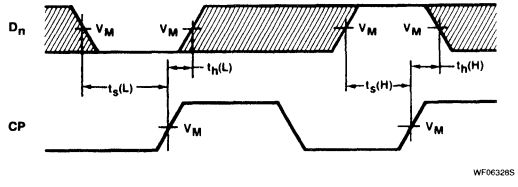
Waveform 4. Propagation Delay Data To Q Outputs



Waveform 5. Data Set-up Hold Times



Waveform 6. Clock To Output Delays And Clock Pulse Width



Waveform 7. Data Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3. AC Waveforms For FAST 74F373, 74F374

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DC SYMBOLS AND DEFINITIONS

Voltages — All voltages are referenced to ground. Negative-voltage limits are specified as absolute values (i.e., −10V is greater than −1.0V).

V_{CC} **Supply voltage:** The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

V_{IKMax} **Input clamp diode voltage:** The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.

V_{IH} **Input HIGH voltage:** The range of input voltages recognized by the device as a logic HIGH.

V_{IHMin} **Minimum input HIGH voltage:** This value is the guaranteed input HIGH threshold for the device. The minimum allowed input HIGH in a logic system.

V_{IL} **Input LOW voltage:** The range of input voltages recognized by the device as a logic LOW.

V_{ILMax} **Maximum input LOW voltage:** This value is the guaranteed input LOW threshold for the device. The maximum allowed input LOW in a logic system.

V_M **Measurement voltage:** The reference voltage level on AC waveforms for determining AC performance. Usually specified as 1.5V for the FAST family.

V_{OHMin} **Output HIGH voltage:** The minimum guaranteed HIGH voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OLMax} **Output LOW voltage:** The maximum guaranteed LOW voltage at an output terminal sinking the specified load current I_{OL}.

V_{T+} **Positive-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-} (Min).

V_{T-} **Negative-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above V_{T+} (Max).

Currents — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply current:** The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst-case operation unless specified.

I_I **Input leakage current:** The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.

I_{IH} **Input HIGH current:** The current flowing into an input when a specified HIGH-level voltage is applied to that input.

I_{IL} **Input LOW current:** The current flowing out of an input when a specified LOW-level voltage is applied to that input.

I_O **Output current:** The output current that is approximately one half of the true short-circuit output current (I_{OS}).

I_{OH} **Output HIGH current:** The leakage current flowing into a turned off Open-Collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OH1} **Output HIGH current:** The current necessary to guarantee the LOW to HIGH transition in a 30Ω transmission line on the incident wave.

I_{OL} **Output LOW current:** The current flowing into an output which is the LOW state.

I_{OL1} **Output LOW current:** The current necessary to guarantee the HIGH to LOW transition in a 30Ω transmission line on the incident wave.

I_{OS} **Output short-circuit current:** The current flowing out of an output which is in the HIGH state when that output is short circuit to ground.

I_{OZH} **Output off current HIGH:** The current flowing into a disabled 3-State output with a specified HIGH output voltage applied.

I_{OZL} **Output off current LOW:** The current flowing out of a disabled 3-State output with a specified LOW output voltage applied.

AC SYMBOLS AND DEFINITIONS

f_{MAX} **Maximum clock frequency:** The maximum input frequency at a Clock input for predictable performance. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PHZ} **Output disable time from HIGH level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the HIGH level to a high-impedance "off" state.

t_{PLZ} **Output disable time from LOW level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the LOW level to a high-impedance "off" state.

t_{PZH} **Output enable time to a HIGH level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high-impedance "off" state to HIGH level.

t_{PZL} **Output enable time to a LOW level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high-impedance "off" state to LOW level.

t_h **Hold time:** The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s **Set-up time:** The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its

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latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_W **Pulse width:** The time between the specified reference points on the leading and trailing edges of a pulse.

t_{REC} **Recovery time:** The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_{TLH} **Transition time, LOW-to-HIGH:** The time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW to HIGH.

t_{THL} **Transition time, HIGH-to-LOW:** The time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH to LOW.

t_r, t_f **Clock input rise and fall times:** 10% to 90% value.

4

Design Considerations

INTRODUCTION

The properties of high-speed FAST logic circuits dictate that care be taken in the design and layout of a system.

Some general design considerations are included in this section. This is not intended to be a thorough guideline for designing FAST systems, but a reference for some of the constraints and techniques to be considered when designing a high-speed system.

HANDLING PRECAUTIONS

As described in the Circuit Characteristics section, FAST devices are susceptible to damage from electrostatic discharge (ESD).

- Signetics FAST devices are shipped in conducting foam or anti-static tubes and foil-lined boxes to minimize ESD during shipment and unloading.
- Before opening the shipment of FAST devices, make sure that the individual is grounded and all handling means (such as tools, fixtures, and benches) are grounded.
- After removal from the shipping material, the leads of the FAST devices should always be grounded. In other words, FAST devices should be placed leads-down on a grounded surface, since ungrounded leads will attract static charge.
- Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn on-off, do not exceed absolute maximum ratings.
- After assembly on PC boards, ensure that ESD is minimized during handling, storage or maintenance.
- FAST inputs should never be left floating on a PC board. This precaution applies to any TTL family. As a temporary measure, a resistor with a resistance greater than 10kΩ should be soldered on the open input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static-generating materials.

INPUT CLAMPING

FAST circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative DC voltages or long-duration, negative pulses. Certain FAST part types with the NPN base input structure also provide clamping of positive overshoots.

UNUSED INPUTS

Proper digital design rules dictate that all unused inputs on TTL devices be tied either HIGH or LOW. This is especially important with FAST logic.

Electrically-open inputs can degrade AC noise immunity as well as the switching speed of the device. Small geometries make FAST more susceptible to damage by electrostatic discharge than other TTL families. Tying inputs to V_{CC} or GND, directly or through a resistor, protects the device from in-circuit electrostatic damage. Additionally, while most unconnected TTL inputs float HIGH, FAST devices with NPN inputs float LOW.

FAST devices do not require an input resistor to tie the input HIGH. Inputs can be connected directly to V_{CC} as well as ground.

Possible ways of handling unused inputs are:

1. Unused active-HIGH NAND or AND inputs to V_{CC}. The inputs should be maintained at a voltage greater than 2.7V, but should not exceed the absolute maximum rating.
2. Connect unused active-HIGH NOR or OR inputs to ground.
3. Tie unused active-HIGH NAND or AND inputs to an used input of the same gate, provided that the HIGH-level fanout of the driving circuit is not impaired.
4. Connect the unused active-HIGH NAND or AND inputs to the output of an unused gate that is forced HIGH.

MIXING FAST WITH OTHER TTL FAMILIES

Mixing the slower TTL families such as 74 and 74LS with the higher speed families such as 74F is possible but must be done with caution. Each family of TTL devices has unique input and output characteristics optimized to achieve the desired speed or power features.

The unique speed/power characteristics of the FAST devices are achieved partially by the internal fast rise and fall times, as well as those at input and output nodes. These fast transitions can cause noise of various types in a system. Power and ground line noise are generated by the faster transitions of the current in the output load capacitance. Signal line noise can also be generated by the fast output transitions.

The noise generated by 74F devices can be minimized in systems designed with shorter signal lines, good ground planes, well-bypassed power distribution networks, layouts that minimize adjacent signal lines that run parallel and improved impedance matching in signal lines to reduce transmission line-type reflections.

INPUT LOADING AND OUTPUT DRIVE COMPARISON

The logic levels of all TTL products are fully compatible with each other. However, the input loading and output drive characteristics of each family are different and must be taken into consideration when mixing them in a system. Table 1 shows the relative drive capabilities of each family for commercial temperature and voltage ranges.

INPUT-OUTPUT LOADING AND FAN-OUT TABLE

For convenience in system design, the input-output loading and fan-out characteristics of each circuit are specified in terms of unit loads and actual load value. One FAST Unit Load (U.L.) in the HIGH state is defined as 20μA; thus both the input HIGH leakage current, I_{IH}, and output HIGH current-sourcing capability, I_{OH}, are normalized to 20μA.

Similarly, one FAST Unit Load (U.L.) in the LOW state is defined as 0.6mA and both the input LOW current, I_{IL}, and input LOW current/TL, and the output LOW current-sinking capability, I_{OL}, are normalized to 0.6mA.

For added convenience, the actual load value in amperes is listed in the column adjacent to U.L.

On some FAST devices, high-impedance NPN base input structure has been utilized.

With this structure, the LOW level input current, I_{IL}, has been reduced to 20μA. This characteristic is 30 times lower than the requirement of devices using the conventional input structure. This feature improves fan-out in the LOW state and can help reduce part count in system design by eliminating buffers in some applications.

Design Considerations

Table 1. Loading Comparisons

DRIVEN DEVICE FAMILY:		74F	74F (NPN)	74LS	74	74S	8200/9300	82S00
DRIVING DEVICE FAMILY	I_{OL} (Min)	I_{IL} (Max)						
		0.6mA	20μA	0.4mA	1.6mA	2.0mA	1.6mA	0.4mA
		Maximum Number of Loads Driven						
74F	20mA	33	1,000	50	12.5	10	12	50
74F (NPN)	64mA	106	3,200	160	40	32	40	160
74LS	8mA	13	400	20	5	4	5	20
74LS Buffer	24mA	40	1,200	60	15	12	15	60
74	16mA	26	800	40	10	8	10	40
74 Buffer	40mA	78	2,400	120	30	24	30	120
74S	20mA	33	1,000	50	12.5	10	12	50
74S Buffer	60mA	100	3,000	150	37.5	30	37	150
8200/9300	16mA	26	800	40	10	8	10	40
82S00	20mA	33	1,000	50	12	10	12	50

CLOCK PULSE REQUIREMENTS

All FAST clock inputs are buffered to increase their tolerance of slow positive-clock edges and heavy ground noise. Nevertheless, the rise time on positive-edge-triggered devices should be less than the nominal clock-to-output delay time measured between 0.8V to 2.0V levels of the clock driver for added safety margin against heavy ground noise. Not only a fast rising, clean clock pulse is required, but the path between the clock drive and clock input of the device should be well-shielded from electromagnetic noise.

FAST OUTPUTS TIED TOGETHER

The only FAST outputs that are designed to be tied together are Open-Collector and 3-State outputs. Standard FAST outputs should not be tied together unless their logic levels will always be the same; either all HIGH or all LOW. When connecting Open-Collector or 3-State outputs together, some general guidelines must be observed.

Open-Collector Outputs

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have a pull-up resistor (or resistors) added between the OR-tie connector and V_{CC} to establish an active-HIGH level. Only special high-voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull-up resistor is determined as follows:

$$R\ (\text{Min}) = \frac{V_{CC}\ (\text{Max}) - V_{OL}}{I_{OL} - N_2\ (I_{IL})}$$

$$R\ (\text{Max}) = \frac{V_{CC}\ (\text{Min}) - V_{OH}}{N_1\ (I_{OH}) + N_2\ (I_{IH})}$$

where: I_{OL} = Minimum I_{OL} guarantee or OR-tied elements.

$N_2\ (I_{IL})$ = Cumulative maximum input LOW current for all inputs tied to OR-tie connection.

$N_1\ (I_{OH})$ = Cumulative maximum output HIGH leakage current for all outputs tied to OR-tie connection.

$N_2\ (I_{IH})$ = Cumulative maximum input HIGH leakage current for all inputs tied to OR-tie connection.

If a resistor divider network is used to provide the HIGH level, the R (Max) must be decreased enough to provide the required [(V_{OH}/R (pull-down)] current.

3-State Outputs

3-State outputs are designed to be tied together, but are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-State output should be active at any time. This generally requires that the output enable signals be non-overlapping. When TTL decoders are used to enable 3-State outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally guarantee when the address is changing.

Since most 3-State output enable signals are active-LOW, shift registers or edge-triggered storage registers provide good output enable buffers. Shift registers with one circulating LOW bit, such as the 'F164 or 'F194, are ideal for sequential enable signals. The 'F174 or 'F273 can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from LOW-to-HIGH faster than from HIGH-to-LOW, the selection of one device at a time is assured.

GND

Good system design starts with a well thought out ground layout. Try to use ground plane if possible. This will save headaches later on. If ground strip is used, try to reduce ground path in order to minimize ground inductance. This prevents crosstalk problems. Quite often, jumper wire is used for connecting to ground at the breadboarding stage, but a solid ground must be used eve at the breadboarding stage.

V_{CC}

Typical dynamic impedance of un-bypassed V_{CC} runs from 50Ω to 100Ω, depending on V_{CC} and GND configuration. This is why a sudden current demand, due to an IC output switching, can cause momentary reduction in V_{CC} unless a bypass (decoupling) capacitor is located near V_{CC}.

Not only is there a sudden current demand due to output switching transient, there is also a heavy current demand by the buffer driver. Assuming the buffer output sees a 50Ω dynamic load and the buffer LOW-to-HIGH transition is 2.5V, the current demand is 50mA per buffer. If it is an octal buffer, the

Design Considerations

current demand could be 0.4mA per package in 3ns time!

The next step is to figure out the capacitance requirement for each bypass capacitor. Using the previously-mentioned octal buffer and assuming the V_{CC} droop is 0.1V, then C is:

$$C = \frac{0.4A \times 3 \times 10^{-9}\ sec}{0.1V} = 12 \times 10F^{-9}$$

$$= 0.012\mu F$$

This formula is derived as follows:

$cQ = CV$

by differentiation:

$$\frac{\Delta Q}{\Delta t} = C\frac{\Delta V}{\Delta t}$$

Since $\frac{\Delta Q}{\Delta t} = I$

the equation becomes $I = C\frac{\Delta t}{\Delta t}$

hence, $C = \frac{I\Delta t}{\Delta V}$

Select the C bypass $\geqslant 0.02\mu F$ and try to use a high-quality RF capacitor. Place one bypass capacitor for each buffer and one bypass capacitor every two other types of IC packages. Make sure that the leads are cut as short as possible.

In addition, place bypass capacitors on a board to take care of board-level current transients.

CROSSTALK

The best way to handle crosstalk is to prevent it from occurring in the first place; quick-fixes are troublesome and costly. To prevent crosstalk, maximize spacing between signal lines and minimize spacing between signal lines and ground lines. Preferably, place ground lines between signal lines. For added precaution, add a ground trace alongside either the potential cross-talker or the cross-listener.

For backplane, or wire-wrap, use twisted pair for sensitive functions — clocks, asynchronous set or reset, asynchronous parallel load. In flat cable, make every other conductor ground.

For multilayer P.C. boards, run signal lines in adjacent planes perpendicular to prevent magnetic coupling, and limit capacitive coupling. Use power shield (V_{CC} or ground plane) in between signal planes.

Since any voltage change, noise or otherwise, arriving at the unterminated end of transmission lines double in amplitude, even a partially terminated line reduces the amplitude of the signal (noise or otherwise) appearing at the end of the line; therefore, using a terminating resistor whose value is equal to the line characteristics impedance will help reduce crosstalk.

Signetics

Logic Products

Section 5
Military Information

Signetics

Military Information

Logic Products

Effective January 1, 1985, this section has been superseded by the 1985 Military Products Data Manual. Information regarding this manual can be obtained from the Military Division in Sacramento. (916) 925-6700.

MILITARY STANDARD PRODUCTS

The Signetics Military product line offering includes JAN Qualified Class S and B, and Class B vendor standard products. These products are designed to offer our customers the optimum of quality, reliability, delivery and cost. The benefits of these products provide our customers:

- Industry-wide standardization.
- Fewer custom specifications.
- Cost savings associated with larger lots.
- Better lead times by reducing specification negotiation time and allowing off-the-shelf procurement.
- Industry standard marking.

JAN QUALIFIED PRODUCT

JAN qualified product is offered to give our customers the highest quality and reliability. The JAN processing levels (Class S and B) are a result of the Governments product standardization programs, and our JAN production lines are certified by the qualifying activity, the Defense Electronics Supply Center (DESC). Signetics strongly recommends the use of JAN product which is listed on the MIL-M-38510 Qualified Products List (QPL).

JAN qualified products are fabricated, assembled, tested, and inspected in U.S. Government certified facilities in Sunnyvale, California (wafer fab), Orem, Utah (wafer fab, assembly), and in Sacramento, California (burn-in, test, quality conformance inspection).

Testing and inspection to MIL-M-38510 is monitored by resident Government Source Inspection (GSI) personnel representing the Defense Contract Administration Services (DCAS).

DESC prohibits any customer imposed additions, deviations, omissions, or waivers on procurement of JAN products. Product must conform completely to Government specifications prior to shipment and is verified by Signetics Quality Control. A Certificate of Conformance and Procurement Traceability is supplied with each lot shipped.

JAN qualified products are listed in QPL-38510, issued periodically by DESC. For current QPL information, customers may contact their local sales representative, Military Marketing in Sacramento, or directly with DESC-EQM at (513) 296-6355. The JAN products listed herein should be considered valid only on its date of publication.

These categories of product conform to Quality Levels A and B of MIL-HDBK-217 ($\pi_Q = 0.5$ Class S, 1.0 for Class B).

The example at the bottom of this page illustrates the part numbering system for JAN product, the part number is per MIL-M-38510.

SIGNETICS CLASS B STANDARD PRODUCT (RB)

Signetics Class B Standard product is offered for use when no JAN product is qualified on the QPL, DESC Drawing product is not available, or when program requirements allow the use of vendor standard product.

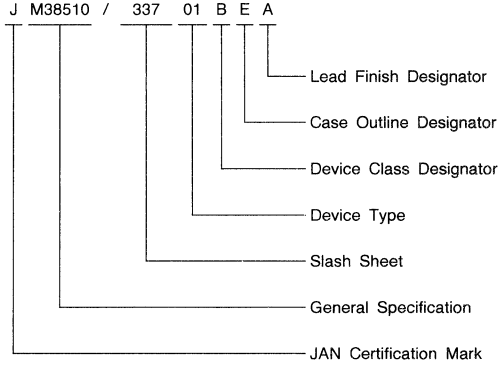
Class B standard product conforms to MIL-STD-883, general provisions Paragraph 1.2.1 (and its sub-paragraphs), except where noted. (See Product Noncompliance Section of Military Data Book and/or Hand Book). No other claims, expressed or implied, are made of equivalence to JAN product or to MIL-M-38510. Signetics compliant product also conforms with JEDEC Publication 101, except for marking content.

Electrical test requirements are as stated in the most current **Signetics Military Data Manual only.**

- 100% final electrical tests include all Data Manual parameter limits, test conditions, and temperatures applicable to Subgroups 1, 2, 3, 7, and 9 of MIL-STD-883, Method 5004 for digital products, or to Subgroups 1, 2, 3, 4, and 9 for Linear Products.
- Group A sample electrical inspection tests include all final electrical subgroups as well as all other Data Manual parameters with specified minimum or maximum limits.
- End point electrical tests used for QCI inspection sampling (Groups C and D) are those Data Manual parameter limits, test conditions, and temperatures applicable to Group A Subgroups 1, 2, and 3 per MIL-STD-883, Method 5005, or to Subgroup 1 for Linear Products.

Data Manual parameters which have no specified minimum or maximum limits (typical performance only) are not tested. Parameters which have limits specified at 25°C only, are tested only at that temperature. Detailed parameter assignment to subgroups and other test detail are contained in documented Signetics internal Product Electrical specifications, and are available upon request. Actual test program symbolics are available for customer review at the factory, but are considered proprietary and will not be copied or otherwise distributed outside of Signetics.

QCI Groups A and B testing are performed on all products and packages per MIL-M-38510 and MIL-STD-883, Method 5005. Signetics utilizes inline Group A and alternate Group B for all lines. QCI Groups C and D are routinely



Military Information

performed on all compliant families and package types.

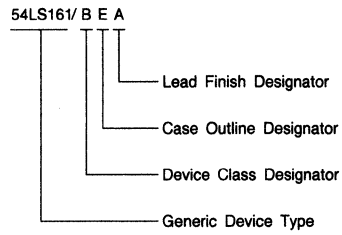
Waivers, deviations, or exceptions of any kind deemed necessary in the course of the contracts must be issued in accordance with DOD-STD-480. Should Signetics have knowledge of the need for waivers at the time of response to quote (RFQ) or order entry, that information will be transmitted prior to order entry.

Package types which do not have case outlines letters assigned in MIL-M-38510, Appendix C, will be assigned case outline letters per JEDEC Publication 101.

The Signetics standard Product Assurance Plan documentation is available for customer review at the factory, and is considered proprietary.

This category of product conforms to quality level B-2 of MIL-HDBK-217 ($\pi_Q = 6.5$).

For Class B Standard Product, the part number is listed as follows:



Signetics

Logic Products

Section 6
74 Series Data Sheets

Signetics

FAST 74F00
Gate

Quad Two-Input NAND Gate
Product Specification

Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F00	3.4ns	4.4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F00N
Plastic SO-14	N74F00D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

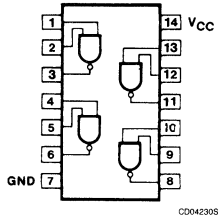
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

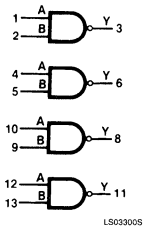
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

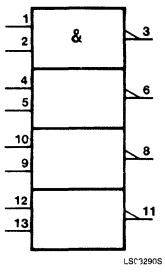
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F00			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.9	2.8	mA
		I_{CCL}		V_{IN} = 4.5V		6.8	10.2	mA

NOTES:

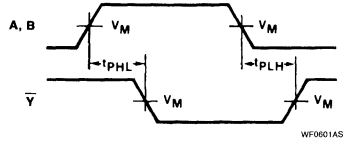
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F00					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

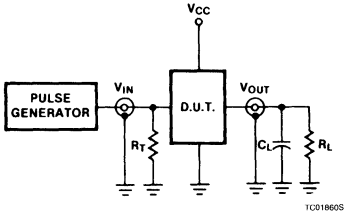
AC WAVEFORM



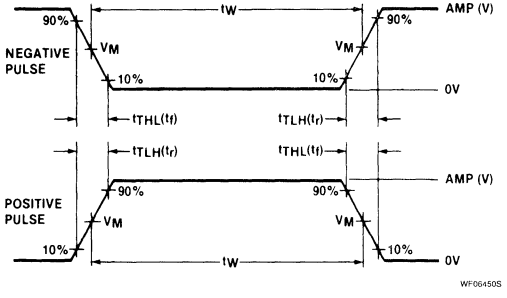
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F02
Gate

Quad Two-Input NOR Gate
Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	$\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F02	3.4ns	4.4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F02N
Plastic SO-14	N74F02D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
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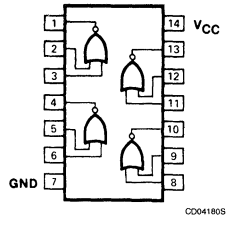
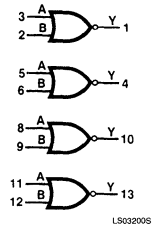
$\overline{Y}$	Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

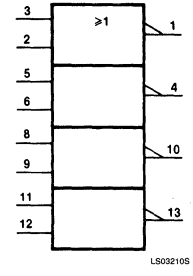
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F02			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			3.0	5.6	mA
		I_{CCL}				7.0	13	mA

NOTES:

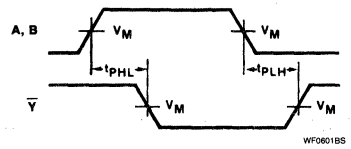
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	74F02					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A, B to $\overline{Y}$	Waveform 1	2.5 2.0	4.4 3.2	5.5 4.3	2.5 2.0	6.5 5.3	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

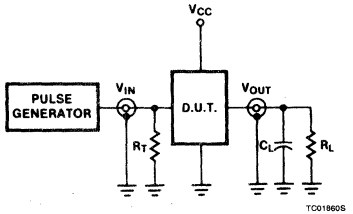
AC WAVEFORM



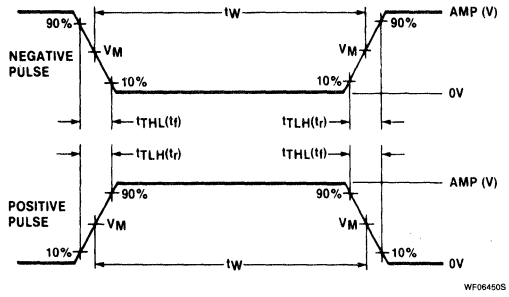
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F04
Inverter

Hex Inverter
Product Specification

Logic Products

FUNCTION TABLE

INPUT	OUTPUT
A	$\overline{Y}$
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F04	3.5ns	6.9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F04N
Plastic SO-14	N74F04D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

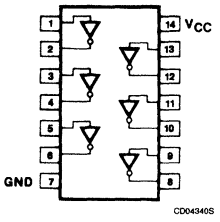
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Outputs	50/33	1.0mA/20mA

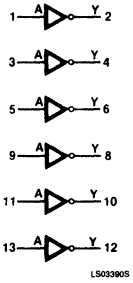
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

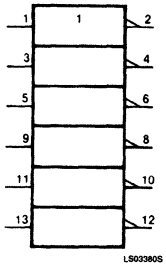
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F04			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−85	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		2.8	4.2	mA
		I_{CCL}		V_{IN} = 4.5V		10.2	15.3	mA

NOTES:

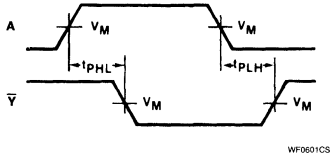
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F04					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.4	3.7	5.0	2.4	6.0	ns
t_{PHL}	A to $\overline{Y}$		1.5	3.2	4.3	1.5	5.3	

NOTE:
Subtract 0.2ns from minimum values for SO package.

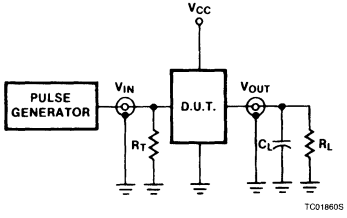
AC WAVEFORM



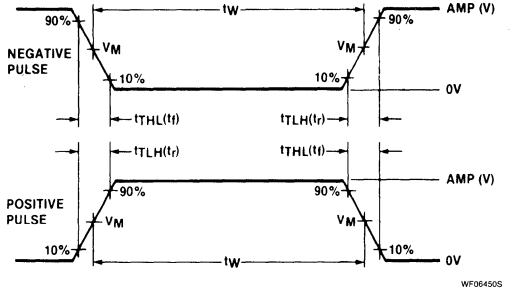
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M=1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F08
Gate

Quad Two-Input AND Gate
Product Specification

Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F08	4.1ns	7.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F08N
Plastic SO-14	N74F08D

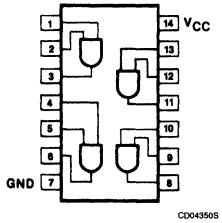
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

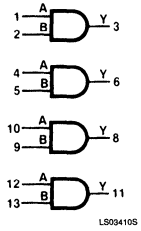
NOTE:
One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



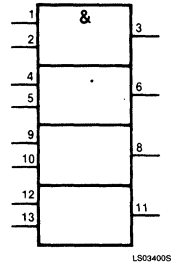
CD04350S

LOGIC SYMBOL



LS03410S

LOGIC SYMBOL (IEEE/IEC)



LS03400S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F08			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V		5.5	8.3	mA
		I_{CCL}		V_{IN} = GND		8.6	12.9	mA

NOTES:

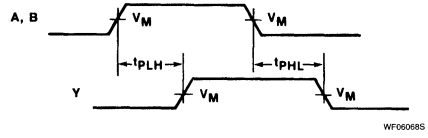
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS

PARAMETER		TEST CONDITIONS	74F08					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to Y	Waveform 1	3.0 2.5	4.2 4.0	5.6 5.3	3.0 2.5	6.6 6.3	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

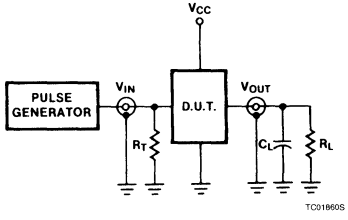
AC WAVEFORM



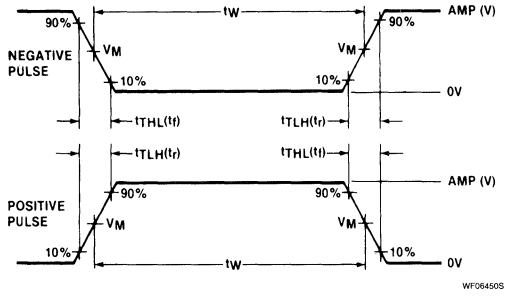
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F10, 74F11 Gates

Triple Three-Input NAND ('F10), AND ('F11) Gates
Product Specification

Logic Products

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	$\overline{Y}$('F10)	Y('F11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = HIGH voltage level
L = LOW voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F10	3.5ns	3.3mA
74F11	4.2ns	5.3mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F10N, N74F11N
Plastic SO-14	N74F10D, N74F11D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

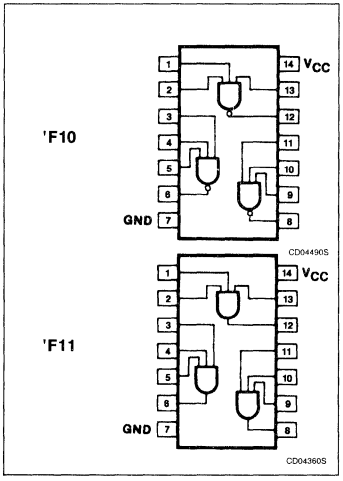
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A – C	Inputs	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	Outputs	50/33	1.0mA/20mA

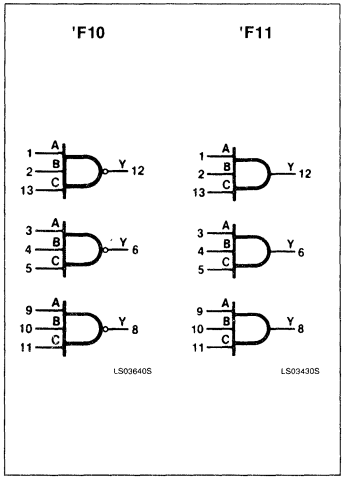
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

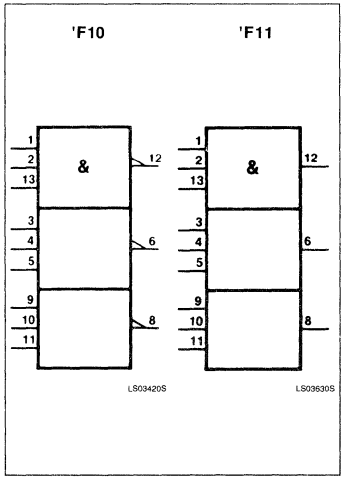
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER				TEST CONDITIONS[1]		74F10, 11			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current			V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current			V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX, V_O = 0.0V		−60	−75	−150	mA
I_{CC}	Supply current (total)	'F10	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.8	2.1	mA
			I_{CCL}		V_{IN} = 4.5V		6.0	7.7	mA
		'F11	I_{CCH}		V_{IN} = 4.5V		4.7	6.2	mA
			I_{CCL}		V_{IN} = GND		7.2	9.7	mA

NOTES:

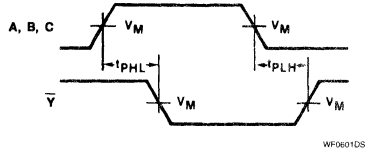
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

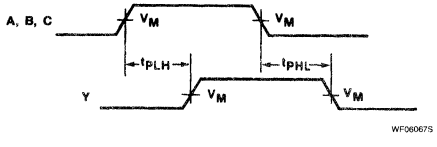
PARAMETER		TEST CONDITIONS	74F10, 11					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C to $\overline{Y}$	Waveform 1 'F10	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	ns
t_{PLH} t_{PHL}	Propagation delay A, B, C to Y	Waveform 2 'F11	3.0 2.5	4.2 4.1	5.6 5.5	3.0 2.5	6.6 6.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



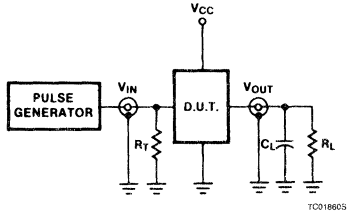
'F10
Waveform 1. For Inverting Outputs



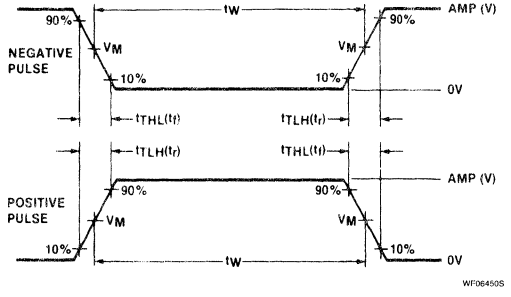
'F11
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M=1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F13
Schmitt Trigger

Dual 4-Input NAND Schmitt Trigger
Product Specification

Logic Products

DESCRIPTION

The F13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F13	7.8ns	5.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F13N
Plastic SO-14	N74F13D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

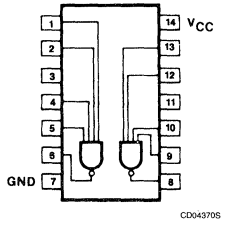
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Outputs	50/33	1.0mA/20mA

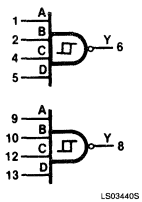
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



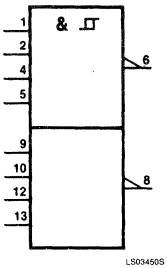
CD04370S

LOGIC SYMBOL



LS03440S

LOGIC SYMBOL (IEEE/IEC)



LS03450S

Schmitt Trigger | FAST 74F13

Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transitions of the other input as shown in Waveform 1.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F13			UNIT
				Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, $V_I = V_{T-MIN}$, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, $V_I = V_{T+MAX}$, I_{OH} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, $V_I = V_{T+}$			0		µA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, $V_I = V_{T-}$			−350		µA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	µA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	µA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.2	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−120	−150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.5	8.5	mA
	Supply current (total) I_{CCL}		V_{IN} = 4.5V		7.0	10.0	mA

NOTES:

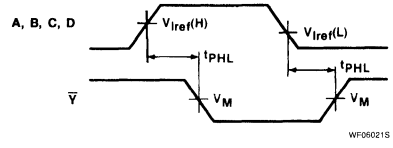
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F13					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	4.0	5.5	7.0	4.0	8.0	ns
t_{PHL}	A, B, C, D to $\overline{Y}$		9.0	11.0	13.5	9.0	13.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

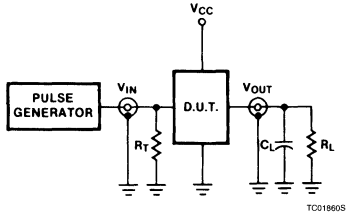
AC WAVEFORM



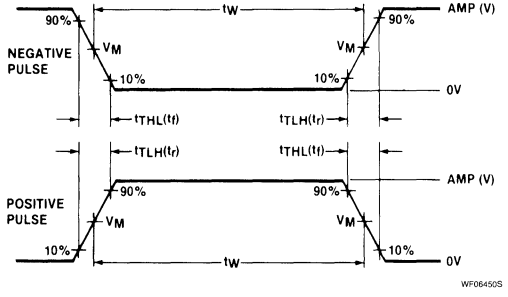
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F14
Schmitt Trigger

Hex Inverter Schmitt Trigger
Product Specification

Logic Products

DESCRIPTION

The 'F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F14	5.0ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F14N
Plastic SO-14	N74F14D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

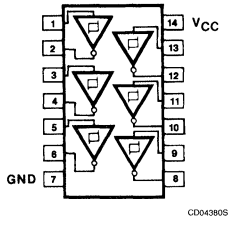
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

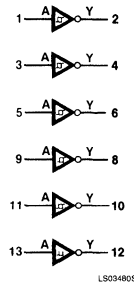
FUNCTION TABLE

INPUT	OUTPUT
A	$\overline{Y}$
0	1
1	0

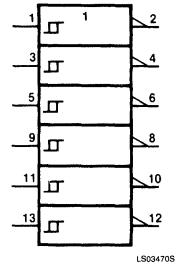
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F14			UNIT
				Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V		1.4	1.7	2.0	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis (V_{T+} − V_{T-})	V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_I = V_{T-MIN}, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_I = V_{T+MAX}, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, V_I = V_{T+}			0.0		μA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, V_I = V_{T-}			175		μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.2	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−135	−150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_{IN} = GND		13	22	mA
	Supply current (total) I_{CCL}		V_{IN} = 4.5V		23	32	mA

NOTES:

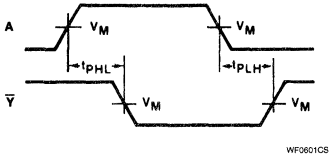
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F14					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to $\overline{Y}$	Waveform 1	4.0 3.5	6.5 5.0	8.5 6.5	4.0 3.5	9.5 7.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

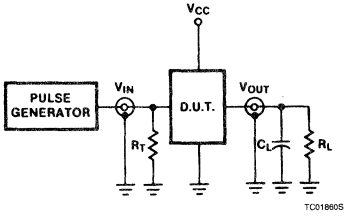
AC WAVEFORM



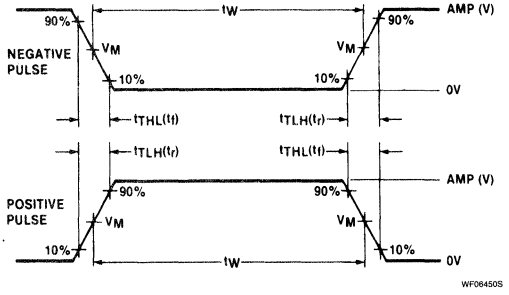
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F20
Gate

Dual Four-Input NAND Gate
Product Specification

Logic Products

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F20	3.5ns	2.2mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F20N
Plastic SO-14	N74F20D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

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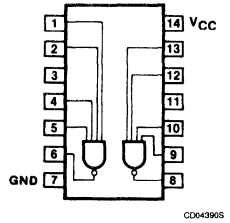
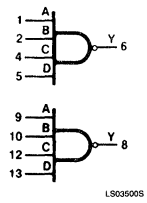
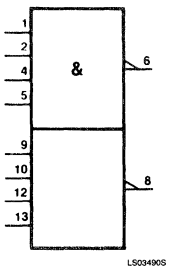
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F20			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−85	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		0.9	1.4	mA
		I_{CCL}		V_{IN} = 4.5V		3.4	5.1	mA

NOTES:

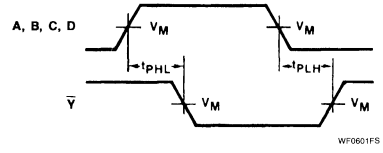
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F20					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.4	3.7	5.0	2.4	6.0	ns
t_{PHL}	A, B, C, D to $\overline{Y}$		2.0	3.2	4.3	2.0	5.3	

NOTE:
Subtract 0.2ns from minimum values for SO package.

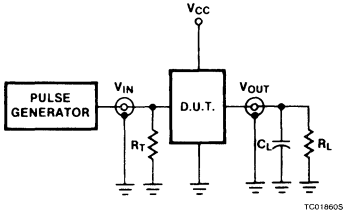
AC WAVEFORM



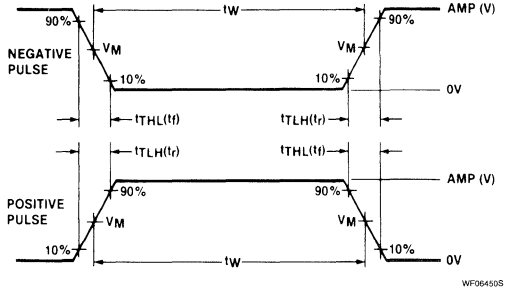
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F27
Gate

Triple Three-Input NOR Gate
Product Specification

Logic Products

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	$\overline{Y}$
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F27	3.0ns	6.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F27N
Plastic SO-14	N74F27D

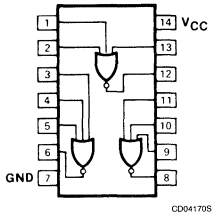
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

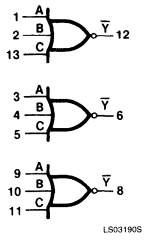
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

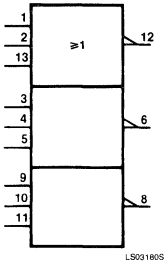
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F27			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			5	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.0	5.5	mA
		I_{CCL}		V_{IN} = 4.5V		8.5	12.0	mA

NOTES:

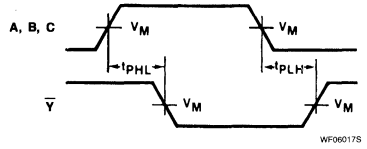
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F27					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C to $\overline{Y}$	Waveform 1	2.0 1.0	3.5 2.5	5.0 4.5	1.5 1.0	5.5 5.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

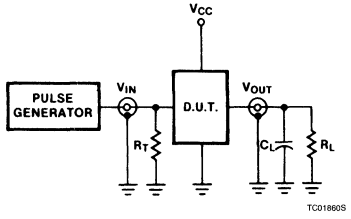
AC WAVEFORM



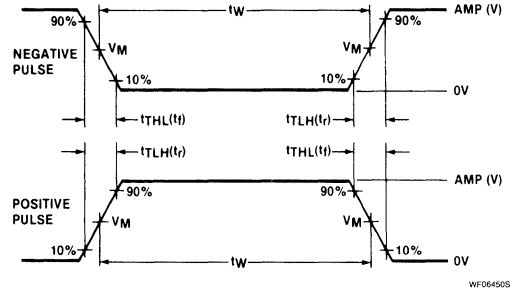
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input To Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F30
Gate

Eight-Input NAND Gate
Product Specification

Logic Products

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	$\overline{Y}$
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30	3.5ns	6.0mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F30N
Plastic SO-14	N74F30D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A – H	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

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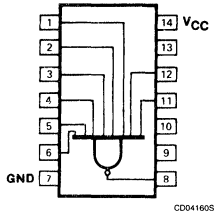
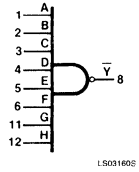
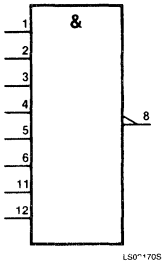
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F30			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			5	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_{IN} = GND		0.6	1.5	mA
	I_{CCL}		V_{IN} = 4.5V		2.8	4.0	mA

NOTES:

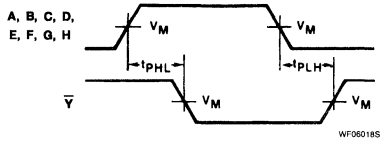
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F30					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to $\overline{Y}$	Waveform 1	1.0 1.5	3.0 3.5	4.5 5.0	1.0 1.5	5.0 5.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

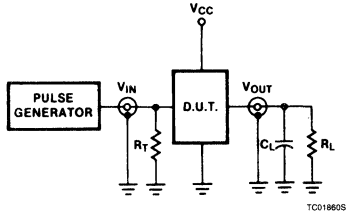
AC WAVEFORM



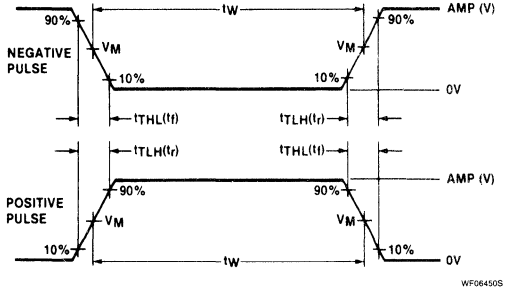
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input To Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F32
Gate

Quad Two-Input OR Gate
Product Specification

Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F32	4.1ns	8.2mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F32N
Plastic SO-14	N74F32D

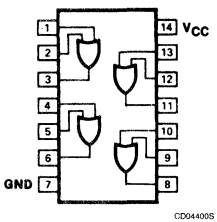
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

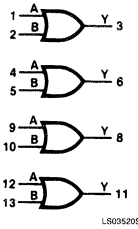
NOTE:
One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



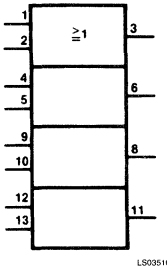
CD04400S

LOGIC SYMBOL



LS03520S

LOGIC SYMBOL (IEEE/IEC)



LS03510S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F32			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V		6.1	9.2	mA
		I_{CCL}		V_{IN} = GND		10.3	15.5	mA

NOTES:

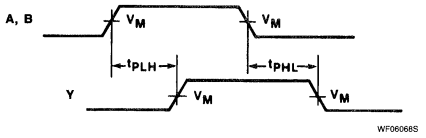
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	74F32					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to Y	Waveform 1	3.0 3.0	4.2 4.0	5.6 5.3	3.0 3.0	6.6 6.3	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

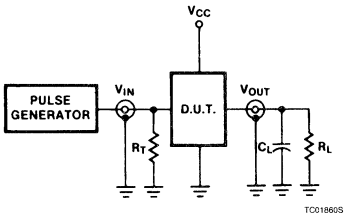
AC WAVEFORM



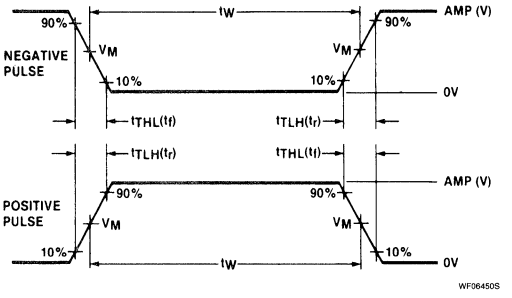
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F37
Buffer

Quad Two-Input NAND Buffer
Product Specification

Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F37	3.5ns	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F37N
Plastic SO-14	N74F37D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

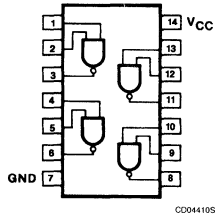
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{Y}$	Data outputs	750/106.6	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

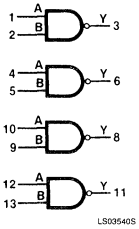
6

PIN CONFIGURATION



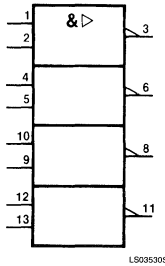
CD04410S

LOGIC SYMBOL



LS03540S

LOGIC SYMBOL (IEEE/IEC)



LS03530S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74F37			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH} = −15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.35	.50	V
			I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				5	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−1.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX		V_{IN} = GND		3	6	mA
	Supply current (total) I_{CCL}			V_{IN} = 4.5V		23	33	mA

NOTES:

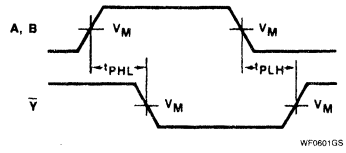
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F37					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.5	3.5	5.5	2.0	6.5	ns
t_{PHL}	A, B to $\overline{Y}$		1.5	2.5	4.5	1.5	5.0	

NOTE:
Subtract 0.2ns from minimum values for SO package.

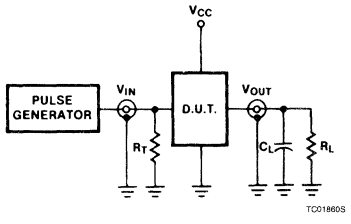
AC WAVEFORM



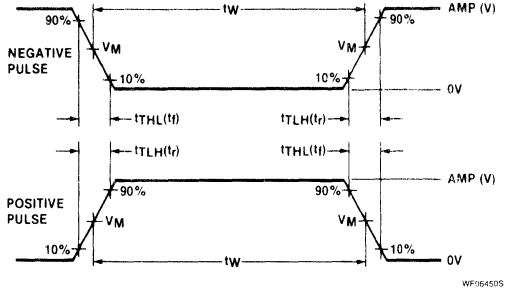
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

FAST 74F38
Buffer

Quad Two-Input NAND Buffer (Open Collector)
Product Specification

Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F38	7.0ns	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F38N
Plastic SO-14	N74F38D

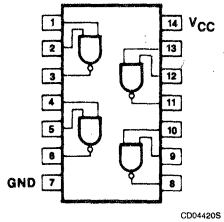
NOTES:
1. SO package is surface-mounted micro-miniature DIP available 1984.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

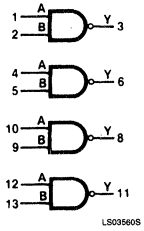
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/1.2mA
$\overline{Y}$	Outputs	OC*/106.7	OC*/64mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. *OC = Open Collector

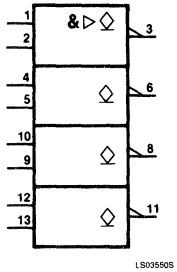
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
V_{OH}	HIGH-level output voltage			4.5	V
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F38			UNIT
						Min	Typ[2]	Max	
I_{OH}	HIGH-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.35	.50	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at others maximum input voltage		V_{CC} = MAX V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				5	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	−1.2	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN} = GND		4	7	mA
		I_{CCL}			V_{IN} = 4.5V		22	30	mA

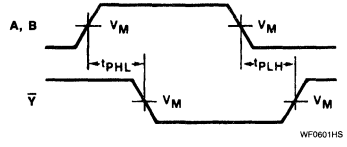
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F38					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	7.5 1.5	10 3.0	12.5 5.0	7.5 1.5	13 5.5	ns

NOTES:
1. Subtract 0.2ns from minimum values for SO package.
2. When using open collector parts, the value of the pull-up resistor greatly affects the value of the TPLH. For example, changing the specified pull-up resistor value from 500 ohms to 100 ohms will improve the TPLH up to 50% with only a slight increase in the TPHL. However, if the value of the pull-up resistor is changed, the user must make certain that the total IOL current through the resistor, plus the total IIL's of the receivers does not exceed the IOL maximum specification.

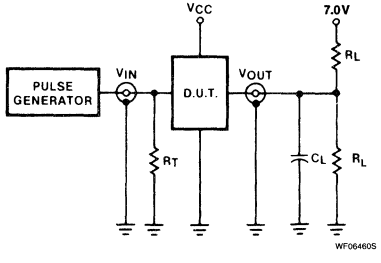
AC WAVEFORM



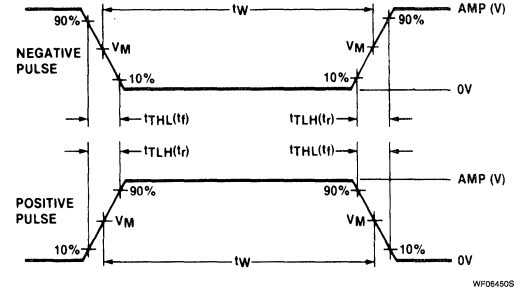
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input To Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F40
Buffer

Dual Four-Input NAND Buffer
Product Specification

Logic Products

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	X	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F40	3.5ns	6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F40N
Plastic SO-14	N74F40D

NOTES:
1. SO package is surface-mounted micro-miniature DIP available 1984.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

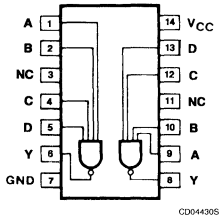
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{Y}$	Data outputs	750/106.7	15mA/64mA

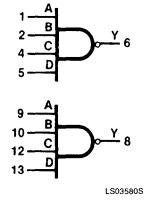
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

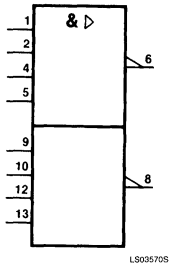
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]			74F40			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.35	.50	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				5	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	−1.2	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN} = GND		1.75	4	mA
		I_{CCL}			V_{IN} = 4.5V		11	17	mA

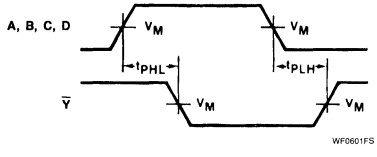
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F40					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D to $\overline{Y}$	Waveform 1	2.0 1.5	4.0 3.0	6.0 5.0	1.5 1.0	7.0 5.5	ns

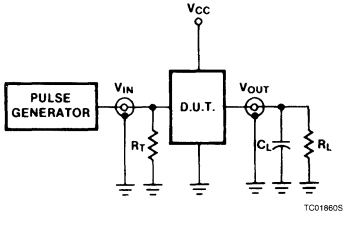
AC WAVEFORM



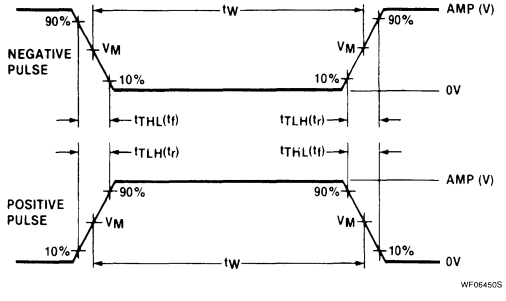
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{THL}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F51
Gate

Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-Invert Gate
Product Specification

Logic Products

FUNCTION TABLE
For 3-Input Gates

INPUTS						OUTPUT
A	B	C	D	E	F	$1\overline{Y}$
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

FUNCTION TABLE
For 2-Input Gates

INPUTS				OUTPUT
A	B	C	D	$2\overline{Y}$
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F51	3.0ns	3.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F51N
Plastic SO-14	N74F51D

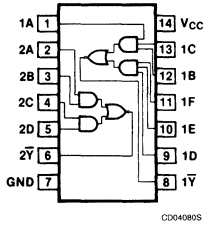
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

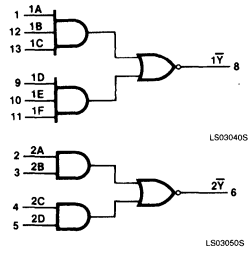
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D, E, F	Data inputs	1.0/1.0	20μA/0.6mA
$1\overline{Y}$, $2\overline{Y}$	Data outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

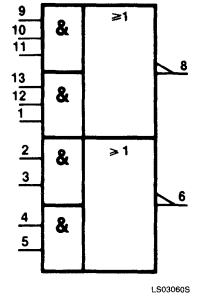
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
V_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F51			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.5	V
				±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.8	3.0	mA
		I_{CCL}		V_{IN} = 4.5V		5.5	7.5	mA

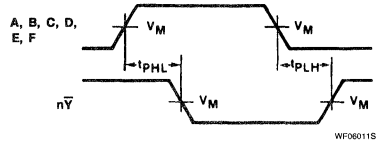
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F51					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F to $n\overline{Y}$	Waveform 1	2.0 1.0	3.5 2.5	5.5 4.0	1.5 1.0	6.5 4.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

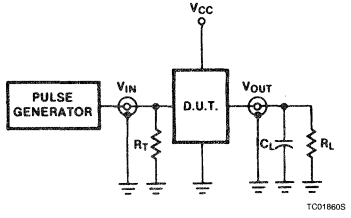
AC WAVEFORM



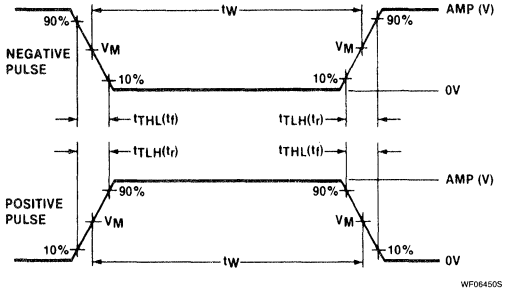
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input To Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F64
Gate

Four-Two-Three-Two-Input AND-OR-Invert Gate
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F64	4.0ns	2.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F64N
Plastic SO-14	N74F64D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS											OUTPUT
A	B	C	D	E	F	G	H	J	K	L	$\overline{Y}$
H	H	X	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

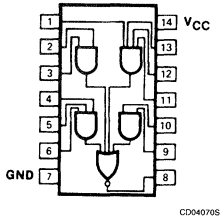
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

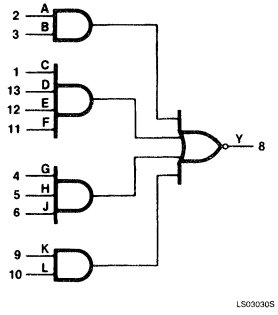
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A – L	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

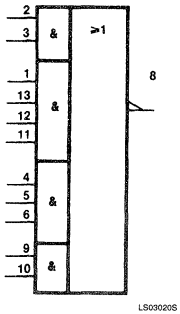
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



6

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F64			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.9	2.8	mA
	Supply current (total) I_{CCL}		V_{IN} = 4.5V		3.1	4.7	mA

NOTES:

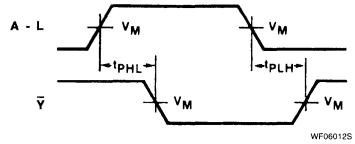
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	74F64					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A – L to $\overline{Y}$	Waveform 1	2.5 2.0	4.6 3.2	6.0 4.5	2.5 2.0	7.0 5.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

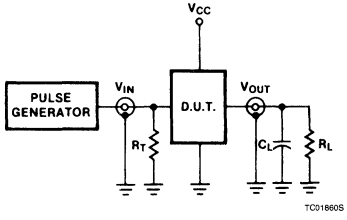
AC WAVEFORM



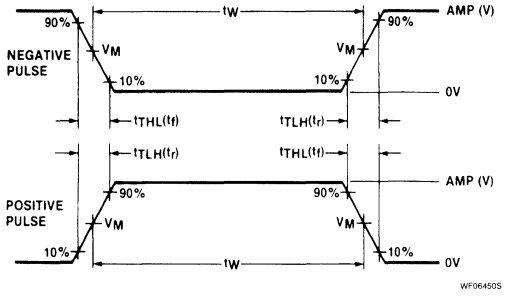
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F74
Flip-Flop

Dual D-Type Flip-Flop
Product Specification

Logic Products

DESCRIPTION

The 'F74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F74	125MHz	11.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F74N
Plastic SO-14	N74F74D

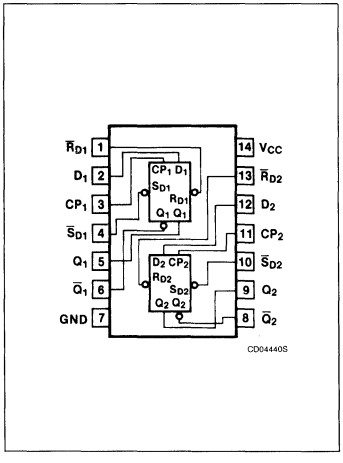
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

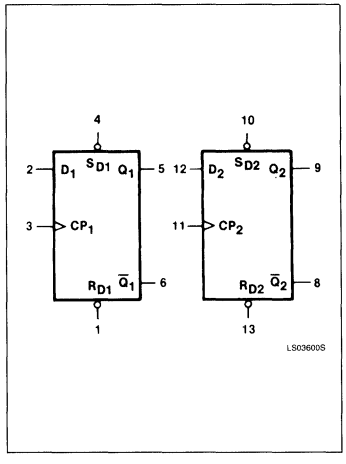
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_1, D_2	Data inputs	1.0/1.0	20μA/0.6mA
CP_1, CP_2	Clock pulse inputs (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset inputs (active LOW)	1.0/3.0	20μA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set inputs (active LOW)	1.0/3.0	20μA/1.8mA
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

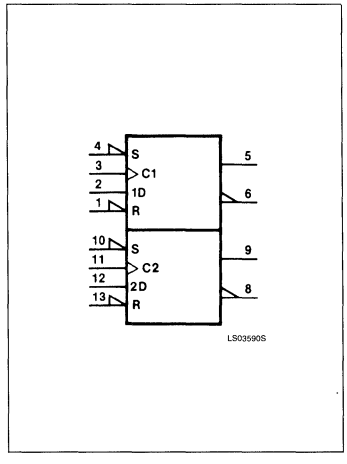
PIN CONFIGURATION



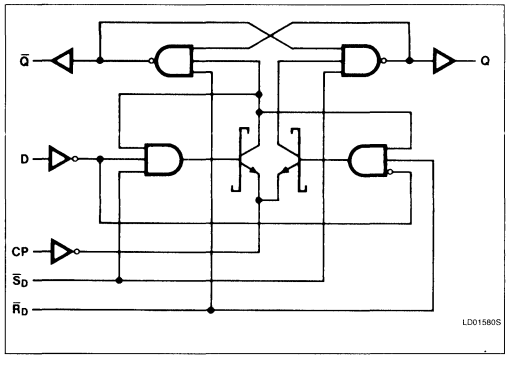
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined(1)	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
NOTE:
(1) Both outputs will be HIGH if both $\overline{S}_D$ and $\overline{R}_D$ go LOW simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F74			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	All inputs		1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	D, CP inputs		−0.4	−0.6	mA
			$\overline{R}_D$, $\overline{S}_D$ inputs		−1.3	−1.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−85	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			11.5	16	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time.For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may rise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and $\overline{Q}$ outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

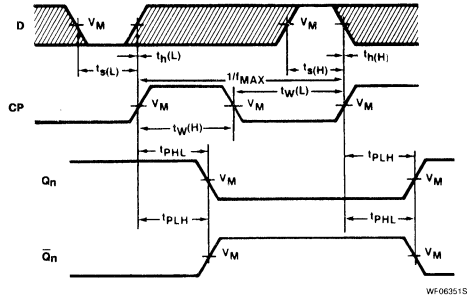
PARAMETER		TEST CONDITIONS	74F74					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	7.8 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}_n$ or $\overline{RD}_n$ to Q_n, $\overline{Q}_n$	Waveform 2	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	7.1 10.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

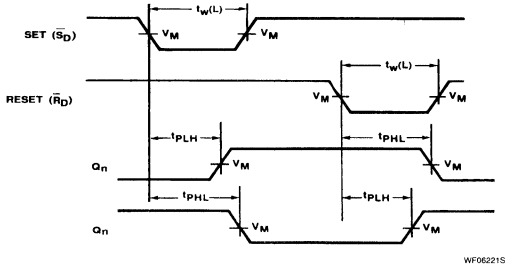
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F74					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_s (H) t_s (L)	Set-up time HIGH or LOW, D_n to CP	Waveform 1	2.0 3.0			2.0 3.0		ns
t_h (H) t_h (L)	Hold time HIGH or LOW, D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
t_W (H) t_W (L)	Clock pulse width, HIGH or LOW	Waveform 1	4.0 5.0			4.0 5.0		ns
t_W (L)	$\overline{R}_D$ or $\overline{S}_D$ pulse width, LOW	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time, $\overline{R}_D$ or $\overline{S}_D$ to CP	Waveform 3	2.0			2.0		ns

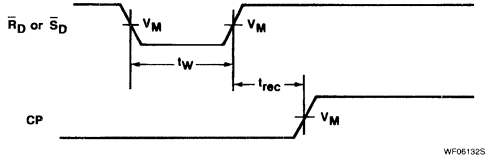
AC WAVEFORMS



Waveform 1. Clock To Output Delays, Data Set-up And Hold Times, Clock Pulse Width



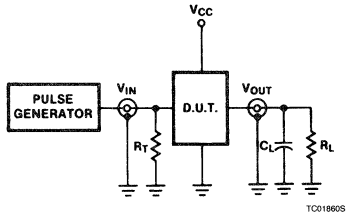
Waveform 2. Set And Reset To Output Delays, Set And Reset Pulse Widths



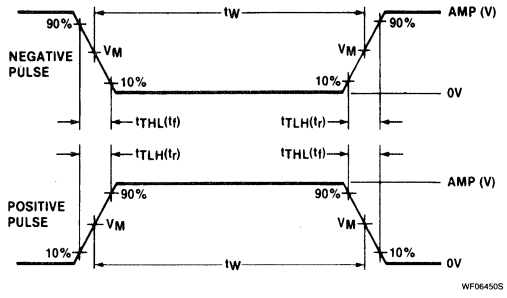
Waveform 3. Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F85
Comparator

4-Bit Magnitude Comparator
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Magnitude comparison of any binary words**
- **Serial or parallel expansion without extra gating**

DESCRIPTION

The 'F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted ($A_0 \rightarrow A_3$) and ($B_0 \rightarrow B_3$), where A_3 and B_3 are the most significant bits.

The operation of the 'F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F85N
Plastic SOL-16	N74F85D

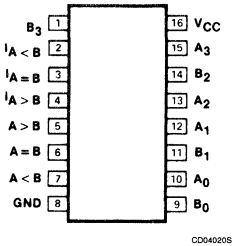
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

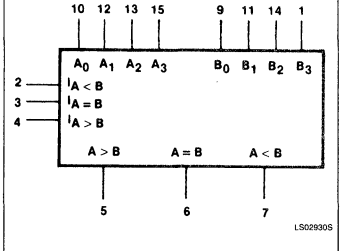
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	Comparing Inputs	1.0/0.033	20μA/20μA
$B_0 - B_3$	Comparing Inputs	1.0/0.033	20μA/20μA
$I_{A<B}$, $I_{A=B}$ $I_{A>B}$	Expansion Inputs	1.0/0.033	20μA/20μA
A > B, A = B A < B	Data Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

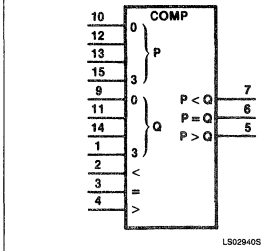
PIN CONFIGURATION



LOGIC SYMBOL



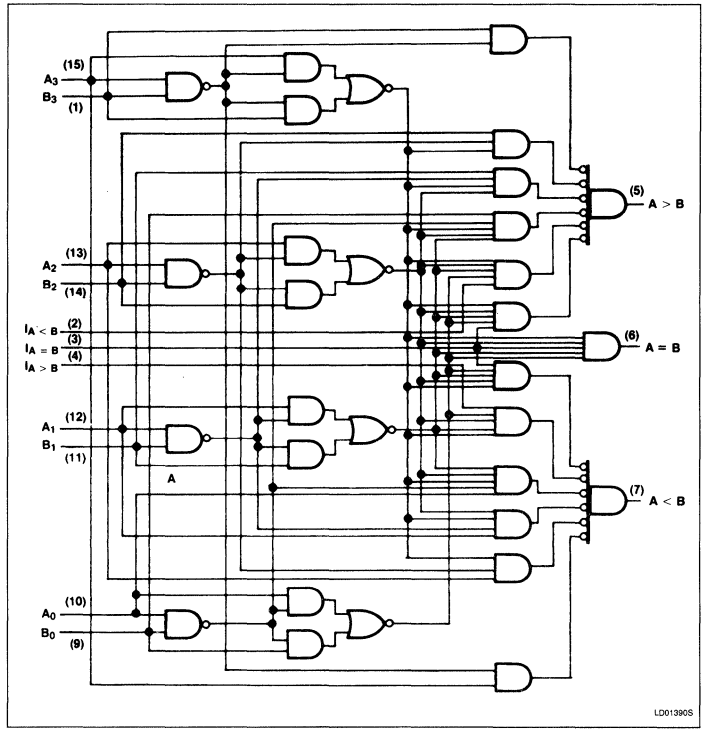
LOGIC SYMBOL (IEEE/IEC)



Comparator | FAST 74F85

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A > B, A = B and A < B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = LOW, $I_{A=B}$ = HIGH, and $I_{A<B}$ = LOW.

LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A > B	A < B	A = B
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

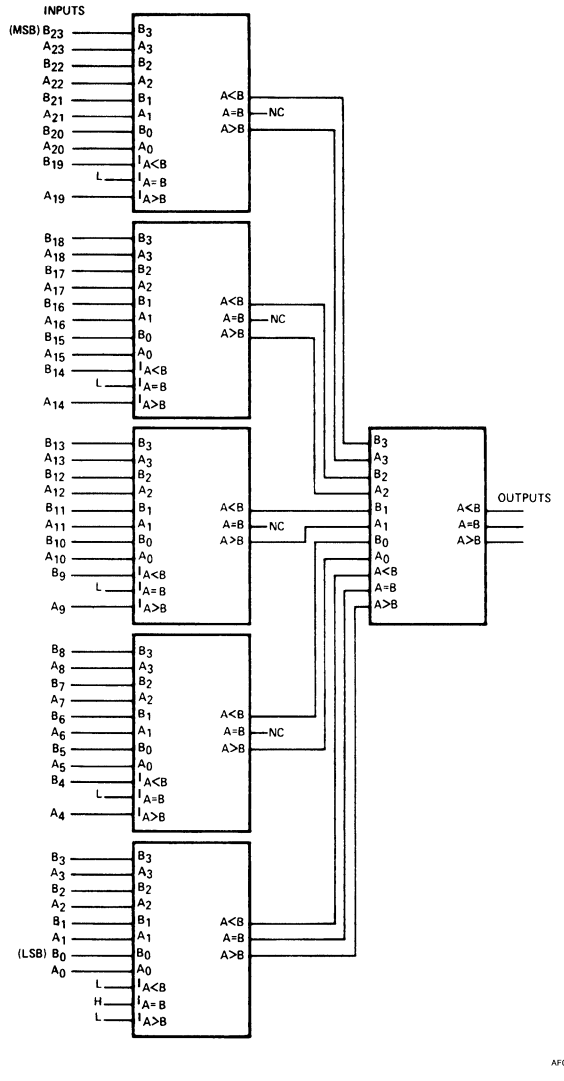


Figure 1. Comparison Of Two 24-Bit Words

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ LOW. The 'F85 can be used as a 5-bit comparator only when the outputs are used to drive the ($A_0 - A_3$) and ($B_0 - B_3$) inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS 74F
1 – 4 Bits	1	12ns
5 – 25 Bits	2 – 6	22ns
25 – 120 Bits	8 – 31	34ns

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F85 Min	74F85 Typ[2]	74F85 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			36	50	mA
		I_{CCL}				40	54	mA

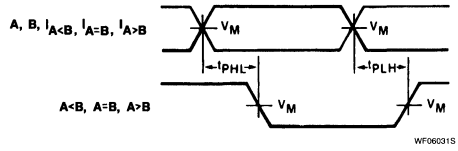
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open, A = B grounded, and all other inputs grounded.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F85 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F85 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output	Waveform 1 3 logic levels	6.0 7.0	8.5 9.5	11.0 14.0	5.5 6.5	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 1 4 logic levels	6.5 7.0	9.0 9.5	11.5 14.0	6.0 6.5	14.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A > B output	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	7.5 9.0	2.5 2.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 1 2 logic levels	2.5 3.5	4.5 7.5	7.0 10.0	2.0 2.5	9.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A < B output	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	8.0 9.0	3.0 2.0	9.5 9.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

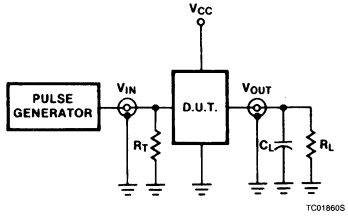
AC WAVEFORM



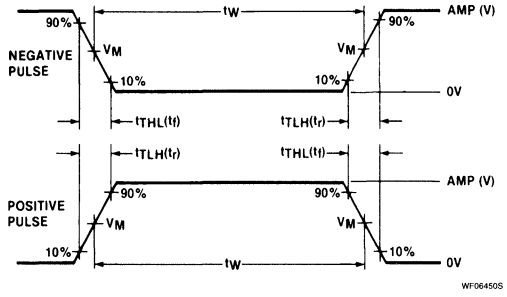
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input To Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F86
Gate

Quad Two-Input Exclusive-OR Gate
Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F86	4.3ns	16.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F86N
Plastic SO-14	N74F86D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

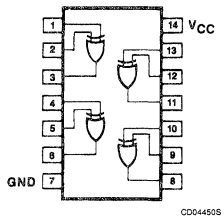
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

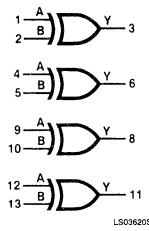
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

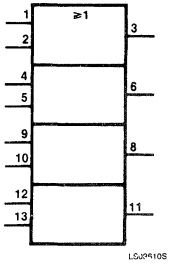
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F86			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_{IN} = GND		15	23	mA
	Supply current (total) I_{CCL}		V_{IN} = 4.5V		18	28	mA

NOTES:

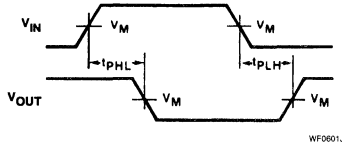
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App note 202 "Testing and Specifying FAST logic.")

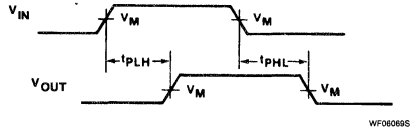
PARAMETER		TEST CONDITIONS	74F86					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to Y	Other input LOW Waveform 2	3.0 3.0	4.0 4.2	5.5 5.5	3.0 3.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B to Y	Other input HIGH Waveform 1	3.5 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.0 7.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



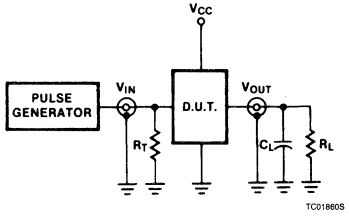
Waveform 1. For Inverting Outputs



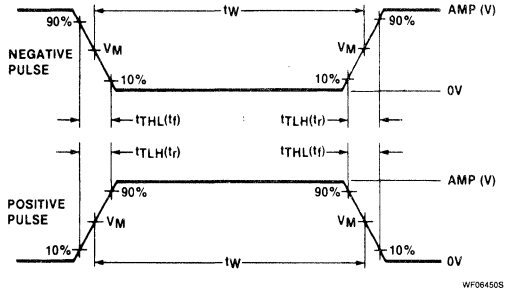
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F109
Flip-Flop

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop
Product Specification

Logic Products

DESCRIPTION

The 'F109 is a dual positive edge-triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs, and complementary $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-LOW inputs and operate independently of the Clock input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition of the positive-going pulse.

The J and $\overline{K}$ inputs must be stable just one set-up time prior to the LOW-to-HIGH transition of the Clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F109	125MHz	12.3mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F109N
Plastic SO-16	N74F109D

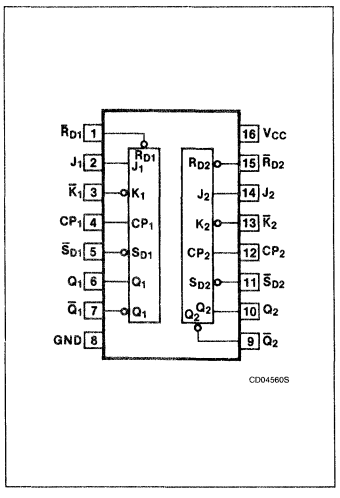
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

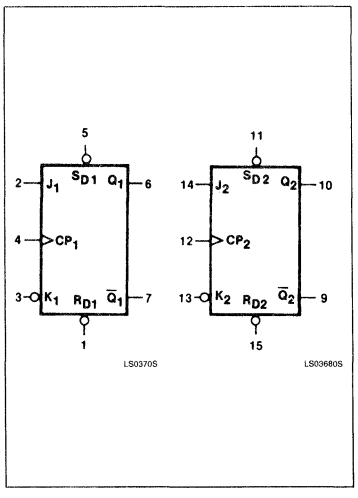
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data inputs	1.0/1.0	20μA/0.6mA
CP_1, CP_2	Clock pulse inputs (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset inputs (active LOW)	1.0/3.0	20μA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set inputs (active LOW)	1.0/3.0	20μA/1.8mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

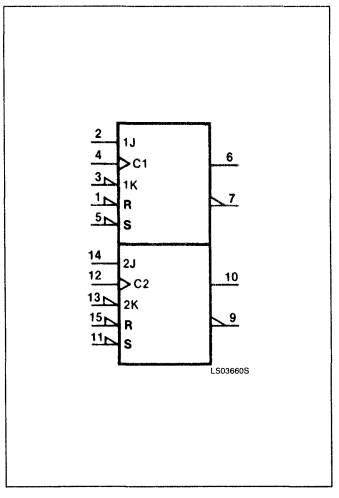
PIN CONFIGURATION



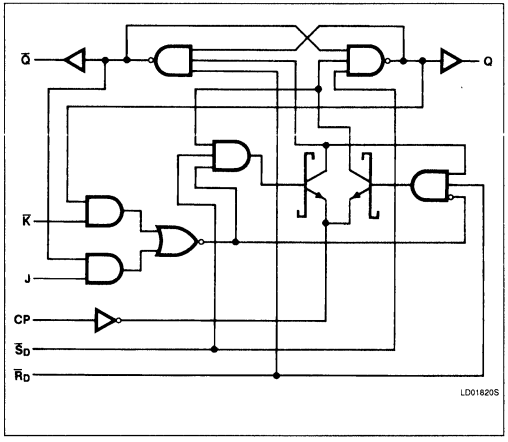
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	↑	l	l	L	H
Load "1" (Set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH Clock transition.
↑ = LOW-to-HIGH Clock transition.
NOTE:
Both outputs will be HIGH if both $\overline{S}_D$ and $\overline{R}_D$ go LOW simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F109 Min	74F109 Typ[2]	74F109 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	J, $\overline{K}$, CP inputs	V_{CC} = MAX, V_I = 2.7V			1	20	μA
		$\overline{S}_D$, $\overline{R}_D$ inputs				1	20	μA
I_{IL}	LOW-level input current	J, $\overline{K}$, CP inputs	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
		$\overline{S}_D$, $\overline{R}_D$ inputs				−1.3	−1.8	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−85	−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			12.3	17	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

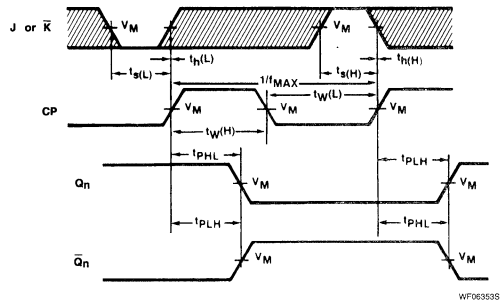
PARAMETER		TEST CONDITIONS	74F109 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F109 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	90	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	8.0 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to Q_n, $\overline{Q}_n$	Waveform 2	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	8.0 10.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

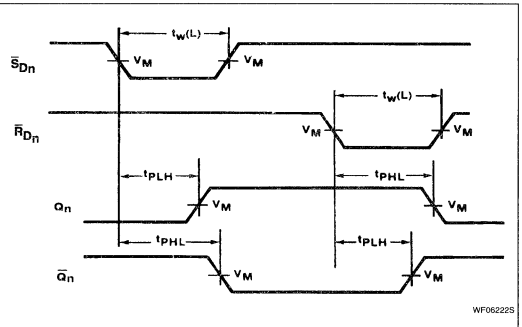
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F109					UNIT
			$T_A = +25°C$, $V_{CC} = 5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time HIGH or LOW, J or $\overline{K}$ to CP	Waveform 1	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW, J or $\overline{K}$ to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_W(H)$ $t_W(L)$	Clock pulse width, HIGH or LOW	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_W(L)$	Set or Reset pulse width, LOW	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time, Set or Reset to clock	Waveform 3	2.0			2.0		ns

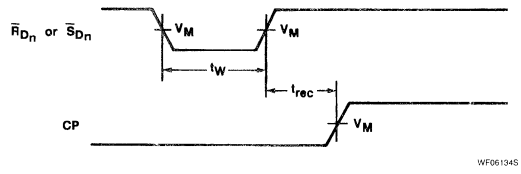
AC WAVEFORMS



Waveform 1. Clock To Output Delays, Data Set-up And Hold Times, Clock Pulse Width



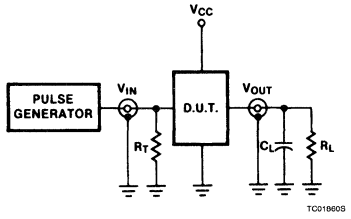
Waveform 2. Set And Reset To Output Delays, Set And Reset Pulse Widths



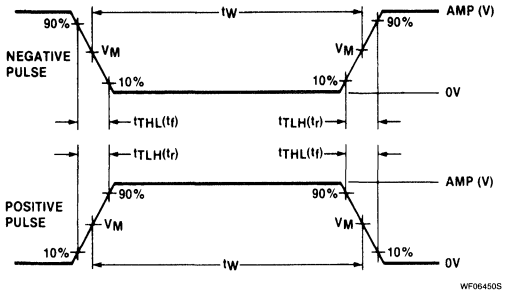
Waveform 3. Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F112
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop
Preliminary Specification

Logic Products

DESCRIPTION

The 'F112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when LOW, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum set-up and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F112	130MHz	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F112N
Plastic SO-14	N74F112D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1, J_2, K_1, K_2	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}_1$, $\overline{CP}_2$	Clock pulse inputs (active falling edge)	1.0/4.0	20μA/2.4mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset input (active LOW)	1.0/5	20μA/3.0mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set input (active LOW)	1.0/5	20μA/3.0mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

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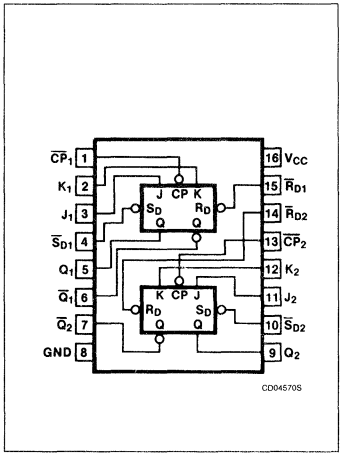
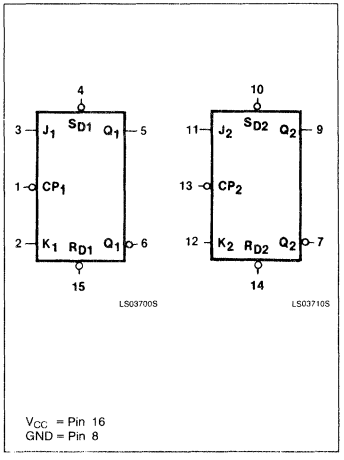
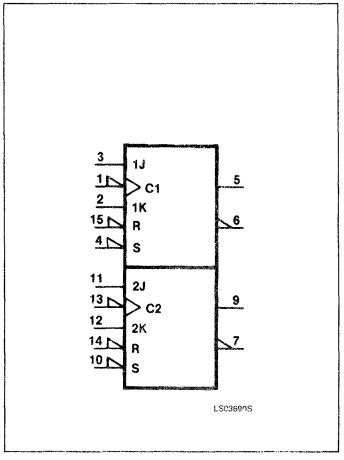
PIN CONFIGURATION



LOGIC SYMBOL

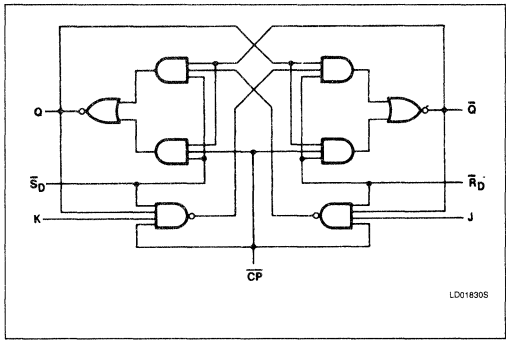


LOGIC SYMBOL (IEEE/IEC)



Flip-Flop | FAST 74F112

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (reset)	H	H	↓	l	h	L	H
Load "1" (set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
↓ = HIGH-to-LOW Clock transition.
NOTE:
Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1.0	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F112 Min	74F112 Typ[2]	74F112 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	J_n, K_n	V_{CC} = MAX, V_I = 7.0V				100	μA
		$\overline{R}_{Dn}$, $\overline{S}_{Dn}$					100	μA
		$\overline{CP}_n$					100	μA
I_{IH}	HIGH-level input current	J_n, K_n	V_{CC} = MAX, V_I = 2.7V				20	μA
		$\overline{R}_{Dn}$, $\overline{S}_{Dn}$					20	μA
		$\overline{CP}_n$					20	μA
I_{IL}	LOW-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{R}_{Dn}$, $\overline{S}_{Dn}$					-3.0	mA
		$\overline{CP}_n$					-2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			12	19	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F112 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F112 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum Clock frequency	Waveform 1	110	130		100		MHz
t_{PLH}	Propagation delay $\overline{CP}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	2.0	5.0	6.5	2.0	7.5	ns
t_{PHL}			2.0	5.0	6.5	2.0	7.5	
t_{PLH}	Propagation delay S_{Dn} or R_{Dn} to Q_n, $\overline{Q}_n$	Waveform 2	2.0	4.5	6.5	2.0	7.5	ns
t_{PHL}			2.0	4.5	6.5	2.0	7.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

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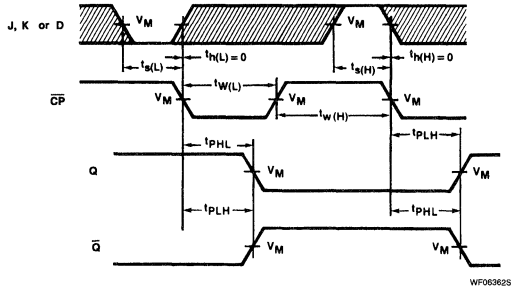
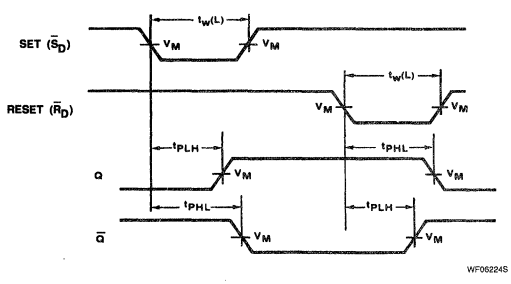
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F112					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	Waveform 1	4.0 3.0			5.0 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	Waveform 1	0 0			0 0		ns
$t_W(H)$ $t_w(L)$	$\overline{CP}_n$ pulse width	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$	RD_n or SD_n pulse width	Waveform 2	4.5			5.0		ns

AC WAVEFORMS



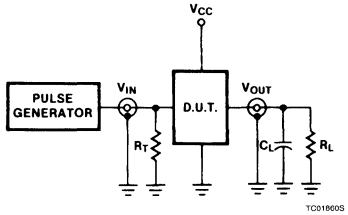
Waveform 1. Clock To Output Delays, Data Set-up And Hold Times, Clock Pulse Width



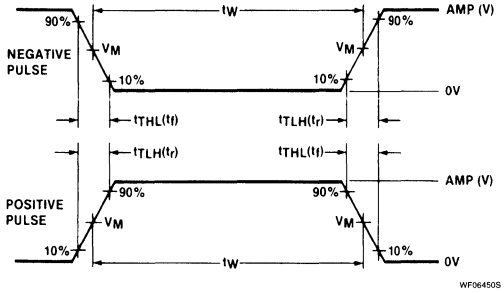
Waveform 2. Set And Reset To Output Delays, Set And Reset Pulse Widths

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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Signetics

FAST 74F113
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop Without Reset
Preliminary Specification

Logic Products

DESCRIPTION

The 'F113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set ($\overline{S}_D$) input, when LOW, forces the outputs to the steady state levels as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum set-up and hold times are observed. Output state changes are intitiated by the HIGH-to-LOW transition of $\overline{CP}$.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F113	125MHz	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F113N
Plastic SO-14	N74F113D

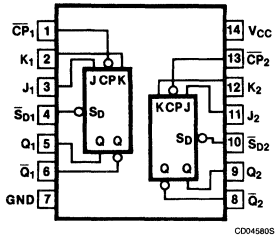
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

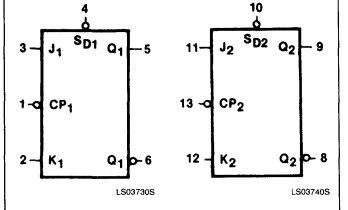
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1, J_2, K_1, K_2	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}_1$, $\overline{CP}_2$	Clock pulse inputs (active falling edge)	1.0/4.0	20μA/2.4mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct set inputs (active low)	1.0/5	20μA/3.0mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

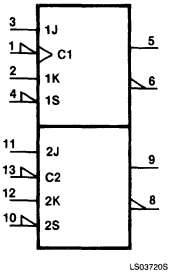


LOGIC SYMBOL

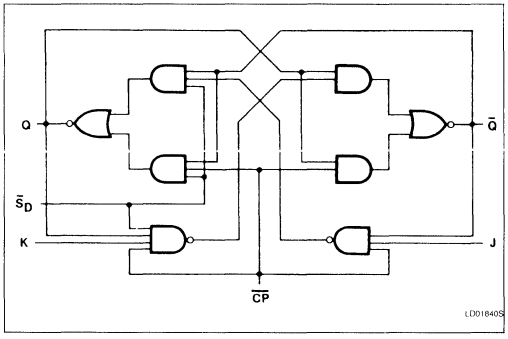


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
↓ = HIGH-to-LOW Clock transition.
Asynchronous input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F113 Min	74F113 Typ[2]	74F113 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	J_n, K_n	V_{CC} = MAX, V_I = 7.0V				100	μA
		$\overline{S}_{Dn}$					100	μA
		$\overline{CP}_n$					100	μA
I_{IH}	HIGH-level input current	J_n, K_n	V_{CC} = MAX, V_I = 2.7V				20	μA
		$\overline{S}_{Dn}$					20	μA
		$\overline{CP}_n$					20	μA
I_{IL}	LOW-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		$\overline{S}_{Dn}$					−3.0	mA
		$\overline{CP}_n$					−2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			12	19	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

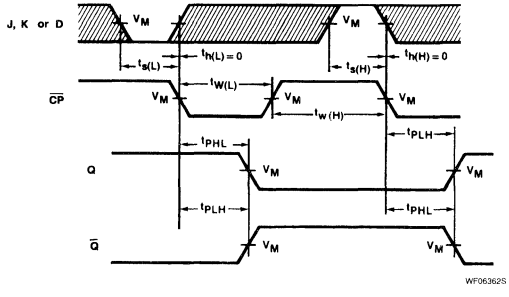
PARAMETER		TEST CONDITIONS	74F113 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F113 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	110	125		100		MHz
t_{PLH}	Propagation delay $\overline{CP}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	2.0	4.0	6.0	2.0	7.0	ns
t_{PHL}			2.0	4.0	6.0	2.0	7.0	
t_{PLH}	Propagation delay S_{Dn} to Q_n, $\overline{Q}_n$	Waveform 2	2.0	4.5	6.5	2.0	7.5	ns
t_{PHL}			2.0	4.5	6.5	2.0	7.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

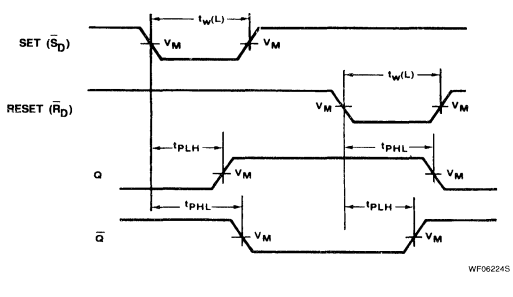
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F113					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	Waveform 1	4.0 3.0			5.0 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	Waveform 1	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ pulse width	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$	SD_n pulse width	Waveform 2	4.5			5.0		ns

AC WAVEFORMS



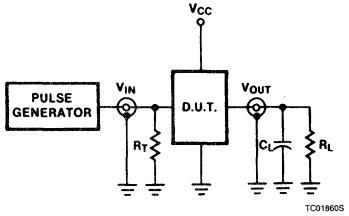
Waveform 1. Clock To Output Delays, Data Set-up And Hold Times, Clock Pulse Width



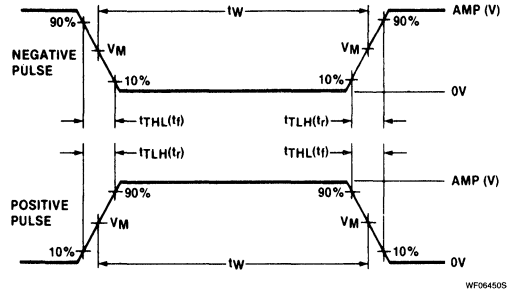
Waveform 2. Set And Reset To Output Delays, Set And Reset Pulse Widths

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F114
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop (With Common Clock and Reset)
Preliminary Specification

DESCRIPTION

The 'F114 is a Dual JK Negative Edge-Triggered Flip-Flop featuring individual J, K, and Set inputs and common Clock and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when LOW, set or reset the outputs as shown in the Truth Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Truth Table as long as minimum set-up and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F114	125	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F114N
Plastic SO-14	N74F114D

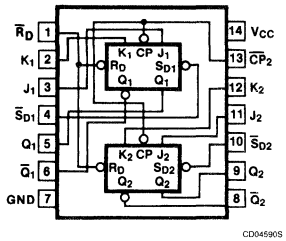
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

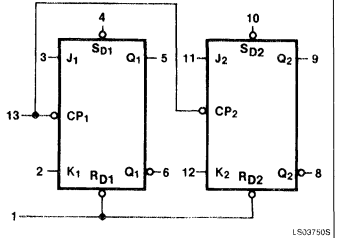
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1, J_2, K_1, K_2	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock pulse input (active falling edge)	1.0/4.0	20μA/2.4mA
$\overline{R}_D$	Direct clear input (active LOW)	1.0/5.0	20μA/3.0mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct set inputs (active LOW)	1.0/5.0	20μA/3.0mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

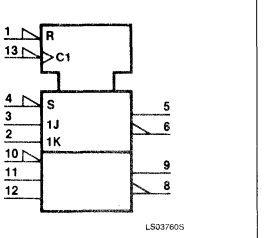
PIN CONFIGURATION



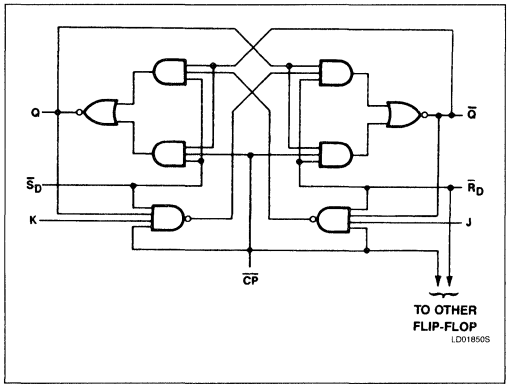
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
Asynchronous inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F114 Min	74F114 Typ[2]	74F114 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	J_n, K_n	V_{CC} = MAX, V_I = 7.0V				100	μA
		$\overline{R}_D$, $\overline{S}_{Dn}$					100	μA
		$\overline{CP}$					100	μA
I_{IH}	HIGH-level input current	J_n, K_n	V_{CC} = MAX, V_I = 2.7V				20	μA
		$\overline{R}_D$, $\overline{S}_{Dn}$					20	μA
		$\overline{CP}$					20	μA
I_{IL}	LOW-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		$\overline{R}_D$, $\overline{S}_{Dn}$					−3.0	mA
		$\overline{CP}$					−2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			12	19	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

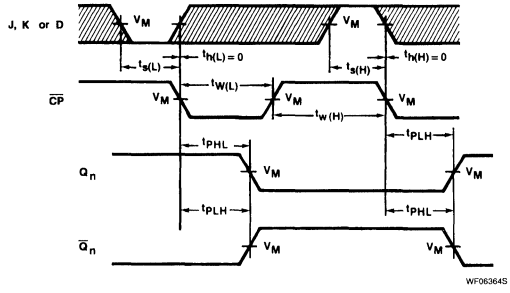
PARAMETER		TEST CONDITIONS	74F114 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F114 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	110	125		90		MHz
t_{PLH}	Propagation delay $\overline{CP}$ to Q_n, $\overline{Q}_n$	Waveform 1	3.0	5.0	6.5	3.0	7.5	ns
t_{PHL}			3.0	5.5	7.5	3.0	8.5	
t_{PLH}	Propagation delay SD_n or RD_n to Q_n, $\overline{Q}_n$	Waveform 2	3.0	4.5	6.5	3.0	7.5	ns
t_{PHL}			3.0	4.5	6.5	3.0	7.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

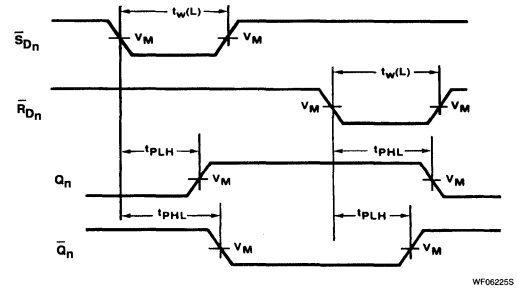
AC SET-UP REQUIREMENTS

PARAMETER	TEST CONDITIONS	74F114					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
$t_s(H)$ Set-up time, HIGH or LOW $t_s(L)$ J_n or K_n to $\overline{CP}_n$	Waveform 1	4.0 3.0			5.0 3.5		ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ J_n or K_n to $\overline{CP}_n$	Waveform 1	0 0			0 0		ns
$t_W(H)$ $t_w(L)$ $\overline{CP}_n$ pulse width	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$ SD_n or RD pulse width	Waveform 2	4.5			5.0		ns

AC WAVEFORMS



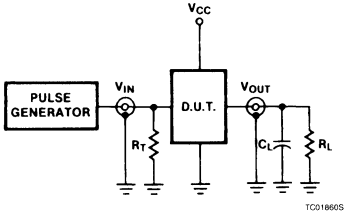
Waveform 1. Clock To Output Delays, Data Set-up And Hold Times, Clock Pulse Width



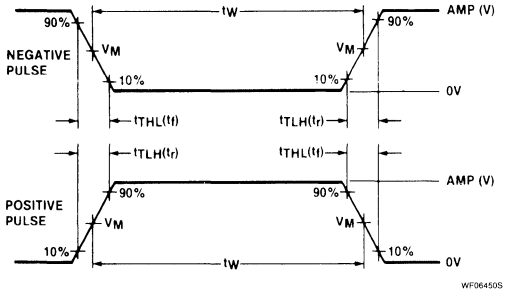
Waveform 2. Set And Reset To Output Delays, Set And Reset Pulse Widths

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F125, 74F126
Buffer

Quad Buffers (3-State)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F125	5.0ns	23mA
74F126	5.0ns	26mA

FUNCTION TABLE 'F125

INPUTS		OUTPUT
$\overline{C}$	A	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE 'F126

INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F125N, N74F126N
Plastic SO-14	N74F125D, N74F126D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

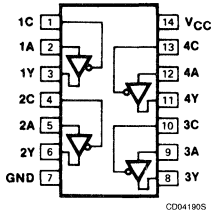
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
1A – 4A	Data inputs	1.0/0.033	20μA/20μA
$\overline{1C}$ – $\overline{4C}$	3-State output enable input (active LOW) 'F125	1.0/0.033	20μA/20μA
1C – 4C	3-State output enable input (active HIGH) 'F126	1.0/0.033	20μA/20μA
1Y – 4Y	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

'F125



LOGIC SYMBOL

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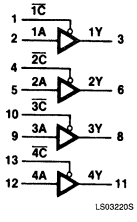
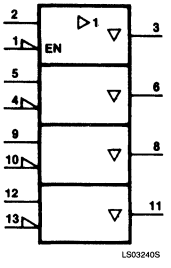


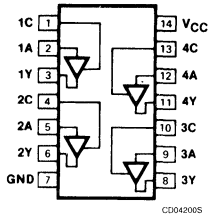
LOGIC SYMBOL (IEEE/IEC)

'F125



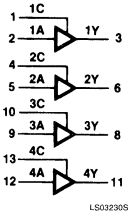
PIN CONFIGURATION

'F126



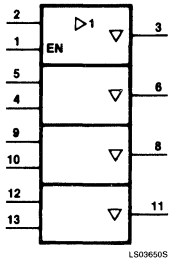
LOGIC SYMBOL

'F126



LOGIC SYMBOL (IEEE/IEC)

'F126



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F125, 74F126			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.35	.50	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100	−150	−225	mA
I_{CC}	Supply current (total)	'F125	I_{CCH}	V_{CC} = MAX	$\overline{nC}$ = GND, nA = 4.5V		17	24	mA
			I_{CCL}		$\overline{nC}$ = nA = GND		28	40	mA
			I_{CCZ}		$\overline{nC}$ = nA = 4.5V		25	35	mA
		'F126	I_{CCH}		nC = nA = 4.5V		20	30	mA
			I_{CCL}		nC = 4.5V, nA = GND		32	48	mA
			I_{CCZ}		nC = GND, nA = 4.5V		26	39	mA

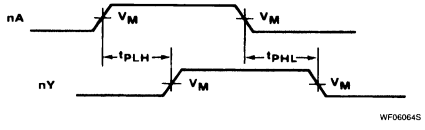
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

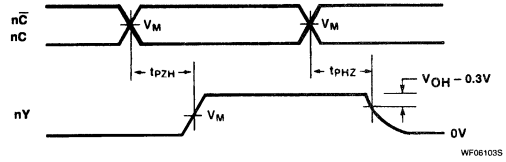
PARAMETER			TEST CONDITIONS	74F125, 74F126					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA to nY	'F125	Waveform 1	2.0 3.0	4.0 5.5	6.0 7.5	2.0 3.0	6.5 8.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level		Waveform 2 Waveform 3	3.5 4.0	5.5 6.0	7.5 8.0	3.5 4.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level		Waveform 2 Waveform 3	1.5 1.5	3.5 3.5	5.0 5.5	1.5 1.5	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay nA to nY	'F126	Waveform 1	2.0 3.0	4.0 5.5	6.5 8.0	2.0 3.0	7.0 8.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level		Waveform 2 Waveform 3	4.0 4.0	6.0 6.0	7.5 8.0	3.5 3.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level		Waveform 2 Waveform 3	2.0 3.0	4.5 5.5	6.5 7.5	2.0 3.0	7.5 8.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

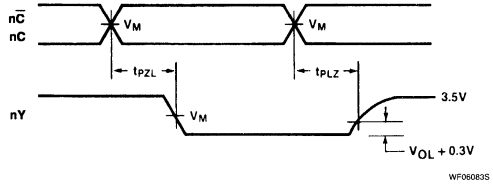
AC WAVEFORMS



Waveform 1. Propagation Delay For Input To Output



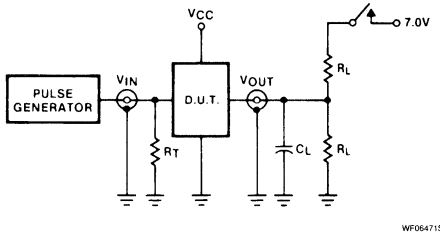
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



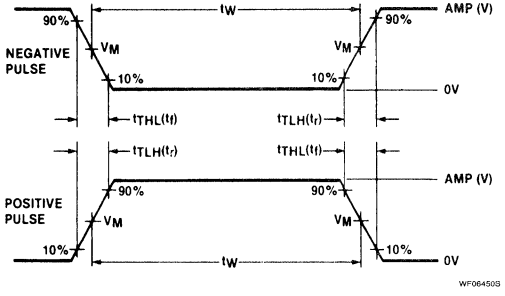
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F132
Schmitt Trigger

Quad 2-Input NAND Schmitt Trigger
Product Specification

Logic Products

DESCRIPTION

The 'F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F132	6.3ns	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F132N
Plastic SO-14	N74F132D

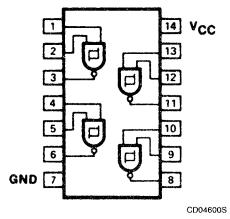
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

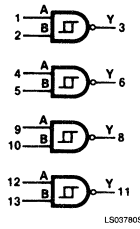
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

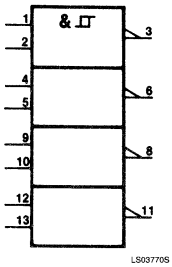
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

6

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F132			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold		V_{CC} = 5.0V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold		V_{CC} = 5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, $V_I = V_{T-MIN}$, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, $V_I = V_{T+MAX}$, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_{T+}	Input current at positive-going threshold		V_{CC} = 5.0V, $V_I = V_{T+}$			0.0		μA
I_{T-}	Input current at negative-going threshold		V_{CC} = 5.0V, $V_I = V_{T-}$			−350		μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−120	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		8.5	12	mA
		I_{CCL}		V_{IN} = 4.5V		13.0	19.5	mA

NOTES:

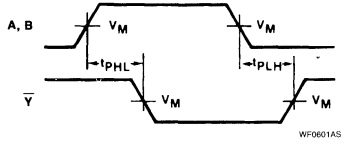
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F132					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	4.0	5.5	7.0	3.5	8.5	ns
t_{PHL}	A, B to $\overline{Y}$		5.5	7.0	8.5	5	8.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

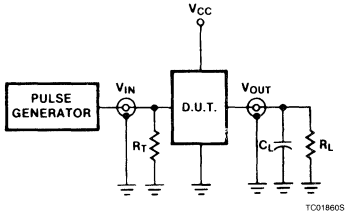
AC WAVEFORM



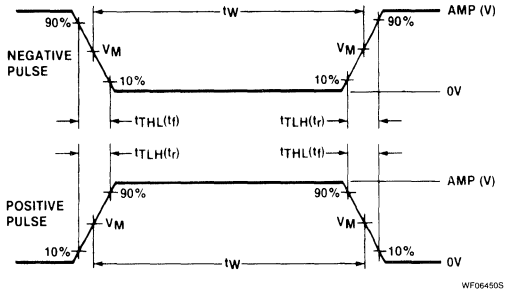
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F138
Decoder/Demultiplexer

1-Of-8 Decoder/Demultiplexer
Product Specification

Logic Products

FEATURES

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **High speed replacement for Intel 3205**

DESCRIPTION

The 'F138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\overline{O}_0 - \overline{O}_7$). The device features three Enable inputs; two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'F138's and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F138	5.8ns	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F138N
Plastic SO-16	N74F138D

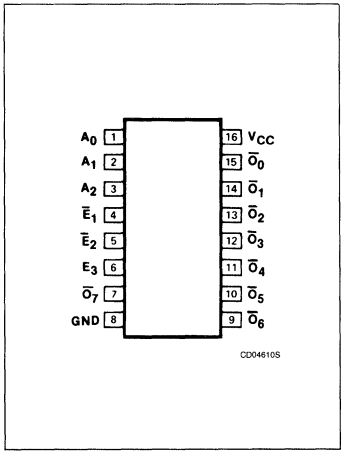
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

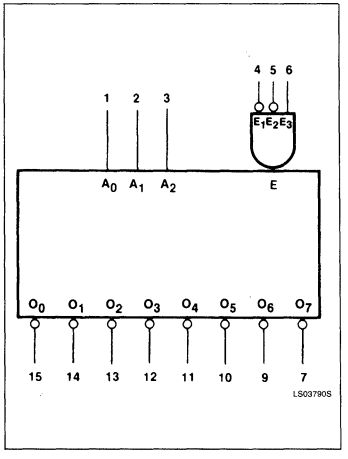
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_2$	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_1 - \overline{E}_2$	Enable inputs (active LOW)	1.0/1.0	20μA/0.6mA
E_3	Enable input (active HIGH)	1.0/1.0	20μA/0.6mA
$\overline{O}_0 - \overline{O}_7$	Outputs (active LOW)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

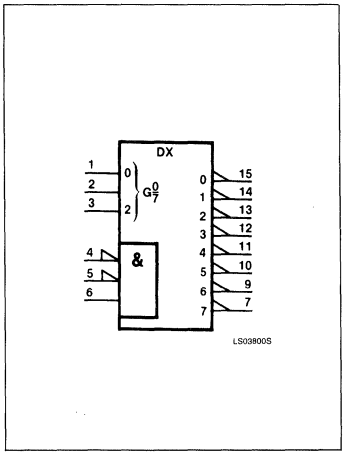
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

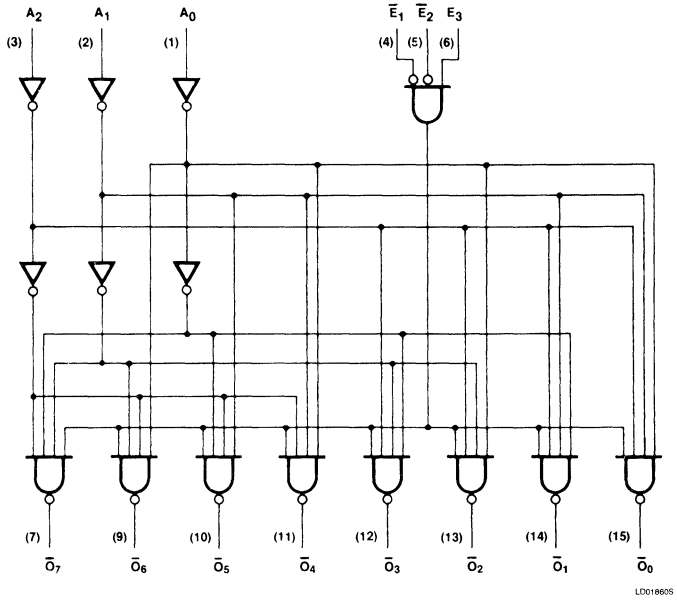


FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

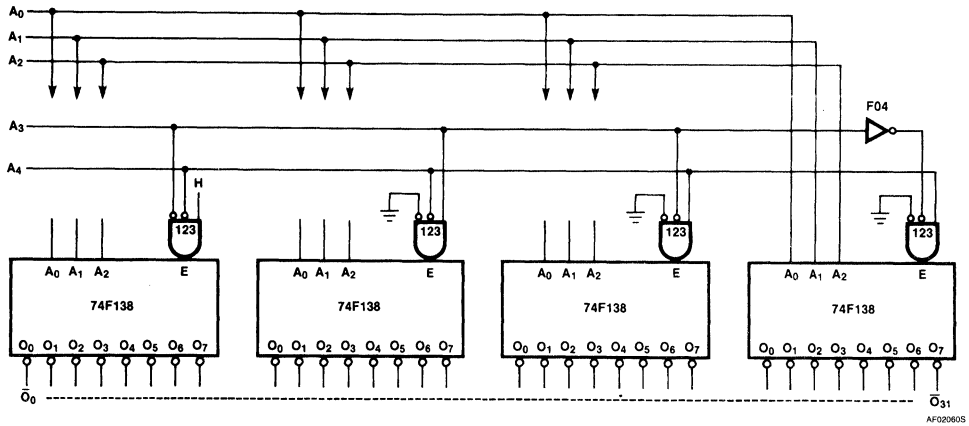
(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER	TEST CONDITIONS[1]		74F138			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			13	20	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs = 4.5V.

APPLICATION



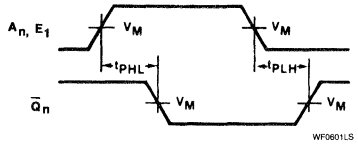
Expansion To 1-of-32 Decoding

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

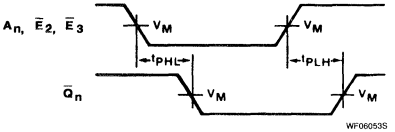
PARAMETER		TEST CONDITIONS	74F138					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output A_n to $\overline{Q}_n$	Waveforms 1 and 2	3.5 4.0	5.6 6.1	7.0 8.0	3.5 4.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{Q}_n$	Waveform 2	3.5 3.0	6.4 5.3	7.0 7.0	3.5 3.0	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to $\overline{Q}_n$	Waveform 1	4.0 3.5	8.2 5.6	8.0 7.5	4.0 3.5	9.0 8.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



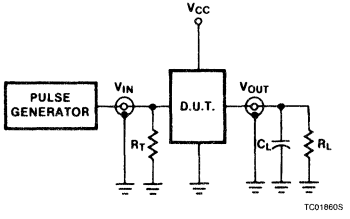
Waveform 1. For Inverting Outputs



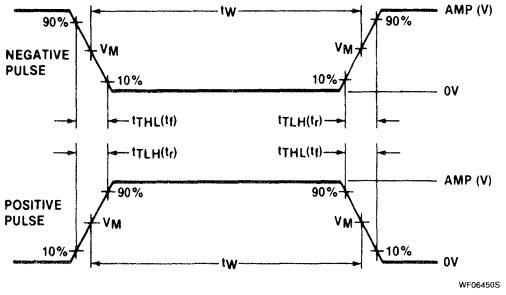
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F139
Decoder/Demultiplexer

Dual 1-of-4 Decoder/Demultiplexer
Product Specification

Logic Products

FEATURES
- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**

DESCRIPTION
The 'F139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0, A_1) and providing four mutually exclusive active LOW outputs ($\overline{Q}_{0n} - \overline{Q}_{3n}$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH, every output is forced HIGH. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F139	5.3ns	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F139N
Plastic SO-16	N74F139D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

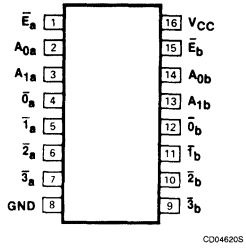
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{na}, A_{nb}	Address Inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_{0a} - \overline{Q}_{3a}$, $\overline{Q}_{0b} - \overline{Q}_{3b}$	Outputs	50/33	1.0mA/20mA

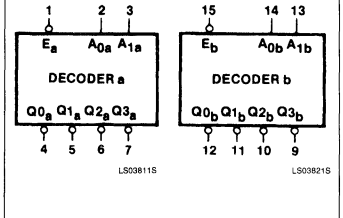
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

PIN CONFIGURATION

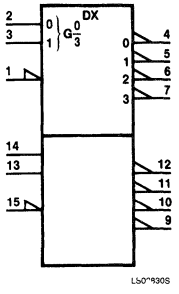


LOGIC SYMBOL

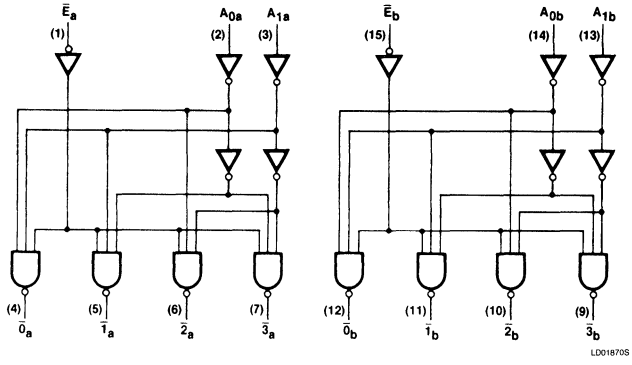


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F139			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			13	20	mA

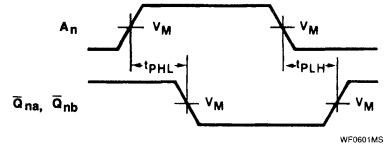
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs = 4.5V.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

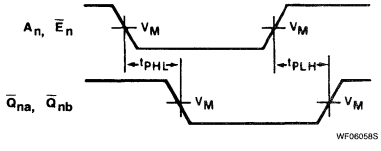
PARAMETER		TEST CONDITIONS	74F139					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_0 or A_1 to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveforms 1 and 2	3.5 4.0	5.3 6.1	7.0 8.0	3.0 4.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveform 2	3.5 3.0	5.4 4.7	7.0 6.5	3.5 3.0	8.0 7.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



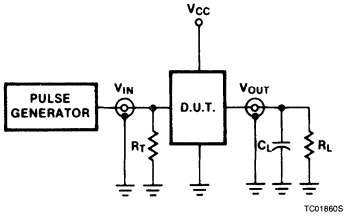
Waveform 1. For Inverting Outputs



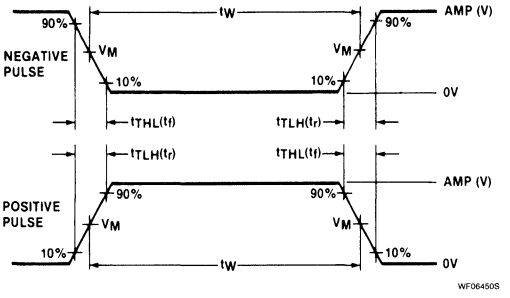
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F148
Encoder

8-Input Priority Encoder
Product Specification

Logic Products

FEATURES

- **Code conversions**
- **Multi-channel D/A converter**
- **Decimal-to-BCD converter**
- **Cascading for priority encoding of "N" bits**
- **Input enable capability**
- **Priority encoding — automatic selection of highest priority input line**
- **Output enable — active LOW when all inputs HIGH**
- **Group signal output — active when any input is LOW**

DESCRIPTION

The 'F148 8-input priority encoder accepts data from eight active-LOW inputs and provides a binary representation on the three active-LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}_7$ having the highest priority.

A HIGH on the Enable Input (EI) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F148	6.0ns	23mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F148N
Plastic SO-16	N74F148D

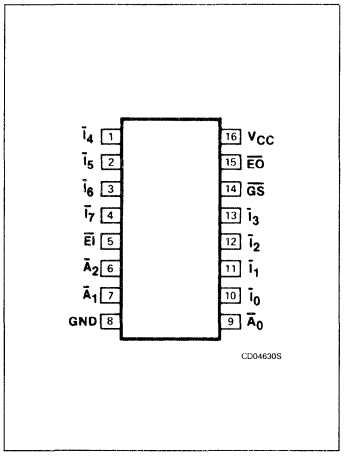
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

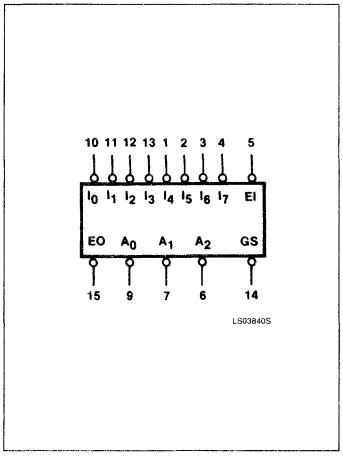
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{I}_0 - \overline{I}_7$	Priority inputs (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{I}_c$	Priority input (active LOW)	1.0/2.0	20μA/1.2m A
$\overline{EI}$	Enable input (active LOW)	1.0/2.0	20μA/1.2mA
$\overline{EO}$	Enable output (active LOW)	50/33	1.0mA/20mA
$\overline{GS}$	Group select output (active LOW)	50/33	1.0mA/20mA
$\overline{A}_0 - \overline{A}_2$	Address outputs (active LOW)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

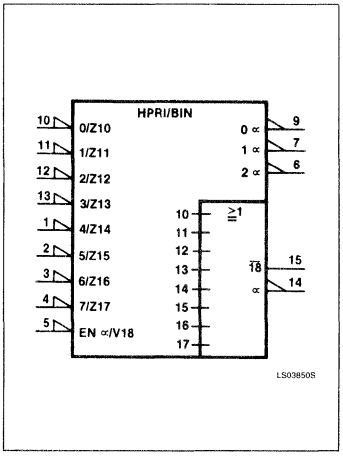
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Encoder | FAST 74F148

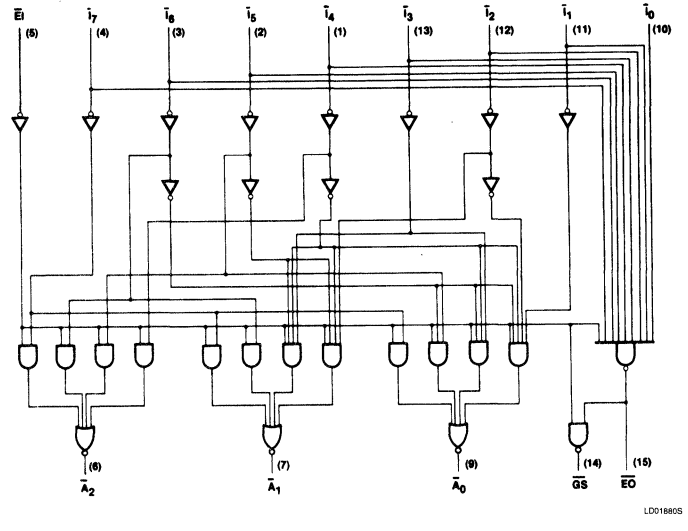
A Group Signal ($\overline{GS}$) output and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active-LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active-LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active-HIGH when the Enable Input is HIGH.

FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F148			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	$\bar{I}_0$, $\overline{EI}$	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
		$\bar{I}_1 - \bar{I}_7$				−0.8	−1.2	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			23	35	mA

NOTES:

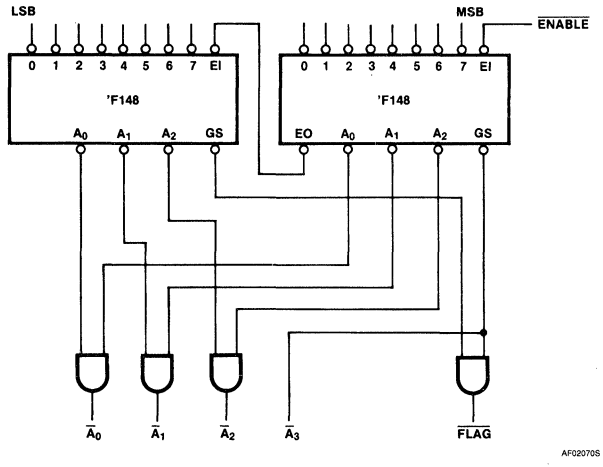
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F148					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ input to $\overline{A}_n$	Waveform 2	3.5 4.0	6.0 6.0	9.0 10.5	3.5 4.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ input to $\overline{EO}$	Waveform 1	2.0 2.5	3.5 4.5	6.5 7.5	2.0 2.5	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ input to $\overline{GS}$	Waveform 2	2.0 2.0	4.0 6.0	9.0 8.0	2.0 2.0	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ input to $\overline{A}_n$	Waveform 2	3.5 3.0	6.0 6.5	8.5 8.0	3.5 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ input to $\overline{GS}$	Waveform 2	2.5 3.0	4.5 6.5	7.0 7.5	2.5 3.0	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ input to $\overline{EO}$	Waveform 2	3.0 4.5	5.0 7.0	7.0 10.5	3.0 4.5	8.0 12.0	ns

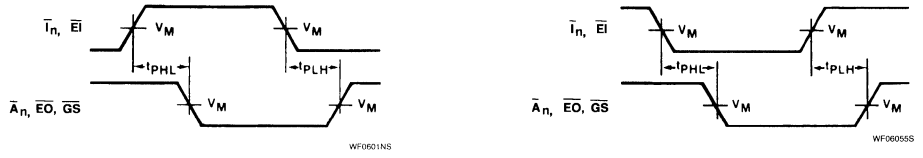
NOTE:
Subtract 0.2ns from minimum values for SO package.

APPLICATION



16-Input Priority Encoder

AC WAVEFORMS

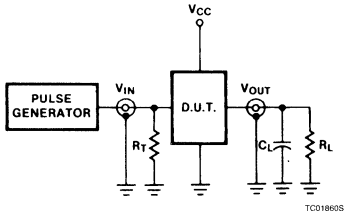


Waveform 1. For Inverting Outputs

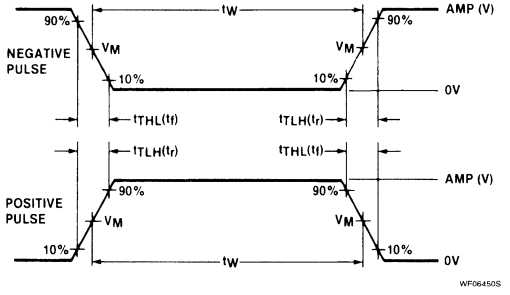
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

FAST 74F151
Multiplexer

8-Input Multiplexer
Product Specification

Logic Products

FEATURES
- **Multifunction capability**
- **Complementary outputs**
- **See 'F251 for 3-state version**

DESCRIPTION
The 'F151 is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. True (Y) and Complement ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, the $\overline{Y}$ output is HIGH and the Y output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Y = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

In one package the 'F151 provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F151	6.0ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F151N
Plastic SO-16	N74F151D

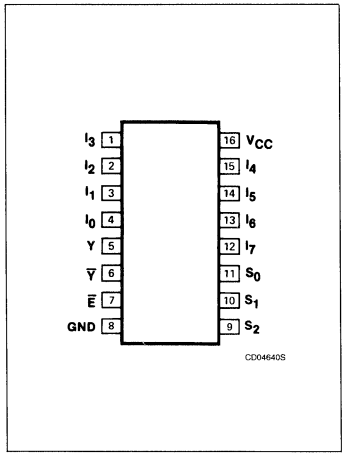
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

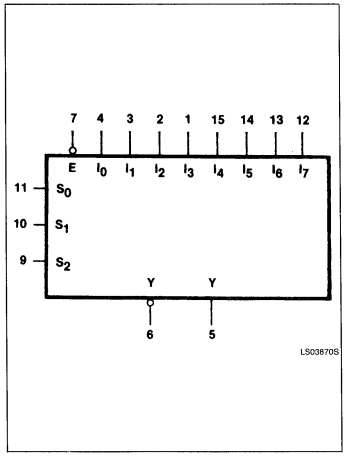
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_0 - I_7$	Data inputs	1.0/1.0	20μA/0.6mA
$S_0 - S_2$	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$	Enable input (active LOW)	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	Data output, Data output inverted	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

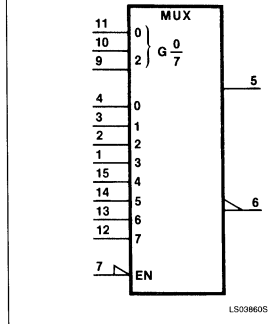
PIN CONFIGURATION



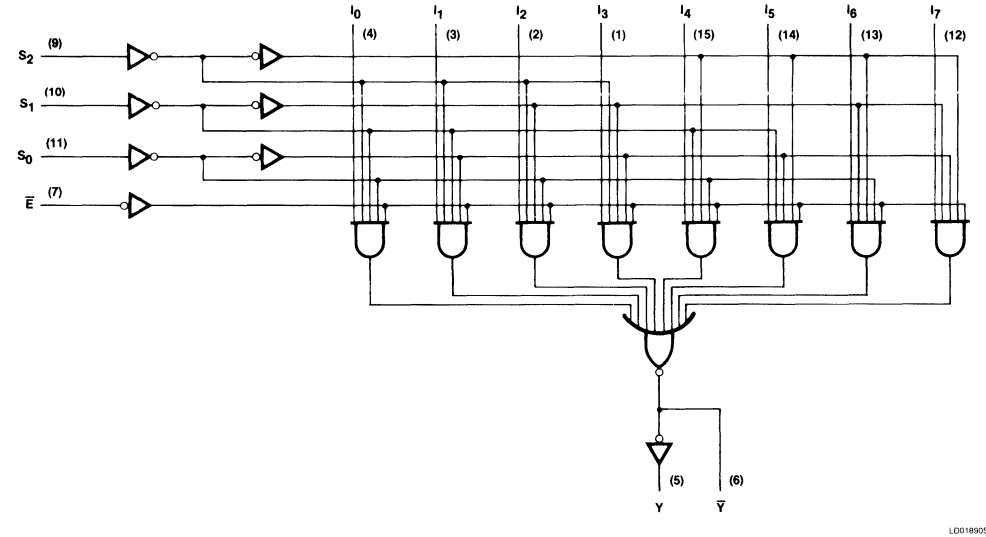
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F151			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−85	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			10	13	mA
		I_{CCL}				14	18	mA

NOTES:

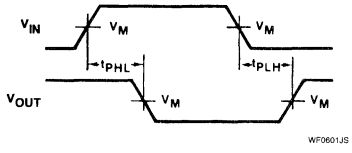
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

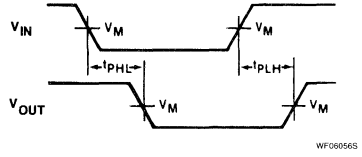
PARAMETER		TEST CONDITIONS	74F151					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	Waveform 2	4.0 4.0	6.0 5.5	9.5 7.0	4.0 4.0	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	Waveform 1	3.0 1.5	4.5 2.5	6.0 4.0	3.0 1.0	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	Waveform 3	4.5 5.0	8.0 8.0	13.0 12.0	4.5 4.5	14.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	Waveform 3	4.5 3.5	7.0 5.0	10.0 6.5	4.5 3.0	11.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	Waveform 1	5.0 4.0	8.0 6.0	10.0 8.0	4.5 4.0	12.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	Waveform 2	3.5 4.5	5.0 7.0	6.5 8.5	3.5 4.5	7.0 9.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

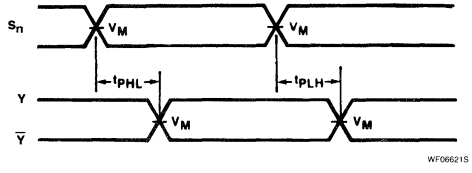
AC WAVEFORMS



Waveform 1. Propagation Delay For Data To Output



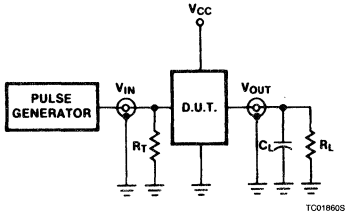
Waveform 2. Propagation Delays For Select Or Enable To Output



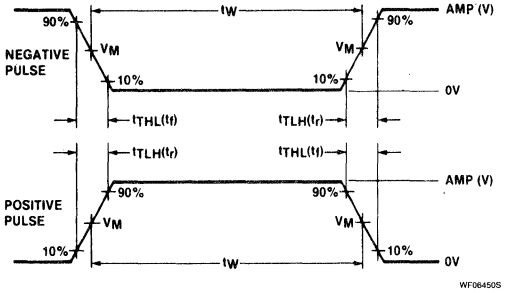
Waveform 3. Propagation Delay For Select To Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F153
Multiplexer

Dual 4-Line to 1-Line Multiplexer
Product Specification

Logic Products

FEATURES
- **Non-inverting outputs**
- **Separate enable for each section**
- **Common select inputs**
- **See 'F253 for 3-state version**

DESCRIPTION
The 'F153 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced LOW when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Y_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

TYPE	TYPICAL PROGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F153	7.0ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F153N
Plastic SO-16	N74F153D

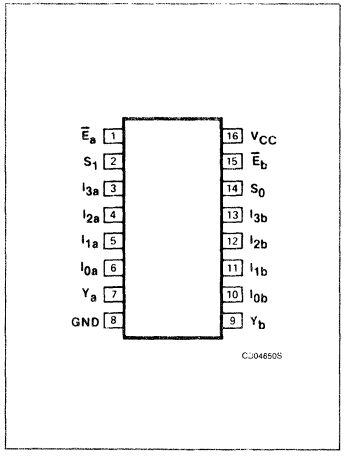
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

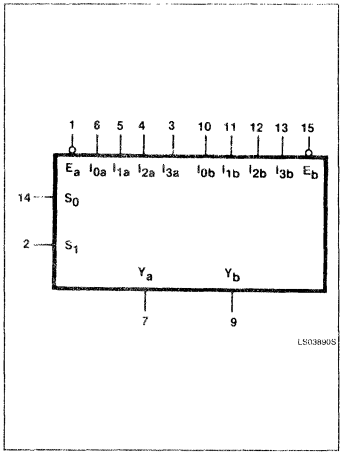
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{3a}$	Side A data inputs	1.0/1.0	20μA/0.6mA
$I_{0b} - I_{3b}$	Side B data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_a$	Side A enable input (active low)	1.0/1.0	20μA/0.6mA
$\overline{E}_b$	Side B enable input (active low)	1.0/1.0	20μA/0.6mA
Y_a	Side A output	50/33	1.0mA/20mA
Y_b	Side B output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

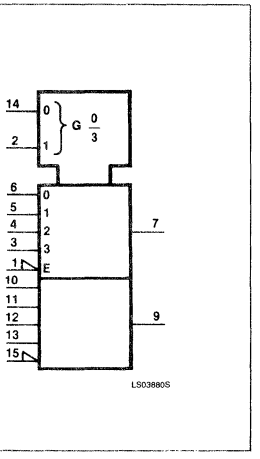
PIN CONFIGURATION



LOGIC SYMBOL

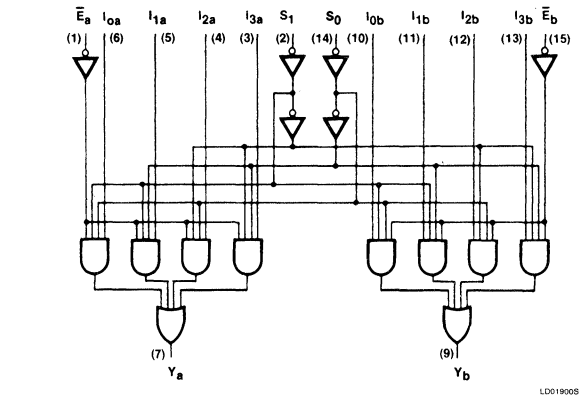


LOGIC SYMBOL (IEEE/IEC)



The '153 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

SELECTS INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\bar{E}$	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F153			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−85	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{E}_n$ = GND; S_n = I_n = 4.5V		12	20	mA
		I_{CCL}		$\overline{E}_n$ = S_n = I_n = GND		12	20	mA

NOTES:

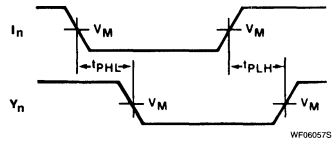
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

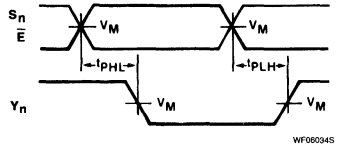
PARAMETER		TEST CONDITIONS	74F153					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 2	5.0 5.0	8.0 8.0	10.5 10.5	4.5 4.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y_n	Waveform 2	5.0 4.0	7.5 5.5	9.0 7.0	4.5 3.5	10.5 8.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



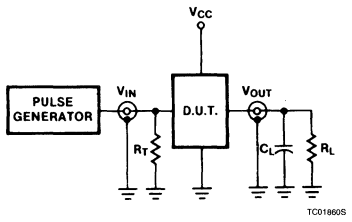
Waveform 1. Propagation Delay Data (I_n) To Output (Y_n)



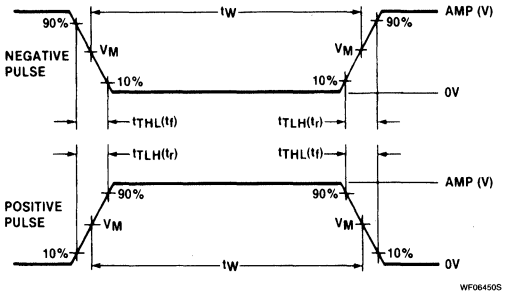
Waveform 2. Propagation Delay Select (S_n) Or Enable ($\overline{E}$) To Output (Y_n)

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F157A, 74F158A
Data Selectors/Multiplexers

'157A Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
'158A Quad 2-Input Data Selector/Multiplexer (Inverted)
Product Specification

Logic Products

DESCRIPTION

The 'F157A is a high-speed quad 2-input multiplexer which selects 4 bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 'F157A. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Y_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Y_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Y_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

The 'F158A is similar but has inverting outputs:

$$\overline{Y}_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$\overline{Y}_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Y}_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$\overline{Y}_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F157A	4.6ns	15mA
74F158A	3.7ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F157AN, N74F158AN
Plastic SO-16	N74F157AD, N74F158AD

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

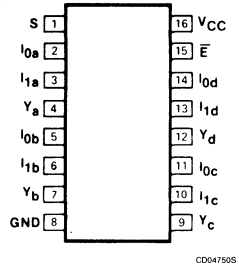
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
All	Inputs	1.0/1.0	20μA/0.6mA
Y_a–Y_d, $\overline{Y}_a$–$\overline{Y}_d$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

PIN CONFIGURATION

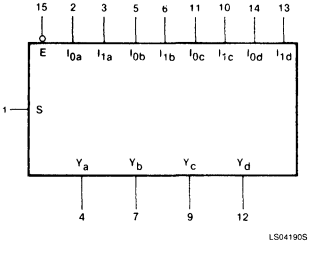
'F157A



CD04750S

LOGIC SYMBOL

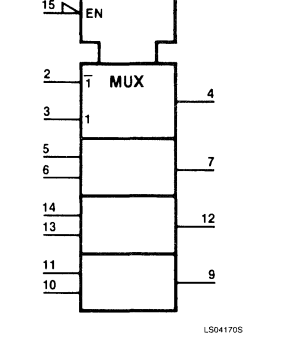
'F157A



LS04190S

LOGIC SYMBOL (IEEE/IEC)

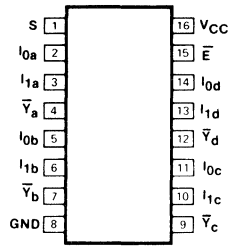
'F157A



LS04170S

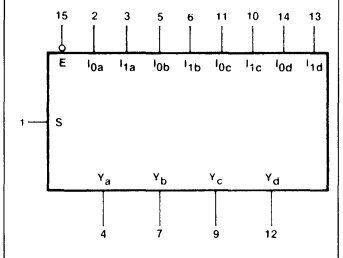
PIN CONFIGURATION

'F158A



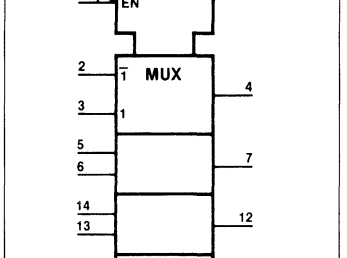
LOGIC SYMBOL

'F158A

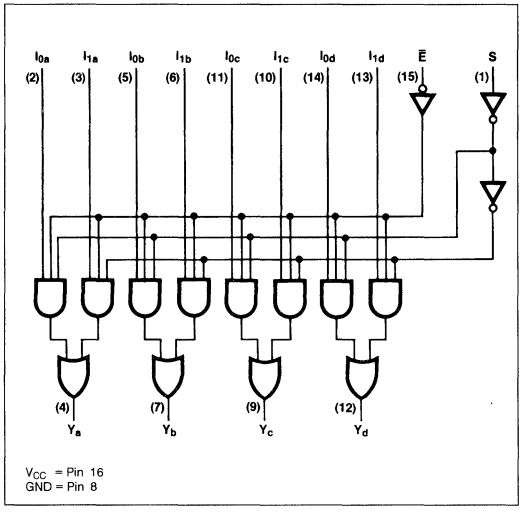


LOGIC SYMBOL (IEEE/IEC)

'F158A

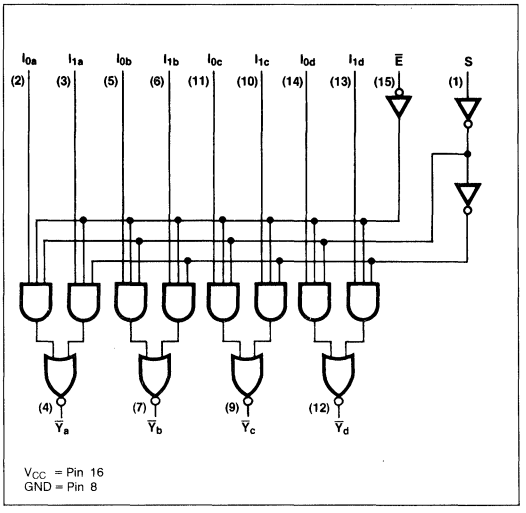


LOGIC DIAGRAM, '157A



VCC = Pin 16
GND = Pin 8

LOGIC DIAGRAM, '158A



VCC = Pin 16
GND = Pin 8

FUNCTION TABLE, '157A

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

FUNCTION TABLE, '158A

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F157A, 158A			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	'F157A	V_{CC} = MAX			15.0	23.0	mA
		'F158A				10.0	15.0	mA

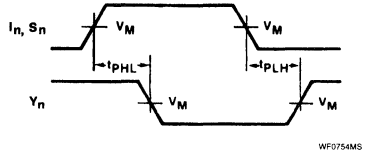
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

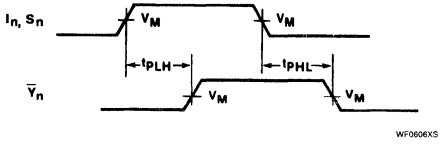
PARAMETER			TEST CONDITIONS	74F157A, 'F158A					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	'F157A	Waveform 2	3.5 2.5	4.5 3.5	6.5 5.0	3.0 1.5	7.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	'F157A	Waveform 1	6.0 4.0	7.5 5.0	9.0 6.5	5.5 4.0	10.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	'F157A	Waveform 2	5.5 4.5	7.5 6.0	10.0 7.5	5.0 4.0	11.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	'F158A	Waveform 3	3.0 1.5	4.0 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	'F158A	Waveform 4	4.5 5.0	5.5 6.0	7.0 7.5	4.0 5.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	'F158A	Waveform 3	4.5 4.0	6.5 5.5	8.5 7.5	4.0 3.5	9.5 8.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

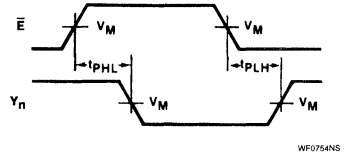
AC WAVEFORMS



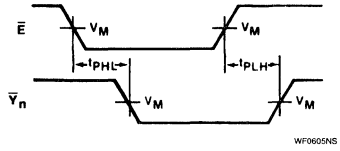
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



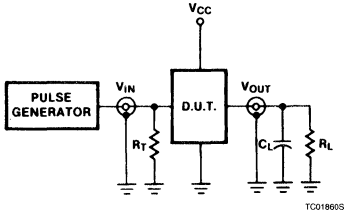
Waveform 3. For Inverting Outputs



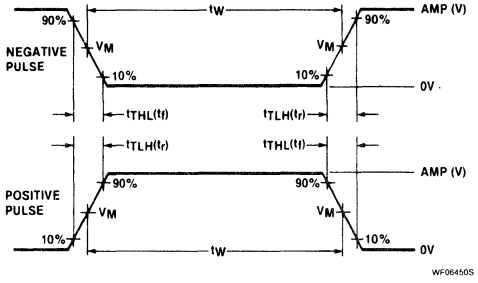
Waveform 4. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F160A, 74F161A, 74F162A, 74F163A Counters

'F160A, 'F162A BCD Decade Counter
'F161A, 'F163A 4-Bit Binary Counter
Product Specification

FEATURES

- **Synchronous counting and loading**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset ('F160A, 'F161A)**
- **Synchronous reset ('F162A, 'F163A)**
- **High-speed synchronous expansion**
- **Typical count rate of 120MHz**

DESCRIPTION

Synchronous presettable decade ('F160A, 'F162A) and 4-bit ('F161A, 'F163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F160A	120MHz	40mA
74F161A	120MHz	40mA
74F162A	120MHz	40mA
74F163A	120MHz	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F160AN, N74F161AN N74F162AN, N74F163AN
Plastic SO-16	N74F160AD, N74F161AD N74F162AD, N74F163AD

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

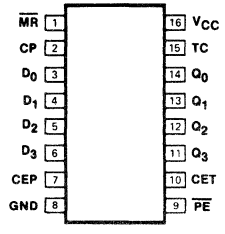
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CEP	Count enable parallel input	1.0/1.0	20μA/0.6mA
CET	Count enable trickle input	1.0/2.0	20μA/1.2mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous reset input (active LOW)	1.0/2.0	20μA/1.2mA
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active LOW)	1.0/2.0	20μA/1.2mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
TC	Terminal count output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

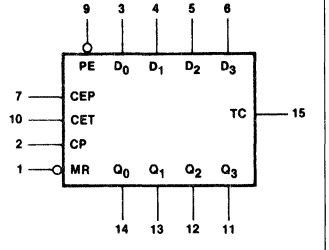
'F160A



CD04741S

LOGIC SYMBOL

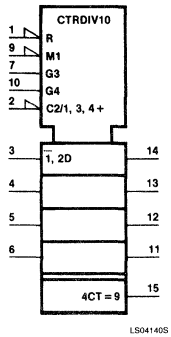
'F160A



LS04161S

LOGIC SYMBOL (IEEE/IEC)

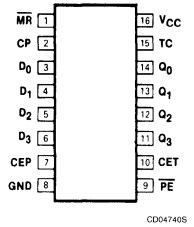
'F160A



LS04140S

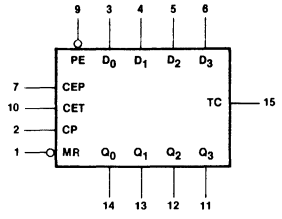
PIN CONFIGURATION

'F161A



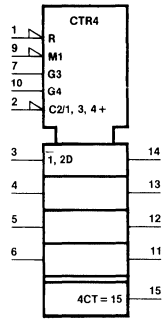
LOGIC SYMBOL

'F161A



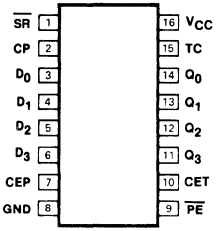
LOGIC SYMBOL

'F161A



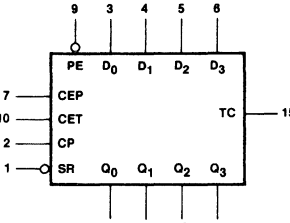
PIN CONFIGURATION

'F162A



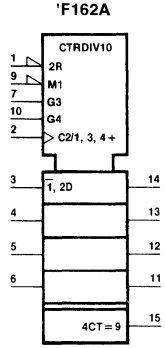
LOGIC SYMBOL

'F162A



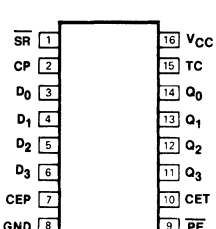
LOGIC SYMBOL

'F162A



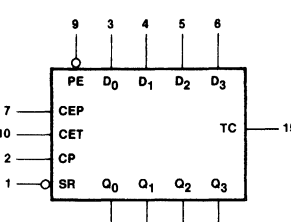
PIN CONFIGURATION

'F163A



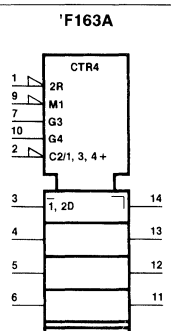
LOGIC SYMBOL

'F163A



LOGIC SYMBOL

'F163A



The outputs of the counters may be preset to HIGH or LOW level. A LOW level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the $D_0 - D_3$ inputs to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A LOW level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) in 'F160A and 'F161A to LOW levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 'F162A and 'F163A, the clear function is synchronous. A LOW level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) to LOW levels after the next positive-going transition on the Clock (CP) input (providing that the set-up and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

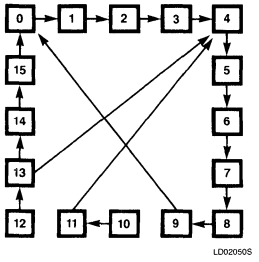
The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to the HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B).

The TC output is subject to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

STATE DIAGRAMS

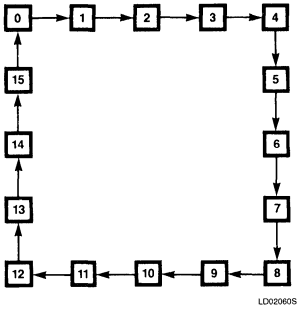
Logic Equations: Count Enable = CEP•CET•PE
$TC = Q_0 \bullet \overline{Q}_1 \bullet Q_2 \bullet Q_3 \bullet CET$

'F160A, 'F162A

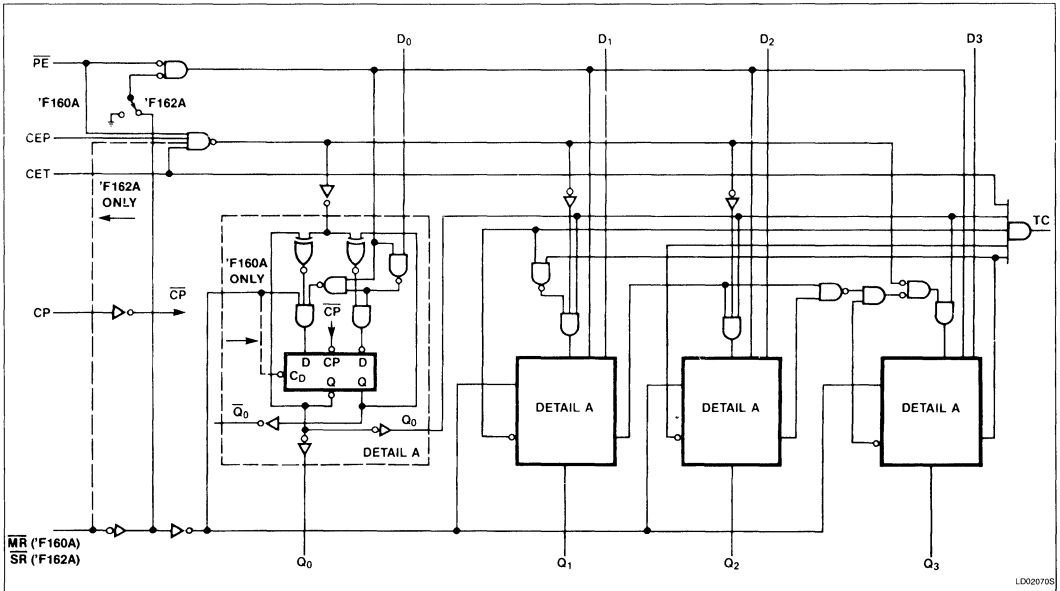


Logic Equations: Count Enable = CEP•CET•PE
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

'F161A, 'F163A

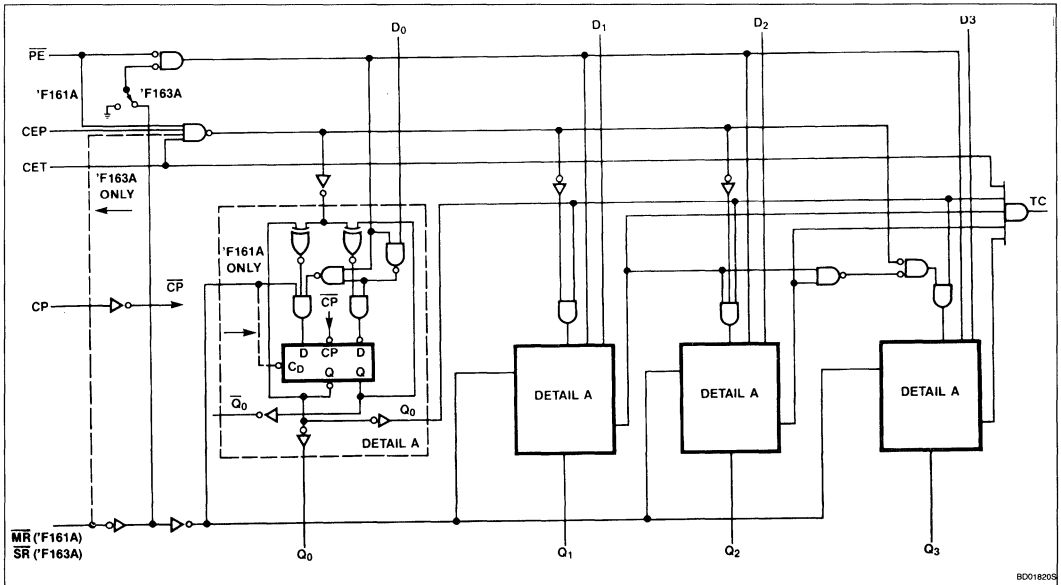


LOGIC DIAGRAM, 'F160A, 'F162A



NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

LOGIC DIAGRAM, 'F161A, 'F163A



NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT — FUNCTION TABLE, 'F160A, 'F161A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H	X	l	X	h	X	q_n	(1)
	H	X	X	l(2)	h	X	q_n	L

MODE SELECT — FUNCTION TABLE, 'F162A, 'F163A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	(2)
Count	h	↑	h	h	h	X	count	(2)
Hold (do nothing)	h	X	l	X	h	X	q_n	(2)
	h	X	X	l	h	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one set-up time prior to LOW-to-HIGH clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTES:

(1) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for 'F161A and HLLH for 'F160A).

(2) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for 'F162A and HHHH for 'F163A).

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.50	5.0	5.50	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F160A, 'F161A, 'F162A, 'F163A			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	$\overline{CET}$, $\overline{SR}$, $\overline{PE}$	V_{CC} = MAX, V_I = 2.7V				40	μA
		Other inputs					20	μA
I_{IL}	LOW-level input current	$\overline{CET}$, $\overline{SR}$, $\overline{PE}$	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		Other inputs					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX				55	mA
		I_{CCL}					55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH} is measured with $\overline{PE}$ input HIGH, again with $\overline{PE}$ input LOW, all other inputs HIGH and outputs open. I_{CCL} is measured with Clock input HIGH, again with Clock input LOW all other inputs LOW, and outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F160A, 'F162A					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1 $\overline{PE}$ = HIGH	3.5 3.5	5.5 7.5	7.5 10.0	3.5 3.5	8.5 4.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1 $\overline{PE}$ = LOW	4.0 4.0	6.0 6.0	8.5 8.5	4.0 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	5.0 5.0	10 10	14 14	5.0 5.0	15 15	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	Waveform 2	2.5 2.5	4.5 4.5	7.5 7.5	2.5 2.5	8.5 8.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n ('F160A)	Waveform 3	5.5	9.0	12	5.5	13	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F160A, 'F162A					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	Waveform 5	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	11 8.5			11.5 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	2.0 0			2.0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW CEP or CET to CP	Waveform 4	11 5.0			11.5 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW CEP or CET to CP	Waveform 4	2.0 0			2.0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width (load), HIGH or LOW	Waveform 1	5.0 5.0			5.0 5.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width (count), HIGH or LOW	Waveform 1	4.0 6.0			4.0 7.0		ns
$t_w(L)$	$\overline{MR}$ pulse width LOW ('F160A, 'F161A)	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP ('F160A)	Waveform 3	6.0			5.0		ns

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

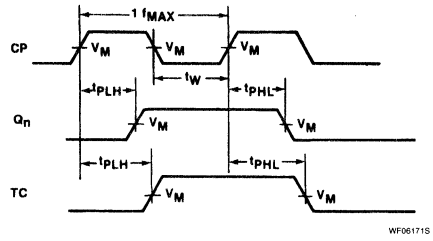
PARAMETER		TEST CONDITIONS	74F161A, 'F163A					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1 $\overline{PE}$ = HIGH	2.0 3.5	4.0 7.0	6.0 10.0	2.0 3.5	7.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1 $\overline{PE}$ = LOW	2.5 4.0	4.0 6.0	7.0 8.5	2.5 4.0	8.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	5.0 5.0	10 14	14 16	5.0 5.0	15 17.5	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	Waveform 2	2.5 2.5	4.5 4.5	7.5 7.5	2.5 2.5	8.5 8.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n ('F161A)	Waveform 3	5.5	9.0	12	5.5	13	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

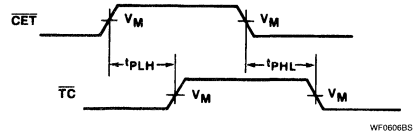
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F161A, 'F163A					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	Waveform 5	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	11 8.5			11.5 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	2.0 0			2.0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW CEP or CET to CP	Waveform 4	11 5.0			11.5 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW CEP or CET to CP	Waveform 4	2.0 0			2.0 0		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (load), HIGH or LOW	Waveform 1	6.5 3.5			6.5 5.0		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (count), HIGH or LOW	Waveform 1	6.5 3.5			7.0 4.0		ns
$t_W(L)$	$\overline{MR}$ pulse width LOW ('F160A, 'F161A)	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP ('F161A)	Waveform 3	6.0			5.0		ns

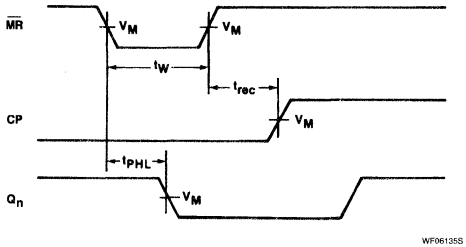
AC WAVEFORMS



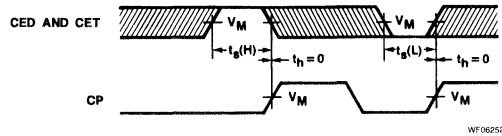
Waveform 1. Clock To Output Delays, Maximum Clock Frequency, And Clock Pulse Width



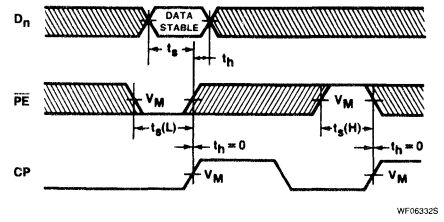
Waveform 2. Propagation Delays CET Input To TC Output



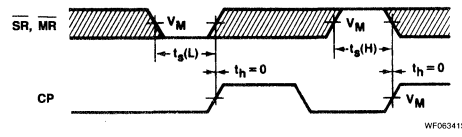
Waveform 3. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time ('F160A, 'F161A)



Waveform 4. CEP And CET Set-up And Hold Times



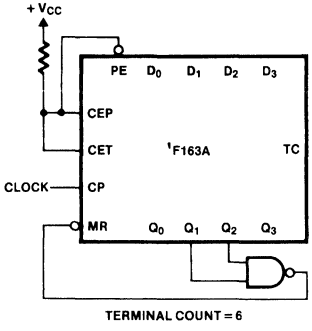
Waveform 5. Parallel Data And Parallel Enable Set-up And Hold Times



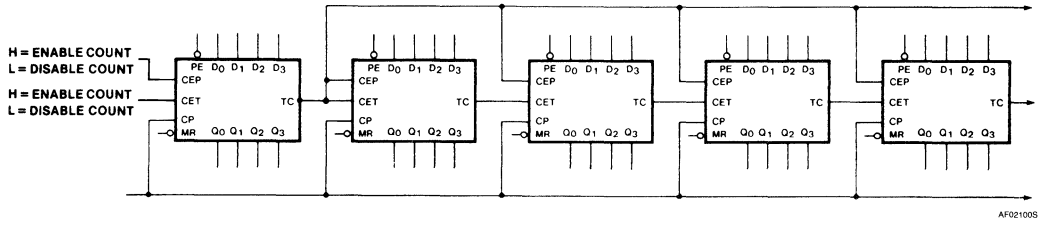
Waveform 6. Synchronous Reset Set-up, Pulse Width And Hold Times ('F162A, 'F163A)

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION

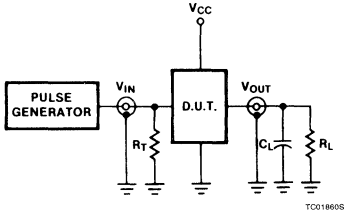


a.

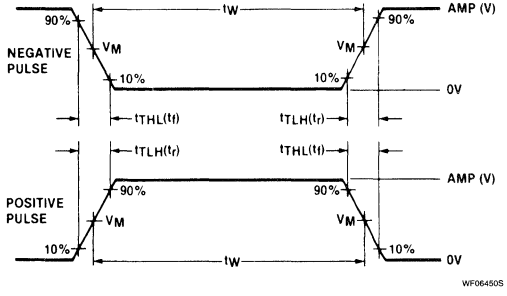


b. Synchronous Multistage Counting Scheme

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F164
Shift Register

8-Bit Serial-In Parallel-Out Shift Register
Preliminary Specification

Logic Products

FEATURES
- **Gated serial data inputs**
- **Typical shift frequency of 90MHz**
- **Asynchronous master reset**
- **Fully buffered Clock and Data inputs**
- **Fully synchronous data transfers**

DESCRIPTION
The 'F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs ($D_{sa} \cdot D_{sb}$); either input can be used as an active HIGH enable for data entry though the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one set-up time before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F164	90MHz	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F164N
Plastic SO-14	N74F164D

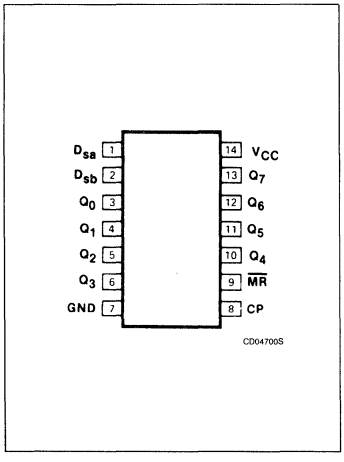
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

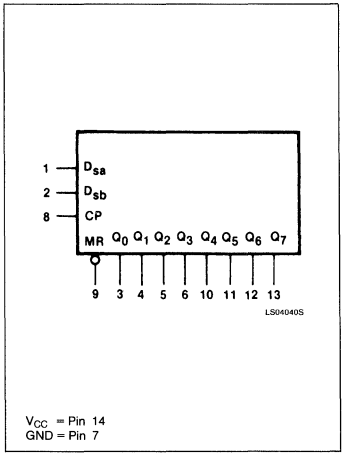
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa}, D_{sb}	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

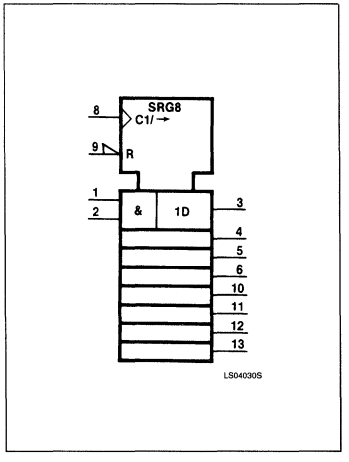
PIN CONFIGURATION



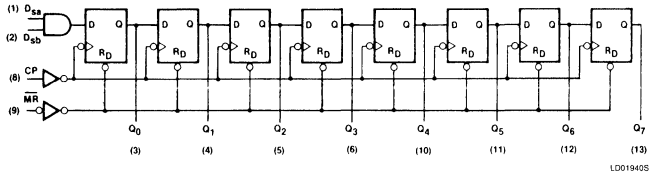
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1	—	Q_7
Reset (clear)	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_6
	H	↑	l	h	L	q_0	—	q_6
	H	↑	h	l	L	q_0	—	q_6
	H	↑	h	h	H	q_0	—	q_6

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

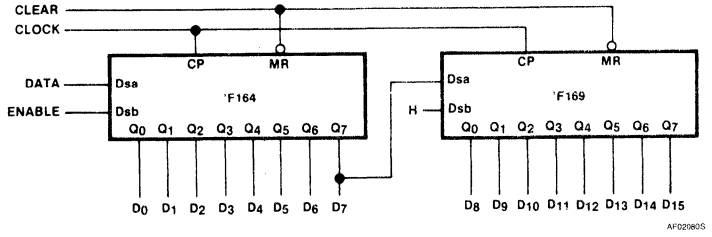
(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F164			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			33	50	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

APPLICATION



NOTES:
The 'F164 can be cascaded to form synchronous shift registers of longer length.
Here, two devices are combined to form a 16-bit shift register.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

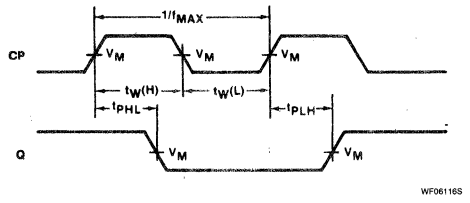
PARAMETER		TEST CONDITIONS	74F164					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	80	90		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.5 5.0	6.0 7.5	8.0 10	4.5 5.0	9.0 11	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.5	10.5	13	8.5	14	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

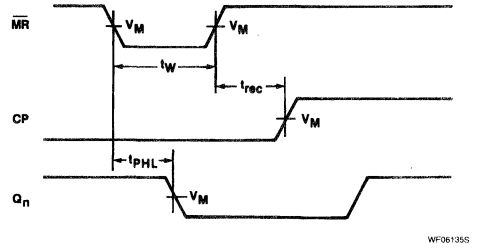
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F164					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW A or B to CP	Waveform 3	7.0 7.0			7.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A or B to CP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW	Waveform 1	4.0 7.0			4.0 7.0		ns
$t_w(L)$	$\overline{MR}$ pulse width LOW	Waveform 2	7.0			7.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			7.0		ns

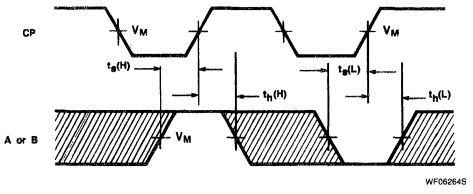
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



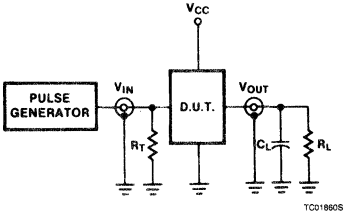
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



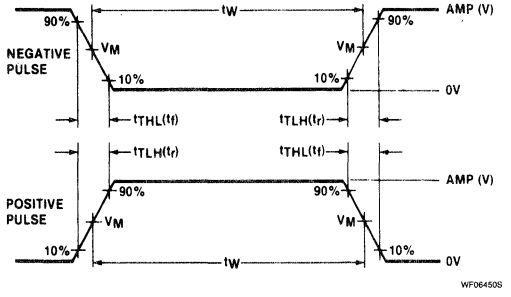
Waveform 3. Data Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F166
Shift Register

8-Bit Serial/Parallel-In, Serial Out Shift Register
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Synchronous parallel to serial applications**
- **Synchronous serial data input for easy expansion**
- **Clock enable for "do nothing" mode**
- **Asynchronous Master Reset**
- **Exandable to 16-bits in 8-bit increments**

DESCRIPTION

The 166 is a high speed 8-bit shift register that has fully synchronous serial parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one set-up time before the LOW-to-HIGH clock transistion, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into internal bit position Q_0 from Serial Data Input (D_s), and the remaining bits are shifted one place to the right ($Q_0 - Q_1 - Q_2$, etc.), with each positive-going clock transition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F166	175MHz	41mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F166N
Plastic SO-16	N74F166D

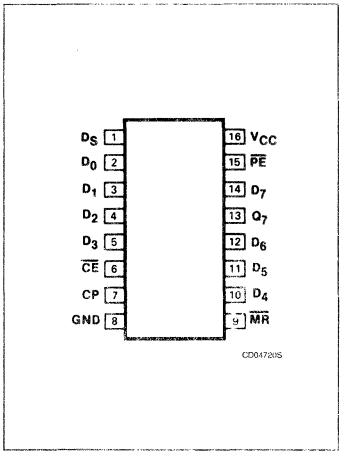
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

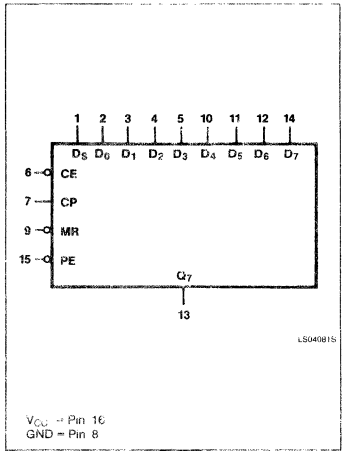
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{PE}$	Parallel enable input	1/0.033	20μA/20μA
$\overline{CE}$	Clock enable input	1/0.033	20μA/20μA
CP	Clock input (active rising edge)	1/0.033	20μA/20μA
D_s	Serial data input	2/0.066	40μA/40μA
$D_0 - D_7$	Parallel data input	1/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active LOW)	2/0.066	40μA/40μA
Q_7	Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

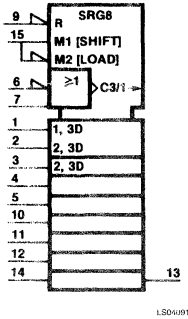
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



6

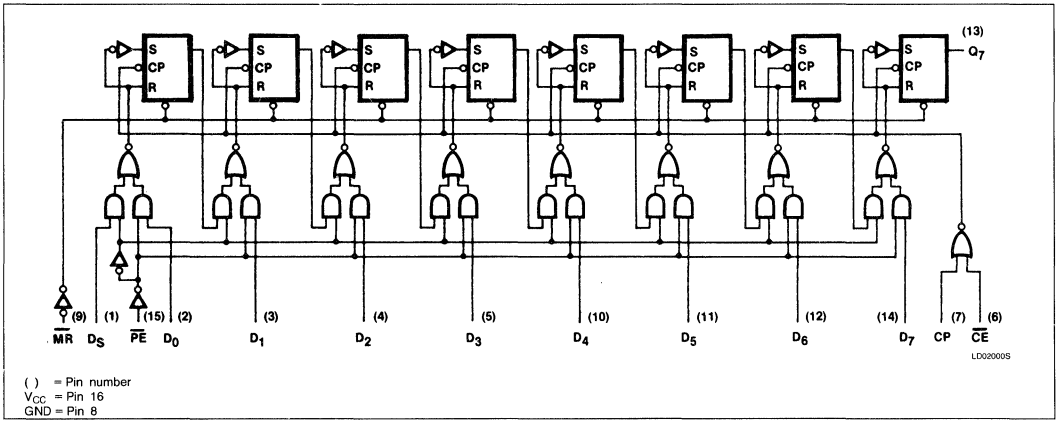
For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_S input of the succeeding stage. The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation. A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUT
	$\overline{PE}$	$\overline{CE}$	CP	D_S	$D_0 - D_7$	Q_0	$Q_1 - Q_6$	Q_7
Parallel load	l	l	↑	X	l – l	L	L – L	L
	l	l	↑	X	h – h	H	H – H	H
Serial shift	h	l	↑	l	X – X	L	$q_0 - q_5$	q_6
	h	l	↑	h	X – X	H	$q_0 - q_5$	q_6
Hold (do nothing)	X	h	X	X	X – X	q_0	$q_1 - q_6$	q_7

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
q_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

LOGIC DIAGRAM



( ) = Pin number
V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F166			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.5	V
				±5%V_{CC}		.35	.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = 0.0V, V_I = 7.0V				100	μA
		$\overline{CE}$, CP[3]					100	μA
I_{IH}	HIGH-level input current	Others	V_{CC} = MAX, V_I = 2.7V			1	20	μA
		$\overline{MR}$, D_S					40	μA
I_{IL}	LOW-level input current	Others	V_{CC} = MAX, V_I = 0.5V				−20	μA
		$\overline{MR}$,D_S					−40	μA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX		−60	−90	−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX; S_n = $\overline{MR}$ = D_S = 4.5V; D_n = GND, CP = ↑			60	85	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. When testing CP, $\overline{CE}$ must remain in HIGH state, whereas CP must remain in HIGH state when testing $\overline{CE}$.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

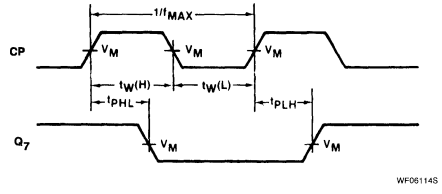
PARAMETER		TEST CONDITIONS	74F166					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	135	175		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_7	Waveform 1	5.0 4.0	7.5 6.0	10.0 8.0	5.0 3.5	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_7	Waveform 2	4.0	6.5	8.5	4.0	9.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

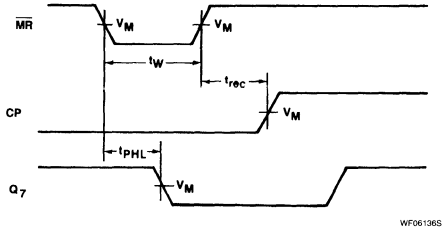
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F166					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n, D_s to CP	Waveform 3	2.5 2.5			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n, D_s to CP	Waveform 3	0 0			0 0		ns
$t_s(L)$	Set-up time, HIGH or LOW $\overline{CE}$ to CP	Waveform 3	5.0			6.0		ns
$t_h(H)$	Hold time, HIGH or LOW $\overline{CE}$ to CP	Waveform 3	0			0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{PE}$ to CP	Waveform 3	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$ to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW	Waveform 1	3.5 5.5			3.5 6.5		ns
$t_w(L)$	$\overline{MR}$ pulse width LOW	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

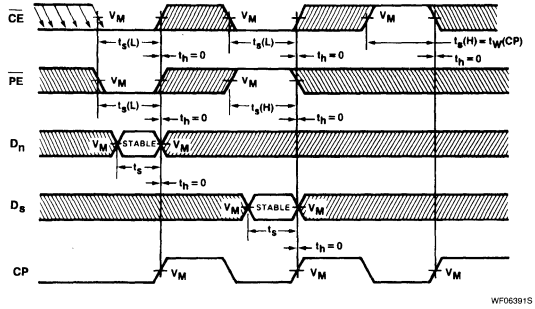
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



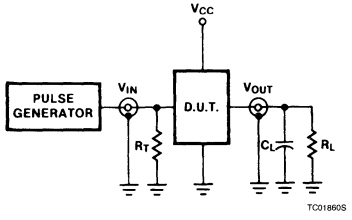
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



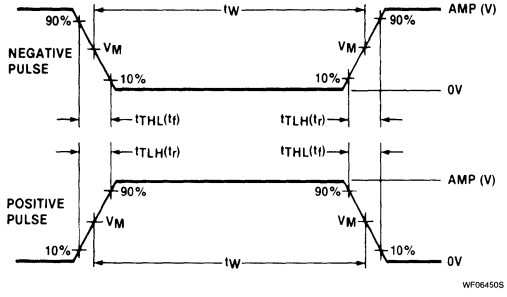
Waveform 3. Set-up And Hold Time For PE, D_n, D_S, And $\overline{CE}$ To CP

NOTE: For all waveforms, $V_M = 1.5V$.
The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.
The shaded areas indicate when the input is permitted to change for predictable performance.
The changing output assumes internal Q_6 opposite state from Q_7.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F168, 74F169 Counters

'F168 — 4-Bit Up/Down BCD Decade Synchronous Counter
'F169 — 4-Bit Up/Down Binary Synchronous Counter
Preliminary Specification

Logic Products

FEATURES

- **Synchronous counting and loading**
- **Up/Down counting**
- **Modulo 16 binary counter — 'F169**
- **BCD decade counter — 'F168**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Built-in lookahead carry capability**
- **Presettable for programmable operation**

DESCRIPTION

The 'F168 is a synchronous, presettable BCD decade up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F168	7.5ns	50mA
74F169	7.5ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F168N, N74F169N
Plastic SO-16	N74F168D, N74F169D

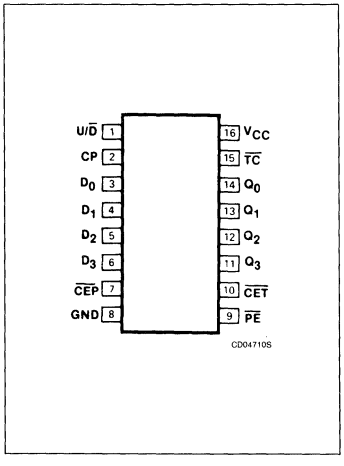
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

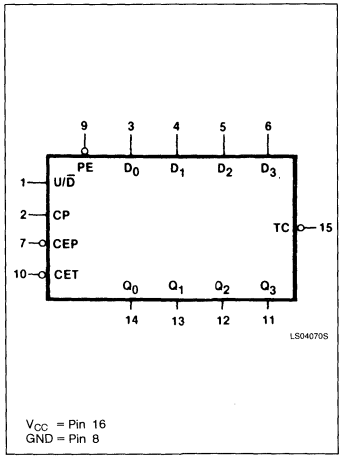
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CEP}$	Count enable parallel input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active LOW)	1.0/2.0	20μA/1.2mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active LOW)	1.0/1.0	20μA/0.6mA
$U/\overline{D}$	Up/down count control input	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}$	Terminal count output (active LOW)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

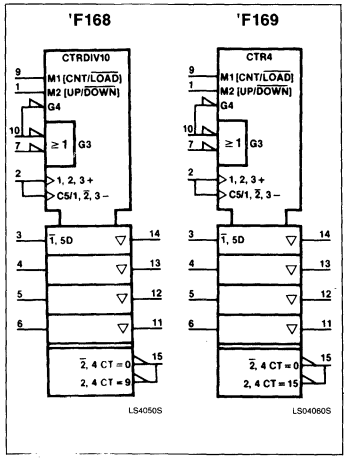
PIN CONFIGRATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

The direction of counting is controlled by the Up/Down ($U/\overline{D}$) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$, $\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure 1 for the fast synchronous multistage counting connections.

The 'F169A is identical except that it is a Modulo 16 counter.

FUNCTIONAL DESCRIPTION

The 'F168 and 'F169 use edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the Clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the $D_0 - D_3$ inputs enter the flip-flops on the next rising edge of the Clock, in order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the $U/\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the 'F169) in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'F168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason, the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$
2) Up: $\overline{TC} = Q_0 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$
3) Down: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	ACTION ON RISING CLOCK EDGE
L	X	X	X	Load ($D_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
X = Don't care

MODE SELECT — FUNCTION TABLE

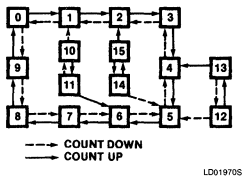
OPERATING MODE	INPUTS						OUTPUTS	
	CP	$U/\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	(1)
	↑	X	X	X	l	h	H	(1)
Count up	↑	h	l	l	h	X	Count Up	(1)
Count down	↑	l	l	l	h	X	Count Down	(1)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition

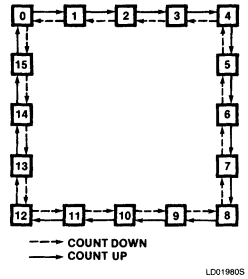
NOTE:
1. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169A. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168A.

STATE DIAGRAMS

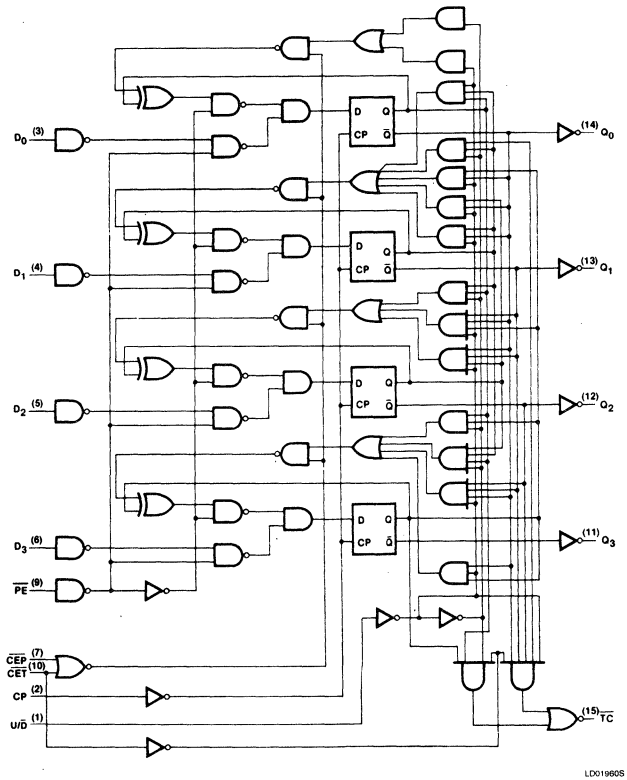
'F168



'F169

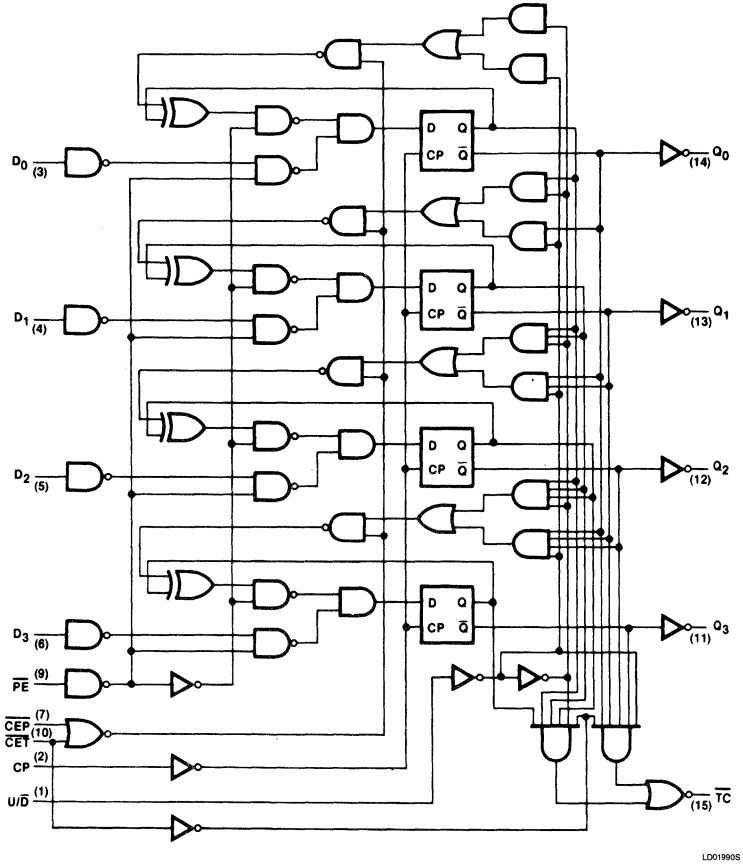


LOGIC DIAGRAM, 'F168



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

LOGIC DIAGRAM, 'F169



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

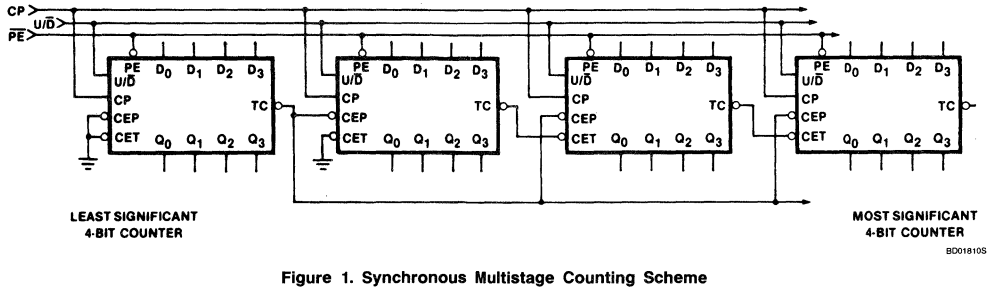


Figure 1. Synchronous Multistage Counting Scheme

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F168, 'F169			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	$\overline{CET}$ input	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		Other inputs					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			50	75	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after applying a momentary 4.5V, then ground to the clock input with all other inputs grounded and outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F168, 'F169					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, HIGH or LOW)	Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	9.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	17.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$ ('F168)	Waveform 3	3.5 4.0	8.5 12.5	11.0 16	3.5 4.0	12.5 17.5	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$ ('F169)	Waveform 3	3.5 4.0	8.5 8.0	11.0 10.5	3.5 4.0	12.5 12.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

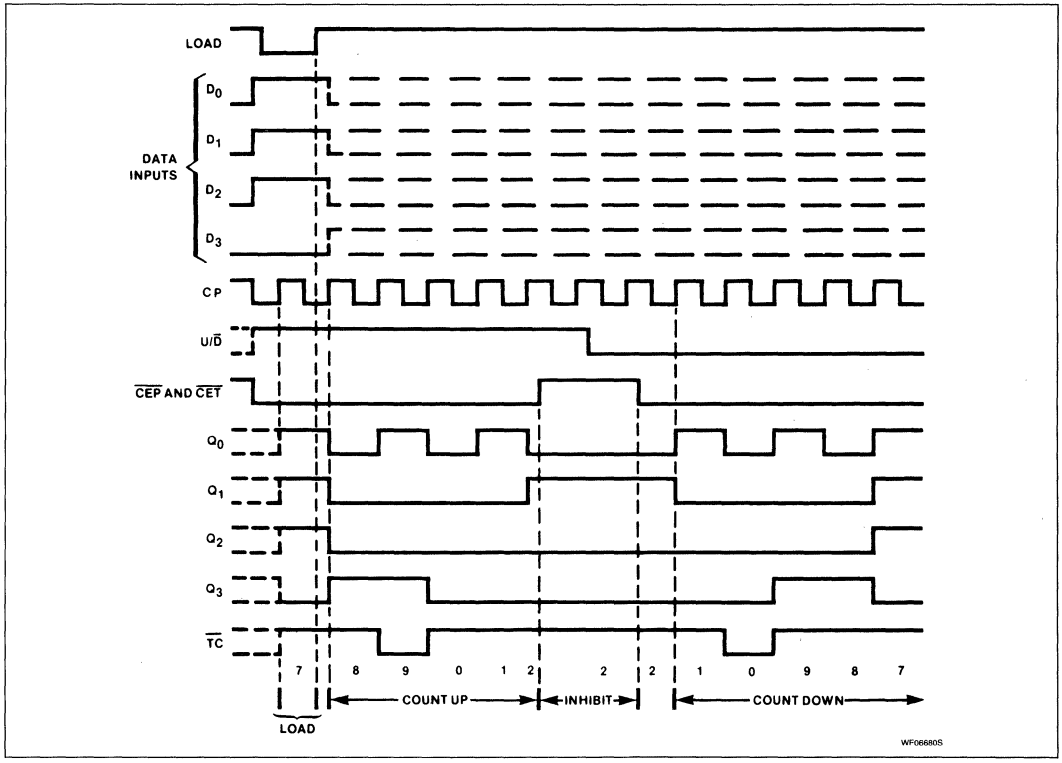
PARAMETER		TEST CONDITIONS	74F168, 'F169					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	Waveform 4	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 4	3.0 3.0			3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{PE}$ to CP	Waveform 4	8.0 8.0			11.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW U/$\overline{D}$ to CP ('F168)	Waveform 6	11.0 16.5			11.0 16.5		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW U/$\overline{D}$ to CP ('F169)	Waveform 6	11.0 7.0			11.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW U/$\overline{D}$ to CP	Waveform 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW	Waveform 1	4.0 6.0			4.0 6.0		ns

6

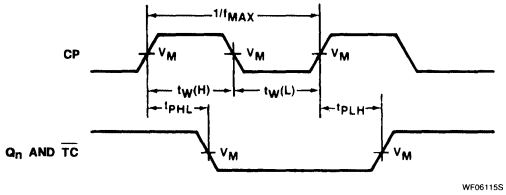
WAVEFORM (Typical Load, Count, and Inhibit Sequences)

Illustrated below is the following sequence for the 'F168. The operation of the 'F169 is similar.

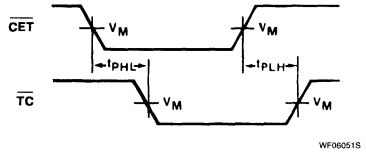
1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



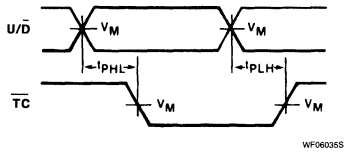
AC WAVEFORMS



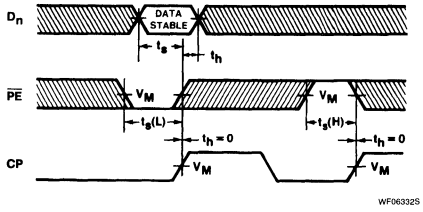
Waveform 1. Clock To Output Delays And Clock Pulse Width



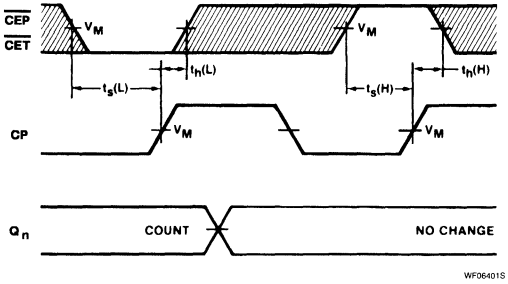
Waveform 2. Propagation Delays CET Input To Terminal Count Output



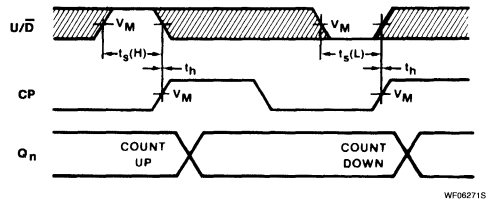
Waveform 3. Propagation Delays U/D Control To Terminal Count Output



Waveform 4. Parallel Data And Parallel Enable Set-up And Hold Times



Waveform 5. Count Enable Set-up And Hold Times

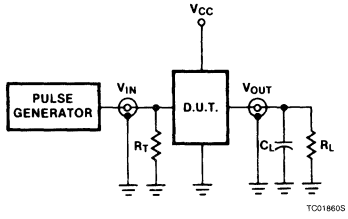


Waveform 6. Up/Down Control Set-up And Hold Times

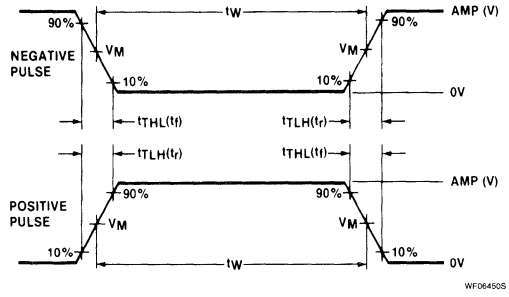
NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

6

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F174
Flip-Flop

Hex D Flip-Flops
Product Specification

Logic Products

FEATURES

- **Six edge-triggered D-type flip-flops.**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**

DESCRIPTION

The 'F174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced LOW independent of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where true outputs only are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F174	100MHz	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F174N
Plastic SO – 16	N74F174D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

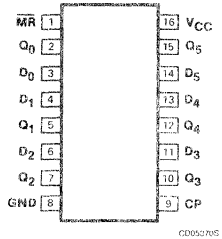
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_5$	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_5$	Data outputs	50/33	1.0mA/20mA

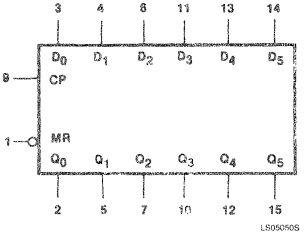
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

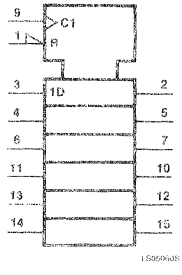
PIN CONFIGURATION



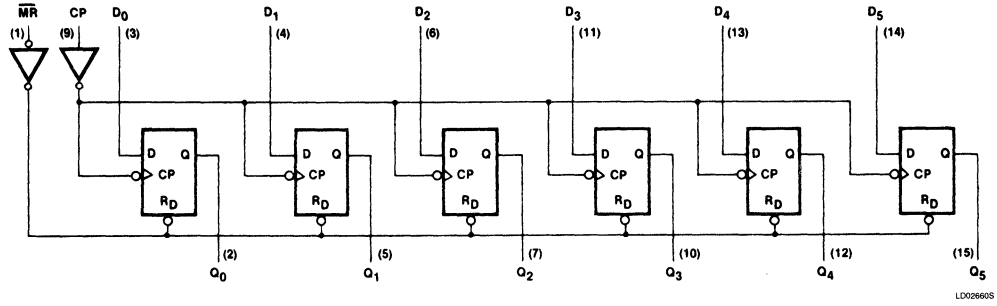
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
GND = Pin Numbers

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F174 Min	74F174 Typ[2]	74F174 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, D_n = $\overline{MR}$ = 4.5V, CP = ↑			35	45	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

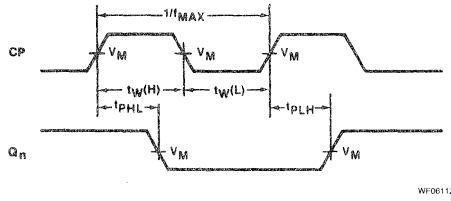
PARAMETER		TEST CONDITIONS	74F174 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F174 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.5 4.5	5.5 6.0	8.0 10.0	3.5 4.5	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	5.0	8.5	14.0	5.0	15.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

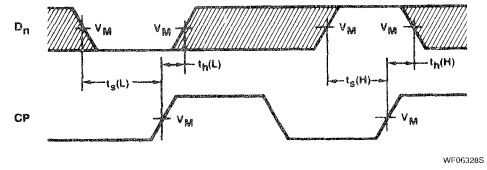
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F174 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F174 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_s(H) t_s(L)	Set-up time, HIGH or LOW D_n to CP	Waveform 2	4.0 4.0			4.0 4.0		ns ns
t_h(H) t_h(L)	Hold time, HIGH or LOW D_n to CP	Waveform 2	0 0			0 0		ns
t_w(H) t_w(L)	CP pulse width, HIGH or LOW	Waveform 1	4.0 6.0			4.0 6.0		ns ns
t_w(L)	$\overline{MR}$ pulse width LOW	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		ns ns

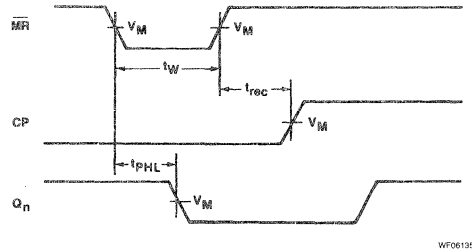
AC WAVEFORMS



Waveform 1. Clock To Output Delays, Clock Pulse Width, And Maximum Clock Frequency



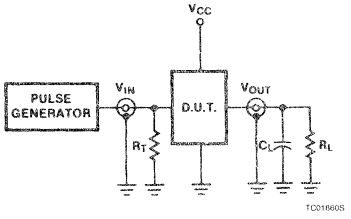
Waveform 2. Data Set-Up And Hold Times



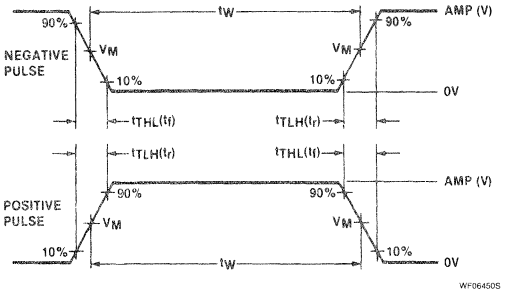
Waveform 3. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; to GND see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F175
Quad D Flip-Flop

Quad D Flip-Flop
Product Specification

Logic Products

FEATURES
- **Four edge-triggered D flip-flops**
- **Buffered common clock**
- **Buffered, asynchronous master reset**
- **True and complementary output**

DESCRIPTION
The 'F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced LOW independantly of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F175	6.0ns	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F175N
Plastic SO-16	N74F175D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	True outputs	50/33	1.0mA/20mA
$\overline{Q}_0 - \overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

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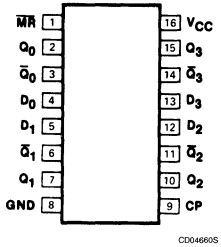
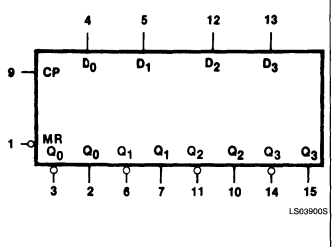
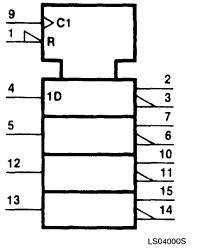
PIN CONFIGURATION



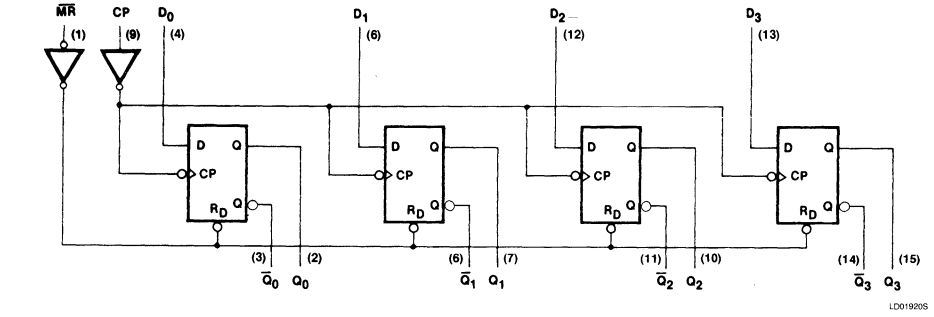
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

MODE SELECT – FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F175			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, D_n = $\overline{MR}$ = 4.5V, CP = ↑			25	34	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

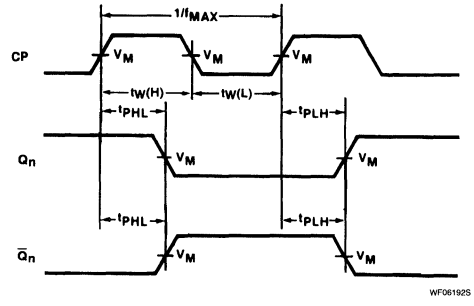
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F175					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	Waveform 1	100	140		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	4.0 4.0	5.0 6.5	6.5 8.5	4.0 4.0	7.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	4.5	9.0	11.5	4.5	13	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	9.0	ns

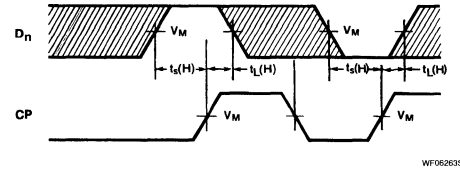
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F175					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, HIGH or LOW	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width LOW	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		ns

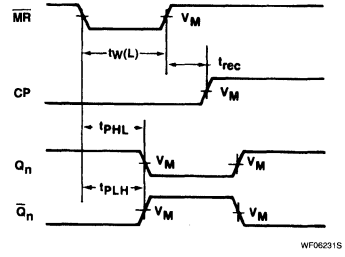
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



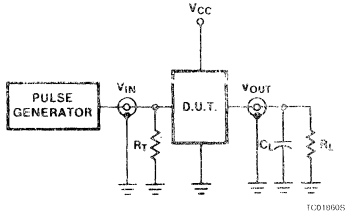
Waveform 2. Data Set-up And Hold Times



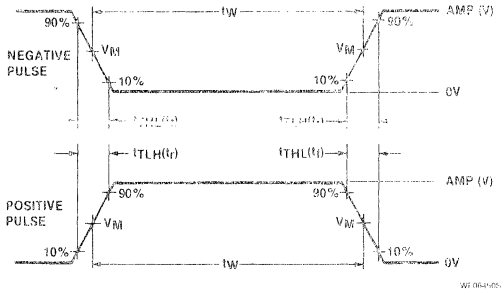
Waveform 3. Master Reset To Output Delay, Master Reset Pulse Width, And Master Reset Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F181
Arithmetic Logic Unit

4-Bit Arithmetic Logic Unit
Product Specification

Logic Products

FEATURES

- **Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full lookahead carry for high-speed arithmetic operation on long words**
- **40% faster than 'S181 with only 30% 'S181 power consumption**
- **Available in 300 mil wide 24 pin SLIM DIP package**

DESCRIPTION

The 'F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0 - S_3$) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F181	7.3ns	43mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F181N
Plastic SOL-24	N74F181D

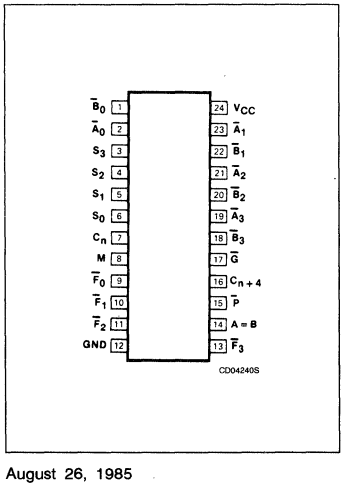
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

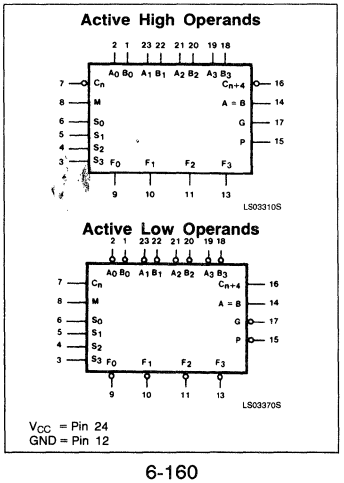
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{A}_0 - \overline{A}_3$, $\overline{B}_0 - \overline{B}_3$	Operand inputs	1.0/1.0	20μA/0.6mA
$S_0 - S_3$	Function select inputs	1.0/1.0	20μA/0.6mA
C_n	Carry input	1.0/1.0	20μA/0.6mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
A = B	Compare output	*OC/33	*OC/20mA
$\overline{F}_0 - \overline{F}_3$	Outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
*OC = Open collector

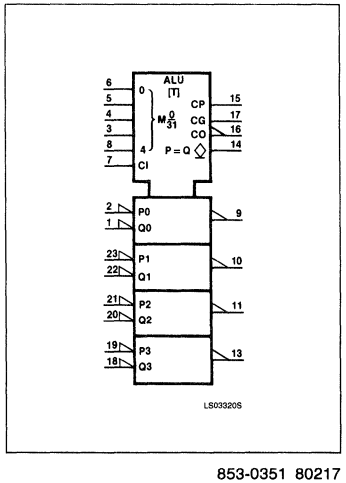
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Arithmetic Logic Unit | FAST 74F181

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the '182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open collector and can be wired – AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

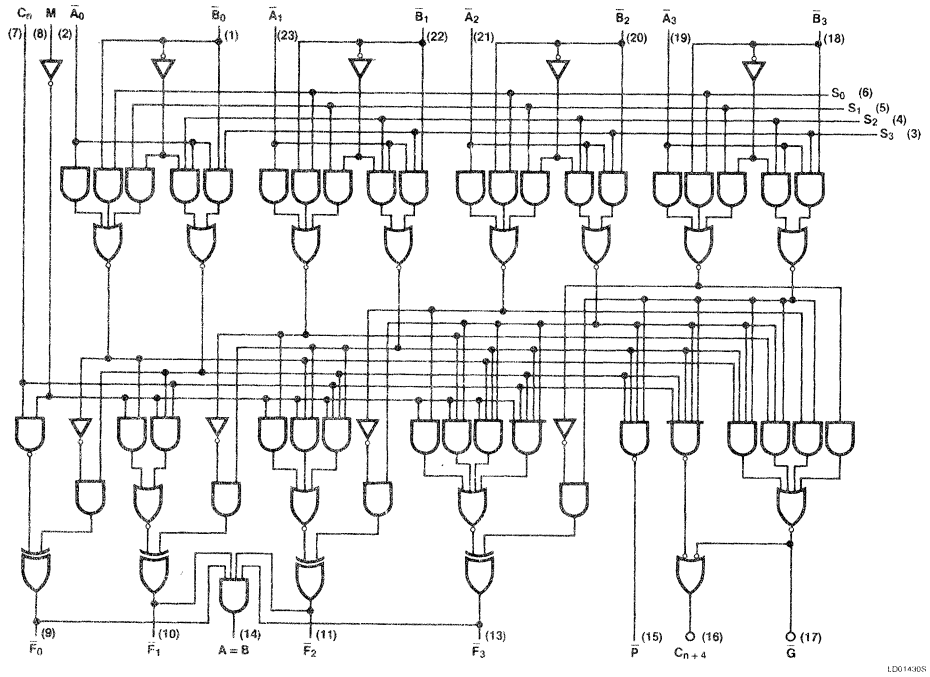
MODE SELECT—FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$A\overline{B}$	A + $\overline{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	A ⊕ B	A minus B minus 1
L	H	H	H	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}$ + B	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}$ + B	A$\overline{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$
H	L	L	L	$\overline{A}$B	A plus (A + B)
H	L	L	H	A ⊕ B	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A
H	H	H	L	AB	A$\overline{B}$ plus A
H	H	H	H	A	A

L = LOW voltage
H = HIGH voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers
Pin 14 is O.C.

SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output current	A = B			4.5	V
I_{OH}	HIGH-level output current	Any output except A = B			−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F181			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	Any output except A = B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OH}	HIGH-level output current	A = B only	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 4.5V				250	μA
I_{OS}	Short-circuit output current[3]	Any output except A = B	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX	$S_0 - S_3 = M = \overline{A}_0 - \overline{A}_3 = 4.5V$, $\overline{B}_0 - \overline{B}_3 = C_n$ = GND		43	65	mA
		I_{CCL}		$S_0 - S_3 = M = 4.5V$, $\overline{B}_0 - \overline{B}_3 = C_n = \overline{A}_0 - \overline{A}_3$ = GND		43	65	mA

NOTES:

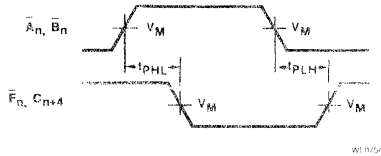
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

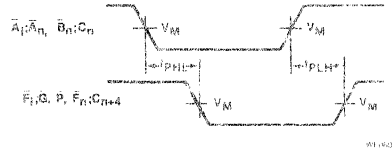
PARAMETER	TEST CONDITIONS				74F181					UNIT
	Mode	Table	Wave-form	Conditions	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
					Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} C_n to C_{n+4}	Sum Diff	I II	2	M = 0V	3.0 3.0	6.4 6.1	8.5 8.0	3.0 3.0	9.5 9.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Sum	I	1	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V	5.0 5.0	10.0 9.4	13 12	5.0 5.0	14.0 13.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Diff	II	4	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	5.0 5.0	10.8 10.0	14 13	5.0 5.0	15.0 14.0	ns
t_{PLH} Propagation delay t_{PHL} C_n to $\overline{F}_n$	Diff Sum	II I	2	M = 0V	3.0 3.0	6.7 6.5	8.5 8.5	3.0 3.0	9.5 9.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Sum	I	2	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V	3.0 3.0	5.7 5.8	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Diff	II	3	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	3.0 3.0	6.5 7.3	8.5 9.5	3.0 3.0	9.5 10.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Sum	I	2	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V	3.0 3.0	5.0 5.5	7.0 7.5	3.0 3.0	8.0 8.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Diff	II	3	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	4.0 4.0	5.8 6.5	7.5 8.5	4.0 4.0	8.5 9.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	I	2	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V	3.0 3.0	7.0 7.2	9.0 10.0	3.0 3.0	10.0 10.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Diff	II	3	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	3.0 3.0	8.2 8.0	11.0 11.0	3.0 3.0	12.0 12.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Sum		1, 2		4.0 4.0	8.0 7.8	10.5 10.0	4.0 4.0	11.5 11.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Diff		1, 2		4.5 4.5	9.4 9.4	12.0 12.0	4.5 4.5	13.0 13.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Logic	III	3	M = 4.5V	4.0 4.0	6.0 6.0	9.0 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_n$ or $\overline{B}_n$ to A = B	Diff	II	3	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V	11.0 7.0	18.5 9.8	27.0 12.5	11.0 7.0	29.0 13.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

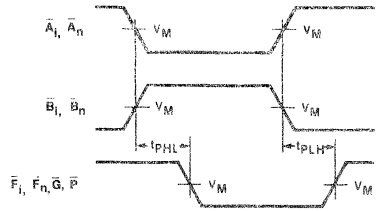
AC WAVEFORMS



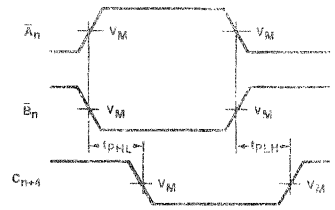
Waveform 1. Propagation Delay For Operands To Carry Output And Outputs



Waveform 2. Propagation Delays For Carry Input To Carry Output, Carry Input To Outputs, And Operands To Carry Generate Operands To Carry Generate And Carry Propagate Outputs



Waveform 3. Propagation Delay For Operands To Carry Generate And Propagate Outputs, Operands To A = B Output, And Outputs

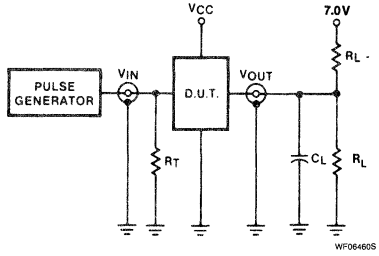


Waveform 4. Propagation Delays For Operands To Carry Output

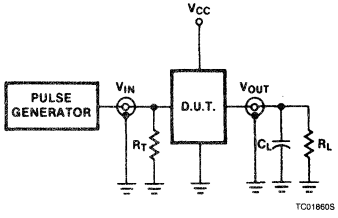
NOTE: For all waveforms, V_M = 1.5V.

6

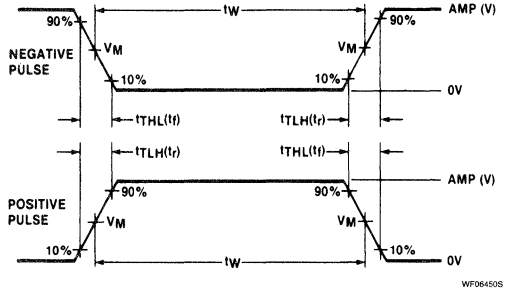
TEST CIRCUITS AND WAVEFORMS



Test Circuit For Open-Collector Outputs



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F182
Carry Lookahead Generator

Carry Lookahead Generator
Product Specification

Logic Products

FEATURES

- **Provides carry lookahead across a group of four ALU's**
- **Multi-level lookahead for high-speed arithmetic operation over long word lengths**

DESCRIPTION

The 'F182 carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH Carry input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 'F182 also has active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 = P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_2G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

The 'F182 can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F182	7.5ns	21mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F182N
Plastic SO-16	N74F182D

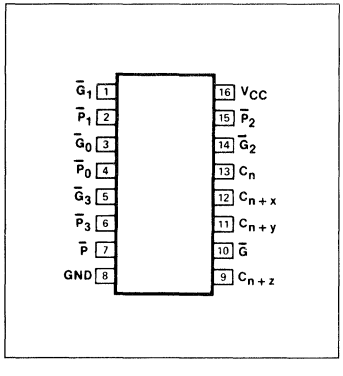
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

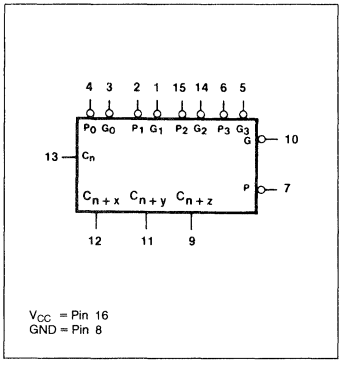
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
C_n	Carry input	1.0/2.0	20μA/1.2mA
$\overline{G}_0$, $\overline{G}_2$	Carry generate inputs (active LOW)	1.0/14.0	20μA/8.4mA
$\overline{G}_1$	Carry generate input (active LOW)	1.0/16.0	20μA/9.6mA
$\overline{G}_3$	Carry generate input (active LOW)	1.0/8.0	20μA/4.8mA
$\overline{P}_0$, $\overline{P}_1$	Carry propagate inputs (active LOW)	1.0/8.0	20μA/4.8mA
$\overline{P}_2$	Carry propagate input (active LOW)	1.0/6.0	20μA/3.6mA
$\overline{P}_3$	Carry propagate input (active LOW)	1.0/4.0	20μA/2.4mA
$C_{n+x} - C_{n+z}$	Carry outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output (active LOW)	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output (active LOW)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

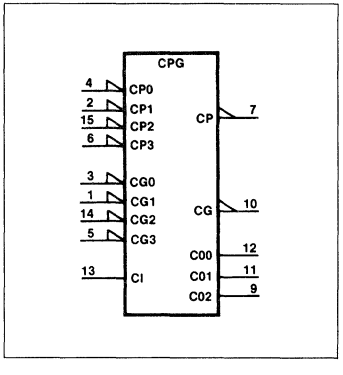
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

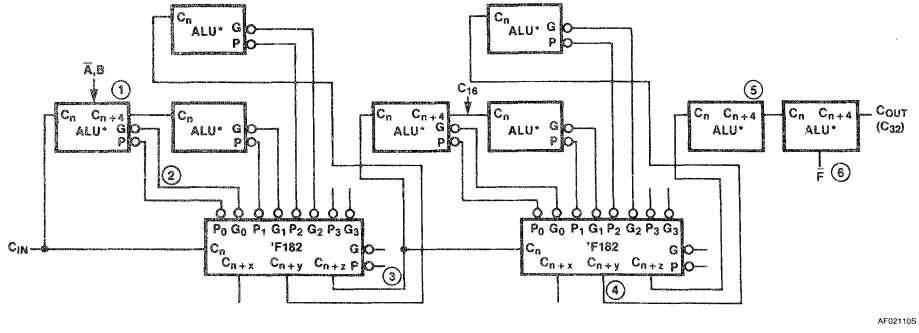


FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	L	X	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

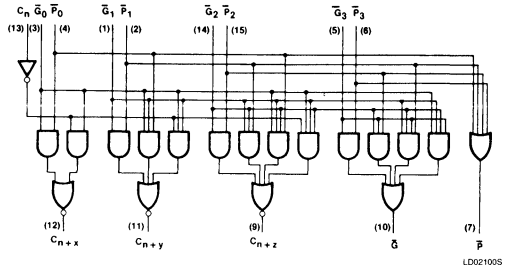
APPLICATION



*ALU's may be either 'F181, F381 or 2901A.

32-Bit ALU With Ripple Carry Between 16-Bit Lookahead ALUs

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F182 Min	74F182 Typ[2]	74F182 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	C_n	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		$\overline{G}_0$, $\overline{G}_2$					−8.4	mA
		$\overline{G}_1$					−9.6	mA
		$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$					−4.8	mA
		$\overline{P}_2$					−3.6	mA
		$\overline{P}_3$					−2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			18.4	28	mA
		I_{CCL}				23.5	36	mA

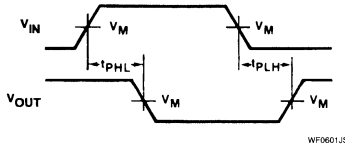
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with $\overline{G}_0$, $\overline{G}_1$, and $\overline{G}_2$ inputs at 4.5V; all other inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

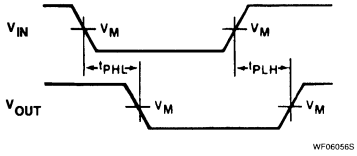
PARAMETER		TEST CONDITIONS	74F182 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F182 T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay	Waveform 2	2.5	5.0	8.0	2.5	8.5	ns
t_{PHL}	C_n to C_{n+x}, C_{n+y}, C_{n+z}		2.5	5.0	7.5	2.5	8.5	
t_{PLH}	Propagation delay	Waveform 1	2.0	5.0	7.0	1.5	8.0	ns
t_{PHL}	$\overline{P}_0$, $\overline{P}_1$ or $\overline{P}_2$, to C_{n+x}, C_{n+y}, C_{n+z}		1.5	3.5	5.0	1.5	6.0	
t_{PLH}	Propagation delay	Waveform 1	1.5	4.0	7.5	1.5	8.5	ns
t_{PHL}	$\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}		1.5	3.0	5.0	1.5	5.5	
t_{PLH}	Propagation delay	Waveform 2	2.0	7.0	10.0	1.5	11.0	ns
t_{PHL}	$\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$		3.0	5.0	7.0	2.5	8.0	
t_{PLH}	Propagation delay	Waveform 2	1.5	5.0	7.0	1.5	7.5	ns
t_{PHL}	$\overline{G}_n$ to $\overline{G}$		3.0	5.0	7.0	2.5	8.0	
t_{PLH}	Propagation delay	Waveform 2	1.5	3.5	6.0	1.5	7.5	ns
t_{PHL}	$\overline{P}_n$ to $\overline{P}$		2.5	4.0	6.0	2.5	6.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



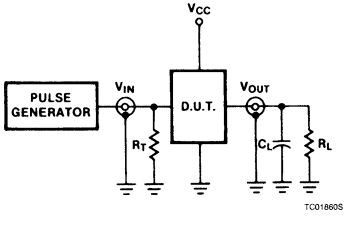
Waveform 1. For Inverting Outputs



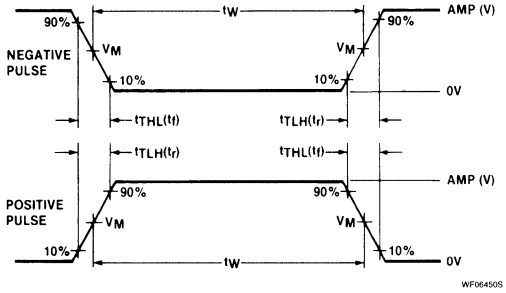
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

Logic Products

FAST 74F190, 74F191 Counters

'F190 Asynchronous Presettable BCD/Decade Up/Down Counter
'F191 Asynchronous Presettable 4-Bit Binary Up/Down Counter
Preliminary Specification

FEATURES

- **High speed—110MHz typical f_{max}**
- **Synchronous, reversible counting**
- **BCD/decade—'F190 4-bit binary—'F191**
- **Asynchronous parallel load capability**
- **Count enable control for synchronous expansion**
- **Single up/down control input**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F190	125MHz	38mA
74F191	125MHz	38mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F190N, N74F191N
Plastic SO-16	N74F190D, N74F191D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

DESCRIPTION

The 'F190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The 'F191 is similar, but is a 4-bit binary counter.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

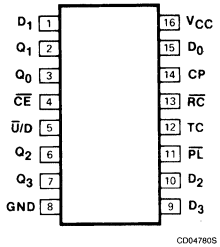
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CE}$	Count enable input (active low)	1.0/3.0	20μA/1.8mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous parallel load input (active low)	1.0/1.0	20μA/0.6mA
$\overline{U}/D$	Up/down count control input	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20μA
$\overline{RC}$	Ripple clock output (active low)	50/33	1.0mA/20μA
TC	Terminal count output (active high)	50/33	1.0mA/20μA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

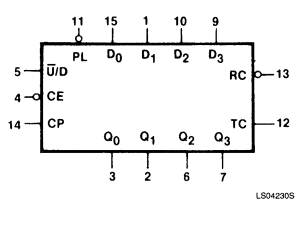
PIN CONFIGURATION

'F190



LOGIC SYMBOL

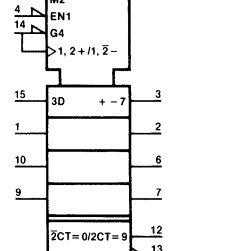
'F190



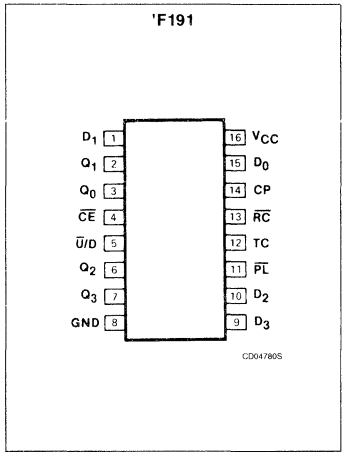
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)

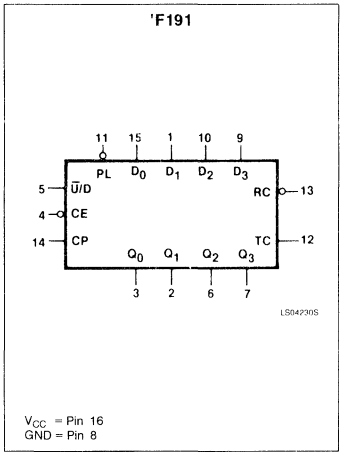
'F190



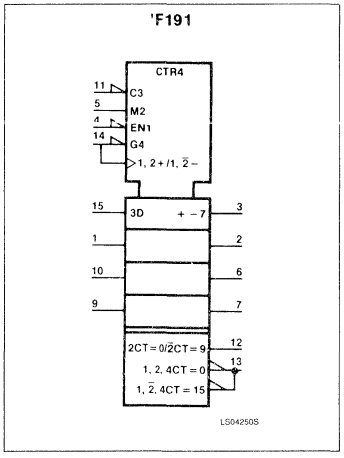
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



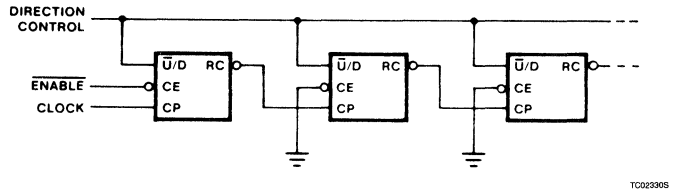
Counting is inhibited by a HIGH level on the Count Enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW, internal state changes are initiated.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode for 'F190 and reaches "15" in the count-up mode for 'F191. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

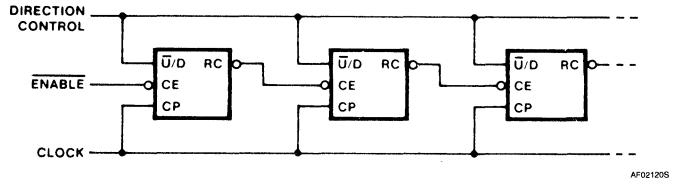
The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the RC follows the Clock Pulse (CP) delayed by two gate delays. The $\overline{RC}$ output essentially duplicates the LOW clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multi-stage counters, as indicated in Figures 1a and 1b. In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The LOW state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH, there is no such restriction on the HIGH state duration of the clock.

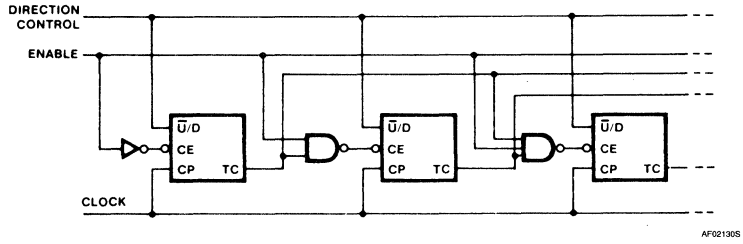
In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.



a. N-Stage Counter Using Ripple Clock



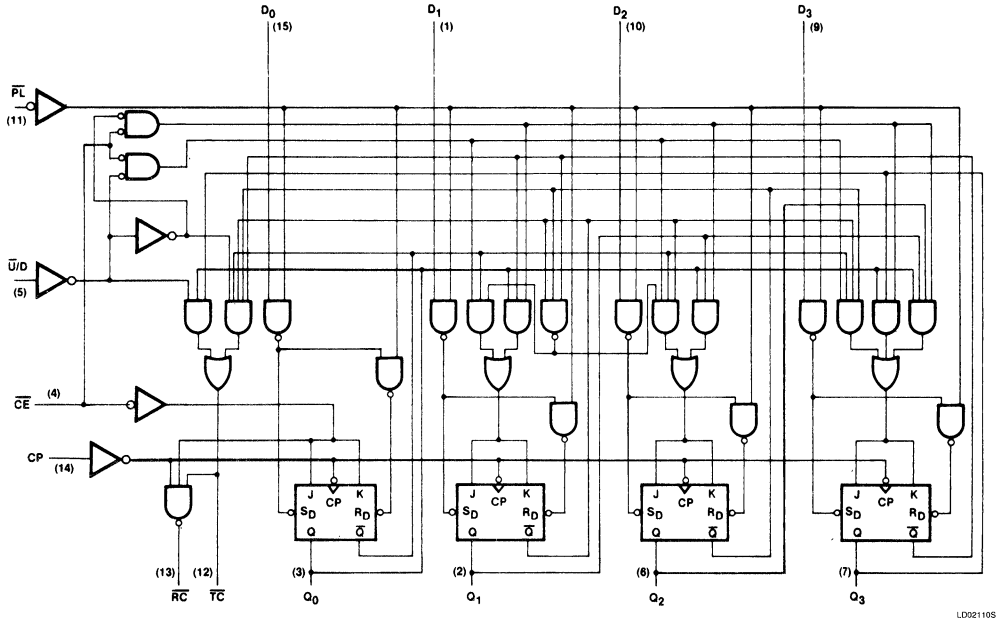
b. Synchronous N-Stage Counter Using Ripple Carry Borrow



c. Synchronous N-Stage Counter With Parallel Gated Carry Borrow

Figure 1

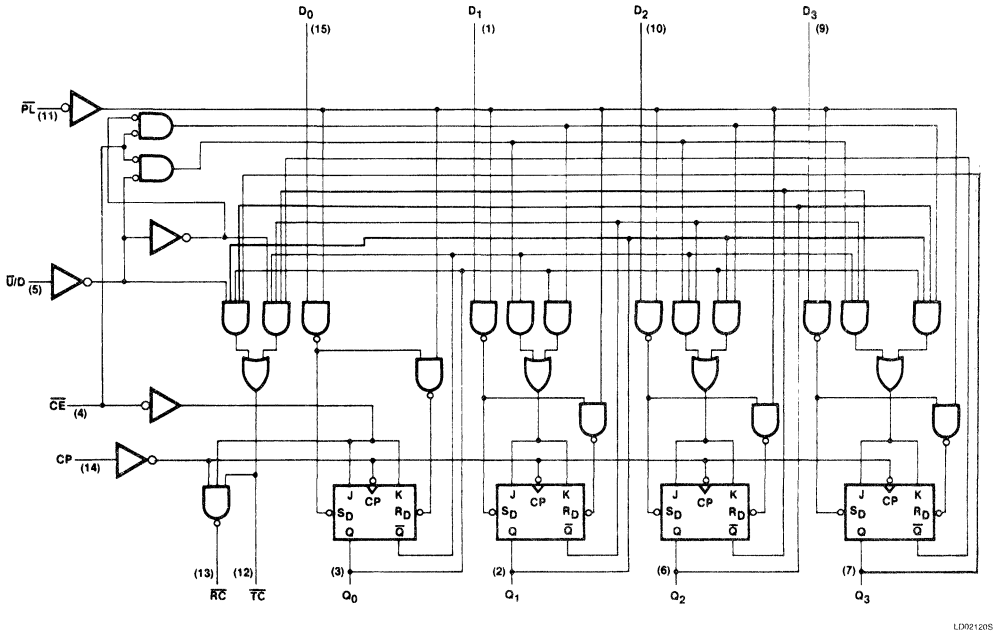
LOGIC DIAGRAM



'F190

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

LOGIC DIAGRAM



'F191

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT — FUNCTION TABLE, 'F190, 'F191

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L L	X X	X X	X X	L H	L H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE, 'F190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊓	H	X	X	H	↓	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	↓	⊓

TC AND $\overline{RC}$ FUNCTION TABLE, 'F191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓	H	H	H	H	↓	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	↓	⊓

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
⊓ = LOW pulse.
↓ = HIGH-to-LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F190, 191			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	CE input	V_{CC} = MAX, V_I = 7.0				0.3	mA
		Other inputs					0.1	mA
I_{IH}	HIGH-level input current	CE input	V_{CC} = MAX, V_I = 2.7V				60	μA
		Other inputs					20	μA
I_{IL}	LOW-level input current	CE input	V_{CC} = MAX, V_I = 0.5V				−1.8	mA
		Other inputs					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			38	55	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F190, 'F191					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100			90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 5.0		7.5 11.0	3.0 5.0	8.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$	Waveform 2	3.0 3.0		7.5 7.0	3.0 3.0	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	6.0 5.0		13.0 11.0	6.0 5.0	14.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$	Waveform 7	7.0 5.5		18.0 12.0	7.0 5.5	20.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC	Waveform 7	4.0 4.0		10.0 10.0	4.0 4.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 3	3.0 6.0		7.0 13.0	3.0 6.0	8.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to any output	Waveform 4	5.0 5.5		11.0 12.0	5.0 5.5	12.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$	Waveform 2	3.0 3.0		7.0 7.0	3.0 3.0	8.0 8.0	ns

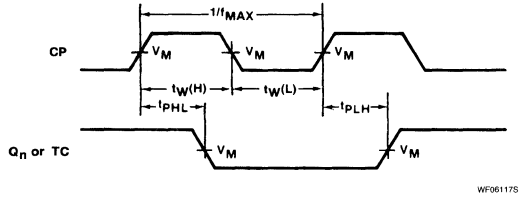
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

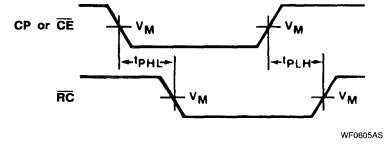
PARAMETER		TEST CONDITIONS	74F190, 'F191					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to $\overline{PL}$	Waveform 6	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{PL}$	Waveform 6	4.0 4.0			4.0 4.0		ns
$t_s(L)$	Set-up time LOW $\overline{CE}$ to CP	Waveform 8	10.0			10.0		ns
$t_h(L)$	Hold time LOW $\overline{CE}$ to CP	Waveform 8	0			0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{U}$/D to CP	Waveform 7	12 12			12 12		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{U}$/D to CP	Waveform 7	0 0			0 0		ns
$t_W(L)$	$\overline{PL}$ pulse width, LOW	Waveform 4	6.0			6.0		ns
$t_W(L)$	CP pulse width, LOW	Waveform 1	5.0			5.0		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	6.0			6.0		ns

6

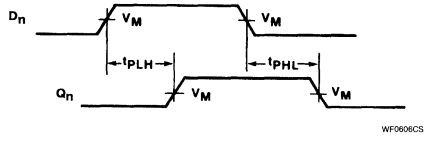
AC WAVEFORMS



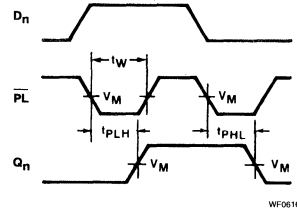
Waveform 1. Clock To Flip-Flop And Terminal Count Output Delays, Clock Pulse Width And Maximum Clock Frequency



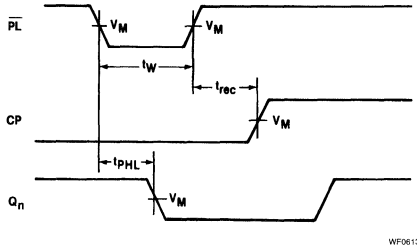
Waveform 2. Clock Or Clock Enable To Ripple Clock Output Delays



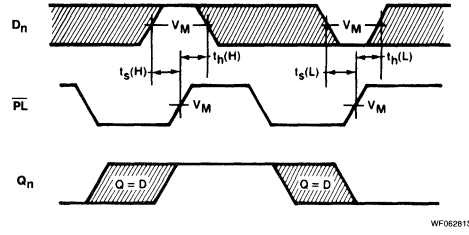
Waveform 3. Data To Flip-Flop Output Delays



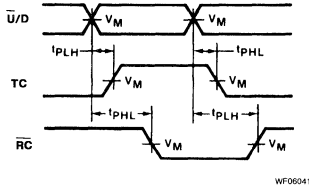
Waveform 4. Parallel Load To Any Output Delays And Parallel Load Pulse Width



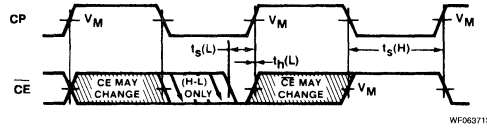
Waveform 5. Parallel Load



Waveform 6. Set-up And Hold Time For Data To Parallel Load



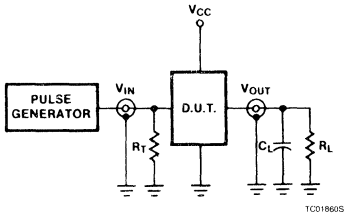
Waveform 7. U/D To RC Or TC Delays, Set-up And Hold Time For U/D To CP



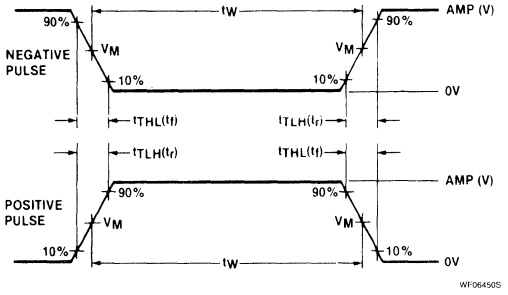
Waveform 8. Set-up And Hold Time For CE To CP

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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Signetics

Logic Products

FAST 74F192, 74F193 Counters

'F192 — Synchronous Presettable BCD Decade Up/Down Counter
'F193 — Synchronous Presettable 4-Bit Binary Down Counter
Preliminary Specification

FEATURES

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

DESCRIPTION

The 'F192 and 'F193 are 4-bit synchronous up/down counters — the 'F192 counts in BCD mode and the 'F193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either Clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up . . . if CP_D is pulsed while CP_U is held HIGH, the device will count down. Only one Clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F192	125MHz	30mA
74F193	125MHz	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F192N, N74F193N
Plastic SO-16	N74F192D, N74F193D

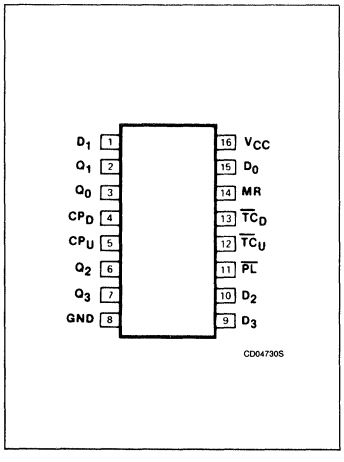
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

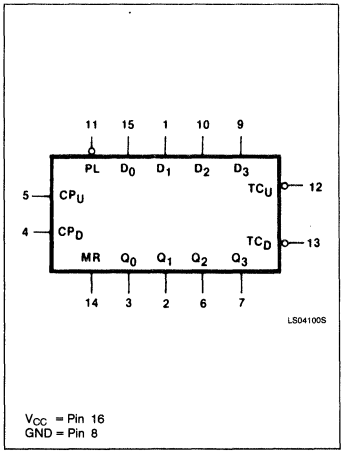
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP_U	Count up clock input (active rising edge)	1.0/2.0	20μA/1.2mA
CP_D	Count down clock input (active rising edge)	1.0/2.0	20μA/1.2mA
MR	Asynchronous master reset input (active high)	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous parallel load input (active low)	1.0/1.0	20μA/0.6mA
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active low)	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

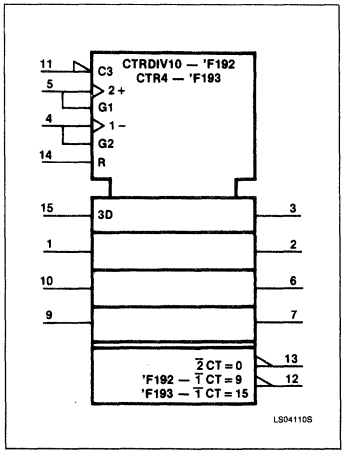
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

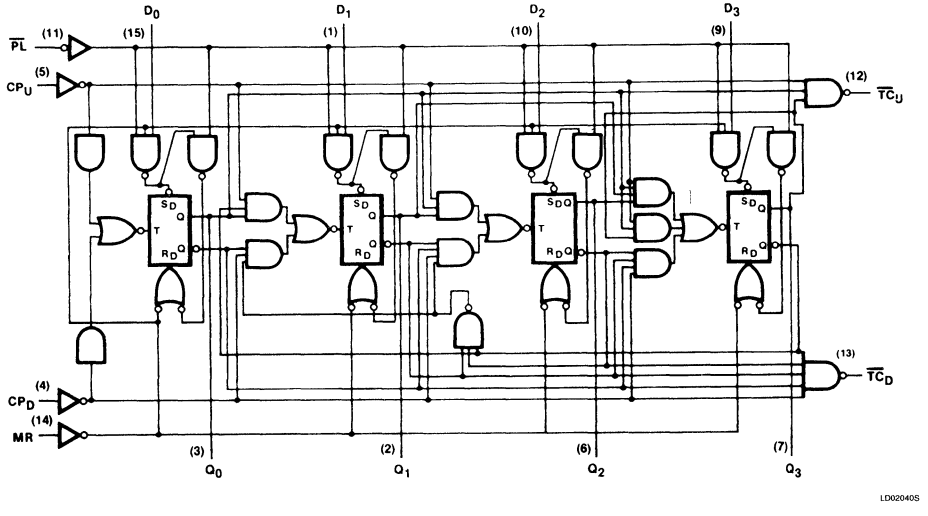


Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

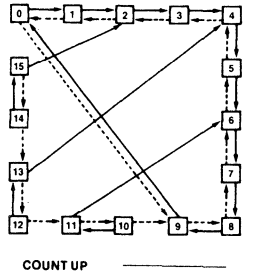
One clock should be held HIGH while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

LOGIC DIAGRAM, 'F192



V_{CC} = Pin 16
GND = Pin 8

STATE DIAGRAM, 'F192



$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$
$\overline{TC}_D = Q_0 \cdot Q_1 \cdot \overline{CP}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

Logic Equations For Terminal Count

MODE SELECT — FUNCTION TABLE, 'F192

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H	$Q_n = D_n$				H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H(1)	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H(2)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

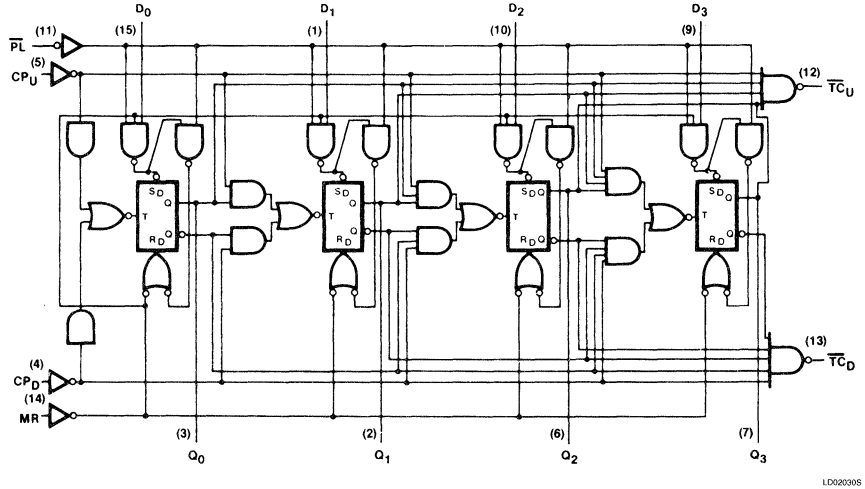
NOTES:
1. $\overline{TC}_U = CP_U$ at terminal count up (HLLH).
2. $\overline{TC}_D = CP_D$ at terminal count down (LLLL).

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9 (for the 'F192 and 15 for the 'F193), the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW.

The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

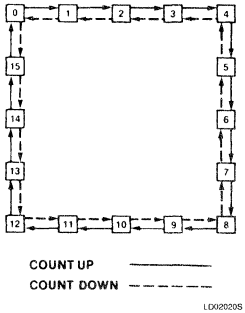
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load ($\overline{PL}$) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs LOW. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM 'F193



V_{CC} = Pin 16
GND = Pin 8

STATE DIAGRAM, 'F193



$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$
$\overline{TC}_D = Q_0 \cdot Q_1 \cdot \overline{CP}_2 \cdot Q_3 \cdot \overline{CP}_D$

Logic Equations For Terminal Count

MODE SELECT — FUNCTION TABLE, 'F193

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	L	H	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				$H^{(1)}$	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	$H^{(2)}$

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTES:
1. $TC_U = CP_U$ at terminal count up (HHHH).
2. $TC_D = CP_D$ at terminal count down (LLLL).

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F192, 'F193			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.5	V
			±5%V_{CC}		.35	.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	CP_U, CP_D			−1.2	mA
			Other inputs		−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			30	45	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with parallel load and Master Reset inputs grounded, all other inputs at 4.5V and all outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

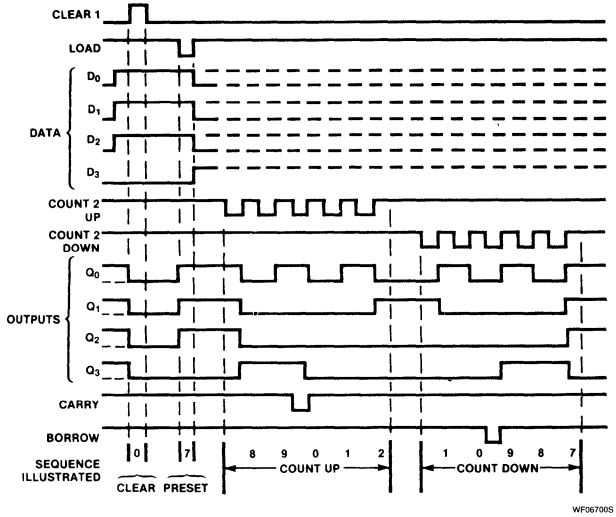
PARAMETER		TEST CONDITIONS	74F192, 'F193					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum count frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to $\overline{TC}_U$	Waveform 1	4.0 3.5	7.0 6.0	9.0 8.0	4.0 3.5	10 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n	Waveform 1	4.0 5.5	6.5 9.5	8.5 12.5	4.0 5.5	9.5 13.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	3.0 6.0	4.5 11	7.0 14.5	3.0 6.0	8.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 2	5.0 5.5	8.5 10	11 13	5.0 5.5	12 14	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 3	6.5	11	14.5	6.5	15.5	ns
t_{PLH}	Propagation delay MR to $\overline{TC}_U$	Waveform 3	6.0	10.5	13.5	6.0	14.5	ns
t_{PHL}	Propagation delay MR to $\overline{TC}_D$	Waveform 3	6.0	10.5	13.5	6.0	14.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	7.0 7.0	12 11.5	15.5 14.5	7.0 7.0	16.5 15.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	7.0 6.5	11.5 11	14.5 14	7.0 6.5	15.5 15	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

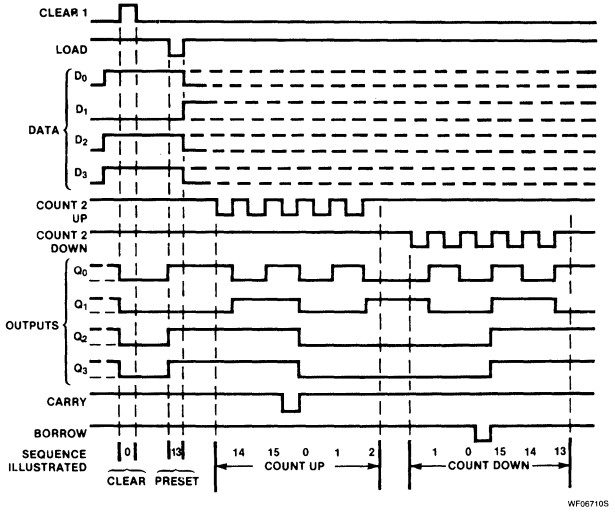
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F192, 'F193					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to $\overline{PL}$	Waveform 4	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{PL}$	Waveform 4	4.0 4.0			4.0 4.0		ns
$t_W(L)$	$\overline{PL}$ pulse width LOW	Waveform 2	6.0			6.0		ns
$t_W(L)$	CP_U or CP_D pulse width LOW	Waveform 1	5.0			5.0		ns
$t_W(L)$	CP_U or CP_D pulse width LOW (change of direction)	Waveform 1	10			10		ns
$t_W(H)$	MR pulse width HIGH	Waveform 3	6.0			6.0		ns
t_{rec}	Recovery time $\overline{PL}$ to CP_U or CP_D	Waveform 2	6.0			6.0		ns
t_{rec}	Recovery time MR to CP_U or CP_D	Waveform 3	4.0			4.0		ns

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



a. 'F192 Decade Counter

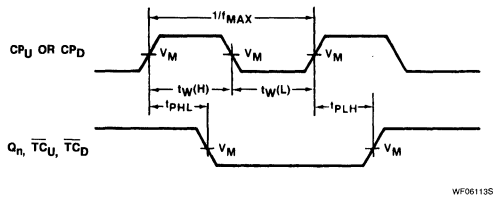


b. 'F193 Binary Counter

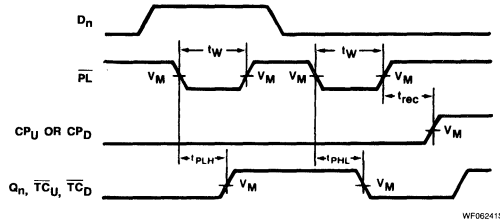
NOTES:
1. Clear overrides load data and count inputs.
2. When counting up, count-down input must be HIGH; when counting down, count-up input must be HIGH.

6

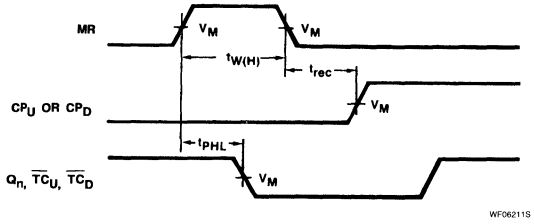
AC WAVEFORMS



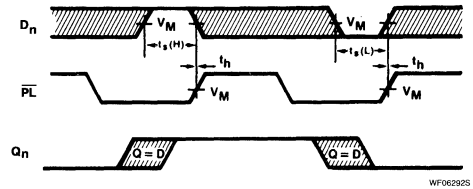
Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Parallel Load Pulse Width, Parallel Load To Output Delays, And Parallel Load To Clock Recovery Time



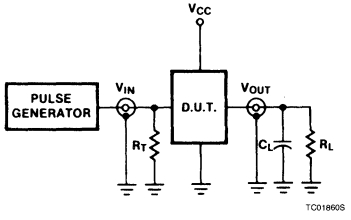
Waveform 3. Master Reset Pulse Width, Master Reset To Output Delay & Master Reset To Clock Recovery Time



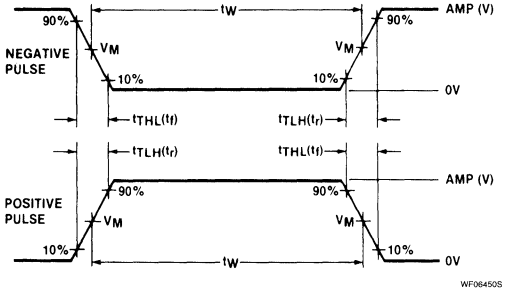
Waveform 4. Set-up And Hold Times Data To Parallel Load (PL)

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F194
Shift Register

4-Bit Bidirectional Universal Shift Register
Product Specification

Logic Products

FEATURES
- **Shift left and shift right capability**
- **Synchronous parallel and serial data transfers**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous Master Reset**
- **Hold (do nothing) mode**

DESCRIPTION
The functional characteristics of the 'F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical) for 74F, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F194	150MHz	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F194N
Plastic SO-16	N74F194D

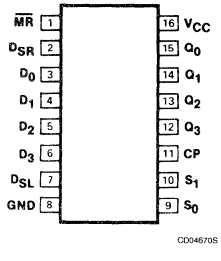
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

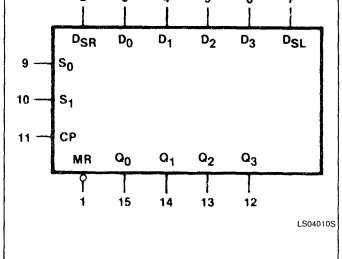
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode control inputs	1.0/1.0	20μA/0.6mA
D_{SR}	Serial data input (shift right)	1.0/1.0	20μA/0.6mA
D_{SL}	Serial data input (shift left)	1.0/1.0	20μA/0.6mA
C_P	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous master reset (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Parallel outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

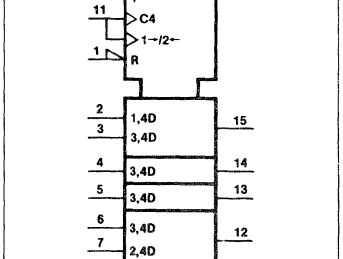
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Shift Register | FAST 74F194

The 'F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode Select and Data inputs on the 'F194 are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one set-up time prior to the positive transition of the clock pulse. Signals on the Select, Parallel Data ($D_0 - D_3$) and Serial Data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only the recommended set-up and hold times, with respect to the clock rising edge, are observed.

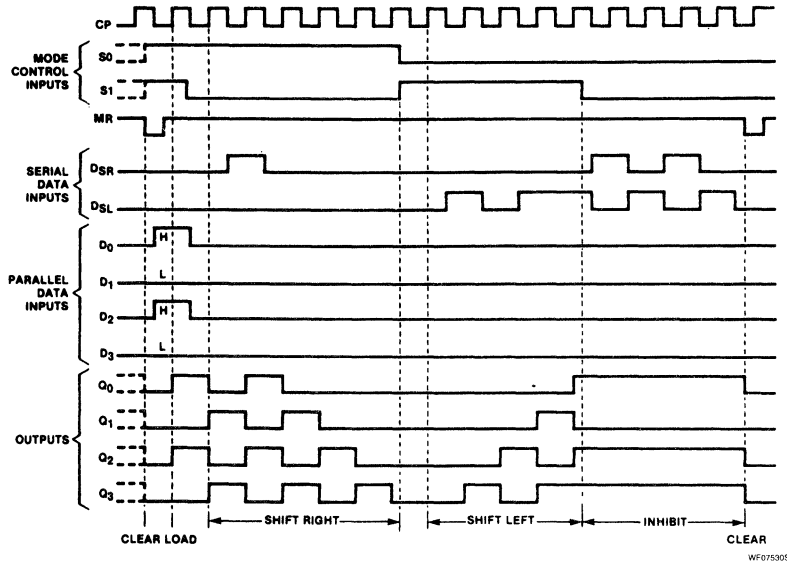
The four Parallel Data inputs ($D_0 - D_3$) are D-type inputs. Data appearing on $D_0 - D_3$ inputs when S_0 and S_1 are HIGH is transferred to the $Q_0 - Q_3$ outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW.

MODE SELECT — FUNCTION TABLE

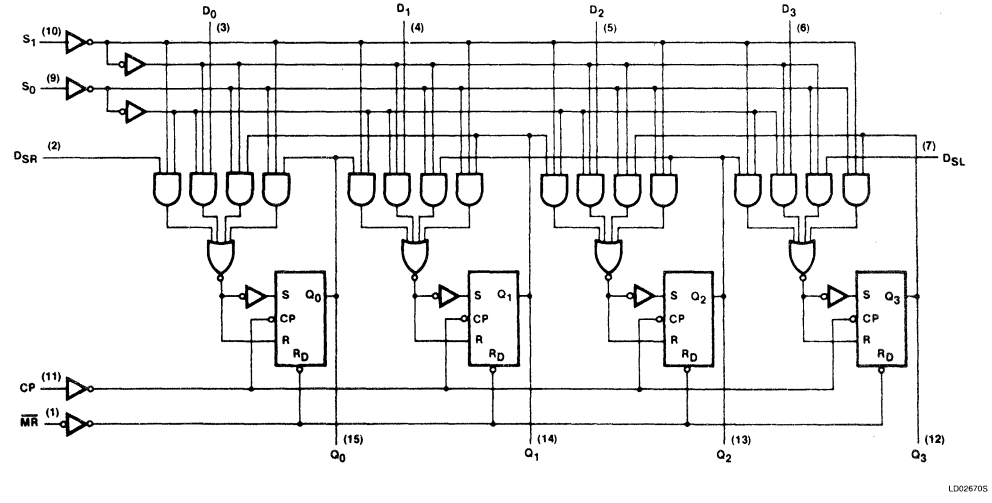
OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift left	†	H	h	l	X	l	X	q_1	q_2	q_3	L
	†	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift right	†	H	l	h	l	X	X	L	q_0	q_1	q_2
	†	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel load	†	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
† = LOW-to-HIGH clock transition.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



LOGIC DIAGRAM



VCC = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F194			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage[3]	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	±10%V_{CC}		.35	.5	V
			±5%V_{CC}		.35	.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[4]	V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current[5] (total)	V_{CC} = MAX			33	46	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Output HIGH state will change to LOW state if an external voltage of less than 0.0V is applied.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. With all outputs open, D_I inputs grounded and 4.5V applied to S_0, S_1, MR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

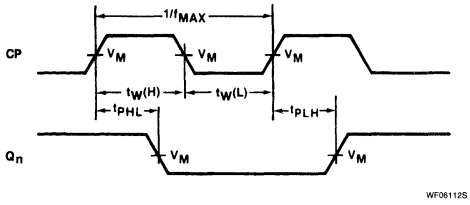
PARAMETER		TEST CONDITIONS	74F194					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5	8.6	12	4.5	14	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

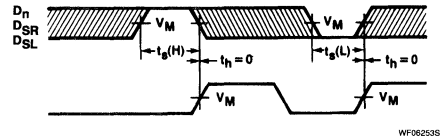
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F194					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_w(H)$	Clock pulse width, HIGH	Waveform 1	5.0			5.5		ns
$t_w(L)$	MR pulse width, LOW	Waveform 3	5.0			5.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, $D_0 - D_3$, D_{SR}, D_{SL} to CP	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW, $D_0 - D_3$, DSR, DSL to CP		0 0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW, S_n to CP	Waveform 4	8.0 8.0			9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW, S_n to CP		0 0			0 0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	7.0			8.0		ns

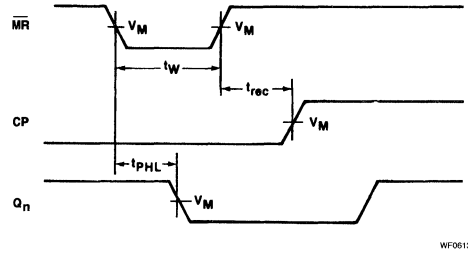
AC WAVEFORMS



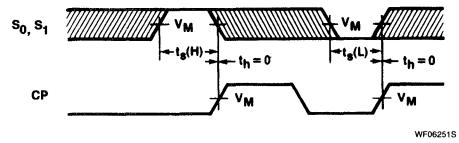
Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Data Set-up And Hold Times



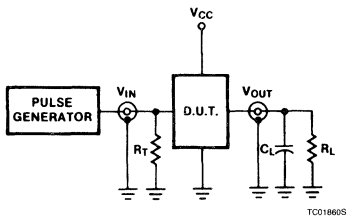
Waveform 3. Master Reset Pulse Width, Master Reset To Output Delay & Master Reset To Clock Recovery Time



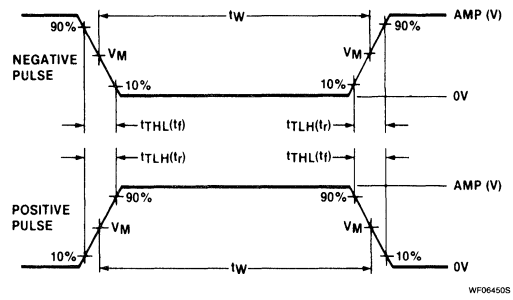
Waveform 4. Set-up And Hold Times For S_0 And S_1 Inputs

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_r	t_f
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F195
Shift Register

4-Bit Parallel Access Shift Register
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in LOW and HIGH states)**
- **Shift right and parallel load capability**
- **J – $\overline{K}$ (D) inputs to first stage**
- **Complement output from last stage**
- **Asynchronous Master Reset**

DESCRIPTION

The functional characteristics of the 'F195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The 'F195 operates on two primary modes: shift right ($Q_0 - Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted 1 bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F195	115MHz	45mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F195N
Plastic SO-16	N74F195D

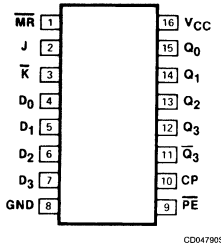
NOTES:
1. SO package is surface mounted micro-miniature DIP
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

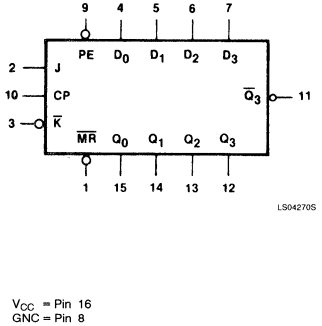
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
$D_0 - D_3$	Parallel data inputs	1.0/0.033	20μA/20μA
$\overline{PE}$	Parallel enable input	1.0/0.033	20μA/20μA
$\overline{MR}$	Asynchronous master reset	2.0/0.066	40μA/40μA
J, $\overline{K}$	J – $\overline{K}$ or D type serial inputs	1.0/0.033	20μA/20μA
$Q_0 - Q_3$, $\overline{Q}_3$	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

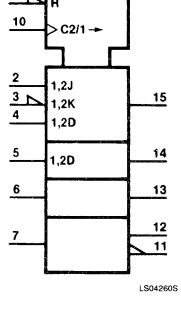
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Shift Register | FAST 74F195

The J and $\overline{K}$ inputs provide the flexibility of the JK type input for special applications and by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_3$) is transferred to the respective $Q_0 - Q_3$ outputs. Shift left operation ($Q_3 - Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input low.

All parallel and serial data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. The 'F195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the set-up and release time requirements.

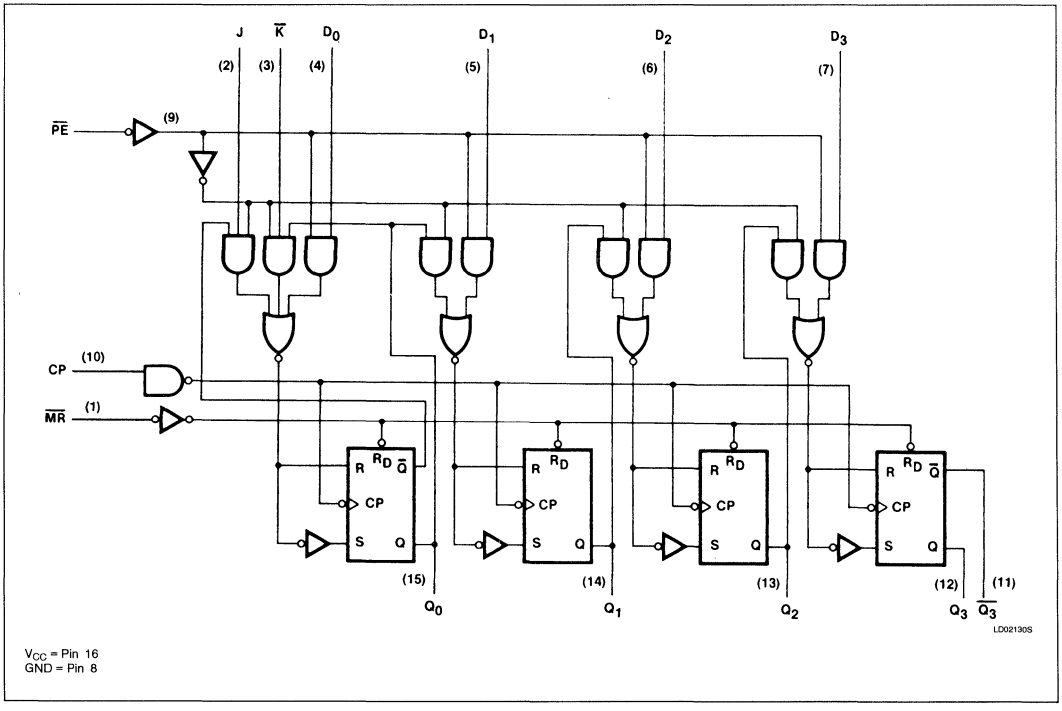
A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT - FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
Shift, set first stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, reset first stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, toggle first stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, retain first stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = HIGH voltage level
L = LOW voltage level
X = Don't care
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F195 Min	74F195 Typ[2]	74F195 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.5	V
				±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	Others	V_{CC} = MAX, V_I = 2.7V			1	20	μA
		$\overline{MR}$					40	μA
I_{IL}	LOW-level input current	Others	V_{CC} = MAX, V_I = 0.5V				−20	μA
		$\overline{MR}$					−40	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			45	58	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With all outputs open, $\overline{PE}$ grounded, and 4.5V applied to the J, $\overline{K}$, and Data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V to $\overline{MR}$, and then a momentary ground followed by 4.5V to clock.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

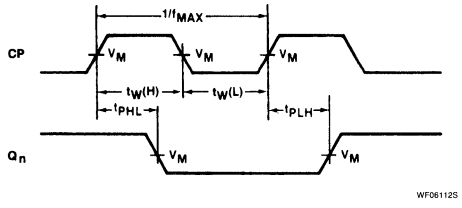
PARAMETER			TEST CONDITIONS	74F195					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	$\overline{PE}$ mode	Waveform 1	120	130		110		MHz
		Toggle mode		100	115		90		
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	9.5 9.0	4.0 4.0	10.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_3$		Waveform 1	7.0 4.5	10.0 7.0	13.0 9.0	7.0 4.0	13.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n		Waveform 2	5.0	7.5	10.5	5.0	11.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_3$		Waveform 2	7.0	10.0	13.5	7.0	14.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

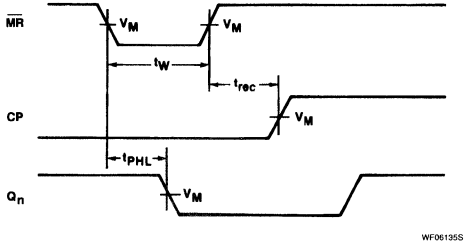
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F195					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW J, $\overline{K}$ and D_n to CP	Waveform 3	4 4			4 4		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW J, $\overline{K}$ and D_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{PE}$ to CP	Waveform 4	3 4			3 5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_w(H)$	CP pulse width, HIGH	Waveform 1	6			6		ns
$t_w(L)$	$\overline{MR}$ pulse width, LOW	Waveform 2	5			5		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	6			6		ns

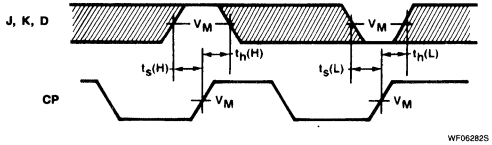
AC WAVEFORMS



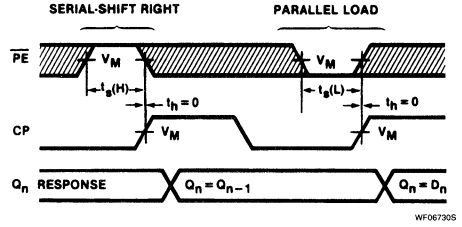
Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay & Master Reset To Clock Recovery Time



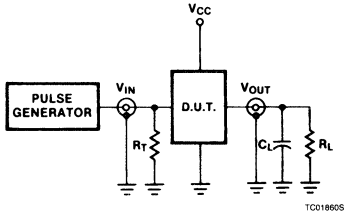
Waveform 3. Data Set-up And Hold Times



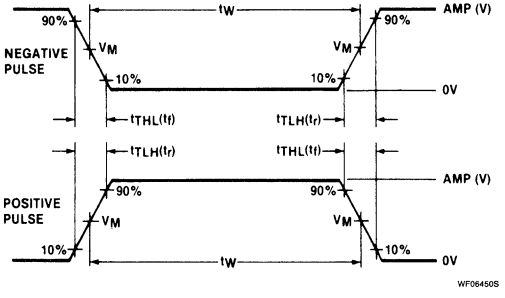
Waveform 4. Set-up And Hold Times Parallel Enable To Clock

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F198
Shift Register

8-Bit Bidirectional Universal Shift Register
Preliminary Specification

Logic Products

DESCRIPTION

This bidirectional register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit contains 87 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

Parallel (broadside) Load

Shift Right (in the direction Q_A toward Q_H)

Shift Left (in the direction Q_H toward Q_A)

Inhibit Clock (do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, HIGH. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the Clock input. During loading, serial data flow is inhibited.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F198	MHz	mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F198N
Plastic SOL-24	N74F198D

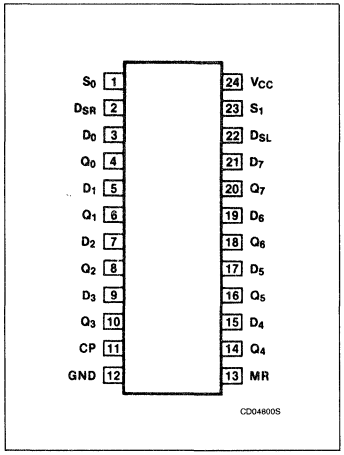
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

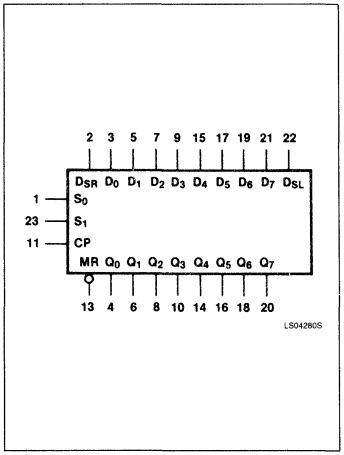
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$S_0 - S_1$	Mode control inputs	1.0/1.0	20μA/0.6mA
D_{SR}	Serial data input (shift right)	1.0/1.0	20μA/0.6mA
D_{SL}	Serial data input (shift left)	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous master reset (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Parallel outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

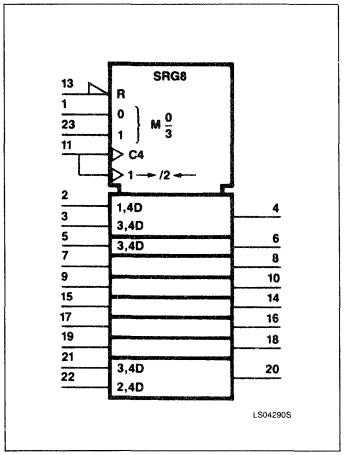
PIN CONFIGURATION



LOGIC SYMBOL



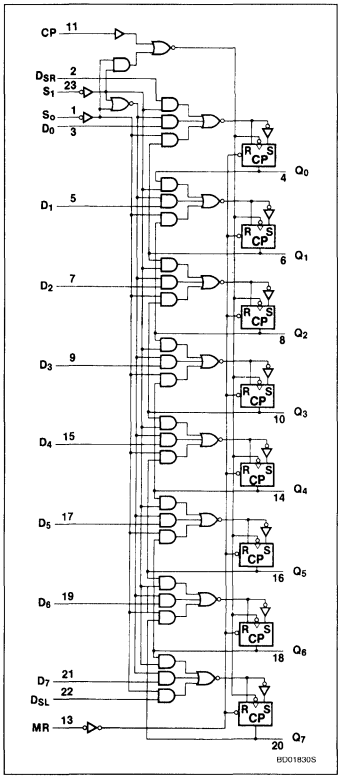
LOGIC SYMBOL (IEEE/IEC)



Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is HIGH and S_1 is LOW. Serial data for this mode is entered at the shift-right data input. When S_0 is LOW and S_1 is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW. The mode controls should be changed only while the Clock input is HIGH.

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				
$\overline{MR}$	Mode		CP	Serial		Parallel	Q_A	Q_B	...	Q_G	Q_H
	S_1	S_0		Left	Right	A...H					
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}
H	H	H	↑	X	X	a...h	a	b		g	h
H	L	H	↑	X	H	X	H	Q_{An}		Q_{Fn}	Q_{Gn}
H	L	H	↑	X	L	X	L	Q_{An}		Q_{Fn}	Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	H
H	H	L	↑	L	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	L
H	L	L	X	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}

H = HIGH level (steady state)
L = LOW level (steady state)
X = Irrelevant (any input, including transition)
↑ = Transition from LOW-to-HIGH level
a...h = The level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = The level of Q_A, Q_B, Q_G or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = The level of Q_A, Q_B, etc., respectively, before the most recent ↑ transition of the clock.

6

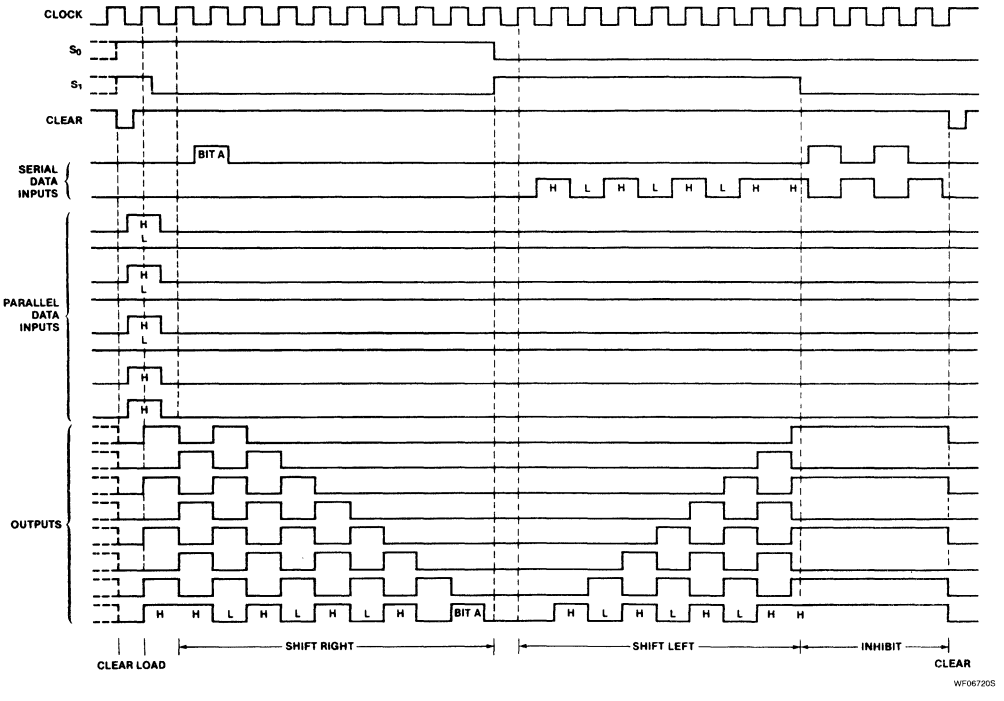
ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

TIMING DIAGRAM



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F198 Min	74F198 Typ[2]	74F198 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.9	2.8	mA
		I_{CCL}		V_{IN} = 4.5V		6.8	10.2	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

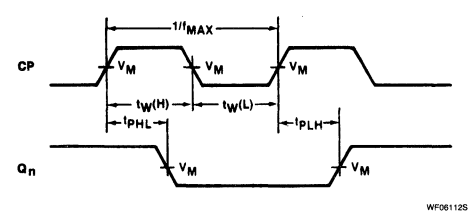
PARAMETER		TEST CONDITIONS	74F198 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			74F198 T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	Waveform 1	105			90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.5 3.5		7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay, MR to Q_n	Waveform 2	4.5		12	4.5	14	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

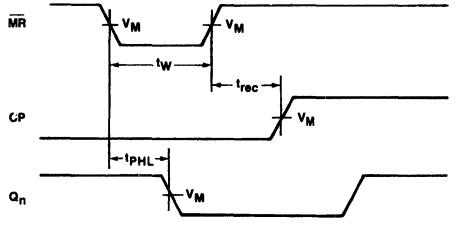
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F198					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, D_{SR}, D_{SL} to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW, D_{SR}, D_{SL} to CP	Waveform 3	0 0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW S_n to CP	Waveform 4	8.0 8.0			9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S_n to CP	Waveform 4	0 0			0 0		ns
$t_W(H)$	Clock pulse width, HIGH	Waveform 1	5.0			5.5		ns
$t_W(L)$	MR pulse width, LOW	Waveform 2	5.0			5.0		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	7.0			8.0		ns

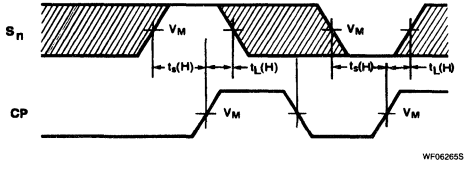
AC WAVEFORMS



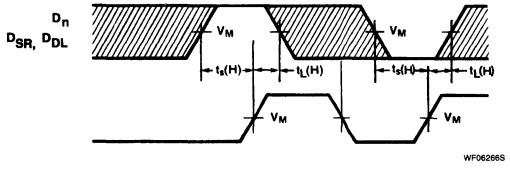
Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



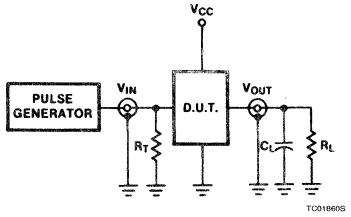
Waveform 3. Data Set-up And Hold Times



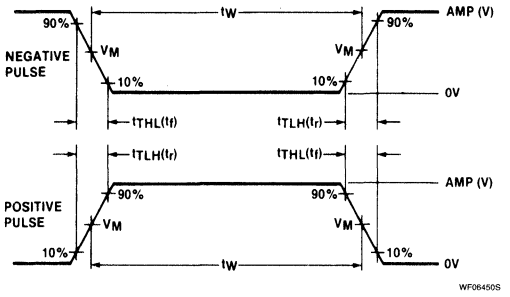
Waveform 4. Set-up And Hold Times For S_0 And S_1 Inputs

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F199
Shift Register

8-Bit Parallel-Access Shift Register
Preliminary Specification

Logic Products

FEATURES
- **Buffered clock and control inputs**
- **Shift right and parallel load capability**
- **Fully synchronous data transfers**
- **J – $\overline{K}$(D) Inputs to first stage**
- **Clock enable for hold (do nothing) mode**
- **Asynchronous Master Reset**

DESCRIPTION
The functional characteristics of the 'F199 8-bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 'F199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2$ following each LOW-to-HIGH clock transition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F199	120MHz	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F199N
Plastic SOL-24	N74F199D

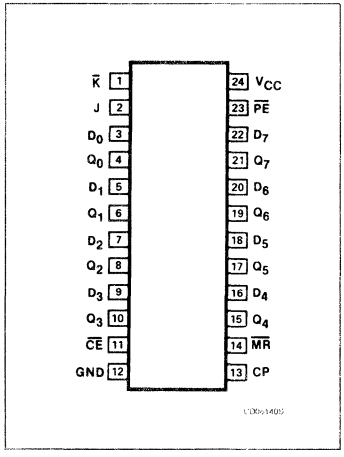
NOTES:
1. SO package is surface-mounted microminiature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

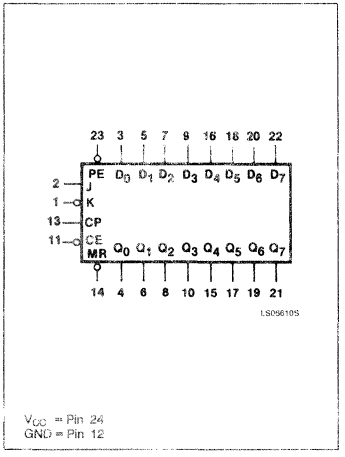
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Parallel data inputs	1.0/1.0	20μA/0.6mA
J, $\overline{K}$	J and K inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input	1.0/1.0	20μA/0.6mA
$\overline{CE}$	Clock enable input	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Parallel outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

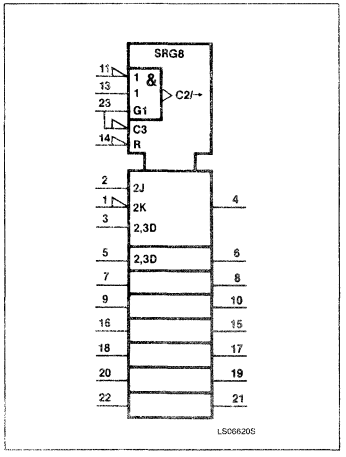
PIN CONFIGURATION



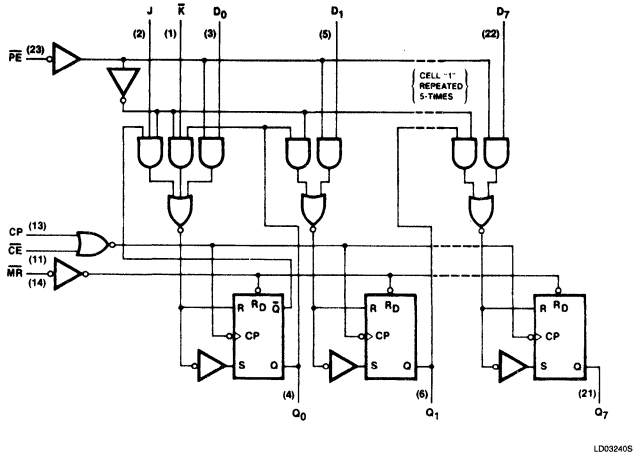
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
( ) = Pin Number

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS							OUTPUTS
	$\overline{MS}$	CP	$\overline{CE}$	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0 Q_1 ... Q_6 Q_7
Reset (clear)	L	X	X	X	X	X	X	L L ... L L
Shift, Set First Stage	H	↑	l	h	h	h	X	H q_0 ... q_5 q_6
Shift, Reset First Stage	H	↑	l	h	l	l	X	L q_0 ... q_5 q_6
Shift, Toggle First Stage	H	↑	l	h	h	l	X	$\overline{q}_0$ q_0 ... q_5 q_6
Shift, Retain First Stage	H	↑	l	h	l	h	X	q_0 q_0 ... q_5 q_6
Parallel Load	H	↑	l	l	X	X	d_n	d_0 d_1 ... d_6 d_7
Hold (do nothing)	H	↑	h[1]	X	X	X	X	q_0 q_1 ... q_6 q_7

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTE:
The LOW-to-HIGH transition of $\overline{CE}$ should only occur while CP is HIGH for conventional operation.

The J and $\overline{K}$ inputs provide the flexibility of the J – $\overline{K}$ type input for special applications and, by tying the two pins together, the simple D-type input for general applications.

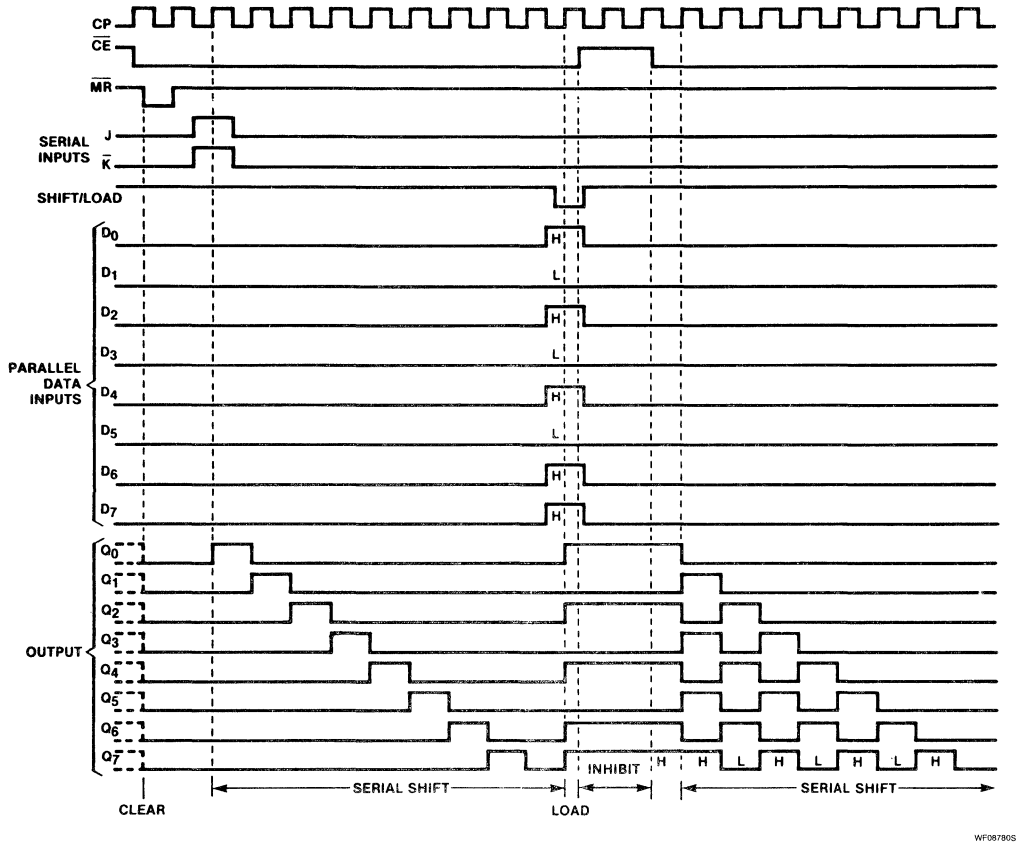
The device appears as eight common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_7$) is transferred to the respective $Q_0 - Q_7$ outputs.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The 'F199 utilizes edge-triggered, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the set-up and release time requirements. The clock input is a gated OR structure which allows one input to be used as an active-LOW Clock Enable ($\overline{CE}$) input.

The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for conventional operation.

A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clear the register asynchronously forcing all bit positions to a LOW state.

TIMING DIAGRAM



Typical Clear, Load, Right-Shift, Left-Shift, Inhibit And Clear Sequences

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F199			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, J = $\overline{K}$ = D_n = 4.5V, CP = $\overline{CE}$ = $\overline{MR}$ = $\overline{PE}$ = GND			40	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

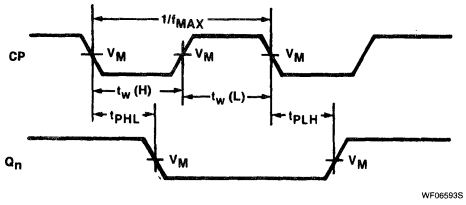
PARAMETER		TEST CONDITIONS	74F199					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	Waveform 1	105	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.5 3.5		7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5		12	4.5	14	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

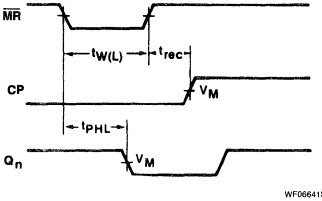
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F199					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW J, $\overline{K}$ to CP	Waveform 3	4.0 4.0			4.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW J, $\overline{K}$ to CP	Waveform 3	0 0			1.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CE}$ to CP	Waveform 3	8.0 8.0			9.0 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CE}$ to CP	Waveform 3	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{PE}$ to CP	Waveform 3	8.0 8.0			9.0 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$ to CP	Waveform 3	0 0			0 0		ns ns
$t_w(H)$	CP Pulse Width,	Waveform 1	5.0			5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW	Waveform 2	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			8.0		ns ns

AC WAVEFORMS

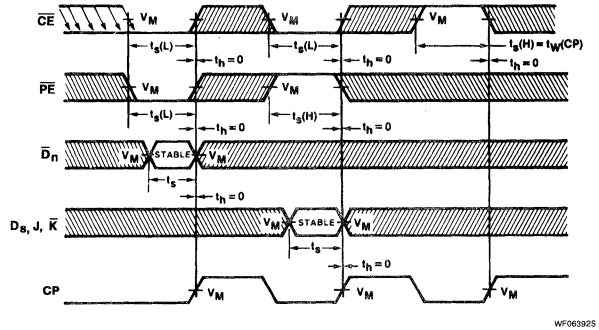


Waveform 1. Clock To Output Delays, Clock Pulse Width, And Maximum Clock Frequency



Condition: MR = HIGH

Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time

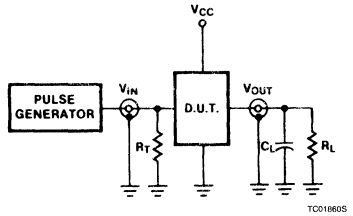


NOTE:
1. The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.
2. The shaded areas indicate when the input is permitted to change for predictable performance.
3. The changing output assumes internal Q_6 opposite state from Q_7.

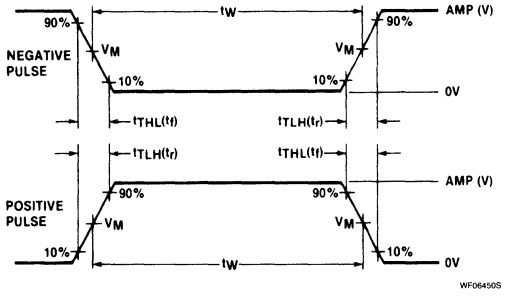
Waveform 3. Set-up And Hold Time For $\overline{PE}$, D_n, D_s, And $\overline{CE}$ To CP

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

FAST 74F240, 74F241
Buffers

'F240 Octal Inverter Buffer (3-State)
'F241 Octal Buffer (3-State)
Product Specification

Logic Products

FEATURES
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION
The 'F240 and 'F241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}$, each controlling four of the 3-state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3ns	37mA
74F241	5.0ns	53mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F240N, N74F241N
Plastic SOL-20	N74F240D, N74F241D

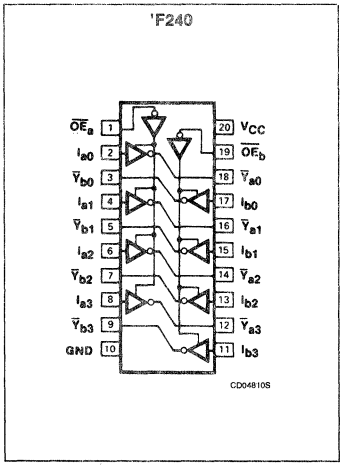
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

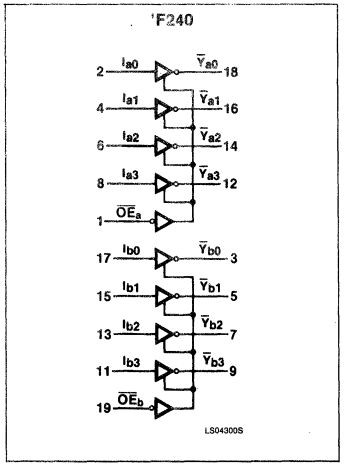
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_a$, $\overline{OE}_b$	3-State output enable input (active HIGH)	1.0/1.67	20μA/1.0mA
OE_b	3-State output enable input (active LOW)	1.0/1.67	20μA/1.0mA
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs ('F240)	1.0/1.67	20μA/1.0mA
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs ('F241)	1.0/2.67	20μA/1.6mA
$\overline{Y}_a$, $\overline{Y}_b$ ('F240) Y_a, Y_b ('F241)	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

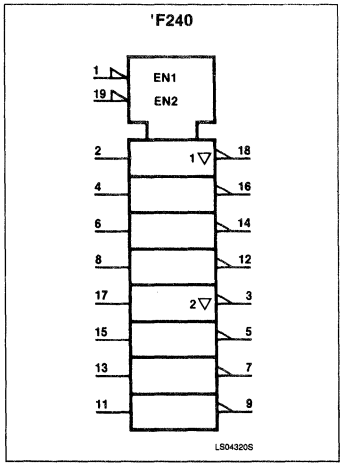
PIN CONFIGURATION



LOGIC SYMBOL

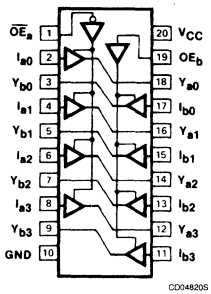


LOGIC SYMBOL (IEEE/IEC)



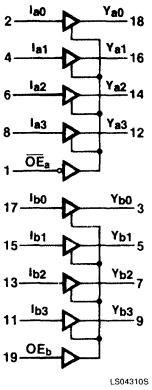
PIN CONFIGURATION

'F241



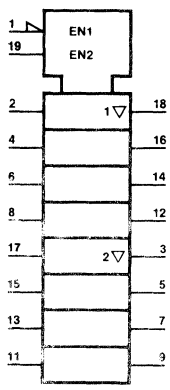
LOGIC SYMBOL

'F241



LOGIC SYMBOL (IEEE/IEC)

'F241



FUNCTION TABLE, 'F240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

FUNCTION TABLE, 'F241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F240, 241			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.35	.50	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	'F240 All inputs	V_{CC} = MAX, V_I = 0.5V				−0.6	−1.0	mA
		'F241 $\overline{OE}_a$, OE_b					−0.6	−1.0	mA
		'F241 I_{a0} − I_{a3}, I_{b0} − I_{b3}					−0.6	−1.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 2.4V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 0.5V				−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V			−100	−150	−225	mA
I_{CC}	Supply current[4] (total)	'F240	V_{CC} = MAX	I_{CCH}			12	18	mA
				I_{CCL}			50	70	mA
				I_{CCZ}			35	45	mA
		'F241		I_{CCH}			40	60	mA
				I_{CCL}			60	90	mA
				I_{CCZ}			60	90	mA

NOTES:

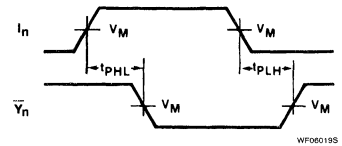
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

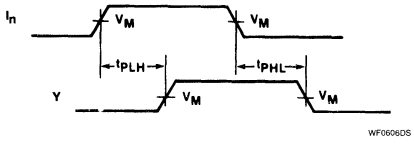
PARAMETER		TEST CONDITIONS	74F240, 241					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output ('F240)	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output enable time ('F240)	Waveform 2 Waveform 3	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time ('F240)	Waveform 2 Waveform 3	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Data to output ('F241)	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time ('F241)	Waveform 2 Waveform 3	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time ('F241)	Waveform 2 Waveform 3	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

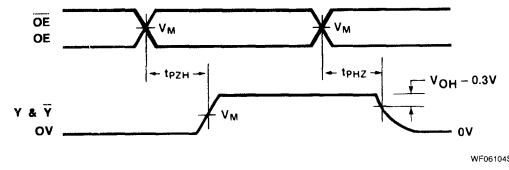
AC WAVEFORMS



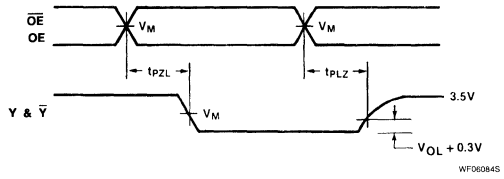
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



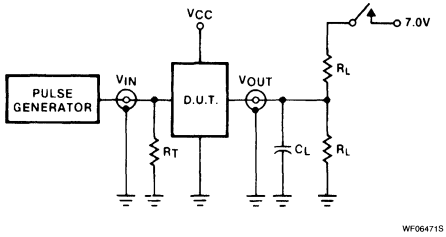
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



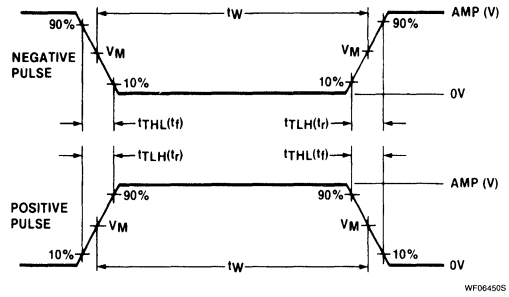
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F242, 74F243
Transceivers

'F242 Quad Transceiver, Inverting (3-State)
'F243 Quad Transceiver (3-State)
Product Specification

Logic Products

FUNCTION TABLE, 'F242

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	$B = \overline{A}$
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	$A = \overline{B}$	INPUT

FUNCTION TABLE, 'F243

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	B = A
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	A = B	INPUT

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state
(a) = This condition is not allowed due to excessive currents.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F242	4.3ns	31.2mA
74F243	4.0ns	66mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F242N, N74F243N
Plastic SO-14	N74F242D, N74F243D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

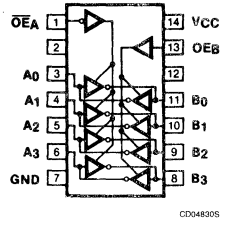
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_A$	Enable input (active LOW)	1.0/1.67	20μA/1mA
OE_B	Enable input (active HIGH)	1.0/1.67	20μA/1mA
A_n, B_n	Inputs ('F242)	3.5/1.67	70μA/1mA
A_n, B_n	Inputs ('F243)	3.5/2.67	70μA/1.6mA
A_n, B_n	Outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

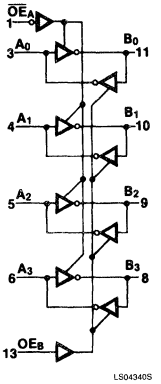
PIN CONFIGURATION

'F242



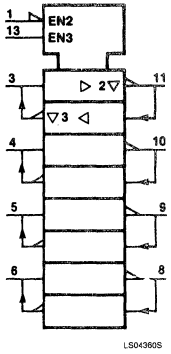
LOGIC SYMBOL

'F242



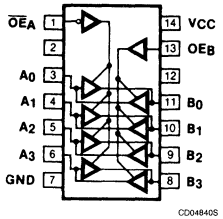
LOGIC SYMBOL (IEEE/IEC)

'F242



PIN CONFIGURATION

'F243



LOGIC SYMBOL

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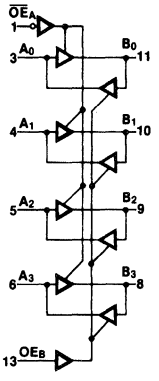

LOGIC SYMBOL (IEEE/IEC)

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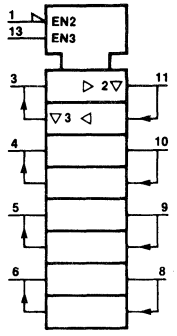


ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER				TEST CONDITIONS[1]			74F242, 74F243			UNIT
							Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4	3.4		V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10%V_{CC}	2.0	3.0		V
						±5%V_{CC}	2.0	3.0		V
V_{OL}	LOW-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.40	.50	V
					I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$A_0 - A_3$, $B_0 - B_3$		V_{CC} = 5.5V, V_I = 5.5V					100	μA
		$\overline{OE}_A$, OE_B		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current for $\overline{OE}_A$ and OE_B inputs only			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current for $\overline{OE}_A$ and OE_B inputs only			V_{CC} = MAX, V_I = 0.5V					−1	mA
I_{OZH} + I_{IH}	Off-state output current HIGH-level voltage applied			V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					70	μA
I_{OZL} + I_{IL}	Off-state output current, LOW-level voltage applied		'F242	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−1.0	mA
			'F243						−1.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F242	I_{CCH}	V_{CC} = MAX				22	35	mA
			I_{CCL}					40	55	mA
			I_{CCZ}					32	45	mA
		'F243	I_{CCH}					64	80	mA
			I_{CCL}					64	90	mA
			I_{CCZ}					71	90	mA

NOTES:

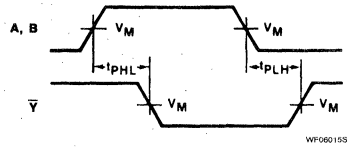
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open and transceivers enabled in one direction only, or with all transceivers disabled.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

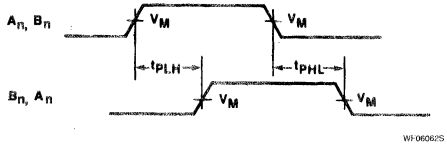
PARAMETER			TEST CONDITIONS	74F242, 'F243					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F242	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 4.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	'F242	Waveform 3	3.5 3.5	6.0 6.5	7.5 9.0	3.5 3.5	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	'F242	Waveform 3	4.0 3.5	7.0 6.0	9.0 9.5	4.0 3.5	9.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F243	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	'F243	Waveform 4	2.0 2.0	4.5 5.0	5.7 7.5	2.0 2.0	6.7 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	'F243	Waveform 4	2.0 2.0	4.0 4.5	6.0 6.0	2.0 2.0	7.0 7.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

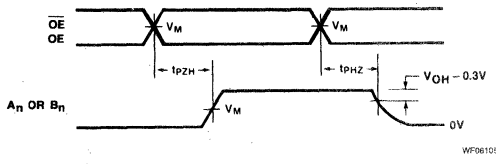
AC WAVEFORMS



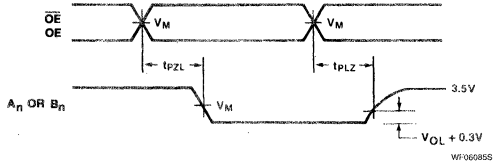
Waveform 1. Waveform For Inverting Outputs



Waveform 2. Waveform For Non-Inverting Outputs



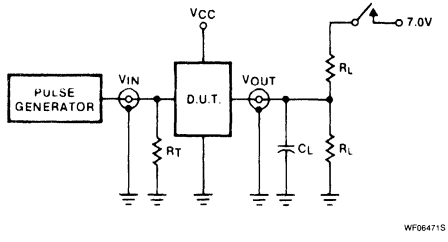
Waveform 3. 3-State Enable Time To HIGH Level And Disable Time From HIGH Level



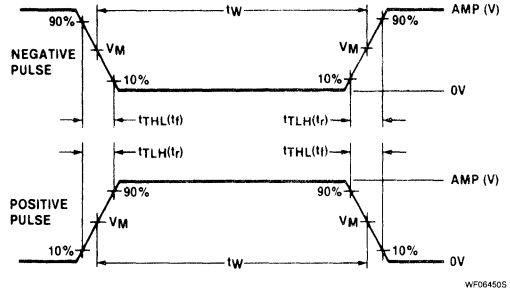
Waveform 4. 3-State Enable Time To LOW Level And Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F244
Buffer

Octal Buffer (3-State)
Product Specification

Logic Products

FEATURES
- **Octal bus interface**
- **3-state buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION
The 'F244 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}$, each controlling four of the 3-state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F244	4.0ns	53mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F244N
Plastic SOL-20	N74F244D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

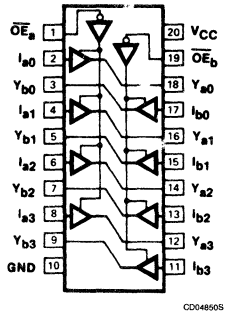
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_a$	3-State output enable input (active LOW)	1.0/1.67	20μA/1.0mA
$\overline{OE}_b$	3-State output enable input (active LOW)	1.0/1.67	20μA/1.0mA
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs	1.0/2.67	20μA/1.6mA
$Y_{a0} - Y_{a3}$, $Y_{b0} - Y_{b3}$	Data outputs	750/106.7	15mA/64mA

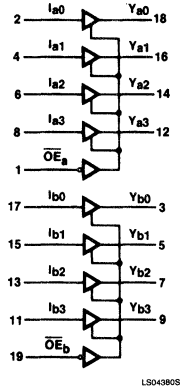
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



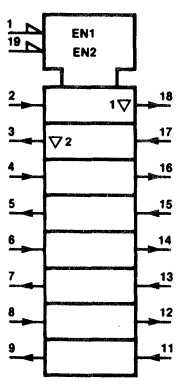
CD04850S

LOGIC SYMBOL



LS04380S

LOGIC SYMBOL (IEEE/IEC)



LS04390S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74F244			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	+10%V_{CC}	2.4			V
				+5%V_{CC}	2.7	3.4		V
			I_{OH} = −15mA	+10%V_{CC}	2.0			V
				+5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	+10%V_{CC}		.35	.50	V
			I_{OL} = 64mA	+5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	$\overline{OE}_a$, $\overline{OE}_b$			−0.7	−1.0	mA
			$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$			−0.6	−1.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 2.4V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{OUT} = 0.5V				−2	−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V			−100	−150	−225	mA
I_{CC}	Supply Current[4] (total)	V_{CC} = MAX	I_{CCH}			40	60	mA
			I_{CCL}			60	90	mA
			I_{CCZ}			60	90	mA

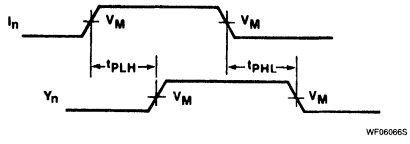
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

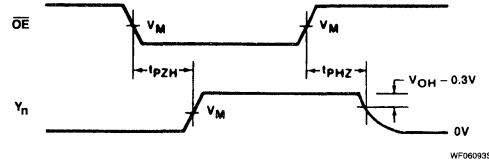
PARAMETER		TEST CONDITIONS	74F244					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.5	4.0	5.2	2.5	6.2	ns
t_{PHL}	Propagation delay	Waveform 1	2.5	4.0	5.2	2.5	6.5	ns
t_{PZH}	Enable to HIGH	Waveform 2	2.0	4.3	5.7	2.0	6.7	ns
t_{PZL}	Enable to LOW	Waveform 3	2.0	5.0	7.0	2.0	8.0	ns
t_{PHZ}	Disable from HIGH	Waveform 2	2.0	3.5	6.0	2.0	7.0	ns
t_{PLZ}	Disable from LOW	Waveform 3	2.0	4.0	6.0	2.0	7.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

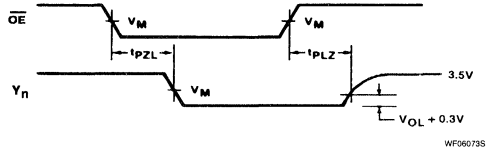
AC WAVEFORMS



Waveform 1. For Non-Inverting Outputs



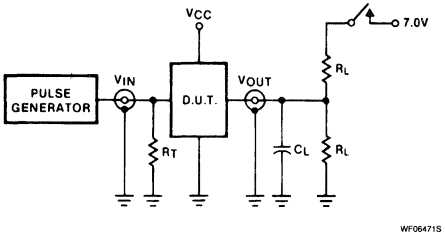
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



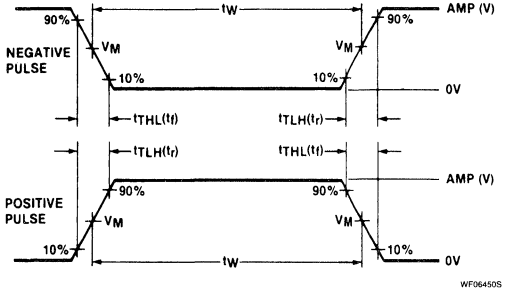
Waveform 3. 3-State Output Enable Time to LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F245 Transceiver

Octal Transceiver (3-state)
Product Specification

Logic Products

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**
- **Outputs are placed in Hi-Z state during power-off conditions**

DESCRIPTION

The 'F245 is an octal transceiver featuring noninverting 3-state bus compatible outputs in both send and receive directions. The B side outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Send/Receive (T/$\overline{R}$) input for direction control. The 3-state outputs, $B_0 - B_7$, have been designed to prevent output bus loading if the power is removed from the device.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F245	3.8ns	100mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F245N
Plastic SOL-20	N74F245D

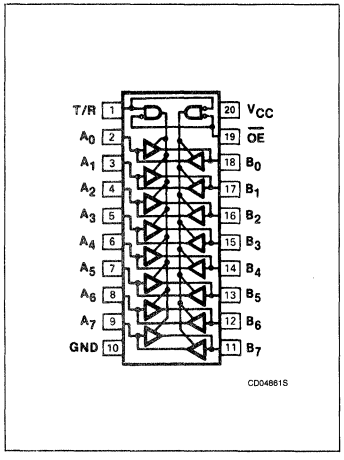
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

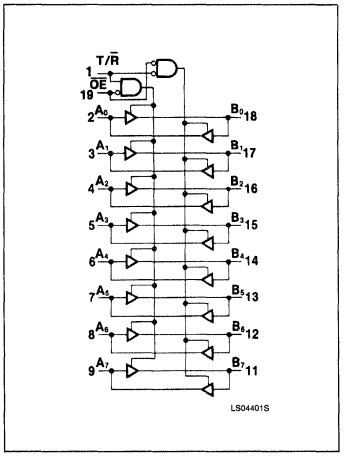
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A Port data inputs	3.5/1.0	70μA/0.6mA
$B_0 - B_7$	B Port data inputs	3.5/1.0	70μA/0.6mA
$\overline{OE}$	Output enable input (active LOW)	2.0/2.0	40μA/1.2mA
T/$\overline{R}$	Transmit/Receive input	2.0/2.0	40μA/1.2mA
$A_0 - A_7$	A Port data outputs	150/40	3.0mA/24mA
$B_0 - B_7$	B Port data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

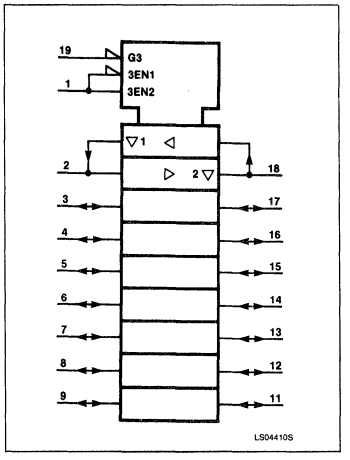
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	HIGH-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

6

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F245			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
		$B_0 - B_7$			±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.35	.50	V
		$B_0 - B_7$		I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 7.0V					100	µA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current $\overline{OE}$ and T/$\overline{R}$ only		V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	LOW-level input current $\overline{OE}$ and T/$\overline{R}$ only		V_{CC} = MAX, V_I = 0.5V				−0.75	−1.2	mA
I_{OZH} + I_{IH}	Off-state current HIGH-level voltage applied		V_{CC} = MAX, $\overline{OE}$ = 2.0V, V_I = 2.7V				0	70	µA
I_{OZL} + I_{IL}	Off-state current LOW-level voltage applied		V_{CC} = MAX, $\overline{OE}$ = 2.0V, V_I = 0.5V					−600	µA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$				−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V			85	114	mA
		I_{CCL}		V_{IN} = GND			100	125	mA
		I_{CCZ}		V_{IN} = $\overline{OE}$ = 4.5V			110	140	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

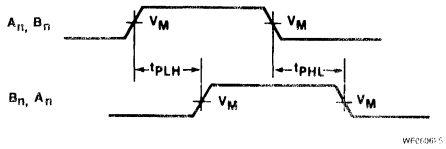
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			74F T_A = 0 to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 1	2.5 2.5	3.5 4.0	5.5 6.0	2.5 2.5	6.5 7.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	Waveform 2 Waveform 3	5.0 3.5	7.0 6.5	8.5 8.0	5.0 3.5	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	Waveform 2 Waveform 3	3.0 2.0	4.5 4.0	6.5 6.0	3.0 2.0	7.5 7.0	ns

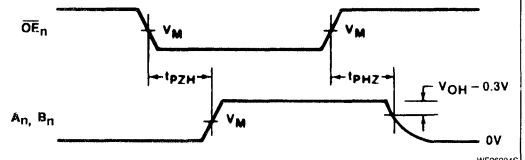
NOTE:

Subtract 0.2ns from minimum values for SO package.

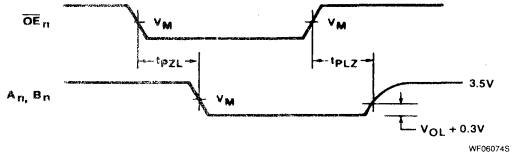
AC WAVEFORMS



Waveform 1. Propagation Delay Data To Output



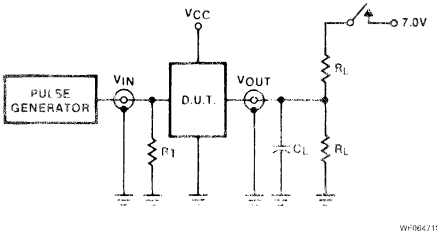
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



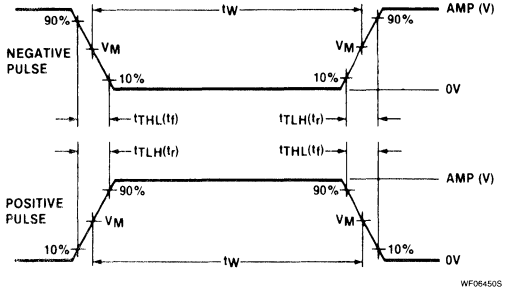
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_r	t_f
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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Signetics

FAST 74F251
Multiplexer

8-Input Multiplexer (3-State)
Preliminary Specification

Logic Products

FEATURES

- **High speed 8-to-1 multiplexing**
- **True and complement outputs**
- **Both outputs are 3-State for further multiplexer expansion**

DESCRIPTION

The 'F251 is a logical implementation of a single-pole, 8-position switch with the state of three Select inputs (S_0, S_1, S_2) controlling the switch position. Assertion (Y) and Negation ($\overline{Y}$) outputs are both provided. The Output Enable input ($\overline{OE}$) is active LOW.

Both outputs are in the HIGH impedance (HIGH Z) state when the output enable is HIGH, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in the HIGH impedance state to avoid high currents that would exceed the maximum ratings, when the outputs of the 3-State devices are tied together. Design of the output enable signals must ensure there is no overlap in the active LOW portion of the enable voltages.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F251	18ns	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74F251N
Plastic SO-16	N74F251D

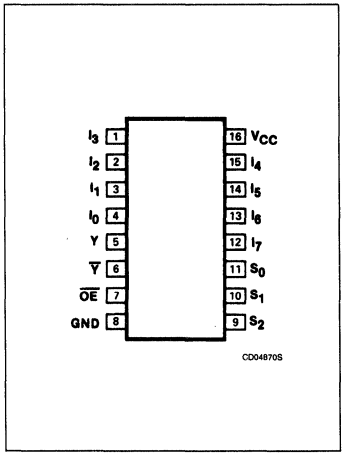
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

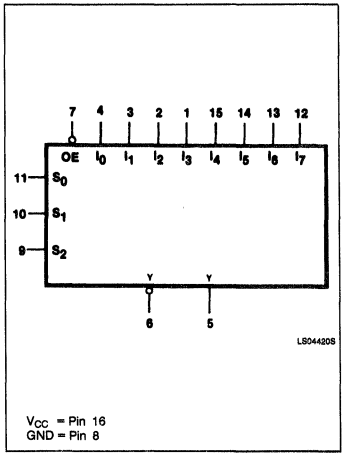
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_0 - I_7$	Data inputs	1.0/1.0	20μA/0.6mA
$S_0 - S_2$	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	3-State output enable input (active LOW)	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	3-State output 3-State output inverted	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

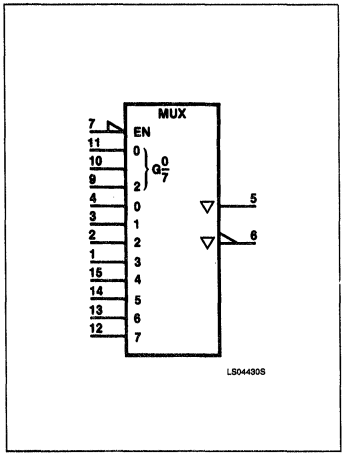
PIN CONFIGURATION



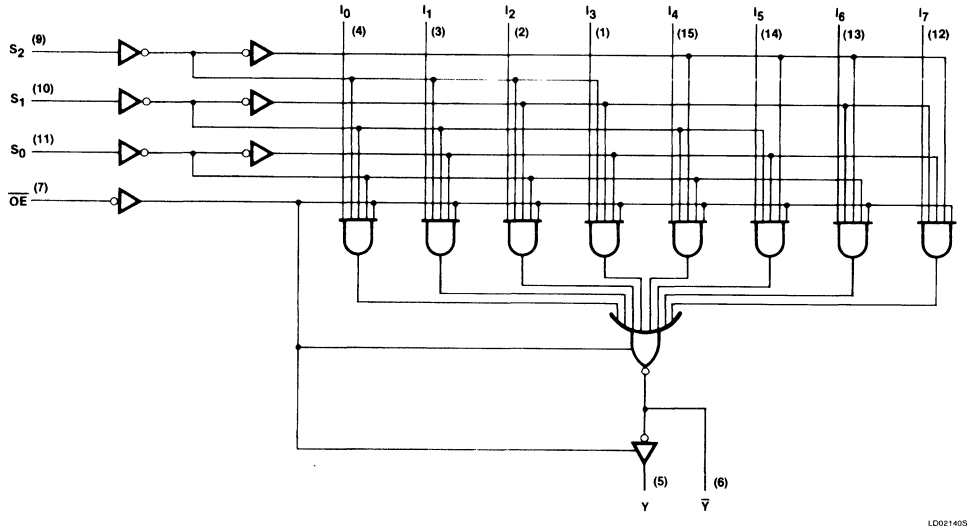
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3.0	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F251			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}		15	22	mA
			I_{CCL}		15	22	mA
			I_{CCZ}		16	24	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is meaured with V_{CC} = MAX, Select and Data inputs at 4.5V, and $\overline{OE}$ ground for output HIGH and LOW conditions; V_{CC} = MAX, Data inputs and the $\overline{OE}$ at 4.5V for outputs OFF condition.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F251					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay S_n to Y	Waveform 2	4.5 5.0	9.6 6.9	13 9.0	4.5 4.0	14 10	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	Waveform 1	4.0 3.2	5.9 5.7	8.0 7.5	4.0 3.2	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y	Waveform 2	5.5 3.7	7.2 5.1	9.5 6.5	5.5 3.7	10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	Waveform 1	3.0 2.0	4.1 3.0	5.7 4.0	3.0 2.0	7.0 5.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{OE}$ to Y	Waveform 3	4.0 3.5	6.9 6.0	9.0 8.0	4.0 3.5	10 9.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{OE}$ to $\overline{Y}$	Waveform 4	3.0 3.5	5.4 6.4	7.0 8.5	3.0 3.5	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level $\overline{OE}$ to $\overline{Y}$	Waveform 3	3.0 2.0	5.0 3.2	6.5 4.5	3.0 2.0	7.5 5.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level $\overline{OE}$ to Y	Waveform 4	3.0 2.0	4.7 3.5	6.0 4.5	3.0 2.0	7.0 5.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

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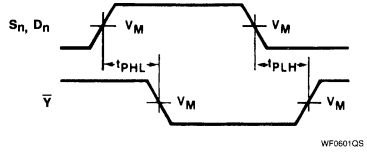
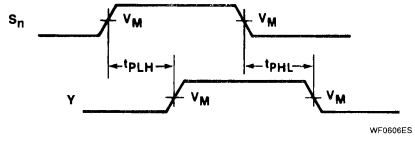
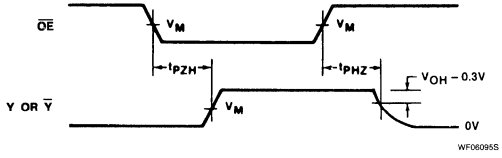
AC WAVEFORMS



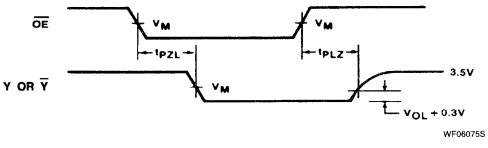
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



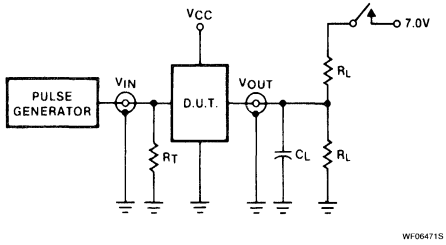
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level

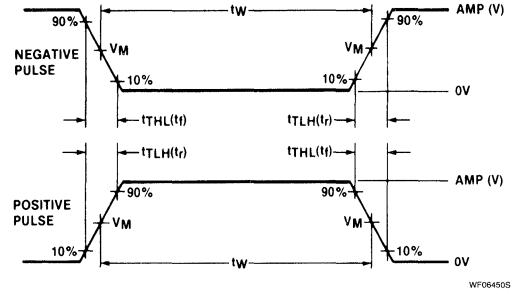


Waveform 4. 3-State Enable Time To LOW Level And Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS





Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F253
Multiplexer

Dual 4-Input Multiplexer (3-State)
Product Specification

Logic Products

FEATURES
- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

DESCRIPTION
The 'F253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

The 'F253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs.

All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F253	7.0ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F253N
Plastic SO-16	N74F253D

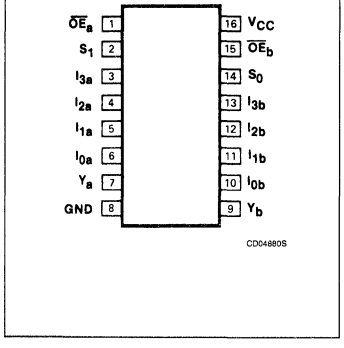
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

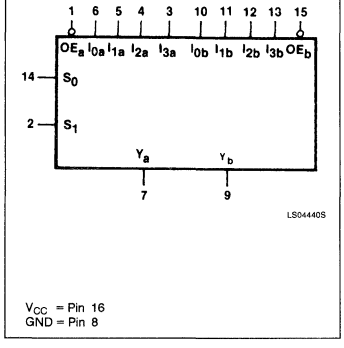
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{3a}$	Port A data inputs	1.0/1.0	20μA/0.6mA
$I_{0b} - I_{3b}$	Port B data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}_a$	Port A output enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}_b$	Port B output enable input (active LOW)	1.0/1.0	20μA/0.6mA
Y_a, Y_b	3-State outputs	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

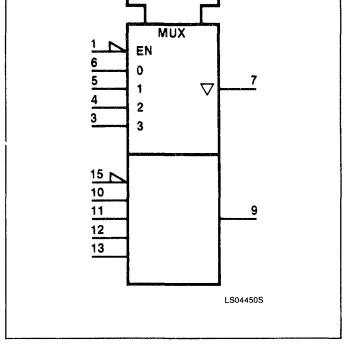
PIN CONFIGURATION



LOGIC SYMBOL

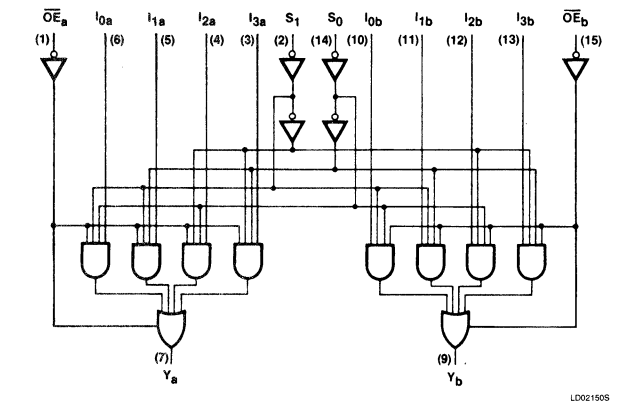


LOGIC SYMBOL (IEEE/IEC)



Multiplexer | FAST 74F253

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS						OUTPUT	
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedence (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F253			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			-0.4	-0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			-2	-50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60	-80	-150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	$\overline{OE}_n$ = GND; S_n = I_n = 4.5V		10	16	mA
	I_{CCL}		$\overline{OE}_n$ = S_n = I_n = GND		12	23	mA
	I_{CCZ}		$\overline{OE}_n$ = 4.5; I_n = S_n = GND		14	23	mA

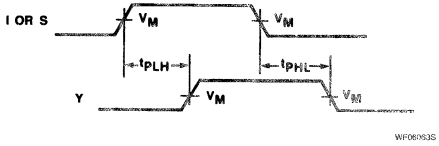
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

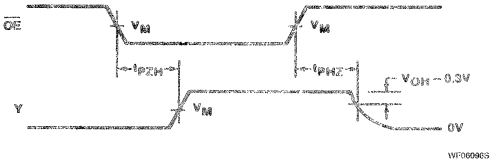
PARAMETER		TEST CONDITIONS	74F253					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	3.0	4.5	7.0	3.0	7.5	ns
t_{PHL}	Data to output		3.0	5.0	7.0	3.0	8.0	
t_{PLH}	Propagation delay	Waveform 1	4.5	7.5	10.5	4.5	11.0	ns
t_{PHL}	Select to output		5.0	8.5	11.0	4.5	12.0	
t_{PZH}	Output enable time to HIGH level	Waveform 2	3.0	6.5	8.0	3.0	9.0	ns
t_{PZL}	Output enable time to LOW level	Waveform 3	3.0	6.5	8.0	3.0	9.0	ns
t_{PHZ}	Output disable time from HIGH level	Waveform 2, Waveform 3	2.5	3.5	5.0	2.0	6.0	ns
t_{PLZ}	Output disable time from LOW level	Waveform 3, Waveform 4	2.0	3.0	5.0	1.5	6.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

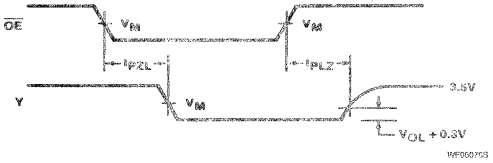
AC WAVEFORMS



Waveform 1. Propagation Delay Data And Select To Output



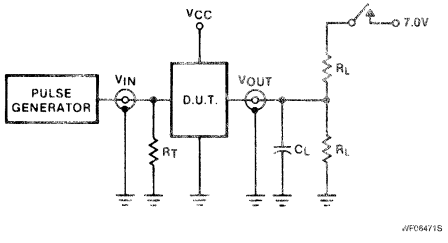
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



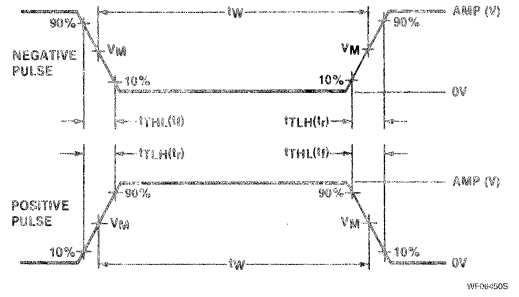
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F256
Latch

Product Specification

Logic Products

FEATURES

- **Combines dual demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common Clear input**
- **Useful as dual 1-of-4 active HIGH decoder**

DESCRIPTION

The 'F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F256	7.0ns	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F256N
Plastic SO-16	N74F256D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_a, D_b	Port A, side B data inputs	1.0/1.0	20μA/0.6mA
A_0, A_1	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$, $\overline{MR}$	Enable, master reset inputs	1.0/1.0	20μA/0.6mA
$Q_{0a} - Q_{3a}$	Port A outputs	50/33	1mA/20mA
$Q_{0b} - Q_{3b}$	Port B outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

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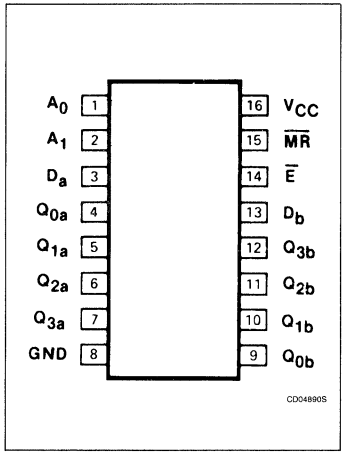
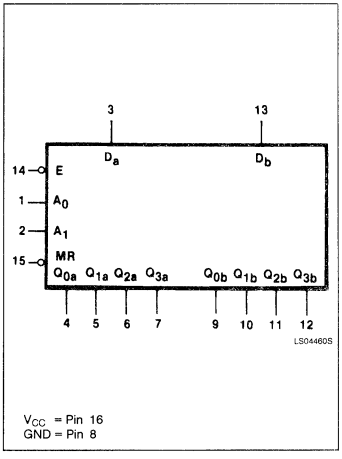
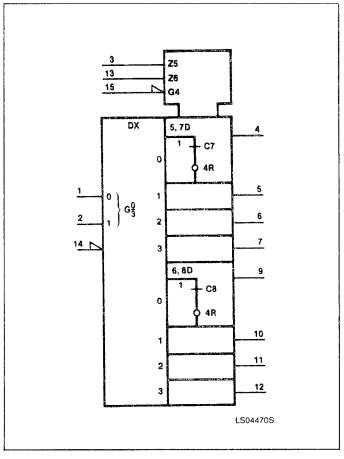
PIN CONFIGURATION



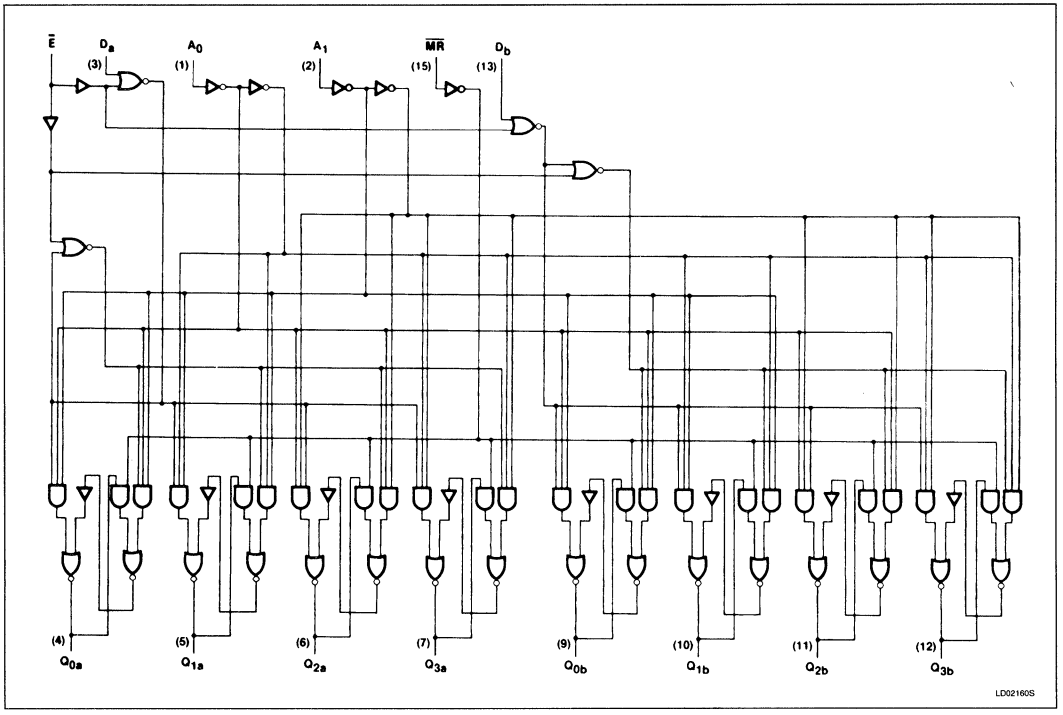
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3
Master reset	L	H	X	X	X	L	L	L	L
Demultiplex	L	L	D	L	L	Q = D	L	L	L
(active HIGH	L	L	d	H	L	L	Q = d	L	L
decoder	L	L	d	L	H	L	L	Q = d	L
when D = H)	L	L	D	H	H	L	L	L	Q = D
Store (do nothing)	H	H	X	X	X	q_0	q_1	q_2	q_3
	H	L	d	L	L	Q = d	q_1	q_2	q_3
Addressable	H	L	d	H	L	q_0	Q = d	q_2	q_3
latch	H	L	d	L	H	q_0	q_1	Q = d	q_3
	H	L	D	H	H	Q_0	Q_1	Q_2	Q = D

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
X = Don't care
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}$ = $\overline{E}$ = LOW), addressed outputs will follow the level of the D inputs, with all other outputs LOW. In the Master Reset mode, all outputs are LOW and unaffected by the Address and Data inputs.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F256			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		21	42	mA
		I_{CCL}			33	60	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequences of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F256					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	5.0 3.0	7.0 5.0	9.5 7.0	5.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	6.0 3.0	8.0 5.0	10.5 7.0	6.0 3.0	12.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 3	5.0 4.5	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns

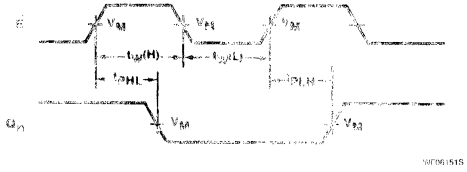
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F256					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to $\overline{E}$	Waveform 5	3.0 6.5			3.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{E}$	Waveform 5	0 0			0 0		ns
t_s	Set-up time, HIGH or LOW A_n to $\overline{E}$[1]	Waveform 6	2.0			2.0		ns
t_g	Hold time, HIGH or LOW A_n to $\overline{E}$[2]	Waveform 6	0			0		ns
t_w	$\overline{E}$ pulse width	Waveform 1	7.5			8.0		ns
t_w	$\overline{MR}$ pulse width	Waveform 4	3.0			3.0		ns

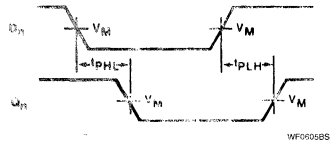
NOTES:
1. The Address to Enable set-up time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC WAVEFORMS



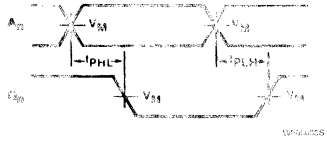
WF06151S

Waveform 1. Propagation Delay Enable To Output And Enable Pulse Width

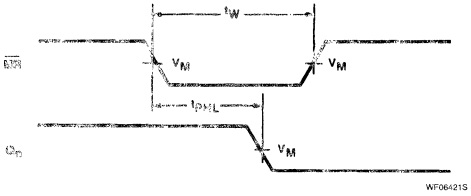


WF06058S

Waveform 2. Propagation Delay Data To Output

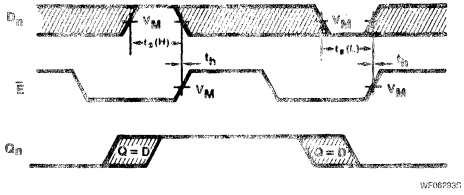


Waveform 3. Propagation Delay Address To Output



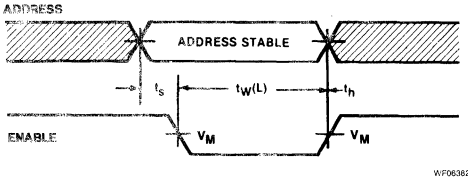
WF06421S

Waveform 4. Master Reset To Output Delay And Master Reset Pulse Width



WF06293S

Waveform 5. Data Set-up And Hold Times

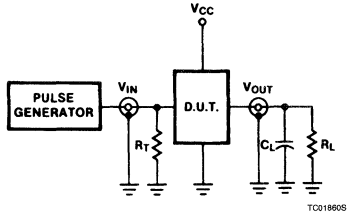


WF06382S

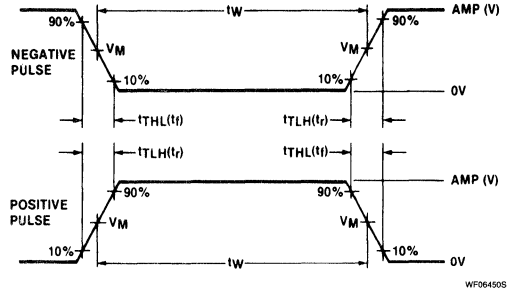
Waveform 6. Address Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F257A
Data Selector/Multiplexer

Quad 2-Line To 1-Line Data Selector Multiplexer (3-State)
Product Specification

Logic Products

FEATURES
- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**
- **See 'F258A for inverting version**

DESCRIPTION
The 'F257A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The 'F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input ($\overline{OE}$) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F257A	4.3ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F257N
Plastic SO-16	N74F257D

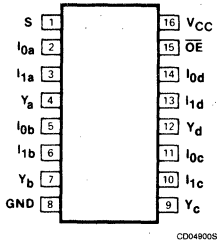
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

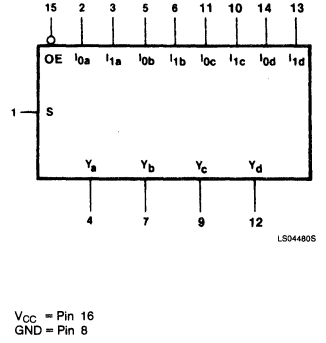
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20μA/0.6mA
S	Common select input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Enable input (Active LOW)	1.0/1.0	20μA 0.6mA
$Y_a - Y_d$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

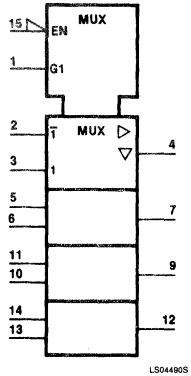
PIN CONFIGURATION



LOGIC SYMBOL

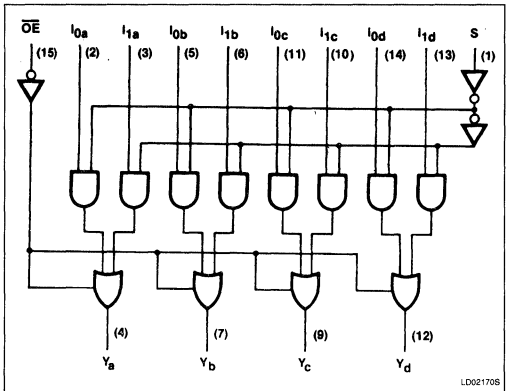


LOGIC SYMBOL (IEEE/IEC)



Data Selector/Multiplexer | FAST 74F257A

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3.0	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F257A			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN.	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX		9.0	15.0	mA
		I_{CCL}			14.5	22.0	mA
		I_{CCZ}			15.0	23.0	mA

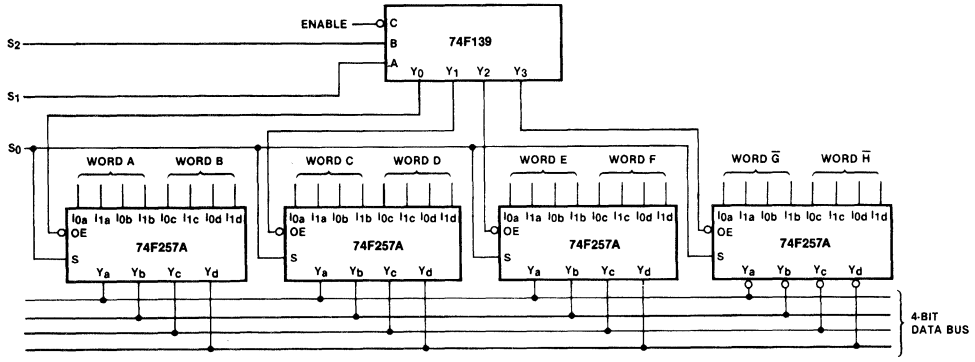
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all outputs open and inputs grounded.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

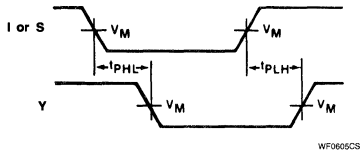
PARAMETER		TEST CONDITIONS	74F257A					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	3.0	4.5	6.0	3.0	7.0	ns
t_{PHL}	I_{na}, I_{nb} to Y_n		2.0	3.5	5.0	2.0	6.0	
t_{PLH}	Propagation delay	Waveform 1	5.5	7.5	9.5	5.0	10.5	ns
t_{PHL}	S to Y_n		4.0	5.5	7.0	4.0	8.0	
t_{PZH}	Output Enable time to	Waveform 2	4.5	6.5	7.5	4.5	8.5	ns
t_{PZL}	HIGH or LOW level	Waveform 3	4.5	6.0	7.5	4.5	8.5	
t_{PHZ}	Output Disable time	Waveform 2	2.0	4.0	5.5	2.0	6.0	ns
t_{PLZ}	from HIGH or LOW	Waveform 3	2.0	3.5	5.5	2.0	6.0	

NOTE:
Subtract 0.2ns from minimum values for SO package.

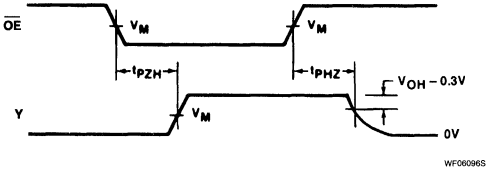
APPLICATIONS



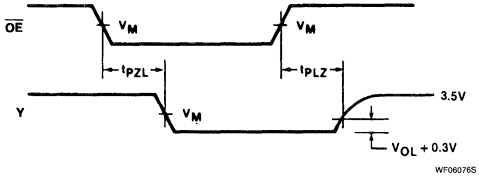
AC WAVEFORMS



Waveform 1. Propagation Delay Data And Select To Output



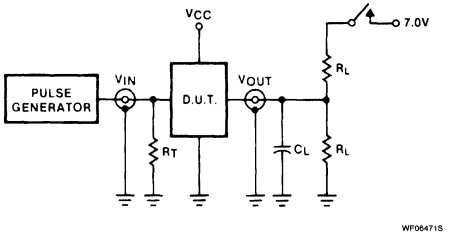
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



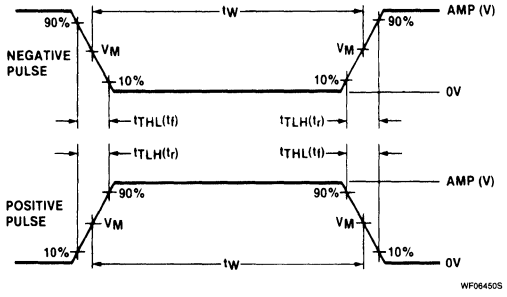
Waveform 3. 3-State Enable Time To LOW Level And Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PZH}	open
t_{PZL}	closed
t_{PHZ}	open
t_{PLZ}	closed

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

6

Signetics

FAST 74F258A
Data Selector/Multiplexer

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)
Product Specification

Logic Products

FEATURES
- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**
- **See 'F257A for non-inverting version**

DESCRIPTION
The 'F258A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Select input (S). The I_{0n} inputs are selected when the Select input is LOW and the I_{1n} inputs are selected when the Select input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The 'F258A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a HIGH impedance "off" state when the Output Enable input ($\overline{OE}$) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs are tied together.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F258A	3.5ns	14mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74F258AN
Plastic SO-16	N74F258AD

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

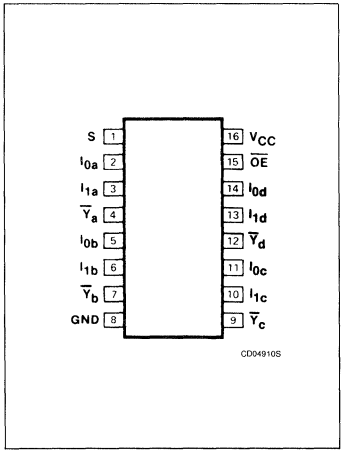
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}•I_{1n}	Data inputs	1.0/1.0	20μA/0.6 mA
S	Common select input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{Y}$a-$\overline{Y}$d	Data outputs	50/40	1.0mA/24mA

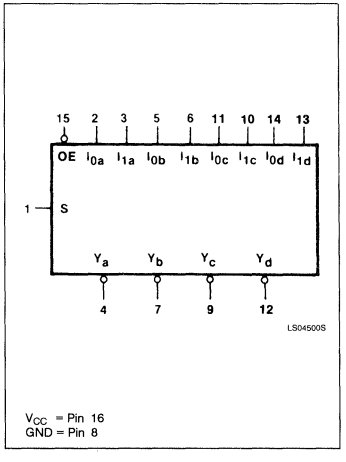
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

Design of the output signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

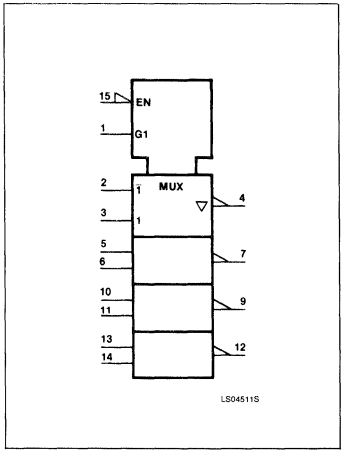
PIN CONFIGURATION



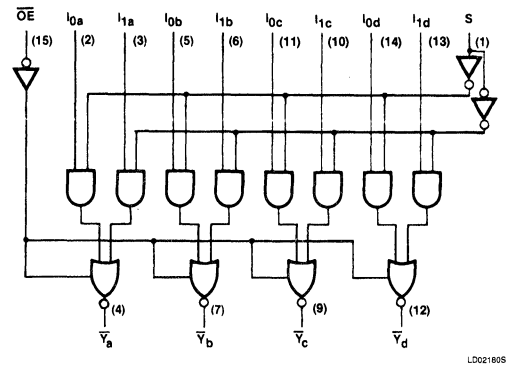
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS[1]		74F258A			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.5	V
			±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		8.5	11.5	mA
		I_{CCL}			17.0	23.0	mA
		I_{CCZ}			16.0	22.0	mA

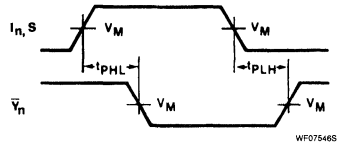
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

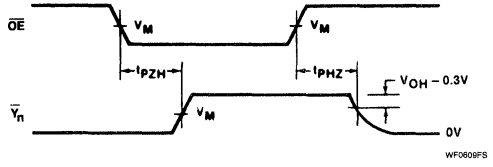
PARAMETER		TEST CONDITIONS	74F258A					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	3.0	4.5	6.0	2.5	7.0	ns
t_{PHL}	I_n to $\overline{Y}_n$		1.0	2.5	4.0	1.0	4.5	
t_{PLH}	Propagation delay	Waveform 1	3.5	6.5	8.0	3.5	9.0	ns
t_{PHL}	S to $\overline{Y}_n$		2.5	6.0	8.0	2.5	9.0	
t_{PZH}	Output enable time	Waveform 2	4.0	6.0	7.5	3.5	8.5	ns
t_{PZL}	to HIGH or LOW level	Waveform 3	4.0	5.5	7.5	3.5	8.5	
t_{PHZ}	Output disable time	Waveform 2	2.0	3.5	5.5	2.0	6.5	ns
t_{PLZ}	from HIGH or LOW level	Waveform 3	2.0	3.5	5.5	2.0	6.0	

NOTE:
Subtract 0.2ns from minimum values for SO package.

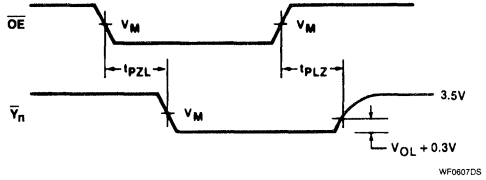
AC WAVEFORMS



Waveform 1. Propagation Delay Data (I_n), Select (S) To Output ($\overline{Y}_n$)



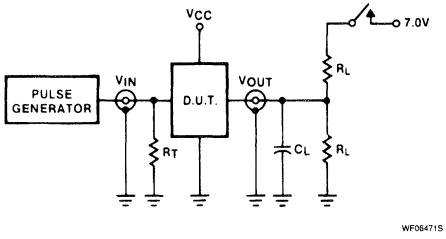
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



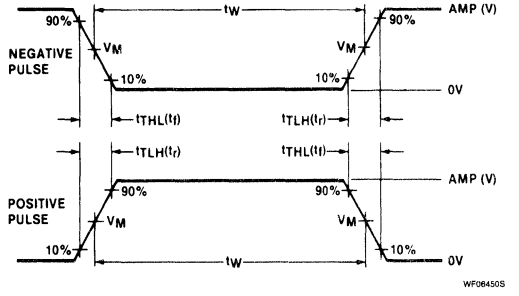
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F259
Latch

8-Bit Addressable Latch
Product Specification

Logic Products

FEATURES

- **Combines demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common Clear input**
- **Useful as a 1-of-8 active HIGH decoder**

DESCRIPTION

The 'F259 addressable latch has four distinct modes of operation that are selectable by controlling the Master Reset and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the store mode, all latches remain in their previous states and are unaffected by the Data or Address inputs.

To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{MR}$ = $\overline{E}$ = LOW), addressed outputs will follow the level of the D inputs, with all other outputs LOW. In the Master Reset mode, all outputs are LOW and unaffected by the Address and Data inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F259	7.5ns	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F259N
Plastic SO-16	N74F259D

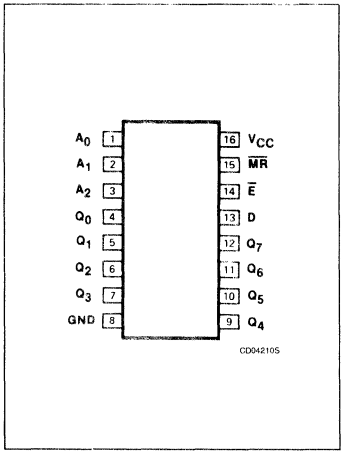
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

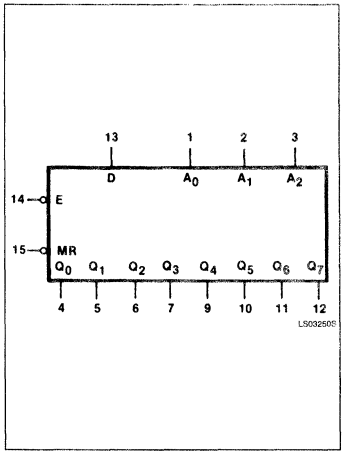
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{MR}$, $\overline{E}$	Master reset, enable inputs	1.0/1.0	20µA/0.6mA
A_0, A_2	Address inputs	1.0/1.0	20µA/0.6mA
D	Data input	1.0/1.0	20µA/0.6mA
$Q_0 - Q_7$	Outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the HIGH state and 0.6mA in the LOW state.

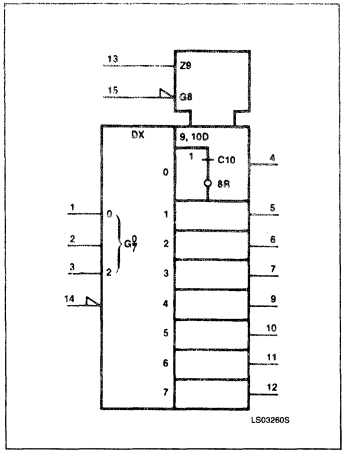
PIN CONFIGURATION



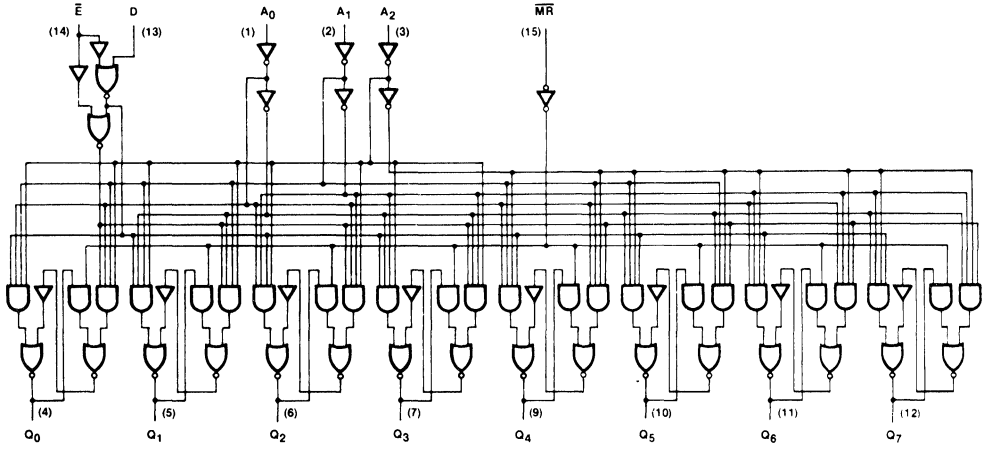
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
X = Don't care.
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F259			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−90	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			24	46	mA
		I_{CCL}				37	75	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F259					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D to Q_n	Waveform 2	5.0 3.0	7.0 5.0	9.0 7.0	5.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	6.0 3.0	8.0 5.0	10.5 7.0	6.0 3.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 3	5.0 4.0	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns

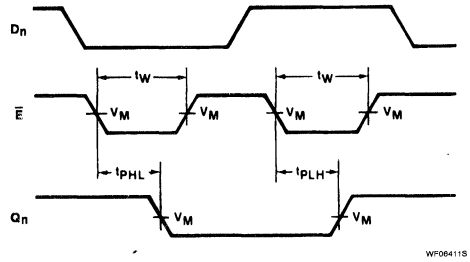
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

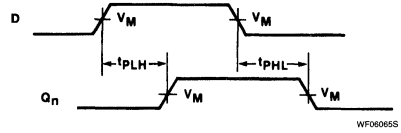
PARAMETER		TEST CONDITIONS	74F259					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D to $\overline{E}$	Waveform 5	3.0 6.5			3.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D to $\overline{E}$	Waveform 5	0 0			0 0		ns
t_s	Set-up time, HIGH or LOW A_n to $\overline{E}$[1]	Waveform 6	2.0			2.0		ns
t_g	Hold time, HIGH or LOW A_n to $\overline{E}$[2]	Waveform 6	0			0		ns
t_w	$\overline{E}$ pulse width	Waveform 1	7.5			8.0		ns
t_w	$\overline{MR}$ pulse width	Waveform 4	3.0			3.0		ns

NOTES:
1. The Address to Enable set-up time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

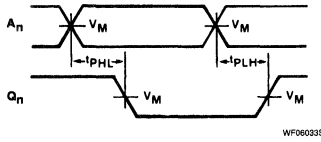
AC WAVEFORMS



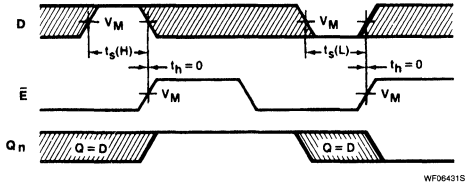
Waveform 1. Propagation Delay Enable To Output And Enable Pulse Width



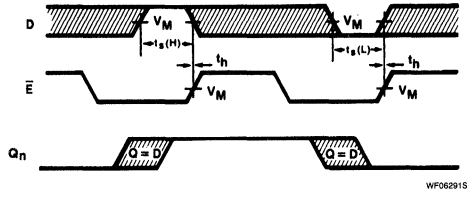
Waveform 2. Propagation Delay Data To Output



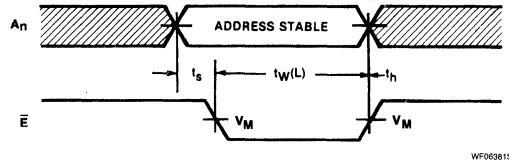
Waveform 3. Propagation Delay Address To Output



Waveform 4. Master Reset To Output Delay And Master Reset Pulse Width



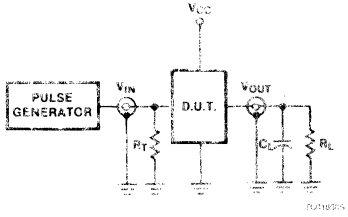
Waveform 5. Data Set-up And Hold Times



Waveform 6. Address Set-up And Hold Times

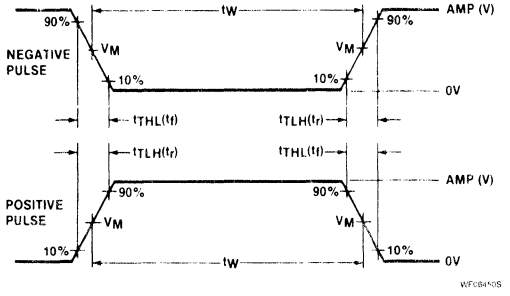
NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

FAST 74F260
Gate

Dual 5-Input NOR Gate
Product Specification

Logic Products

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	$\overline{Y}$
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F260	3.5ns	6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F260N
Plastic SO-14	N74F260D

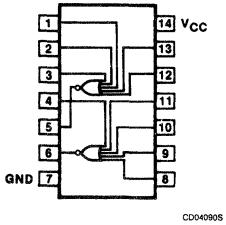
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A – E	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data outputs	50/33	1mA/20mA

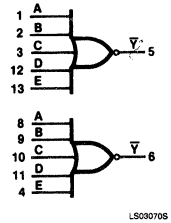
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



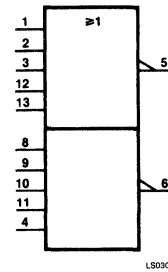
CD04090S

LOGIC SYMBOL



LS03070S

LOGIC SYMBOL (IEEE/IEC)



LS03080S

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F260			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			5	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.6	6.5	mA
		I_{CCL}		V_{IN} = 4.5V		7.3	9.5	mA

NOTES:

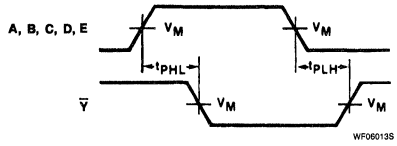
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F260					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E to $\overline{Y}$	Waveform 1	2.5 1.5	4.0 2.5	5.5 4.0	2.0 1.0	6.5 4.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

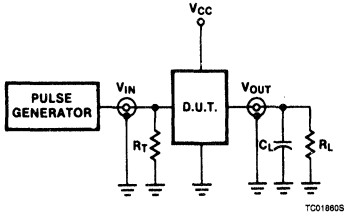
AC WAVEFORM



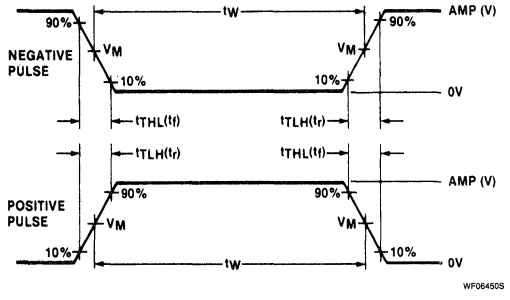
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay Input To Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F269
8-Bit Counter

8-Bit Bidirectional Binary Counter
Product Specification

Logic Products

FEATURES
- **Synchronous counting and loading**
- **Built-in lookahead carry capability**
- **Count frequency 115MHz typ**
- **Supply current 95mA typ**

DESCRIPTION
The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F269N
Plastic SOL-24	N74F269D

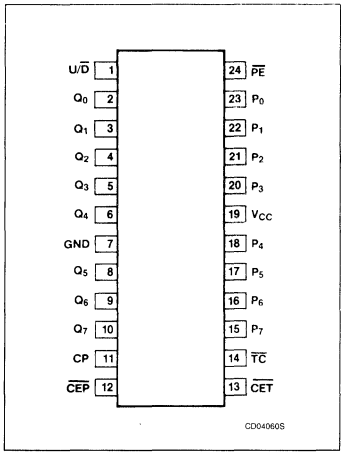
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

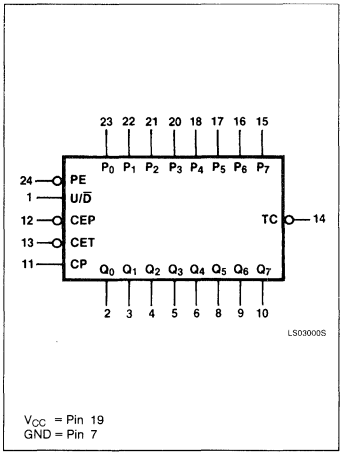
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$P_0 - P_7$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active LOW)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up-Down count control input	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count enable parallel input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Flip-flop outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

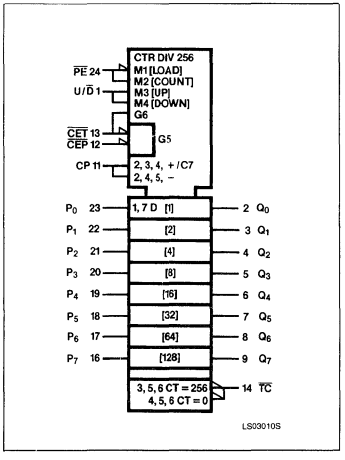
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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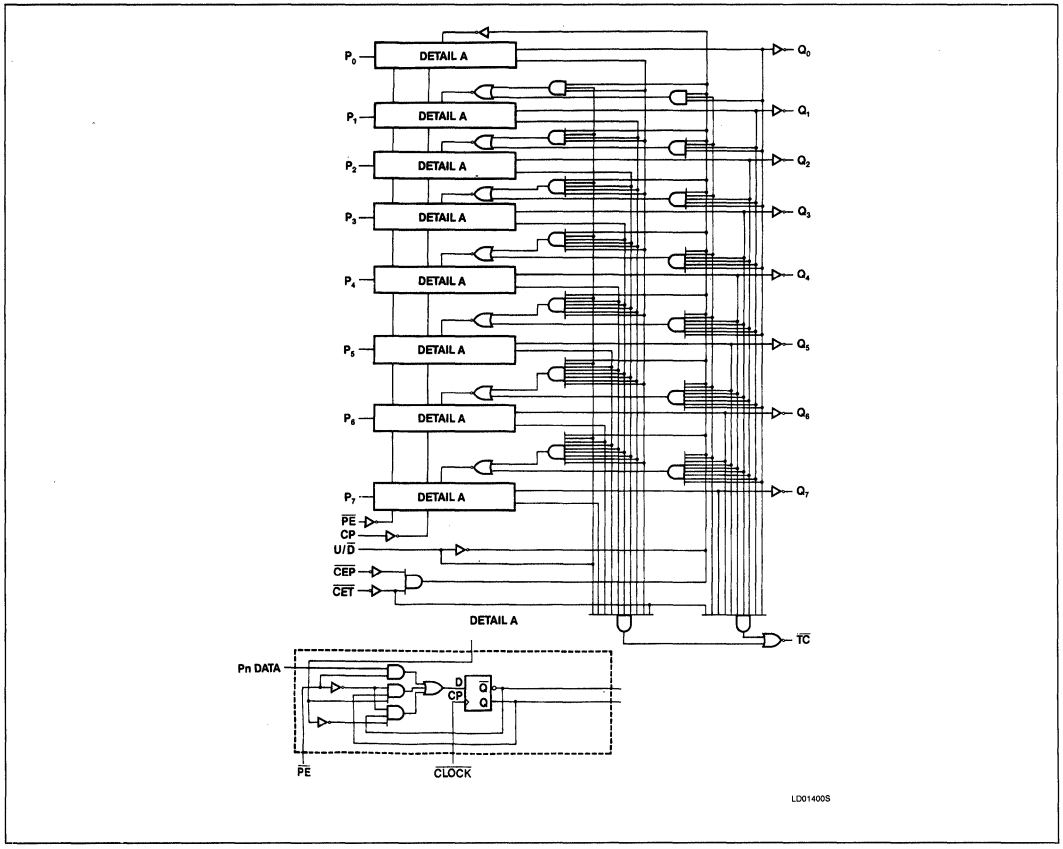
LOGIC DIAGRAM

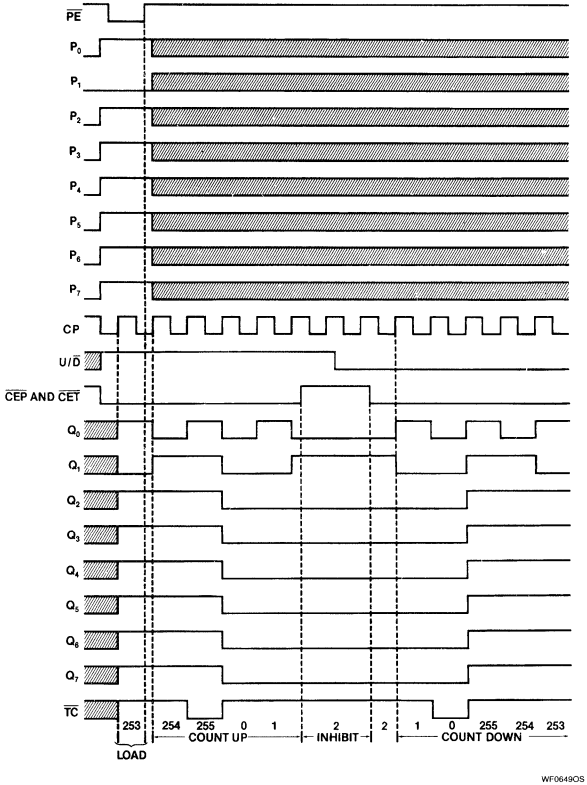


FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	P_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	(a)
	↑	X	X	X	l	h	H	(a)
Count Up	↑	h	l	l	h	X	Count Up	(a)
Count Down	↑	l	l	l	h	X	Count Down	(a)
Hold	↑	X	h	X	h	X	q_n	(a)
do nothing	↑	X	X	h	h	X	q_n	H

H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition
(a) = The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs HIGH and Terminal Count Down is with all Q_n outputs LOW.

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.50	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F269			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX,		−60	−115	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	PE = $\overline{CET}$ = $\overline{CEP}$ = U/$\overline{D}$ = GND, P_n = 4.5V, CP = ↑		93	120	mA
		I_{CCL}		PE = $\overline{CET}$ = $\overline{CEP}$ = U/$\overline{D}$ = GND CP = ↑		98	125	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F269					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Load)	Waveform 1 $\overline{PE}$ = LOW	3.5 4.0	6.0 6.5	9.0 8.5	3.5 4.0	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Count)	Waveform 1 $\overline{PE}$ = HIGH	3.5 4.5	5.5 7.5	8.0 10.5	3.5 4.5	9.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 6.0	6.5 8.0	9.5 10.0	4.5 5.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.5 3.0	6.5 7.0	9.0 10.5	3.5 3.0	10.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 3	5.5 4.5	7.5 7.0	9.5 9.5	5.5 4.5	10.0 11.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F269					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW P_n to CP	Waveform 4	1.5 2.0			1.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW P_n to CP	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{PE}$ to CP	Waveform 4	5.0 5.0			5.5 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CET}$, $\overline{CEP}$ to CP	Waveform 5	4.5 6.5			4.5 7.0		ns
$t_h(H)$ $t_h(L)$	Set-up time, HIGH or LOW $\overline{CET}$, $\overline{CEP}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW U/$\overline{D}$ to CP	Waveform 6	7.0 5.5			7.5 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW U/$\overline{D}$ to CP	Waveform 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width HIGH or LOW	Waveform 1	3.5 3.5			3.5 4.0		ns

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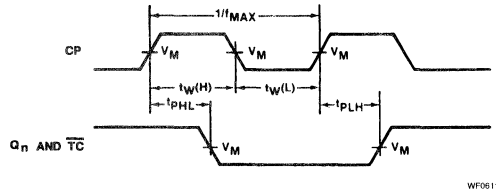
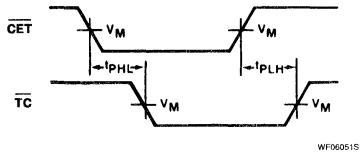
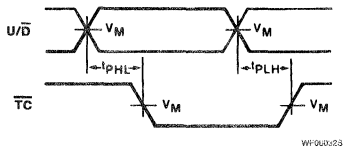
AC WAVEFORMS



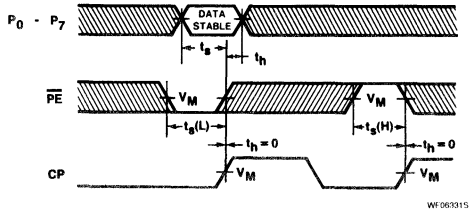
Waveform 1. Clock To Output Delays And Clock Pulse Width



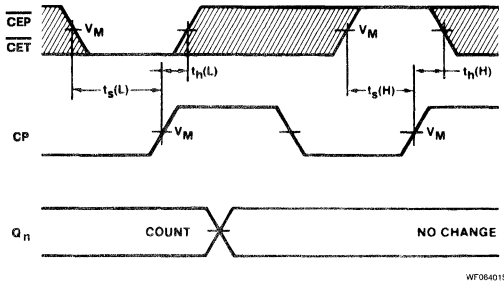
Waveform 2. Propagation Delays CET Input To Terminal Count Output



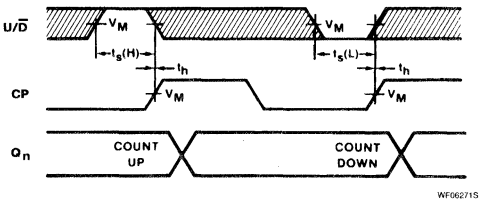
Waveform 3. Propagation Delays U/D Control To Terminal Count Output



Waveform 4. Parallel Data And Parallel Enable Set-up And Hold Times



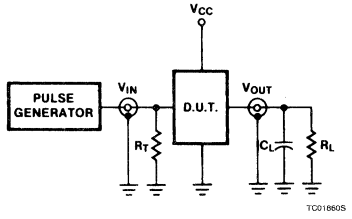
Waveform 5. Count Enable Set-up And Hold Times



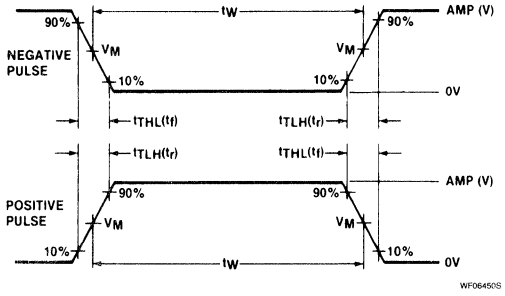
Waveform 6. Up/Down Control Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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Signetics

FAST 74F273
Flip-Flop

Octal D Flip-Flop
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in LOW and HIGH states)**
- **Ideal buffer for MOS microprocessor or memory**
- **Eight edge-triggered D-type flip-flops**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**
- **See 'F377 for Clock Enable version**
- **See 'F373 for transparent latch version**
- **See 'F374 for 3-State version**

DESCRIPTION

The 'F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F273	145MHz	66mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F273N
Plastic SOL-20	N74F273D

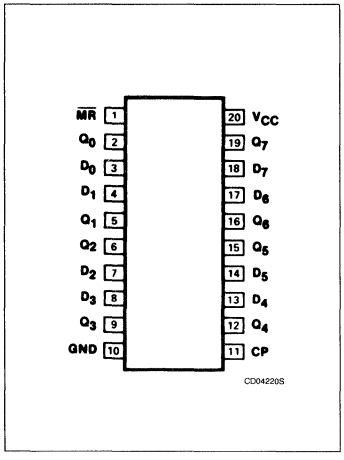
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

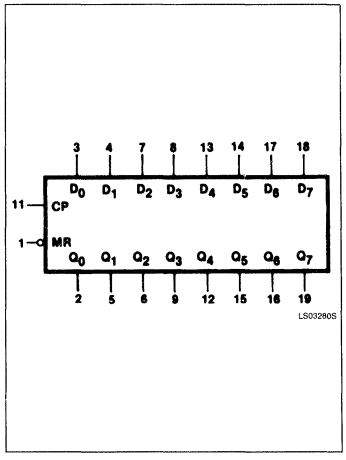
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/0.033	20μA/20μA
$\overline{MR}$	Master reset (active LOW)	1.0/0.033	20μA/20μA
CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
Q_0-Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

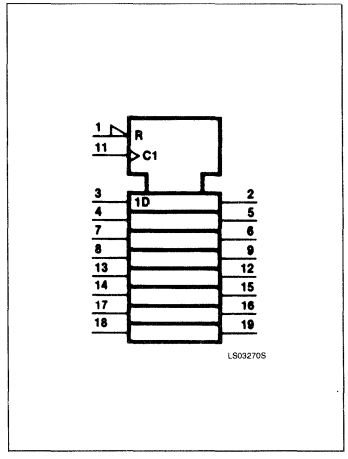
PIN CONFIGURATION



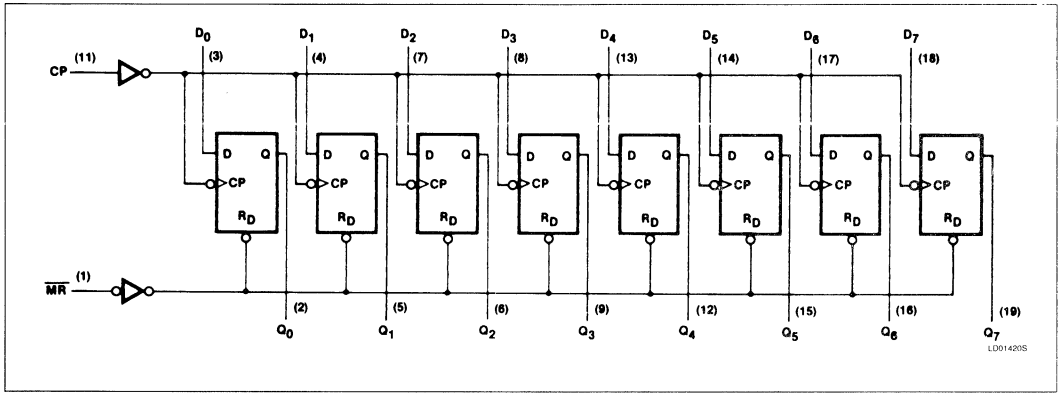
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F273			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$\overline{MR}$ & CP inputs[3]	V_{CC} = MIN, V_{IL} = 0.0V, V_{IH} = 4.5V, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
		Other inputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−20	mA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[5] (total)	I_{CCH}	V_{CC} = MAX			65	85	mA
		I_{CCL}				68	88	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise durung test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-spped test apparatus and/or sample- and-hold techniques are freferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter test. In any sequence of parameter test, I_{OS} tests should be performed last.
5. Measure I_{CC} after a momentary ground, then 4.5V is applied to clock with all outputs open and 4.5V applied to clock with all outputs open and 4.5V applied to he Master Reset input. all data inputs and the Master Reset input.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

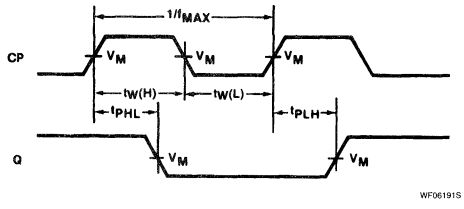
PARAMETER		TEST CONDITIONS	74F273					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	130	145		120		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.0 4.0	7.5 7.5		4.0 4.0	11 12	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5	7.0	9.5	3.5	10.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

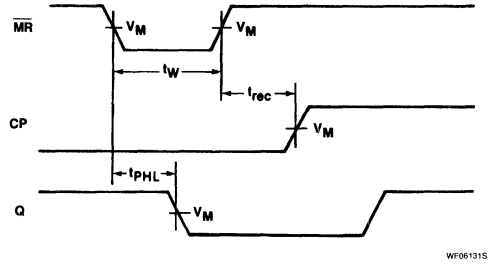
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F273					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	Waveform 3	1.5 1.5			1.5 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 3	0 0			0 0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	8.0			8.5		ns
$t_w(H)$ $t_w(L)$	Clock pulse width HIGH or LOW	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	Master Reset pulse width	Waveform 2	3.5			4.0		ns

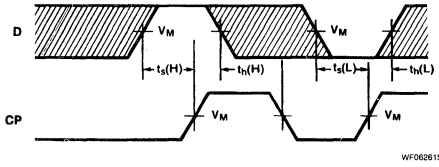
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Master Reset Pulse Width, Master Reset To Output And Master Reset To Clock Recovery Time

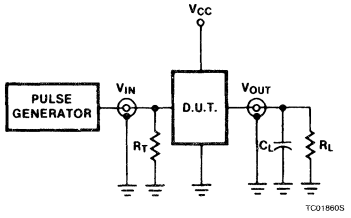


Waveform 3. Data Set-up And Hold Times

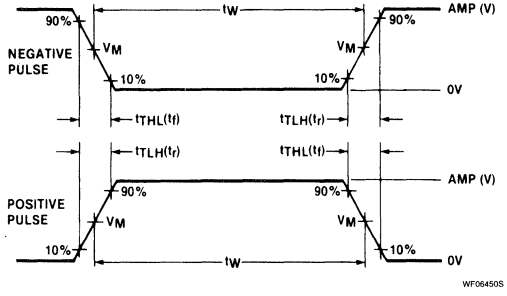
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F280A
Parity Generator Checker

9-Bit Odd/Even Parity Generator/Checker
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in LOW and HIGH states)**
- **Buffered inputs — one normalized load**
- **Word length easily expanded by cascading**

DESCRIPTION

The 'F280A is a 9-bit parity generator or checker commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is HIGH when an even number of Data inputs ($I_0 - I_8$) are HIGH. The Odd parity output (Σ_O) is HIGH when an odd number of Data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E) of up to nine parallel devices to the Data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 25ns with the 'F280A.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F280A	9.0ns	26mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F280AN
Plastic SO-14	N74F280AD

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

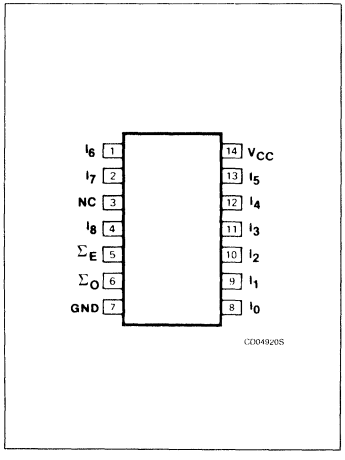
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_0 - I_8$	Data inputs	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	50/33	1.0mA/20mA

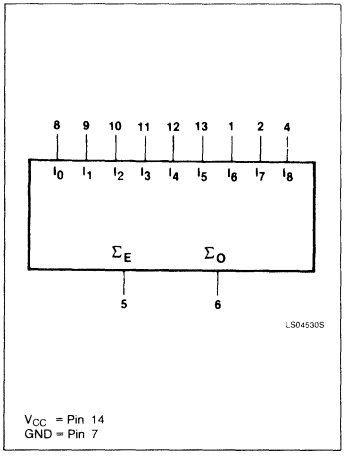
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

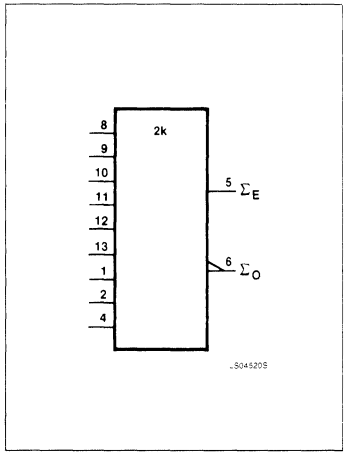
PIN CONFIGURATION



LOGIC SYMBOL

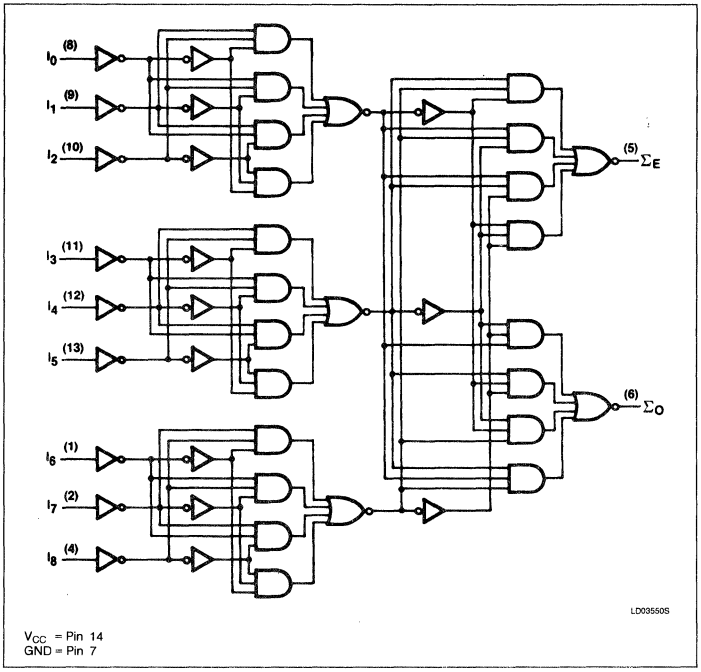


LOGIC SYMBOL (IEEE/IEC)



Parity Generator Checker — FAST 74F280A

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

FUNCTION TABLE

INPUTS	OUTPUTS	
Number of HIGH Data Inputs ($I_0 - I_8$)	Σ_E	Σ_O
Even — 0, 2, 4, 6, 8	H	L
Odd — 1, 3, 5, 7, 9	L	H

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F280A			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			4.0	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.1	−20	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−114	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			26	35	mA

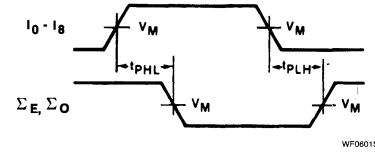
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

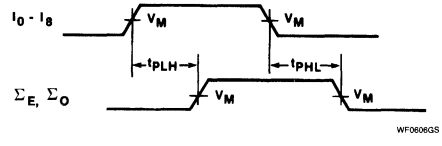
PARAMETER		TEST CONDITIONS	74F280A					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $I_0 - I_8$ to Σ_E	Waveform 1, 2	5.0 9.0	7.0 11.1	9.0 13.0	5.0 7.5	10.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_0 - I_8$ to Σ_C	Waveform 1, 2	6.5 7.0	8.6 9.1	10.5 11.0	6.5 6.0	11.0 13.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



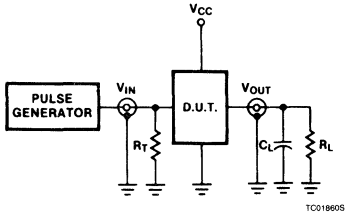
Waveform 1. For Inverting Outputs



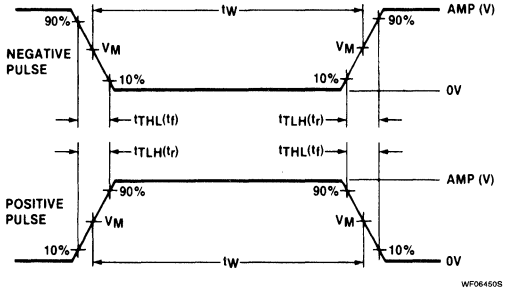
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F283
4-Bit Adder

4-Bit Binary Full Adder With Fast Carry
Product Specification

Logic Products

FEATURES
- **High-speed 4-bit binary addition**
- **Cascadable in 4-bit increments**
- **Fast internal carry lookahead**

DESCRIPTION
The 'F283 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry (C_{OUT}) according to the equation:

$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$

where (+) = plus.

Due to the symmetry of the binary add function, the 'F283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic) — see Function Table. In case of all active LOW operands the results $\Sigma_1 - \Sigma_4$ and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1 can arbitrarily be assigned to pins 5, 6, 7, etc.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F283	7.0ns	36mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F283N
Plastic SO-16	N74F283D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

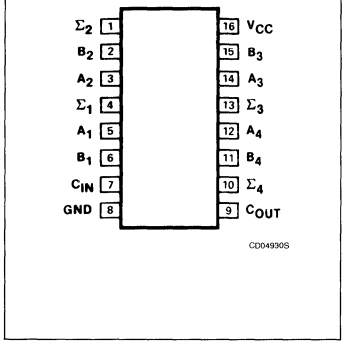
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_4$	A operand inputs	1.0/2.0	20μA/1.2mA
$B_1 - B_4$	B operand inputs	1.0/2.0	20μA/1.2mA
C_{IN}	Carry input	1.0/1.0	20μA/0.6mA
$\Sigma_1 - \Sigma_4$	Sum outputs	50/33	1.0mA/20mA
C_{OUT}	Carry output	50/33	1.0mA/20mA

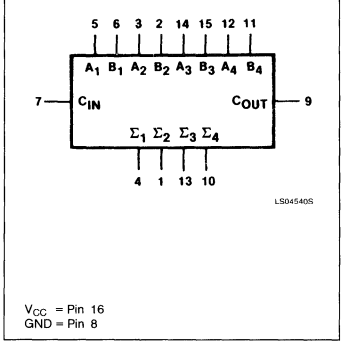
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

PIN CONFIGURATION

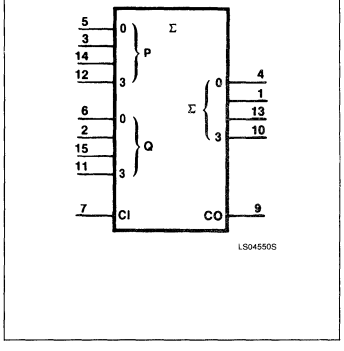


LOGIC SYMBOL



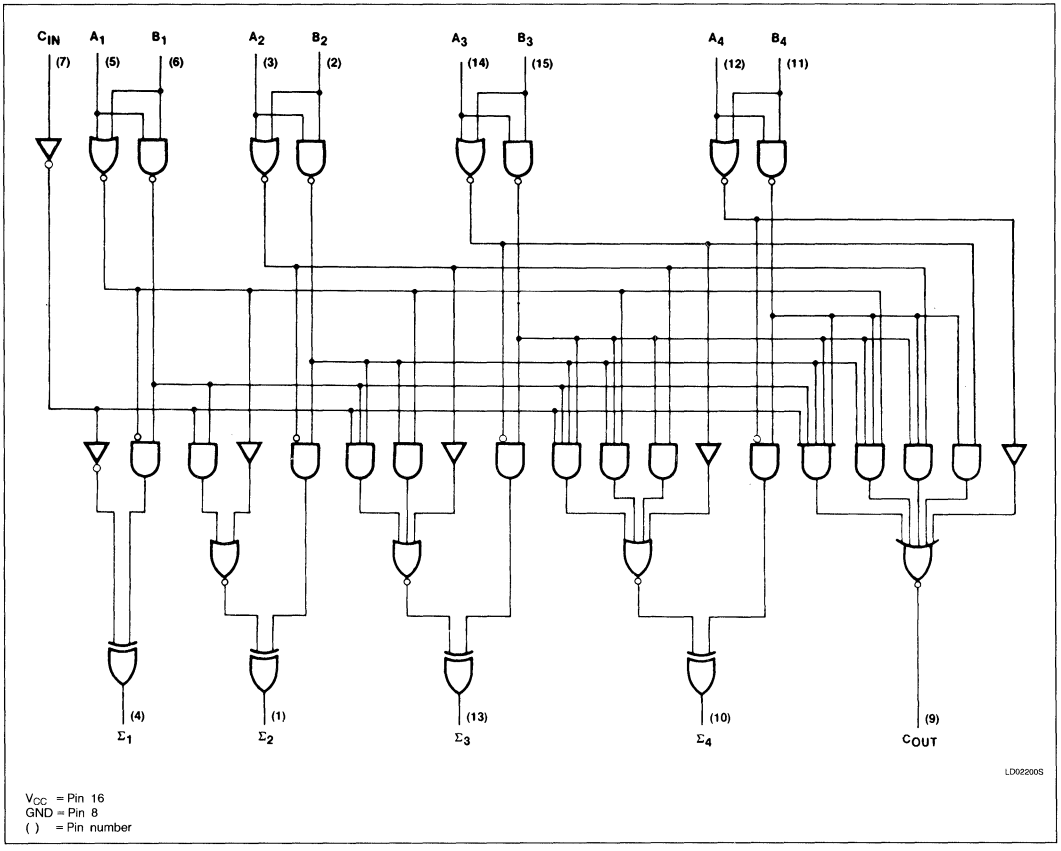
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



4-Bit Adder FAST 74F283

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin number

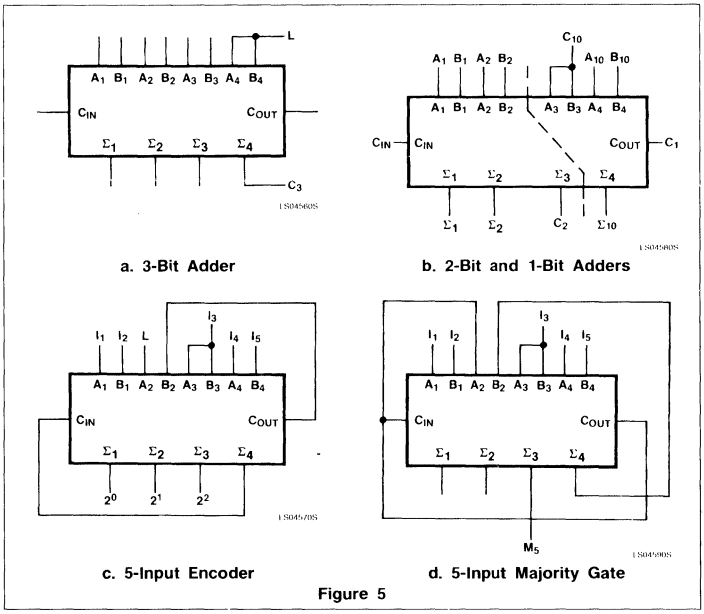
FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

H = HIGH voltage level
L = LOW voltage level

Example:
1001
1010
10011
(10 + 9 = 19)
(carry + 5 + 6 = 12)

Due to pin limitations, the intermediate carries of the '283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure a shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure b shows a way of dividing the '283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. Figure c shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs $I_1 - I_5$ that are true. Figure d shows one method of implementing a 5-input majority gate. When three or more of the inputs $I_1 - I_5$ are true, the output M_5 is true.



a. 3-Bit Adder

b. 2-Bit and 1-Bit Adders

c. 5-Input Encoder

d. 5-Input Majority Gate

Figure 5

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F283 Min	74F283 Typ[2]	74F283 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	$A_1 - A_4$, $B_1 - B_4$	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		C_{IN}				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				55	mA

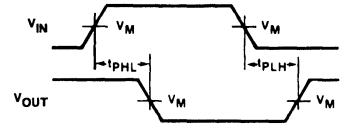
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} should be measured with all outputs open and the following conditions:
   Condition 1: all inputs grounded
   Condition 2: all B inputs LOW, other inputs at 4.5V
   Condition 3: all inputs at 4.5V.

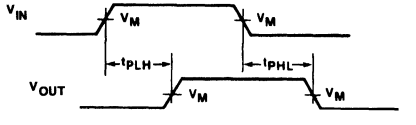
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F283 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F283 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_i	Waveforms 1 and 2	3.5 4.0	7.0 7.0	9.5 9.5	3.5 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveforms 1 and 2	4.0 3.5	7.0 7.0	9.5 9.5	4.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5 3.0	5.7 5.4	7.5 7.0	3.5 3.0	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveforms 1 and 2	3.5 3.0	5.7 5.3	7.5 7.0	3.5 3.0	8.5 8.0	ns

AC WAVEFORMS



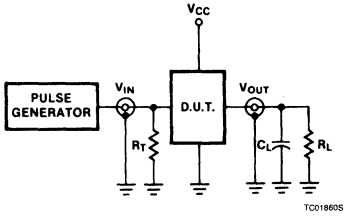
Waveform 1. For Inverting Outputs



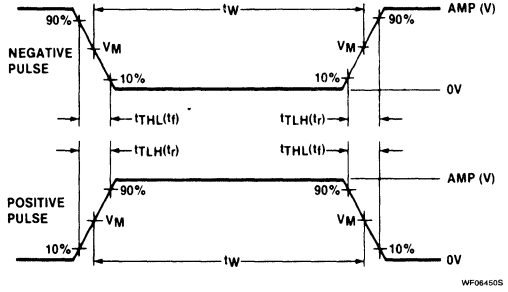
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F298
Multiplexer

Quad 2-Input Multiplexer With Storage
Product Specification

Logic Products

FEATURES

- **Fully synchronous operation**
- **Select from two data sources**
- **Buffered, negative edge triggered clock**
- **Provides the equivalent of function capabilities of two separate MSI functions (74F157 and 74F175)**

DESCRIPTION

The 'F298 is a high-speed Multiplexer with storage. It selects 4 bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit register is fully edge triggered. The Data inputs (I_0 and I_1) and Select input (S) must be stable only one set-up time prior to the HIGH-to-LOW transition of the clock for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F298	115MHz	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F298N
Plastic SO-16	N74F298D

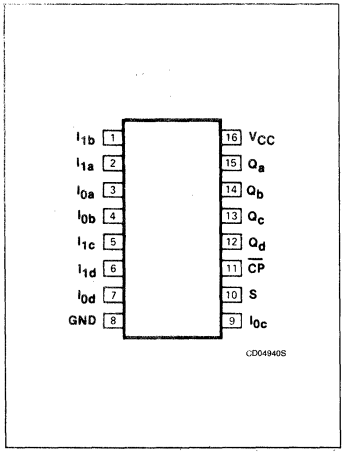
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

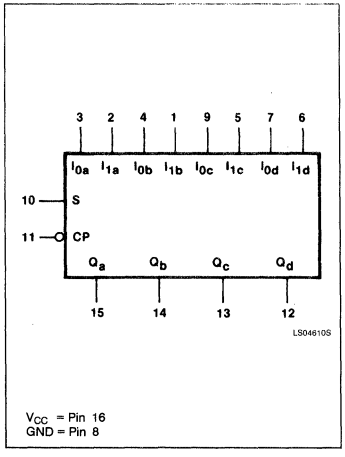
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{1a}, I_{1b}, I_{1c}, I_{1d}	Data inputs	1.0/1.0	20μA/0.6mA
I_{0a}, I_{0b}, I_{0c}, I_{0d}	Data inputs	1.0/1.0	20μA/0.6mA
S	Select input	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
Q_a, Q_b, Q_c, Q_d	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

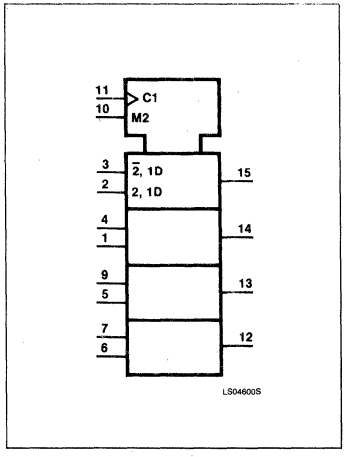
PIN CONFIGURATION



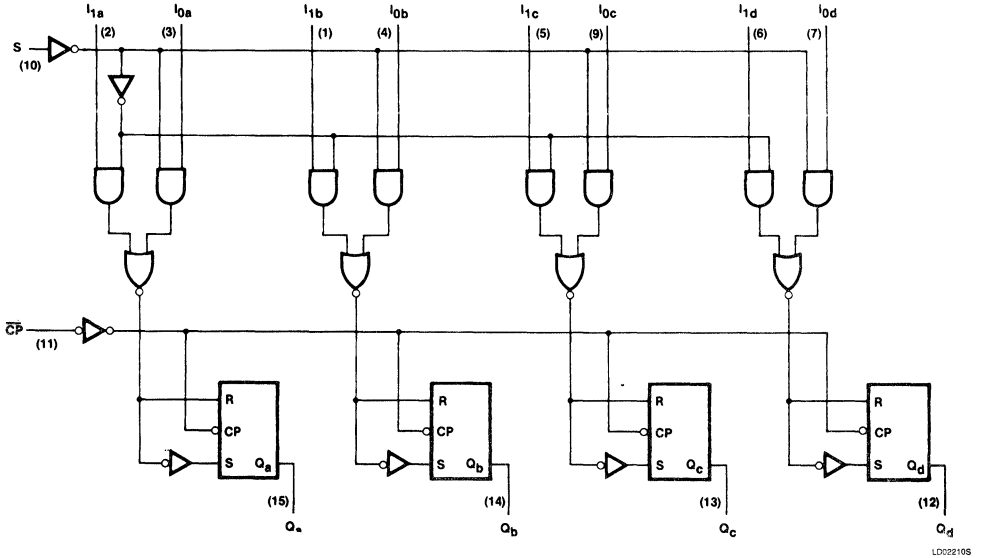
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F298 Min	74F298 Typ[2]	74F298 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				32	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

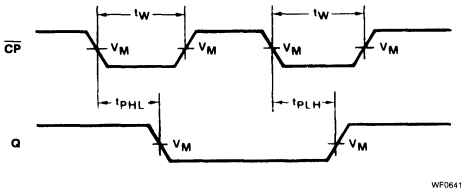
PARAMETER		TEST CONDITIONS	74F298 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F298 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	110	115		105		MHz
t_{PLH}	Propagation delay, $\overline{CP}$ to Q_n	Waveform 1	4.0	5.5	7.5	4.0	9.0	ns
t_{PHL}			4.5	6.5	8.5	4.5	9.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

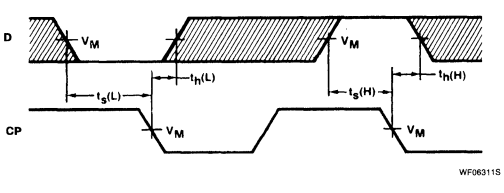
PARAMETER		TEST CONDITIONS	74F298 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F298 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_s(H)	Set-up time, HIGH or LOW I_{On}, I_{1n} to $\overline{CP}$	Waveform 2	2.0			2.0		ns
t_s(L)			2.0			2.0		ns
t_h(H)	Hold time, HIGH or LOW I_{On}, I_{1n} to $\overline{CP}$	Waveform 2	1.0			1.0		ns
t_h(L)			1.0			1.0		ns
t_s(H)	Set-up time, HIGH or LOW S to $\overline{CP}$	Waveform 2	6.0			7.0		ns
t_s(L)			5.0			6.0		ns
t_h(H)	Hold time, HIGH or LOW S to $\overline{CP}$	Waveform 2	0			0		ns
t_h(L)			0			0		ns
t_w(H)	$\overline{CP}$ pulse width, HIGH or LOW	Waveform 1	5.0			5.0		ns
t_w(L)			5.0			7.0		ns

AC WAVEFORMS



WF06412S

Waveform 1. Clock To Output Delays And Clock Pulse Width

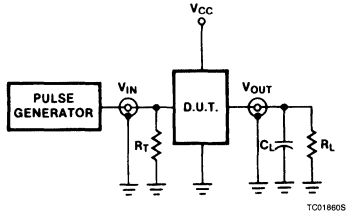


WF06311S

Waveform 2. Data Set-up And Hold Times

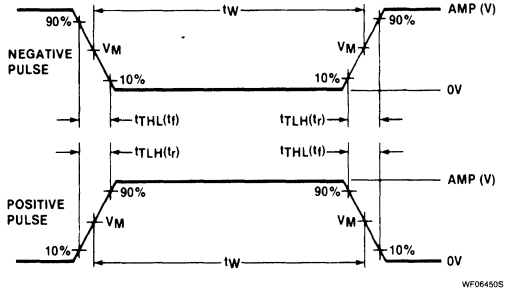
NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



TC01860S

Test Circuit For Totem-Pole Outputs



WF06450S

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

FAST 74F299
Register

8-Input Universal Shift/Storage Register (3-State)
Preliminary Specification

Logic Products

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional Serial inputs and outputs for expansion**
- **Four operating modes: Shift Left, Shift Right, Load and Store**
- **3-State outputs for bus-oriented applications**

DESCRIPTION

The 'F299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-LOW Master Reset is used to reset the register.

TYPE	TYPICAL	TYPICAL SUPPLY CURRENT (TOTAL)
74F299	100MHz	68mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F299N
Plastic SOL-20	N74F299D

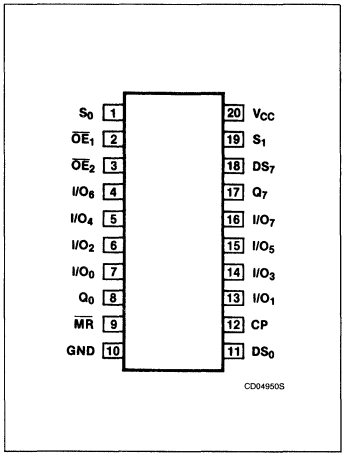
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

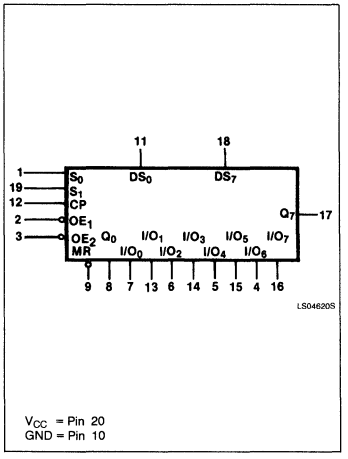
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
DS_0	Serial data input for right shift	1.0/1.0	20μA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode select inputs	1.0/2.0	20μA/1.2mA
$\overline{MR}$	Asynchronous master reset input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}_1$, $\overline{OE}_2$	3-State output enable inputs (active Low)	1.0/1.0	20μA/0.6mA
$\overline{I/O}_0$, $\overline{I/O}_7$	Parallel data inputs or 3-state parallel outputs	1.0/1.0 150/33	20μA/0.6mA 3.0mA/20mA
Q_0, Q_7	Serial outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

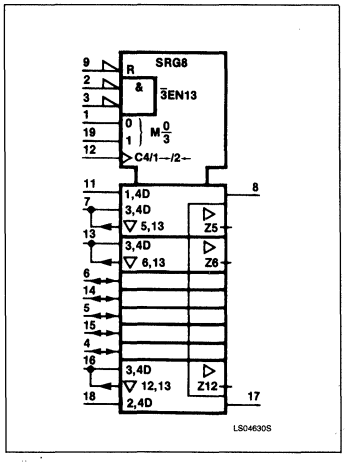
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



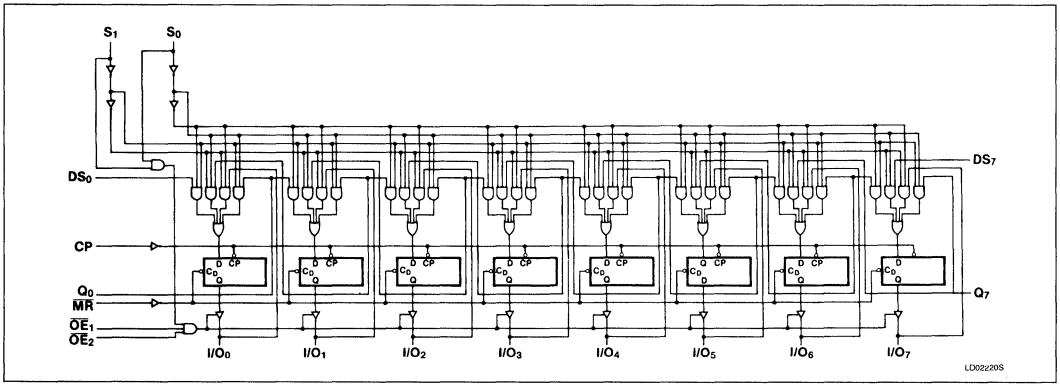
Register | FAST 74F299

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; $Q_0 - Q_7$ = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F299			UNIT
				Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL} LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH} HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL} LOW-level input current	S_0, S_1	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
	Other inputs				−0.4	−0.6	mA
I_{OZH} Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	70	μA
I_{OZL} Off-state output current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−650	μA
I_{OS} Short-circuit output current[3]		V_{CC} = MAX		−60	−80	−150	mA
I_{CC} Supply current (total)	I_{CCH}	V_{CC} = MAX					mA
	I_{CCL}				68	92	mA
	I_{CCZ}						mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

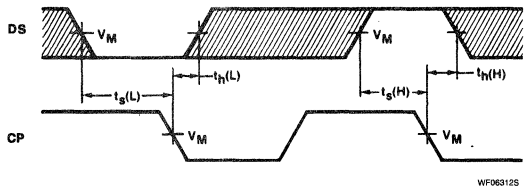
PARAMETER		TEST CONDITIONS	74F299					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 2	70	100		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0 or Q_7	Waveform 2	4.0 3.5	7.0 6.5	9.0 8.5	4.0 3.5	10 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 2	4.0 5.0	7.0 8.5	9.0 11	4.0 5.0	10 12	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_0 or Q_7	Waveform 3	4.5	7.5	9.5	4.5	10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 3	6.5	11	14	6.5	15	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	Waveform 4 Waveform 5	3.5 4.0	6.0 7.0	8.0 10.0	3.5 4.0	9.0 11	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 4 Waveform 5	2.5 2.0	4.5 4.0	6.0 5.5	2.5 2.0	7.0 6.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

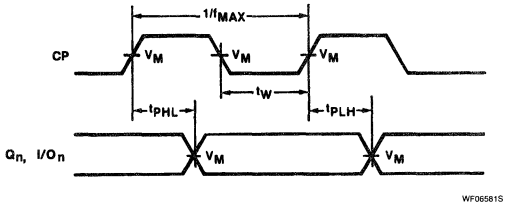
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F299					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW S_0 or S_1 to CP	Waveform 1	8.5 8.5			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S_0 or S_1 to CP	Waveform 1	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	Waveform 1	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	Waveform 1	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW	Waveform 2	7.0 7.0			7.0 7.0		ns
$t_w(L)$	$\overline{MR}$ pulse width LOW	Waveform 3	7.0			7.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	7.0			7.0		ns

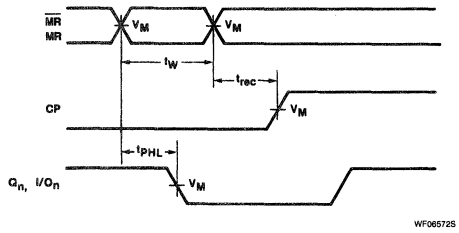
AC WAVEFORMS



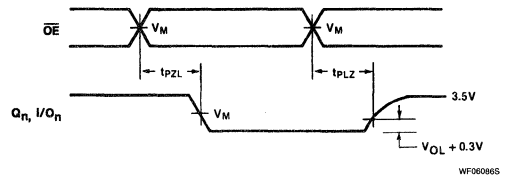
Waveform 1. Data Set-up And Hold Times



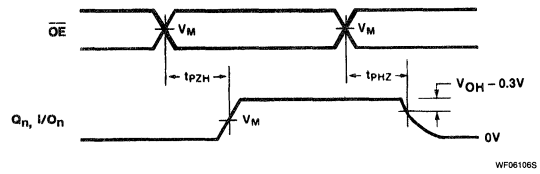
Waveform 2. Clock To Output Delays And Clock Pulse Width



Waveform 3. Master Reset Pulse Width Master Reset To Output Delay & Master Reset To Clock Recovery Time



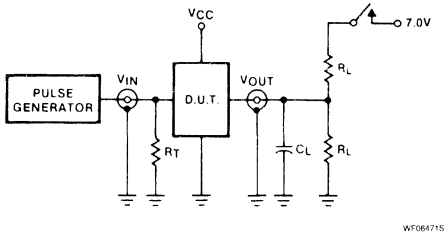
Waveform 4. 3-State Enable Time To LOW Level And Disable Time From LOW Level

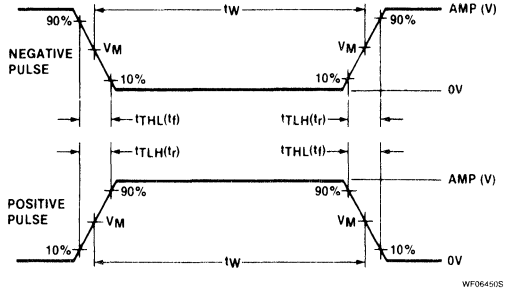


Waveform 5. 3-State Time To HIGH Level And Disable Time From HIGH Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS





Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

FAST 74F322
Register

8-Bit Serial/Parallel Register With Sign Extend (3-State)
Preliminary Specification

Logic Products

FEATURES
- **Multiplexed parallel I/O ports**
- **Separate Serial input and output**
- **Sign extend function**
- **3-State outputs for bus applications**

DESCRIPTION
The 'F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-State parallel outputs plus a bi-state Serial output. Parallel Data inputs and outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend, and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F322	90 MHz	60mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F322N
Plastic SOL-24	N74F322D

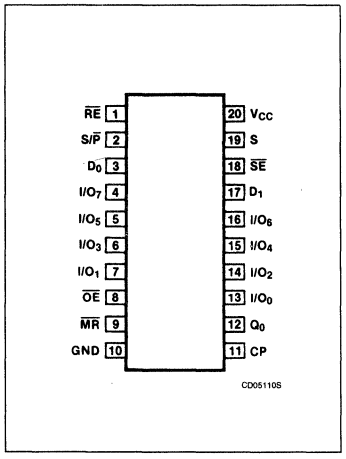
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

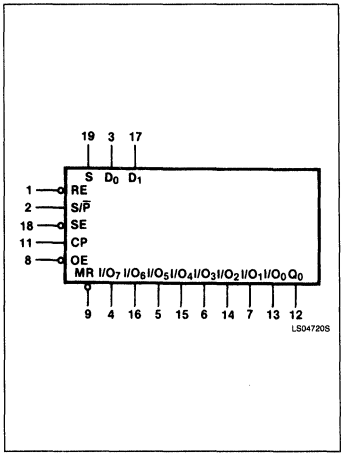
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{RE}$	Register enable input (active LOW)	1.0/1.0	20μA/0.6mA
S/$\overline{P}$	Serial (HIGH) or parallel (LOW) mode Control input	1.0/1.0	20μA/0.6mA
$\overline{SE}$	Sign extend input (active LOW)	1.0/3.0	20μA/1.8mA
S	Serial data select input	1.0/2.0	20μA/1.2mA
D_0, D_1	Serial data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	3-State output enable input (active LOW)	1.0/1.0	20μA/0.6mA
Q_0	Bi-state serial output	50/33	1.0mA/20mA
$I/O_0 - I/O_7$	Multiplexed parallel data inputs or	1.0/1.0	20μA/0.6mA
	3-State parallel data outputs	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

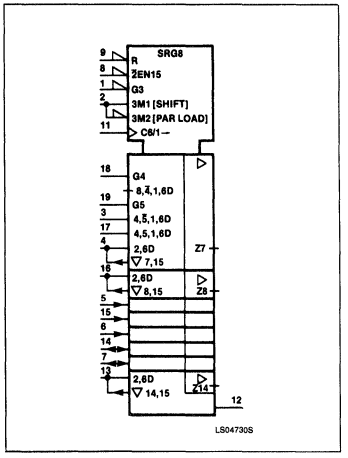
PIN CONFIGURATION



LOGIC SYMBOL



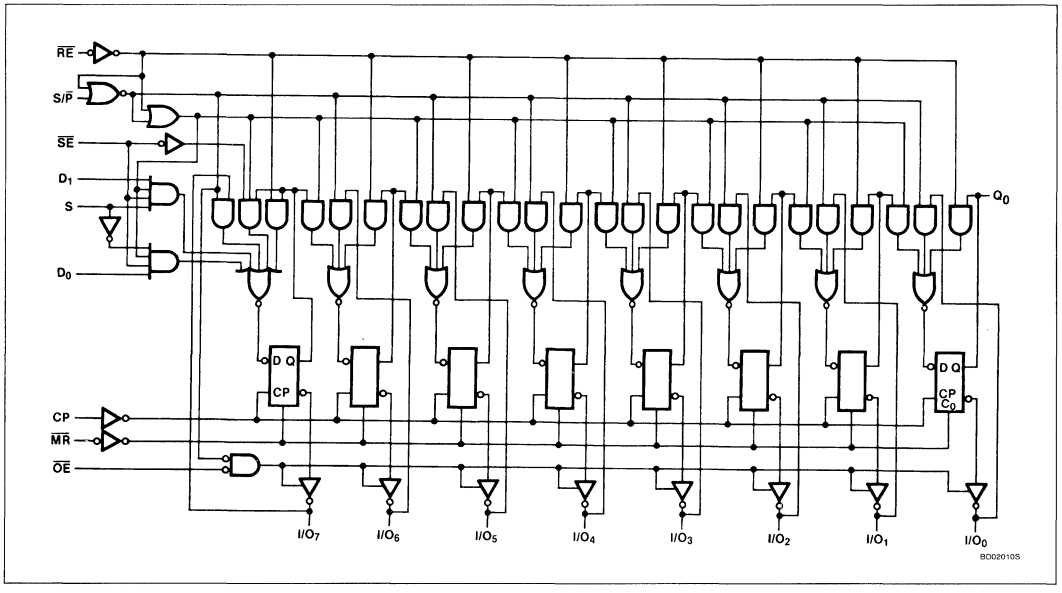
LOGIC SYMBOL (IEEE/IEC)



Register | FAST 74F322

The 'F322 contains eight D-type edge-triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/$\overline{P}$ enables shift right, while a LOW signal disables the 3-State output buffers and enables parallel loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents, thus performing the sign extend function required for the 'LS384 Two's Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the 3-State output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

LOGIC DIAGRAM



FUNCTION TABLE

MODE	INPUTS							OUTPUTS								
	$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Q_0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I_0
Shift Right	H	L	H	H	L	L	↑	D_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
	H	L	H	H	H	L	↑	D_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Sign Extend	H	L	H	L	X	L	↑	O_7	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH, all I/O_n terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

NOTES:

1. $I_7 - I_0$ = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the I/O terminal.
2. $D_0 - D_1$ = The level of the steady-state inputs to the serial multiplexer input.
3. $O_7 - O_0$ = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.
4. NC = No change; Z = High-Impedance Output State; H = HIGH Voltage Level; L = LOW Voltage Level; ↑ = LOW-to-HIGH Clock Transition.
5. ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F322			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	$\overline{SE}$	V_{CC} = MAX, V_I = 0.5V				−1.8	mA
		S					−1.2	mA
		Others				−0.4	−0.6	mA
I_{OZH} + I_{IH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				70	μA
I_{OZL} + I_{IL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−600	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX, CP = $\overline{OE}$ = 4.5V			60	84	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F322					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	70	90		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4 5	7 8.5	9 11	4 5	10 12	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_0	Waveform 1	3.5 3.5	7 7	9 9	3.5 3.5	10 10	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 3	6	10	13	6	14	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_0	Waveform 3	5.5	9.5	12.0	5.5	13	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	3 4	6.5 8.5	9 11	3 4	10 12	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	2 2	4.5 5	6 7	2 2	7 8	ns
t_{PZH} t_{PZL}	Output enable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.5 5.5	8 10	10.5 14	4.5 5.5	11.5 15	ns
t_{PHZ} t_{PLZ}	Output disable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	5 6	9 12	11.5 15.5	5 6	12.5 16.5	ns

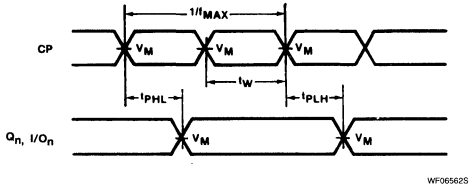
NOTE:
Subtract 0.2ns from minimum values for SO package.

6

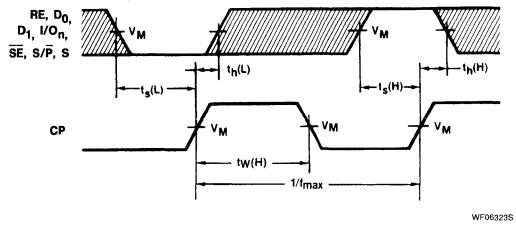
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F322					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{RE}$ to CP	Waveform 2	12 12			13 13		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{RE}$ to CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_0, D_1 or I/O_n to CP	Waveform 2	8 8			9 9		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_0, D_1 or I/O_n to CP	Waveform 2	2 2			3 3		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{SE}$ to CP	Waveform 2	7 7			8 8		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{SE}$ to CP	Waveform 2	2 2			2 2		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW S/$\overline{P}$ to CP	Waveform 2	12 12			13 13		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW S to CP	Waveform 2	8 8			9 9		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S or S/$\overline{P}$ to CP	Waveform 2	0 0			0 0		ns
$t_W(H)$	CP pulse width HIGH	Waveform 1	7			7		ns
$t_W(L)$	$\overline{MR}$ pulse width LOW	Waveform 3	7			7		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	8			8		ns

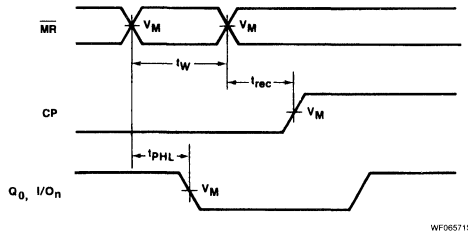
AC WAVEFORMS



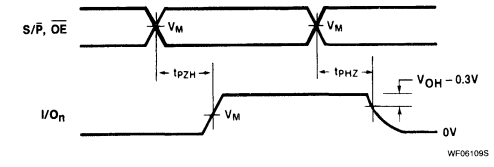
Waveform 1. Clock To Output Delays And Clock Pulse Width



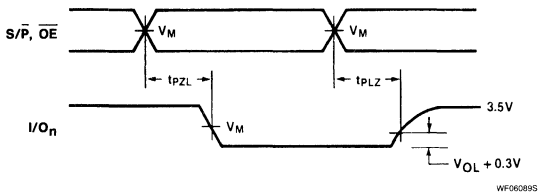
Waveform 2. Data Set-up And Hold Times



Waveform 3. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



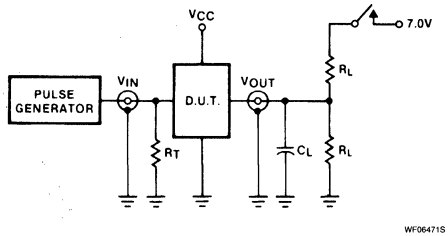
Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



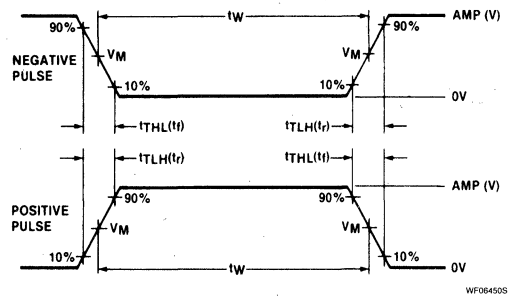
Waveform 5. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F323
Register

8-Bit Universal Shift/Storage Register
With Synchronous Reset and Common I/O Pins (3-State)
Preliminary Specification

Logic Products

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional Serial inputs and outputs for expansion**
- **Four operating modes: Shift Left, Shift Right, Load and Store**
- **3-State outputs for bus-oriented applications**

DESCRIPTION

The 'F323 is an 8-bit universal shift/storage register with 3-State outputs. Its function is similar to the 'F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

The 'F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select table.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F323	100 MHz	68mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F323N
Plastic SOL-20	N74F323D

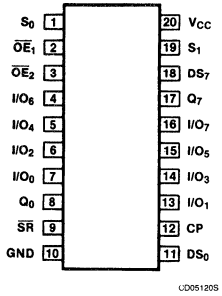
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

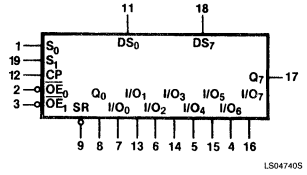
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
DS_0	Serial data input for right shift	1.0/1.0	20μA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode select inputs	1.0/2.0	20μA/1.2mA
$\overline{SR}$	Synchronous reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	3-State output enable inputs (active LOW)	1.0/1.0	20μA/0.6mA
$I/O_0 - I/O_7$	Multiplexed parallel data inputs or	1.0/1.0	20μA/0.6mA
	3-State parallel data outputs	150/33	3.0mA/20mA
Q_0, Q_7	Serial outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

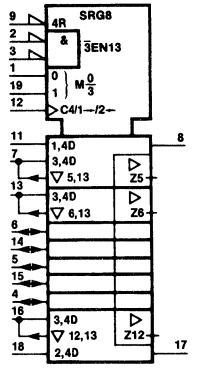
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



6

Register | FAST 74F323

All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change with the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

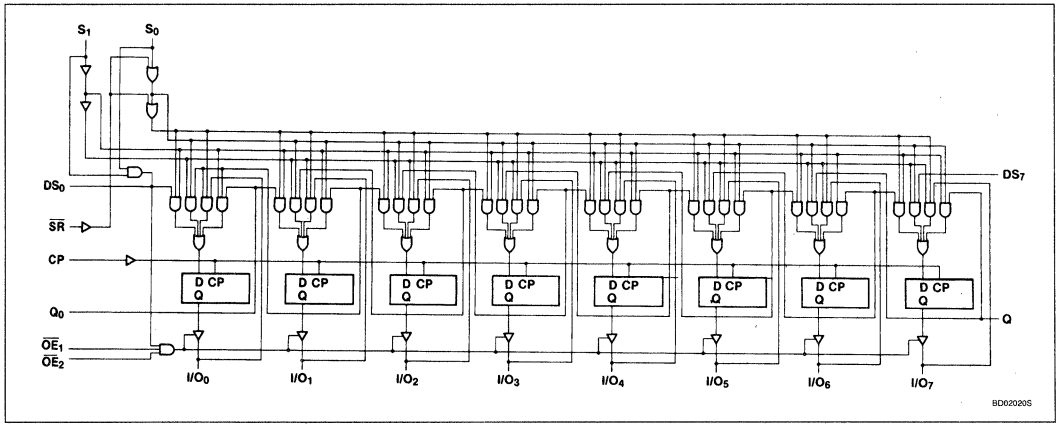
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-State buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The 3-State buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

FUNCTION TABLE

INPUTS				RESPONSE
$\overline{SR}$	S_1	S_0	CP	
L	X	X		Synchronous Reset; $Q_0 - Q_7$ = LOW
H	H	H		Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H		Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.)
H	H	L		Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	H	H	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F323			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_L	LOW-level input current	S_0, S_1	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		Others				−0.4	−0.6	mA
I_{OZH} + I_{IH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				70	μA
I_{OZL} + I_{IL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−650	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX					mA
		I_{CCL}					92	mA
		I_{CCZ}						mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

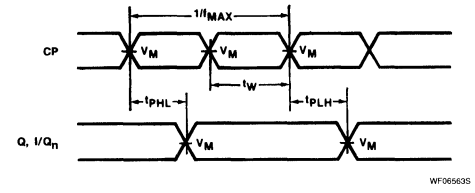
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F323					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum input frequency	Waveform 1	70			70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0 or Q_7	Waveform 1	4.0 3.5	7.0 6.5	9.0 8.5	4.0 3.5	10 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 5.0	7.0 8.5	9.0 11	4.0 5.0	10 12	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	Waveform 3 Waveform 4	3.5 4.0	6.0 7.0	8.0 10	3.5 4.0	9.0 11	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 3 Waveform 4	2.5 2.0	4.5 4.0	6.0 5.5	2.5 2.0	7.0 6.5	ns

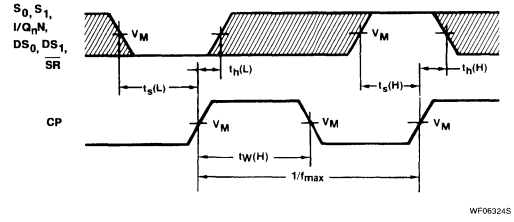
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F323					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW S_0 or S_1 to CP	Waveform 2	8.5 8.5					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S_0 or S_1 to CP	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	Waveform 2	5.0 5.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	Waveform 2	2.0 2.0					ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{SR}$ to CP	Waveform 2	10 10					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{SR}$ to CP	Waveform 2	0 0					ns
$t_W(H)$ $t_W(L)$	CP pulse width, HIGH or LOW	Waveform 1	7.0 7.0					ns

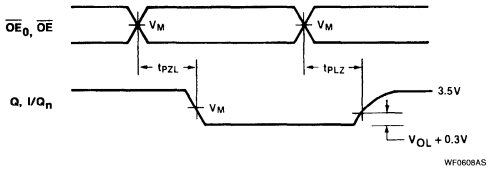
AC WAVEFORMS



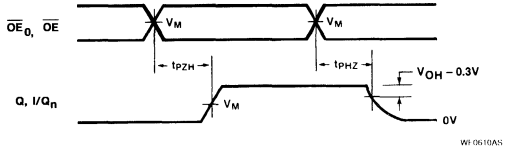
Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Data Set-up And Hold Times



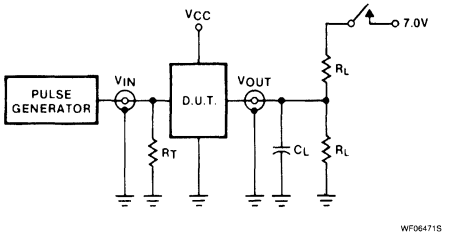
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



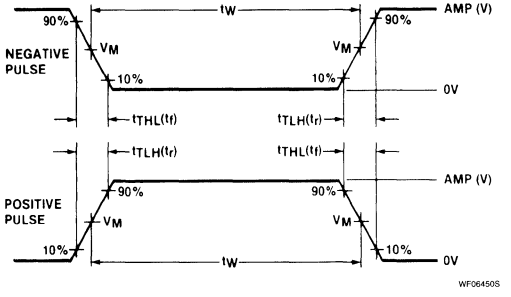
Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F350
Shifter

4-Bit Shifter (3-State)
Product Specification

Logic Products

FEATURES

- **Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines**
- **3-State outputs for bus organized systems**

DESCRIPTION

The 'F350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.

The 'F350 can be used to shift any number of places up or down by suitable interconnection. Shifting can be:

1. Logical — with logic zeros filled in at either end of the shifting field.
2. Arithmetic — where the sign bit is extended during a shift down.
3. End around — where the data word forms a continuous loop.

The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active LOW Output Enable ($\overline{OE}$) input controls the state of the outputs. The outputs are in the HIGH impedance "off" state when $\overline{OE}$ is HIGH, and they are active when $\overline{OE}$ is LOW.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F350	5.2ns	24mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F350N
Plastic SO-16	N74F350D

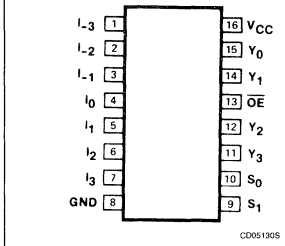
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

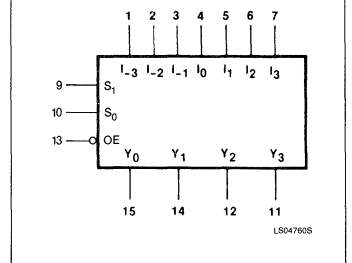
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
S_0, S_1	Select inputs	1.0/2.0	20μA/1.2mA
$I_{-3} - I_3$	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{OE}$	Output enable input (Active LOW)	1.0/2.0	20μA/1.2mA
$Y_0 - Y_3$	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

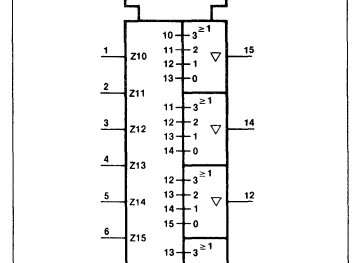
PIN CONFIGURATION



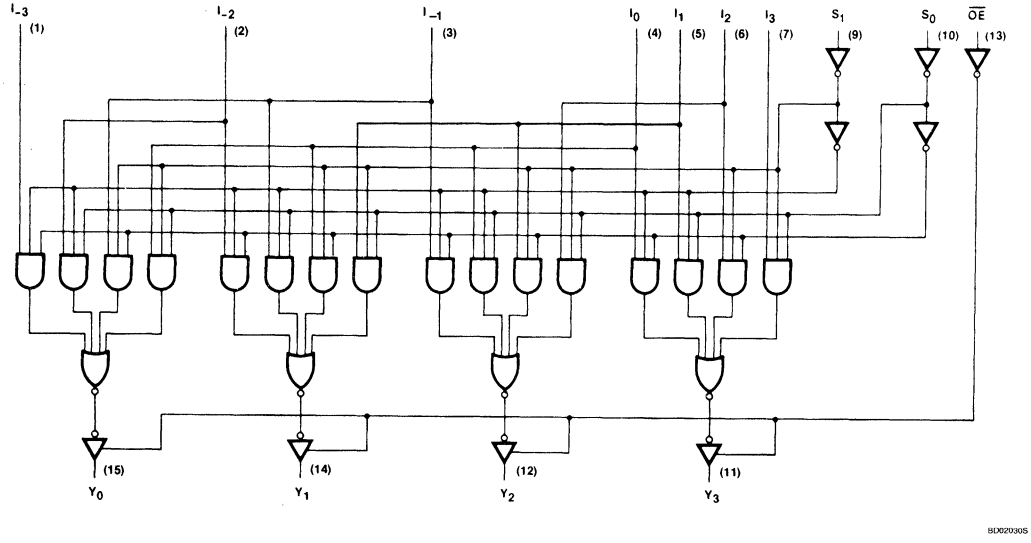
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTION TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state
D_n = HIGH or LOW state of referenced I_n input

LOGIC EQUATIONS

$$Y_0 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_0 + S_0 \cdot \overline{S}_1 \cdot I_{-1} + \overline{S}_0 \cdot S_1 \cdot I_{-2} + S_0 \cdot S_1 \cdot I_{-3}$$
$$Y_1 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_1 + S_0 \cdot \overline{S}_1 \cdot I_0 + \overline{S}_0 \cdot S_1 \cdot I_{-1} + S_0 \cdot S_1 \cdot I_{-2}$$
$$Y_2 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_2 + S_0 \cdot \overline{S}_1 \cdot I_1 + \overline{S}_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot I_{-1}$$
$$Y_3 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_3 + S_0 \cdot \overline{S}_1 \cdot I_2 + \overline{S}_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0$$

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F350 Min	74F350 Typ[2]	74F350 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.9	−1.2	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX			22	35	mA
	I_{CCL}				26	41	mA
	I_{CCZ}				26	42	mA

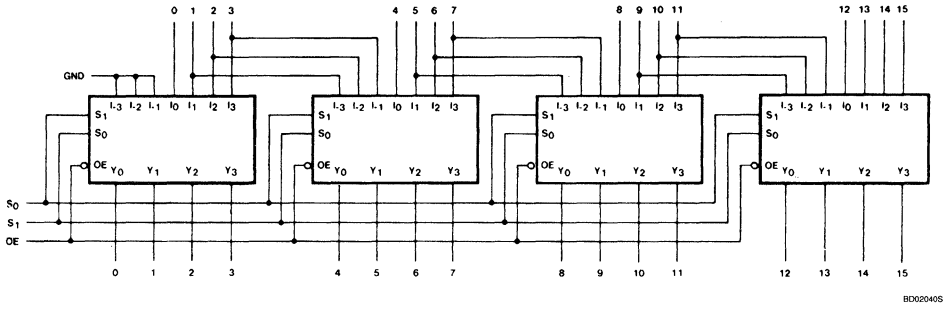
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F350 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F350 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay	Waveform 1	3.0	4.5	6.0	3.0	7.0	ns
t_{PHL}	I_n to Y_n		2.5	4.0	5.5	2.5	6.5	
t_{PLH}	Propagation delay	Waveform 1	4.0	7.8	10	4.0	11	ns
t_{PHL}	S_n to Y_n		3.0	6.5	8.5	3.0	9.5	
t_{PZH}	Output enable time to	Waveform 2	2.5	5.0	7.0	2.5	8.0	ns
t_{PZL}	HIGH or LOW level	Waveform 3	4.0	7.0	9.0	4.0	10	
t_{PHZ}	Output disable time from	Waveform 2	2.0	3.9	5.5	2.0	6.5	ns
t_{PLZ}	HIGH or LOW level	Waveform 3	2.0	4.0	5.5	2.0	6.5	

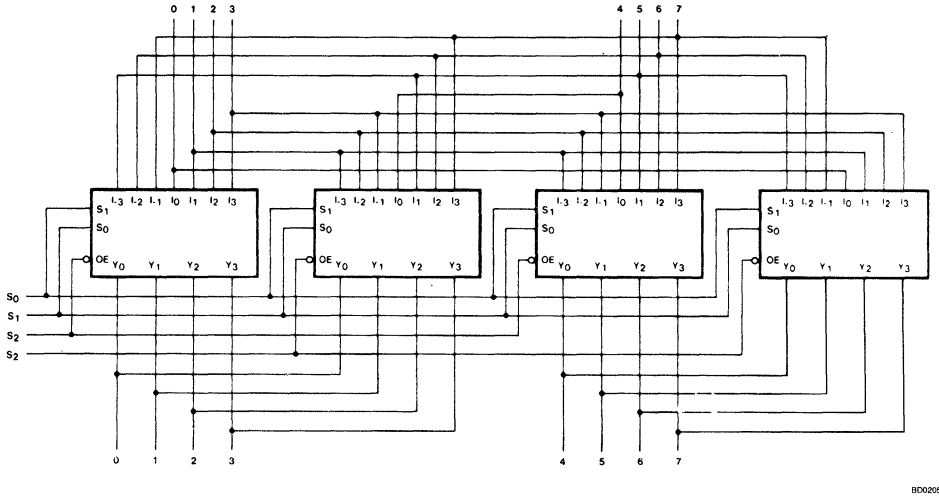
NOTE:
Subtract 0.2ns from minimum values for SO package.

APPLICATIONS



S_2	S_1	S_0	
L	L	L	No shift
L	L	H	Shift end around 1
L	H	L	Shift end around 2
L	H	H	Shift end around 3
H	L	L	Shift end around 4
H	L	H	Shift end around 5
H	H	L	Shift end around 6
H	H	H	Shift end around 7

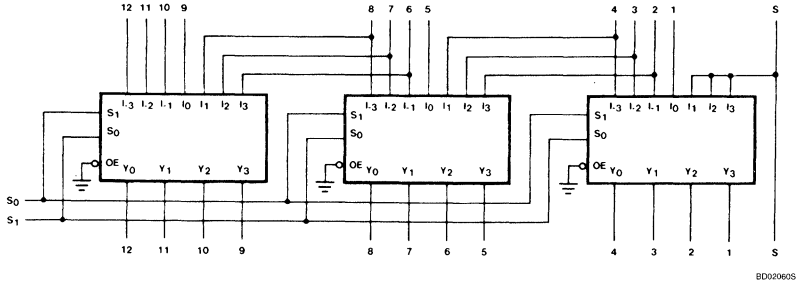
8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places



S_1	S_0	Scale
L	L ÷ 8	1/8
L	H ÷ 4	1/4
H	L ÷ 2	1/2
H	H No change	1

13-Bit 2's Complement Scaler

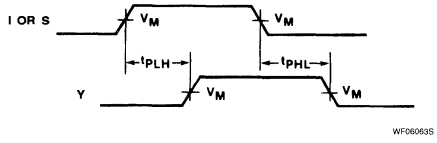
APPLICATIONS Continued



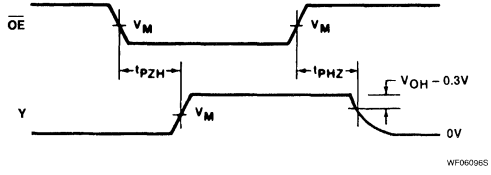
S_1	S_0	
L	L	No shift
L	H	Shift 1 place
H	L	Shift 2 places
H	H	Shift 3 places

16-Bit Shift Up 0, 1, 2, or 3 Places

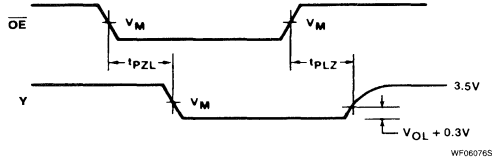
AC WAVEFORMS



Waveform 1. Propogation Delay Data And Select To Output



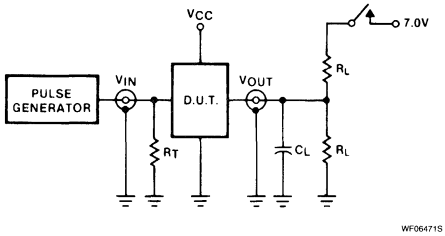
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



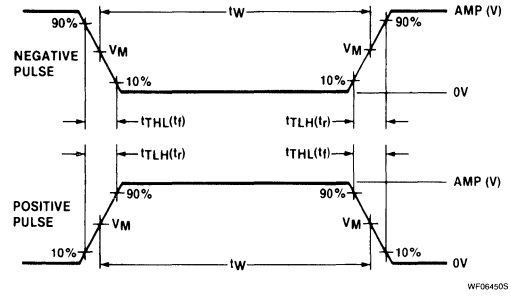
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F352
Multiplexer

Dual 4-Line to 1-Line Multiplexer
Product Specification

Logic Products

FEATURES
- **Inverting version of 'F153**
- **Separate Enable for each multiplexer section**
- **Common Select inputs**
- **See 'F353 for 3-State version**

DESCRIPTION
The 'F352 has a dual 4-input multiplexer that can select 2 bits of data from up to eight sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs ($\overline{Y}_a$, $\overline{Y}_b$) are forced HIGH when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs.

The 'F352 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F352	5.5ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F352N
Plastic SO-16	N74F352D

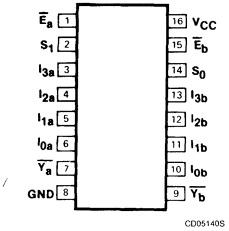
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

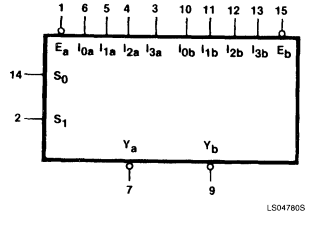
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{3a}$	Port A data inputs	1.0/1.0	20μA/0.6mA
$I_{0b} - I_{3b}$	Port B data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Port A, B enable inputs (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{Y}_a$, $\overline{Y}_b$	Multiplexer outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

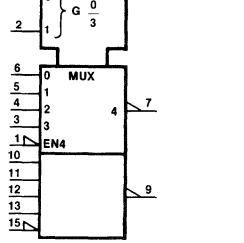
PIN CONFIGURATION



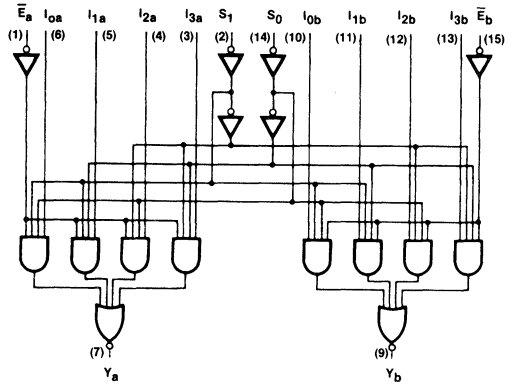
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	$\overline{E}$	I_{0n}	I_{1n}	I_{2n}	I_{3n}	$\overline{Y}_n$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F352			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−85	−150	mA
I_{CC}	Supply current (total I_{CCH})	V_{CC} = MAX	$\overline{E}_n$ = S_n = I_n = GND		8	14	mA
	Supply current (total I_{CCL})		$\overline{E}_n$ = GND, S_n = I_n = 4.5V		12	20	mA

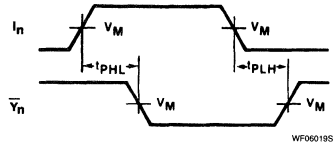
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequences of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

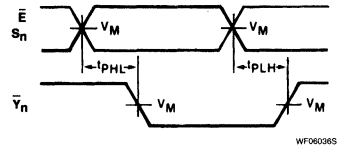
PARAMETER		TEST CONDITIONS	74F352					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.5	5.0	7.0	2.0	8.0	ns
t_{PHL}	I_{on} to $\overline{Y}_n$		1.5	3.0	4.5	1.0	8.0	
t_{PLH}	Propagation delay	Waveform 2	4.5	6.5	11.0	4.0	12.5	ns
t_{PHL}	S_n to $\overline{Y}_n$		4.0	6.0	8.5	3.5	9.5	
t_{PLH}	Propagation delay	Waveform 2	2.5	5.0	6.5	2.0	7.0	ns
t_{PHL}	$\overline{E}_n$ to $\overline{Y}_n$		3.5	6.0	8.0	3.0	8.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



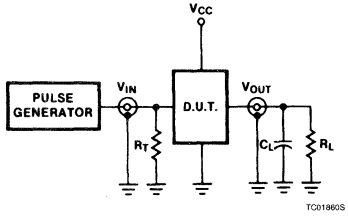
Waveform 1. Propagation Delay For Data To Output



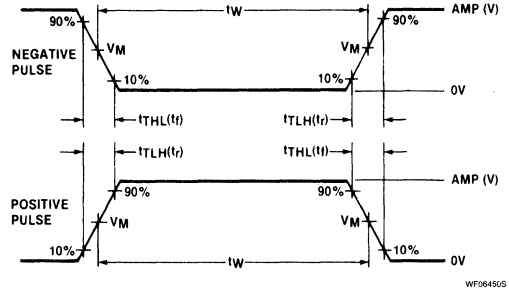
Waveform 2. Propagation Delay For Select Or Enable To Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F353
Multiplexer

Dual 4-Input Multiplexer (3-State)
Product Specification

Logic Products

FEATURES

- **Inverting version of 'F253**
- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

DESCRIPTION

The 'F353 has two identical 4-input multiplexers with 3-State outputs which select two bits from eight sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

The 'F353 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs.

Logic equations for the outputs are shown below:

$$\overline{Y}_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet = o + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Y}_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet = o + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F353	6.0ns	11mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F353N
Plastic SO-16	N74F353D

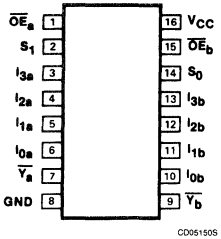
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

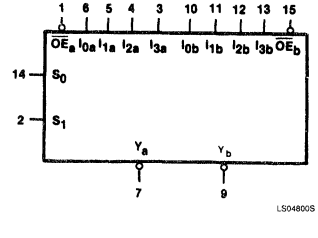
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{3a}$	Port A data inputs	1.0/1.0	20μA/0.6mA
$I_{0b} - I_{1b}$	Port B data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}_a$, $\overline{OE}_b$	Port A, B output enable inputs (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{Y}_a$, $\overline{Y}_b$	3-State outputs (inverted)	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

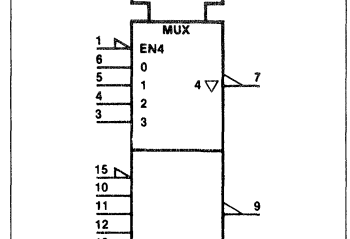
PIN CONFIGURATION



LOGIC SYMBOL

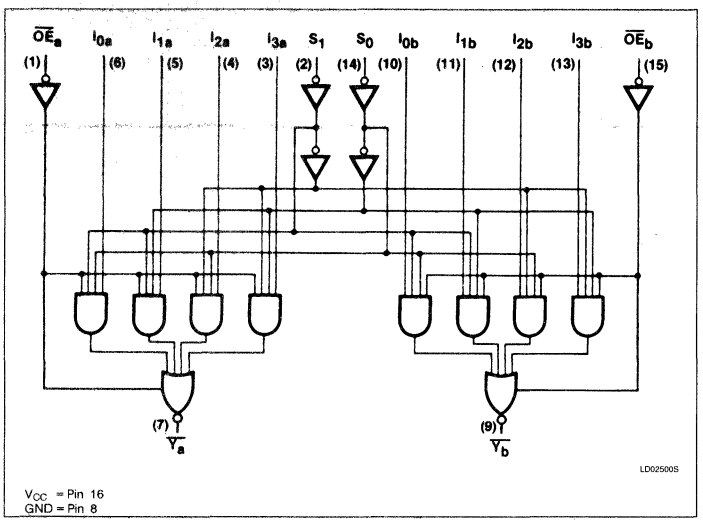


LOGIC SYMBOL (IEEE/IEC)



Multiplexer FAST 74F353

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F353			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−90	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX, $\overline{OE}_n$ = S_n = I_n = GND		9	14	mA
		I_{CCL}	V_{CC} = MAX, S_n = $\overline{OE}_n$ = GND; I_n = 4.5		11	20	mA
		I_{CCZ}	V_{CC} = MAX, $\overline{OE}_n$ = 4.5V; S_n = I_n = GND		13	23	mA

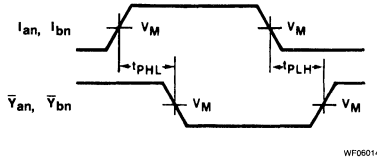
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

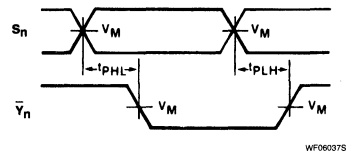
PARAMETER		TEST CONDITIONS	74F353					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	3.0	5.0	7.0	3.0	8.0	ns
t_{PHL}	I_n to $\overline{Y}_n$		1.5	3.0	5.0	1.0	5.5	
t_{PLH}	Propagation delay	Waveform 2	5.0	9.0	12.0	4.5	12.5	ns
t_{PHL}	S_n to $\overline{Y}_n$		3.0	6.0	8.5	3.0	9.5	
t_{PZH}	Output enable time to	Waveform 3	4.0	6.0	8.0	3.5	9.0	ns
t_{PZL}	HIGH or LOW level	Waveform 4	4.0	6.5	8.0	3.5	9.0	
t_{PHZ}	Output disable time from	Waveform 3	2.5	4.0	5.5	2.0	6.0	ns
t_{PLZ}	HIGH or LOW level	Waveform 4	1.5	2.5	6.0	1.5	7.0	

NOTE:
Subtract 0.2ns from minimum values for SO package.

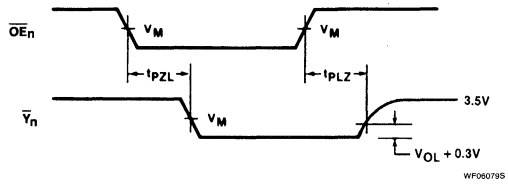
AC WAVEFORMS



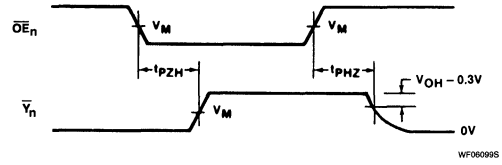
Waveform 1. Propagation Delay (I_n) To Output (Y_n)



Waveform 2. Propagation Delay Select (S_n) To Output (Y_n)



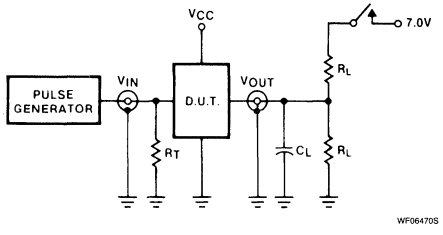
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



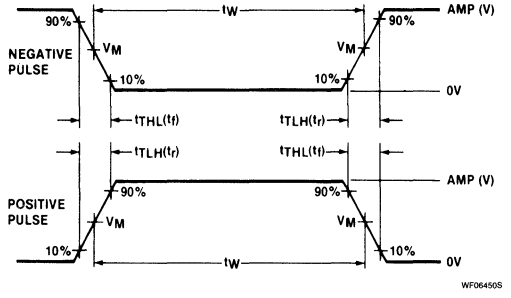
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F365, F366, F367, F368
Buffers/Drivers

'F365, 'F367 Hex Buffer/Driver (3-State)
'F366, 'F368 Hex Inverter Buffer (3-State)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in LOW and HIGH states)**
- **3-State buffer outputs sink 64mA**
- **High speed**
- **Bus oriented**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F365	5.0ns	36mA
74F366	5.0ns	36mA
74F367	5.0ns	36mA
74F368	5.0ns	36mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F365N, N74F366N N74F367N, N74F368N
Plastic SO-16	N74F365D, N74F366D N74F367D, N74F368D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE, 'F365, 'F366

INPUTS			OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I	Y_n	$\overline{Y}_n$
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

FUNCTION TABLE, 'F367, 'F368

INPUTS		OUTPUTS	
$\overline{OE}_n$	I	Y_n	$\overline{Y}_n$
L	L	L	H
L	H	H	L
H	X	(Z)	(Z)

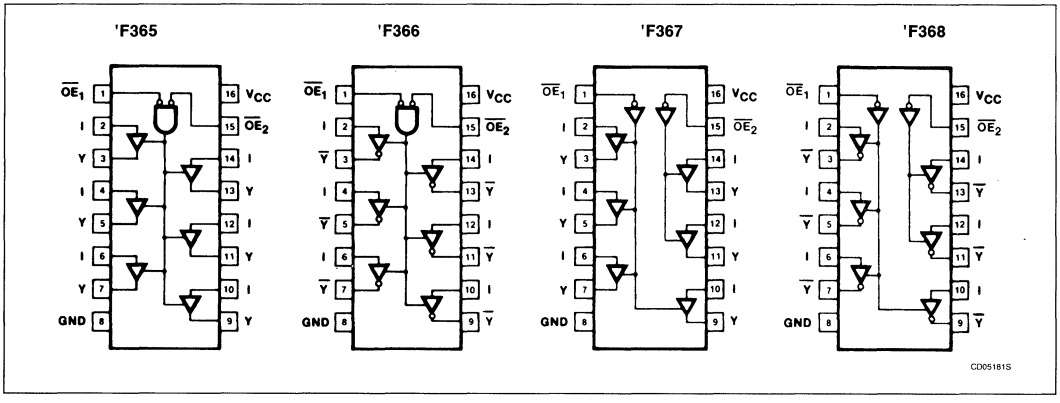
L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

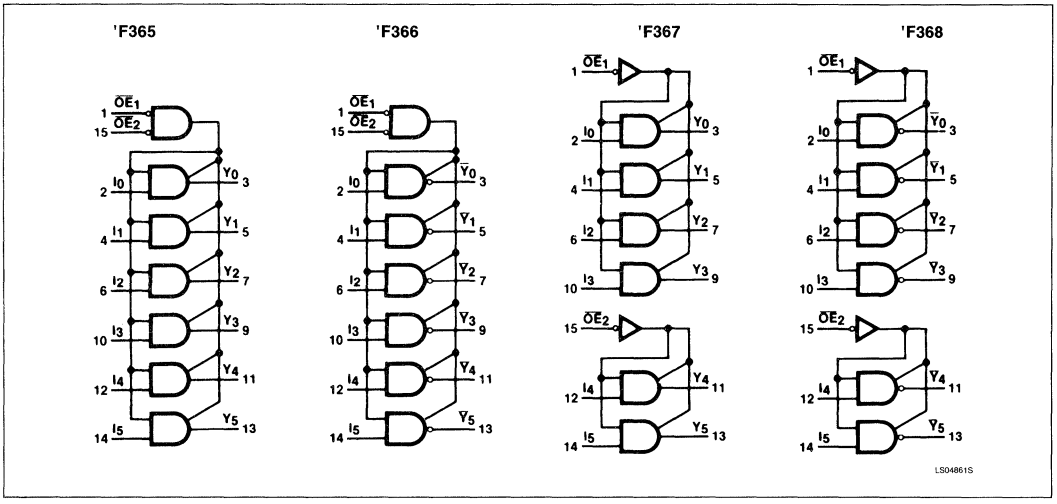
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	3-State output enable input (active LOW)	1.0/0.033	20μA/20μA
$I_0 - I_5$	Inputs	1.0/0.033	20μA/20μA
$Y_0 - Y_5$, $\overline{Y}_0 - \overline{Y}_5$	Outputs	750/106.6	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

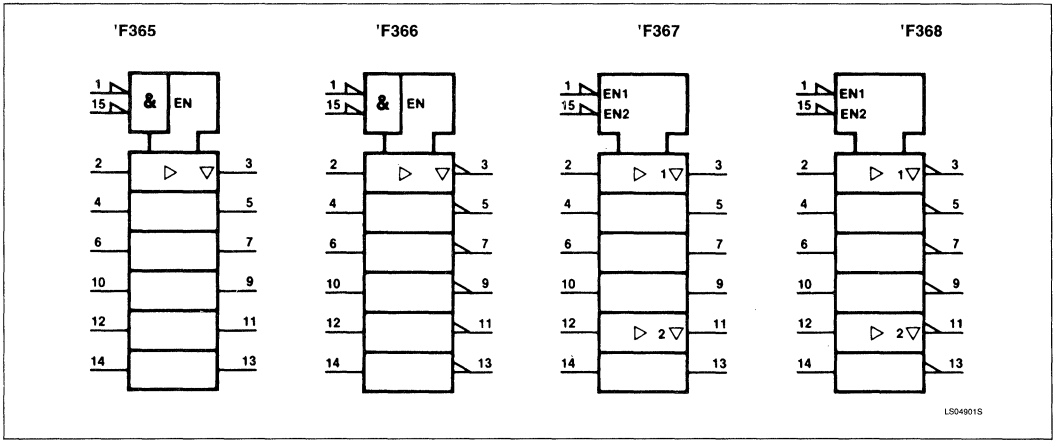
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F365, 'F366 'F367, 'F368			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−1	−20	μA
I_{OZH}	Off-state current HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V				2	50	μA
I_{OZL}	Off-state current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F365, 'F367	I_{CCH}	V_{CC} = MAX			25	35	mA
			I_{CCL}				47	62	mA
			I_{CCZ}				35	48	mA
		'F366, 'F368	I_{CCH}				18	25	mA
			I_{CCL}				47	62	mA
			I_{CCZ}				35	48	mA

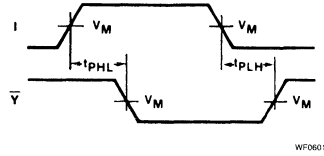
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

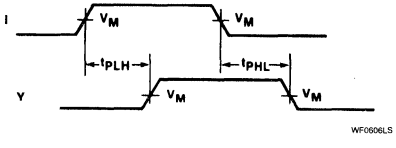
PARAMETER			TEST CONDITIONS	74F365, 'F366, 'F367, 'F368					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	'F366, 'F368	Waveform 1	3.0 2.0	5.0 3.0	6.5 5.0	3.0 1.5	7.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	'F365, 'F367	Waveform 2	3.0 3.0	4.5 5.5	6.5 7.0	3.0 3.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	'F365, 'F366	Waveform 3 & 4	4.0 4.0	6.5 6.0	9.5 9.0	4.0 4.0	10.0 9.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	'F367, 'F368	Waveform 3 & 4	3.0 3.0	5.5 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 3 & 4	2.5 2.5	4.5 4.0	6.5 6.0	2.5 2.0	7.0 6.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

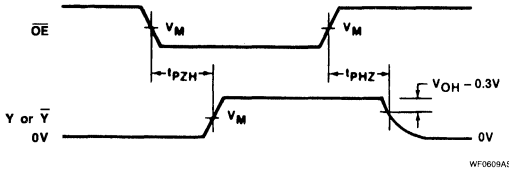
AC WAVEFORMS



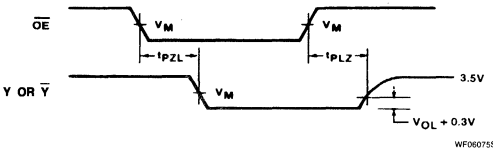
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



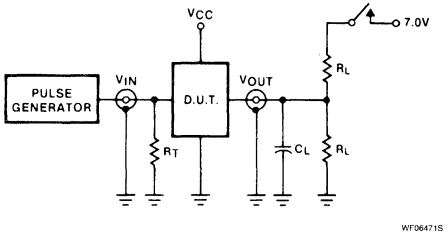
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



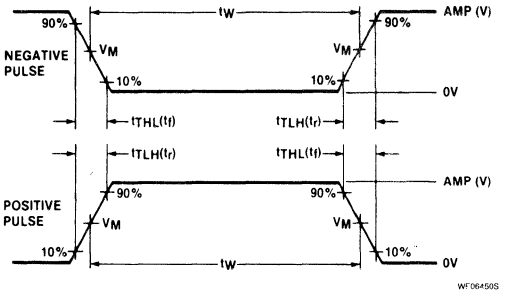
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

Signetics

FAST 74F373, 74F374
Latches/Flip-Flops

'F373 Octal Transparent Latch (3-State)
'F374 Octal D Flip-Flop (3-State)
Product Specification

Logic Products

FEATURES

- **8-bit transparent latch – 'F373**
- **8-bit positive, edge-triggered register – 'F374**
- **3-State output buffers**
- **Common 3-State output enable**
- **Independent register and 3-state buffer operation**

DESCRIPTION

The 'F373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data that is present one set-up time before the HIGH-to-LOW enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F373	4.5ns	35mA
74F374	6.5ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F373N, N74F374N
Plastic SOL-20	N74F373D, N74F374D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

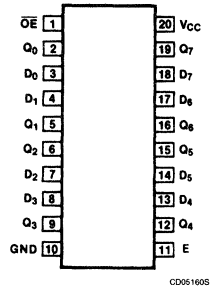
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/1.0	20μA/0.6mA
E ('F373)	Latch enable input (active HIGH)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
CP ('F374)	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	3-State outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

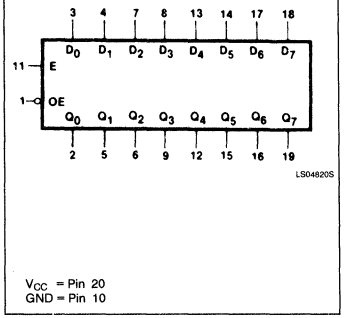
PIN CONFIGURATION

'F373



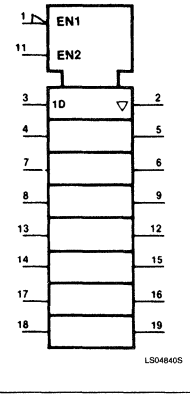
LOGIC SYMBOL

'F373



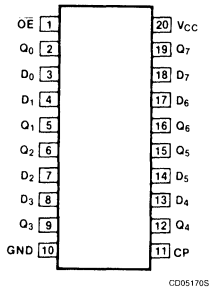
LOGIC SYMBOL (IEEE/IEC)

'F373



PIN CONFIGURATION

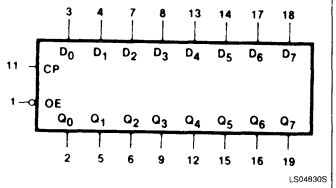
'F374



CD05170S

LOGIC SYMBOL

'F374

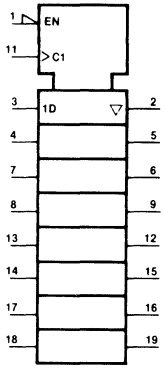


LS04830S

V_{CC} = Pin 20
GND = Pin 10

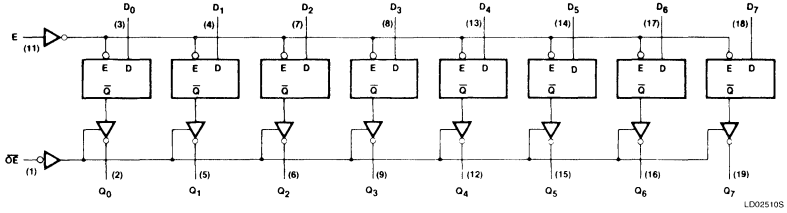
LOGIC SYMBOL (IEEE/IEC)

'F374



LS04850S

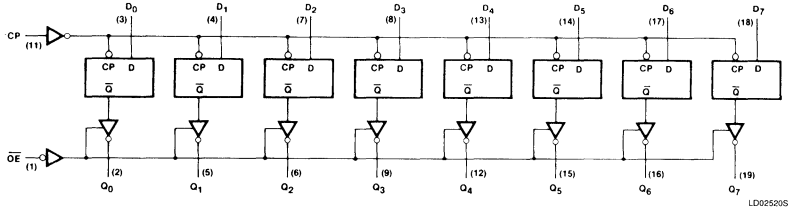
LOGIC DIAGRAM, 'F373



LD02510S

V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 'F374



LD02520S

V_{CC} = Pin 20
GND = Pin 10

When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

The 'F374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT — FUNCTION TABLE, 'F373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$Q_0 - Q_7$
Enable and read register	L L	H H	X X	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	X X	X X	X X	(Z) (Z)

MODE SELECT — FUNCTION TABLE, 'F374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$Q_0 - Q_7$
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	X X	X X	X X	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW E transition
L = LOW voltage level
X = Don't care
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW E transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F373, 'F374			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,		±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH}=MIN,		±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V			-60		-150	mA
I_{CC}	Supply current (total)	'F373	V_{CC} = MAX	I_{CCZ}	$\overline{OE}$ = 4.5V, D inputs = E = GND		35	55	mA
		'F374		I_{CCZ}	CP = $\overline{OE}$ = 4.5V, D inputs = GND		57	86	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

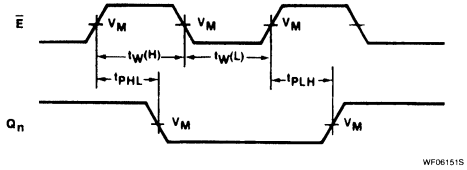
PARAMETER			TEST CONDITIONS	74F373, 'F374					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	'F374	Waveform 6	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay E to Q_n	'F373	Waveform 1	3.0 2.0	9.0 4.0	11.5 7.0	5.0 3.0	13.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F373	Waveform 4	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	'F374	Waveform 6	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH}	Output enable time to HIGH level	'F373 'F374	Waveform 2	2.0 2.0	5.0 9.0	11.0 11.5	2.0 2.0	12.0 12.5	ns
t_{PZL}	Output enable time to LOW level	'F373 'F374	Waveform 3	2.0 2.0	5.6 5.3	7.5 7.5	2.0 2.0	8.5 8.5	ns
t_{PHZ}	Output disable time from HIGH level	'F373 'F374	Waveform 2	2.0 2.0	4.5 5.3	6.5 7.0	2.0 2.0	7.5 8.0	ns
t_{PLZ}	Output disable time from LOW level	'F373 'F374	Waveform 3	2.0 2.0	3.8 4.3	5.0 5.5	2.0 2.0	6.0 6.5	ns

AC SET-UP REQUIREMENTS

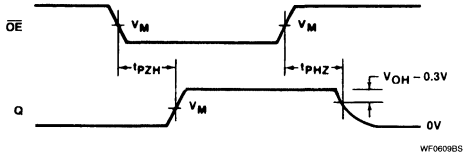
PARAMETER			TEST CONDITIONS	74F373, 'F374					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to E	'F373	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to E	'F373	Waveform 5	3.0 3.0			3.0 3.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width	'F374	Waveform 6	7.0 6.0			7.0 6.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	'F374	Waveform 7	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	'F374	Waveform 7	2.0 2.0			2.0 2.0		ns
$t_W(H)$	Latch enable pulse width	'F373	Waveform 1	6.0			6.0		ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

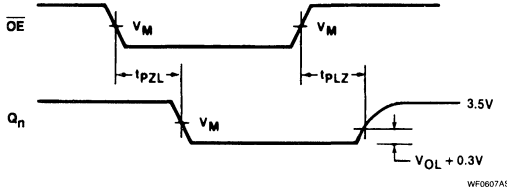
AC WAVEFORMS



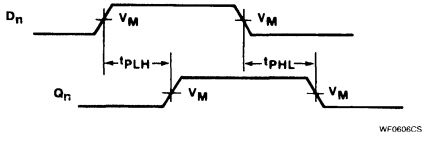
Waveform 1. Latch Enable To Output Delays And Latch Enable Pulse Width



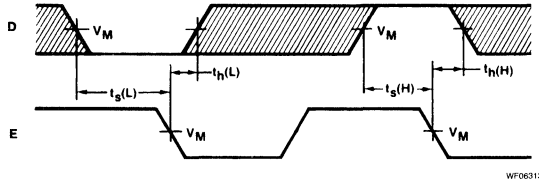
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



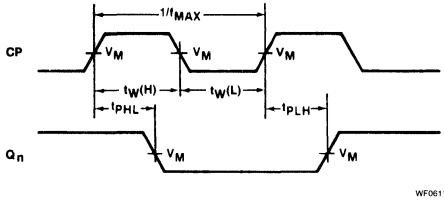
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



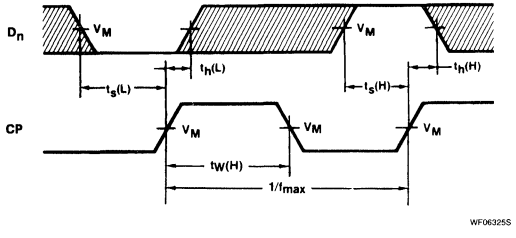
Waveform 4. Propagation Delay Data To Q Outputs



Waveform 5. Data Set-up And Hold Times



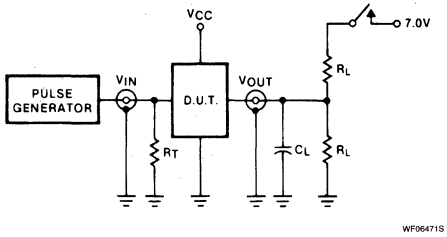
Waveform 6. Clock To Output Delays And Pulse Width



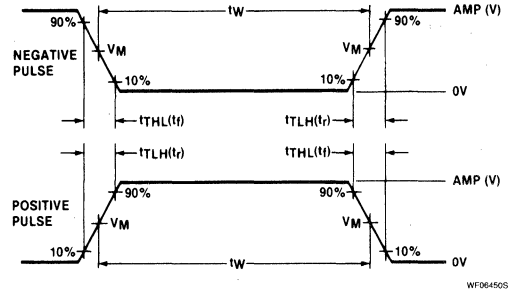
Waveform 7. Data Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F377
Flip-Flop

Octal D Flip-Flop With Enable
Product Specification

Logic Products

FEATURES

- **High impedance NPN Base Inputs for reduced loading (20μA in HIGH and LOW states)**
- **Ideal for addressable register applications**
- **Enable for address and data synchronization applications**
- **Eight edge-triggered D flip-flops**
- **Buffered common clock**
- **See 'F273 for Master Reset version**
- **See 'F373 for transparent latch version**
- **See 'F374 for 3-State version**

DESCRIPTION

The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Enable ($\overline{E}$) is LOW.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F377	120MHz	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F377N
Plastic SOL-20	N74F377D

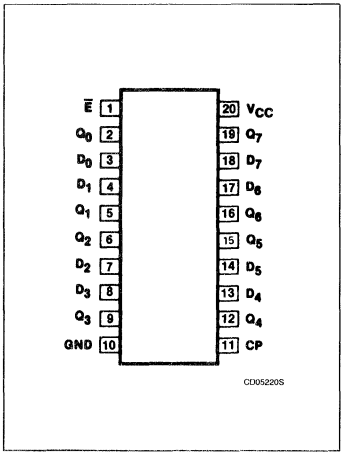
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

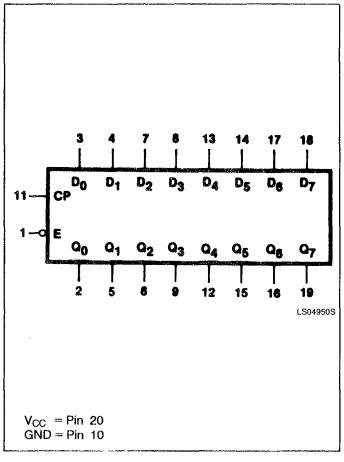
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/1.0	20μA/20μA
CP	Clock input (active rising edge)	1.0/1.0	20μA/20μA
$\overline{E}$	Enable input (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Data outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

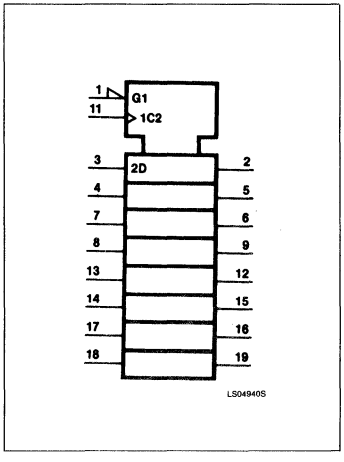
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

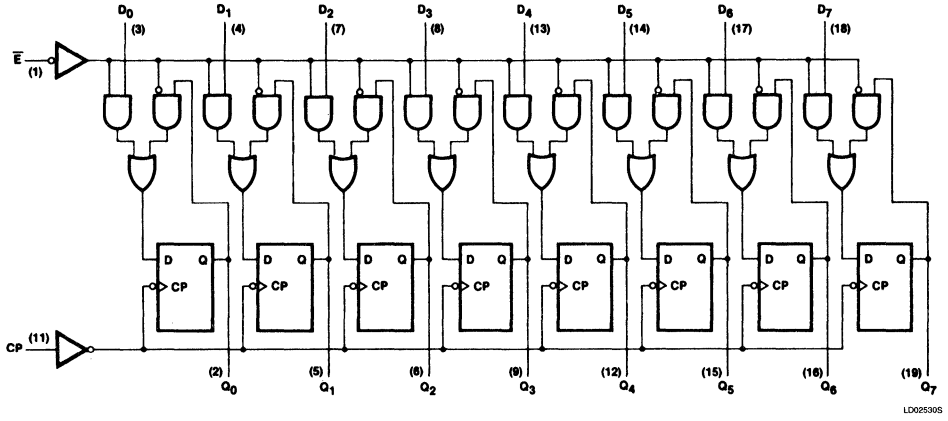


MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{E}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H= HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
X= Don't care.
↑= LOW-to-HIGH clock transition.

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F377			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$\overline{MR}$ & CP inputs[3]	V_{CC} = MIN, V_{IL} = 0.0V, V_{IH} = 4.5V, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
		other inputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−1	−20	mA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	D_n = 4.5V, CP = ↑, $\overline{E}$ = GND		55	72	mA
		I_{CCL}		D_n = $\overline{E}$ = GND, CP = ↑		70	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

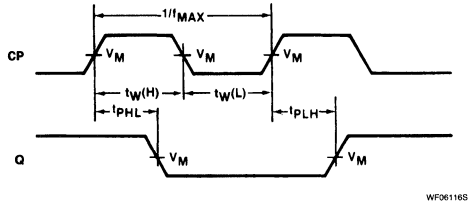
PARAMETER		TEST CONDITIONS	74F377					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	120		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	10.0 10.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO packages.

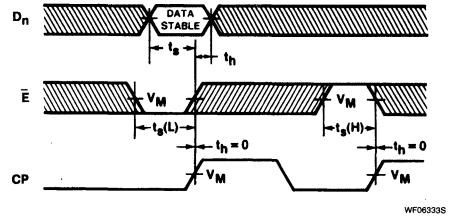
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F377					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	Waveform 2	2.0 2.0			2.5 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 2	0 0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{E}$ to CP	Waveform 2	2.5 3.0			2.5 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, HIGH or LOW	Waveform 1	4.0 4.0			5.0 5.0		ns

AC WAVEFORMS



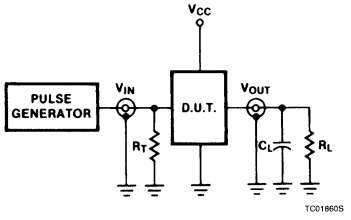
Waveform 1. Clock To Output Delays And Clock Pulse Width



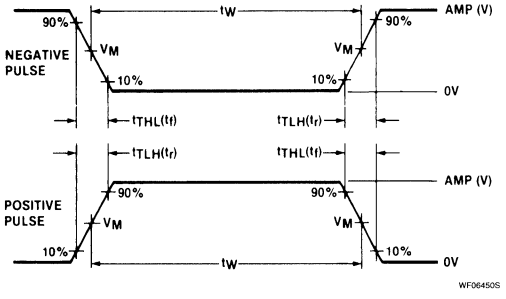
Waveform 2. Data And Clock Enable Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

FAST 74F378
Flip-Flop

Hex D Flip-Flop With Enable
Product Specification

Logic Products

FEATURES

- **6-bit high-speed parallel register**
- **Positive edge-triggered D-type inputs**
- **Fully buffered common clock and enable inputs**
- **Input clamp diodes limit high speed termination effects**
- **Fully TTL and CMOS compatible**

DESCRIPTION

The '74F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) is LOW.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F378	100MHz	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F378N
Plastic SO-16	N74F378D

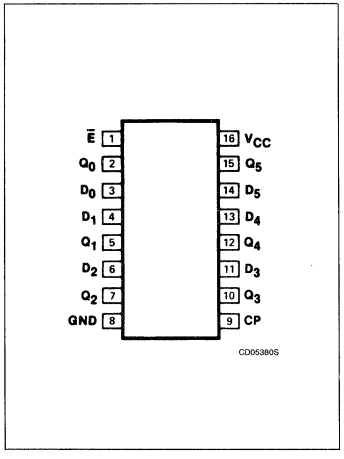
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

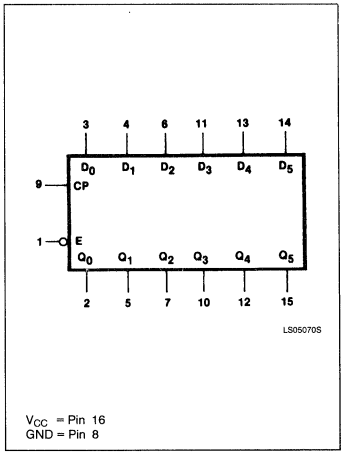
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_5$	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{E}$	Enable input (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_5$	Data outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

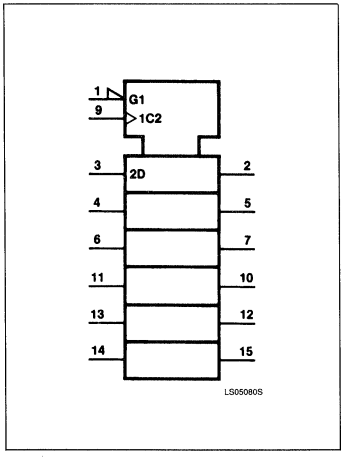
PIN CONFIGURATION



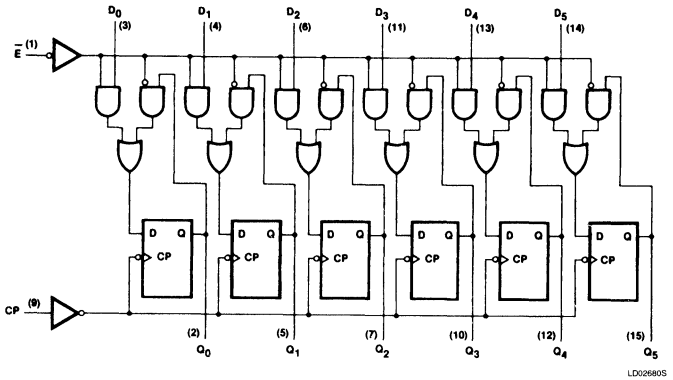
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\bar{E}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F378			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			32	45	mA
		I_{CCL}				35	45	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequences of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

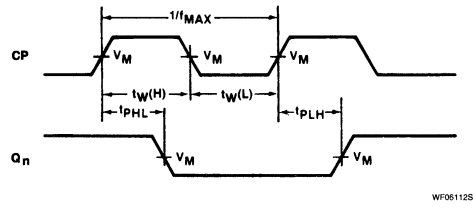
PARAMETER		TEST CONDITIONS	74F378					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	8.5 9.5	ns ns

NOTE: Subtract 0.2ns from minimum values for SO package.

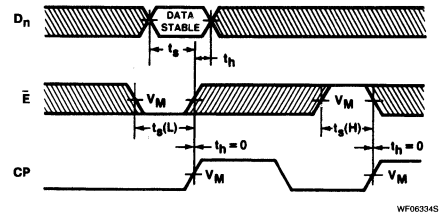
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F378					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{E}$ to CP	Waveform 2	4.0 10.0			4.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width HIGH or LOW	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



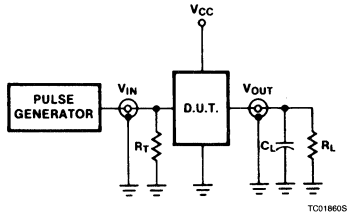
Waveform 1. Clock To Output Delays, Clock Pulse Width, And Maximum Clock Frequency



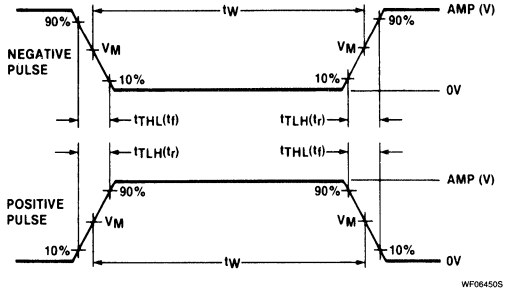
Waveform 2. Data And Enable Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F379
Quad Register

Quad Parallel Register (with Enable)
Product Specification

Logic Products

FEATURES

- **Edge-triggered D-type inputs**
- **Buffered positive edge-triggered clock**
- **Buffered common enable input**
- **True and complementary outputs**

DESCRIPTION

The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F379	120MHz	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F379N
Plastic SO-16	N74F379D

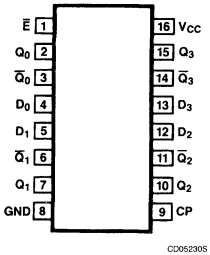
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

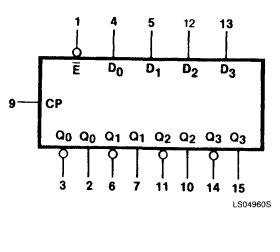
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{E}$	Enable input (active low)	1.0/1.0	20μA/0.6mA
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{Q}_0 - \overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

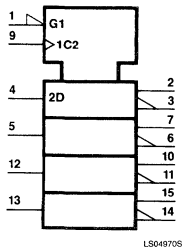


LOGIC SYMBOL



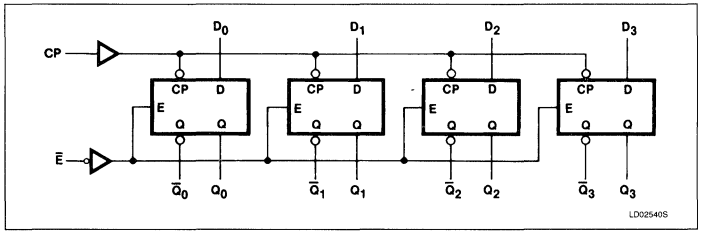
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



Quad Register | FAST 74F379

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	↑	X	NC	NC
L	↑	h	H	L
L	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
NC = No Change

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F379 Min	74F379 Typ[2]	74F379 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, D_n = $\overline{MR}$ = 4.5V, CP = ↑			28	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

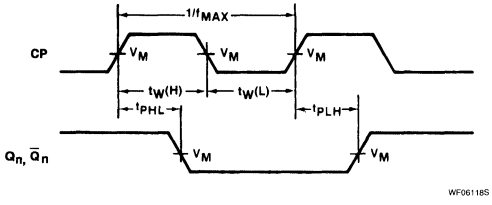
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F379 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F379 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	3.5 4.5	5.0 6.5	7.0 8.5	3.5 4.5	8.0 9.5	ns

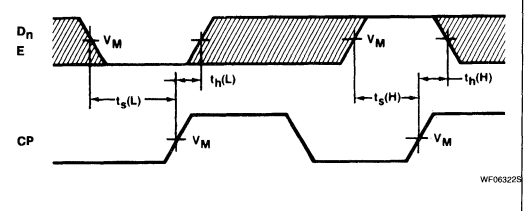
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F379 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F379 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{E}$ to CP	Waveform 2	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW	Waveform 1	4.0 5.0			4.0 5.0		ns

AC WAVEFORMS



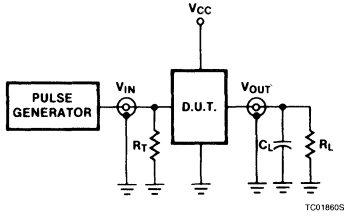
Waveform 1. Clock To Output Delays And Clock Pulse Width



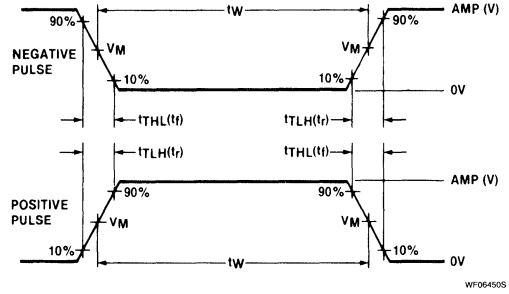
Waveform 2. Data Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F381
Arithmetic Logic Unit

4-Bit Arithmetic Logic Unit
Product Specification

Logic Products

FEATURES

- **Low input loading minimizes drive requirements**
- **Performs six arithmetic and logic functions**
- **Selectable LOW (clear) and HIGH (preset) functions**
- **Carry Generate and Propagate outputs for use with carry lookahead generator**

DESCRIPTION

The 'F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select ($S_0 - S_2$) input codes force the Function outputs LOW or HIGH. Carry Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are provided for use with the 'F182 Carry Lookahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F381	6.4ns	59mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F381N
Plastic SOL-20	N74F381D

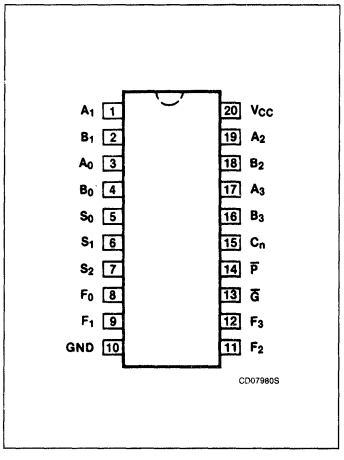
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

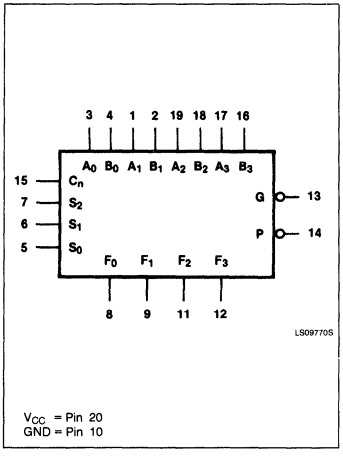
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	A operand inputs	1.0/4.0	20μA/0.6mA
$B_0 - B_3$	B operand inputs	1.0/4.0	20μA/0.6mA
$S_0 - S_2$	Function select inputs	1.0/1.0	20μA/0.6mA
C_n	Carry input	1.0/4.0	20μA/0.6mA
$\overline{G}$	Carry generate output (active LOW)	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output (active LOW)	50/33	1.0mA/20mA
$F_0 - F_3$	Function Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

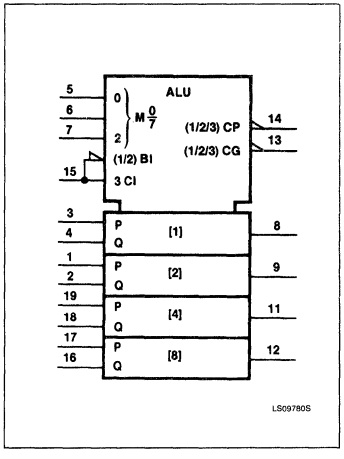
PIN CONFIGURATION



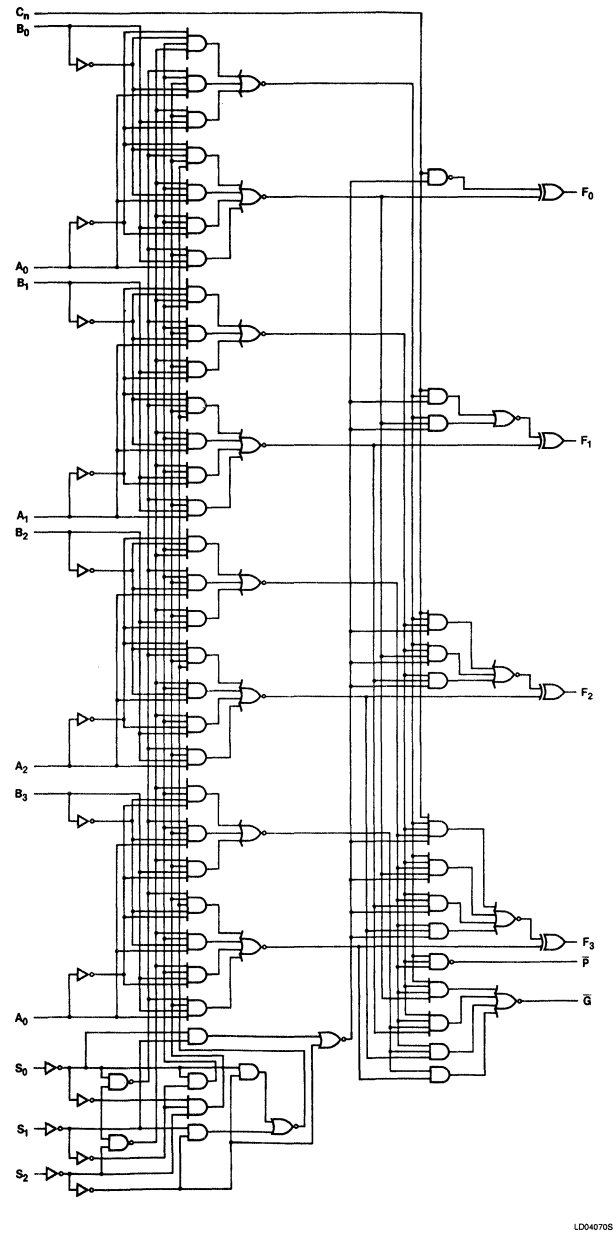
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Signals applied to the Select inputs $S_0 - S_2$ determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output Function levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-HIGH or active-LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active-HIGH operands, LOW for active-LOW operands) into the C_n input of the least significant package.

The Carry Generate ($\overline{G}$) and Carry Propagate ($\overline{P}$) outputs supply input signals to the 'F182 carry lookahead generator for expansion to longer word length, as shown in Figure 1. Note that an 'F382 ALU is used for the most significant package. Typical delays for Figure 1 are given in Table 1.

FUNCTION SELECT TABLE

SELECT			OPERATION
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A ⊕ B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH voltage level
L = LOW voltage level

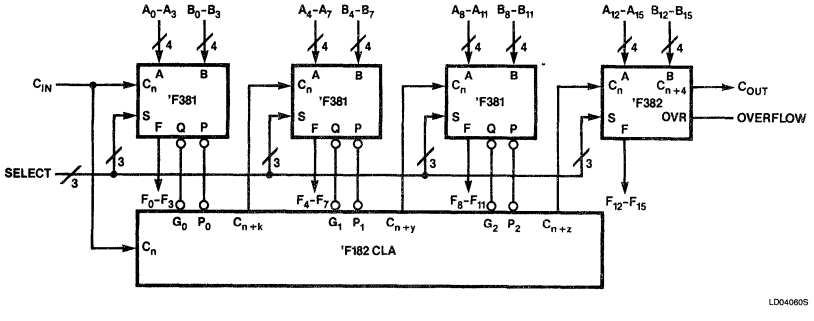


Figure 1. 16-Bit Look-Ahead Carry ALU Expansion

Table 1. 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to $\overline{P}$	7.2ns	7.2ns
$\overline{P}_i$ to C_{n+j} ('F182)	6.2ns	6.2ns
C_n to F	8.1ns	—
C_n to C_{n+4}, OVR	—	8.0ns
Total delay	21.5ns	21.4ns

FUNCTION TABLE

	INPUTS						OUTPUTS					
Function	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
Clear	0	0	0	X	X	X	0	0	0	0	0	0
B Minus A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A Minus B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A Plus B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A ⊕ B	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
Preset	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

1 = HIGH voltage level
0 = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F381			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.50	5.0	5.50	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F381			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	$A_0 - A_3$, $B_0 - B_3$, C_n	V_{CC} = MAX, V_I = 0.5V				−2.4	mA
		S_0, S_1, S_2				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			59	89	mA

NOTES:

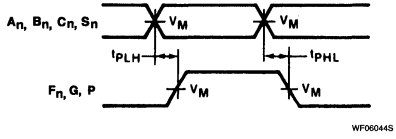
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F381					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.5	6.0	11.0	2.5	12.5	ns
t_{PHL}	C_n to F_n		2.5	4.5	6.5	2.5	7.5	ns
t_{PLH}	Propagation delay	Waveform 1	3.5	7.0	13.0	3.5	16.0	ns
t_{PHL}	Any A or B to any F		3.0	6.0	9.0	3.0	10.0	ns
t_{PLH}	Propagation delay	Waveform 1	5.0	9.0	13.0	5.0	16.0	ns
t_{PHL}	S_n to F_n		4.0	7.5	10.5	4.0	11.5	ns
t_{PLH}	Propagation delay	Waveform 1	3.5	6.5	9.0	3.5	10.0	ns
t_{PHL}	A_n or B_n to $\overline{G}$		3.0	6.0	8.5	3.0	9.0	ns
t_{PLH}	Propagation delay	Waveform 1	3.0	5.5	8.0	3.0	9.0	ns
t_{PHL}	A_n or B_n to $\overline{P}$		3.5	6.0	8.5	3.5	9.0	ns
t_{PLH}	Propagation delay	Waveform 1	5.0	7.5	11.0	5.0	12.5	ns
t_{PHL}	S_n to $\overline{G}$ or $\overline{P}$		5.5	8.5	12.5	5.0	14.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

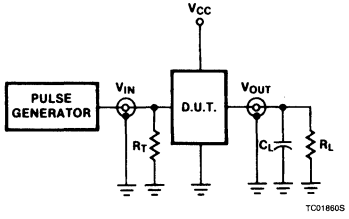
AC WAVEFORM



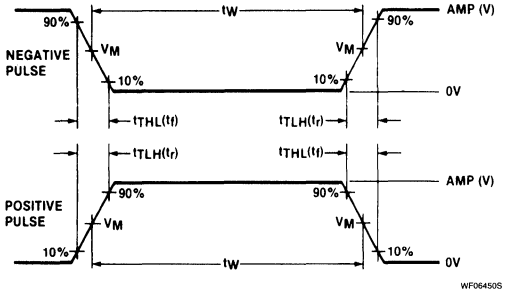
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay For Carry Input (C_n) To Function Output (F_n) A Or B Operand Input (A_n Or B_n) To Function Outputs (F_n) Function Select Inputs (S_n) To Function Outputs (F_n) A Or B Operand Input (A_n Or B_n) To Carry Generate (G) And Propagate (P) Output Function Select Inputs (S_n) To Carry Generate (G) And Propagate ($\overline{P}$) Output.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

FAST 74F382
Arithmetic Logic Unit (ALU)

4-Bit Arithmetic Logic Unit
Product Specification

Logic Products

FEATURES

- **Performs six arithmetic logic functions**
- **Selectable LOW (clear) and HIGH (preset) functions**
- **Low input loading minimizes drive requirements**
- **Carry output for ripple expansion**
- **Overflow output for Two's Complement Arithmetic**

DESCRIPTION

The 'F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select ($S_0 - S_2$) input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in two's complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a carry lookahead generator, refer to the 'F381 data sheet.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F382	7.0ns	54mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F382N
Plastic SOL-20	N74F382D

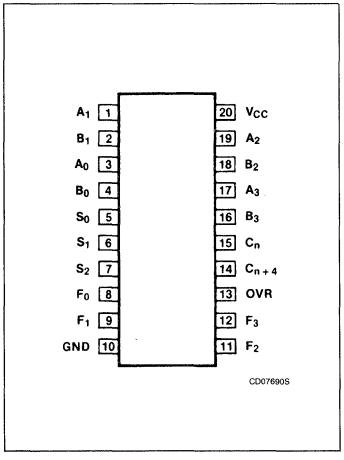
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

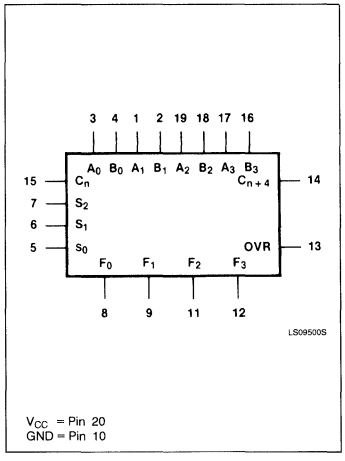
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	A operand inputs	1.0/4.0	20μA/2.4mA
$B_0 - B_3$	B operand inputs	1.0/4.0	20μA/2.4mA
$S_0 - S_2$	Function select inputs	1.0/4.0	20μA/0.6mA
C_n	Carry input	1.0/5.0	20μA/3mA
C_n	Carry output	50/33.3	1mA/20mA
OVR	Overflow output	50/33.3	1mA/20mA
$F_0 - F_3$	Outputs	50/33.3	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

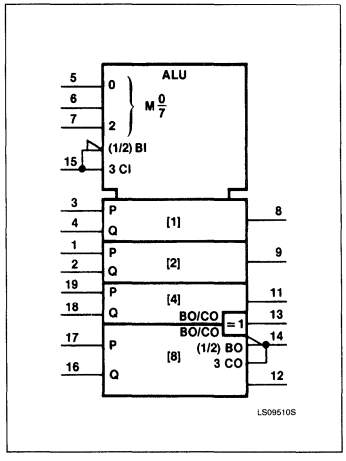
PIN CONFIGURATION



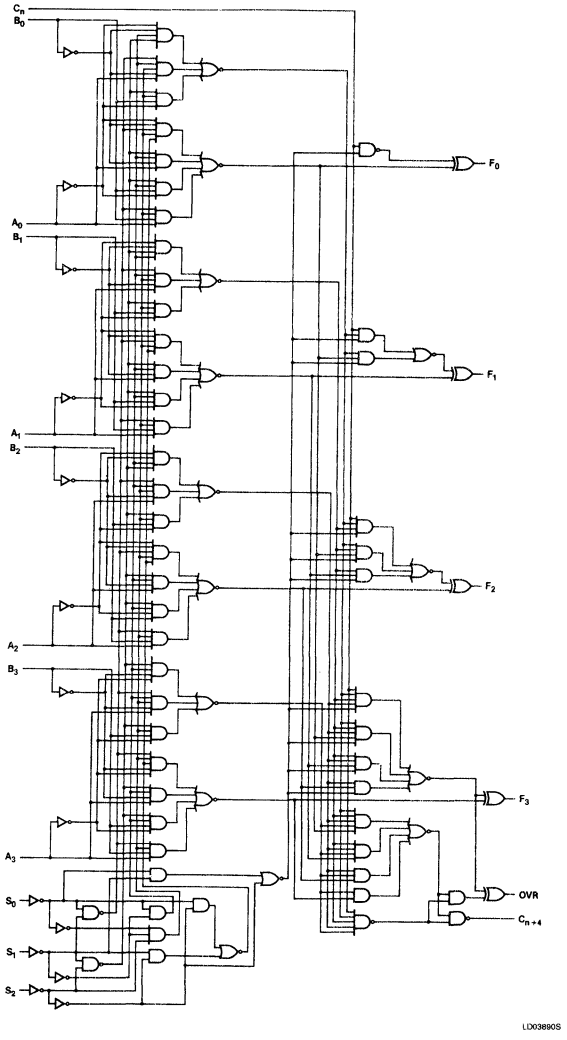
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



Functional Description

Signals applied to the Select inputs S0 – S2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands, LOW for active LOW operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a HIGH signal on OVR indicates overflow in two's complement operation. Typical delays for Figure 1 are given in Table 1.

FUNCTION SELECT TABLE

SELECT			OPERATION
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level
L = LOW Voltage Level

Table 1. 16 Bit-Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to C_{n+4}	6.5 ns	6.5 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to F	8.1 ns	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

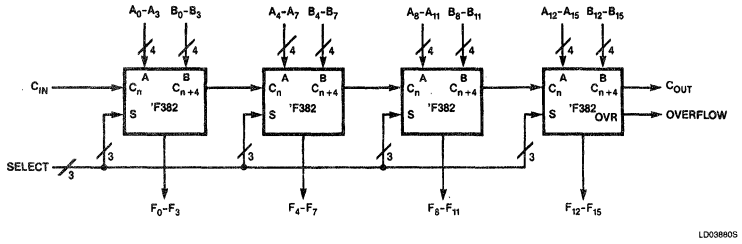


Figure 1. 16-Bit Ripple Carry ALU Expansion

FUNCTION TABLE

FUNCTION	INPUTS						OUTPUTS					
	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	OVR	C_{n+4}
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1
				1	X	X	0	0	0	0	1	1
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	1
				0	1	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	1	0	1
				1	1	0	1	0	0	0	0	0
				1	1	1	0	0	0	0	0	1
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	0
				0	1	0	0	1	1	1	0	1
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	0	0	0	0	0
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	0	1
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	1	1	1	0	1
				1	0	0	1	0	0	0	0	0
				1	0	1	0	0	0	0	0	1
				1	1	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	0	1
A ⊕ B	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				X	1	1	0	0	0	0	1	1
				1	1	0	1	1	1	1	1	1
A + B	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
AB	0	1	1	X	0	0	0	0	0	0	1	1
				X	0	1	0	0	0	0	0	0
				X	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
PRESET	1	1	1	X	0	0	1	1	1	1	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1

1 = HIGH Voltage Level 0 = LOW Voltage Level X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F182			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F382 Min	74F382 Typ[2]	74F382 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	C_n	V_{CC} = MAX, V_I = 0.5V				−5.0	mA
		$A_0 - A_3$, $B_0 - B_3$					−2.4	mA
		S_0, S_1, S_2				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			54	81	mA

NOTES:

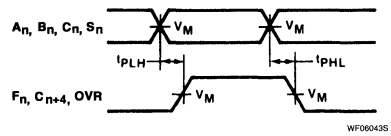
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying Fast Logic.")

PARAMETER		TEST CONDITIONS	74F382 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F382 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay	Waveform 1	3.0	7.0	12.0	2.5	13.5	ns
t_{PHL}	C_n to F_n		2.5	4.5	6.5	2.5	7.5	ns
t_{PLH}	Propagation delay	Waveform 1	3.5	8.0	13.5	3.5	17.0	ns
t_{PHL}	Any A or B to any F		3.0	6.0	10.0	2.5	11.0	ns
t_{PLH}	Propagation delay	Waveform 1	5.5	9.0	15.0	5.5	16.0	ns
t_{PHL}	S_i to F_i		5.5	7.5	10.5	5.5	12.0	ns
t_{PLH}	Propagation delay	Waveform 1	3.5	7.0	10.5	3.5	11.5	ns
t_{PHL}	A_i or B_i to C_{n+4}		3.5	6.5	9.5	3.5	10.5	ns
t_{PLH}	Propagation delay	Waveform 1	7.0	10.5	14.5	6.5	17.0	ns
t_{PHL}	S_i to OVR or C_{n+4}		5.0	8.0	11.0	5.0	12.0	ns
t_{PLH}	Propagation delay	Waveform 1	3.0	4.5	6.0	2.5	6.5	ns
t_{PHL}	C_n to C_{n+4}		3.5	5.0	6.5	3.5	7.0	ns
t_{PLH}	Propagation delay	Waveform 1	4.5	9.0	13.5	4.0	15.0	ns
t_{PHL}	C_n to OVR		3.0	5.0	6.5	3.0	7.0	ns
t_{PLH}	Propagation delay	Waveform 1	6.0	9.0	12.5	5.5	16.5	ns
t_{PHL}	A_i or B_i to OVR		3.5	6.5	9.0	3.5	10.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

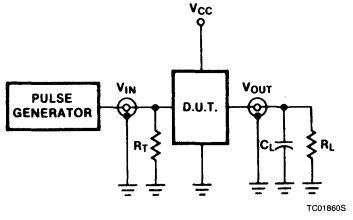
AC WAVEFORM



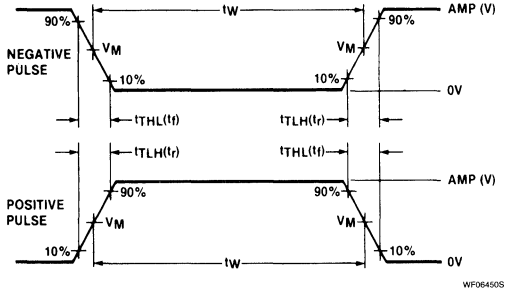
Waveform 1. Propagation Delay For Carry Input (C_n) To Function Output (F_n) A Or B Operand Input (A_n Or B_n) To Function Outputs (F_n) Function Select Inputs (S_n) To Overflow Output (OVR) Or Carry Output (C_{n+4}) A Or B Operand Input (A_n Or B_n) To Carry Output (C_{n+4}) And Overflow Output (OVR)

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F384
Multiplier

8-Bit Serial/Parallel Two's Complement Multiplier
Preliminary Specification

Logic Products

FEATURES

- **8-bit by 1-bit sequential logic element**
- **Multiplies two numbers represented in Two's Complement**
- **Parallel inputs accept and store an 8-bit multiplicand ($X_0 - X_7$)**
- **K input is used for expansion to longer words**
- **Mode Control (M) is used to establish the most significant device**
- **Asynchronous Parallel Load (PL) input clears the internal flip-flop to the start condition and enables the X latches to accept new multiplicand data**

DESCRIPTION

The 'F384 is an 8-bit sequential logic element that multiplies two numbers represented in two's complement notation. The device implements Booth's algorithm internally to produce a two's complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand ($X_0 - X_7$). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output, least significant bit first.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F384	100MHz	60mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F384N
Plastic SOL-16	N74F384D

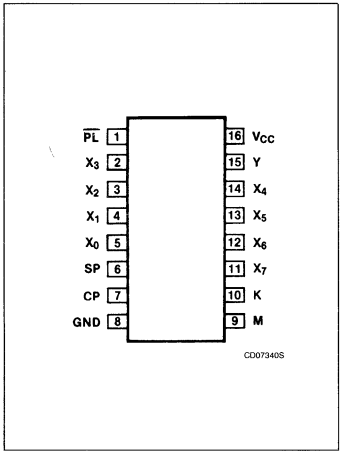
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

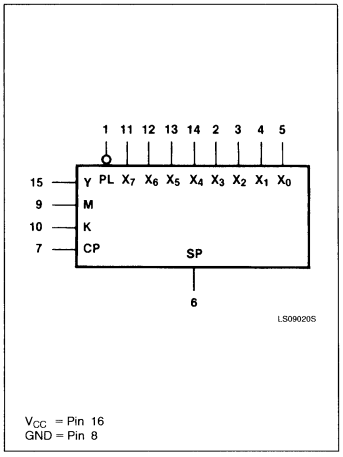
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$X_0 - X_7$	Multiplicand data inputs	1.0/1.0	20μA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
K	Serial expansion input	1.0/1.0	20μA/0.6mA
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous parallel load input	1.0/1.0	20μA/0.6mA
Y	Serial multiplier inputs	1.0/1.0	20μA/0.6mA
SP	Serial X.Y product output	50/33.3	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

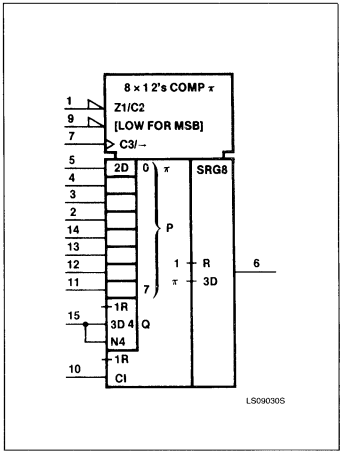
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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The K input is used for expansion to longer X words, using two or more 'F384 devices. The Mode Control (M) input is used to establish the most significant device. An asynchronous Parallel Load (PL) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

Referring to the Logic Diagram, the multiplicand ($X_0 - X_7$) latches are enabled to receive new data when $\overline{PL}$ is LOW. Data that meets the set-up time requirements is latched and stored when $\overline{PL}$ goes HIGH. The LOW signal on $\overline{PL}$ also clears the Y_{a-1} flip-flop as well as the carry-save flip-flops and the partial product register in the arithmetic section. Figure 1 is a conceptual logic diagram of a typical cell in the arithmetic section, except for the first (X_7) cell, in which K is the B_i input and M is incorporated into the carry logic. The cells use the carry-save technique to avoid the complexity and delays inherent in look-ahead carry schemes for longer words.

Figure 2 is a timing diagram for an 8 × 8 multiplication process. New multiplicand data enters the X latches during bit time T_0. It is assumed that $\overline{PL}$ goes LOW shortly after the CP rising edge that marks the beginning of T_0 and goes HIGH again shortly after the beginning of T_1. The LSB (Y_0) of the multiplier is applied to the Y input during T_1 and combines with X_0 in the least significant cell to form the appropriate D input (X_0Y_0) to the sum flip-flop. This is clocked into the sum flip-flop by the CP rising edge at the beginning of T_2 and this LSB (S_0) of the product is available shortly thereafter at the SP output of the package.

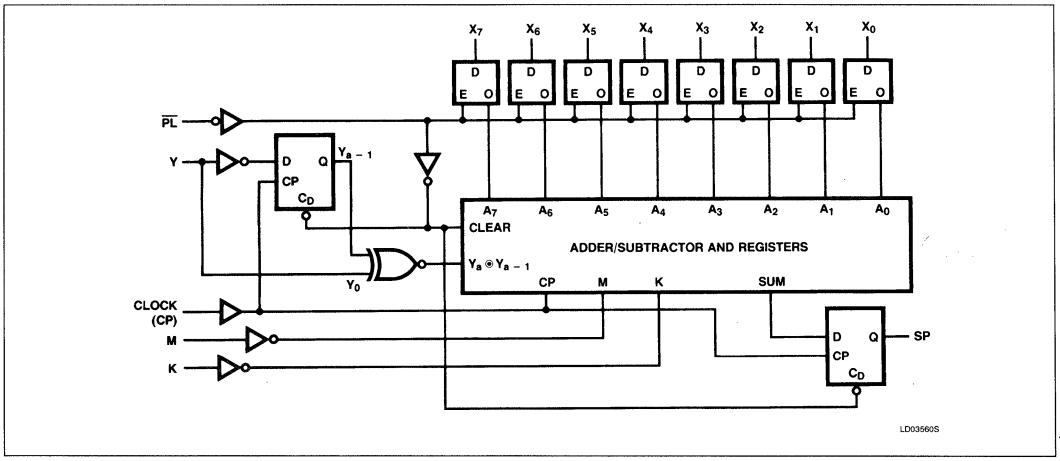
FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{PL}$	CP	K	M	X_1	Y	Y_{a-1}	SP	
X	X	L	L	X	X	X	X	Most significant multiplier device
X	X	CS	H	X	X	X	X	Device cascaded in multiplier string
L	X	X	X	OP	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	X	X	X	X	X	X	X	Device enabled
H	↑	X	X	X	L	L	AR	Shift sum register
H	↑	X	X	X	L	H	AR	Add multiplicand to sum register and shift
H	↑	X	X	X	H	L	AR	Subtract multiplicand from sum register and shift
H	↑	X	X	X	H	H	AR	Shift sum register

H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH Transition
CS = Connected to SP output of high order device
OP = X_1 latches open for new data (I = 0 – 7)
AR = Output as required per Booth's algorithm
X = Don't care

The next-least bit (Y_1) of the multiplier is also applied during T_2. The detailed logic design of the cell is such that during T_2 the D input to the sum flip-flop of the least significant cell contains not only X_0Y_1 but also, the X_1Y_0 product. Thus the term ($X_1Y_0 + X_0Y_1$) is formed at the D input of the least significant sum flip-flop during T_2 and this next-least term S_1 of the product is available at the SP output shortly after the CP rising edge at the beginning of T_3. Due to storage in the two preceding cells and in its own carry flip-flop, the D input to the least significant sum flip-flop during T_3 will contain the products X_2Y_0 and X_1Y_1 as well as X_0Y_2. During each succeeding bit time the SP output contains information formed one stage further upstream. For example, the SP output during T_9 contains X_7Y_0, which was actually formed during T_1.

LOGIC DIAGRAM



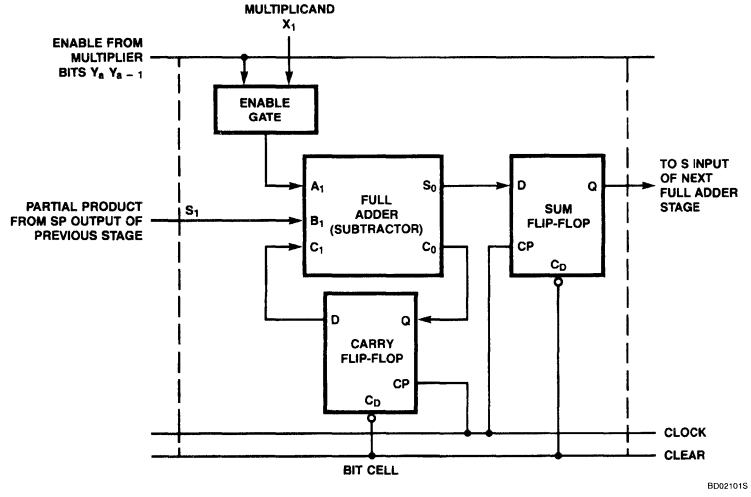


Figure 1. Conceptual Carry Save Adder Cell

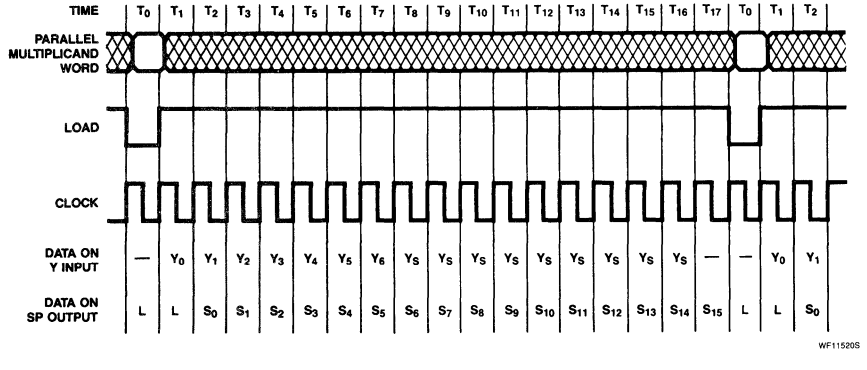


Figure 2. Timing Diagram Showing 18 Clock Cycle Operation of 8x8 Multiplication

The MSB Y_7 (the sign bit Y_S) of the multiplier is first applied to the Y input during T_8 and must also be applied during bit times T_9 through T_{16}. This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm and is a built-in feature of the 'F322 Shift Register. Figure 3 shows the method of using two 'F384s to perform a $12 \times n$ bit multiplication. Notice that the sign of X is effectively extended by connecting X_{11} to $X_4 - X_7$ of the most significant package. Whereas the 8×8 multiplication required 18 clock periods ($m + n$ to form the product terms plus T_0 to clear the multiplier plus T_{17} to recognize and store S_{15}), the arrangement of Figure 3 requires $12 + n$ bits to form the product terms plus the bit times to clear the multiplier and to recognize and store SP_{n+11}.

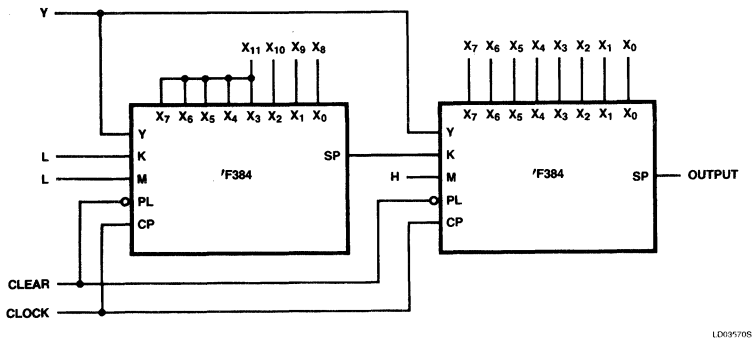


Figure 3. 12-Bit by n-Bit Two's Complement Multiplier

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F384			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			60	90	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F384					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to SP	Waveform 1	3.5 3.5	4.5 4.5	5.5 5.5	3.5 3.5	10.0 10.0	ns
t_{PHL}	Propagation delay $\overline{PL}$ to SP	Waveform 2	6.0	10.0	13.0	6.0	14.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

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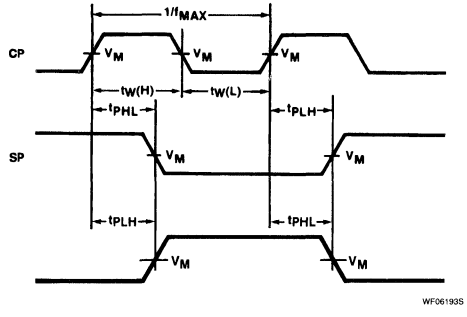
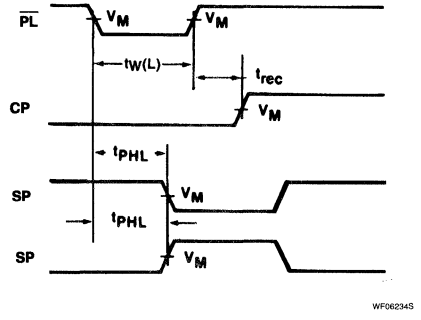
AC SET-UP REQUIREMENTS

PARAMETER	TEST CONDITIONS	74F384					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
$t_s(H)$ Set-up time, HIGH or LOW $t_s(L)$ K to CP	Waveform 3	13.5 13.5			15.0 15.0		ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ K to CP	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ Set-up time, HIGH or LOW $t_s(L)$ Y to CP	Waveform 3	15.0 15.0			15.0 15.0		ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ Y to CP	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ Set-up time, HIGH or LOW $t_s(L)$ X_n to $\overline{PL}$	Waveform 3	5.5 5.5			6.5 6.5		ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ X_n to $\overline{PL}$	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_w(H)$ CP pulse width $t_w(L)$ HIGH or LOW	Waveform 1	7.0 5.5			7.5 6.0		ns
$t_w(L)$ $\overline{PL}$ pulse width LOW	Waveform 2	6.5			7.0		ns
t_{rec} Recovery time $\overline{PL}$ to CP	Waveform 2	5.5			6.0		ns

AC WAVEFORMS



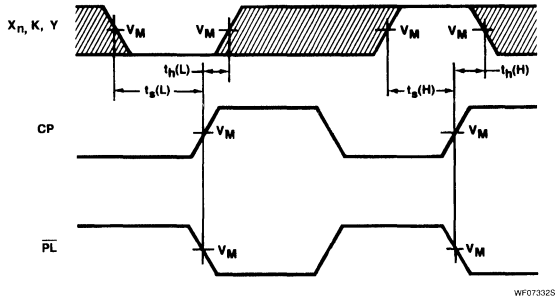
Waveform 1. Clock To Output Delays, Clock Pulse Width And Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master To Output Delay And Master Reset To Clock Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.

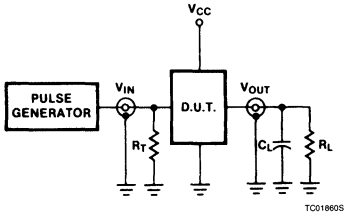
AC WAVEFORMS (Continued)



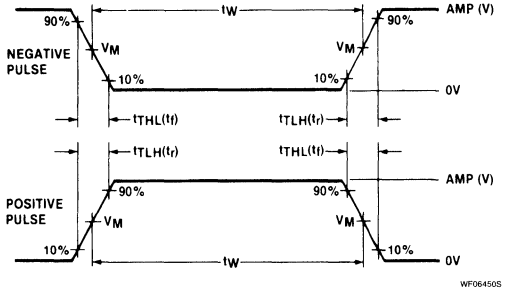
Waveform 3. Data And Select Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F385
Adder/Subtracter

Quad Serial Adder/Subtracter
Preliminary Specification

Logic Products

FEATURES

- **Four independent adder/ subtractors**
- **Two's complement arithmetic**
- **Synchronous operation**
- **Common Clear and Clock**
- **One's complement or magnitude-only capability**
- **'F385 is designed for use with 'F384 and 'F784 serial multipliers in implementing digital filters or butterfly networks in fast Fourier transforms**

DESCRIPTION

The 'F385 contains four serial adder/ subtractors with common Clock and Clear inputs, but independent Operand and Mode Select inputs. Each adder/ subtractor contains a sum flip-flop and a carry-save flip-flop for synchronous operations. Each circuit performs either A plus B or A minus B in two's complement notation, but can also be used for magnitude-only or one's complement operation. The 'F385 is designed for use with the 'F384 and 'F784 serial multipliers in implementing digital filters or butterfly networks in fast Fourier transforms.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F385	100MHz	68mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F385N
Plastic SOL-20	N74F385D

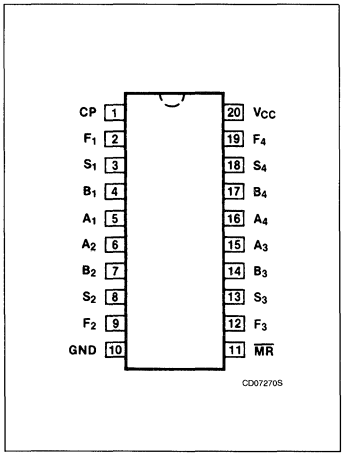
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

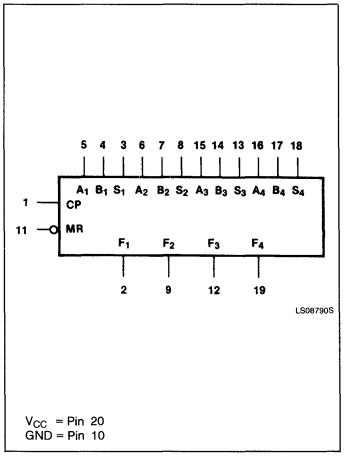
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_4$	A operand inputs	1.0/1.0	20μA/0.6mA
$B_1 - B_4$	B operand inputs	1.0/1.0	20μA/0.6mA
$S_1 - S_4$	Function select inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$F_1 - F_4$	Sum or difference outputs	50/33.3	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

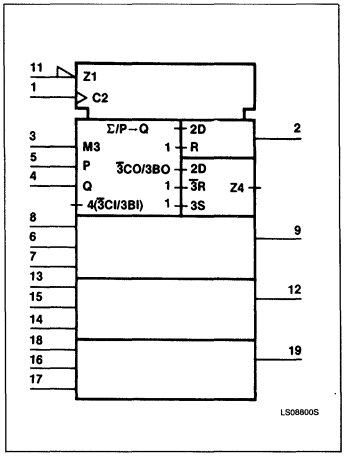
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Adder/Subtracter | FAST 74F385

Each adder contains two edge-triggered flip-flops to store the sum and carry, as shown in the Logic Diagram. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be LOW for the Add (A plus B) mode and HIGH for the Subtract (A minus B) mode. A LOW signal on the asynchronous Master Reset (MR) input clears the sum flip-flop and resets the carry flip-flop to zero in the Add more or presets it to one in the Subtract mode.

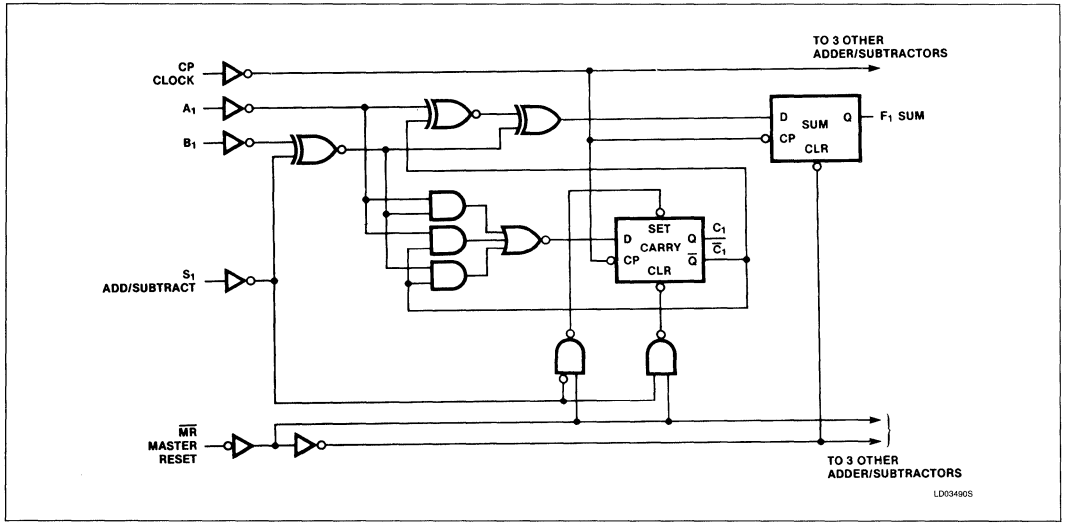
In the Subtract mode, the B operand is internally complemented. Presetting the carry flip-flop to one completes the two's complement transformation by adding one to "A plus B" during the first (LSB) operation after $\overline{MR}$ is released. For one's complement subtraction, the carry flip-flop can be set to zero by making S LOW during the reset, then making S HIGH after the reset but before the next clock.

TRUTH TABLE

INPUTS*				INTERNAL CARRY		OUTPUT*	FUNCTION
$\overline{MR}$	S	A	B	C	C_1	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = HIGH voltage level
L = LOW voltage level
X = Don't care
* = Inputs before CP transition, output after C
C_1 = Carry flip-flop state before (C) and after (C_1) Clock transition

LOGIC DIAGRAM (One Adder/Subtractor shown)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F384, 74F385			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	'F385	V_{CC} = MAX			68	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

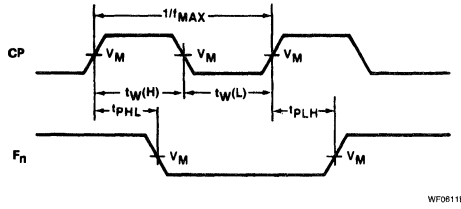
PARAMETER		TEST CONDITIONS	74F385					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	Waveform 1	70	100		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to F_n	Waveform 1	3.5 4.0	6.0 7.0	8.0 9.0	3.5 4.0	9.0 10	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to F_n	Waveform 2	5.5	9.0	12	5.5	13	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

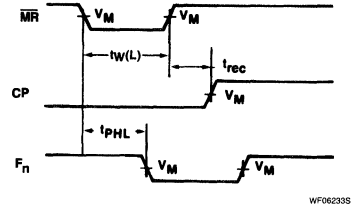
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F385					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW A_n to CP	Waveform 3	15 15			15 15		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW B_n or S_n to CP	Waveform 3	15 15			15 15		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW B_n or S_n to CP	Waveform 3	0 0			0 0		ns
$t_W(H)$ $t_W(L)$	CP pulse width, HIGH or LOW	Waveform 1	6.0 6.0			6.0 6.0		ns
$t_W(L)$	$\overline{MR}$ pulse width LOW	Waveform 2	6.0			6.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	8.5			9.5		ns

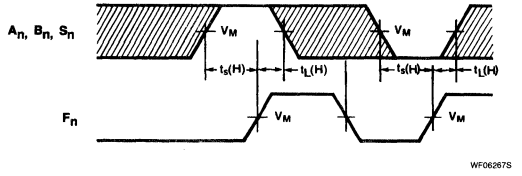
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



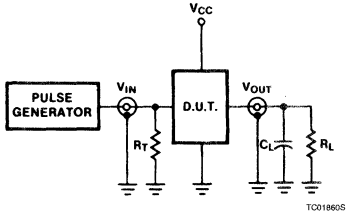
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



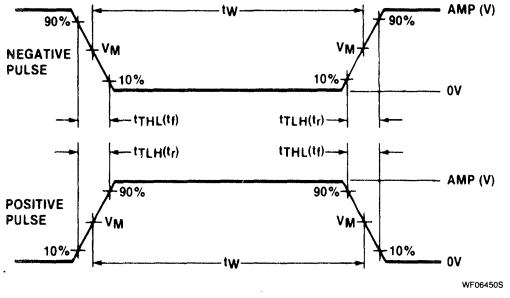
Waveform 3. Data Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F395
Shift Register

4-Bit Cascadable Shift Register (3-State)
Preliminary Specification

Logic Products

FEATURES

- **4-bit parallel load shift register**
- **Independent 3-State buffer outputs**
- **Separate Q_S output for serial expansion**
- **Asynchronous Master Reset**

DESCRIPTION

The 'F395 is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs ($D_0 - D_3$) into the register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one set-up prior to the HIGH-to-LOW transition of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F395	120MHz	32mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F395N
Plastic SO-16	N74F395D

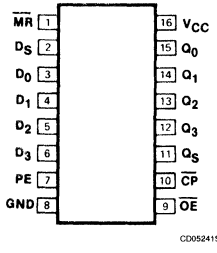
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

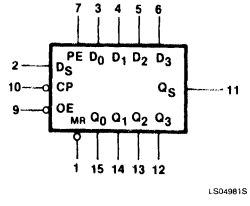
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
D_S	Serial data input	1.0/1.0	20μA/0.6mA
PE	Enable input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
Q_S	Serial expansion output	50/33	1.0mA/20mA
$Q_0 - Q_3$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

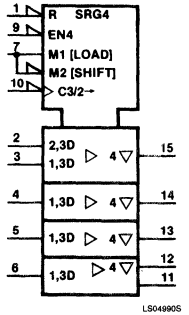


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)

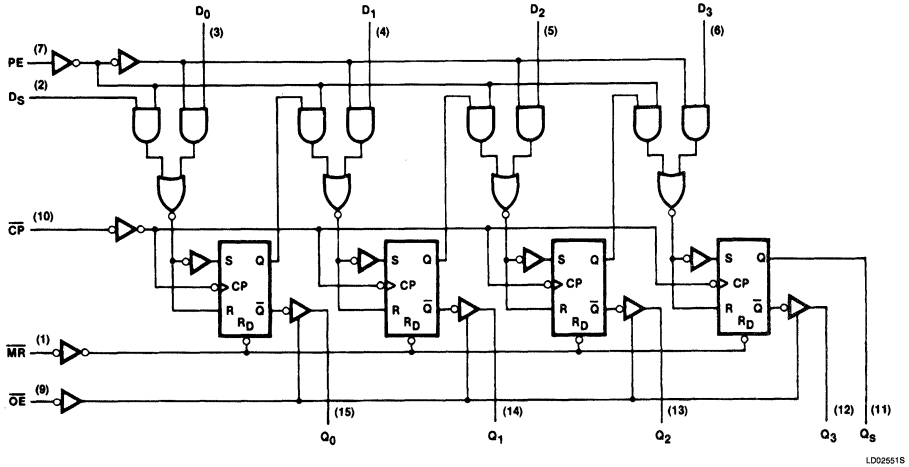


Shift Register | FAST 74F395

The Master Reset ($\overline{MR}$) is an asynchronous active-LOW input. When LOW, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, or large capacitive loads. The active-LOW Output Enable ($\overline{OE}$) controls all four 3-State buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is LOW. The outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus when $\overline{OE}$ is HIGH. The output from the last stage is brought out separately. This output (Q'_S is tied to the Serial Data input (D_S) of the next register for serial expansion applications. The Q'_3 output is not affected by the 3-State buffer operation.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS			
	$\overline{MR}$	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H	↓	l	l	X	L	q_0	q_1	q_2
	H	↓	l	h	X	H	q_0	q_1	q_2
Parallel load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	$\overline{OE}$	Q_n (Register)	Q_0, Q_1, Q_2, Q_3	Q_S
Read	L	L	L	L
	L	H	H	H
Disable buffers	H	L	(Z)	L
	H	H	(Z)	H

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition
L = LOW voltage level
l = LOW voltage voltage level one set-up time prior to the HIGH-to-LOW clock transition
q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW clock transition
X = Don't care
(Z) = HIGH impedance "off" state
↓ = HIGH-to-LOW transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Q_S			−1	mA
		$Q_0 - Q_3$			−3	mA
I_{OL}	LOW-level output current	Q_S			20	mA
		$Q_0 - Q_3$			24	mA
T_A	Operating free-air temperature		0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F395			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		$Q_0 - Q_3$		I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX		±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{OZH}	Off-state current HIGH level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					50	μA
I_{OZL}	Off-state current LOW level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{MR}$ = PE = D_n = D_s = 4.5V, $\overline{OE}$ = GND, $\overline{CP}$ = ↓			33	48	mA
		I_{CCL}		PE = 4.5V, $\overline{MR}$ = $\overline{OE}$ = D_n = D_s = GND, $\overline{CP}$ = ↓			35	50	mA
		I_{CCZ}		$\overline{OE}$ = 4.5V, $\overline{MR}$ = D_n = D_s = GND			32	46	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

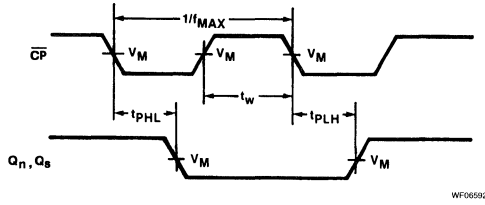
PARAMETER		TEST CONDITIONS	74F395					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	120		95		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n	Waveform 1	3.5 5.0	6.0 8.0	8.5 11.0	3.5 5.0	9.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_s	Waveform 1	5.0 5.5	6.5 7.0	9.0 9.5	4.5 5.0	10.0 10.0	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q_n	Waveform 2	5.0	7.5	10.0	5.0	10.5	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q_s	Waveform 2	4.5	6.5	8.5	4.5	9.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	Waveform 3 Waveform 4	4.0 3.5	6.5 6.0	9.0 8.0	4.0 3.5	10.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW	Waveform 3 Waveform 4	1.0 1.0	2.5 3.5	4.5 5.5	1.0 1.0	5.5 6.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

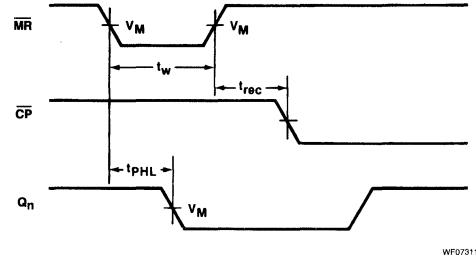
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F395					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to $\overline{CP}$	Waveform 5	1.0 1.0			1.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{CP}$	Waveform 5	1.0 1.5			1.0 1.5		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW PE to $\overline{CP}$	Waveform 5	6.5 4.0			7.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW PE to $\overline{CP}$	Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ pulse width, HIGH or LOW	Waveform 1	5.0 4.0			5.5 4.5		ns
$t_w(L)$	$\overline{MR}$ pulse width LOW	Waveform 2	2.5			3.0		ns
t_{rec}	Recovery time $\overline{MR}$ to $\overline{CP}$	Waveform 2	6.0			7.0		ns

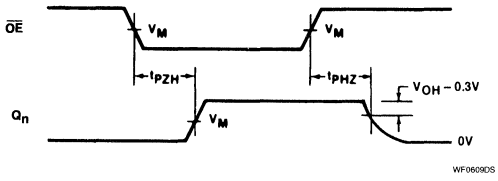
AC WAVEFORMS



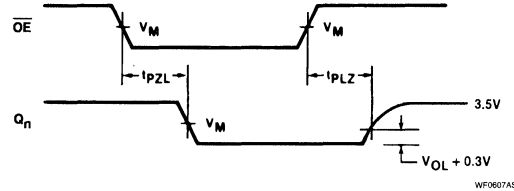
Waveform 1. Clock To Output Delays And Clock Pulse Width



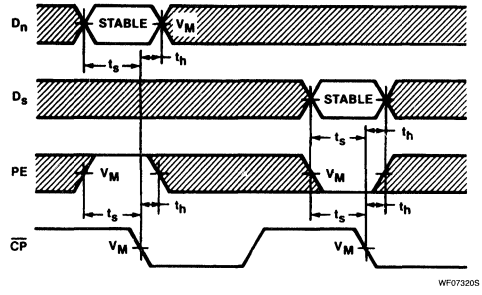
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



Waveform 3. 3-State Output Enable Time To HIGH Level And Disable Output Time From HIGH Level



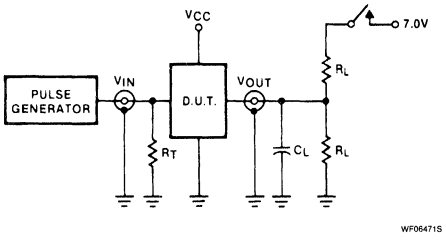
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

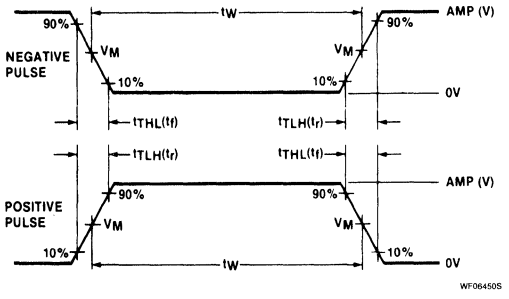


Waveform 5. Parallel Enable And Data Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS



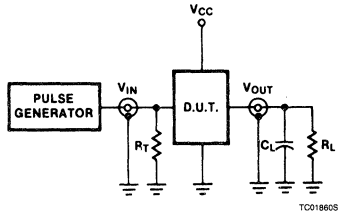


Test Circuit For 3-State Outputs

$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns



Test Circuit For Totem-Pole Output (Q_S Only)

SWITCH POSITION

TEST	SWITCH
t_{PZH}	open
t_{PZL}	closed
t_{PHZ}	open
t_{PLZ}	closed

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

6

Signetics

Logic Products

FAST 74F398, F399 Registers

'F398 – Quad 2-Port Register With True & Complementary Outputs
'F399 – Quad 2-Port Register
Product Specification

FEATURES

- **Select inputs from two data sources**
- **Fully positive edge-triggered operation**
- **Both True and Complementary outputs – 'F398**

DESCRIPTION

The 'F398 and 'F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F398	120MHz	25mA
74F399	120MHz	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F398N, N74F399N
Plastic SOL-20	N74F398D
Plastic SO-16	N74F399D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

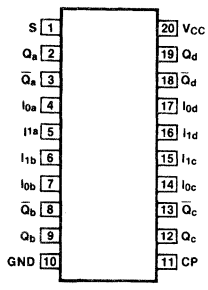
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{0d}$	Data inputs from source 0	1.0/1.0	20μA/0.6mA
$I_{1a} - I_{1d}$	Data inputs from source 1	1.0/1.0	20μA/0.6mA
S	Common select input	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$Q_a - Q_d$	Register true outputs	50/33	1.0mA/20mA
$\overline{Q}_a - \overline{Q}_d$	Register complementary outputs ('F398)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

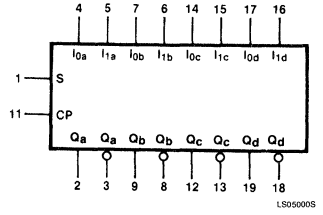
'F398



CD05250S

LOGIC SYMBOL

'F398

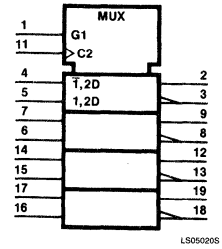


LS05000S

VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

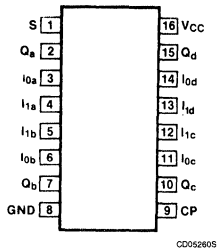
'F398



LS05020S

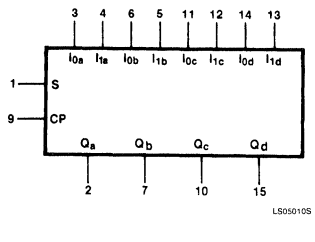
PIN CONFIGURATION

'F399



LOGIC SYMBOL

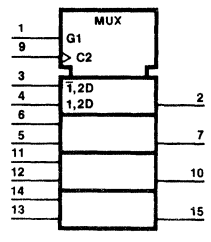
'F399



VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

'F399



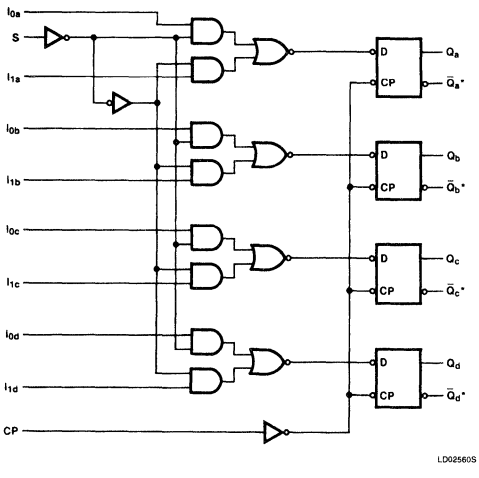
The 'F398 and 'F399 are high-speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a set-up time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 'F398 has both Q and $\overline{Q}$ outputs.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	**I_0**	**I_1**	**Q**	**$\overline{Q}$***
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

*F398 only
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
H = HIGH voltage level
X = Don't care

LOGIC DIAGRAM



*'F398 only

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F398, 74F399			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	'F398	V_{CC} = MAX			25	38	mA
		'F399				22	34	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH} V_{IN} = GND; I_{CCL} = Open

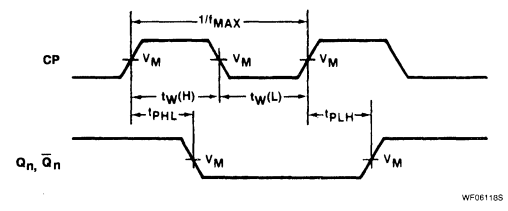
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F398, 74F399					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q or $\overline{Q}$	Waveform 1	3.0 3.0	5.7 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns

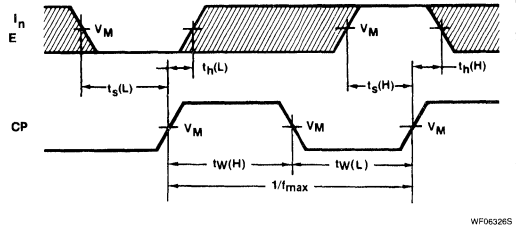
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F398, 'F399					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_l = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW I_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW I_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW S to CP	Waveform 2	7.5 7.5			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



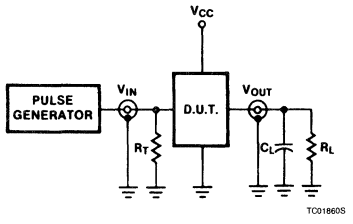
Waveform 1. Clock To Output Delays And Clock Pulse Width



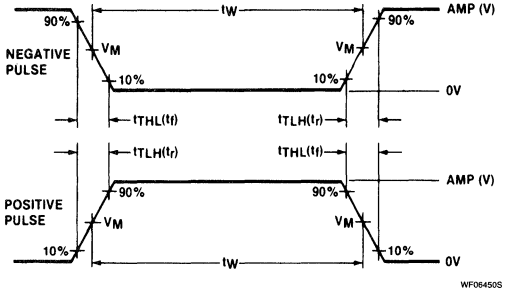
Waveform 2. Data Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F412, 74F432
Multi-Mode Buffered Latches

'F412 Multi-Mode Buffered Latch, Non-Inverting (3-State)
'F432 Multi-Mode Buffered Latch, Inverting (3-State)
Preliminary Specification

Logic Products

FEATURES

- **Status flip-flop for interrupt commands**
- **Asynchronous or latched Receiver modes**
- **'F412 Non-inverting 'F432 Inverting**
- **3-State outputs**
- **300 mil SLIM DIP package**
- **Functional equivalent to Intel 8212 except that 'F432 has inverting outputs**

DESCRIPTION

The 'F412/'F432 are 8-bit latch with 3-state output buffers. Also included is a status flip-flop for providing device-busy or request-interrupt commands.

Separate Mode (M) and Select ($\overline{S}_0$, S_1) inputs allow data to be stored with the outputs enabled or disabled. The devices can be also be operated in a fully transparent mode.

Both 'F412 and 'F432 are functional equivalent to the Intel 8212 except that 'F432 has the inverting outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F412	6.0ns	40mA
74F432	7.0ns	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F412N, N74F432N
Plastic SOL-24	N74F412D, N74F432D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

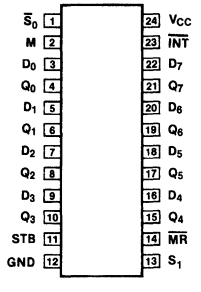
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{S}_0$, S_1	Select Inputs	1.0/1.0	20μA/0.6mA
STB	Strobe Input	1.0/1.0	20μA/0.6mA
M	Mode Control Input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset Input	1.0/1.0	20μA/0.6mA
$\overline{INT}$	Interrupt Output	50/40	1mA/24mA
$Q_0 - Q_7$	Data Latched Outputs	50/40	1mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

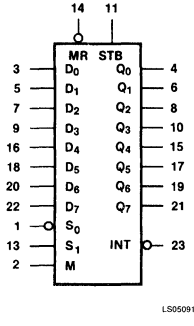
PIN CONFIGURATION

'F412



LOGIC SYMBOL

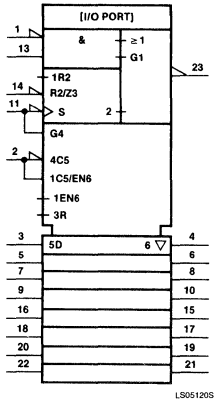
'F412



VCC = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

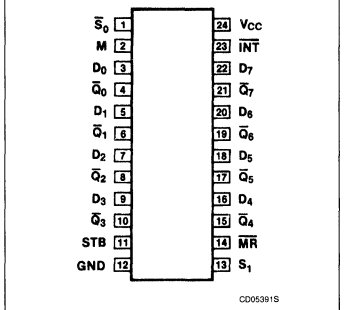
'F412



Multi-Mode Buffered Latches | FAST 74F412, 74F432

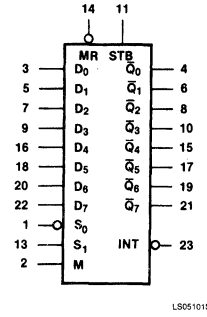
PIN CONFIGURATION

'F432



LOGIC SYMBOL

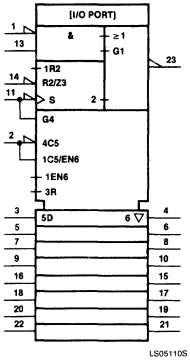
'F432



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

'F432



FUNCTIONAL DESCRIPTION

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The 3-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is HIGH and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_0$ and S_1), and the strobe (STB) inputs and during transparency each data output (Q_n) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M = L, the eight data latch inputs are enabled when the strobe is HIGH regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW, the latches will store the most-recently set-up data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S}_0$ and S_1) inputs.

FUNCTION TABLE for Data Latches

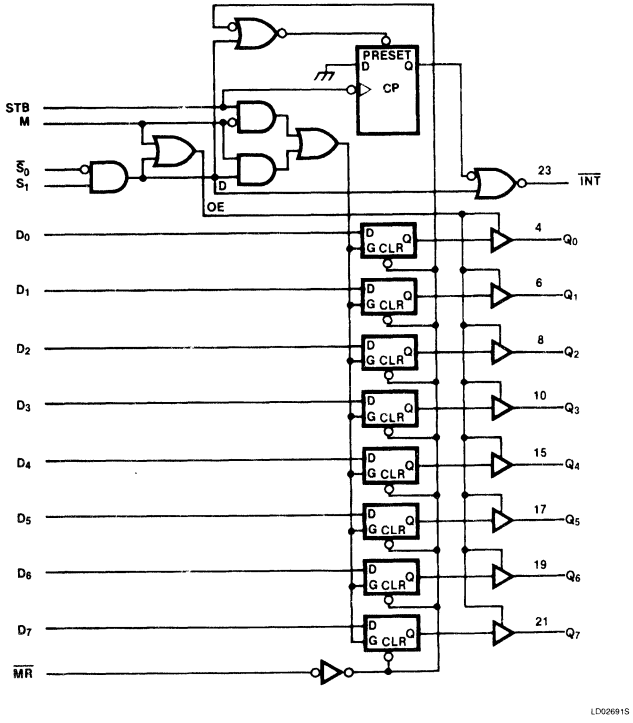
INPUTS					DATA IN	DATA OUT		OPERATING MODE
$\overline{MR}$	M	$\overline{S}_0$	S_1	STB		'F412	'F432	
L	H	H	X	X	X	L	H	Clear
L	L	L	H	L	X	L	H	
X	L	X	L	X	X	Z	Z	De – select
X	L	H	X	X	X	Z	Z	
H	H	H	L	X	X	Q_0	$\overline{Q}_0$	Hold
H	L	L	H	L	X	Q_0	$\overline{Q}_0$	
H	H	L	H	X	L	L	H	Data Bus
H	H	L	H	X	H	H	L	
H	L	L	H	H	L	L	H	Data Bus
H	L	L	H	H	H	H	L	

FUNCTION TABLE for Status Flip-flop

INPUTS				$\overline{INT}$
$\overline{MR}$	$\overline{S}_0$	S_1	STB	
L	H	X	X	H
L	X	L	X	H
H	X	X	↑	L
H	L	H	X	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER				TEST CONDITIONS[1]		74F412, 74F432			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current			V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	'F412	I_{CCH}	V_{CC} = MAX			38	50	mA
			I_{CCL}				45	60	mA
			I_{CCZ}				45	60	mA
		'F432	I_{CCH}	V_{CC} = MAX			43	65	mA
			I_{CCL}				29	43	mA
			I_{CCZ}				29	43	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F412					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	3.5 2.5	6.5 5.0	8.5 6.5	3.0 2.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 or STB to Q_n	Waveform 1	8.5 7.5	14.5 12.5	18.5 16.0	7.5 6.5	20.5 17.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S_0}$ or S_1 to $\overline{INT}$	Waveform 2	4.5 4.5	7.5 8.0	9.5 10.5	4.0 4.0	10.5 11.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 1	7.5	12.5	16.0	6.5	17.5	ns
t_{PHL}	Propagation delay STB to $\overline{INT}$	Waveform 2	6.5	11.0	14.0	5.5	15.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{S_0}$ to Q_n	Waveform 4 Waveform 5	8.0 6.5	12.5 11.0	18.0 14.0	7.0 5.5	19.0 15.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level $\overline{S_0}$ to Q_n	Waveform 4 Waveform 5	4.5 6.5	8.0 11.0	10.5 14.0	4.0 5.5	11.5 15.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level S_1 to Q_n	Waveform 4 Waveform 5	7.5 5.0	12.5 9.0	16.0 11.5	6.5 4.5	17.5 12.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level S_1 to Q_n	Waveform 4 Waveform 5	4.5 5.5	7.5 9.5	9.5 12.0	4.0 4.5	10.5 13.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level M to Q_n	Waveform 4 Waveform 5	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level M to Q_n	Waveform 4 Waveform 5	4.0 5.0	7.0 8.5	9.0 11.0	3.5 4.5	10.0 12.0	ns

NOTE: Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F412					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to $\overline{S_0}$, S_1 or STB	Waveform 3	0 0			2.0 2.0	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{S_0}$, S_1 or STB	Waveform 3	8.0 8.0			10.0 10.0	9.0 9.0	ns
$t_w(H)$ $t_w(L)$	$\overline{S_0}$, S_1 or STB Pulse width, HIGH or LOW	Waveform 3	8.0 8.0			11.0 11.0	9.0 9.0	ns
t_w	$\overline{MR}$ pulse width	Waveform 2	8.0			11.5	9.0	ns

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AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

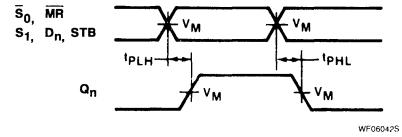
PARAMETER		TEST CONDITIONS	74F432					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 2	3.5 2.5	8.5 5.5	10.5 7.0	3.0 3.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 or STB to $\overline{Q}_n$	Waveform 1	8.5 6.5	16.0 12.5	21.0 16.0	7.5 5.5	23.0 18.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 2	7.0	15.0	18.5	6.0	20.5	ns
t_{PHL}	Propagation delay STB to $\overline{INT}$	Waveform 2	6.0	11.5	14.5	5.0	16.0	ns
t_{PHL}	Propagation delay $\overline{S}_0$, S_1 to $\overline{INT}$	Waveform 2	4.0	7.5	9.5	3.5	10.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{Q}_n$	Waveform 2	9.0 6.5	15.0 11.0	19.0 14.0	9.0 6.5	20.0 15.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{S}_0$, S_1 to $\overline{Q}_n$	Waveform 4 Waveform 5	4.5 5.0	13.0 11.0	18.0 15.0	4.0 4.0	20.0 17.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level $\overline{S}_0$, S_1 to $\overline{Q}_n$	Waveform 4 Waveform 5	4.0 5.0	8.0 11.0	11.0 15.5	3.5 4.0	12.5 17.5	ns

NOTE: Subtract 0.2ns from minimum values for SO package.

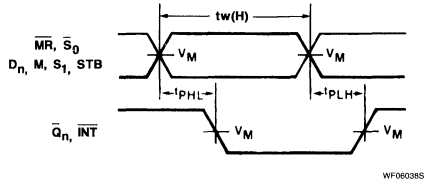
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F432					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to $\overline{S}_0$ S_1 or STB	Waveform 3	0 0			2.0 2.0	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{S}_0$, S_1 or STB	Waveform 3	11.0 8.5			12.5 9.5	9.0 9.0	ns
$t_w(H)$ $t_w(L)$	$\overline{S}_0$, S_1 or STB Pulse width, HIGH or LOW	Waveform 3	8.0 8.0			9.0 9.0	9.0 9.0	ns
$t_w(L)$	$\overline{MR}$ pulse width LOW	Waveform 2	8.0			9.0	9.0	ns

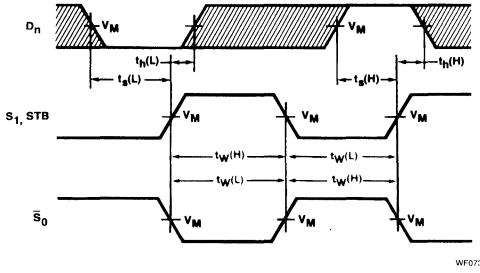
AC WAVEFORMS



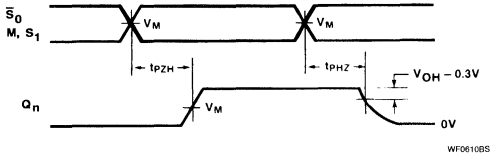
Waveform 1. Propagation Delay For Non-Inverting Outputs



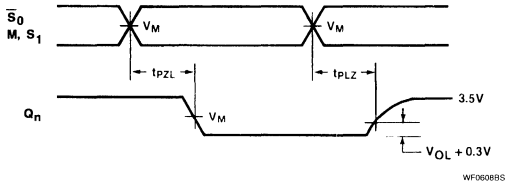
Waveform 2. Propagation Delay For Inverting Outputs Disable Time From HIGH Level



Waveform 3. Set-up and Hold Times



Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



Waveform 5. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

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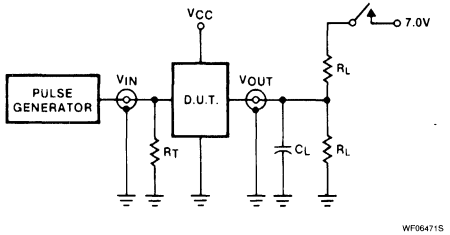
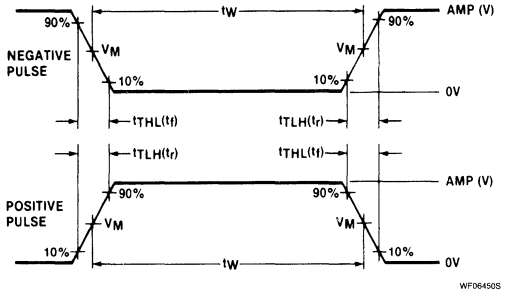
TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F455, 74F456
Buffers/Drivers

'F455 Octal Buffer/Line Driver with Parity, Inverting (3-State)
'F456 Octal Buffer/Line Driver with Parity, Inverting (3-State)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **'F455 combines 'F240 and 'F280A functions in one package**
- **'F456 combines 'F241 and 'F280A functions in one package**
- **'F455A and 'F456A are center pin versions of the 'F655A and 'F656A respectively**
- **'F455 Inverting**
  'F456 Non-inverting
- **3-State outputs sink 64mA and source 15mA**
- **24-pin plastic slim DIP (300 mil) package**
- **Inputs on one side and outputs on the other side simply PC board layout**

DESCRIPTION

The 'F455 and 'F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F455	3.5ns	70mA
74F456	4.5ns	70mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F455N, N74F456N
Plastic SOL-24	N74F455D, N74F456D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	1.0/0.033	20μA/20μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$	3-State output enable inputs (active LOW)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs ('F455)	750/106.7	15mA/64mA
Y_n	Data outputs ('F456)	750/106.7	15mA/64mA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA

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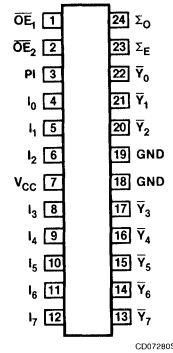
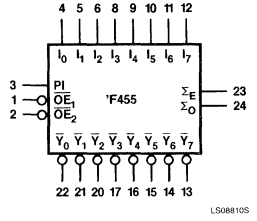
PIN CONFIGURATION

'F455



LOGIC SYMBOL

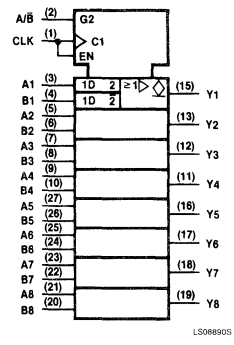
'F455



V_{CC} = Pin 16
GND = Pin 18 and 19

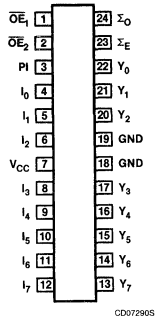
LOGIC SYMBOL (IEEE/IEC)

'F455



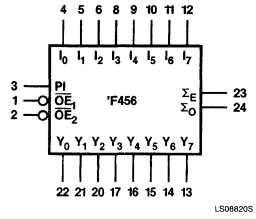
PIN CONFIGURATION

'F456



LOGIC SYMBOL

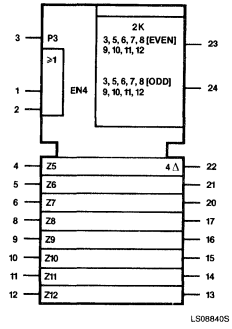
'F456



V_{CC} = Pin 16
GND = Pin 18 and 19

LOGIC SYMBOL (IEEE/IEC)

'F456



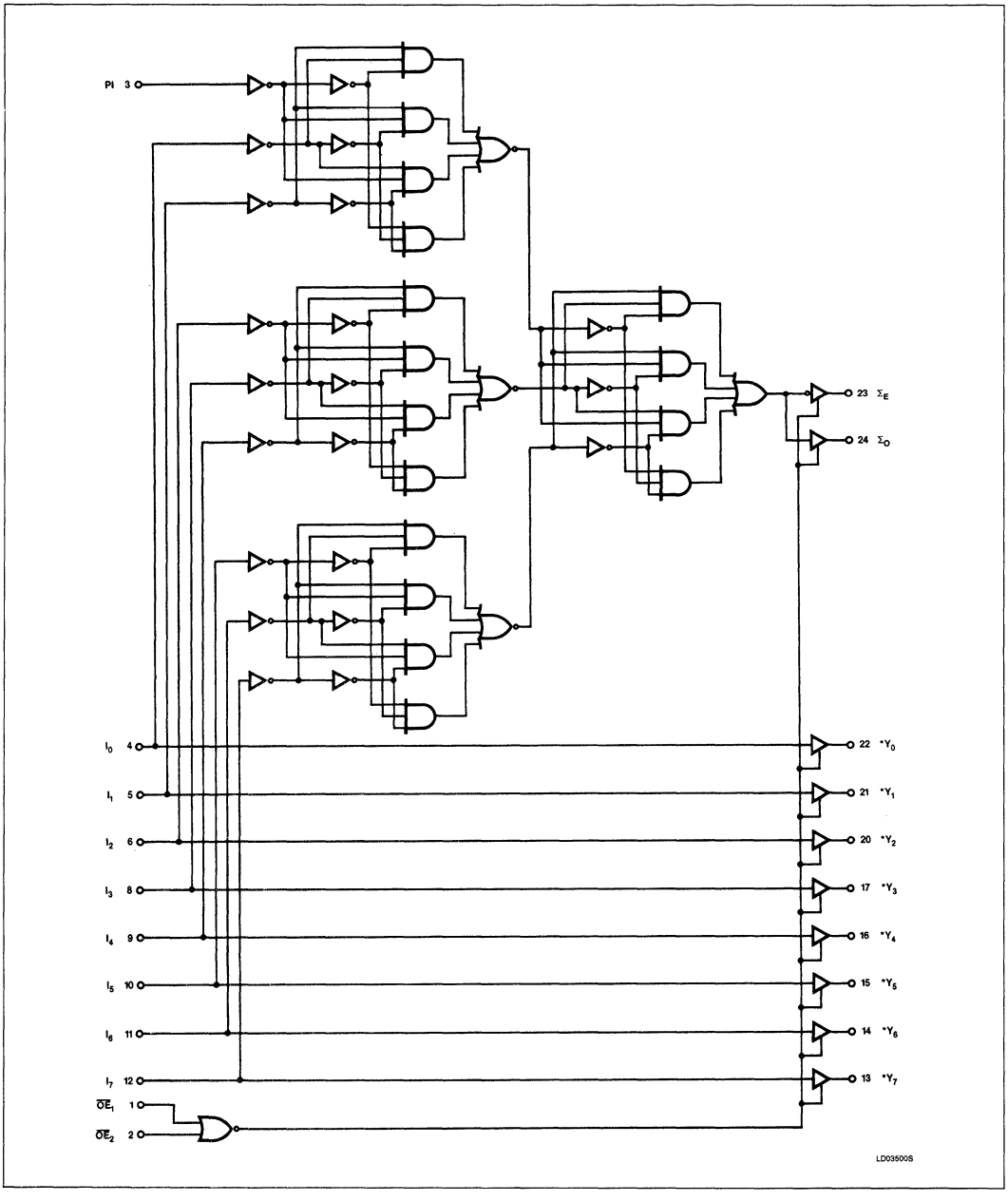
FUNCTION TABLES

INPUTS			DATA OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I_n	'F455	'F456
L	L	L	H	L
L	L	H	L	H
H	X	X	(Z)	(Z)
X	H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance level

INPUTS	PARITY OUTPUTS	
Number of inputs HIGH (PI, $I_0 - I_7$)	Σ_E	Σ_O
Even – 0, 2, 4, 6, 8	H	L
Odd – 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = HIGH	(Z)	(Z)

LOGIC DIAGRAM FOR 'F456 (*outputs are inverted for 'F455)



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F455, 74F456			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.35	.50	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{OZH}	Off-state current HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					50	μA
I_{OZL}	Off-state current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					63	90	mA

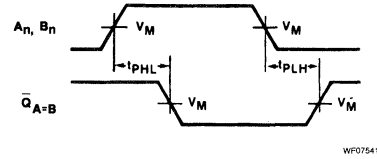
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

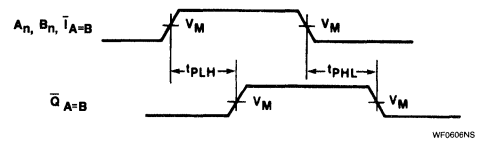
PARAMETER			TEST CONDITIONS	74F455, 74F456					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	'F455	Waveform 1	2.0	4.5	6.5	2.0	7.5	ns
t_{PHL}	I_n to Y_n			1.0	2.0	4.0	1.0	4.5	
t_{PLH}	Propagation delay	'F456	Waveform 2	2.0	4.5	6.5	2.0	7.0	ns
t_{PHL}	I_n to Y_n			2.5	5.0	7.0	2.5	7.5	
t_{PLH}	Propagation delay		Waveform 1, 2	5.5	10.0	13.0	5.5	14.0	ns
t_{PHL}	I_n to Σ_E, Σ_O			5.5	11.0	14.5	5.5	16.5	
t_{PZH}	Enable Time to HIGH level		Waveform 3	4.5	7.0	9.5	4.0	10.5	ns
t_{PZL}	Enable Time to LOW level		Waveform 4	4.5	8.0	10.5	4.5	11.5	
t_{PHZ}	Disable Time from HIGH level		Waveform 3	1.5	4.0	6.5	1.5	7.5	ns
t_{PLZ}	Disable Time from LOW level		Waveform 4	2.0	5.0	7.5	2.0	8.0	

NOTE:
Subtract 0.2ns from minimum values for SO package.

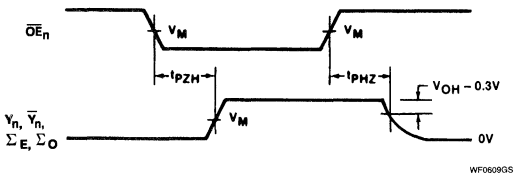
AC WAVEFORMS



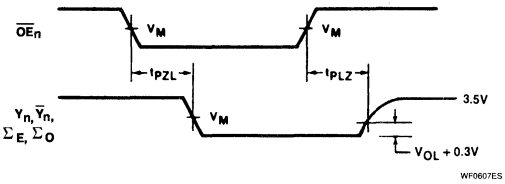
Waveform 1. Propagation Delay For I_n To Σ_E, Σ_O, Y_n



Waveform 2. Propagation Delay For I_n To Σ_E, Σ_O, Y_n



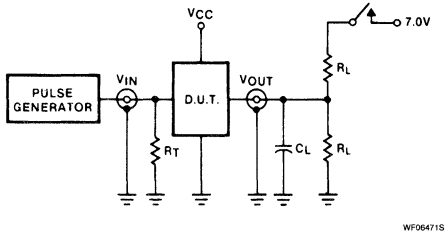
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



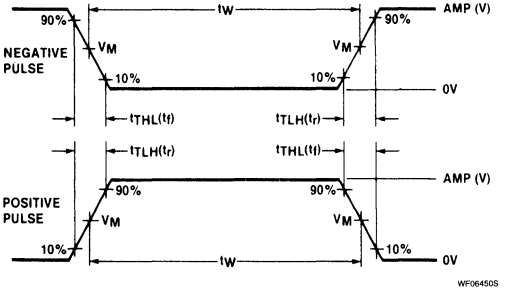
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F521 Comparator

8 Bit Identity Comparator
Product Specification

Logic Products

FEATURES

- **Compares two 8-bit words in 6.5ns typical**
- **Expandable to any word length**
- **High Speed version of ALS688**

DESCRIPTION

The 'F521 is an expandable 8-bit comparator. It compares two words of up to 8 bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active-LOW enable input.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F521	7.0ns	20.0mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F521N
Plastic SOL-20	N74F521D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

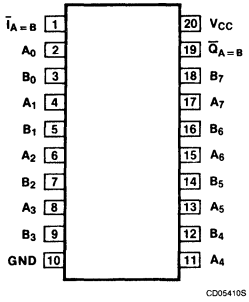
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7	Word A inputs	1.0/1.0	20μA/0.6mA
B_0-B_7	Word B inputs	1.0/1.0	20μA/0.6mA
$T_{A=B}$	Expansion or enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{Q}_{A=B}$	Identity output (active LOW)	50/33	1.0mA/20mA

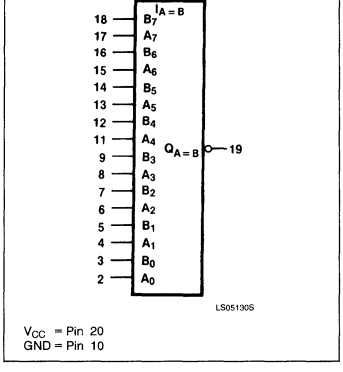
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

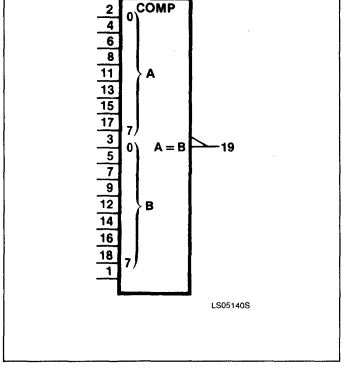
PIN CONFIGURATION



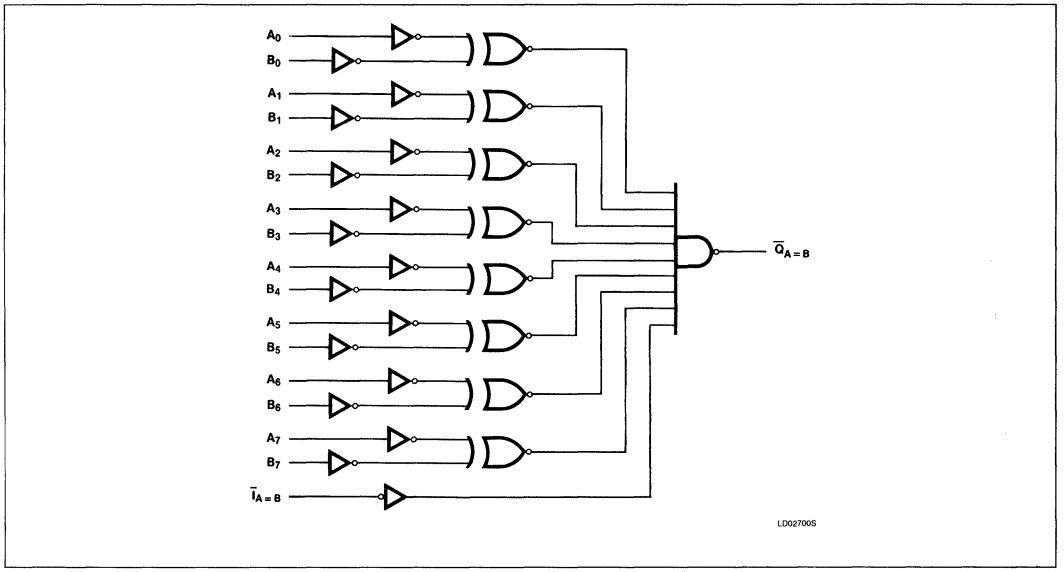
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{Q}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH voltage level
L = LOW voltage level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F521			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			24	36	mA
		I_{CCL}				15.5	23	mA

NOTES:

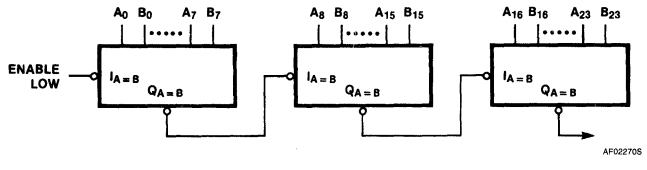
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. For I_{CCH} all inputs are grounded except B_0 can be any one input, which is at 4.5V. For I_{CCL} all inputs are grounded.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

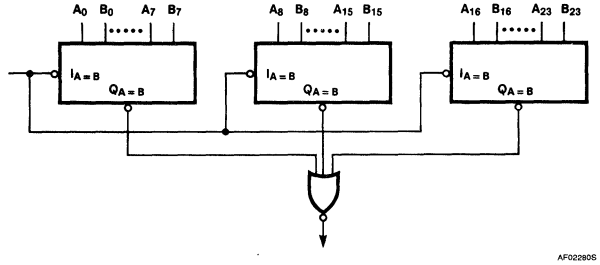
PARAMETER		TEST CONDITIONS	74F521					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{Q}_{A=B}$	Waveform 1, 2	3.5 4.0	8.0 8.0	9.5 9.0	3.5 4.0	11 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_{A=B}$ to $\overline{Q}_{A=B}$	Waveform 2	3.0 3.5	5.0 6.5	6.5 7.0	3.0 3.5	7.5 8.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

APPLICATION DIAGRAMS

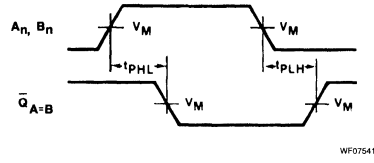


Ripple Expansion

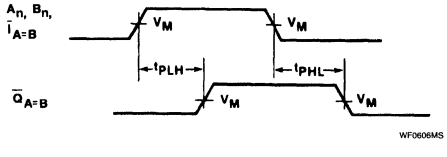


Parallel Expansion

AC WAVEFORMS



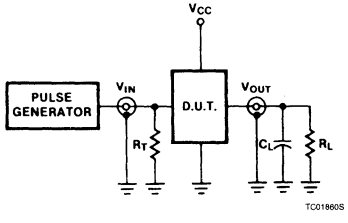
Waveform 1. For Inverting Outputs



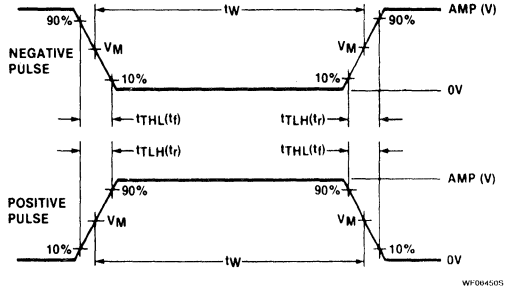
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F524
Comparator

8-Bit Register Comparator (Open-Collector + 3-State)
Preliminary Specification

Logic Products

FEATURES

- **8-bit bidirectional register with bus-oriented input-output**
- **Independent serial input-output to register**
- **Register bus comparator with 'equal to', 'greater than' and 'less than' outputs**
- **Cascadable in groups of 8 bits**
- **Open-collector comparator outputs for AND-wired expansion**
- **Two's complement or magnitude compare**

DESCRIPTION

The 'F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines (S_0, S_1) to execute shift, load, hold and read out.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F524		

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74F524N
Plastic SOL-20	N74F524D

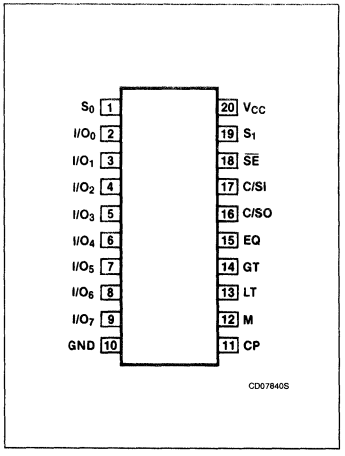
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

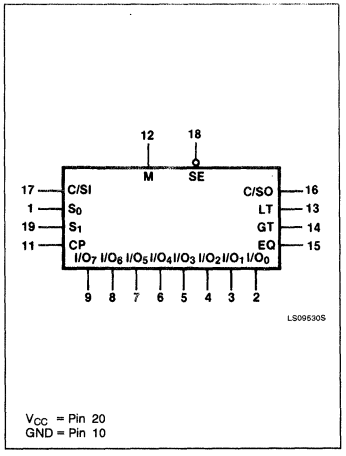
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
S_0, S_1	Mode select inputs	1.0/1.0	20μA/0.6mA
C/SI	Status priority or serial data input	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{SE}$	Status enable input (active LOW)	1.0/1.0	20μA/0.6mA
M	Compare mode select input	1.0/1.0	20μA/0.6mA
$I/O_0 - I/O_7$	Parallel data inputs or	2.5/1.0	50μA/0.6mA
	3-State parallel data outputs	150/33	3.0mA/20mA
C/SO	Status priority or serial data output	50/33	1.0mA/20mA
LT	Register less than bus output	OC*/33	OC*/20mA
EQ	Register equal to bus output	OC*/33	OC*/20mA
GT	Register greater than bus output	OC*/33	OC*/20mA

NOTES:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
*OC = Open Collector

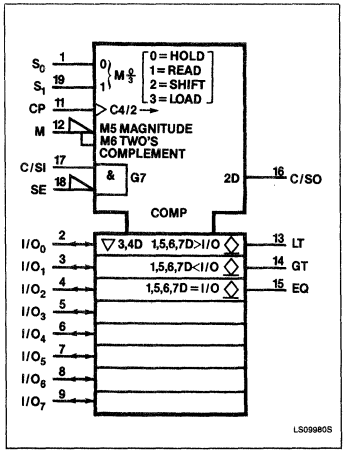
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Comparator | FAST 74F524

An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-HIGH, open-collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow two's complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

FUNCTIONAL DESCRIPTION

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus $I/O_0 - I/O_7$. Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occurs on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals, S_0 and S_1, according to the Select Truth Table. The 3-State parallel output buffers are enabled only in the Read mode.

SELECT TRUTH TABLE

S_0	S_1	OPERATION
L	L	HOLD — Retains data in shift register
L	H	READ — Read contents in register onto data bus
H	L	SHIFT — Allows serial shifting on next rising clock edge
H	H	LOAD — Load data on bus into register.

H = HIGH Voltage Level
L = LOW Voltage Level

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, open-collector outputs indicate whether the contents held in the shift register are 'greater than' (GT), 'less than' (LT), or 'equal to (EQ) the data on the input bus. A HIGH signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A Mode control input (M) allows selection between a straightforward magnitude compare or a comparison between two's complement numbers.

NUMBER REPRESENTATION SELECT TABLE

M	OPERATION
L	Magnitude compare
H	Two's complement compare

H = HIGH Voltage Level
L = LOW Voltage Level

For 'greater than' or 'less than' detection, the C/SI input must be held HIGH, as indicated in the Status Truth Table. The internal logic is arranged such that a LOW signal on the C/SI input disables the 'greater than' and 'less than' outputs. The C/SO output will be forced HIGH if the 'equal to' status condition exists, otherwise C/SO will be held LOW. These facilities enable the 'F524 to be cascaded for word lengths greater than 8 bits.

STATUS TRUTH TABLE (Hold Mode)

INPUTS			OUTPUTS			
$\overline{SE}$	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	X	X	H	H	H	①
L	L	$O_A - O_H > I/O_0 - I/O_7$	L	H	H	L
L	L	$O_A - O_H = I/O_0 - I/O_7$	H	H	H	H
L	L	$O_A - O_H < I/O_0 - I/O_7$	L	H	H	L
L	H	$O_A - O_H > I/O_0 - I/O_7$	L	H	L	L
L	H	$O_A - O_H = I/O_0 - I/O_7$	H	L	L	H
L	H	$O_A - O_H < I/O_0 - I/O_7$	L	L	H	L

① = HIGH if data are not equal, otherwise LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Word length expansion (in groups of 8 bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Figure 1). The C/SI input of the most significant device is held HIGH while the $\overline{SE}$ input of the least significant device is held LOW. The corresponding status outputs are AND-wired together. In the case of two's complement number compare, only the Mode input to the most significant device should be HIGH. The Mode inputs to all other cascaded devices are held LOW.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, then the EQ and LT outputs will be pulled LOW, whereas the GT output will float HIGH. Also, the C/SO output of the most significant device will be forced LOW, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go LOW, whereas LT output floats HIGH.

If an equality condition is detected in the most significant device, its C/SO output is forced HIGH. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving 'n' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35 + 6 (n-s) ns.

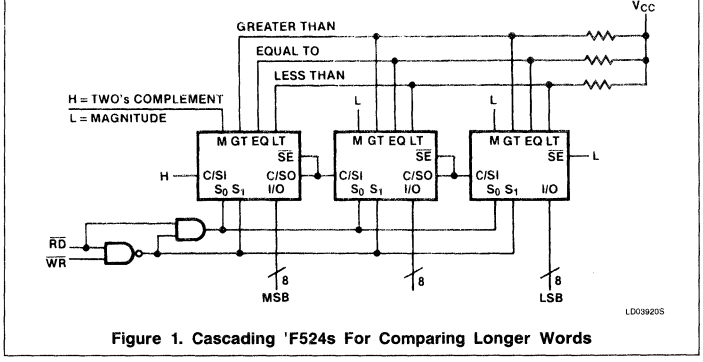
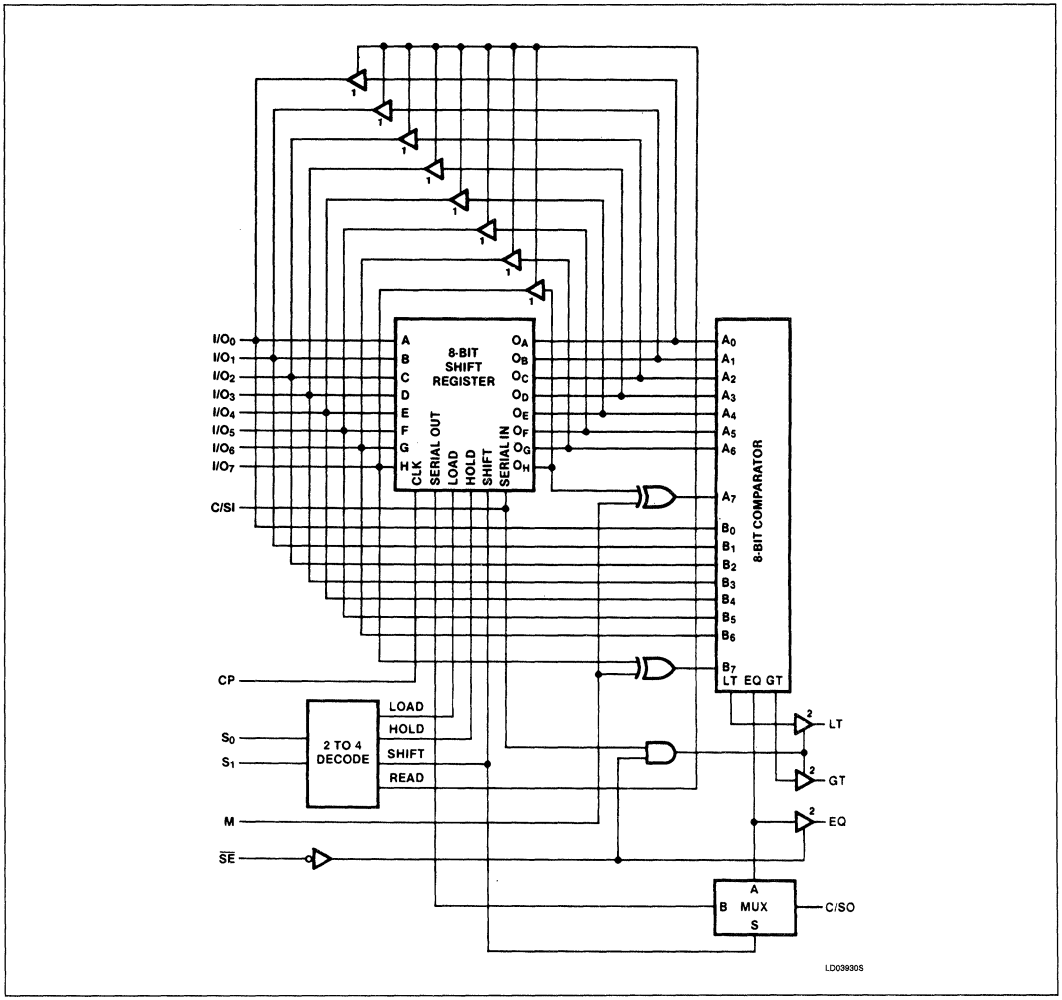


Figure 1. Cascading 'F524s For Comparing Longer Words

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage	LT, EQ, GT only			4.5	V
I_{OH}	HIGH-level output current	Except LT, EQ, GT			−3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F524			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	LT, EQ, GT only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OH}	HIGH-level output voltage	Except LT, EQ, GT	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V			2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]	Except LT, EQ, GT	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX					mA
		I_{CCL}					180	mA
		I_{CCZ}						mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

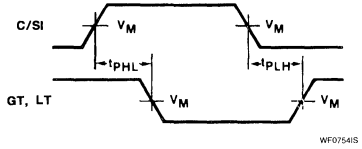
PARAMETER		TEST CONDITIONS	74F524					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V$ $\pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 4	50			50		MHz
t_{PLH} t_{PHL}	Propagation delay I/O_n to EQ	Waveform 2	9.5 6.0		20 12	9.5 6.0	22.5 13	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to GT	Waveform 2	8.5 7.0		18 14.5	8.5 7.0	19 15.5	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to LT	Waveform 2	7.0 6.0		16 14	7.0 6.0	18 15	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to C/SO	Waveform 2	9.0 6.0		19.5 13	9.0 6.0	21.5 14	ns
t_{PLH} t_{PHL}	Propagation delay CP to EQ	Waveform 4	10.5 4.0		22 9.0	10.5 3.5	24.5 10	ns
t_{PLH} t_{PHL}	Propagation delay GP to GT	Waveform 4	10 9.0		21 20	10 9.0	22 21.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to LT	Waveform 4	9.0 6.0		19.5 12.5	9.0 6.0	21 13.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO (compare)	Waveform 4	8.5		18.5	8.5	21.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO (serial shift)	Waveform 4	5.0 5.0		10.5 10	5.0 5.0	11.5 11	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to GT	Waveform 1	9.0 3.5		19 8.5	9.0 3.0	20 9.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to LT	Waveform 1	8.0 4.0		17 8.5	8.0 4.0	18 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to C/SO	Waveform 2	7.0 6.0		14.5 12	7.0 6.0	15.5 13	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to EQ	Waveform 2	4.0 2.5		8.0 6.0	4.0 2.5	9.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to GT	Waveform 2	7.5 3.5		16 8.0	7.5 3.5	17 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to LT	Waveform 2	5.0 3.5		11 8.0	5.0 3.5	12 9.0	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to C/SO	Waveform 2	4.5 4.0		9.5 9.5	4.5 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay M to GT	Waveform 2	8.0 7.0		17 15.5	8.0 7.0	18 17	ns
t_{PLH} t_{PHL}	Propagation delay M to LT	Waveform 2	8.5 5.5		19 12	8.5 5.5	21 13	ns
t_{PZH} t_{PZL}	Output enable time S_0, S_1 to I/O_n	Waveform 5, 6	6.0 6.5		13 14.5	6.0 6.5	14 15.5	ns
t_{PHZ} t_{PLZ}	Output disable time S_0, S_1 to I/O_n	Waveform 5, 6	5.0 5.5		10 12.5	5.0 5.5	11 13.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

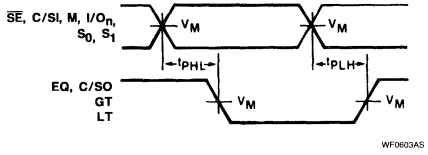
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F524					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V$ ± 10% $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW I/O_n to CP	Waveform 3	5.0 5.0		5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW I/O_n to CP	Waveform 3	0 0		0 0			ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW S_0, S_1 to CP	Waveform 3	10 10		10 10			ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW C/SI to CP	Waveform 3	5.0 7.0		5.0 7.0			ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW C/SI to CP	Waveform 3	0 0		0 0			ns
$t_W(H)$	Clock pulse width HIGH	Waveform 4	4.0		4.0			ns

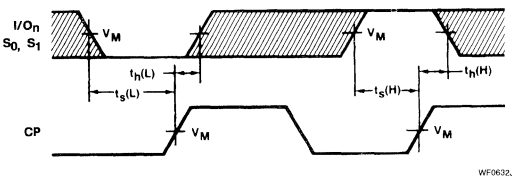
AC WAVEFORMS



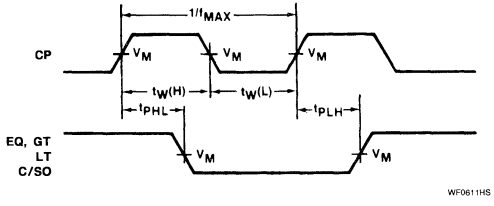
Waveform 1. For Inverting Outputs



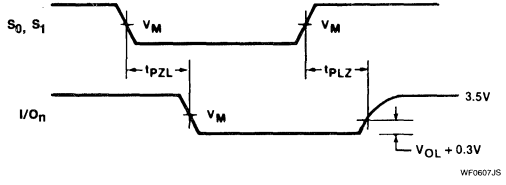
Waveform 2. For Non-Inverting Outputs



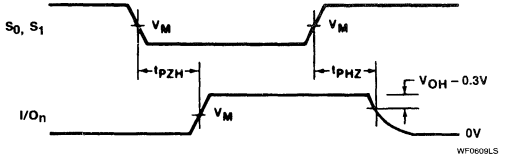
Waveform 3. Data Set-up And Hold Times



Waveform 4. Clock To Output Delays And Clock Pulse Width



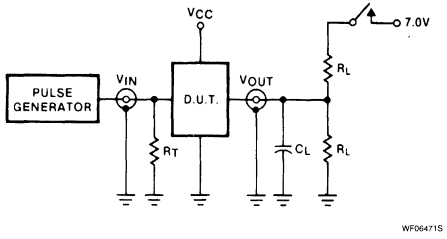
Waveform 5. 3-State Enable Time To Low Level And Disable Time From Low Level



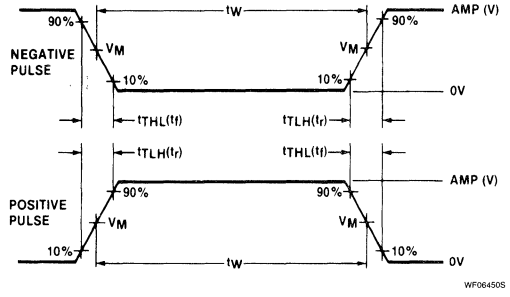
Waveform 6. 3-State Enable Time To High Level And Disable Time From High Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State And Open Collector Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

Logic Products

FAST 74F533, 74F534
Latch/Flip-Flop

'F533 Octal Transparent Latch (3-State)
'F534 Octal D Flip-Flop (3-State)
Product Specification

FEATURES

- **8-bit transparent latch — 'F533**
- **8-bit positive edge-triggered register — 'F534**
- **3-State inverting output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

DESCRIPTION

The 'F533 is an octal transparent latch coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the HIGH-to-LOW enable transition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F533	6.0ns	41mA
74F534	6.6ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F533N, N74F534N
Plastic SOL-20	N74F533D, N74F534D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

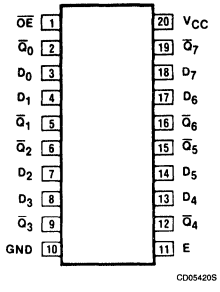
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/1.0	20μA/0.6mA
E ('F533)	Latch enable input (active HIGH)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
CP ('F534)	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0 - \overline{Q}_7$	3-State outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

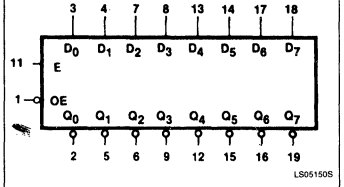
PIN CONFIGURATION

'F533



LOGIC SYMBOL

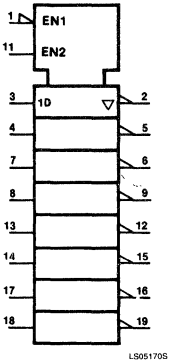
'F533



VCC = Pin 20
GND = Pin 10

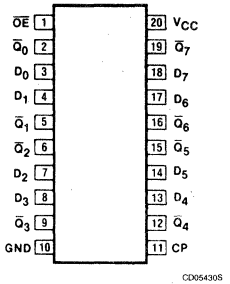
LOGIC SYMBOL (IEEE/IEC)

'F533



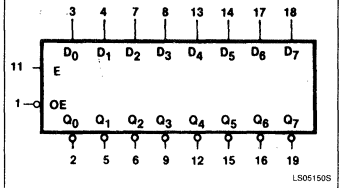
PIN CONFIGURATION

'F534



LOGIC SYMBOL

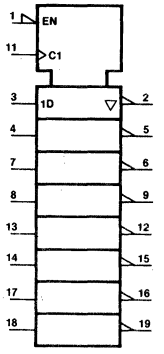
'F534



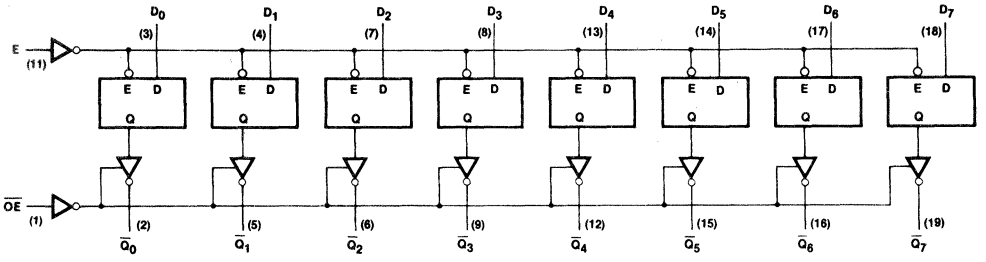
VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

'F534

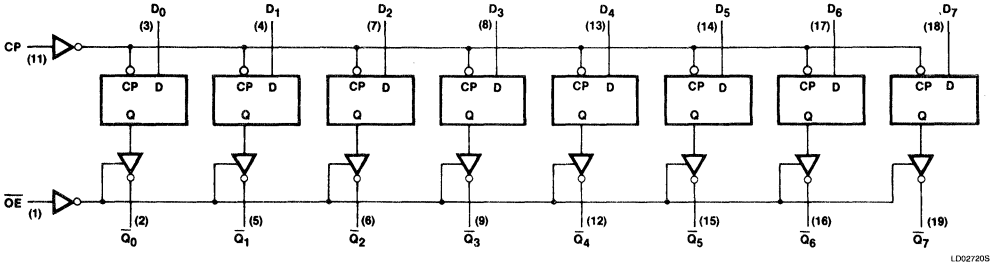


LOGIC DIAGRAM, 'F533



VCC = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 'F534



VCC = Pin 20
GND = Pin 10

MODE SELECT — FUNCTION TABLE, 'F533

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$\overline{Q}_0 - \overline{Q}_7$
Enable and read register	L	H	X	L	H
	L	H	X	H	L
Latch and read register	L	L	L	L	H
	L	L	H	H	L
Latch register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

MODE SELECT — FUNCTION TABLE, 'F534

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0 - \overline{Q}_7$
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
X = Don't care
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{E}$ transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

The 'F534 is an 8-bit edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause the clocking operation.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{CE}$ is LOW, data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F533, 'F534			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}	Off-stage output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V			2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−90	−150	mA
I_{CC}	Supply current[4] (total)	'F533	V_{CC} = MAX			41	61	mA
		'F534				55	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. 'F533 measure I_{CCZ} with $\overline{OE}$ input at 4.5V, D_n and E inputs at ground and all outputs open.
   'F534 measure I_{CCZ} with $\overline{OE}$ inputs at 4.5V and D_n inputs at ground and all outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

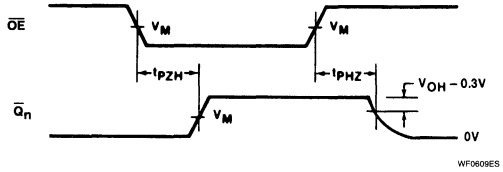
PARAMETER		TEST CONDITIONS	74F533, 'F534					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V$ ± 10% $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 3 'F534	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 6 'F533	4.0 3.0	6.9 5.2	9.0 7.0	4.0 3.0	10 8.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$	Waveform 7 'F533	5.0 3.0	8.5 5.6	11 7.0	5.0 3.0	13 8.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	Waveform 3 'F534	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10 10	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	Waveform 1 'F533 Waveform 2	2.0 2.0	7.7 5.1	10 6.5	2.0 2.0	11 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 1 'F533 Waveform 2	2.0 2.0	4.7 4.1	6.0 5.5	2.0 2.0	7.0 6.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	Waveform 1 'F534 Waveform 2	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 1 'F534 Waveform 2	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 6.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

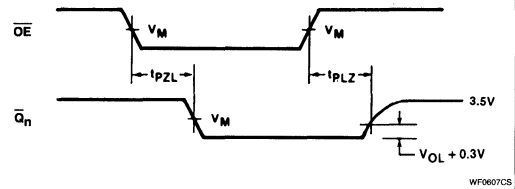
AC SET-UP REQUIREMENTS

PARAMETER			TEST CONDITIONS	74F533, 'F534					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V$ ± 10% $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, D_n to E	'F533	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, D_n to E		Waveform 5	3.0 3.0			3.0 3.0		ns
$t_w(H)$	E pulse width HIGH		Waveform 5	6.0			6.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, D_n to CP	'F534	Waveform 4	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 4	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW		Waveform 3	7.0 6.0			7.0 6.0		ns

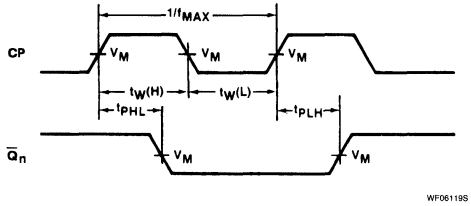
AC WAVEFORMS



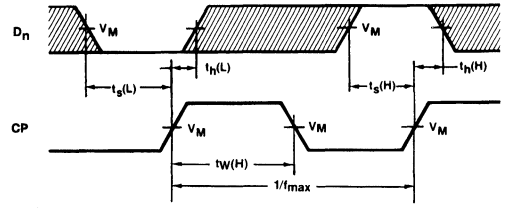
Waveform 1. 3-State Output Enable Time To HIGH Level and Output Disable Time From HIGH Level



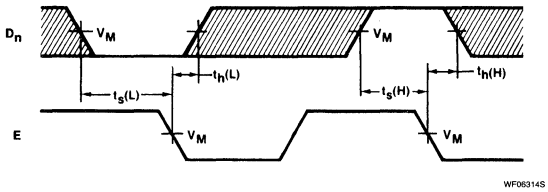
Waveform 2. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



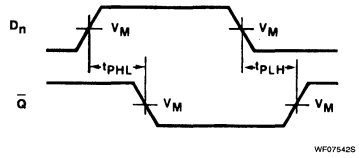
Waveform 3. Clock To Output Delays And Clock Pulse Width



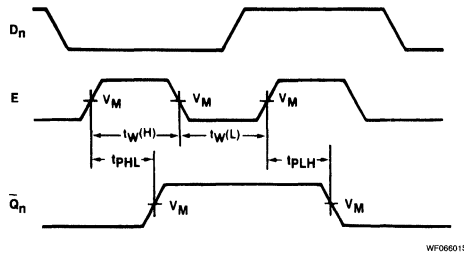
Waveform 4. Data Set-up And Hold Times



Waveform 5. Data Set-up And Hold Times



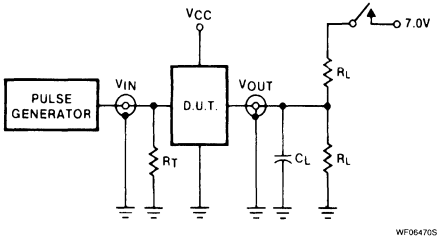
Waveform 6. Data To Output Delays



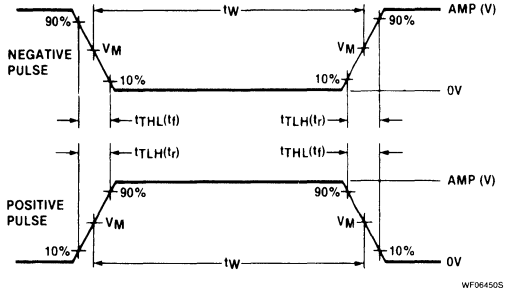
Waveform 7. Latch Enable To Output Delays

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

6

Signetics

Logic Products

FAST 74F537, 74F538, 74F539 Decoders

Preliminary Specification

'F537 1-Of-10 Decoder (3-State)
'F538 1-Of-8 Decoder (3-State)
'F539 Dual 1-Of-4 Decoder (3-State)

DESCRIPTION

The 'F537 is one-of-ten decoder/demultoplexer with four active HIGH BCD inputs and ten mutually exclusive outputs. A polarity control (P) input determines whether the outputs are active LOW or active HIGH. The 'F537 has 3-state outputs, and a HIGH signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high impedance state. Two input Enables, active HIGH (E_1) and active LOW ($\overline{E}_0$), are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

The 'F538 decoder/demultiplexer accepts three address ($A_0 - A_3$) input signals and decodes them to select one of eight mutually exclusive outputs A polarity control (P) input determines whether the outputs are active LOW or active HIGH. The 'F538 has 3-state outputs, and a HIGH signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high impedance state. Two active HIGH and two active LOW input Enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

The 'F539 contains two independent decoders. Each accepts two Address (A_0, A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control (P) input determines whether the outputs are active LOW or active HIGH. An active LOW input Enable (E) is available for demultiplexing data to the selected output in either non-inverted or inverted form.

TYPE	TYPICAL fMAX	TYPICAL SUPPLY CURRENT (TOTAL)
74F537	9ns	44mA
74F538	9ns	37mA
74F539	12ns	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F537N, N74F538N, N74F539N
Plastic SOL-20	N74F537D, N74F538D, N74F539D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

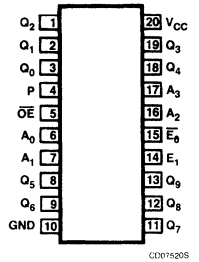
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F537	$A_0 - A_3$	Address inputs	1.0/1.0	20μA/0.6mA
	$\overline{E}_0$	Enable input (active LOW)	1.0/1.0	20μA/0.6mA
	E_1	Enable input (active HIGH)	1.0/1.0	20μA/0.6mA
	P	Polarity control input	1.0/1.0	20μA/0.6mA
	$\overline{OE}$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
	$Q_0 - Q_9$	Data outputs	150/40	3mA/24mA
'F538	$A_0 - A_3$	Address inputs	1.0/1.0	20μA/0.6mA
	$\overline{E}_0$, $\overline{E}_1$	Enable input (active LOW)	1.0/1.0	20μA/0.6mA
	E_2, E_3	Enable input (active HIGH)	1.0/1.0	20μA/0.6mA
	P	Polarity control input	1.0/1.0	20μA/0.6mA
	$\overline{OE}_0$, $\overline{OE}_1$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
	$Q_0 - Q_7$	Data outputs	150/40	3mA/24mA
'F539	$A_{0a} - A_{1a}$	Decoder a address inputs	1.0/1.0	20μA/0.6mA
	$A_{0b} - A_{1b}$	Decoder a address inputs	1.0/1.0	20μA/0.6mA
	$\overline{E}_a$, $\overline{E}_b$	Enable input (active LOW)	1.0/1.0	20μA/0.6mA
	$\overline{OE}_a$, $\overline{OE}_b$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
	P_a, P_b	Polarity control input	1.0/1.0	20μA/0.6mA
	$Q_{0a} - Q_{3a}$	Decoder a data outputs	150/40	3mA/24mA
	$Q_{0b} - Q_{3b}$	Decoder b data outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

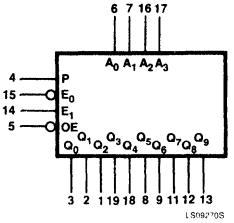
PIN CONFIGURATION

'F537



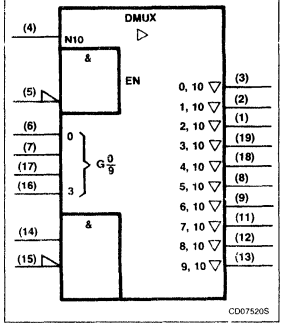
LOGIC SYMBOL

'F537



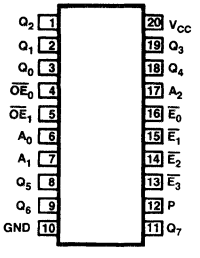
LOGIC SYMBOL (IEEE/IEC)

'F537



PIN CONFIGURATION

'F538



LOGIC SYMBOL

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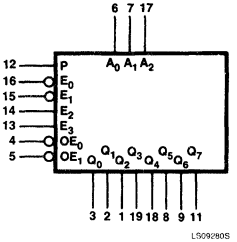
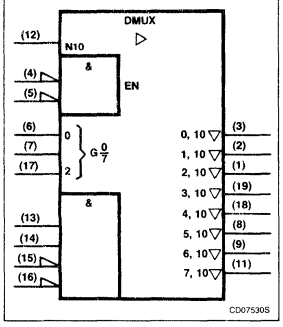


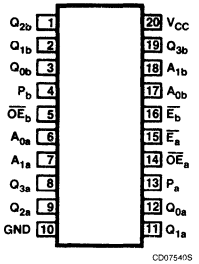
LOGIC SYMBOL (IEEE/IEC)

'F538



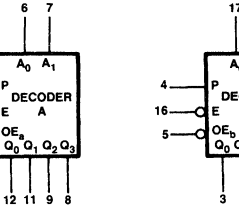
PIN CONFIGURATION

'F539



LOGIC SYMBOL

'F539



LOGIC SYMBOL (IEEE/IEC)

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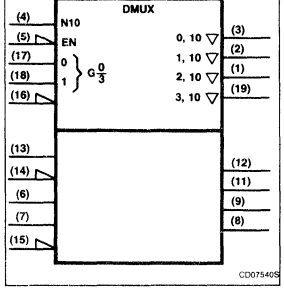
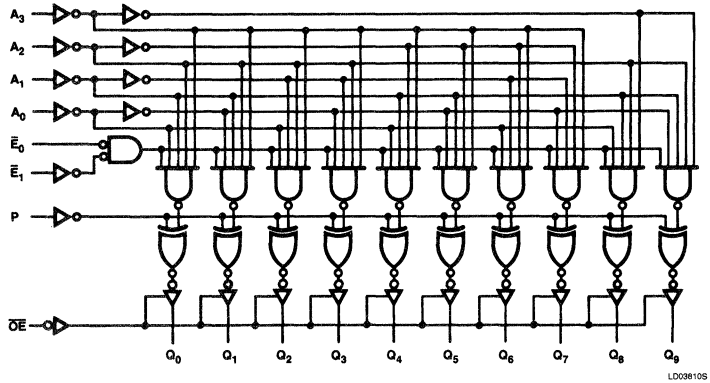


LOGIC DIAGRAM FOR 'F537

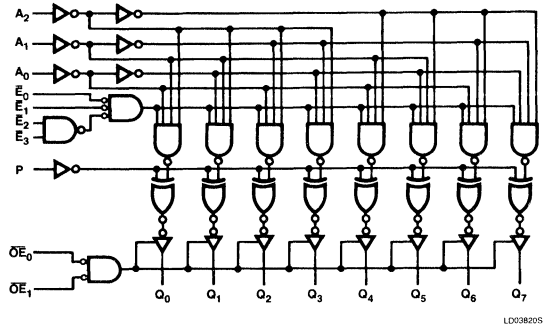


FUNCTION TABLE FOR 'F537

INPUTS							OUTPUTS										OPERATING MODE
$\overline{OE}$	$\overline{E}_0$	E_1	A_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	
H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High impedance
L	H	X	X	X	X	X	Outputs equal P input										Disable
L	X	L	X	X	X	X											
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Active HIGH Output (P = L)
L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L	
L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	
L	L	H	L	H	L	H	L	L	L	L	L	H	L	L	L	L	
L	L	H	L	H	H	L	L	L	L	L	L	L	H	L	L	L	
L	L	H	L	H	H	H	L	L	L	L	L	L	L	H	L	L	
L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	
L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	
L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	X	X	L	L	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	Active LOW Output (P = H)
L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H	
L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H	
L	L	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H	
L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	
L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H	
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L	
L	L	H	H	X	H	X	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H	

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance

LOGIC DIAGRAM FOR 'F538

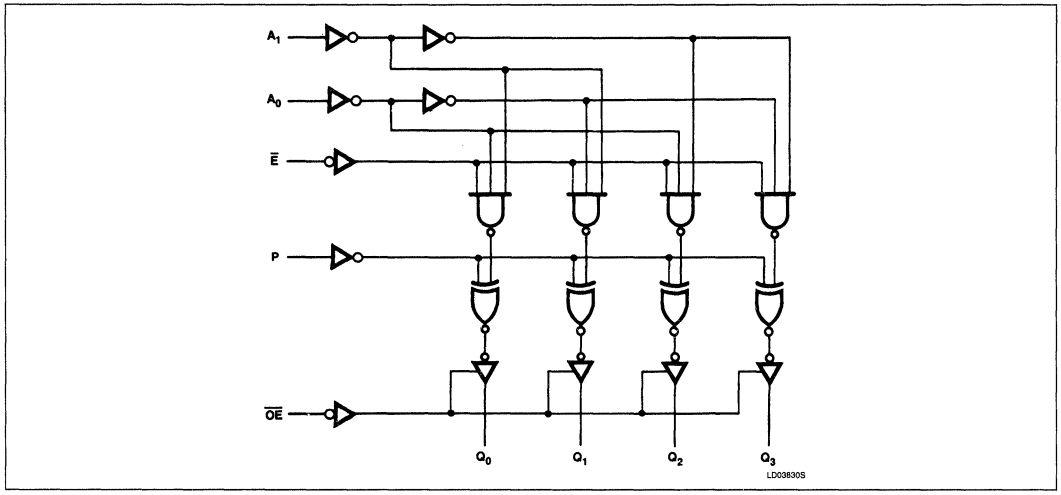


FUNCTION TABLE FOR 'F538

INPUTS									OUTPUTS								OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	High impedance
X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	L	H	X	X	X	X	X	X	Outputs equal P input								Disable
L	L	X	H	X	X	X	X	X									
L	L	X	X	L	X	X	X	X									
L	L	X	X	X	L	X	X	X									
L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	Active HIGH Output (P = L)
L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L	
L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L	
L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L	
L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	
L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L	
L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L	
L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H	
L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H	Active LOW Output (P = H)
L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance

LOGIC DIAGRAM FOR 'F539 (one half shown)



FUNCTION TABLE FOR 'F539

INPUTS				OUTPUTS				OPERATING MODE
$\overline{OE}$	E	A_1	A_0	Q_0	Q_1	Q_2	Q_3	
H	X	X	X	Z	Z	Z	Z	High impedance
L	H	X	X	$Q_n = P$				Disable
L	L	L	L	H	L	L	L	Active HIGH Output (P = L)
L	L	L	H	L	H	L	L	
L	L	H	L	L	L	H	L	
L	L	H	H	L	L	L	H	
L	L	L	L	L	H	H	H	Active LOW Output (P = H)
L	L	L	H	H	L	H	H	
L	L	H	L	H	H	L	H	
L	L	H	H	H	H	H	L	

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F537, 74F538, 74F539			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
			±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total) 'F537	V_{CC} = MAX	$A_0 - A_3 = \overline{E}_0$ = GND, $\overline{OE}$ = E_1 = P = 4.5V		44	66	mA
	Supply current (total) 'F538		$A_0 - A_3 = \overline{E}_0 = \overline{E}_1$ = GND, $\overline{OE}_0 = \overline{OE}_1 = E_2 = E_3$ = P = 4.5V		37	56	mA
	Supply current (total) 'F539		$A_{0n} - A_{3n}$ = E = GND, $\overline{OE}$ = P = 4.5V		40	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F537					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1	6.0 4.0	11.0 7.5	16.0 11.0	6.0 4.0	17.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ to Q_n	Waveform 2	5.0 4.0	8.5 6.5	14.5 9.0	5.0 4.0	15.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_1$ to Q_n	Waveform 2	6.0 5.0	11.0 10.0	16.0 14.0	6.0 5.0	17.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1	6.0 6.0	11.5 11.0	18.0 16.0	6.0 6.0	20.0 17.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	3.0 5.0	5.5 9.0	10.5 13.0	3.0 5.0	11.5 14.0	ns
t_{PHZ} t_{PLZ}	Output enable time from HIGH or LOW level $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	2.0 3.0	4.0 5.0	6.0 7.0	2.0 3.0	7.0 8.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F538					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1	6.0 4.0	11.0 7.5	16.0 11.0	6.0 4.0	17.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to Q_n	Waveform 2	5.0 4.0	8.5 6.5	15.0 9.0	5.0 4.0	16.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_2$ or $\overline{E}_3$ to Q_n	Waveform 2	6.0 5.0	11.0 10.0	16.0 14.0	6.0 5.0	17.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1	6.0 6.0	11.5 11.0	18.0 16.0	6.0 6.0	20.0 17.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	3.0 5.0	5.5 9.0	10.0 13.0	3.0 5.0	11.0 14.0	ns
t_{PHZ} t_{PLZ}	Output enable time from HIGH or LOW level $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	2.0 3.0	4.0 5.0	6.0 8.0	2.0 3.0	7.0 9.0	ns

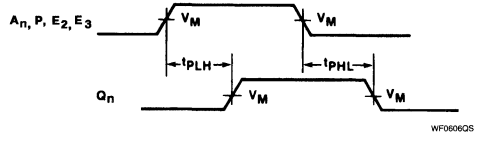
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

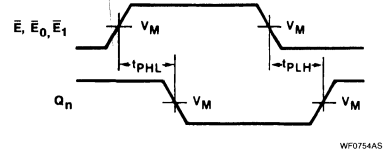
PARAMETER		TEST CONDITIONS	74F539					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1	9.0 4.0	14.5 9.5	18.5 12.0	9.0 4.0	19.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 2	5.5 4.0	12.0 7.5	16.0 9.5	5.5 4.0	17.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1	7.5 5.0	14.5 11.0	21.5 16.5	7.5 5.0	22.5 17.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	4.5 5.5	8.0 10.0	10.5 13.0	4.5 5.5	11.5 14.0	ns
t_{PHZ} t_{PLZ}	Output enable time from HIGH or LOW level $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	2.0 3.0	4.5 6.5	6.0 8.5	2.0 3.0	7.0 9.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

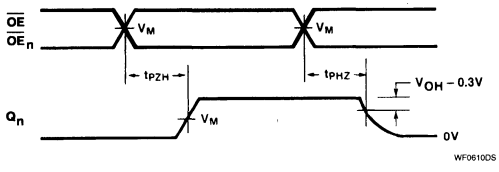
AC WAVEFORMS



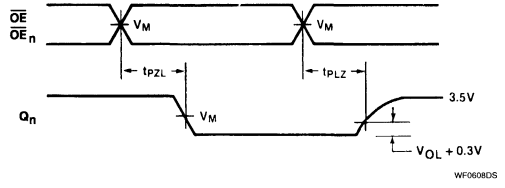
Waveform 1. Propagation Delay For Non-Inverting Outputs



Waveform 2. Propagation Delay For Inverting Outputs



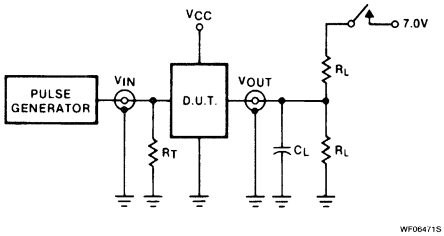
Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



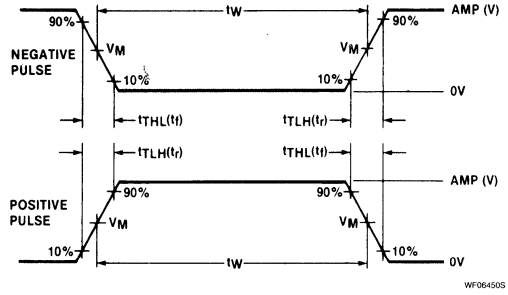
Waveform 5. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F540, 74F541
Buffers

'540 Octal Inverter Buffer (3-State)
'541 Octal Buffer (3-State)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20uA in HIGH and LOW states)**
- **Low power, light bus loading**
- **Functionally similar to the 'F240 and 'F244**
- **Provides ideal interface and increases fanout of MOS Microprocessors**
- **Efficient pinout to facilitate PC board layout**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION

The 'F540 and 'F541 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature input and outputs on opposite sides of the package to facilitate printed circuit board layout.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F540	3.5ns	58mA
74F541	5.5ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F540N, N74F541N
Plastic SOL-20	N74F540D, N74F541D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

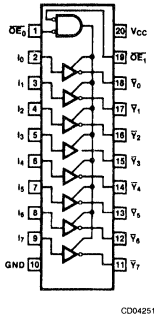
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_0$, $\overline{OE}_1$	3-State output enable inputs (active LOW)	1.0/0.033	20μA/20μA
$I_0 - I_7$	Data inputs	1.0/0.033	20μA/20μA
$\overline{Y}_0 - \overline{Y}_7$	Data outputs, 'F540	750/106.7	15mA/64mA
$Y_0 - Y_7$	Data outputs, 'F541		

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

PIN CONFIGURATION

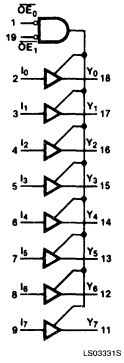
'540



CD04251S

LOGIC SYMBOL

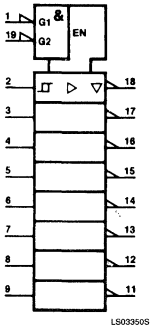
'540



LS03331S

LOGIC SYMBOL (IEEE/IEC)

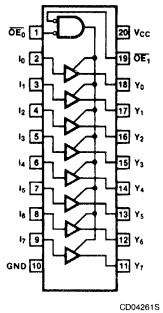
'540



LS03350S

PIN CONFIGURATION

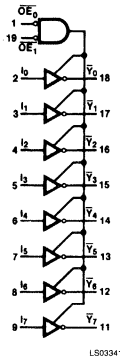
'541



CD04261S

LOGIC SYMBOL

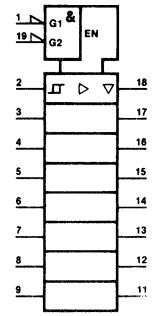
'541



LS03341S

LOGIC SYMBOL (IEEE/IEC)

'541



LS03360S

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE}_0$	$\overline{OE}_1$	I_n	Y_n	$\overline{Y}_n$
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER				TEST CONDITIONS[1]			74F540, 74F541			UNIT
							Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.35	.50	V
					I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current			V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current			V_{CC} = MAX, V_I = 0.5V				−1	−20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied			V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied			V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−2	−50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100	−150	−225	mA
I_{CC}	Supply current (total)	I_{CCH}	'F540	V_{CC} = MAX	I_n = $\overline{OE}_n$ = GND			22	30	mA
		I_{CCL}			I_n = 4.5V, $\overline{OE}_n$ = GND			58	75	mA
		I_{CCZ}			I_n = GND, $\overline{OE}_n$ = 4.5V			40	55	mA
		I_{CCH}	'F541		I_n = 4.5V, $\overline{OE}_n$ = GND			30	40	mA
		I_{CCL}			I_n = $\overline{OE}_n$ = GND			55	72	mA
		I_{CCZ}			I_n = GND, $\overline{OE}_n$ = 4.5V			45	58	mA

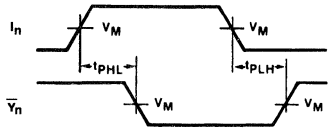
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

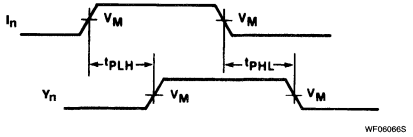
PARAMETER			TEST CONDITIONS	74F540, 74F541					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
'F540	t_{PLH} / t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns
	t_{PZH} / t_{PZL}	Output enable time to HIGH or LOW	Waveform 3 Waveform 4	3.0 4.0	5.5 7.5	7.5 9.5	3.0 4.0	8.0 10.0	ns
	t_{PHZ} / t_{PLZ}	Output disable time from HIGH or LOW	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns
'F541	t_{PLH} / t_{PHL}	Propagation delay I_n to Y_n	Waveform 2	2.5 3.5	5.0 6.0	6.5 7.0	2.5 3.0	7.0 7.5	ns
	t_{PZH} / t_{PZL}	Output enable time to HIGH or LOW	Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.0 8.5	3.0 3.0	7.5 9.5	ns
	t_{PHZ} / t_{PLZ}	Output disable time from HIGH or LOW	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

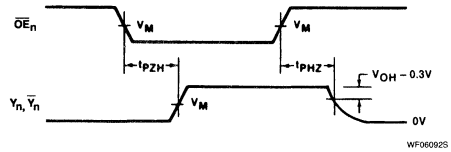
AC WAVEFORMS



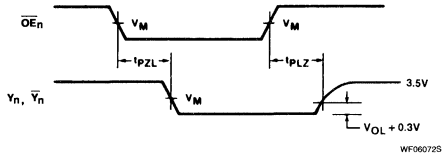
Waveform 1. Propagation Delay Data To Output For 'F540



Waveform 2. Propagation Delay Data To Output For 'F540



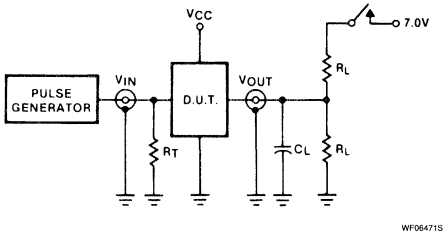
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



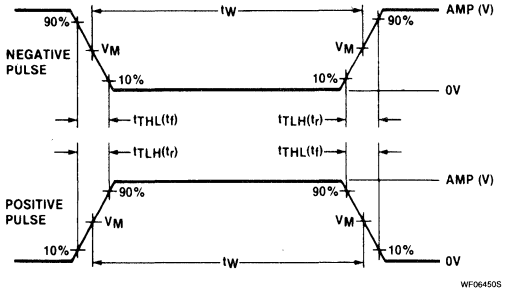
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F543, 74F544
Transceivers

Octal Registered Transceiver, Non-Inverting (3-State)
Octal Registered Transceiver, Inverting (3-State)
Preliminary Specification

Logic Products

FEATURES

- **8-bit Octal Transceiver**
- **'F543 Non-Inverting**
  'F544 Inverting
- **Back-to-Back Registers for storage**
- **Separate controls for Data flow in each direction**
- **A outputs sink 20mA and source 15mA**
- **B outputs sink 64mA and source 15mA**
- **24 pin plastic slim DIP (300 mil) package**

DESCRIPTION

The 'F543 and 'F544 Octal Registered Transceivers contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. While the 'F543 has noninverting data path, the 'F544 inverts data in both direction. The A outputs are guaranteed to sink 20mA while the B outputs are rated for 64mA.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	5.5ns	80mA
74F544	6.0ns	80mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F543N, N74F544N
Plastic SOL-24	N74F543D, N74F544D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$ ('F543)	Port A, 3-State inputs	3.5/1.08	70μA/0.65mA
$B_0 - B_7$ ('F543)	Port B, 3-State inputs	3.5/1.08	70μA/0.65mA
$\overline{A}_0 - \overline{A}_7$ ('F544)	Port $\overline{A}$, 3-State inputs	3.5/1.08	70μA/0.65mA
$\overline{B}_0 - \overline{B}_7$ ('F544)	Port $\overline{B}$, 3-State inputs	3.5/1.08	70μA/0.65mA
$\overline{OEAB}$	A-to-B output enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OEBA}$	A-to-B output enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{EAB}$	A-to-B enable input (active LOW)	1.0/2.0	20μA/1.2mA
$\overline{EBA}$	A-to-B enable input (active LOW)	1.0/2.0	20μA/1.2mA
$\overline{LEAB}$	A-to-B latch enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{LEBA}$	A-to-B latch enable input (active LOW)	1.0/1.0	20μA/0.6mA
$A_0 - A_7$ ('F543)	Port A, 3-State outputs	50/40	1.0mA/24mA
$B_0 - B_7$ ('F543)	Port B, 3-State outputs	750/106.7	15mA/64mA
$\overline{A}_0 - \overline{A}_7$ ('F544)	Port $\overline{A}$, 3-State outputs	50/40	1.0mA/24mA
$\overline{B}_0 - \overline{B}_7$ ('F544)	Port $\overline{B}$, 3-State outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

FUNCTIONAL DESCRIPTION

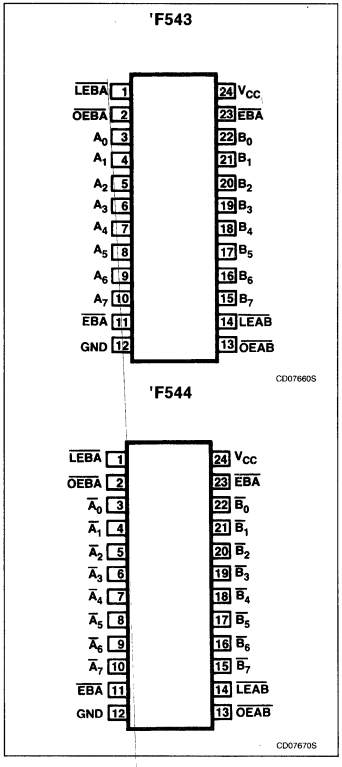
The 'F543 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) Input must be LOW in order to enter data from $A_0 - A_7$ or take data from $B_0 - B_7$, as indicated in the Function Table. With $\overline{EAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition fof the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both LOW, the 3-State B output buffers are active and reflects the data present at the loutput of the A latches. Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

FUNCTION TABLE for 'F543 and 'F544

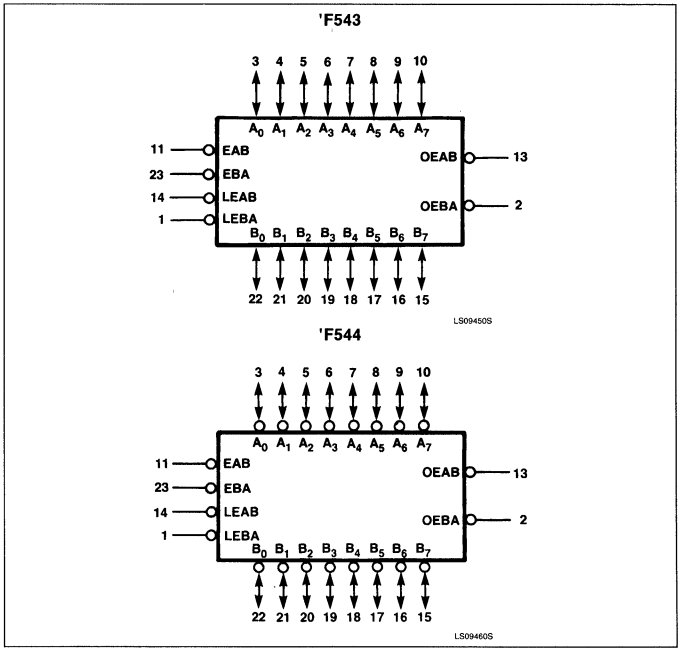
INPUTS				OUTPUTS		STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	Data	'F543	'F544	
H	X	X	X	Z	Z	Outputs disabled
L	H	L	I	Z	Z	Outputs disabled
L	H	L	h	Z	Z	Data latched
L	L	H	I	L	H	Data latched
L	L	H	h	H	L	
L	L	L	L	L	H	Transparent
L	L	L	H	H	L	

H = HIGH voltage level
h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
L = LOW voltage level
I = LOW state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
X = Don't care
Z = HIGH impedance state

PIN CONFIGURATION

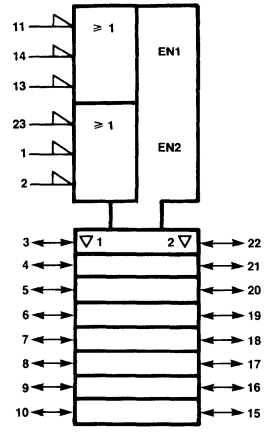


LOGIC SYMBOL



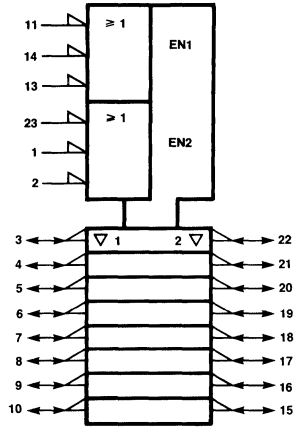
LOGIC SYMBOL (IEEE/IEC)

'F543



LS09480S

'F544



LS09470S

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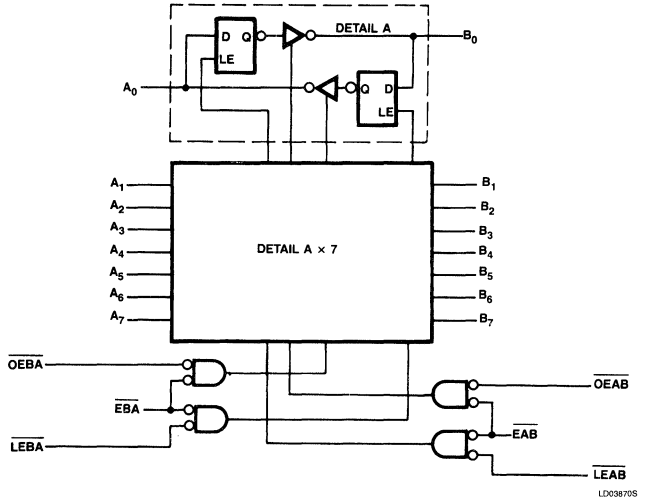
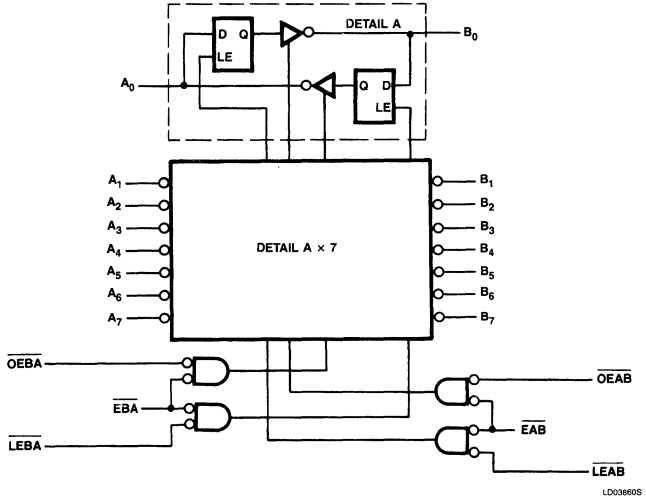
LOGIC DIAGRAM FOR 'F543



NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

LOGIC DIAGRAM FOR 'F544



NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER		74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$	48	mA
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$			−1	mA
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$			−15	mA
I_{OL}	LOW-level output current	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$			24	mA
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F543, 74F544			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$		I_{OL} = 48mA	±10%V_{CC}		.40	.55	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$, $\overline{EAB}$, $\overline{EBA}$, $\overline{LEAB}$, $\overline{LEBA}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		Others	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	Others	V_{CC} = MAX, V_I = 0.5V					−0.6	mA
		$\overline{EAB}$, $\overline{EBA}$						−1.2	mA
$I_{IH} + I_{OZH}$	Off-state current HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					70	μA
$I_{IL} + I_{OZL}$	Off-state current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−600	μA
I_{OS}	Short circuit output current[3]	$A_0 - A_7$, $\overline{A}_0 - \overline{A}_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$, $\overline{B}_0 - \overline{B}_7$				−100		−225	mA
I_{CC}	Supply current (total)	'F543	I_{CCH}	V_{CC} = MAX			67	100	mA
			I_{CCL}				83	125	mA
			I_{CCZ}				83	125	mA
I_{CC}	Supply current (total)	'F544	I_{CCH}	V_{CC} = MAX			70	105	mA
			I_{CCL}				85	130	mA
			I_{CCZ}				83	125	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

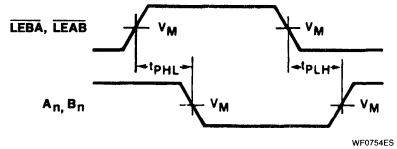
PARAMETER			TEST CONDITIONS	74F543, 74F544					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	'F543	Waveform 2	3.0 3.0	5.5 5.0	7.5 6.5	3.0 3.0	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{B}_n$ or $\overline{B}_n$ to $\overline{A}_n$	'F544	Waveform 2	3.0 3.0	7.0 5.0	9.5 6.5	3.0 3.0	10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to A_n	'F543	Waveform 1	4.5 4.5	8.5 8.5	11.0 11.0	4.5 4.5	12.5 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to $\overline{A}_n$	'F544	Waveform 2	6.0 4.0	10.0 7.0	13.0 9.5	6.0 4.0	14.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	'F543	Waveform 1	4.5 4.5	8.5 8.5	11.0 11.0	4.5 4.5	12.5 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to $\overline{B}_n$	'F544	Waveform 2	6.0 4.0	10.0 7.0	13.0 9.5	6.0 4.0	12.5 12.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{EBA}$ or $\overline{EAB}$ to A_n or B_n	'F543	Waveform 4 Waveform 5	3.0 4.0	7.0 7.5	9.0 10.5	3.0 4.0	10.0 12.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$ $\overline{EBA}$ or $\overline{EAB}$ to $\overline{A}_n$ or $\overline{B}_n$	'F544	Waveform 4 Waveform 5	3.0 4.0	7.0 7.5	9.0 10.5	3.0 4.0	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{EBA}$ or $\overline{EAB}$ to A_n or B_n	'F543	Waveform 4 Waveform 5	2.5 2.5	6.0 5.5	8.0 7.5	2.5 2.5	9.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$ $\overline{EBA}$ or $\overline{EAB}$ to $\overline{A}_n$ or $\overline{B}_n$	'F544	Waveform 4 Waveform 5	2.5 2.5	6.0 5.5	8.0 7.5	2.5 2.5	9.0 8.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

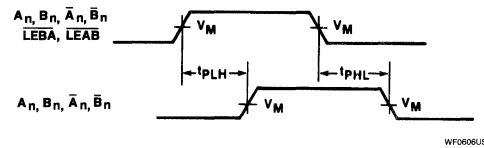
AC SET-UP REQUIREMENTS

PARAMETER			TEST CONDITIONS	74F543, 74F544					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$ $V_{CC} = +5.0V + 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW A_n or B_n to $\overline{LEAB}$ or $\overline{LEBA}$ A_n or B_n to $\overline{EAB}$ or $\overline{EBA}$	'F543	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Hold time, HIGH or LOW A_n or B_n to $\overline{LEAB}$ or $\overline{LEBA}$ A_n or B_n to $\overline{EAB}$ or $\overline{EBA}$			3.0 3.0			3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{A}_n$ or $\overline{B}_n$ to $\overline{LEAB}$ or $\overline{LEBA}$ $\overline{A}_n$ or $\overline{B}_n$ to $\overline{EAB}$ or $\overline{EBA}$	'F544		3.0 3.0			3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Hold time, HIGH or LOW $\overline{A}_n$ or $\overline{B}_n$ to $\overline{LEAB}$ or $\overline{LEBA}$ $\overline{A}_n$ or $\overline{B}_n$ to $\overline{EAB}$ or $\overline{EBA}$			3.0 3.0			3.0 3.0		ns

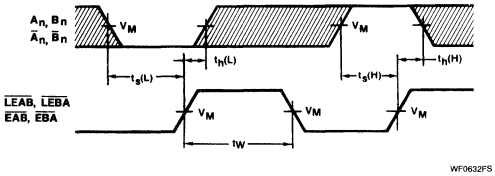
AC WAVEFORMS



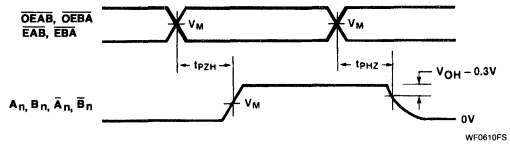
Waveform 1. Propagation Delay For Inverting Outputs



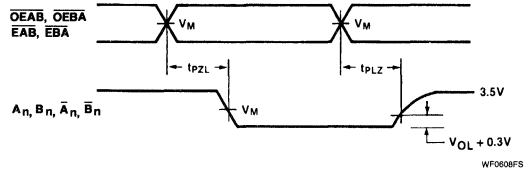
Waveform 2. Propagation Delay For Non-Inverting Outputs



Waveform 3. Data And Select Set-up And Hold Times



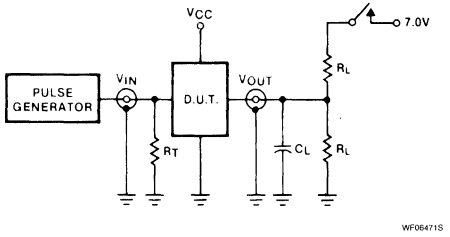
Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



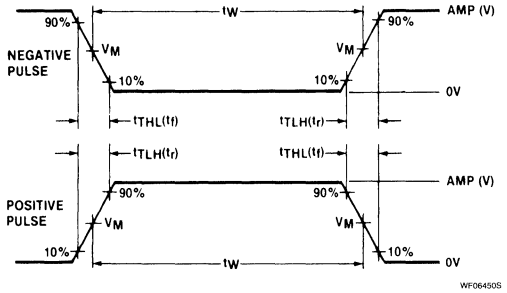
Waveform 5. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to changed for predicatable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

6

Signetics

FAST 74F545
Transceivers

Octal Bidirectional Transceiver
(With 3-State Inputs/Outputs)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (70μA in HIGH and LOW states)**
- **Higher drive than 8304**
- **8-bit bidirectional data flow reduces system package count**
- **3-State inputs/outputs for interfacing with bus-oriented systems**
- **20mA and 64mA bus drive capability on A and B ports, respectively**
- **Transmit/Receive and Output Enable simplify control logic**
- **Pin for pin replacement for Intel 8286**

DESCRIPTION

The 'F545 is an 8-bit, 3-State, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 20mA bus drive capability on the A ports and 64mA bus drive capability on the B ports.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F545	4.0ns	87mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F545N
Plastic SOL-20	N74F545D

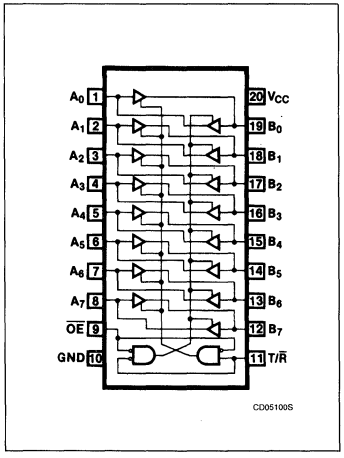
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

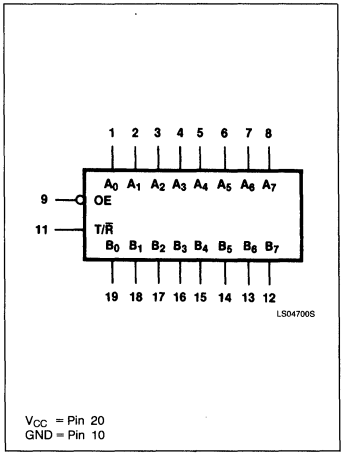
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$, $B_0 - B_7$	Data inputs	3.50/0.117	70μA/70μA
$\overline{OE}$	Output enable input (active LOW)	2.0/0.067	40μA/40μA
$T/\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
$A_0 - A_7$	Port A 3-state outputs	150/40	3mA/24mA
$B_0 - B_7$	Port B 3-state outputs	750/107	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

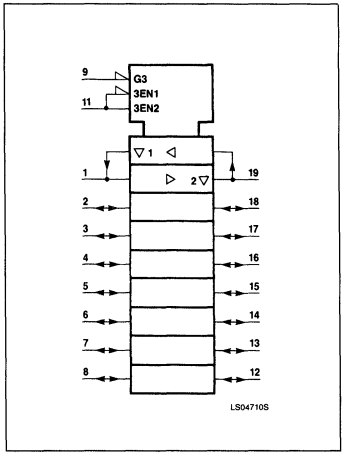
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



One input, Transmit/Receive ($T/\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a 3-state condition.

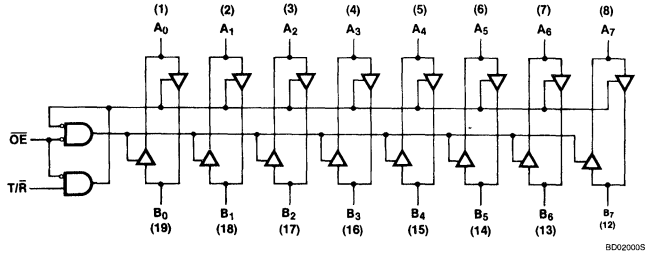
The 'F545 performs the same function as the 'F245 the only difference being package pin assignments.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH voltage level
L = LOW voltage level
X = Immaterial
Z = High impedance

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	LOW-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F545			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$A_0 - A_7$, $B_0 - B_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
		$B_0 - B_7$		I_{OL} = 48mA	±10%V_{CC}		.40	.55	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input voltage at maximum input voltage	$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
		$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	μA
I_{IL}	LOW-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					−40	μA
I_{OZH} + I_{IH}	Off-state current HIGH-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	μA
I_{OZL} + I_{IH}	Off-state current LOW-level volt age applied		V_{CC} = MAX, V_I = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$				−100		−225	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX	T/$\overline{R}$ = $A_0 - A_7$ = 4.5V; $\overline{OE}$ = GND			77	90	mA
		I_{CCL}		$\overline{OE}$ = T/$\overline{R}$ = $B_0 - B_7$ = GND			96	120	mA
		I_{CCZ}		$\overline{OE}$=4.5V; T/$\overline{R}$ = $B_0 - B_7$ = GND			89	110	mA

NOTES:

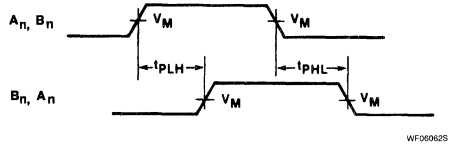
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

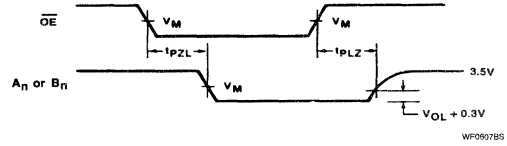
PARAMETER		TEST CONDITIONS	74F545					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	1.5	3.5	5.5	1.5	6.5	ns
t_{PHL}	A_n to B_n or B_n to A_n	Waveform 1	2.5	4.5	6.5	2.5	7.0	
t_{PZH}	Output enable time	Waveform 2	6.0	8.5	10.5	6.0	11.0	ns
t_{PZL}	to HIGH or LOW level	Waveform 3	5.5	8.0	9.5	5.5	10.0	
t_{PHZ}	Output disable time from	Waveform 2	2.5	5.0	7.0	2.5	8.0	ns
t_{PLZ}	HIGH or LOW level	Waveform 3	2.0	4.5	6.5	2.0	7.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

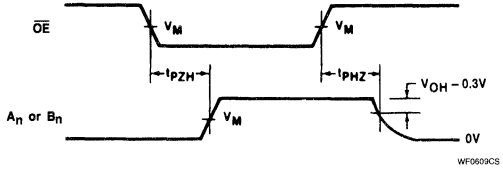
AC WAVEFORMS



Waveform 1. For Non-Inverting Outputs



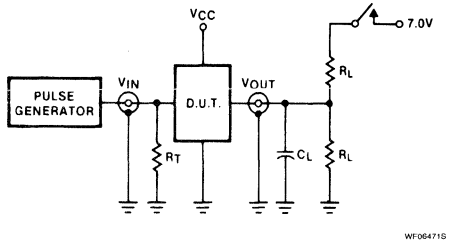
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



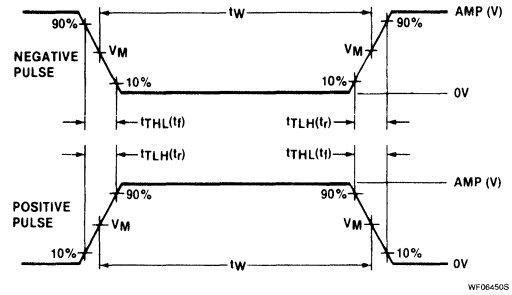
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

Logic Products

FAST 74F547
Decoder/Demultiplexer

Octal Decoder/Demultiplexer With Address Latches And Acknowledge

Preliminary Specification

FEATURES

- **3-to-8 line address decoder**
- **Address storage latches**
- **Multiple enables for address extension**
- **Open-Collector Acknowledge output**

DESCRIPTION

The 'F547 is a 3-to-8 line address decoder with latches for address storage. Designed primarily to simplify multiple-chip selection in a microprocessor system, it contains one active-LOW and two active-HIGH Enables to conserve address space. Also included is an active-LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F547	8.0ns	17mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F547N
Plastic SOL-20	N74F547D

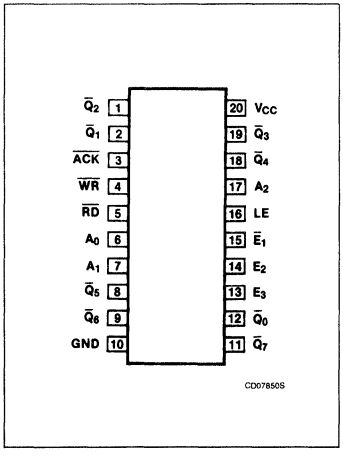
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

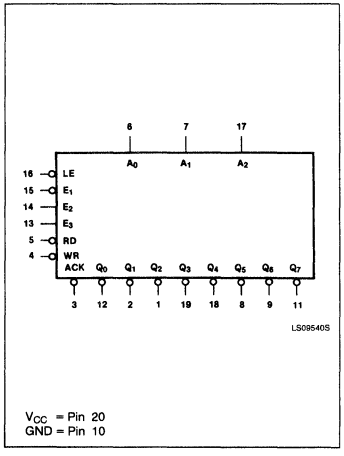
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_2$	Output select address input	1.0/1.0	20μA/0.6mA
$\overline{E}_1$	Chip enable input (active LOW)	1.0/1.0	20μA/0.6mA
E_2, E_3	Chip enable inputs	1.0/1.0	20μA/0.6mA
LE	Latch enable input	1.0/1.0	20μA/0.6mA
$\overline{RD}$	Read acknowledge input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{WR}$	Write acknowledge input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0 - \overline{Q}_7$	Decoder outputs (active LOW)	50/33.3	1mA/20mA
$\overline{ACK}$	Open-collector acknowledge output (active LOW)	OC*/33.3	OC*/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. *OC = Open-collector.

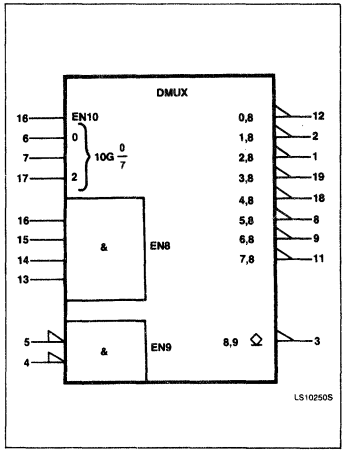
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



For applications in which the separation of latch enable and chip enable functions is not required, LE and $\overline{E}_1$ can be tied together such that when HIGH the outputs are OFF and the latches are transparent, and when LOW the latches are storing and the selected output is enabled.

The open-collector Acknowledge ($\overline{ACK}$) output is normally HIGH (i.e. OFF) and goes LOW when $\overline{E}_1$, E_2 and E_3 are all active and either the READ ($\overline{RD}$) or Write ($\overline{WR}$) input is LOW, as indicated in the Acknowledge Function Table.

FUNCTION TABLE (Decoder*)

INPUTS			OUTPUTS							
A_2	A_1	A_0	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

* Assuming $\overline{E}_1$ = LOW and $E_2 = E_3$ = HIGH

FUNCTION TABLE (Acknowledge)

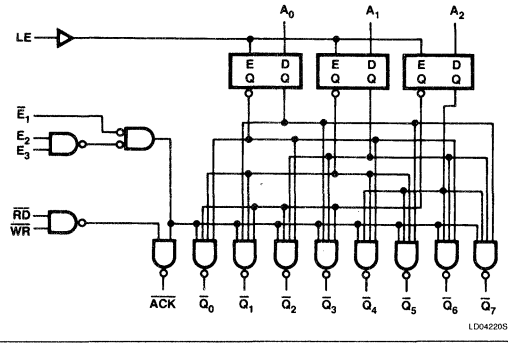
INPUTS					OUTPUT
$\overline{E}_1$	E_2	E_3	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
L	H	H	H	H	H
L	H	H	L	X	L
L	H	H	X	L	L

FUNCTION TABLE (Latch and Output Status)

INPUTS				LATCH STATUS	DECODER OUTPUTS
$\overline{E}_1$	E_2	E_3	LE		
L	H	H	H	Transparent	Address inputs decoded ($\overline{Q}_n$ = LOW)
L	H	H	L	Storing	Latched address decoded ($\overline{Q}_n$ = LOW)
H	X	X	H	Transparent	$\overline{Q}_n$ = HIGH
H	X	X	L	Storing	
X	L	X	H	Transparent	
X	L	X	L	Storing	
X	X	L	H	Transparent	
X	X	L	L	Storing	

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	$\overline{ACK}$ only			4.5	V
I_{OH}	HIGH-level output current	Except $\overline{ACK}$			−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F547			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	$\overline{ACK}$ only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	Except $\overline{ACK}$	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			17	25	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

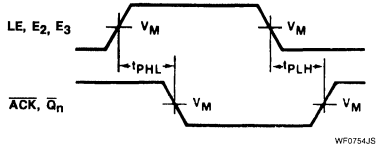
PARAMETER	TEST CONDITIONS	74F547					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A_n to $\overline{Q}_n$	Waveform 3	4.0 5.0	7.0 9.0	9.0 12.0	4.0 5.0	10.0 13.0	ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{E}_1$ to $\overline{Q}_n$	Waveform 2	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	9.5 9.5	ns ns
t_{PLH} Propagation delay t_{PHL} LE to $\overline{Q}_n$	Waveform 1	4.0 9.0	7.5 14.5	9.5 18.0	4.0 9.0	10.5 19.0	ns ns
t_{PLH} Propagation delay t_{PHL} E_2 or E_3 to $\overline{Q}_n$	Waveform 1	5.0 5.0	8.5 8.5	11.0 11.0	5.0 5.0	12.0 12.0	ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{E}_1$, $\overline{RD}$, or $\overline{WR}$ to $\overline{ACK}$	Waveform 2	6.5 4.0	11.0 7.5	14.0 9.5	6.5 4.0	15.0 10.5	ns ns
t_{PLH} Propagation delay t_{PHL} E_2 or E_3 to $\overline{ACK}$	Waveform 1	8.0 5.0	13.0 8.5	16.5 11.0	8.0 5.0	17.5 12.0	ns ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

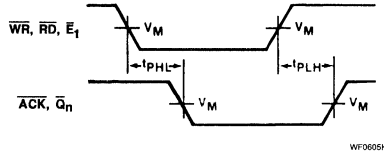
AC SET-UP REQUIREMENTS

PARAMETER	TEST CONDITIONS	74F547					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
$t_s(H)$ Set-up time, HIGH or LOW $t_s(L)$ A_n to LE	Waveform 4	5.0 5.0			5.0 5.0		ns ns
$t_h(H)$ Hold time, HIGH or LOW $t_h(L)$ A_n to LE	Waveform 4	6.0 6.0			6.0 6.0		ns ns
$t_w(H)$ LE pulse width, HIGH	Waveform 4	6.0			6.0		ns

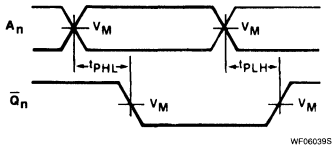
AC WAVEFORMS



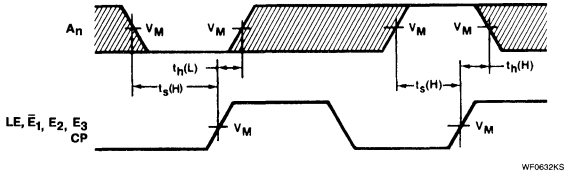
Waveform 1. Propagation Delay For Chip Enable Inputs (E_2, E_3) And Latch Enable Input (LE) To Write Acknowledge ($\overline{ACK}$) And Decoder (Q_n) Outputs



Waveform 2. Propagation Delay For Chip Enable Input (E_1) To Decoder Outputs (Q_n) And Write Acknowledge Inputs ($\overline{WR}$, $\overline{RD}$) To Acknowledge Output ($\overline{ACK}$)



Waveform 3. Propagation Delay For Output Select Address Input (A_n) To Decoder Outputs ($\overline{Q}_n$)

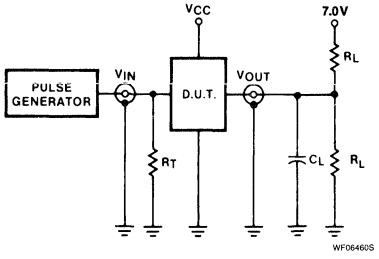


Waveform 4. Data Set-up And Hold Times For Output Select Address Inputs (A_n) To Latch Enable Inputs (LE) And Chip Enable Inputs ($\overline{E}_1$, E_2, E_3)

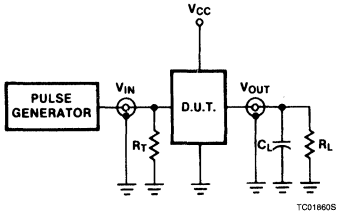
NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable performance.

6

TEST CIRCUITS AND WAVEFORMS



Test Circuit For Open-Collector Outputs



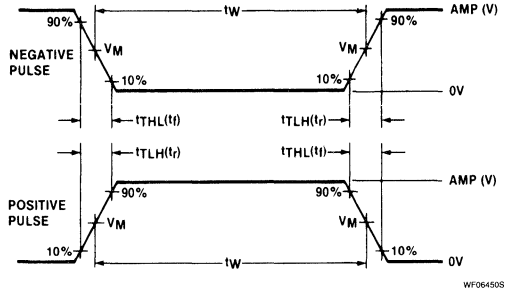
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F548
Decoder/Demultiplexer

Octal Decoder/Demultiplexer with Acknowledge
Preliminary Specification

FEATURES

- **3-to-8 line address decoder**
- **Multiple enables for address extension**
- **Open-Collector Acknowledge output**
- **Active-LOW Decoder outputs**

DESCRIPTION

The 'F548 is a 3-to-8 line address decoder with four Enable inputs. Two of the Enables are active-LOW and two are active-HIGH for maximum addressing versatility. Also provided is an active-LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

When enabled, the 'F548 accepts the $A_0 - A_2$ address inputs and decodes them to select one of eight active-LOW mutually exclusive outputs, as shown in the Decoder Function Table. When one or more Enables is active, all decoder outputs are HIGH. Thus, the 'F548 can be used as a demultiplexer by applying data to one of the Enables.

The open-collector Acknowledge ($\overline{ACK}$) output is normally HIGH (i.e. OFF) and goes LOW when the Enables are all active and either the READ ($\overline{RD}$) or Write ($\overline{WR}$) input is LOW, as indicated in the Acknowledge Function Table.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F548	7.0 ns	16mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F548N
Plastic SOL-20	N74F548D

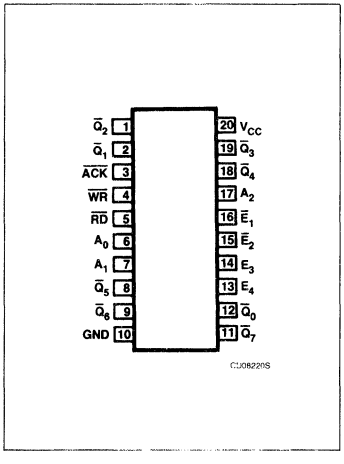
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

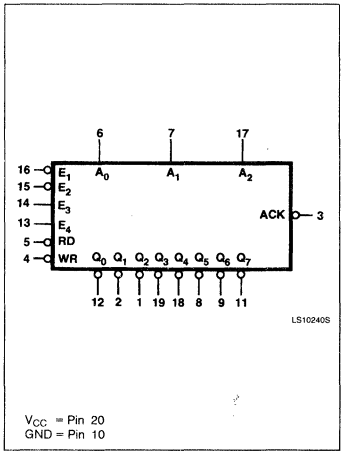
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_2$	Output select address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_1$, $\overline{E}_2$	Chip enable inputs (active LOW)	1.0/1.0	20μA/0.6mA
E_3, E_4	Chip enable inputs	1.0/1.0	20μA/0.6mA
$\overline{RD}$	Read acknowledge input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{WR}$	Write acknowledge input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0 - \overline{Q}_7$	Decoder outputs (active LOW)	50/33	1mA/20mA
ACK	Open-collector acknowledge output (active LOW)	OC*/33	OC*/20mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. *OC = Open-collector.

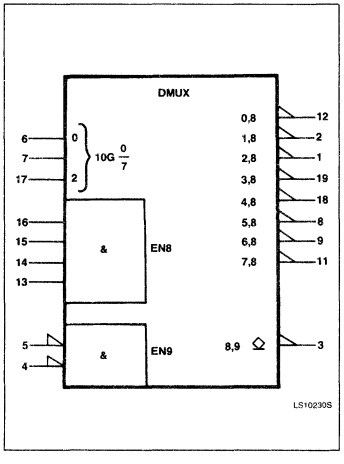
PIN CONFIGURATION



LOGIC SYMBOL

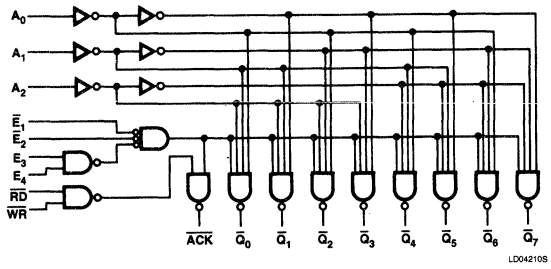


LOGIC SYMBOL (IEEE/IEC)



Decoder/Demultiplexer FAST 74F548

LOGIC DIAGRAM



NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTION TABLE (Decoder)

INPUTS							OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	A_2	A_1	A_0	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
H	X	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

FUNCTION TABLE (Acknowledge)

INPUTS						OUTPUT
$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	H	H	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage	$\overline{ACK}$ only			4.5	V
I_{OH}	HIGH-level output current	Except $\overline{ACK}$			−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F548			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	$\overline{ACK}$ only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OH}	HIGH-level output voltage	Except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	Except $\overline{ACK}$	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			16	21	mA

NOTES:

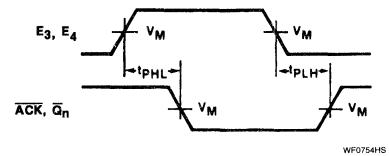
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

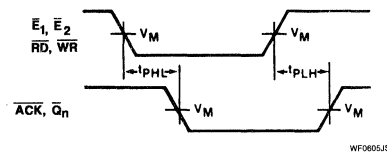
PARAMETER		TEST CONDITIONS	74F548					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 3	3.0 5.0	5.5 8.0	7.5 10.5	3.0 5.0	8.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_1$ or $\overline{E}_2$ to Q_n	Waveform 2	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	9.5 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_3$ or $\overline{E}_4$ to Q_n	Waveform 1	5.0 5.0	8.5 8.5	11.0 11.0	5.0 5.0	12.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay E_1 or E_2 to $\overline{ACK}$	Waveform 1	6.5 4.0	11.0 7.5	14.0 9.5	6.5 4.0	15.0 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay E_3 or E_4 to $\overline{ACK}$	Waveform 2	8.0 5.0	13.0 8.5	16.5 11.0	8.0 5.0	17.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	Waveform 1	5.5 3.0	10.0 5.0	12.5 6.5	5.5 3.0	13.5 7.5	ns ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

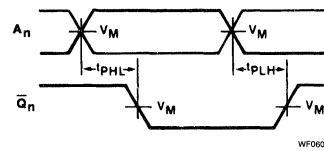
AC WAVEFORMS



Waveform 1. Propagation Delay For Chip Enable Inputs (E_3, E_4) To Write Acknowledge ($\overline{ACK}$) And Decoder (Q_n) Outputs



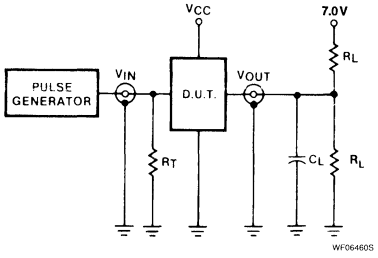
Waveform 2. Propagation Delay For Chip Enable Inputs ($\overline{E}_1$, $\overline{E}_2$) To Decoder Outputs ($\overline{Q}_n$) And Write Acknowledge Output ($\overline{ACK}$)



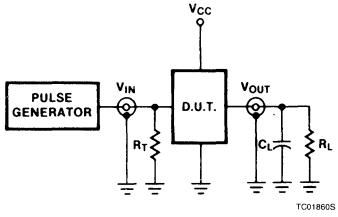
Waveform 3. Propagation Delays For Output Select Address Input (A_n) To Decoder Outputs ($\overline{Q}_n$)

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUITS AND WAVEFORMS



Test Circuit For Open-Collector Outputs



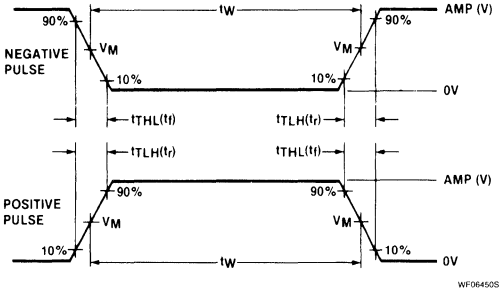
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

Logic Products

FAST 74F563, 74F564
Latch/Flip-Flop

'F563 Octal Transparent Latch (3-State)
'F564 Octal D Flip-Flop (3-State)
Preliminary Specification

FEATURES

- **'F563 is broadside pinout version or 'F533**
- **'F564 is broadside pinout version of 'F534**
- **Inputs and outputs on opposite side of package allow easy interface to microprocessors**
- **Useful as an Input or Outport for microprocessors**
- **3-State Outputs for Bus Interfacing**
- **Common Output Enable**
- **'F573 and 'F574 are Non-Inverting versions of 'F563 and 'F564 respectively**
- **These are High Speed replacements for 8TS807 and 8TS808**

DESCRIPTION

The 'F563 is an octal transparent latch coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F563	6.0ns	41mA
74F564	6.6ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F563N, F74F564N
Plastic SOL-20	N74F563D, N74F564D

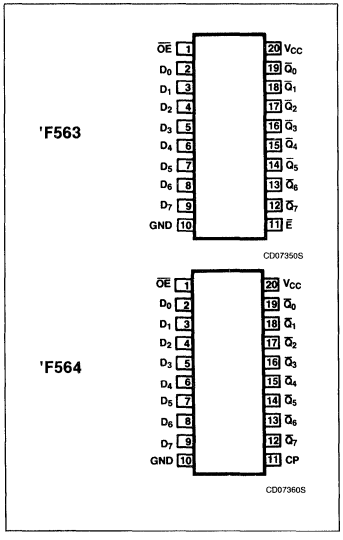
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

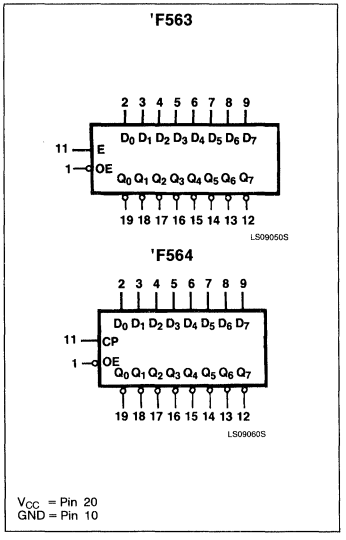
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$ ('F563 & 'F564)	Data inputs	1.0/1.0	20μA/0.6mA
E ('F563)	Latch enable input (active HIGH))	1.0/1.0	20μA/0.6mA
$\overline{OE}$ ('F563 & 'F564)	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
CP ('F564)	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0 - \overline{Q}_7$ ('F563 & 'F564)	3-State outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

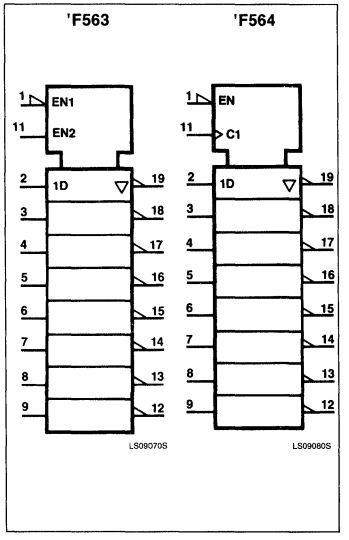
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Latch/Flip-Flop

FAST 74F563, 74F564

The 'F563 is functionally identical to the 'F533 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors

The data on the D inputs are transferred to the latch outputs when the latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the HIGH-to-LOW enable transition.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance 'off' state, which means they will neither drive nor load the bus.

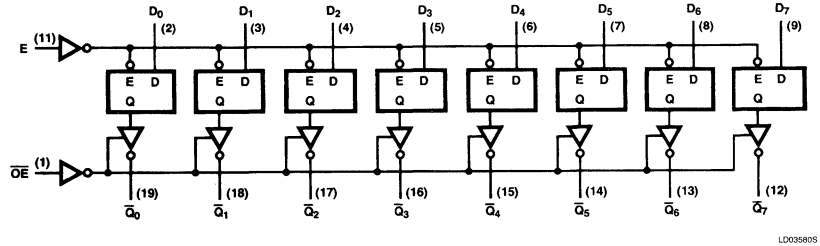
The 'F564 is an 8-bit edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The F564 is functionally identical to the 'F534 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause the clocking operation.

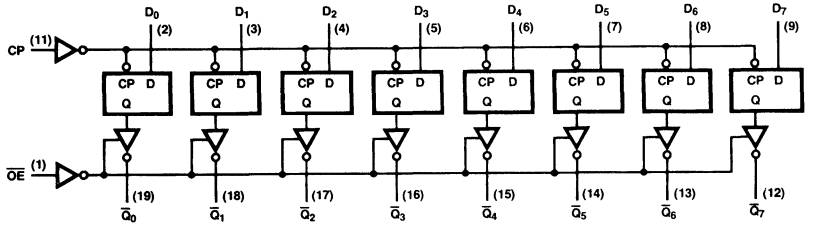
The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses. MOS memories, or MOS microprocessors. The active-LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance 'off' state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 'F563



V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 'F564



V_{CC} = Pin 20
GND = Pin 10

MODE SELECT — FUNCTION TABLE, 'F563

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$\overline{Q}_0 - \overline{Q}_7$
Enable and register	L	H	X	L	H
	L	H	X	H	L
Latch and read register	L	L	L	L	H
	L	L	H	H	L
Latch register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

MODE SELECT — FUNCTION TABLE, 'F563

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0 - \overline{Q}_7$
Load and read register	L	H	X	L	H
	L	H	X	H	L
Disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
X = Don't care
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F563, 74F564			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_o = 2.7V			2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−90	−150	mA
I_{CC}	Supply current (total)	'F563	V_{CC} = MAX			41	61	mA
		'F564				55	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. 'F633 measure I_{CCZ} with $\overline{OE}$ input at 4.5V, D_n and E inputs at ground and all outputs open.
   'F634 measure I_{CCZ} with $\overline{OE}$ inputs at 4.5V and D_n inputs at ground and all outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

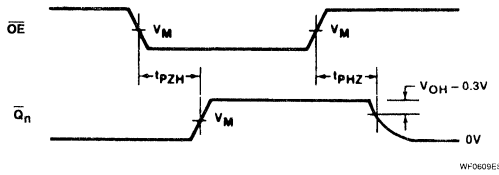
PARAMETER			TEST CONDITIONS	74F563, 74F564					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			T_A, V_{CC} Comp'l $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	'F564	Waveform 3	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay Data to output	'F563	Waveform 6	4.0 3.0	6.9 5.2	9.0 7.0	4.0 3.0	10 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	'F563	Waveform 7	5.0 3.0	8.5 5.6	11 7.0	5.0 3.0	13 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	'F564	Waveform 3	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10 10	ns
t_{PZH} t_{PZL}	Enable time to HIGH level Enable time to LOW level	'F563	Waveform 1 Waveform 2	2.0 2.0	7.7 5.1	10 6.5	2.0 2.0	11 7.5	ns
t_{PHZ} t_{PLZ}	Disable time from HIGH level Disable time from LOW level	'F563	Waveform 1 Waveform 2	2.0 2.0	4.7 4.1	6.0 5.5	2.0 2.0	7.0 6.5	ns
t_{PZH} T_{PZL}	Enable time to HIGH level Enable time to LOW level	'F564	Waveform 1 Waveform 2	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Disable time from HIGH level Disable time from LOW level	'F564	Waveform 1 Waveform 2	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 6.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

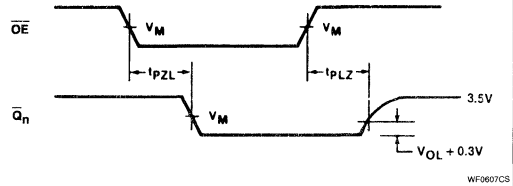
AC SET-UP REQUIREMENTS

PARAMETER			TEST CONDITIONS	74F563, 74F564					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, Data to Enable, HIGH or LOW	'F563	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, Data to Enable, HIGH or LOW	'F563	Waveform 5	3.0 3.0			3.0 3.0		ns
$t_W(H)$	Enable pulse width HIGH	'F563	Waveform 5	6.0			6.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, Data to Clock, HIGH or LOW	'F564	Waveform 4	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, Data to Clock, HIGH or LOW	'F564	Waveform 4	2.0 2.0			2.0 2.0		ns
$t_W(H)$ $t_W(L)$	HIGH or LOW	'F564	Waveform 3	5.0 5.0			7.0 6.0		ns

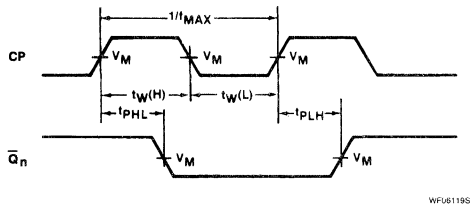
AC WAVEFORMS



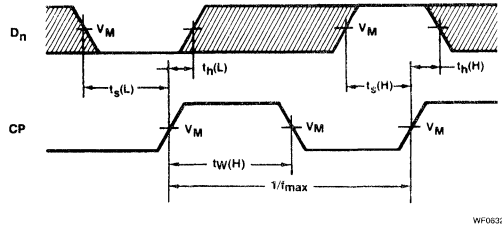
Waveform 1. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



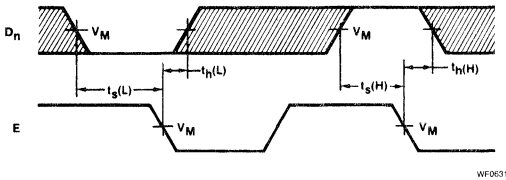
Waveform 2. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



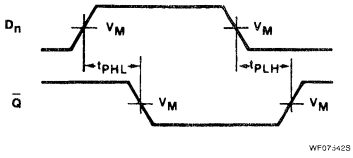
Waveform 3. Clock To Output Delays And Clock Pulse Width



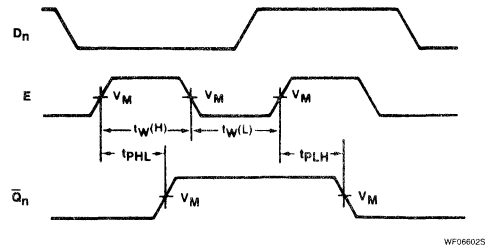
Waveform 4. Data Set-up And Hold Times



Waveform 5. Data Set-up And Hold Times



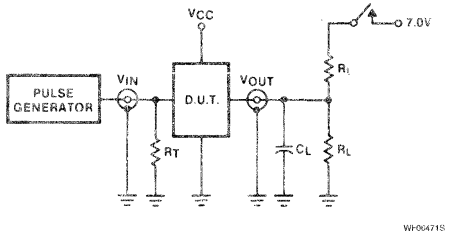
Waveform 6. Data To Output Delays



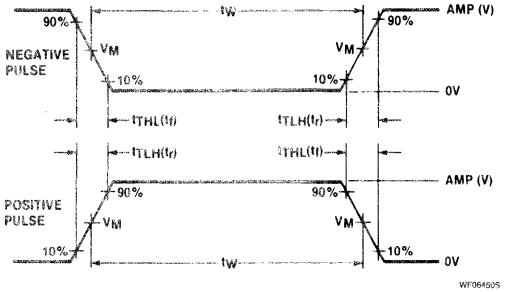
Waveform 7. Latch Enable To Output Delays

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

Logic Products

FAST 74F568, 74F569
Bidirectional Counters

'F568 4-Bit Bidirectional Decade Counter (3-State)
'F569 4-Bit Bidirectional Binary Counter (3-State)
Preliminary Specification

FEATURES

- **4-Bit Bidirectional Counters**
  - **'F568-Decade Counter**
  - **'F569-Binary Counter**
- **Synchronous counting and loading**
- **Lookahead Carry capability for easy cascading**
- **Preset capability for programmable operation**
- **Master Reset ($\overline{MR}$) overrides all other inputs**
- **Synchronous Reset ($\overline{SR}$) overrides counting and parallel loading**
- **Clocked carry (CC) output to be used as a clock for flip-flops, registers and counters**
- **3-State outputs for bus organized systems**

TYPE	TYPICAL fMAX	TYPICAL SUPPLY CURRENT (TOTAL)
74F568, 74F569	115MHz	45mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F568N, N74F569N
Plastic SOL-20	N74F568D, N74F569D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

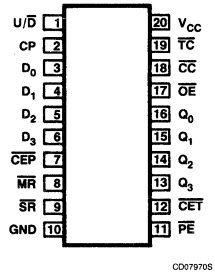
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count enable parallel input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active LOW)	1.0/2.0	20μA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active LOW)	1.0/2.0	20μA/1.2mA
$\overline{U}$/D	Up/Down count control input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active LOW)	50/40	1mA/24mA
$\overline{CC}$	Clocked carry output (active LOW)	50/40	1mA/24mA
$Q_0 - Q_3$	Data outputs	50/40	1mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

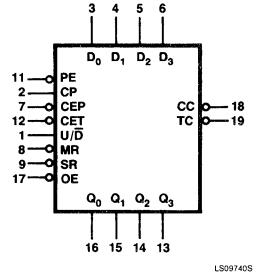
'F568



CD07970S

LOGIC SYMBOL

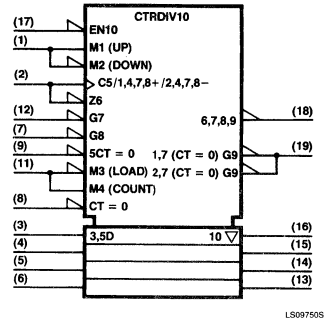
'F568



LS09740S

LOGIC SYMBOL (IEEE/IEC)

'F568



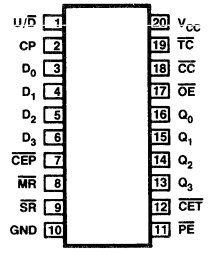
LS09750S

Bidirectional Counters

FAST 74F568, 74F569

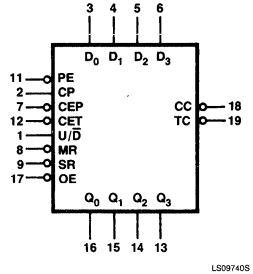
PIN CONFIGURATION

'F569



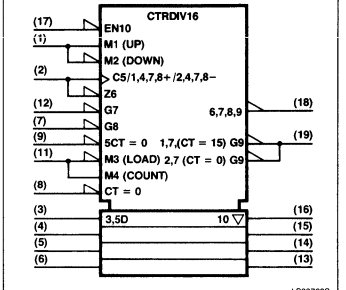
LOGIC SYMBOL

'F569



LOGIC SYMBOL (IEEE/IEC)

'F569



FUNCTIONAL DESCRIPTION

The "F568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The 'F569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs — Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$) and Count Enable Trickle ($\overline{CET}$) — plus the Up/Down (U/$\overline{D}$) input, determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$ and $\overline{PE}$ HIGH, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are LOW. Conversely, a HIGH signal on either $\overline{CEP}$ or $\overline{CET}$ inhibits counting.

The 'F568 and 'F569 use edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended set-up and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW providing $\overline{CET}$ is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the 'F568, 15 for the 'F569) in the Up mode. $\overline{TC}$ will then remain LOW until a state change occurs, whether by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed. To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP set-up time of the last stage. This total delay plus set-up time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 ('F568) or 16 ('F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP set-up time of the last stage.

The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs $Q_0 - Q_3$ are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces $Q_0 - Q_3$ to the High Z state but does not prevent counting, loading or resetting.

LOGIC EQUATIONS:

Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet PE$

Up ('F568): $\overline{TC} = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

('F569): $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

Down (Both): $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Down) \bullet \overline{CET}$

$\overline{CC}$ FUNCTION TABLE

INPUTS						OUTPUT
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊔	⊔

* = $\overline{TC}$ is generated internally

H = HIGH voltage level

L = LOW voltage level

X = Don't care

MODE SELECT TABLE

INPUTS						OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	
L	X	X	X	X	X	Asynchronous Reset
H	L	X	X	X	X	Synchronous Reset
H	H	L	X	X	X	Parallel Load
H	H	H	H	X	X	Hold
H	H	H	X	H	X	Hold
H	H	H	L	L	H	Count Up
H	H	H	L	L	L	Count Down

H = HIGH voltage level
L = LOW voltage level
X = Don't care

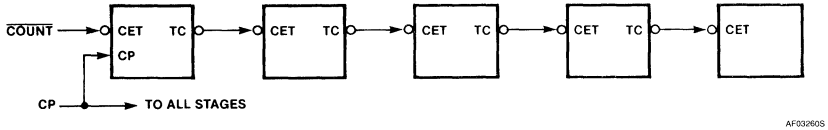


Figure 1. Multistage Counter with Ripple Carry

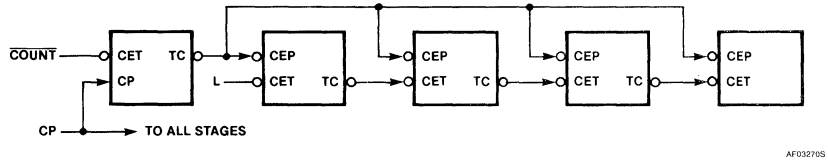
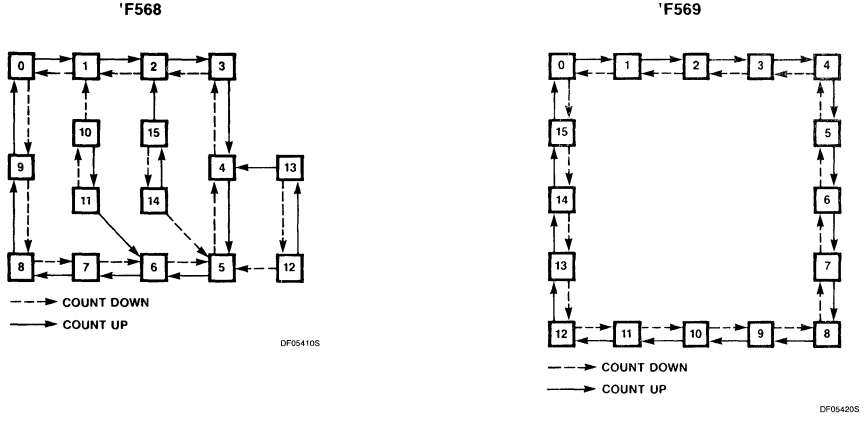
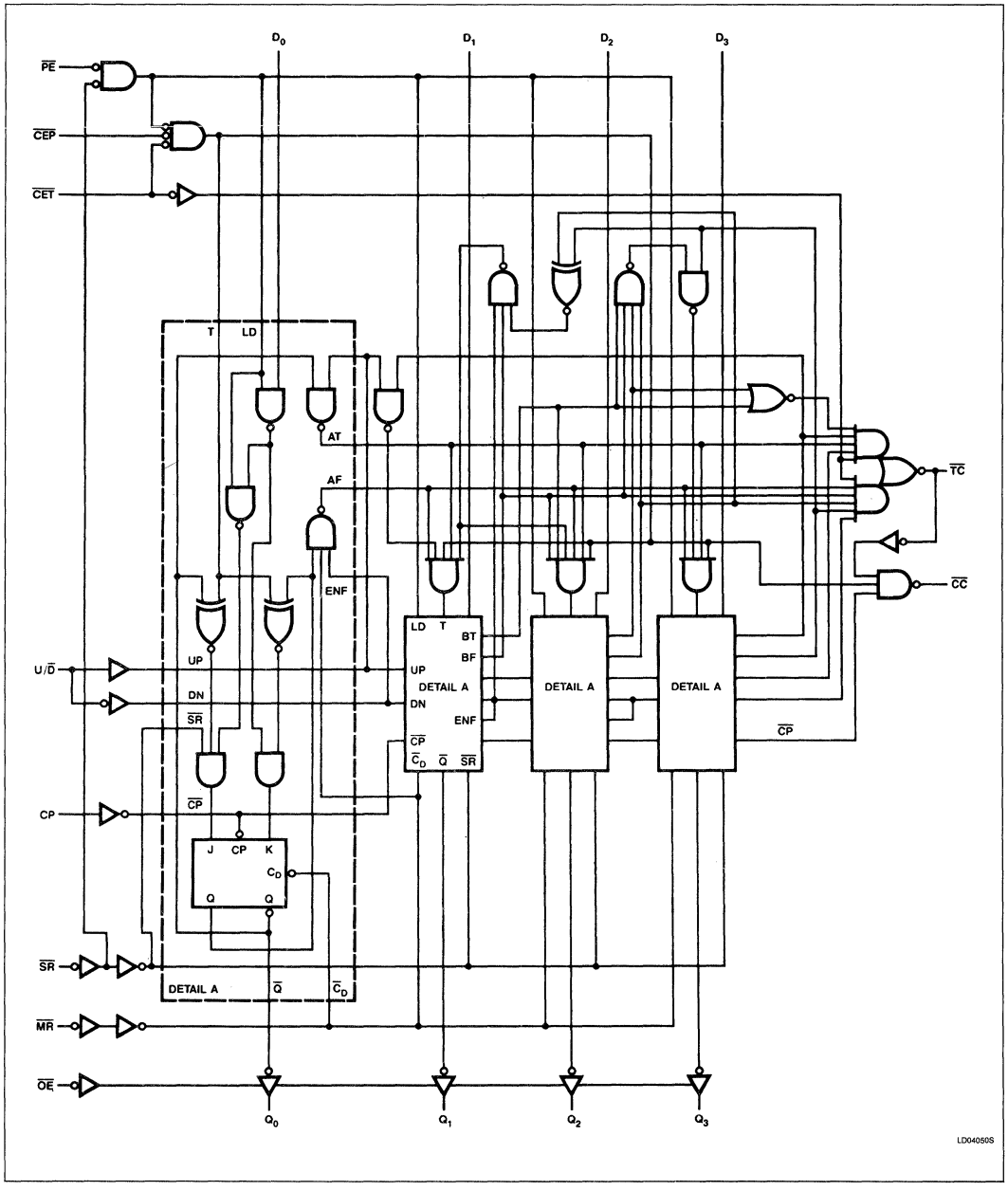


Figure 2. Multistage Counter with Lookahead Carry

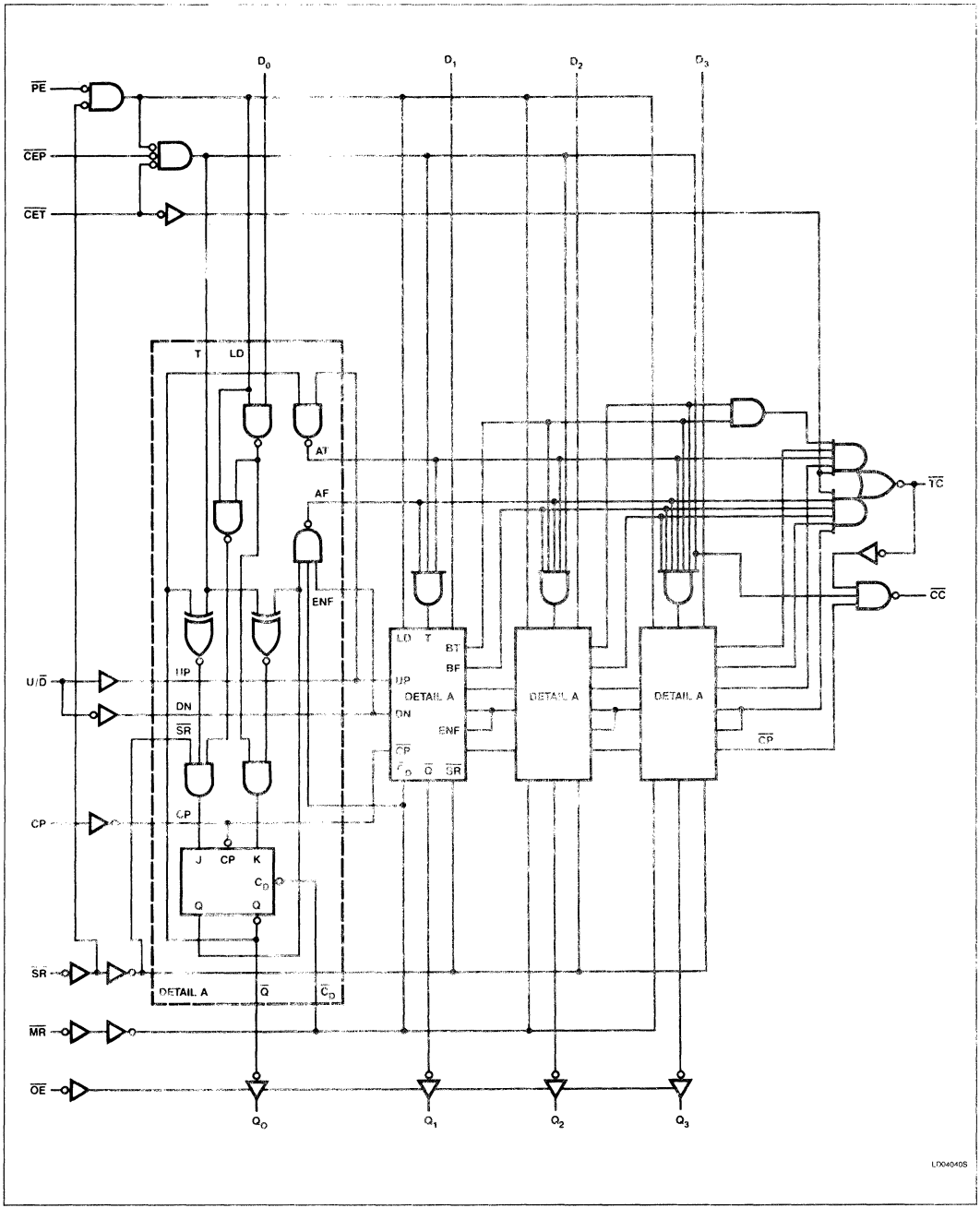
STATE DIAGRAMS



LOGIC DIAGRAM FOR 'F568



LOGIC DIAGRAM FOR 'F569



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F568, 74F569			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX V_I = 7.0V					100
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			45	67	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

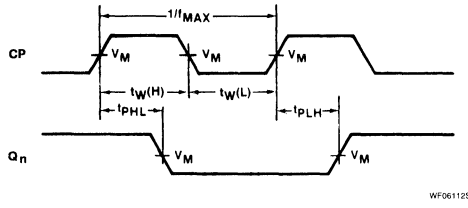
PARAMETER		TEST CONDITIONS	74F568, 74F569					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = HIGH or LOW)	Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	9.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	17.5 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/D to $\overline{TC}$ ('F568)	Waveform 3	3.5 4.0	8.5 12.5	11.0 16.0	3.5 4.0	12.5 18.0	ns
t_{PLH} t_{PHL}	Propagation delay U/D to $\overline{TC}$ ('F569)	Waveform 3	3.5 4.0	8.5 8.0	11.0 10.5	3.5 4.0	12.5 12.0	ns
t_{PLH} t_{PHL}	Output enable time to HIGH or CP to $\overline{CC}$	Waveform 8 Waveform 9	2.5 2.0	5.5 4.5	7.0 6.0	2.5 2.0	8.0 7.0	ns
t_{PLH} t_{PHL}	Output enable time from HIGH $\overline{CEP}$, $\overline{CET}$ TO $\overline{CC}$	Waveform 8 Waveform 9	2.5 4.0	5.0 8.5	6.5 11.0	2.5 4.0	7.5 12.5	ns
t_{PHL}	Output enable time to HIGH or $\overline{MR}$ to Q_n	Waveform 7	5.0	10.0	13.0	5.0	14.5	ns
t_{PHZ} t_{PLZ}	Output enable time from HIGH or LOW level $\overline{OE}$ to Q_n	Waveform 8 Waveform 9	2.5 3.0	5.5 6.0	7.0 3.0	2.5 3.0	8.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{OE}$ to Q_n	Waveform 8 Waveform 9	1.5 2.0	5.0 2.0	5.0 4.5	6.5 6.0	1.5 2.0	7.5 7.0

NOTE:
Subtract 0.2ns from minimum values for SO package.

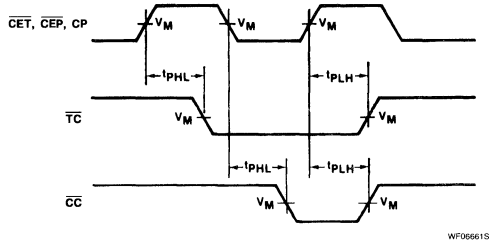
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F568, 74F569					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP	Waveform 8	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP	Waveform 8	3.0 3.0			3.5 3.5		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CEP}$, $\overline{CET}$ to CP	Waveform 9	5.0 5.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CEP}$, $\overline{CET}$ to CP	Waveform 9	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{PE}$ to CP	Waveform 8	8.0 8.0			9.0 9.0		ns
$t_h(H$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$ to CP	Waveform 8	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW U/$\overline{D}$ to CP ('F568)	Waveform 10	11.0 16.5			12.5 17.5		ns
$t_h(H)$ $t_h(L)$	Set-up time, HIGH or LOW U/$\overline{D}$ to CP ('F569)	Waveform 10	11.0 7.0			12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW U/$\overline{D}$ to CP	Waveform 10	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{SR}$ to CP	Waveform 11	9.5 8.5			10.5 9.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{SR}$ to CP	Waveform 11	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW	Waveform 1	4.0 6.0			4.5 6.5		ns
$t_w(L)$	$\overline{MR}$ pulse width, LOW	Waveform 5	4.5			5.0		ns
t_{rec}	$\overline{MR}$ recovery time	Waveform 5	6.0			7.0		ns

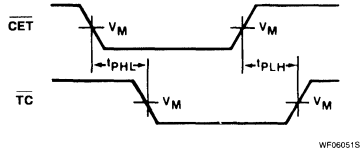
AC WAVEFORMS



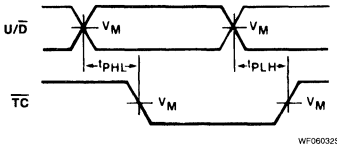
Waveform 1. Clock To Output Delays And Clock Pulse Width



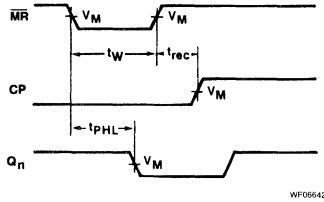
Waveform 2. Clock To Terminal Count Delays



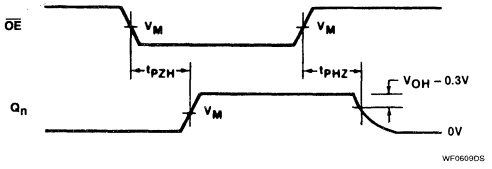
Waveform 3. Propagation Delays $\overline{CET}$ Input To Terminal Count Output



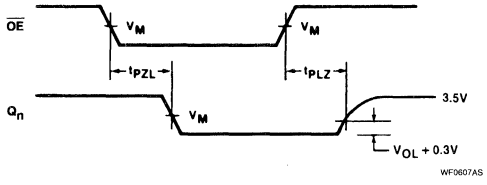
Waveform 4. Propagation Delays U/$\overline{D}$ Control to Terminal Count Output



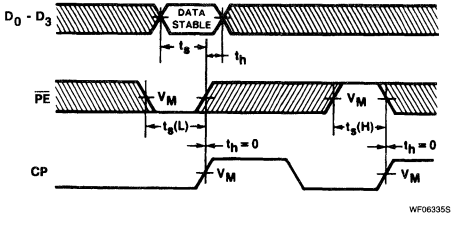
Waveform 5. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



Waveform 6. 3-State Enable Time To HIGH Level And Disable Time From HIGH Level



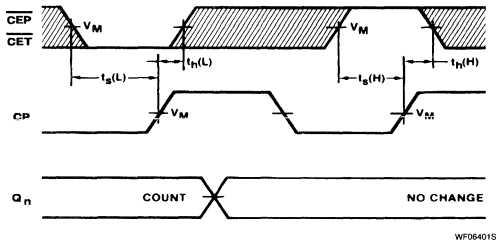
Waveform 7. 3-State Enable Time To LOW Level And Disable Time From LOW Level



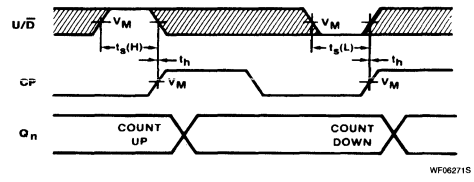
Waveform 8. Parallel Data And Paralled Enable Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

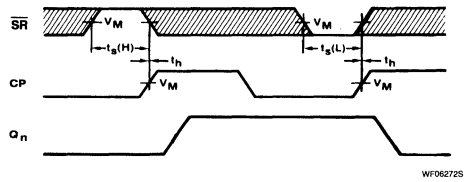
AC WAVEFORMS (Continued)



Waveform 9. Count Enable Set-up And Hold Times



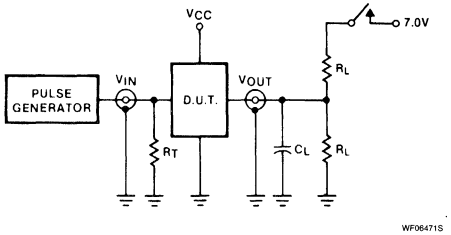
Waveform 10. Up/Down Control Set-up And Hold Times



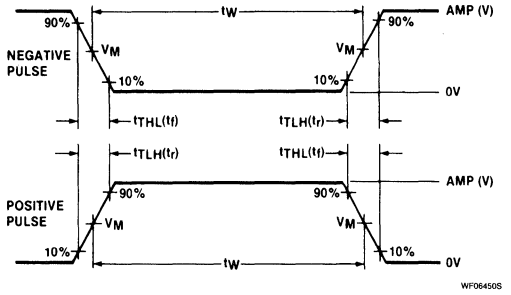
Waveform 11. Synchronous Reset Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

Logic Products

FAST 74F573, 74F574
Latch/Flip-Flops

'F573 Octal Transparent Latch (3-State)
'F574 Octal D Flip-Flop (3-State)
Preliminary Specification

FEATURES

- **'573 is broadside pinout version of 'F373**
- **'574 is broadside pinout version of 'F374**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus interfacing**
- **Common Output Enable**
- **'F563 and 'F564 are inverting versions of 'F573 and 'F574 respectively**
- **These are High-Speed replacements for N8TS805 and N8TS806**

DESCRIPTION

The 'F573 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F573	4.5ns	35mA
74F574	6.5ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F573N, N74F574N
Plastic SOL-20	N74F573D, N74F574D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

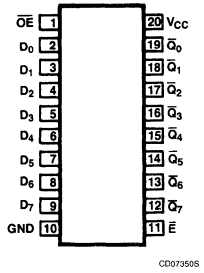
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$ ('F573 & 'F574)	Data inputs	1.0/1.0	20μA/0.6mA
E ('F573)	Latch enable input (active HIGH)	1.0/1.0	20μA/0.6mA
$\overline{OE}$ ('F573 & 'F574)	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
CP ('F574)	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$O_0 - O_7$ ('F573 & 'F574)	3-State outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

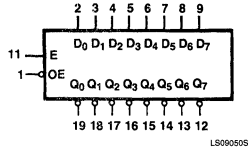
PIN CONFIGURATION

'F573



LOGIC SYMBOL

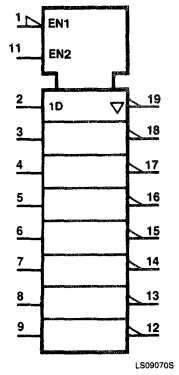
'F573



VCC = Pin 24
GND = Pin 12

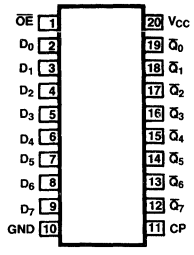
LOGIC SYMBOL (IEEE/IEC)

'F573



PIN CONFIGURATION

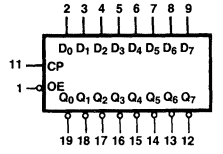
'F574



CD07360S

LOGIC SYMBOL

'F574

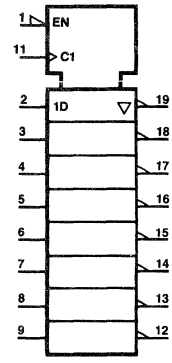


LS09060S

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

'F574



LS09080S

The 'F573 is functionally identical to the 'F373 but has a broadside pinout configuration to facilitate PC Board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data that is present one set-up time before the HIGH-to-LOW enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

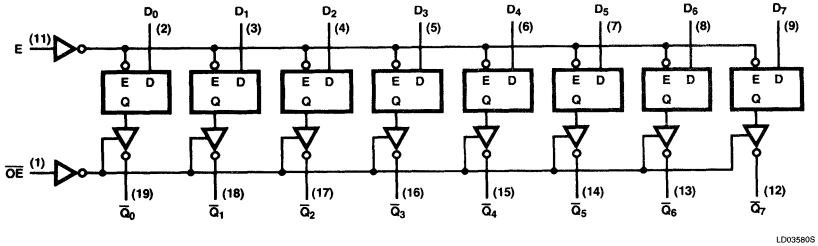
The 'F574 is functionally identical to the 'F374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface to microprocessors.

It is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

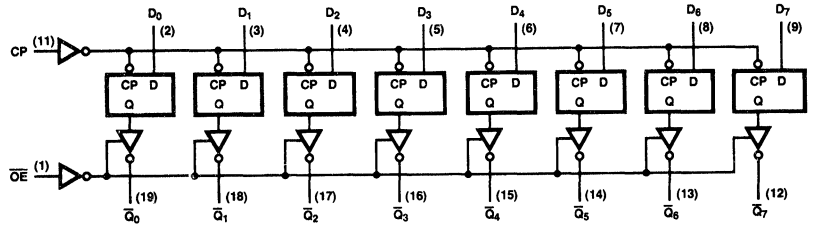
LOGIC DIAGRAM, 'F573



LD03580S

V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 'F574



V_{CC} = Pin 20
GND = Pin 10

MODE SELECT — FUNCTION TABLE, 'F573

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$Q_0 - Q_7$
Enable and read register	L	H	X	L	L
	L	H	X	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

MODE SELECT — FUNCTION TABLE, 'F574

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$Q_0 - Q_7$
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
X = Don't care
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER				TEST CONDITIONS[1]		74F573, 74F574			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage			V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	±10%V_{CC}	2.4	3.4		V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage			V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX, V_{IL} = MAX	±10%V_{CC}		0.35	0.5	V
					±5%V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current			V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied			V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied			V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX, V_O = 0.0V		−60		−150	mA
I_{CC}	Supply current (total)	I_{CC2}	'573	V_{CC} = MAX	$\overline{OE}$ = 4.5V, D = E = GND		35	55	mA
			'574		CP = $\overline{OE}$ = 4.5V, D_n inputs = GND		57	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

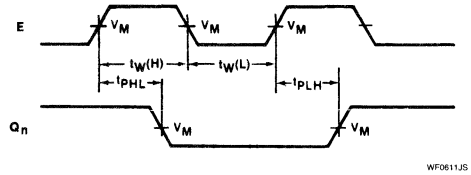
PARAMETER			TEST CONDITIONS	74F573, 74F574					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	'F574	Waveform 6	100			70		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	'F573	Waveform 1	3.0 2.0	9.0 4.0	11.5 7.0	5.0 3.0	13.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	'F573	Waveform 4	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	'F574	Waveform 6	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH}	Enable time to HIGH level	'F573 'F574	Waveform 2	2.0 2.0	5.0 9.0	11.0 11.5	2.0 2.0	12.0 12.5	ns
t_{PZL}	Enable time to LOW level	'F573 'F574	Waveform 3	2.0 2.0	5.6 5.3	7.5 7.5	2.0 2.0	8.5 8.5	ns
t_{PHZ}	Disable time to HIGH level	'F573 'F574	Waveform 2	2.0 2.0	4.5 5.3	6.5 7.0	2.0 2.0	7.5 8.0	ns
t_{PLZ}	Disable time to LOW level	'F573 'F574	Waveform 3	2.0 2.0	3.8 4.3	5.0 5.5	2.0 2.0	6.0 6.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

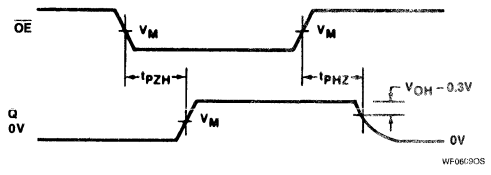
AC SET-UP REQUIREMENTS

PARAMETER			TEST CONDITIONS	74F573, 74F574					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_w(H)$ $t_w(L)$	Latch enable pulse width	'F573	Waveform 1	6.0 6.0			6.0 6.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, data to latch enable	'F573	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, data to latch enable	'F573	Waveform 5	3.0 3.0			3.0 3.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width	'F574	Waveform 6	7.0 6.0			7.0 6.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, data to clock	'F574	Waveform 7	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, data to clock	'F574	Waveform 7	2.0 2.0			2.0 2.0		ns

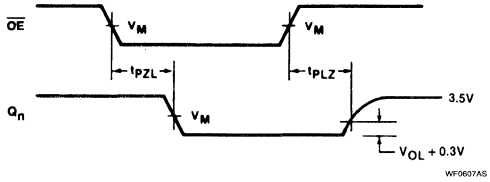
AC WAVEFORMS



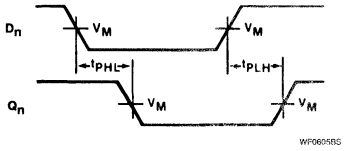
Waveform 1. Latch Enable To Output Delays And Latch Enable Pulse Width



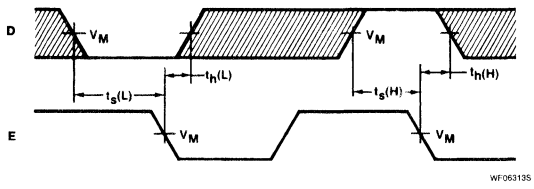
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



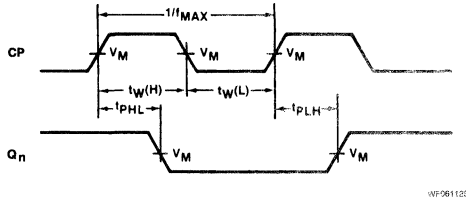
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



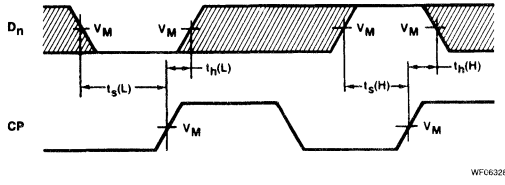
Waveform 4. Propagation Delay Data To Q Outputs



Waveform 5. Data Set-up And Hold Times



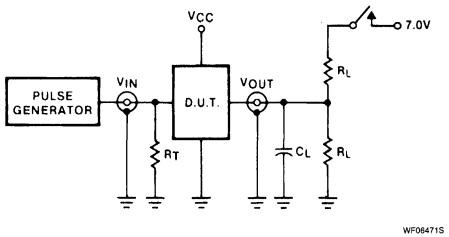
Waveform 6. Clock To Output Delays And Clock Pulse Width



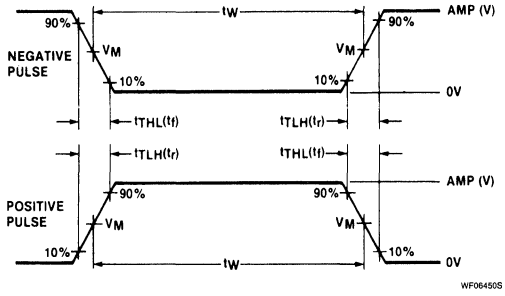
Waveform 7. Data Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

6

Signetics

FAST 74F579
Counter

8-Bit Bidirectional Binary Counter (3-State)
Product Specification

Logic Products

FEATURES

- **Multiplexed 3-State I/O ports for bus-oriented applications**
- **Built-in cascading carry capability**
- **Count frequency 115MHz typ**
- **Supply current 100mA typ**
- **Fully synchronous operation**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master Reset and Synchronous Reset**
- **Center power pins to reduce effects of package inductance**
- **See 'F269 for 24-pin separate I/O port version**
- **See 'F779 for 16-pin version**

DESCRIPTION

The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock.

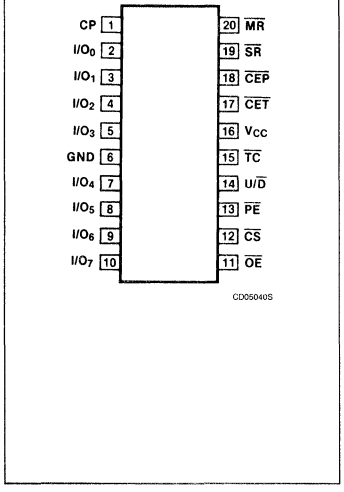
TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100mA

ORDERING CODE

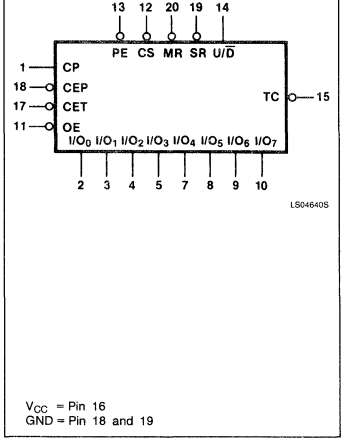
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F579N
Plastic SOL-20	N74F579D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

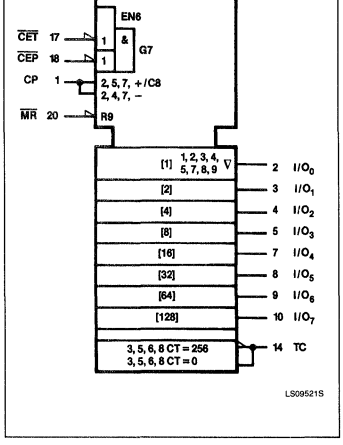
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I/O_0 - I/O_7$	Data inputs	1.0/1.0	20μA/0.6mA
	Data outputs	150/40	3mA/24mA
$\overline{PE}$	Parallel enable input (active LOW)	1.0/1.0	20μA/0.6mA
$U/\overline{D}$	Up-down count control input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count enable parallel input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip select input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active LOW)	150/33	3mA/20mA

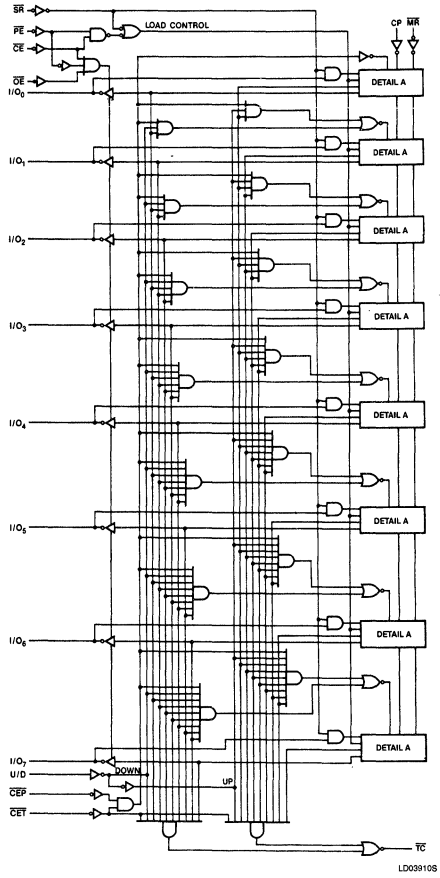
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

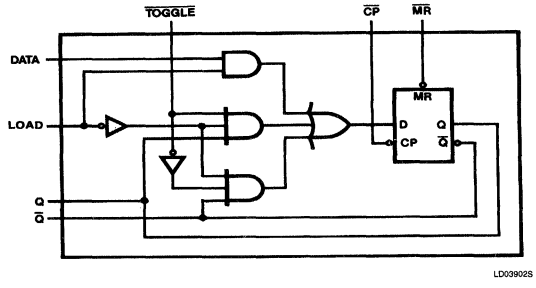
FUNCTION TABLE

$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	$\overline{OE}$	CP	FUNCTION
X	X	H	X	X	X	X	X	X	I/Oa to I/Oh in High-Z ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/Oa to I/Oh in High-Z
X	X	L	H	X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held high)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = HIGH voltage level
L = LOW voltage level
X = Don't Care
↑ = LOW-to-HIGH clock transition not LL means $\overline{CS}$ and $\overline{PE}$ should never both be LOW voltage level at the same time.

LOGIC DIAGRAM





Detail A

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F579			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$\overline{MR}$, CP	V_{CC} = MIN, V_{IL} = 0.0V, V_{IH} = 4.5V, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
		Others	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = MAX, V_I = 5.5V				1.0	mA
		Others	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	HIGH-level input current	All inputs except I/O_n	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH} + I_{IH}	Off-state current HIGH-level voltage applied	I/O_n	V_{CC} = MAX, V_{IH} = MIN, V_I = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_I = 0.5V				−600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			95	135	mA
		I_{CCL}				105	145	mA
		I_{CCZ}				105	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F579					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	5.0 5.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to	Waveform 1	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	Waveform 1	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t_{PHZ} t_{PLZ}	Output Enable Time to High or LOW level $\overline{CS}$,$\overline{PE}$ to I/O_n	Waveform 3 Waveform 4	6.0 6.5	8.0 9.0	10.5 10.5	6.0 6.0	11.5 11.5	ns
t_{PZH} t_{PZL}	Output Disable Time from High or LOW level $\overline{CS}$, $\overline{PE}$ to I/O_n	Waveform 3 Waveform 4	3.0 6.5	6.0 8.5	7.5 9.5	3.0 6.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Enable Time to HIGH or LOW level $\overline{OE}$ tol/O_n	Waveform 3 Waveform 4	4.0 6.5	6.5 8.5	8.5 9.5	4.0 5.0	9.5 10.5	ns
t_{PZH} t_{PZL}	Output Disable Time from HIGH or LOW level $\overline{OE}$ to I/O_n	Waveform 3 Waveform 4	1.0 2.5	2.5 5.0	4.0 7.0	1.0 2.5	5.5 8.0	ns

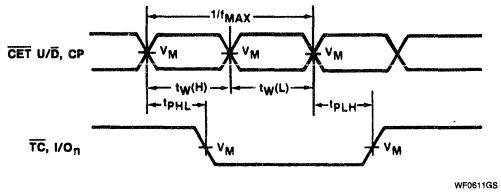
NOTE:
Subtract 0.3ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

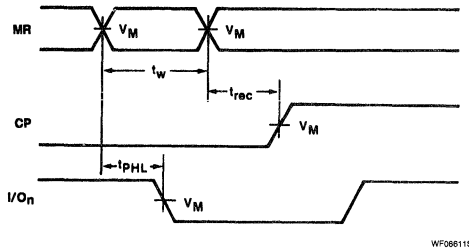
PARAMETER		TEST CONDITIONS	74F579					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW I/O_n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW I/O_n to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{PE}$,$\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	9.5 9.5			10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	Waveform 5	5.0 9.0			5.5 10.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	Waveform 5	0 0			0 0		ns
t_w	Clock pulse width	Waveform 1	4.5			6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse Wiuth	Waveform 2	3.0			3.0		ns
t_{rec}	$\overline{MR}$ Recovery Time	Waveform 2	4.0			4.5		ns

6

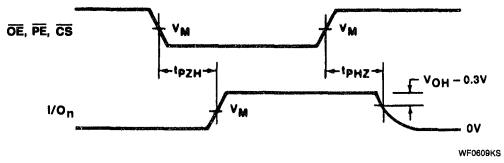
AC WAVEFORMS



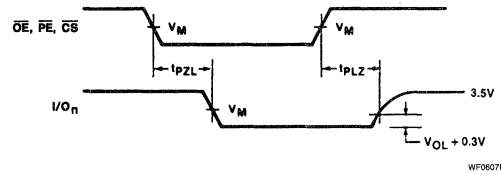
Waveform 1. Clock To Output Delays, Clock Pulse Width, And Maximum Clock Frequency



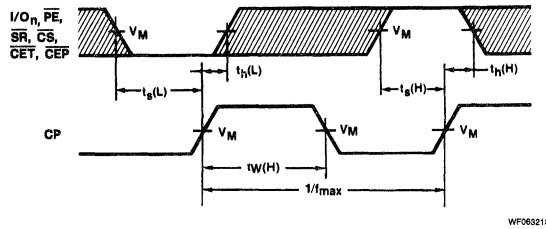
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



Waveform 3. 3-State Enable Time To HIGH Level And Disable Time From HIGH Level



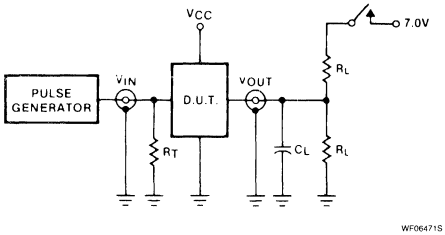
Waveform 4. 3-State Enable Time To LOW Level And Disable Time From LOW Level

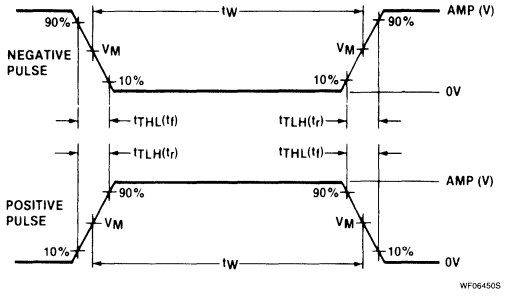


Waveform 5. Data Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable performance.

TEST CIRCUIT AND WAVEFORMS





Test Circuit For 3-State Outputs

Input Pulse Definition

$V_M = 1.5V$

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

Logic Products

FAST 74F582, 74F583
BCD Arithmetic Logic Unit/BCD Adder

4-Bit BCD Arithmetic Logic Unit
4-Bit BCD Adder
Preliminary Specification

'F582 FEATURES
- **Performs four BCD functions**
- **P and G outputs for high-speed expansion**
- **Add/Subtract delay 22ns max**
- **Look-ahead delay 15.5ns max**
- **Supply current 85mA max**
- **24 pin 300mil Slim DIP package**

'F583 FEATURES
- **Adds two decimal numbers**
- **Full internal look-ahead**
- **Fast ripple carry for economical expansion**
- **Sum output delay 16.5ns max**
- **Ripple carry delay 8.5ns max**
- **Input to ripple delay 14.0ns max**
- **Supply current 60mA max**

DESCRIPTION

The 'F582 Binary Coded Decimal (BCD) Arithmetic Logic Unit (ALU) is a 24-pin expandable unit that performs addition, subtraction, comparison of two numbers, and binary to BCD conversion.

The 'F582 input and output logic includes a Carry/$\overline{\text{Borrow}}$ which is generated internally in the look-ahead mode, allowing BCD arithmetic to be computed directly. For more than one BCD decade, the Carry/$\overline{\text{Borrow}}$ term may ripple between 'F582s.

When A/S is LOW, BCD addition is performed (A + B + C/$\overline{\text{B}}$ = F). If an input is greater than 9, binary to BCD conversion results at the output.

When A/$\overline{\text{S}}$ is HIGH, subtraction is performed. If the C/$\overline{\text{B}}$ is LOW, then the subtraction is accomplished by internally computing the nine's complement addition of two BCD numbers (A – B – 1 = F). When C/$\overline{\text{B}}$ is HIGH, the difference of the two numbers is figured as A – F = F. For A is greater than or equal to B, the BCD difference appears at the output F in its true form. If A is less than B and C/$\overline{\text{B}}$ is LOW, the nine's complement of the true form appears at the output F.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F582	17.5ns	55mA
74F583	12.0ns	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74F582N
Plastic SOL-24	N74F582D

NOTES:
1. SO package is surface-mounted micro-miniature DIP
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

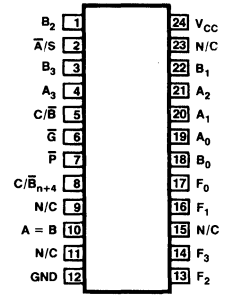
	PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F582	$A_0 - A_3$	A operand inputs	1.0/2.0	20μA/1.2mA
	B_0	B operand input	1.0/1.0	20μA/0.6mA
	B_1	B operand input	1.0/5.0	20μA/3.0mA
	B_2	B operand input	1.0/3.0	20μA/1.8mA
	B_3	B operand input	1.0/2.0	20μA/1.2mA
	$\overline{A}$/S	Add/subtract input	1.0/3.0	20μA/1.8mA
	C/$\overline{B}$	Carry/borrow input	1.0/2.3	20μA/1.4mA
	C/$\overline{B}_{n+4}$	Carry/borrow output	50/33	1.0mA/20mA
	$\overline{P}$	Carry propagate output	50/33	1.0mA/20mA
	$\overline{G}$	Carry generate output	50/33	1.0mA/20mA
	A = B	Comparator output	0C*/33	0C*/20mA
	$F_0 - F_3$	Outputs	50/33	1.0mA/20mA
'F583	$A_0 - A_3$	A operand inputs	1.0/2.0	20μA/1.2mA
	$B_0 - B_3$	B operand inputs	1.0/2.0	20μA/1.2mA
	C_n	Carry input	1.0/1.0	20μA/0.6mA
	$S_0 - S_3$	Sum outputs	1.0/33	20μA/20mA
	C_n	Carry output	1.0/1.0	20μA/0.6mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

BCD Arithmetic Logic Unit/BCD Adder | FAST 74F582, 74F583

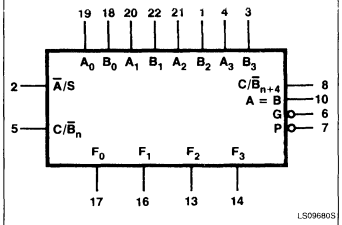
PIN CONFIGURATION

'F582



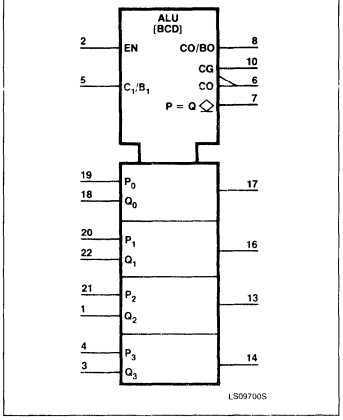
LOGIC SYMBOL

'F582



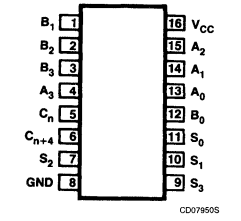
LOGIC SYMBOL (IEEE/IEC)

'F582



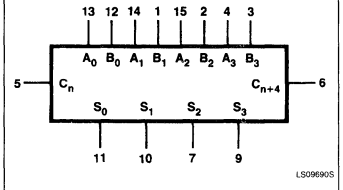
PIN CONFIGURATION

'F583



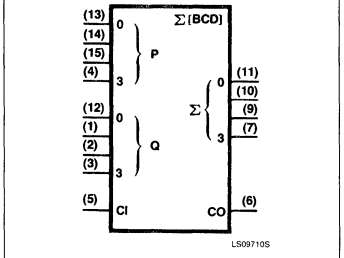
LOGIC SYMBOL

'F583



LOGIC SYMBOL (IEEE/IEC)

'F583



BCD Arithmetic Logic Unit/BCD Adder FAST 74F582, 74F583

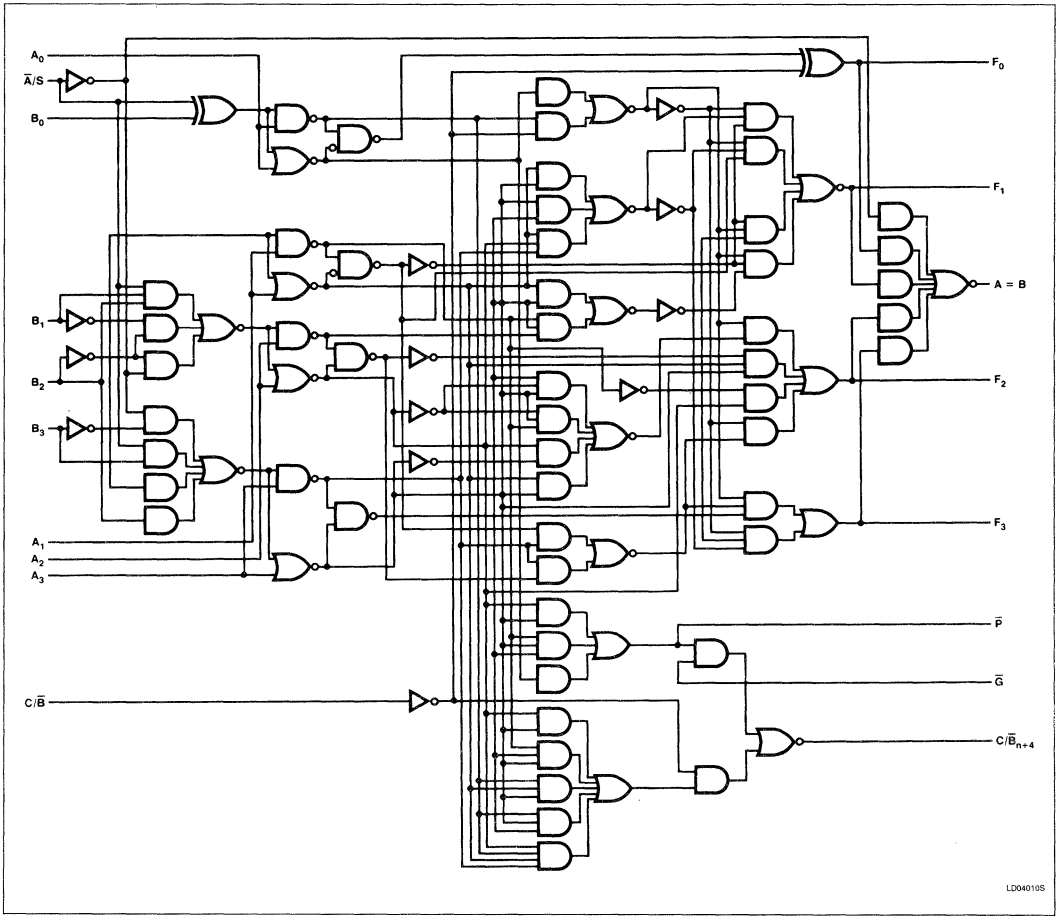
DESCRIPTION (Continued)

As long as A is less than B, an active LOW borrow is also generated. The 'F582 also performs binary to BCD conversion. For inputs between 10 and 15, binary to BCD conversion occurs by grounding one set of inputs, A or B, and applying the binary number to the other set of inputs. This will generate a carry term to the next decade.

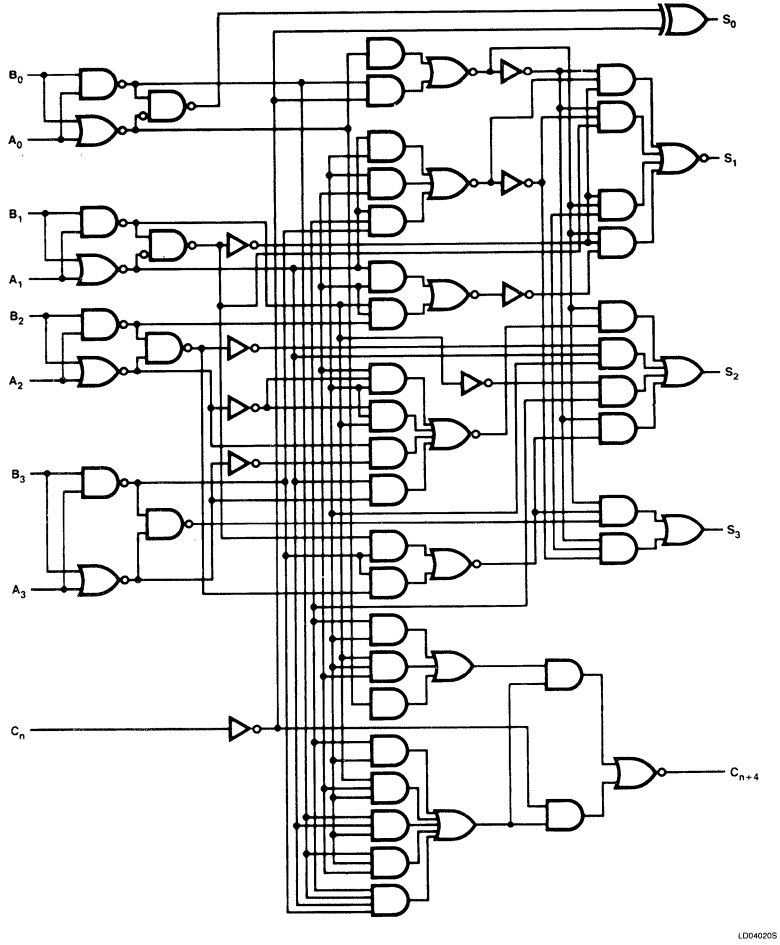
The 'F583 4-bit coded (BCD) full adder performs the addition of two decimal numbers ($A_0 - A_3$, $B_0 - B_3$). The look-ahead generates BCD carry terms internally, allowing the 'F583 to then do BCD addition correctly. For BCD numbers 0 through 9 at A and B inputs, the BCD sum forms at the output.

In the addition of two BCD numbers totalling a number greater than 9, a valid BCD number and a carry will result. For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n, and applying a 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved by cascading 'F583s.

LOGIC DIAGRAM FOR 'F582



LOGIC DIAGRAM FOR 'F583



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
i_{IN}	input current	−30 to + i	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage	A = B only			4.5	V
I_{OH}	HIGH-level output current	except A = B			−1	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F582, 74F583			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	A = B only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]	except A = B	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			40	60	mA
		I_{CCL}				60	90	mA
		I_{CCZ}				60	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic".)

PARAMETER	TEST CONDITIONS	74F582					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A_n or B_n to F_n	Waveform 1	2.5 2.5	17.5 17.5	22.0 22.0	2.5 2.5	23.0 23.0	ns
t_{PLH} Propagation delay t_{PHL} A_n or B_n to $C/\overline{B}_{n+4}$	Waveform 1	4.0 4.0	17.0 12.5	21.5 16.0	4.0 4.0	22.5 17.0	ns
t_{PLH} Propagation delay t_{PHL} $C/\overline{B}_n$ to $C/\overline{B}_{n+4}$	Waveform 1	4.0 2.5	6.5 4.5	8.5 6.0	4.0 2.5	9.5 7.0	ns
t_{PLH} Propagation delay t_{PHL} A_n or B_n to $A = B$	Waveform 1	8.0 8.0	19.0 17.0	24.0 21.5	8.0 8.0	25.0 22.5	ns
t_{PLH} Propagation delay t_{PHL} A_n or B_n to $\overline{G}$ or $\overline{P}$	Waveform 2	4.0 4.0	12.0 12.0	15.5 15.5	4.0 4.0	16.5 16.5	ns
t_{PLH} Propagation delay $\overline{A}/S$ to F_n	Waveform 3	2.5	21.0	27.0	2.5	28.0	ns

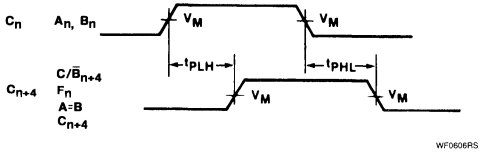
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic".)

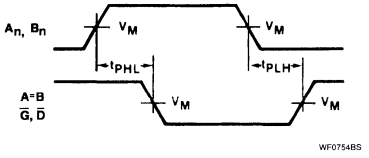
PARAMETER	TEST CONDITIONS	74F583					UNIT
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A_n or B_n to S_n	Waveform 3	2.5 2.5	13.0 11.0	16.5 14.0	2.5 2.5	17.5 15.0	ns
t_{PLH} Propagation delay t_{PHL} A_n or B_{n+4}	Waveform 1	2.5 2.5	6.5 5.0	8.5 6.5	2.5 2.5	9.5 7.5	ns
t_{PLH} Propagation delay t_{PHL} A_n or B_n to C_{n+4}	Waveform 1	4.0 4.0	11.0 8.0	14.0 10.5	4.0 4.0	15.0 11.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

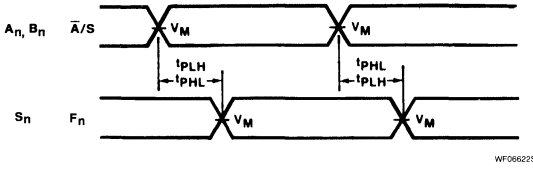
AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Outputs



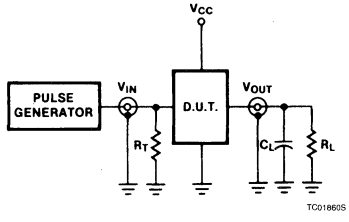
Waveform 2. Propagation Delay For Inverting Outputs



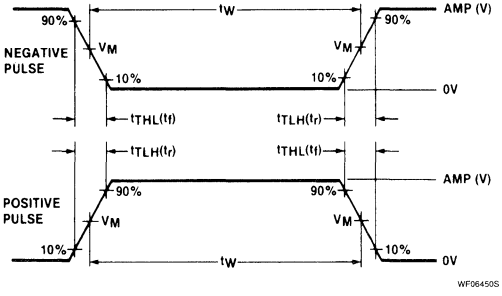
Waveform 3. Propagation Delay Operands To Sum Output And $\overline{Add}$/Subtract To Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F588
Transceiver

Octal Bidirectional Transceiver With IEEE-488 Termination Resistors (3-State Inputs and Outputs)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base input for reduced loading (70μA in HIGH and LOW states)**
- **Non-inverting buffers**
- **Bidirectional data path**
- **B outputs sink 48mA, source 15mA**

DESCRIPTION

The 'F588 contains eight non-inverting bidirectional buffers with 3-State outputs and is intended for bus-oriented applications. The B ports have termination resistors as specified in the IEEE-488 specifications. Current sinking capability is 20mA at the A ports and 48mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high impedance condition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F588	4.0ns	96mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F588N
Plastic SOL-20	N74F588D

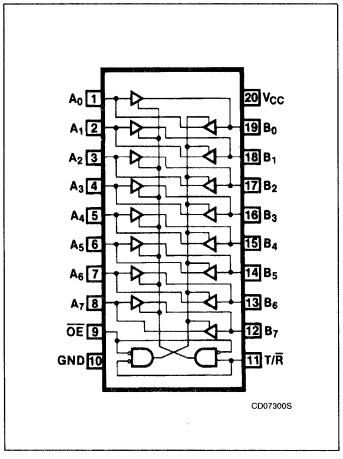
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

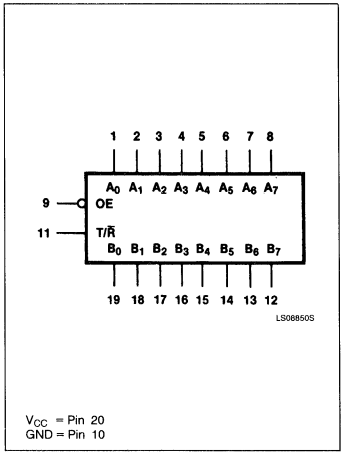
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	Port A data inputs	3.5/0.115	70μA/70μA
$B_0 - B_7$	Port B data inputs	*T/5.33	*T/3.2mA
$T/\overline{R}$	Transmit/receive input	2.0/0.067	40μA/40μA
$\overline{OE}$	Output enable input (active LOW)	2.0/0.067	40μA/40μA
$A_0 - A_7$	Port A data outputs	150/40	3mA/24mA
$B_0 - B_7$	Port B data outputs	750/106.7	15mA/64mA

NOTES:
1. One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. *T = Resistance Termination per IEEE-488 Standard.

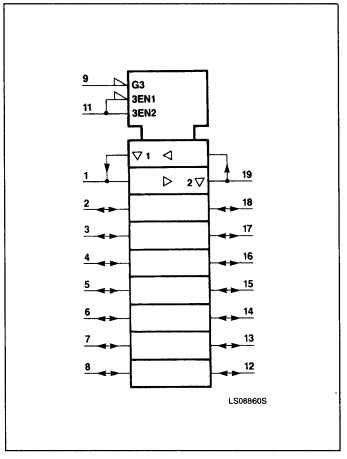
PIN CONFIGURATION

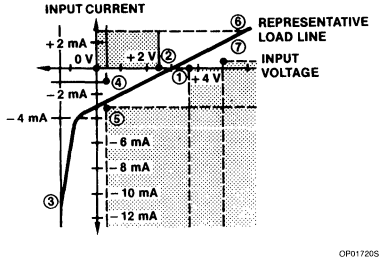


LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)





① , ② No-load voltage
③ Clamp diode
④ , ⑤ I_{IL}
⑥ , ⑦ I_{IH}

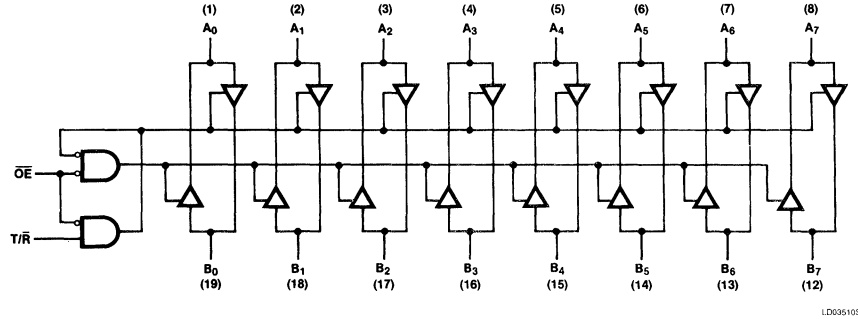
B Port Input Characteristics with T/$\overline{R}$ LOW

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to bus A
L	H	Bus A data to bus B
H	X	High impedance

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	LOW-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F588			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$A_0 - A_7$, $B_0 - B_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, $\overline{OE}$ = 0.0V	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, $\overline{OE}$ = 0.0V	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		$B_0 - B_7$		I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{NL}	No load voltage	$B_0 - B_7$	I_{OUT} = 0mA, T/$\overline{R}$ = 0.0V			2.5		3.7	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$A_0 - A_7$	V_{CC} = 5.5V, V_I = 5.5V					10	mA
		$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 2.7V					40	μA
I_{IL}	LOW-level input current	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 0.5V					−40	μA
I_{OZH} + I_{IH}	Off-state current, HIGH-level voltage applied	$A_0 - A_7$	V_{CC} = MAX, V_I = 2.7V, T/$\overline{R}$ = 4.5V					70	μA
I_{OZL} + I_{IL}	Off-state current, LOW-level voltage applied	$A_0 - A_7$	V_{CC} = MAX, V_I = 0.5V, T/$\overline{R}$ = 4.5V					−70	μA
I_{OZH} + I_{IH}	Off-state current, HIGH-level voltage applied	$B_0 - B_7$	V_{CC} = MAX, V_I = 5.0V, T/$\overline{R}$ = 0.0V			0.7			mA
			V_{CC} = MAX, V_I = 5.5V, T/$\overline{R}$ = 0.0V					2.5	mA
I_{OZL} + I_{IL}	Off-state current LOW-level voltage applied	$B_0 - B_7$	V_{CC} = MAX, V_I = 0.4V, T/$\overline{R}$ = 0.0V			−1.3		−3.2	mA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$				−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	A_n = T/$\overline{R}$ = HIGH; $\overline{OE}$ = 0.0V			82	100	mA
		I_{CCL}		A_n = $\overline{OE}$ = LOW; T/$\overline{R}$ = 4.5V			110	135	mA
		I_{CCZ}		$\overline{OE}$ = 4.5V			95	125	mA

NOTES:

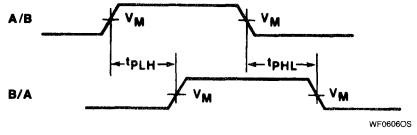
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

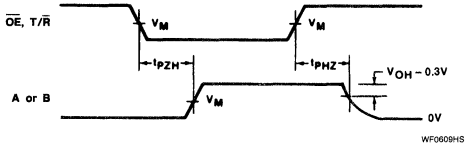
PARAMETER		TEST CONDITIONS	74F588					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0 2.5	3.5 4.5	6.0 7.0	2.0 2.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	Waveform 2 Waveform 3	5.5 5.0	7.5 7.5	10.0 9.5	5.5 5.0	11.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 2 Waveform 3	2.5 2.5	4.5 4.0	7.0 7.0	2.5 2.5	8.0 7.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

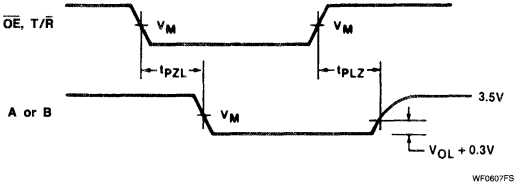
AC WAVEFORMS



Waveform 1. For Non-Inverting Outputs



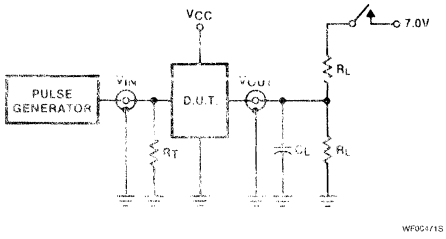
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



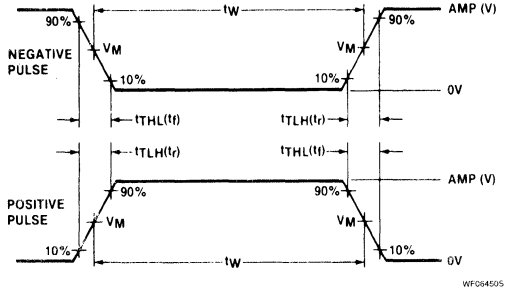
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

6

Signetics

FAST 74F595
8-Bit Shift Register

8-Bit Shift Register with Output Latches (3-State)
Preliminary Specification

Logic Products

FEATURES

- **High impedance NPN base input for reduced loading (20μA in HIGH and LOW states)**
- **8-bit serial-in, parallel-out shift register with storage**
- **3-State outputs**
- **Shift register has direct clear**
- **Guaranteed shift frequency – DC to 120MHz**

DESCRIPTION

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-State outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct overriding clear, Serial input and Serial output pins for cascading.

Both the shift register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F595	120MHz	75mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F595N
Plastic SO-16	N74F595D

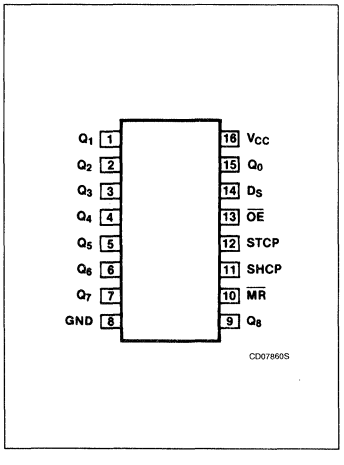
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

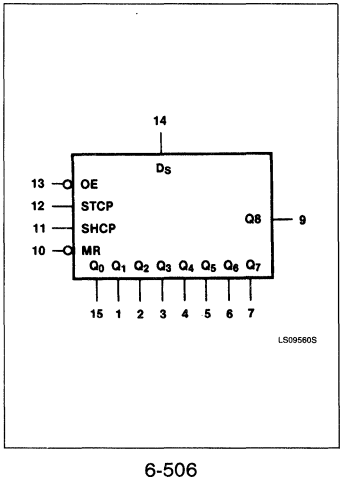
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_S	Serial data input	1.0/0.033	20μA/20μA
SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
STCP	Storage register clock pulse input	1.0/0.033	20μA/20μA
$\overline{MR}$	Master reset input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (Active LOW)	1.0/1.0	20μA/0.6mA
Q_8	Serial expansion output	50/33	1.0mA/20mA
$Q_0 - Q_7$	Data outputs	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

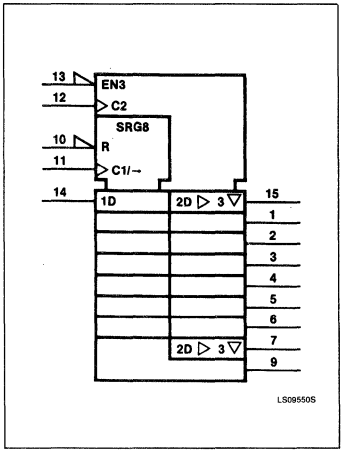
PIN CONFIGURATION



LOGIC SYMBOL

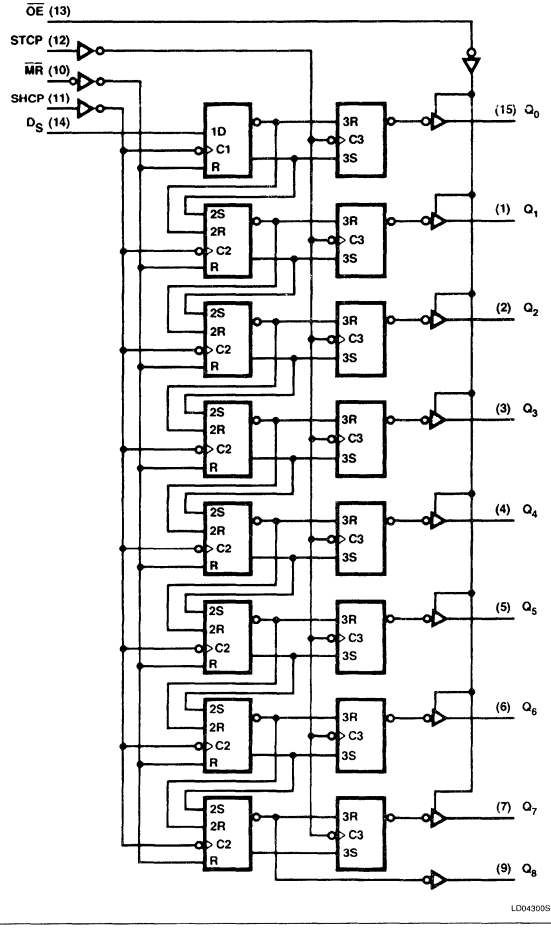


LOGIC SYMBOL (IEEE/IEC)



8-Bit Shift Register FAST 74F595

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F595 Min	74F595 Typ[2]	74F595 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	Others	V_{CC} = MAX, V_I = 0.5V				−20	μA
		$\overline{MR}$ & $\overline{OE}$					−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V			2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	Outputs HIGH		60	75	mA
		I_{CCL}		Outputs LOW		70	85	mA
		I_{CCZ}		Outputs OFF		80	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

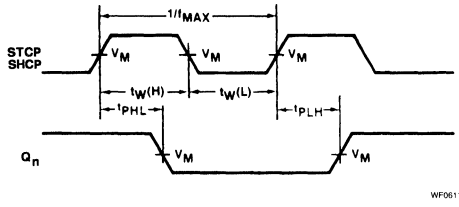
PARAMETER		TEST CONDITIONS	74F595					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_8	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to $Q_0 - Q_8$	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_8	Waveform 3	4.0	7.0	9.0	4.0	10.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	Waveform 5 Waveform 6	2.0 2.0	6.5 5.5	8.0 7.0	2.0 2.0	9.5 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 5 Waveform 6	2.0 2.0	5.5 5.5	7.0 7.0	2.0 2.0	8.5 9.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

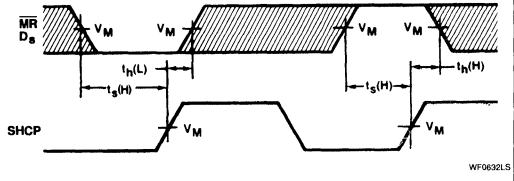
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F595					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, D_s to SHCP	Waveform 2	3.0 3.0			3.0 3.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, D_s to SHCP	Waveform 2	1.0 1.0			1.0 1.0		ns ns
$t_s(H)$	Set-up time, $\overline{MR}$ to SHCP	Waveform 2	6.0			7.0		ns
$t_s(L)$	Set-up time, $\overline{MR}$ to STCP	Waveform 4	5.0			6.0		ns
$t_s(L)$	Set-up time, SHCP to STCP	Waveform 4	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	Pulse width SHCP	Waveform 1	4.0 5.0			4.0 5.0		ns ns
$t_w(H)$ $t_w(L)$	Pulse width STCP	Waveform 1	4.0 5.0			4.0 5.0		ns ns

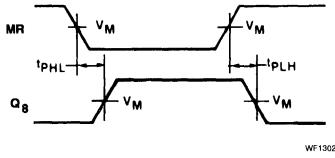
AC WAVEFORMS



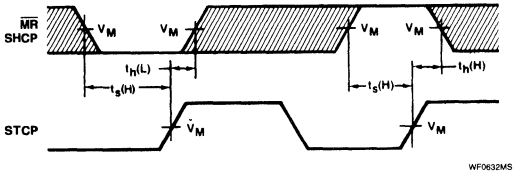
Waveform 1. Clock To Output Delays, Clock Pulse Width, And Maximum Clock Frequency



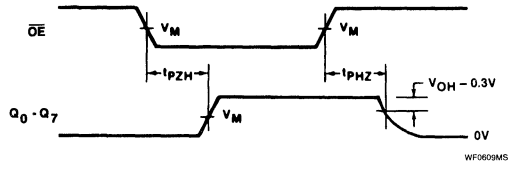
Waveform 2. Data Set-up And Hold Times



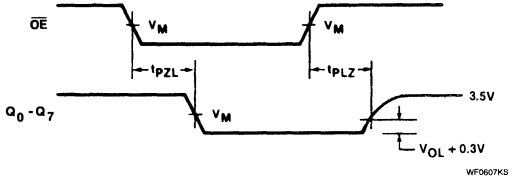
Waveform 3. Master Reset To Serial Expansion Output



Waveform 4. Data Set-up And Hold Times



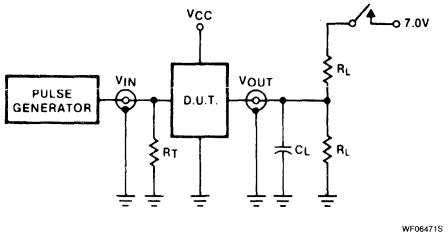
Waveform 5. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level

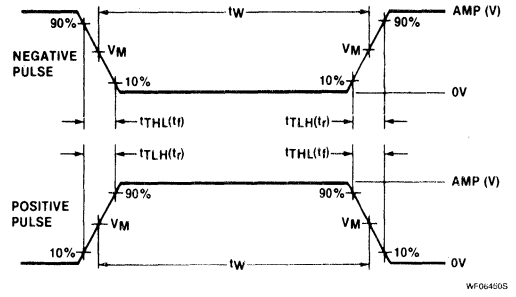


Waveform 6. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS





Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

V_M = 1.5V

Input Pulse Definitions

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F597
8-Bit Shift Register

8-Bit Shift Register with Input Latches (3-State)
Preliminary Specification

Logic Products

FEATURES

- **High impedance NPN Base inputs for reduced loading (20μA in HIGH and LOW states**
- **8-bit Parallel Storage Register inputs**
- **Shift Register has Direct Overriding Load and Clear**
- **Guaranteed Shift Frequency**

DESCRIPTION

The 'F597 consists of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. The storage register and shift register have separate positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F597	120MHz	46mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F597N
Plastic SO-16	N74F597D

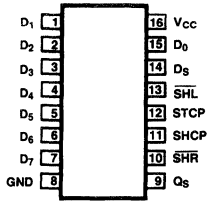
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

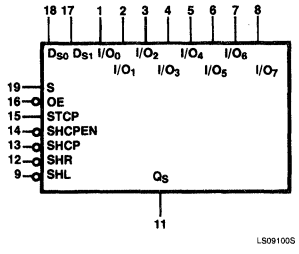
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_S	Serial data input	1/0.033	20μA/20μA
$D_0 - D_7$	Parallel data inputs	1/0.033	20μA/20μA
SHCP	Shift register clock input	1/0.033	20μA/20μA
STCP	Storage register clock input	1/0.033	20μA/20μA
$\overline{SL}$	Serial load enable input	1/0.033	20μA/20μA
$\overline{MR}$	Master reset input	1/0.033	20μA/20μA
Q	Serial data output	55/33	3.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

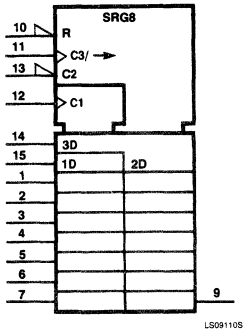


LOGIC SYMBOL



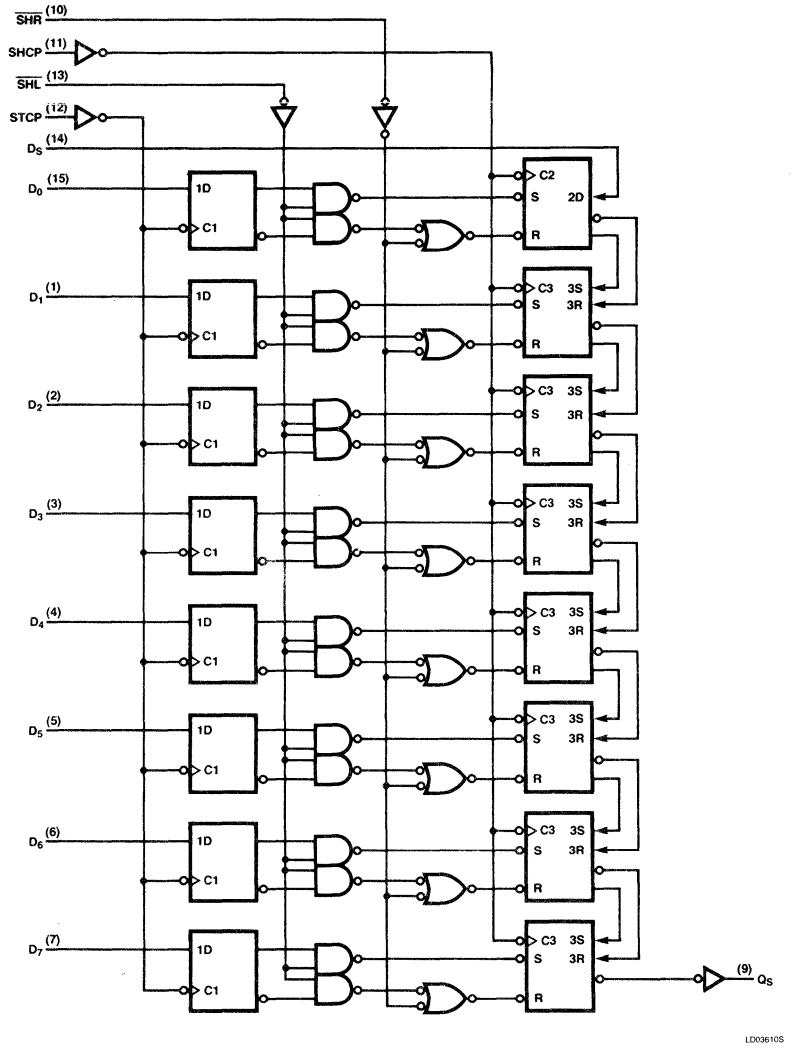
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)

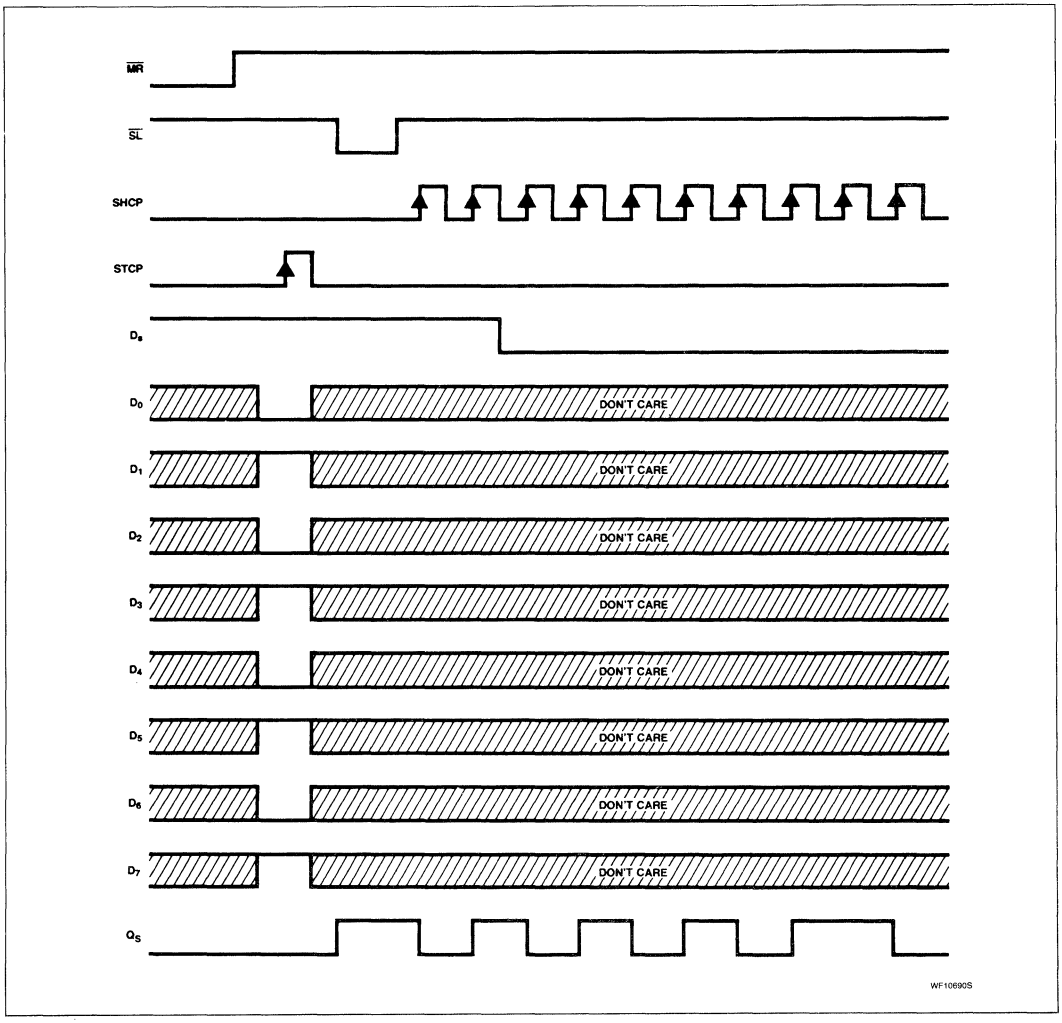


8-Bit Shift Register FAST 74F597

LOGIC DIAGRAM



TYPICAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F597			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−1	−20	μA
I_{OZH}	Off-state current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V			2	50	μA
I_{OZL}	Off-state current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			45	70	mA
		I_{CCL}				48	75	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F597					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80		MHz
t_{PLH}	Propagation delay		4.0	6.5	8.5	4.0	9.5	ns
t_{PHL}	SHCP to Q	Waveform 1	4.0	7.0	9.0	4.0	10.0	ns
t_{PLH}	Propagation delay		4.0	7.5	9.5	4.0	10.0	ns
t_{PHL}	$\overline{SL}$ to Q	Waveform 3	4.0	8.0	10.0	4.0	11.0	ns
t_{PLH}	Propagation delay		4.0	7.5	9.5	4.0	10.0	ns
t_{PHL}	STCP to Q	Waveform 1	4.0	8.0	10.0	4.0	11.0	ns
t_{PLH}	Propagation delay, $\overline{MR}$ to Q	Waveform 3	4.0	8.0	10.0	4.0	11.0	ns

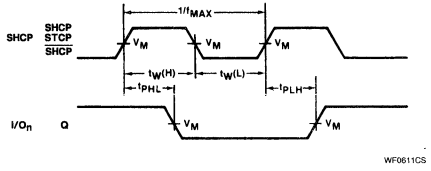
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

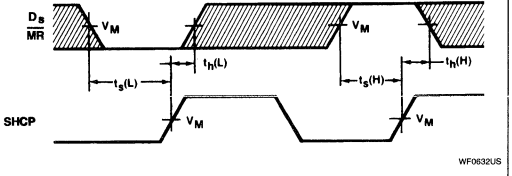
PARAMETER		TEST CONDITIONS	74F597					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$	Set-up time	Waveform 2	3.0			3.0		ns
$t_s(L)$	D_s to SHCP		3.0			3.0		ns
$t_h(H)$	Hold time	Waveform 2	1.0			1.0		ns
$t_h(L)$	D_s to SHCP		1.0			1.0		ns
$t_s(H)$	Set-up time, $\overline{MR}$ to SHCP	Waveform 2	6.0			7.0		ns
$t_w(H)$	SHCP pulse width	Waveform 1	4.0			4.0		ns
$t_w(L)$	HIGH or LOW		5.0			5.0		ns
$t_w(H)$	STCP pulse width	Waveform 1	4.0			4.0		ns
$t_w(L)$	HIGH or LOW		5.0			5.0		ns

6

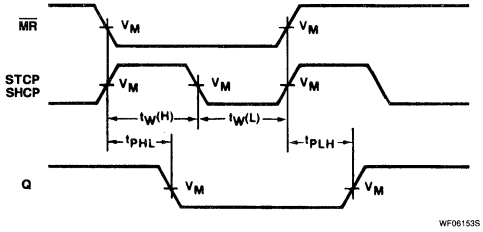
AC WAVEFORMS



Waveform 1. Clock To Output Delays, Clock Pulse Width, And Maximum Clock Frequency



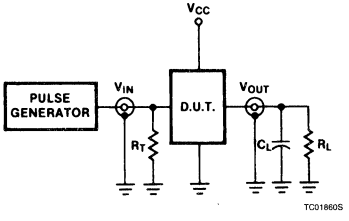
Waveform 2. Data Set-up And Hold Times



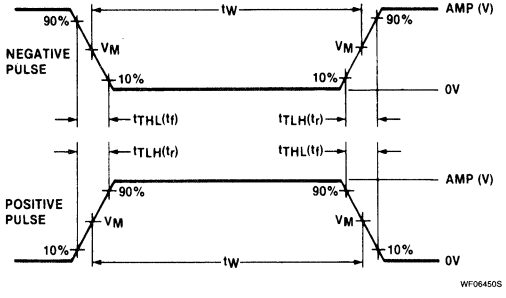
Waveform 3. Master Reset And Serial Load Enable To Output Delays And Pulse Width

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F598
Shift Register

8 Bit Shift Registers With Input Latches (3-States)
Preliminary Specification

Logic Products

FEATURES

- **High impedance NPN Base inputs for reduced loading (20μA in HIGH and LOW states)**
- **8-Bit Parallel storage Register inputs**
- **Shift Register has Direct Overriding Load and Reset**
- **Guaranteed Shift Frequency DC to 120MHz**

DESCRIPTION

The 'F598 comes in a 20-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and reset inputs.

The 'F598 has 3-State I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F598	120MHz	75mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F598N
Plastic SOL-20	N74F598D

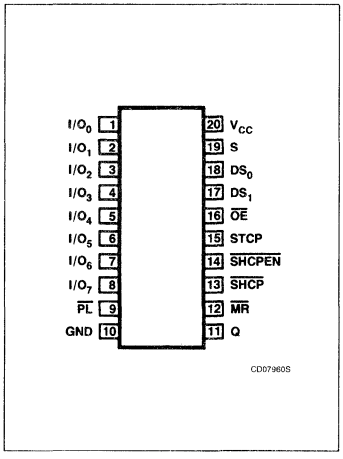
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

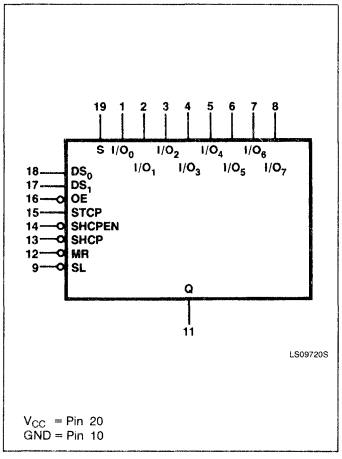
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Data inputs	1/0.033	20μA/20μA
S	Serial data input	1/0.033	20μA/20μA
DS_0, DS_1	Serial data selector input	1/0.033	20μA/20μA
$\overline{SHCP}$	Shift register clock pulse input	1/0.033	20μA/20μA
$\overline{SHCPEN}$	Shift register clock enable input	1/0.033	20μA/20μA
STCP	Storage register clock pulse input	1/0.033	20μA/20μA
$\overline{SL}$	Serial load enable input	1/0.033	20μA/20μA
$\overline{MR}$	Master reset input	1/0.033	20μA/20μA
$\overline{OE}$	Output enable input	1/0.033	20μA/20μA
Q	Output	55/33	1.0mA/20mA
I/On	Data outputs	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

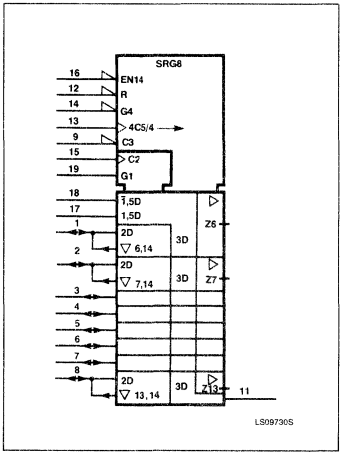
PIN CONFIGURATION



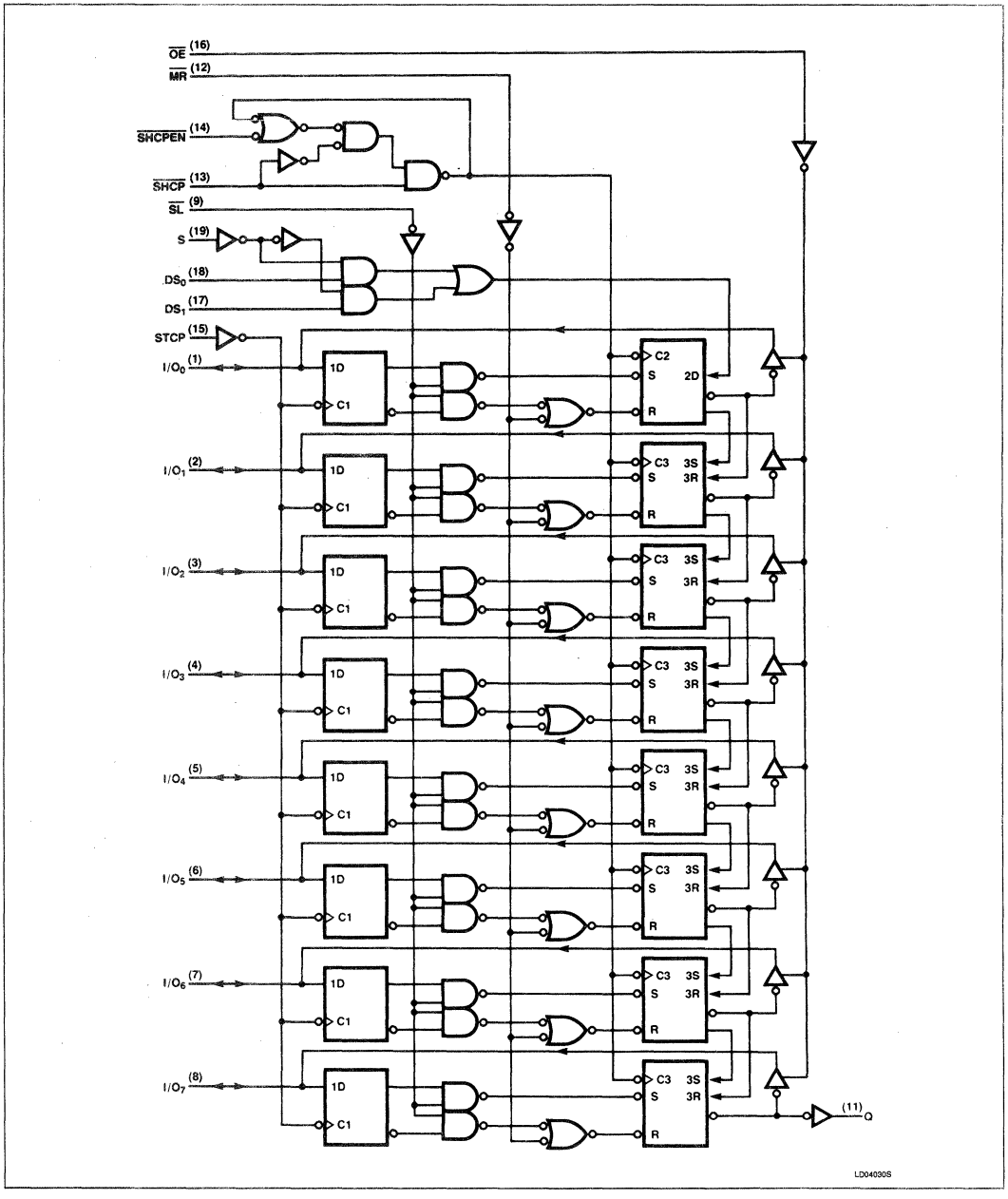
LOGIC SYMBOL



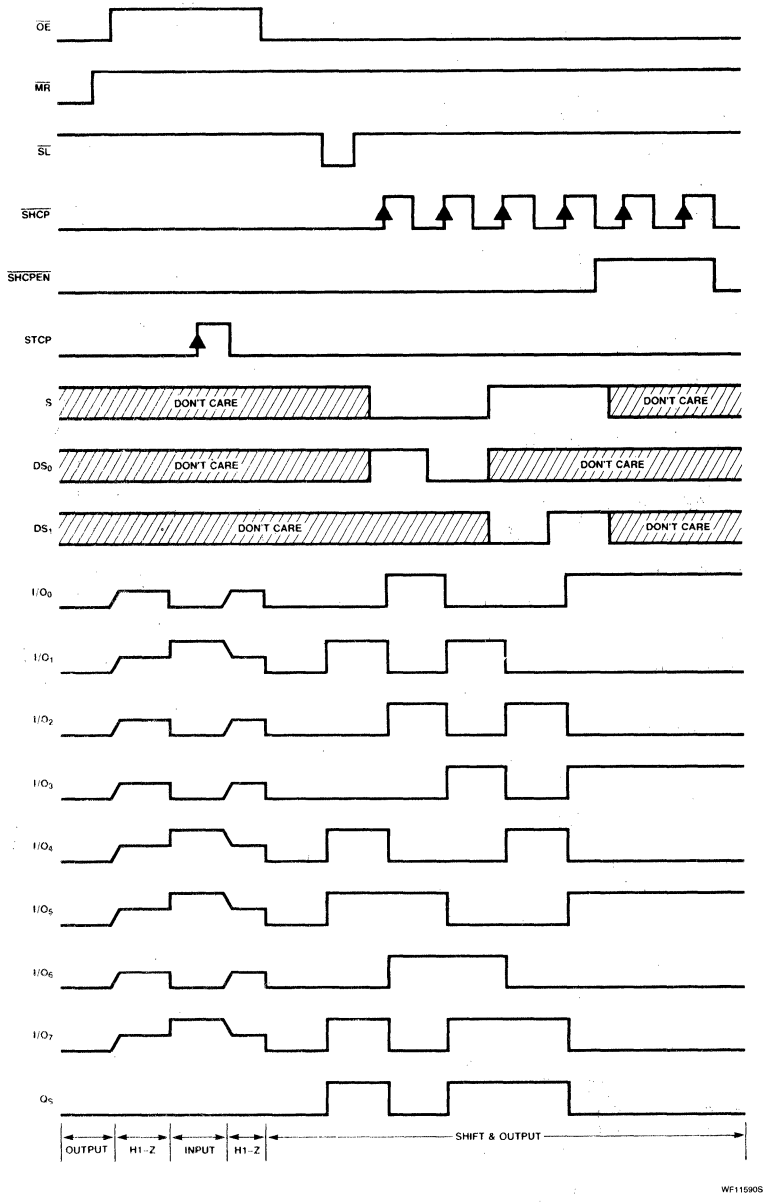
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



TYPICAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
i_{IN}	input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F598			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			.5	1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−1	−20	μA
I_{OZH}	Off-state current HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_{IN} = GND		75	90	mA
	I_{CCL}		V_{IN} = GND		78	95	mA
	I_{CCZ}		V_{IN} = GND		85	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC AN 202, "Testing and Specifying FAST Logic".

PARAMETER		TEST CONDITIONS	74F598					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{SHCP}$ to Q	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SL}$ to Q	Waveform 3	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHCP}$ to I/O_n	Waveform 1	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SL}$ to I/O_n	Waveform 3	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PHL}	$\overline{MR}$ to I/O_n	Waveform 3	4.0	8.0	10.0	4.0	11.0	ns
t_{PHL}	$\overline{MR}$ to Q	Waveform 3	4.0	8.0	10.0	4.0	11.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH to LOW level	Waveform 5 Waveform 6	4.0 4.0	7.5 7.5	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 5 Waveform 6	3.0 3.0	6.0 6.0	8.0 8.0	3.0 3.0	9.0 9.0	ns

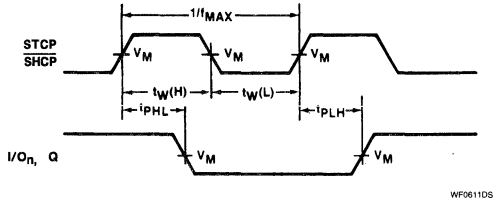
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

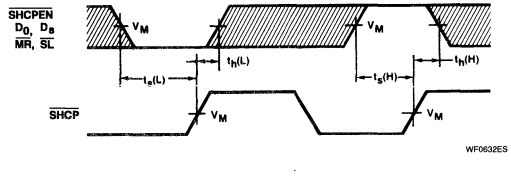
PARAMETER		TEST CONDITIONS	74F598					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, DS_n to $\overline{SHCP}$	Waveform 2	3.0 3.0			3.0 3.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, DS_n to $\overline{SHCP}$	Waveform 2	0.0 0.0			1.0 1.0		ns ns
$t_s(H)$	Set-up time, $\overline{MR}$ to $\overline{SHCP}$	Waveform 2	6.0			7.0		ns
$s_h(L)$	Set-up time, $\overline{MR}$ to STCP	Waveform 2	5.0			6.0		ns
$t_s(L)$	Set-up time, $\overline{SHCP}$ to $\overline{STCP}$	Waveform 4	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	Pulse width $\overline{SHCP}$	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(H)$	Pulse width $\overline{STCP}$	Waveform 1	4.0 5.0			4.0 5.0		ns

6

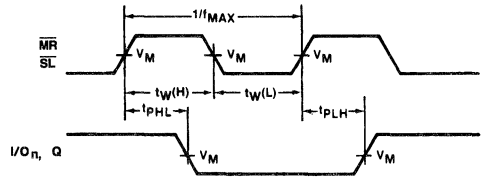
AC WAVEFORMS



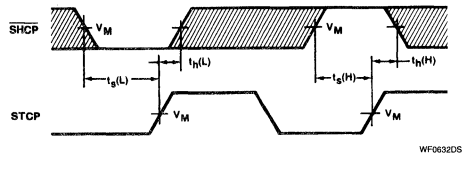
Waveform 1. Clock To Output Delays And Clock Pulse Width



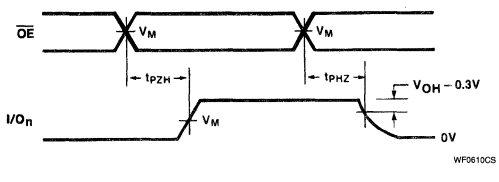
Waveform 2. Data Set-up And Hold Times



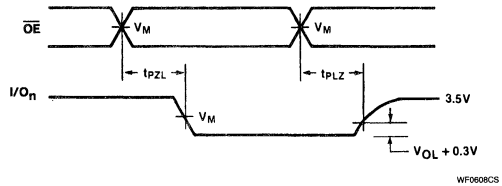
Waveform 3. Master Reset And Serial Load Enable To Output Delays And Pulse Width



Waveform 4. Data Set-up And Hold Times



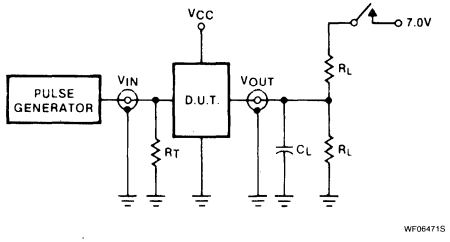
Waveform 5. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



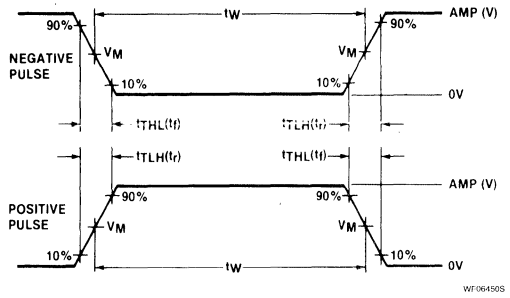
Waveform 6. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F604
Register

Dual Octal Register (3-State)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **3-State outputs**
- **Typical shift frequency of 105 MHz**
- **Power supply current 75mA typical**

DESCRIPTION

The 'F604 contains 16 D-type edge-triggered data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A SELECT (SELECT A/$\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight 3-State outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is LOW: data from the A inputs are selected when SELECT A/$\overline{B}$ is HIGH. Data enters the flip-flops on the rising edge of the Clock (CP) input, which also controls the 3-State outputs. The outputs are enabled when CP is HIGH and disabled when CP is LOW.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F604	105MHz	85mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F604N
Plastic SOL-28	N74F604D

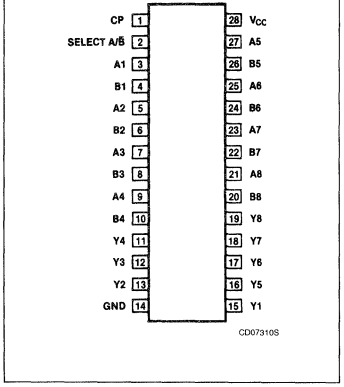
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

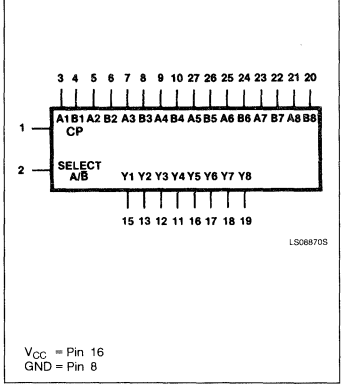
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$	Inputs A	1.0/0.033	20μA/20μA
$B_1 - B_8$	Inputs B	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select inputs	1.0/0.033	20μA/20μA
CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
$Y_1 - Y_8$	Outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

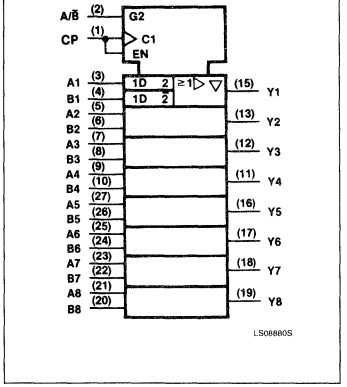
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

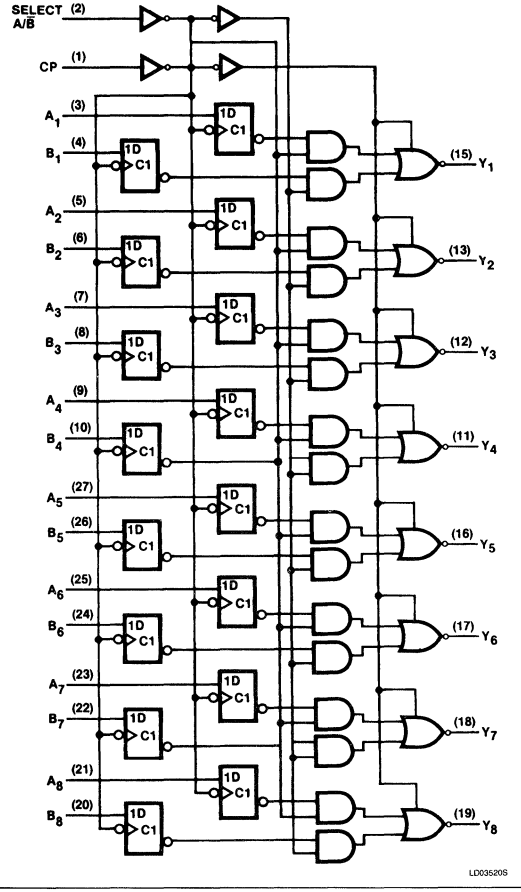


FUNCTION TABLE

INPUTS				OUTPUTS
$A_1 - A_8$	$B_1 - B_8$	SELECT $A/\overline{B}$	CP	$Y_1 - Y_8$
A data	B data	L	I	B data
A data	B data	H	I	A data
X	X	X	L	Z
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = HIGH level (steady state)
L = LOW level (steady state)
X = Don't care
Z = HIGH impedance state
I = Transition from LOW-to-HIGH level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F604			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5			−1	−20	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V			2	50	mA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	A_n, B_n, SELECT A/$\overline{B}$ = 4.5V, CP = ↑		60	82	mA
		I_{CCL}		A_n, B_n, SELECT A/$\overline{B}$ = GND, CP = ↑		75	100	mA
		I_{CCZ}		A_n, B_n, SELECT A/$\overline{B}$ = GND, CP = GND		75	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

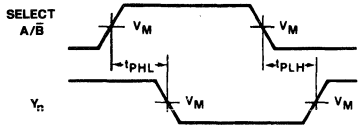
PARAMETER		TEST CONDITIONS	74F604					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 5	95	105		80		MHz
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Y_n	Waveform 2	5.0 6.0	7.0 8.5	9.0 10.5	4.5 5.5	10.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Y_n	Waveform 3	6.0 4.0	8.0 6.5	10.0 8.5	5.5 3.5	11.5 9.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level	Waveform 3, 4	5.0 6.5	7.5 9.0	9.5 11.0	4.5 6.0	10.5 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 3, 4	5.0 5.0	7.0 7.0	9.5 9.5	4.5 4.5	11.0 11.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

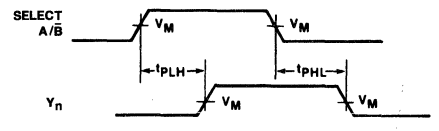
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F604					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 5	1 2			2 3		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 4	0 1			0 1.5		ns
$t_w(H)$	Clock pulse width, HIGH	Waveform 4	5			6		ns

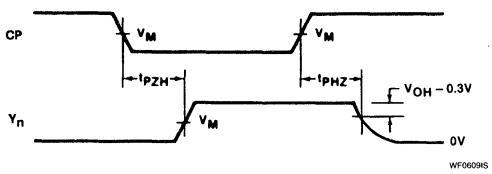
AC WAVEFORMS



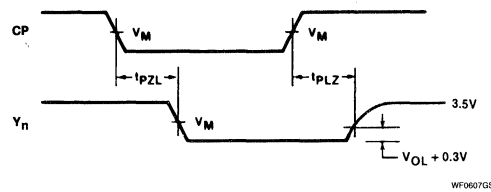
Waveform 1. Propagation Delay Select A/$\overline{B}$ To Output (Y_n) (A Register Stored Data = L, CP = H)



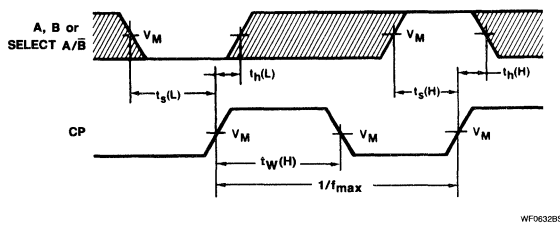
Waveform 2. Propagation Delay Select A/$\overline{B}$ To Output (Y_n) (B Register Stored Data = L, CP = H)



Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time Frof HIGH Level



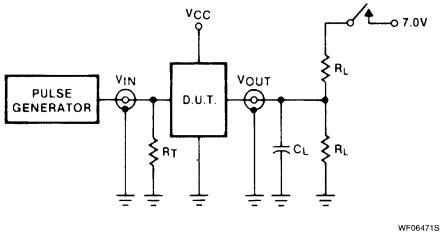
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

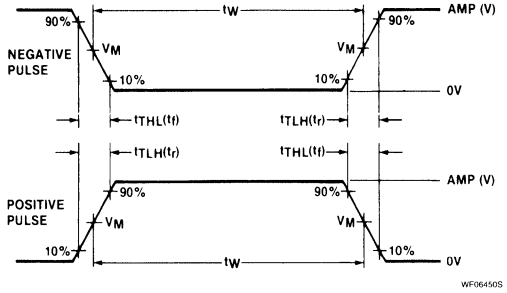


Waveform 5. Data And Select Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS





Test Circuit For 3-State Outputs

Input Pulse Definition

$V_M = 1.5V$

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

6

Signetics

FAST 74F605 Register

Dual Octal Register (Open Collector)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Stores 16-bit-wide data inputs, multiplexed 8-bit outputs**
- **Open-collector outputs**
- **Propagation delay 10ns typical**
- **Power supply current 85mA typical**

DESCRIPTION

The 'F605 contains 16 D-type edge-triggered flip-flops with common clock and individual data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A SELECT (SELECT A/$\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight open-collector outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is LOW; data from the A inputs are selected when SELECT A/$\overline{B}$ is HIGH. Data enters the flip-flops on the rising edge of the Clock (CP) input, which also controls the open-collector outputs. The outputs are enabled when CP is HIGH and disabled when CP is LOW.

These functions are well suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F605	105MHz	85mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F605N
Plastic SOL-28	N74F605D

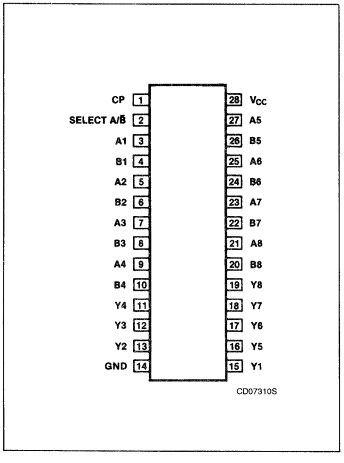
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

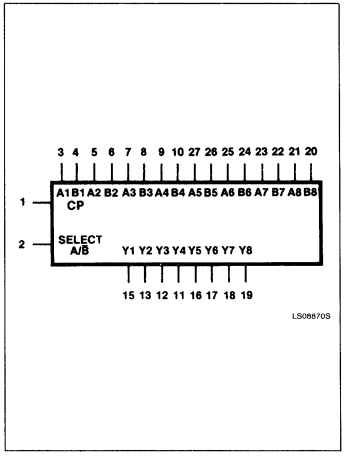
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$	Inputs A	1.0/0.033	20μA/20μA
$B_1 - B_8$	Inputs B	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20μA/20μA
CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
$Y_1 - Y_8$	Outputs	*OC /33.3	*OC /20mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. *OC = Open Collector.

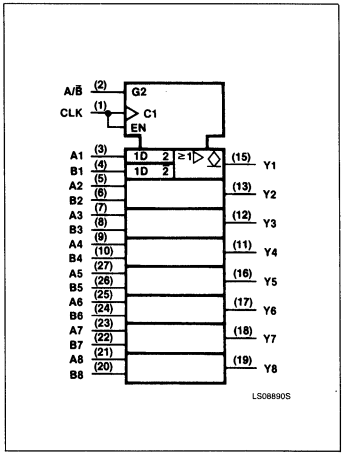
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

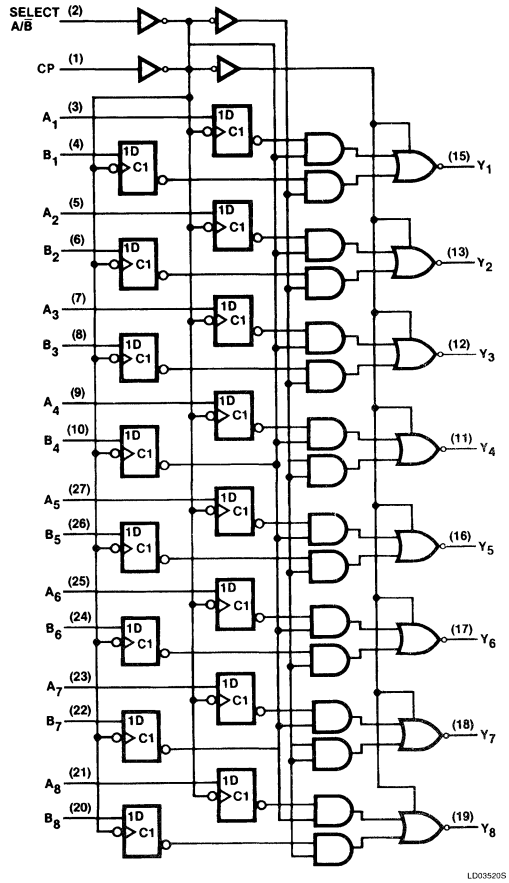


FUNCTION TABLE

INPUTS				OUTPUTS
$A_1 - A_8$	$B_1 - B_8$	SELECT $A/\overline{B}$	CP	$Y_1 - Y_8$
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z or Off
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = HIGH level (steady state)
L = LOW level (steady state)
Off = H if pull-up resistor is connected to Open-Collector output
X = Don't care
Z = High-impedance state
↑ = Transition from LOW-to-HIGH level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
i_{IN}	input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F605 Min	74F605 Typ[2]	74F605 Max	UNIT
I_{OH}	HIGH-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 4.5V				250	μA
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	± 10%V_{CC}		0.35	0.50	V
				± 5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			-1	-20	μA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	A_n = B_n = SELECT A/$\overline{B}$ = 4.5V, CP = ↑		80	100	mA
		I_{CCL}		A_n = B_n = SELECT A/$\overline{B}$ = GND, CP = ↑		85	105	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

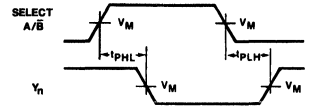
PARAMETER		TEST CONDITIONS	74F605 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F605 T_A = 0 to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 4	95	105		80		MHz
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Y_n	Waveform 2	7.5 7.5	9.5 10.0	11.5 12.0	7.0 7.0	12.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Y_n	Waveform 3	8.5 6.5	11.0 8.5	13.0 11.0	8.0 6.0	14.5 11.5	ns
t_{PLH} t_{PHL}	Clock pulse width	Waveform 2	8.5 6.5	11.0 9.0	13.0 11.0	8.0 6.0	14.5 12.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

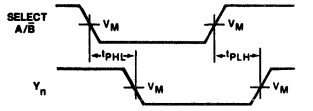
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F605 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F605 T_A = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_s(H) t_s(L)	Set-up time, HIGH or LOW A_n, B_n, Select A/$\overline{B}$ to CP	Waveform 4	1 3			2 4		ns ns
t_h(H) t_h(L)	Hold time, HIGH or LOW A_n, B_n, Select A/$\overline{B}$ to CP	Waveform 4	1 2			2 3		ns ns
t_w	Clock pulse width	Waveform 4	5			6		ns

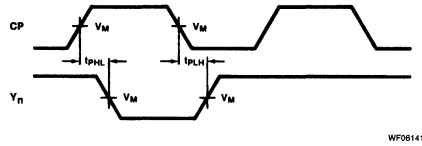
AC WAVEFORMS



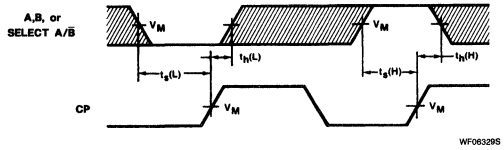
Waveform 1. Propagation Delay SELECT A/$\overline{B}$ To Output (Y_n) (A Register stored data = L, CP = H)



Waveform 2. Propagation Delay SELECT A/$\overline{B}$ To Output (Y_n) (B Register stored data = L, CP = H)



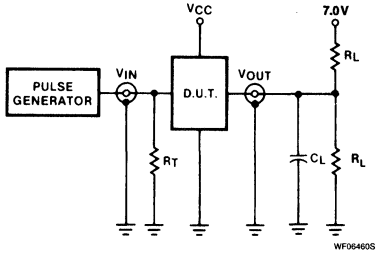
Waveform 3. Clock To Output Delays (SELECT A/$\overline{B}$ = H)



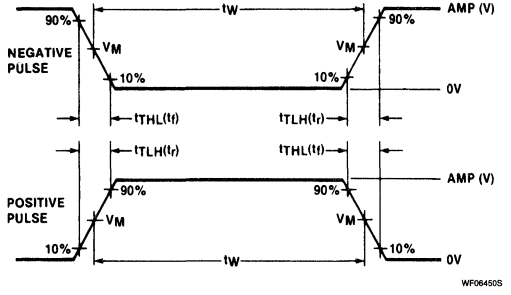
Waveform 4. Data And SELECT Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open-Collector Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F620, F623 Transcievers

Octal Bus Transceiver
('F620 — Inverting 3-State)
('F623 — Non-Inverting 3-State)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 64mA and source 15mA**
  - **'F620, inverting**
  - **'F623, non-inverting**

DESCRIPTION

The 'F623 is an octal transceiver featuring non-inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 'F620 is an inverting version of the 'F623.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F620	3.5ns	75mA
74F623	4.5ns	105mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F620N, N74F623N
Plastic SOL-20	N74F620D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

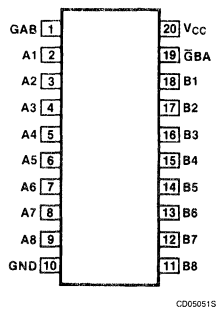
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$, $B_1 - B_8$	Data inputs	3.5/0.116	70μA/70μA
$\overline{G}BA$, GAB	3-State output enable inputs (active LOW)	1.0/0.033	20μA/20μA
$A_1 - A_8$	Data outputs	150/40	3mA/24mA
$B_1 - B_8$	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

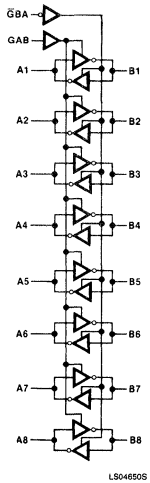
PIN CONFIGURATION

'F620



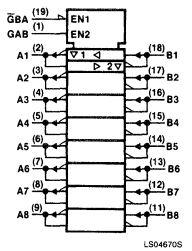
LOGIC SYMBOL

'F620



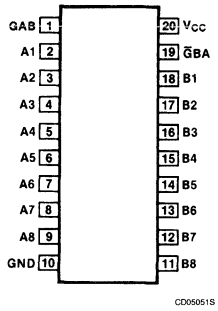
LOGIC SYMBOL (IEEE)

'F620



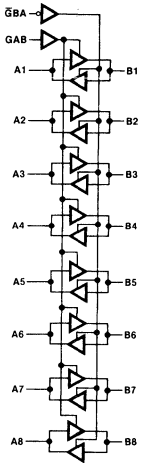
PIN CONFIGURATION

'F623



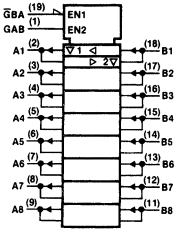
LOGIC SYMBOL

'F623



LOGIC SYMBOL (IEEE)

'F623



These devices allow data transmisstion from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{G}BA$ and GAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'F620 and 'F623 the capability to store data by simultaneous enabling of $\overline{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
$\overline{G}BA$	GAB	'F620	'F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	(Z)	(Z)
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER		74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	$A_1 - A_8$	48	mA
		$B_1 - B_8$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_1 - A_8$			−3	mA
		$B_1 - B_8$			−15	mA
I_{OL}	LOW-level output current	$A_1 - A_8$			24	mA
		$B_1 - B_8$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F620, 'F623			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$A_1 - A_8$ $B_1 - B_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_1 - B_8$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	$A_1 - A_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
		$B_1 - B_8$		I_{OL} = 48mA	±10%V_{CC}		.40	.55	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$\overline{G}BA$, GAB	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		Others	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	HIGH-level input current	$\overline{G}BA$, GAB only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V					−20	µA
I_{OZH} + I_{IH}	Off-state current HIGH-level voltage applied	$A_1 - A_8$ $B_1 - B_8$	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off-state current LOW-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−70	µA
I_{OS}	Short-circuit output current[3]	$A_1 - A_8$	V_{CC} = MAX			−60		−150	mA
		$B_1 - B_8$				−100		−225	mA
I_{CC}	Supply current (total)	'F620 I_{CCH}	V_{CC} = MAX	$\overline{G}BA$ = GAB = 4.5V; $A_1 - A_8$ = GND			70	92	mA
		'F620 I_{CCL}		$\overline{G}BA$ = GAB = 4.5V; $A_1 - A_8$ = 4.5V			84	110	mA
		'F620 I_{CCZ}		GAB = GND; $\overline{G}BA$ = $A_1 - A_8$ = 4.5V			70	92	mA
		'F623 I_{CCH}		$\overline{G}BA$ = GAB = 4.5V; $A_1 - A_8$ = 4.5V			110	140	mA
		'F623 I_{CCL}		$\overline{G}BA$=GAB = 4.5V; $A_1 - A_8$ = GND			110	140	mA
		'F623 I_{CCZ}		GAB = GND; $\overline{G}BA$ = $A_1 - A_8$ = 4.5V			99	130	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F620					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output enable to HIGH or LOW level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	3.0 4.0	7.5 7.5	10.5 10.5	2.5 3.5	11.5 11.5	ns
t_{PHZ} t_{PLZ}	Output disable from HIGH or LOW level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	7.5 7.0	2.0 1.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output enable to HIGH or LOW level GAB to B_n	Waveform 3 Waveform 4	4.5 4.5	7.5 7.5	10.5 10.0	4.0 4.0	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output disable from HIGH or LOW level GAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.5 6.5	9.5 9.5	2.5 3.5	10.5 10.5	ns

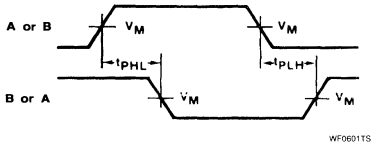
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

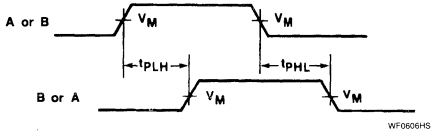
PARAMETER		TEST CONDITIONS	74F623					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.0 3.0	4.0 5.0	5.5 7.0	2.0 2.5	6.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.0 2.5	4.0 4.5	5.5 6.5	2.0 2.5	6.5 7.5	ns
t_{PZH} t_{PZL}	Output enable to HIGH or LOW level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	5.0 5.0	8.5 7.5	10.5 9.5	5.0 5.0	12.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable from HIGH or LOW level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.5 6.5	2.5 2.5	7.5 7.0	ns
t_{PZH} t_{PZL}	Output enable to HIGH or LOW level GAB to B_n	Waveform 3 Waveform 4	5.0 4.5	8.0 7.0	10.0 9.0	5.0 4.5	11.5 9.5	ns
t_{PHZ} t_{PLZ}	Output disable from HIGH or LOW level GAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.0 7.0	8.5 9.0	3.0 4.0	10.0 10.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

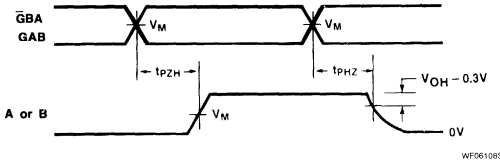
AC WAVEFORMS



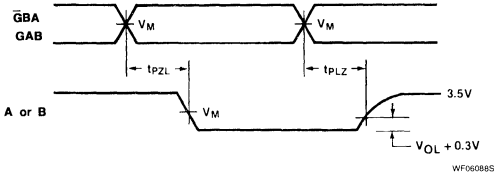
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



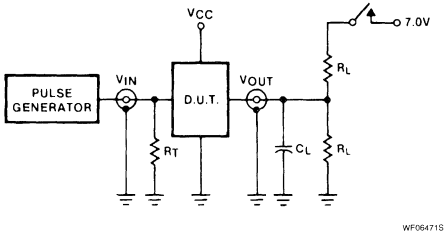
Waveform 3. 3-State Output Enable Time To HIGH Level Output Disable Time From HIGH Level



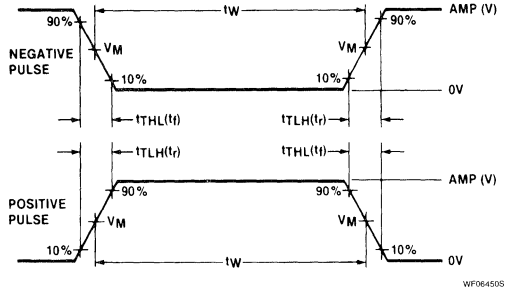
Waveform 4. 3-State Output Enable Time To LOW Level Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F621, F622
Transceivers

Octal Bus Transceiver
'F621 — Non-Inverting (Open Collector)
'F622 — Inverting (Open Collector)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Octal bidirectional bus interface**
- **Open-Collector outputs sink 64mA**
  - **'F621, non-inverting**
  - **'F622, inverting**
- **15mA source current**

DESCRIPTION

The 'F621 is an octal transceiver featuring non-inverting Open-Collector bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 'F622 is an inverting version of the 'F621.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F621	8.0ns	105mA
74F622	8.5ns	53mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F621N, N74F622N
Plastic SOL-20	N74F621D, N74F622D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

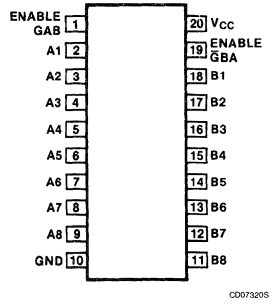
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{G}BA$, GAB	Enable inputs	1.0/0.033	20μA/20μA
$A_1 - A_8$, $B_1 - B_8$	3-State inputs	1.0/0.033	20μA/20μA
$A_1 - A_8$	3-State outputs	*OC/40	*OC/24mA
$B_1 - B_8$	3-State outputs	*OC/106.7	*OC/64mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. *OC = Open Collector

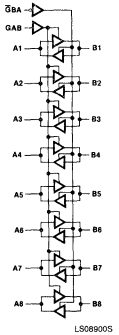
PIN CONFIGURATION

'F621



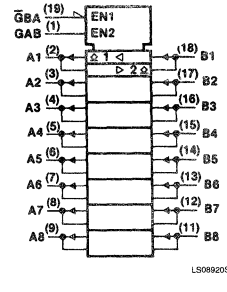
LOGIC SYMBOL

'F621



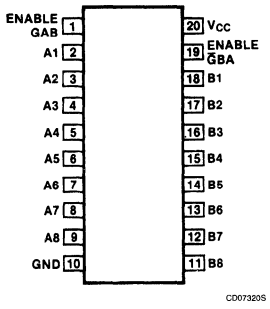
LOGIC SYMBOL (IEEE/IEC)

'F621



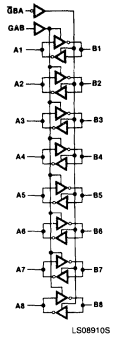
PIN CONFIGURATION

'F622



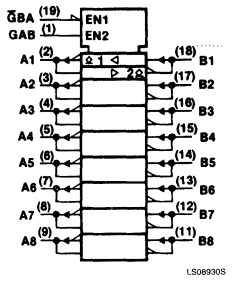
LOGIC SYMBOL

'F622



LOGIC SYMBOL (IEEE/IEC)

'F622



These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{G}$BA and GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated

The dual-enable configuration gives the 'F621 and 'F622 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

FUNCTION TABLE

ENABLE INPUTS		MODE OF OPERATION	
$\overline{G}$BA	GAB	'F621	'F622
L	L	B data to A bus	$\overline{B}$ data to A bus
H	H	A data to B bus	$\overline{A}$ data to B bus
H	L	(Z) or OFF	(Z) or OFF
L	H	B data to A bus, A data to B bus	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (OFF) state
OFF = HIGH if pull-up resistor is connected to Open Collector output

6

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
$\overline{V}_{OH}$	HIGH-level output voltage				4.5	V
I_{OL}	LOW-level output current	$A_1 - A_8$			20	mA
		$B_1 - B_8$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F621, 74F622			UNIT
						Min	Typ[2]	Max	
I_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OL}	LOW-level output voltage	$A_1 - A_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
		$B_1 - B_8$		I_{OL} = 48mA	±10%V_{CC}		.40	.55	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$\overline{G}BA$, GAB	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		Others	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V					−20	μA
I_{CC}	Supply current (total)	'F621 I_{CCH}	V_{CC} = MAX	$\overline{G}BA$ = GAB = 4.5V; $A_1 - A_8$ = 4.5V			105	140	mA
		'F621 I_{CCL}		$\overline{G}BA$ = GAB = 4.5V; $A_1 - A_8$ = GND			105	140	mA
		'F622 I_{CCH}		$\overline{G}BA$ = GAB = 4.5V; $A_1 - A_8$ = GND			37	48	mA
		'F622 I_{CCL}		$\overline{G}BA$ = GAB = 4.5V; $A_1 - A_8$ = 4.5V			68	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	74F621					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A to B	Waveform 2	6.0 4.0	9.5 6.0	12.0 8.0	5.5 3.5	13.0 8.5	ns
t_{PLH} Propagation delay t_{PHL} B to A	Waveform 2	6.0 3.5	9.0 5.5	12.0 7.5	5.5 3.0	12.5 8.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{G}$BA to A	Waveform 3	6.0 3.5	10.0 6.5	13.5 10.5	5.5 3.0	14.0 11.0	ns
t_{PLH} Propagation delay t_{PHL} GAB to B	Waveform 4	7.0 3.5	12.0 6.5	15.0 9.5	6.0 3.0	17.0 10.0	ns

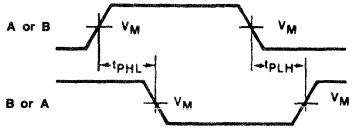
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

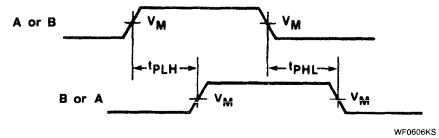
PARAMETER	TEST CONDITIONS	74F622					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A to B	Waveform 1	8.0 1.5	11.0 4.0	12.5 5.5	8.0 1.5	13.5 6.0	ns
t_{PLH} Propagation delay t_{PHL} B to A	Waveform 1	7.5 1.5	10.0 3.5	12.0 5.0	7.5 1.5	12.5 5.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{G}$BA to A	Waveform 3	8.0 6.0	10.5 8.0	12.0 10.0	8.0 6.0	12.5 10.5	ns
t_{PLH} Propagation delay t_{PHL} GAB to B	Waveform 4	10.0 5.0	12.5 7.5	14.5 9.0	10.0 5.0	15.5 9.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

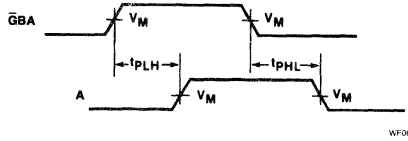
AC WAVEFORMS



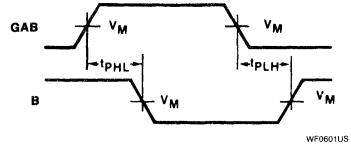
Waveform 1. Propagation Delay For A To B Or B To A (F622)



Waveform 2. Propagation Delay For A To B Or B To A (F621)



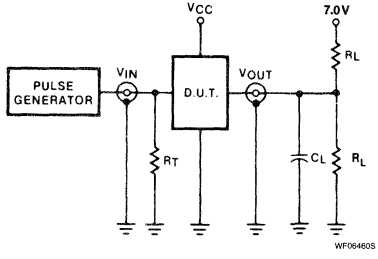
Waveform 3. Propagation Delay For GBA To A



Waveform 4. Propagation Delay For GAB To B

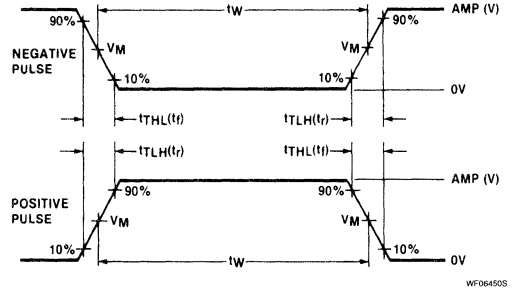
NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F630, 74F631
Error Detection Correction

16-Bit Parallel Error Detection and Correction
('F630 — 3-State)
('F631 — Open-Collector)
Preliminary Specification

FEATURES

- **High impedance NPN base input for reduced loading (20μA in HIGH and LOW states)**
- **Detects and corrects single-bit errors**
- **Detects and flags dual-bit errors**
- **Fast processing times:**
  - **Write cycle: Generates check word in 20ns typical**
  - **Read cycle: Flags errors in 25ns typical**
- **Power dissipation 600mW (typical)**
- **Choice of output configurations**
  - **'F630: 3-State**
  - **'F631: Open-Collector**

DESCRIPTION

The 'F630 and 'F631 devices are 16-bit parallel error detection and correction circuits (EDACs) in 28-pin, 600-mil packages. They use a modified Hamming code to generate a 6-bit check word from a 16-bit data word.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F630	17ns	120mA
74F631	17ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F630N, N74F631N
Plastic SOL-28	N74F630D, N74F631D

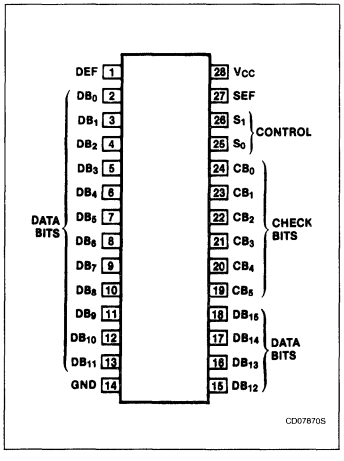
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
S_0, S_1	Control	1.0/0.033	20μA/20μA
$CB_0 - CB_{15}$	Check bits, input	1.0/0.033	20μA/20μA
$DB_0 - DB_{15}$	Data bits, input	1.0/0.033	20μA/20μA
$CB_0 - CB_{15}$	Check bits, output for 'F630	150/33.3	3mA/20mA
$CB_0 - CB_{15}$	Check bits, output for 'F631	*OC/33.3	*OC/20mA
$DB_0 - DB_{15}$	Data bits, output for 'F630	150/33.3	3mA/20mA
$DB_0 - DB_{15}$	Data bits, outputs for 'F631	*OC/33.3	*OC/20mA
SEF, DEF	Error flags outputs for 'F630	150/33.3	3mA/20mA
SEF, DEF	Error flags outputs for 'F631	*OC/33.3	*OC/20mA

NOTES:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
*OC = Open Collector

PIN CONFIGURATION



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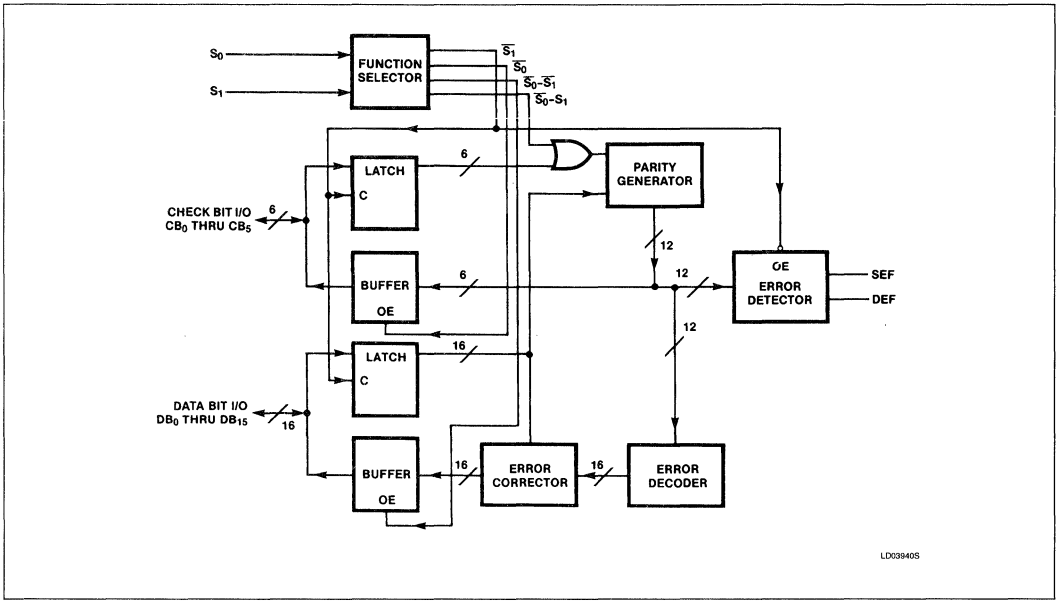
LOGIC DIAGRAM



This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected.

Single-bit errors in the 6-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 16-bit word is not in error. The correction cycle will simply pass along the original 16-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. Thes e dual errors may occur in any 2 bits of the 22-bit word from memory (two errors in the 16-bit data word, two errors in the 6-bit check word, or one error in each word).

The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 16-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

ERROR DETECTION AND CORRECTION DETAILS

During a memory write cycle, six check bits ($CB_0 - CB_5$) are generated by eight-input parity generators using the data bits as defined below. During a memory read cycle, the 6-bit check word is retrieved along with the actual data.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits is correct, it is assumed that no error has occurred and both error flags will be low. (It should be noted that the sense of two of the check bits, CB_0 and CB_1, is inverted to ensure that the gross-error condition of all lows and all highs is detected.)

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high.

Any single error in the 16-bit data word will change the sense of exactly 3 bits of the 6-bit check word. Any single error in the 6-bit check word changes the sense of only that one bit. In either case, the single-error flag will be set high while the dual-error flag will remain low.

Any 2-bit error will change the sense of an even number of check bits. The 2-bit error is not correctable, since the parity tree can only identify single-bit errors. Both error flags are set high when any 2-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit data word and 6-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the check word I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

FUNCTION TABLE

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
16-Bit Data	6-Bit Checkword	SEF	DEF	
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

H = HIGH voltage level, L = LOW voltage level

CHECK WORD BIT	16-BIT DATA WORD															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB_0	X	X		X	X				X	X	X			X		
CB_1	X		X	X		X	X		X			X			X	
CB_2		X	X		X	X		X		X			X			X
CB_3	X	X	X				X	X			X	X	X			
CB_4				X	X	X	X	X						X	X	X
CB_5									X	X	X	X	X	X	X	X

NOTE:
The six check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

ERROR SYNDROME TABLE

ERROR LOCATION	SYNDROME ERROR CODE					
	CB_0	CB_1	CB_2	CB_3	CB_4	CB_5
DB_0	L	L	H	L	H	H
DB_1	L	H	L	L	H	H
DB_2	H	L	L	L	H	H
DB_3	L	L	H	H	L	H
DB_4	L	H	L	H	L	H
DB_5	H	L	L	H	L	H
DB_6	H	L	H	L	L	H
DB_7	H	H	L	L	L	H
DB_8	L	L	H	H	H	L
DB_9	L	H	L	H	H	L
DB_{10}	L	H	H	L	H	L
DB_{11}	H	L	H	L	H	L
DB_{12}	H	H	L	L	H	L
DB_{13}	L	H	H	H	L	L
DB_{14}	H	L	H	H	L	L
DB_{15}	H	H	L	H	L	L
CB_0	L	H	H	H	H	H
CB_1	H	L	H	H	H	H
CB_2	H	H	L	H	H	H
CB_3	H	H	H	L	H	H
CB_4	H	H	H	H	L	H
CB_5	H	H	H	H	H	L
No Error	H	H	H	H	H	H

H = HIGH voltage level
L = LOW voltage level

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage	'F631			4.5	V
I_{OH}	HIGH-level output current	'F630			−3	mA
I_{OL}	LOW-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F630			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				+5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V			2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX					mA
		I_{CCL}						mA
		I_{CCZ}						mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F631			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OH}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX					mA
		I_{CCL}						mA
		I_{CCZ}						mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER	TEST CONDITIONS	74F630					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} DB to CB	Waveform 1			22 20			ns
t_{PLH} Propagation delay t_{PHL} SI to DEF, SEF	Waveform 1			13 12			ns
t_{PZH} Output enable time to HIGH level, t_{PZL} SO to CB, DB	Waveform 3 & 4			12 12			ns
t_{PHZ} Output disable time from HIGH level, t_{PLZ} SO to CB, DB	Waveform 3 & 4			15 15			ns

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

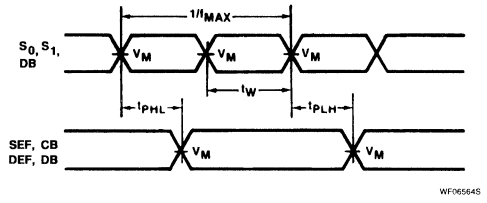
PARAMETER	TEST CONDITIONS	74F631					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} DB to CB	Waveform 1			25 18			ns
t_{PLH} Propagation delay t_{PHL} SI to DEF, SEF	Waveform 1			16 11			ns
t_{PHL} Propagation delay time, HIGH-to-LOW t_{PLH} level output, SO to CB, DB	Waveform 1			12 16			ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

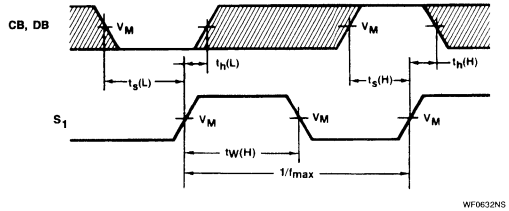
AC SET-UP REQUIREMENTS

PARAMETER	TEST CONDITIONS	74F630, 'F631					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_s Set-up time, CB or DB to SI	Waveform 2	4					ns
t_h Hold time, CB or DB to SI	Waveform 2	4					ns

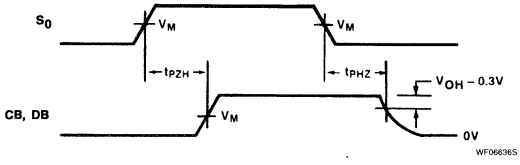
AC WAVEFORMS



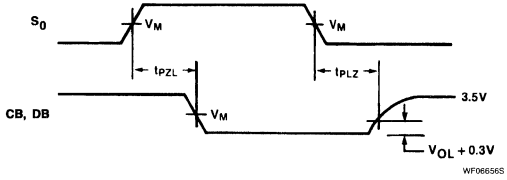
Waveform 1.
DB To CB
S_I To DEF, SEF
S_O To CB, DB
} Delays



Waveform 2. Data Set-up And Hold Times



Waveform 3. 3-State Enable Time To HIGH Level And Disable Time From HIGH Level



Waveform 4. 3-State Enable Time To LOW Level And Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

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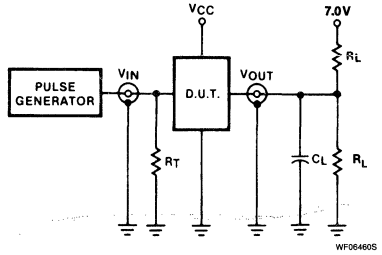
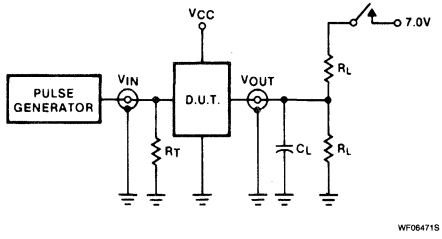
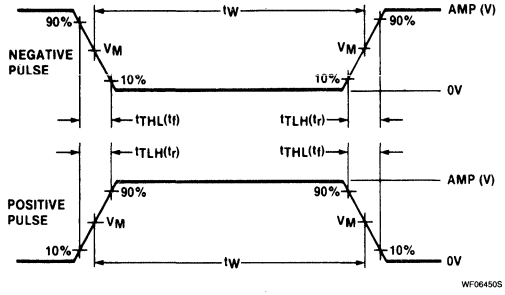
TEST CIRCUITS AND WAVEFORMS



Test Circuit For Open Collector Outputs ('F631)



Test Circuit For 3-State Outputs ('F630)



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SWITCH POSITION

TEST	SWITCH
t_{PZH}	open
t_{PZL}	closed
t_{PHZ}	open
t_{PLZ}	closed

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F640 Transceiver

Octal Bus Transceiver, Inverting (3-State)
Product Specification

Logic Products

FEATURES

- High impedance NPN base inputs for reduced loading (70μA in HIGH and LOW states)
- Ideal for applications which require high output drive and minimal bus loading
- Inverting version of 'F245
- Octal bidirectional bus interface
- 3-State buffer outputs sink 64mA and source 15mA

DESCRIPTION

The 'F640 is an octal transceiver featuring inverting 3-State bus-compatible outputs in both send and receive directions.

The $B_1 - B_8$ outputs are capable of sinking 64mA and sourcing 15mA, providing very good capacitive drive characteristics.

These octal bus transceivers are designed for asynchronous two-way communication between data busses.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F640	3.5ns	78mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F640N
Plastic SOL-20	N74F640D

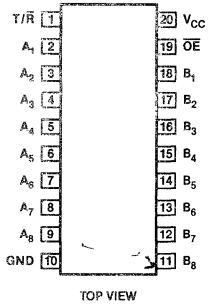
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

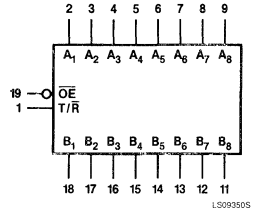
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$, $B_1 - B_8$	Data inputs	3.5/0.115	70uA/70μA
$T/\overline{R}$	Transmit/receive input	2.0/0.067	40uA/40μA
$\overline{OE}$	Output enable inputs (active LOW)	2.0/0.067	40uA/40μA
$A_1 - A_8$	Data outputs	150/40	3mA/24mA
$B_1 - B_8$	Data outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

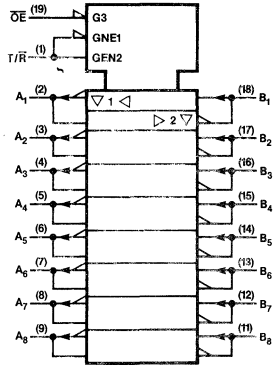


LOGIC SYMBOL



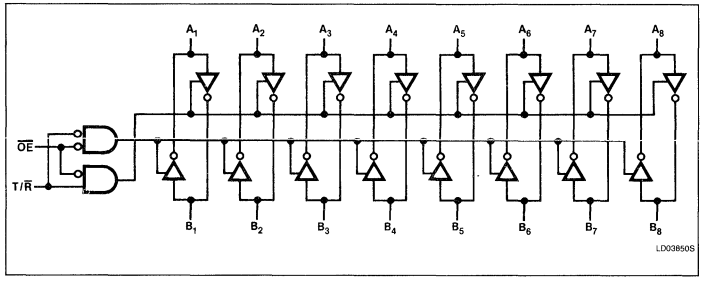
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



6

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus $\overline{B}$ data to Bus A
L	H	Bus $\overline{A}$ data to Bus B
H	X	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	$A_1 - A_8$	48	mA
		$B_1 - B_8$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_1 - A_8$			−3	mA
		$B_1 - B_8$			−15	mA
I_{OL}	LOW-level output current	$A_1 - A_8$			24	mA
		$B_1 - B_8$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74F640			UNIT
					Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	$A_1 - A_8$, $B_1 - B_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
	$B_1 - B_8$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL} LOW-level output voltage	$A_1 - A_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
	$B_1 - B_8$		I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
			I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I Input current at maximum input voltage	$A_1 - A_8$, $B_1 - B_8$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
	$\overline{OE}$, $T/\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH} HIGH-level input current	$\overline{OE}$, $T/\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL} LOW-level input current	$\overline{OE}$, $T/\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					−40	µA
I_{IH}+ I_{OZH} Off-state current HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_I = 2.7V					70	µA
I_{IL}+ I_{OZL} Off-state current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_I = 0.5V					−70	µA
I_{OS} Short-circuit output current[3]	$A_1 - A_8$	V_{CC} = MAX			−60		−150	mA
	$B_1 - B_8$				−100		−225	mA
I_{CC} Supply current (total)	I_{CCH}	V_{CC} = MAX	$T/\overline{R}$ = $A_1 - A_8$ = 4.5V; $\overline{OE}$ = GND			66	85	mA
	I_{CCL}		$\overline{OE}$ = $T/\overline{R}$ = $B_1 - B_8$ = GND			91	120	mA
	I_{CCZ}		$\overline{OE}$ = 4.5V; $T/\overline{R}$ = $B_1 - B_8$ = GND			78	102	mA

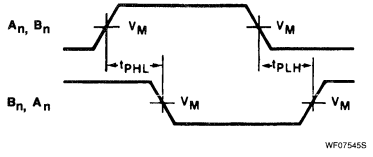
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

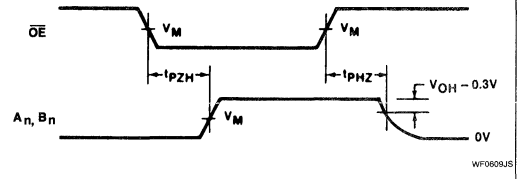
PARAMETER	TEST CONDITIONS	74F640					UNIT
		T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A_n to B_n, B_n to A_n	Waveform 1	2.0 1.0	4.5 2.5	7.0 5.0	2.0 1.0	8.0 5.5	ns
t_{PZH} Output enable time t_{PZL} to HIGH or LOW level	Waveform 2 Waveform 3	6.0 6.0	9.0 9.0	11.0 11.0	6.0 6.0	13.0 11.5	ns
t_{PHZ} Output disable time t_{PLZ} from HIGH or LOW level	Waveform 2 Waveform 3	2.5 2.0	5.5 4.5	8.0 7.0	2.5 2.0	9.0 7.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

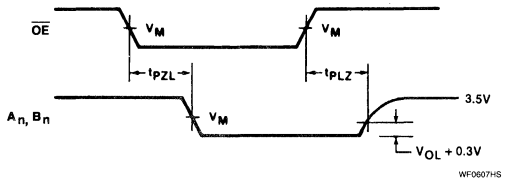
AC WAVEFORMS



Waveform 1. Propagation Delays For A_n To B_n Or B_n To A_n



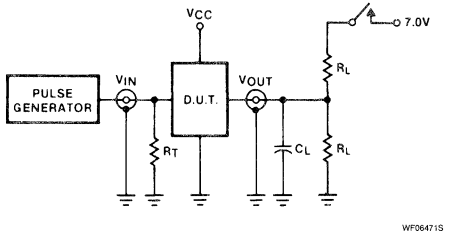
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



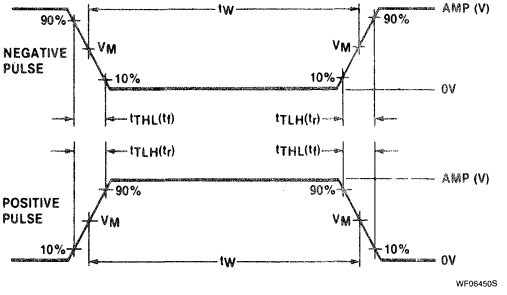
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

Logic Products

FAST 74F641, 74F642
Transceivers

'F641 – Octal Bus Transceiver with Common Output Enable, Non-Inverting (Open Collector)
'F642 – Octal Bus Transceiver with C
Product Specification

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)
- Octal bidirectional bus interface
- Common Output Enable for both Transmit and Receive modes
- Open-Collector outputs sink 64mA
- 'F641 Non-inverting
  'F642 Inverting

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F641	8.0ns	69mA
74F642	8.5ns	52mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F641N, N74F642N
Plastic SOL-20	N74F641D, N74F642D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE 'F641

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	(Z)	(Z)

FUNCTION TABLE 'F642

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	INPUTS
L	H	INPUTS	B = $\overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z)= HIGH impedance state

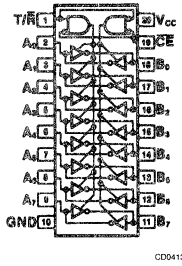
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$, $B_0 - B_7$	Data inputs	1.0/0.033	20μA/20μA
T/$\overline{R}$	Transmit/receive input	2.0/0.067	40μA/40μA
$\overline{OE}$	Common output enable input (active LOW)	2.0/0.067	40μA/40μA
$A_0 - A_7$	Data outputs	*OC/33	*OC/20mA
$B_0 - B_7$	Data outputs	*OC/106.7	*OC/64mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. *OC = Open Collector

PIN CONFIGURATION

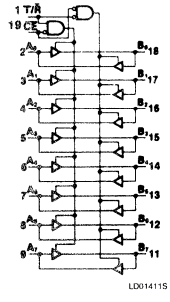
'F641



CD04131S

LOGIC SYMBOL

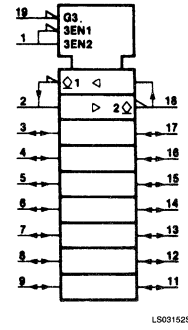
'F641



LD01411S

LOGIC SYMBOL (IEEE/IEC)

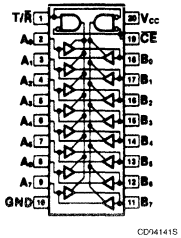
'F641



LS03152S

PIN CONFIGURATION

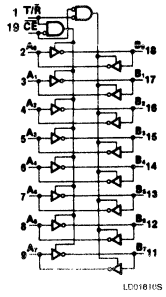
'F642



CD04141S

LOGIC SYMBOL

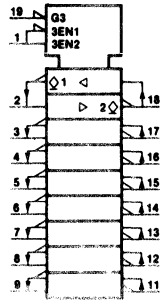
'F642



LD01810S

LOGIC SYMBOL (IEEE/IEC)

'F642



LD01965S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$	40	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage				4.5	V
I_{OL}	LOW-level output current	$A_0 - A_7$			20	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F641/74F642 Min	74F641/74F642 Typ[2]	74F641/74F642 Max	UNIT
I_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OL}	LOW-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
		$B_0 - B_7$		I_{OL} = 48mA	±10%V_{CC}		.40	.55	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	T/$\overline{R}$, $\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_i = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	T/$\overline{R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 2.7V					40	μA
		$A_0 - A_7$, $B_0 - B_7$						20	μA
I_{IL}	LOW-level input current	T/$\overline{R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					−40	μA
		$A_0 - A_7$, $B_0 - B_7$						−20	μA
I_{CC}	Supply current (total)	'F641 I_{CCH}	V_{CC} = MAX	A_n = T/$\overline{R}$ = 4.5V; $\overline{OE}$ = GND			60	90	mA
		'F641 I_{CCL}		T/$\overline{R}$ = 4.5V; A_n = $\overline{OE}$ = GND			78	120	mA
		'F642 I_{CCH}		A_n = T/$\overline{R}$ = $\overline{OE}$ = 4.5V			37	55	mA
		'F642 I_{CCL}		A_n = T/$\overline{R}$ = 4.5V; $\overline{OE}$ = GND			67	98	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F641 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F641 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay	Waveform 2	7.5	10.0	12.5	7.5	13.0	ns
t_{PHL}	A_n to B_n		4.0	6.0	9.5	4.0	11.0	
t_{PLH}	Propagation delay	Waveform 2	6.0	9.5	12.0	6.0	12.0	ns
t_{PHL}	B_n to A_n		3.5	5.5	7.5	3.5	8.0	
t_{PLH}	Propagation delay	Waveform 3	7.0	10.5	12.5	7.0	13.0	ns
t_{PHL}	$\overline{OE}$ to A_n		5.0	7.0	9.0	5.0	10.0	
t_{PLH}	Propagation delay	Waveform 4	9.0	10.5	12.5	9.0	13.5	ns
t_{PHL}	$\overline{OE}$ to B_n		5.5	7.5	9.5	5.5	10.5	

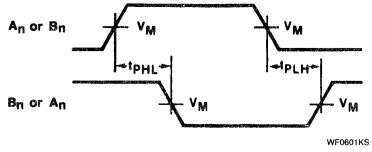
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

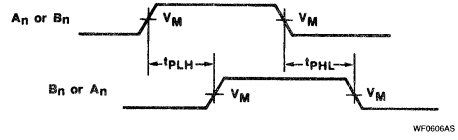
PARAMETER		TEST CONDITIONS	74F642					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	9.0 2.0	11.5 4.5	13.5 6.5	9.0 2.0	14.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	8.5 1.5	10.5 4.0	12.5 6.0	8.5 1.5	13.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	Waveform 3	8.5 6.0	10.5 8.0	12.5 10.5	8.5 6.0	13.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	Waveform 4	9.0 6.5	11.5 9.0	13.5 11.0	9.0 6.5	14.0 11.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

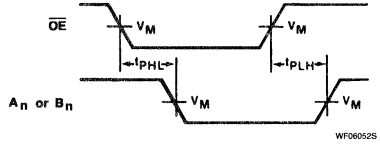
AC WAVEFORM



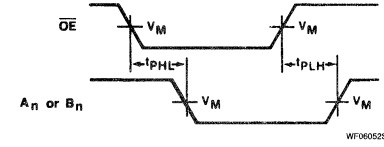
Waveform 1. Propagation Delay For A_n To B_n Or B_n To A_n (F642)



Waveform 2. Propagation Delays For A_n To B_n Or B_n To A_n (F641)



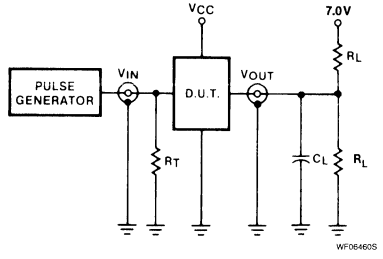
Waveform 3. Propagation Delay For $\overline{OE}$ To A_n Or B_n Outputs ('F642) (B_n Or A_n Inputs In HIGH State)



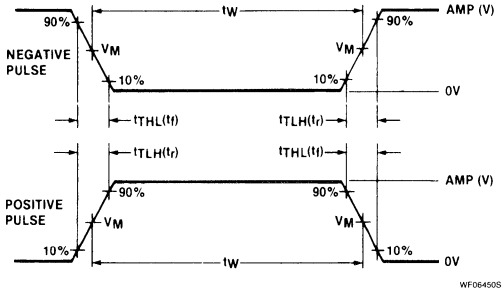
Waveform 4. Propagation Delays For $\overline{OE}$ To A_n Or B_n Outputs ('F641) (B_n Or A_n Inputs In LOW State)

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open-Collector Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

Logic Products

FAST 74F646, 74F648
Transceivers/Registers

'F646 — Octal Transceiver/Register, Non-Inverting (3-State)
'F648 — Octal Transceiver/Register, Inverting (3-State)
Preliminary Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-State outputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F646	7.5ns	115mA
74F648	7.5ns	115mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F646N, N74F648N
Plastic SOL-24	N74F646D, N74F648D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

DESCRIPTION

These devices consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable $\overline{G}$ and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (S) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Enable $\overline{G}$ is active (LOW). In the isolation mode (Enable G, HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed with the 'F646 and 'F648.

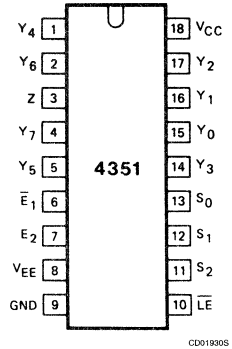
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$, $B_1 - B_8$	A and B inputs	1/0.033	20μA/20μA
CPAB, CPBA	Clock pulse input	1/0.033	20μA/20μA
SAB, SBA	Transmit/receive input	1/0.033	20μA/20μA
DIR, $\overline{G}$	Output enable inputs	1/0.033	20μA/20μA
$A_1 - A_8$, $B_1 - B_8$	A and B outputs	150/33.3	3mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

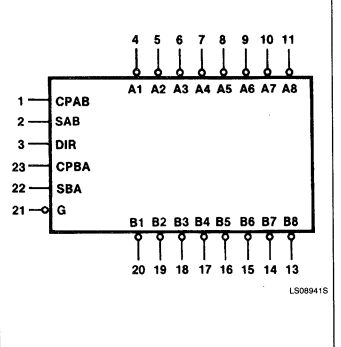
PIN CONFIGURATION

'F646



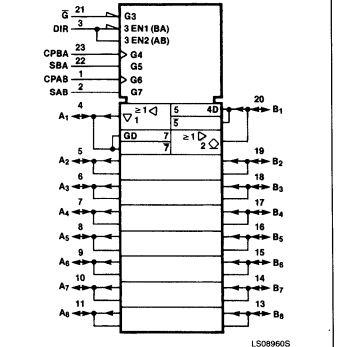
LOGIC SYMBOL

'F646



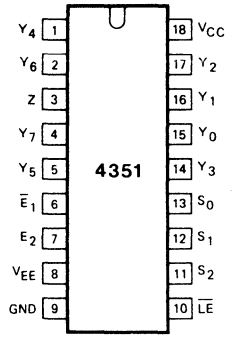
LOGIC SYMBOL (IEEE/IEC)

'F646



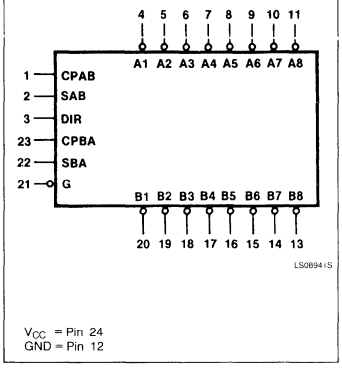
PIN CONFIGURATION

'F648



LOGIC SYMBOL

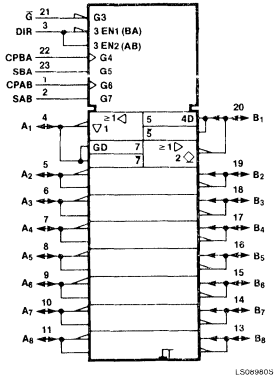
'F648



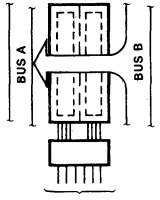
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

'F648

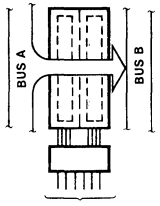


REAL-TIME TRANSFER BUS B TO BUS A



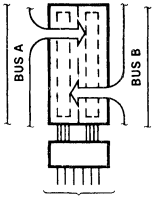
(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
H	L	X	X	X	L

REAL-TIME TRANSFER BUS A TO BUS B



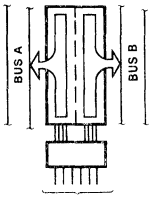
(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
H	L	X	X	L	X

STORAGE



(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
X	H	↑	↑	X	X

TRANSFER STORAGE DATA TO A OR B



(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
L	L	H or L	H or L	X	X
H				H	X

Figure 1

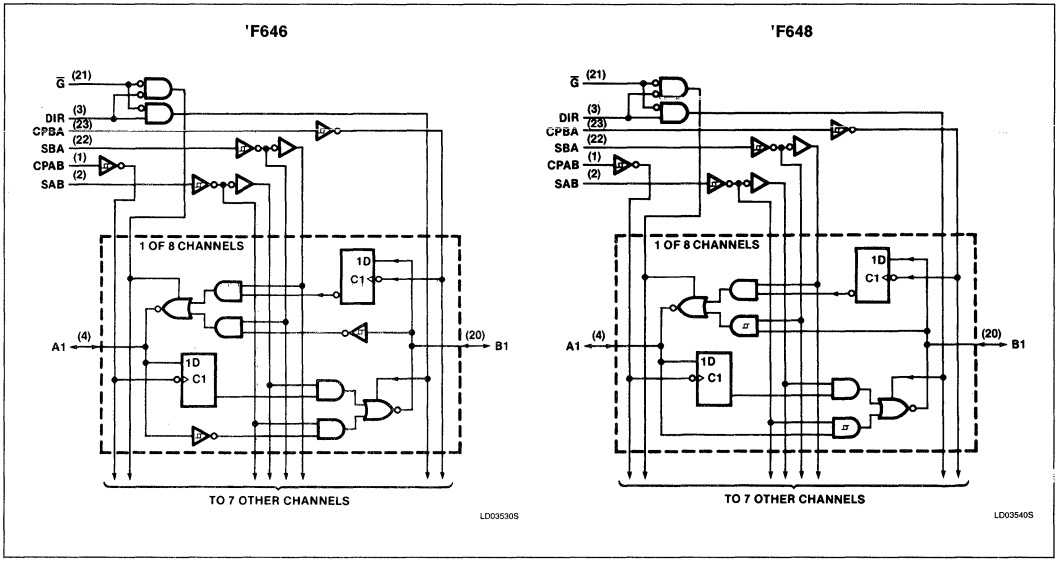
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	$A_1 - A_8$	$B_1 - B_8$	'F646, 'F647	'F648, 'F649
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B data	Store A and B data
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	X	X	H			Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Stored A data to B bus	Stored $\overline{A}$ data to B bus

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

H = high level X = irrelevant
L = low level ↑ = low-to-high level transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F646, 'F648 Min	74F646, 'F648 Typ[2]	74F646, 'F648 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−1	−20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			60	82	mA
		I_{CCL}				75	100	mA
		I_{CCZ}				75	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

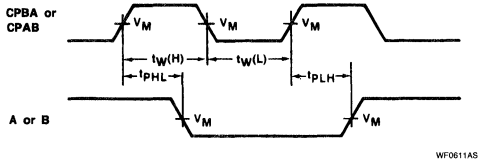
PARAMETER		TEST CONDITIONS	74F646, 'F648 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F646, 'F648 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A or B	Waveform 1						ns
t_{PLH} t_{PHL}	Propagation delay A or B to B or A	Waveform 2, 3						ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A or B	Waveform 2, 3						ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A or B	Waveform 2, 3						ns
t_{PZH} t_{PZL}	Output enable time $\overline{G}$ to A or B	Waveform 4 Waveform 5						ns
t_{PZH} t_{PZL}	Output enable time DIR to A or B	Waveform 4 Waveform 5						ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{G}$ to A or B	Waveform 4 Waveform 5						ns
t_{PHZ} t_{PLZ}	Output disable time DIR to A or B	Waveform 4 Waveform 5						ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

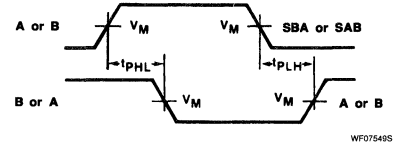
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F646, 'F648					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW A or B to CPBA or CPAB	Waveform 6						ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A or B to CPBA or CPAB	Waveform 6						ns
t_w	Clock pulse width	Waveform 1						ns

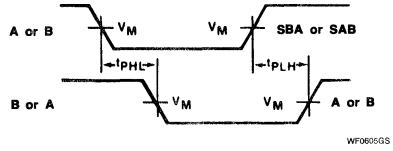
AC WAVEFORMS



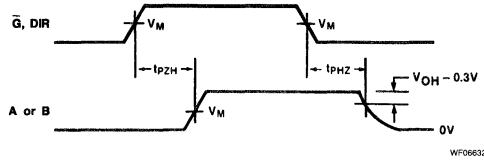
Waveform 1. Clock To Bus Delays, Clock Pulse Width



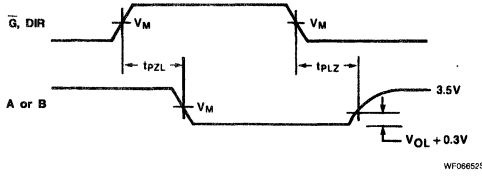
Waveform 2. Propaation Delay SELECT A/$\overline{B}$ To Output (Y_n) (A Register Stored Data = L, CP = H)



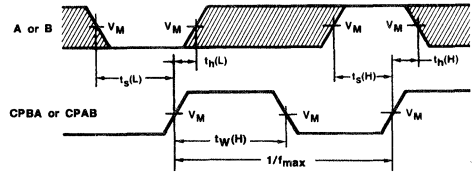
Waveform 3. Propaation Delay SELECT A/$\overline{B}$ To Output (Y_n) (B Register Stored Data = L, CP = H)



Waveform 4. 3-State Enable Time To HIGH Level And Disable Time From HIGH Level



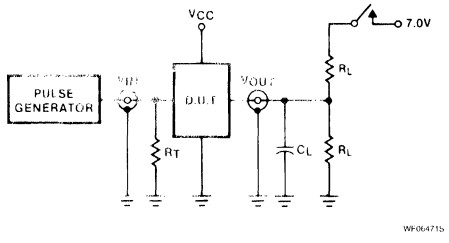
Waveform 5. 3-State Enable Time To LOW Level And Disable Time From LOW Level



Waveform 6. Data and Select Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



WF064715

Test Circuit For 3-State Outputs

SWITCH POSITION

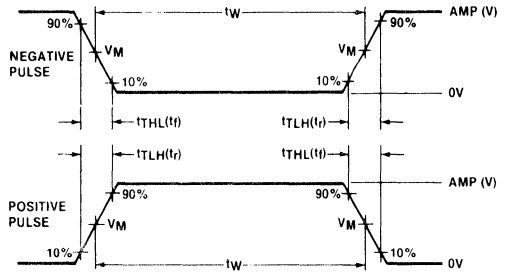
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



WF064505

V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

Logic Products

FAST 74F647, 74F649
Transceivers/Registers

'F647 — Octal Transceiver/Register, Non-Inverting (Open-Collector)
'F649 — Octal Transceiver/Register, Inverting (Open
Preliminary Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **Open-collector outputs**

DESCRIPTION

These devices consist of bus transceiver circuits with Open-Collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Enable $\overline{G}$ and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (S) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Enable $\overline{G}$ is active (LOW). In the isolation mode (Enable $\overline{G}$, HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed with the 'F647, and 'F649.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F647	7.5ns	115mA
74F649	7.5ns	115mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F647N, N74F649N
Plastic SOL-24	N74F647D, N74F649D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

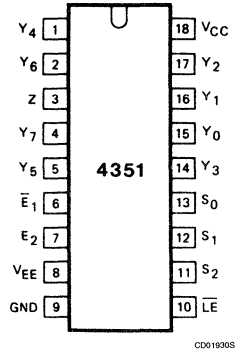
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$, $B_1 - B_8$	A and B inputs	1.0/0.033	20μA/20μA
CPAB, CPBA	Clock pulse inputs	1.0/0.033	20μA/20μA
SAB, SBA	Transmit/Receive input	1.0/0.033	20μA/20μA
DIR, $\overline{G}$	Output enable inputs	1.0/0.033	20μA/20μA
$A_1 - A_8$, $B_1 - B_8$	A and B outputs	150/33.3	3mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

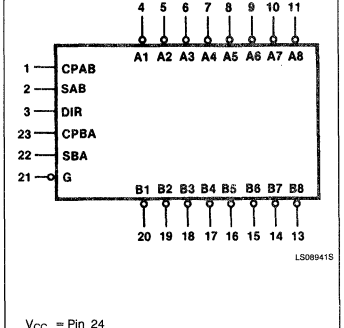
PIN CONFIGURATION

'F647



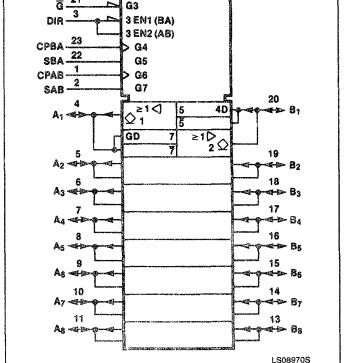
LOGIC SYMBOL

F'647



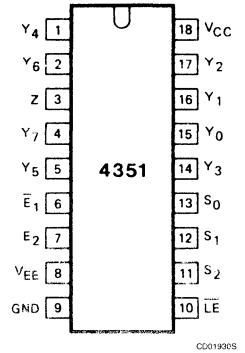
LOGIC SYMBOL (IEEE/IEC)

'F647



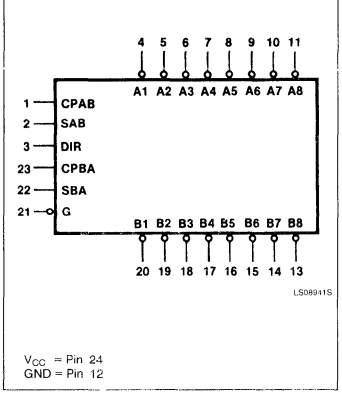
PIN CONFIGURATION

'F649



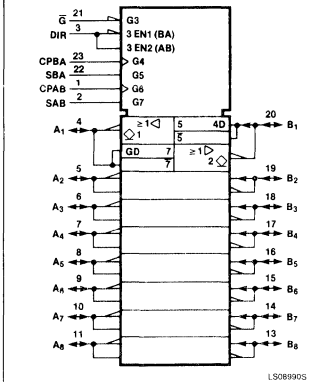
LOGIC SYMBOL

'F649

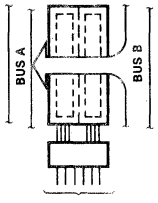


LOGIC SYMBOL (IEEE/IEC)

'F649

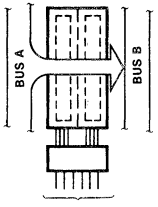


REAL-TIME TRANSFER BUS B TO BUS A



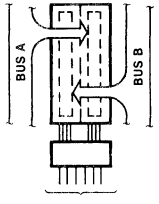
(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
H	L	X	X	X	L

REAL-TIME TRANSFER BUS A TO BUS B



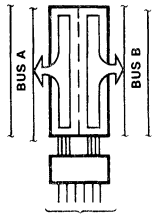
(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
H	L	X	X	L	X

STORAGE



(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
X	H	↑	↑	X	X

TRANSFER STORAGE DATA TO A OR B



(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
L	L	H or L	H or L	X	X
H				H	X

Figure 1

FUNCTION TABLE

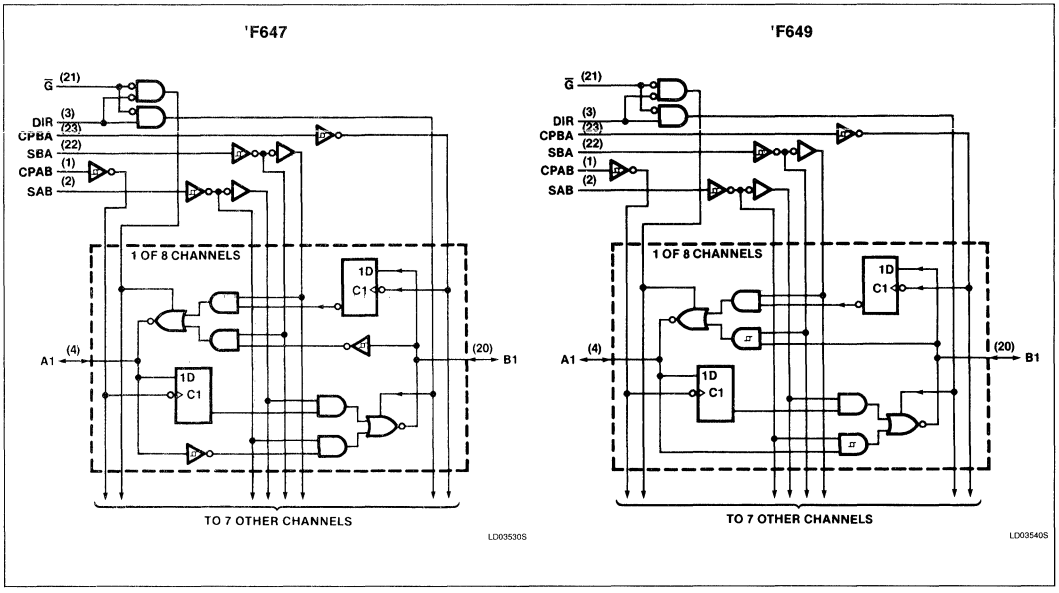
INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	$A_1 - A_8$	$B_1 - B_8$	'F647	'F649
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B data	Store A and B data
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	X	X	H			Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Stored A data to B bus	Stored $\overline{A}$ data to B bus

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

H = high level X = irrelevant

L = low level ↑ = low-to-high level transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
V_{OH}	HIGH-level output voltage			4.5	V
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F647, 'F649			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−1	−20	μA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			60	82	mA
		I_{CCL}				75	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

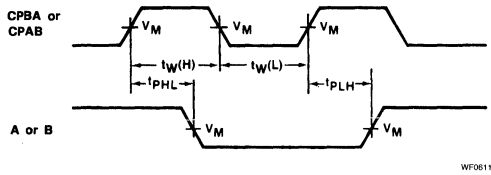
PARAMETER		TEST CONDITIONS	74F647, 'F649					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A or B	Waveform 1						ns
t_{PLH} t_{PHL}	Propagation delay A or B to B or A	Waveform 2, 3						ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A or B	Waveform 4, 5						ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A or B	Waveform 4, 5						ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

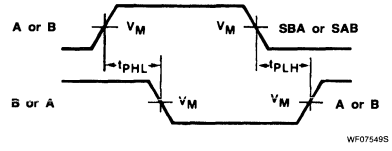
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F647, 'F649					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW A or B to CPBA or CPAB	Waveform 4						ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A or B to CPBA or CPAB	Waveform 4						ns
t_w	Clock pulse width	Waveform 1						ns

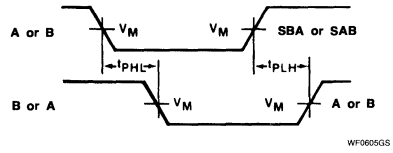
AC WAVEFORMS



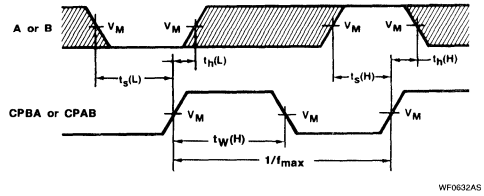
Waveform 1. Clock To Bus Delays, Clock Pulse Width



Waveform 2. Progation Delay SELECT A/$\overline{B}$ To Output (Y_n) (A Register Stored Data = L, CP = H)



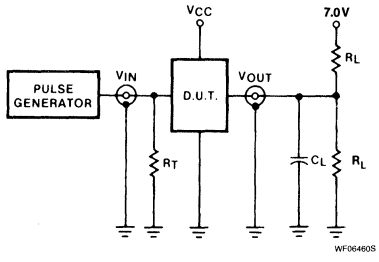
Waveform 3. Progation Delay SELECT A/$\overline{B}$ To Output (Y_n) (B Register Stored Data = L, CP = H)



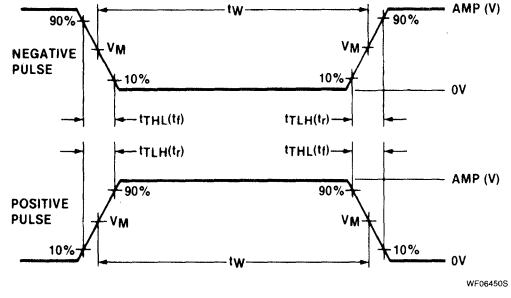
Waveform 4. Data And Select Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F651, 74F652, 74F653, 74F654
Transceivers/Registers

'F651/'F652 Octal Transceivers/Registers, INV/NINV (3-State)
'F653/'F654 Octal Transceivers/Registers, INV/NINV (O.C.)
Preliminary Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
  'F651, 'F653 Inverting
  'F652, 'F654 Non-Inverting
- **Choice of 3-State or Open-Collector outputs to A bus**
  'F651, 'F652 3-State
  'F653, 'F654 ($B_0 - B_7$) 3-State
  'F653, 'F654 ($A_0 - A_7$) Open-Collector

DESCRIPTION

These devices consist of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F651	12ns	56mA
74F652	12ns	65mA
74F653	18ns	56mA
74F654	18ns	65mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F651N, N74F652N, N74F653N, N74F654N
Plastic SOL-24	N74F651D, N74F652D, N74F653D, N74F654D

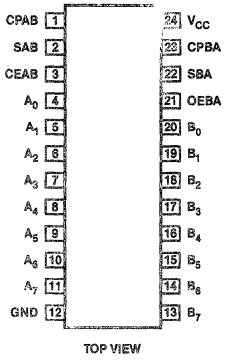
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

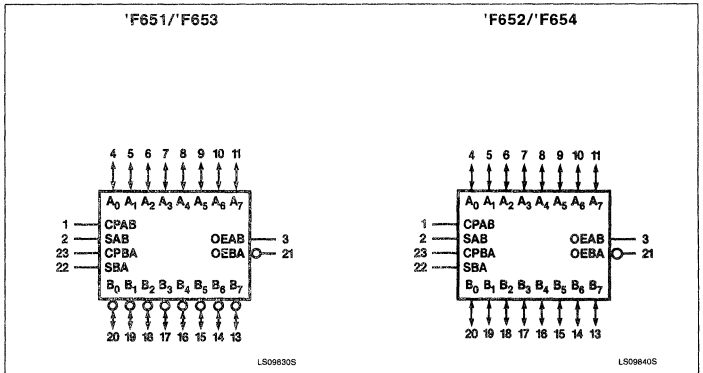
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$, $B_0 - B_7$		A and B inputs	1/0.033	20μA/20μA
CPAB, CPBA		Clock inputs	1/0.033	20μA/20μA
SAB, SBA		Select inputs	1/0.033	20μA/20μA
OEAB, $\overline{OEBA}$		Output enable inputs	1/0.033	20μA/20μA
'F651 'F652	$A_0 - A_7$	A outputs	150/40	3mA/24mA
	$B_0 - B_7$	B outputs	750/106.7	15mA/64mA
'F653 'F654	$A_0 - A_7$	A outputs	OC*/40	15mA/24mA
	$B_0 - B_7$	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

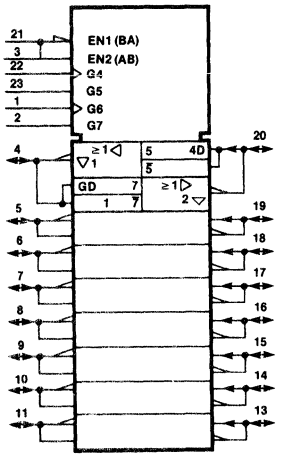


LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

'F651



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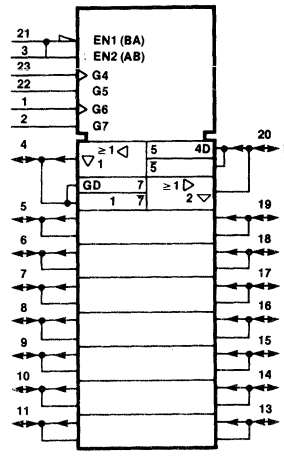

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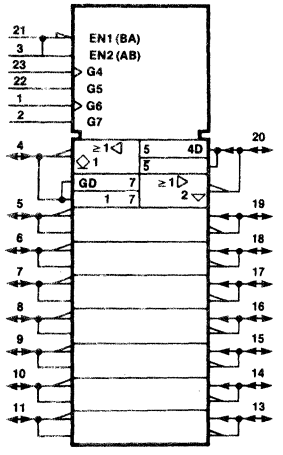
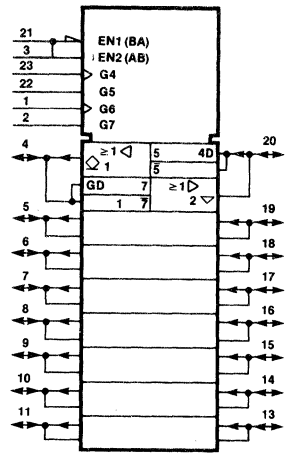


'F654



In the transceiver mode, data present at the high impedance port may be stored in either the A or B registor or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate Clock inputs (CPAB or CPBA) regardless of the Select or Output Enable inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration each output reinforces its input. Thus when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

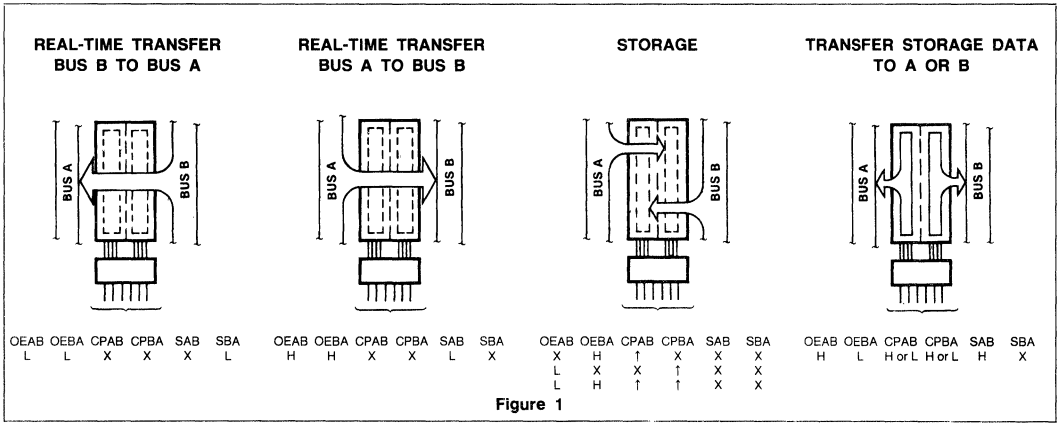


Figure 1

FUNCTION TABLE

INPUTS						INPUTS/OUTPUTS[1]		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	'F651, 'F653
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			Store $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and Stored $\overline{B}$ data to A bus

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTE:

1. The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

FUNCTION TABLE

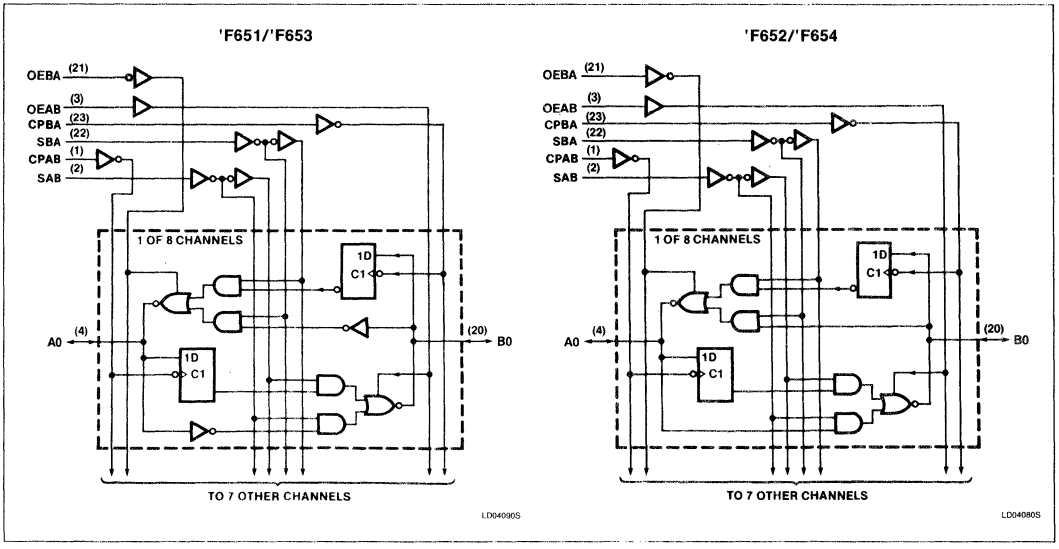
INPUTS						INPUTS/OUTPUTS[1]		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	'F652, 'F654
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B data
X	H	↑	H or L	X	X	Input	Not specified	Hold A, Store B
H	H	↑	↑	X	X	Input	Output	Store B in both registers
L	X	H or L	↑	X	X	Not specified	Input	Store A, Hold B
L	L	↑	↑	X	X	Output	Input	Store A in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H			Store B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X			Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTE:

1. The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS FOR 'F651 AND 'F652

PARAMETER			74F651, 74F652			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	LOW-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

RECOMMENDED OPERATING CONDITIONS FOR 'F653 AND 'F654

PARAMETER			74F653, 74F654			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage	$A_0 - A_7$			4.5	V
I_{OH}	HIGH-level output current	$B_0 - B_7$			−15	mA
I_{OL}	LOW-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

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DC ELECTRICAL CHARACTERISTICS

Except $A_0 - A_7$ of 74F653 and 74F654 (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F651, 74F652 74F653 ($B_0 - B_7$) 74F654 ($B_0 - B_7$)			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		.35	.50	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	SAB, SBA OEAB, $\overline{OEBA}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 0.5V					1.0	mA
I_{IH}	HIGH-level input current	SAB, SBA OEAB, $\overline{OEBA}$	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	SAB, SBA OEAB, $\overline{OEBA}$	V_{CC} = MAX, V_I = 0.5V					−20	μA
$I_{OZH} + I_{IH}$	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_I = 2.7V					70	μA
$I_{OZL} + I_{IL}$	Off-state output current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_I = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$				−150		−225	mA
I_{CC}	Supply current (total)	'F651	I_{CCH}	V_{CC} = MAX			52		mA
			I_{CCL}				57		mA
			I_{CCZ}				58		mA
		'F652	I_{CCH}	V_{CC} = MAX			60		mA
			I_{CCL}				68		mA
			I_{CCZ}				68		mA
		'F653 $B_0 - B_7$ only	I_{CCH}	V_{CC} = MAX			60		mA
			I_{CCL}				68		mA
			I_{CCZ}				68		mA
		'F654 $B_0 - B_7$ only	I_{CCH}	V_{CC} = MAX			60		mA
			I_{CCL}				68		mA
			I_{CCZ}				68		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

DC ELECTRICAL CHARACTERISTICS Except $A_0 - A_7$ of 74F653 and 74F654 (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER				TEST CONDITIONS[1]	74F651, 74F652 74F653, 74F654			UNIT
					Min	Typ[2]	Max	
I_{CC}	Supply current (total)	'F654 $B_0 - B_7$ only	I_{CCH}	V_{CC} = MAX		60		mA
			I_{CCL}			68		mA
			I_{CCZ}			68		mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

DC ELECTRICAL CHARACTERISTICS for A ports of 74F653 and 74F654 (Over recommended operating for free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F653, 74F654 A PORTS ONLY			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			-1	-20	μA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			60	82	mA
		I_{CCL}				75	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifing FAST Logic.")

PARAMETER		TEST CONDITIONS	74F651, 74F652					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	110		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A_n or B_n	Waveform 1				2.0 2.0	8.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay A or B to B_n or A_n	Waveform 2, 3				2.0 1.0	8.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A_n or B_n	Waveform 2, 3 (A or B = HIGH)				2.0 2.0	11.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A_n or B_n	Waveform 2, 3 (A or B = LOW)				2.0 2.0	11.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to A_n	Waveform 5 Waveform 6				2.0 3.0	10.0 16.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to A_n	Waveform 5 Waveform 6				2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to B_n	Waveform 5 Waveform 6				3.0 3.0	11.0 16.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to B_n	Waveform 5 Waveform 6				2.0 2.0	10.0 11.0	ns

NOTE:
1. Subtract 0.2ns from minimum values for SO package.

AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F651, 74F652					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW A_n or B_n to CPBA or CPAB	Waveform 4				6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A_n or B_n to CPBA or CPAB	Waveform 4				0 0		ns
$t_w(H)$ $t_w(L)$	CPAB, CPBA pulse width HIGH or LOW	Waveform 1				5.0 6.0		ns

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

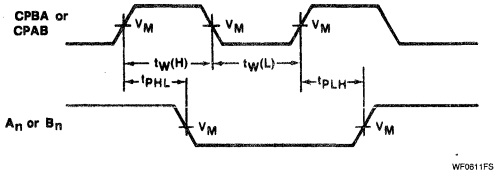
PARAMETER		TEST CONDITIONS	74F653, 74F654					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	110		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A_n or B_n	Waveform 1				3.0 3.0	9.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2, 3				3.0 2.0	9.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A_n or B_n	Waveform 2, 3 (A or B = HIGH)				3.0 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A_n or B_n	Waveform 2, 3 (A or B = LOW)				3.0 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEBA}$ to A_n	Waveform 3				5.5 3.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay OEAB to B_n	Waveform 2				6.0 3.0	16.0 10.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

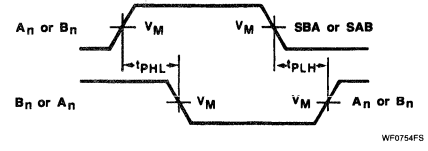
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F653, 74F654					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW A_n or B_n to CPBA or CPAB	Waveform 4				6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A_n or B_n to CPBA or CPAB	Waveform 4				0 0		ns
$t_w(H)$ $t_w(L)$	CPAB, CPBA pulse width HIGH or LOW	Waveform 1				5.0 6.0		ns

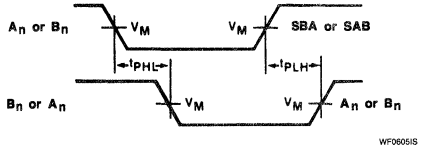
AC WAVEFORMS



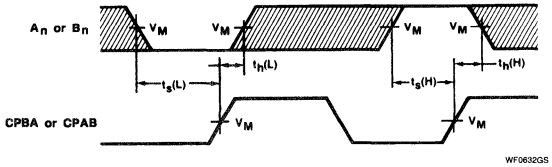
Waveform 1. Clock To Output Delays, Clock Pulse Width



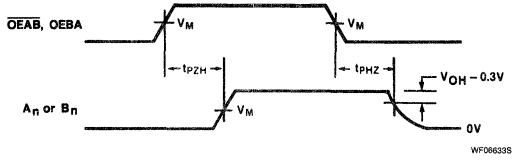
Waveform 2. Propagation Delay Data And Select To Outputs (An Or Bn = HIGH)



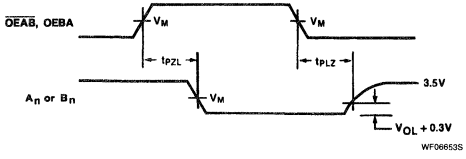
Waveform 3. Propagation Delay Data And Select To Outputs (An Or Bn = LOW)



Waveform 4. Data Set-up And Hold Times



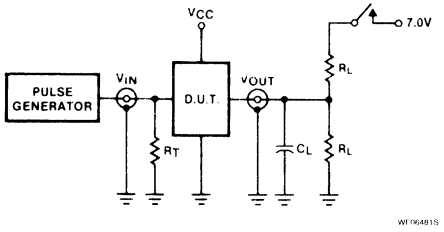
Waveform 5. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



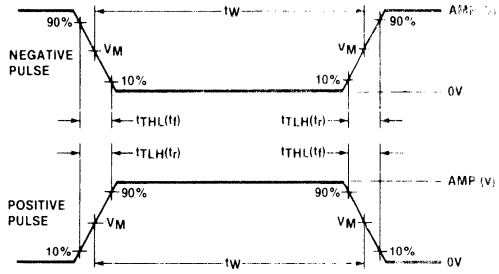
Waveform 6. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State And Open Collector (OC) Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F655A, 74F656A
Buffers/Drivers

Octal Buffer/Line Driver with Parity
('F655A — Inverting 3-State)
('F656A — Non-Inverting 3-State)
Product Specification

FEATURES

- **Significantly improved AC performance over 'F655 and 'F656**
- **High impedance NPN base input for reduced loading (20μA in HIGH and LOW states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA vs FAST std of 600μA)**
- **'F655A combines 'F240 and 'F280 functions in one package**
- **'F656A combines 'F244 and 'F280A functions in one package**
- **'F655A Inverting**
  'F656A Non-inverting
- **3-State outputs sink 64mA**
- **Inputs source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Inputs on one side and outputs on the other side simplify PC board layout**
- **Combined functions reduce part count and enhance system performance**

DESCRIPTION

The 'F655A and 'F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F655A	6.5ns	64mA
74F656A	6.5ns	64mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F655AN, N74F656AN
Plastic SOL-24	N74F655AD, N74F656AD

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

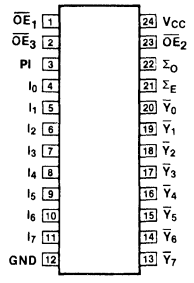
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	1.0/0.033	20μA/20μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$ $\overline{OE}_3$	3-State output enable inputs (active LOW)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs ('F655A)	750/106.7	15mA/64mA
Y_n	Data outputs ('F656A)	750/106.7	15mA/64mA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

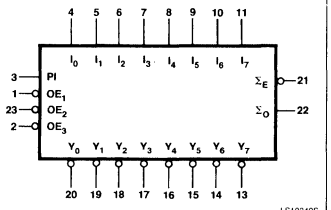
'F655A



CD08061S

LOGIC SYMBOL

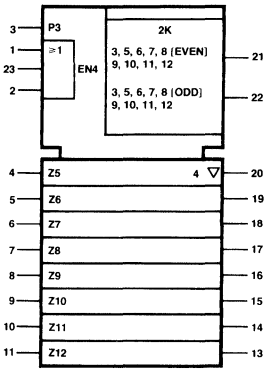
'F655A



LS10340S

LOGIC SYMBOL (IEEE/IEC)

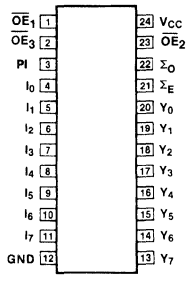
'F655A



LS10310S

PIN CONFIGURATION

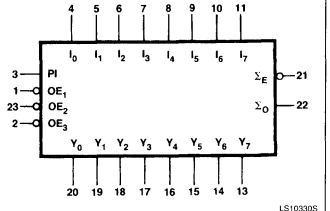
'F656A



CD08071S

LOGIC SYMBOL

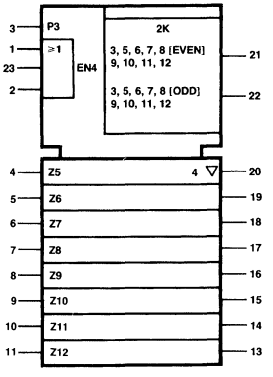
'F656A



LS10330S

LOGIC SYMBOL (IEEE/IEC)

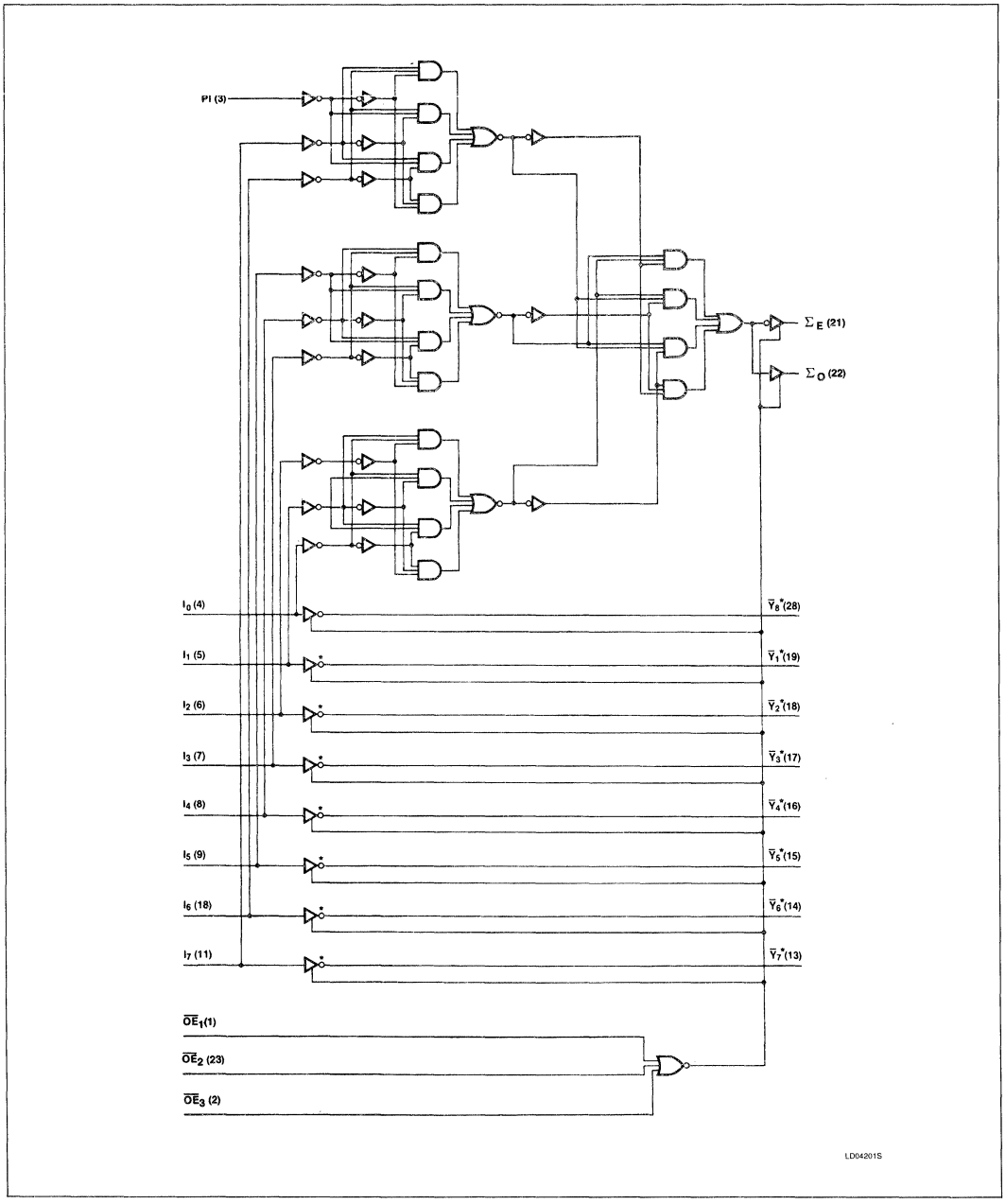
'F656A



LS10320S

6

LOGIC DIAGRAM FOR 'F655A
(Non-inverting For 'F656A)



FUNCTION TABLES

INPUTS				DATA OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	I_n	'F655A	'F656A
L	L	L	L	H	L
L	L	L	H	L	H
H	X	X	X	Z	Z
X	H	X	X	Z	Z
X	X	H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance state

INPUTS	PARITY OUTPUTS	
Number of inputs HIGH (PI, $I_0 - I_7$)	Σ_E	Σ_0
EVEN – 0, 2, 4, 6, 8	H	L
ODD – 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = HIGH	(Z)	(Z)

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F655A, 'F656A			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−1	−20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					50	μA
I_{OZL}	Off-state output current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					63	90	mA

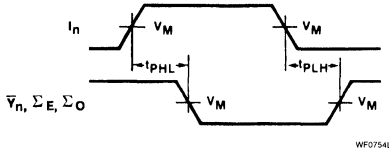
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

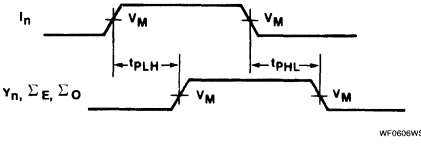
PARAMETER			TEST CONDITIONS	74F655A, 656A					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	'F655A	Waveform 1	2.0 1.0	4.5 2.5	6.5 4.0	2.0 1.0	7.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	'F656A	Waveform 2	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E, Σ_0		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 3 Waveform 4	4.5 4.5	7.0 8.0	10.5 11.0	4.0 4.5	11.5 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	9.0 9.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

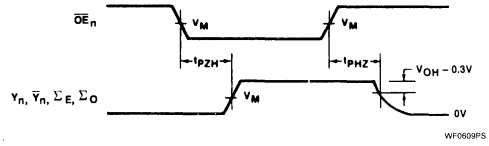
AC WAVEFORMS



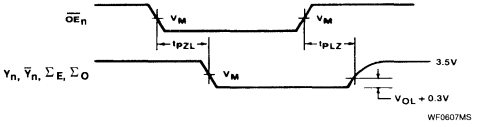
Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Propagation Delay for I_n to Y_n, Σ_E, Σ_O



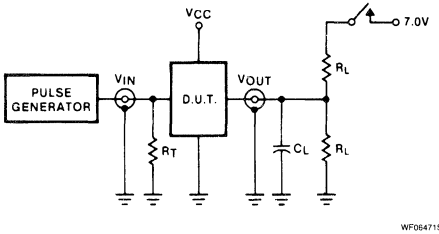
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



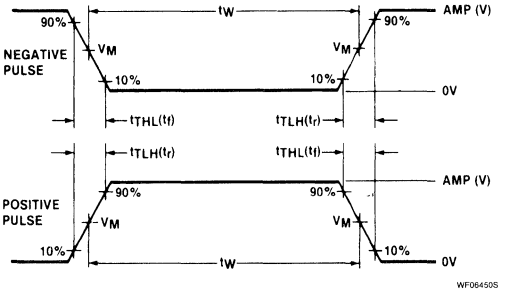
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Signetics

Logic Products

FAST 74F657
Transceiver

Octal Bidirectional Transceiver With 8-Bit Parity Generator/Checker (3-State Outputs)
Product Specification

FEATURES

- **High-impedance NPN base input for reduced loading (20μA in HIGH and LOW states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA Vs FAST std of 600μA)**
- **24-pin plastic slim dip (300-mil) package**
- **Combines 'F245 and 'F280A functions in one package**
- **3-State outputs**
- **Outputs sink 64mA**
- **15mA source current**
- **Input diodes for termination effects**

DESCRIPTION

The 'F657 contains eight non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 20mA at the A ports and 64mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F657	5ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F657N
Plastic SOL-24	N74F657D

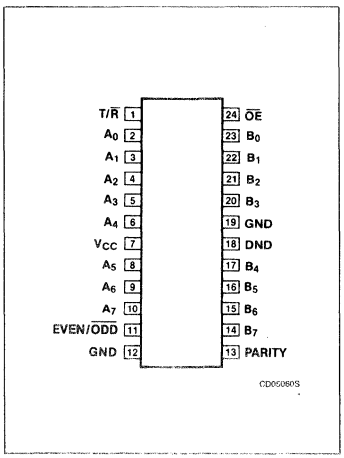
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

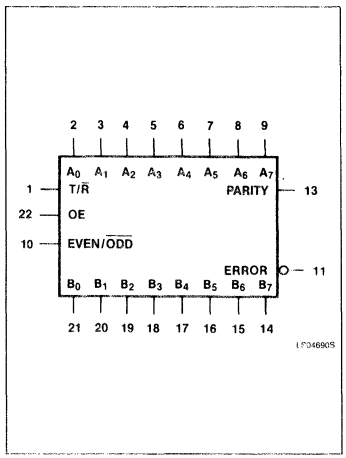
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A ports 3-State inputs	5.0/0.167	100μA/100μA
$B_0 - B_7$	B ports 3-State inputs	3.5/0.117	70μA/70μA
PARITY	Parity input	3.5/0.117	70μA/70μA
T/$\overline{R}$	Transmit/receive input	2.0/0.066	40μA/40μA
EVEN/$\overline{ODD}$	EVEN/ODD input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active LOW)	2.0/0.066	40μA/40μA
$A_0 - A_7$	A ports 3-State outputs	150/40	3mA/24mA
$B_0 - B_7$	B ports 3-State outputs	750/106.7	15mA/64mA
PARITY	Parity output	150/40	3mA/24mA
$\overline{ERROR}$	Error output	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

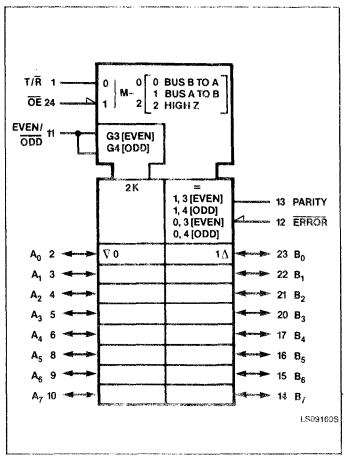
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The Output Enable inputs disable both the A and B ports by placing them in a High-Z condition when either the $\overline{OE}$ input is HIGH or the $\overline{OE}$ input is LOW.

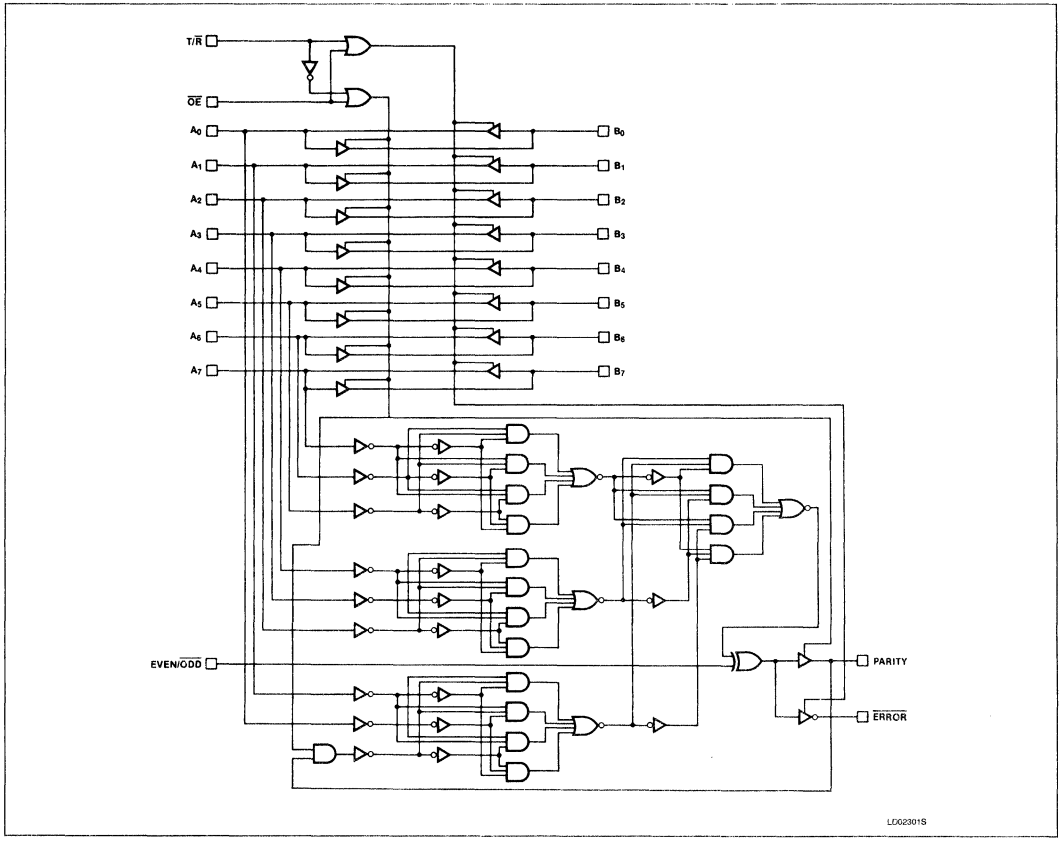
The parity generator detects whether an even or odd number of bits on the A ports are HIGH, depending on the condition of the Parity Select input. If the Even input is active HIGH and an even number of A inputs are HIGH, the Parity output is HIGH. The parity of the data received on the B ports is compared with the Parity Select input and the Error output is LOW if not equal.

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	EVEN/$\overline{ODD}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	(Z)	Transmit
	L	H	L	L	(Z)	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	(Z)	Transmit
	L	H	L	H	(Z)	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	(Z)	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$, PARITY, $\overline{ERROR}$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$, PARITY, $\overline{ERROR}$			−15	mA
I_{OL}	LOW-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$, PARITY, $\overline{ERROR}$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F657			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	All Outputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$, PARITY, $\overline{ERROR}$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
		$B_0 - B_7$, PARITY, $\overline{ERROR}$		I_{OL} = 48mA	±10%V_{CC}		.40	.55	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	T/$\overline{R}$,$\overline{OE}$,EVEN/$\overline{ODD}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		$A_0 - A_7$	V_{CC} = 5.5V, V_I = 5.5V					2	mA
		$B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	HIGH-level input current	EVEN/$\overline{ODD}$	V_{CC} = MAX, V_I = 2.7V					20	μA
		T/$\overline{R}$,$\overline{OE}$						40	μA
I_{IL}	LOW-level input current	EVEN/$\overline{ODD}$	V_{CC} = MAX, V_I = 0.5V					−20	μA
		T/$\overline{R}$,$\overline{OE}$						−40	μA
I_{IH} + I_{OZH}	Off-state current HIGH level voltage applied	$A_0 - A_7$	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					100	μA
I_{IL} + I_{OZL}	Off-state current LOW level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−100	μA
I_{IH} + I_{OZH}	Off-state current HIGH level voltage applied	$B_0 - B_7$ PARITY	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					70	μA
I_{IL} + I_{OZL}	Off-state current LOW level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−70	μA
I_{OZH}	Off-state current HIGH level voltage applied	$\overline{ERROR}$	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					50	μA
I_{OZL}	Off-state current LOW level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$				−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	125	mA
		I_{CCL}					106	150	mA
		I_{CCZ}					98	145	mA

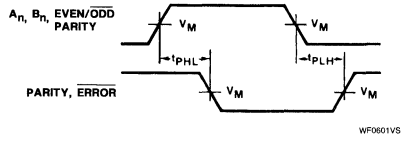
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

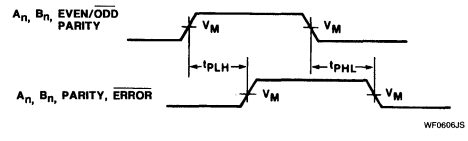
PARAMETER		TEST CONDITIONS	74F657					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to PARITY	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 14.0	7.0 7.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay EVEN/$\overline{ODD}$ to PARITY, $\overline{ERROR}$	Waveform 1, 2	4.5 4.5	7.5 8.0	11.0 11.5	4.5 4.5	12.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{ERROR}$	Waveform 1, 2	8.0 8.0	14.0 14.0	20.5 20.5	7.5 7.5	22.5 22.5	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{ERROR}$	Waveform 1, 2	8.0 8.0	11.5 12.0	15.5 15.5	7.5 8.0	16.5 17.0	ns
t_{PZH} t_{PZL}	Output enable time[2] to HIGH or LOW level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

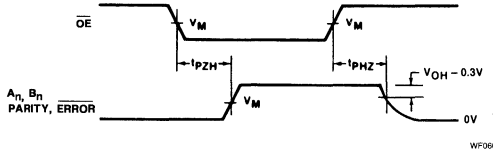
AC WAVEFORMS



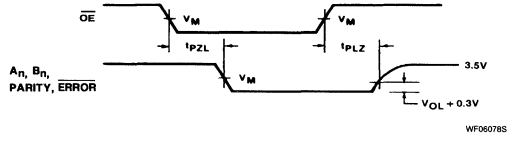
Waveform 1. Propagation Delay For Inverting Outputs



Waveform 2. Propagation Delay For Non-Inverting Outputs



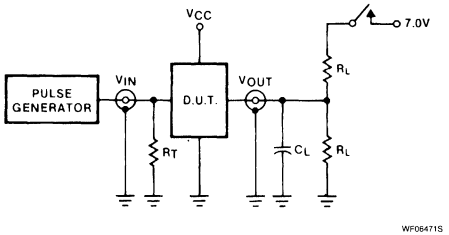
Waveform 3. 3-State Enable Time To HIGH Level And Disable Time From HIGH Level



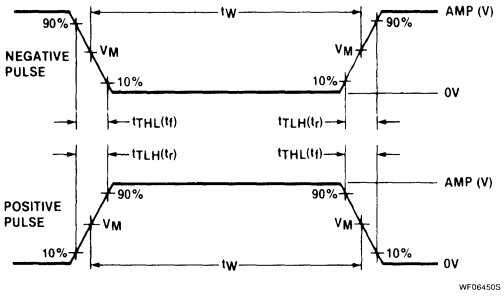
Waveform 4. 3-State Enable Time To LOW Level And Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

6

Signetics

FAST 74F673A
16-Bit Shift Register

16-Bit Shift Register (Serial-In/Serial-Parallel Out)
Preliminary Specification

Logic Products

FEATURES

- **Serial-to-parallel converter**
- **16-bit serial I/O shift register**
- **16-bit parallel-out storage register**
- **Recirculating serial shifting**
- **Recirculating parallel transfer**
- **Common serial data I/O pin**

DESCRIPTION

The 'F673A contains a 16-bit serial-in/serial-out shift register and a 16-bit parallel-out storage register. A single pin serves either as an input for serial entry or as a 3-State serial output. In the Serial-out mode, the data recirculates in the shift register. By means of a separate clock, the contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A HIGH-signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via STMR.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F673A	130MHz	106mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F673N
Plastic SOL-24	N74F673D

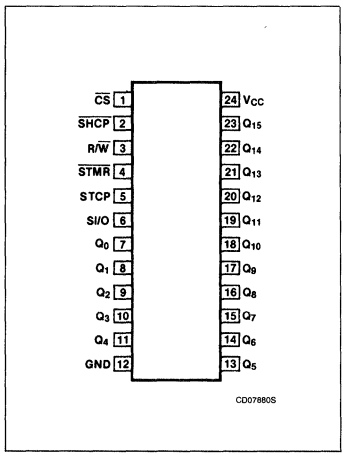
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

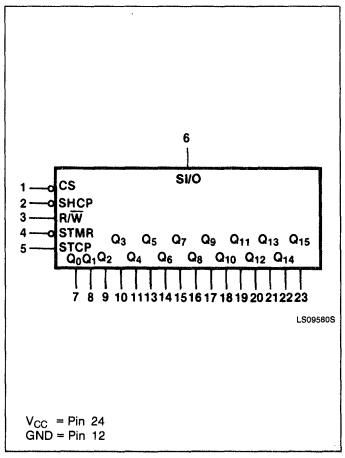
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CS}$	Chip select input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SHCP}$	Shift clock pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
STMR	Store master reset input (active LOW)	1.0/1.0	20μA/0.6mA
STCP	Store clock pulse input	1.0/1.0	20μA/0.6mA
R/$\overline{W}$	Read/write input	1.0/1.0	20μA/0.6mA
SI/O	Serial data input or	3.5/1.0	70μA/0.6mA
	3-State serial output	50/33	1.0mA/20mA
$Q_0 - Q_5$	Parallel data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

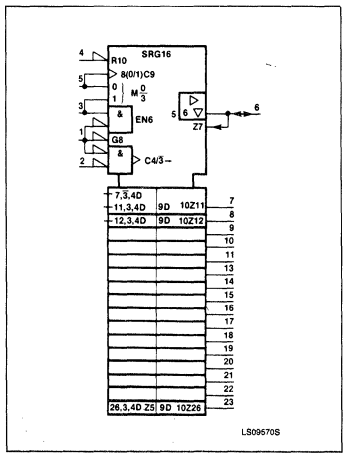
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



16-Bit Shift Register | FAST 74F673A

FUNCTIONAL DESCRIPTION

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-State buffer into the high-impedance state. During serial shift-out operations, the SI/O buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous MASTER RESET ($\overline{STMR}$) input that overrides all other inputs and forces the $Q_0 - Q_{15}$ outputs LOW. The storage register is in the Hold mode whether $\overline{CS}$ or the Read/Write (R/$\overline{W}$) input is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

STORAGE REGISTER OPERATIONS TABLE

CONTROL INPUTS				OPERATING MODE
$\overline{STMR}$	$\overline{CS}$	R/$\overline{W}$	$\overline{STCP}$	
L	X	X	X	Reset; Outputs LOW
H	H	X	X	Hold
H	X	H	X	Hold
H	L	L	↑	Parallel Load

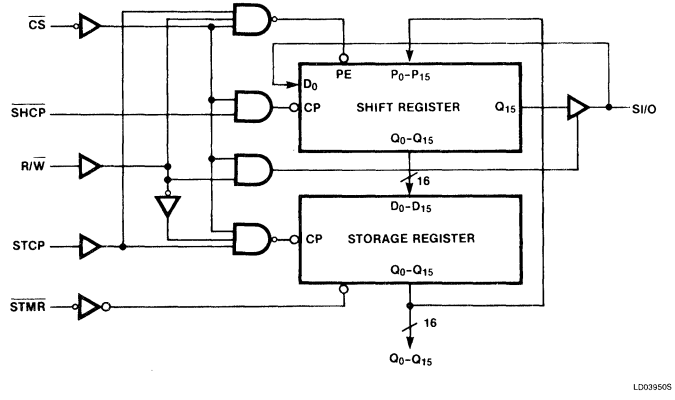
↑ = LOW-to-HIGH clock transition

SHIFT REGISTER OPERATIONS TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP		
H	X	X	X	High Z	Hold
L	L	↓	X	Data in	Serial load
L	H	↓	L	Data out	Serial output with recirculation
L	H	↓	H	Active	Parallel load; no shifting

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW clock transition

FUNCTIONAL BLOCK DIAGRAM



LD03950S

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F673A			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN,	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	70	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−600	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				mA
		I_{CCL}				160	mA
		I_{CCZ}					mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequences of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

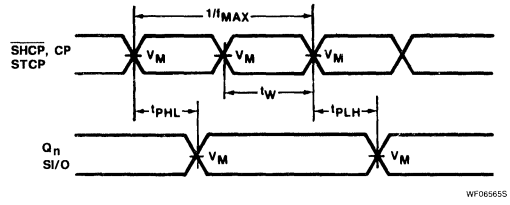
PARAMETER		TEST CONDITIONS	74F673A					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	130				MHz
t_{PLH} t_{PHL}	Propagation delay STCP to Q_n	Waveform 1	7.5 9.5	13 16	18 22			ns
t_{PHL}	Propagation delay $\overline{STMR}$ to Q_n	Waveform 2	6.0	10	14			ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHCP}$ to SI/O	Waveform 1	4.5 5.0	8.0 9.0	11 12.5			ns
t_{PZH} t_{PZL}	Output enable time $\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	3.0 3.0	5.0 5.0	7.0 7.0			ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	3.0 3.0	5.0 5.0	7.0 7.0			ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

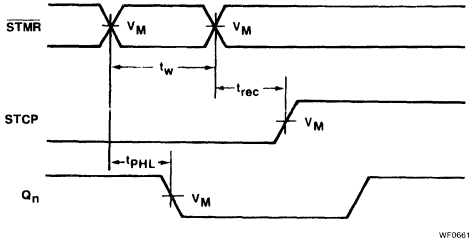
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F673A					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 5	7.0 7.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 5	0 0					ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW SI/O to $\overline{SHCP}$	Waveform 5	3.0 3.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW SI/O to $\overline{SHCP}$	Waveform 5	0 0					ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to $\overline{SHCP}$	Waveform 5	5.0 5.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to $\overline{SHCP}$	Waveform 5	0 0					ns
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ pulse width, HIGH or LOW	Waveform 1	4.0 5.0					ns
$t_w(H)$ $t_w(L)$	STCP pulse width, HIGH or LOW	Waveform 1	5.0 10					ns
$t_w(L)$	$\overline{STMR}$ pulse width LOW	Waveform 2	7.0					ns
t_{rec}	Recovery time $\overline{STMR}$ to STCP	Waveform 2	10					ns

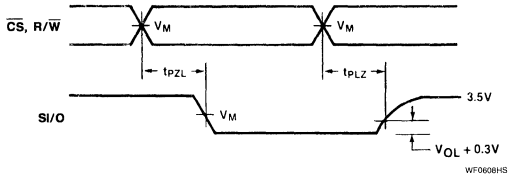
AC WAVEFORMS



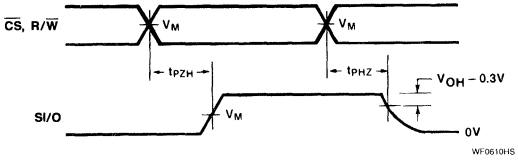
Waveform 1. Clock To Output Delays And Clock Pulse Width



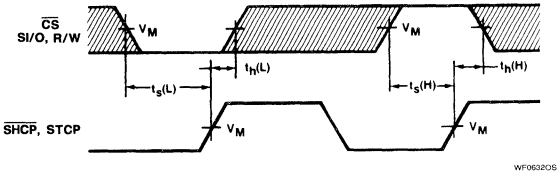
Waveform 2. Master Reset Pulse Width Master Reset To Output Delay And Master Reset To Clock Recovery Time



Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



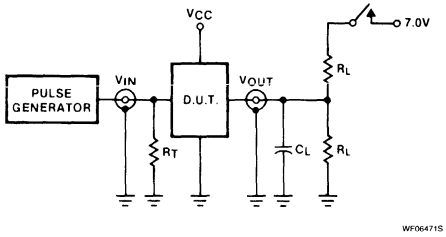
Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



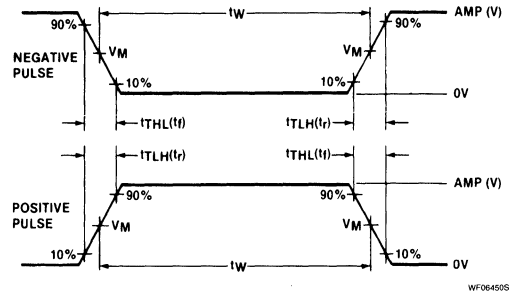
Waveform 5. Data Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F674
16-Bit Shift Register

16-Bit Shift Register, Serial-Parallel-In/Serial-Out (3-State)
Preliminary Specification

Logic Products

FEATURES
- **16-bit serial I/O shift register**
- **16-bit parallel-in/serial-out converter**
- **Recirculating serial shifting**
- **Common serial data I/O pin**

DESCRIPTION
The 'F674 is a 16-bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as a 3-State serial output. In the Serial-out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility.

FUNCTIONAL DESCRIPTION
The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table.

Hold — a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-State buffer into the high impedance state.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F674	140MHz	53mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F674N
Plastic SOL-24	N74F674D

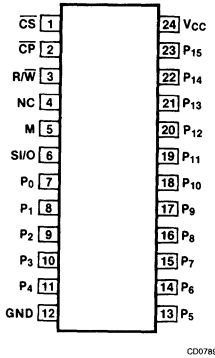
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

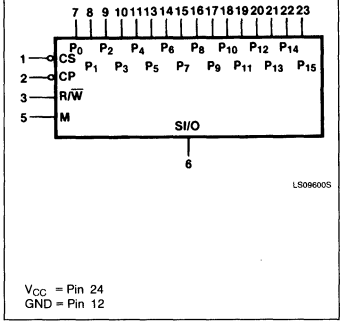
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$P_0 - P_{15}$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip select input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock pulse input (active LOW)	1.0/1.0	20μA/0.6mA
M	Mode select input	1.0/1.0	20μA/0.6mA
R/$\overline{W}$	Read/write input	1.0/1.0	20μA/0.6mA
SI/O	3-State serial data input or	3.75/1.0	70μA/0.6mA
	3-State serial output	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

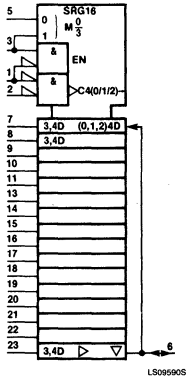
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



16-Bit Shift Register | FAST 74F674

Serial Load — data present on the SI/O pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

Serial Output — the SI/O 3-State buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0.

Parallel Load — data present on $P_0 - P_{15}$ are entered into the register on the falling edge of CP. The SI/O 3-State buffer is active and represents the Q_{15} output.

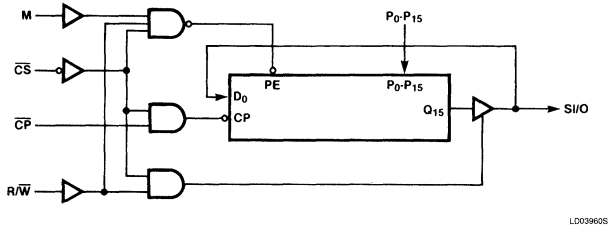
To prevent false clocking, CP must be LOW during a LOW-to-HIGH transition of CS.

SHIFT REGISTER OPERATIONS TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	M	$\overline{CP}$		
H	X	X	X	High Z	Hold
L	L	X		Data in	Serial load
L	H	L	↓	Data out	Serial output with recirculation
L	H	H	↓	Active	Parallel load; no shifting

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F674 Min	74F674 Typ[2]	74F674 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	µA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V			2	70	µA
I_{OZL}	Off-state output current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−650	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		−60	−80	−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.8	3.0	mA
		I_{CCL}		V_{IN} = 4.5V		5.5	7.5	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

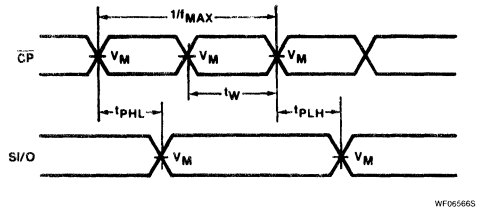
PARAMETER		TEST CONDITIONS	74F674 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F674 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum input frequency	Waveform 1	100	140				MHz
t_{PLH}	Propagation delay	Waveform 1	4.5	8.0	11			ns
t_{PHL}	$\overline{CP}$ to SI/O		5.0	9.0	12.5			
t_{PZH}	Output enable time	Waveform 3	3.0	5.0	7.0			ns
t_{PZL}	$\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 4	3.0	5.0	7.0			
t_{PHZ}	Output disable time	Waveform 3	3.0	5.0	7.0			ns
t_{PLZ}	$\overline{CS}$ or R/$\overline{W}$ to SI/O	Waveform 4	3.0	5.0	7.0			

NOTE:
Subtract 0.2ns from minimum values for SO package.

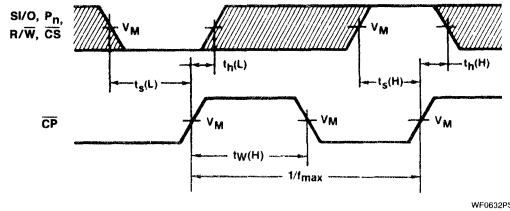
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F674					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW SIO to $\overline{CP}$	Waveform 2	7.0 7.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW SI/O to $\overline{CP}$	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW P_n to $\overline{CP}$	Waveform 2	3.0 3.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW P_N to $\overline{CP}$	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	Waveform 2	5.0 5.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to f$\overline{CP}$	Waveform 2	0 0					ns
$t_W(H)$ $t_W(L)$	$\overline{CP}$ pulse width, HIGH or LOW	Waveform 1	4.0 5.0					ns

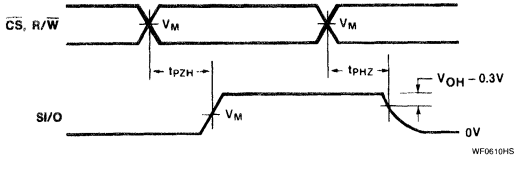
AC WAVEFORMS



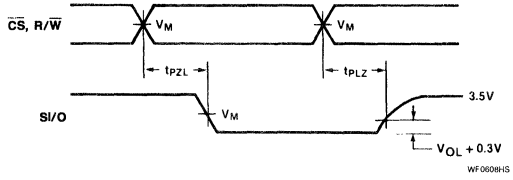
Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Data Set-up And Hold Times



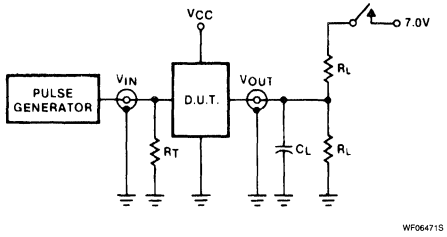
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



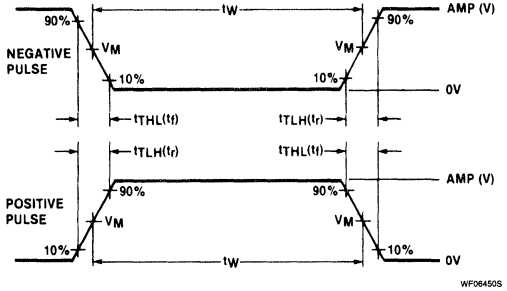
Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

6

Signetics

FAST 74F675
16-Bit Shift Register

16-Bit Shift Registers (Serial-In/Serial-Parallel Out)
Preliminary Specification

Logic Products

FEATURES

- **Serial-to-parallel converter**
- **16-bit serial I/O shift register**
- **16-bit parallel-out storage register**
- **Recirculating parallel transfer**
- **Expandable for longer words**

DESCRIPTION

The 'F675 contains a 16-bit serial-in/serial-out shift register and a 16-bit parallel-out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F675	130MHz	106mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F675N
Plastic SOL-24	N74F675D

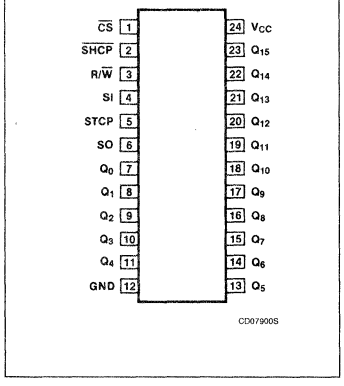
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

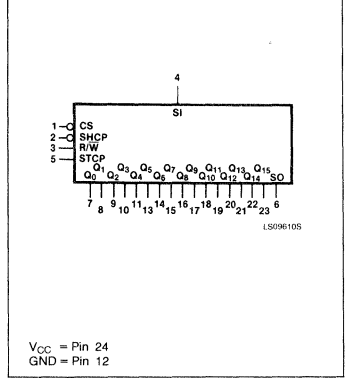
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
SI	Serial data input	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip select input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SHCP}$	Shift clock pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
STCP	Store clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
R/$\overline{W}$	Read/write input	1.0/1.0	20μA/0.6mA
SO	Serial data output	50/33	1.0mA/20mA
Q_0-Q_{15}	Parallel data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

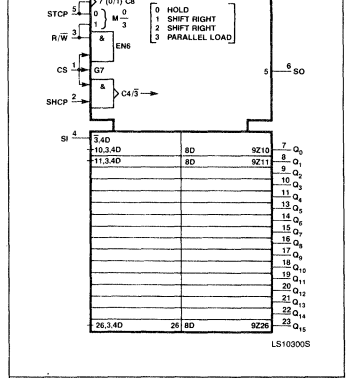


LOGIC SYMBOL



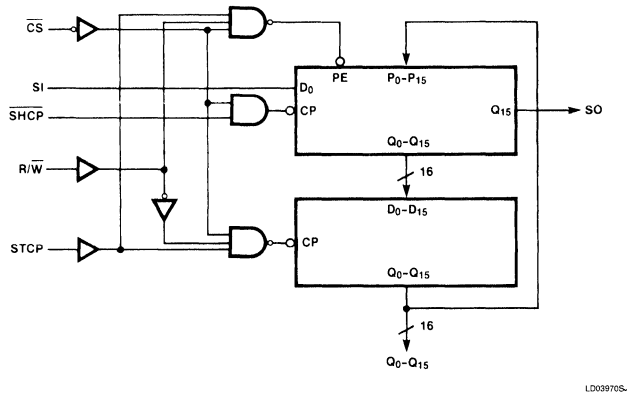
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)



16-Bit Shift Register | FAST 74F675

FUNCTIONAL BLOCK DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The 16-bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$) and Store Clock Pulse (STCP) inputs. State changes are indicated by the falling edge of the Shift Clock Pulse ($\overline{SHCP}$). In the Shift-right mode, data enters D_0 from the Serial Input (SI) pin and exits from Q_{15} via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either $\overline{CS}$ or R/$\overline{W}$ is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

SHIFT REGISTER OPERATIONS TABLE

CONTROL INPUTS				OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP	
H	X	X	X	Hold
L	L	↓	X	Shift right
L	H	↓	L	Shift right
L	H	↓	H	Parallel load; No shifting

STORAGE REGISTER OPERATIONS TABLE

INPUTS			OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	↑	Parallel load

H = HIGH voltage level
L = LOW voltage level
XX = Don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

6

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F675			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V			5	100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				160	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

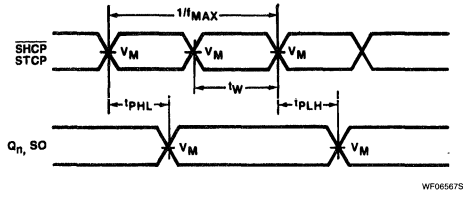
PARAMETER		TEST CONDITIONS	74F675					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	130				MHz
t_{PLH} t_{PHL}	Propagation delay STCP to Q_n	Waveform 1	7.5 9.5	13 16	18 22			ns
t_{PLH} t_{PHL}	Propagation delay SHCP to SO	Waveform 1	4.5 5.0	8.0 9.0	11 12.5			ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

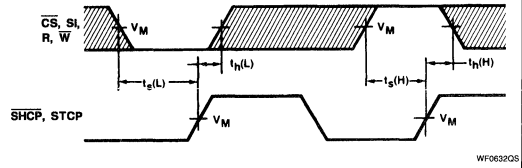
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F675					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 2	7.0 7.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW SI to $\overline{SHCP}$	Waveform 2	3.0 3.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW SI to $\overline{SHCP}$	Waveform 2	0 0					ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{SHCP}$	Waveform 2	5.0 5.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{SHCP}$	Waveform 2	0 0					ns
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ pulse width, HIGH or LOW	Waveform 1	4.0 5.0					ns
$t_w(H)$ $t_w(L)$	STCP pulse width, HIGH or LOW	Waveform 1	5.0 10					ns

AC WAVEFORMS



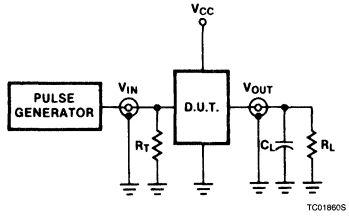
Waveform 1. Clock To Output Delays And Clock Pulse Width



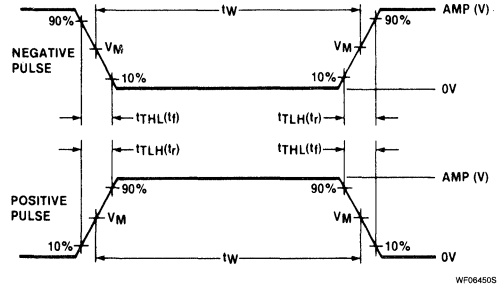
Waveform 2. Data Set-up And Hold Times.

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F676
Shift Register

'F676 16-Bit Shift Register
Preliminary Specification

Logic Products

FEATURES

- **16-bit parallel-to-serial conversion**
- **16-bit serial-in, serial-out**
- **Chip Select control**
- **Power supply current 48mA typical**
- **Shift frequency 110MHz typical**

DESCRIPTION

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data ($P_0 - P_{15}$) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F676	110MHz	48mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F676N
Plastic SOL-24	N74F676D

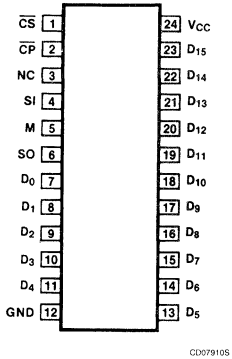
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

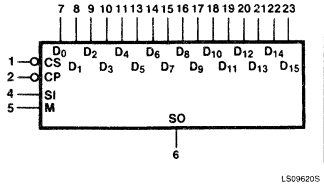
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CS}$	Chip select input (active LOW)	1.0/1.0	20μA/0.6mA
SI	Serial data input	1.0/1.0	20μA/0.6mA
M	Mode select input	1.0/1.0	20μA/0.6mA
$D_0 - D_{15}$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
SO	Serial data output	50/33	1mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

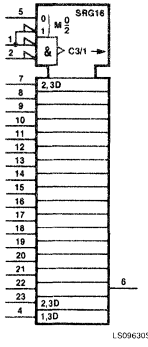
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Shift Register | FAST 74F676

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

HOLD — a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the 16 registers.

Shift/Serial Load — data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load — data present on $P_0 - P_{15}$ are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

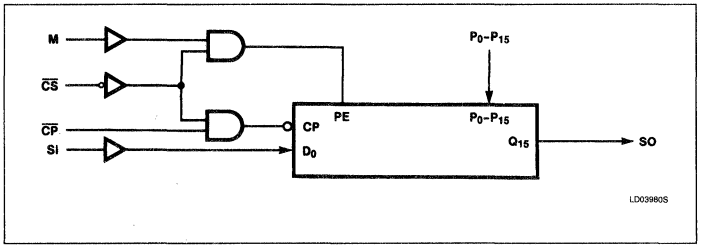
To prevent false clocking, $\overline{CP}$ must be LOW during a LOW-to-HIGH transition of $\overline{CS}$.

FUNCTION TABLE

CONTROL INPUT			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/serial load
L	H	↓	Parallel load

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74F676 Min	74F676 Typ[2]	74F676 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60	−80	−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			48	72	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

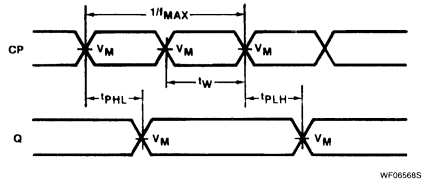
PARAMETER		TEST CONDITIONS	74F676 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F676 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	100	110		90		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SO	Waveform 1	4.5 5.0	9.0 9.0	11 12.5	4.5 5.0	12 13.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

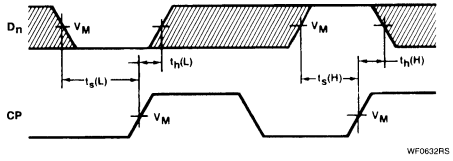
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F676					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW SI to $\overline{CP}$	Waveform 2	4.0 4.0				4.0 4.0	
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW SI to $\overline{CP}$	Waveform 2	4.0 4.0				4.0 4.0	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n $\overline{CP}$	Waveform 2	3.0 3.0				3.0 3.0	
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to $\overline{CP}$	Waveform 2	4.0 4.0				4.0 4.0	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW M to $\overline{CP}$	Waveform 2	4.0 6.5				4.5 7.5	
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW M to $\overline{CP}$	Waveform 2	0 2.0				0 2.0	
$t_s(L)$	Set-up time, LOW $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0				10.0	
$t_h(H)$	Hold time, HIGH $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0				10.0	
$t_w(H)$ $t_w(L)$	$\overline{CP}$ pulse width HIGH or LOW	Waveform 2	4.0 6.0				4.0 6.0	

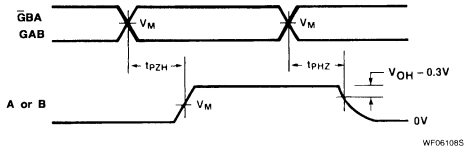
AC WAVEFORMS



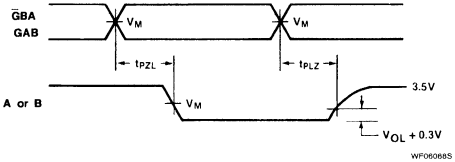
Waveform 1. Clock To Output Delays And Clock Pulse Width



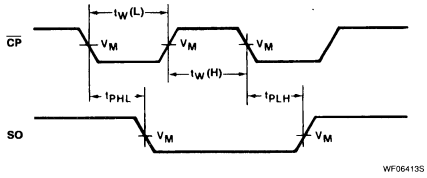
Waveform 2. Data Set-up And Hold Times



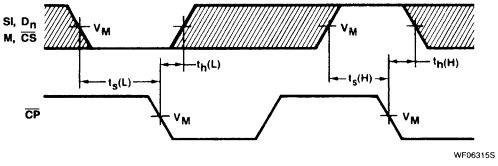
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



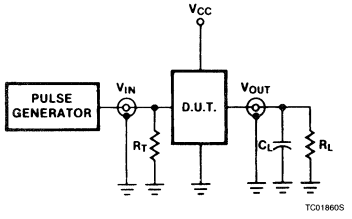
Waveform 5. Clock To Output Delays And Clock Pulse Width



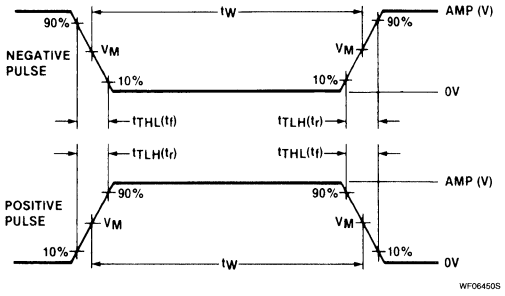
Waveform 6. Data Set-up And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F732, 74F733
Multiplexers

'F732 Quad Data Multiplexer, Inverting (3-State)
'F733 Quad Data Multiplexer, Non-Inverting (3-State)
Preliminary Specification

Logic Products

FEATURES

- **Quad 2-to-1 (two busses to one bus) Multiplexer**
- **Data can flow in either direction between busses resulting in six-way data paths (A → B, A → C, B → A, B → C, C → A, C → B)**
- **A built-in "break-before-make" feature eliminates current glitches and simplifies PC board design**
- **Output Enable for each bus to allow flexible contention control**
- **3-State outputs sink 64mA**

DESCRIPTION

'F732/'F733 are Quad Data Multiplexers designed to provide a simple means to control the flow of bidirectional data between three data busses.

The 'F732/'F733 consist of four multiplexers. Each multiplexer has three I/O (A_n,B_n,C_n) pins and one Output Enable ($\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$) pins. There are 3 Select (S_0,S_1,S_3) pins to control data flow paths for all four multiplexers.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F732	8.0ns	80mA
74F733	8.0ns	80mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F732N, N74F733N
Plastic SOL-20	N74F732D, N74F733D

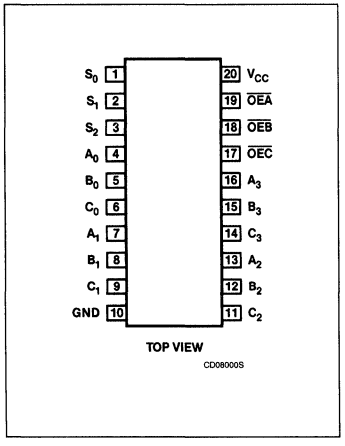
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

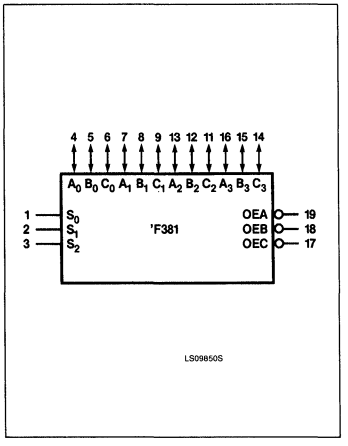
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	Data inputs for Bus A	4.0/4.0	80μA/2.4mA
$B_0 - B_3$	Data inputs for Bus B	2.0/2.0	40μA/1.2mA
$C_0 - C_3$	Data inputs for Bus C	2.0/2.0	40μA/1.2mA
$S_0 - S_2$	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$	Output enable inputs (active LOW)	1.0/1.0	20μA/0.6mA
$A_0 - A_3$	Data outputs for Bus A	150/106.7	3.0mA/64mA
$B_0 - B_3$	Data outputs for Bus B	150/106.7	3.0mA/64mA
$C_0 - C_3$	Data outputs for Bus C	150/106.7	3.0mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20,μA in the HIGH state and 0.6mA in the LOW state.

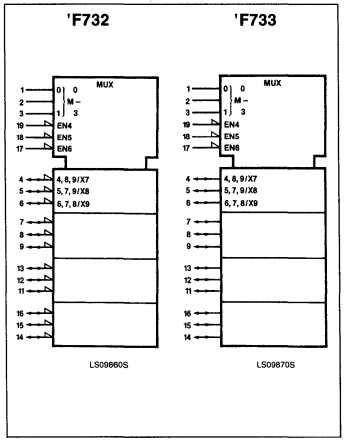
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



With the Select control, data can flow in the following directions between busses: A to B, A to C, B to A, B to C C to A,C to B, A to B and C.

A built-in "break-before-make" feature eliminates current glitches common to systems using 3-State transceivers to accomplish the same function.

FUNCTION TABLE

INPUTS						OPERATING MODE
S_0	S_1	S_2	$\overline{OEA}$	$\overline{OEB}$	$\overline{OEC}$	
X	X	X	H	X	X	Bus A disabled except for input
X	X	X	X	H	X	Bus B disabled except for input
X	X	X	X	X	H	Bus C disabled except for input
L	L	L	X	X	L	Data flow from Bus A to Bus C
H	L	L	L	X	X	Data flow from Bus C to Bus A
L	L	H	X	X	L	Data flow from Bus B to Bus C
H	L	H	X	L	X	Data flow from Bus C to Bus B
L	H	L	X	L	X	Data flow from Bus A to Bus B
H	H	L	L	X	X	Data flow from Bus B to Bus A
L	H	H	X	L	L	Data flow from Bus A to Bus B and Bus C

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER				TEST CONDITIONS[1]			74F732,74F733			UNIT
							Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$, $S_0 - S_3$		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$, $S_0 - S_3$		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OZH} + I_{IH}	Off-state output current, HIGH-level voltage applied	$A_0 - A_3$		V_{CC} = MAX, V_I = 2.7V					100	μA
		$B_0 - B_3$, $C_0 - C_3$							70	μA
I_{OZL} + I_{IL}	Off-state output LOW-level current, voltage applied	$A_0 - A_3$		V_{CC} = MAX, V_O = 0.5V					−2.4	mA
		$B_0 - B_3$, $C_0 - C_3$							−0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)		I_{CCH}	V_{CC} = MAX					70	mA
		'F732	I_{CCL}						100	mA
			I_{CCZ}						85	mA
		'F733	I_{CCH}						80	mA
			I_{CCL}						110	mA
			I_{CCZ}						95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F732					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to B_n, C_n, A_n	Waveform 1, 2		8.5 8.5				ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1, S_2 to A_n, B_n, C_n	Waveform 1		8.0 8.0				ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4		9.0 9.0				ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4		6.0 6.0				ns

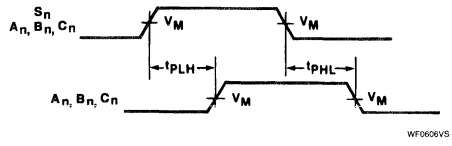
NOTE:
Subtract 0.2ns from minimum values for SO package.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

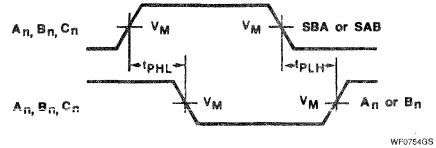
PARAMETER		TEST CONDITIONS	74F733					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to B_n, C_n, A_n	Waveform 1, 2		7.5 7.5				ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1, S_2 to A_n, B_n, C_n	Waveform 1		8.0 8.0				ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4		9.0 9.0				ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4		6.0 6.0				ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

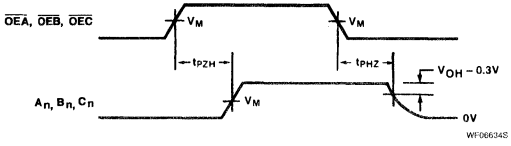
AC WAVEFORMS



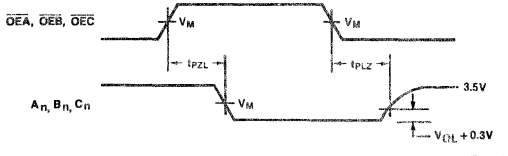
Waveform 1. Propagation Delay Select, Busses To Busses



Waveform 2. Propagation Delay Busses To Busses



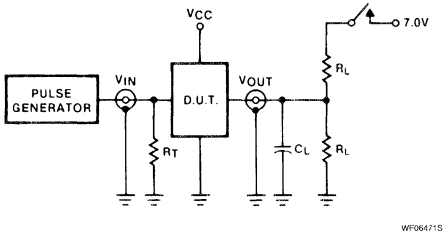
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level From HIGH Level



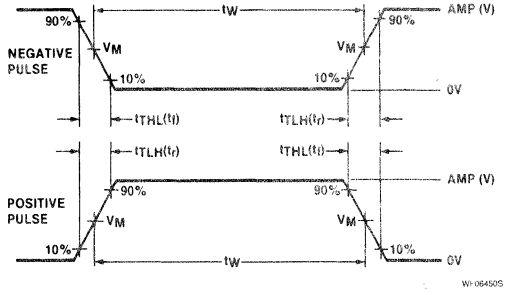
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F764
DRAM Controller

DRAM Dual-Ported Controller
Preliminary Specification

Logic Products

FEATURES

- **Allows two microprocessors to access the same bank of DRAM**
- **Replaces 25 TTL devices to perform arbitration, signal timing, multiplexing, and refresh generation**
- **9 address output pins allow control of up to 256K DRAMS**
- **Separate refresh clock allows adjustable refresh timing**
- **50MHz Maximum Clock rate**

DESCRIPTION

The 74F764 DRAM Dual-Ported Controller is a high-speed, clocked dual port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of memory. The device performs arbitration, signal timing, address multiplexing and refresh, replacing up to 25 discrete TTL devices.

The 'F764 contains an on-board 18-bit address input latch which latches the address inputs at the start of an access cycle.

The device is available in a 40-pin plastic DIP or 44 pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F764	60MHz	150mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F764N
PLCC 44	N74F764A

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

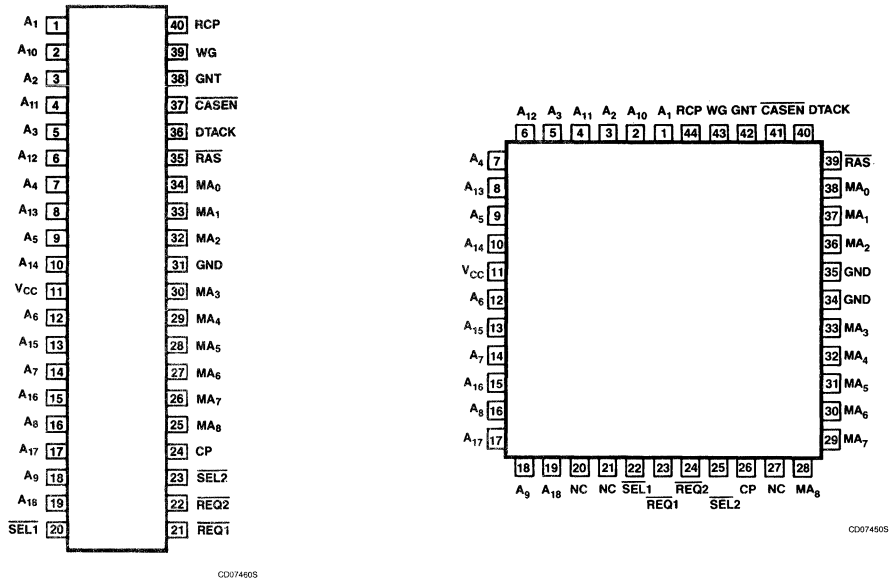
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ1}$, $\overline{REQ2}$	Request inputs (active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
RCP	Refresh clock input	1.0/1.0	20μA/0.6mA
$A_1 - A_{18}$	Address inputs	1.0/1.0	20μA/0.6mA
GNT	Grant output	50/80	1.0mA/48mA
$\overline{SEL1}$, $\overline{SEL2}$	Select outputs (active LOW)	50/80	1.0mA/48mA
DTACK	Data transfer acknowledge output	50/80	1.0mA/48mA
$\overline{RAS}$	Row address strobe output (active LOW)	50/80	1.0mA/48mA
WG	Write gate output	50/80	1.0mA/48mA
$\overline{CASEN}$	Column address strobe enable output (active LOW)	50/80	1.0mA/48mA
$MA_0 - MA_8$	Address outputs	50/80	1.0mA/48mA

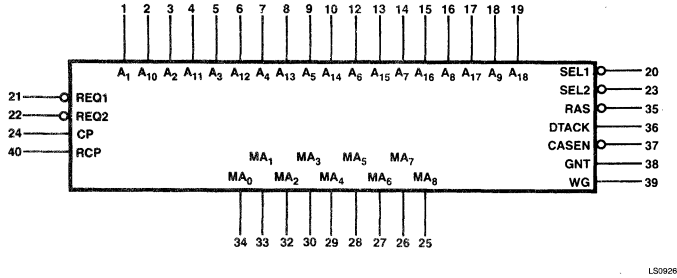
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

6

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A_1	1	1	I	Address inputs used to generate memory row address.
A_2	3	3	I	
A_3	5	5	I	
A_4	7	7	I	
A_5	9	9	I	
A_6	11	12	I	
A_7	13	14	I	
A_8	15	16	I	
A_9	17	18	I	
A_{10}	2	2	I	Address inputs used to generate memory column address.
A_{11}	4	4	I	
A_{12}	6	6	I	
A_{13}	8	8	I	
A_{14}	10	10	I	
A_{15}	12	13	I	
A_{16}	14	15	I	
A_{17}	16	17	I	
A_{18}	18	19	I	
$\overline{REQ1}$	21	23	I	Memory access request from microprocessor one.
$\overline{REQ2}$	22	24	I	Memory access request from microprocessor two.
CP	24	26	I	Clock input which determines the master timing and arbitration rates.
RCP	40	44	I	Refresh Clock determines the period of refresh for each row after it is internally divided by 64.
$\overline{SEL1}$	20	22	O	Select signal is activated in response to the active $\overline{REQ1}$ input, indicating that access will be granted to microprocessor one.
V_{CC}	11	11		Power supply +5V ±10%
GND	31	34 35		Ground
$\overline{SEL2}$	20	25	O	Select signal is activated in response to the active $\overline{REQ2}$ input, indicating that access will be granted to microprocessor two.
MA_0	34	38	O	Memory address output pins, designed to drive the address lines of a DRAM.
MA_1	33	37	O	
MA_2	32	36	O	
MA_3	30	33	O	
MA_4	29	32	O	
MA_5	28	31	O	
MA_6	27	30	O	
MA_7	26	29	O	
MA_8	25	28	O	
GNT	38	42	O	Grant output internally activated upon start of memory access cycle.
$\overline{RAS}$	35	39	O	Row address strobe is used to latch the row address into the bank of DRAM (to be connected directly to the $\overline{RAS}$ inputs of the DRAMs).
WG	39	43	O	When activated, the "Write Gate" signal from the device could be gated with the microprocessor's write strobe to perform an "Early Write".
$\overline{CASEN}$	37	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs.
DTACK	36	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has occurred.

DRAM Controller | FAST 74F764

ARCHITECTURE

The 'F764 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. The $\overline{SEL}$ output signals have been provided for use as look-ahead enables for 3-State address lines from each of the microprocessors connected to the address inputs of the 'F764.

The second arbitration stage controls arbitration between the $\overline{SEL}$ signals and refresh requests. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle via the GNT output signal. GNT is provided to indicate to the requesting microprocessor that its access cycle has begun. The GNT and $\overline{SEL}$ outputs can be used to generate wait states.

The 'F764 has an 18-bit internal latch which latches the address inputs, $A_1 - A_{18}$, at the start of the access cycle. The latched address inputs are propagated to the $MA_0 - MA_8$ address outputs via an internal 18-bit MUX, which multiplexes the 18 address inputs to 9 row address and 9 column address signals, giving the 'F764 the capability to interface 256K DRAMs to the masters.

The internal refresh row counter has 9 outputs, allowing the 'F764 to refresh up to 512 row DRAMs.

The generation of $\overline{RAS}$, $\overline{CASEN}$, WRITE GATE (WG), and Data Transfer Acknowledge (DTACK) outputs is controlled by on-chip timing logic.

FUNCTIONAL DESCRIPTION

The speed at which the 'F764 operates is determined by the CP input, with a maximum limit of 50MHz. All internal signal timing and control is based on this input.

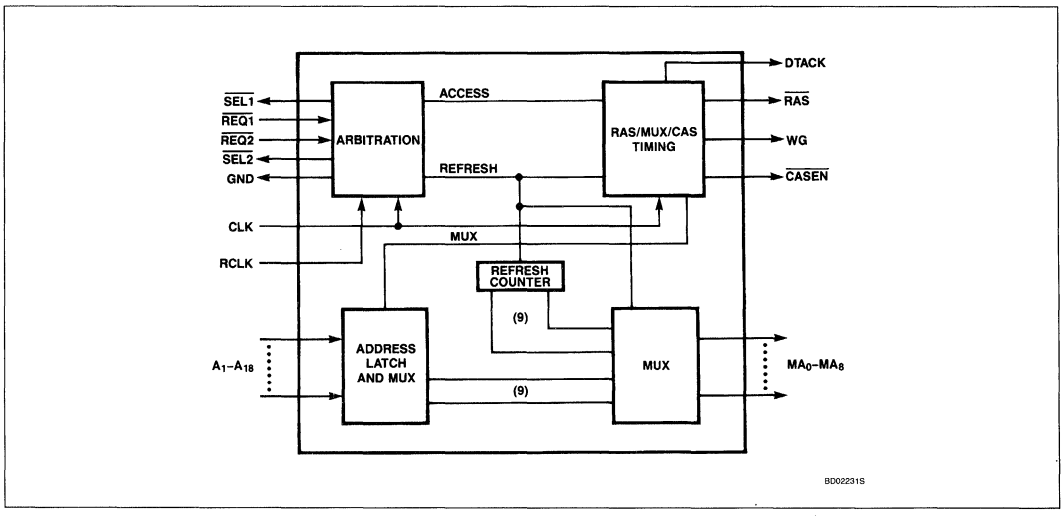
A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will go LOW to indicate that access will be granted. The GNT output then goes HIGH (by the LOW-to-HIGH transition) indicating that a memory access cycle is now commencing. If an access or refresh cycle is in process, and the other microprocessor has not requested access, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will go LOW to indicate that access will be granted, but GNT will not go HIGH until the current cycle is completed. After completion of current cycle, and followed by a synchronization period, GNT will automatically become active.

If access to the DRAM is requested by both microprocessors, the initial arbitration stage will determine which processor will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress at the time access is requested. $\overline{REQ}$ contention is arbitrated by internal circuitry sampling the $\overline{REQ1}$ and $\overline{REQ2}$ inputs on different edges of the CP input: $\overline{REQ1}$ is sampled on the rising edge of the clock and $\overline{REQ2}$ is sampled on the falling edge of the same clock. Specially designed CTL flip-flops have been used in this circuitry to eliminate meta-stable states. Again, if a refresh cycle is in progress, the GNT output will not become active until the refresh cycle is completed.

When GNT becomes true on the 'F764, the $A_1 - A_{18}$ address input signals are latched internally and the $A_1 - A_9$ signals are propagated to the $MA_0 - MA_8$ output pins. One-half clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is brought valid.

At the next half clock cycle, the $A_{10} - A_{18}$ latch outputs in the 'F764 are selected and propagated to the $MA_0 - MA_9$ outputs. The write gate (WG) output becomes valid at this time to indicate the proper time to gate the WRITE signal from the selected processor to the DRAM to perform an EARLY WRITE cycle. One-half clock cycle is again allowed for the $A_{10} - A_{18}$ signals to propagate and stabilize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as a CAS output or decoded with higher-order address signals to produce multiple CAS signals. Once $\overline{CASEN}$ is valid, the controller will wait three clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of 4 clock cycles. At the time $\overline{RAS}$ becomes inactive, the DTACK output becomes true to indicate that data on the DRAM data lines is valid, or that the proper access time has been met. DTACK can be used to indicate a valid data transfer acknowledge for processors requiring this signal. All controller output signals will be held in this final state until the selected processor withdraws its request by driving its $\overline{REQ}$ input HIGH. When the request is withdrawn, internal synchronization takes place, the control-

BLOCK DIAGRAM

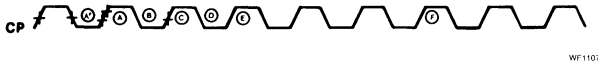


ler output signals become inactive, and any pending access or refresh cycles are serviced.

The refresh cycle commences from internally generated refresh requests. RCP is divided by 64 to produce a refresh request internally. Refresh requests are arbitrated with $\overline{SEL}$ outputs in the second stage of arbitration. Refresh always has priority and will be serviced immediately or upon completion of the current access cycle. At the start of a refresh grant, the 9 refresh counter address signals are allowed to propagate to the $MA_0 - MA_8$ outputs for one-half clock, at which time the $\overline{RAS}$ signal becomes active for 4 clock cycles, then inactive for 3 clock cycles to meet the $\overline{RAS}$ precharge requirement of the DRAMs, at which time the refresh cycle is terminated.

All signal outputs on the 'F764 are guaranteed to source 35mA at 2.4V in the HIGH state and sink 60mA in the LOW state. This ensures that the part will incident wave switch the 70Ω lines that are commonly seen in memory arrays using DIP packages.

AC WAVEFORM FOR IMMEDIATE ACCESS (Sequence of events for $\overline{REQ1}$ access when no refresh or $\overline{REQ2}$ access)



WF11070S

A' $\overline{REQ2}$ sampled

A $\overline{REQ1}$ sampled
$\overline{SEL1}$ triggered ($\overline{SEL1}$ triggered by $\overline{REQ1}$ sample circuitry)

B GNT triggered ($\overline{SEL1}$ and GNT propagation paths are the same)
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)
$A_1 - A_9$ propagate to MA outputs

C $\overline{RAS}$ triggered

D WG triggered
$A_{10} - A_{18}$ selected

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

6

SYSTEM CYCLES

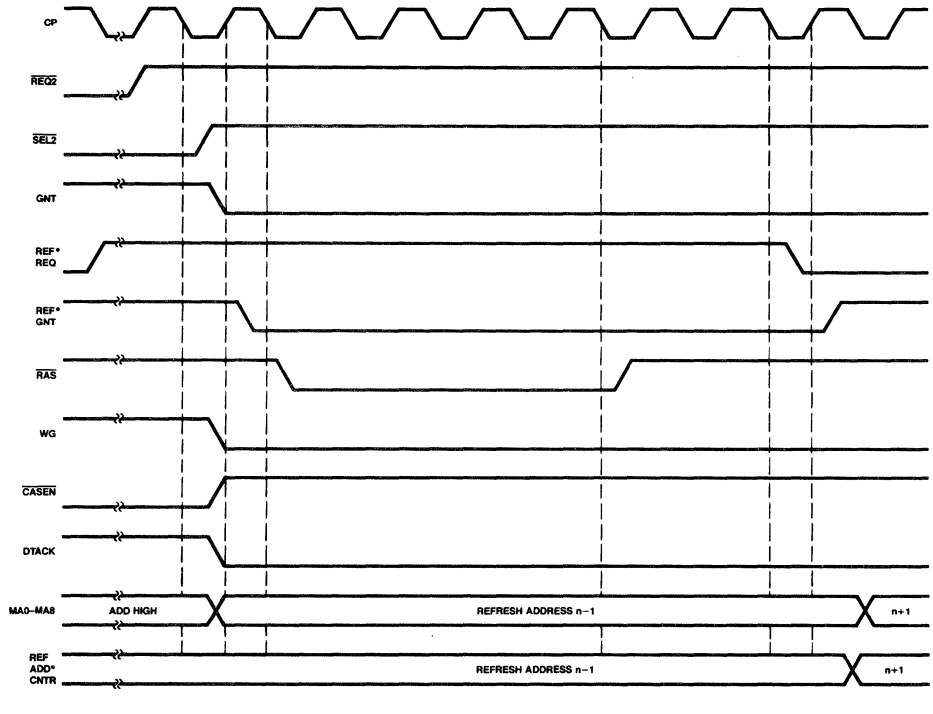
The 74F764 is always in one of the following cycles.

A. IDLE — There is no request pending and the refresh clock has not completed 64 clock cycles since the last refresh request.

B. REFRESH — A refresh request is initiated every 64 refresh clock cycles, unless there is a refresh cycle already in progress. It is a $\overline{RAS}$ only refresh cycle, derived from the clock (CP).

C. REQUEST1 — This is a memory access cycle for processor 1. It can only be initiated when there is no refresh or request 2 cycle in progress.

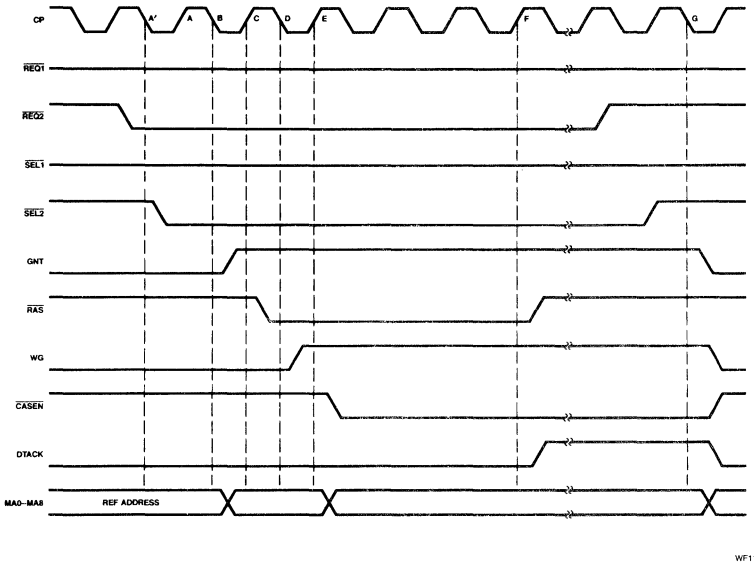
D. REQUEST2 — This is a memory access cycle for processor 2. It can only be initiated when there is no refresh or request 1 cycle in progress.



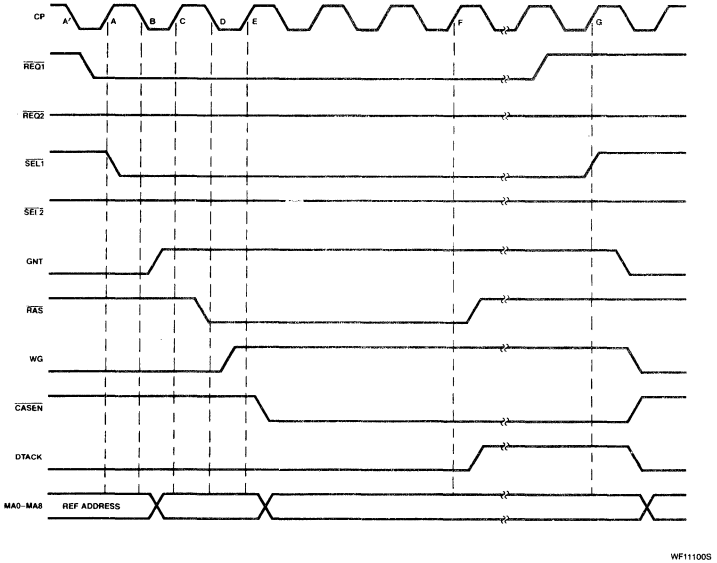
NOTE:
* These are internal signals only.

Refresh Cycle

SYSTEM CYCLES

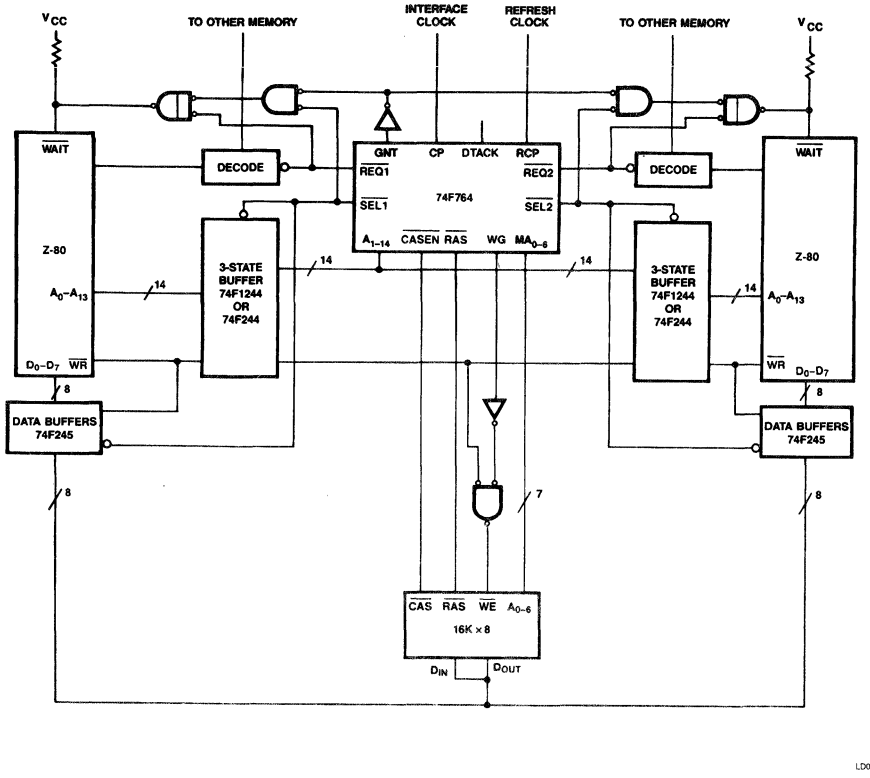


Request 2 Cycle



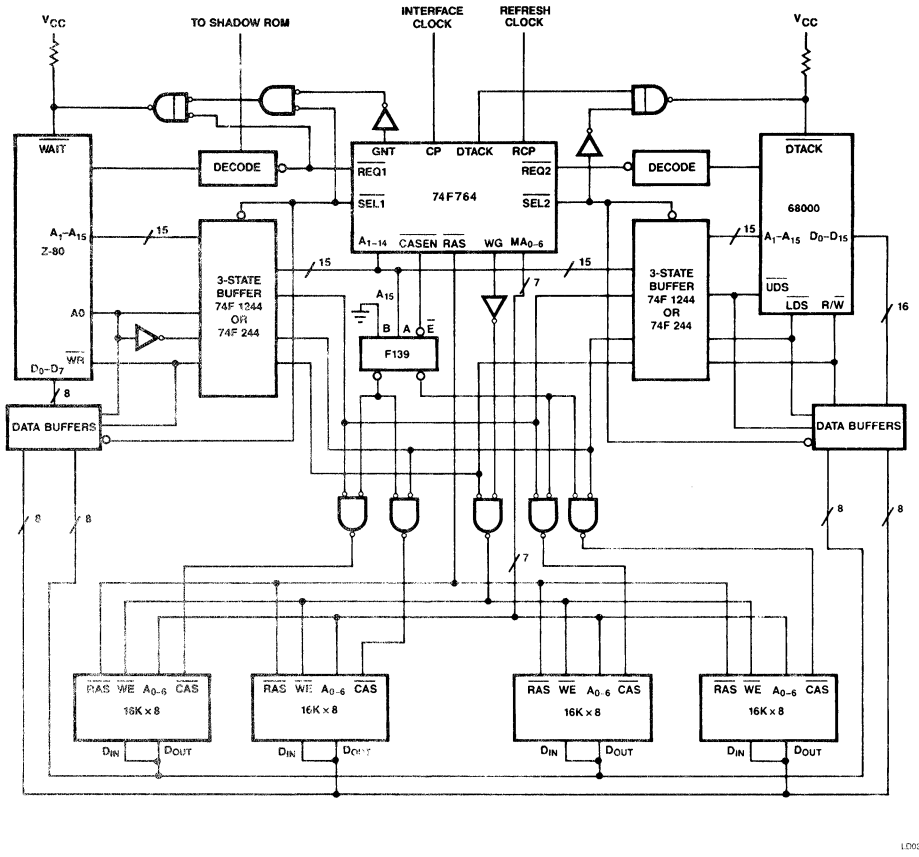
Request 1 Cycle

TYPICAL APPLICATION



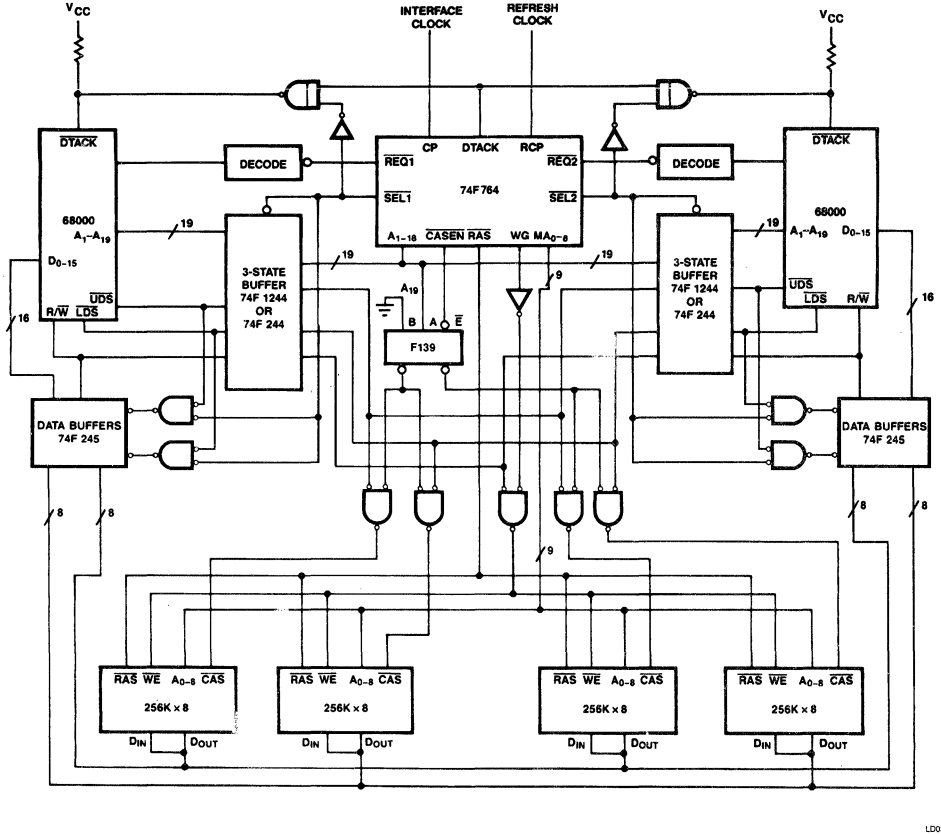
Two Z-80s Sharing 16K RAM

TYPICAL APPLICATION



68000 With Z-80 Sharing 64K RAM

TYPICAL APPLICATION



Two 68000 Processors With 1 Mbyte RAM

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	120	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−35	mA
I_{OL}	LOW-level output current	Buffer			60	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F764			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
				I_{OH2} = −35mA	±10%V_{CC}	2.4			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
				I_{OL2} = 60mA	±10%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OS}	Short circuit output current		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX					120	mA
		I_{CCL}						175	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee the LOW to HIGH transition in a 70Ω transmission line.
4. I_{OL2} is the current necessary to guarantee the HIGH to LOW transition in a 70Ω transmission line.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

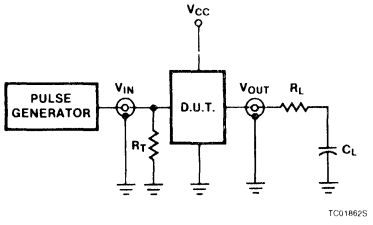
PARAMETER		TEST CONDITIONS	74F764					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 300pF$, $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 300pF$, $R_L = 70\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	AC Waveforms	50	60		50		MHz
t_{PLH} t_{PHL}	Propagation delay CP(↑) to $\overline{SEL1}$		5 5	10 10	14 14	5 5	16 16	ns
t_{PLH} t_{PHL}	Propagation delay CP(↓) to $\overline{SEL2}$		5 5	10 10	14 14	5 5	16 16	ns
t_{PLH}	Propagation delay CP(B) to GNT		5	10	14	5	16	ns
t_{PHL}	Propagation delay (Note 1)		5	10	14	5	16	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(Row Address)		5 5	10 10	15 15	5 5	16 16	ns
t_{PLH}	Propagation delay CP(F) to $\overline{RAS}$		6	12	16	5	18	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$		6	12	16	5	18	ns
t_{PLH}	Propagation delay CP(D) to WG		5	10	14	5	16	ns
t_{PHL}	Propagation delay (Note 1)		8	10	14	5	16	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(Column Address)		6 6	12 12	16 16	5 5	18 18	ns
t_{PLH}	Propagation delay (Note 1)		5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$		5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(F) to DTACK		5	10	14	5	16	ns
t_{PHL}	Propagation delay (Note 1)		5	10	14	5	16	ns
t_{PLH} t_{PHL}	Propagation delay CP(transition) to MA(Refresh)		5 5	10 10	14 14	5 5	16 16	ns

NOTE 1:
These delays are with respect to clock edge "G" of the $\overline{REQ1}$ or $\overline{REQ2}$ access cycle shown on the AC Waveforms.

AC SET-UP REQUIREMENTS

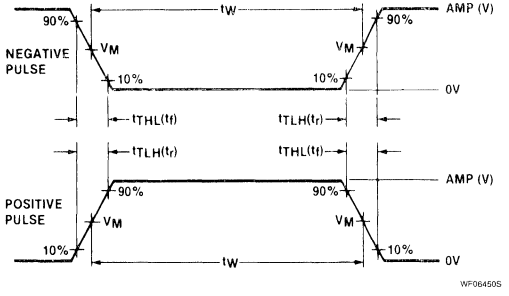
PARAMETER		TEST CONDITIONS	74F764					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 300pF$, $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 300pF$, $R_L = 70\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{REQ1}$, $\overline{REQ2}$ to CP	AC Waveforms	2 2			2 2		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW CP to $\overline{REQ1}$, $\overline{REQ2}$		3 3			3 3		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $A_1 - A_{18}$ to CP(falling edge)		2 2			2 2		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW CP(falling edge) to $A_1 - A_{18}$		4 4			4 4		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW		5 5			5 5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width, HIGH or LOW		4 4			4 4		ns

TEST CIRCUIT AND WAVEFORMS



C_L = 300pF
R_L = 70Ω

Test Circuit Simulating RAM Boards



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

74F765
DRAM Controller

DRAM Dual-Ported Controller
Preliminary Specification

Logic Products

FEATURES

- **Allows two microprocessors to access the same bank of DRAM**
- **Replaces 25 TTL devices to perform arbitration, signal timing, multiplexing, and refresh generation**
- **9 address output pins allow control of up to 256K DRAMS**
- **Separate refresh clock allows adjustable refresh timing**
- **Same as F764 but without address input latch**
- **50MHz Maximum Clock rate**

DESCRIPTION

The 74F765 DRAM Dual-Ported Controller is a high-speed, clocked dual port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of memory. The device performs arbitration, signal timing, address multiplexing and refresh, replacing up to 25 discrete TTL devices.

The 'F765 is an unlatched option of the 'F764, designed to be used in systems that provide latched address lines.

The device is available in a 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

TYPE	TYPICAL fMAX	TYPICAL SUPPLY CURRENT (TOTAL)
74F765	50MHz	mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F765N
PLCC-44	N74F765A

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

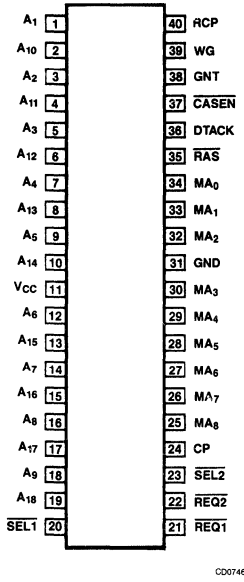
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ1}$, $\overline{REQ2}$	Request inputs (active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
RCP	Refresh clock input	1.0/1.0	20μA/0.6mA
A1 – A18	Address inputs	1.0/1.0	20μA/0.6mA
GNT	Grant output	50/80	1.0mA/48mA
$\overline{SEL1}$, $\overline{SEL2}$	Select outputs (active LOW)	50/80	1.0mA/48mA
DTACK	Data transfer acknowledge output	50/80	1.0mA/48mA
$\overline{RAS}$	Row address strobe (output active LOW)	50/80	1.0mA/48mA
WG	Write gate output	50/80	1.0mA/48mA
$\overline{CASEN}$	Column address strobe enable output (active LOW)	50/80	1.0mA/48mA
MA0 – MA8	Address outputs	50/80	1.0mA/48ma

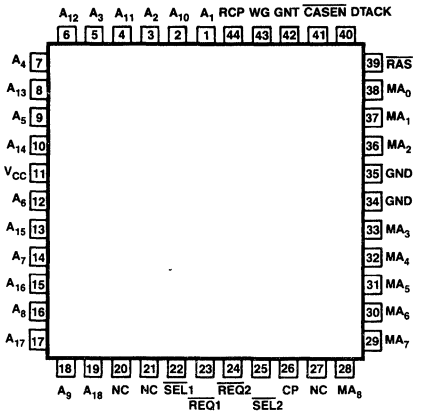
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DRAM Controller 74F765

PIN CONFIGURATION

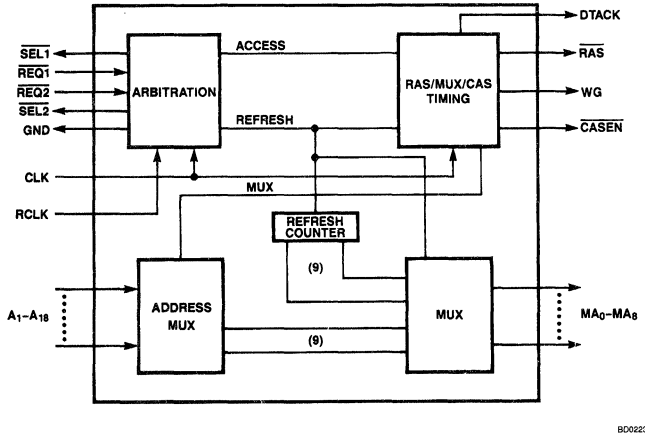


CD07460S



CD07450S

BLOCK DIAGRAM



BD02232S

Signetics

FAST 74F779
8-Bit Counter

8-Bit Bidirectional Binary Counter (3-State)
Product Specification

Logic Products

FEATURES

- **Multiplexed 3-State I/O ports**
- **Built-in lookahead carry capability**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24-pin separate I/O port version**
- **See 'F579 for 20-pin version**

DESCRIPTION

The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0, S_1). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F779	145MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F779N
Plastic SOL-16	N74F779D

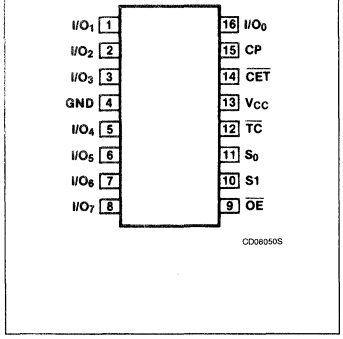
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

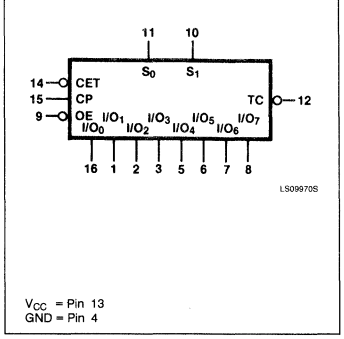
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I/O_0 - I/O_7$	Data inputs	3.5/1.0	70μA/0.6mA
	Data outputs	150/40	3mA/24mA
S_0, S_1	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock input pulse (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active LOW)	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

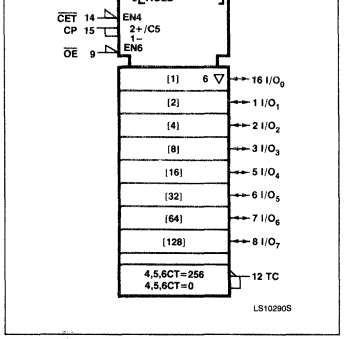
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



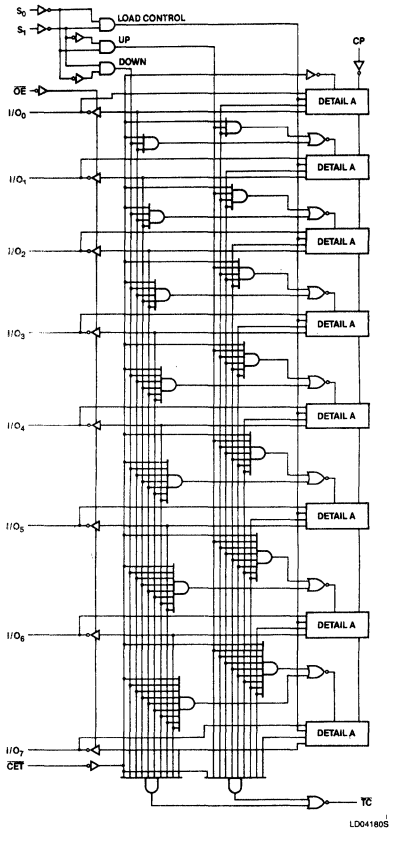
8-Bit Counter | FAST 74F779

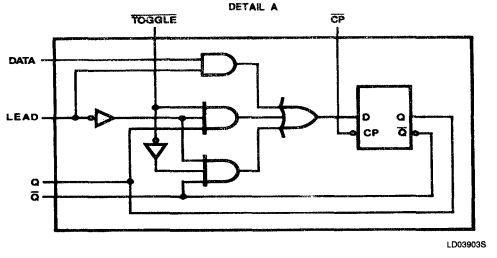
FUNCTION TABLE

INPUTS					OPERATING MODE
S1	S0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/Oa to I/Oh in HIGH Z
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	X	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held HIGH)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = HIGH voltage level
L = LOW voltage level
X = don't care
not LL means S0 and S1 should never both be LOW level at the same time.
↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM





ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$I/O_0 - I/O_7$			−3	mA
		$\overline{TC}$			−1	mA
I_{OL}	LOW-level output current	$I/O_0 - I/O_7$			24	mA
		$\overline{TC}$			20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F779			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$I/O_0 - I/O_7$	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.4			V
		TC		±10%V_{CC}	2.5			V
		all inputs		±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	S_n,CP,$\overline{CET}$,$\overline{OE}$	V_{CC} = MAX, V_I = 7.0V				100	µA
		$I/O_0 - I/O_7$	V_{CC} = 5.5V, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH} + I_{IH}	Off-state current HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_I = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_I = 0.5V				-600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60	-80	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			82	116	mA
		I_{CCL}				91	128	mA
		I_{CCZ}				97	136	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

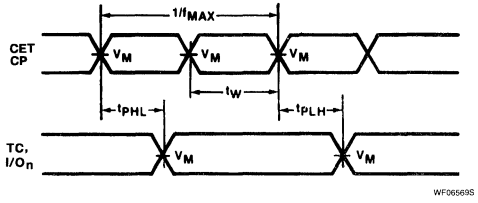
PARAMETER		TEST CONDITIONS	74F779					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	125	145		115		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.5 5.5	7.0 8.0	10.5 10.5	4.5 5.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 4.5	7.0 7.0	9.0 9.0	4.5 4.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.0 3.0	4.5 5.5	6.5 7.5	2.5 2.5	7.5 8.0	ns
t_{PZH} t_{PZL}	Disable time from HIGH or LOW level	Waveform 4 Waveform 5	2.5 4.5	4.5 6.5	7.0 9.0	2.5 4.5	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Enable time from HIGH or LOW level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.5 7.0	1.0 1.0	8.0 8.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

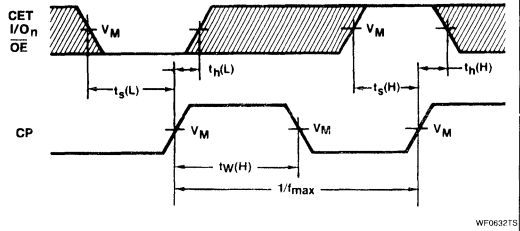
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F779					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW I/O_n to CP	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW I/O_n to CP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CET}$ to CP	Waveform 3	5.0 5.5			5.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW S_n to CP	Waveform 3	8.0 8.0			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width HIGH or LOW	Waveform 1	4.0 4.0			4.0 4.0		ns

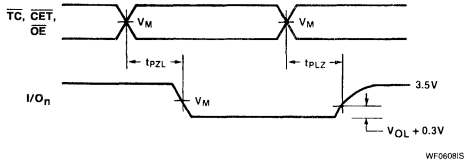
AC WAVEFORMS



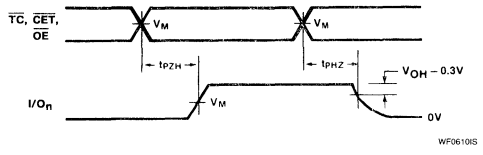
Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Data Set-up And Hold Times



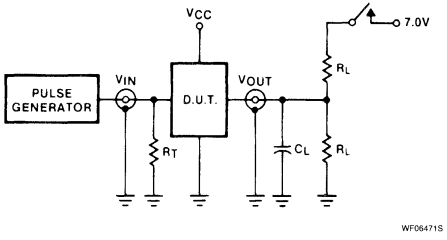
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level



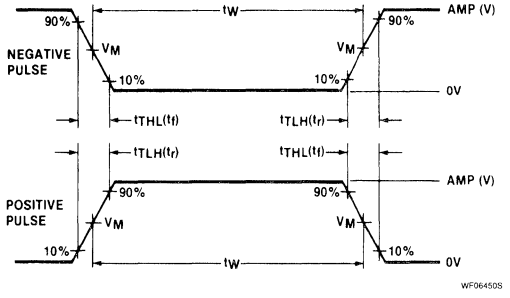
Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F784
Multiplier

8-Bit Serial/Parallel Multiplier (With Adder/Subtractor)
Preliminary Specification

Logic Products

FEATURES

- **Serial (n × 8)-bit multiplication**
- **Final stage adder/subtractor for optional use in adding a B bit to obtain S ±B.**
- **Two's complement multiplication**
- **Cascadable for any number of bits**
- **Full Adder and B – 1 input included for maximum flexibility**
- **Maximum clock frequency 50MHz guaranteed**
- **Supply current 100mA max**

DESCRIPTION

The 'F784 is a serial n × 8-bit multiplier with a final stage adder/subtractor for optional use in adding a B bit to obtain S ±B. A 'B – 1' bit can also be added via an internal flip-flop to achieve a 1-bit delay. The X word is parallel loaded (8 bits wide) into latches and the Y word is clocked in serially from a shift register. The 'F784 is particularly useful for high-speed digital filtering or butterfly networks in fast Fourier transforms.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F784	65 MHz	67mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F784N
Plastic SOL-20	N74F784D

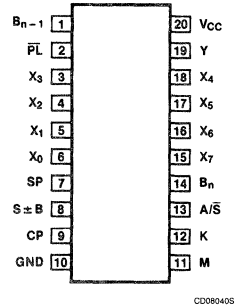
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

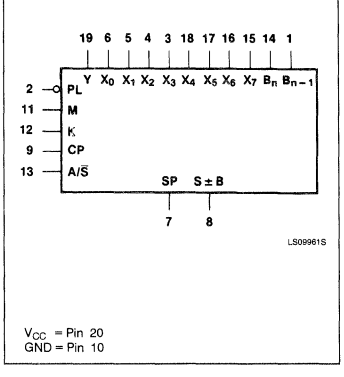
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$X_0 - X_7$	Multiplicand data inputs	1.0/1.0	20μA/0.6mA
Y	Serial multiplier input	1.0/1.0	20μA/0.6mA
CP	Clock pulse input	1.0/1.0	20μA/0.6mA
K	Serial expansion input	1.0/1.0	20μA/0.6mA
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Parallel load input	1.0/2.0	20μA/1.2mA
A/$\overline{S}$	Add/subtract input	1.0/1.0	20μA/0.6mA
B_n	Serial B input	1.0/1.0	20μA/0.6mA
B_{n-1}	Delayed serial B input	1.0/1.0	20μA/0.6mA
SP	Serial X·Y product output	50/33.3	1mA/20mA
S ±B	Serial Y·Y ±B output	50/33.3	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

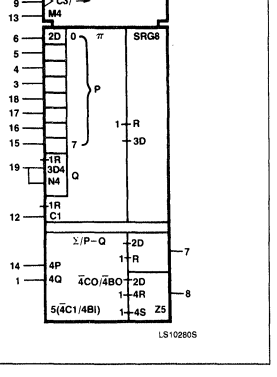
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Multiplier | FAST 74F784

The 'F784 is a serial/parallel 8-bit multiplier. Also included is an adder/subtractor stage. The X word (multiplicand) is loaded into a register while simultaneously clearing the arithmetic cell flip-flops in preparation for a multiplication. The Y word (multiplier) is clocked in serially.

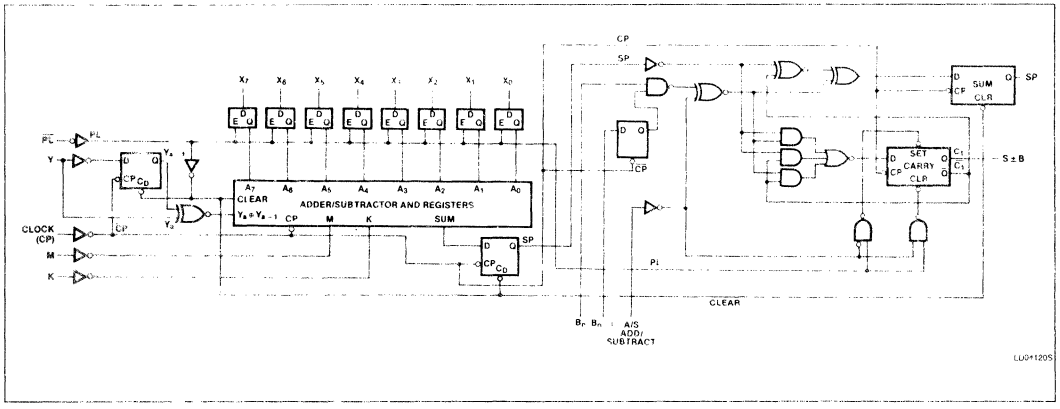
Expansion capability is provided via the M and K inputs. The K (cascade) input is connected to the SO output of the more significant chip. The M (mode) input is used to determine whether the multiplicand is to be treated as a two's complement or unsigned number.

The 'F784 has logic to enable complex arithmetic to be performed. A serial adder/subtractor enables constants to be added to the product. Typically, this feature would be used in FFT butterfly networks to reduce package count and power.

Two outputs are provided; the product X•Y and the product X•Y ± B. Because of the internal adder/subtractor, a speed advantage is gained when using the 'F784 over using a separate adder and multiplier chip.

During a multiplication operation, the first clock cycle is used to load both the X word (multiplicand) and the first bit of the Y word (operand) into the input registers. At this time there is no valid data at the SP output, so that B bits added will not give the correct sum output. In order to load the first B bit on the same clock as X and Y, a B_{n-1} input is provided which delays the B data by one clock cycle. Thus, a valid output results.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F784 Min	74F784 Typ[2]	74F784 Max	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	$\overline{PL}$	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		Others				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			67	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

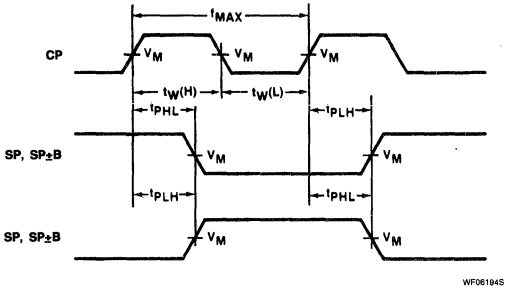
PARAMETER		TEST CONDITIONS	74F784 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F784 T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	50	65		50		MHz
t_{PHL}	Propagation delay $\overline{PL}$ to SP	Waveform 2	6.0		13.0	5.0	14.5	ns
t_{PHL}	Propagation delay $\overline{PL}$ to S ± B	Waveform 2	5.5		12.0	4.5	13.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to SP	Waveform 1	4.0 4.5		9 10.5	3.5 4.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to S ± B	Waveform 1	4.0 4.0		9.0 9.0	3.5 3.5	10.0 10.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

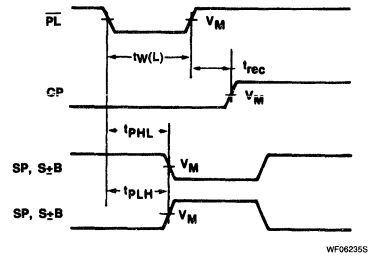
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F784					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time K to CP	Waveform 3	13.0 9.0			14.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time K to CP	Waveform 3	0 1.0			0 1.0		ns
$t_s(H)$ $t_s(L)$	Set-up time Y to CP	Waveform 3	15 15			16.0 16.0		ns
$t_h(H)$ $t_h(L)$	Hold time Y to CP	Waveform 3	1.5 1.5			1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Set-up time X_3 to $\overline{PL}$	Waveform 3	5.0 5.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time X_3 to $\overline{PL}$	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Set-up time B_n to CP	Waveform 3	7.0 7.0			8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time B_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Set-up time $A/\overline{S}$ to CP	Waveform 3	12.0 12.0			13.0 13.0		ns
$t_h(H)$ $t_h(L)$	Hold time $A/\overline{S}$ to CP	Waveform 3	1.5 1.5			1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Set-up time B_n to CP	Waveform 3	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time B_n to CP	Waveform 3	0 0			1.0 1.0		ns
t_{rec}	Recovery time $\overline{PL}$ to CP	Waveform 2	6.5			7.5		ns
$t_W(L)$	Pulse width		5.0			6.0		ns
$t_W(H)$ $t_W(L)$	CP pulse width	Waveform 1	5.0 5.0			6.0 6.0		ns

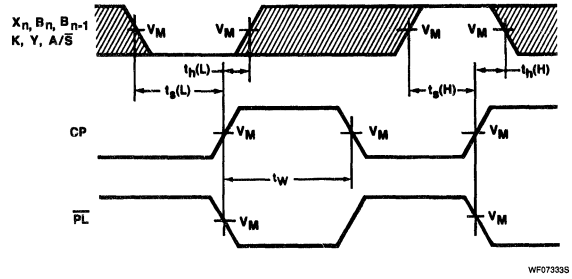
AC WAVEFORMS



Waveform 1. Clock To Output Delays, Clock Pulse Width, And Maximum Clock Frequency



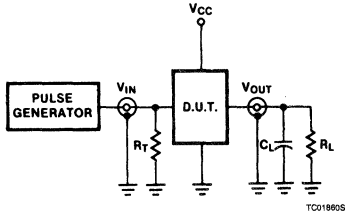
Waveform 2. Parallel Load Pulse Width, Parallel Load To Output Delay And Parallel Load To Clock Recovery Time



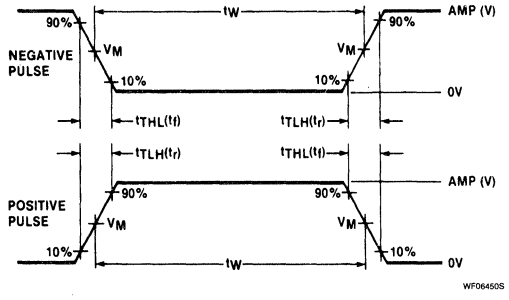
Waveform 3. Data Set-up And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F821/822/823/824/825/826
Bus Interface Registers

Preliminary Specification

'F821 10-Bit Bus Interface Register, Non-Inverting (3-State)
'F822 10-Bit Bus Interface Register, Inverting (3-State)
'F823 9-Bit Bus Interface Register, Non-Inverting (3-State)
'F824 9-Bit Bus Interface Register, Inverting (3-State)
'F825 8-Bit Bus Interface Register, Non-Inverting (3-State)
'F826 8-Bit Bus Interface Register, Inverting (3-State)

FEATURES

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
- **Extra data width for wide address/data paths or buses with parity**
- **High impedance NPN base input structure minimizes bus loading**
- **I_{IL} is 20μA vs 1000μA for AM29821 series**
- **Buffered control inputs reduce AC effects**
- **Ideal where high-speed, light loading, or increased fan-in are required as with MOS microprocessors**
- **Positive and negative overshoots are clamped to ground**
- **3-State outputs glitch free during power-up and down**
- **48mA Sink current**
- **Slim DIP 300 mil package**
- **Broadside pinout**
- **Pin-for-pin and function compatible with AMD AM29821 - 29826 series**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
'F821/ 'F822/ 'F823 'F824/ 'F825/ 'F826	115MHz	75mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F821N, N74F823N, N74F825N N74F822N, N74F824N, N74F826N
Plastic SOL-24	N74F821D, N74F823D, N74F825D N74F822D, N74F824D, N74F826D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/0.033	20μA/20μA
CP	Clock input	1.0/0.033	20μA/20μA
$\overline{EN}$	Clock enable input (active LOW)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master reset input (active LOW)	1.0/0.033	20μA/20μA
$\overline{OE}$ $\overline{OE_n}$	Output enable inputs (active LOW)	1.0/0.033	20μA/20μA
Q_n	Data outputs	150/80	3.0mA/48mA
$\overline{Q_n}$	Data outputs	150/80	3.0mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DESCRIPTION

The 74F821 Series Bus Interface Registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carring parity.

The 'F821 and 'F822 are buffered 10-Bit wide versions of the popular 'F374/ 'F534 functions.

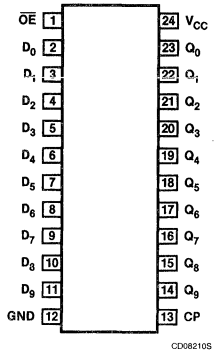
The 'F823 and 'F824 are 9-bit wide buffered registers with Clock Enable and Master Reset which are ideal for parity bus interfacing in high performance microprogrammed systems.

The 'F825 and 'F826 are 8-bit buffered registers with all the 'F823/'F824 controls plus multiple Enables ($\overline{OE_0}$, $\overline{OE_1}$, $\overline{OE_2}$) to allow multiuser control of the interface, e.g., CS, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high $\overline{I_{OL}}/\overline{I_{OH}}$.

6

PIN CONFIGURATION

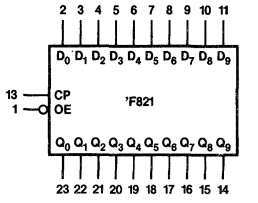
'F821



CD08210S

LOGIC SYMBOL

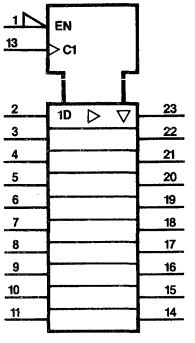
'F821



LS10220S

LOGIC SYMBOL (IEEE/IEC)

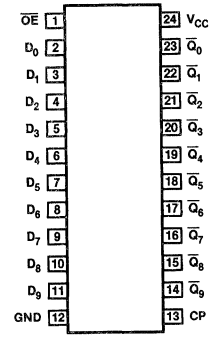
'F821



LS10090S

PIN CONFIGURATION

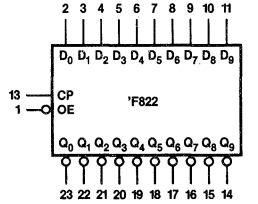
'F822



CD08200S

LOGIC SYMBOL

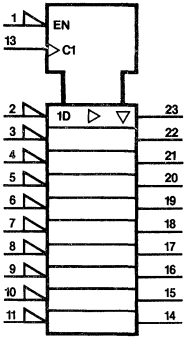
'F822



LS10210S

LOGIC SYMBOL (IEEE/IEC)

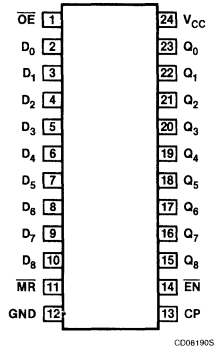
'F822



LS10100S

PIN CONFIGURATION

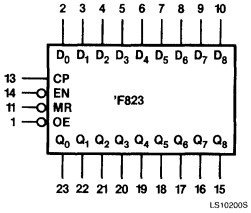
'F823



CD08190S

LOGIC SYMBOL

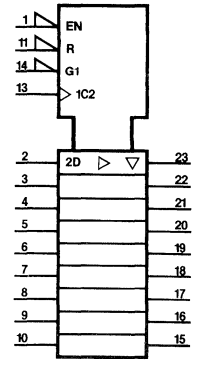
'F823



LS10200S

LOGIC SYMBOL (IEEE/IEC)

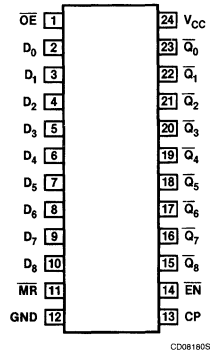
'F823



LS10070S

PIN CONFIGURATION

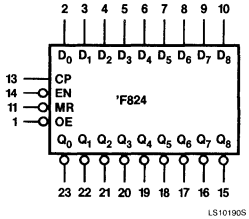
'F824



CD08180S

LOGIC SYMBOL

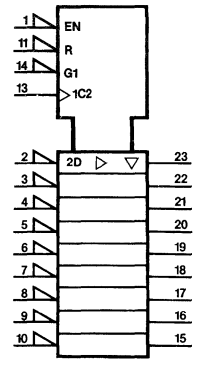
'F824



LS10190S

LOGIC SYMBOL (IEEE/IEC)

'F824



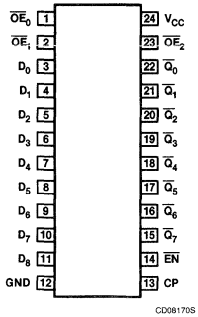
LS10080S

6

Bus Interface Registers FAST 74F821/822/823/824/825/826

PIN CONFIGURATION

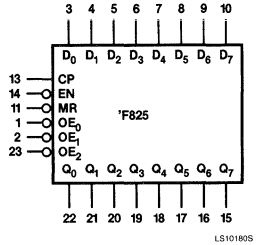
'F825



CD08170S

LOGIC SYMBOL

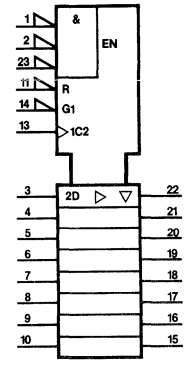
'F825



LS10180S

LOGIC SYMBOL (IEEE/IEC)

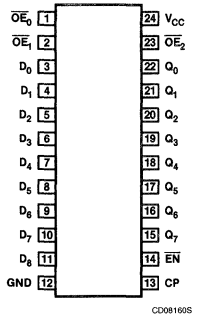
'F825



LS10050S

PIN CONFIGURATION

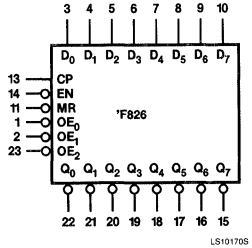
'F826



CD08160S

LOGIC SYMBOL

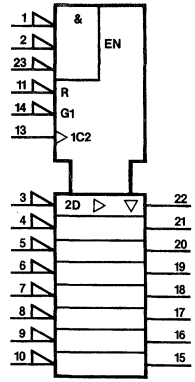
'F826



LS10170S

LOGIC SYMBOL (IEEE/IEC)

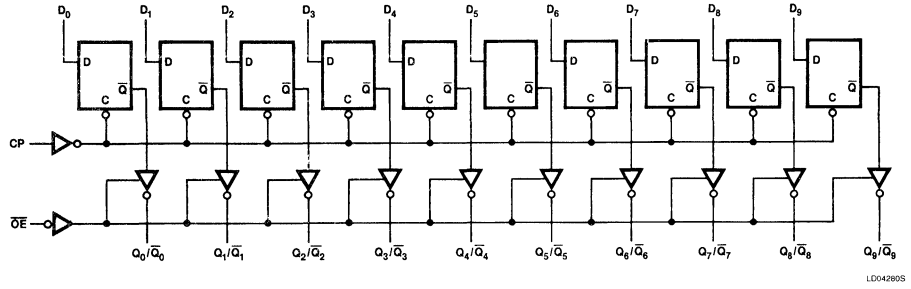
'F826



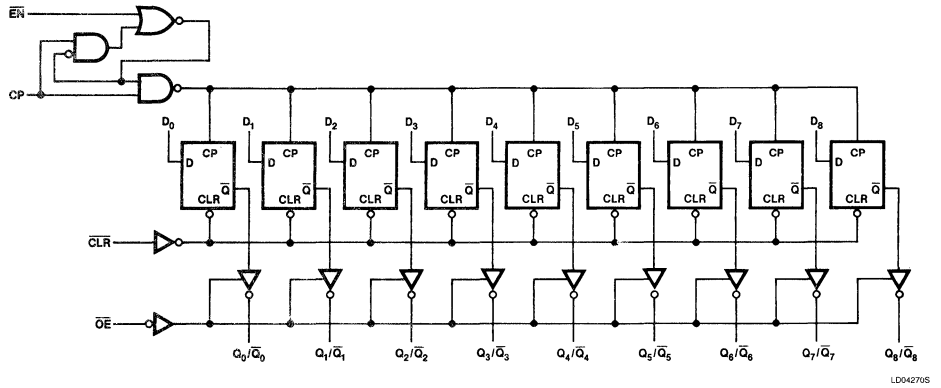
LS10060S

LOGIC DIAGRAM

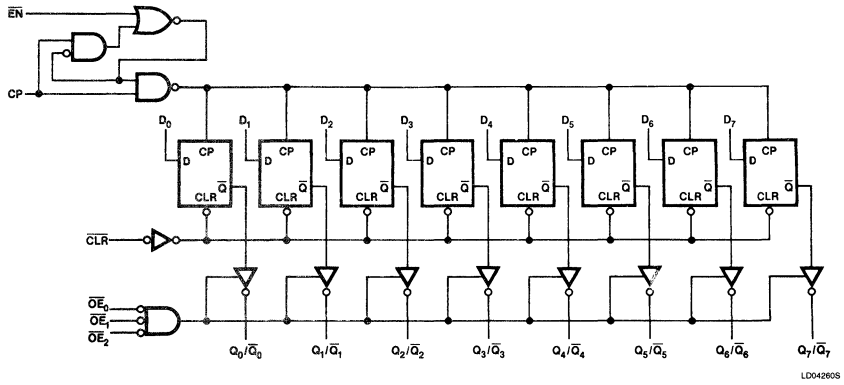
'F821/'F822



'F823/'F824



'F825/'F826



FUNCTION TABLE FOR 'F821 AND 'F822

INPUTS			OUTPUTS	
$\overline{OE}$	CP	D_n	Q 'F821	$\overline{Q}$ 'F822
L	↑	l	L	H
L	↑	h	H	L
L	L	X	No change	No change
L	H	X	No change	No change
H	X	X	Z	Z

FUNCTION TABLE FOR 'F823 AND 'F824

INPUTS					OUTPUTS	
$\overline{OE}$	$\overline{MR}$	$\overline{EN}$	CP	D_n	Q 'F823	$\overline{Q}$ 'F824
L	L	X	X	X	L	L
L	H	L	↑	h	H	L
L	H	L	↑	l	L	H
L	H	H	X	X	No change	No change
H	X	X	X	X	Z	Z

FUNCTION TABLE FOR 'F825 AND 'F826

INPUTS					OUTPUTS	
$\overline{OE}_n$	$\overline{MR}$	$\overline{EN}$	CP	D_n	Q 'F825	$\overline{Q}$ 'F826
L	L	X	X	X	L	L
L	H	L	↑	h	H	L
L	H	L	↑	l	L	H
L	H	H	X	X	No change	No change
H	X	X	X	X	Z	Z

H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	96	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F821, 822, 823 74F824, 825, 826			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−20	μA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V			2	50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V			−2	−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−100		−250	mA
I_{CC}	Supply current (total)	'F821, 'F822	V_{CC} = MAX			75	110	mA
		'F823, 'F824					110	mA
		'F825, 'F826					86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

PRELIMINARY

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

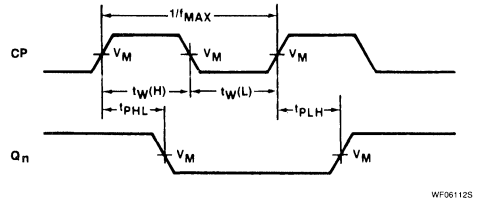
PARAMETER			TEST CONDITIONS	74F821, 74F822, 74F823, 74F824, 74F825, 74F826					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100					MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$		Waveform 1			7.0 9.5			ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	'F823, 'F824 'F825, 'F826	Waveform 2			15.0			ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 4			10.5 9.5			ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 5			7.0 7.0			ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

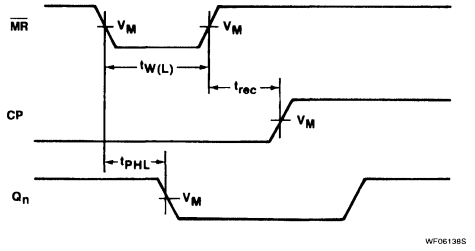
AC SET-UP REQUIREMENTS

PARAMETER			TEST CONDITIONS	74F821, 74F822, 74F823, 74F824, 74F825, 74F826					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to CP		Waveform 3	2.0 2.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to CP		Waveform 3	2.0 2.0					ns
$t_w(H)$ $t_w(L)$	Clock pulse width HIGH or LOW		Waveform 1	5.0 5.0					ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{EN}$ to CP	'F823, 'F824 'F825, 'F826	Waveform 3	3.0 3.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{EN}$ to CP		Waveform 3	0 0					ns
$t_w(H)$ $t_w(L)$	CP pulse width HIGH or LOW		Waveform 1	5.0 5.0					ns
$t_w(L)$	$\overline{MR}$ pulse width, LOW	'F823, 'F824 'F825, 'F826	Waveform 2	5.0					ns
t_{rec}	$\overline{MR}$ recovery time		Waveform 2	5.0					ns

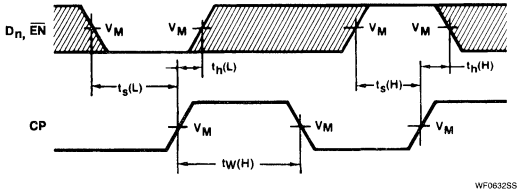
AC WAVEFORMS



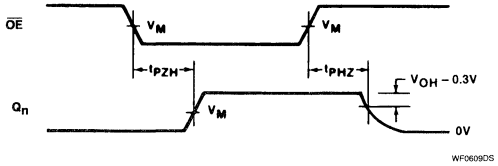
Waveform 1. Clock To Output Delays, Clock Pulse Width, And Maximum Clock Frequency



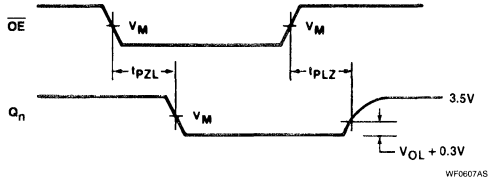
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



Waveform 3. Data And Select Set-up And Hold Times



Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level

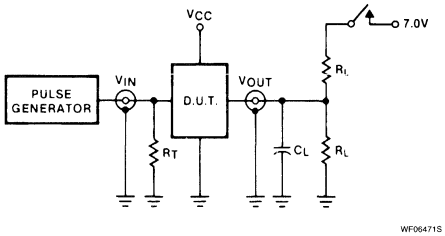


Waveform 5. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

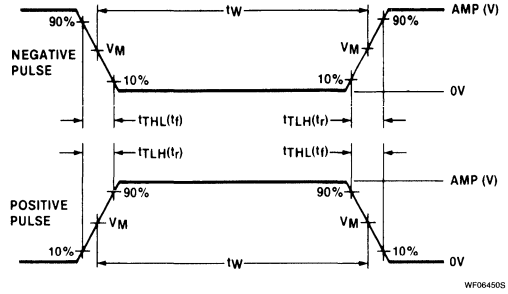
NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

6

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

Logic Products

FAST 74F827, 74F828 Buffers

'F827 10-Bit Buffer/Line Driver, Non-Inverting (3-State)
'F828 10-Bit Buffer/Line Driver, Inverting (3-State)
Preliminary Specification

DESCRIPTION

The 'F827 and 'F828 10-Bit bus buffers provide high performance bus interface buffering for wide data/address paths or busses carrying parity. They have NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

The 'F827 and 'F828 are functionally and pin compatible to AMD AM29827 and AM29828.

The 'F828 is an inverting version of 'F827.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F827 74F828	ns	mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F827N, N74F828N
Plastic SOL-24	N74F827D, N74F828D

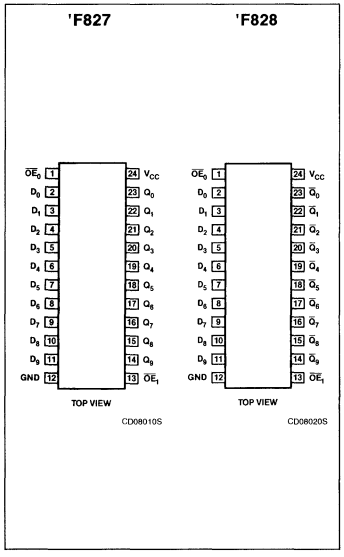
NOTE:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

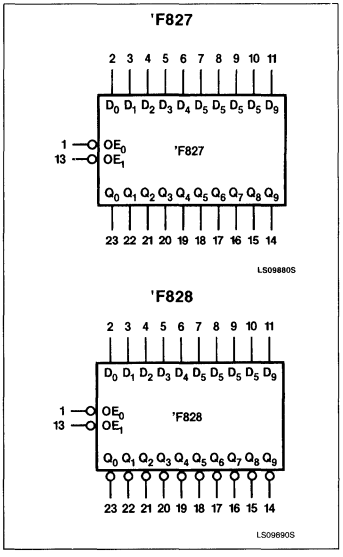
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Data outputs for 'F827	150/80	3mA/48mA
$\overline{Q}_0 - \overline{Q}_7$	Data outputs for 'F828	150/80	3mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

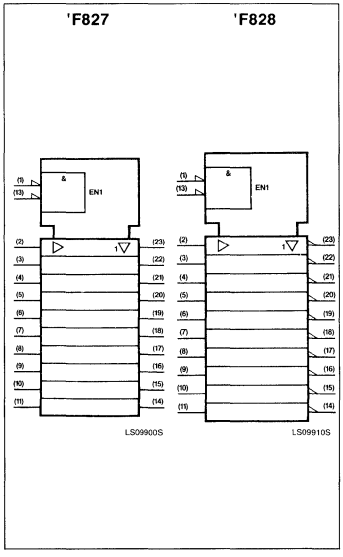
PIN CONFIGURATION



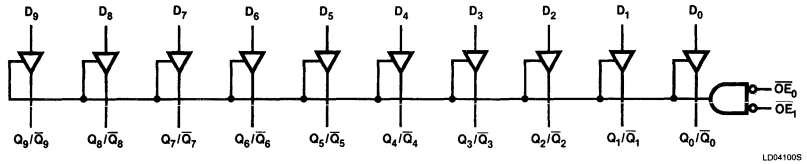
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
		'F827	'F828	
$\overline{OE}$	D_n	Q_n	Q_n	
H	X	H	L	Transparent
L	H	L	H	Transparent
L	X	Z	Z	High Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	96	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F827, 74F828			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.5	V
				±5%V_{CC}		.35	.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			40	60	mA
		I_{CCL}				60	90	mA
		I_{CCZ}				60	90	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

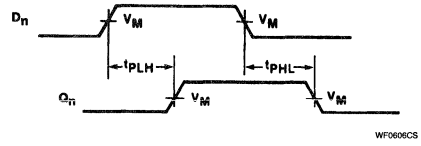
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER			TEST CONDITIONS	74F827, 74F828					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F827	Waveform 1			6.0 5.0			ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F828	Waveform 1			5.0 5.0			ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{OE}$ to Q_n, $\overline{Q}_n$		Waveform 3 Waveform 4			7.0 8.0			ns
t_{PHZ} t_{PLZ}	Output enable time from HIGH or LOW level $\overline{OE}$ to Q_n, $\overline{Q}_n$		Waveform 3 Waveform 4			7.0 8.0			ns

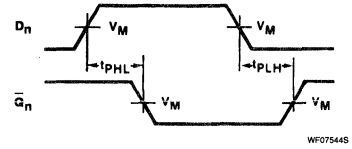
NOTE:
Subtract 0.2ns from minimum values for SO package.

6

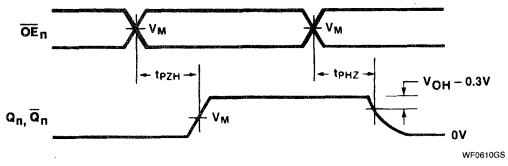
AC WAVEFORMS



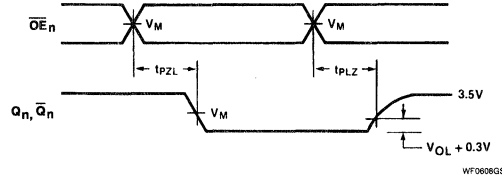
Waveform 1. Propagation Delay For Non-Inverting Outputs



Waveform 2. Propagation Delay For Inverting Outputs



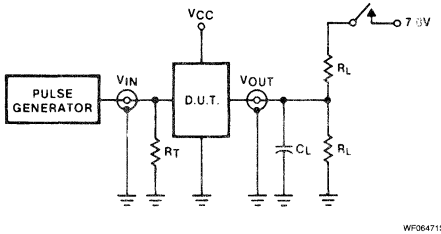
Waveform 3. 3-State Enable Time To HIGH Level And Disable Time From HIGH Level



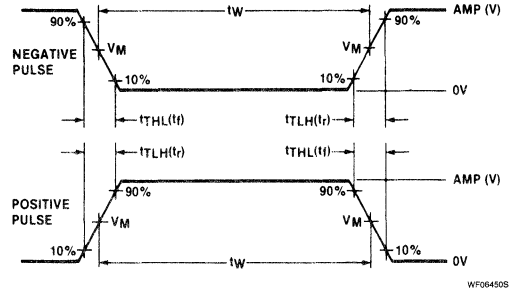
Waveform 4. 3-State Enable Time To LOW Level And Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F841/842/843/844/845/846
Bus Interface Latches

Preliminary Specification

'F841/'F842 10-Bit Bus Interface Latches, NINV/INV (3-State)
'F843/'F844 9-Bit Bus Interface Latches, NINV/INV (3-State)
'F845/'F846 8-Bit Bus Interface Latches, NINV/INV (3-State)

FEATURES

- High-speed parallel latches
- Extra data width for wide address/data paths or buses with parity
- High impedance NPN base input structure minimizes bus loading
- I_{IL} is 20μA vs 1000μA for AM29841 series
- Buffered control inputs to reduce AC effects
- Ideal where high-speed, light loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and down
- 48mA Sink current
- Slim DIP 300mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29841 – 29846 series

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	6.2ns	50mA
74F843, 74F844	6.2ns	50mA
74F845, 74F846	6.2ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F841N, N74F842N, N74F843N N74F844N, N74F845N, N74F846N
Plastic SOL-24	N74F841D, N74F842D, N74F843D N74F844N, N74F845N, N74F846N

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/0.033	20μA/20μA
LE	Latch enable input	1.0/0.033	20μA/20μA
$\overline{OE}$, $\overline{OE}_n$	Output enable input (active LOW)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master reset input (active LOW)	1.0/0.033	20μA/20μA
$\overline{PRE}$	Preset input (active LOW)	1.0/0.033	20μA/20μA
Q_n	Data outputs	150/80	3mA/48mA
$\overline{Q}_n$	Data outputs	150/80	3mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DESCRIPTION

The 'F841 – 'F846 bus interface latch series are designed to provide extra data width for wider address/data paths or busses carrying parity. The 'F841 – 'F846 series are functionally and pin compatible to AMD AM29841 – AM29846 series.

The 'F841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the set-up and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When OE is HIGH the output is in the high impedance state. The 'F842 is the inverted output version of 'F841.

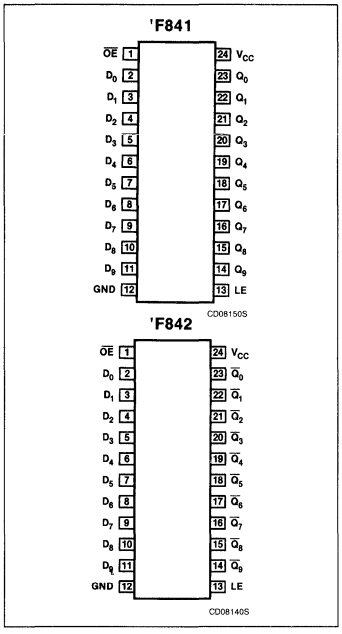
The 'F843 consists of nine D-type latches with 3-State outputs.

In addition to the LE and $\overline{OE}$ pins, the 'F843 has a Master Reset ($\overline{MR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{MR}$ is HIGH, data can be entered into the latch. When $\overline{PRE}$ is LOW, the outputs are HIGH, if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides $\overline{MR}$. The 'F844 is the inverted output version of 'F843. The 'F845 consists of eight D-type latches with 3-State outputs.

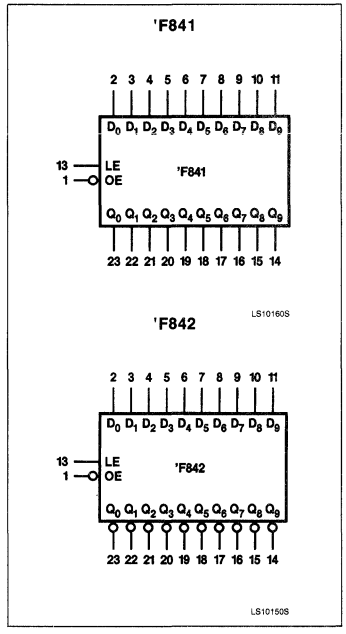
In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 'F845 has two additional $\overline{OE}$ pins making a total of three Output Enable ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) pins.

The multiple Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. The 'F846 is the inverted output version of 'F845.

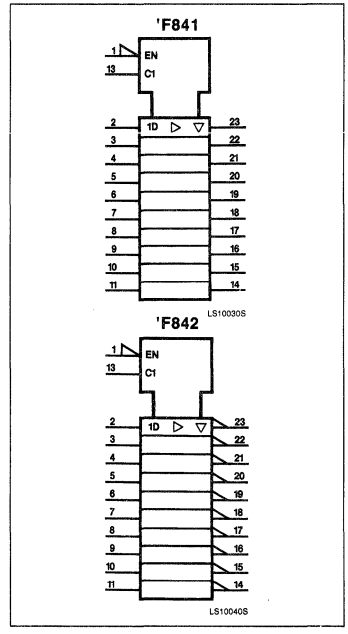
PIN CONFIGURATION



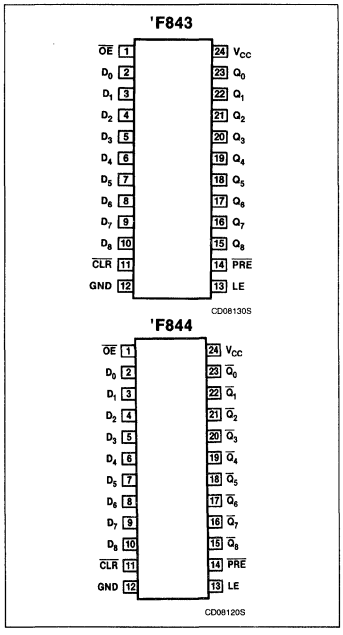
LOGIC SYMBOL



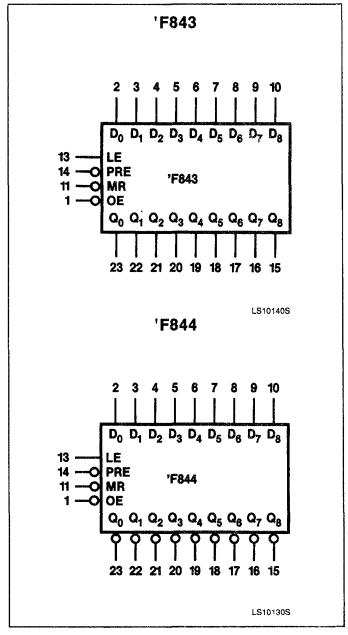
LOGIC SYMBOL (IEEE/IEC)



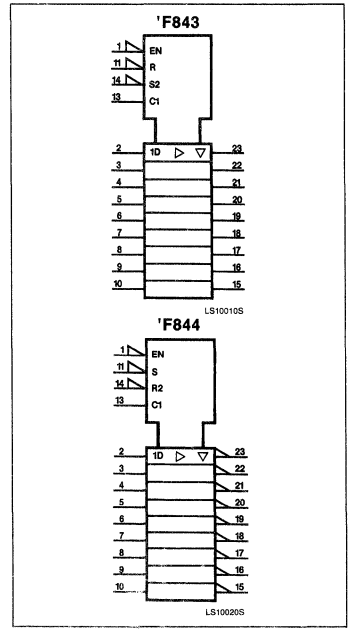
PIN CONFIGURATION



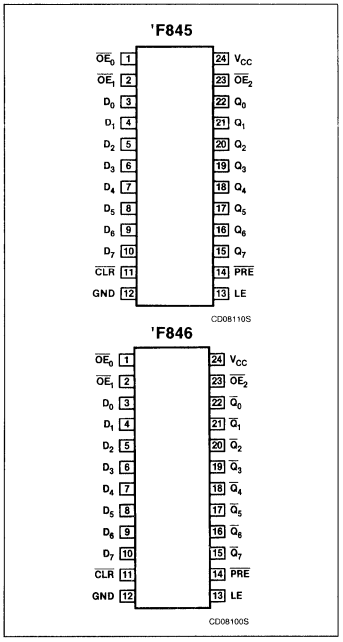
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



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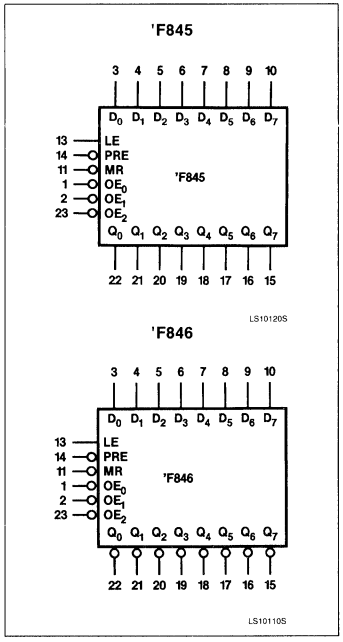

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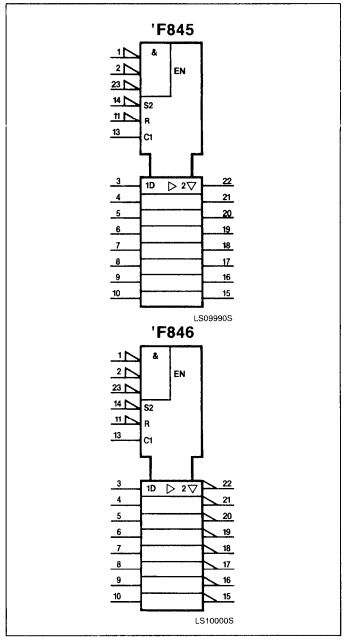

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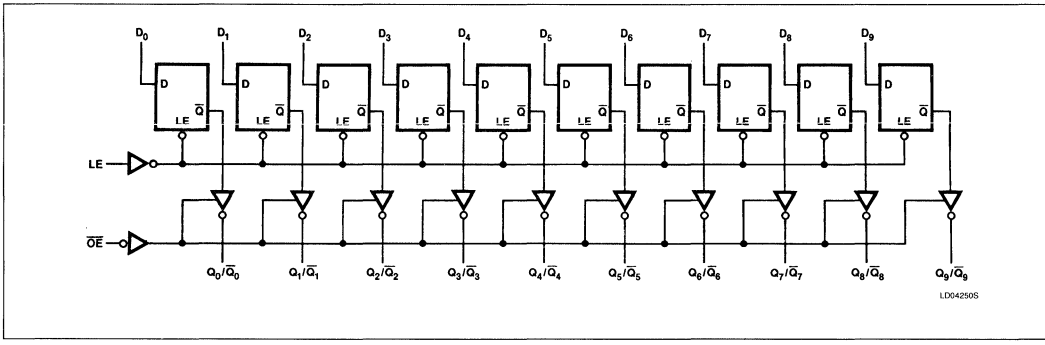
LOGIC DIAGRAM FOR 'F841 AND 'F842

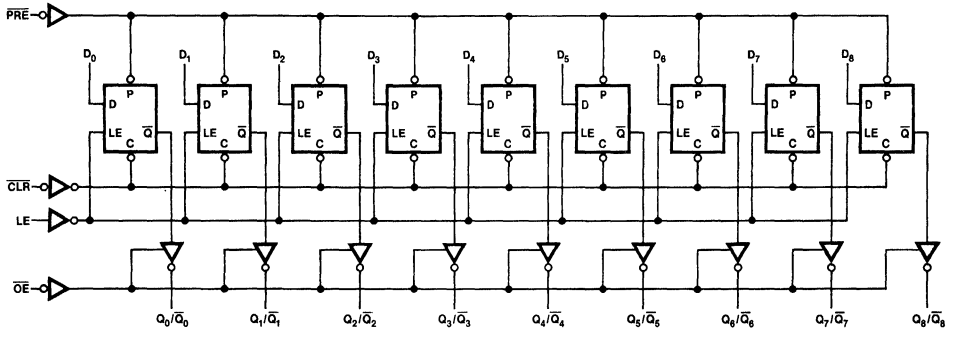


FUNCTION TABLE FOR 'F841 AND 'F842

INPUTS			OUTPUTS		OPERATING MODE
			'F841	'F842	
$\overline{OE}$	LE	D_n	Q	$\overline{Q}$	
L	H	L	L	H	
L	H	H	H	L	Transparent
L	L	l	L	H	
L	L	h	H	L	Latched
H	X	X	Z	Z	High Z

H=HIGH voltage level steady state
h=HIGH voltage level one set-up time prior to the HIGH-to-LOW transition of LE
L=LOW voltage level steady state
l=LOW voltage level one set-up time prior to the HIGH-to-LOW transition of LE
X=Don't care
Z=High impedance

LOGIC DIAGRAM FOR 'F843 AND 'F844

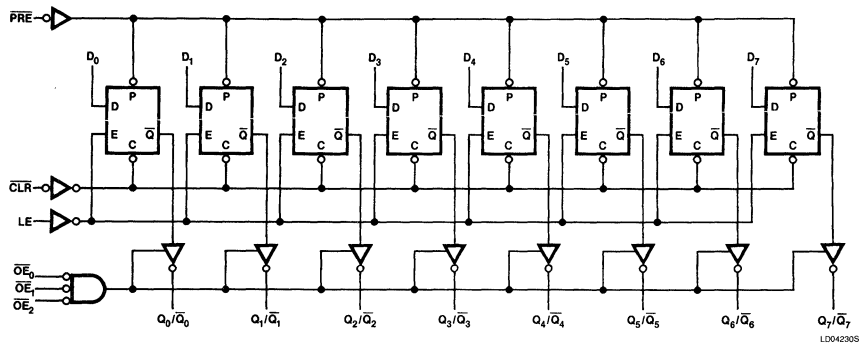


FUNCTION TABLE FOR 'F843 AND 'F844

INPUTS					OUTPUTS		OPERATING MODE
					'F843	'F844	
$\overline{OE}_n$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q	$\overline{Q}$	
H	X	X	X	X	Z	Z	High Z
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L L	H H	H H	L L	L H	L H	H L	Transparent
L L	H H	H H	L L	l h	L H	H L	Latched

H=HIGH voltage level steady state
h=HIGH voltage level one set-up time prior to the HIGH-to-LOW transition of LE
L=LOW voltage level steady state
l=LOW voltage level one set-up time prior to the HIGH-to-LOW transition of LE
X=Don't care
Z=High impedance

LOGIC DIAGRAM FOR 'F845 AND 'F846



FUNCTION TABLE FOR 'F845 AND 'F846

INPUTS					OUTPUTS		OPERATING MODE
					'F845	'F846	
$\overline{OE}_n$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q	$\overline{Q}$	
H	X	X	X	X	Z	Z	High Z
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	H	H	H	L	L	H	Transparent
L	H	H	H	H	H	L	
L	H	H	L	l	L	H	Latched
L	H	H	L	h	H	L	

H=HIGH voltage level steady state
h=HIGH voltage level one set-up time prior to the HIGH-to-LOW transition of LE
L=LOW voltage level steady state
l=LOW voltage level one set-up time prior to the HIGH-to-LOW transition of LE
X=Don't care
Z=High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	96	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]		74F841, 74F842 74F843, 74F844 74F845, 74F846			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−20	mA
I_{OZH}	Off-state output current, HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−100		−250	mA
I_{CC}	Supply current (total)	'F841, 'F842	V_{CC} = MAX			50	75	mA
		'F843, 'F844				50	75	mA
		'F845, 'F846				50	75	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

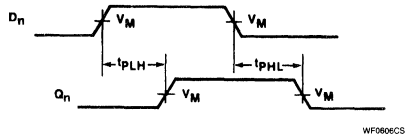
PARAMETER			TEST CONDITIONS	74F841, 74F842, 74F843, 74F844, 74F845, 74F846					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$		Waveform 1 or 2			8.0 6.0			ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$		Waveform 1 or 2			13.0 8.0			ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Q_n or $\overline{Q}_n$	'F843, 'F844 'F845, 'F846	Waveform 3			 9.0			ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	'F843, 'F844 'F845, 'F846	Waveform 3			 18.0			ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 5 Waveform 6			11.0 8.0			ns
t_{PHZ} t_{PLZ}	Output enable time from HIGH or LOW level $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 5 Waveform 6			7.0 5.0			ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

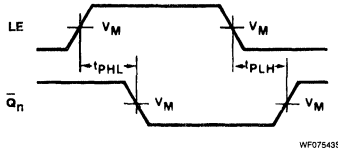
AC SET-UP REQUIREMENTS

PARAMETER			TEST CONDITIONS	74F841, 74F842, 74F843, 74F844, 74F845, 74F846					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW D_n to LE		Waveform 4	3.0 3.0					ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW D_n to LE		Waveform 4	3.0 3.0					ns
$t_w(H)$	LE pulse width HIGH		Waveform 4	4.0					ns
$t_w(L)$	$\overline{PRE}$ pulse width LOW	'F843 – 'F846	Waveform 3	5.0					ns
$t_w(L)$	$\overline{MR}$ pulse width LOW	'F843 – 'F846	Waveform 3	6.0					ns
t_{rec}	$\overline{PRE}$ recovery time	'F843 – 'F846	Waveform 3	12.0					ns
t_{rec}	$\overline{MR}$ recovery time	'F843 – 'F846	Waveform 3	12.0					ns

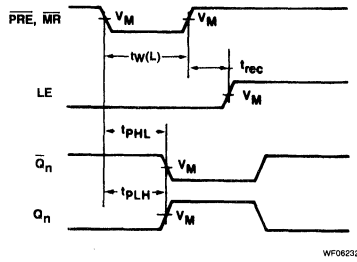
AC WAVEFORMS



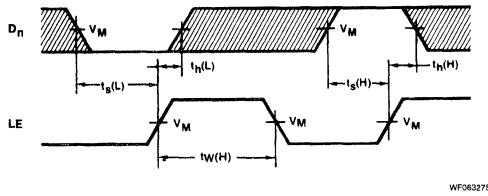
Waveform 1. Propagation Delay For Non-Inverting Outputs



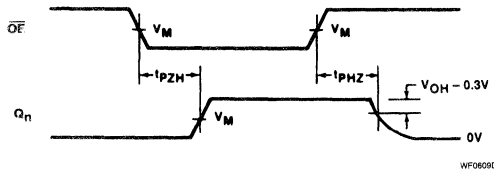
Waveform 2. Propagation Delay For Inverting Outputs



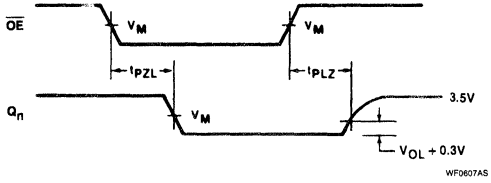
Waveform 3. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



Waveform 4. Data And Select Set-up And Hold Times



Waveform 5. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



Waveform 6. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

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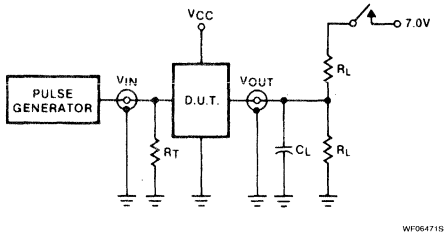
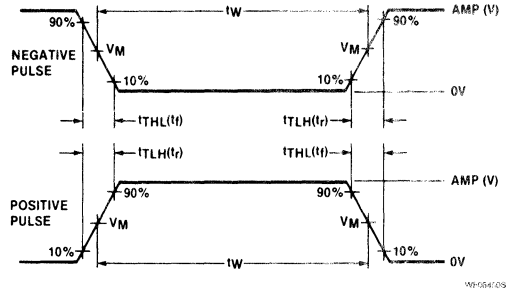
TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

Logic Products

FAST 74F861, 74F862, 74F863, 74F864
Bus Transceivers

'F861/'F862 10-Bit Bus Transceivers, NINV/INV (3-State)
'F863/'F864 9-Bit Bus Transceivers, NINV/INV (3-State)
Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F861, 74F863	4.5ns	mA
74F862, 74F864	4.0ns	mA

FEATURES

- **High-speed parallel registers address/data paths or buses with parity**
- **High-impedance NPN base input structure minimizes bus loading**
- **I_{IL} is 20μA vs 1000μA for AM29861 series**
- **Buffered control inputs to light loading, or increased fan-in are required as with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-State outputs glitch free during power-up and down**
- **Slim DIP 300mil package**
- **Broadside pinout compatible with AMD AM29861 - 29864 series**

DESCRIPTION

The 'F861 series Bus Transceivers provide high performance bus interface buffering for wide data/address paths or buses carrying parity.

The 'F863/'F864 9-Bit Bus Transceivers have NORed Transmit and Receive Output Enables for maximum control flexibility.

All Data Transmit and Receive inputs have 200mV minimum input hysteresis to provide improved noise rejection.

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10% , T_A = 0°C to +70°C
Plastic DIP	N74F861N, N74F862N, N74F863N, N74F864N
Plastic SOL-24	N74F861D, N74F862D, N74F863D, N74F864D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L) HIGH/LOW	LOAD VALUE HIGH/LOW
'F861 'F862	$A_0 - A_9$	Data transmit inputs	1.0/0.033	20μA/20μA
	$B_0 - B_9$	Data receive inputs	1.0/0.033	20μA/20μA
	$\overline{OEBA}$	Transmit output enable input	1.0/0.033	20μA/20μA
	$\overline{OEAB}$	Receive output enable input	1.0/0.033	20μA/20μA
	$A_0 - A_9$	Data transmit outputs	150/80	3mA/48mA
	$\overline{B}_0 - \overline{B}_9$	Data receive outputs	150/80	3mA/48mA
'F863 'F864	$A_0 - A_8$	Data transmit inputs	1.0/0.033	20μA/20μA
	$B_0 - B_8$	Data receive inputs	1.0/0.033	20μA/20μA
	$\overline{OEBA}_0$ $\overline{OEBA}_1$	Transmit output enable input	1.0/0.033	20μA/20μA
	$\overline{OEAB}_0$ $\overline{OEAB}_1$	Receive output enable input	1.0/0.033	20μA/20μA
	$A_0 - A_8$	Data transmit outputs	150/80	3mA/48mA
	$B_0 - B_8$	Data receive outputs	150/80	3mA/48mA

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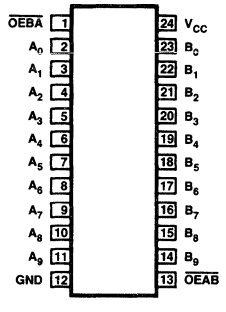
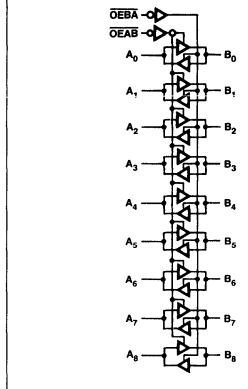
PIN CONFIGURATION

'F861/'F862



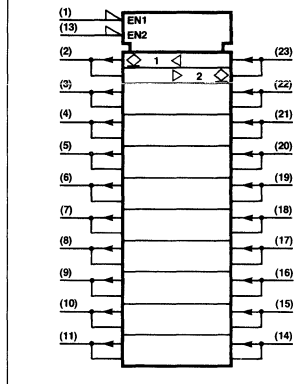
LOGIC SYMBOL

'F861/'F862



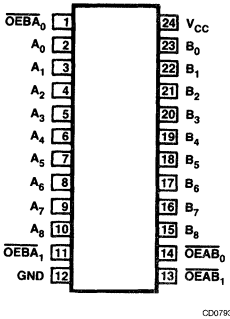
LOGIC SYMBOL (IEEE/IEC)

'F861/'F862



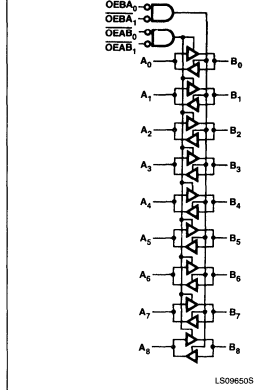
PIN CONFIGURATION

'F863/'F864



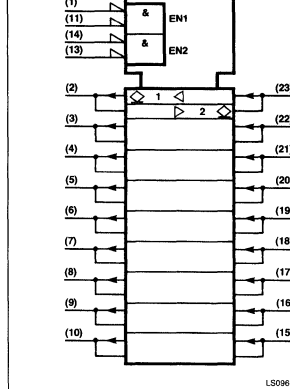
LOGIC SYMBOL

'F863/'F864



LOGIC SYMBOL (IEEE/IEC)

'F863/'F864

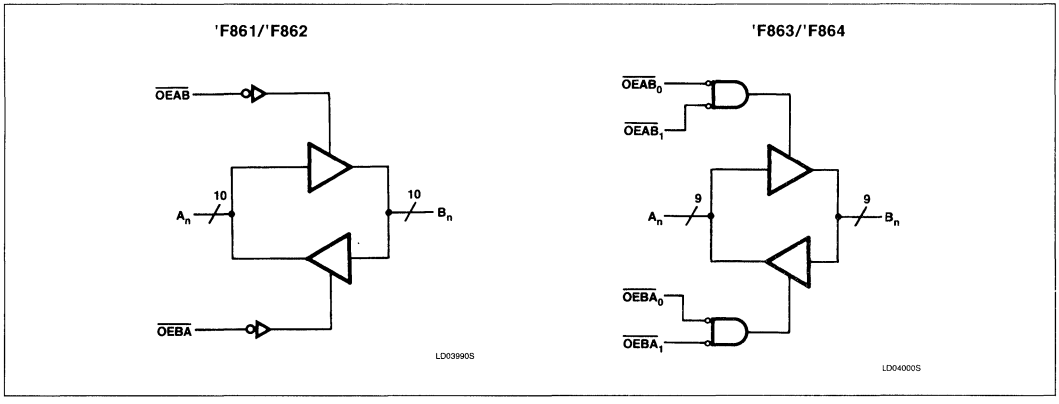


FUNCTION TABLE FOR 'F861 AND 'F862

INPUTS		MODE OF OPERATION	
$\overline{OEAB}$	$\overline{OEBA}$	'F861	'F862
L	H	A data to B bus	A data to $\overline{B}$ bus
H	L	B bus to A data	B bus to $\overline{A}$ data
H	H	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance state

LOGIC DIAGRAM



FUNCTION TABLE FOR 'F863 AND 'F864

INPUTS				MODE OF OPERATION	
$OEAB_0$	$OEAB_1$	$OEBA_0$	$OEBA_1$	'F863	'F864
L	L	H	X	A data to B bus	A data to B bus
L	L	X	H		
H	X	L	L	B bus to A data	B bus to A data
X	H	L	L		
H	H	H	H	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance state

ABSOLUTE MAXIMUM RATINGS (Operation beyong the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	96	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−3	mA
I_{OL}	LOW-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F861, 74F862 74F863, 74F864			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
V_{HYST}	Input hysteresis		V_{CC} = MIN		200			mV
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OZH}+ I_{IH}	Off-state current, HIGH-level voltage applied	A_0 – A_9	V_{CC} = MAX, V_O = 2.7V				70	μA
I_{OZL}+ I_{IL}	Off-state current, LOW-level voltage applied	B_0 – B_9	V_{CC} = MAX, V_O = 0.5V				−70	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply current (total)	I_{CCL}	V_{CC} = MAX				145	mA
		I_{CCZ}					155	mA

NOTES:

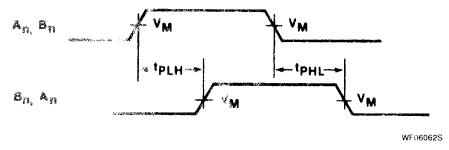
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic".)

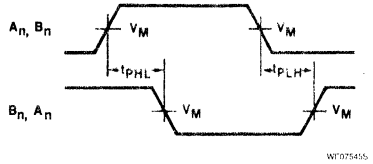
PARAMETER		TEST CONDITIONS	74F861, 74F862, 74F863, 74F864					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		4.5	5.5		10	ns
t_{PHL}	A_n to B_n or B_n to A_n			4.5	5.5		10	
t_{PLH}	Propagation delay	Waveform 2		4.0	5.0		9	ns
t_{PHL}	$\overline{A}_n$ to B_n or B_n to $\overline{A}_n$			4.0	5.0		9	
t_{PZH}	Output enable time to HIGH or LOW	Waveform 3		6.5			15	ns
t_{PZL}	level $\overline{OEBA}_n$ to A_n, $\overline{OEAB}_n$ to B_n	Waveform 4		9.5			15	
t_{PHZ}	Output enable time from HIGH or LOW	Waveform 3		11.2			18.5	ns
t_{PLZ}	level $\overline{OEBA}_n$ to A_n, $\overline{OEAB}_n$ to B_n	Waveform 4		4.2			18.5	

NOTE:
Subtract 0.2ns from minimum values for SO package.

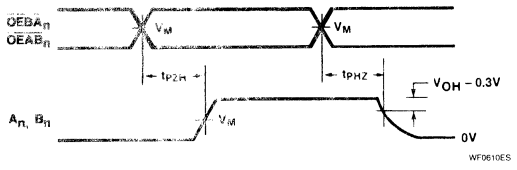
AC WAVEFORMS



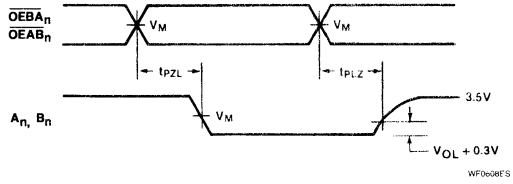
Waveform 1. Propagation Delay For Non-Inverting Outputs



Waveform 2. Propagation Delay For Inverting Outputs



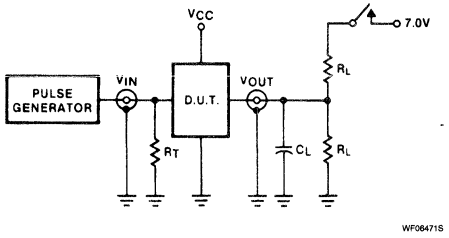
Waveform 4. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



Waveform 5. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

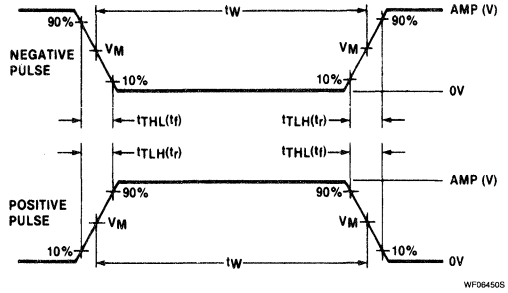
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F881
Arithmetic Logic Unit/Function Generator

Preliminary Specification

Logic Products

FEATURES

- Full look-ahead carry for high-speed arithmetic operation on long words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other Arithmetic operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Provides status register check
  - Plus ten other Logic operations
- Replaces 'AS 881
- Same pinout and function as 'F181 except for $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in Logic Mode (M = H)
- Available in 300mil wide 24-pin Slim DIP package

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F881	7.3ns	43mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F881N
Plastic SOL-24	N74F881D

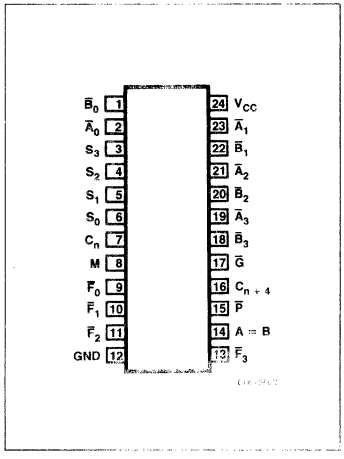
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

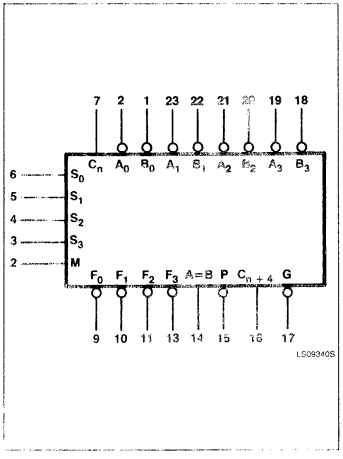
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{A}_0 - \overline{A}_3$, $\overline{B}_0 - \overline{B}_3$	Operand inputs	3.0/3.0	60μA/1.8mA
$S_0 - S_3$	Function select inputs	4.0/4.0	80μA/2.4mA
C_n	Carry input	6.0/6.0	120μA/3.6mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
A = B	Compare output	OC*/33	OC*/20mA
$\overline{F}_0 - \overline{F}_3$	Outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output	50/33	1.0mA/20mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. OC* = Open collector

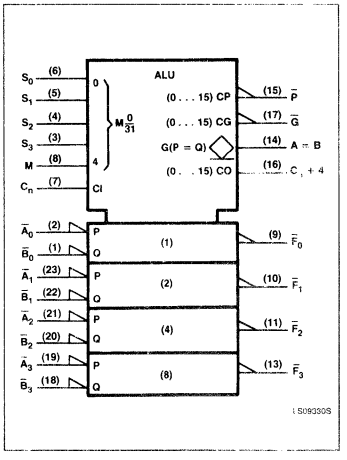
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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Arithmetic Logic Unit/Function Generator | FAST 74F881

PIN DESIGNATION TABLE

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

DESCRIPTION

The 'F881 is an arithmetic logic unit (ALU)/function generator that has a complexity of 77 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the Pin Designation Table. These operations are selected by the four function-select lines (S_0, S_1, S_2, S_3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means oftwo cascade-ouputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 'F882 full carry look-ahead circuit, high-speed arithmetic operations can be performed.

The method of cascading 'F882 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under signal designations.

If high-speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'F881 will accommodate active-high or active-low data if the pin designations are interpreted as indicated in the Pin Designation Table.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A – B – 1, which requires an end-around or forced carry to provide A – B.

The 'F881 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F_0, F_1, F_2, F_3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S_3, S_2, S_1, S_0 at L, H, H, L, respectively.

COMPARATOR TABLE

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA	ACTIVE-HIGH DATA
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

This circuit has been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S_0, S_1, S_2, S_3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the Logic Function Table and include Exclusive-OR, NAND, AND, NOR, and OR functions.

The 'F881 has the same pinout and same functionality as the 'F181 except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

In the logic mode the 'F881 provides the user with a status check on the input words, A and B, and the output word F. While in the logic mode the $\overline{P}$, $\overline{G}$ and C_{n+4} outputs supply status information based upon the following logical combinations:

$$\overline{P} = F_0 + F_1 + F_2 + F_3$$
$$\overline{G} = H$$
$$C_{n+4} = PC_n$$

The combination of signals on the S_3 through S_0 control lines determine the operation performed on the data words to generate the output bits F_i. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal or if any pair of inputs are both high (see Function Table). The 'F881 has the unique feature of providing an A = B status while the exclusive-OR (⊕) function is being utilized. When the control inputs (S_3, S_2, S_1, S_0) equal H, L, L, H; a status check is generated to determine whether all pairs (A_i, B_i) are equal in the following manner: $\overline{P} = (A_0 \oplus B_0) + (A_1 \oplus B_1) + (A_2 \oplus B_2) + (A_3 \oplus B_3)$. This unique bit-by-bit comparison of the data words which is available on the totem pole $\overline{P}$ output is particularly useful when cascading 'F881's. As the A = B condition is sensed in the first stage the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}_i$, $\overline{B}_i$) being high, it is necessary to set the control lines (S_3, S_2, S_1, S_0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}_0\overline{B}_0 + \overline{A}_1\overline{B}_1 + \overline{A}_2\overline{B}_2 + \overline{A}_3\overline{B}_3$.

SIGNAL DESIGNATIONS

In both Figures 1 and 2, the polarity indicators indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'F181 and 'F881 together with the 'F882 and 'F182 can be used with the signal designation of either Figure 1 or Figure 2.

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL

$S_0 = S_3 = H$, $S_1 = S_2 = L$, and $M = H$

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$A_0 = B_0$	$A_1 = B_1$	$A_2 = B_2$	$A_3 = B_3$	H	L	H
L	$A_0 = B_0$	$A_1 = B_1$	$A_2 = B_2$	$A_3 = B_3$	H	L	L
X	$A_0 \neq B_0$	X	X	X	H	H	L
X	X	$A_1 \neq B_1$	X	X	H	H	L
X	X	X	$A_2 \neq B_2$	X	H	H	L
X	X	X	X	$A_3 \neq B_3$	H	H	L

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH

$S_0 = S_1 = S_3 = L$, $S_2 = H$, and $M = H$

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}_0$ or $\overline{B}_0 = L$	$\overline{A}_1$ or $\overline{B}_1 = L$	$\overline{A}_2$ or $\overline{B}_2 = L$	$\overline{A}_3$ or $\overline{B}_3 = L$	H	L	
L	$\overline{A}_0$ or $\overline{B}_0 = L$	$\overline{A}_1$ or $\overline{B}_1 = L$	$\overline{A}_2$ or $\overline{B}_2 = L$	$\overline{A}_3$ or $\overline{B}_3 = L$	H	L	
X	$\overline{A}_0 = \overline{B}_0 = H$	X	X	X	H	H	L
X	X	$\overline{A}_1 = \overline{B}_1 = H$	X	X	H	H	L
X	X	X	$\overline{A}_2 = \overline{B}_2 = H$	X	H	H	L
X	X	X	X	$\overline{A}_3 = \overline{B}_3 = H$	H	H	L

SELECT TABLE FOR DATA INPUT PAIRS

S_3	S_2	S_1	S_0	M	$\overline{P} = F_0 + F_1 + F_2 + F_3$
L	H	L	L	H	$\overline{A}_0\overline{B}_0 + \overline{A}_1\overline{B}_1 + \overline{A}_2\overline{B}_2 + \overline{A}_3\overline{B}_3$
H	L	L	H	H	$(A_0 \oplus B_0) + (A_1 \oplus B_1) + (A_2 \oplus B_2) + (A_3 \oplus B_3)$

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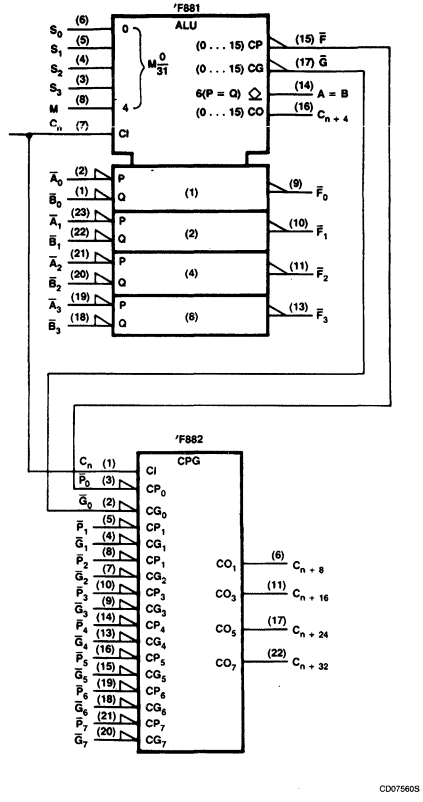


Figure 1
(Use With Table 1)

Table 1

SELECTION				ACTIVE-LOW DATA		
					M = L; Arithmetic Operations	
S_3	S_2	S_1	S_0	M = H Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{AB}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

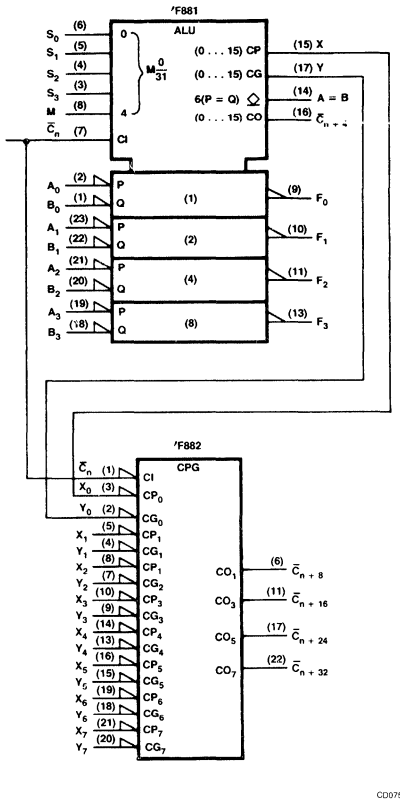


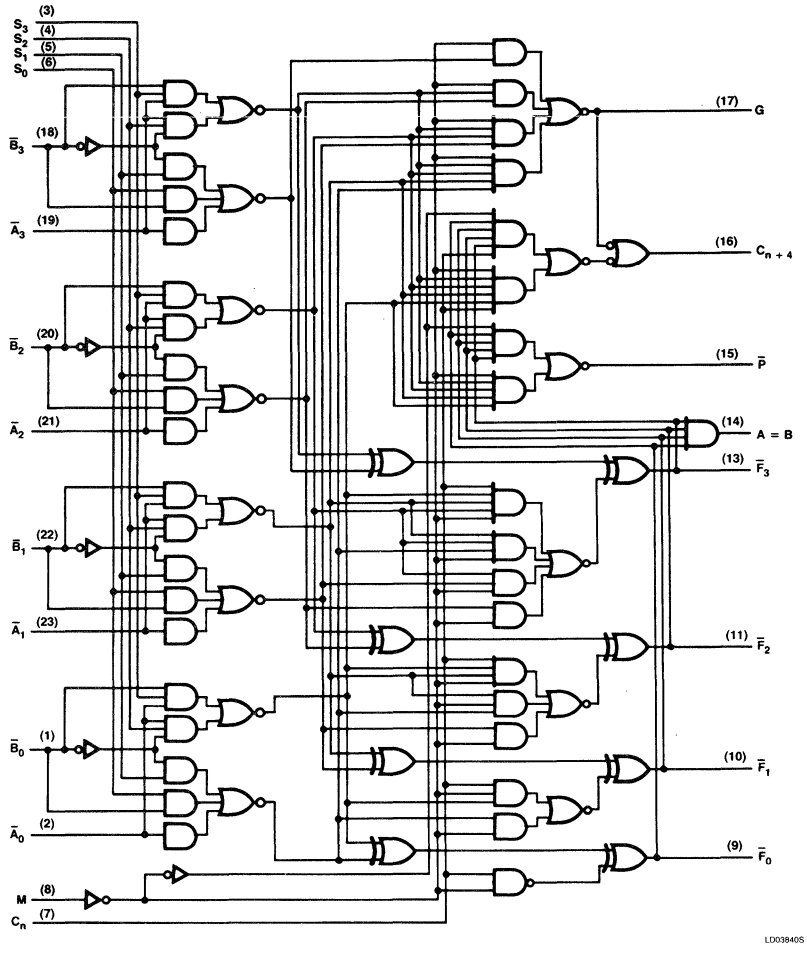
Figure 2
(Use with Table 2)

Table 2

SELECTION				ACTIVE-LOW DATA		
					M = L; Arithmetic Operations	
S_3	S_2	S_1	S_0	M – H Logic Functions	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = \overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

LOGIC DIAGRAM (POSITIVE LOGIC)



SUM MODE TEST TABLE

Function Inputs: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE

Function Inputs: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

INPUT BITS EQUAL/NOT EQUAL TEST TABLE

Function Inputs: $S_0 = S_3 = M = 4.5V$, $S_1 = S_2 = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}

INPUT PAIRS HIGH/NOT HIGH TEST TABLE

Function Inputs: $S_2 = M = 4.5V$, $S_0 = S_1 = S_3 = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaing $\overline{B}$	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in LOW output state	Any output except $\overline{G}$	40	mA
		$\overline{G}$	96	mA
T_A	Operating free-air temperature range		0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage	A = B only			4.5	V
I_{OH}	HIGH-level output current	Any output except A = B and $\overline{G}$			−1	mA
		$\overline{G}$			−3	mA
I_{OL}	LOW-level output current	Any output except $\overline{G}$			20	mA
		$\overline{G}$			48	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F881 Min	74F881 Typ[2]	74F881 Max	UNIT
V_{OH}	HIGH-level output voltage	Any output except A = B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	Any output except $\overline{G}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 20mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
		$\overline{G}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	HIGH-level input current	M	V_{CC} = MAX, V_I = 2.7V				20	μA
		A_n, B_n					60	μA
		S_n					80	μA
		C_n					120	μA
I_{IL}	LOW-level input current	M	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		A_n, B_n					−1.8	mA
		S_n					−2.4	mA
		C_n					−3.6	mA
I_{OH}	HIGH level output current	A = B only	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 4.5V				250	μA
I_{OS}	Short-circuit output current[3]	Any output except A = B and $\overline{G}$	V_{CC} = MAX		−60	−80	−150	mA
		$\overline{G}$			−150		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$S_0 - S_3$ = M = $\overline{A}_0 - \overline{A}_3$ = 4.5V, $\overline{B}_0 - \overline{B}_3$ = C_n = GND			200	mA
		I_{CCL}		$S_0 - S_3$ = M = 4.5V, $\overline{B}_0 - \overline{B}_3$ = C_n = $\overline{A}_0 - \overline{A}_3$ = GND			210	mA

NOTES:

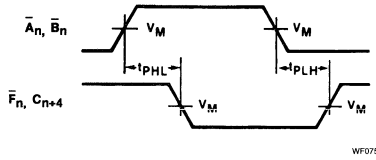
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

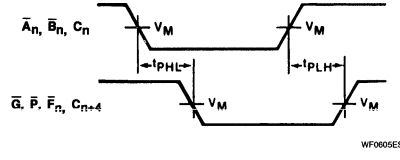
PARAMETER	TEST CONDITIONS				74F881					UNIT
	Mode	Table	Wave-form	Conditions	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
					Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay C_n to C_{n+4}					3.0 3.0	6.4 6.1	8.5 8.0	3.0 3.0	9.5 9.0	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Sum	III	1	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	5.0 5.0	10.0 9.4	13 12	5.0 5.0	14.0 13.0	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or B_n to C_{n+4}	Diff	IV	4	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	5.0 5.0	10.8 10.0	14 13	5.0 5.0	15.0 14.0	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4} (status check)	Equality $\overline{A}_i = \overline{B}_i$ or $\overline{A}_i \neq \overline{B}_i$	VI	1	$M = C_n = 4.5V$, $S_0 = S_3 = 4.5V$ $S_1 = S_2 = 0V$ $\overline{A}_i = \overline{B}_i$ or $\overline{A}_i = \overline{B}_i$	4.0 4.0	10.0 10.0	16 16	4.0 4.0	18.0 18.0	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4} (status check)	$\overline{A}_i = \overline{B}_i = H$ or $\overline{A}_i = \overline{B}_i = L$	VII	1	$M = C_n = 4.5V$, $S_2 = 4.5V$ $S_0 = S_1 = S_3 = 0V$	5.0 5.0	11.0 11.0	17 17	5.0 5.0	19.0 19.0	ns
t_{PLH} t_{PHL} Propagation delay C_n to $\overline{F}_n$		IV	2	$M = 0V$	3.0 3.0	6.7 6.5	8.5 8.5	3.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Sum	III	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	5.7 5.8	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Diff	IV	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	3.0 3.0	6.5 7.3	8.5 9.5	3.0 3.0	9.5 10.5	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Sum	III	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	5.0 5.5	7.0 7.5	3.0 3.0	8.0 8.5	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Diff	IV	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	4.0 4.0	5.8 6.5	7.5 8.5	4.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Sum	III	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	5.0 5.5	7.0 7.5	3.0 3.0	8.0 8.5	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Diff	IV	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	4.0 4.0	5.8 6.5	7.5 8.5	4.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to P_n (status checks)	Equality $\overline{A}_i = \overline{B}_i$ or $\overline{A}_i \neq \overline{B}_i$	VI	3	$M = C_n = 0V$, $S_2 = S_3 = 4.5V$	2.0 2.0	8.0 8.0	13.0 13.0	2.0 2.0	15.0 15.0	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}_n$ (status checks)	$\overline{A}_i = \overline{B}_i = H$ or $\overline{A}_i = \overline{B}_i = L$	VII	3	$M = C_n = 4.5V$ $S_2 = 4.5V$ $S_0 = S_1 = S_3 = 0V$	2.0 2.0	8.0 8.0	13.0 13.0	2.0 2.0	15.0 15.0	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	III	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	7.0 7.2	9.0 10.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Diff	IV	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	3.0 3.0	8.2 8.0	11.0 11.0	3.0 3.0	12.0 12.0	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Logic	V	3	$M = 4.5V$	4.0 4.0	6.0 6.0	9.0 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL} Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to A = B	Diff	IV	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	11.0 7.0	18.5 9.8	27.0 12.5	11.0 7.0	29.0 13.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

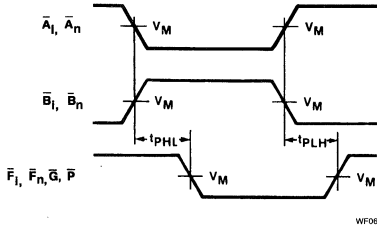
AC WAVEFORMS



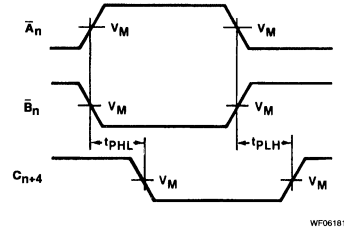
Waveform 1. Propagation Delay For Operands To Carry Output And Outputs



Waveform 2. Propagation Delays For Carry Input To Carry Output, Carry Input To Outputs, And Operands To Carry Generate And Carry Propagate Outputs



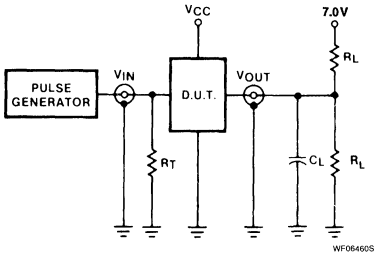
Waveform 3. Propagation Delay For Operands To Carry Generate And Propagate Outputs, Operands To A = B Output, And Outputs



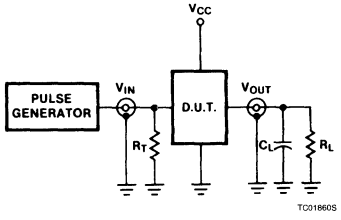
Waveform 4. Propagation Delays For Operands Carry Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUITS AND WAVEFORMS

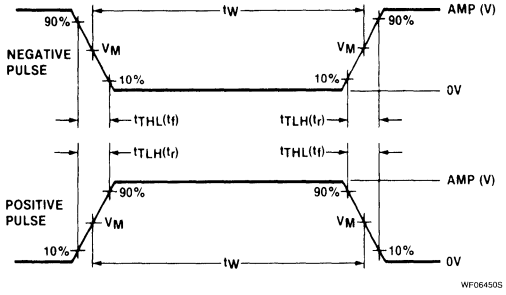


Test Circuit For Open-Collector Outputs



Test Circuit For Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F882
Look-Ahead Carry Generator

32-bit Look-Ahead Carry Generator
Preliminary Specification

Logic Products

FEATURES

- **Capable of anticipating the Carry Across a group of eight 4-bit Binary Adders**
- **Cascadable to perform Look-Ahead Across n-bit Adders**
- **Available in 300 mil wide 24 pin Slim DIP package**
- **Typical Carry Time, C_N to any C_{n+1} is less than 6_{ns}**
- **Replaces AS 882**

DESCRIPTION

The 'F882 is a high-speed carry look-ahead generator capable of anticipating the carry across a group of eight 4-bit adders permitting the designer to implement look-ahead for a 32-bit ALU with a single package or, by cascading 'F882's, full look-ahead is possible across n-bit adders.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F882	7.3ns	43mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F882N
Plastic SOL-24	N74F882D

NOTES:
1. SO package is surface-mounted micro-miniature DIP
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

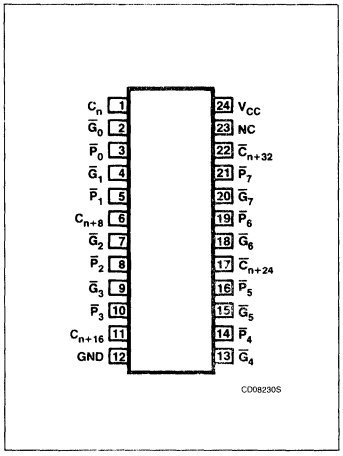
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
C_n	Carry input	5.0/1.0	100μA/0.6mA
$\overline{G}_0$, $\overline{G}_4$	Carry generate inputs	6.0/8.0	120μA/4.8mA
$\overline{G}_1$	Carry generate input	9.0/12.0	180μA/7.2mA
$\overline{G}_2$	Carry generate input	9.0/11.0	160μA/6.6mA
$\overline{G}_3$	Carry generate input	10.0/13.0	200μA/7.8mA
$\overline{G}_5$	Carry generate input	7.0/9.0	140μA/5.4mA
$\overline{G}_6$	Carry generate input	2.0/2.0	40μA/1.2mA
$\overline{G}_7$	Carry generate input	3.0/3.0	60μA/1.8mA
$\overline{P}_0$, $\overline{P}_1$	Carry propagate inputs	3.0/4.0	60μA/2.4mA
$\overline{P}_2$, $\overline{P}_3$	Carry propagate inputs	2.0/2.6	40μA/1.6mA
$\overline{P}_4$, $\overline{P}_5$, $\overline{P}_6$, $\overline{P}_7$	Carry propagate inputs	1.0/1.0	20μA/0.6mA
C_{n+8}	Carry output	50/33	1.0mA/20mA
C_{n+16}	Carry output	50/33	1.0mA/20mA
C_{n+24}	Carry output	50/33	1.0mA/20mA
C_{n+32}	Carry output	50/33	1.0mA/20mA

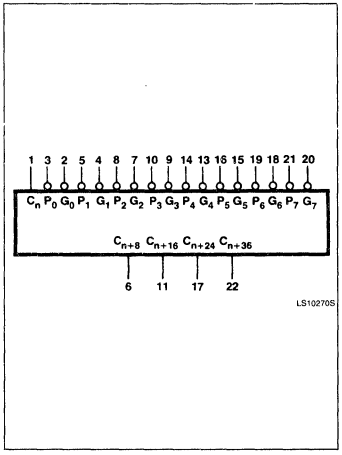
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

Look-Ahead Carry Generator | FAST 74F882

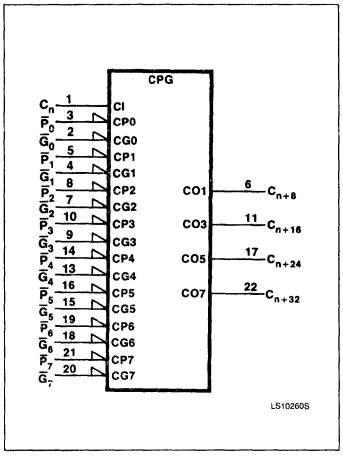
PIN CONFIGURATION



LOGIC SYMBOL

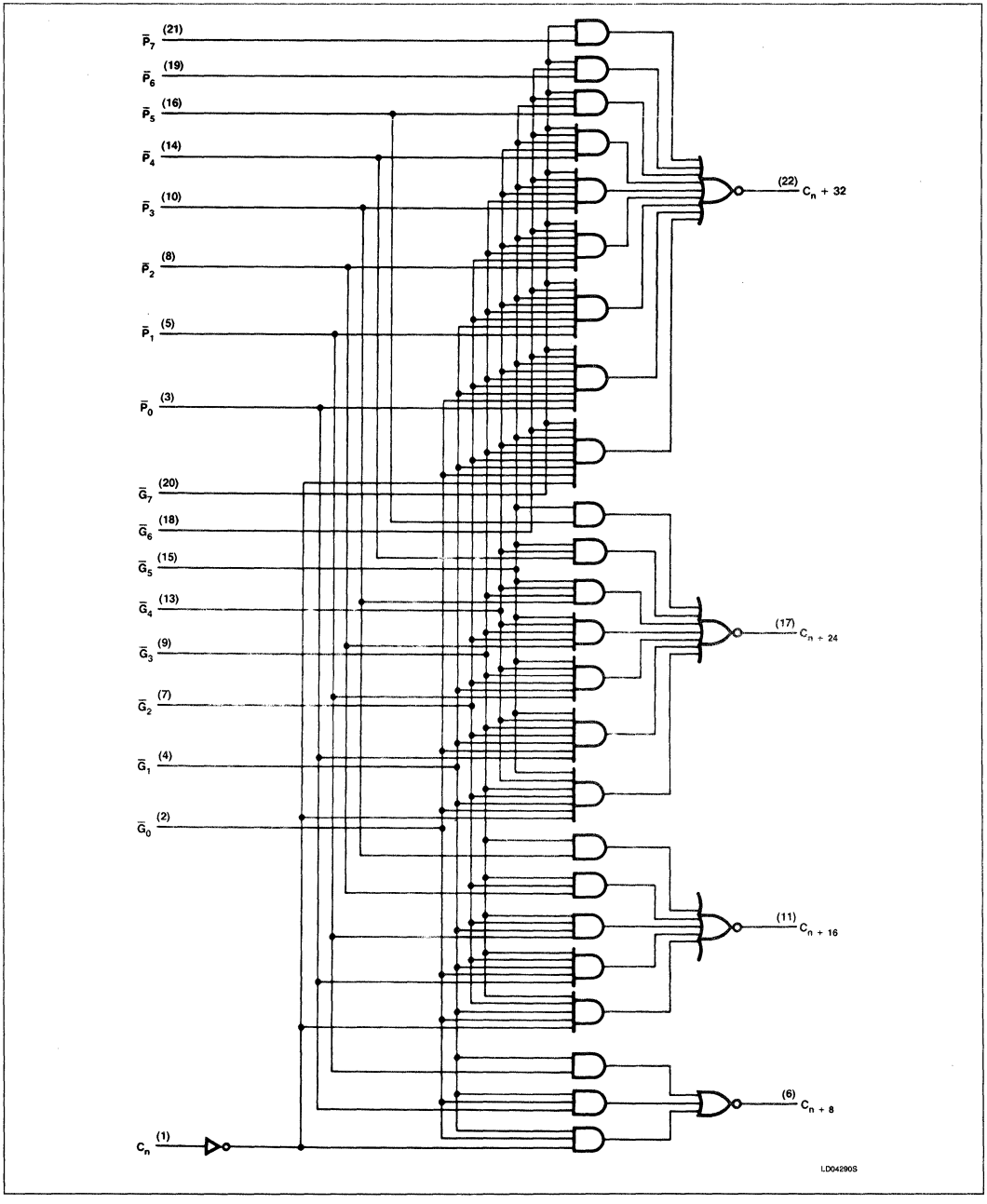


LOGIC SYMBOL (IEEE/IEC)



Look-Ahead Carry Generator FAST 74F882

LOGIC DIAGRAM



FUNCTION TABLE FOR C_{n+32} OUTPUT

INPUTS																	OUTPUT
$\overline{G}_7$	$\overline{G}_6$	$\overline{G}_5$	$\overline{G}_4$	$\overline{G}_3$	$\overline{G}_2$	$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_7$	$\overline{P}_6$	$\overline{P}_5$	$\overline{P}_4$	$\overline{P}_3$	$\overline{P}_2$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+32}
L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	L	L	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	L	L	L	L	X	X	X	X	X	H
X	X	X	X	X	L	X	X	L	L	L	L	L	X	X	X	X	H
X	X	X	X	X	X	L	X	L	L	L	L	L	L	X	X	X	H
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	H	H
All other combinations																	L

FUNCTION TABLE FOR C_{n+24} OUTPUT

INPUTS													OUTPUT
$\overline{G}_5$	$\overline{G}_4$	$\overline{G}_3$	$\overline{G}_2$	$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_5$	$\overline{P}_4$	$\overline{P}_3$	$\overline{P}_2$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+24}
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	L	L	X	X	X	X	X	H
X	X	X	L	X	X	L	L	L	X	X	X	X	H
X	X	X	X	L	X	L	L	L	L	X	X	X	H
X	X	X	X	X	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	L	L	L	L	L	L	H	H
All other combinations													L

FUNCTION TABLE FOR C_{n+16} OUTPUT

INPUTS									OUTPUT
$\overline{G}_3$	$\overline{G}_2$	$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_3$	$\overline{P}_2$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+16}
L	X	X	X	X	X	X	X	X	H
X	L	X	X	L	X	X	X	X	H
X	X	L	X	L	L	X	X	X	H
X	X	X	L	L	L	L	X	X	H
X	X	X	X	L	L	L	L	H	H
All other combinations									L

FUNCTION TABLE FOR C_{n+8} OUTPUT

INPUTS					OUTPUT
$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+8}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

Any inputs not shown in a given table are irrelevant with respect to that output.

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	40	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−1	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]		74F882 Min	74F882 Typ[2]	74F882 Max	Unit
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		.35	.5	V
				±5%V_{CC}		.35	.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	C_n	V_{CC} = MAX, V_I = 7.0V				100	µA
		$\overline{G}_0$, $\overline{G}_4$					600	
		$\overline{G}_1$					900	
		$\overline{G}_2$					600	
		$\overline{G}_3$					1000	
		$\overline{G}_5$					700	
		$\overline{G}_6$					200	
		$\overline{G}_7$					300	
		$\overline{P}_0$, $\overline{P}_1$					300	
		$\overline{P}_2$, $\overline{P}_3$					200	
		$\overline{P}_4$, $\overline{P}_5$, $\overline{P}_6$, $\overline{P}_7$					100	
I_{IH}	HIGH-level input current	C_n	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{G}_0$, $\overline{G}_4$					120	
		$\overline{G}_1$					180	
		$\overline{G}_2$					160	
		$\overline{G}_3$					200	
		$\overline{G}_5$					140	
		$\overline{G}_6$					40	
		$\overline{G}_7$					60	
		$\overline{P}_0$, $\overline{P}_1$					60	
		$\overline{P}_2$, $\overline{P}_3$					40	
		$\overline{P}_4$, $\overline{P}_5$, $\overline{P}_6$, $\overline{P}_7$					20	
I_{IL}	LOW-level input current	C_n	V_{CC} = 5.5V, V_I = 0.4V			5	−0.6	mA
		$\overline{G}_0$, $\overline{G}_4$				30	−4.8	
		$\overline{G}_1$				45	−7.2	
		$\overline{G}_2$				40	−6.6	
		$\overline{G}_3$				50	−7.8	
		$\overline{G}_5$				35	−5.4	
		$\overline{G}_6$				10	−1.2	
		$\overline{G}_7$				15	−1.8	
		$\overline{P}_0$, $\overline{P}_1$				15	−2.4	
		$\overline{P}_2$, $\overline{P}_3$				10	−1.6	
		$\overline{P}_4$, $\overline{P}_5$, $\overline{P}_6$, $\overline{P}_7$				5	−0.6	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60	−100	−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX					mA
		I_{CCL}				25	35	mA

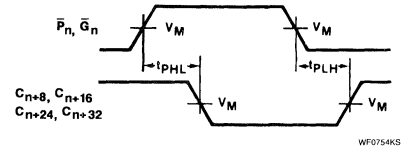
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

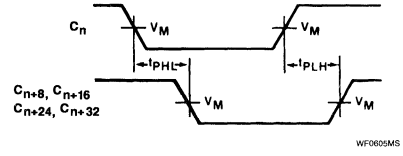
PARAMETER	TEST CONDITIONS	74F882					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} C_n to Any output	Waveform 2		6.0 6.0		4.0 4.0	14.0 14.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{P}_n$ or $\overline{G}_n$ to C_{n+8}	Waveform 1		4.0 4.0		2.0 2.0	8.0 8.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{P}_n$ to $\overline{G}_n$ to C_{n+16}	Waveform 1		6.0 6.0		2.0 2.0	8.0 8.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{P}_n$ or $\overline{G}_n$ to C_{n+24}	Waveform 1		7.0 7.0		2.0 2.0	10.0 10.0	ns
t_{PLH} Propagation delay t_{PHL} $\overline{P}_n$ or $\overline{G}_n$ to C_{n+32}	Waveform 1		10.5 10.5		2.0 2.0	12.0 12.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



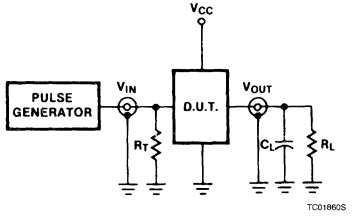
Waveform 1. Propagation Delay For Carry Propagate, Carry Generate Inputs To Carry Outputs



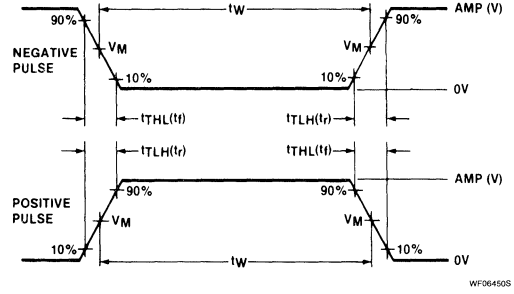
Waveform 2. Propagation Delays For Carry Input To Carry Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1240, F1241 Buffers

'F1240 Octal Inverter Buffer (3-State)
'F1241 Octal Buffer (3-State)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Low power, light bus loading**
- **Functional pin for pin equivalent of 'F240 and 'F241**
- **1/30th the bus loading of 'F240 or 'F241**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION

The 'F1240 and 'F1241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_n$, each controlling four of the 3-State outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1240	3.5ns	40mA
74F1241	4.5ns	46mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F1240N, N74F1241N
Plastic SOL-20	N74F1240D, N74F1241D

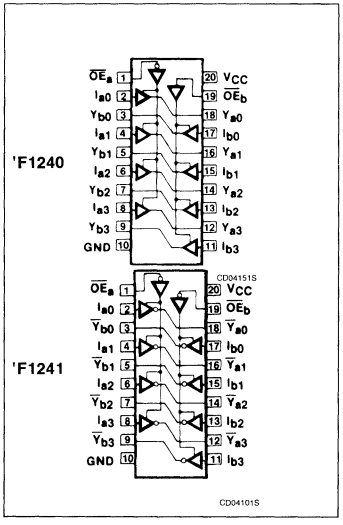
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

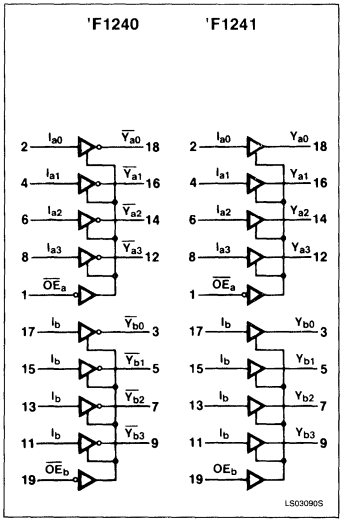
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_a$, $\overline{OE}_b$	3-State output enable input (active LOW)	1.0/0.033	20μA/20μA
OE_b	3-State output enable input (active HIGH)	1.0/0.033	20μA/20μA
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs	1.0/0.033	20μA/20μA
$\overline{Y}_{a0} - \overline{Y}_{a3}$, $\overline{Y}_{b0} - \overline{Y}_{b3}$ 'F1240	Data outputs	750/106.7	15mA/64mA
$Y_{a0} - Y_{a3}$, $Y_{b0} - Y_{b3}$ 'F1241	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

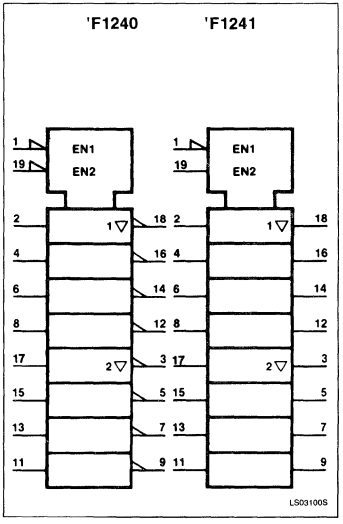
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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FUNCTION TABLE for 'F1240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_{an}$	$\overline{Y}_{bn}$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

FUNCTION TABLE for 'F1241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_{an}	Y_{bn}
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER				TEST CONDITIONS[1]			74F1240, 74F1241			UNIT
							Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = −15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
					I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current			V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current			V_{CC} = MAX, V_I = 0.5V				−1	−20	mA
I_{OZH}	Off-state output current HIGH-level voltage applied			V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				2	50	mA
I_{OZL}	Off-state output current LOW-level voltage applied			V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−2	−50	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F1240	I_{CCH}	V_{CC} = MAX				22	30	mA
			I_{CCL}					58	75	mA
			I_{CCZ}					44	58	mA
		'F1241	I_{CCH}					33	44	mA
			I_{CCL}					62	80	mA
			I_{CCZ}					45	60	mA

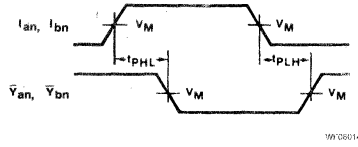
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

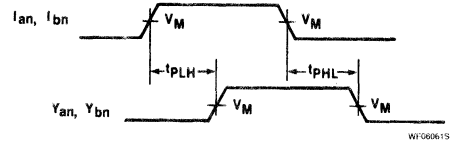
PARAMETER			TEST CONDITIONS	74F1240, 74F1241					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
'F1240	t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns
	t_{PZH} t_{PZL}	Output enable time To HIGH or LOW	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	7.5 9.0	3.0 4.0	8.0 9.5	ns
	t_{PHZ} t_{PLZ}	Output disable time From HIGH or LOW	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns
'F1241	t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2	2.5 2.5	4.0 5.0	5.5 6.5	2.5 2.5	6.0 7.0	ns
	t_{PZH} t_{PZL}	Output enable time To HIGH or LOW	Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.0 8.0	3.0 3.0	7.5 8.5	ns
	t_{PHZ} t_{PLZ}	Output disable time From HIGH or LOW	Waveform 3 Waveform 4	3.0 3.0	5.5 6.0	7.5 8.0	3.0 3.0	8.5 8.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

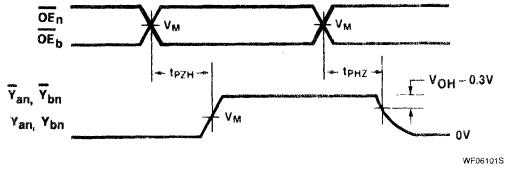
AC WAVEFORMS



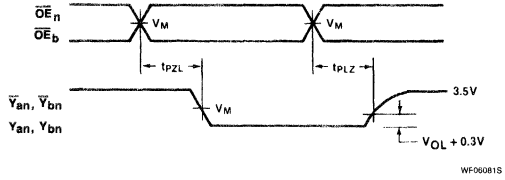
Waveform 1. Propagation Delay Data To Output For 'F1240



Waveform 2. Propagation Delay Data To Output For 'F1241



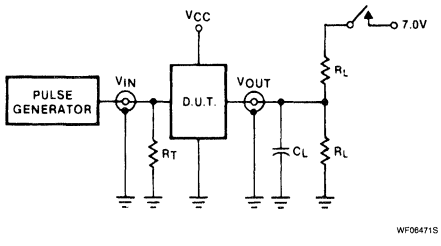
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



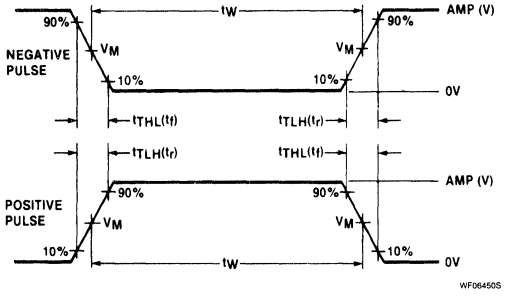
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

6

Signetics

FAST 74F1242, F1243
Transceivers

'F1242 Quad Inverting Transceiver (3-State)
'F1243 Quad Transceiver (3-State)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (70μA in HIGH and LOW states)**
- **Low power, light bus loading**
- **Functional pin for pin equivalent of 'F242 and 'F243**
- **1/30th the bus loading of 'F242 or 'F243**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **3-State outputs sink 64mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1242	3.5ns	43mA
74F1243	4.5ns	44mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F1242N, N74F1243N
Plastic SOL-20	N74F1242D, N74F1243D

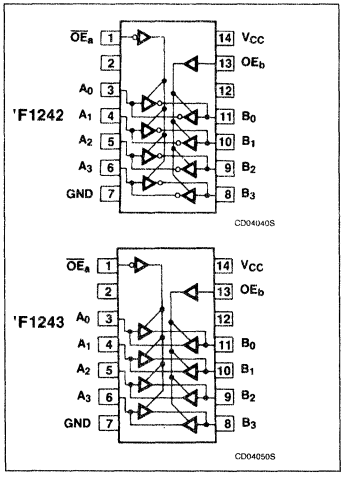
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

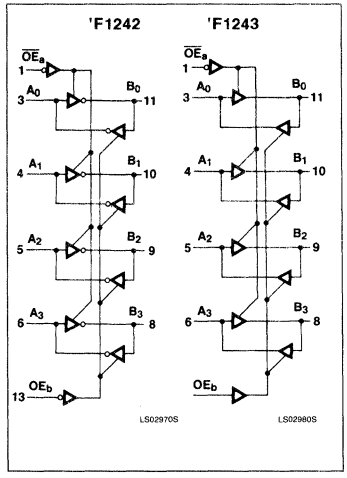
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs	3.5/0.117	70μA/70μA
$\overline{OE}_a$	3-State output enable input (active LOW)	1.0/0.033	20μA/20μA
OE_b	3-State output enable input (active HIGH)	1.0/0.033	20μA/20μA
A_n, B_n	Data outputs	750/80	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

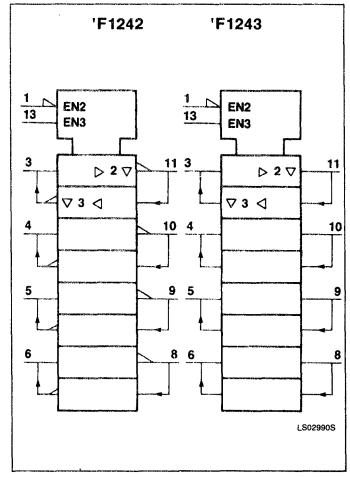
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for 'F1242

INPUTS		INPUT/OUTPUT	
$\overline{OE}_a$	OE_b	A_n	B_n
L	L	INPUT	B = A
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	A = B	INPUT

FUNCTION TABLE for 'F1243

INPUTS		INPUT/OUTPUT	
$\overline{OE}_a$	OE_b	A_n	B_n
L	L	INPUT	B = A
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	A = B	INPUT

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state
(a) = This condition is not allowed due to excessive currents.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F1242/74F1243			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$A_0 - A_3$, $B_0 - B_3$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
		$\overline{OE}_a$, OE_b	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current for $\overline{OE}_a$ and OE_b inputs only		V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current for $\overline{OE}_a$ and OE_b inputs only		V_{CC} = MAX, V_I = 0.5V				−1	−20	μA
I_{IH} + I_{OZH}	Off-state output current HIGH-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				5	70	μA
I_{IL} + I_{OZL}	Off-state output current LOW-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				−5	−70	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	'F1242	V_{CC} = MAX	I_{CCH}			35	46	mA
				I_{CCL}			50	72	mA
				I_{CCZ}			45	60	mA
		'F1243		I_{CCH}			40	50	mA
				I_{CCL}			52	65	mA
				I_{CCZ}			44	55	mA

NOTES:

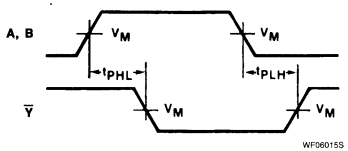
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

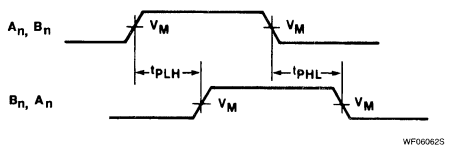
PARAMETER			TEST CONDITIONS	74F1242/74F1243					UNIT
				$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
'F1242	t_{PLH} t_{PHL}	Propagation delay data to output	Waveform 1	3.0 1.5	4.5 2.5	6.0 4.0	2.5 1.5	6.5 4.5	ns
	t_{PZH} t_{PZL}	Output enable time to HIGH or LOW	Waveform 3 Waveform 4	3.5 3.0	5.5 5.5	7.5 7.5	3.0 3.0	8.0 8.0	ns
	t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW	Waveform 3 Waveform 4	3.5 3.0	6.0 5.0	8.0 7.5	3.5 3.0	9.0 9.0	ns
'F1243	t_{PLH} t_{PHL}	Propagation delay data to output	Waveform 2	2.0 3.0	4.0 5.0	5.5 6.5	2.0 3.0	6.0 7.0	ns
	t_{PZH} t_{PZL}	Output enable time to HIGH or LOW	Waveform 3 Waveform 4	2.5 2.5	5.5 5.0	8.0 7.5	2.5 2.5	8.5 8.0	ns
	t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW	Waveform 3 Waveform 4	3.5 2.0	6.5 5.0	8.5 7.5	3.0 2.0	9.0 8.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

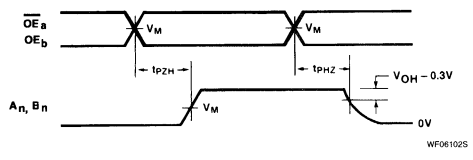
AC WAVEFORMS



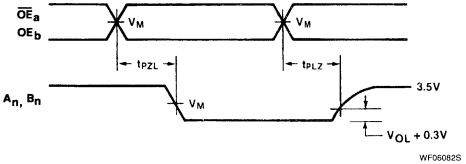
Waveform 1. Propagation Delay Data To Output For 'F1242



Waveform 2. Propagation Delay Data To Output For 'F1243



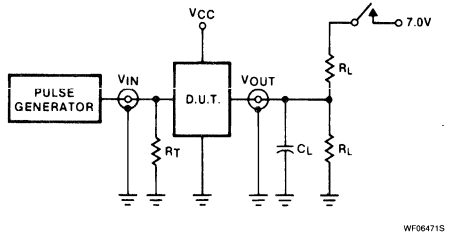
Waveform 3. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



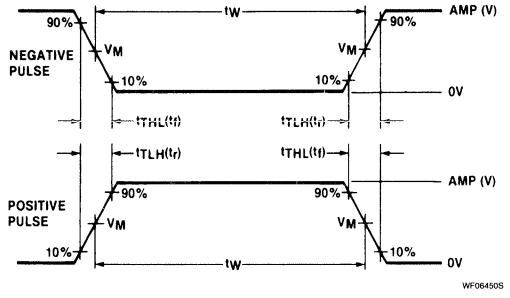
Waveform 4. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1
t_{PZH}	open
t_{PZL}	closed
t_{PHZ}	open
t_{PLZ}	closed

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

Signetics

FAST 74F1244
Buffer

Octal Buffer (3-State)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Functional pin for pin equivalent of 'F244**
- **1/30th the bus loading of 'F244**
- **Low power, light bus loading**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA and source 15mA**

DESCRIPTION

The 'F1244 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two output enables, $\overline{OE}_n$, each controlling four of the 3-State outputs. The 'F1244 is pin and functional compatible with the 'F244. The lower power and light bus loading features make it an ideal part to interface directly with MOS Microprocessors.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1244	4.5ns	43mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F1244N
Plastic SOL-20	N74F1244D

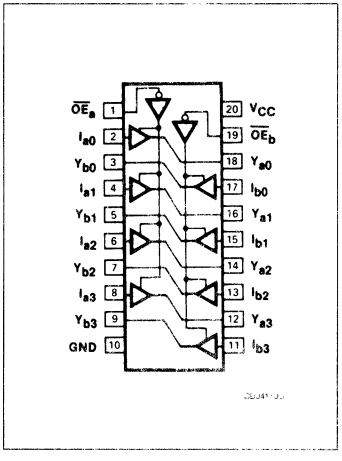
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

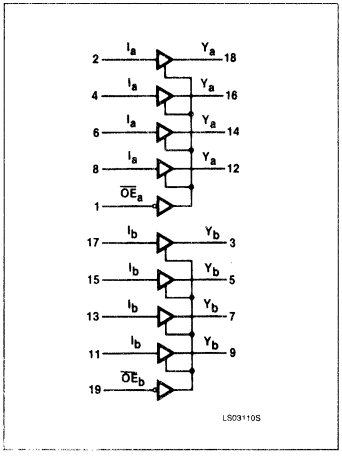
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_a$	3-State output enable input (active LOW)	1.0/0.033	20μA/20μA
$\overline{OE}_b$	3-State output enable input (active LOW)	1.0/0.033	20μA/20μA
$Y_{a0} - Y_{a3}$, $Y_{b0} - Y_{b3}$	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

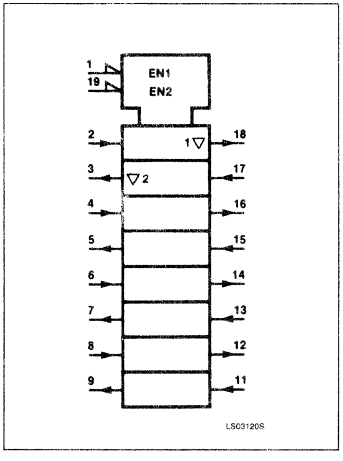
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for 'F1244

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_{an}	Y_{bn}
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z)= High impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER		74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74F1244 Min	74F1244 Typ[2]	74F1244 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH} = -15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
			I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				-1	-20	μA
I_{OZH}	Off-state output current HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				2	50	μA
I_{OZL}	Off-state output current LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V				-2	-50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-100		-255	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				57	75	mA
		I_{CCZ}				43	58	mA

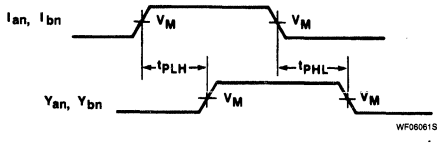
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

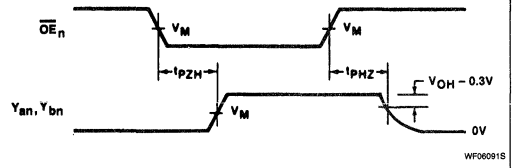
PARAMETER		TEST CONDITIONS	74F1244 T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	74F1244 T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay	Waveform 1	2.5	4.0	5.5	2.5	7.5	ns
t_{PHL}	I_{an}, I_{bn} to Y_{an}, Y_{bn}		2.0	5.0	7.0	2.0	6.0	
t_{PZH}	Output enable time	Waveform 2	3.0	6.0	7.5	3.0	8.5	ns
t_{PZL}	to HIGH or LOW	Waveform 3	3.0	6.5	8.0	3.0	8.5	
t_{PHZ}	Output disable time	Waveform 2	2.0	4.0	5.5	2.0	6.0	ns
t_{PLZ}	from HIGH or LOW	Waveform 3	2.0	4.0	5.5	2.0	6.0	

NOTE:
Subtract 0.2ns from minimum values for SO package.

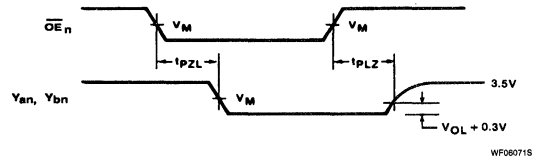
AC WAVEFORMS



Waveform 1. Propagation Delay Data To Output



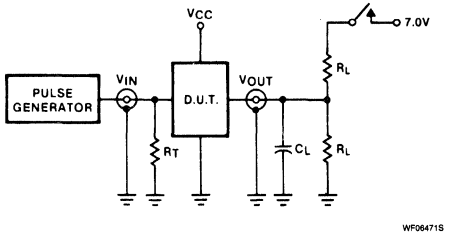
Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



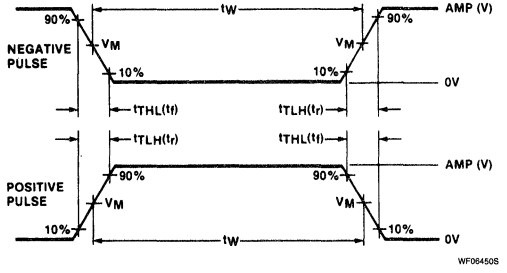
Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

Signetics

FAST 74F1245
Transceiver

Octal Transceiver (3-State)
Preliminary Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**
- **Outputs are placed in Hi-Z state during power-off conditions**

DESCRIPTION

The 'F1245 is octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The B port outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features an Ouput Enable ($\overline{OE}$) input for easy cascading and a Transmit/Receive ($T/\overline{R}$) input for direction control. The 3-State ouputs, $B_0 - B_7$, have been designed to prevent ouput bus loading if the power is removed from the device.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1245	3.8ns	100mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F1245N
Plastic SOL-20	N74F1245D

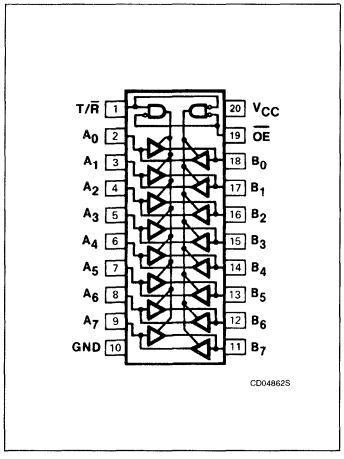
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

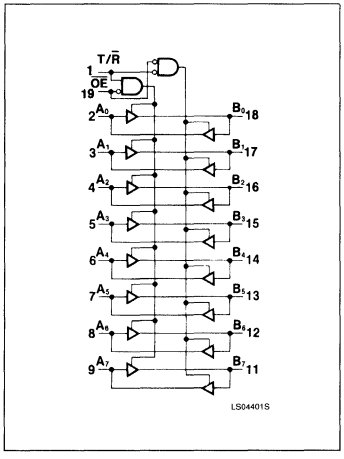
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}$	Output enable input (active LOW)	1.0/0.033	20μA/20μA
$T/\overline{R}$	Transmit/receive input	1.0/0.033	20μA/20μA
$A_0 - A_7$	3-State A data inputs	1.0/0.033	20μA/20μA
$B_0 - B_7$	3-State B data inputs	1.0/0.033	20μA/20μA
$A_0 - A_7$	3-State A data outputs	150/40	3.0mA/24mA
$B_0 - B_7$	3-State B data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

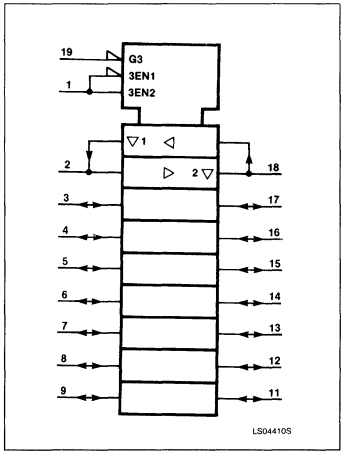
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A = B	INPUT
L	H	INPUT	B = A
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH inpedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER		74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		74F			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	LOW-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F1245			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$A_0 - A_7$, $B_0 - B_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
		$B_0 - B_7$		I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	HIGH-level input current $\overline{OE}$ and S/$\overline{R}$ only		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	LOW-level input current $\overline{OE}$ and S/$\overline{R}$ only		V_{CC} = MAX, V_I = 0.5V					−20	µA
$I_{OZH} + I_{IH}$	Off-state current HIGH-level voltage applied		V_{CC} = MAX, $\overline{OE}$ = 2.0V, V_I = 2.7V				0	70	µA
$I_{OZL} + I_{IL}$	Off-state current LOW-level voltage applied		V_{CC} = MAX, $\overline{OE}$ = 2.0V, V_I = 0.5V					−600	µA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−150	mA
		$B_0 - B_7$	V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V			85	114	mA
		I_{CCL}		V_{IN} = GND			100	125	mA
		I_{CCZ}		V_{IN} = $\overline{OE}$ = 4.5V			110	140	mA

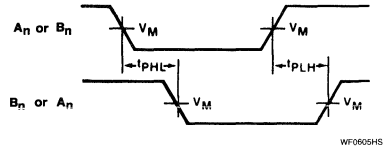
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

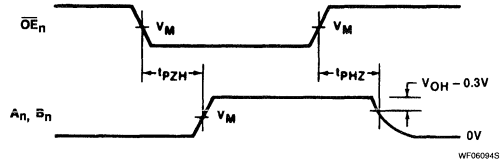
PARAMETER		TEST CONDITIONS	74F1245					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.5	3.5	5.5	2.5	6.5	
t_{PHL}	A_n to B_n or B_n to A_n		2.5	4.0	6.0	2.5	7.0	ns
t_{PZH}	Output enable time	Waveform 2	5.0	7.0	8.5	5.0	9.5	
t_{PZL}	to HIGH and LOW level	Waveform 3	3.5	6.5	8.0	3.5	9.0	ns
t_{PHZ}	Output disable time	Waveform 2	3.0	4.5	6.5	3.0	7.5	
t_{PLZ}	from HIGH and LOW level	Waveform 3	2.0	4.0	6.0	2.0	7.0	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

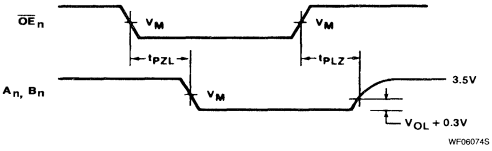
AC WAVEFORMS



Waveform 1. Propagation Delay For Input To Output



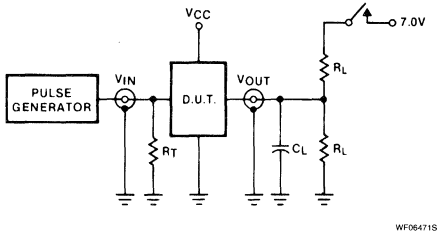
Waveform 2. 3-Sate Output Enable Time To HIGH Level And Output Disable Time From HIGH Level



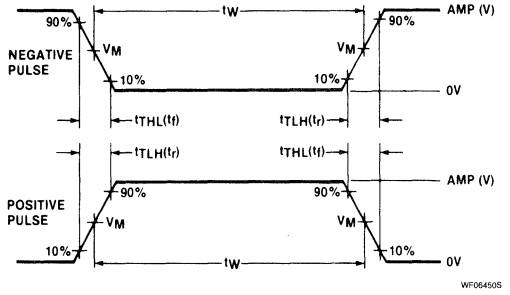
Waveform 3. 3-Sate Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

74F2952, 74F2953
Registered Transceivers

'F2952 8-Bit Registered Transceivers, Non-Inverting (3-State)
'F2953 8-Bit Registered Transceivers, Inverting (3-State)
Preliminary Specification

Logic Products

FEATURES

- **Eight Bit Registered Transceivers**
- **Two 8-Bit, back to back registers store data moving in both directions between two bidirectional busses**
- **Separate Clock, Clock Enable and 3-State Output Enable provided for each Register**
- **'F2952 Non-inverting 'F2953 Inverting**
- **AM2952/2953 functional equivalent**
- **A Outputs sinks 24mA B Outputs sinks 64mA**
- **24 pin Slim DIP package**

DESCRIPTION

The 'F2952 and 'F2953 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional busses. Data applied to the A inputs is entered and stored on the rising edge of the clock (CPAB), provided that the Clock Enable ($\overline{CEAB}$) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952	12ns	56mA
74F2953	12ns	65mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F2952N, N74F2953N
Plastic SOL-24	N74F2952D, N74F2953D

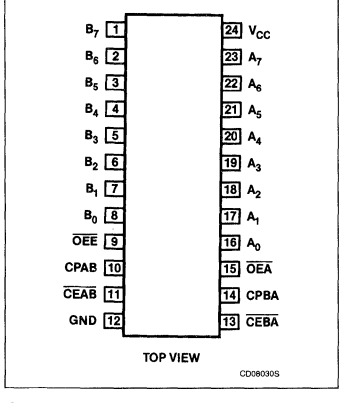
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

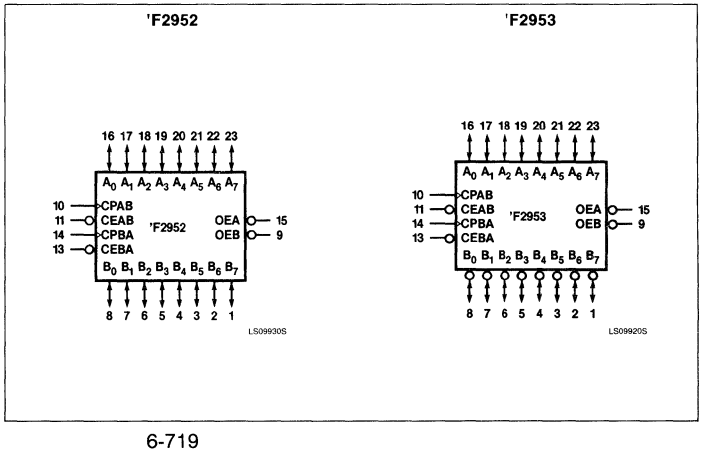
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$, $B_0 - B_7$	A and B inputs	1.0/1.0	20μA/0.6mA
CPAB, CPBA	Clock inputs	1.0/0.033	20μA/20μA
$\overline{CEAB}$, $\overline{CEBA}$	Clock enable inputs	1.0/0.033	20μA/20μA
$\overline{OEA}$, $\overline{OEB}$	Output enable inputs	1.0/0.033	20μA/20μA
$A_0 - A_7$	A Outputs	150/40	3mA/24mA
$B_0 - B_7$	B Outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



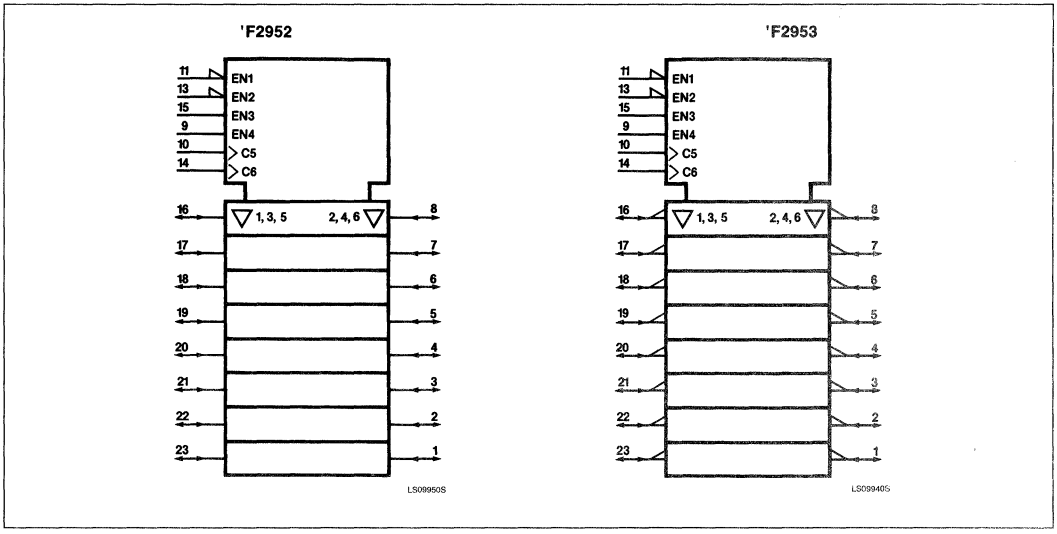
LOGIC SYMBOL



6

Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{OEB}$) is made LOW. Data flow from B inputs to A outputs proceeds in the same manner as described for A inputs to B outputs flow.

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for Register A or B

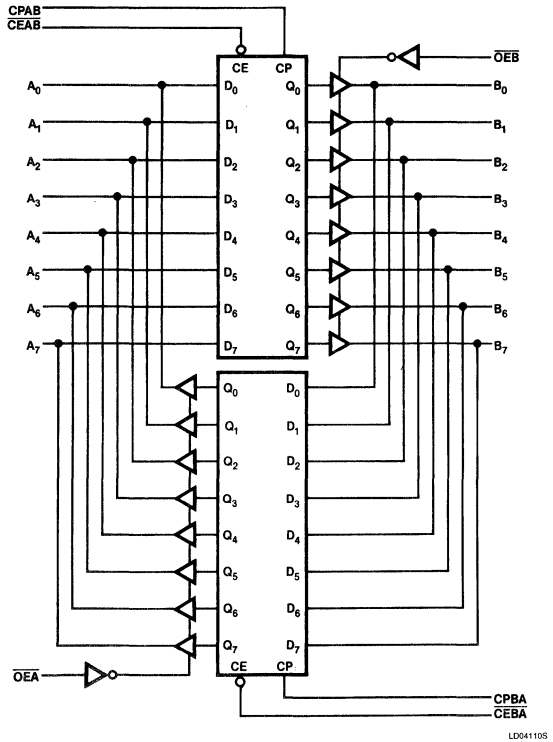
INPUTS			INTERNAL Q	OPERATING MODE
D	CP	CE		
X	X	H	NC	Hold data
L		L	L	Load data
H		L	H	

FUNCTION TABLE for Output Control

$\overline{OE}$	INTERNAL Q	A OR B OUTPUTS		OPERATING MODE
		F2952	F2953	
H	X	(Z)	(Z)	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state
= LOW-to-HIGH transition
NC = No change

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$	48	mA
		$B_0 - B_7$	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$A_0 - A_7$			−3	mA
		$B_0 - B_7$			−15	mA
I_{OL}	LOW-level output current	$A_0 - A_7$			24	mA
		$B_0 - B_7$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F2952, 74F2953			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
		$B_0 - B_7$			±5%V_{CC}	2.7	3.4		V
		$B_0 - B_7$		I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	$A_0 - A_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
		$B_0 - B_7$		I_{OL} = 48mA	±10%V_{CC}		.40	.55	V
				I_{OL} = 64mA	±5%V_{CC}		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	CPAB, CPBA, $\overline{OEAB}$, $\overline{OEBA}$, CEAB, $\overline{CEBA}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	HIGH-level input current	CPAB, CPBA, $\overline{OEAB}$, $\overline{OEBA}$, CEAB, $\overline{CEBA}$	V_{CC} = MAX, V_I = 2.7V				1	20	µA
I_{IL}	LOW-level input current	CPAB, CPBA, $\overline{OEAB}$, $\overline{OEBA}$, CEAB, $\overline{CEBA}$	V_{CC} = MAX, V_I = 0.5V				−1	−20	µA
I_{OZH} + I_{IH}	Off-state output current, HIGH-level voltage applied	A_n, B_n	V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL} + I_{IL}	Off-state output current, LOW-level voltage applied	A_n, B_n	V_{CC} = MAX, V_I = 0.5V					−70	µA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$	V_{CC} = MAX			−60		−100	mA
		$B_0 - B_7$	V_{CC} = MAX			−150		−225	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				130	190	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

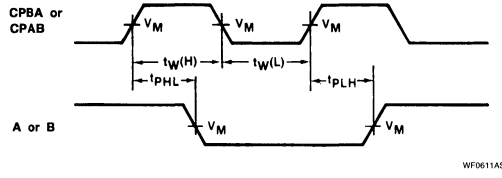
PARAMETER		TEST CONDITIONS	74F2952, 74F2953					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A_n or B_n	Waveform 1	3.0 4.0	5.5 7.0	7.5 9.0	2.5 3.5	8.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	Waveform 3 Waveform 4	2.5 3.5	5.5 7.0	7.5 9.5	2.0 3.0	8.5 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	Waveform 3 Waveform 4	3.0 2.5	6.5 5.5	9.0 7.5	2.5 2.0	10.0 8.5	ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

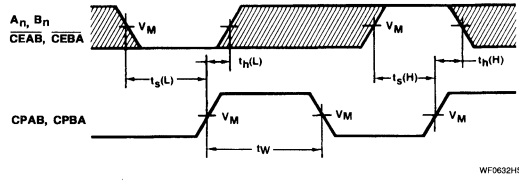
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74F2952, 74F2953					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $\pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW A_n or B_n to CPBA or CPAB	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW A_n or B_n to CPBA or CPAB	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA	Waveform 2	1.0 4.0			1.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CPAB, CPBA pulse width HIGH or LOW	Waveform 1	3.0 3.0			3.0 3.0		ns

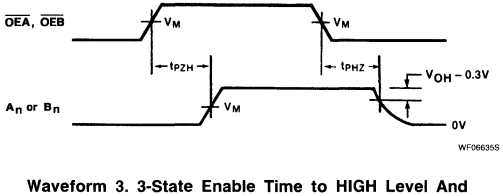
AC WAVEFORMS



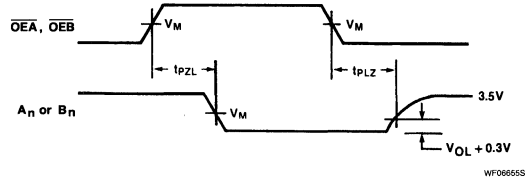
Waveform 1. Propagation Delay Clocks To Outputs And Clock Pulse Widths



Waveform 2. Data And Select Set-up And Hold Times



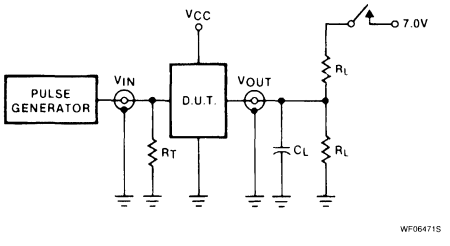
Waveform 3. 3-State Enable Time to HIGH Level And Disable Time From HIGH Level



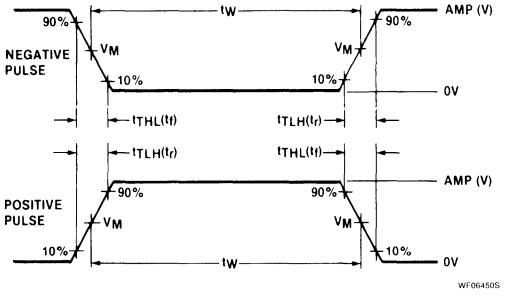
Waveform 4. 3-State Enable Time To LOW Level And Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predicatable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F3037
30Ω Line Driver

Quad 2-Input NAND 30Ω Line Driver
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3037	3.8ns	15mA

FEATURES

- **30Ω line driver**
- **160mA output drive capability in the LOW state**
- **67mA output drive capability in the HIGH state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F3037N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

DESCRIPTION

The F3037 is a high current Line driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the F3037 is 67mA source and 160mA sink with a V_{CC} as low as 4.5 volts. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

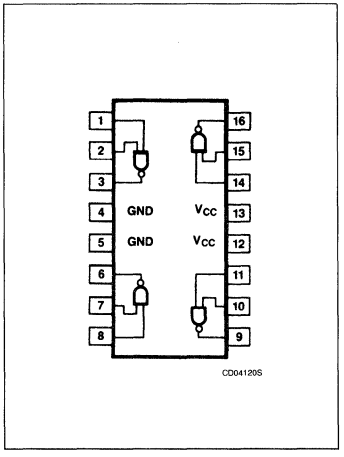
The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

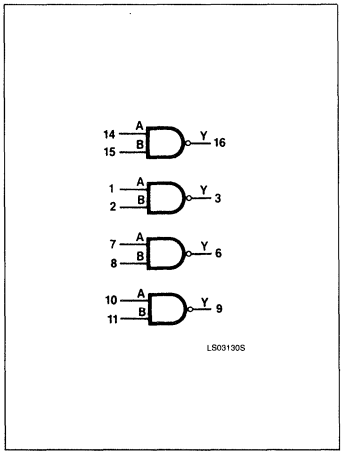
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data outputs	3350/266	67mA/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

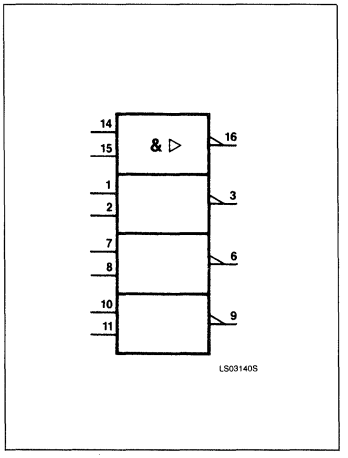
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	320	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH level input voltage	2.0			V
V_{IL}	LOW level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH level output current			−67	mA
I_{OL}	LOW level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

30Ω Line Driver | FAST 74F3037

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

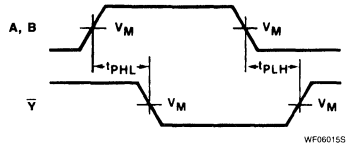
PARAMETER		TEST CONDITIONS[1]			74F3037			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −45mA	±10%V_{CC}	2.5			V
				± 5%V_{CC}	2.7	3.4		V
			I_{OH1} = −67mA[3]	±10%V_{CC}	2.0			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		.40	.55	V
			I_{OL1} = 160mA[4]	±10%V_{CC}			.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_O[5]		V_{CC} = MAX, V_O = 2.25V			−60		−160	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				3.5	6.0	mA
	Supply current (total) I_{CCL}					27	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the LOW to HIGH transition in a 30Ω transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the HIGH to LOW transition in a 30Ω transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F3037					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0 to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A, B to $\overline{Y}$	Waveform 1	3.0	4.5	6.0	2.5	6.5	ns
t_{PHL}			1.5	3.0	5.0	1.5	5.5	

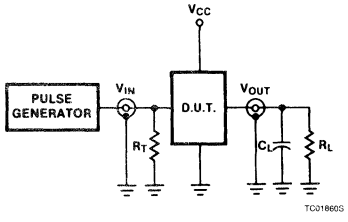
AC WAVEFORM



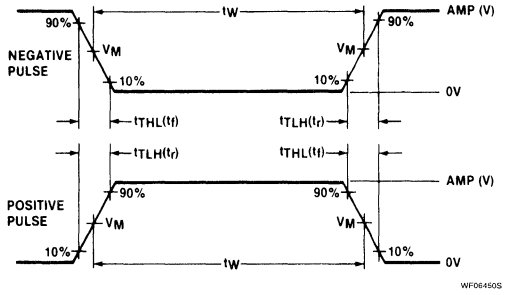
NOTE: V_M = 1.5V.

Waveform 1. Propagation Delay for Inputs to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

6

Signetics

FAST 74F3038
30Ω Line Driver

Quad 2-Input NAND 30Ω Line Driver (Open Collector)
Product Specification

Logic Products

FEATURES
- **30Ω line driver**
- **160mA output drive capability**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION
The F3038 is a high current Open Collector Line Driver composed of four 2-input NAND gates.

It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The F3038 can sink 160mA with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The AC specifications for the F3038 were determined using the standard Fast load for open collector parts of 50pF capacitance, a 500Ω pull-up resistor and a 500Ω pull-down (See Test Circuit).

Reducing the load resistors to 100Ω will decrease the T_{PLH} propagation delay by approximately 50% while increasing T_{PHL} only slightly. The graph of Typical Propagation Delay vs Load Resistor shows a spline fit curve from four measured data points; $R_L = 30Ω$, $R_L = 100Ω$, $R_L = 300Ω$, and $R_L = 500Ω$.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	9.0ns	17mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F3038N

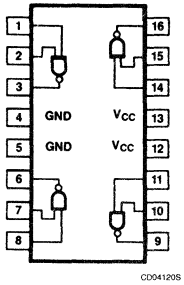
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

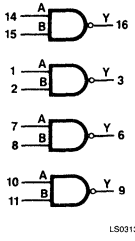
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Data inputs	1.0/1.0	20μA/0.6mA
Y	Data outputs	OC*/266	OC*/160mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. OC* = Open Collector

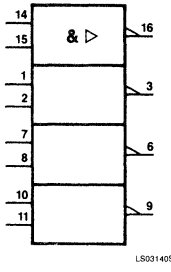
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	320	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH level input voltage	2.0			V
V_{IL}	LOW level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
V_{OH}	HIGH level output voltage			4.5	V
I_{OL}	LOW level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

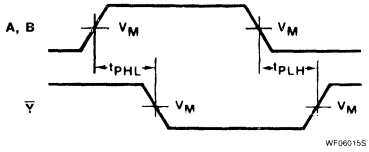
PARAMETER			TEST CONDITIONS[1]			74F3038			UNIT
						Min	Typ[2]	Max	
I_{OH}	HIGH-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}			.55	V
				I_{OL1} = 160mA[3]	±10%V_{CC}			.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND			3.5	6.0	mA
		I_{CCL}		V_{IN} = 4.5V			30	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the HIGH to LOW transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F3038					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	6.0	9.5	12.0	5.5	12.5	ns
t_{PHL}	A, B to Y		1.5	3.0	5.0	1.5	5.5	

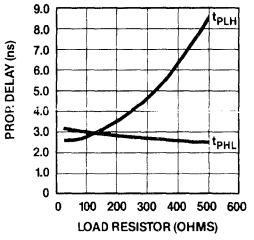
AC WAVEFORM



NOTE: For all waveforms, V_M = 1.5V.

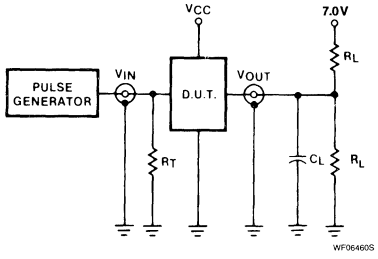
Waveform 1. Propagation Delay For Input To Output

AC CHARACTERISTICS

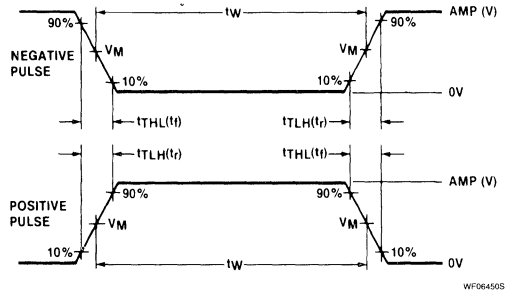


Typical Prop. Delay vs. Load Resistor

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F3040
30Ω Line Driver

Dual 4-Input NAND 30Ω Line Driver
Product Specification

Logic Products

FEATURES

- **30Ω iine driver**
- **160mA output drive capability in the LOW state**
- **67mA output drive capability in the HIGH state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION

The F3040 is a high current Line driver composed of two 2-Input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the F3040 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3040	3.7ns	7.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F3040N

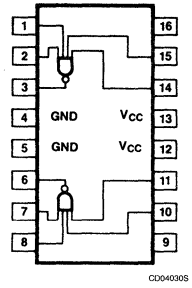
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D	Data inputs	1.0/1.0	20μA/0.6mA
Y	Data outputs	3350/266	67mA/160mA

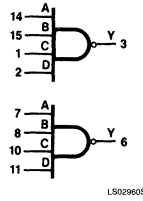
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION



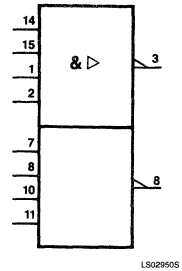
CD04030S

LOGIC SYMBOL



LS02960S

LOGIC SYMBOL (IEEE/IEC)



LS02950S

FUNCTION TABLE

INPUT				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	320	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−67	mA
I_{OL}	LOW-level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

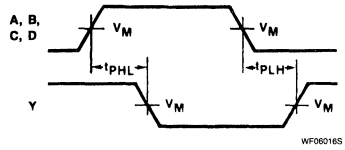
PARAMETER			TEST CONDITIONS[1]			74F3040			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −45mA	±10%V_{CC}	2.5			V
				I_{OH1} = −67mA[3]	±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		.4	.55	V
				I_{OL1} = 160mA[4]	±10%V_{CC}			.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				5	100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_O[5]			V_{CC} = MAX, V_O = 2.25V			−60		−160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				2.0	4.0	mA
		I_{CCL}					14	20	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the LOW to HIGH transition in a 30Ω transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the the HIGH to LOW transition in a 30Ω transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER		TEST CONDITIONS	74F3040					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.5	4.5	6.5	2.5	7.0	ns
t_{PHL}	A, B, C, D to Y		1.0	2.5	4.5	1.0	5.0	

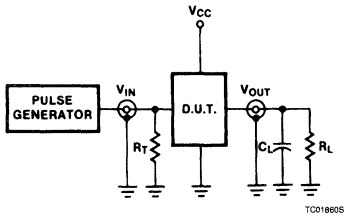
AC WAVEFORM



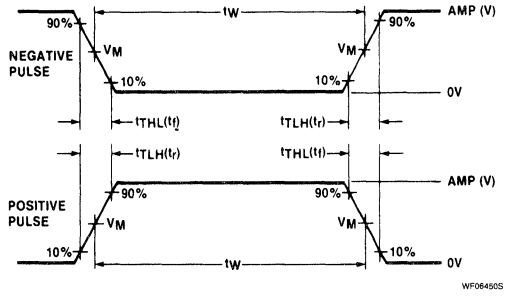
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delays for Inputs to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F30240A, 74F30244A
30Ω Line Drivers

Preliminary Specification

'F30240A Octal 30Ω Line Driver With Enable, INV (Open Collector)
'F30244A Octal 30Ω Line Driver With Enable, NINV (Open Collector)

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bus interface**
- **'F30240A Inverting 'F30244A Non-Inverting**
- **Open-Collector outputs sink 160mA**
- **160mA I_{OL} ideal for low impedance applications and transmission line effects with impedance as low as 30Ω**
- **Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)**
- **24 pin Slim DIP package**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F30240A	9.5ns	62.5mA
74F30244A	10.5ns	69mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
Plastic DIP	N74F30240AN, N74F30244AN

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

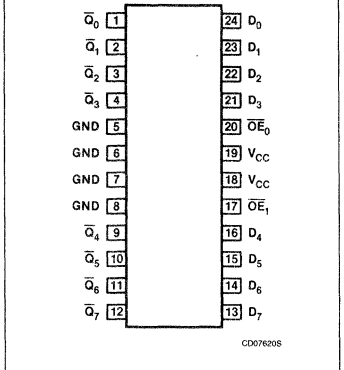
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0, \overline{OE}_1$	Output enable inputs (active LOW)	1.0/0.033	20μA/20μA
$\overline{Q}_0 - \overline{Q}_7$	Data outputs (OC*)'F30240A	OC*/266.7	OC*/160mA
$Q_0 - Q_7$	Data outputs (OC*)'F30244A	OC*/266.7	OC*/160mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. OC* = Open Collector

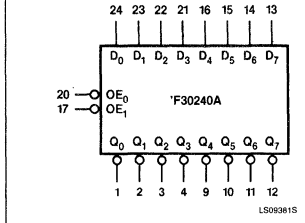
PIN CONFIGURATION

'F30240A



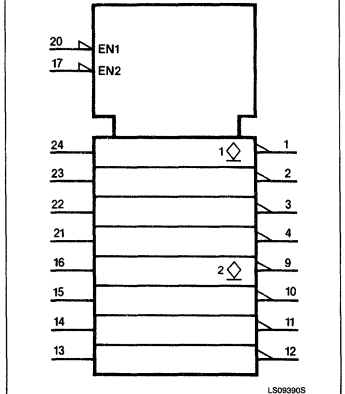
LOGIC SYMBOL

'F30240A

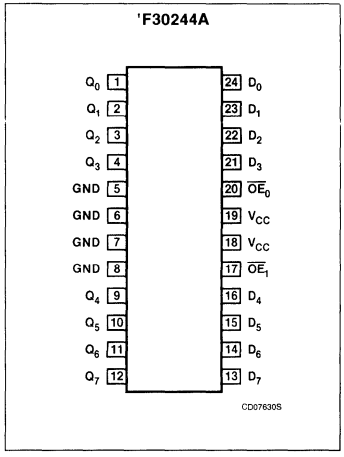


LOGIC SYMBOL (IEEE/IEC)

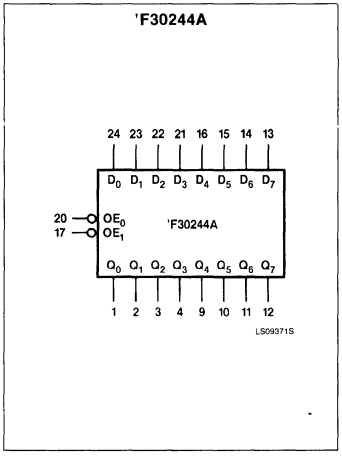
'F30240A



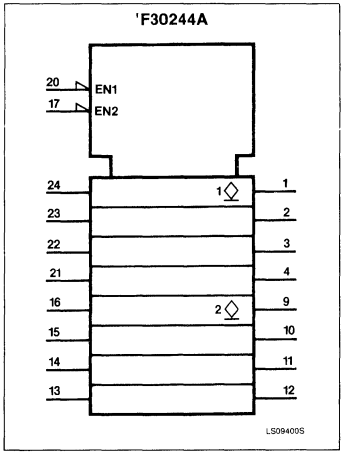
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



DESCRIPTION

The 'F30240A/'F30244A are high current Open Collector Octal Buffers composed of eight inverters.

The 'F30240A has inverting data paths and the 'F30244A has non-inverting paths. Each device has eight inverters with two Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) each controlling four outputs. Both drivers are designed to deal with the low impedance transmission line effects found on printed circuit boards when fast edge rates are used.

The 160mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

FUNCTION TABLE

INPUTS		OUTPUTS	
		'F30240A	'F30244A
$\overline{OE}_n$	D_n	$\overline{Q}_n$	Q_n
L	L	H	L
L	H	L	H
H	X	OFF	OFF

H = HIGH voltage level
L = LOW voltage level
X = Don't care

6

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	320	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
V_{OH}	HIGH-level output voltage			4.5	V
I_{OL}	LOW-level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating for free-air temperature range unless otherwise noted.)

	PARAMETER		TEST CONDITIONS[1]			74F30240A 74F30244A			Unit
						Min	Typ[2]	Max	
I_{OH}	HIGH-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	μA
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}			.55	V
				I_{OL1} = 160mA[3]	±5%V_{CC}			.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5V				−1	−20	μA
I_{CC}	Supply current (total)	'F30240A	V_{CC} = MAX				62.5		mA
		'F30244A					60		mA

NOTES:

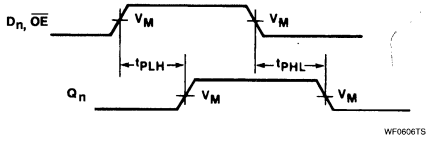
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the HIGH to LOW transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

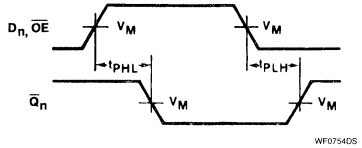
PARAMETER		TEST CONDITIONS	74F30240A, 74F30244A					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} D_n to $\overline{Q}_n$	'F30240A	Waveform 2		9.5 9.5				ns ns
t_{PLH} Propagation delay t_{PHL} D_n to Q_n	'F30244A	Waveform 1		10.5 10.5				ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{OE}$ to Q_n, $\overline{Q}_n$		Waveform 1, 2		10.0 10.0				ns ns

NOTE:
Subtract 0.2ns from minimum values for SO package.

AC WAVEFORMS



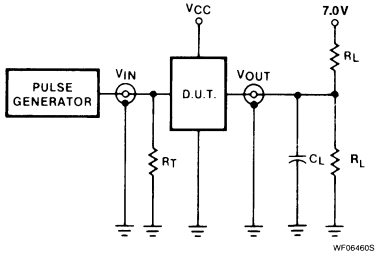
Waveform 1. Propagation Delay For Data To Output



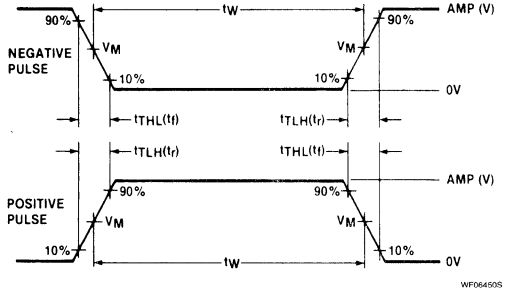
Waveform 2. Propagation Delay For Data To Output

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Logic Products

FAST 74F30245A, 74F30640A Transceivers

Preliminary Specification

'F30245A Octal Transceivers, NINV (Open Collector With Enable + 3-State)
'F30640A Octal Transceivers, INV (Open Collector With Enable + 3-State)

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)
- Ideal for applications which require high output drive and minimal bus loading
- Octal bidirectional bus interface
- 'F30245 Non-inverting 'F30640 Inverting
- Choice of outputs Open Collectors ($A_0 - A_7$) and 3-States ($B_0 - B_7$)
- Open-Collector outputs sink 160mA
- 160mA I_{OL} ideal for low impedance applications and transmission line effects with impedance as low as 30Ω.
- 3-State outputs sink 20mA
- Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- 24 pin Slim DIP package

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30245A	10.5ns	110mA
74F30640A	9.5ns	100mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F30245AN, N74F30640AN

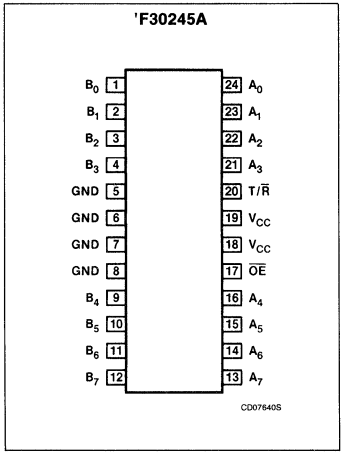
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

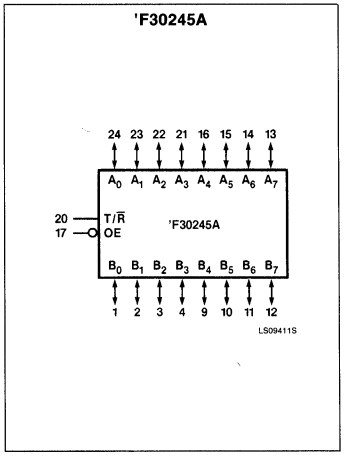
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	Data inputs	1.0/1.0	20μA/0.6mA
$B_0 - B_7$	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active LOW)	1.0/0.033	20μA/20μA
T/R	Transmit/receive input	1.0/0.033	20μA/20μA
$A_0 - A_7$	Data outputs (OC*)	OC*/266.7	OC*/16mA
$B_0 - B_7$	Data outputs (3-state)	150/40	3mA/24mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.
2. OC* = Open Collector

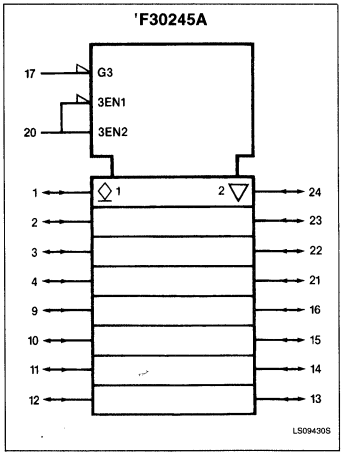
PIN CONFIGURATION



LOGIC SYMBOL

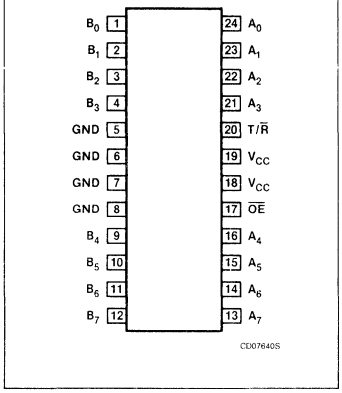


LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION

'F30640A



LOGIC SYMBOL

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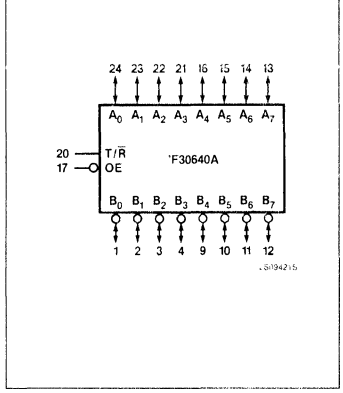
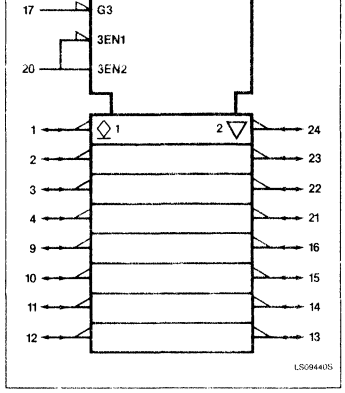


LOGIC SYMBOL (IEEE/IEC)

'F30640A



DESCRIPTION

The 'F30245/'F30640 are high current Octal Transceivers.

The 'F30245A has non-inverting data paths and the 'F30640A has inverting paths. The A outputs are open collectors with 160mA I_{OL} while the B outputs are 3-States with 20mA I_{OL}. Both transceivers are designed to deal with the low impedance transmission line effects found on printed circuit boards when fast edge rates are used.

The 160mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS			
		'F30245A		'F30604A	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n	A_n	B_n
L	L	A = B	Inputs	A = $\overline{B}$	Inputs
L	H	Inputs	B = A	Inputs	B = $\overline{A}$
H	X	Z	Z	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = HIGH impedance

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

PARAMETER			74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	$A_0 - A_7$	320	mA
		$B_0 - B_7$	48	mA
T_A	Operating free-air temperature range		0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74F30245A, 74F30640A			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage	$A_0 - A_7$			4.5	V
I_{OH}	HIGH-level output current	$B_0 - B_7$			−3	mA
I_{OL}	LOW-level output current	$A_0 - A_7$			160	mA
		$B_0 - B_7$			24	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS except for $A_0 - A_7$ (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER			TEST CONDITIONS[1]			74F30245A, 74F30640A except for $A_0 - A_7$			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	T/$\overline{R}$,$\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
		$B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	T/$\overline{R}$,$\overline{OE}$	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	T/$\overline{R}$,$\overline{OE}$	V_{CC} = MAX, V_I = 0.5V				−1	−20	μA
I_{OZH} + I_{IH}	Off-state output current, HIGH-level voltage applied	$B_0 - B_7$	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					70	μA
I_{OZL} + I_{IL}	Off-state output current LOW-level voltage applied	$B_0 - B_7$	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−70	μA
I_{OS}	Short-circuit output current[3]	$B_0 - B_7$	V_{CC} = MAX			−60		−150	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

DC ELECTRICAL CHARACTERISTICS for $A_0 - A_7$ only (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74F30245A ($A_0 - A_7$) 74F30640A ($A_0 - A_7$)			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = MAX					250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}			.55	V
			I_{OL1} = 160mA[3]	±5%V_{CC}			.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				1	20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−600	μA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the HIGH to LOW transition in a 30Ω transmission line on the incident wave.

DC SUPPLY CURRENT CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

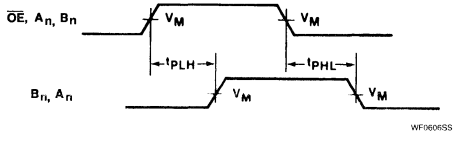
PARAMETER			TEST CONDITIONS[1]		74F30245A 74F30640A			UNIT
					Min	Typ[2]	Max	
I_{CC} Supply current (total)	'F30245	I_{CCH}	V_{CC} = MAX			95		mA
		I_{CCL}				120		mA
		I_{CCZ}				110		mA
	'F30640	I_{CCH}	V_{CC} = MAX			85		mA
		I_{CCL}				110		mA
		I_{CCZ}				100		mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

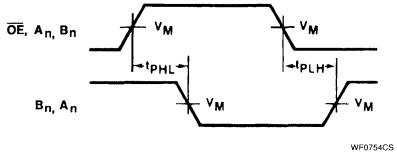
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

PARAMETER			TEST CONDITIONS	74F30245, 74F30640					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F30245A	Waveform 1						ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F30640A	Waveform 1						ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	A_n Outputs	Waveform 1, 2		10.0 10.0				ns
t_{PZH} t_{PZL}	Output enable time from HIGH or LOW	B_n Outputs	Waveform 3 Waveform 4						ns
t_{PHZ} t_{PLZ}	Output disable time to HIGH or LOW	B_n Outputs	Waveform 3 Waveform 4						ns

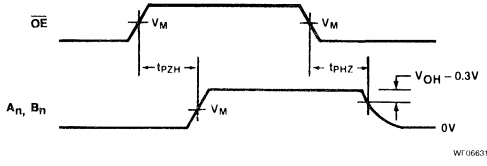
AC WAVEFORMS



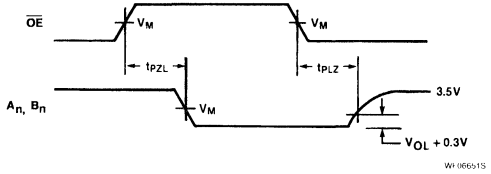
Waveform 1. Propagation Delay For Data To Output



Waveform 2. Propagation Delay For Data To Output



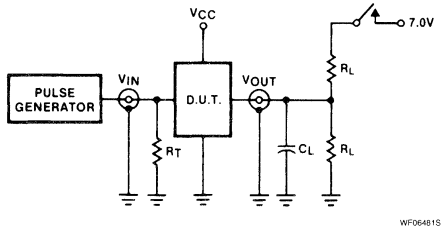
Waveform 3. 3-State Enable Time To HIGH Level And Disable Time From HIGH Level



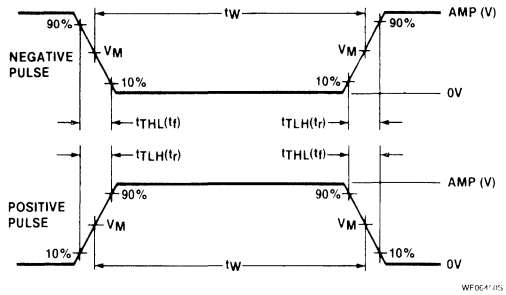
Waveform 4. 3-State Enable Time To LOW Level And Disable Time From LOW Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State And Open Collector (OC) Outputs



V_M = 1.5V

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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Signetics

Logic Products

Section 7
FAST Application Notes

Signetics

AN202
Testing And Specifying FAST Logic

Application Note

Logic Products

INTRODUCTION

FAST™ is a second generation Schottky logic family that utilizes advanced oxide-isolation techniques to increase the speed and decrease the power dissipation beyond the levels achievable with conventional junction-isolated families. The improved performance of the family is exhibited in two ways — first, the speed and power characteristics of the devices are improved, and second, the conditions under which speed and power are specified are much tighter. For instance, LS and S TTL families offer AC limits only at a nominal +5.00V V_{CC} supply voltage and at room temperature, 25°C. By contrast, FAST guarantees improved AC performance and specifies that performance over a supply variation of +5.00V ±5% and at temperatures from 0° to 70°C. Thus the designer no longer needs to derate his propagation delays from the data sheet limits to compensate for speed degradation over the temperature range.

With every advance of this magnitude, there arise new considerations that must be kept in mind both by the system designer and the user setting up test procedures. FAST is no exception, and it is these considerations that will be addressed in this application note. This paper represents an attempt to describe the way the FAST logic parts are specified, why they are spec'd in the way they are, and how the parts may be tested in the qualification lab and at incoming inspection to verify their performance.

THE FAST DATA SHEET PHILOSOPHY

Signetics FAST data sheets have been configured with an eye to quick useability . . . they are self contained and should require no reference to other sections for information. The typical propagation delays listed at the top of the page are the average between t_{PLH} and t_{PHL} for the most significant data path through the part. In the case of clocked products, this is sometimes the max frequency of operation, but in any event this number is a 5.00V - 25°C typical specification. The I_{CC} typical current shown in that same specification block is the average current (in the case of a gate, this will be the average of the I_{CCH} and I_{CCL} currents) at room temperature and V_{CC} = 5.00V. It represents the total current through the package, not the current through individual functions.

Other considerations are the Fanout And Loading tables. Some manufacturers relate these numbers in terms of 7400 gate loads . . . Signetics feels that FAST is unlikely to be mixed with other logic families and so gives the loading factors in terms of FAST unit loads. A FAST unit load is defined to be 0.6mA in the LOW state and 20μA in the HIGH state. Thus in the case of the 74F00 gate, the inputs are specified as 1 Ful (FAST unit load) each . . . the outputs need a little explanation. The standard FAST output is specified with an I_{OL} sink current of 20mA and an I_{OH} of −1.0mA. Thus the fanout of this gate in the LOW state is 20mA/0.6mA or 33 FAST unit loads. In the HIGH state the fanout is 1mA/20μA or 50 FAST unit loads. In each case, the Fanout and Loading Table on the Signetics data sheets states the HIGH/LOW fanout numbers... thus the 74F00 output fanout is specified as 50/33 Ful.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it . . . there is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than −0.5V is applied to the output pin, after that voltage is removed the part will still be functional and its useful life will not have been shortened — it is difficult to imagine the meaning of the term "functionality" WHILE that voltage is applied to the output.

Input voltage and output voltage specs in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (−0.5V).

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has a dual-purpose. In one sense, it sets some environmental conditions (operating free-air temperature), and in another, it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it, not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics Tables.

Some care must be used in interpreting the numbers in this table. Signetics feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment . . . if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by the DC Electrical Characteristics table providing that there is adequate grounding and the input voltages are free from noise, otherwise a guardbanded V_{IH} and V_{IL} should be used, ie., 2.5V instead of 2.0V and .5V instead of .8V. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under

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Testing And Specifying FAST Logic AN202

the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. (This is not the case with clocked or enabled parts and poor or moderate fixturing may induce oscillations or severe ground bounce if noise is present.) But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Since these are unloaded outputs, having faster edge rates, this causes more noise. If the outputs are loaded, the 50pF per output pin can cause substantial ground bounce. Thus V_{IH} and V_{IL} should never be used in testing the functionality of any TTL part including FAST. For these types of tests input voltages of +4.5V and 0.0V should be used for the HIGH and LOW states respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" HIGHs and LOWs during functional testing is done primarily to (1) reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet and (2) deal with testing parts exhibiting fast edge rates and 50pF per outpin pin. The situation in a system on a PC board is less severe than in a noisy production environment.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during its testing operations and conducted under the conditions set forth under the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with V_{CC} = +4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, across the temperature range from 0° to 70°C, and with an output current of I_{OH} = −1.0mA. In this table, one sees the heritage of the original junction-isolated Schottky family . . . V_{OL} = 0.5V at I_{OL} = 20mA. This gives the user a guaranteed worst-case LOW state noise immunity of 0.3V. In the HIGH state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the HIGH state than in the LOW, this is a useful state of affairs. Because the impedance of an output in the HIGH state is generally much higher than in the LOW state, more noise immunity in the HIGH state is needed. This is because the noise source couples noise onto the output connection of the device — that output tries to pull the noise source down by sinking the energy to ground or to V_{CC} depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective in shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the HIGH state compensates for the higher impedance. The result is a nice balance of sink and drive current capabilities with the optimum amount of noise immunity in both states.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at the guaranteed minimum input breakdown voltage of 7.0V. Although some users consider this to be a test of the input breakdown itself, that voltage is typically over 15V. At room temperature, this leakage current should be less than 10μA. (This is not the case with NPN input designed parts.)

Short-Circuit Output Current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that spec have totally changed. Originally I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally induced malfunctions could occur after several seconds of sustained test. Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the LOW state. When the output is switched HIGH, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to its new state of V_{OH}. At the instant that the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μFd of line capacitance tied to the output, a load that is unrealistically high by several orders of magnitude.

The effect of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious, AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through that output state and may cause functional failure or damage to the structure. A test induced failure may occur if the I_{OS} test time is excessive. As long as the I_{OS} condition is very brief, typically 50ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures might occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging line capacitance. The Signetics data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground an output for too long a time causing functional failure or damage.

AC TESTING

FAST data sheets carry several types of AC information. The AC Characteristics table contains the guaranteed limits when tested under the conditions set forth under the AC Test Circuits And Waveforms. In some cases, the test conditions are further defined by the AC Set-up Conditions — this is generally the case with counters and flip-flops where set-up and hold times are involved. All of the AC Characteristics are guaranteed with 50 pF load capacitances and with the fewest number possible of outputs switching, depending upon the functionality of the device. One of the sets of limits is spec'd at 25°C and +5.00V V_{CC} — these relate closely to the standard Schottky specs which are under similar conditions but use only 15pF load capacitances. While these numbers are convenient for comparing the two families, keep in mind that using full 50pF loads with the Schottky devices would add several nanoseconds to their propagation delays. These numbers are ideal for checking out test jigs and correlating data since they do not involve temperature or supply voltage spreads. For system design, full specifications are included that include temperature and supply voltage variations — in one case the military ranges and in the other, the commercial ranges.

AC TEST JIGS AND SET-UPS

Each FAST data sheet spells out the test circuit used to check AC performance, the waveforms, measurement points, rep rate, test loads, etc. But these are only the quantifiable variables involved in this testing. There is another more complex side to the issue — test jigs and equipment set-ups.

To get an appreciation for the problems involved in testing FAST, consider these facts. The output rise and fall times on FAST outputs are very sharp. Translating these edge rates into the effective sine wave equivalents generates frequencies on the order of several hundred MHz. At these frequencies, attention to RF phenomena is required.

Because of these RF frequencies, it is necessary to have an AC test jig that has minimal modifying effect on the input and output waveforms. To do this the jig must be con-

structed properly. The following items are key in dealing with AC jig construction.

BYPASSING CAPACITORS

Signetics uses high quality capacitors that have good RF qualities to decouple the power supply lines on the test jig, right at the V_{CC} pin to the ground plane. Four capacitors with absolute minimum lead length are used. Microwave chip capacitors are recommended. (Note: In some sensitive test environments it is advisable to decouple the V_{CC}, as well as bypass. This is done by passing the V_{CC} through a wire wrapped around a ferrite core 6 – 8 times. The inductor created helps decouple the noise from V_{CC} and reduces dramatically, the tendancy for feedback oscillations through the V_{CC} and ground current loop. This is a key problem on clocked parts since the ground bounce created by the fast edge rates and high currents will effect V_{CC} and ground substantially and thereby effect internal thresholds.) These are one each, 10μFd dipped tantalum, 0.1μFd dipped tantalum or chip, .001μFd chip and 100pF chip.

GROUNDING

One of the biggest contributors to waveform degradation is improper grounding. In reference to the test jig, the grounding is best done with one or more large ground planes that are directly connected to the ground pin of the test socket. The Signetics AC Test Jigs, both DIP and SO styles, are constructed as a four layer PC board with the 2 internal layers as ground planes. Ground planes are also interdigitated between all signal lines to decrease crosstalk. There are holes drilled in these and they are plated through to connect with the internal 2 layers and the top and bottom layers. See Figure 3 to see the interdigitated ground planes on the PCB layout of the SO jig. This grounding scheme has been used with great success in 10k and 100k ECL fixturing. The board is laid out so that the characteristic impedance of the signal lines is 50Ω. This is done by using industry standard stripline techniques. The ground plane also passes down through the center of the part on the bottom side of the board and ground pin is soldered to it using copper wire to connect the pin and the ground plane. On the top side of the board, the V_{CC} plane goes through the center of the part too, and connects to the V_{CC} pin in like manner as the ground pin. See Figure 1. The bypass capacitors are attached on the bottomside to the V_{CC} pin from the ground plane, see Figure 1. As the V_{CC} is brought on board, the V_{CC} wire is wrapped around a ½ inch ferrite core, 6 – 8 times, then makes connection with the V_{CC} plane on the top side.

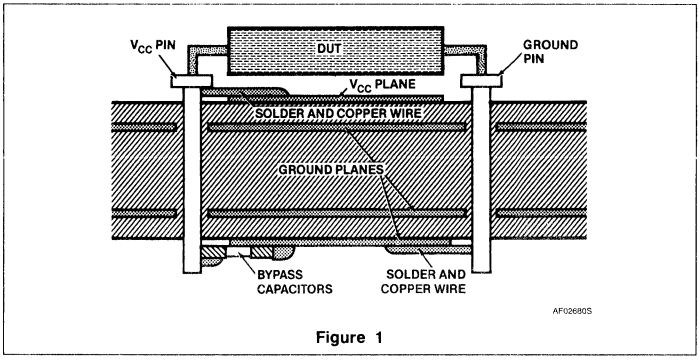


Figure 1

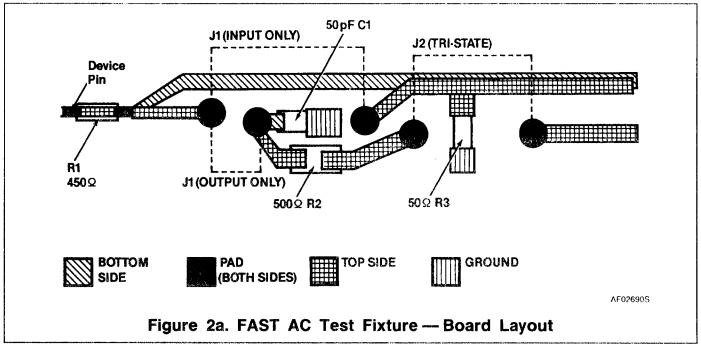


Figure 2a. FAST AC Test Fixture — Board Layout

INTERCONNECTS

The next concern is getting the input signal to the part and the output signal to the measurement system. As stated before, the Signetics jig is laid out for a 50Ω characteristic impedance. We recommend that the user maintain a 50Ω environment for the input signal as close as possible to the input pin and then terminate in 50Ω. On our jig, we terminate with a 50Ω chip resistor. The signal is brought on board through an SMB connector to the 50Ω trace on the top side of the board. The signal is terminated by the chip resistor, R3, see Figure 2a and 2b. The signal proceeds to the DUT pin, a distance of about .5 inches, through Jumper 1 (in the Input Only position), and the rest of the trace. The same pin on the opposite side of the board has a 450Ω chip resistor soldered to it. The other side of this resistor, R1, is soldered to a 50Ω trace on the bottom side of the board that runs to an SMB connector on the edge of the jig. This connects to the 50Ω input of the Sampling Oscilloscope. This 450Ω resistor in series with the 50Ω input of the scope creates a 10X divided 500Ω probe for the scope and provides impedance matching for the scope. See Figure 2b. This circuit also doubles as the resistive portion of the FAST AC Output Load and thereby allows the output to be sensed in the same fashion. When the input is not used for a signal or generator input, the line may be switched to one of three voltage sources, V_S 1 – V_S 3, by the use of a DIP switch on each pin. It may also be left open and then the 50Ω pull-down resistor that is used for an input terminator, pulls the line to ground and can be used as a hard low level. See Figure 2b. This scheme eliminates excessive cabling to each input to provide static input levels and thereby reduces parasitic inductances and crosstalk. It also eliminates the need for bulky and sometimes unreliable high impedance probes by using the 50Ω input of the Sampling Scope. With the designed-in flexibility of Jumper 1 and Jumper 2, and the selectable nature of V_{CC} and Ground pin designations, one can configure this board for any V_{CC} and Ground pin designations, select which pins are outputs or inputs and even provide the proper pull-up for 3-state outputs. This makes the board entirely universal for designated V_{CC}/Ground configurations. To explain this, the output of the device is connected to its capacitive load by Jumper 1 in the Output Only position. This means that no pin can be both output and input at the same time, but can be either. Jumper 2 allows an output to

7

be connected to the 3-state pull-up resistor, R2, and have that connected to the needed 7V. See Figure 2a and 2b. The scope is connected in the same way as the input, with the 450Ω resistor and the 50Ω of the scope comprising the 500Ω needed for the FAST load. One other consideration exists. In small part quantity testing, the elimination of a socket is very desirable, using inserted pins that are flush with the jig. In larger quantity testing, sockets may be needed, however. If this is the case, some degradation in the performance will occur due to the increased lead inductance for each pin, which is observable, and the addition of group delay through the socket may alter or affect the readings obtained.

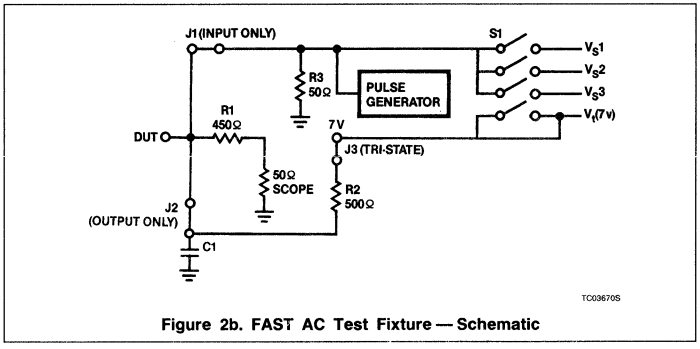


Figure 2b. FAST AC Test Fixture — Schematic

HIGH FREQUENCY DESIGN

The exact jig delay time is determined by the size of the universal jig that is being used. It is important to know that the frequency response of the jig must be high to prevent any delay factor from varying with the edge rates. The frequency response of the jig indicates how constant the impedance remains over frequency. The characteristic impedance of a transmission line is expressed as . . .

$$Z_o = \frac{V}{I} = \sqrt{\frac{L_o}{C_o}}$$

where L_o is the inductance per unit length, C_o is the capacitance per unit length, Z_o is in Ohms, L_o in Henrys, and C_o in Farads. Propagation velocity and its inverse, delay per unit length δ, are also expressed in L_o and C_o ...

$$V = \frac{1}{\sqrt{L_o\, C_o}} \qquad \delta = \sqrt{L_o\, C_o}$$

where δ is expressed in nanoseconds, L_o is in microhenrys per unit length, and C_o in microfarads per unit length. From this, it is clear that if the Z_o changes over frequency, then the delay per unit length will vary as well. Therefore, it is imperative to know how the jig responds over frequency and that all measurement line lengths are identical.

Frequency response also depends on the phase as well as the magnitude of the impedance. If the phase changes so does the delay, since delay is the derivative of phase change with frequency. An S-parameter analysis is needed in evaluating jig performance.

UNIVERSAL JIG CONSTRUCTION

Jig universality is with respect to chip pin count and V_{CC} and ground pin placements and as such, separate universal test jigs are built for 14, 16, 20, 24 and 28 pin parts.

An S-parameter analysis was performed in a network analyzer to optimize the jig layout. This assured that the jig had a flat frequency response over the spectrum of interest for FAST products. Figure 2b shows the schematic of the fixture and Figure 2a shows a drawing of the board layout, component placement and signal paths. The equipment used to analyze the jigs and loads was: HP8505A Network Analyzer, HP8503A S-Parameter Test Set, HP8501A Storage Normalizer. In some measurements the equipment was driven by an HP9845B desk-top computer.

Jigs produced in this way should have minimal lead length to reduce the characteristic inductance. This in turn minimizes reflections with their accompanying waveform distortions and measurement inaccuracies.

AC TEST LOADS FOR THE SIGNETICS UNIVERSAL JIG

As stated previously, the Network Analyzer was also used to design and optimize AC test loads to be used with the universal jig. FAST product loads require 50pF load capacitance and 500Ω resistance to ground.

Signetics meets the 50pF requirement through the use of a 45pF load, 4pF jig capacitance, and 3pF probe capacitance. The result, 52pF, is slightly more stringent than required.

A few words about load capacitors are in order. All capacitors have an associated inductance. Due to this inductance, a capacitor will form a series resonant circuit at some frequency. For single 50pF capacitors, this typically occurs between 200 and 600MHz depending on the type of capacitor. Above this resonant frequency, the capacitor has inductive characteristics and does not present a capacitive load. This is very important with FAST because harmonics due to the sharp edge transition rates occur at 600MHz and above.

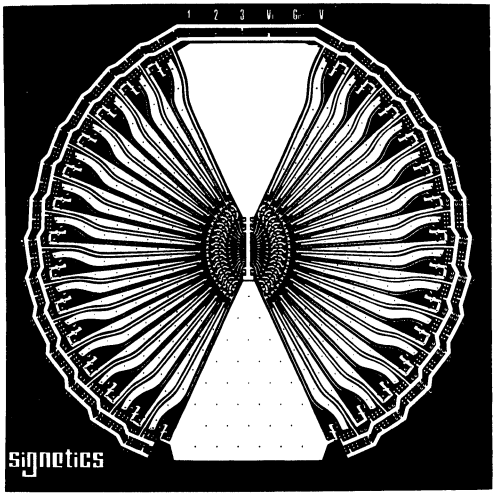
The Signetics FAST loads solve this problem by reducing the load capacitor lead inductance by paralleling three 15pF chip capacitors. The resulting load is 45pF. At the same time, since smaller value caps are used to build up the capacitive load, the associated series resonant point is above 1.2GHz.

The load resistors are 1/8W selected 510Ω ± 10Ω chip resistors.

The entire load assembly is constructed on the jig PCB along with the input termination, and the jumpers which select an input or output path. The load circuit is detailed on the FAST data sheets for 3-state parts.

CORRELATION

While numerous ATE systems are available, and are very efficient, it is imperative that the ATE correlate to a user's bench set-up. Since the Signetics FAST parts are all characterized on the set-up described in this note, it is just as important that the user bench jigs meet the same performance criteria. Without similar jigs, it will be very difficult to correlate AC data.



CD07580S

Figure 3

Signetics

AN205
Using FAST ICs For μP-To-Memory Interfaces

Application Note

Logic Products

INTRODUCTION

Most microprocessor-based systems use some form of bipolar interface between the processor and memory; only a very primitive system does not require such interface support. TTL devices in quad, hex, or octal configurations are used to meet functional and circuit-interface requirements of the system. For complex systems, the interface support may be extensive while, for simple systems, only a few devices may be required to ensure operational integrity. In a majority of system designs, one or more of the following interface requirements must be addressed.

- Buffering and Demultiplexing of Data/Address Buses
- Signal Timing and Signal Isolation
- Address Decoding
- Bank Switching
- Handling of Wait States
- Adjusting Read/ Write Data Rates
- Refreshing Dynamic RAM
- Unique Interface Requirements such as Multi-Processor Networks, Data Communication Links, etc.

Interface support is an important part of the overall design job; when implemented with the proper parts, system efficiency can be dramatically improved, higher reliability can be obtained and the design can be executed with minimum parts. This Application Note shows how common interface problems can be solved by using a minimum of high-performance bipolar devices from Signetics.

BUFFERING AND DEMULTIPLEXING

Microprocessor outputs are inherently fanout-limited; thus, some form of buffering is required to drive multiple loads such as those found on address and data buses. Extended bus configurations coupled with MOS loads tend to produce large capacitive sinks which degrade waveforms and also increase propagation delays. The use of TTL buffers provides an easy and economical way of overcoming or, at least, minimizing these harmful effects. In those systems that use shared memories and direct memory access (DMA), buffers are frequently used for isolation and as a method for switching between multiple buses. Buffers are also commonly used to optimize signal-to-noise ratios and to drive multicard bus interfaces. For the most part, buffer and latch-control functions can be summarized as follows:

- Latch the address information in systems that use multiplexed buses.
- During read operations, avoid bus contention by preventing the system from driving the multiplexed address/data bus until the address information is removed.
- Control the direction of data transceivers according to processor operation while preserving write-data and read-data hold times and avoiding bus contention when switching direction.
- Isolate the microprocessor from the system bus during DMA and multiprocessor operations.

With the use of 16-bit microprocessors, systems have become more sophisticated; likewise, buffer control and interface circuits have become somewhat more complex. Many of the 16-bit machines use multiplexed address/data buses to reduce I/O pin count; as a result, latches are required to demultiplex, hold, and buffer the address bus. Not only must the address information be latched at the correct time but the date bus must usually be buffered with bidirectional transceivers to provide the necessary drive. As previously indicated, the interface circuits must be able to avoid bus contention and, when required, to isolate the processor from the system bus.

Buffers and latch-control signals for three popular 16-bit microprocessors — the 8086, the Z8001, and the 68000 — are shown in Figure 1. For each processor, the buffer and interface functions are summarized at the bottom of the figure. Although the timing-and-control functions of the interface support circuits are fairly complex, these internal complexities are transparent to the user; only the bus connections and a few control lines are required to achieve the management goals of the system.

INTERFACE FUNCTIONS (8086 SYSTEM)

- Multiplexed address/data bus ($AD_0 - AD_{15}$)
- Three-state latches (74F373) used for demultiplexing; latches are continuously enabled by ALE until data is stable on the bus and a timing pulse is delivered by the microprocessor.
- HLDA is used to float address bus during DMA operation.
- Data bus buffered by 74F1245 or 74F245 Transceivers; data direction controlled by DT/$\overline{R}$ in minimum mode.
- Bus control and DMA isolation controlled by $\overline{DEN}$ is minimum mode.

INTERFACE FUNCTIONS (Z8001 SYSTEM)

- Address bus ($AD_0 - AD_{15}$) latched with 74F373s using $\overline{AS}$ for latch enable and $\overline{BUSAK}$ for isolation. (Note: The segmented outputs are designed to drive a Memory Management Unit with internal latches; however, in this application, the address outputs are prelatched since they are not stable for the entire cycle.)
- Data bus buffered with 74F1245s or 74F245s; $\overline{DS}$ and R/$\overline{W}$, respectively, control data direction and bus contention.
- BUSAK controls DMA isolation.

Using FAST ICs For μP-To-Memory Interfaces AN205

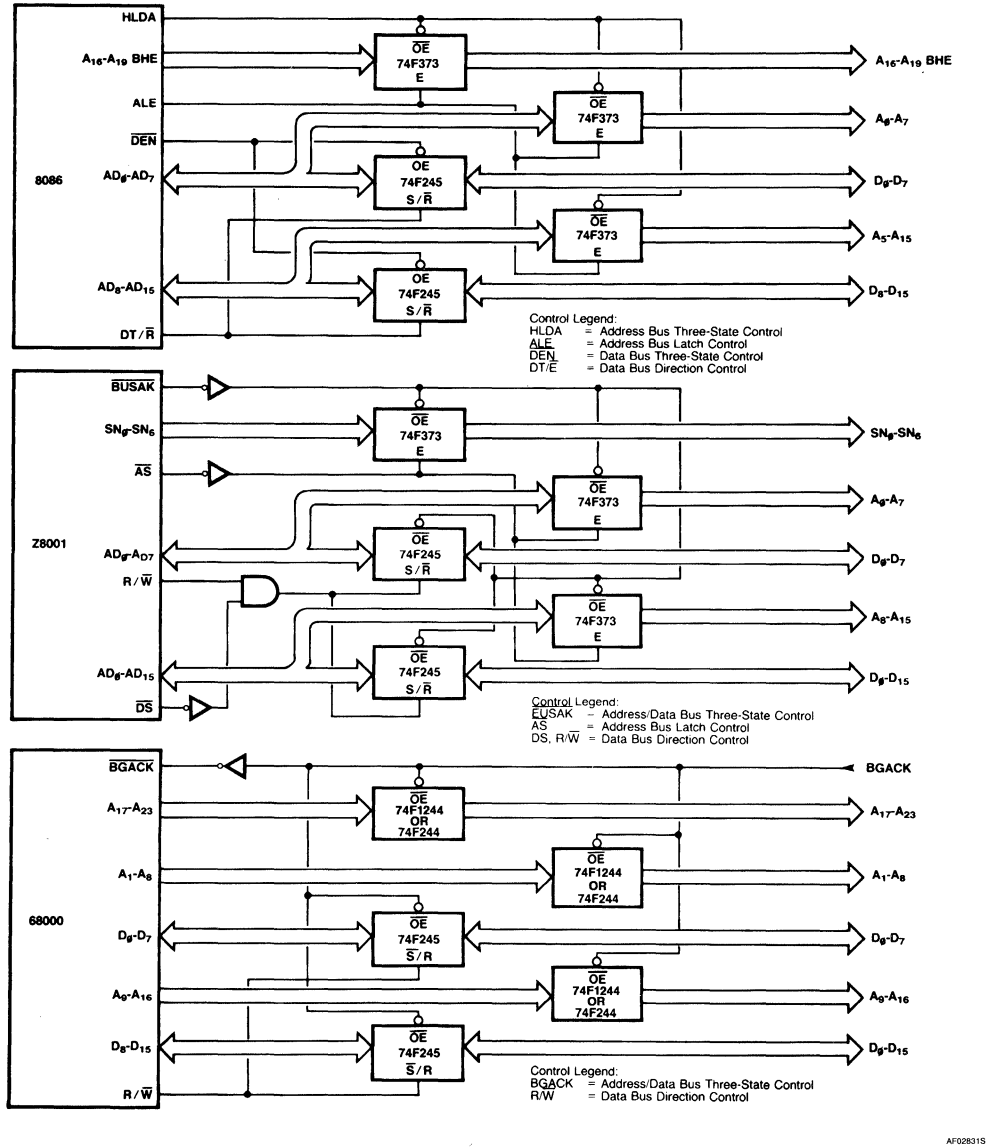


Figure 1. Examples Of Processor-to-Bus Interfaces

Using FAST ICs For μP-To-Memory Interfaces AN205

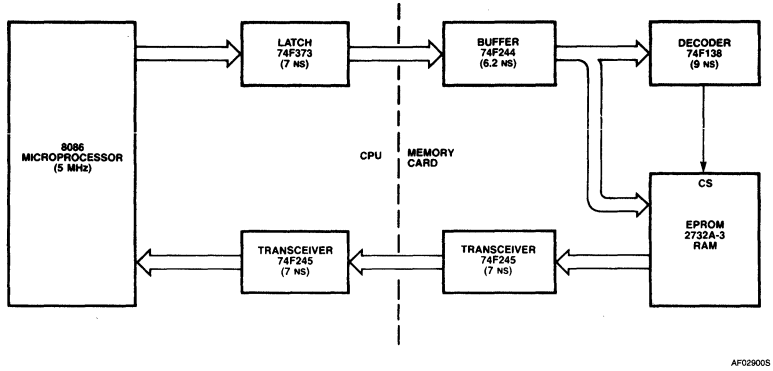


Figure 2. System Showing Typical Interface Delays

INTERFACE FUNCTIONS (68000 SYSTEM)

- Address bus buffered by 74F1244s or 74F244s and DMA isolation controlled by BGACK.
- Data bus buffered by 74F1245 or 74F245 Transceivers with R/W and BGACK, respectively, controlling data direction and bus isolation. (Note: In this configuration, a larger processor package is required since the address and data buses are separate; some advantage in speed and simplified timing areto be gained.)

Figure 2 shows the effects of buffers and an address decoder on the memory access time in a system configuration. The access time of the 8086 microprocessor is defined as the time from which a valid address appears at the input of the processor assuming that there are no wait states. Observe that each buffer and the decoding function adds a specific delay to the data-processing chain. In addition to these propagation delays, the system designer must consider capacitive loading, buffer access delays, (that is, are buffers enabled when valid data appears at input) and any other delay parameters that would extend the memory access time. (Note: The normal 8086 buffer control does not affect access time.) The delay should be calculated using maximum propagation delays over the operating temperature range of the system. Based on these considerations, the memory access time for the system shown in Figure 2 can be approximated as follows:

8086 READ CYCLE — Address Valid Output to Data Valid Input 460ns

2732 MEMORY ACCESS TIME (T_{CE})-T_{CE} = 460ns-3 (7ns) — 6.2ns-9ns = 423.8ns

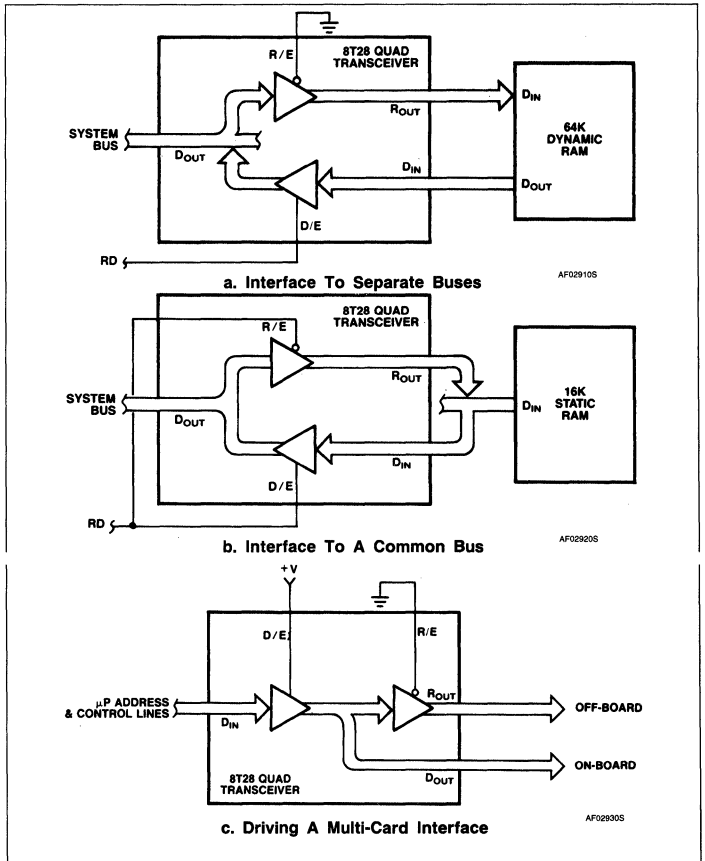


Figure 3. Using 8T28 Transceive To Obtain Optimum Interface Flexibility

Using FAST ICs For μP-To-Memory Interfaces AN205

BIDIRECTIONAL BUS INTERFACES

Virtually all microprocessor-based systems use a bidirectional bus interface between the processor and I/O peripherals; the memory interface may require separate-or-common bus connections. In either case, the 8T28 Quad Transceiver is well suited to this type of application. The 8T28 is able to drive a capacitive load of 300-picofarads without waveform degradation and the three-state outputs provide the switching speeds of TTL while offering the drive capabilities of open-collector gates. Typical bus interfaces are shown in Figure 3.

In Figure 3a, the transceiver provides a bidirectional interface between the system bus and separate input/output buses of the dynamic RAM. The D_{IN} bus is continuously driven while the D_{OUT} bus is gated onto the system bus via D/E.

Figure 3b shows a static RAM interface implemented by tying R_{OUT} and D_{IN} together. Here, the 8T28 functions as a normal bidirectional transceiver, providing buffered drive between the system bus on one hand and the memory I/O bus on the other. The bottom panel shows how the 8T28 can be used in the dual capacity of an on-board/off-board buffer/driver. To prevent signal degradation in such multi-board systems, the address/data/control buses must be buffered if off-board extensions are to be driven. Furthermore, the on-board/off-board buses should be buffer-isolated to prevent down-stream noise and/or failures from feeding back to the mother board. In Figure 3, observe that driver gates of the 8T28 are used to drive the on-board bus and receiver gates are used for the off-board bus. Low cost and minimum component count make the 8T28 ideally suited for such double-buffered applications.

MEMORY ADDRESS DECODING

In any computer system, information on the address bus must be decoded to generate select signals for memory and any I/O peripherals. There are numerous decoding schemes and a variety of implementation techniques. Generally, the methods used depend on system complexity which, in turn, depends on memory size, mapping parameters, access time, the particular technology, etc. Although simple decoders are frequently used in uncomplicated systems, the more sophisticated applications use PROMs to provide the required flexibility and to satisfy the mapping complexities that are usually encountered.

To develop trouble-free decoding circuits, the designer must be aware of those areas that can degrade system performance. For instance, caution is advised when using decoder outputs to terminate date write cycles. When read/write strobes (such as "E" on the 6801) are used to enable the address decoder, the data hold time is reduced because the trailing edge of the address decoder output now follows the trailing edge of the strobe signal to which the "hold time" is referenced. In systems that are sensitive to hold time, read and write strobes should not be used to enable address decoding circuits. Instead, the strobes should be gated with the decoder outputs to reduce the hold time.

Signetics makes a wide range of decoders, demultiplexers, and PROMs that are suitable for both simple and complex decoding functions. Some of the more common decoding applications are summarized in Figures 4 through 7.

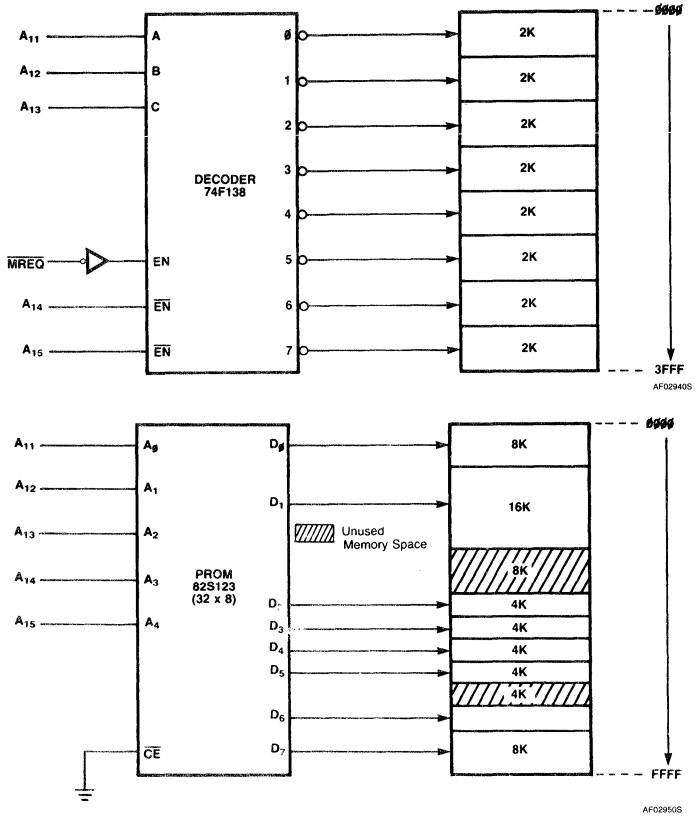
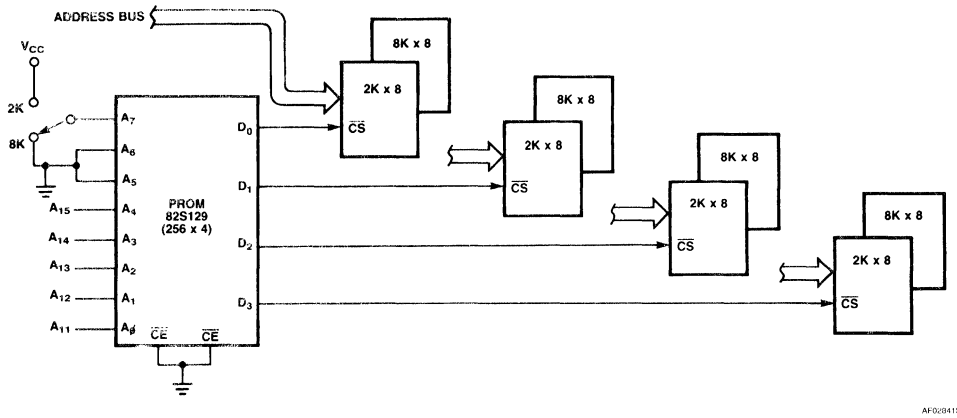


Figure 4. Two Simple Decoding Methods

OPERATION & APPLICATIONS SUMMARY

For small uncomplicated systems, the 74F138 decoder provides a cost-effective interface between the system address bus and memory. The configuration shown above is not only economical, it is fast, uses very little power, and requires no programming. Such systems are commonly used to generate contiguous memory addresses and to decode memory segments of equal size. With additional decoding circuits, the memory mapping capabilities of the system can be expanded.

Where speed is not a critical factor, the PROM decoder shown below adds considerable flexibility with no increase in chip count. The 82S123 can generate contiguous or non-contiguous address space and can be memory-mapped to satisfy the requirements of most applications. Although the PROM decoder is a bit more expensive and uses slightly more power, it has the advantage of being field programmable.



PROM PROGRAMMING

PROM ADDRESS								PROM DATA				SYSTEM ADDRESS BUS
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	D_0	D_1	D_2	D_3	
1	0	0	0	0	0	0	0	0	1	1	1	0000–07FF
1	0	0	0	0	0	0	1	1	0	1	1	0800–0FFF
1	0	0	0	0	0	1	0	1	1	0	1	1000–17FF
1	0	0	0	0	0	1	1	1	1	1	0	1800–1FFF
0	0	0	0	0	0	x	x	0	1	1	1	0000–1FFF
0	0	0	0	0	1	x	x	1	0	1	1	2000–3FFF
0	0	0	0	1	0	x	x	1	1	0	1	4000–5FFF
0	0	0	0	1	1	x	x	1	1	1	0	6000–7FFF
ALL OTHERS								1	1	1	1	

TB03000S

NOTE:
Higher density memory devices can be used to meet the requirements of the system.

Figure 5. Switch-Controlled PROM Decoder

OPERATION & APPLICATIONS SUMMARY

The switch input to this PROM decoder permits easy upgrades to higher density memory arrays (up to 64K devices) without any hardware changes. Contents of the PROM for 2K and 8K devices are as shown. In this configuration, any number of memory maps can reside in the same PROM; output port lines or switches connected to the PROM address inputs can be used to select the appropriate memory map. As previously indicated in the general discussion, read or write strobes can be used to enable the PROM; however, this delays the trailing edge of the chip selects and reduces the data hold time. For systems sensitive to hold time, it is recommended that the read/write strobes be used to drive multiple enables on the memory array or that the PROM outputs be gated.

The chief advantages for this type of decoder is simplicity, the ability to change memory mapping for memories of different densities, and the flexibility of programming address changes for the memory devices.

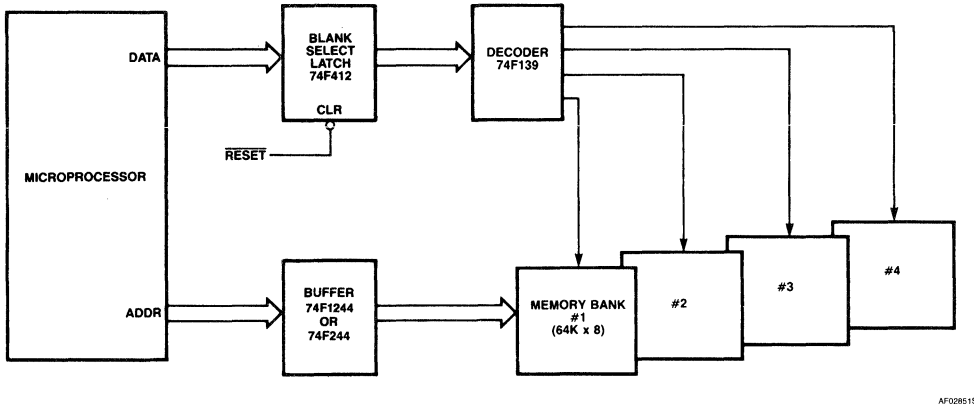


Figure 6. Extending The Logical Address Space Via Bank Switching

OPERATION & APPLICATIONS SUMMARY

In some applications, it is desirable for the system memory to extend beyond the logical address space of the processor. As shown, such a system can be easily implemented with a few interface parts and a bit of software. The four memory banks are wired in parallel; each bank can be as large as the logical memory space of the microprocessor — 512 bytes for 8-bits of address and 64K for a 16-bit address bus. An output port under software control selects the active bank; the bank address is decoded to ensure that only the appropriate memory bank is enabled. In this way, the possibility of bank contention is eliminated.

Memory allocation schemes such as these are frequently used in multiprocessor environments and, in this type of application, a copy of the operating system kernel must reside in each memory bank. The system can be enhanced by providing direct switching between the memory banks; however, additional hardware is required for such operations.

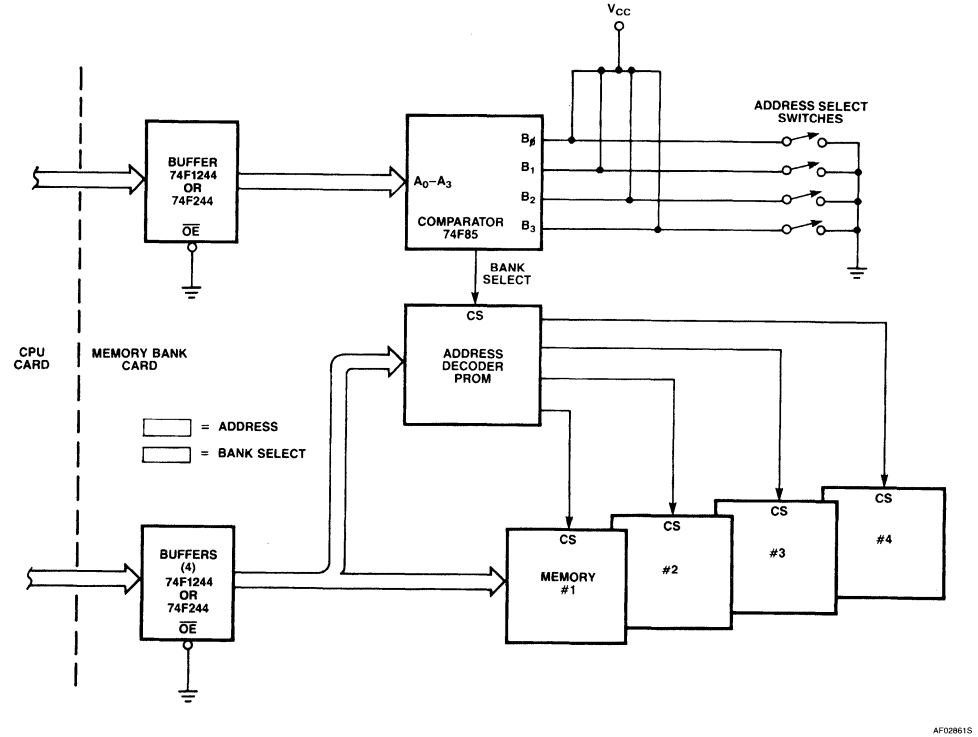


Figure 7. Multi-Board Decoding System With Extended Address Space

OPERATION & APPLICATIONS SUMMARY

In a multi-board system, the address decoding and memory-bank select functions can be implemented as shown here. The bank address on the memory card is identified by setting the address select switches of the comparator to a predetermined configuration. When the bank select signals from the CPU card match the present bank address, the PROM is enabled and the appropriate memory bank is placed on-line. Data bus control for the system is not shown.

The system show in Figure 6 and the one shown here are similar in that the four memory banks are wired in parallel and each bank can be as large as the logical address space of the microprocessor.

Using FAST ICs For μP-To-Memory Interfaces AN205

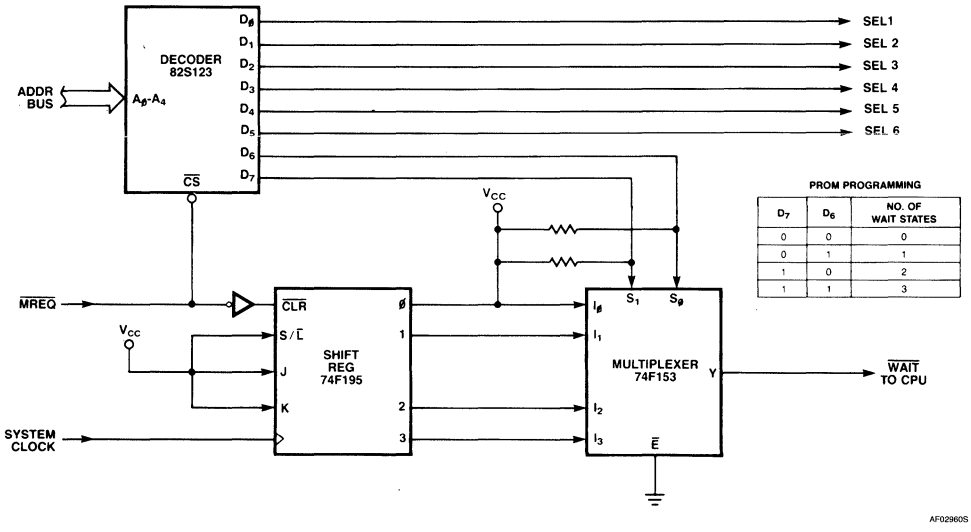


Figure 8. Programming Wait States To Optimize Data Throughput

SPECIAL MEMORY-INTERFACE CIRCUITS

In some applications, the memory interface circuits must be adapted to the unique requirements of the system. For instance, a system may use devices whose response time and wait-state requirements are vastly different, necessitating programmed wait states for optimum throughput.

Other examples include capturing a high-speed bit stream without the use of high speed (high cost) memories, refreshing dynamic RAM via interleaving, and minimizing leakage problems when driving open-collector buses. Figures 8 through 11 show how Signetics ICs can be used to solve interface problems of this type.

OPERATION & APPLICATIONS SUMMARY

Using the "slowest" device in the system as a reference for data through-put is a gross waste of processor time. ROM is usually slower than RAM, and I/O devices are generally slowest of all. One way of reducing the harmful effects of these diverse characteristics is to program wait states for each device such that inactive periods for the CPU will be minimized. With the PROM decoder in the system shown above programmed in this manner, the multiplexer selects the appropriate tap of the shift register to initiate the required number of wait states. The wait cycle is terminated when a "1" is shifted to the selected tap; the shift register is cleared at the end of each wait state cycle.

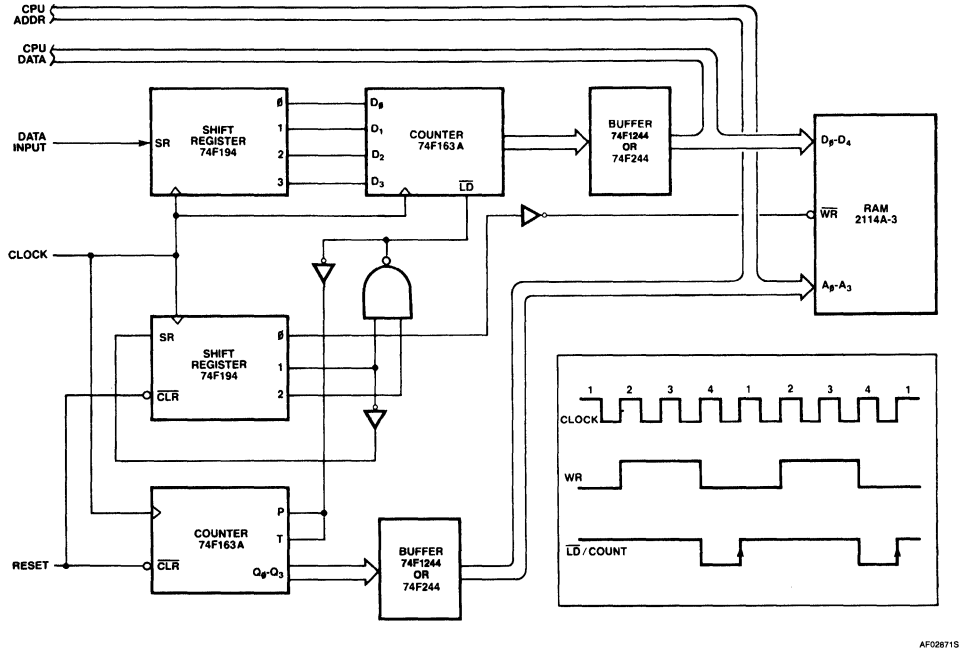


Figure 9. Storing High-Speed Serial Bit Stream With Low-Speed RAM

OPERATION & APPLICATIONS SUMMARY

In the design and use of logic analyzers, disk media, modems, and other similar equipment, a high-speed serial bit stream must be stored in memory. The above system shows how a 20MHz serial data stream can be captured and stored in a relatively low-speed RAM that has a 5MHz (200ns) cycle rate. The system uses a simple parallel to serial converter, thus, saving the cost of high-speed memory devices. Other than the synchronizing clock being supplied by the serial-input system and the setup/hold times of the shift registers being met, operation is simple and straightforward.

- Incoming serial data is clocked into shift register.
- After each fourth bit, data is transferred in parallel to a 4-bit counter (74F163) used as a latch.
- Data is written into RAM while four new bits enter shift register.
- Memory addressing is performed by incrementing the 74F163s and timing is controlled by a simple ring counter.

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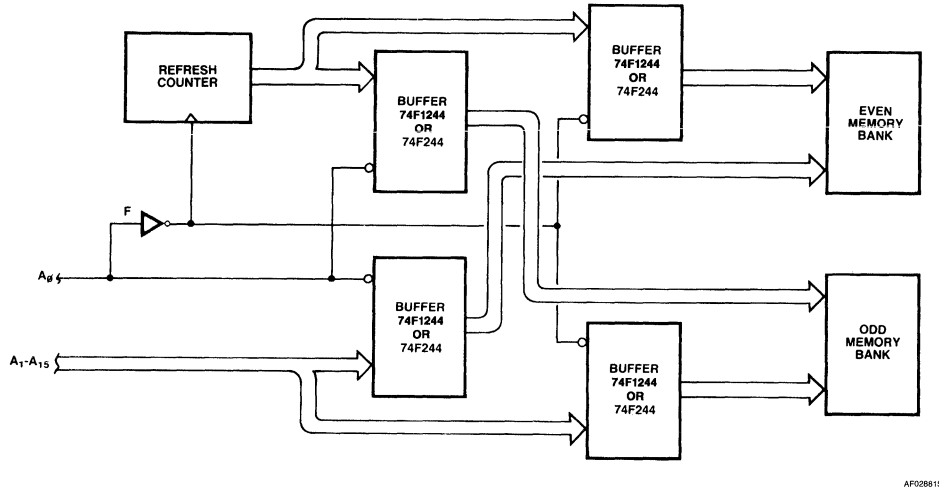


Figure 10. Using Interleaving Technique To Refresh Dynamic RAM Memories

OPERATION & APPLICATIONS SUMMARY

Most dynamic RAMs must be refreshed at least every 2-milliseconds to ensure retention of valid data. One method of memory refresh is shown in the above example. This system uses interleaving and relies on the premise that, during normal program execution, A_0 toggles frequently enough to refresh the RAM without slowing the microprocessor with wait-states or DMA cycles to refresh the counter. If the system program uses wait-states, halt instructions, or address incrementing is otherwise limited, A_0 may not toggle at a rate sufficient to accomplish refresh. For such situations, additional circuits or special programming may be required to prevent loss of data. Operation of the system can be summarized as follows:

- When even bank is addressed by CPU, odd bank is refreshed by address counter.
- Even bank is refreshed when CPU addresses the odd bank.
- A_0 increments the refresh counter before each odd-bank refresh.

Using FAST ICs For μP-To-Memory Interfaces AN205

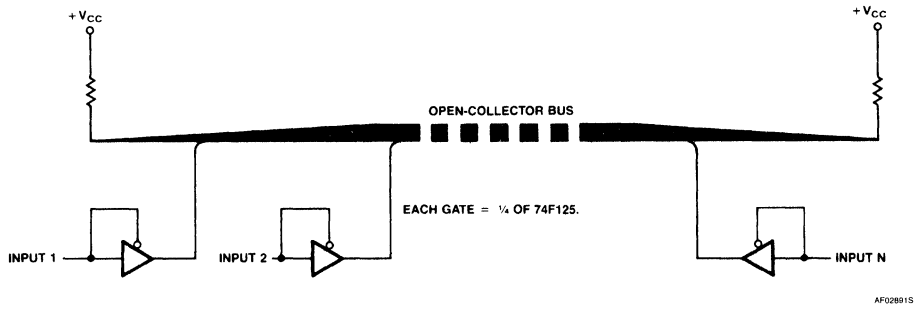


Figure 11. Reducing Leakage Current When Driving Open Collector Buses

OPERATION & APPLICATIONS SUMMARY

The number of buffers (7406 type) that can share an open-collector bus is often limited by device leakage or by the increased power consumption caused by lowering the values of the pullup resistors. A method of reducing the leakage current is shown in the above example. Here, the logic input and output enables of each gate are tied together; thus, the gate output is floated high to drive the open-collector bus. Floating the gate outputs provides a significant reduction in leakage current which allows the use of more gates and/or reduced power consumption by the pullups.

SUMMARY

Many of the applications and concepts provided in this document were direct contributions or heavily influenced by entries in the Signetics' Interface Circuit Design contest. Our special thanks to those individuals whose entries are referenced in whole or in part.

As integrated circuits become more and more complex, fewer and fewer parts are required to implement a functional system; thus, interface support is a major consideration in the overall design process. To produce a competitive and cost effective product, the user must choose interface components that are efficient, reliable, and those that reflect the best features of current technologies. Signetics has met these challenges in the past and will continue to meet them in the future, providing silicon solutions that are truly state of the art — be it logic, memories, gate arrays, or other. For further documentation and/or applications assistance, call or write to your nearest Signetics Sales and Service Office — there is one near you.

Signetics

AN206
Using μP I/O Ports With FAST Logic

Application Note

Logic Products

INTRODUCTION

Signetics interface ICs are most often used to implement input and output ports in microprocessor based systems. This application note illustrates the effective use of Signetics FAST devices to interface microprocessor data and address buses to general purpose I/O ports. Topics illustrated include handshaking, multiplexing, arbitration, and bit manipulating. More complex circuits involving memory interfacing, shared memory, and multiple processors are covered in other application notes.

Simple I/O Ports

The simple Input/Output ports shown in Figure 1 use 74F374 octal flip-flops and 74F244 octal 3-State buffers to interface to a microprocessor's data bus. The input port is enabled by $\overline{RD}$ AND $\overline{PORTSEL}$. The output is enabled by $\overline{WR}$ and $\overline{PORTSEL}$.

When 16 pin packages are preferable to 20 pin packages for physical design considerations, 3-State multiplexers may be used as input ports. In Figure 2, 74F257 quad two-input multiplexers are used. A_0 selects between port A and port B.

In Figure 3, a 74F373 octal transparent latch is used to drive a light emitting diode annunciator array. The output follows the data bus while E is high, and the display freezes when E goes low. The 20mA sink current of the 74F373 permits interface to most LED devices.

A potential hazard exists when using transparent latches as output ports. The timing diagram of Figure 4 shows that data may not be valid when E is brought high, causing invalid data to be present on the output for a brief period. This will not cause a problem when driving LEDs because the duration of the invalid data is too short to be seen. But, problems will occur if the outputs are used to trigger other circuits that cannot tolerate glitches. Flip-flops should be used instead of transparent latches when these conditions exist.

Interfacing microprocessors to slow peripherals, such as printers, usually requires handshaking logic. In Figure 5, the 74F374, 3-State octal flip-flop acts as an output port for the microprocessor and as an input port for peripheral. The microprocessor writes data to the output port which sets /data available low. The peripheral then reads input port which sets /data accepted low and /data available back to high. The low /data accepted line interrupts microprocessor indicating that peripheral is ready for another data transfer.

Bit Manipulation

In Figure 6, the 74F251, 3-State 8 to 1 multiplexer provides a bit-oriented input port. This technique permits processors which do not have built-in bit manipulating capability to examine single bits at input ports efficiently. In addition, parallel inputs may be read bit-serially over a single data line. Address lines A_0, A_1, and A_2 select the bit to be read, and data bus line D_7 is selected to permit a simple software decision based on JUMP-ON-SIGN or SHIFT-LEFT & JUMP-ON-CARRY.

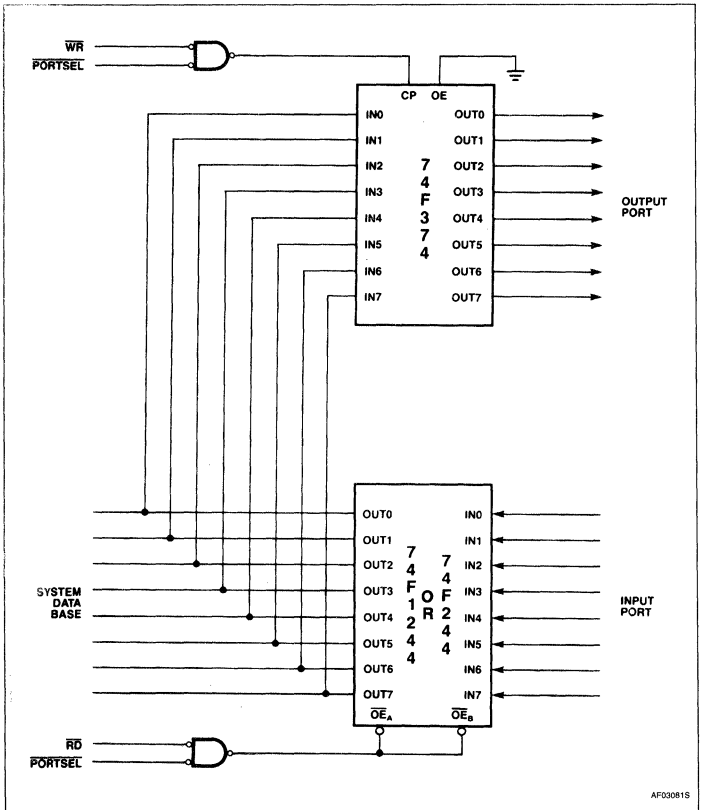


Figure 1. Simple Input/Output Ports Interface With Microprocessor Data Bus

A versatile bit-oriented output port may be implemented with a 74F259, eight-bit addressable latch as shown in Figure 7. With this technique single output bits may be manipulated without maintaining a copy of the output port contents in memory. This is useful in bit-oriented control applications. The addressable latch effectively performs serial to parallel conversion on data supplied from the system bus. Data is written to 1 of 8 output bit locations specified by address lines A_0, A_1, and A_2.

Caution: Address inputs must be stable before latch is enabled or data can be entered into incorrect locations. If output glitches cannot be tolerated, data input must also be stable before the latch is enabled.

A similar technique is used in Figure 8, to accomplish bit manipulation without using the data bus. Each bit is associated with two addresses. If A_0 is high, the bit is set high; if A_0 is low, the bit is set low. With this approach bit-manipulation is faster and requires less program memory because data does not have to be loaded and output from the accumulator. Also PCB layout complexity is reduced by removing the data bus from the output port.

I/O Timing

In many applications it is necessary to adjust timing to match microprocessor specifications to bus specifications. For example, the MC6809 microprocessor has data write hold time of 30ns, making it difficult to interface to peripheral chips such as floppy disk controllers that have longer hold time requirements.

Figure 9 extends this hold time for interface to slow peripheral devices. A 74F373 3-State octal transparent latch is used to freeze data on I/O bus during write operations. During read operations, the 74F373 outputs are floated and data is read through the 74F244 3-State octal buffer.

Figure 10 shows the timing diagram for an I/O bus with extended hold time. During the write cycle, data is latched by 74F373 on the falling edge of E. Data remains on the outputs of the 74F373 until the rising edge of Q at the beginning of the next cycle, when the outputs are floated. The read cycle is unaffected. Data hold time is extended to ¼ cycle – from 30ns to 250ns for a 1MHz cycle rate. Note that a latch is used instead of a flip-flop to preserve the data set-up time of the 6809.

A dedicated hardware solution is faster in systems requiring high throughput rates where the required function is performed frequently. In Figure 11, a 74F374 3-State octal flip-flop is used as both input and output port. By jumpering the output data lines of the 74F374 to different system data bus lines, various dedicated functions can be realized – examples are nibble swapping, bit transposing, and data encryption. The software to perform data manipulation is simple – data is written to the octal flip-flop, and manipulated data is read back into the processor using the following instructions: OUT (DATA MANIPULATOR), A IN A, (DATA MANIPULATOR)

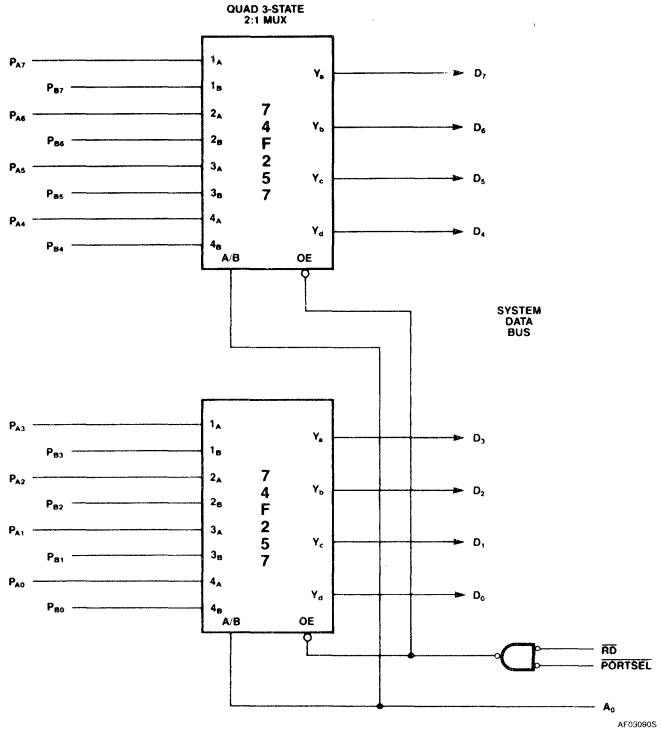


Figure 2. Use Of 3-State Multiplexers As Input Ports

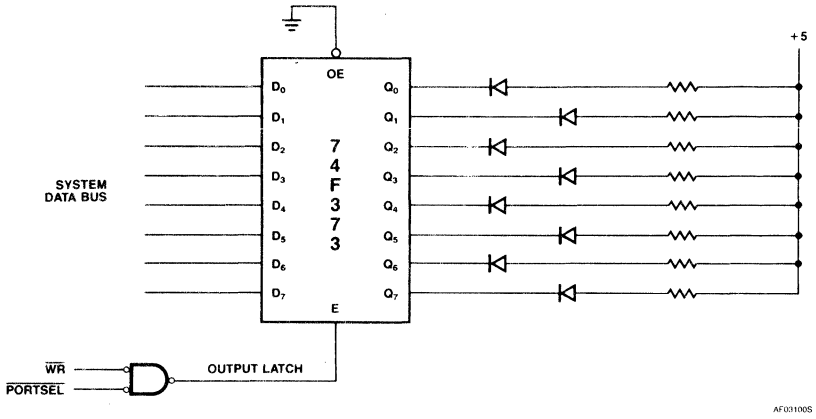


Figure 3. Output Port Driving LED's Using 74F373 Octal Transparent Latch

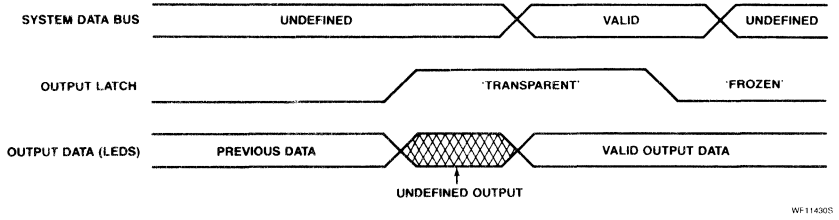


Figure 4. Potential Hazard Exists When Using Transparent Latch As Output Port

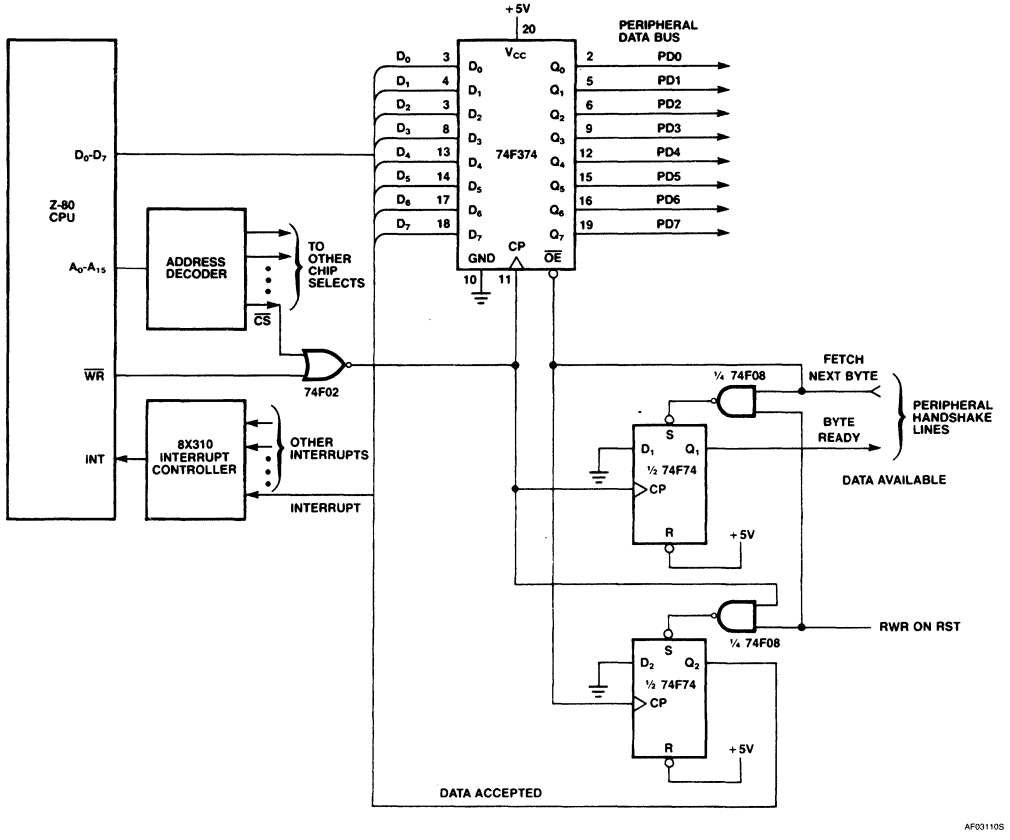


Figure 5. Interfacing Microprocessors To Slow Peripherals, Such As Printers, Using Handshaking Logic

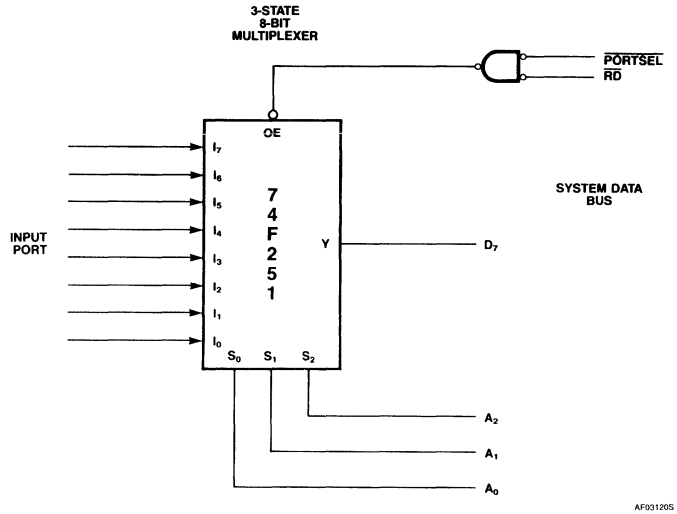


Figure 6. Three-State 8 To 1 Multiplexer Provides Versatile Bit-Oriented Input Port

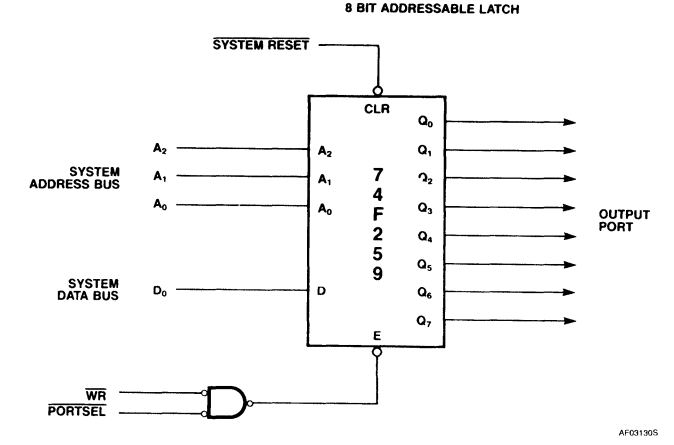


Figure 7. Eight-Bit Addressable Latch Provides Versatile Bit-Oriented Output Port

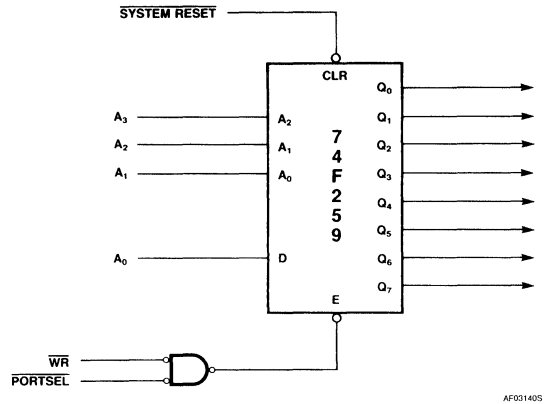


Figure 8. Bit Addressable Output Port Does Not Require Data Bus

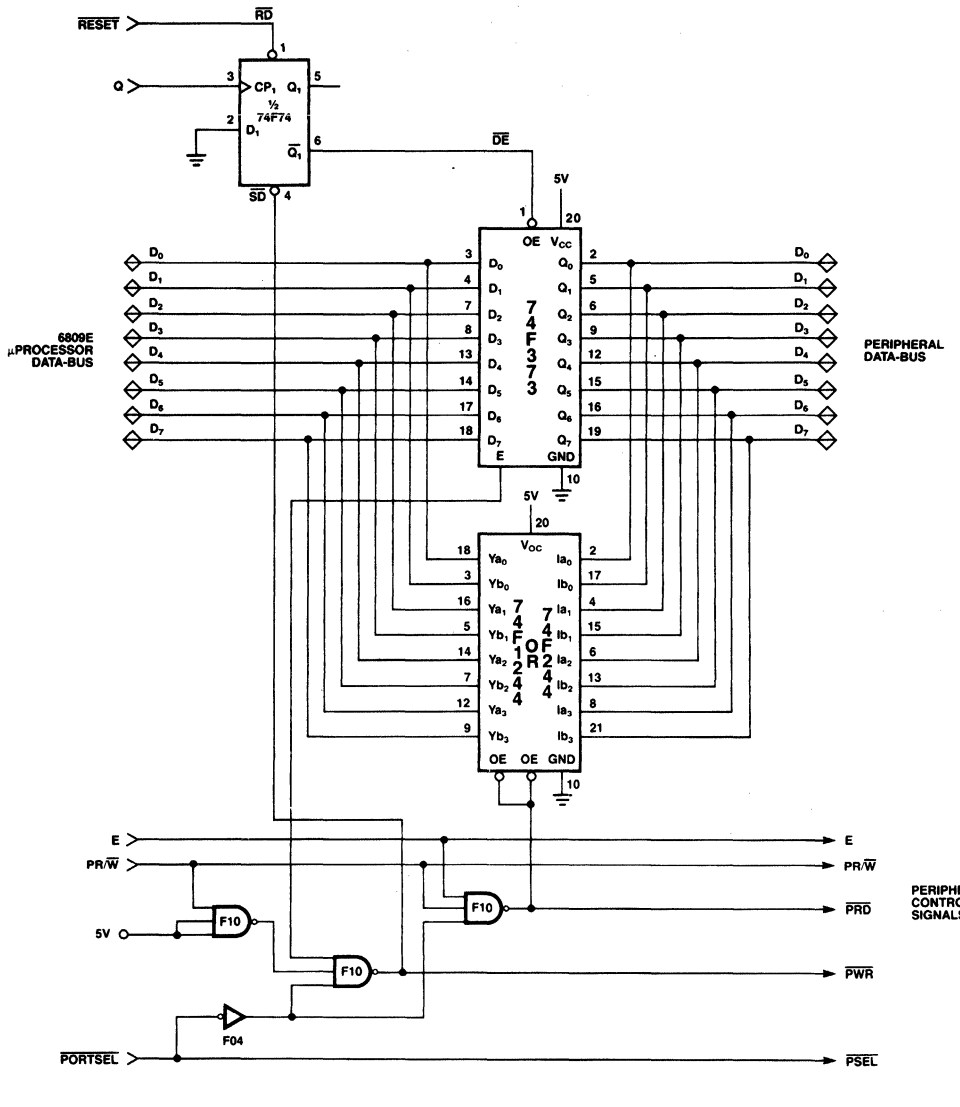
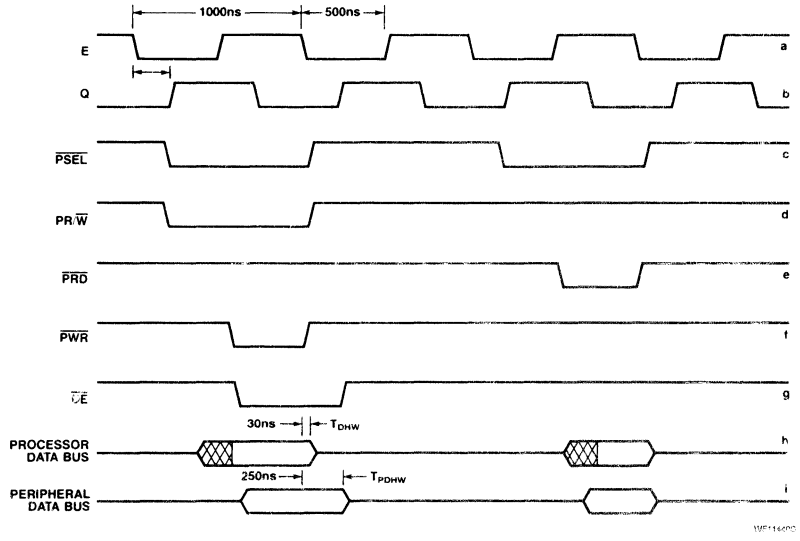


Figure 9. Hold Time Extended For Interface To Slow Peripheral With MC6809 Microprocessor



NOTES:
1. RESET -Power on reset
2. Q -6809E processor clock (1MHz shown)
3. O -Quadrature clock for 5809?
4. DE -Peripheral bus driver enable
5. PR/$\overline{W}$ -Peripheral READ/$\overline{WRITE}$
6. PSEL -Peripheral select
7. PRD -Peripheral read
8. PWR -Peripheral write
9. T_{DHW} -6809E output data hold time
10. T_{PDHW} -Peripheral write data hold time

Figure 10. Timing Diagram For I/O Bus With Extended Hold Time

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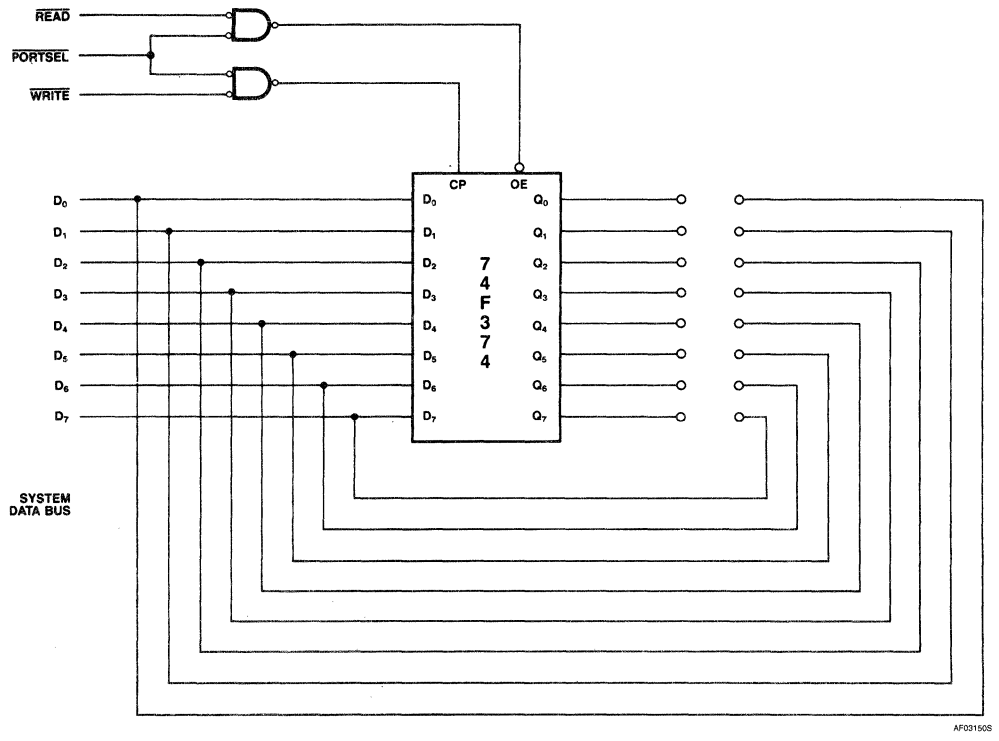

Figure 11. Data Manipulator Uses Dedicated Hardware

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the following individuals whose entries were referenced in whole or in part in this note:
V.K. Agrawal
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G.B. Livingston
Joseph Mastroieni
Jonathan A. Titus
Eugene M. Zumchak

Signetics

AN207
Multiple μP Interfacing With FAST ICs

Application Note

Logic Products

INTRODUCTION

As microprocessor costs continue to decrease and the demands on product performance continue to increase, designers are increasingly turning to multiple microprocessor systems to meet the performance challenge. The introduction of many "peripheral controller" type processors has made this choice even more attractive. This application note addresses typical problems associated with interfacing multiple microprocessors, and illustrates the use of Signetics Interface Circuits in solving these problems.

A multi-processor system contains two or more processors communicating through parallel ports, multi-port memories, serial data links, and/or shared buses. The most popular multi-processor architectures are "loosely coupled" systems. In loosely coupled systems each processor operates asynchronously with the other processors, usually performing a separate function. Communication is not continuous, and occurs only when necessary.

A special application for multiple microprocessor systems is in redundant systems. As the price of microprocessors dropped, it became economically feasible to achieve greatly increased reliability by employing several processors operating in parallel, performing identical functions. After each operation a vote is taken on the result. If there is disagreement, a fault has been detected, and appropriate corrective action can be taken. Appropriate action might be switching in a third processor, repeating the process, or activating an error sequence and/or an alarm.

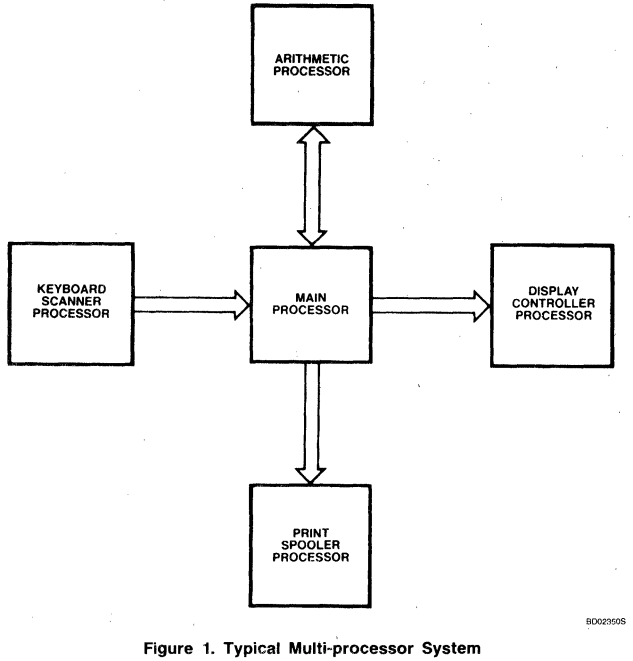

Figure 1. Typical Multi-processor System

In the typical loosely coupled multiple processor system of Figure 1, a main processor "delegates" processing work to four other processors. A keyboard scanner microprocessor scans the keyboard continuously, debounces key closures, performs code conversions, and transmits key codes to the main processor in a format that it can easily assimilate. A separate arithmetic processor accepts parameters from the main processor, performs arithmetic calculations, and provides the results for the main processor to read when it is not busy with other tasks. The display controller accepts data and commands from the main processor, then displays and manipulates data on CRT or other displays. The display controller refreshes the display and supports graphic displays without tying up the main processor. The print spooler is a separate processor that accepts files to be printed from the main processor using high-speed data transfers. Then the print spooler stores and feeds data to the printer at the printer's lower data rate, freeing the main processor for other chores. Each processor module contains its own "local" ROM, RAM, or I/O, so that it performs its task independently, and communicates with other processors only when necessary. As a result, the system as a whole operates closer to its maximum speed.

Some of the advantages of multiple microprocessor systems are:

- Each processor performs a relatively independent task.
  - Design is easily split among team members.
  - Testing is easily performed on a modular level.
  - Modules can be added or modified without affecting other modules.
- Multi-processing allows distributed processing where modules may be physically separated from the main system.

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Multiple μP Interfacing With FAST ICs AN207

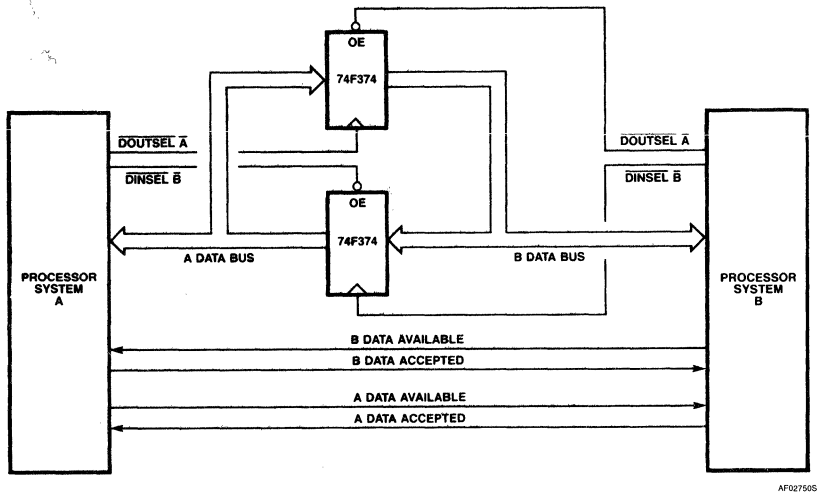

Figure 2. Basic Inter-processor Communication Using Parallel I/O Ports

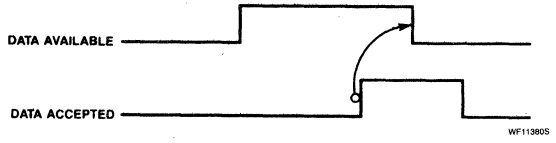

Figure 3. Handshake For Parallel Port Communication

- Parallel processing greatly increases system performance and throughput.
- Hardware cost is less than single-processor systems with similar performance.
- Reliability can be increased easily by redundant processing.

The following application examples illustrate the use of Signetics FAST Interface Circuits in multiple processor systems.

PARALLEL I/O PORT COMMUNICATIONS

Figure 2 shows how parallel I/O ports using Signetics FAST Interface devices are used to accomplish simple 2-processor communications. Two 74F374 octal 3-State registers are used to implement bi-directional parallel data communication. Each 74F374 acts as output port to one processor and input port to the other. The handshake lines are needed when the processors operate asynchronously to ensure that data has been received before new data is transmitted. A handshake timing protocol (Figure 3) implemented in software acts as a traffic cop to assure valid data communications. The transmitting processor starts the handshake by setting Data Available to indicate that data is valid. The receiving processor sets Data Accepted to indicate data has been read. The transmitter then resets Data Available allowing the receiver to reset Data Accepted. The transmitter will not send new data until Data Accepted is reset.

COMMUNICATIONS VIA MULTI-PORT MEMORY

Figure 4 shows the logic required for two processors to communicate through a multi-port memory. The RAM is accessible from both processor A and processor B via 74F157 multiplexers used to select one processor's bus at a time. Multi-byte messages and data blocks may be written into the memory by one processor and read out by the other at a later time. No byte-by-byte handshake is required. The multi-port memory provides increased system performance at somewhat higher cost compared to a parallel port technique. Because of the use of multi-port memories in microprocessor systems, these systems can become quite complex. Another application note in this series covers interfacing to multi-port memories in greater depth.

Multiple μP Interfacing With FAST ICs AN207

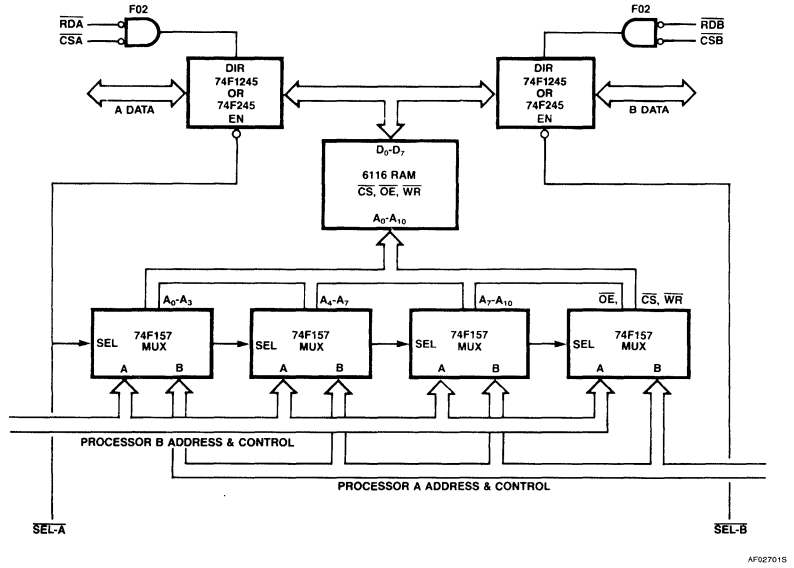

Figure 4. Multiport Memory Provides High-performance Multi-processor Communications

SERIAL COMMUNICATIONS

Although serial communications between multiple processors is slower than the parallel methods examined above, it is usually less expensive and very useful for communicating with remote units. Serial communications via RS-232 or RS-422 links can provide reliable communications over great distances. Implementation of serial communications is simplified by the availability of Universal Asynchronous Receiver Transmitter (UART) devices and well established standards for circuit interfaces and protocols. Figure 5 shows local/remote processor communication using Signetics SC2681 UART devices. In many cases additional interface lines are required for handshaking.

SHARED BUS ARCHITECTURE

One of the most powerful multiple processor architectures uses the popular shared bus concept. In Figure 6, each processor has its own local bus with some combination of RAM, ROM, and I/O available locally. The shared bus permits use of "global resources" such as global memory and global I/O which are accessible to all processors on the shared bus. Common interfaces such as printer ports do not have to be implemented for each processor, and may be connected to the shared bus. Multiple processors communicate indirectly with one another through the global RAM. This technique provides highest throughput when interconnecting more than two processors. It also reduces cost through sharing of global resources.

Any processor permitted to drive the system address, data, and control buses is known as a "master." Processors not having this capability are "slaves." A useful attribute of shared bus systems is the ability to add whole new functions by connecting a new master to the bus. Figure 7 shows a typical shared system bus interface using Signetics Interface circuits. Three 74F244 octal 3-State buffers are used to drive the 24 bit system address bus (16 bits in some cases). Two 74F245 octal bidirectional 3-State buffers are used to drive the 16 bit data bus (8 bits in some cases). In addition, half a 74F244 is used to drive the system command bus, composed of the signals $\overline{IORD}$, $\overline{IOWR}$, $\overline{MEMRD}$, and $\overline{MEMWR}$.

Multiple local processors may request use of the shared bus by setting $\overline{BUS\ REQUEST}$ active and waiting for the arbitration logic to assert $\overline{BUS\ GRANT}$. The arbitration logic indicates to the local processor when it may access the shared bus after a request has been made. This is necessary to prevent more than one local processor from accessing the system bus at the same time, resulting in bus contention and possible system failure.

ARBITRATION

Contention by several processors for use of shared resources can create sticky timing problems unless care is exercised in the design of appropriate arbitration logic to resolve timing conflicts. Schemes for bus arbitration vary in speed, cost, and flexibility and involve parallel, serial, transparent, pseudo-transparent, polled, and flag operations.

Parallel Priority Resolution

Parallel priority resolution is most useful in systems with 4 or more masters, where its speed outweighs the disadvantage of the additional hardware. A scheme for system bus arbitration using parallel priority resolution is shown in Figure 8.

A master's priority is determined by using a 74F148 priority encoder. Each master's arbitration logic generates a $\overline{REQ}$ to the priority encoder. When there is contention, the master whose $\overline{REQ}$ is connected to the highest priority input will be granted access.

A 74F138 is used to decode the encoder outputs to generate the $\overline{EI}$ (enable input) to the arbitration logic of the master which has been granted access. $\overline{CLEAR}$ is used to remove all masters from the bus during reset or when an error condition is present. $\overline{ARB\ CLOCK}$ is used to synchronize all bus arbitration inputs and outputs to prevent race conditions and to facilitate a standard interface

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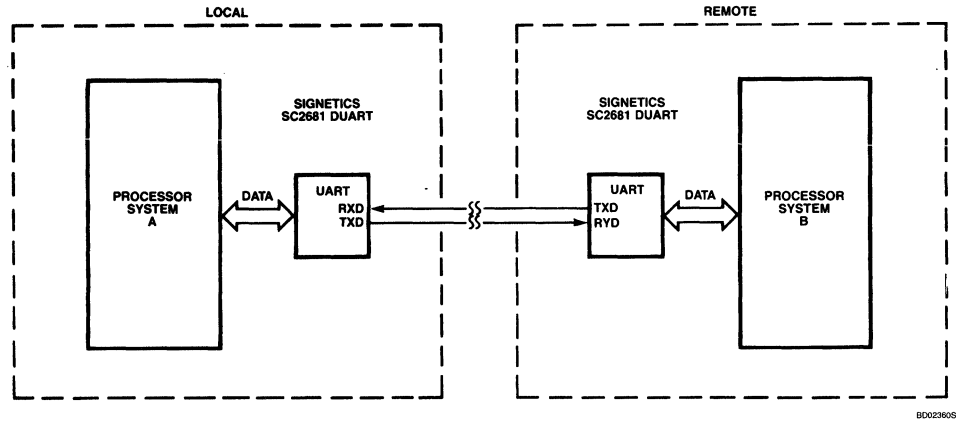

Figure 5. Serial Communications Link Provides Economical Inter-processor Communications

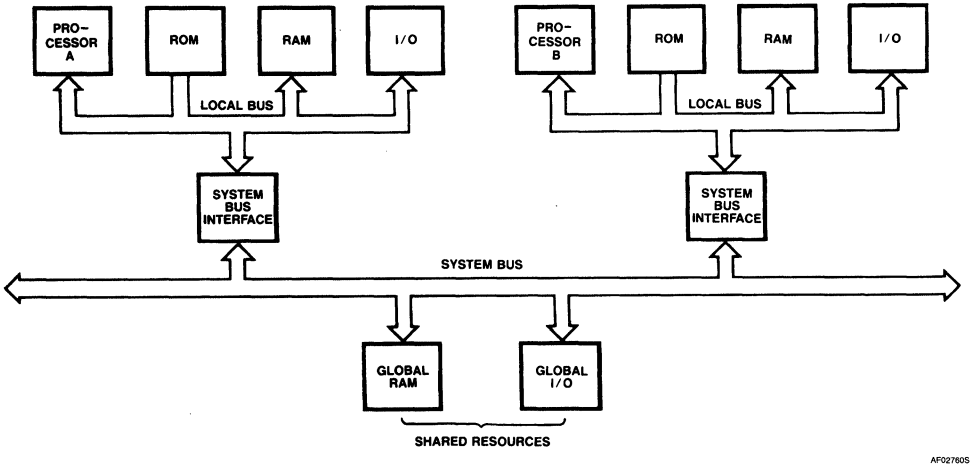

Figure 6. Shared Bus Provides Most Powerful Multiple Processor Architecture

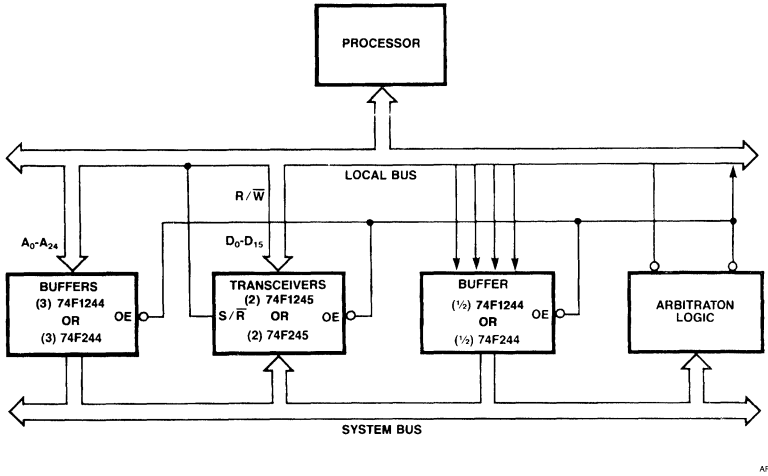

Figure 7. Typical System Bus Interface

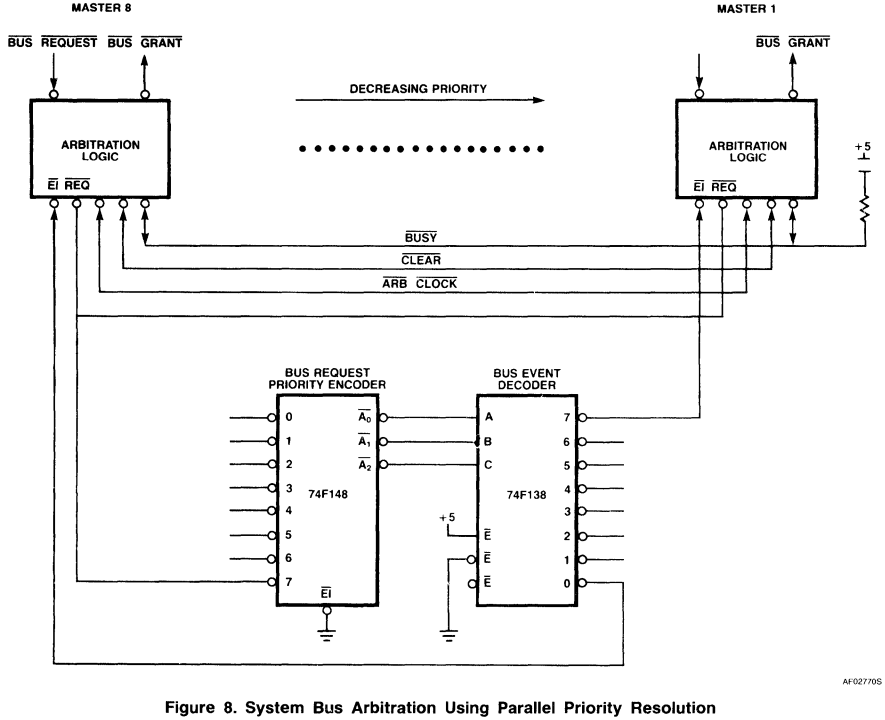

Figure 8. System Bus Arbitration Using Parallel Priority Resolution

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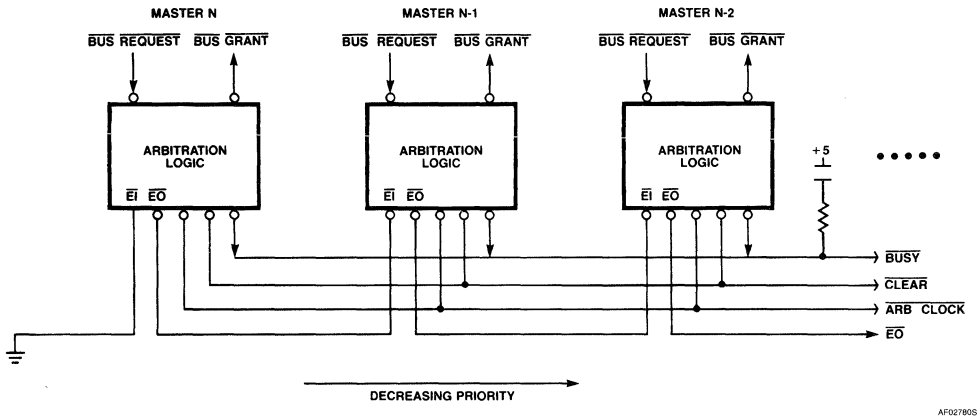

Figure 9. System Bus Arbitration Using Serial Priority Resolution

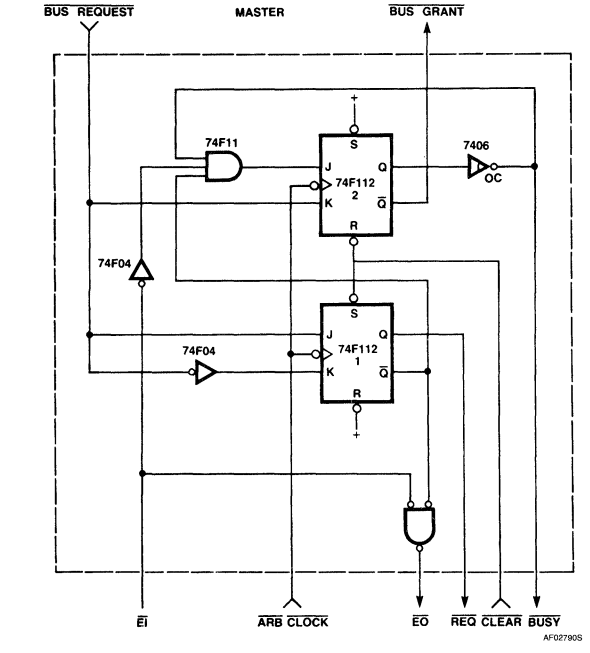

Figure 10. Arbitration Logic Supports Serial Or Parallel Priority Resolution Techniques

design. $\overline{BUSY}$ is generated by the master currently accessing the bus to indicate that the bus is in use. Even after a master has been granted access by the priority resolution, it must still wait for the current master to vacate the bus, i.e., $\overline{BUSY}$ going inactive. The arbitration logic generates a $\overline{BUS\ GRANT}$ to a master when $\overline{EI}$ is asserted and $\overline{BUSY}$ is not.

Serial Priority Resolution

Serial priority resolution eliminates the need for encoder/decoder hardware at the expense of speed. In Figure 9 a master's priority is determined by its physical location in a daisy chain configuration. A master negates its $\overline{EO}$ (enable output) when its $\overline{EI}$ (enable input) is negated or when it wants to access the bus. This negates $\overline{EO}$ for all masters further down the line *to go inactive*. If a master requests the bus, and no higher priority master is requesting the bus, as indicated by $\overline{EI}$ being asserted, the master may access the bus when the current master is finished. The ARB clock rate is limited to the speed at which the daisy chain signals can propagate through all masters.

Arbitration Logic

Arbitration logic suitable for either parallel or serial priority resolution is shown in Figure 10. The logic shown synchronizes a master's $\overline{BUS\ REQUEST}$ input to $\overline{ARB\ CLOCK}$ using flip-flop 1, asserting $\overline{REQ}$ and negating $\overline{EO}$. If $\overline{EI}$ is asserted and $\overline{BUSY}$ is not, the master may access the bus on the next falling edge of $\overline{ARB\ CLOCK}$. This arbitration is provided by flip-flop 2. $\overline{BUS\ GRANT}$ and $\overline{BUSY}$ are asserted. When the access is complete, the master negates $\overline{BUS\ REQUEST}$ inactive. On the falling edge of $\overline{ARB\ CLOCK}$, $\overline{REQ}$ negated and, if $\overline{EI}$ is asserted $\overline{EO}$ is asserted. On the next falling edge $\overline{BUSY}$ and $\overline{BUS\ GRANT}$ are negated. The timing diagram for this sequence is shown in Figure 11. Note that a master must wait for the current master to complete a transfer and negate $\overline{BUSY}$ before it may access the bus.

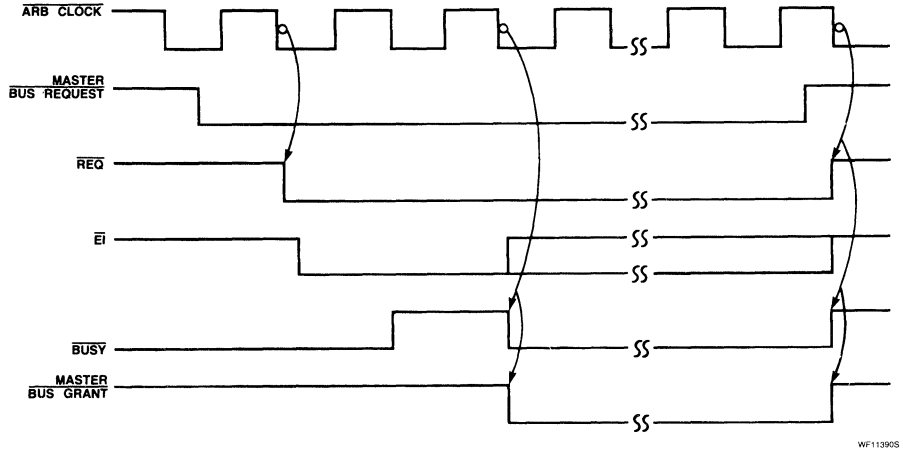

Figure 11. Timing Diagram For Arbitration Logic

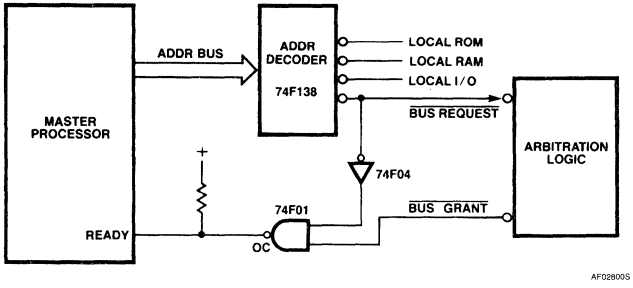

Figure 12. Pseudo-transparent Access To Shared Bus

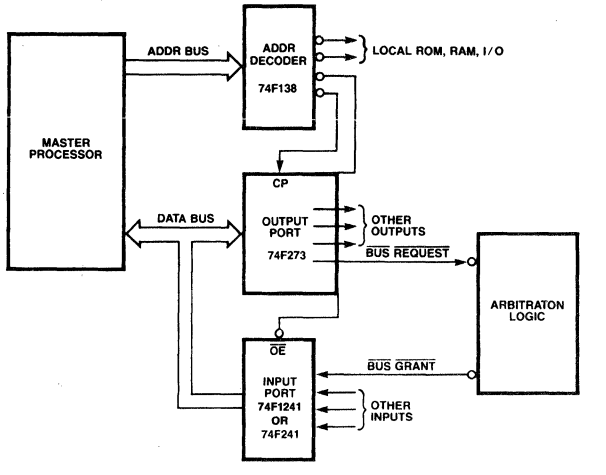

Figure 13. Polled Access To Shared Bus

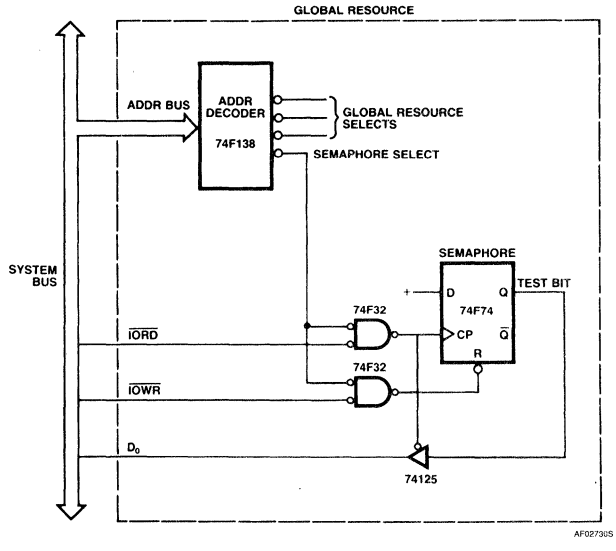

Figure 14. Semaphore (Flag) Register Permits Access To Shared Resource Without Monopolizing Shared Bus

Pseudo-Transparent Priority Resolution

The logic of Figure 12 uses "cycle stealing" to permit single byte transfers with pseudo-transparent arbitration. When the address decoder determines that a master requires access to shared bus, it asserts $\overline{\text{BUS REQUEST}}$. The processor's READY line is held negated, "freezing" the processor until the arbitration logic asserts $\overline{\text{BUS GRANT}}$. Then READY is asserted and the shared bus cycle occurs. The processor is unaware of arbitration and unaware that the bus is shared. With this technique, a watchdog timer should be used to ensure that the processor doesn't "hang up" if faulty bus operation prevents access. Access occurs one cycle at a time, preventing any one master from "hogging" the bus.

Polled Access to Shared Bus

The logic in Figure 13 uses an output port to request access to the bus, and polls an input port to determine when access has been granted. Once access is granted, the master retains the bus until it negates the $\overline{\text{BUS REQUEST}}$ output port bit. Large block moves may occur without fear of another master changing the data as with cycle-by-cycle arbitration. However, this approach greatly slows down the response time of the system, because of the waiting while each master performs. All other masters must wait, even if they do not require the use of the same shared resource.

Semaphore (Flag) Arbitration

The logic of Figure 14 improves on the polled access technique by permitting access to a shared resource when that resource is available. A master first reads the semaphore register associated with the resource it wishes to access. The master may not access the resource unless the semaphore bit is false. When the semaphore bit is false, reading the register automatically sets the bit true. When the master reads a false semaphore, it may then access the resource. All other masters reading the semaphore will see it set and will not access the resource. The master may access the resource until it is no longer needed. By writing to the semaphore register, it is automatically reset, allowing other masters to access the resource. Only the one resource, not the entire shared bus, is monopolized by one master at a time. The hardware performs a function similar to a software read-modify-write operation.

The timing for the semaphore operation is shown in Figure 15. If the semaphore bit is false and the register is read, the bit is set true at the end of the read cycle (rising edge of $\overline{\text{IORD}}$). The semaphore bit is reset by doing a "dummy" write to the semaphore register. The bit is set false at the beginning of the cycle ($\overline{\text{IOWR}}$ going low).

INTERFACING THE MC68000 TO THE MULTIBUS™*

One of the best examples of a multi-processor shared bus is the MULTIBUS. One of the

*MULTIBUS is a trademark of Intel Corporation.

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most popular 16 bit processors in new designs today is the MC68000. Yet, to our knowledge, there are currently (mid-83) no LSI MULTIBUS arbiter ICs available to allow a designer to easily interface the two. There are arbiter ICs available, but they were designed for other processors and are cumbersome and limited in performance when interfaced to the 68000.

The following is the design for a 68000 MULTIBUS interface. The design supports serial or parallel arbitration and performs with a 10MHz bus clock. Operation is similar to the example described previously. Tables 1 and 2 define the MC68000 bus control signals and the MULTIBUS arbitration signals. The timing diagram for MC68000 read and write cycles is shown in Figure 16.

Figure 17 shows the control circuitry for the MC68000 to MULTIBUS interface. The master initiates a MULTIBUS transfer by asserting $\overline{\text{MULTIREQ}}$ active. This is usually the output of address decode circuitry. $\overline{\text{AS}}$ clears the request at the end of the transfer. Flip-flops 1, 2, and 3 sample and synchronize the bus request to the falling edge of $\overline{\text{BCLK}}$. Since $\overline{\text{MULTIREQ}}$ is asynchronous to $\overline{\text{BCLK}}$, flip-flop 2 serves as a synchronizer and is clocked on the rising edge of $\overline{\text{BCLK}}$. All inputs to the arbiter are thus synchronous so that race conditions at flip-flop inputs are avoided.

If the bus is not in use ($\overline{\text{BUSY}}$ is not asserted), and no higher priority master requests the bus ($\overline{\text{BRPN}}$ is asserted), the master is granted access on the next falling edge of $\overline{\text{BCLK}}$. Flip-flop 4 provides this function. If these conditions are not satisfied, $\overline{\text{DTACK}}$ is used to force the CPU to wait. Once the master is granted access, it sets $\overline{\text{BUSY}}$ active to indicate that the bus is in use. $\overline{\text{BUSEN}}$ (bus enable) also becomes active and gates the master's address, data, and control buses onto the MULTIBUS. One half cycle later, on the rising edge of $\overline{\text{BCLK}}$, flip-flop 5 sets CMDEN (Command Enable) active. This allows RD or WR strobes to be asserted on the MULTIBUS. This delay is necessary because the MULTIBUS requires data and address valid 50ns before read or write commands. DS is used to generate the read or write strobes.

The MULTIBUS transfer is completed when $\overline{\text{XACK}}$ is asserted terminating the 68000 cycle by asserting $\overline{\text{DTACK}}$. The master maintains control of the MULTIBUS until another master requests access, as indicated by asserted $\overline{\text{CBRQ}}$. If the current master is not performing a MULTIBUS transfer, it loses the bus on the next falling edge of $\overline{\text{BCLK}}$. CMDEN, $\overline{\text{BUSEN}}$, and $\overline{\text{BUSY}}$ are negated. Flip-flop 4 provides this function.

Table 1. MC68000 Bus Control Signals. (Refer To The Signetics 68000 Microprocessor Data Sheet For More Information.)

CLK	Clock. Time reference for 68000 microprocessor bus control.
$\overline{\text{AS}}$	Address Strobe. Indicates that address on address bus is valid.
$\overline{\text{UDS}}$, $\overline{\text{LDS}}$	Upper and Lower Data Strobe. Indicates that the processor is reading from or writing to the upper data byte ($D_7 - D_{15}$) and/or the lower data byte ($D_0 - D_7$).
R/$\overline{\text{W}}$	Read/Write. Indicates whether the current bus cycle is a read or a write cycle.
$\overline{\text{DTAK}}$	Data Transfer Acknowledge. Input to the 68000 indicating that the data transfer can be completed, on the high to low transition.
$\overline{\text{BCLK}}$	Bus Clock. All arbitration signals listed below must be synchronized to the negative edge of this clock. It is independent of any processor clock.
$\overline{\text{BPRN}}$	Bus Priority In. Indicates that no higher priority master is requesting the bus. Similar to $\overline{\text{EI}}$ in previous examples.
$\overline{\text{BPRO}}$	Bus Priority Out. Used in serial priority resolution circuits. Similar to $\overline{\text{EO}}$ in previous examples.
$\overline{\text{BUSY}}$	Bus Busy. Driven by current bus master to indicate that the bus is in use.
$\overline{\text{BREQ}}$	Bus Request. Used in parallel priority resolution circuits. Similar to $\overline{\text{REQ}}$ in previous examples.
$\overline{\text{CBRQ}}$	Common Bus Request. Driven by all potential bus masters requesting bus. Used to save time by allowing the present bus master to avoid arbitration after each cycle if no other requests are active.
$\overline{\text{XACK}}$	Transfer Acknowledge. Indicates that the MULTIBUS data transfer is completed on high to low transition.

The logic that interfaces the MC68000 to the MULTIBUS is shown in Figure 18. 74F533 inverting octal 3-State latches are used to gate the 20 bit address and 16 bits of data onto the MULTIBUS. Note that the data and address bus is negative true. 74F240 octal 3-State inverting buffers are used to gate 16 bits of data onto and off of the MULTIBUS. Data direction is determined by the MC68000's R/W line. A 74F139, 2 to 4 decoder is used to decode I/O and RD/WR to generate the 4 MULTIBUS commands. I/O is the output of address decode circuitry which decodes I/O addresses. A 74F244 is used to gate the commands onto the MULTIBUS.

Signetics FAST logic family is used in this design to increase speed and bus drive capability while minimizing MULTIBUS loading.

REDUNDANT MICROPROCESSORS ENHANCE RELIABILITY

Figure 19 shows how two 6809E microprocessors are used in a parallel redundancy scheme to prevent faulty operation from damaging external systems. Two systems with identical processors, RAM, ROM, and I/O are first synchronized. After synchronization, their data buses are compared every cycle. If the data on the two buses is different, an error has occurred and the system shuts down.

A common clock is used to drive the 6809E processor in each system so that a timing reference is established. Upon reset, both processors execute a sync instruction and the critical output circuits are turned off. When both processors have executed the sync instruction, as indicated by BA = 0 and BS = 1, the START button is used to interrupt the processors and they begin program execution in synchronism. The critical outputs are also turned on. On the falling edge of E, the data buses of the two systems are compared using the 74F521 octal comparator. If the data does not match, at least one system is operating incorrectly. The 74F74 flip-flop latches the error condition and turns off the critical outputs.

A similar technique should be used on outputs to ensure that an output goes active only when the output of both systems goes active.

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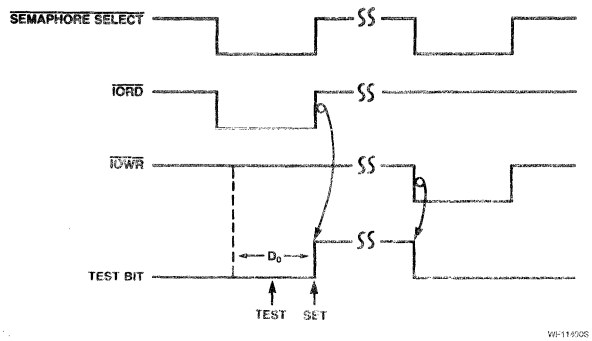

Figure 15. Timing Diagram For Semaphore Operation

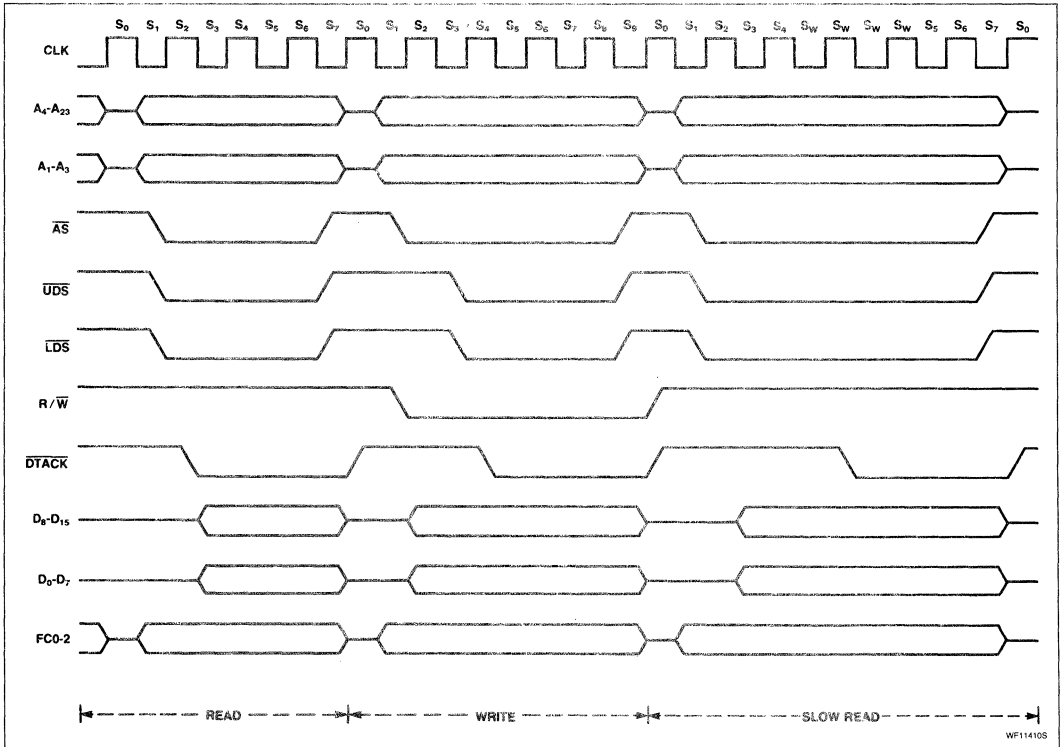

Figure 16. MC68000 Read And Write Cycle Timing Diagram

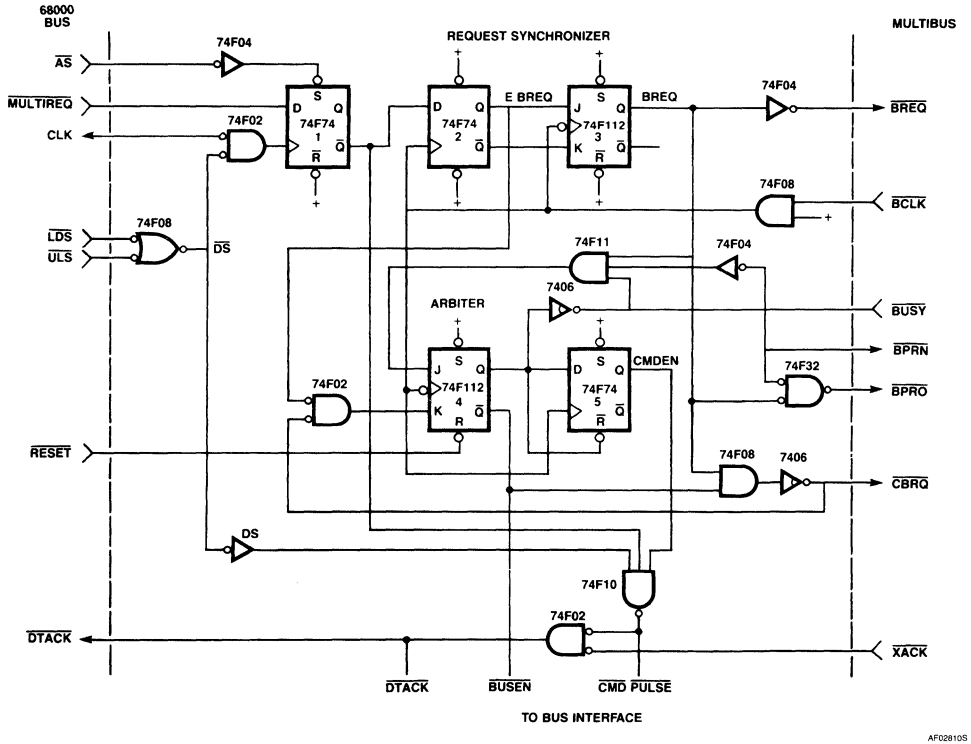

Figure 17. MC68000 MULTIBUS Interface Control Circuitry

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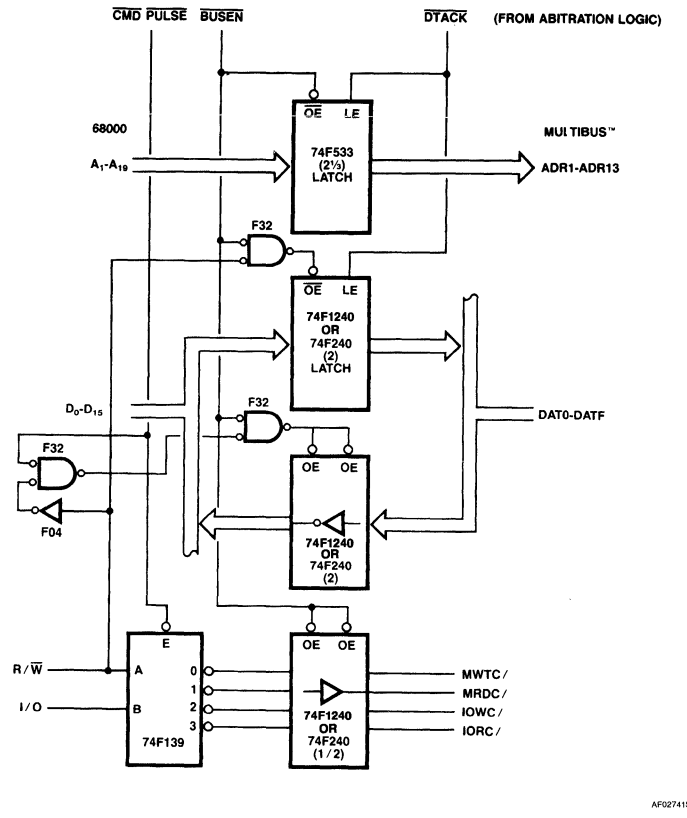

Figure 18. MC68000 To MULTIBUS Interface Logic

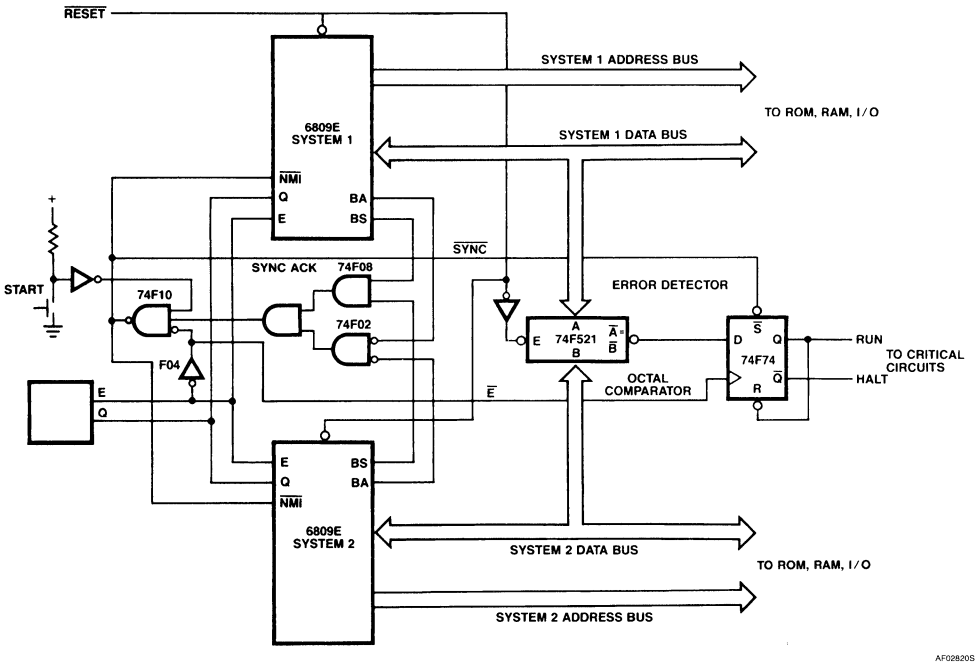

Figure 19. Redundant 6809E Microprocessors Prevent I/O Damage

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the individuals whose entries were referenced in whole or in part in this note.

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Signetics

AN208
Interrupt Control Logic Using FAST ICs

Application Note

Logic Products

INTRODUCTION

This application note shows how Signetics FAST circuits can be used to implement interrupt control logic for a variety of microprocessors. The circuits presented serve a variety of functions, which include:

- Masking: How to selectively enable interrupt inputs
- Prioritizing: Which interrupt is serviced when more than one interrupt occurs.
- Vector Generation: How the interrupt service routine is selected

An interrupt is an asynchronous input to a microprocessor that suspends current program execution and causes a jump to an interrupt service routine. Interrupts are especially useful in real-time systems and have become a standard feature in microprocessor designs.

REASONS FOR USING INTERRUPTS

The use of interrupts generally increases the efficiency of the system. Without interrupts, the microprocessor must poll each peripheral to determine when it is ready for service. The time spent polling cuts down available processing time, and polling is unnecessary when the peripheral devices are not ready for service. With interrupts, the peripheral device informs the processor when it is ready; thus no time is wasted.

Interrupts also provide faster response to service requests from a peripheral. The high data rate of many devices, (e.g. disk drives) requires immediate response to prevent loss of data. As another example, a power-fail interrupt can be used to initiate an orderly shutdown in the remaining moments.

Interrupts can also be used for error handling. If a parity error is detected in the memory, for example, an interrupt can be generated to suspend the operation of the program or invoke an error-handling routine.

INTERRUPT LATCHING

Figure 1 shows a circuit that captures asynchronous events and generates an interrupt to the microprocessor. The 74F533 inverting octal latch is used to "freeze" the state of the interrupt inputs. This is necessary to catch short interrupt request pulses. When all interrupt requests are inactive, the latch enable (LE) input of the 74F533 is asserted. When any request is asserted, the interrupt signal to the microprocessor ($\overline{INT}$) is asserted and the latch is disabled. Thus, the state of the interrupt inputs is latched.

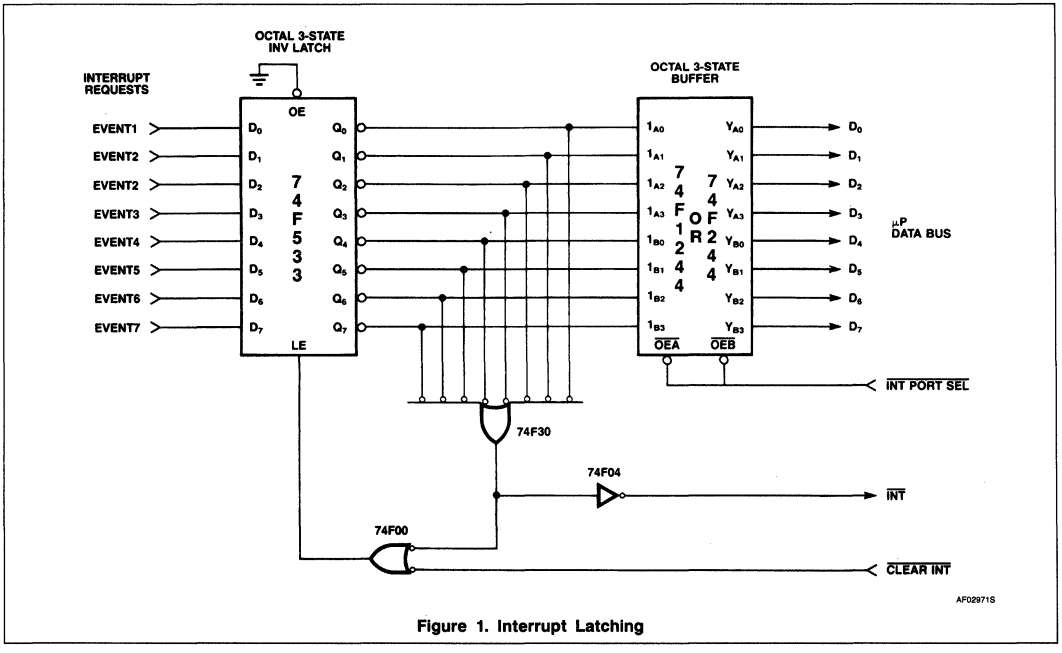

Figure 1. Interrupt Latching

Interrupt Control Logic Using FAST ICs AN208

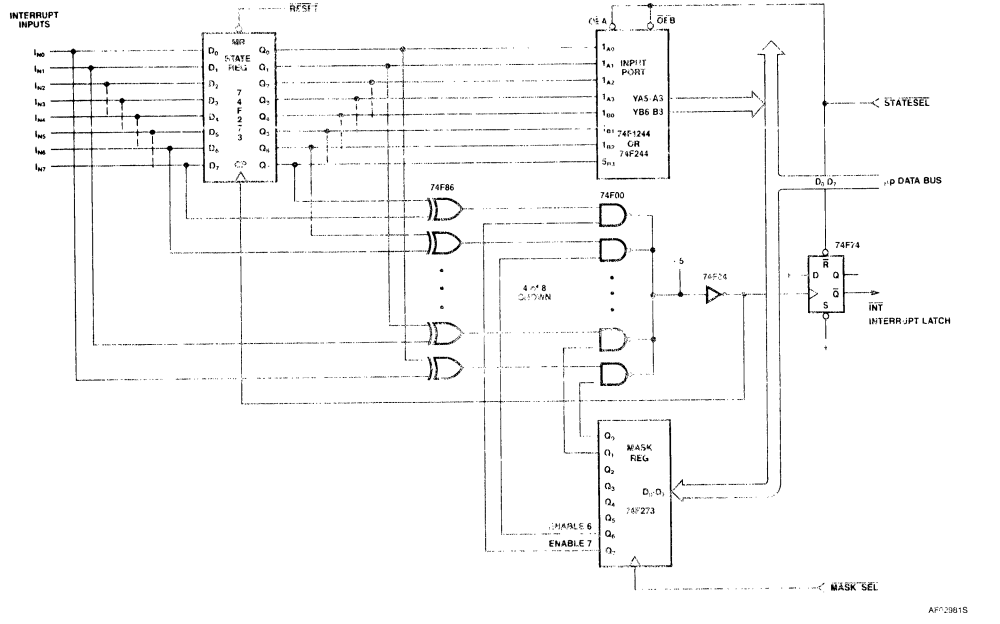

Figure 2. Interrupt Masking

During its interrupt service routine, the microprocessor reads the interrupt latch outputs via the74F1244 or 74F244 octal 3-State buffer to determine which event caused the interrupt. This scheme is most useful with microprocessors such as the 6800 family that do not have vectored interrupts.

At the end of the interrupt service routine, the microprocessor resets the latch by pulsing the /CLEARINT output line. This would typically be generated by decoding a write to a particular address.

INTERRUPT MASKING

Figure 2 shows an interrupt controller that allows each interrupt input to be individually enabled or disabled (masked). A 74F273 octal D flip-flop stores the state of the interrupt inputs whenever any input changes.

Exclusive-OR gates 74F86 compare the inputs of the state register to its outputs; whenever an input changes, the corresponding exclusive-OR gate output goes high.

Another 74F273, connected as an output port, serves as the mask register. The microprocessor writes a bit pattern to this port to determine which interrupts are enabled. The outputs of the exclusive-OR gates are then ANDed with the mask register outputs, so that interrupt inputs with a zero in their mask bit are ignored.

Whenever any unmasked input changes state, the state register is clocked, and the interrupt latch is set. The microprocessor reads the state register via the 74F1244 or 74F244 3-State buffer acting as an input port, and the interrupt latch is cleared.

Caution: This circuit can be fooled if an interrupt input changes twice before the microprocessor reads the state register. Therefore, this design should be used only for relatively slow-changing interrupt inputs.

INTERRUPT PRIORITIZING

In the previous circuits, the hardware does not select which interrupt has highest priority. If two or more interrupts are simultaneously asserted, the microprocessor software must decide which to process first.

Figure 3 shows a circuit with prioritization logic to select the highest priority interrupt. Interrupt inputs are sampled by the 74F377 octal flip-flop. This register is also used to freeze the state of the interrupt inputs when the output of the priority encoder is being read by the microprocessor. If one (or more) interrupt input is asserted, the output of the 74F148 priority encoder will indicate the number of the highest priority active interrupt.

The GS output of the encoder is effectively the OR of all the inputs, and produces the interrupt signal to the microprocessor. The microprocessor then reads the interrupt number via the 74F1244 or 74F244 3-State buffer connected as an input port. The microprocessor can use the interrupt number as an index pointer into a branch table, to access the appropriate service routine.

A 74F138 3-to-8 decoder decodes the interrupt number to generate individual reset signals for each interrupt source. The decoder is enabled when the microprocessor reads the interrupt number, so the interrupt output of the device being serviced is automatically reset.

RESTART VECTOR GENERATION FOR 8080-FAMILY PROCESSORS

The 8080, 8085, NSC800, and Z80 all have interrupt modes in which a vector is automatically read from the interrupting device. (For the 8080, this is the only mode; the other processors also have additional modes.) This vector is treated as an instruction; the single-byte CALL instructions called RESTARTs are

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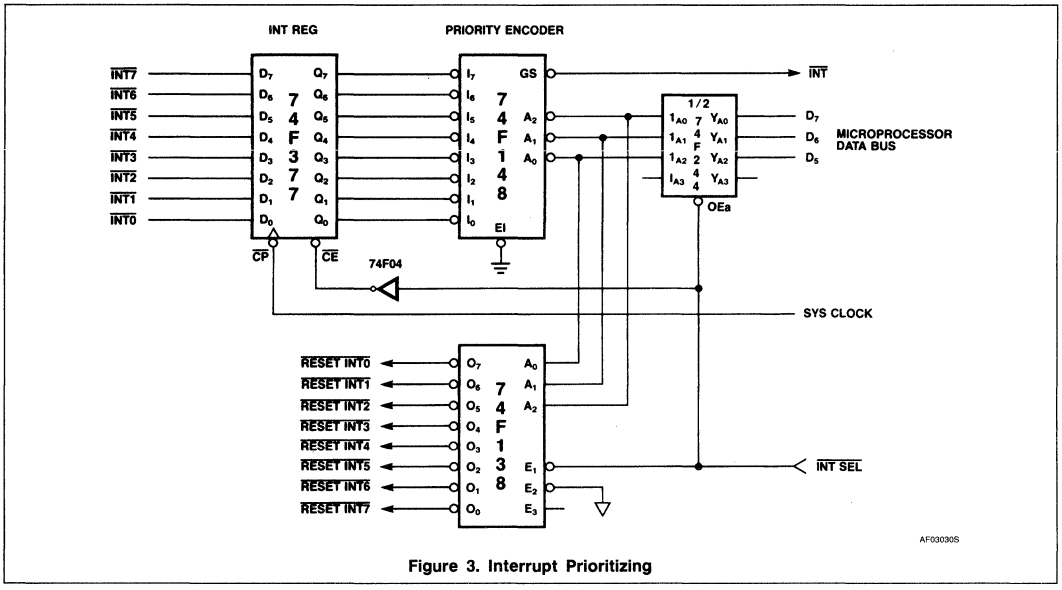

Figure 3. Interrupt Prioritizing

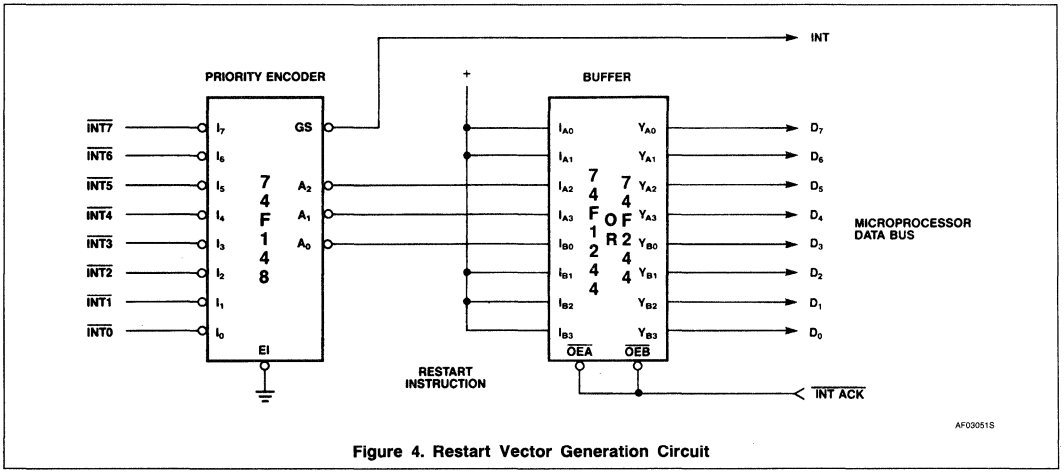

Figure 4. Restart Vector Generation Circuit

generally used for the vectors. The format of the restart instructions is 11CBA111 (binary), where CBA represents the three-bit identifier. Figure 4 illustrates a restart vector generation circuit.

The 74F148 priority encoder generates the interrupt request to the microprocessor when any interrupt input is asserted. It also provides the three-bit identifier to the appropriate inputs of the 74F1244 or 74F244. When the microprocessor performs an interrupt acknowledge cycle, the restart instruction is read via the 74F244 octal buffer. Table 1 shows the vectors generated for each input. Interrupt input 7 produces an identification code of 000, since the priority encoder outputs are active low.

Note that the interrupt inputs are not latched by this circuit, and thus must remain asserted until the interrupt acknowledge cycle is completed.

The Z80 microprocessor has several modes of interrupt operation. The mode described above is called mode 1. Mode 2 is a table-driven mode in which the vector supplied by the peripheral is used as a pointer to a table. The service routine address is then read from the table.

Figure 5 shows a circuit for generating the vectors for Z80 mode 2 interrupts. The 74F148 priority encoder generates a three-bit binary number corresponding to the highest priority active interrupt. This number is read by the microprocessor during the interrupt

Table 1. 8080-Family Interrupt Vector Generation

HIGHEST PRIORITY ACTIVE INPUT	VECTOR GENERATED	INSTRUCTION NAME 8080	Z80
INT7	11000111	RST0	RST 0
INT6	11001111	RST1	RST 8
INT5	11010111	RST2	RST 16
INT4	11011111	RST3	RST 24
INT3	11100111	RST4	RST 32
INT2	11101111	RST5	RST 40
INT1	11110111	RST6	RST 48
INT0	11111111	RST7	RST 56

acknowledge cycle via the 74F244 octal 3-State driver.

Table 2 shows the vectors generated by the circuit. The least significant data input of the 74F1244 or 74F244 is grounded, and the code from the priority encoder provides the next three bits. This is necessary because each interrupt vector must point to a two-byte entry in the service routine address table. The four most significant bits are set by the switches. This allows the same circuit to be used in several places in a system by setting the switches differently on each.

VECTORED INTERRUPTS FOR 6800-FAMILY MICROPROCESSORS

The 6800 microprocessor and its derivatives (6802 and 6502) do not have a built-in mechanism for handling vectored interrupts. When an interrupt occurs, the microprocessor fetches the address of the service routine from memory locations FFF8 and FFF9 (for the 6502, locations FFFE and FFFF). Normally these are ROM locations, and the interrupt service routine address is therefore fixed.

Figure 6 shows a circuit that provides vectored, prioritized interrupts for these microprocessors. When the microprocessor reads from address FFF8 or FFF9, this circuit disables the normal address buffers and substitutes a different address via a second set of 74F1244 or 74F244 octal 3-State drivers. Bits 1, 2 and 3 of the substituted address are determined by the highest priority active interrupt input. Thus, the service routine address is fetched from a different memory location for each interrupt input. The high-order address bits are set by the switches.

Table 2. Interrupt Vectors Generated By Circuit In Figure 5

HIGHEST-PRIORITY ACTIVE INPUT	VECTOR GENERATED (HEX)
INT7	X 0
INT6	X 2
INT5	X 4
INT4	X 6
INT3	X 8
INT2	X A
INT1	X C
INT0	X E

NOTE:
1. X = Switch settings

DAISY CHAIN INTERRUPT PRIORITY SYSTEM

In the previous examples, a priority encoder was used to set the priority of each interrupt source. Another way to set priority is with an interrupt priority daisy chain, as shown in Figure 7. The priority of each device is determined by its physical location in the chain. Support for an interrupt daisy chain is built into the peripheral chips for some microprocessor families, such as the Z80. This example shows how a similar daisy chain can be implemented for other microprocessors such as the 8085 or 68000.

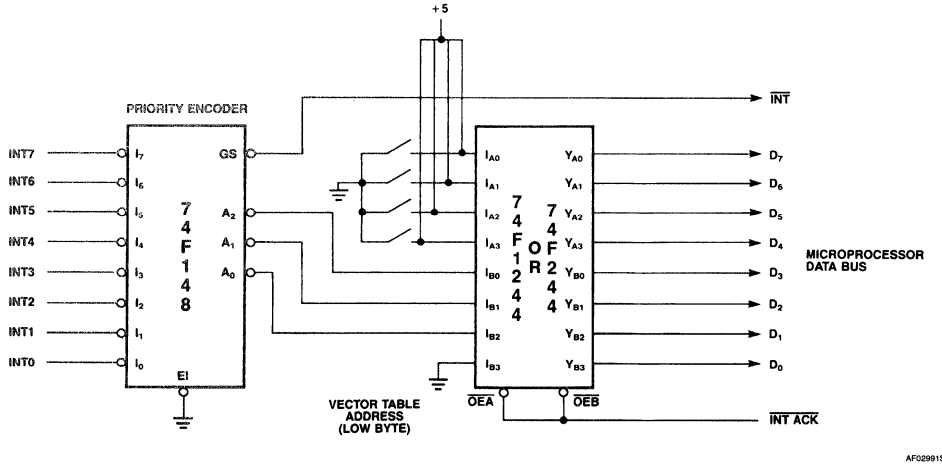

Figure 5. Vector Generation For Two Interrupt Modes

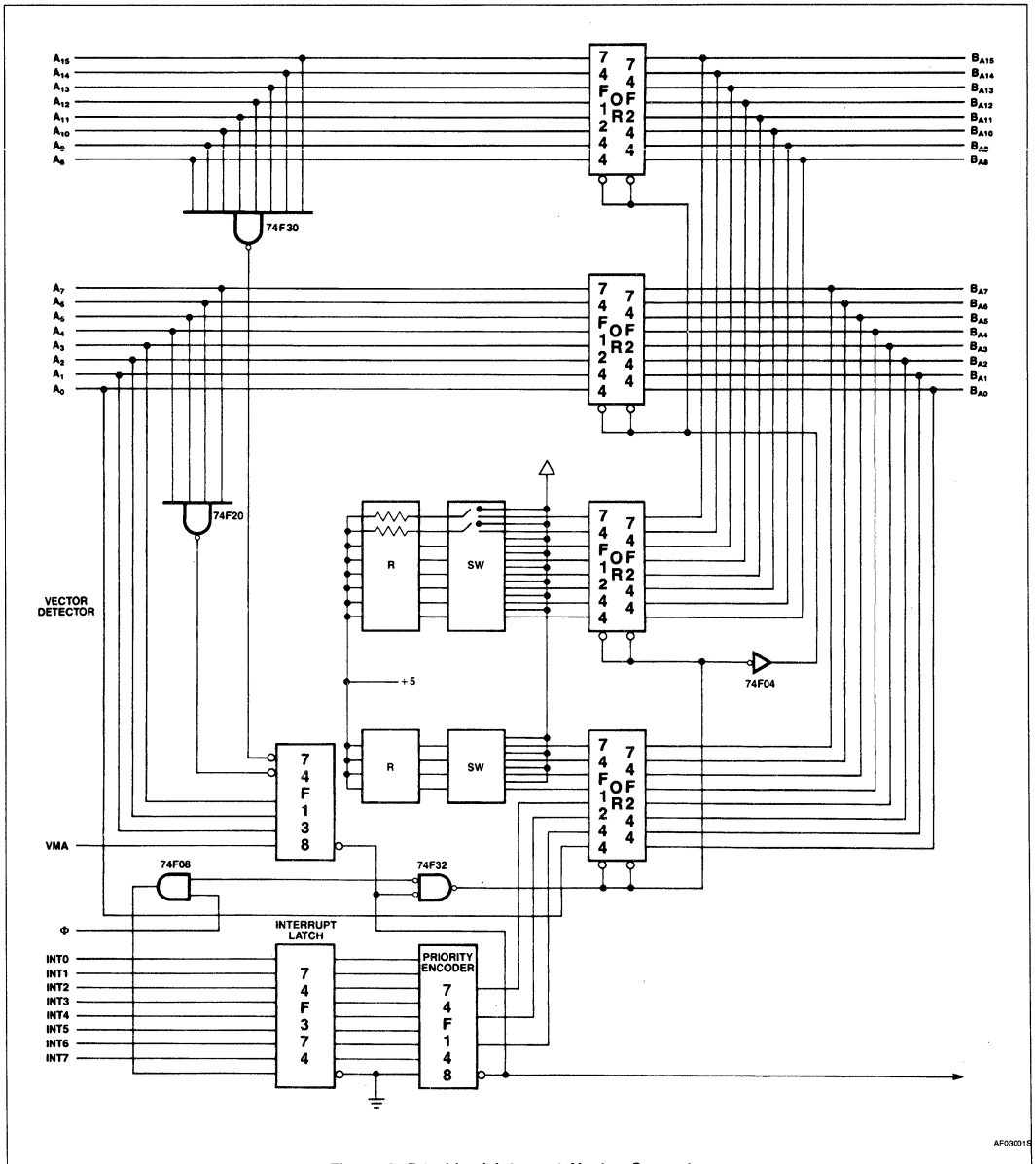

Figure 6. Prioritized Interrupt Vector Generator

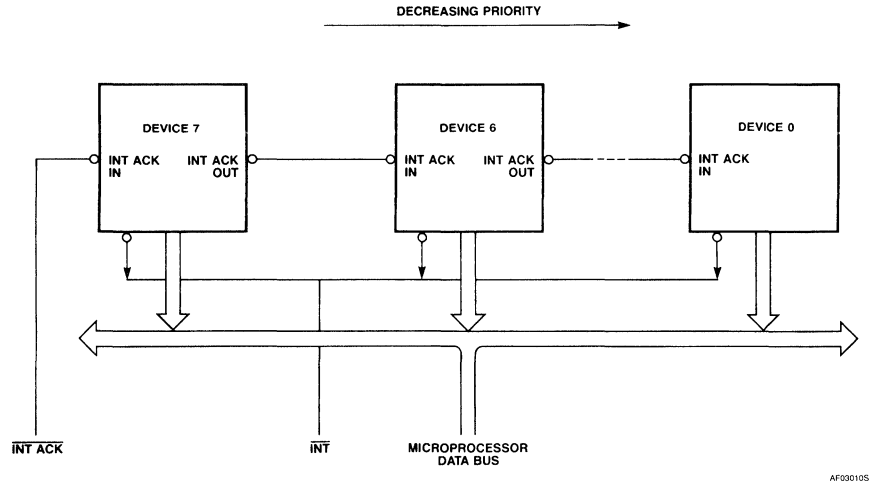

Figure 7. Daisy Chain Interrupt

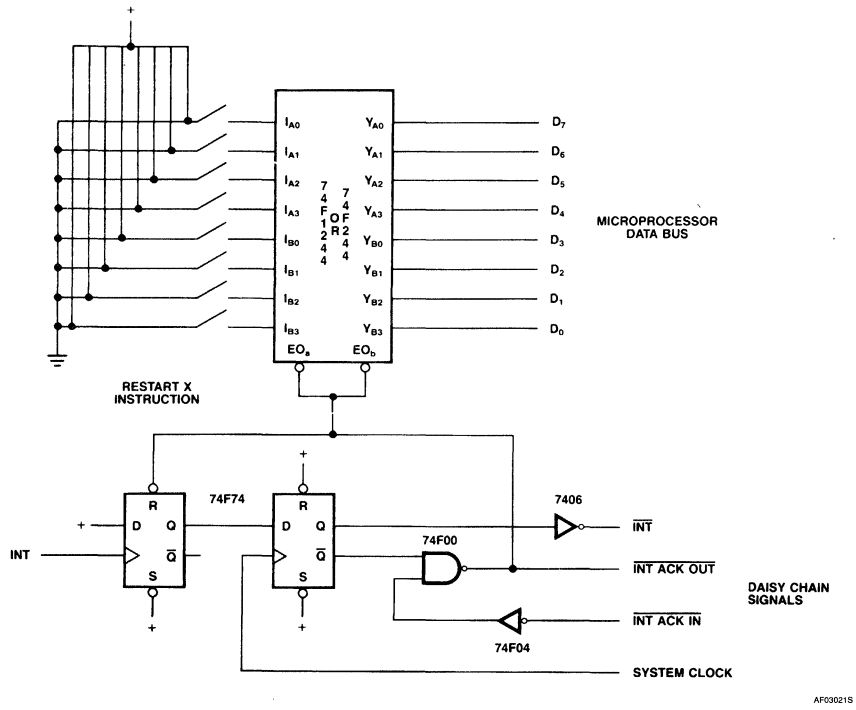

Figure 8. Logic Circuit For Implementation Of Daisy Chain Interrupt

Interrupt Control Logic Using FAST ICs AN208

When one or more device asserts an interrupt, the microprocessor responds by asserting $\overline{\text{INTACK}}$ active. This signal connects directly to the highest priority device's $\overline{\text{INTACK IN}}$ input. If that device had not asserted an interrupt, then it passes the interrupt acknowledge signal to the next device via its $\overline{\text{INTACK OUT}}$ signal. Thus, the interrupt acknowledge is passed along from one device to the next until it reaches the highest priority device that generated an interrupt. That device then places its interrupt vector on the data bus.

Figure 8 shows an implementation of this system. The two 74F74 flip-flops latch the interrupt request and synchronize it with the system clock. The signal at $\overline{\text{INTACK IN}}$ is passed to $\overline{\text{INTACK OUT}}$ unless the interrupt latch is set. The 74F244 drives the interrupt vector (restart instruction) to the data bus when $\overline{\text{INTACK IN}}$ is active and the interrupt latch is set. Switches allow the interrupt instruction to be selected for each device.

68000 INTERRUPT STRUCTURE

The 68000 16-bit microprocessor provides an extremely versatile interrupt structure. There are seven interrupt priority levels with up to 256 different vectors per level. The 68000 has a three-bit interrupt input which specifies the interrupt level. A code of 000 means no interrupt; any other code produces an interrupt, and the level corresponds to the code.

Figure 9 shows the timing diagram for the interrupt acknowledge cycle. When the 68000 recognizes the interrupt, it places the interrupt acknowledge code on the function code outputs $/FC_0 - /FC_2$, and outputs the interrupt level being serviced on address lines A_0, A_1 and A_2. The interrupting device then places the interrupt vector on the data bus from which it is read by the 68000.

Figure 10 shows a circuit that allows the user, under program control, to generate an interrupt of any priority level and to supply any interrupt vector. The program uses a MOVE instruction to output the desired interrupt level and vector. The circuit then generates the interrupt. This allows subroutines to be implemented as interrupt service routines. It is also useful for testing interrupt service routines.

All signals are VERSABUS™ signals, with the exception of INT ADDR* which is the output of the address decoder, and RD/$\overline{\text{WR}}$* which must be derived from the VERSABUS™ control signals. Note that the address and data buses are active low; VERSABUS™ notation is used (active low signal names are followed by an asterisk "*"). DS0* and DS1* are basically the same as the 68000's $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$. IACKIN* and IACKOUT* are priority daisy chain signals as described previously. IPL1* through IPL7* are the seven interrupt signals which are fed through a priority encoder on the CPU board (not shown) to generate the binary-encoded interrupt signals to the 68000.

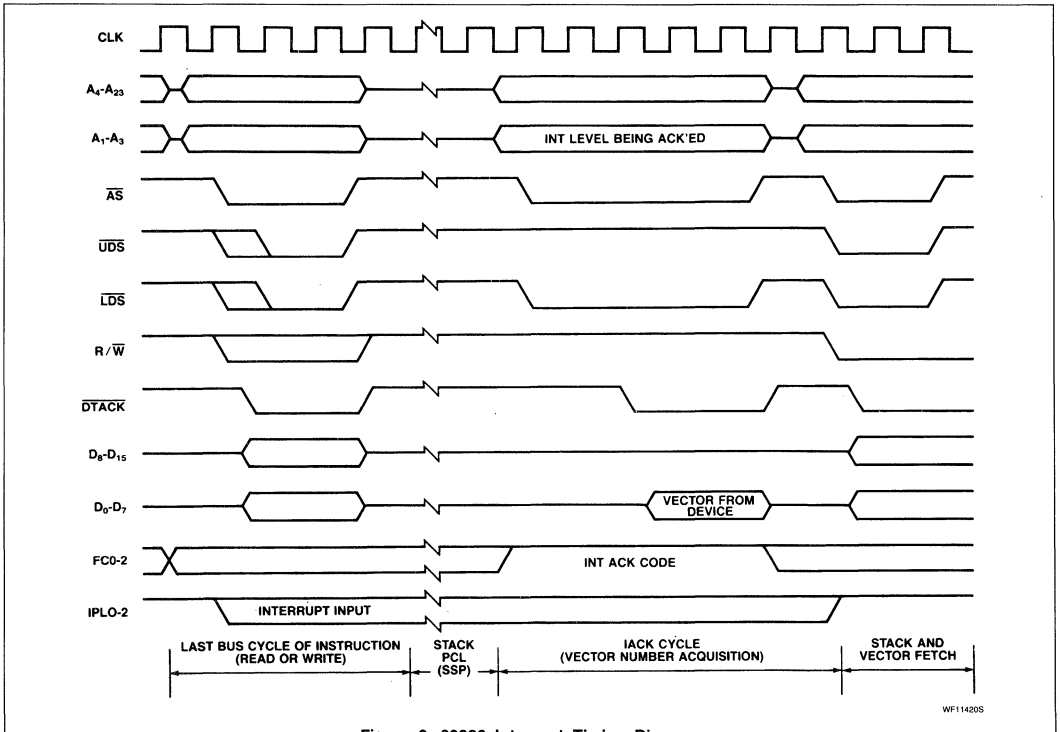

Figure 9. 68000 Interrupt Timing Diagram

Interrupt Control Logic Using FAST ICs AN208

The operation of the circuit is as follows:

- The software performs a move instruction to the address decoded as INTADDR*, with the interrupt vector in $D_0 - D_7$ and the interrupt level in D_8, D_9 and D_A.
- Flip-flop I is set, releasing the clear from the 74F175 priority register C. The new interrupt level is clocked into the register and an interrupt of that level is generated by the 74F138 decoder D.
- At the same time, the interrupt vector is loaded into the 74F373 latch L.
- After an appropriate delay 74F73A flip-flops P and Q generate XACK*, and the cycle completes.

When the 68000 recognizes the interrupt, the following sequence occurs:

- The priority level being serviced, as indicated by the state of A_0, A_1 and A_2, is compared to the contents of the interrupt priority latch C by the 74F85 comparator B. (Note that the $\overline{Q}$ outputs of the 74F175 are used to invert the active low address signals.)
- If the levels match, the interrupt vector is placed on the data bus, XACK* is generated, and the cycle terminates. Flip-flop I is reset, which removes the interrupt by clearing the interrupt request register.

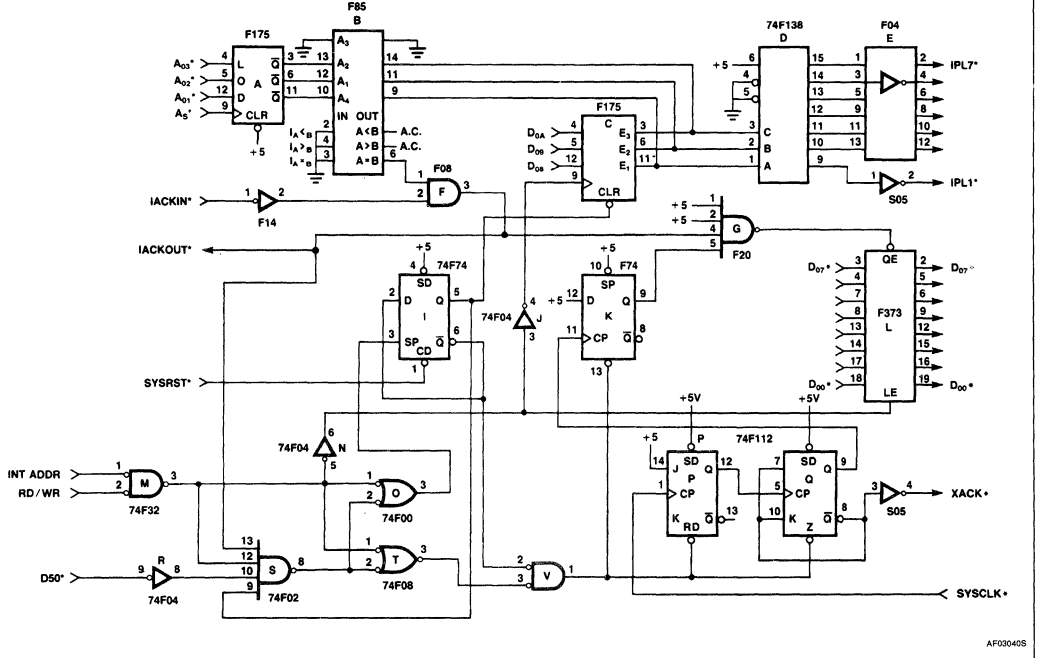

Figure 10. Complete Interrupt Circuit For 68000

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the individuals whose entries were referenced in whole or in part in this note.

Signetics

AN212
Package Lead Inductance Considerations In High-Speed Applications

Logic Products

Application Note

Authors: Stephen C. Hinkle, Jeffrey A. West

INTRODUCTION

As circuits become faster, more concern needs to be focused on packaging and interconnects in order to fully utilize device performance. One area of concern is with the package leads between the chip and the board environment. The current flowing into or out of an integrated circuit is conducted through a lead frame trace and bonding wire connecting the integrated circuit to outside circuitry. These leads are circuit elements, inductors, and have a definite effect on the circuit performance because they generate noise in high-speed applications.

Inductance is the measure of change in the magnetic field surrounding a conductor resulting from the variation of the current flowing through the conductor. The change in current through the inductor induces a counter electromotive force, EMF, which opposes that change in current.

An example is a buffer driver discharging a 50pF load. At a switching rate of about 3V in 2ns, the current generated by discharging that capacitor at that rate is:

$$I = C\frac{dV}{dt} \simeq 50pF * \frac{3v}{2ns} = 75mA.$$

All this current flows through the ground lead of the package. Changing the current through this lead generates a ground lead voltage or ground bounce. A typical lead inductance has been measured to be about 10nH. Switching 75mA through a ground lead with an inductive value of 10nH causes a ground bounce of about:

$$V = L\frac{dI}{dt} \simeq 10nH * \frac{75mA}{1ns} = 750mV.$$

Figure 1 illustrates the current surge and ground bounce during switching. This was modeled using the equations:

$$V(t) = \frac{3V}{1 + e^{(t\text{-}to)/K}}$$

$$I_C(t) = C\frac{dV(t)}{dt}$$

$$V_L(t) = L\frac{dI_C(t)}{dt} = LC\frac{d^2V(t)}{dt^2}$$

If more than one output is switched at a time this ground bounce can get very large. Changing the ground reference on the chip can have significant effects on circuit performance. A V_{CC} bounce can also be calculated when the 50pF load capacitors are being charged and can also have serious effects on circuit performance.

Some of the problems caused by package lead inductance are:

1. Adding delay through buffer parts.
2. Changing the state of flip-flop parts.
3. Output glitching on unswitched outputs.
4. Circuit oscillations.

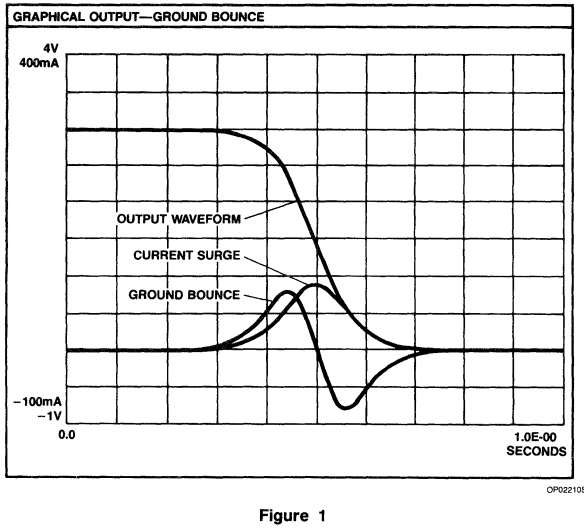

Figure 1

GENERAL PROBLEMS ASSOCIATED WITH GROUND BOUNCE IN HIGH-SPEED CIRCUITS

Adding Delay Through Buffer Parts

Delay through a buffer part is not only a function of the gate itself but is also a function of how many gates in the package are switching at once. Switching more than one output at a time adds to the current being forced through the ground lead of the package. The ground potential seen by the chip rises because of the lead inductance. This rise in ground potential raises the threshold of the gate and tends to turn the gate back off slowing the discharge rate of the load capacitor. The gate doesn't finish switching until the ground bounce settles out.

Package Lead Inductance Considerations In High-Speed Applications

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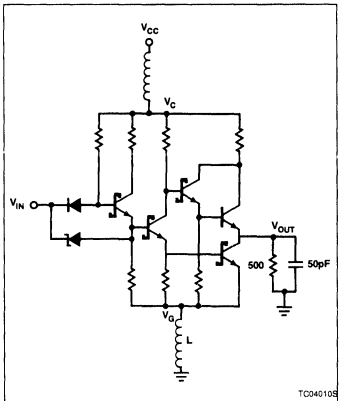

Figure 2

Figure 2 shows an example of a buffer connected to a test load. Probing on the ground pad, V_G, shows the effect ground lead inductance has on the ground pad potential.

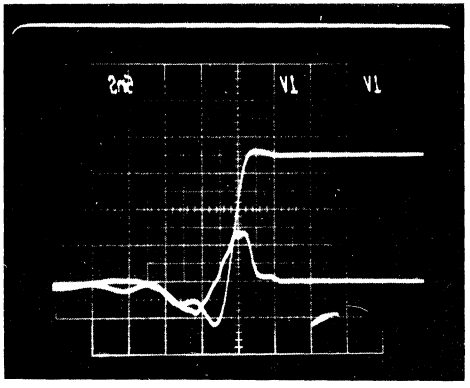

Figure 3

Figures 3 and 4 show the ground and V_{CC} bounce during switching on an 'F240 Buffer. The effect of ground bounce on this part is to slow the propagation delays from 3ns with only one output switching to 5ns with all 8 outputs switching at once. AC specifications are usually generated with only one gate switching at a time. For example the 'F240 T_{PHL} limits are 2.0ns minimum, 3.5ns typical and 4.7ns maximum. Therefore when using AC specifications based on single gate switching, a derating factor for multiple switching should be used. A derating factor of 250 to 300ps per output switching has been suggested as a reasonable number and some customers are using this in their internal specifications.

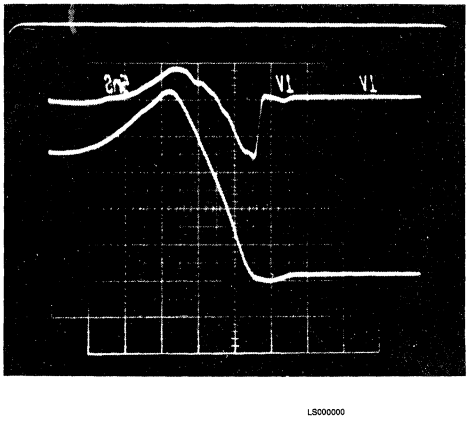

Figure 4

Integrated Circuits Containing Flip-Flops

Integrated circuits containing flip-flops might be seriously affected by inductive ground bounce because of the possibility of the flip-flops changing states. To explore this effect, the 'F374, an Octal D-type flip-flop, was analyzed by comparing test results from the conventional corner mount V_{CC} and ground package to that of a side mount V_{CC} and ground version. A test set-up was used where alternate 1's and 0's were clocked into seven of the eight flip-flops to obtain simultaneous output switching and worst case ground bounce. The eighth flip-flop input was held at a DC bias of 2.0V. This should result in its output being held at a constant 1 level.

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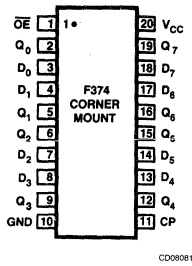
Package Lead Inductance Considerations In High-Speed Applications



74F374 Failure Analysis

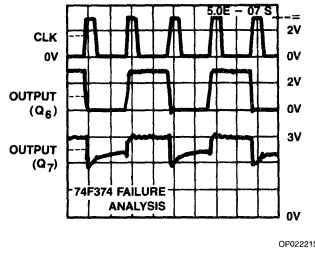
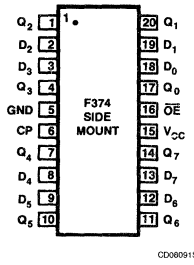


Figure 5



74F374XL

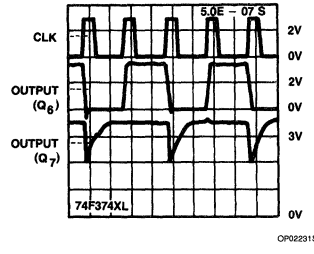


Figure 6

Figure 5 shows the corner mount results. The ground bounce is sufficient to couple the output of the eighth flip-flop (Q_7) to less than 2.0V during the transition of the other seven outputs represented by Q_6. The output then charges to a marginal V_{OH} level.

Figure 6 shows the results from the side mount version. Output glitching during the transition of the other seven outputs is still present, but due to the approximately 50% reduction in lead inductance over the corner mount version the output is allowed to charge back to its original V_{OH} level.

Output Glitching During Multiple Switching

In some cases the effects of ground bounce can be minimized if properly taken into consideration during the design and layout of the integrated circuit. Note in Figure 7 the glitch that was present on the output of the 'F11, a triple 3-input AND gate, during an early transition of the other two outputs. A newer version of the 'F11 is shown in Figure 8. Note that the glitch has been greatly minimized.

Circuit Oscillations

A fourth area of concern is the possibility of circuit oscillations during slow input transitions through threshold. This would be of importance if the delay through the part is on the order of the natural period of oscillations of the ground inductance and the load capacitance.

During testing, a particular problem has been seen when the inputs are driven by a power supply by way of a cable. Because there is a delay through the cable, it takes time for the power supply to sense a change in the impedance at the input near threshold. This delay sets up oscillations between the power supply and the input of the part when the input is held near threshold.

Inductance Measurements And Verification

To verify that lead inductance caused these problems, the lead inductance was measured and circuit simulations done to show circuit behavior. Measurement of lead inductance was accomplished using an HP S-parameter test set. These measured values of lead inductance were used in a circuit simulation program. The results of the simulation show voltage and current wave forms similar to the measured waveforms.

Package Lead Inductance Considerations In High-Speed Applications

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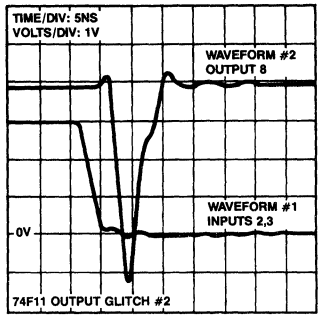

Figure 7

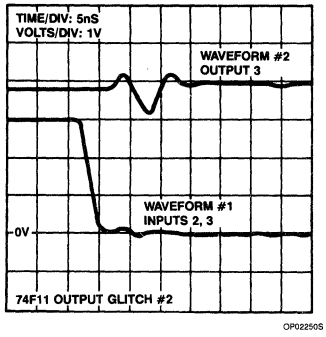

Figure 8

Derivation of the S-parameter Method

The general form for voltage and current along a transmission line is:

$\bar{V}(z) = V^+ e^{-\gamma z} + V^- e^{\gamma z}$

$\bar{I}(z) = I^+ e^{-\gamma z} - I^- e^{\gamma z}$

Where V^+, V^-, I^+, I^- are constants, usually complex, determined by the boundary conditions, z is the distance from the load and gamma (γ) is a complex term involving a real or loss term and an imaginary or phase shift term.

$\gamma = \alpha + j\beta$

$\gamma \simeq 1/2(R\sqrt{C/L} + G\sqrt{L/C}) + j\omega\sqrt{LC}.$

Considering the lossless case where R = 0 and G = 0, $\gamma = j\beta$ and only results in a phase shift. The equations for voltage and current then become,

$\bar{V}(z) = V^+ e^{-j\beta z} + V^- e^{j\beta z}$

$\bar{I}(z) = I^+ e^{-j\beta z} - I^- e^{j\beta z}$

To find Z_1 set z = O. (See Figure 9).

$\bar{Z}_1 = \bar{V}_1/\bar{I}_1 = (V^+ + V^-)/(I^+ - I^-)$

since, $I^+ = V^+/Z_0$ and,

$I^- = V^-/Z_0$,

$\bar{Z}_1 = (V^+ + V^-)/(V^-/Z_0 - V^+/Z_0)$, or,

$$\bar{Z}_1 = Z_0 \frac{1 + V^-/V^+}{1 - V^-/V^+}$$

V^-/V^+ is called the reflection coefficient and is usually complex,

$\Gamma = V^-/V^+$.

The impedance at the load then becomes,

$$\bar{Z}_1 = Z_0 \frac{1 + \Gamma}{1 - \Gamma}$$

On the S-parameter test set, the magnitude of the reflection coefficient, $|\Gamma|$, is measured in dB at a particular angle,

$\Gamma_{real} = 10^{(|\Gamma_{dB}|/20)} \angle \theta.$

For an inductor,

$$\bar{Z}_1 = Z_0 \frac{1 + \Gamma}{1 - \Gamma} = R + j\omega L ,$$

usually $R \simeq 0$ and L can be solved for directly.

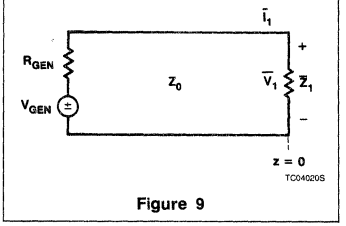

Figure 9

7

Package Lead Inductance Considerations In High-Speed Applications

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Table 1

PACKAGE	REFLECTION COEFFICIENT	INDUCTANCE
16-pin		
8 to 16	−0.50 ∠ 162°C	25.62nH
4 to 12	−0.32 ∠ 172°C	11.51nH
24-pin		
12 to 24	−0.56 ∠ 157°C	32.78nH
6 to 18	−0.29 ∠ 157°C	18.33nH
24-pin skinny		
12 to 24	−0.47 ∠ 160°C	28.39nH
6 to 18	−0.34 ∠ 170°C	14.27nH

Example

A 16-pin package measuring from pin 8 to 16 has a reflection coefficient $\Gamma_{dB} = -0.5 \angle 162°$, Z_0 of the system is 50Ω and the measurement frequency is 50MHz.

$$\Gamma_{dB} = -0.5 \angle 162°$$

$$\Gamma_{real} = 0.944 \angle 162° = -0.898 + j0.292$$

$$\overline{Z}_1 = Z_0 \frac{1+\Gamma}{1-\Gamma} = 50^* \frac{0.102+j0.292}{1.898-j0.292}$$

$$= 50^* \frac{0.309 \angle 70.7°}{1.920 \angle -8.74°}$$

$$= 8.05 \angle 79°$$

$$\overline{Z}_1 = 1.475 + j7.914$$

$L = 7.914/(2\pi^*50\text{MHz}) = \underline{25.19\text{nH}}$.

Alternately, using the approximation R = 0, so $|Z_1| = \omega L$:

$$L = \frac{8.05}{2\pi^*50\text{MHz}} = \underline{25.62\text{nH}}$$

Three packages were used to measure lead inductance, a 16-pin CERDIP, a 24-pin CERDIP and a 24-pin skinny CERDIP. V_{CC} and ground were double bonded to an 80 × 80 mil blank die. Table 1 shows the results of the measurements.

These values are the total inductance V_{CC} to ground. Each lead inductance would be about one half these members.

Simulation of Measured Values

Both ground and V_{CC} bounce for the 'F240 were simulated using the inductive values measured. The results were similar to the measured data of the 'F240, Figures 3 and 4. The simulation of the 'F240 is shown in Figure 10. This shows the pad V_{CC}, the pad ground (V_G) and the inputs (V_{IN}) and outputs (V_{OUT}) when all 8 buffers are switched simultaneously.

SUMMARY

A major contributor to noise in high-speed circuits is package lead inductance. Integrated circuits are packaged with lead frame traces and bonding wire. These leads act as inductors. Voltage generated across these leads follow the law:

$$V = L \frac{di}{dt}$$

This represents noise to an integrated circuit chip and can cause performance degradation. The faster the switching rates become, the more lead inductance can affect circuit performance.

As circuits become faster, more care should be taken in packaging and chip layout. In some cases like the 'F11, a better layout can help remove potential problems but in most cases like the 'F240, the noise is strictly a function of the package. Care should be taken in integrated circuit packages to minimize lead lengths. Side mount V_{CC} and ground pins, smaller packages such as the surface mounted SO, and high levels of board integration are a few possibilities which would help minimize lead lengths.

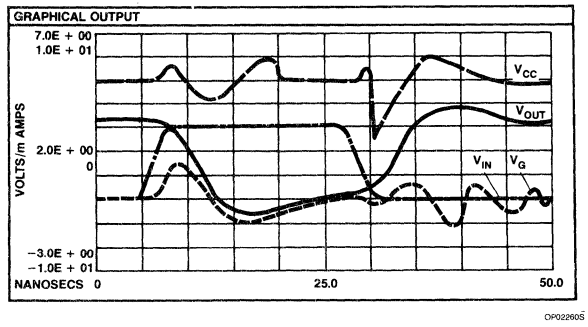


Figure 10

Signetics

AN SMD-100
Thermal Considerations For Surface Mounted Devices

Application Note

INTRODUCTION

Thermal characteristics of integrated circuit (IC) packages have always been a major consideration to both producers and users of electronics products. This is because an increase in junction temperature (T_J) can have an adverse effect on the long term operating life of an IC. As will be shown in this paper, the advantages realized by miniaturization can often have trade-offs in terms of increased junction temperatures. Some of the **VARIABLES affecting T_J are controlled by the PRODUCER of the IC, while others are controlled by the USER and the ENVIRONMENT in which the device is used.**

With the increased use of Surface Mount Device (SMD) technology, management of thermal characteristics remains a valid concern because not only are the SMD packages much smaller, but the thermal energy is concentrated more densely on the printed wiring board (PWB). For these reasons, the designer and manufacturer of surface mount assemblies (SMAs) must be more aware of all the variables affecting T_J.

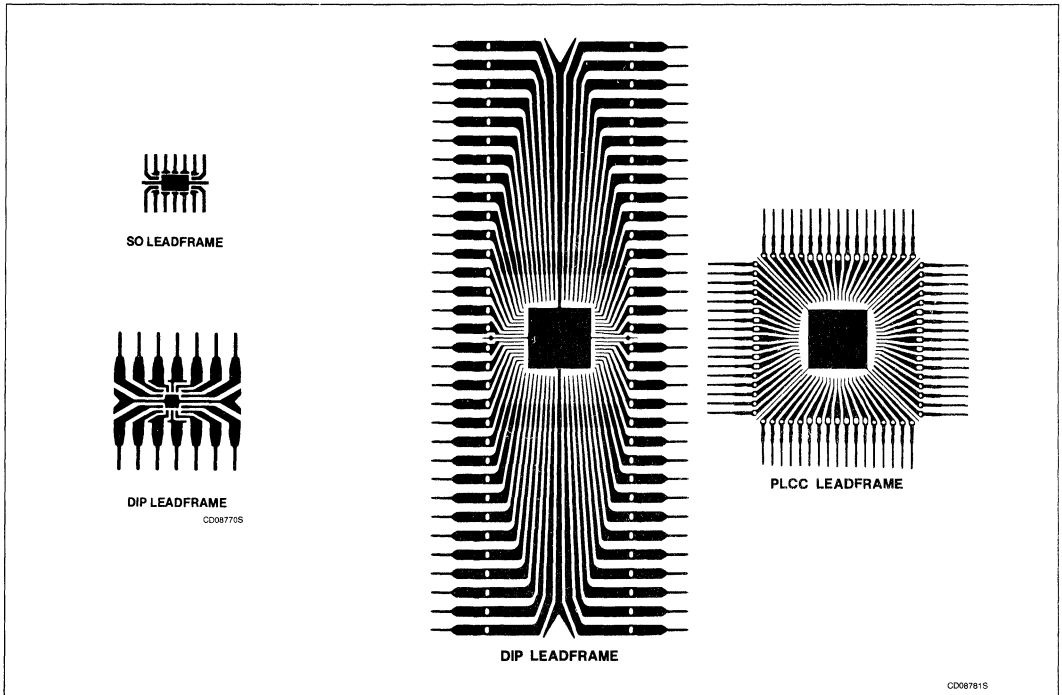
POWER DISSIPATION

Power dissipation (P_D), varies from one device to another and can be obtained by multiplying V_{CC} Max by typical I_{CC}. Since I_{CC} decreases with an increase in temperature, maximum I_{CC} values are not used.

THERMAL RESISTANCE

The ability of the package to conduct this heat from the chip to the environment is expressed in terms of thermal resistance. The term normally used is Theta JA (θ_{JA}). θ_{JA} is often separated into two components: thermal resistance from the junction to case, and the thermal resistance from the case to ambient. θ_{JA} represents the total resistance to heat flow from the chip to ambient and is expressed as follows:

$$\theta_{JC} + \theta_{CA} = \theta_{JA}$$



a. SO-14 Leadframe Compared to a 14-Pin DIP Leadframe

b. PLCC-68 Leadframe Compared to a 64-Pin DIP Leadframe

Figure 1

7

Thermal Considerations For Surface Mounted Devices

AN SMD-100

JUNCTION TEMPERATURE (T_J)

Junction temperature (T_J) is the temperature of a powered IC measured by Signetics at the substrate diode. When the chip is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A). T_J is calculated by multiplying the power dissipation of the device by the thermal resistance of the package and adding the ambient temperature to the result.

$$T_J = (P_D \times \theta_{JA}) + T_A$$

FACTORS AFFECTING θ_{JA}

There are several factors which affect the thermal resistance of any IC package. Effective thermal management demands a sound understanding of all these variables. Package variables include the leadframe design and materials, the plastic used to encapsulate the device, and to a lesser extent other variables such as the die size and die attach methods. Other factors that have a significant impact on the θ_{JA} include the substrate upon which the IC is mounted, the density of the layout, the air-gap between the package and the substrate, the number and length of traces on the board, the use of thermally conductive epoxies, and external cooling methods.

PACKAGE CONSIDERATIONS

Studies with dual-in-line plastic (DIP) packages over the years have shown the value of proper leadframe design in achieving minimum thermal resistance. SMD leadframes are smaller than their DIP counterparts (see Figures 1a and 1b). Because the same die is used in each of the packages, the die-pad, or flag, must be at least as large in the SO as in the DIP.

While the size and shape of the leads have a measurable effect on θ_{JA}, the design factors that have the most significant effect are the die-pad size and the tie-bar size. With design constraints caused by both miniaturization and the need to assemble packages in an automated environment, the internal design of an SMD is much different than in a DIP. However, the design is one that strikes a balance between the need to miniaturize, the need to automate the assembly of the package, and the need to obtain optimum thermal characteristics.

LEAD FRAME MATERIAL is one of the more important factors in thermal management. For years the DIP leadframes were constructed out of Alloy-42. These leadframes met the producers' and users' specifications in quality and reliability. However three to five years ago, the leadframe material of DIPs was changed from Alloy-42 to Copper (CLF) in order to provide reduced θ_{JA} and extend the reliable temperature-operating range. While this change has already taken place for the DIP, it is still taking place for the SO package. Signetics began making 14-pin SO packages with CLF in April 1984 and completed conversion to CLF for all SO packages by 1985. As is shown in Figures 10 through 14, the change to CLF is producing dramatic results in the θ_{JA} of SO packages. All PLCCs are assembled with copper leadframes.

The MOLDING COMPOUND is another factor in thermal management. The compound used by Signetics and Philips is the same high purity epoxy used in DIP packages (at present, HC-10, Type II). This reduces corrosion caused by impurities and moisture.

OTHER FACTORS often considered are the die size, die attach methods, and wire bonding. Tests have shown that die size has a minor effect on θ_{JA} (see Figures 10 through 14).

While there is a difference between the thermal resistance of the silver-filled adhesive used for die attach and a gold silicon eutectic die attach, the thickness of this layer (1 – 2 mils) is so small as to make the difference insignificant.

Gold wire bonding in the range of 1.0 to 1.3 mils does not provide a significant thermal path in any package.

In summary, the SMD leadframe is much smaller then in a DIP and, out of necessity, is designed differently; however, the SMD package offers an adequate θ_{JA} for all moderate power devices. Further, the change to CLF will reduce the θ_{JA} even more, lowering the T_J and providing an even greater margin of reliability.

SIGNETICS' THERMAL RESISTANCE MEASUREMENTS — SMD PACKAGES

The graphs illustrated in this application note show the thermal resistance of Signetics' SMD devices. These graphs give the relationship between θ_{JA} (junction-to-ambient) or θ_{JC} (junction-to-case) and the device die size. Data is also provided showing the difference between still air (natural convection cooling) and air flow (forced cooling) ambients. All θ_{JA} tests were run with the SMD device soldered to test boards (See the Test Ambient section for details). It is important to recognize that the test board is an essential part of the test environment and that boards of different sizes, trace layouts or compositions may give different results from this data. Each SMD user should compare their system to the Signetics test system and determine if the data is appropriate or needs adjustment for their application.

Test Method

Signetics uses what is commonly called the TSP (temperature sensitive parameter) method. This method meets MIL-STD 883C, Method 1012.1. The basic idea of this method is to use the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power dissipation. The thermal resistance can be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{T_J - T_A}{P_D}$$

Test Procedure

TSP Calibration

The TSP diode is calibrated using a constant temperature oil bath and constant current power supply. The calibration temperatures used are typically 25°C and 75°C and are measured to an accuracy of ±0.1°C. The calibration current must be kept low to avoid significant junction heating, data given in this report used constant currents of either 1.0mA or 3.0mA. The temperature coefficient (K-Factor) is calculated using the following equation:

$$K = \frac{T_2 - T_1}{V_{F2} - V_{F1}} \quad \Big| \quad I_F = \text{Constant}$$

Where: K = Temperature Coefficient (°C/mV)
T_2 = Higher Test Temperature (°C)
T_1 = Lower Test Temperature (°C)
V_{F2} = Forward Voltage at I_F and T_2
V_{F1} = Forward Voltage at I_F and T_1
I_F = Constant Forward Measurement Current
(See Figure 2)

Thermal Resistance Measurement

The thermal resistance is measured by applying a sequence of constant current and constant voltage pulses to the device under test. The constant current pulse (same current at which the TSP was calibrated) is used to measure the forward voltage of the TSP. The constant voltage pulse is used to heat the part. The measurement pulse is very short

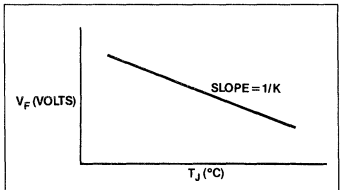


Figure 2. Forward Voltage — Junction Temperature Characteristics of a Semiconductor Junction Operating at a Constant Current. The K Factor is the Reciprocal of the Slope

(less than 1% of cycle) compared to the heating pulse (greater than 99% of cycle) to minimize junction cooling during measurement. This cycle starts at ambient temperature and continues until steady-state conditions are reached. The thermal resistance can then be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{K\ (V_{FA} - V_{FS})}{V_H \times I_H}$$

Where: V_{FA} = Forward Voltage of TSP at Ambient Temperature (mV)
V_{FS} = Forward Voltage of TSP at Steady-State Temperature (mV)
V_H = Heating Voltage (V)
I_H = Heating Current (A)

Test Ambient

θ_{JA} Tests

All θ_{JA} test data collected in this application note was obtained with the SMD devices soldered to either Philips SO Thermal Resistance Test Boards or Signetics PLCC Thermal Resistance Test Boards with the following parameters:

Board size - SO Small: 1.12″ × 0.75″ × 0.059″
- SO Large: 1.58″ × 0.75″ × 0.059″
- PLCC: 2.24″ × 2.24″ × 0.062″

Board Material - Glass epoxy, FR-4 type with 1 oz. sq.ft. copper solder coated

Board Trace Configuration - See Figure 3.

SO devices are set at 8 – 9 mil stand-off and SO boards use one connection pin per device lead. PLCC boards generally use 2 – 4 connection pins regardless of device lead count. Figure 5 shows a cross-section of an SO part soldered to test board and Figure 4 shows typical board/device assemblies ready for θ_{JA} Test.

The still air tests were run in a box having a volume of 1 cubic foot of air at room temperature. The air flow tests were run in a 4″ × 4″ cross-section by 26″ long wind tunnel with air at room temperature. All devices were soldered on test boards and held in a horizontal test position. The test boards were held in a Textool ZIF socket with 0.16″ stand-off. Figure 6 shows the air flow test setup.

θ_{JC} Tests

The θ_{JC} test is run by holding the test device against an "infinite" heat sink (water cooled block approximately 4″ × 7″ × 0.75″) to give a θ_{CA} (case-to-ambient) approaching zero. The copper heat sink is held at a constant temperature (≈20°C) and monitored with a thermocouple (0.040″ diameter sheath, grounded junction type K) mounted flush with heat sink surface and centered below die in the test device. Figure 7 shows the θ_{JC} test mounting for a PLCC device.

SO devices are mounted with the bottom of the package held against the heat sink. This is achieved by bending the device leads straight out from the package body. Two small wires are soldered to the appropriate leads for tester connection. Thermal grease is used between the test device and heat sink to assure good thermal coupling.

PLCC devices are mounted with the top of the package held against the heat sink. A small spacer is used between the hold-down mechanism and PLCC bottom pedestal. Small hook up wires and thermal grease are used as with the SO setup. Figure 7 shows the PLCC mounting.

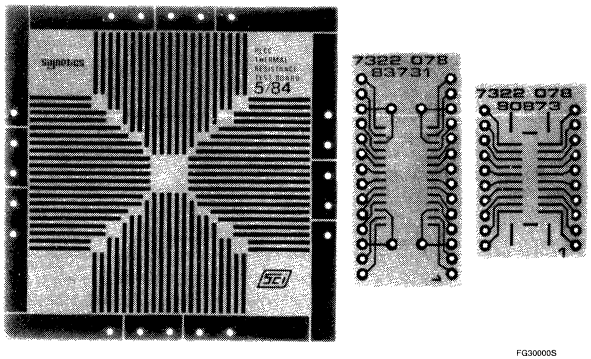


Figure 3. Board Trace Configuration for Thermal Resistance Test Boards

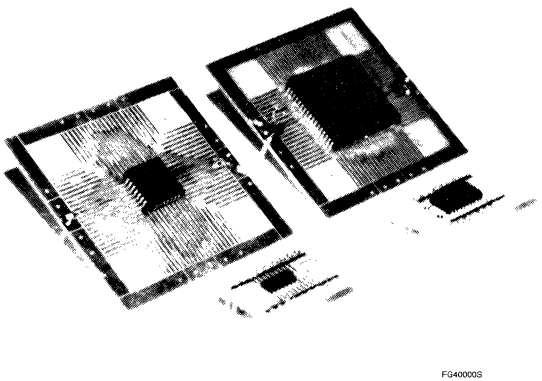


Figure 4. Device/Board Assemblies

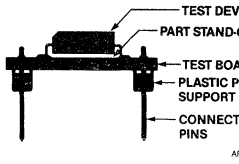
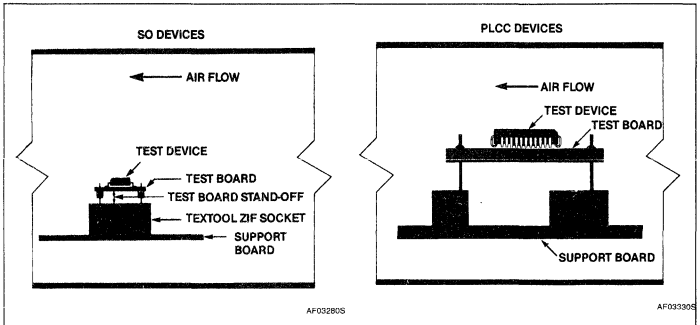


Figure 5. Cross-Section of Test Device Soldered to Test Board

Thermal Considerations For Surface Mounted Devices

AN SMD-100



SO Devices PLCC Devices

Figure 6. Air Flow Test Setup

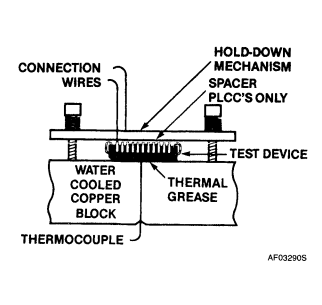


Figure 7. θ_{JC} Test Setup With PLCC Device

DATA PRESENTATION

The data presented in this application note was run at constant power dissipation for each package type. The power dissipation used is given under Test Conditions for each graph. Higher or lower power dissipation will have a slight effect on thermal resistance. The general trend of thermal resistance decreasing with increasing power is common to all packages. Figure 8 shows the average effect of power dissipation on SMD θ_{JA}.

Thermal resistance can also be affected by slight variations in internal leadframe design such as pad size. Larger pads give slightly lower thermal resistance for the same size die. The data presented represents the typical Signetics leadframe/die combinations with large die on large pads and small die on small pads. The effect of leadframe design is within the ±15% accuracy of these graphs.

SO devices are currently available in both copper or alloy 42 leadframes; however, Signetics is converting to copper only. PLCC devices are only available using copper leadframes.

The average lowering effect of air flow on SMD θ_{JA} is shown in Figure 9.

Thermal Calculations

The approximate junction temperature can be calculated using the following equation:

$$T_J = (\theta_{JA} \times P_D) + T_A$$

Where: T_J = Junction Temperature (°C)
θ_{JA} = Thermal Resistance Junction-to-Ambient (°C/W)
P_D = Power Dissipation at a T_J ($V_{CC} \times I_{CC}$) (W)
T_A = Temperature of Ambient (°C)

Example: Determine approximate junction temperature of SOL-20 at 0.5W dissipation using 10,000 sq. mil die and copper leadframe in still air and 200 LFPM air flow ambients. Given $T_A = 30°C$,

1. Find θ_{JA} for SOL-20 using 10,000 sq. mil die and copper leadframe from typical θ_{JA} data —SOL-20 graph.
   Answer: 88°C/W @ 0.7W
2. Determine θ_{JA} @ 0.5W using Average Effect of Power Dissipation on AMD θ_{JA}, Figure 8.
   Percent change in Power =

$$\frac{0.5W - 0.7W}{0.7W} \times 100 = -28.6\%$$

   From Figure 8:
   28.6% change in power gives 3.5% increase in θ_{JA}
   Answer:
   88°C/W + (88 × 0.035) = 91°C/W @ 0.5W
3. Determine θ_{JA} @ 0.5W in 200 LFPM air flow from Average Effect of Air Flow on SMD θ_{JA}, Figure 9.
   From Figure 9:
   200 LFPM air flow gives 14% decrease in θ_{JA}
   Answer:
   91°C/W – (91 × 0.14)
   = 78°C/W
4. Calculate approximate junction temperature
   Answer:
   T_J (still air) = (91°C/W × 0.5W) + 30 = 76°C
   T_J (200 LFPM) = (78°C/W × 0.5W) + 30 = 69°C

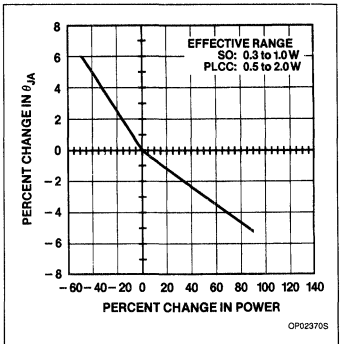


Figure 8. Average Effect of Power Dissipation on SMD θ_{JA}

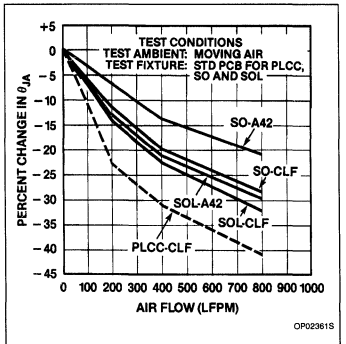
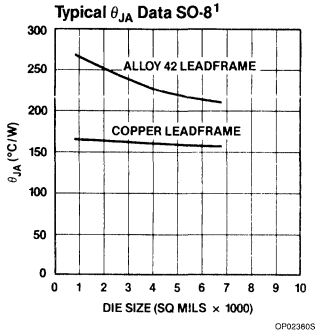
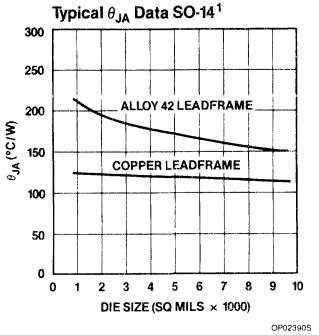
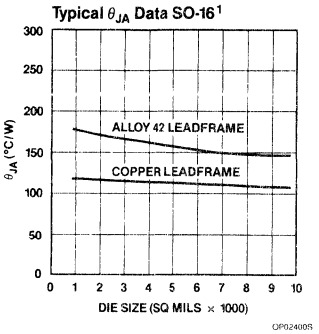


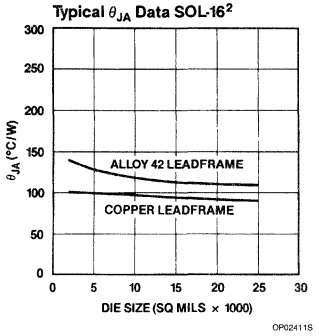
Figure 9. Average Effect of Air Flow on SMD θ_{JA}

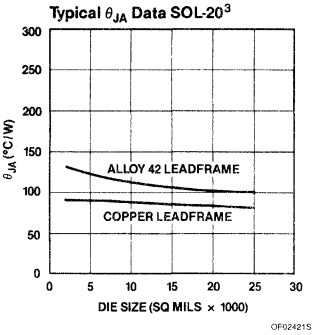
TYPICAL SMD THERMAL (θ_{JA})

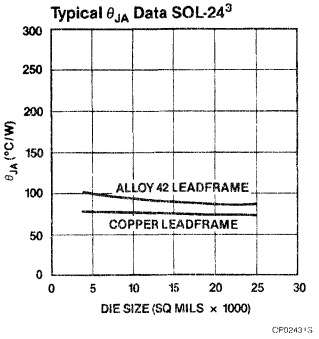


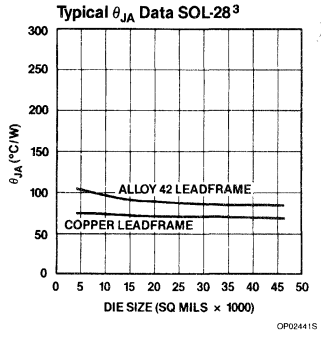












NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.12" × 0.75" × 0.059")
Accuracy:	±15%

2. TEST CONDITIONS:

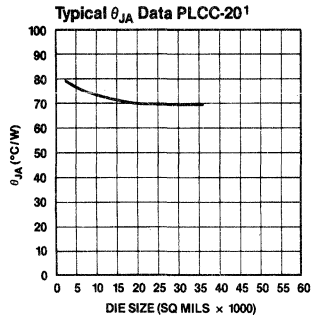
Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")
Accuracy:	±15%

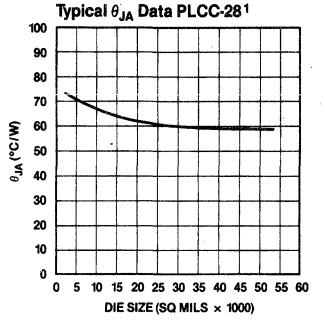
3. TEST CONDITIONS:

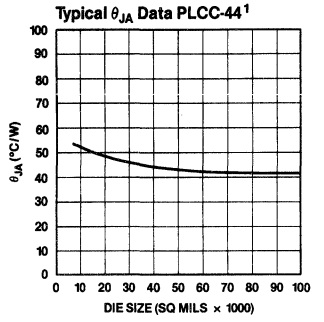
Test ambient:	Still air
Power dissipation:	0.7W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")
Accuracy:	±15%

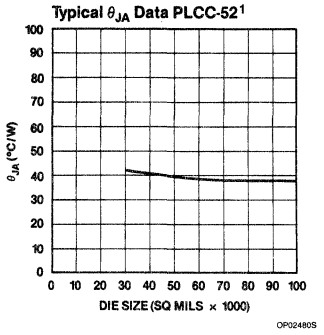
Figure 10

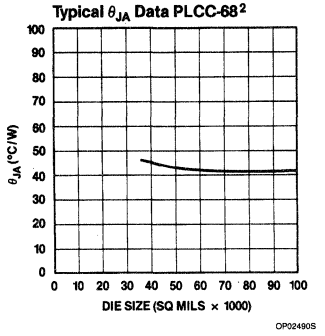
TYPICAL SMD THERMAL (θ_{JA})

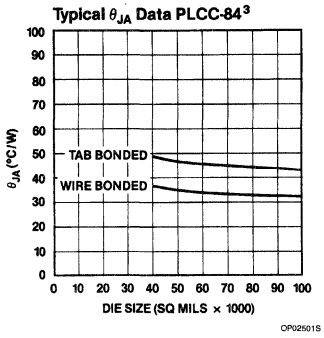












NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	±15%

2. TEST CONDITIONS:

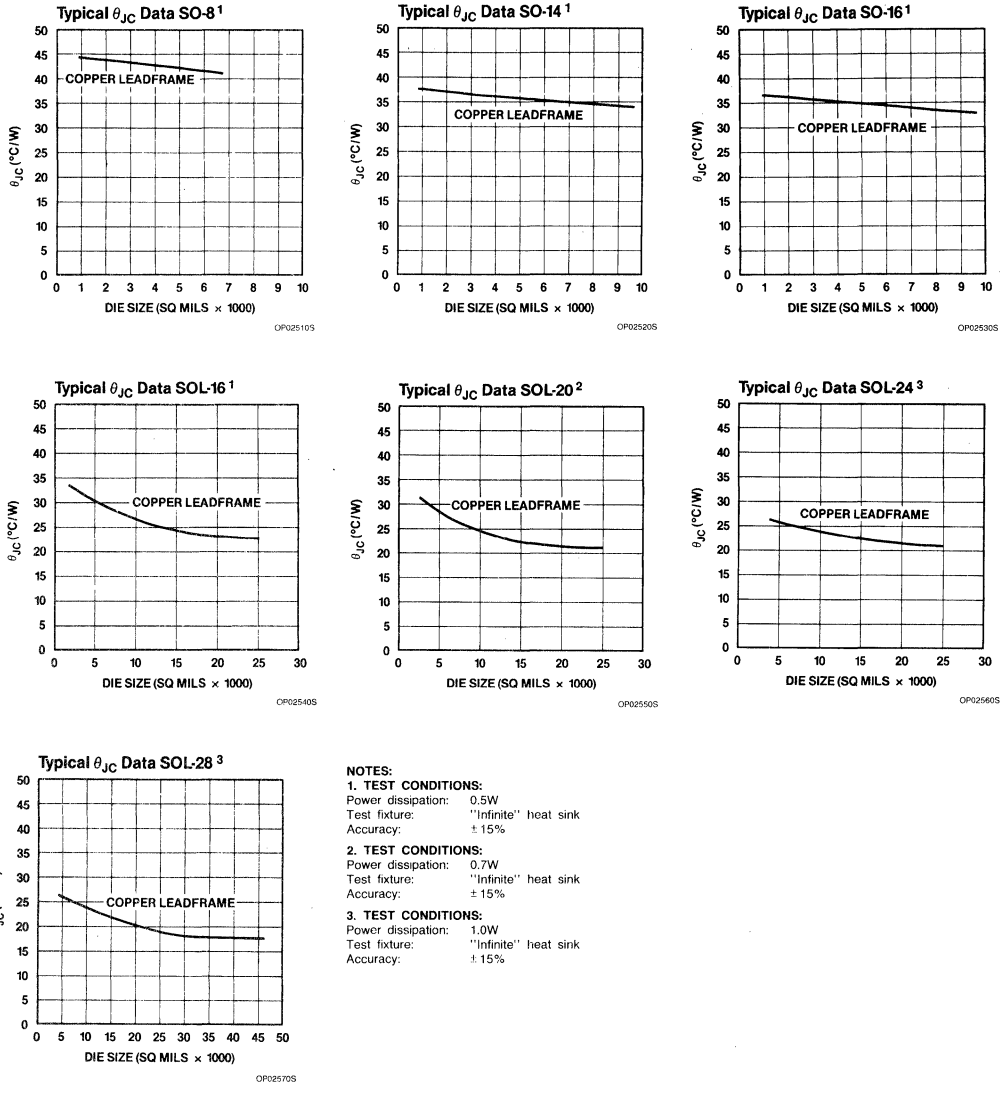
Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	±15%

3. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	1.5W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	±15%

Figure 11

TYPICAL SMD THERMAL (θ_{JC})



NOTES:

1. TEST CONDITIONS:
Power dissipation: 0.5W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

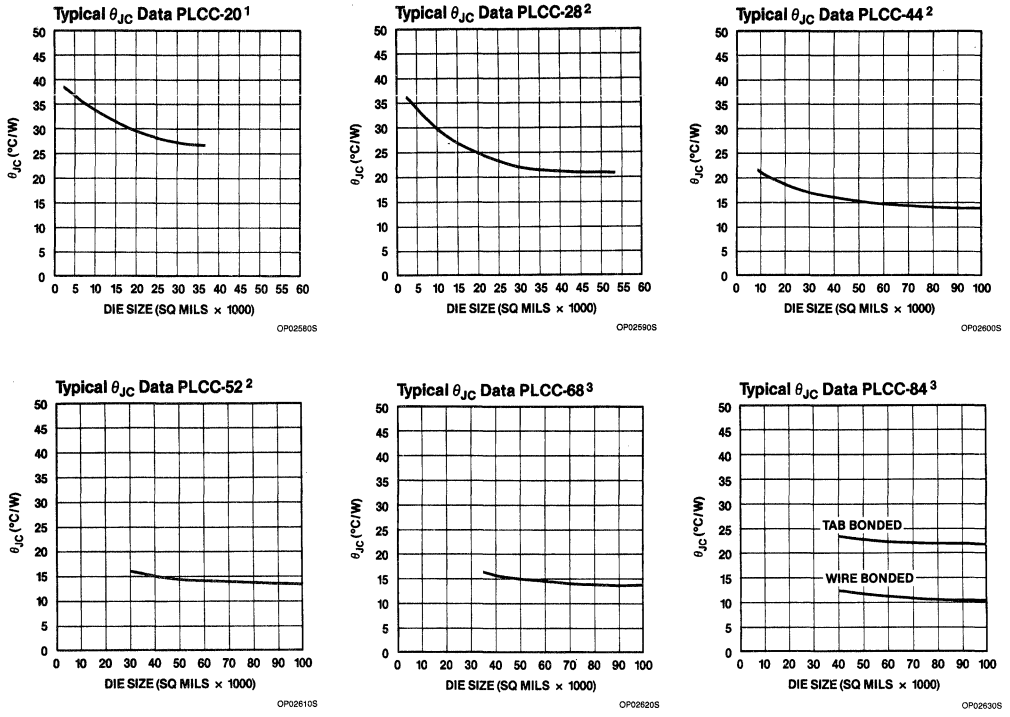
2. TEST CONDITIONS:
Power dissipation: 0.7W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

3. TEST CONDITIONS:
Power dissipation: 1.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

Figure 12

7

TYPICAL SMD THERMAL (θ_{JC})



NOTES:

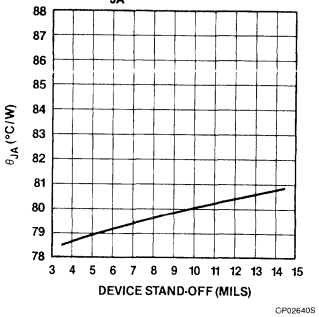
1. TEST CONDITIONS:
Power dissipation: 0.75W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

2. TEST CONDITIONS:
Power dissipation: 1.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

3. TEST CONDITIONS:
Power dissipation: 2.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

Figure 13

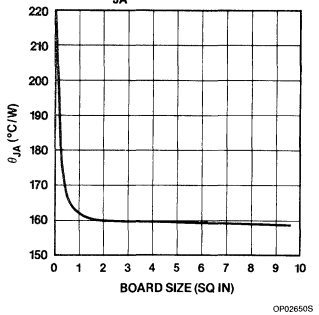
Effect of Device Stand-Off on SO θ_{JA}[1]



NOTES:
1. TEST CONDITIONS:

Package type:	SOL-20 CLF
Die size:	11,322 sq mils
Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")

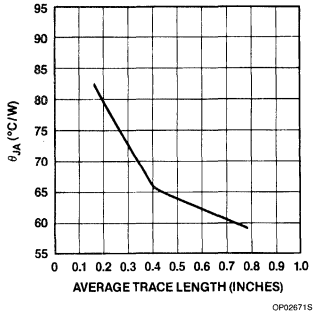
Effect of Board Size on SO θ_{JA}[2]



2. TEST CONDITIONS:

Package type:	SO-14 CLF
Die size:	5,040 sq mils
Test ambient:	Still air
Power dissipation:	0.6W
Test fixture:	0.062" thick PCB with "No Traces" 0-9 MIL stand-off

Effect of Trace Length on 28-Lead PLCC θ_{JA}[3]



3. TEST CONDITIONS:

Package type:	PLCC-28 CLF
Die size:	10,445 sq mils
Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062") trace 27 MIL wide 1 oz SQ ft copper

Figure 14

7

Thermal Considerations For Surface Mounted Devices

SYSTEM CONSIDERATIONS

With the increases in layout density resulting from surface mounting with much smaller packages, other factors become even more important. THE USER IS IN CONTROL OF THESE FACTORS.

One of the most obvious factors is the substrate material on which the parts are mounted. Environmental constraints, cost considerations and other factors come into play when choosing a substrate. The choice is expanding rapidly, from the standard glass epoxy PWB materials and ceramic substrates to flexible circuits, injection molded plastics, and coated metals. Each of these has its own thermal characteristics which must be considered when choosing a substrate material.

Studies have shown that the air gap between the bottom of the package and the substrate has an effect on θ_{JA}. The larger the gap, the higher the θ_{JA}. Using thermally conductive epoxies in this gap can slightly reduce the θ_{JA}.

It has long been recognized that external cooling can reduce the junction temperatures of devices by carrying heat away from both the devices and the board itself. Signetics has done several studies on the effects of external cooling on boards with SO packages. The results are shown in Figures 15 through 18.

The designer should avoid close spacing of high power devices so that the heat load is spread over as large an area as possible. Locate components with a higher junction temperature in the cooler locations on the PCBs.

The number and size of traces on a PWB can affect θ_{JA} since these metal lines can act as radiators, carrying heat away from the package and radiating it to the ambient. Although the chips themselves use the same amount of energy in either a DIP or an SO package, the increased density of a Surface Mounted Assembly concentrates the thermal energy into a smaller area.

It is evident that nothing is free in PWB layout. More heat concentrated into a smaller area makes it incumbent on the system designer to provide for the removal of thermal energy from his system.

Large conductor traces on the PCB conduct heat away from the package faster than small traces. Thermal vias from the mounting surface of the PCB to a large area ground plane in the PCB reduces the heat buildup at the package.

In addition to the package's thermal considerations, thermal management requires one to at least be aware of potential problems caused by mismatch in thermal expansion.

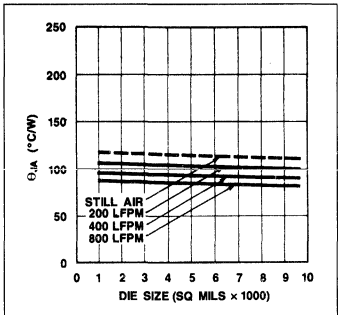


Figure 15. Results of Air Flow on θ_{JA} on SO-14 With Copper Leadframe

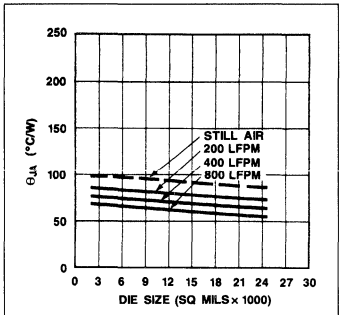


Figure 16. Results of Air Flow on θ_{JA} on SOL-16 With Copper Leadframe

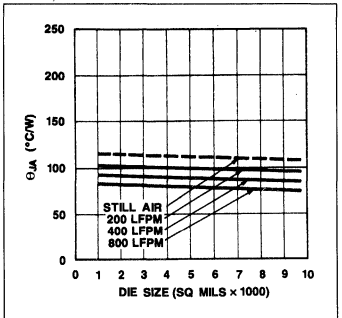


Figure 17. Results of Air Flow on θ_{JA} on SO-16 With Copper Leadframe

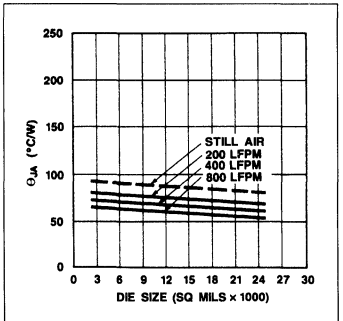


Figure 18. Results of Air Flow on θ_{JA} on SOL-20 With Copper Leadframe

The very nature of the SMD assembly, where the devices are soldered directly onto the surface, not through it, results in a very rigid structure. If the substrate material exhibits a different thermal coefficient of expansion (TCE) than the IC package, stresses can be setup in the solder joints when they are subjected to temperature cycling (and during the soldering process itself) that may ultimately result in failure.

Because some of the boards assembled will require the use of Leadless Ceramic Chip Carriers (LCCCs), TCE must be understood. As will be seen below, TCE is less of a problem with the commercial SMD packages with leads.

Take the example of a leadless ceramic chip carrier with a TCE of about 6×10^{-6}/K soldered to a conventional glass-epoxy laminate with a TCE in the region of 16×10^{-6}/K. This thermal expansion mismatch has been shown to fracture the solder joints during thermal cycling. Substrate materials with matched TCEs should be evaluated for these SMD assemblies to avoid problems caused by thermal expansion mismatch.

The stress level associated with thermal expansion and contraction of small SMDs such as capacitors and resistors, where the actual change in length is small, are normally rather low. However, as component sizes increase, stresses can increase substantially.

Thermal expansion mismatch is unlikely to cause too many problems in systems operating in benign environments; but, in harsher conditions, such as thermal cycling in military or avionic applications, the mechanical stresses setup in solder joints due to the different TCEs of the substrate and the component are likely to cause failure.

The basic problem is outlined in Figure 19. The leadless SMD is soldered to the substrate as shown, resulting in a very rigid structure. If the substrate material exhibits a different TCE from that of the SMD material, the amount of expansion for each will differ for any given increase in temperature. The soldered joint will have to accommodate this difference, and failure can ultimately result. The larger the component size, the higher the stress levels so that this phenomenon is at its most critical in applications requiring large LCCCs with high pin-counts.

Thermal Considerations For Surface Mounted Devices

AN SMD-100

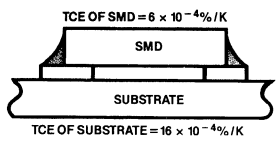


Figure 19. The Basic Problem of Thermal Expansion Mismatch Is That the Substrate and Component May Each Have Different Thermal Coefficients of Expansion.
NOTE: Data provided by N.V. Philips

To address this problem, three basic solutions are emerging. First, the use of leadless ceramic chip carriers can sometimes be avoided by using leaded devices; the leads can flex and absorb the stress. Second, when this solution is not feasible, the stresses can be taken up by inserting a compliant elastomeric layer between the ceramic package and the epoxy glass substrate. Third, TCE values of component and substrate can be matched.

USING LEADED DEVICES (SO, SOL & PLCC)

The current evolution in commercial electronics includes the adoption of the commercial SMD packages, i.e. SO with gull-wing leads or the PLCC with rolled-under J-leads, rely on the compliance of the leads themselves to avoid any serious problems of thermal expansion mismatch. At elevated temperatures, the leads flex slightly and absorb most of the mechanical stress resulting from the thermal expansion differentials.

Similarly, leaded holders can be used with LCCCs to attach them to the substrate and thus absorb the stress.

Unfortunately, using a lead does not always ensure sufficient compliancy. The material from which the lead is made, and the way it is formed and soldered can adversely affect it. For example, improper soldering techniques, which cause excess solder to over-fill the bend of the gull-wing lead of an SO can significantly reduce the lead's compliancy.

COMPLIANT LAYER

This approach introduces a compliant layer onto the interface surface of the substrate to absorb some of the stresses. A 50μm thick elastomeric layer is bonded to the laminate. To make contacts, carbon or metalic powders are introduced to form conductive stripes in the nonconductive elastomer material. Unfortunately, substrates using this technique are substantially more expensive than standard uncoated boards.

Another solution is to increase the compliancy of the solder joint. This is done by increasing the stand-off height between the underside of the component and the substrate. To do this, a solder paste containing lead or ceramic spheres which do not melt when the surrounding solder reflows, thus keeping the component above the substrate can be used.

MATCHING TCE

There are two ways to approach this solution. The TCE of the substrate laminate material can be matched to that of the LCCC either by replacing the glass fibers with fibers exhibiting a lower TCE (composites such as epoxy-Kevlar ® or polyimide-Kevlar and polyimide-quartz), or by using low TCE metals (such as Invar ®, Kovar, or molybdenum).

This latter approach involves bonding a glass-polyimide or a glass-epoxy multilayer to the low TCE restraining core material. Typical of such materials are copper-Invar-copper, Alloy-42, copper-molybdenum-copper, and copper-graphite. These restraining-core constructions usually require that the laminate be bonded to both sides to form a balanced structure so that they will not warp or twist.

This inevitably means an increase in weight, which has always been a negative factor in this approach. However, the SMD substrate can be smaller and the components more densely packed in many cases overcoming the weight disadvantages. On the positive side, the material's high thermal conductivity helps to keep the components cool. Moreover, copper-clad-Invar lends itself readily to moisture-proof multilayering for the creation of ground and power planes and for providing good inherent EMI/RFI shielding.

Kevlar is lighter and widely used for substrates in military applications; but, it suffers from a serious drawback which, although overcome to a certain extent by careful attention to detail, can cause problems. The material, when laminated, can absorb moisture and chemical processing fluids around the edges. Thermal conductivity, machinability and cost are not as attractive as for copper-clad Invar.

For the majority of commercial substrates however, where the use of ceramic chip carriers in any quantity is the exception rather than the rule, and when adequate cooling is available, the mismatch of TCEs poses little or no problem. For these substrates traditional FR-4 glass-epoxy and phenolic-paper will no doubt remain the most widely used materials.

Although FR-4 epoxy-glass has been the traditional material for plated-through professional substrates, it is phenolic-paper laminate (FR-2) which finds the widest use in consumer electronics. While it is the cheapest material, it unfortunately has the lowest dimensional stability, rendering it unsuitable for the mounting of LCCCs.

SUBSTRATE TYPES

FR-4 glass-epoxy substrates are the most commonly used for commercial electronic circuits. They have the advantage of being cheap, machinable, and lightweight. Substrate size is not limited. On the negative side, they have poor thermal conductivity and a high TCE, between 13 and 17 $\times$ 10^{-6}/K. This means they are a poor match to ceramic.

Glass polyimide substrates have a similar TCE range to glass-epoxy boards, but better thermal conductivity. They are, however, three to four times more expensive.

Polyimide Kevlar substrates have the advantage of being lightweight and not restricted in size. Conventional substrate processing methods can be used and its TCE (between 4 and 8), matches that of ceramic. Its disadvantages are that it is expensive, difficult to drill and is prone to resin microcracking and water absorption.

Polyimide quartz substrates have a TCE between 6 and 12 making them a good match for LCCCs. They can be processed using conventional techniques, although drilling vias can be difficult. They have good dielectric properties and compare favorably with FR-4 for substrate size and weight.

Alumina (ceramic) substrates are used extensively for high-reliability military applications and thick-film hybrids. The weight, cost, limited substrate size and inherent brittleness of alumina means that its use as a substrate material is limited to applications where these disadvantages are outweighed by the advantage of good thermal conductivity and a TCE that exactly matches that of LCCCs. A further limitation is that they require Thick-film screening processing.

Copper-clad Invar substrates are the leading contenders for TCE control at present. It can be tailored to provide a selected TCE by varying the copper-to-Invar ratio. Figure 20 shows the construction of a typical multilayer substrate employing two cores providing the power and ground planes. Plated-through holes provide an integral board-to-board interconnection. The low TCE of the core dominates the TCE of the overall substrate, making it possible to mount LCCCs with confidence.

Because the TCE of copper is high, and that of Invar is low, the overall TCE of the substrate can be adjusted by varying the thickness of the copper layers. Figure 21 plots the TCE range of the copper-clad Invar as a function of copper thickness, and shows the TCE range of each of several other materials to which the clad material can be matched. For example, if the TCE of Alumina is to be matched, then the core should have about 46% thickness of copper. When this material is used as a thermal mounting plane, it also acts as a heatsink.

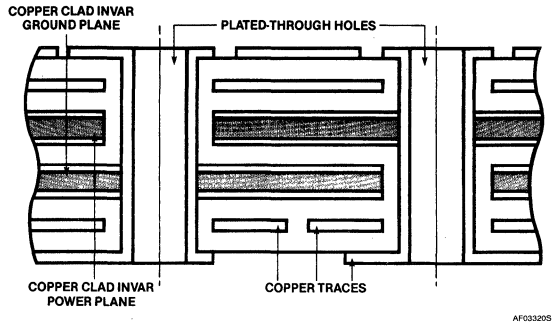


Figure 20. Section Through a Typical Multilayer Substrate Incorporating Copper-clad Invar Ground and Power Planes, Interconnected Via Plated-though Holes.

NOTE: Data provided by N.V. Philips

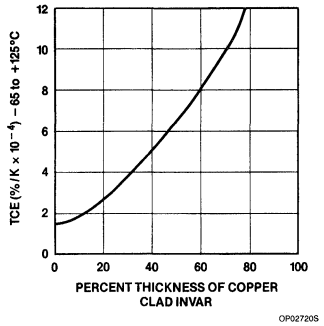


Figure 21. The TCE Range of Copper-clad Invar as a Function of Copper Thickness.

NOTE: Data provided by N.V. Philips

Table 1. Substrate Material Properties

SUBSTRATE MATERIAL	TCE (10^{-6}/K)	THERMAL CONDUCTIVITY (W/m^{3}K)
Glass-epoxy (FR-4)	13 – 17	0.15
Glass polyimide	12 – 16	0.35
Polyimide Kevlar	4 – 8	0.12
Polyimide quartz	6 – 12	TBD
Copper-clad Invar	6.4 (typical)	165 (lateral) 16 (transverse)
Alumina	5 – 7	21
Compliant layer Substrate	See Notes	0.15 – 0.3

NOTES:
Compliant layer conforms to TCE of the LCCC and to base substrate material.
Data provided by N.V. Philips
KEVLAR® is a registered trademark of DU PONT.
INVAR® is a registered trademark of TEXAS INSTRUMENTS.

CONCLUSION

Thermal management remains a major concern of producers and users of ICs. The advent of SMD technology has made a thorough understanding of the thermal characteristics of both the devices and the systems they are used in mandatory. The SMD package, being smaller, does have a higher θ_{JA} than its standard DIP counterpart . . . even with Copper Lead Frames. That is the major trade-off one accepts for package miniaturization. However, consideration of all the variables affecting IC junction temperatures will allow the user to take maximum advantage of the benefits derived from use of this technology.

Signetics

Logic Products

Section 8
Surface Mounted ICs

Signetics

Surface Mounted ICs

Logic Products

INTRODUCTION

Economic survival is driving the electronics industry to use cheaper, faster, more reliable and more dense systems and components. Assembly technologies, such as SMD (Surface Mounted Device) technology, developed and used in hybrids and for military electronics for over two decades, is being adapted to commercial electronics as part of this evolution. With SMD technology, components are soldered directly to a metalized footprint on the surface of the board or substrate rather than being inserted through holes drilled in the board and then soldered. Because of this evolution, package styles specially designed to facilitate surface mounting are now in high demand.

The reasons for the change to SMD technology vary from one customer to another; but the primary motivator is higher profits through lower manufacturing and material costs, or an improved product, or both.

Improved Electrical Performance

Because SMD packages are much smaller than their DIP counterparts, they have much less capacitance and inductance, and provide improved AC performance, especially in high-speed environments. They help to minimize problems associated with ground bounce and multiple output switching found with standard DIP packages. The SO package is especially suitable for high-speed families such as FAST and High-Speed CMOS where package inductance can induce or compound problems not normally found in slower technologies.

Ease Of Automation

SMD pick-and-place machines offer higher yields, faster cycle rates (3 – 10x faster), and much higher throughput volumes than automatic insertion machines for DIP packages.

Greatly Increased Densities

Greatly increased densities can be achieved through surface mounting. The packages themselves are much smaller (as much as 70%) and can be placed much closer together. Furthermore, both sides of the board can be used with SMDs.

Reduced Board Costs

The number of layers, total size of the board and the number of plated through holes can be reduced, thus lowering the total cost of the board (many companies claim savings of 30 to 50%).

Easier Board Rework

In those instances where rework is necessary, it is much faster and cheaper with SMDs.

Improved Reliability

Not only are the components proving to be at least as reliable as their DIP counterparts but, surface mounted assemblies show fewer failures in stress tests than equivalent through hole assemblies.

Lower Shipping, Storage And Handling Costs

SMD components are up to 70% smaller and weigh up to 90% less than DIPs (up to 95% savings in storage area for Tape & Reel SMD components vs DIPs and up to 90% savings in component weight). Surface mount assemblies offer additional savings in both weight and space, both of which can be linked to increased profits.

SMD packages for integrated circuits fall into two categories: Swiss Outline also known as Small Outline (SO) and the Plastic Leaded Chip Carrier (PLCC).

SO PACKAGE

The SO package was developed by N.V. Philips Corp, originally for the Swiss watch industry. In the mid 1970s Signetics introduced linear ICs in SO packages to the US market (hybrid and telecommunications). As demand grew, other technologies such as FAST, Low Power Schottky, Schottky, TTL, CMOS, High-Speed CMOS (HC and HCT), ECL, ROMs, RAMs, PROMs, were made available in SO packages.

The SO is a dual-in-line plastic package with leads spaced 0.050″ apart and bent down and out in a Gull-Wing format. It comes in two widths: 0.150″ SO, and 0.300″ SOL (SO-Large) depending on the pin count.

As ICs became more complex and the number of pins grew, the standard dual-in-line packages grew longer and wider, presenting new electrical and mechanical problems. Some of these were resolved with the introduction of the ceramic leadless chip carrier (LCC). These were square, ceramic packages without leads which can be socketed or soldered directly to a substrate if the thermal coefficient of expansion of the chip carrier and the substrate are be matched.

In 1980, the Plastic Leaded Chip Carrier (PLCC) was introduced as a cheaper alternative to the LCC. However, this was at the same time that SMD was winning acceptance in commercial electronics and the PLCC was seen as an ideal SMD package for the higher pin count devices (those with more than 28 leads). The PLCC is a square, plastic package with leads on four sides, spaced down and under in a J-Bend configuration. It is available in the higher pin counts: 20, 28, 44, 52, 68, 84 with even higher pin counts under development.

The smallest square PLCC is the 20 pin package. There are many reasons for this; the primary one is that below 20 pins, the package would be as thick as it is square,

Table 1

PIN COUNT	SO	SOL	PLCC
8	x		
14	x		
16	x	x	
18		x	x (rectangular)
20		x	x
24		x	
28		x	x
44			x
52			x
68			x
84			x

Table 2. Maximum Thermal Resistance (θ_{JA}) Values For SMD Packages (°C/W)

PINS	SO	SOL	PLCC
8	160		
14	115		
16	110	90	
20		85	70
24		75	
28		70	60
44			42
52			39
68			42
84			32

resulting in a cube-like package which would be very difficult to handle in an automated environment.

Logic and linear devices are available in SO while the more complex parts such as microprocessors, microcontrollers, complex peripherals, large memory devices, and other higher pin count integrated circuits will be found in the PLCC.

ASSEMBLY

The assembly of these SMD packages is virtually the same as for the older DIP packages using the same materials and most of the same equipment and assembly technologies.
The only differences in the process are the smaller lead frames, different lead bends (gull-wing for SO and J-Bend for the PLCC), and closer spacing resulting in a much smaller package for the same basic die.

RELIABILITY

Reliability studies of SMD components, conducted not only by Signetics and Philips, but many of our competitors and our customers have revealed that these packages are at least as reliable as the standard plastic DIP packages that have been used over the past 20 years. In several cases, test results of the SMD packages have been better than their DIP counterparts.

THERMAL CHARACTERISTICS

Thermal characteristics of ICs have always been a major consideration to producers and users of electronics products because an increase in junction temperature (T_J) can have an adverse effect on the long term operating life of an IC. The advantages realized by miniaturization have trade-offs in terms of increased junction temperatures. Some of the variables affecting T_J are controlled by the producer of the IC, while others are controlled by the user and the environment in which the device is used.

With the increased use of SMD, thermal management remains a valid concern because not only are the packages much smaller, but the thermal energy is concentrated much more densely on the PCB. For these reasons users of SMD must be more aware of all the variables affecting T_J.

Power Dissipation

Power dissipation (P_D) varies from one device to another depending on technology and complexity. It can be obtained by multiplying V_{CCmax} by the I_{CC} Characterized at the maximum ambient temperature expected (in the case of TTL, 70°C).

- Junction temperature (T_J) is the temperature of a powered IC measured at the substrate diode. When the device is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A).
- All standard TTL, Schottky, Low Power Schottky, and FAST being built by Signetics use copper leadframes.
- The ability of the package to conduct heat from the chip to the environment is expressed in terms of thermal resistance, normally called Theta JA (θ_{JA}). θ_{JA} is the total resistance from the junction to ambient and is often separated into two components: θ_{JC} (junction to case) and θ_{CA} (case to ambient). $\theta_{JA} = \theta_{JC} + \theta_{CA}$ θ_{JA} values for SMD packages are listed in Table 2.
- All measurements are in still air.
- $T_{A\ max}$ is +70°C.
- I_{CC} Characterized at nominal V_{CC} and +70°C ambient.
- Calculate power (P) by multiplying V_{CC} nominal $\times$ I_{CC} at +70°C.
  $P = I_E$
- Calculate rise in (T_J) by multiplying Power by θ_{JA}.
  $T_J = P \times \theta_{JA}$
- Add $T_J + T_{A\ max}$. If result is greater than 120°C, then thermal mounting or some other way to reduce the T_J must be used.

Factors Affecting Thermal Resistance

In addition to possible loading and duty cycle factors in some technologies, there are several factors which affect θ_{JA} of any IC package. Effective thermal management demands a sound understanding of all these variables.

Package variables include the leadframe design, leadframe material, the plastic used to encapsulate the device, and to a lesser extent, other variables such as the die size and die attach methods. While the thermal conductivity of the wire can be calculated, it is too insignificant to be considered as a factor.

Other factors that have a significant impact on the θ_{JA} include the substrate upon which the package is mounted, the density of the layout, the gap between the package and substrate, the number and length of traces on the surfaces of the board, the use of thermally conductive epoxies, and any external cooling methods.

STANDARDIZATION

The SO package is an industry standard format. In June 1985, the JEDEC (Joint Electronics Engineering Council) of the EIA (Electronics Industries Association) issued a Solid State Product Outlines Standard for each of the SO formats: MS-012 AA-AC for the 0.150″ body width SO and Ms-013 AA-AE for the 0.300″ body width SOL. In addition to the JEDEC Standard, de facto standardization has been achieved in the industry in that most of the major US and European IC manufacturers (more than 15 companies currently) use this standard.

The PLCC is also a standardized format, with a JEDEC Registered Outline #MO-047 AA-AH. It also is multiple sourced with over 10 US IC manufacturers using this standard.

Points worth noting: ALL SO AND SOL PACKAGES HAVE 0.050″ LEAD SPACING AND A GULL-WING LEAD BEND, WHILE ALL PLCC PACKAGES HAVE THE SAME LEAD SPACING AND A J-BEND LEAD BEND.

TAPE AND REEL

One revolutionary phenomenon in SMD is the development of Tape and Reel for the IC packages. Philips and several other companies making automatic placement equipment recognized the need for a feed system which allows for positive indexing large volumes of components at high-speed in order to get maximum efficiency out of the new pick-and-place machines. Tubes are limited to a relatively small number of parts (dictated by tube length) and depend on gravity to feed components to the placement head. After several proposed tape formats, Philips, Signetics, many of the component and placement equipment manufacturers, and board manufacturers convened under the auspices of EIA (Electronic Industries Association) and agreed on an industry standard specification for Tape and Reel for both SO and PLCC packages. The proposed EIA specification

Surface Mounted ICs

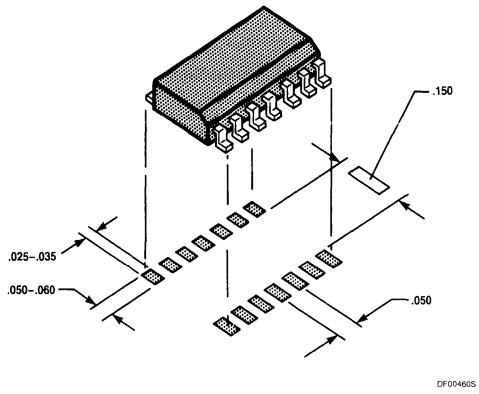
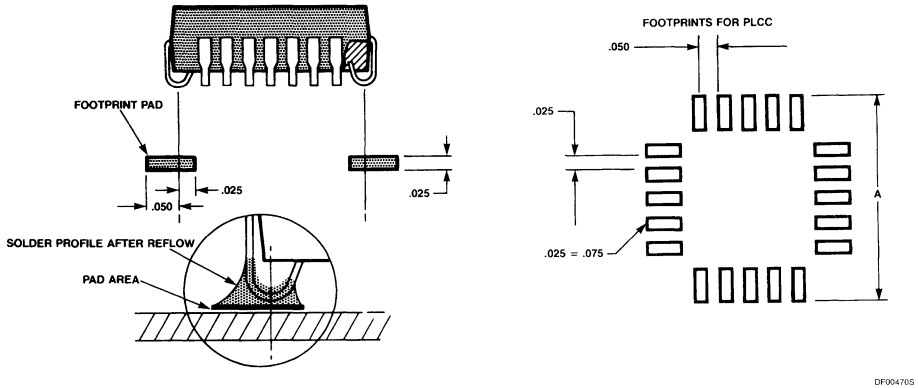


Figure 1. Manufacturers' Recommended Footprint



PINS	A
20	.425
28	.525
44	.725
52	.825
68	1.025

Figure 2. Footprint Design For The PLCC-IC

RS 481A is being used by Signetics and Philips, both of whom have shipped components on Tape and Reel since late 1984.

SUCCESS IN SURFACE MOUNTING BEGINS WITH THE DESIGNER

In addition to the different package configurations, surface mounting is done on a much smaller scale. Instead of the plated through holes, metallized footprints must be etched onto the substrate surface.

The designer will be using a more refined set of rules for layout of the surface mount PC board. Because the components can be spaced closer together with small contact spacing, a narrower conductor trace width is necessary. A common signal conductor can be 0.010″ to 0.012″ wide and 0.015″ through 0.030″ is adequate for power and ground bussing. The suggested footprint contact area has a generous tolerance. For the SO I.C., a rectangular pattern is used on 0.050″ spacing. The length of the pad is 0.050″ to 0.060″ and the width can vary from 0.020″ to 0.035″. The 0.025″ × 0.050″ footprint pattern will work well using the grid placement system favored by most designers. The 0.012″ conductor width spaced at 0.025″ provides a reasonable 0.013″ air gap between traces. However, if conductor traces are routed between contact pads, it will be necessary to neck down the trace width to 0.008″ and still retain an equal airgap at each side. Because neck down traces require additional time in both hand taping or CAD/photo plot generation of artmasters, some compromises may be justified. By reducing the contact pad size to 0.020″ × 0.050″, it is possible to route a consistent 0.010″ conductor trace width and still maintain the desired clearances. However, some PC board shops may not maintain the consistent quality necessary when using this fine line approach over the entire board. It is important to discuss limitation and premium cost penalties with your supplier before full commitment to the 0.010″, and smaller, trace widths.

Another very important consideration to be taken into account is the thermal concentration caused by miniaturization. The same die is being used in the SMD as in the DIP, thus the power dissipated is the same; however, the smaller packages are being placed much closer together, concentrating the thermal energy. The trade-offs between the increase in density and the concentration of thermal energy must be evaluated by the board manufacturer.

These factors may influence the choice of PCB material, the number of layers, and the thickness of the PCB board. New methods to transfer heat from the package to the board and then away from the board should be considered by the designer.

Other factors to be considered are the placement system, soldering method, post-assembly cleaning, inspection, test, and the availability of parts in SMD packages.

One of the first steps is to list all the devices needed and to determine which ones are available in SMD format. With the growth of popularity of SMD, the number of different functions offered by Signetics continues to grow rapidly. In addition to the SIGNETICS SMD POCKET GUIDE, there are several cross-reference lists available from design and assembly services. However, with the explosive growth of this market NONE OF THESE LISTS ARE NECESSARILY CURRENT. Please check with your local sales office because the parts availability lists are growing almost daily.

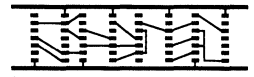
When choosing the type of footprints to use, it is very important that the designer considers the soldering method being used.

Basically there are two types of soldering in use today: flow soldering (wave, drag, or hot solder dip) and reflow soldering (vapor phase, infrared, thermal conduction through the PCB, and hot air).

The SO package can be soldered using a flow soldering method. The devices must be attached to the PCB by means of an adhesive because the device side of the board will be facing down as it goes through the solder wave. The orientation of the part as it goes through the solder wave can play an important role in the elimination of bridges. Experiments should be conducted by the user to determine the best footprints for use in a particular soldering system. Some users feel that the narrower footprints help to reduce solder bridges. Others have been experimenting with rounded footprints to reduce bridging during wave soldering and claim to have had very good results.

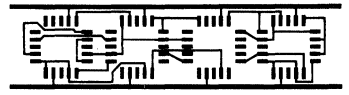
Reflow soldering has been done for many years in the hybrid industry. A solder paste or solder cream is applied to the footprint prior to placement of the component. These pastes and creams contain tiny spheres of solder suspended in a carrier which contains the flux. As the substrate temperature is raised, the flux, solvents, and carriers are driven off and the solder liquifies. Various melting point pastes and creams are available. As the liquid solder migrates to the metallized footprints, the surface tension is enough to move the leaded components. For SO packages, this can be an advantage because it acts as a self-positioning mechanism. However, it can be a problem for the smaller passive components if the solder paste isn't printed on evenly. If there is an uneven amount of solder paste on one end of one of these smaller devices, the surface tension can pull stronger on one side causing a "tombstoning" effect, i.e., one end of the device is lifted straight up.

Many variations of footprint patterns are possible. The formula shown in Figure 1 is applicable for both reflow and wave solder processes. Many configurations are possible



SO-I.C.

DF00490S



PCC-I.C.

DF00500S

Figure 3. Planning – Layout And Component Placement

Surface Mounted ICs

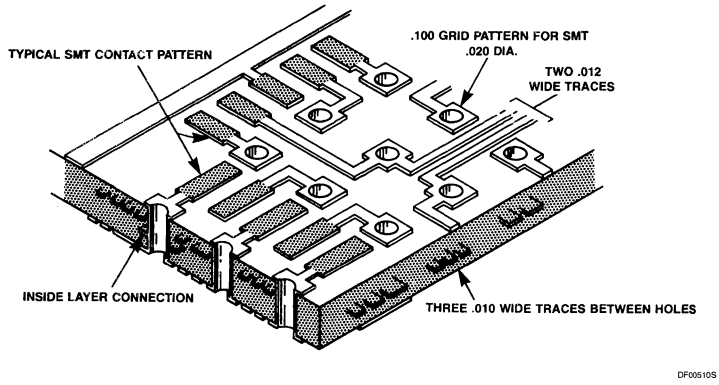


Figure 4

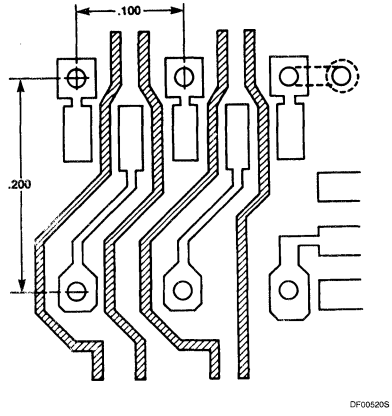


Figure 5

Surface Mounted ICs

and should be tried on an experimental basis before commitment to a large production run. Both time and development costs can be conserved by utilizing design and process consultants specializing in surface mount technology.

Figures 1 and 2 show some typical footprints used in reflow soldering. Note that the width of the footprint for the SO package varies from 0.025″ to 0.035″. Most users tend towards the narrow footprint. Further, the length of these prints should be kept as short as possible to prevent the part from swimming or sliding back and forth on the footprint while still allowing a good meniscus.

Another factor worth noting is that the footprint for PLCC should not extend too far under the package as this could promote solder bridges under the package where they can not be seen during inspection. The footprint for the PLCC should extend out further from the package than the lead itself to allow a good meniscus that will result in a strong, inspectable bond.

Careful placement of related components will allow a more effective use of a much smaller surface area. The interconnections that can be made on the substrate surface result in the elimination of feedthrough holes. Reduction of these holes and their associated pad areas further increase the density of the layout, and reduce total board cost as well. As indicated, the SO package has the same pinout on two parallel rows as found on the older DIP packages being replaced. Arranging related ICs in blocks or functional clusters with their associated discreet components can also help to maximize the use of the available surface area.

For several reasons, many users have expressed their preference for SO format through 28 pins. The SO is much smaller and lighter than the PLCC. The SOL, although a bit longer than the PLCC, still occupies about the same board space.

Further, when using several packages and connecting them together, a given number of SO and SOL packages would take much less space than the same number of PLCCs, simply because of the interconnect geography. (See Figure 3).

Besides being smaller, the SO format is dual-in-line and has the same pinouts as those of a standard DIP (PLCC pinouts vary between devices as well as between manufacturers). The SO format is easier to handle and is much easier to visually inspect.

For devices over 28 pins, the PLCC is the package of choice, largely because it can hold a much larger die than the 0.300″ wide SO packages.

In the early days of PCB technology when plated through holes were not possible, designers were forced to carefully plan component arrangements and connections. Using experience and ingenuity, they were able to eliminate crossovers while reducing the need for unwanted jumpers. With the advent of plated through holes and mutilayer boards, the restriction to single sided boards was eliminated. Using the single sided concept the techniques used to interconnect the SMDs are as important as the footprint patterns. As noted before, the contact pads on 0.050″ centers, range between 0.025″ and 0.035″ in width. Prior to choosing to add a feedthrough hole on the pad itself, two factors should be considered: 1) The hole diameter selected must allow for a reasonable location tolerance. A 0.010″ to 0.015″ diameter plated through hole in 0.062″ thick FR4 material may increase the cost of your PCB. 2) Unless the feedthrough hole on the footprint area is either plugged or masked, in a reflow soldering situation, the solder will tend to migrate away from the IC contact resulting in a poor solder joint.

It is more desirable to add a separate pad for via or feedthrough requirements. To further provide for routing conductor traces while insuring an acceptable air gap, you may choose to use a 0.035″ to 0.037″ square pad for these feedthrough holes. The square configuration will furnish more than enough metal in the diagonal corners to compensate for the reduced annular cross section at the sides of the square. The 0.035″ – 0.037″ square feedthrough pad can be spaced at 0.050″ when necessary or on the more traditional 0.100″ pad. With this spacing it is possible to route two 0.012″ wide conductor traces between pads, something only possible before with costly mutilayer designs using leaded through hole technology.

The feedthrough pad is then connected to the component contact area with a narrow trace. This narrow trace reduces migration of the solder paste during the reflow process. To further reduce migration of the liquid solder, application of solder mask coating over surface areas not requiring solder is recommended. This coating is applied with a wet screen process or photographically as a dry film and will act as a dam to contain solder to the contract area. (See Figures 4 and 5).

When using reflow soldering, the trace width should be about half the width of the footprint pattern. As noted before the signal carrying conductors are generally 0.012″ to 0.015″ wide. Supply voltages are carried on wider traces. When running traces between the device leads, it will be necessary to reduce the width to about 0.008″ which provides an 0.008″ gap between the trace and the edge of the pads when using 0.025″ pads.

Because the SMDs are so much smaller than their leaded counterparts, the scale of the layout should be considered. On larger boards with a mix of SMDs and leaded devices, a 2:1 scale may be adequate. More complex layouts can be designed at 4:1 scale with excellent results. The larger scale will make it possible to increase density while assuring accuracy. If designing with a CAD system, accuracy and density can both be increased by increasing the grid resolution. Routing conductor traces will require careful planning, it is customary to use a 90° or 45° angle (Figure 6) when traces must divert from a continuous line.

Offset stepping several 0.012″ wide conductor traces on 0.025″ spacing will require necking down at the point of direction change to maintain the desired air gap. The start and stop points of photoplotter aperture runs must be carefully executed to reduce the chance of overlay and shorting. If outside services are used for digitizing or photoplotting, discuss your requirements for accuracy before proceeding. Some compromises may have to be made to insure quality and control costs. Preparing artmasters on mylar using precision tape products and pre-printed footprint patterns may afford more flexibility during your entry into SMD technology. Changes can be made easily, and economical photo reduction processes will provide high quality working film. The technique used to prepare working film is a choice generally influenced by in-house capability or services available in a region.

Dramatic changes are taking place throughout this industry. Surface mount technology is key to an efficient transition into miniaturization and automation of electronic production.

Surface Mounted ICs

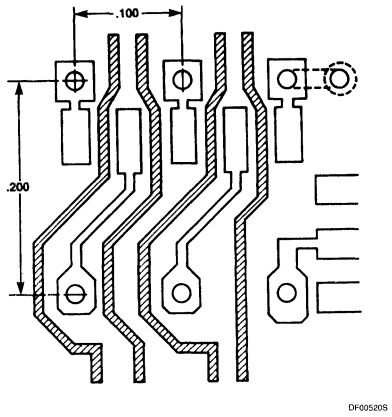


Figure 6

Signetics

Logic Products

Section 9
Package Outlines

INDEX

Signetics

Package Outlines

Logic Products

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

1. Dimensions are shown in Metric units (Millimeters) and English units (Inches).
2. Lead material: Copper Alloy, solder (63%Sn/37%Pb) dipped.
3. Body material: Plastic (Epoxy)
4. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. The substrate diode of a Bipolar technology device is generally the diode used in these tests. Die size and test environment have significant effects on thermal resistance values.

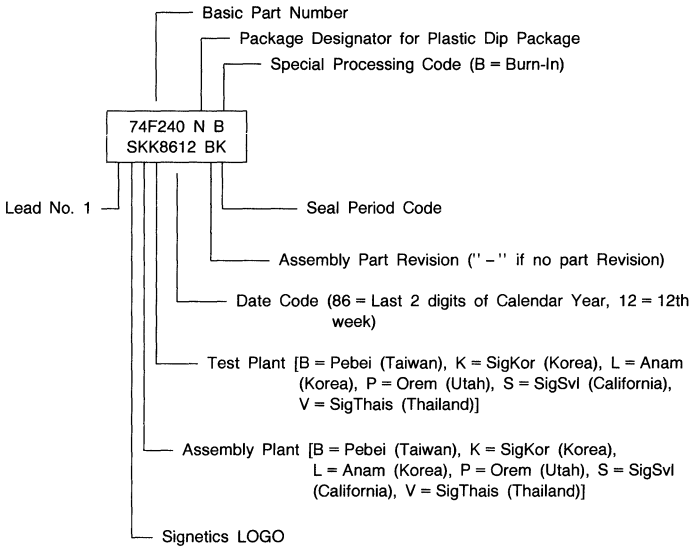
PLASTIC PACKAGES OUTLINES

Package Type	Number of Leads	Package Feature	Package Ordering Code	Package Outline Code	Thermal Resistance θ_{JA}/θ_{JC} (°C/W)	Die Size (square mils)	Test Conditions	
							Test Ambient	Test Fixture
SO[1] (Copper Leadframe)	14 pin (SO-14)	3.9mm (0.15″) Body width	D	DH1	124/37	2,500	Still air at room temperature	Device soldered to Philips glass epoxy test board (1.12″ × 0.75″ × 0.059″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
	16 pin (SO-16)		D	DJ1	113/36			
	16 pin (SOL-16)	7.5mm (0.30″) Body width	D	DJ2	98/30	5,000		Device soldered to Philips glass epoxy test board (1.58″ × 0.75″ × 0.059″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
	20 pin (SOL-20)		D	DL2	90/28			
	24 pin (SOL-24)		D	DN2	76/26			
	28 pin (SOL-28)		D	DQ2	70/24	10,000		
PLCC[2] (Copper Leadframe)	44 pin (PLCC-44)	0.650″ Square body	A	AX1	50/20	15,000	Still air at room temperature	Device soldered to Philips glass epoxy test board (2.24″ × 2.24″ × 0.062″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
DIP[3] (Copper Leadframe)	14 pin (DIP-14)	0.300″ Lead row centers	N	NH1	89/44	2,500	Still air at room temperature	Device in Textool ZIF socket with 0.040″, stand-off. Accuracy: ± 15%
	16 pin (DIP-16)		N	NJ1	86/43			
	20 pin (DIP-20)		N	NL1	74/32	5,000		Device in Textool ZIF socket with 0.040″, stand-off. Accuracy: ± 15%
	24 pin SLIM DIP (DIP-24)		N	NN1	65/36			
	24 pin (DIP-24)	0.600″ Lead row centers	N	NN3	59/30			
	28 pin (DIP-28)		N	NQ3	52/27	10,000		
	40 pin (DIP-40)		N	NW3	45/19	15,000		

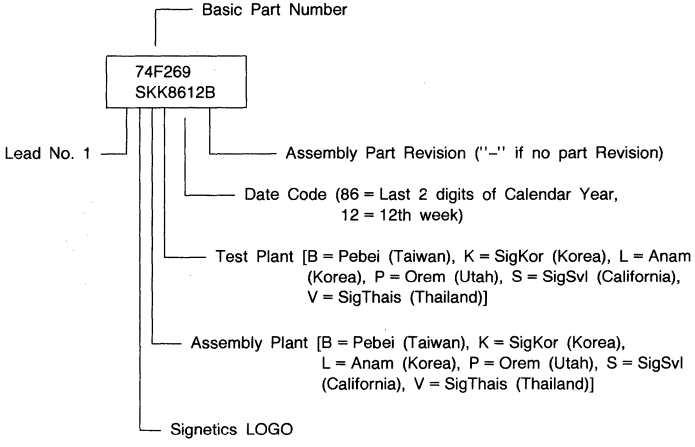
NOTES:
1. SO = **S**mall **O**utline
2. PLCC = **P**lastic **L**eaded **C**hip **C**arrier
3. DIP = **D**ual-**I**n-Line **P**ackage

Package Outlines

4. Package Symbolization for Plastic Dual-In-Line Package (DIP) Top Side

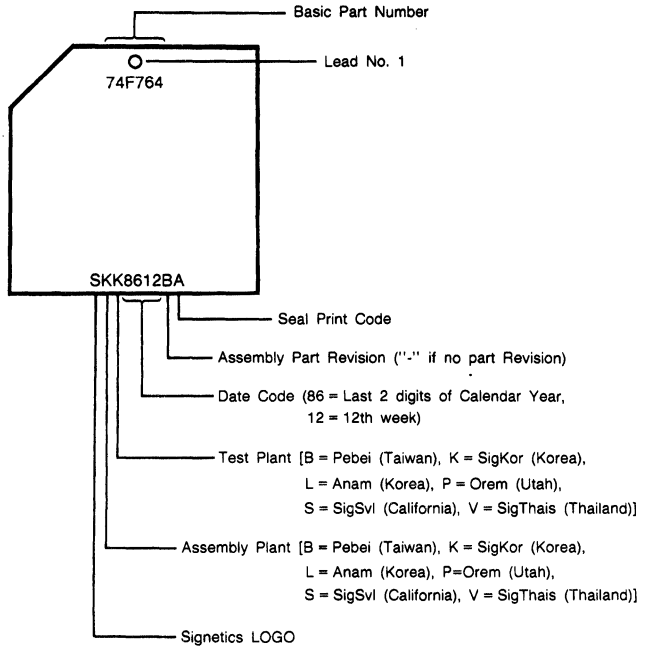


5. Package Symbolization for Plastic Small Outline Package (SO) Top Side



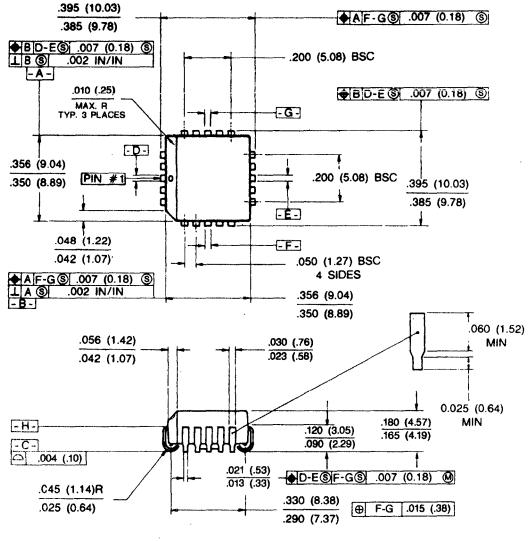
Package Outlines

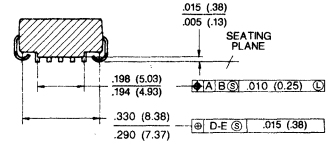
6. Package Symbolization for Plastic Leaded Chip Carrier (PLCC)



Package Outlines

AL1 PLASTIC PLCC-20



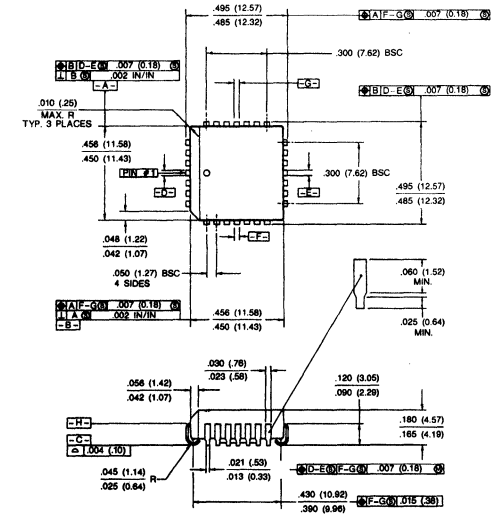


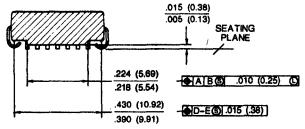
NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #20 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0400 081226

PO00632S

AQ1 PLASTIC PLCC-28





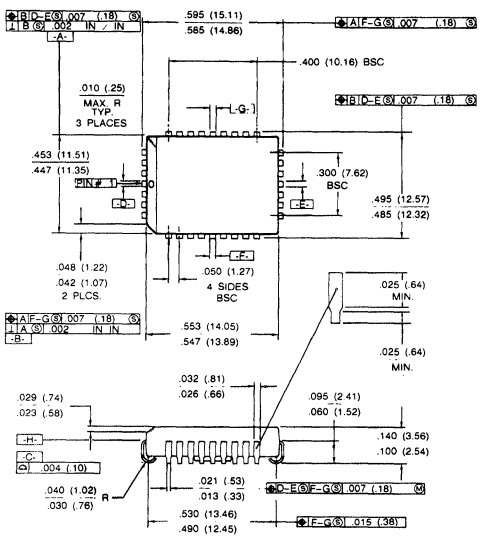
NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #28 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0401 081227

PO00612S

Package Outlines

AR2 PLASTIC PLCC-32

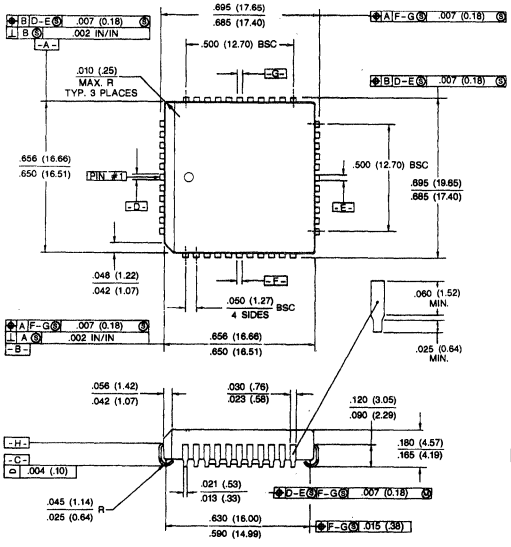


853-0402 081228

PO00171S

NOTES:
1. Package dimensions conform to JEDEC specification MO-052-AE for plastic leaded chip carrier 32 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #32 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

AX1 PLASTIC PLCC-44



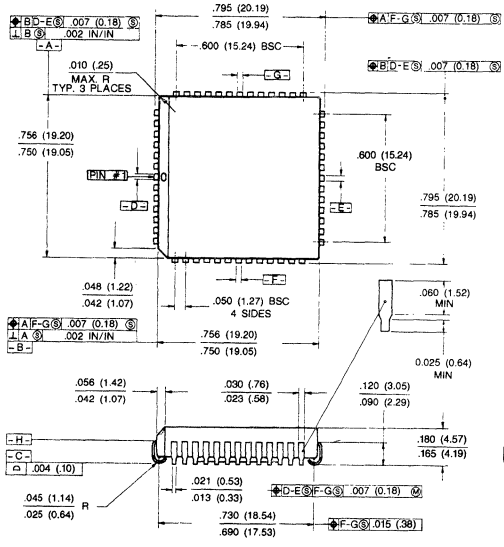
853-0403 081229

PO00602S

NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AL for plastic leaded chip carrier 44 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #44 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

Package Outlines

AA1 PLASTIC PLCC-52

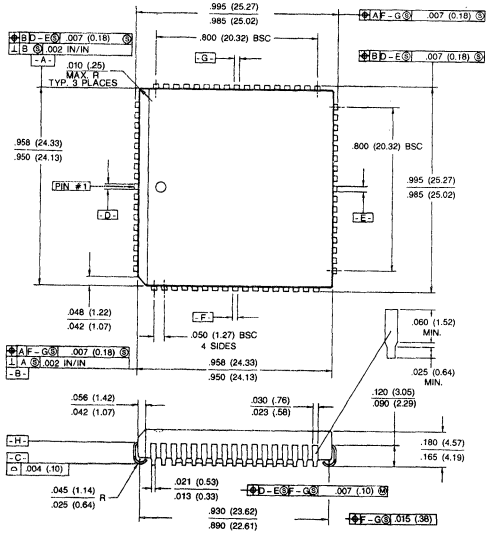


NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AD for plastic leaded chip carrier 52 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #52 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0397 081223

PO00642S

AB1 PLASTIC PLCC-68



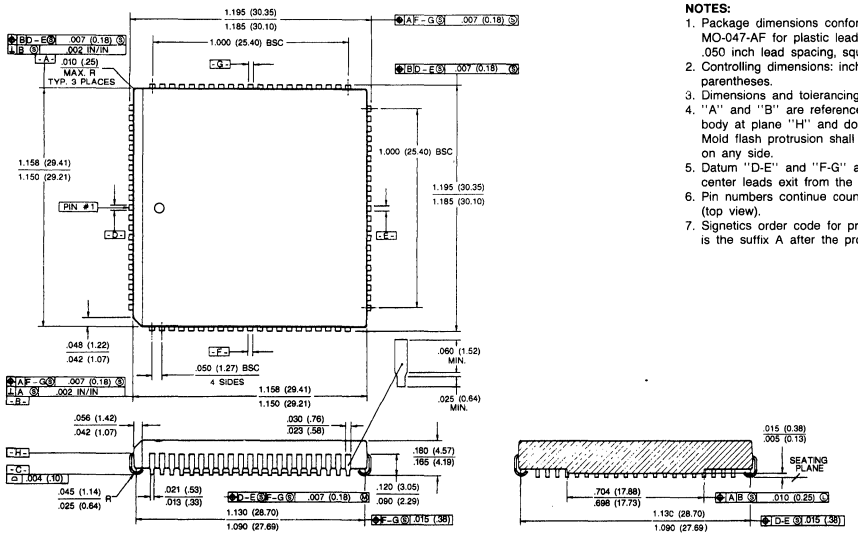
NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AE for plastic leaded chip carrier 68 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #68 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0398 081224

PO00622S

Package Outlines

AC1 PLASTIC PLCC-84



NOTES:

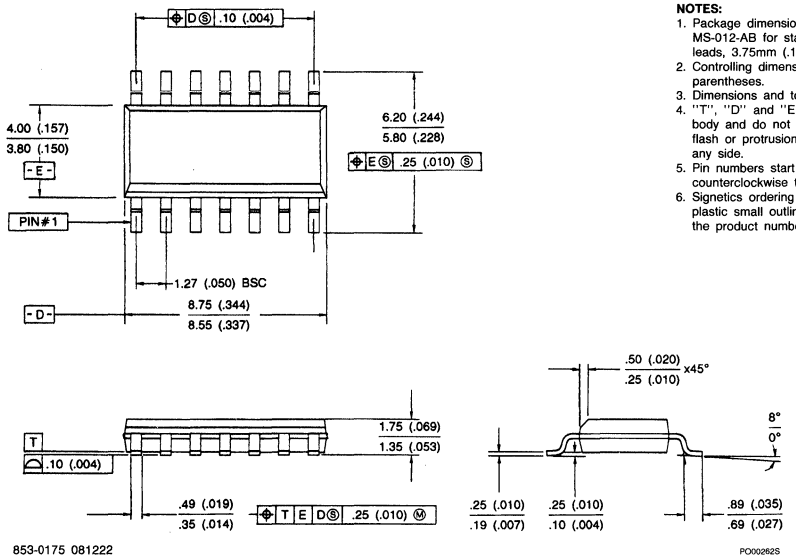
1. Package dimensions conform to JEDEC specification MO-047-AF for plastic leaded chip carrier 84 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #84 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0399 081225

PC00592S

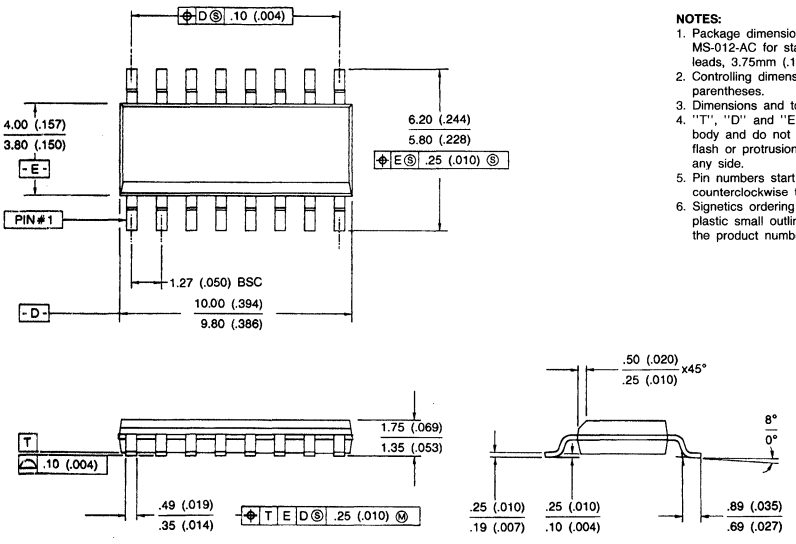
Package Outlines

DH1 PLASTIC SO-14



NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

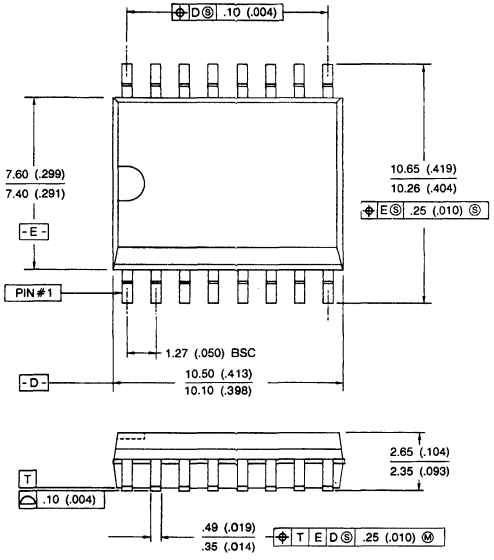
DJ1 PLASTIC SO-16

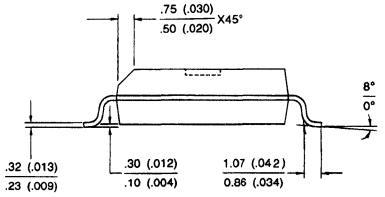


NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Package Outlines

DJ2 PLASTIC SOL-16



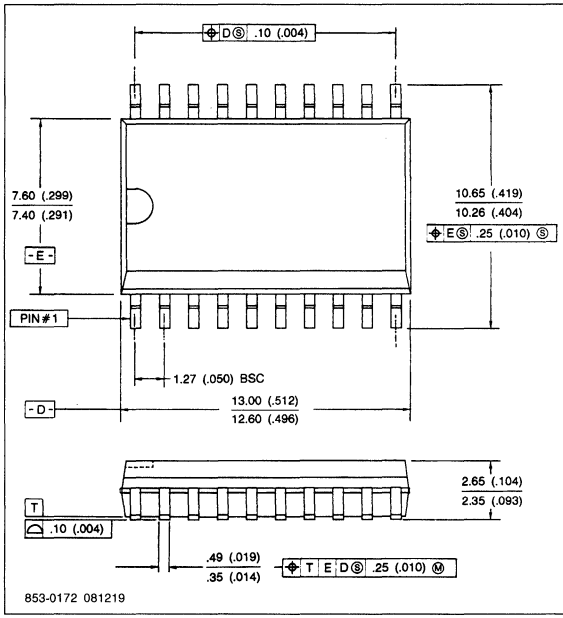


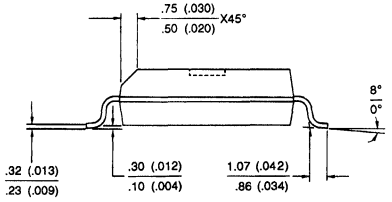
853-0171 081218

PO00241S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

DL2 PLASTIC SOL-20





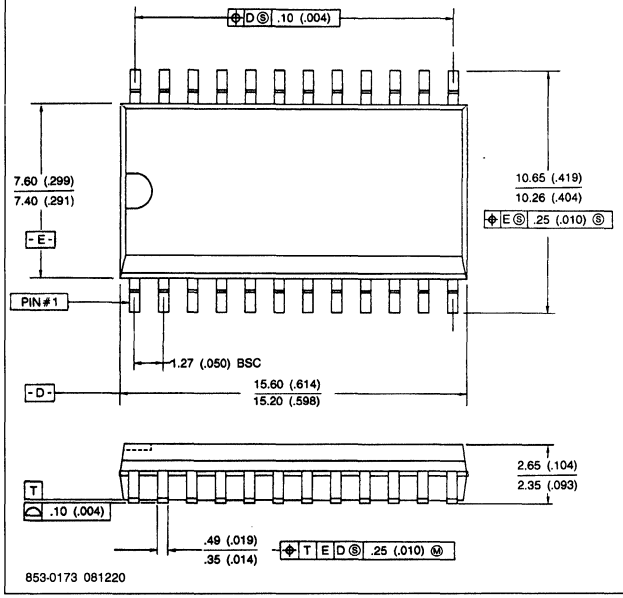
853-0172 081219

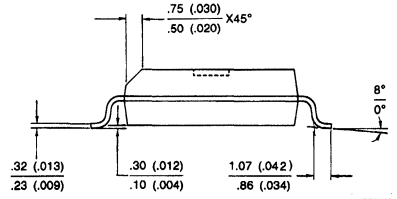
PO00231S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Package Outlines

DN2 PLASTIC SOL-24



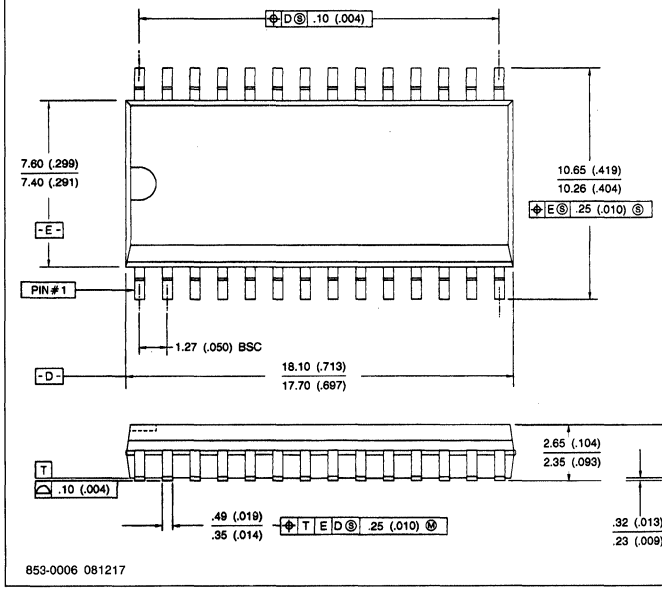


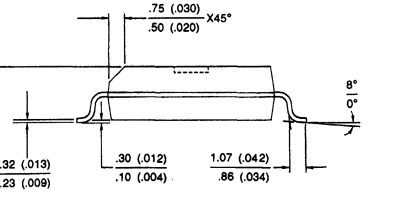
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0173 081220

PO00221S

DQ2 PLASTIC SOL-28





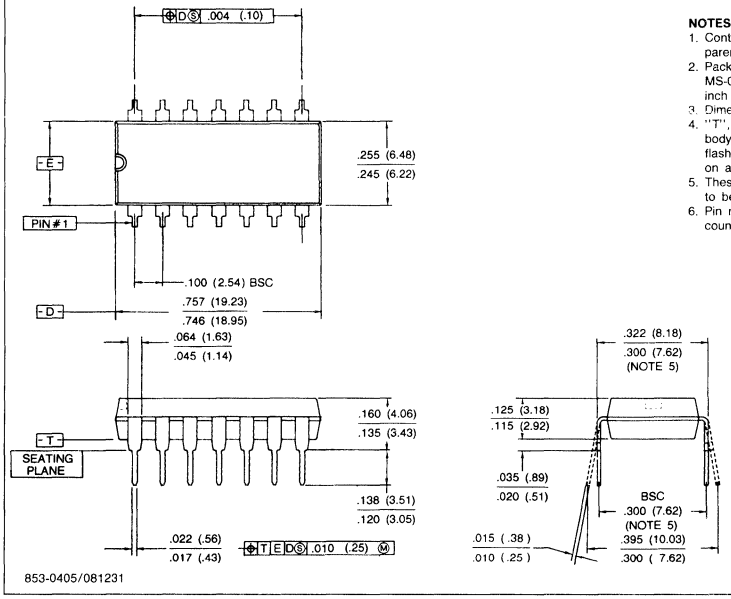
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0006 081217

PO00212S

Package Outlines

NH1 PLASTIC PDIP-14

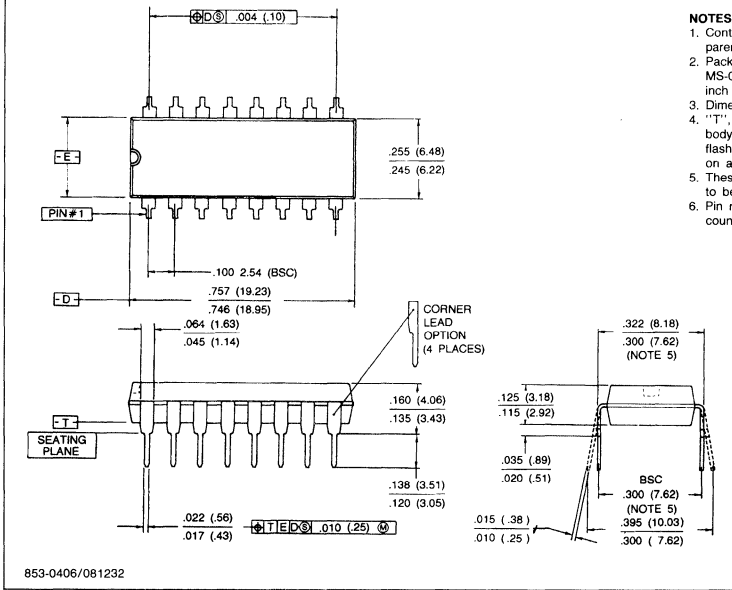


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0405/081231

PO00330S

NJ1 PLASTIC PDIP-16



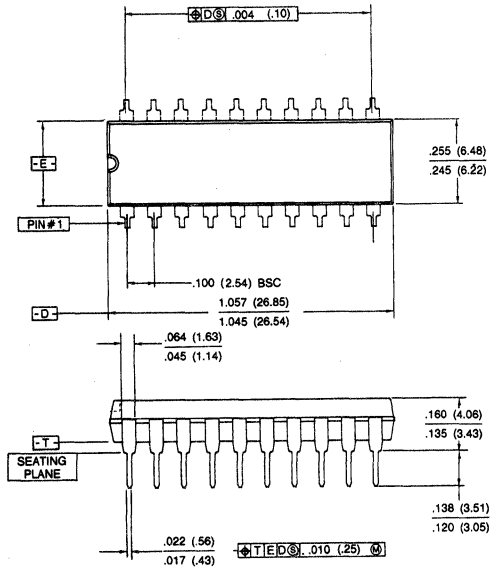
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

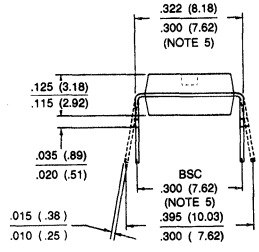
853-0406/081232

PO00280S

Package Outlines

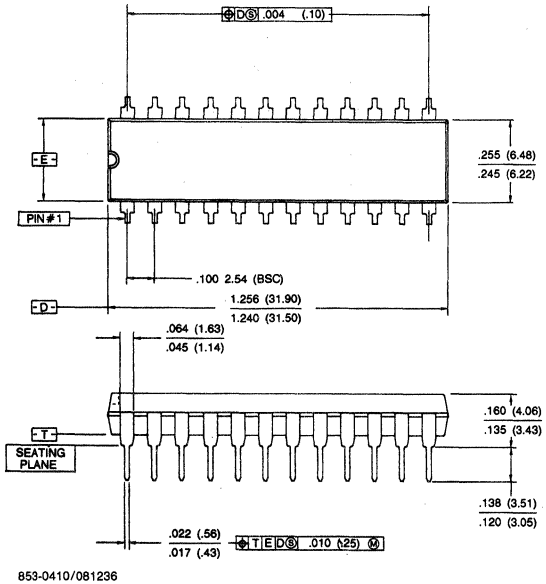
NL1 PLASTIC PDIP-20

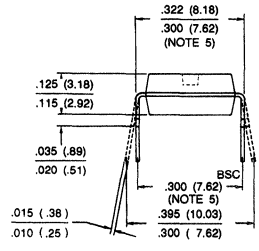




NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

NN1 PLASTIC PDIP-24

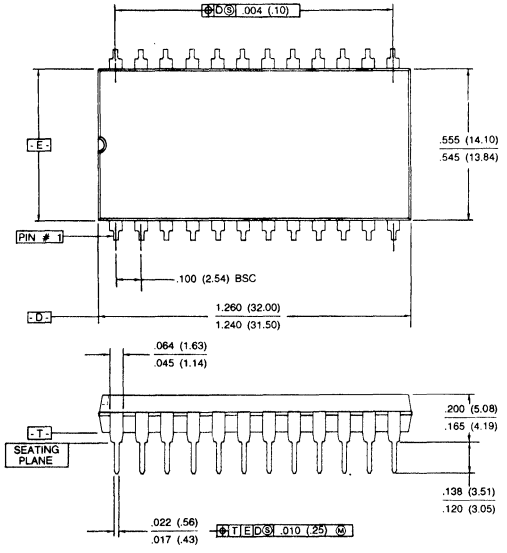




NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AR for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

Package Outlines

NN3 PLASTIC PDIP-24

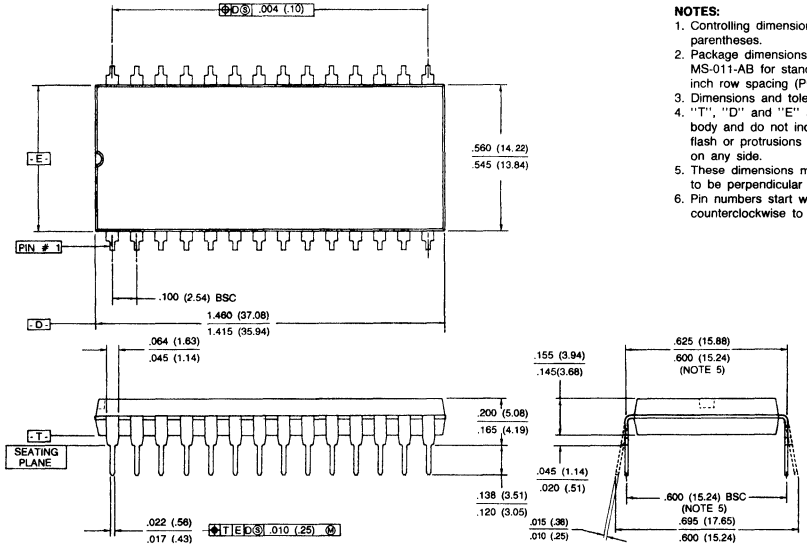


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AA for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0412/081238

PO00361S

NQ3 PLASTIC PDIP-28



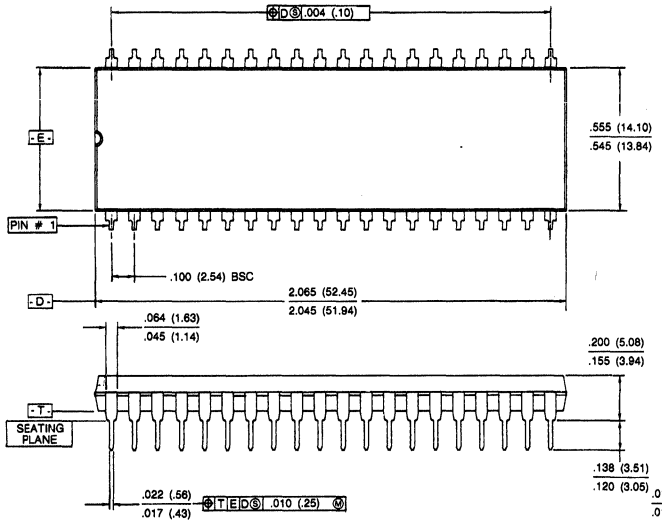
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0413/081239

PO00371S

Package Outlines

NW3 PLASTIC PDIP-40



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AC for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 40 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #40 when viewed from the top.

853-0415/081241

PO00381S

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