

1986
1987

Linear and Conversion Products

Linear and Conversion Products

1986/1987
Data Book

Precision
Monolithics
Inc.

Operational
Amplifiers
Instrumentation
Amplifiers
Voltage Followers/
Buffers
Voltage
Comparators
Matched
Transistors

Voltage
References
Digital-to-Analog
Converters
Analog-to-Digital
Converters
Analog Switches/
Multiplexers

Sample-and-Hold
Amplifiers
Special
Functions
Communications
Products



Alpha- numeric Index

Part Number	Page
ADC-910	12-7
ADC-8208	12-19
AMP-01	6-5
AMP-05	6-27
BUF-03	7-4
CMP-01	8-6
CMP-02	8-14
CMP-04	8-22
CMP-05	8-30
CMP-07	8-37
CMP-404	8-40
DAC-01	11-10
DAC-02	11-14
DAC-03	11-14
DAC-05	11-14
DAC-06	11-19
DAC-08	11-23
DAC-10	11-34
DAC-20	11-42
DAC-86	11-50
DAC-88	11-58
DAC-89	11-67
DAC-100	11-76
DAC-208	11-84
DAC-210	11-88
DAC-312	11-92
DAC-888	11-104
DAC-1408	11-116
DAC-1508	11-116
DAC-8012	11-122
DAC-8212	11-131
DAC-8408	11-136
DMX-88	13-74
GAP-01	15-4
JM38510/10104	5-273
JM38510/10106	5-276
JM38510/11004	5-279
JM38510/11301	11-209
JM38510/11302	11-209
JM38510/11401	5-282
JM38510/11402	5-282

JM38510/11403	5-282
JM38510/11404	5-282
JM38510/11405	5-282
JM38510/11406	5-282
JM38510/13501	5-292
JM38510/13502	5-292
JM38510/13503	5-295
MAT-01	9-5
MAT-02	9-11
MAT-04	9-23
MUX-08	13-48
MUX-16	13-59
MUX-24	13-48
MUX-28	13-59
MUX-88	13-69
OP-01	5-12
OP-02	5-18
OP-04	5-26
OP-05	5-34
OP-06	5-43
OP-07	5-51
OP-08	5-61
OP-09	5-68
OP-10	5-75
OP-11	5-68
OP-12	5-87
OP-14	5-26
OP-15	5-91
OP-16	5-91
OP-17	5-91
OP-20	5-105
OP-21	5-111
OP-22	5-117
OP-27	5-128
OP-32	5-140
OP-37	5-152
OP-41	5-164
OP-43	5-175
OP-50	5-180
OP-77	5-191
OP-90	5-197
OP-207	5-199
OP-215	5-205
OP-220	5-212
OP-221	5-220
OP-227	5-228
OP-400	5-239
OP-420	5-241
OP-421	5-246
PKD-01	15-19
PM-108	5-252

PM-111	8-48
PM-119	8-54
PM-139	8-56
PM-146	5-256
PM-155	5-259
PM-156	5-259
PM-157	5-259
PM-208	5-252
PM-211	8-48
PM-219	8-54
PM-246	5-256
PM-308	5-252
PM-319	8-54
PM-339	8-56
PM-355	5-259
PM-356	5-259
PM-357	5-259
PM-562	11-140
PM-565	11-148
PM-725	5-265
PM-741	5-268
PM-747	5-270
PM-2108	5-252
PM-7226	11-149
PM-7524	11-150
PM-7528	11-159
PM-7533	11-175
PM-7541	11-185
PM-7542	11-195
PM-7543	11-196
PM-7545	11-197
PM-7548	11-208
PM-7645	11-197
REF-01	10-4
REF-02	10-11
REF-03	10-19
REF-05	10-21
REF-10	10-22
RPT-82	16-4
RPT-83	16-4
SMP-10	14-6
SMP-11	14-6
SMP-81	14-15
SW-01	13-7
SW-02	13-7
SW-05	13-14
SW-06	13-22
SW-201	13-33
SW-202	13-33
SW-7510	13-40
SW-7511	13-40



Applications Subject Index

This index provides an easy reference to all application circuits that are in the PMI 1986/1987 Data Book. It may be attached to the title page. To attach, remove strip and press on firmly.

Circuit Function	Page
Absolute Value Circuit	5-24, 5-60, 15-13
Ammeter, Low-Current	5-173
Amplifier	
Buffer	5-190, 7-10
Composite Amplifier	5-59
Differential Input/Output	6-23
Driver	5-190, 6-19
Gated	5-125
Instrumentation	5-42, 5-85/86, 5-126, 5-160, 5-218, 5-219, 5-236/238, 6-22, 6-23, 6-26, 9-31
Integrator	5-190
Inverting	6-24
Logarithmic	9-22
Low-Noise	9-22
Microphone	5-138, 5-139, 5-163
Micropower	5-151
Peak Detector	15-36
Piezo-Electric Transducer	5-173
Precision	6-23
Programmable Gain	11-184, 13-39
Phono RIAA	5-137, 5-162
Sample and Hold	7-10, 13-31, 15-14
Summing	5-59
Tape Head	5-138, 5-162
Temperature Transducer	10-17
Thermocouple Amplifier	5-60
Vector-Summer	9-30
Wideband, Micropower	1-151
Analog Switch	8-46
Isolation	13-32
Single Supply	13-31
Analog-to-Digital Converter	
Companding AD/DA Converter System	11-65
Compressing	11-53
Dual Slope	13-13
High-Speed	8-36, 11-103
Peak-Reading	15-36
Sign-Magnitude, 10-Bit	11-91
Software SAR	11-114
Tracking	8-13, 11-83
Analog-to-Digital Divider	11-158, 11-194

Attenuator	
Audio	11-87
Telephone, Digitally Controlled	11-174
Voltage Controlled	9-32
Audio Attenuator	11-87
Auto-Zero Instrumentation Amplifier	6-26
Booster, Power	5-17
Buffer Amplifier	5-190, 7-10
Bulk Resistance Compensation	9-19
CODEC PCM Encoder	13-72, 14-21
Companding AD/DA Converter System	11-65
Compensation, Bulk Resistance	9-19
Composite Amplifier	5-59
Compressing A/D Converter	11-53
Converter	
Analog-to-Digital	8-13, 8-36, 11-53, 11-65, 11-66, 11-83, 11-91, 11-103, 11-114, 13-13, 15-36
Companding AD/DA System	11-65
Compressing A/D	11-53
Current-to-Voltage	5-104, 5-172
DC/DC, Regulated	8-47
Digital-to-Analog	11-65, 15-15
4-20mA Output D/A	11-146
Multifunction	9-21
Voltage-to-Current	6-21
Current Ammeter	5-173
Current Integrator	5-190
Current Mirror	9-28
Current-to-Voltage Converter	5-104, 5-172
Current Sink	9-29, 10-9
Current Source	
Bilateral	5-67, 5-190, 6-21
Source	10-9
Current Transmitter, 4-20mA	5-126, 6-21, 11-146
DC/DC Converter	8-47
Demodulator, LVDT	15-16
Differential Input/Output Amplifier	6-23
Digitally Controlled 4-20mA Transmitter	11-146
Digitally Controlled Gain Divider	11-158, 11-194
Digitally Controlled R.F. Generator	11-147
Digitally Controlled Telephone Attenuator	11-174

Digitally Programmable Window-Comparator	11-173
Divider, Analog-to-Digital	11-194
Divider/Multiplier	9-18
Driver, 50Ω Load	5-190, 6-19
Dual Slope A/D Converter	13-13
Filter	
Low-Pass, Programmable	13-47
Notch, High-Q	5-173
4-20mA Current Transmitter	5-126, 6-21, 11-146
Gain Divider, Digitally Controlled	11-158, 11-194
Instrumentation Amplifier	5-42, 5-85, 5-86
Auto-Zero	6-26
Micropower	5-126, 5-218, 5-219
High Output Current	6-22, 6-23
High-Speed	5-160, 9-31
Low-Noise	5-236/238, 9-31
Programmable Gain	6-22
Integrator	5-190
Isolation Switch	13-32
Light Detector	5-171
Linearization, Photo-Diode A/D Converter	11-66
Logarithmic Amplifier	9-22
Low-Noise Amplifier	9-22
Low-Noise Instrumentation Amplifier	9-31
Low-Pass Filter, Programmable	13-47
LVDT Signal Demodulator	15-16
Microphone Amplifier	5-138, 5-139, 5-163
Multifunction Converter	9-21
Multiplier/Divider	9-18, 9-20
Noise Test Circuit	5-64
Oscillator	8-28, 8-47
R.F., Digitally Controlled	11-147
Wien Bridge	5-127
PCM Encoder	13-72, 14-21
Peak Detector	15-30/36
Peak-Reading A/D Converter	15-36
Phono Amplifier, RIAA	5-137, 5-162
Photo Detector Amplifier	5-171
Photo-Diode Linearizing A/D Converter	11-66
Piezo-Electric Transducer Amplifier	5-173
Power Booster	5-17

Programmable Absolute Value Circuit	15-13
Programmable Gain Amplifier	11-184, 13-39
Programmable Gain Divider	11-158
Programmable Gain Instrumentation Amplifier	6-22
Programmable Ramp Generator	15-37
Programmable Window Comparator	11-173
Ramp Generator, Programmable	15-37
Repeater System, 1.544 MHz	16-9
R.F. Generator, Digitally Controlled	11-147
RIAA Phono Amplifier	5-137, 5-162
Sample and Hold Amplifier	
Multi-Channel	13-31, 15-14
High-Speed	7-10
Summing Amplifier	5-59
Switch, Analog	8-46, 13-31, 13-32
Tape-Head Amplifier	5-138
Temperature Controller	10-17
Temperature Sensor	5-110
Temperature Transducer Amplifier	10-17
Thermocouple Amplifier	5-60
Time Delay Generator	8-29
Transmitter, 4-20mA Current	5-126, 6-21
Vector-Summing Amplifier	9-30
Voltage Comparator	8-27, 11-81
High-Sensitivity	5-189
Window Comparator	8-21, 8-45, 11-173, 15-17
Voltage Controlled Attenuator	9-32
Voltage Reference	
High Stability	5-24
Dual Tracking	5-86
Micropower 1.23 Volt	5-125
+3 Volt	10-18
+10 Volt	10-9
Voltage Regulated DC/DC Converter	8-47
Voltage Regulator, Micropower	5-127
Voltage-to-Current Converter	6-21
Wien-Bridge Oscillator	5-127
Window Comparator	8-21, 8-45, 11-173, 15-17

Linear and Conversion Products

1986/1987
Data Book

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Table of Contents 1

Ordering Information 2

Product Assurance Program 3

Industry Cross Reference 4

Operational Amplifiers 5

Instrumentation Amplifiers 6

Voltage Followers/Buffers 7

Voltage Comparators 8

Matched Transistors 9

Voltage References 10

Digital-to-Analog Converters 11

Analog-to-Digital Converters 12

Analog Switches/Multiplexers 13

Sample-and-Hold Amplifiers 14

Special Functions 15

Communications Products 16

Package Information 17

Sales Offices, Representatives and Distributors 18



TABLE OF CONTENTS

Precision Monolithics Inc.

Section 2 Ordering Information

- 2-2 Package Products Part Numbering System
- 2-3 Dice Part Numbering System
- 2-4 Dice Information
- 2-5 Reliability Information
- 2-6 Discontinued Device Types Ordering Guide

Section 3 Product Assurance Program

- 3-3 Introduction
- 3-3 Processing

Section 4 Industry Cross Reference

- 4-2 Alphanumeric Direct Replacement Guide

Section 5 Operational Amplifiers

- 5-4 Introduction
- 5-4 Definitions
- 5-6 Selection Guide
- 5-12 **OP-01**

Inverting High-Speed Operational Amplifier
- 5-18 **OP-02**

General-Purpose Operational Amplifier

Section 5 continued

- 5-26 **OP-04/OP-14**

Dual Matched High-Performance Operational Amplifiers
- 5-34 **OP-05**

Instrumentation Operational Amplifier
- 5-43 **OP-06**

High-Gain Instrumentation Operational Amplifier
- 5-51 **OP-07**

Ultra-Low Offset Voltage Operational Amplifier
- 5-61 **OP-08**

Precision Low-Input-Current Operational Amplifier
- 5-68 **OP-09/OP-11**

Quad Matched 741-Type Operational Amplifiers
- 5-75 **OP-10**

Dual Matched Instrumentation Operational Amplifier
- 5-87 **OP-12**

Precision Low-Input-Current Operational Amplifier
- 5-91 **OP-15/OP-16/OP-17**

Precision JFET-Input Operational Amplifiers
- 5-105 **OP-20**

Micropower Operational Amplifier
- 5-111 **OP-21**

Low-Power Operational Amplifier



TABLE OF CONTENTS

Precision Monolithics Inc.

Section **5** continued

5-117	OP-22
	Programmable Micropower Operational Amplifier
5-128	OP-27
	Low-Noise Precision Operational Amplifier
5-140	OP-32
	High-Speed Programmable Micropower Operational Amplifier
5-152	OP-37
	Low-Noise Precision High-Speed Operational Amplifier
5-164	OP-41
	Low-Bias-Current JFET Operational Amplifier
5-175	OP-43
	Low-Bias-Current, Fast JFET Operational Amplifier
5-180	OP-50
	High-Output-Current Operational Amplifier
5-191	OP-77
	Next Generation OP-07 (Ultra-Low Offset Voltage Operational Amplifier)
5-197	OP-90
	Low-Voltage Micropower Operational Amplifier
5-199	OP-207
	Dual Ultra-Low V_{OS} Matched Operational Amplifier
5-205	OP-215
	Dual Precision JFET-Input Operational Amplifier

Section **5** continued

5-212	OP-220
	Dual Micropower Operational Amplifier
5-220	OP-221
	Dual Low-Power Operational Amplifier
5-228	OP-227
	Dual Low-Noise Low-Offset Instrumentation Operational Amplifier
5-239	OP-400
	Quad Low-Offset Low-Power Operational Amplifier
5-241	OP-420
	Quad Micropower Operational Amplifier
5-246	OP-421
	Quad Low-Power Operational Amplifier
5-252	PM-108A/PM-208A/PM-308A/ PM-108/PM-208/PM-308/ PM-2108A/PM-2108
	Low-Input-Current Operational Amplifiers
5-256	PM-146/PM-246
	Programmable Quad Operational Amplifiers
5-259	PM-155A/PM-355A/PM-155/ PM-156A/PM-356A/PM-156/ PM-157A/PM-357A/PM-157
	Monolithic JFET-Input Operational Amplifiers
5-265	PM-725
	Instrumentation Operational Amplifier
5-268	PM-741
	Compensated Operational Amplifier



TABLE OF CONTENTS

Precision Monolithics Inc.

Section 5 continued

-
- 5-270 **PM-747**
Dual Compensated
Operational Amplifier
-
- 5-273 **JM38510/10104**
JAN Single Low-Input-Current
Operational Amplifier
-
- 5-276 **JM38510/10106**
JAN Dual Low-Input-Current
Operational Amplifier
-
- 5-279 **JM38510/11004**
JAN Quad 741-Type
Operational Amplifier
-
- 5-282 **JM38510/11401/11402/11403/11404/
11405/11406**
JAN JFET-Input Operational Amplifiers
-
- 5-292 **JM38510/13501/13502**
Ultra-Low Offset Voltage
Operational Amplifiers
-
- 5-295 **JM38510/13503**
Low-Noise Precision
Operational Amplifier

Section 6 **Instrumentation Amplifiers**

-
- 6-3 Introduction
-
- 6-3 Definitions
-
- 6-5 **AMP-01**
Low-Noise Precision
Instrumentation Amplifier
-
- 6-27 **AMP-05**
Fast-Settling JFET
Instrumentation Amplifier

Section 7 **Voltage Followers/Buffers**

-
- 7-3 Introduction
-
- 7-4 **BUF-03**
High-Speed Voltage Follower/Buffer

Section 8 **Voltage Comparators**

-
- 8-3 Introduction
-
- 8-3 Definitions
-
- 8-6 **CMP-01**
Fast Precision Comparator
-
- 8-14 **CMP-02**
Low-Input-Current
Precision Comparator
-
- 8-22 **CMP-04**
Quad Low-Power Precision Comparator
-
- 8-30 **CMP-05**
High-Speed Precision Comparator
-
- 8-37 **CMP-07**
Very High-Speed Comparator
-
- 8-40 **CMP-404**
Quad Low-Power Precision Comparator
-
- 8-48 **PM-111/PM-211**
Precision Voltage Comparators
-
- 8-54 **PM-119/PM-219/PM-319**
Dual Comparators
-
- 8-56 **PM-139/PM-139A/PM-339A**
Quad Low-Power Voltage Comparators



Section 9 Matched Transistor Arrays

- 9-3 Introduction
- 9-3 Definitions
- 9-4 Parameter Comparison Tables
- 9-5 **MAT-01**
Matched Monolithic Dual Transistor
- 9-11 **MAT-02**
Low-Noise, Matched Dual Monolithic Transistor
- 9-23 **MAT-04**
Matched Monolithic Quad Transistor

Section 10 Voltage References

- 10-3 Introduction
- 10-3 Definitions
- 10-4 **REF-01**
+10V Precision Voltage Reference
- 10-11 **REF-02**
+5V Precision Voltage Reference/Temperature Transducer
- 10-19 **REF-03**
+2.5V Precision Voltage Reference
- 10-21 **REF-05**
+5V Precision Voltage Reference
- 10-22 **REF-10**
+10V Precision Voltage Reference

Section 11 Digital-to-Analog Converters

- 11-4 Introduction
- 11-4 Definitions
- 11-8 Selection Guide
- 11-10 **DAC-01**
6-Bit Voltage-Output D/A Converter
- 11-14 **DAC-02/DAC-03/DAC-05**
10-Bit-Plus-Sign Voltage-Output D/A Converters
- 11-19 **DAC-06**
Two's-Complement 10-Bit Voltage-Output D/A Converter
- 11-23 **DAC-08**
8-Bit High-Speed Multiplying D/A Converter
- 11-34 **DAC-10**
10-Bit High-Speed Multiplying D/A Converter
- 11-42 **DAC-20**
2-Digit BCD High-Speed Multiplying D/A Converter
- 11-50 **DAC-86**
COMDAC® Companding D/A Converter
- 11-58 **DAC-88**
COMDAC® Companding D/A Converter
- 11-67 **DAC-89**
COMDAC® Companding D/A Converter

Section **11** continued

11-76	DAC-100 10-Bit Current-Output D/A Converter
11-84	DAC-208 9-Bit Voltage-Output D/A Converter
11-88	DAC-210 11-Bit Voltage-Output D/A Converter
11-92	DAC-312 12-Bit High-Speed Multiplying D/A Converter
11-104	DAC-888 BYTEDAC® 8-Bit High-Speed "Microprocessor Compatible" Multiplying D/A Converter
11-116	DAC-1508A/1408A 8-Bit Multiplying D/A Converters
11-122	DAC-8012 CMOS 12-Bit Multiplying D/A Converter "With Memory"
11-131	DAC-8212 Dual 12-Bit Buffered Multiplying CMOS D/A Converter
11-136	DAC-8408 Quad 8-Bit Multiplying CMOS D/A Converter With Memory
11-140	PM-562 12-Bit Multiplying Current-Output D/A Converter
11-148	PM-565A Complete High-Speed 12-Bit Monolithic D/A Converter

Section **11** continued

11-149	PM-7226 Quad 8-Bit CMOS D/A Converter With Voltage Output
11-150	PM-7524 CMOS 8-Bit Buffered Multiplying D/A Converter
11-159	PM-7528 Dual 8-Bit Buffered Multiplying CMOS D/A Converter
11-175	PM-7533 CMOS Low Cost 10-Bit Multiplying D/A Converter
11-185	PM-7541 CMOS 12-Bit Monolithic Multiplying D/A Converter
11-195	PM-7542 12-Bit Multiplying CMOS D/A Converter
11-196	PM-7543 12-Bit Serial-Input Multiplying CMOS D/A Converter
11-197	PM-7545/PM-7645 12-Bit Buffered Multiplying CMOS D/A Converters
11-208	PM-7548 12-Bit Multiplying CMOS D/A Converter
11-209	JM38510/11301/11302 JAN 8-Bit Multiplying D/A Converters

Section 12 Analog-to-Digital Converters

12-3 Introduction

12-3 Definitions

12-7 ADC-910

High-Speed "Microprocessor Compatible" A/D Converter

12-19 ADC-8208

Microprocessor-Compatible 8-Bit CMOS A/D Converter

Section 13 Analog Switches/Multiplexers

13-3 Introduction

13-3 Definitions

13-7 SW-01/SW-02

Quad SPST JFET Analog Switches

13-14 SW-05

Dual SPST JFET Analog Switch

13-22 SW-06

Quad SPST JFET Analog Switch

13-33 SW-201/SW-202

Quad SPST JFET Analog Switches

13-40 SW-7510/SW-7511

Quad SPST JFET Analog Switches

13-48 MUX-08/MUX-24

8-Channel/Dual 4-Channel JFET Analog Multiplexers

13-59 MUX-16/MUX-28

16-Channel/Dual 8-Channel JFET Analog Multiplexers

Section 13 continued

13-69 MUX-88

8-Channel Analog Multiplexer For PCM CODECs

13-74 DMX-88

8-Channel Analog De-Multiplexer

Section 14 Sample-and-Hold Amplifiers

14-3 Introduction

14-3 Definitions

14-6 SMP-10/SMP-11

Low-Droop-Rate/Accurate Sample-and-Hold Amplifiers

14-15 SMP-81

Telecommunications Sample-and-Hold Amplifier

Section 15 Special Functions

15-3 Introduction

15-3 Definitions

15-4 GAP-01

General-Purpose Analog Signal Processing Subsystem

15-19 PKD-01

Monolithic Peak Detector



TABLE OF CONTENTS

Precision Monolithics Inc.

Section 16 Communications Products

- 16-3 Introduction
- 16-4 **RPT-82/RPT-83**
PCM Repeaters

Section 17 Package Information

Metal Cans

- 17-3 6-Lead TO-78 Metal Can
- 17-3 8-Lead TO-99 Metal Can
- 17-3 10-Lead TO-100 Metal Can

Ceramic DIPs

- 17-4 8-Lead Ceramic DIP
- 17-4 14-Lead Ceramic DIP
- 17-5 16-Lead Ceramic DIP
- 17-5 18-Lead Ceramic DIP
- 17-6 20-Lead Ceramic DIP
- 17-7 24-Lead Ceramic DIP
- 17-8 28-Lead Ceramic DIP

Side-Brazed DIPs

- 17-9 14-Lead Side-Brazed DIP
- 17-9 16-Lead Side-Brazed DIP
- 17-10 18-Lead Side-Brazed DIP
- 17-10 20-Lead Side-Brazed DIP
- 17-11 24-Lead Side-Brazed DIP
- 17-12 28-Lead Side-Brazed DIP

Epoxy DIPs

- 17-13 8-Lead Epoxy DIP
- 17-13 14-Lead Epoxy DIP
- 17-14 16-Lead Epoxy DIP
- 17-14 18-Lead Epoxy DIP
- 17-15 20-Lead Epoxy DIP
- 17-16 24-Lead Epoxy DIP

Section 17 continued

Cerpacks

- 17-17 10-Lead Cerpack
- 17-17 14-Lead Cerpack
- 17-18 16-Lead Cerpack
- 17-18 24-Lead Cerpack

Flatpacks

- 17-19 10-Lead Flatpack
- 17-19 10-Lead Flatpack, Bottom-Brazed
- 17-19 14-Lead Flatpack
- 17-19 14-Lead Flatpack, Bottom-Brazed
- 17-20 16-Lead Flatpack
- 17-20 16-Lead Flatpack, Bottom-Brazed
- 17-20 24-Lead Flatpack
- 17-20 24-Lead Flatpack, Bottom-Brazed

Leadless Chip Carriers

- 17-21 20-Position Chip Carrier
- 17-22 28-Position Chip Carrier

Section 18 Sales Offices, Representatives, and Distributors

- 18-2 Sales Offices, Representatives
North America
- 18-4 Authorized Distributors
North America
- 18-6 Sales Offices, Representatives
International
- 18-7 Authorized Distributors
International

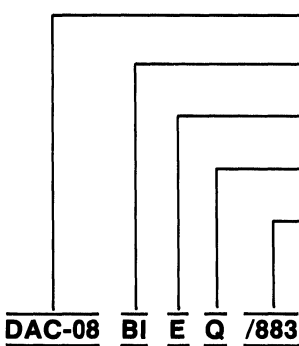
Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



ORDERING INFORMATION

Precision Monolithics Inc.

PACKAGED PRODUCTS PART NUMBERING SYSTEM



Device Type & Model Number

Burn-In Option

Electrical Grade

Package Suffix

MIL-STD-883, Class B, Revision C Option

PMI -55°C to +125°C devices are available with MIL-STD-883, Class B, Revision C screening as standard products. To order an 883 part, simply add the designation /883 to the part number. For example, the DAC-08AQ, screened to the 883 requirements would be ordered as a DAC-08AQ/883. Contact factory for 883 device specifications.

Package Type

- | | |
|--------------------------------|--------------------------------|
| H = 6 lead TO-78 Can | S = Not used |
| J = 8 lead TO-99 Can | T = 28 lead Ceramic DIP |
| K = 10 lead TO-100 Can | TC = 28 position LCC* |
| O = Not used | U = Not used |
| P = Epoxy DIP | V = 24 lead Ceramic DIP |
| Q = 16 lead Ceramic DIP | X = 18 lead Ceramic DIP |
| R = 20 lead Ceramic DIP | Y = 14 lead Ceramic DIP |
| RC = 20 position LCC* | Z = 8 lead Ceramic DIP |

*Available on certain 883 products

Note: See more complete listing on page 17-2.

Select electrical grade from data sheet.

PMI offers all 0°/70°C and -25°/+85°C devices with burn-in per method 1015.5 of MIL-STD-883, 160 hours at +125°C or 80 hours at +150°C at PMI's option. Parts with this option are specified with the letters BI added between the model number and the electrical grade. For example, to order DAC-08EQ with burn-in, the part number is DAC-08BIEQ.

Device types are listed on next page. Select model number from product listings.

MIL-M-38510

PMI's factory is certified to produce JAN parts per MIL-M-38510. Consult factory for availability of specific slash sheet part numbers. At this writing, devices with Part 1 or Part 2 approval include PM-155A, PM-156A, PM-157A, PM-108A, PM-2108A, PM-4136, DAC-08, OP-07, and OP-27. Other types are being qualified.

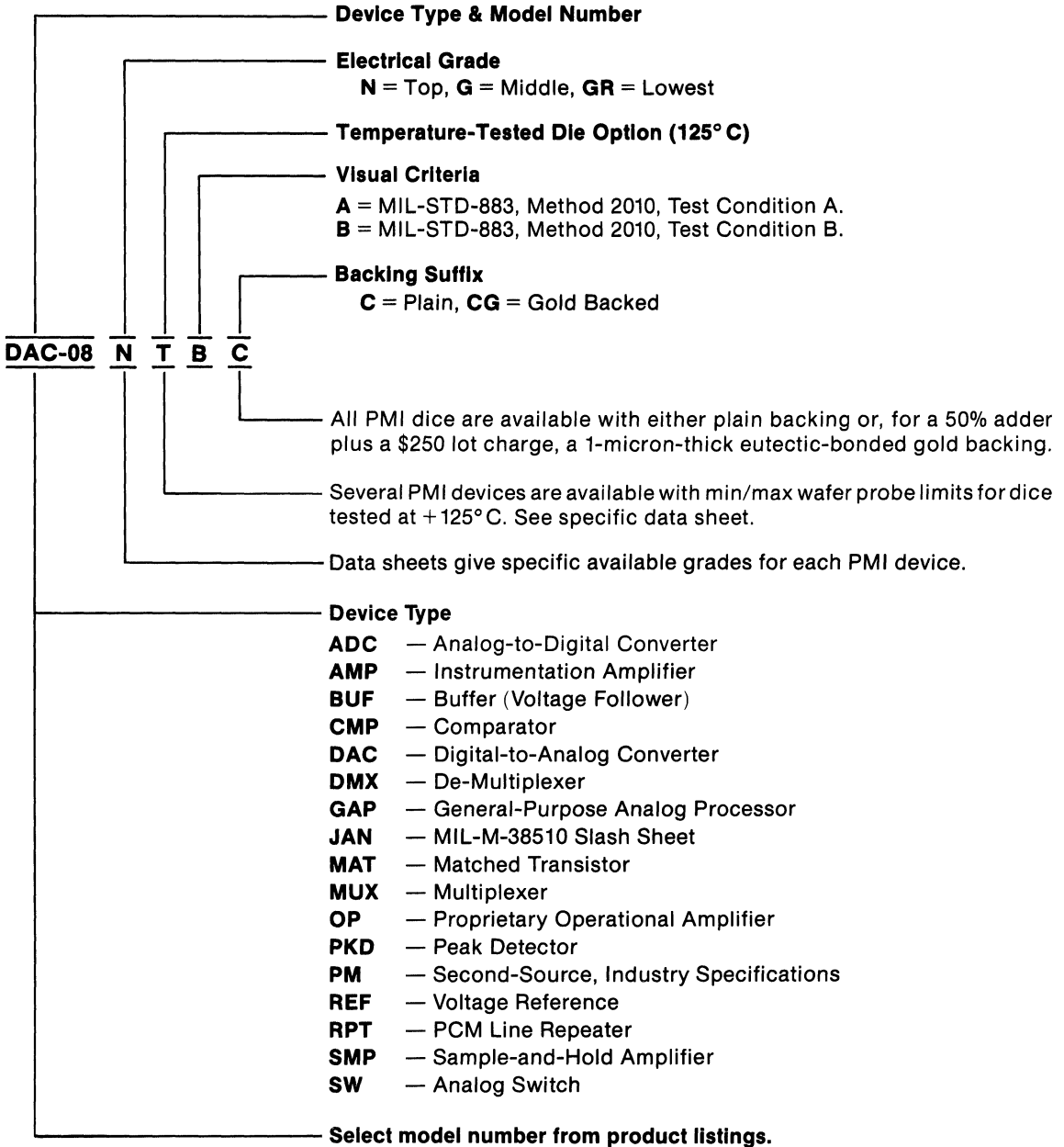
See Table of Contents for JAN data sheet listings.



ORDERING INFORMATION

Precision Monolithics Inc.

DICE PART NUMBERING SYSTEM



ORDERING INFORMATION



ORDERING INFORMATION

Precision Monolithics Inc.

DICE INFORMATION

Triple Passivation

Triple Passivation is a three-step process which provides superior reliability and protection for all PMI integrated circuits. First, a specially treated thermal silicon dioxide layer is grown. This protects the junctions and also attracts any residual ionic impurities to the top surface of the oxide, where they are held fixed. Next, a layer of silicon nitride is applied to prevent the entry of any potential contamination or impurities. The third step is the thick glass overcoat layer which leaves only the bonding pads exposed. This "glassivation" protects the die from damage during assembly and is especially important in minimizing yield loss during shipment and assembly of dice for hybrid circuits.

Quality Assurance

PMI believes that quality and reliability must be built into the product; no amount of testing can replace these inherent properties. For this reason, devices are fabricated and processed with many exclusive processes and controls added to improve quality and reliability. The integrity of aluminum metallization is confirmed by sampling wafer lots using Scanning Electron Microscope (SEM) examinations per Method 2018 specifications.

Mechanical Information

Aluminum metallization with a nominal thickness of 10,000 angstroms is standard for all devices. Die thickness is 19 mils minimum to 21 mils maximum. Minimum bonding pad size is 4.0 mils X 4.0 mils for all devices.

Visual Inspection

All dice are 100% visually inspected to the applicable visual criteria per MIL-STD-883 Method 2010, Condition B.

Electrical Testing

All dice are 100% tested to the 25° C DC wafer test limits shown in this catalog before the wafer

is separated into individual dice. Due to variations in assembly methods and normal yield loss, PMI does not guarantee specifications after packaging for standard dice. Sample assembly and testing in standard PMI packages to specified LTPD's and min/max specifications are available at extra cost. Consult factory for dice lot qualification negotiation.

Shipping

Protection during shipment is provided by a waferpack carrier with anti-static shield and cushioning strip. In addition, the waferpack is vacuum sealed in a polyethylene bag.

Military/Aerospace Applications

PMI devices are widely used in military and aerospace programs. A partial listing includes:

Military Aircraft

F-4	F-11
B-1B	F-15
Sikorsky UH-60A	B-52
A-10	F-18
Sikorsky SH-3	Alpha Jet
YC-15	E-3A
P-3	F-16
S-3A	F-5
KC-10	Tornado

Missile/Spacecraft

Viking (Mars Orbitor)	Milstar Voyager (Jupiter/Saturn)
Aerosat	Stinger Missile
Harm Missile	Standard Missile II
DSCS-3	Tiros-N
Sparrow Missile	Cruise Missile
Trident	Ariane
TDRSS	Roland
TV SAT	Eurosat
Intelsat 5	Space Shuttle
Minuteman	



ORDERING INFORMATION

Precision Monolithics Inc.

2

Electronic Systems

Omega	A4KU
Tram	MK-48
Aims (MK86)	B-52 Radar Mod
F-16	Pathfinder Radar
(Ground Support)	MK-46
Pave Spike	Seaguard
AWACS	Gepard

Miscellaneous

RFP Model 35 #13	Cutty Sark
Project 4620	Compass Tie
Heads-Up Display	System 27
DST 1860	ACM
Walleye	VCS
PMS	Naval Submarine
Aerial Surveillance Camera	Periscope

RELIABILITY INFORMATION

MIL-STD-883C

PMI standard "883" parts are manufactured to be in full compliance with all MIL-STD-883 requirements. See Section 3 for more details.

Specials

At PMI, we have a proven track record for handling "customer specials". Many IC manufacturers shy away from processing precision linear

ICs to the unique in-house specifications of their customers. PMI recognizes your special needs and welcomes the opportunities provided by the military/aerospace industry. Hi-rel is a cornerstone of PMI's business and we will continue to offer the extra processing that your applications require.

Radiation Resistance

As a leading supplier of precision linear ICs to the military/aerospace industry, PMI is supportive of the system designer's needs for readily available, standard components that are radiation resistant. A number of standard PMI linear integrated circuits have characteristically demonstrated good resistance to radiation. These devices have been subjected to radiation levels necessary to perform effectively in military/aerospace radiation environments, and they are now being used in a number of demanding military and space programs.

Experiments to isolate the processing mechanisms that led to PMI's increased radiation hardness characteristics have pointed heavily toward the use of a silicon nitride passivation layer. While we do not believe that this process is the only radiation hardening advantage of PMI devices, it does add a great deal to survivability.

For more information request PMI's "Radiation Resistance" brochure.

ORDERING INFORMATION



ORDERING INFORMATION

Precision Monolithics Inc.

DISCONTINUED DEVICE TYPES ORDERING GUIDE

Between 1978 and 1985 some device types, individual grades, and package options were discontinued. This guide is provided to help the designer to select an appropriate alternative device.

Type	Alternative Device Type	Note(s)
BUF-01	OP-07 connected as a voltage follower.	—
BUF-02	OP-16 connected as a voltage follower.	—
DAC-04	DAC-06 nearest grade.	1
DAC-76	DAC-86 nearest grade.	1, 2
DAC-78	DAC-88EX.	1
DAC-87	DAC-89EX.	3
DAC-101	DAC-100 "Q3" nearest grade.	1
DAC-206	DAC-01 nearest grade.	1
DAC-808	DAC-888 is the most similar device.	—
OP-03	OP-04 with externally-connected V+ pins.	1
OP-18	LM101 is the most similar device.	—
OP-19	MC1741S is the most similar device.	—
OP-24	OP-27GP, improved replacement.	1
OP-34	OP-37GP, improved replacement.	1
PM-1458	OP-14 nearest grade.	1
PM-1558	OP-14 nearest grade.	1
PM-4136	OP-09 nearest grade.	1
SSS-725	OP-06 or PM-725 nearest grade.	1
SSS-741	OP-02 nearest grade.	1
SSS-747	OP-04 or PM-747 nearest grade.	1
SSS-1458	OP-14 nearest grade.	1
SSS-1558	OP-14 nearest grade.	1
SW-03	SW-06 is a functional replacement.	—
SW-04	SW-06 is a functional replacement.	—

Note 1. Direct, pin-for-pin replacement. No design changes required.

Note 2. DAC-76 -55°C/+125°C types may be ordered as DAC-86 specials.

Note 3. DAC-89EX has idling currents on the outputs requiring matched load resistors. DAC-89EX has higher speed and accuracy and is an improved, direct, pin-for-pin replacement for DAC-87 in most designs.

Package Type	Affected Device Type	Remarks
"K" (TO-100)	PM-747.	Available on Specials.
"N" (Flatpack)	DAC-100N9.	Available on Specials.
"Y" (14-pin DIP)	See list below.	Available on Specials.

"Y" Package Option: Affected Device Types

CMP-01	OP-02	PM-725
CMP-02	OP-06	PM-741
OP-01	OP-220	

The "Y" package option was discontinued for some products. They are all available in other package types including "J" (TO-99), "P" (Epoxy DIP), or "Z" (Ceramic 8-pin Mini-DIP). See individual data sheets for available package options for each device.

Discontinued-Electrical-Grade Ordering Guide

The following electrical grades were discontinued but are available with different specifications in the same packages. See individual data sheets.

CMP-01B	MAT-01F	PM-255
CMP-02B	OP-01E	PM-256
DAC-05B	OP-01F	PM-257
DAC-05F	OP-04GR	PM-339
DAC-20E	OP-08B	PM-355
DAC-88C	OP-08F	PM-356
DAC-89C	OP-09C	PM-357
DAC-100Q1	OP-09G	PM-2208
DAC-100Q2	PM-239	PM-2308
DAC-100DDQ5	PM-239A	REF-01D
DAC-100DDQ6		

Five volt output versions of DAC-02 and DAC-05, "X2" suffix, were discontinued. They may be ordered as DAC-03X2 specials.

Sixty volt breakdown versions of MAT-01 were discontinued (MAT-01H and MAT-01FH).

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



PRODUCT ASSURANCE

Precision Monolithics Inc.

3-3 Introduction

3-3 Processing



PRODUCT ASSURANCE

Precision Monolithics Inc.

INTRODUCTION

PMI has long been recognized as a High Quality/Reliability supplier of Commercial, Industrial and Military/Aerospace Products. The PMI Product Assurance Department plays a vital role in controlling processes to ensure the manufacture of highly reliable, cost-effective product, and to make certain that all pertinent customer specifications and requirements are met.

ORGANIZATION

Product Assurance Department of PMI is composed of four functional departments: Process Quality Control, Quality Assurance, Reliability, and Program Management.

RESPONSIBILITIES

Process Control — The primary responsibility of the Process Control Department is to establish and maintain effective controls over process integrity by monitoring manufacturing processes and equipment operation; to provide real-time feedback of information concerning the status of these controls; and to initiate statistically valid techniques to further improve quality and reliability levels. These concepts are used extensively throughout all manufacturing processes.

Quality Assurance (Standard and Hi-Rel) — The primary responsibility of the Quality Assurance Department is to assure that the delivered product meets PMI or Customer Product Standards of reliability and quality. Process monitors and gate inspections are designed so that all devices are properly tested and required sample tests are performed prior to shipment. Inspection records and reports concerning monitor and inspection data keep all cognizant personnel fully informed about the status of the quality level of products going through final test operations.

Reliability — The Reliability Department assures a high and consistent reliability of PMI products. The Reliability Department establishes, defines, and maintains evaluation programs to determine process/product reliability. The Reliability Department will issue periodic reports on the results of all evaluation testing. Contact the

nearest PMI Sales Office or the Literature Department for the latest issue of the PMI Reliability Bulletin.

The Reliability Department also performs failure analyses as required.

Program Management — The primary responsibility of the Program Management Department is to ensure that the MIL-M-38510 JAN Program and other special customer program requirements are met. This is accomplished by monitoring the in-house procedures used to define each process step of a particular program. If necessary, baselining documentation is written detailing specific procedures and processing flows. A Configuration Control System consisting of maintenance of PMI standard baselining for each device type, as well as notification to customers of major process and product changes, are also responsibilities of this group.

Contact the nearest PMI Sales Office or the Literature Department for a copy of the comprehensive PMI Product Assurance Manual.

QUALITY LEVELS

PMI processes to stringent quality standards. Quality guarantees range from parts-per-million on Standard Product to imposed Quality Levels dictated by customer specification on custom orders.

Current information on Quality Levels is available upon request; contact the nearest PMI Sales Office or the Literature Department.

PROCESSING

The cornerstone of the manufacturing of PMI hermetic products is the strict adherence to all requirements of MIL-STD-883, Level B, for our "883" product line. All PMI hermetic products, be they "full 883" or not, receive the benefit of MIL-STD-883 processing through assembly.

The manufacture of plastic devices is inherently different from hermetic in the area of assembly. Automation of the assembly line has produced a tightly process-controlled product that requires few interim inspections from wafer fabrication to pre-mold visual. Plastic product may also be obtained with a burn-in (BI) option (see Section 2, Ordering Information for further details).



Precision Monolithics Inc.

DATA SHEET SPECIFICATIONS

PMI standard product is guaranteed to meet the published limits under the test conditions shown in the data sheet. Where practical, PMI performs 100% testing of the indicated parameters; however, following accepted industry practice, certain parameters may be guaranteed by sample testing or by using design and/or characterization data.

PMI provides separate data sheets for all "883" products in strict conformance with MIL-STD-883, Method 5005.8 and MIL-M-38510F, Appendix B. Interim Electrical Test Parameters (pre-burn-in), Final Electrical Test Parameters, Group A Test Parameters, and guidelines used for PDA calculations, are all detailed in tabular form on the "883" data sheets.

It is highly recommended that the "883" data sheet be used as a baseline for new military or aerospace Source Control Drawings. Consult your sales representative to obtain these "883" data sheets.

TESTING

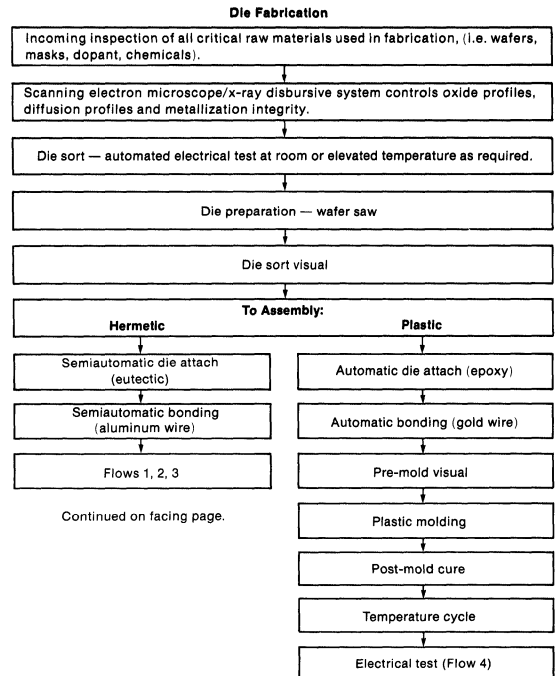
Testing of electrical parameters is generally performed using pulse testing techniques on automated test equipment. Unless otherwise specified, chip temperature remains close to the ambient temperature.

PROCESS CHANGE NOTIFICATION

PMI reviews all process, product, and package changes for possible impact on form, fit, or function. All major changes are submitted for a re-qualification, which may include electrical, mechanical, and/or thermal characterization. Where applicable, reliability re-qualification is performed.

Upon completion of this internal re-qualification, PMI informs all customers who have requested process change notification with a complete description of the change, along with applicable reliability or characterization data. Upon request, PMI will assist customers in their internal re-qualification effort.

STANDARD PROCESS FLOWS (JAN 38510, Class B, 883 Class B; PMI Industrial/Commercial)



Continued on facing page.

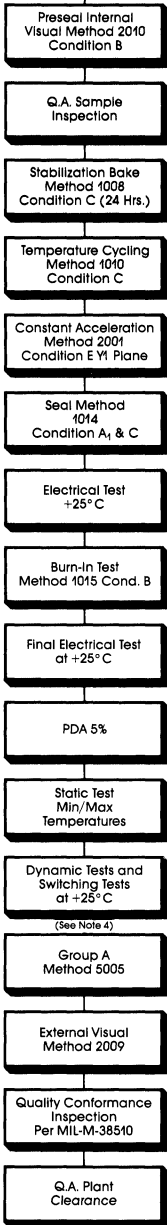
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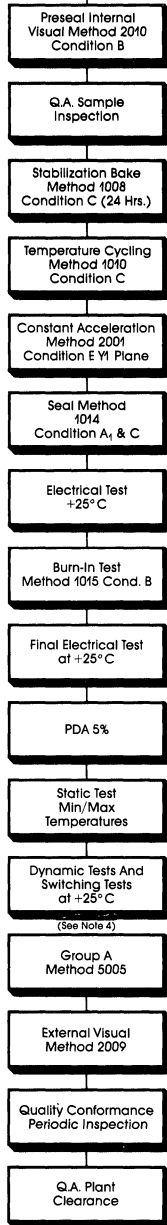
PRODUCT ASSURANCE

Precision Monolithics Inc.

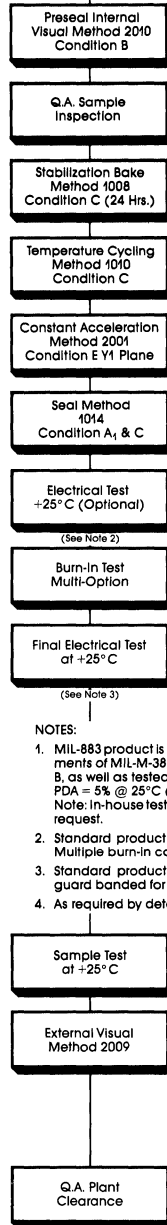
Flow 1
MIL-STD-883
METHOD 5004 CLASS B/
JAN 38510



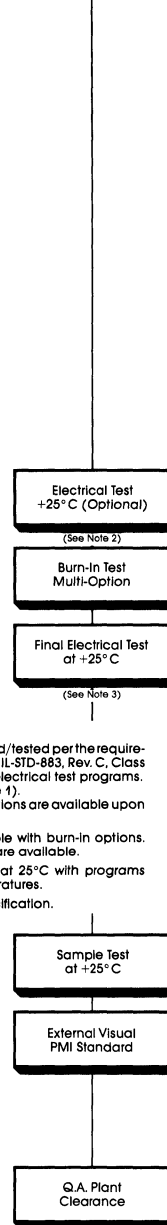
Flow 2
MIL-STD-883
METHOD 5004 CLASS B
(See Note 1)



Flow 3
PMI STANDARD
HERMETIC DEVICES



Flow 4
PMI STANDARD
PLASTIC DEVICES



NOTES:

- MIL-883 product is assembled/tested per the requirements of MIL-M-38510 and MIL-STD-883, Rev. C, Class B, as well as tested per PMI electrical test programs. PDA = 5% @ 25°C (Subgroup 1). Note: In-house test specifications are available upon request.
- Standard product is available with burn-in options. Multiple burn-in conditions are available.
- Standard product is tested at 25°C with programs guard banded for all temperatures.
- As required by detailed specification.

Country of Origin Assembly Codes: United States = S, Korea = K, Philippines = D, Puerto Rico = P



Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



ALPHANUMERIC DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>
AD108AH	PM108AJ	AD7524KN	PM7524HP	ADDAC08CD	DAC08CQ
AD108H	PM108J	AD7524LN	PM7524GP	ADDAC08D	DAC08Q
AD1408-7D	DAC1408A7Q	AD7524SD	PM7524BQ	ADDAC08ED	DAC08EQ
AD1408-8D	DAC1408A8Q	AD7524TD	PM7524BQ	ADDAC08HD	DAC08HQ
AD1508-8D	DAC1508A8Q	AD7524UD	PM7524AQ	ADDAC100JD	DAC100BCQ7
AD208AH	PM208AJ	AD7528AQ	PM7528FR	ADDAC100KD	DAC100ABQ7
AD208H	PM208J	AD7528BQ	PM7528FR	ADDAC100LD	DAC100AAQ7
AD308AH	PM308AJ	AD7528CQ	PM7528ER	ADDAC100SD	DAC100BCQ5
AD308AN	PM308AP	AD7528JN	PM7528HP	ADG200AA	SW05BK
AD308H	PM308J	AD7528KN	PM7528HP	ADG200AP	SW05BY
AD562AD	PM562FV	AD7528LN	PM7528GP	ADG200BA	SW05FK
AD562KD	PM562HV	AD7528SD	PM7528BR	ADG200BP	SW05FY
AD562SD	PM562AV	AD7528TD	PM7528BR	ADG200CJ	SW05GP
AD7226KN	PM7226GP	AD7528UD	PM7528AR	ADG201AP	SW201BQ
AD7226TD	PM7226AR	AD7533AD	PM7533FQ	ADG201BP	SW201FQ
AD7506JD	MUX16ET	AD7533BD	PM7533FQ	ADG201CJ	SW201GP
AD7506JN	MUX16ET	AD7533CD	PM7533EQ	ADOP07AH	OP07AJ
AD7506KD	MUX16ET	AD7533JN	PM7533HP	ADOP07CH	OP07CJ
AD7506KN	MUX16ET	AD7533KN	PM7533HP	ADOP07CN	OP07CP
AD7506SD	MUX16BT	AD7533LN	PM7533GP	ADOP07DH	OP07DJ
AD7506TD	MUX16BT	AD7533SD	PM7533BQ	ADOP07DN	OP07DP
AD7507JD	MUX28ET	AD7533TD	PM7533BQ	ADOP07EH	OP07EJ
AD7507JN	MUX28ET	AD7533UD	PM7533AQ	ADOP07EN	OP07EP
AD7507KD	MUX28ET	AD7541AD	PM7541FX	ADOP07H	OP07J
AD7507KN	MUX28ET	AD7541BD	PM7541EX	Am1408L6	DAC1408A6Q
AD7507SD	MUX28BT	AD7541JN	PM7541HP	Am1408L7	DAC1408A7Q
AD7507TD	MUX28BT	AD7541KN	PM7541GP	Am1408L8	DAC1408A8Q
AD7510DIJD	SW7510FQ	AD7541SD	PM7541BX	Am1408N6	DAC1408A6P
AD7510DIKD	SW7510FQ	AD7541TD	PM7541AX	Am1408N7	DAC1408A7P
AD7510DISD	SW7510BQ	AD7542BD	PM7542FR	Am1408N8	DAC1408A8P
AD7511DIJD	SW7511FQ	AD7542GBD	PM7542ER	Am1508L8	DAC1508A8Q
AD7511DIKD	SW7511FQ	AD7542GKN	PM7542GP	Am6012DC	DAC312FR
AD7511DISD	SW7511BQ	AD7542GTD	PM7542AR	Am6012DM	DAC312BR
AD7511DITD	SW7511BQ	AD7542KN	PM7542HP	Am6012PC	DAC312FR
AD7520JD	PM7533FQ	AD7542TD	PM7542BR	Am6070ADC	DAC86CX
AD7520JN	PM7533HP	AD7543BD	PM7543FR	Am6070DC	DAC86EX
AD7520KD	PM7533FQ	AD7543GBD	PM7543ER	Am6072DM	DAC88EX
AD7520KN	PM7533HP	AD7543GKN	PM7543GP	Am685DL	CMP07FQ
AD7520LD	PM7533EQ	AD7543GTD	PM7543AR	Am685DM	CMP07BQ
AD7520LN	PM7533GP	AD7543KN	PM7543HP	Am685HL	CMP07FK
AD7520SD	PM7533BQ	AD7543TD	PM7543BR	Am685HM	CMP07BK
AD7520TD	PM7533BQ	AD7545CQ	PM7545FR	CA108AT	PM108AJ
AD7520UD	PM7533AQ	AD7545GCQ	PM7545ER	CA108T	PM108J
AD7521JD	PM7541FX	AD7545GLN	PM7545GP	CA1458E	OP14CP
AD7521JN	PM7541HP	AD7545GUD	PM7545AR	CA1458G	OP14EP
AD7521KD	PM7541FX	AD7545LN	PM7545HP	CA1458S	OP14EP
AD7521LD	PM7541FX	AD7545TD	PM7545CR	CA1458T	OP14C
AD7521LN	PM7541HP	AD7545UD	PM7545BR	CA1558S	OP14J
AD7521SD	PM7541BX	AD7548AQ	PM7548FR	CA1558T	OP14J
AD7521TD	PM7541BX	AD7548BQ	PM7548ER	CA208AT	PM208AJ
AD7521UD	PM7541BX	AD7548JN	PM7548HP	CA208T	PM208J
AD7524AD	PM7524FQ	AD7548KN	PM7548GP	CA308AT	PM308AJ
AD7524BD	PM7524FQ	AD7548SD	PM7548BR	CA308E	PM308P
AD7524CD	PM7524EQ	AD7548TD	PM7548AR	CA308T	PM308J
AD7524JN	PM7524HP	ADDAC08AD	DAC08AQ	CA339AD	PM339AY



ALPHANUMERIC DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>
CA339AG	CMP04FP	DG202CJ	SW202GP	LF13201N	SW201GP
CA747CE	OP04CY	DG202CK	SW202FQ	LF13202D	SW202FQ
CA747CG	OP04CY	DG506AR	MUX16AT	LF13202N	SW202GP
CA747CT	OP04CK	DG506BR	MUX16ET	LF13333D	SW06FQ
CA747T	OP04K	DG506CJ	MUX16FT	LF13333N	SW06GP
DAC0800LCJ	DAC08EQ	DG507AR	MUX28AT	LF13508D	MUX08EQ
DAC0800LCN	DAC08EP	DG507BR	MUX28ET	LF13508N	MUX08EP
DAC0801LCJ	DAC08CQ	DG507CJ	MUX28FT	LF13509D	MUX24EQ
DAC0801LCN	DAC08CP	DG508AP	MUX08AQ	LF13509N	MUX24EQ
DAC0802LCJ	DAC08HQ	DG508BP	MUX08EQ	LF155AH	PM155AJ
DAC0802LCN	DAC08HP	DG508CJ	MUX08FP	LF155AJ-8	PM155AZ
DAC0806LCJ	DAC1408A6Q	DG509AP	MUX24AQ	LF155H	PM155J
DAC0806LCN	DAC1408A6P	DG509BP	MUX24EQ	LF156AH	PM156AJ
DAC0807LCJ	DAC1408A7Q	DG509CJ	MUX24FP	LF156AJ-8	PM156AZ
DAC0807LCN	DAC1408A7P	HI-200-2	SW05BY	LF156H	PM156J
DAC0808LCJ	DAC1408A8Q	HI-200-4	SW05FY	LF156J-8	PM156Z
DAC0808LCN	DAC1408A8P	HI-200-5	SW05GP	LF157AH	PM157AJ
DAC0808LD	DAC1508A8Q	HI-201-2	SW201BQ	LF157AJ-8	PM157AZ
DAC08ADM	DAC08AQ	HI-201-4	SW201FQ	LF157H	PM157J
DAC08CDC	DAC08CQ	HI-201-5	SW201GP	LF351H	OP15FJ
DAC08CN	DAC08CQ	HI1-506-2	MUX16BT	LF353H	OP215FJ
DAC08DM	DAC08Q	HI1-506-5	MUX16FT	LF355AH	PM355AJ
DAC08EDC	DAC08EQ	HI1-506A-2	MUX16BT	LF355AJ-8	PM355AZ
DAC08EF	DAC08EQ	HI1-506A-5	MUX16ET	LF355BJ	PM355Z
DAC08EN	DAC08EP	HI1-507-2	MUX28BT	LF356AH	PM356AJ
DAC08F	DAC08Q	HI1-507-5	MUX28ET	LF356AJ-8	PM356AZ
DAC08HC	DAC08HP	HI1-507A-2	MUX28AT	LF357AH	PM357AJ
DAC08HD	DAC08HQ	HI1-507A-5	MUX28ET	LF357AJ-8	PM357AZ
DAC08HF	DAC08HQ	HI1-562A-2	PM562AV	LF411ACH	OP15EJ
DAC08HN	DAC08HP	HI1-562A-5	PM562AV	LF411ACN	OP15EZ
DAC10BDM	DAC10BX	HI1-562A-8	PM562HV/883	LF411AMH	OP15AJ
DAC10CDM	DAC10CX	HI1-7541AD-4	PM7541FX	LM108AD	PM108AZ
DAC10FCC	DAC10FX	HI1-7541BD-4	PM7541EX	LM108AH	PM108AJ
DAC10GDC	DAC10GX	HI1-7541JD-5	PM7541HP	LM108AJ-8	PM108AZ
DAC6012ADC	DAC312FR	HI1-7541KD-5	PM7541GP	LM108D	PM108Z
DAC6012ADM	DAC312BR	HI1-7541SD-2	PM7541BX	LM108H	PM108J
DAC6012DC	DAC312FR	HI1-7541TD-2	PM7541AX	LM108J-8	PM108Z
DAC6012DM	DAC312BR	HI2-200-2	SW05BK	LM139AD	PM139AY
DG200AA	SW05BK	HI2-200-4	SW05FK	LM139AF	PM139AY
DG200AAA	SW05BK	HI3-506-5	MUX16FT	LM139AJ	PM139AY
DG200AAK	SW05BY	HI3-506A-5	MUX16ET	LM139D	PM139Y
DG200ABA	SW05FK	HI3-507-5	MUX28FT	LM139F	PM139Y
DG200ABK	SW05FY	HI3-507A-5	MUX28ET	LM139J	PM139Y
DG200ACJ	SW05GP	HI3-508A-5	MUX08EP	LM1458AH	OP14EJ
DG200AP	SW05BY	HI3-509A-5	MUX24EP	LM1458AJ-8	OP14EZ
DG200BA	SW05FK	HI4-508A-2	MUX08BQ	LM1458AN	OP14EP
DG200BP	SW05BY	HI4-508A-5	MUX08EQ	LM1458H	OP14CJ
DG200CJ	SW05GP	HI4-509A-2	MUX24BQ	LM1458J	OP14CZ
DG201AAK	SW201BQ	HI4-509A-5	MUX24FQ	LM1458N	OP14DP
DG201ABK	SW201FQ	LF11201D	SW201BQ	LM1558AH	OP14AJ
DG201AP	SW201BQ	LF11202D	SW202BQ	LM1558AJ	OP14AZ
DG201BP	SW201FQ	LF11333D	SW06BQ	LM194H	MAT02AH
DG201CJ	SW201GP	LF11508D	MUX08AQ	LM208AD	PM208AZ
DG202AK	SW202BQ	LF11509D	MUX24AQ	LM208AH	PM208AJ
DG202BK	SW202FQ	LF13201D	SW201FQ	LM208AN	PM208AZ

4

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Precision Monolithics Inc.

<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>
LM208D	PM208Z	MC1504U10	REF01AZ	MP7506KD	MUX16ET
LM208H	PM208J	MC1504U5	REF02AZ	MP7506TD	MUX16BT
LM208N	PM208Z	MC15088F	DAC15088Q	MP7507JD	MUX28ET
LM239AD	CMP04FY	MC1508L8	DAC1508A8Q	MP7507JN	MUX28FT
LM239D	CMP04FY	MC1558G	OP14J	MP7507KD	MUX28ET
LM239F	CMP04FY	MC1558NG	OP14AJ	MP7507KN	MUX28FT
LM239N	CMP04FP	MC1558NU	OP14AZ	MP7507SD	MUX28BT
LM258P	OP221GZ	MC1558U	OP14Z	MP7507TD	MUX28BT
LM2901F	CMP04FY	MC1741CG	OP02CJ	MP7508DIJD	MUX08EQ
LM2901J	CMP04BY	MC1741CP1	OP02CP	MP7508DIJN	MUX08EP
LM2901N	CMP04FP	MC1741CU	OP02HJ	MP7508DIKD	MUX08EQ
LM308AD	PM308AZ	MC1741G	OP02J	MP7508DISD	MUX08AQ
LM308AH	PM308AJ	MC1741NCG	OP02Z	MP7524AD	PM7524FQ
LM308AJ-8	PM308AZ	MC1741NCP1	OP02HZ	MP7524BD	PM7524FQ
LM308AN	PM308AP	MC1741NG	OP02J	MP7524CD	PM7524EQ
LM308D	PM308Z	MC1741NU	OP02Z	MP7524JN	PM7524HP
LM308H	PM308J	MC1741SCG	OP01HJ	MP7524KN	PM7524HP
LM308J-8	PM308Z	MC1741SCPI	OP01CP	MP7524LN	PM7524GP
LM3302N	CMP04FP	MC1741SG	OP01J	MP7524SD	PM7524BQ
LM339AD	PM339AY	MC1741U	OP02Z	MP7524TD	PM7524BQ
LM339AF	PM339AY	MC1747CL	OP04EY	MP7524UD	PM7524AQ
LM339AJ	PM339AY	MC1747CP2	OP04EY	MP7528BD	PM7528FR
LM339AN	CMP04FP	MC1747G	OP04BK	MP7528CD	PM7528ER
LM339D	PM339AY	MC1747L	OP04BY	MP7528KN	PM7528HP
LM339N	CMP04FP	MC3302N	CMP04FP	MP7528LN	PM7528GP
LM358JG	OP221HZ	MC35001AG	OP16AJ	MP7528TD	PM7528BR
LM394H	MAT02EH	MC35001AU	OP16AZ	MP7528UD	PM7528AR
LM725AH	OP06AJ	MC35001BG	OP16GJ	MP7533BD	PM7533FQ
LM725CH	OP06EJ	MC35001BU	OP16BZ	MP7533CD	PM7533EQ
LM725CN	OP06GZ	MC4741CL	OP11GY	MP7533KN	PM7533HP
LM725H	OP06BJ	MC4741CP	OP11GP	MP7533LN	PM7533GP
LM747AH	OP04K	MC4741L	OP11CY	MP7533TD	PM7533BQ
LM747AJ	OP04AY	MC7506KN	MUX16FT	MP7533UD	PM7533AQ
LM747CH	OP04CK	MC7506SD	MUX16BT	MP7541TD	PM7541AX
LM747CJ	OP04CY	MP200DIAA	SW05BK	MP7621AD	PM7541FX
LM747CN	OP04DY	MP200DIAP	SW05BY	MP7621BD	PM7541EX
LM747EJ	OP04EY	MP200DIBA	SW05FK	MP7621JN	PM7541HP
LM747EN	OP04CY	MP200DIBP	SW05BY	MP7621KN	PM7541GP
LM747H	OP04BK	MP201DIAP	SW201BQ	MP7621SD	PM7541BX
LM747J	OP04Y	MP201DIBP	SW201FQ	MP7621TD	PM7541AX
MC14087F	DAC14087Q	MP201DICJ	SW201GP	MP7623AD	PM7541FX
MC14088F	DAC14088Q	MP4136CY	OP09FY	MP7623BD	PM7541EX
MC1408F	DAC1408A7Q	MP4136Y	OP09BY	MP7623JN	PM7541HP
MC1408L6	DAC1408A6Q	MP5520AD	DAC01Y	MP7623KN	PM7541GP
MC1408L7	DAC1408A7Q	MP5520AZ	DAC01AY	MP7623SD	PM7541BX
MC1408L8	DAC1408A8Q	MP5520BD	DAC01BY	MP7623TD	PM7541AX
MC1458CG	OP14CJ	MP5520CD	DAC01CY	MP7645CD	PM7645ER
MC1458CP1	OP14CP	MP5520DD	DAC01DY	MP7645LN	PM7645GP
MC1458CU	OP14CZ	MP5520FD	DAC01FY	MP7645UD	PM7645AR
MC1458G	OP14CJ	MP5520HD	DAC01HY	MPC4D	MUX24FQ
MC1458N	OP14CP	MP562AD/BIN	PM562FV	MPC8S	MUX08FQ
MC1458NP1	OP14EP	MP562KD/BIN	PM562HV	MPOP01AJ	OP01AJ
MC1458NU	OP14EZ	MP562SD/BIN	PM562AV	MPOP01AZ	OP01AZ
MC1458P	OP14CP	MP7506JD	MUX16ET	MPOP01CJ	OP01CJ
MC1458P1	OP14DP	MP7506JN	MUX16FT	MPOP01CP	OP01CP



ALPHANUMERIC DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>
MPOP01CZ	OP01CZ	MPOP12FJ	OP12FJ	MPREF02HP	REF02HP
MPOP01GJ	OP01GJ	MPOP12FZ	OP12FZ	MPREF02HZ	REF02HZ
MPOP01GZ	OP01GZ	MPOP12GJ	OP12GJ	MPREF02J	REF02J
MPOP01HJ	OP01HJ	MPOP12GZ	OP12GZ	MPREF02Z	REF02Z
MPOP01HP	OP01HP	MPOP27AJ	OP27AJ	NE5007E	DAC08CQ
MPOP01HZ	OP01HZ	MPOP27AZ	OP27AZ	NE5008F	DAC08EQ
MPOP02AJ	OP02AJ	MPOP27BJ	OP27BJ	NE5009F	DAC08HQ
MPOP02AZ	OP02AZ	MPOP27BZ	OP27BZ	NE532H	OP221CJ
MPOP02BJ	OP02BJ	MPOP27CJ	OP27CJ	NE532N	OP221GZ
MPOP02BZ	OP02BZ	MPOP27CZ	OP27CZ	OP07AH	OP07AJ
MPOP02CJ	OP02CJ	MPOP27EJ	OP27EJ	OP07AH/883	OP07AJ/883
MPOP02CP	OP02CP	MPOP27EP	OP27EP	OP07AJ8	OP07AZ
MPOP02CZ	OP02CZ	MPOP27EZ	OP27EZ	OP07AJ8/883	OP07AZ/883
MPOP02DJ	OP02DJ	MPOP27FP	OP27FP	OP07AT	OP07AJ
MPOP02DP	OP02DP	MPOP27FZ	OP27FZ	OP07CH	OP07CJ
MPOP02DZ	OP02DZ	MPOP27GJ	OP27GJ	OP07CJ8	OP07CZ
MPOP02EJ	OP02EJ	MPOP27GP	OP27GP	OP07CJG	OP07CZ
MPOP02EP	OP02EP	MPOP27GZ	OP27GZ	OP07CN8	OP07CP
MPOP02EZ	OP02EZ	MPOP37AJ	OP37AJ	OP07CNB	OP07CP
MPOP02J	OP02J	MPOP37AZ	OP37AZ	OP07CT	OP07CJ
MPOP05AJ	OP05AJ	MPOP37BJ	OP37BJ	OP07DE	OP07Z
MPOP05AZ	OP05AZ	MPOP37BZ	OP37BZ	OP07DH	OP07DJ
MPOP05BJ	OP05BJ	MPOP37CJ	OP37CJ	OP07DN8	OP07DP
MPOP05CJ	OP05CJ	MPOP37CZ	OP37CZ	OP07DNB	OP07DP
MPOP05CZ	OP05CZ	MPOP37EJ	OP37EJ	OP07DT	OP07DJ
MPOP05DJ	OP05DJ	MPOP37EP	OP37EP	OP07EDE	OP07EZ
MPOP05EJ	OP05EJ	MPOP37EZ	OP37EZ	OP07EH	OP07EJ
MPOP05EZ	OP05EZ	MPOP37FJ	OP37FJ	OP07EJ8	OP07EZ
MPOP05J	OP05J	MPOP37FP	OP37FP	OP07EJG	OP07EZ
MPOP05Z	OP05Z	MPOP37GJ	OP37GJ	OP07EN8	OP07EP
MPOP07AJ	OP07AJ	MPOP37GP	OP37GP	OP07ET	OP07EJ
MPOP07AZ	OP07AZ	MPOP37GZ	OP37GZ	OP07H	OP07J
MPOP07CJ	OP07CJ	MPREF01AJ	REF01AJ	OP07H/883	OP07J/883
MPOP07CP	OP07CP	MPREF01AZ	REF01AZ	OP07J8	OP07Z
MPOP07CZ	OP07CZ	MPREF01CJ	REF01CJ	OP07J8/883	OP07Z/883
MPOP07DJ	OP07DJ	MPREF01CP	REF01CP	OP07T	OP07J
MPOP07DP	OP07DP	MPREF01CZ	REF01CZ	OP12AJG	OP12AZ
MPOP07DZ	OP07DZ	MPREF01EJ	REF01EJ	OP12BJG	OP12BZ
MPOP07EJ	OP07EJ	MPREF01EZ	REF01EZ	OP12CJG	OP12CZ
MPOP07EP	OP07EP	MPREF01HJ	REF01HJ	OP12EJG	OP12EZ
MPOP07EZ	OP07EZ	MPREF01HP	REF01HP	OP12FJG	OP12FZ
MPOP07J	OP07J	MPREF01HZ	REF01HZ	OP12GJG	OP12GZ
MPOP10CY	OP10CY	MPREF01J	REF01J	OP15AH	OP15AJ
MPOP10EY	OP10EY	MPREF01Z	REF01Z	OP15BH	OP15BJ
MPOP11AY	OP11AY	MPREF02AJ	REF02AJ	OP15CH	OP15CJ
MPOP11BY	OP11BY	MPREF02AZ	REF02AZ	OP15EH	OP15EJ
MPOP11EY	OP11EY	MPREF02CJ	REF02CJ	OP15FH	OP15FJ
MPOP12AJ	OP12AJ	MPREF02CP	REF02CP	OP15GH	OP15GJ
MPOP12AZ	OP12AZ	MPREF02CZ	REF02CZ	OP16AH	OP16AJ
MPOP12BJ	OP12BJ	MPREF02DJ	REF02DJ	OP16BH	OP16BJ
MPOP12BZ	OP12BZ	MPREF02DP	REF02DP	OP16CH	OP16CJ
MPOP12CJ	OP12CJ	MPREF02DZ	REF02DZ	OP16EH	OP16EJ
MPOP12CZ	OP12CZ	MPREF02EJ	REF02EJ	OP16FH	OP16FJ
MPOP12EJ	OP12EJ	MPREF02EZ	REF02EZ	OP16GH	OP16GJ
MPOP12EZ	OP12EZ	MPREF02HJ	REF02HJ	OP227AJ	OP227AY

4

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ALPHANUMERIC DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>	<u>Device</u>	<u>PMI Replacement</u>
OP227CJ	OP227CY	REF-01CDE	REF01CZ	TSC9496CJ	REF01HP
OP227EJ	OP227EY	REF-01CT	REF01CJ	TSC9496EE	REF01EJ
OP227FJ	OP227FY	REF-01DDE	REF01HZ	XRC277	RPT82FQ
OP227GJ	OP227GY	REF-01DE	REF01Z	μ A0801CDC	DAC08EQ
OP27AT	OP27AJ	REF-01EDE	REF01EZ	μ A0801CPC	DAC08CP
OP27BDE	OP27BZ	REF-01ET	REF01EJ	μ A0801DM	DAC08Q
OP27BT	OP27BJ	REF-01HT	REF01HJ	μ A0801EDC	DAC08EQ
OP27BT/883	OP27BJ/883	REF-01T	REF01J	μ A0802ADC	DAC1408A8Q
OP27CDE	OP27CZ	REF-02ADE	REF02AZ	μ A0802APC	DAC1408A8P
OP27CH	OP27CJ	REF-02AT	REF02AJ	μ A0802BDC	DAC1408A7Q
OP27CH/883	OP27CJ/883	REF-02CDE	REF02CZ	μ A0802BPC	DAC1408A7P
OP27CJ8	OP27CZ	REF-02CT	REF02CJ	μ A0802CDC	DAC1408A6Q
OP27CJ8/883	OP27CZ/883	REF-02DDE	REF02HZ	μ A0802CPC	DAC1408A6P
OP27CT	OP27CJ	REF-02DE	REF02Z	μ A0802DM	DAC1508A8Q
OP27EDE	OP27EZ	REF-02EDE	REF02EZ	μ A0802DMQB	DAC1508A8Q/883
OP27EH	OP27EJ	REF-02ET	REF02EJ	μ A0802EPC	DAC08EP
OP27EJ8	OP27EZ	REF-02HT	REF02HJ	μ A108AH	PM108AJ
OP27EN8	OP27EP	REF-02T	REF02J	μ A108H	PM108J
OP27ET	OP27EJ	REF01AH	REF01AJ	μ A139ADM	PM139AY
OP27FT	OP27FJ	REF01CH	REF01CJ	μ A139DM	PM139Y
OP27GDE	OP27GZ	REF01CN8	REF01CP	μ A208AH	PM208AJ
OP27GH	OP27GJ	REF01EH	REF01EJ	μ A208H	PM208J
OP27GJ8	OP27GZ	REF01H	REF01J	μ A308AH	PM308AJ
OP27GN8	OP27GP	REF01HH	REF01HJ	μ A308H	PM308J
OP27GT	OP27GJ	REF01HN8	REF01HP	μ A3303PC	OP11FP
OP37ADE	OP37AZ	REF02AH	REF02AJ	μ A339ADC	PM339AY
OP37AH	OP37AJ	REF02CH	REF02CJ	μ A714EHC	OP07EJ
OP37AH/883	OP37AJ/883	REF02CN8	REF02CP	μ A714HC	OP07CJ
OP37AJ8	OP37AZ	REF02DH	REF02DJ	μ A714HM	OP07AJ
OP37AJ8/883	OP37AZ/883	REF02DN8	REF02DP	μ A714LHC	OP07DJ
OP37AT	OP37AJ	REF02EH	REF02EJ	μ A725HC	PM725CJ
OP37BDE	OP37BZ	REF02H	REF02J	μ A725HM	PM725J
OP37BT	OP37BJ	REF02HH	REF02HJ	μ A725TC	PM725CP
OP37BT/883	OP37BJ/883	REF02HN8	REF02HP	μ A741CJG	PM741CZ
OP37CDE	OP37CZ	RM725T	PM725J	μ PC1251C	OP220GZ
OP37CH	OP37CJ	RM741T	PM741J	μ PC1251D	OP220FZ
OP37CH/883	OP37CJ/883	RM747DC	OP04Y	μ PC151C	OP02BZ
OP37CJ8	OP37CZ	SA1458N	OP14BZ	μ PC151D	OP02CZ
OP37CJ8/883	OP37CZ/883	SA741	OP02BZ	μ PC154D	OP05CZ
OP37CT	OP37CJ	SE532H	OP221BJ	μ PC156D	PM208Z
OP37EDE	OP37EZ	SE5534AFE	OP27BZ	μ PC251C	OP14EP
OP37EH	OP37EJ	SE5534FE	OP27CZ	μ PC251D	OP14EZ
OP37EJ8	OP37EZ	SSS1408A-6Q	DAC1408A6Q	μ PC339C	CMP04FP
OP37EN8	OP37EJ	SSS1408A-7Q	DAC1408A7Q	μ PC358C	OP221HZ
OP37ET	OP37EJ	SSS1408A-8Q	DAC1408A8Q	μ PC4581C	OP15GZ
OP37GDE	OP37GZ	SSS1508A-8Q	DAC1508A8Q	μ PC603D	DAC01CY
OP37GH	OP37GJ	TSC7541BD	PM7541EX	μ PC610D	DAC02CCX1
OP37GJ8	OP37GZ	TSC7541JN	PM7541HP	μ PC624C	DAC08EP
OP37GN8	OP37GP	TSC7541KN	PM7541GP	μ PC624D	DAC08EQ
OP37GT	OP37GJ	TSC7541SD	PM7541BX	μ PC648D	DAC312FR
RC1458NB	OP14CP	TSC7541TD	PM7541AX	μ PC801C	OP15FZ
RC3302DB	CMP04FP	TSC9495CE	REF02HJ		
RC725T	PM725CJ	TSC9495CJ	REF02HP		
REF-01ADE	REF01AZ	TSC9495EE	REF02EJ		
REF-01AT	REF01AJ	TSC9496CE	REF01HJ		

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

5-4	Introduction	5-91	OP-15/OP-16/OP-17
5-4	Definitions		Precision JFET-Input Operational Amplifiers
5-6	Selection Guide	5-105	OP-20
5-12	OP-01		Micropower Operational Amplifier
	Inverting High-Speed Operational Amplifier	5-111	OP-21
5-18	OP-02		Low-Power Operational Amplifier
	General-Purpose Operational Amplifier	5-117	OP-22
5-26	OP-04/OP-14		Programmable Micropower Operational Amplifier
	Dual Matched High-Performance Operational Amplifiers	5-128	OP-27
5-34	OP-05		Low-Noise Precision Operational Amplifier
	Instrumentation Operational Amplifier	5-140	OP-32
5-43	OP-06		High-Speed Programmable Micropower Operational Amplifier
	High-Gain Instrumentation Operational Amplifier	5-152	OP-37
5-51	OP-07		Low-Noise Precision High-Speed Operational Amplifier
	Ultra-Low Offset Voltage Operational Amplifier	5-164	OP-41
5-61	OP-08		Low-Bias-Current JFET Operational Amplifier
	Precision Low-Input-Current Operational Amplifier	5-175	OP-43
5-68	OP-09/OP-11		Low-Bias-Current, Fast JFET Operational Amplifier
	Quad Matched 741-Type Operational Amplifiers	5-180	OP-50
5-75	OP-10		High-Output-Current Operational Amplifier
	Dual Matched Instrumentation Operational Amplifier	5-191	OP-77
5-87	OP-12		Next Generation OP-07 (Ultra-Low Offset Voltage Operational Amplifier)
	Precision Low-Input-Current Operational Amplifier	5-197	OP-90
			Low-Voltage Micropower Operational Amplifier



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

5-199 **OP-207**
Dual Ultra-Low V_{OS} Matched
Operational Amplifier

5-205 **OP-215**
Dual Precision JFET-Input
Operational Amplifier

5-212 **OP-220**
Dual Micropower Operational Amplifier

5-220 **OP-221**
Dual Low-Power Operational Amplifier

5-228 **OP-227**
Dual Low-Noise Low-Offset
Instrumentation Operational Amplifier

5-239 **OP-400**
Quad Low-Offset Low-Power
Operational Amplifier

5-241 **OP-420**
Quad Micropower Operational Amplifier

5-246 **OP-421**
Quad Low-Power Operational Amplifier

**PM-108A/PM-208A/PM-308A/
PM-108/PM-208/PM-308/
PM-2108A/PM-2108**
Low-Input-Current
Operational Amplifiers

5-256 **PM-146/PM-246**
Programmable Quad
Operational Amplifiers

**PM-155A/PM-355A/PM-155/
PM-156A/PM-356A/PM-156/
PM-157A/PM-357A/PM-157**
Monolithic JFET-Input
Operational Amplifiers

5-265 **PM-725**
Instrumentation Operational Amplifier

5-268 **PM-741**
Compensated Operational Amplifier

5-270 **PM-747**
Dual Compensated
Operational Amplifier

5-273 **JM38510/10104**
JAN Single Low-Input-Current
Operational Amplifier

5-276 **JM38510/10106**
JAN Dual Low-Input-Current
Operational Amplifier

5-279 **JM38510/11004**
JAN Quad 741-Type
Operational Amplifier

**JM38510/11401/11402/11403/11404/
11405/11406**
JAN JFET-Input Operational Amplifiers

5-292 **JM38510/13501/13502**
Ultra-Low Offset Voltage
Operational Amplifiers

5-295 **JM38510/13503**
Low-Noise Precision
Operational Amplifier

5
OPERATIONAL AMPLIFIERS



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

INTRODUCTION

Precision Monolithics pioneered in the development of low-offset, high-gain operational amplifiers for use in precision applications. A proprietary linear bipolar process with nitride passivation was developed to achieve low noise, enhanced long-term reliability, and improved resistance to radiation effects. PMI operational amplifier processing capability includes JFET and super-beta devices as well as standard NPN and PNP devices. A zener-zap trimming technique was designed to reduce input offset voltage at the wafer testing stage. Offset trimming is performed in discrete steps by applying high-current pulses through automatically-selected zener diodes. High-current pulsing shorts the zener which is parallel-connected to a trim resistor. Zener-zap trimming provides a very reliable and stable reduction of input offset voltage. PMI has developed many innovative operational-amplifier circuit designs based on their low-noise, low-drift processing in combination with zener-zap offset trimming.

The table below summarizes the PMI families of operational amplifiers. All feature low input offset voltage, low drift, and high open-loop gain.

Operational Amplifiers

General Purpose, Bipolar Input	
OP-02	Single
OP-04, OP-14	Dual
OP-09, OP-11	Quad
OP-01	High Speed, Inverting
General Purpose, JFET Input	
PM-155, PM-156,	
PM-157	Standard JFET Input
38510 Versions	MIL-Grade, 38510
Precision, High-Speed Improved JFET Input	
OP-15, OP-16, OP-17,	
OP-43, OP-215 (Dual)	

High Accuracy	
OP-05, OP-06,	
OP-07, OP-77	Low V_{OS} , High Gain
OP-27, OP-37, OP-50	Low V_{OS} , Low Noise
OP-227, OP-207, OP-10	Dual
OP-08, OP-12	Low I_B , Low Power
OP-50	High Output Current
Low Power, Low Input-Bias-Current	
OP-21	Single
OP-221	Dual
OP-41	JFET Input
PM-108/208/308,	
PM-2108 (Dual)	Low I_B , LM-108 Type
Micropower	
OP-20	Singles, Low I_{SY}
OP-22/32	Programmable
OP-220	Dual
OP-420, OP-421	Quad

DEFINITIONS

Average Bias Current Drift (TCI_B) — The ratio of change in input bias current to a change in temperature.

Average Offset Current Drift (TCI_{OS}) — The ratio of change in input offset current to a change in temperature.

Average Offset Voltage Drift (TCV_{OS}) — The ratio of change in input offset voltage to a change in temperature.

Average Offset Voltage Drift With External Trimming (TCV_{OSN}) — The ratio of the change in input offset voltage to a change in temperature with the input offset voltage trimmed to zero at room temperature.

Common-Mode Input Resistance (R_{inCM}) — The ratio of input voltage range to the change in input bias current over this range.

Common-Mode Rejection Ratio (CMRR) — The ratio of the common-mode voltage range (CMVR) to the peak-to-peak change in equivalent input offset voltage (CME) over this range. CMRR is specified for a specific CMVR. $CMRR = 20 \log_{10} (CMVR/CME)$



OPERATIONAL AMPLIFIERS

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5

OPERATIONAL AMPLIFIERS

Gain-Bandwidth Product (GBW) — The frequency at which the open-loop gain equals unity.

Input Bias Current (I_B) — The average of the currents into the two input terminals when the output is at zero volts with no load. I_B is measured at $V_{CM} = 0$.

Input Noise Current (I_{np-p}) — The peak-to-peak noise current within a specified frequency band.

Input Noise Current Density (I_n) — The rms noise current in a 1Hz band centered on a specified frequency.

Input Noise Voltage (e_{np-p}) — The peak-to-peak noise voltage within a specified frequency band.

Input Noise Voltage Density (e_n) — The rms noise voltage in a 1Hz band centered on a specified frequency.

Input Offset Current (I_{OS}) — The difference between the currents into the two input terminals when the output is at zero volts with no load.

Input Offset Voltage (V_{OS}) — The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

Input Resistance-Differential Mode (R_{IN}) — The ratio of small-signal change in input voltage to a change in input current at either input terminal with the other grounded.

Input Voltage Range (IVR) — The range of input voltage for which the device will operate as a linear amplifier.

Large-Signal Voltage Gain (A_{VO}) — The ratio of change in output voltage (over a specified range) to a change in input voltage.

Open-Loop Output Resistance (R_O) — The small-signal driving-point resistance of the output terminal with respect to ground at a specified quiescent DC output voltage and current.

Output Voltage Swing (V_O) — The peak output voltage that can be obtained without clipping into a specified load resistance.

Power Dissipation (P_d) — The total power dissipated in the amplifier with the output at zero volts with no load.

Power Supply Rejection Ratio (PSRR) — The inverse ratio of change in input offset voltage to a change in power supply voltage. PSRR can be specified in dB or $\mu V/V$.

Slew Rate (SR) — The ratio of a change in output voltage to the minimum time required to effect this change under large-signal drive conditions. Slew rate may be specified separately for positive and negative-going changes.

Supply Current (I_{SY}) — The current required from the power supply to operate the amplifier with no load and the output at zero volts.

Unity-Gain Closed-Loop Bandwidth (BW) — The frequency at which the magnitude of the small-signal voltage gain of the amplifier, operated closed-loop as a unity-gain follower, is 3dB below unity.

MATCHING PARAMETER DEFINITIONS

Input Offset Voltage Match (ΔV_{OS}) — The difference between the offset voltages of side A and side B ($V_{OSA} - V_{OSB}$). If $V_{OSA} = V_{OSB}$, the net differential offset voltage at the output of the amplifier pair equals zero.

Input Offset Voltage Tracking ($TC\Delta V_{OS}$) — The ratio of change in ΔV_{OS} to a change in temperature.

Average Noninverting Bias Current (I_{B+}) — The average of the side A and side B noninverting input bias currents:

$$\frac{I_{BA+} + I_{BB+}}{2}$$

Noninverting Input Offset Current (I_{OS+}) — The difference between the noninverting input bias currents of side A and side B; ($I_{BA+} - I_{BB+}$).

Inverting Input Offset Current (I_{OS-}) — The difference between the inverting input bias currents of side A and side B; ($I_{BA-} - I_{BB-}$).

Average Drift Of Noninverting Bias Current (TCI_{B+}) — The ratio of change in noninverting bias current to a change in temperature.

Average Drift of Noninverting Offset Current ($TC_{I_{OS}^+}$) — The ratio of change in noninverting offset current to a change in temperature.

Common-Mode Rejection-Ratio Match ($\Delta CMRR$) — The difference between the common-mode rejection ratios (expressed in volt/volt of side A and side B. $\Delta CMRR$ in dB = $20 \log_{10} (\Delta CMRR$ in volt/volt).

Power Supply Rejection-Ratio Match ($\Delta PSRR$) — The difference between the power supply rejection ratios (expressed in volt/volt) of side A and side B. $\Delta PSRR$ in dB = $20 \log_{10} (\Delta PSRR$ in volt/volt).

Channel Separation — The ratio of change in offset voltage of one channel to a change in output voltage in the second channel.

SELECTION PRINCIPLES

Selecting an operational amplifier can be a frustrating experience. The choice of circuit configuration, and of associated component values, interrelates to the choice of op amp for a given application. Op amps are specified as open-loop devices, but in a circuit application they generally have feedback applied. The designer must predict the closed-loop circuit performance as determined by his choice of op amp and choice of circuit configuration (and component tolerances). Detailed literature is available on circuit configurations to accomplish particular analog circuit functions using op amps. This Selection Guide gives recommended guidelines and a design strategy for selecting op amps to best meet your needs.

The first design steps are to:

1. Completely define the design objectives.

Input Signal — Determine the signal level, frequency content, and impedance of the input.

Accuracy Required — For linear amplification, this consists of limits for offset, gain error, and nonlinearity. Establish your bandwidth and slew

rate needs. Distortion is often critical for audio use and fast settling may be essential in a data-conversion application.

Output Load — Op amps are sometimes called upon to drive long cables, storage capacitors, transformers, or other semiconductors. High-speed circuits generally require low-impedance feedback elements and the load is usually low impedance; therefore, relatively high output current drive is needed for high-speed circuits.

Environmental Conditions — Temperature range and power supply characteristics are very important factors. Power supply drain is often critical in battery-powered equipment, process control systems, and satellites. In addition, op-amp package type is generally dictated by environmental and cost factors. Another factor to consider is the *electrical environment*. Minimize accuracy degradation from unavoidable ground noise and power supply fluctuations by choosing an op amp with high CMRR and PSRR.

2. Use the published op-amp specifications and characterization graphs.

PMI provides comprehensive specification tables with well-defined test conditions for operation at 25° C and over specific temperature ranges. The "Typical Performance Curves" show the characteristic response of an op amp to variations in frequency, temperature, supply voltage, or load impedance. Since op amps often perform much better than indicated by their min/max specification limits, the designer may be tempted to ask for special selection to tighter limits. Although sometimes necessary, special selection tends to be costly. A better strategy is to select a standard op amp that meets the application need on a worst-case basis. Careful initial selection of a high-performance standard op amp will provide predictable circuit performance on a continuing basis.



OPERATIONAL AMPLIFIERS

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Selection Process

Operational amplifiers can be divided into four basic functional categories:

Category	Primary Characteristics
General Purpose	"741" types.
High Accuracy	Low input offsets ($V_{OS} < 1\text{mV}$), high DC gain, high CMRR, and low noise. Leading part types are OP-05, OP-07, OP-27, OP-50, and OP-77.
High Speed	Optimized for high slew rate, high gain-bandwidth, and fast settling time.
Low Power, Wide Supply Range	Low supply drain ($I_{SY} < 1\text{mA}$), wide input and output voltage range. Includes micropower ($I_{SY} < 100\mu\text{A}$) units for battery operation.

There can be overlap between some categories, while others are mutually exclusive. For example, the PMI OP-22 covers both "High Accuracy" and "Low Power". However, "High Speed" and "Low Power" tend to be mutually exclusive; it is difficult to simultaneously optimize both speed and power.

Economics is another important dimension of the selection process. The "General Purpose" category is generally lowest in cost, but a "High Accuracy" op amp with low input-offset-voltage may be more cost effective if it eliminates the need for external trimming components. The PMI high-accuracy OP-07 is often used in place of general-purpose 741-types because of its low input-offset-voltage and high gain.

AC Considerations

Consideration of AC requirements for an application is a good starting point in the op amp selection process. If high frequency ($\text{GBW} > 10\text{MHz}$, $\text{SR} > 10\text{V}/\mu\text{s}$) is the primary concern, then the choice quickly narrows down to the "High Speed" category.

Two factors will generally dictate the op amp choice:

1. The loop gain (excess of open-loop gain over closed-loop gain) must be sufficient at the highest frequency of interest. For example, if 1.0% accuracy at 10kHz is required when operating at closed-loop gain of 10, then the op amp must have an open-loop gain of at least 1000 at 10kHz ($10/1000 = 1\%$). When operating at high closed-loop gains, decompensated op amps generally offer the advantage of better gain bandwidth product without a price/performance penalty.

2. Slew rate must be high enough to follow the fastest signal input without causing distortion or other anomalies. Slew-rate symmetry, linearity, and overload recovery should be considered. The detrimental effects of slew-rate limiting can be subtle; it is best to avoid trouble by choosing an op amp with at least a 20% safety margin in minimum slew-rate.

High speed implies a need for high output current. Applications such as audio amplifiers, active filters, DAC-output amplifiers, and fast integrators often require high output currents for driving feedback capacitors or low-impedance networks. Driving such capacitive loads as long cables or storage capacitors at high frequency requires high output currents.

DC Considerations

If the frequency requirements are relatively modest ($\text{SR} < 10\text{V}/\mu\text{s}$) and the circuit requires closed-loop gain above unity, choose a "High Accuracy" op amp. These op amps feature:

Low Input Offsets	
Low Input Offset Voltage	$V_{OS} \leq 1\text{mV}$, $\text{TCV}_{OS} \leq 2\mu\text{V}/^\circ\text{C}$
Low Input Bias Current	
— Bipolar Input Stage	$I_B \leq 100\text{nA}$ ($I_B \leq 10\text{nA}$ is desirable)
— JFET Input Stage	$I_B \leq 200\text{pA}$



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OPERATIONAL AMPLIFIERS

High Open-Loop DC Gain	$A_{VOL} \geq 1,000,000$
High Common-Mode Rejection	$CMR \geq 100\text{dB}$
Low Input Noise at 100Hz	$e_n \leq 15\text{nV}/\sqrt{\text{Hz}}$

A leading op amp in the High-Accuracy category is the PMI OP-77 with these key specifications:

$$\begin{aligned}V_{OS} &\leq 25\mu\text{V} \\ I_B &\leq \pm 2\text{nA}, I_{OS} \leq 2\text{nA} \\ A_{VOL} &\geq 5,000,000 \\ CMRR &\geq 114\text{dB} \\ e_n &\leq 11\text{nV}/\sqrt{\text{Hz}} \text{ at } 1000\text{Hz}\end{aligned}$$

The OP-77 performs very well even at high closed-loop gains. For example, consider a noninverting configuration with a closed-loop gain of 100. Assume a signal source with a range of $\pm 0.1\text{V}$ and source impedance of $10\text{k}\Omega$. If the feedback resistances are chosen to be relatively low, then the maximum offset caused by input bias current will be 4.4nA ($I_B + I_{OS}/2 = 4.4\text{nA}$) multiplied by the $10\text{k}\Omega$ source resistance, or $44\mu\text{V}$. Total input offset, even without external offset nulling, will be less than $119\mu\text{V}$ (approximately 0.12% of full-scale). The effect of CMRR is negligible in this example; the $\pm 0.1\text{V}$ input divided by 110dB of common-mode rejection is only $0.3\mu\text{V}$ referred-to-input. Gain error factor is $1/(1 + A_{VCL}/A_{VOL})$, which is a gain error of approximately A_{VCL}/A_{VOL} . The DC gain error at A_{VCL} of 100 will be less than $100/5,000,000$, a 0.002%-of-full-scale gain error. The worst-case sum of offset and gain errors for this example is only 0.12% of full-scale, and is achieved without any external trimming of offset or gain.

Selection of a specific op-amp type within the High-Accuracy category is generally determined by impedance levels of the input signal and feedback elements. High impedances ($R_S > 10\text{k}\Omega$) imply a need for an op amp with low input bias currents. This need for low bias current can be met through use of FET-input op amps, or by using bipolar-input op amps specifically designed for low input-bias-current.

The OP-41/43 JFET-input op amps have less than $\pm 5\text{pA}$ of input bias current, and the OP-15/16/17 JFET-input op amps have bias currents specified to within $\pm 50\text{pA}$. At high temperature, however, the input bias current for JFET-input op amps rises to a level which is typically 3 orders of magnitude higher than the room-temperature value.

The OP-05, OP-07, OP-77, and OP-50 are bipolar op amps which have input bias cancellation circuitry that significantly reduces input-bias-current, and maintain low input-bias-current levels over temperature. For example, the OP-05/07/77 op amps have bias-current limits set at $\pm 4\text{nA}$ over the full Military temperature range. The OP-08, which is an improved LM108, has a superbeta input stage which also provides very good high-temperature high-impedance operation ($I_B \leq 3\text{nA}$ at 125°C).

The OP-22/32 programmable micropower op amps have PNP input stages which also have very low input bias current over temperature. Their input-bias-current remains below 5nA over the full Military temperature range.

Low noise, always desirable, is sometimes the primary consideration. In many high-gain active-filter or audio-amplifier applications, low noise can be more important than DC offset. These are the three basic rules for obtaining low noise:

- 1. Design with low impedances** — Using low impedances minimizes the effect of current noise flowing through the source impedance, reduces resistor thermal noise, and reduces stray pick-up of RF noise.
- 2. Restrict the system bandwidth** — Noise outside the frequency range of interest can usually be attenuated by filtering. Block high-frequency power-supply noise from the signal path by use of decoupling capacitors at the op-amp supply inputs.
- 3. Select a low-noise op amp** — Some op amps, such as the bipolar-input OP-27, are designed for minimum noise. The input stage current is set to a relatively high value which reduces input noise ($5.5\text{nV}/\sqrt{\text{Hz}}$ max at 10Hz). Output swing

is increased to $\pm 10V$ into 600Ω to allow the use of low-impedance, low-noise feedback elements.

Power Supply Considerations

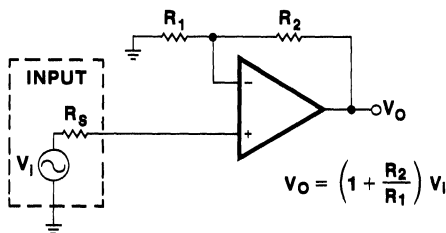
The op-amp power-supply requirements are the next factors to consider. If the circuit is to be operated from a battery, such as in portable instruments, missiles, or spacecraft, then narrow the selection to the "Low-Power, Wide Supply Range" category. Low-power op amps are designed for minimum quiescent supply current. Speed is traded off for lower power consumption and output drive is generally reduced. The input and output stages are designed for linear operation over a wide voltage range which is very helpful for single-power-supply operation.

The PMI line of low-power, wide-supply-range op amps all feature high open-loop gain, low input offsets, and high CMRR. They can provide high accuracy even at high closed-loop gain.

The low-power family includes *programmable* micropower op amps that offer the designer another dimension in circuit design. The quiescent supply current is set by an external resistor which allows the circuit designer to trade off quiescent supply current against speed. Since the quiescent current directly controls slew rate and gain-bandwidth product, these programmable op amps are easily frequency-compensated in such circuits as active filters, oscillators, or multi-stage instrumentation amplifiers.

DC ERROR CALCULATIONS FOR STANDARD CONFIGURATIONS

NONINVERTING CONFIGURATION



$$\text{Output Offset} = \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left(\frac{R_1 R_2}{R_1 + R_2} - R_S\right) I_B + \left(\frac{R_1 R_2}{R_1 + R_2} + R_S\right) \frac{I_{OS}}{2} \right]$$

Special Cases:

$$\text{Max Output Offset} = \left(1 + \frac{R_2}{R_1}\right) (V_{OS} + R_S I_{OS}) \text{ if } R_S = \frac{R_1 R_2}{R_1 + R_2}$$

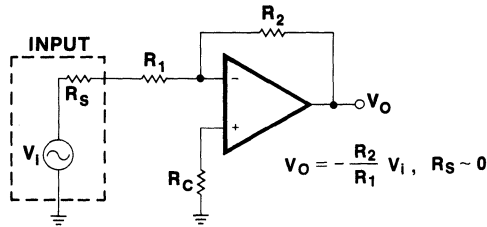
$$\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left| \frac{R_1 R_2}{R_1 + R_2} - R_S \right| I_B \right] \text{ if } I_{OS} \ll I_B$$

$$\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + R_S \left(I_B + \frac{I_{OS}}{2} \right) \right] \text{ if } R_S \gg \frac{R_1 R_2}{R_1 + R_2}$$

Note: I_B is the average of the input bias currents and I_{OS} is the difference.

$$\text{Gain Error} \sim \left(1 + \frac{R_2}{R_1}\right) \frac{1}{A_{VO}} + \frac{1}{CMRR}, \text{ where } A_{VO} = \text{Open-Loop Gain and } A_{VO} \gg \left(1 + \frac{R_2}{R_1}\right)$$

INVERTING CONFIGURATION



$$\text{Output Offset} = \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left(\frac{R_1 R_2}{R_1 + R_2} - R_C\right) I_B + \left(\frac{R_1 R_2}{R_1 + R_2} + R_C\right) \frac{I_{OS}}{2} \right] \text{ if } R_S \sim 0$$

Special Cases:

$$\text{Max Output Offset} = \left(1 + \frac{R_2}{R_1}\right) (V_{OS} + R_C I_{OS}) \text{ if } R_C = \frac{R_1 R_2}{R_1 + R_2}$$

$$\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left| \frac{R_1 R_2}{R_1 + R_2} - R_C \right| I_B \right] \text{ if } I_{OS} \ll I_B$$

$$\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \frac{R_1 R_2}{R_1 + R_2} \left(I_B + \frac{I_{OS}}{2} \right) \right] \text{ if } R_C = 0$$

Note: I_B is the average of the input bias currents and I_{OS} is the difference.

$$\text{Gain Error} \sim \left(1 + \frac{R_2}{R_1}\right) \frac{1}{A_{VO}} + \frac{R_S}{R_1} \frac{R_2}{R_1}, \text{ where } A_{VO} = \text{Open-Loop Gain and } R_S \ll R_1$$



OPERATIONAL AMPLIFIERS

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OPERATIONAL AMPLIFIER SELECTION GUIDE

The Operational Amplifier Selection Guide chart highlights PMI's line of operational amplifiers. The matrix indicates the most essential parametric differences for each product group.

"General Purpose" op amps are usually the least expensive and are recommended for applications where impedance levels are relatively low, closed-loop gain is low, and speed requirements are moderate. JFET inputs provide lower input-bias-currents and better bandwidth than standard bipolar inputs, but input voltage offsets and noise are generally better for the bipolar input amplifiers.

The "High Accuracy" category presents the best amplifiers for high-gain applications. A combination of low input-offset-voltage, high open-loop gain, and high CMRR provide excellent DC accuracy even at high closed-loop gain. The OP-27, OP-37 and OP-50 are best for minimum

input voltage noise. The OP-08 and OP-12 provide an excellent combination of low input-bias-current, low offset voltage, and moderate power drain. The OP-07 and its improved version, the OP-77 offer a selection of the lowest offset voltages ($60\mu\text{V}$ max to $250\mu\text{V}$ max) combined with low input-bias-current ($\pm 2\text{nA}$ max to $\pm 12\text{nA}$ max) and have become an industry standard for high-precision applications.

PMI is a leader in op amps featuring low power consumption. The OP-20/21/22/32 are micropower op amps that operate with only a few microamps of supply drain. PSRR and CMRR are high, and the input-voltage-range is wide. Such features work together to make these amplifiers ideal for battery-powered applications or for operation from a single supply voltage. The OP-22/32 can be programmed to operate over any supply current from $1\mu\text{A}$ to $400\mu\text{A}$ and is excellent for battery-powered designs.

5

OPERATIONAL AMPLIFIERS

	General Purpose				Precision High-Speed JFET Input	High Accuracy	Low Power, Low Input-Bias-Current	Micropower																					
	Bipolar		JFET																										
	OP-01	OP-02	OP-04, OP-14	OP-09, OP-11	PM-155	PM-156, PM-157	OP-15	OP-16, OP-17	OP-43	OP-215	OP-05, OP-06, OP-07	OP-08, OP-12	OP-27, OP-37	OP-50, OP-77	OP-207, OP-227	OP-400	OP-41	PM-108	PM-2108	PM-148	OP-20	OP-21	OP-22	OP-220	OP-221	OP-420	OP-421	OP-32	
Monolithic Technology																													
Bipolar Input	•	•	•	•							•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
JFET					•	•	•	•	•	•							•												
Packages																													
Single	•	•			•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Dual			•																										
Quad				•												•													
Ultra Low Offset, $V_{OS} \leq 200\mu\text{V}$											•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Low Offset, $V_{OS} \leq 1\text{mV}$	•	•	•	•			•	•	•	•							•	•	•	•	•	•	•	•	•	•	•	•	•
Low Bias Current																													
$I_B \leq 100\text{pA}$					•	•	•	•	•	•							•												
$I_B \leq 5\text{nA}$											•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
High Gain, $A_{VOL} \geq 1$ Million V/V								•																					
High Slew Rate, $SR \geq 10\text{V}/\mu\text{s}$	•				•		•						•																
Low Power																													
$I_{SY} \leq 1\text{mA}/\text{Amplifier}$												•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
$I_{SY} \leq 100\mu\text{A}/\text{Amplifier}$																							•	•	•	•	•	•	•
Low Noise ($f_O = 1\text{kHz}$)																													
$e_n \leq 6\text{nV}/\sqrt{\text{Hz}}$													•	•	•														
$i_n \leq 0.25\text{pA}/\sqrt{\text{Hz}}$																	•												

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FEATURES

- **Fast Settling Time** 1 μ s to 0.1% Max
- **High Slew Rate** 12V/ μ s Min
- **Power Bandwidth** 150kHz Min
- **Low Power Consumption** 90mW Max
- **Excellent DC Specifications**
- **Internally Compensated**
- **Ideal DAC Output Amplifier**
- **MIL-STD-883 Processing Available**
- **Fits Standard 741 Sockets**
- **Low Cost**

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	
0.7	OP01J*	OP01Z*		MIL
0.7	OP01HJ	OP01HZ	OP01HP	COM
5.0	OP01GJ*	OP01GZ*		MIL
5.0	OP01CJ	OP01CZ	OP01CP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

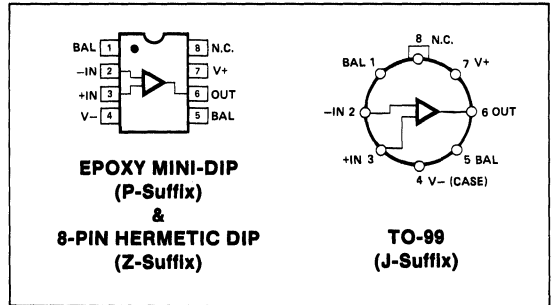
GENERAL DESCRIPTION

The OP-01 series of monolithic inverting high-speed operational amplifiers combines high slew rate, fast settling time

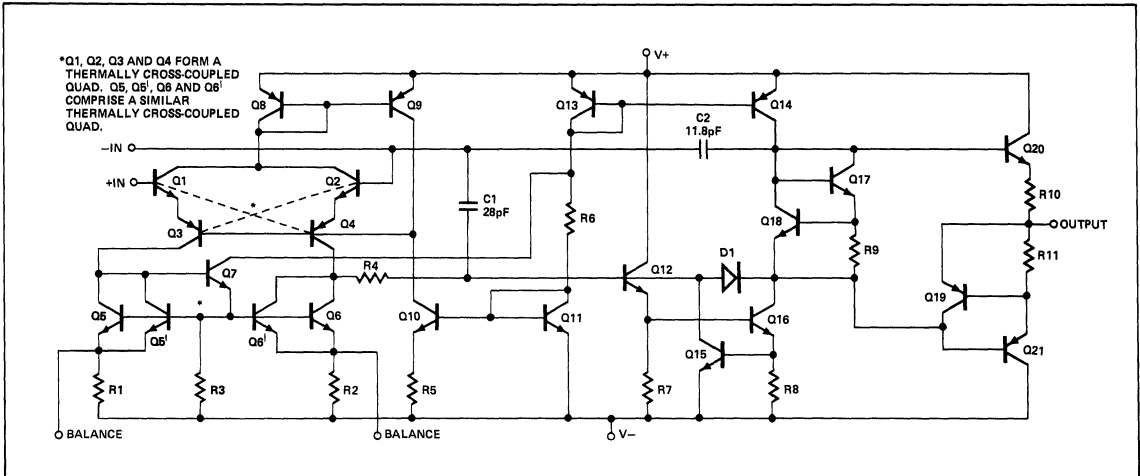
and excellent DC input characteristics. An internal feed-forward frequency compensation network provides simplicity of application — no external capacitors are required for stable, high-speed performance. The fast output response is achieved without sacrifice of input bias current or power consumption. A 250kHz typical power bandwidth is attained with a small-signal bandwidth of only 2.5MHz, thus board layout is non-critical. The OP-01 is completely protected at both input and output, fits standard 741 sockets, and is offset nulled with a 10k Ω potentiometer.

The fast output response combined with excellent settling time makes the OP-01 ideal for use as a D/A converter output amplifier.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS (Note 2)

Total Supply Voltage, OP-01, OP-01H, OP-01N, OP-01NT, OP-01G, OP-01GT	±22V
OP-01G, OP-01C, OP-01GR	±20V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 3)	±15V
Short-Circuit Duration	Indefinite
Operating Temperature Range	
OP-01, OP-01G	-55°C to +125°C
OP-01H, OP-01C	0°C to +70°C
DICE Junction Temperature (T _J)	-65°C to +150°C
Storage Temperature Range	
J and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C

Lead Temperature (Soldering, 60 sec) 300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	35°C	5.6mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

3. For supply voltages less than ±15V, the maximum input voltage is the supply voltage.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01 OP-01H			OP-01G OP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S ≤ 20kΩ	—	0.3	0.7	—	2.0	5.0	mV
Input Offset Current	I _{OS}		—	0.5	2.0	—	2.0	20	nA
Input Bias Current	I _B		—	18	30	—	25	100	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±10V R _S ≤ 20kΩ	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±5V to ±20V R _S ≤ 20kΩ	—	10	60	—	100	150	μV/V
Output Voltage Swing	V _O	R _L ≥ 5kΩ R _L ≥ 2kΩ	±12.5 ±12.0	±13.5 ±13.0	—	±12.5 ±12.0	±13.5 ±13.0	—	V
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2kΩ V _O = ±10V	50	100	—	25	75	—	V/mV
Power Consumption	P _d	V _{OUT} = 0	—	50	90	—	50	90	mW
Settling Time to 0.1% (Summing Node Error)	t _S	A _V = -1 (Notes 1, 2) V _{IN} = 5V	—	0.7	1.0	—	0.7	1.0	μs
Slew Rate (Notes 2, 3)	SR	A _V = -1, R _S = 3k to 5kΩ	12	18	—	12	18	—	V/μs
Large-Signal Bandwidth (Notes 3, 4)			150	250	—	150	250	—	kHz
Small-Signal Bandwidth (Notes 3, 4)			1.5	2.5	—	1.5	2.5	—	MHz
Risetime	t _r	A _V = -1 V _{IN} = 50mV	—	150	—	—	150	—	ns
Overshoot	OS		—	2	—	—	2	—	%

NOTES:

1. R_L = 25kΩ; C_L = 50pF. See Settling Time Test Circuit.
2. Sample tested.
3. See applications information.
4. Guaranteed by design.

5
OPERATIONAL AMPLIFIERS



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-01, OP-01G and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-01H, OP-01C, unless otherwise noted.

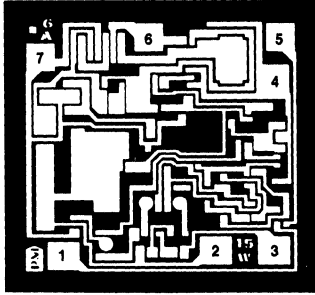
PARAMETER	SYMBOL	CONDITIONS	OP-01 OP-01H			OP-01G OP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.0	—	3.0	6.0	mV
Input Offset Current	I_{OS}		—	1	4	—	4	40	nA
Input Bias Current	I_B		—	30	50	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	60	—	15	50	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	± 12.5 ± 12.0	± 13.5 ± 13.0	—	± 12.5 ± 12.0	± 13.5 ± 13.0	—	V
Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S \leq 5k\Omega$	—	2	8	—	5	20	$\mu V/^\circ C$

NOTE:

1. Sample tested.



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)

DIE SIZE 0.046 × 0.042 inch, 1932 sq. mils
(1.17 × 1.07 mm, 1.25 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
5. NULL
6. OUTPUT
7. V+

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-01N, OP-01G and OP-01GR devices; $T_A = 125^\circ C$ for OP-01NT and OP-01GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01NT LIMIT	OP-01N LIMIT	OP-01GT LIMIT	OP-01G LIMIT	OP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1.0	0.7	3.0	2.0	5.0	mV MAX
Input Offset Current	I_{OS}		4	2	10	5	20	nA MAX
Input Bias Current	I_B		50	30	100	50	100	nA MAX
Input Voltage Range	IVR		± 10	± 12	± 10	± 12	± 12	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	85	80	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	$\mu V/V$ MAX
Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	± 12.5 ± 12.0	± 12.5 ± 12.0	± 12.5 ± 12.0	± 12.5 ± 12.0	± 12.5 ± 12.0	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	50	25	50	25	V/mV MIN
Power Consumption	P_d	$V_{OUT} = 0$	—	90	—	90	90	mW MAX

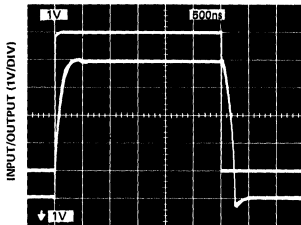
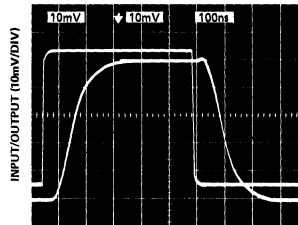
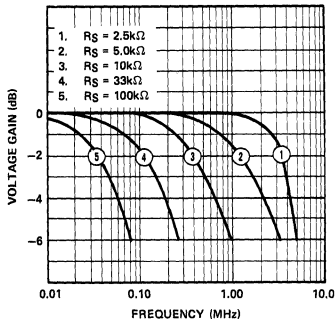
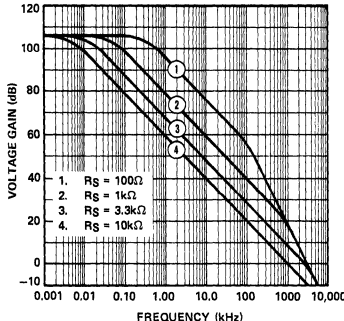
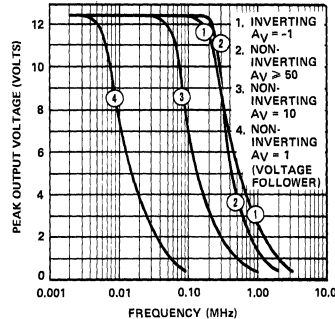
NOTES:

For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.

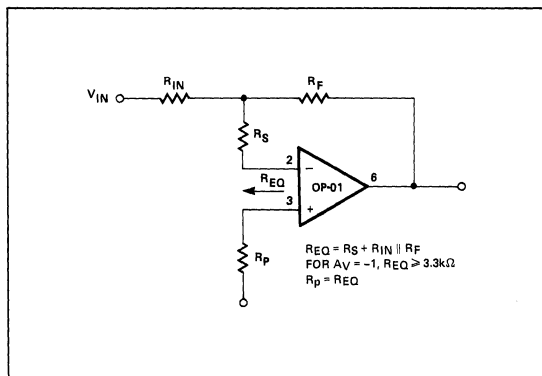
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES TYPICAL	UNITS
Slew Rate	SR	$A_{VCL} = -1$, $R_S = 3k\Omega$ to $5k\Omega$	18	V/ μs
Settling Time to 0.1% (Summing Node Error)	t_S	$V_{IN} = 5V$ $A_V = -1$ $R_L = 2k\Omega$ (See Settling Time Test Circuit) $C_L = 50pF$	1.0	μs
Large-Signal Bandwidth			250	kHz
Small-Signal Bandwidth			2.5	MHz
Risetime	t_r	$V_{IN} = 50mV$ $A_V = -1$	150	ns

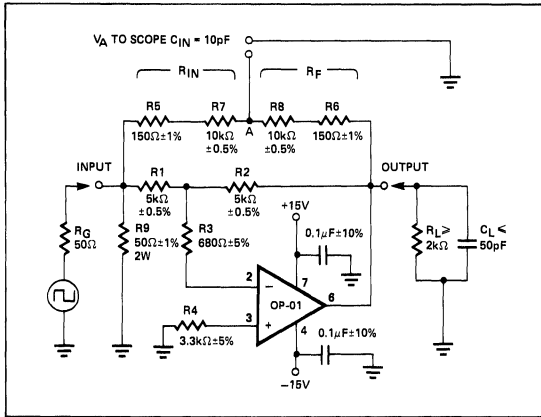
TYPICAL PERFORMANCE CHARACTERISTICS
LARGE-SIGNAL PULSE RESPONSE

 TIME (500ns/DIV)
 $V_S = \pm 15V, A_V = -1, R_L = 2k\Omega, C_L = 50pF$
SMALL-SIGNAL PULSE RESPONSE

 TIME (100ns/DIV)
 $V_S = \pm 15V, A_V = -1, R_L = 2k\Omega, C_L = 50pF$
UNITY-GAIN BANDWIDTH vs SOURCE RESISTANCE

OPEN-LOOP GAIN vs FREQUENCY

LARGE-SIGNAL OUTPUT SWING vs FREQUENCY

APPLICATIONS INFORMATION

The OP-01 incorporates an internal feed-forward compensation network to provide fast slewing and settling times in all inverting and moderate-to-high-gain noninverting applications. Unity-gain bandwidth is a function of the total equivalent source resistance seen by the inverting terminal. Proper choice of this resistance will allow the user to maximize bandwidth while assuring proper stability. The equivalent-inverting-terminal-resistance is defined as $R_{IN} \parallel R_F$, and it must be greater than $3.3k\Omega$ to assure stability in all closed-loop gain configurations including unity gain. Should $R_{IN} \parallel R_F \leq 3.3k\Omega$, a resistor (R_S) may be placed between the inverting input and the sum node to provide the required resistance. (See Fast Inverting Amplifier Diagram.) Lower values of total equivalent resistance may be used to improve bandwidth in higher closed-loop gain configurations, as indicated by the Open-Loop Gain vs. Frequency plot.

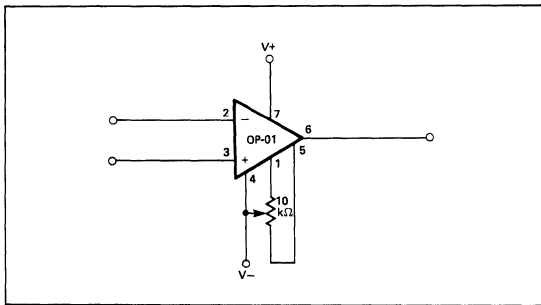
FAST INVERTING AMPLIFIER


SETTLING-TIME TEST CIRCUIT

Settling time may be measured using the circuit shown below. This circuit incorporates the "false sum node" technique to produce accurate, repeatable results. For a 5V input step, 0.1% settling will be achieved when the false sum node settles to within $\pm 2.5\text{mV}$ of its final value. The oscilloscope used for observation of the false sum node should have wide bandwidth, fast overload recovery time, and be used with a low capacity probe ($\leq 10\text{pF}$, including strays). A Tektronix 7504 scope with a 7A11 probe or equivalent is suggested. The pulse generator should have a 50Ω output impedance and be capable of a 5V rise time in $\leq 20\text{ns}$ with ringing less than 2.5mV after $0.5\mu\text{s}$. Measurements to 0.1% require R_{IN} to equal R_F within 0.01%; R_5 and R_6 are used as trimming resistors to achieve this matching.

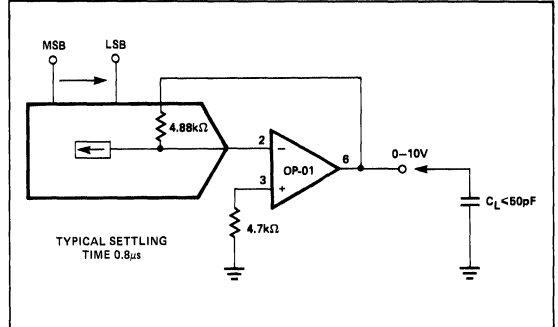


OFFSET NULLING CIRCUIT

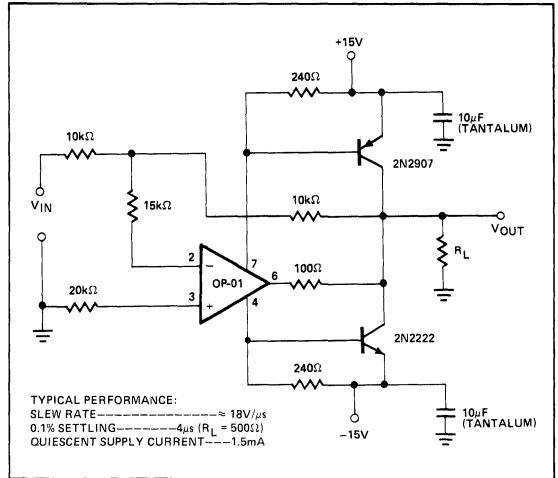


TYPICAL APPLICATIONS

FAST VOLTAGE-OUTPUT D/A CONVERTER



PRECISION POWER-BOOSTER CIRCUIT



Precision Monolithics Inc.

FEATURES

- Excellent DC Specifications
- Low Noise $0.65 \mu V_{p-p}$ Typ
- Low Drift (TCV_{OS}) $8 \mu V/^{\circ}C$ Max
- Silicon-Nitride Passivation
- 125° C Tested Dice Available
- "Premium" 741 Replacement

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	
0.5	OP02AJ*	OP02AZ*		MIL
0.5	OP02EJ	OP02EZ	OP02EP	COM
2.0	OP02J*	OP02Z*		MIL
2.0	OP02CJ	OP02CZ	OP02CP	COM
5.0	OP02BJ*	OP02BZ*		MIL
5.0	OP02DJ	OP02DZ	OP02DP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

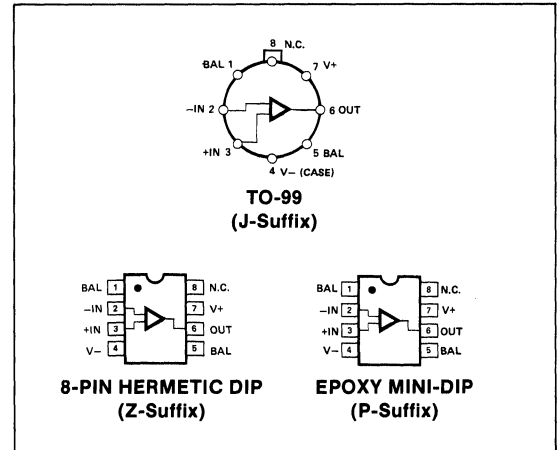
GENERAL DESCRIPTION

This high-performance general-purpose operational amplifier provides significant improvements over industry-standard and "premium" 741 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS} , I_{OS} , I_B , CMRR, PSRR, and A_{VO} are

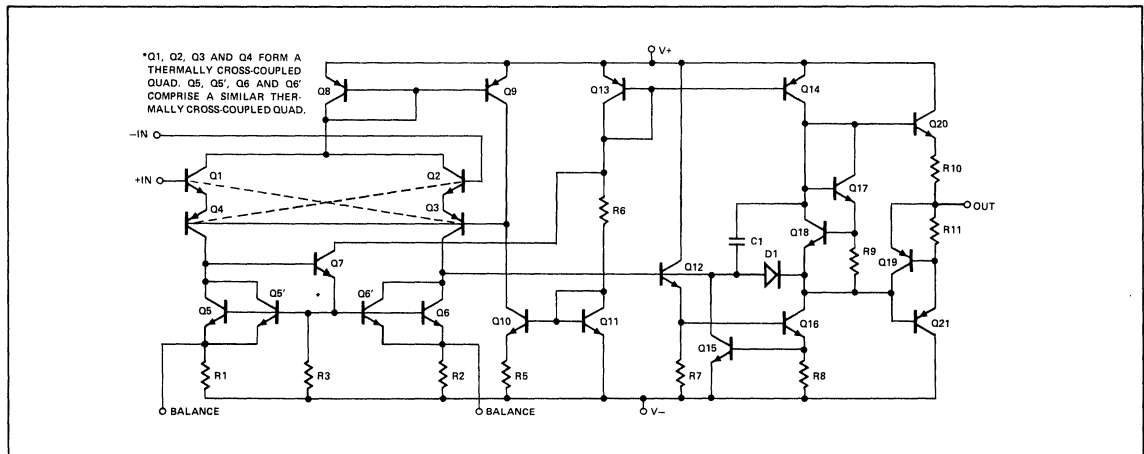
guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise." A thermally-symmetrical input-stage design provides low input offset voltage drift and insensitivity to output load conditions.

The OP-02 is a direct replacement for the 741. It is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low-drift or low-noise selected types.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±22V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
OP-02A, OP-02, OP-02B	-55°C to +125°C
OP-02E, OP-02C, OP-02D	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T _J)	-65°C to +150°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

- Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02A OP-02E			OP-02 OP-02C			OP-02B OP-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S ≤ 20kΩ	—	0.3	0.5	—	1	2	—	3	5	mV
Input Offset Current	I _{OS}		—	0.5	2	—	1	5	—	5	25	nA
Input Bias Current	I _B		—	18	30	—	20	50	—	30	100	nA
Input Resistance-Differential-Mode	R _{IN}	(Note 2)	3.4	5.7	—	2.0	5.2	—	1	3.5	—	MΩ
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±10V R _S ≤ 20kΩ	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±5 to ±20V R _S ≤ 20kΩ	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V _O	R _L ≥ 2kΩ	±12	±13	—	±12	±13	—	±12	±13	—	V
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2kΩ V _O = ±10V	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption	P _d	V _O = 0V	—	40	70	—	50	90	—	50	90	mW
Input Noise Voltage	e _{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV _{p-p}
Input Noise Voltage Density	e _n	f _O = 10Hz	—	25	—	—	25	—	—	25	—	nV/√Hz
		f _O = 100Hz	—	22	—	—	22	—	—	22	—	
		f _O = 1000Hz	—	21	—	—	21	—	—	21	—	
Input Noise Current	i _{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA _{p-p}
Input Noise Current Density	i _n	f _O = 10Hz	—	1.4	—	—	1.4	—	—	1.4	—	pA/√Hz
		f _O = 100Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		f _O = 1000Hz	—	0.4	—	—	0.4	—	—	0.4	—	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large-Signal Bandwidth		V _O = 20V _{p-p} (Note 1)	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth	BW	A _{VCL} = +1 (Note 3)	1	1.3	—	1	1.3	—	1	1.3	—	MHz
Risetime	t _r	A _{VCL} = +1 V _{IN} = 50mV (Note 1)	—	200	350	—	200	350	—	200	350	ns
Overshoot	OS	(Note 1)	—	5	10	—	5	10	—	5	10	%

NOTES:

- Sample tested.
- Guaranteed by input bias current.
- Guaranteed by risetime.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02A			OP-02			OP-02B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.5	1	—	1.4	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1	5	—	2	10	—	5	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	75	—	15	150	—	30	300	$pA/^\circ C$
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	95	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 10	± 13	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

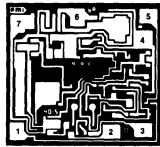
PARAMETER	SYMBOL	CONDITIONS	OP-02E			OP-02C			OP-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.7	4	—	1.4	10	—	5	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	$pA/^\circ C$
Input Bias Current	I_B		—	22	50	—	25	100	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	90	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 10	± 13	—	V

NOTE:

1. Sample tested.



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.046 × 0.042 Inch, 1932 sq. mils
(1.17 × 1.07 mm, 1.25 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V⁻
5. NULL
6. OUTPUT
7. V⁺

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at V_S = ±15V, T_A = 25°C for OP-02N, OP-02G and OP-02GR devices; T_A = 125°C for OP-02NT and OP-02GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02NT LIMIT	OP-02N LIMIT	OP-02GT LIMIT	OP-02G LIMIT	OP-02GR LIMIT	UNITS
Input Offset Voltage	V _{OS}	R _S ≤ 20kΩ	1	0.5	3	2	5	mV MAX
Input Offset Current	I _{OS}		5	3	6	5	25	nA MAX
Input Bias Current	I _B		50	30	60	50	200	nA MAX
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±10V R _S ≤ 20kΩ	80	85	80	80	70	dB MIN
Power Supply Rejection Ratio	PSRR	V _S = ±5V to ±20V R _S ≤ 20kΩ	60	60	100	100	150	μV/V MAX
Output Voltage Swing	V _O	R _L ≥ 2kΩ	±12	±12	±12	±12	±12	V MIN
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2kΩ V _O = ±10V	50	100	25	50	25	V/mV MIN
Power Consumption	P _d	V _O = 0V	—	90	—	90	90	mW MAX

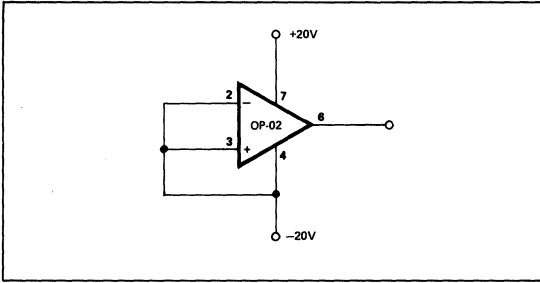
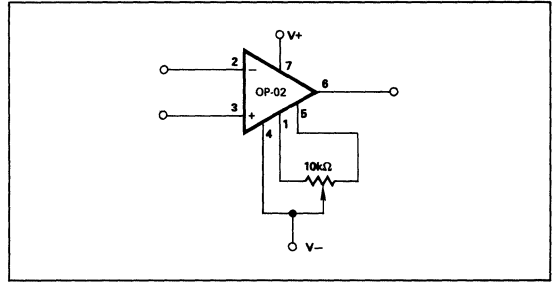
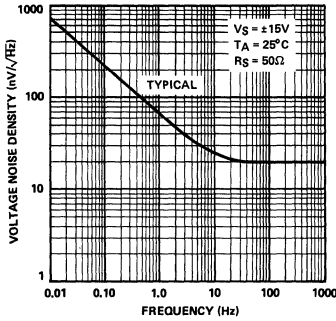
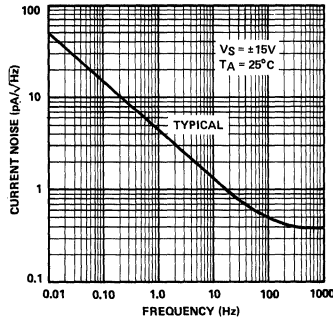
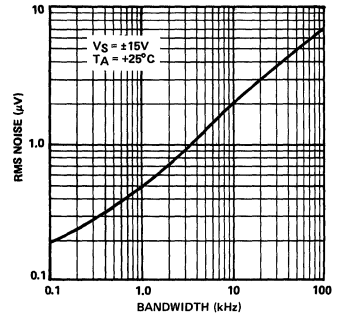
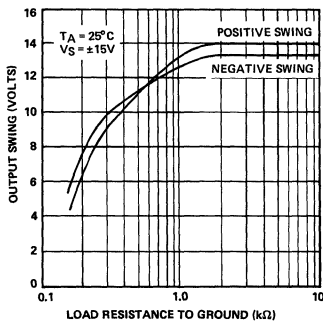
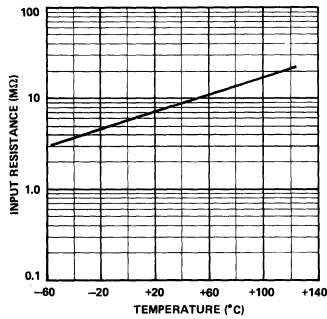
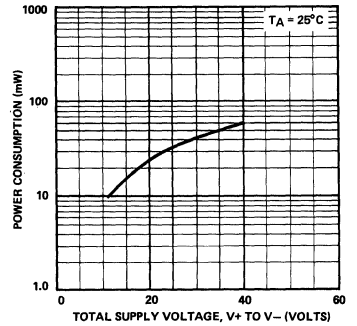
NOTE:

For 25°C characteristics of NT and GT devices, see N and G characteristics, respectively.

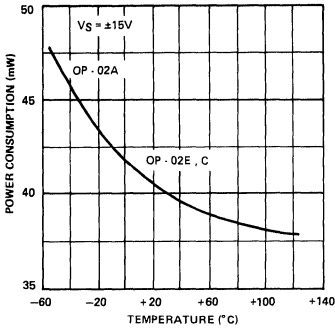
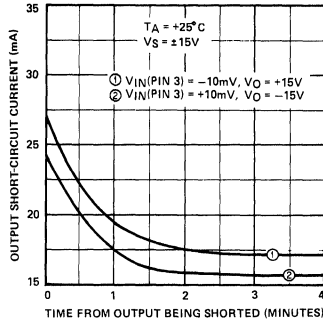
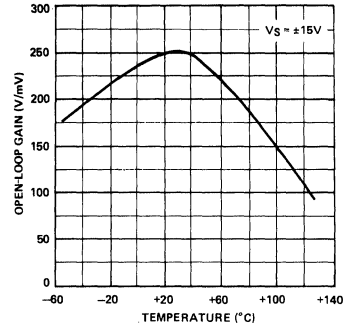
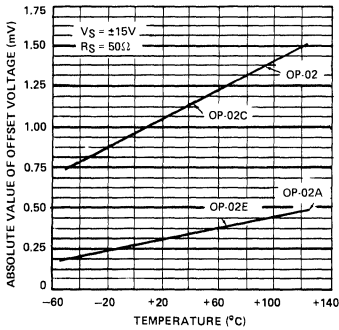
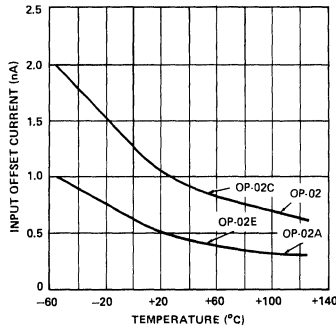
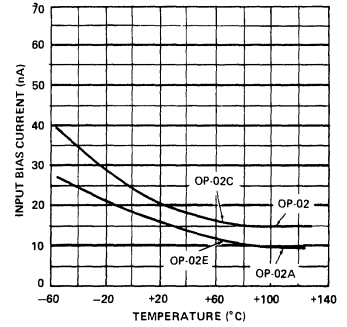
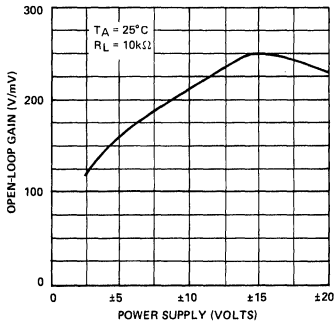
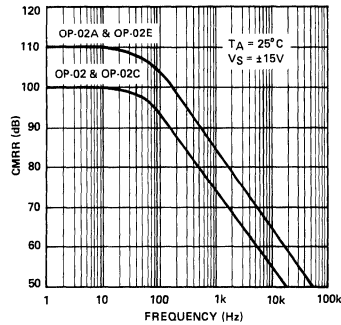
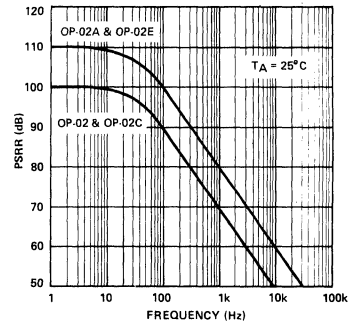
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

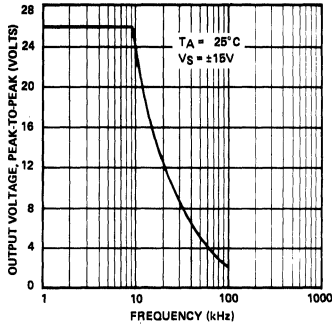
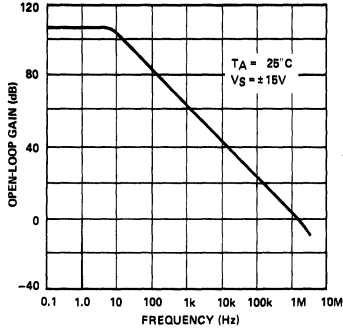
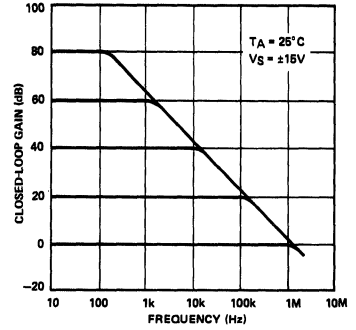
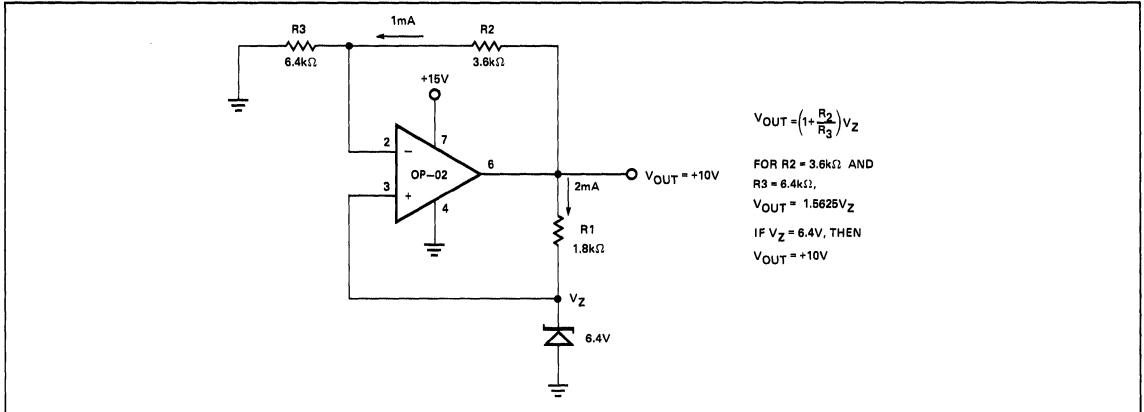
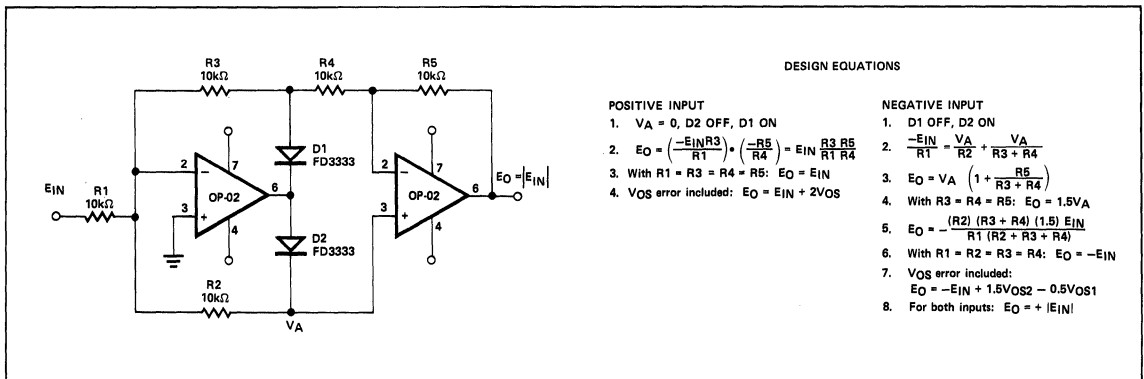
TYPICAL ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02NT OP-02N TYPICAL	OP-02GT OP-02G TYPICAL	OP-02GR TYPICAL	UNITS
Input Resistance Differential-Mode	R _{IN}		5.7	5.2	3.5	MΩ
Input Noise Voltage	e _{np-p}	0.1Hz to 10Hz	0.65	0.65	0.65	μV _{p-p}
Input Noise Voltage Density	e _n	f _O = 10Hz	25	25	25	nV/√Hz
		f _O = 100Hz	22	22	22	
		f _O = 1000Hz	21	21	21	
Input Noise Current	i _{np-p}	0.1Hz to 10Hz	12.8	12.8	12.8	pA _{p-p}
Input Noise Current Density	i _n	f _O = 10Hz	1.4	1.4	1.4	pA/√Hz
		f _O = 100Hz	0.7	0.7	0.7	
		f _O = 1000Hz	0.4	0.4	0.4	
Slew Rate	SR		0.5	0.5	0.5	V/μs
Large-Signal Bandwidth		V _O = 20V _{p-p}	8	8	8	kHz
Closed-Loop Bandwidth	BW	A _{VCL} = +1	1.3	1.3	1.3	MHz
Risetime	t _r	A _V = +1 V _{IN} = 50mV	200	200	200	ns
Overshoot	OS		15	15	15	%
Average Input Offset Voltage Drift	TCV _{OS}	R _S = 500Ω (Note 1)	2	4	8	μV/°C
Average Input Offset Current Drift	TCI _{OS}		7.5	15	30	pA/°C

BURN-IN CIRCUIT

OFFSET NULLING CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS
INPUT SPOT NOISE VOLTAGE vs FREQUENCY

INPUT SPOT NOISE CURRENT vs FREQUENCY

INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

OUTPUT VOLTAGE vs LOAD RESISTANCE

DIFFERENTIAL INPUT RESISTANCE vs TEMPERATURE

POWER CONSUMPTION vs POWER SUPPLY


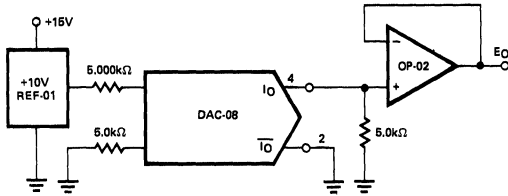
TYPICAL PERFORMANCE CHARACTERISTICS

POWER CONSUMPTION vs TEMPERATURE

OUTPUT SHORT-CIRCUIT CURRENT vs TIME

OPEN-LOOP GAIN vs TEMPERATURE

UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE

INPUT OFFSET CURRENT vs TEMPERATURE

INPUT BIAS CURRENT vs TEMPERATURE

OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE

CMRR vs FREQUENCY

PSRR vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY

OPEN-LOOP FREQUENCY RESPONSE

CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS

TYPICAL APPLICATIONS
HIGH-STABILITY VOLTAGE REFERENCE

ABSOLUTE VALUE CIRCUIT


TYPICAL APPLICATIONS

DAC-08 OUTPUT AMPLIFIER



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC) CONNECT NON-INVERTING INPUT OF OP-AMP TO \bar{I}_0 (PIN 2), CONNECT I_0 (PIN 4) TO GROUND.

INPUT/OUTPUT TABLE

	B1	B2	B3	B4	B5	B6	B7	B8	I_0 mA	E_0
FULL-SCALE -1 LSB	1	1	1	1	1	1	1	1	1.992	-9.960
FULL-SCALE -2 LSB	1	1	1	1	1	1	1	0	1.984	-9.920
HALF-SCALE +LSB	1	0	0	0	0	0	0	0	1.008	-5.040
HALF-SCALE -LSB	1	0	0	0	0	0	0	0	1.000	-5.000
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	0.992	-4.960
ZERO-SCALE +LSB	0	0	0	0	0	0	0	0	0.0008	-0.040
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	0.000

Precision Monolithics Inc.

FEATURES

- Excellent DC Input Specifications
- Matched V_{OS} and CMRR
- OP-14 Fits Standard 1458/1558 Sockets
- Internally Compensated
- Low Noise
- Low Drift
- Low Cost
- 0° C/ +70° C and -55° C/ +125° C Models
- Silicon-Nitride Passivation
- Models with MIL-STD-883 Class B Processing Available From Stock

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$	PACKAGE					
	HERMETIC		PLASTIC		OPERATING	
	TO-99 8-PIN	TO-100 10-PIN	DIP 8-PIN	DIP 14-PIN	DIP 8-PIN	TEMPERATURE RANGE
V_{OS} (mV)						
0.75	OP14AJ*	OP04AK*	OP14AZ*	OP04AY*		MIL
0.75	OP14EJ	OP14EZ	OP04EY	OP14EP		COM
2.0	OP14J*	OP04K*	OP14Z*	OP04Y*		MIL
2.0	OP14CJ	OP04CK	OP14CZ	OP04CY	OP14CP	COM
5.0	OP14BJ*	OP04BK*	OP14BZ*	OP04BY*		MIL
5.0	OP14DJ	OP14DZ	OP04DY	OP14DP		COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

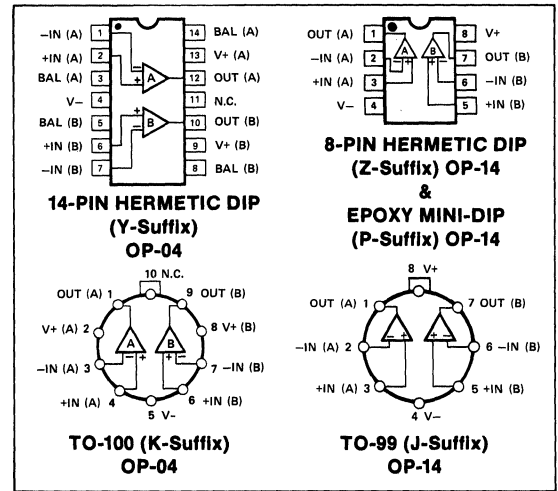
† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

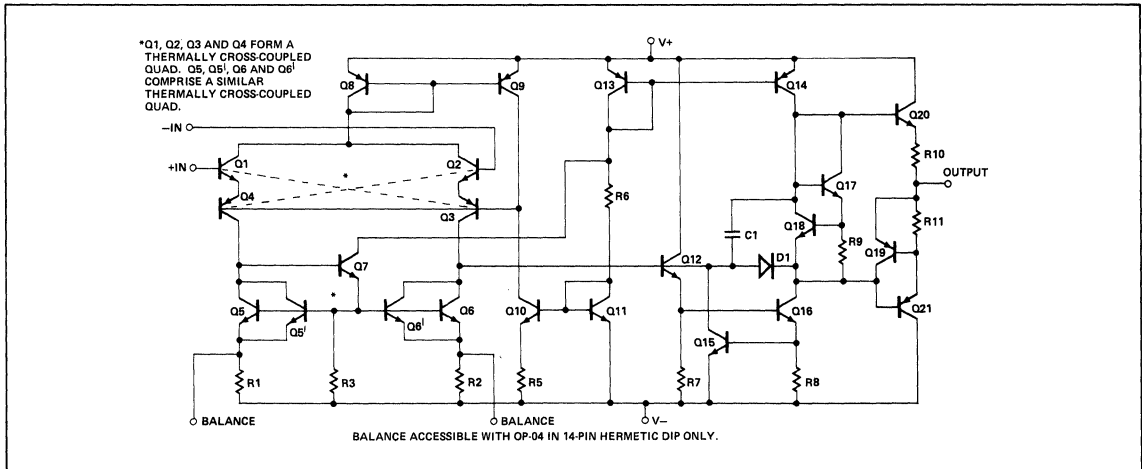
The OP-04/OP-14 series of dual general-purpose operational amplifiers provides significant improvements over industry-standard 747 and 1458/1558 (OP-14) types while maintaining

pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS} , I_{OS} , I_B , CMRR, PSRR and A_{VO} , are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise". A thermally-symmetrical input stage design provides low TCV_{OS} , TCI_{OS} , and insensitivity to output load conditions. This series is ideal for upgrading existing designs where accuracy improvements are desired. For more stringent requirements, refer to the OP-207, OP-220, or OP-221 dual-matched operational amplifier data sheets.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (Each Amplifier)





ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	± 22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	± 30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, K, Y, and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
A, Plain, B-Suffix	-55°C to +125°C
E, C, D-Suffix	0°C to +70°C
DICE Junction Temperature (T _J)	-65°C to +150°C

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y) OP-04	100°C	10.0mW/°C
TO-100 (K) OP-04	80°C	7.1mW/°C
TO-99 (J) OP-14	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z) OP-14	75°C	6.7mW/°C
8-Pin Plastic DIP (P) OP-14	36°C	5.6mW/°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

MATCHING CHARACTERISTICS at V_S = ± 15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A OP-04E OP-14A OP-14E			OP-04 OP-04C OP-14 OP-14C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV _{OS}	R _S ≤ 20kΩ	—	0.3	1	—	1	2	mV
Common-Mode Rejection Ratio Match	ΔCMRR	V _{CM} = ± 10V, R _S ≤ 100Ω	94	106	—	94	106	—	dB

MATCHING CHARACTERISTICS at V_S = ± 15V, -55°C ≤ T_A ≤ + 125°C for OP-04A, OP-14A, OP-04 and OP-14, 0°C ≤ T_A ≤ 70°C for OP-04E, OP-14E, OP-04C and OP-14C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A OP-04E OP-14A OP-14E			OP-04 OP-04C OP-14 OP-14C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV _{OS}	R _S ≤ 20kΩ	—	0.5	1.5	—	1.5	3	mV
Common-Mode Rejection Ratio Match	ΔCMRR	V _{CM} = ± 10V, R _S ≤ 100Ω	90	100	—	90	100	—	dB

ELECTRICAL CHARACTERISTICS (Each Amplifier) at V_S = ± 15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A			OP-04/OP-14			OP-04B/OP-14B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S ≤ 20kΩ	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	I _{OS}		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	I _B		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	R _{IN}	(Note 3)	2.0	7.5	—	1.35	7	—	1	5	—	MΩ
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ± 10V R _S ≤ 20kΩ	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ± 5V to ± 20V R _S ≤ 20kΩ	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V _O	R _L ≥ 2kΩ	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

**ELECTRICAL CHARACTERISTICS (Each Amplifier)** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A			OP-04/OP-14			OP-04B/OP-14B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	200	—	V/mV
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	25	—	—	25	—	—	25	—	nV/\sqrt{Hz}
		$f_O = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_O = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	pA/\sqrt{Hz}
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	$V/\mu s$
Large-Signal Bandwidth (Note 1)		$V_O = 20V_{p-p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1.0$	1.0	1.3	—	1.0	1.3	—	1.0	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$, $V_{IN} = 50mV_{p-p}$ $R_L = 2k\Omega$, $C_L = 50pF$	—	260	350	—	260	350	—	260	350	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV_{p-p}$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A			OP-04/OP-14			OP-04B/OP-14B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	$pA/^\circ C$
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 10	± 13	—	V

NOTES:

1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by input bias current.
4. Guaranteed by maximum risetime.

**ELECTRICAL CHARACTERISTICS (Each Amplifier)** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04E/OP-14E			OP-04C/OP-14C			OP-04D/OP-14D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	2.0	7.5	—	1.35	7	—	1	5	—	M Ω
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	25	—	—	25	—	—	25	—	nV/\sqrt{Hz}
		$f_O = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_O = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	pA/\sqrt{Hz}
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/ μs
Large-Signal Bandwidth (Note 1)		$V_O = 20V_{p-p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1$	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	260	350	—	260	350	—	260	350	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

NOTES:

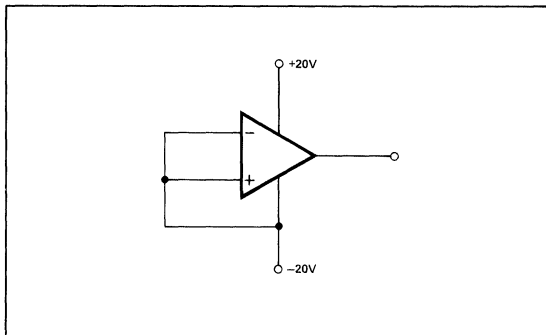
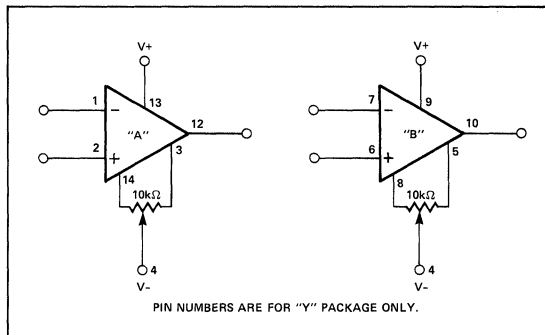
1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by input bias current.
4. Guaranteed by maximum risetime.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04E/OP-14E			OP-04C/OP-14C			OP-04D/OP-14D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	$pA/^\circ C$
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 10	± 13	—	V

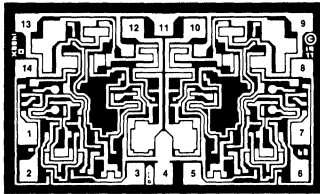
NOTES:

1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by design.

BURN-IN CIRCUIT (1/2 of OP-04, OP-14)

OFFSET ADJUST CIRCUIT




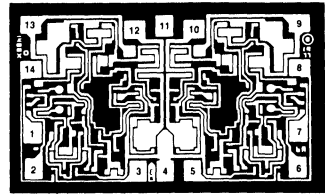
DICE CHARACTERISTICS



OP-14

DIE SIZE 0.080 × 0.050 Inch, 4000 sq. mils
(2.03 × 1.27 mm, 2.58 sq. mm)

For additional DICE information refer to
1986 Data Book, Section 2.



OP-04

- 1. INVERTING INPUT (A)
- 2. NONINVERTING INPUT (A)
- 3. BALANCE (A)
- 4. V-
- 5. BALANCE (B)
- 6. NONINVERTING INPUT (B)
- 7. INVERTING INPUT (B)
- 8. BALANCE (B)
- 9. V+
- 10. OUTPUT (B)
- 11. V+
- 12. OUTPUT (A)
- 13. V+
- 14. BALANCE (A)

NOTE: 9, 11 and 13 are internally connected.

- 1. INVERTING INPUT (A)
- 2. NONINVERTING INPUT (A)
- 3. BALANCE (A)
- 4. V-
- 5. BALANCE (B)
- 6. NONINVERTING INPUT (B)
- 7. INVERTING INPUT (B)
- 8. BALANCE (B)
- 9. V+ (B)
- 10. OUTPUT (B)
- 11. NO CONNECTIONS
- 12. OUTPUT (A)
- 13. V+ (A)
- 14. BALANCE (A)

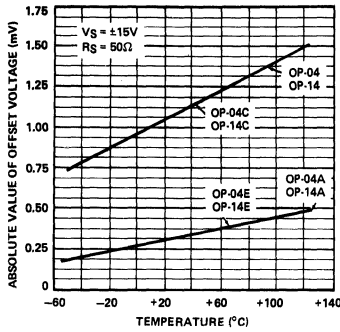
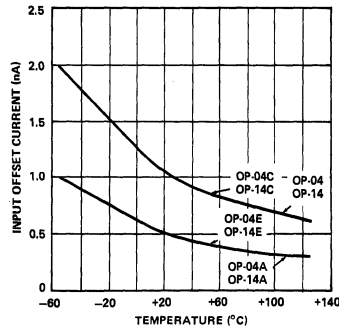
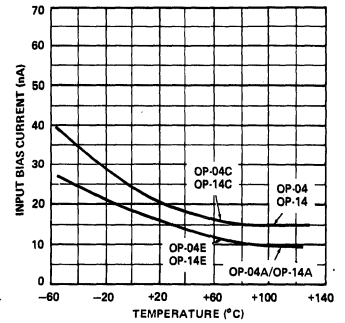
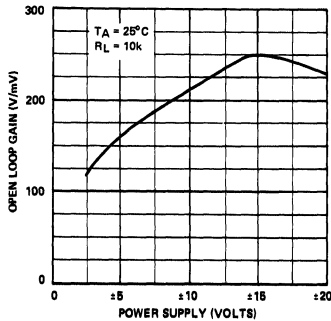
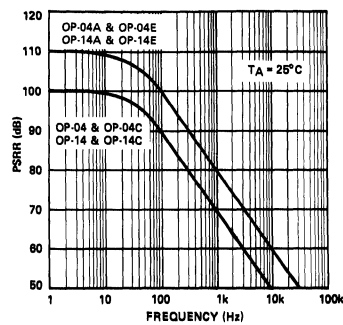
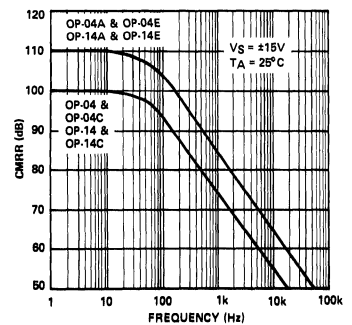
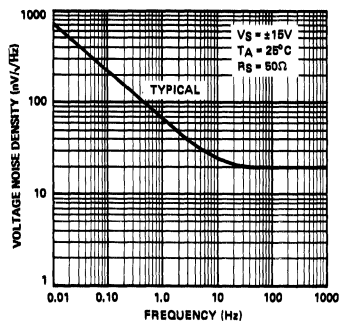
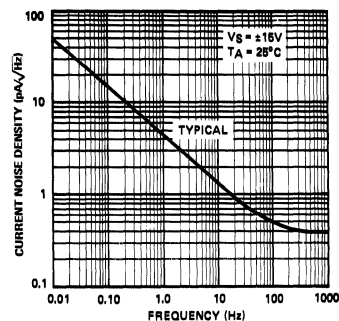
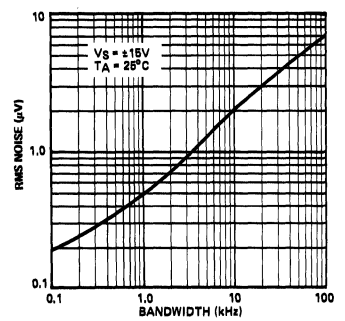
WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N LIMIT	OP-04G OP-14G LIMIT	OP-14GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	0.75	2	6	mV MAX
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	1	2	—	mV MAX
Input Offset Current	I_{OS}		5	5	200	nA MAX
Input Bias Current	I_B		50	75	500	nA MAX
Input Voltage Range	IVR		± 10	± 10	± 10	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	80	70	dB MIN
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$ $R_S \leq 100\Omega$	94	94	—	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	100	150	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	± 12 ± 12	± 12 ± 12	± 12 ± 10	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	50	25	V/mV MIN
Power Consumption (Both Amplifiers)	P_d	$V_{OUT} = 0$	170	170	180	mW MAX
Channel Separation	CS		100	100	—	dB MIN

NOTE: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

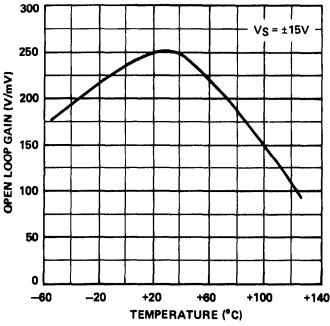
PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N TYPICAL	OP-04G OP-14G TYPICAL	OP-14GR TYPICAL	UNITS
Risetime	t_r	$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$ $C_L = 50pF$	200	200	200	ns
Overshoot	OS	$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$ $C_L = 50pF$	5	5	5	%
Slew Rate	SR	$R_L = 2k\Omega$ $C_L = 100pF$	0.25	0.25	—	V/ μs MIN

TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE

INPUT OFFSET CURRENT vs TEMPERATURE

INPUT BIAS CURRENT vs TEMPERATURE

OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE

PSRR vs FREQUENCY

CMRR vs FREQUENCY

INPUT SPOT NOISE VOLTAGE vs FREQUENCY

INPUT SPOT NOISE CURRENT vs FREQUENCY

INPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz to FREQUENCY INDICATED)


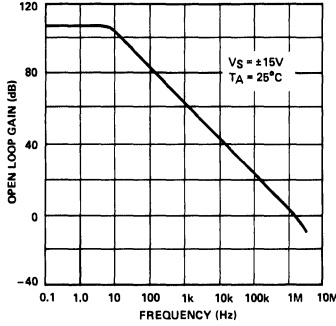


TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)

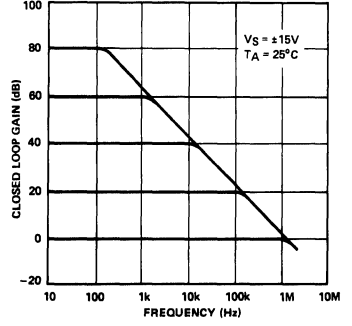
OPEN-LOOP GAIN vs TEMPERATURE



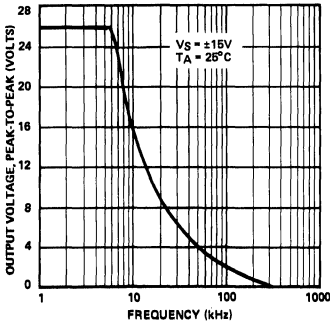
OPEN-LOOP FREQUENCY RESPONSE



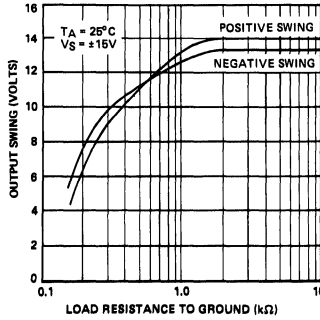
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



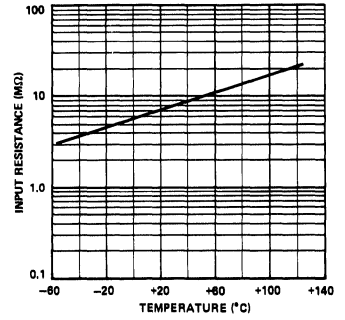
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



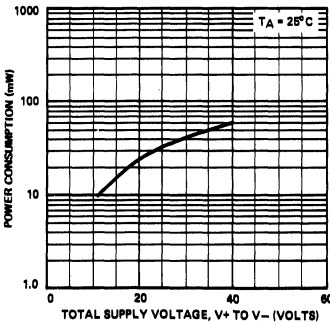
OUTPUT VOLTAGE vs LOAD RESISTANCE



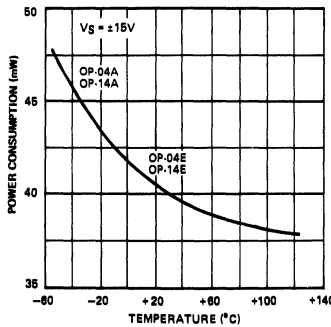
INPUT RESISTANCE vs TEMPERATURE



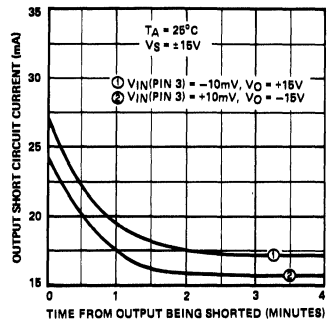
POWER CONSUMPTION vs POWER SUPPLY



POWER CONSUMPTION vs TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT vs TIME





OP-05

INSTRUMENTATION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Noise $0.6\mu\text{Vp-p Max, 0.1 to 10Hz}$
- Low Drift vs. Temperature $0.5\mu\text{V}/^\circ\text{C Max}$
- Low Drift vs. Time $0.2\mu\text{V}/\text{Month Typ}$
- Low Bias Current 2.0nA Max
- High CMRR 114dB Min
- High PSRR 100dB Min
- High Gain $300,000\text{ Min}$
- High R_{IN} Differential $30\text{M}\Omega\text{ Min}$
- High R_{IN} CM $200\text{G}\Omega\text{ Typ}$
- Internally Compensated Stable to 500pF Load
- Fits 725, 108A and 741 Sockets
- 125°C Temperature Tested Dice

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	HERMETIC				
	TO-99 8-PIN	DIP		PLASTIC DIP 8-PIN	
0.15	OP05AJ*	OP05AZ*	OP05AY*		MIL
0.5	OP05J*	OP05Z*	OP05Y*		MIL
0.5	OP05EJ	OP05EZ	OP05EY	OP-05EP	COM
1.3	OP05CJ	OP05CZ	OP05CY	OP05CP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

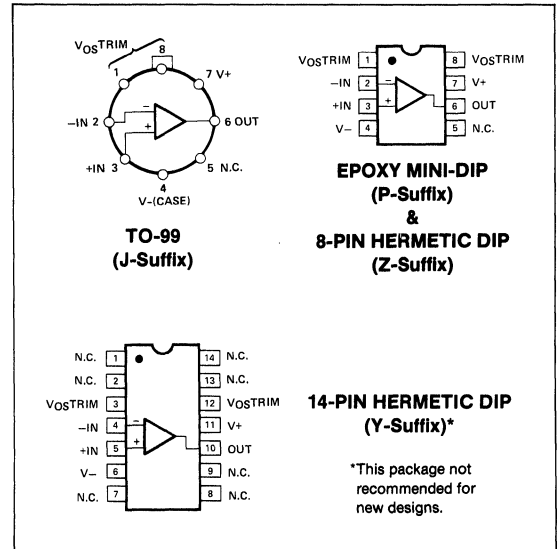
GENERAL DESCRIPTION

The OP-05 series of monolithic instrumentation operational amplifiers combine excellent performance in low-signal-level applications with the simplicity of use of a fully-protected, internally-compensated op amp. The OP-05 has low input offset

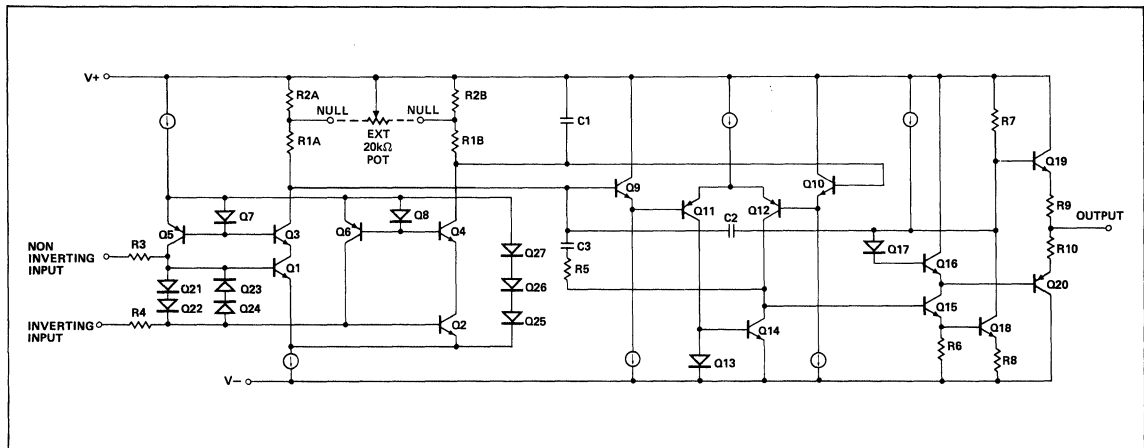
voltage and bias current combined with very high levels of gain, input impedance, CMRR, and PSRR.

The OP-05 is a direct replacement in 725, 108A, and unnull 741 sockets allowing instant system performance improvement without redesign. The OP-05 is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high-gain active filters, buffers, integrators, and sample-and-hold amplifiers. For dual-matched versions, refer to the OP-207 and OP-10 data sheets.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, Y, and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range	
OP-05A, OP-05	-55°C to +125°C
OP-05E, OP-05C	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

3. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)	—	0.2	1.0	—	0.2	1.0	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	0.7	2.0	—	1.0	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage (Note 2)	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.6	11.0	
Input Noise Current (Note 2)	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	30	80	—	20	60	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	114	126	—	114	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$	150	500	—	150	500	—	
		$V_S = \pm 3V$ (Note 3)							
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slewing Rate (Note 2)	SR	$R_L \geq 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load	—	90	120	—	90	120	mW
		$V_S = \pm 3V$, No load	—	4	6	—	4	6	
Offset Adjustment Range	$R_P = 20k\Omega$		—	4	—	—	4	—	mV

NOTES:

1. Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30

operating days are typically 2.5 μV . Refer to typical performance curve.

2. Sample tested.

3. Guaranteed by design.

5

OPERATIONAL AMPLIFIERS

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.10	0.24	—	0.3	0.7	mV
Average Input Offset Voltage									
Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.3	0.9	—	0.7	2.0	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.5	—	0.3	1.0	
Input Offset Current	I_{OS}		—	1.0	4.0	—	1.8	5.6	nA
Average Input Offset Current									
Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	$\mu A/^\circ C$
Input Bias Current	I_B		—	± 1	± 4	—	± 2	± 6	nA
Average Input Bias Current									
Drift	TCI_B	(Note 2)	—	8	25	—	13	50	$\mu A/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	110	123	—	110	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 12.0	± 12.6	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.3	1.3	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/Time$	(Notes 1, 2)	—	0.3	1.5	—	0.4	2.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	± 1.2	± 4.0	—	± 1.8	± 7.0	nA
Input Noise Voltage (Note 2)	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	—	10.3	18.0	—	10.5	20.0	nV/\sqrt{Hz}
Input Noise Current (Note 2)	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	—	0.32	0.80	—	0.35	0.90	pA/\sqrt{Hz}
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	G Ω
Input Voltage Range	IVR		± 13.5	± 14.0	—	± 13.0	± 14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	110	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	200	500	—	120	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 12.5	± 13.0	—	± 12.0	± 13.0	—	V
Slewing Rate (Note 2)	SR	$R_L \geq 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load $V_S = \pm 3V$, No load	—	90	120	—	95	150	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	4	6	—	4	8	mV

NOTE: See notes on previous page.

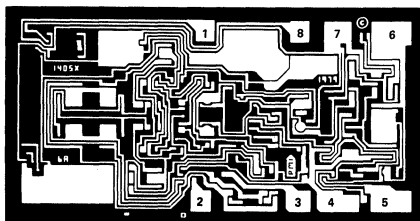
**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	1.3	4.5	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.4	1.5	
Input Offset Current	I_{OS}		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1.5	± 5.5	—	± 2.2	± 9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	107	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 11.0	± 12.6	—	V

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



**DIE SIZE 0.100 × 0.051 inch, 5100 sq. mils
(2.54 × 1.30 mm, 3.29 sq. mm)**

- 1. BALANCE
- 2. INVERTING INPUT
- 3. NONINVERTING INPUT
- 4. V-
- 5. NO CONNECTION
- 6. OUTPUT
- 7. V+
- 8. BALANCE

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-05N, OP-05G and OP-05GR devices; $T_A = 125^\circ C$ for OP-05NT and OP-05GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05NT LIMIT	OP-05N LIMIT	OP-05GT LIMIT	OP-05G LIMIT	OP-05GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.25	0.15	0.7	0.5	1.3	mV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.7	3.8	6.0	nA MAX
Input Bias Current	I_B		± 4	± 2	± 6	± 4	± 7	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 2)	—	20	—	15	8	M Ω MIN
Input Voltage Range	IVR		± 13.0	± 13.5	± 13.0	± 13.5	± 13.0	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ at $+25^\circ C$ $V_{CM} = \pm 13.0$ at $+125^\circ C$	110	114	110	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	20	30	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$	—	± 12.5	—	± 12.5	± 12.0	V MIN
		$R_L = 2k\Omega$	± 12.0	± 12.0	± 12.0	± 12.0	± 11.5	
		$R_L = 1k\Omega$	—	± 10.5	—	± 10.5	—	
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	200	120	V/mV MIN
Differential Input Voltage			± 30	± 30	± 30	± 30	± 30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTES:

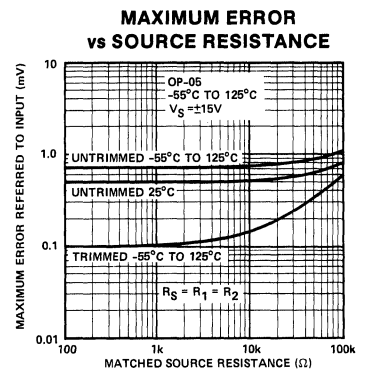
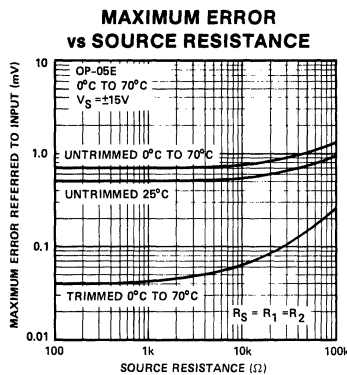
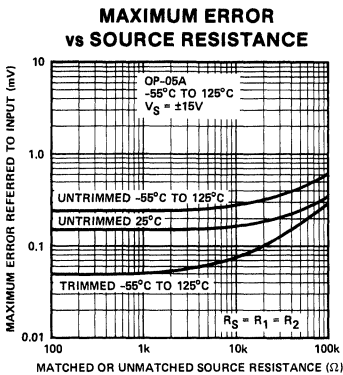
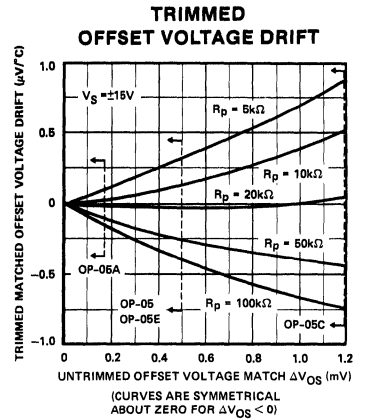
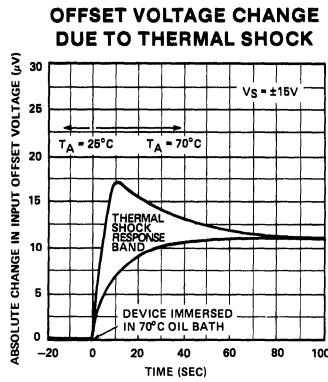
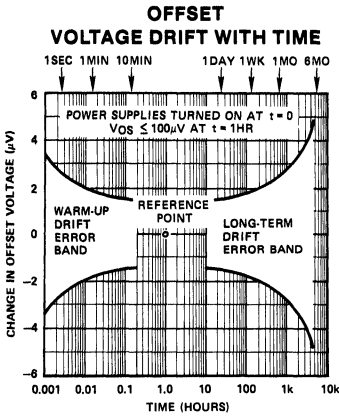
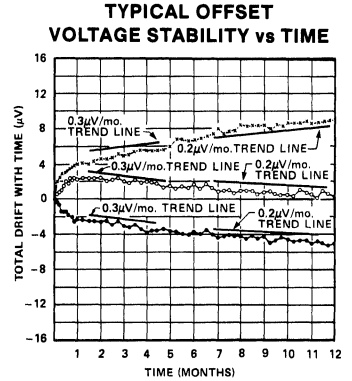
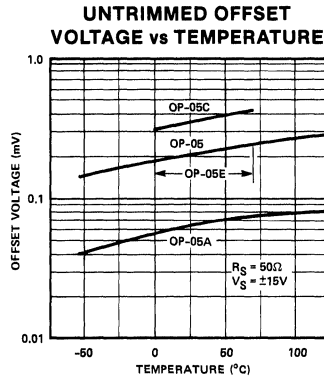
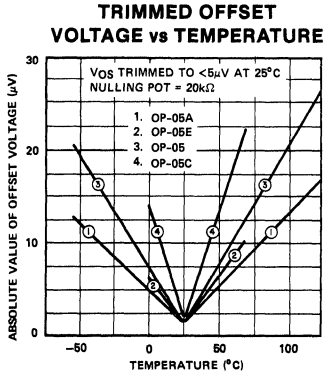
- 1. For $25^\circ C$ characteristics of NT & GT devices see N & G characteristics respectively.
- 2. Guaranteed by design.

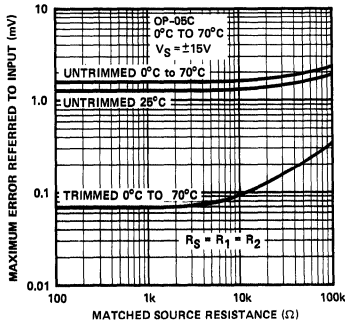
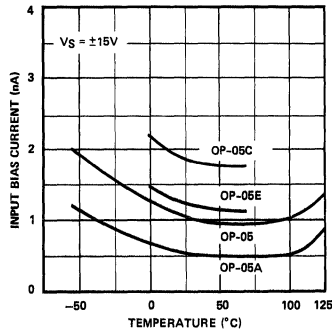
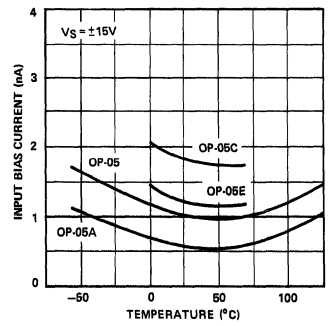
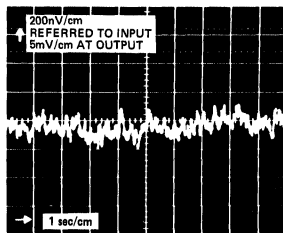
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

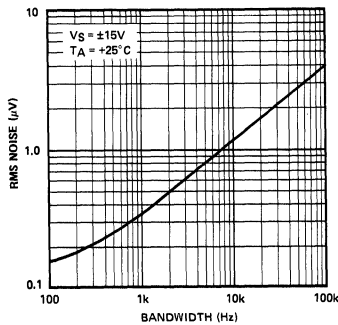
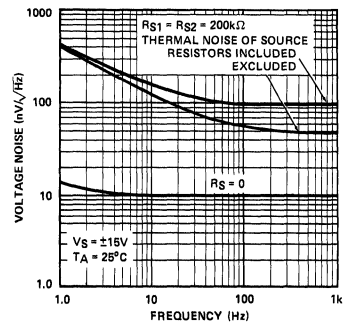
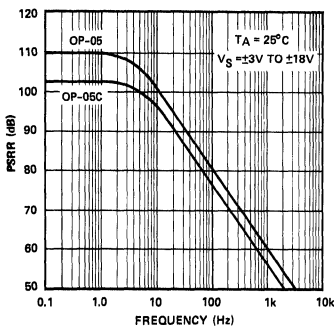
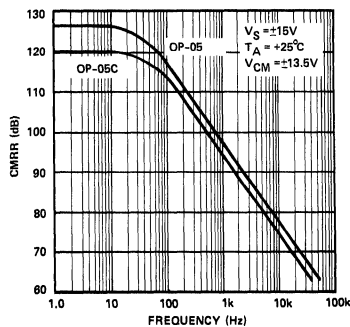
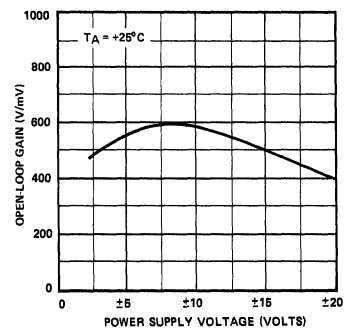
PARAMETER	SYMBOL	CONDITIONS	OP-05NT TYPICAL	OP-05N TYPICAL	OP-05GT TYPICAL	OP-05G TYPICAL	OP-05GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.2	$\mu V/^\circ C$
Nullled Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50\Omega$, $R_p = 20k\Omega$	0.2	0.2	0.3	0.3	0.4	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		5	5	8	8	12	$pA/^\circ C$
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

TYPICAL PERFORMANCE CHARACTERISTICS


 5
 OPERATIONAL AMPLIFIERS

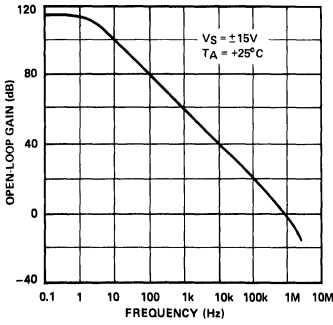
TYPICAL PERFORMANCE CHARACTERISTICS
MAXIMUM ERROR vs SOURCE RESISTANCE

INPUT BIAS CURRENT vs TEMPERATURE

INPUT OFFSET CURRENT vs TEMPERATURE

OP-05 LOW FREQUENCY NOISE


(SEE NOISE TEST CIRCUIT)

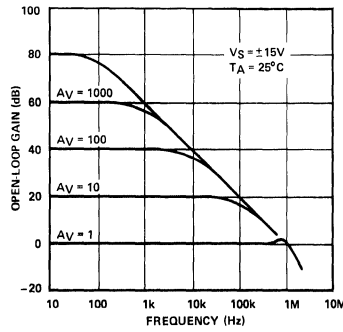
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

VOLTAGE NOISE DENSITY vs FREQUENCY

PSRR vs FREQUENCY

CMRR vs FREQUENCY

OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE


TYPICAL PERFORMANCE CHARACTERISTICS

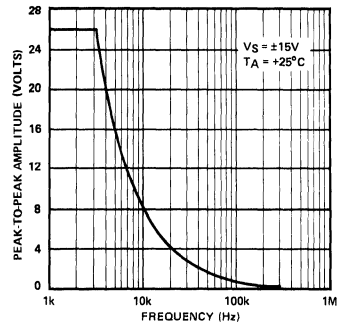
OPEN-LOOP GAIN vs FREQUENCY



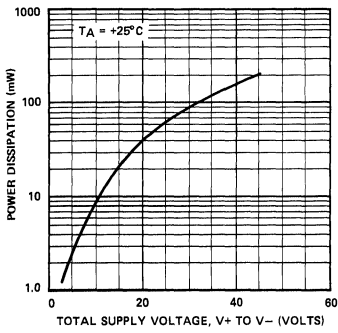
CLOSED-LOOP GAIN vs FREQUENCY



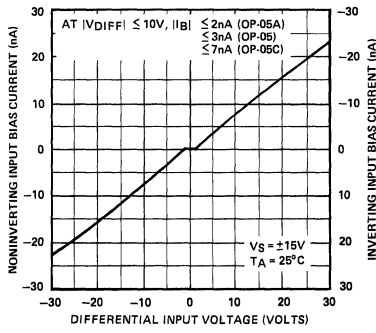
MAXIMUM OUTPUT SWING vs FREQUENCY



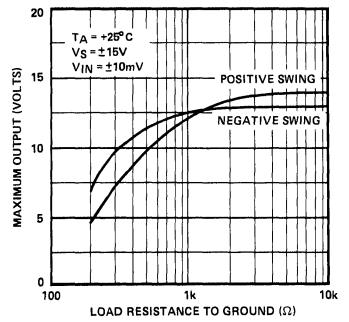
POWER CONSUMPTION vs POWER SUPPLY



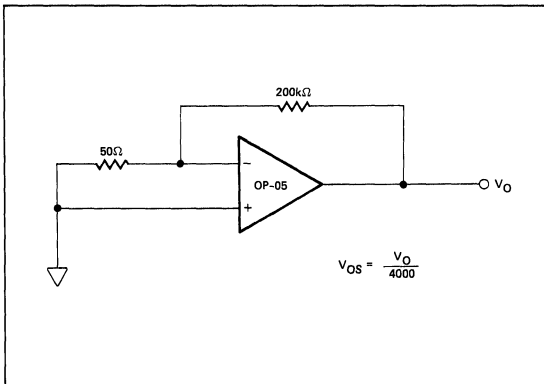
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



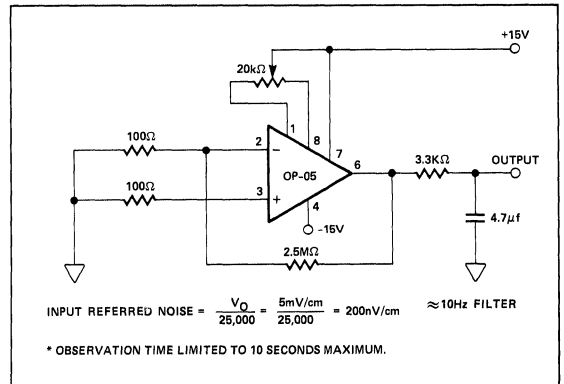
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

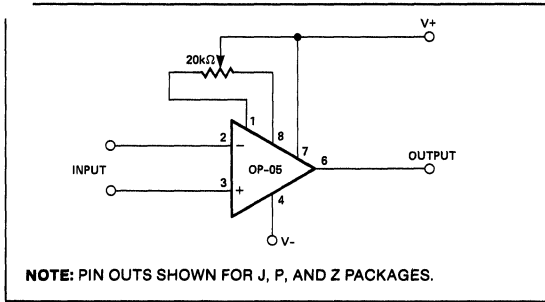
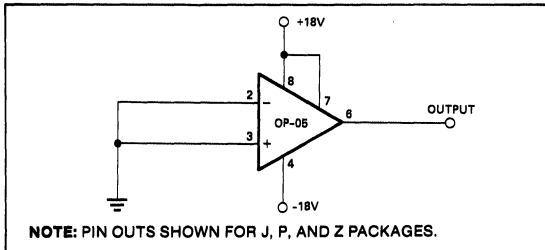


TYPICAL OFFSET VOLTAGE TEST CIRCUIT



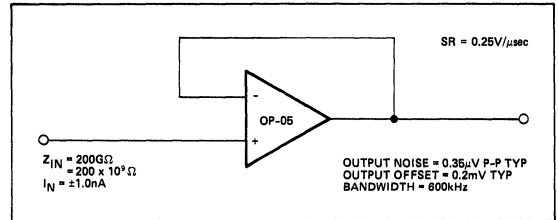
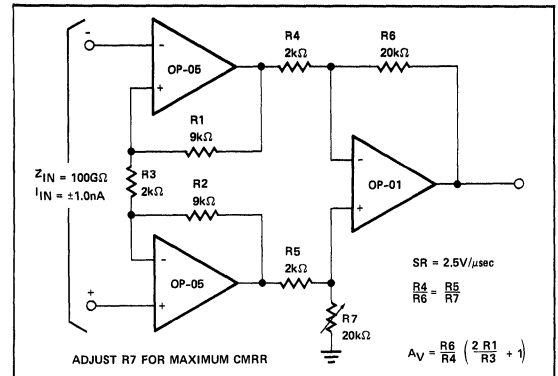
TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT*



FSET NULLING CIRCUIT

BURN-IN CIRCUIT

APPLICATIONS INFORMATION

OP-05 series devices may be fitted directly to 725 and 108/108A Series sockets with or without removal of external compensation components. Additionally, the OP-05 may be fitted to unnullified 741 series sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-05 operation. The OP-05 provides stable operation with load capacitance of up to 500pF and $\pm 10V$ swings; larger capacitances should be decoupled with a 50 Ω resistor.

Offset stability can be degraded by stray thermoelectric voltages arising from dissimilar metals at the contacts to the input terminals. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

TYPICAL APPLICATIONS
STABLE, HIGH-IMPEDANCE BUFFER

HIGH IMPEDANCE, HIGH COMMON-MODE REJECTION INSTRUMENTATION AMPLIFIER




Precision Monolithics Inc.

OP-06

HIGH-GAIN INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- Very High Voltage Gain 1,000V/mV Min
- Low Offset Voltage and Offset Current
- Low Drift vs. Temperature (TCV_{OS}) 0.8μV/°C Max
- Low Input Voltage and Current Noise
- Low Offset Voltage Drift with Time
- High Common-Mode Rejection 120dB Typ
- High Power Supply Rejection 2μV/V Max
- Wide Supply Range ±3.0V to ±22V
- MIL-STD-883 Processing Available
- Slew Rate to 100V/μs

ORDERING INFORMATION†

T _A = 25° C V _{OS} MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	
0.2	OP06EJ	OP06EZ	COM
0.2	OP06AJ*	OP06AZ*	MIL
0.5	OP06FJ	OP06FZ	COM
0.5	OP06BJ*	OP06BZ*	MIL
1.3	OP06GJ	OP06GZ	COM
1.3	OP06CJ*	OP06CZ*	MIL

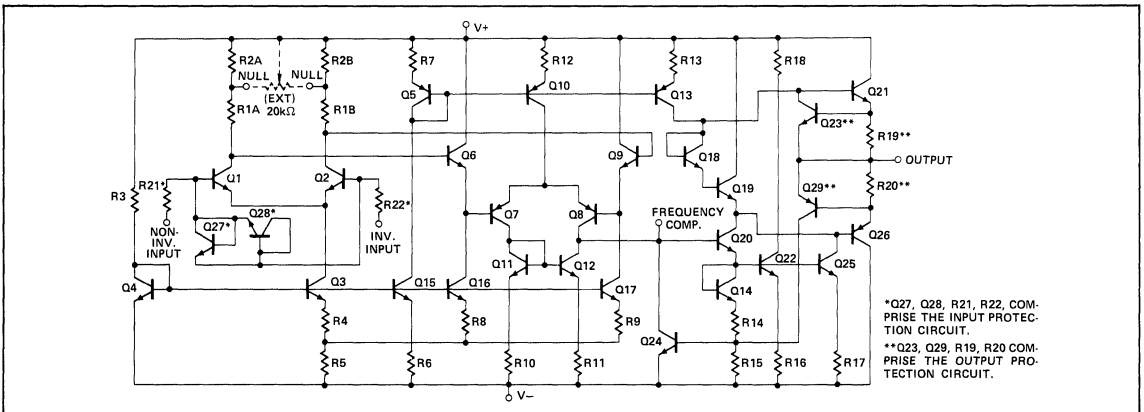
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-06 monolithic instrumentation operational amplifier is designed for accurate high-gain amplification of low level signals. High common-mode rejection reduces signal degradation when large common-mode voltages are present.

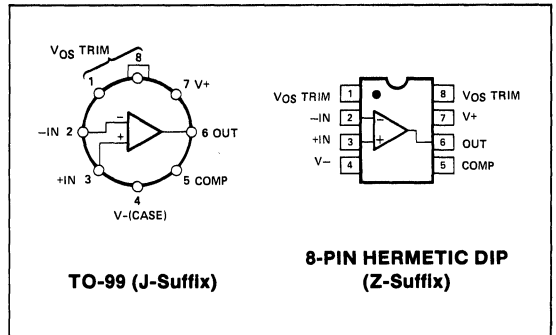
SIMPLIFIED SCHEMATIC



Superior DC input characteristics include very low offset voltage and current, extremely high open-loop gain, low 1/f and wideband noise, and low "popcorn" noise. Low offset voltage drift is improved by a nulling technique that optimizes TCV_{OS} performance when V_{OS} is nulled to zero. Very high common-mode and power supply rejection enable accurate performance in noisy environments.

Flexible external compensation provides wide-bandwidth and high slew rate operation in high closed-loop gain applications. Excellent long-term stability, and compatibility with MIL-STD-883 processing, make the OP-06 an excellent choice for high-reliability applications. For example, process control and aerospace applications; including strain gauge and thermocouple amplifiers, low-noise audio amplifiers, and instrumentation amplifiers. The OP-06 is a direct replacement for all 725 types providing superior DC and noise performance plus the unique feature of **complete input differential voltage and output short-circuit protection.**

PIN CONNECTIONS



5
OPERATIONAL AMPLIFIERS

**ABSOLUTE MAXIMUM RATINGS** (Note 3)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-06A, OP-06B, OP-06C	-55°C to +125°C
OP-06E, OP-06F, OP-06G	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

3. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06A/E			OP-06B/F			OP-06C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	0.06	0.2	—	0.2	0.5	—	0.4	1.3	mV
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.75	5.0	—	2	13	nA
Input Bias Current	I_B		—	30	70	—	30	80	—	40	110	nA
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 1)	—	9.0	15.0	—	9.0	15.0	—	9.0	15.0	nV/ $\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 1)	—	8.0	9.0	—	8.0	9.0	—	8.0	9.0	
		$f_O = 1000\text{Hz}$ (Note 1)	—	7.0	7.5	—	7.0	7.5	—	7.0	7.5	
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Note 1)	—	0.5	1.2	—	0.5	1.2	—	0.6	1.4	pA/ $\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 1)	—	0.25	0.6	—	0.25	0.6	—	0.3	0.7	
		$f_O = 1000\text{Hz}$ (Note 1)	—	0.15	0.25	—	0.15	0.25	—	0.2	0.3	
Input Resistance	R_{IN}	(Note 3)	0.8	1.8	—	0.7	1.8	—	0.5	1.5	—	M Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1,000	3,000	—	1,000	3,000	—	500	3,000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±11.0	±12.5	—	±11.0	±12.5	—	—	±12.0	—	
Input Voltage Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \leq 20k\Omega$	114	120	—	114	120	—	110	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	—	0.5	2.0	—	1.0	5.0	—	2.0	10	$\mu V/V$
Power Consumption	P_d		—	90	120	—	90	120	—	110	150	mW
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 500\Omega$, (Note 3) $V_O = \pm 0.5V$ $V_S = \pm 3V$	100	600	—	100	600	—	60	600	—	V/mV
Power Consumption	P_d	$V_S = \pm 3V$	—	4	6	—	4	6	—	4	8	mW

NOTES:

- Sample tested.
- Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Both sides of the contacts should be kept at approximately the same temperature. All temperature gradients should be minimized.
- Guaranteed by design.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06A			OP-06B			OP-06C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	0.08	0.28	—	0.3	0.7	—	0.5	1.6	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1, 2)	—	0.3	0.8	—	0.7	2.0	—	1.4	4.5	$\mu V/^\circ C$
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 2, 3) $R_P = 20k\Omega$	—	0.2	0.6	—	0.28	1.0	—	0.5	1.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}	T_A MAX T_A MIN	—	0.25 0.8	1.0 4.0	—	0.6 2.0	4.0 18.0	—	2.0 3.0	15 25	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	3	20	—	8	90	—	14	150	$\mu A/^\circ C$
Input Bias Current	I_B	T_A MAX T_A MIN	—	22 40	60 120	—	25 45	70 180	—	35 45	110 180	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \leq 20k\Omega$	109	112	—	109	112	—	95	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	—	1	5	—	2	8	—	3	15	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L \geq 2k\Omega$ T_A MAX T_A MIN	1,000 700	3,500 2,000	—	1,000 700	3,500 1,800	—	400 300	3,200 1,700	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 12.0	± 12.6	—	± 11.0	± 12.6	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06E			OP-06F			OP-06G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	0.08	0.28	—	0.25	0.6	—	0.5	1.6	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1, 2)	—	0.3	0.8	—	0.7	2.0	—	1.4	4.5	$\mu V/^\circ C$
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 2, 3) $R_P = 20k\Omega$	—	0.2	0.6	—	0.28	1.0	—	0.5	1.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}	T_A MAX T_A MIN	—	0.25 0.8	1.0 4.0	—	0.65 2.0	5.0 18.0	—	2.0 3.0	15 25	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	3	20	—	8	90	—	14	150	$\mu A/^\circ C$
Input Bias Current	I_B	T_A MAX T_A MIN	—	22 40	60 120	—	30 45	80 180	—	35 45	110 180	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \leq 20k\Omega$	109	112	—	109	112	—	95	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	—	1.0	5.0	—	1.5	7.0	—	3.0	15	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L \geq 2k\Omega$ T_A MAX T_A MIN	1,000 800	3,500 2,000	—	1,000 800	3,500 1,800	—	400 300	3,200 1,700	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 12.0	± 12.6	—	± 11.0	± 12.6	—	V

NOTES:

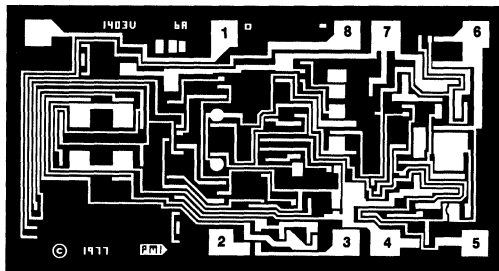
- Sample tested.
- Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Both sides of the

contacts should be kept at approximately the same temperature. All temperature gradients should be minimized.

- Guaranteed by input bias current.



DICE CHARACTERISTICS



DIE SIZE 0.094 × 0.050 inch, 4700sq. mils
(2.39 × 1.27 mm, 3.03 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V⁻
5. COMPENSATION
6. OUTPUT
7. V⁺
8. NULL

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-06N, OP-06G and OP-06GR devices; $T_A = 125^\circ C$ for OP-06NT and OP-06GT devices, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	OP-06NT LIMIT	OP-06N LIMIT	OP-06GT LIMIT	OP-06G LIMIT	OP-06GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	0.3	0.2	0.7	0.5	1.3	mV MAX
Input Offset Current	I_{OS}		1	2	4	5	13	nA MAX
Input Bias Current	I_B		60	70	70	80	110	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 1)	—	0.8	—	0.7	0.5	M Ω MIN
Input Voltage Range	IVR		± 13.0	± 13.5	± 13.0	± 13.5	± 13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5$ $R_S \leq 20k\Omega$	108	114	108	114	110	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	6	2	8	5	10	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	—	± 12.5	—	± 12.5	± 12.0	V MIN
		$R_L \geq 2k\Omega$	± 12.0	± 12.0	± 12.0	± 12.0	± 11.5	
		$R_L \geq 1k\Omega$	—	± 11.0	—	± 11.0	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	1000	1000	800	1000	500	V/mV MIN
Differential Input Voltage			± 30	± 30	± 30	± 30	± 30	V MAX
Power Consumption ($V_{OUT} = 0V$)	P_d		—	120	—	120	150	mW MAX

NOTE:

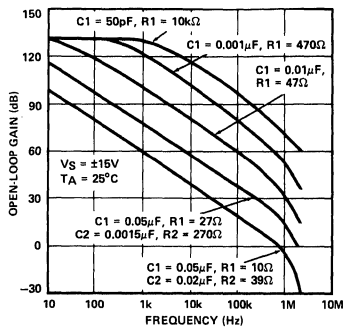
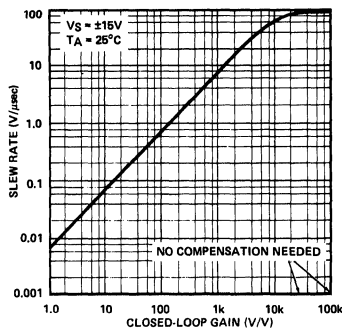
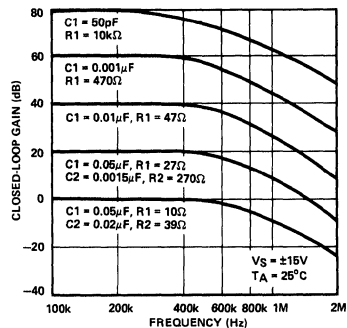
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

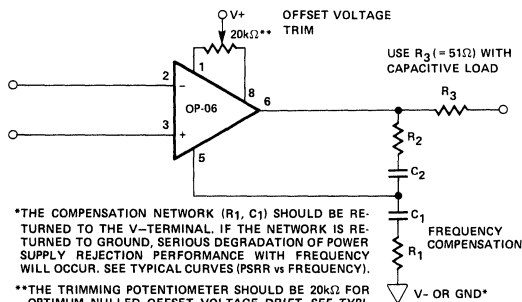
PARAMETER	SYMBOL	CONDITIONS	OP-06NT TYPICAL	OP-06N TYPICAL	OP-06GT TYPICAL	OP-06G TYPICAL	OP-06GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.4	$\mu V/^\circ C$
Nullled Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50k\Omega$ $R_P = 20k\Omega$	0.2	0.2	0.28	0.28	0.5	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		3	3	8	8	14	pA/°C

NOTES:

1. Guaranteed by input bias current.
2. For $+25^\circ C$ specifications of OP-06NT and OP-06GT, see OP-06N and OP-06G respectively.

TYPICAL PERFORMANCE CHARACTERISTICS
OPEN-LOOP RESPONSE FOR VALUES OF COMPENSATION

SLEW RATE USING RECOMMENDED COMPENSATION NETWORKS

CLOSED-LOOP FREQUENCY RESPONSE FOR VALUES OF COMPENSATION

FREQUENCY COMPENSATION
COMPENSATION VALUES

A_{vcl}	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10000	10k	50pF	—	—
1000	470	0.001	—	—
100	47	0.01	—	—
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

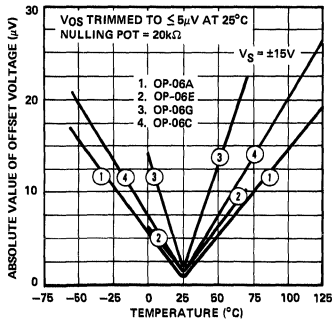
COMPENSATION CIRCUIT (J or Z PACKAGE)


*THE COMPENSATION NETWORK (R_1 , C_1) SHOULD BE RETURNED TO THE V-TERMINAL. IF THE NETWORK IS RETURNED TO GROUND, SERIOUS DEGRADATION OF POWER SUPPLY REJECTION PERFORMANCE WITH FREQUENCY WILL OCCUR. SEE TYPICAL CURVES (PSRR vs FREQUENCY).

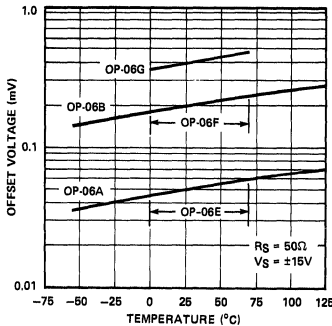
**THE TRIMMING POTENTIOMETER SHOULD BE 20k Ω FOR OPTIMUM NULLED OFFSET VOLTAGE DRIFT. SEE TYPICAL CURVES (TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER).

TYPICAL PERFORMANCE CHARACTERISTICS

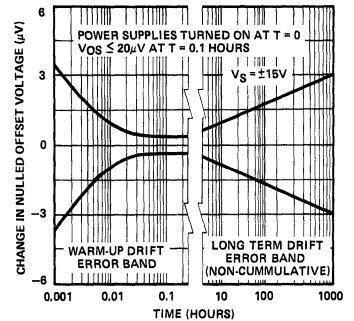
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



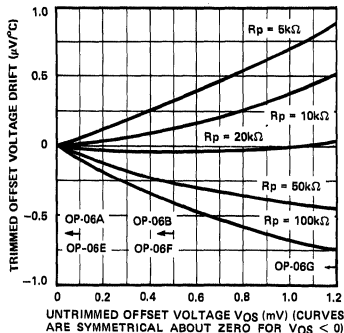
OFFSET VOLTAGE vs TEMPERATURE



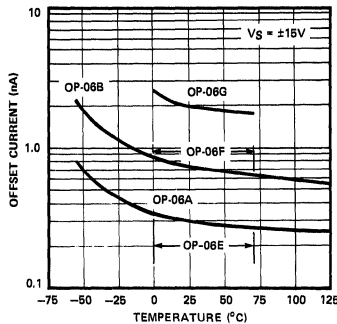
OFFSET VOLTAGE DRIFT WITH TIME



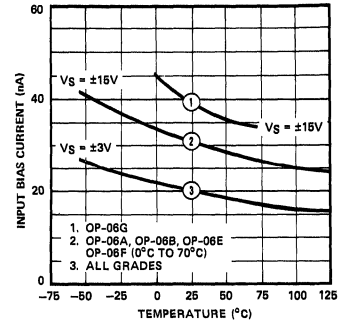
TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER (Rp) SIZE AND VOS



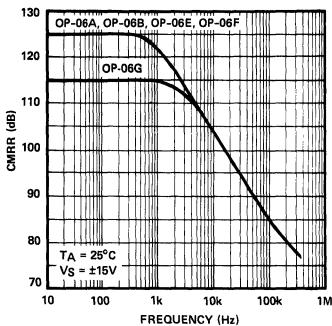
OFFSET CURRENT vs TEMPERATURE



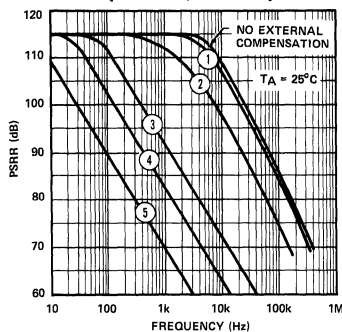
INPUT BIAS CURRENT vs TEMPERATURE



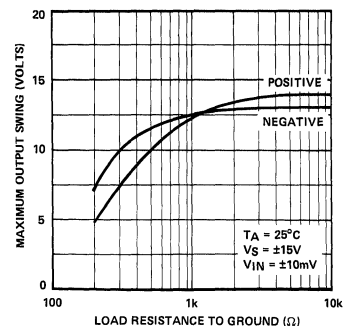
CMRR vs FREQUENCY



PSRR vs FREQUENCY (OP-06B, OP-06E)

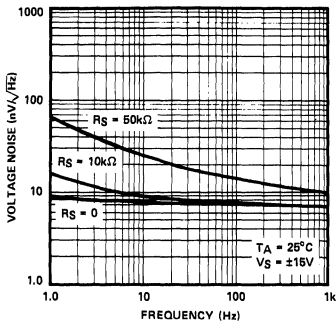
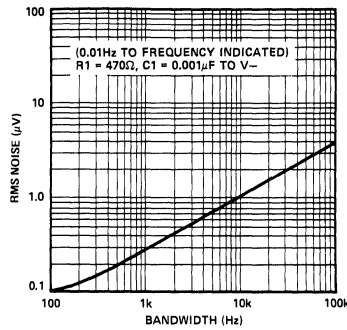
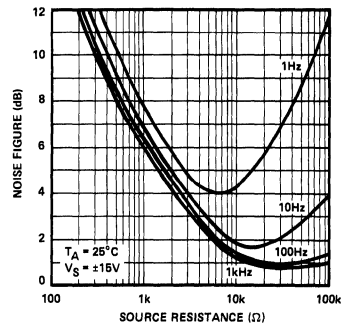
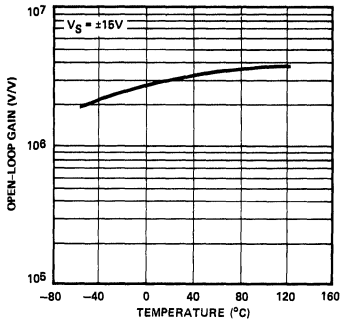
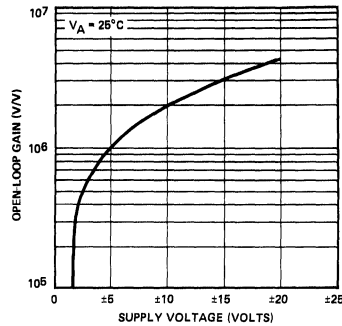
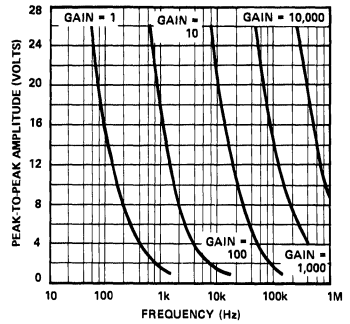
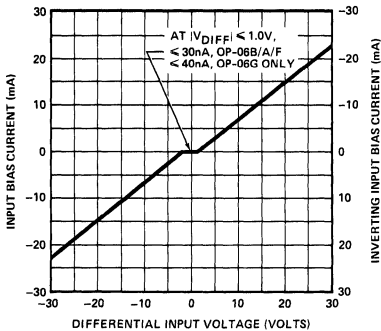
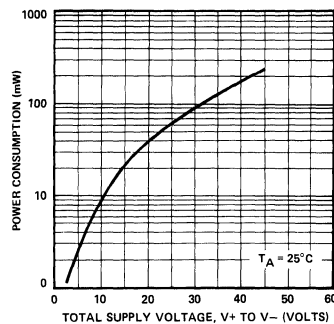
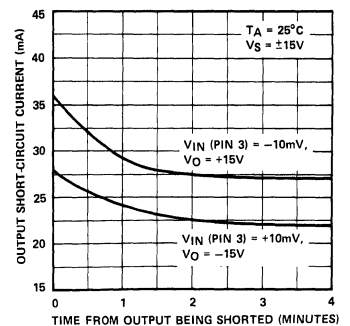


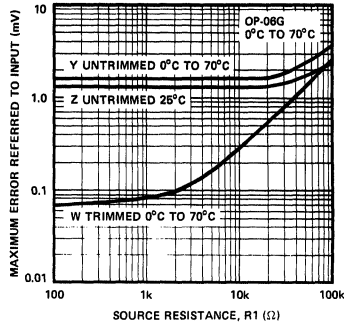
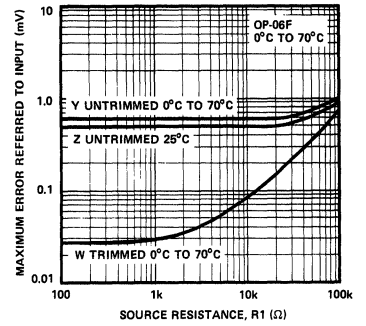
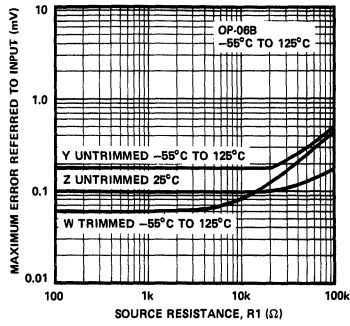
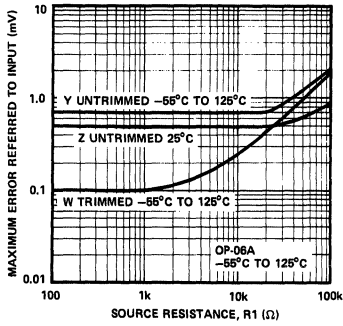
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



1. C1 = 0.001µF, R1 = 470Ω FROM PIN 5 TO V-
2. C1 = 0.1µF, R1 = 5Ω TO V-
3. C1 = 0.001µF, R1 = 470Ω FROM PIN 5 TO GND
4. C1 = 0.05µF, R1 = 10Ω, C2 = 0.02µF, R2 = 39Ω TO V-
5. C1 = 0.05µF, R1 = 10Ω, C2 = 0.02µF, R2 = 39Ω TO GND

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE DENSITY vs FREQUENCY

INPUT WIDEBAND NOISE vs BANDWIDTH

NOISE FIGURE vs SOURCE RESISTANCE

OPEN-LOOP GAIN vs TEMPERATURE

OPEN-LOOP GAIN vs SUPPLY VOLTAGE

MAXIMUM OUTPUT SWING vs FREQUENCY

INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

POWER CONSUMPTION vs SUPPLY VOLTAGE

OUTPUT SHORT-CIRCUIT CURRENT


GUARANTEED PERFORMANCE CHARACTERISTICS


These graphs depict maximum error referred to the input as a function of source resistance (R_1). Curves W are shown with V_{OS} trimmed at $+25^\circ\text{C}$ and include errors due to V_{OS} and I_{OS} over the indicated temperature range. Curves Y and Z plot maximum errors with V_{OS} not trimmed.



OP-07

ULTRA-LOW OFFSET VOLTAGE OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low V_{OS} $25\mu V$ Max
- Low V_{OS} Drift $0.6\mu V/^{\circ}C$ Max
- Ultra-Stable vs Time $1.0\mu V$ /Month Max
- Low Noise $0.6\mu V_{p-p}$ Max
- Wide Input Voltage Range $\pm 14V$
- Wide Supply Voltage Range $\pm 3V$ to $\pm 18V$
- Fits 725, 108A/308A, 741, AD510 Sockets
- $125^{\circ}C$ Temperature-Tested Dice

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ ΔV_{OS} MAX (μV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	LCC	
25	OP07AJ*	OP07AZ*			MIL
75	OP07EJ	OP07EZ	OP07EP		COM
75	OP07J*	OP07Z*		OP07RC/883	MIL
150	OP07CJ	OP07CZ	OP07CP		COM
150	OP07DJ	OP07DP			COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-07 has very low input offset voltage ($25\mu V$ max for OP-07A) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current ($\pm 2nA$ for OP-07A) and high open-loop gain ($300V/mV$ for OP-07A). The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain instrumentation applications.

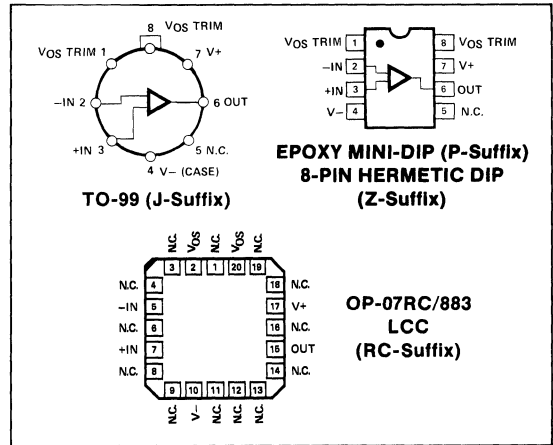
The wide input voltage range of $\pm 13V$ minimum combined with high CMRR of 110dB (OP-07A) and high input impedance provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP-07, even at high gain, combined with the freedom from external nulling have made the OP-07 a new industry standard for instrumentation and military applications.

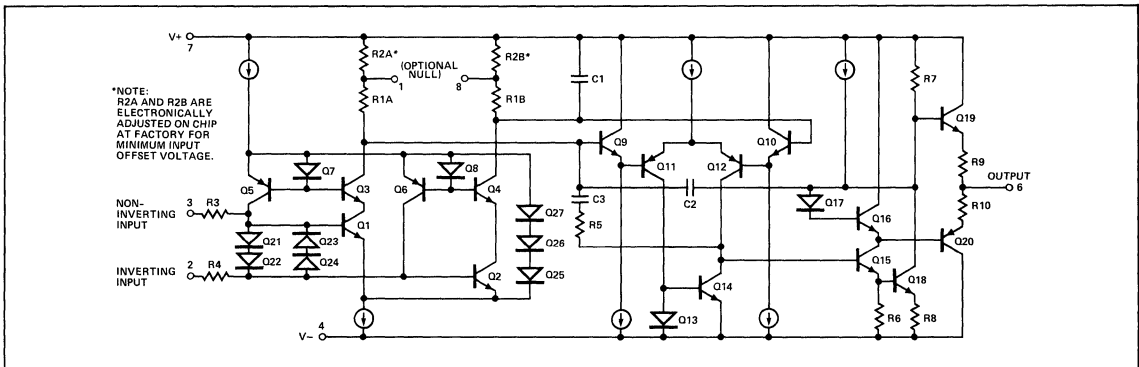
The OP-07 is available in five standard performance grades. The OP-07A and the OP-07 are specified for operation over the full military range of $-55^{\circ}C$ to $+125^{\circ}C$; the OP-07 E, C, and D are specified for operation over the $0^{\circ}C$ to $+70^{\circ}C$ range.

The OP-07 is available in hermetically-sealed TO-99 metal can or ceramic 8-pin Mini-DIP, and in epoxy 8-pin Mini-DIP. It is a direct replacement for 725, 108A, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer. The OP-207, a dual OP-07, is available for applications requiring close matching of two OP-07 amplifiers. For improved specifications, see the OP-77.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, RC and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range	
OP-07A, OP-07, OP-07RC	-55°C to +125°C
OP-07E, OP-07C, OP-07D	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T _J)	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
	TO-99 (J)	80°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
LCC (RC)	72°C	7.8mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	(Note 1)	—	10	25	—	30	75	μV
Long-Term Input Offset Voltage Stability	ΔV _{OS} /Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I _{OS}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I _B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e _{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV _{p-p}
Input Noise Voltage Density	e _n	f _O = 10Hz (Note 3)	—	10.3	18.0	—	10.3	18.0	nV/√Hz
		f _O = 100Hz (Note 3)	—	10.0	13.0	—	10.0	13.0	
		f _O = 1000Hz (Note 3)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i _{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA _{p-p}
Input Noise Current Density	i _n	f _O = 10Hz (Note 3)	—	0.32	0.80	—	0.32	0.80	pA/√Hz
		f _O = 100Hz (Note 3)	—	0.14	0.23	—	0.14	0.23	
		f _O = 1000Hz (Note 3)	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R _{IN}	(Note 4)	30	80	—	20	60	—	MΩ
Input Resistance — Common-Mode	R _{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±13V	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±3V to ±18V	—	4	10	—	4	10	μV/V
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2kΩ, V _O = ±10V	300	500	—	200	500	—	V/mV
		R _L ≥ 500Ω, V _O = ±0.5V, V _S = ±3V (Note 4)	150	400	—	150	400	—	
Output Voltage Swing	V _O	R _L ≥ 10kΩ	±12.5	±13.0	—	±12.5	±13.0	—	V
		R _L ≥ 2kΩ	±12.0	±12.8	—	±12.0	±12.8	—	
		R _L ≥ 1kΩ	±10.5	±12.0	—	±10.5	±12.0	—	
Slew Rate	SR	R _L ≥ 2kΩ (Note 3)	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	A _{VCL} = +1 (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R _O	V _O = 0, I _O = 0	—	60	—	—	60	—	Ω
Power Consumption	P _d	V _S = ±15V, No Load	—	75	120	—	75	120	mW
		V _S = ±3V, No Load	—	4	6	—	4	6	
Offset Adjustment Range	R _P	20kΩ	—	±4	—	—	±4	—	mV

NOTES:

- OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
- Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation.

Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.

- Sample tested.
- Guaranteed by design.



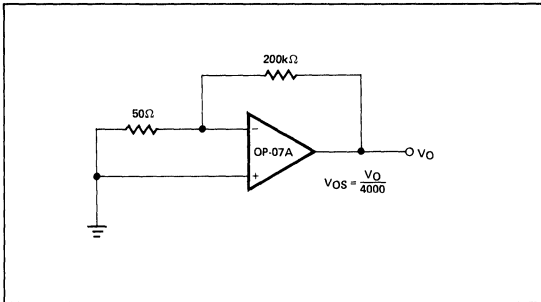
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.3	1.3	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.8	4	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1	± 4	—	± 2	± 6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13	± 13.5	—	± 13	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 12.6	—	± 12	± 12.6	—	V

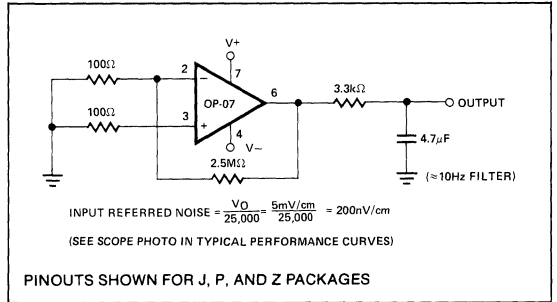
NOTES:

1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

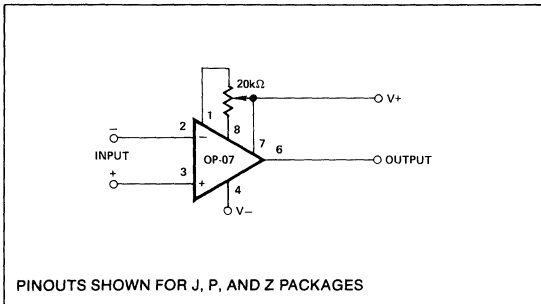
TYPICAL OFFSET VOLTAGE TEST CIRCUIT



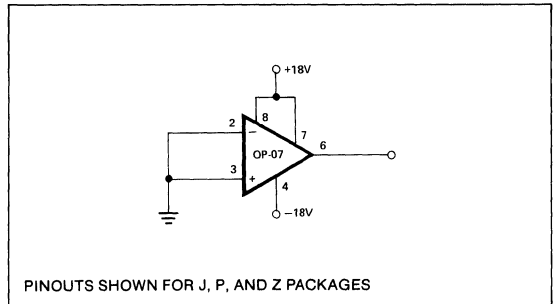
TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



5 OPERATIONAL AMPLIFIERS

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	30	75	—	60	150	—	60	150	μV
Long-Term V_{OS} Stability	$V_{OS}/Time$	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	I_B		—	± 1.2	± 4.0	—	± 1.8	± 7.0	—	± 2.0	± 12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	nV/\sqrt{Hz}
		$f_O = 100Hz$ (Note 3)	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		$f_O = 1000Hz$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	pA/\sqrt{Hz}
		$f_O = 100Hz$ (Note 3)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_O = 1000Hz$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	15	50	—	8	33	—	7	31	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	—	120	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	120	400	—	V/mV
		$R_L \geq 500\Omega$	150	400	—	100	400	—	—	400	—	
		$V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 4)										
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.0	± 13.0	—	± 12.0	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 11.5	± 12.8	—	± 11.5	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.5	± 12.0	—	—	± 12.0	—	—	± 12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 5)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0, I_O = 0$	—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	75	120	—	80	150	—	80	150	mW
		$V_S = \pm 3V$, No Load	—	4	6	—	4	8	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	± 4	—	—	± 4	—	—	± 4	—	mV

NOTES:

- Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
- Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves. Parameter is sample tested.
- Sample tested.
- Guaranteed by design.
- Guaranteed but not tested.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

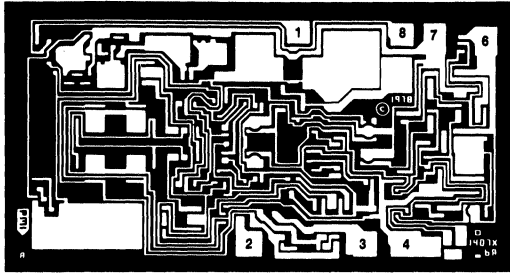
PARAMETER	SYMBOL	CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	45	130	—	85	250	—	85	250	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 3)	—	0.3	1.3	—	0.5	1.8	—	0.7	2.5	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.3	—	0.4	1.6	—	0.7	2.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	—	12	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1.5	± 5.5	—	± 2.2	± 9.0	—	± 3.0	± 14	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	—	18	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	180	450	—	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 12.6	—	± 11	± 12.6	—	± 11	± 12.6	—	V

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

5

OPERATIONAL AMPLIFIERS

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)


DIE SIZE 0.100 × 0.053 inch, 5300 sq. mils
(2.54 × 1.35 mm, 3.42 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V⁻
6. OUTPUT
7. V⁺
8. BALANCE

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-07N, OP-07G and OP-07GR devices; $T_A = 125^\circ C$ for OP-07NT and OP-07GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT LIMIT	OP-07N LIMIT	OP-07GT LIMIT	OP-07G LIMIT	OP-07GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		140	40	210	80	150	μV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.6	2.8	6.0	nA MAX
Input Bias Current	I_B		± 4	± 2	± 6	± 3	± 7	nA MAX
Input Resistance Differential-Mode	R_{IN}	(Note 2)	—	20	—	20	8	M Ω MIN
Input Voltage Range	IVR		± 13	± 13	± 13	± 13	± 13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	110	100	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	10	30	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$	—	± 12.5	—	± 12.0	± 12.0	V MIN
		$R_L = 2k\Omega$	± 12.0	± 12.0	± 12.0	± 11.5	± 11.5	
		$R_L = 1k\Omega$	—	± 10.5	—	± 10.5	—	
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	120	120	V/mV MIN
Differential Input Voltage			± 30	± 30	± 30	± 30	± 30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTES:

1. For 25° C characteristics of OP-07NT and OP-07GT, see OP-07N and OP-07G characteristics, respectively.
2. Guaranteed by design.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

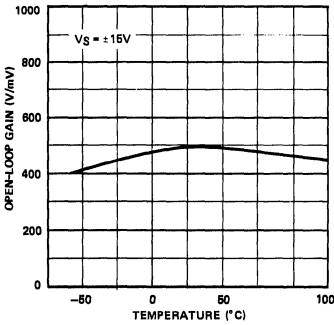
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT TYPICAL	OP-07N TYPICAL	OP-07GT TYPICAL	OP-07G TYPICAL	OP-07GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	0.2	0.2	0.3	0.3	0.7	$\mu V/^\circ C$
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, $R_P = 20k\Omega$	0.2	0.2	0.3	0.3	0.7	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		5	5	8	8	12	pA/° C
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

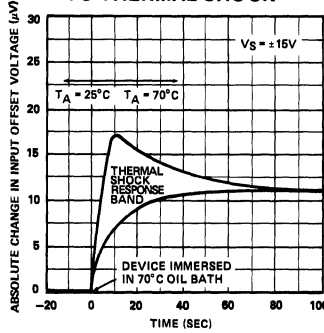


TYPICAL PERFORMANCE CHARACTERISTICS

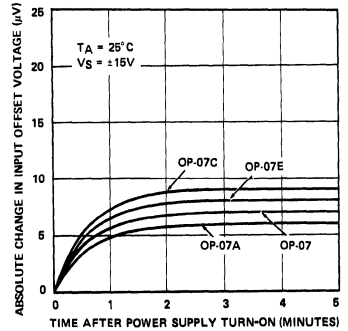
OPEN-LOOP GAIN vs TEMPERATURE



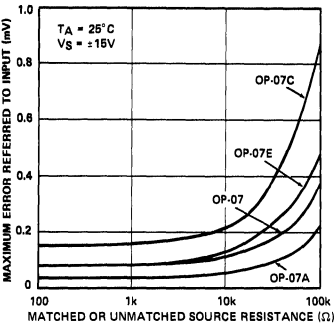
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



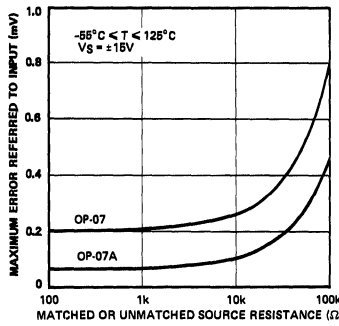
WARM-UP DRIFT



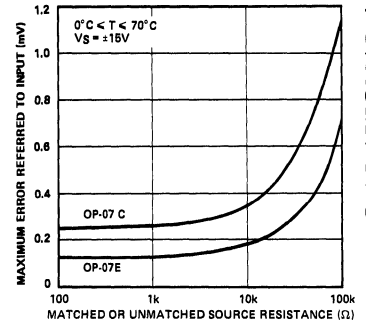
MAXIMUM ERROR vs SOURCE RESISTANCE



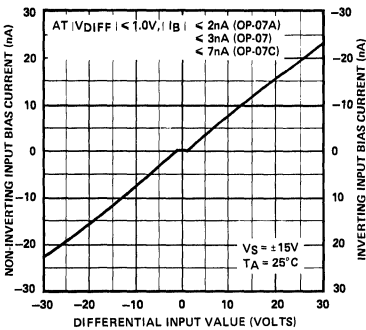
MAXIMUM ERROR vs SOURCE RESISTANCE



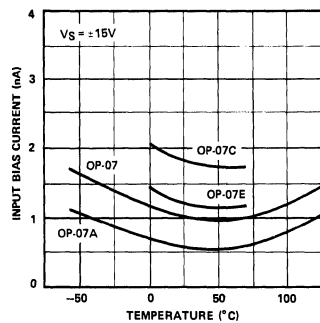
MAXIMUM ERROR vs SOURCE RESISTANCE



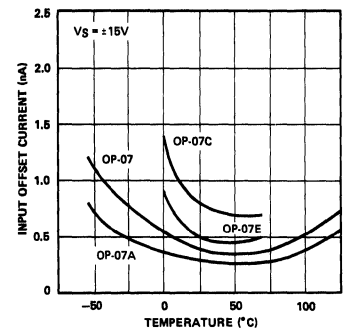
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

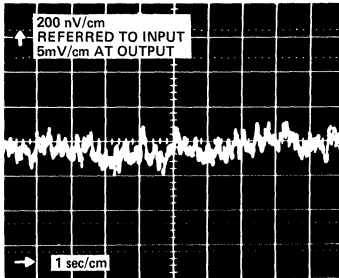


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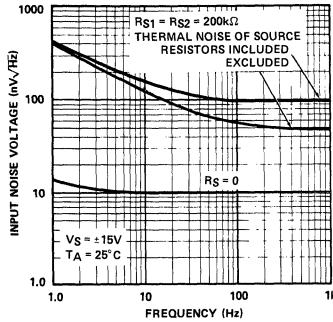
OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS

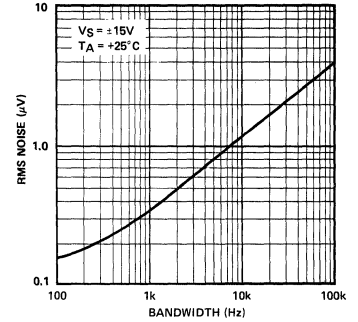
OP-07 LOW FREQUENCY NOISE



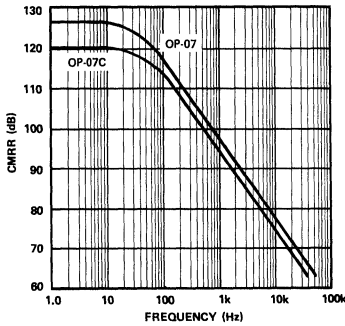
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



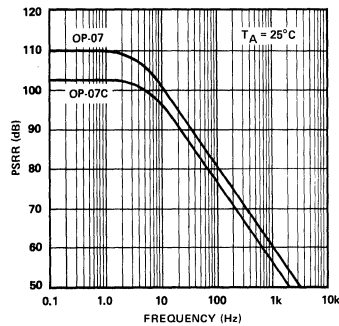
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



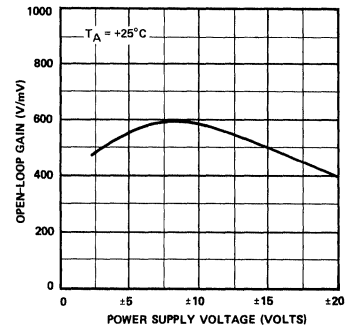
CMRR vs FREQUENCY



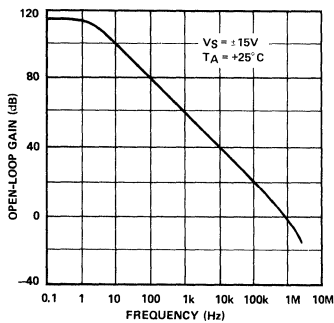
PSRR vs FREQUENCY



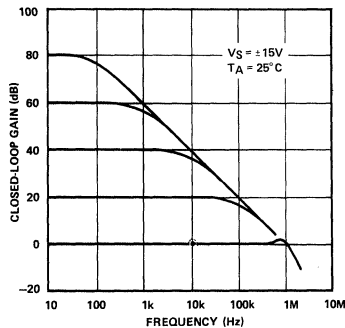
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



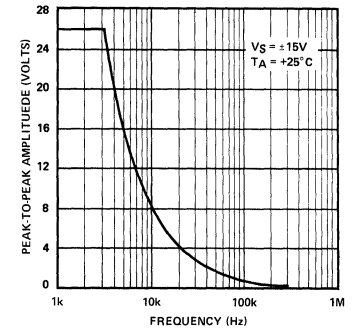
OPEN-LOOP FREQUENCY RESPONSE

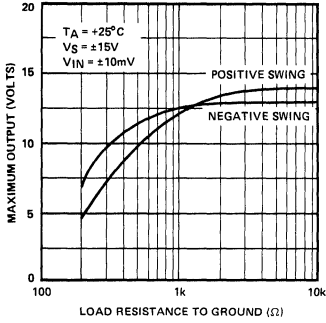
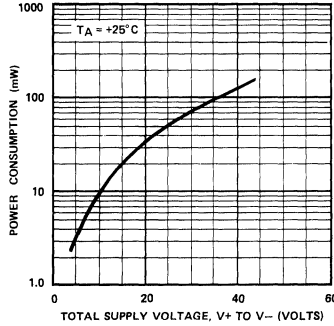
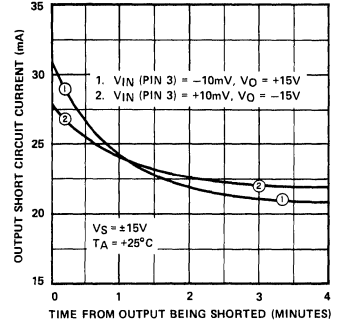
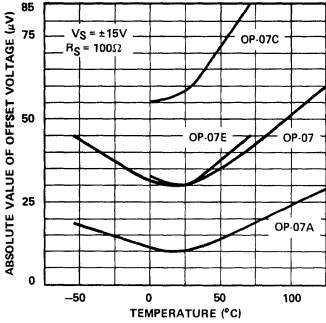
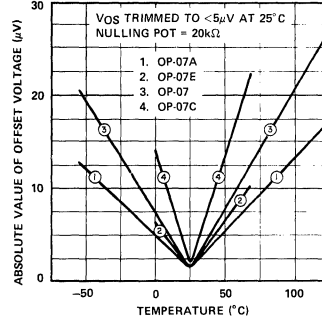
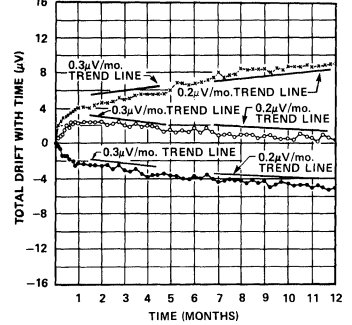
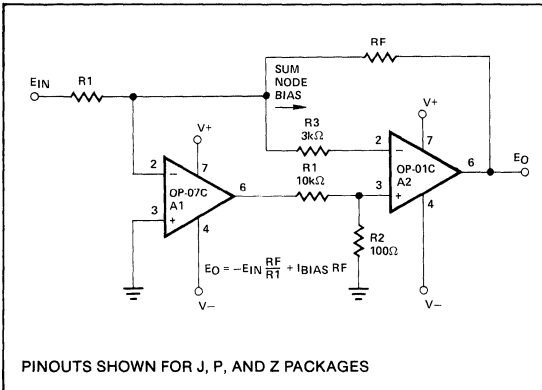
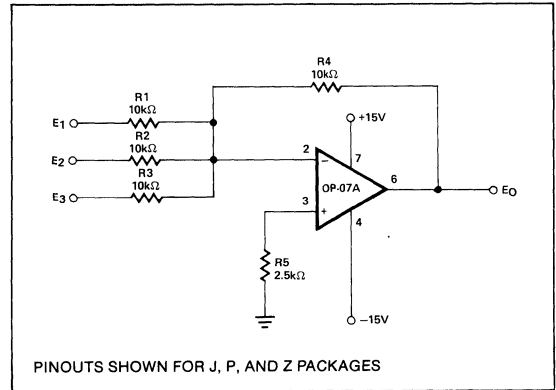


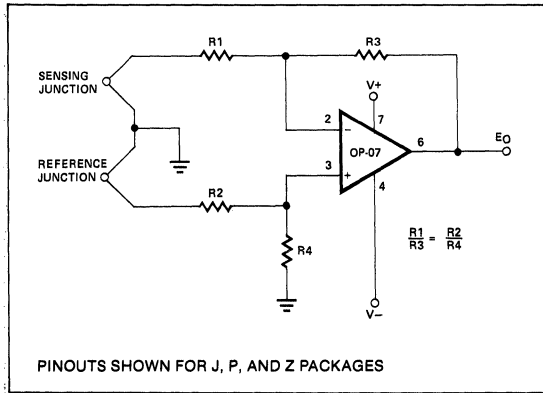
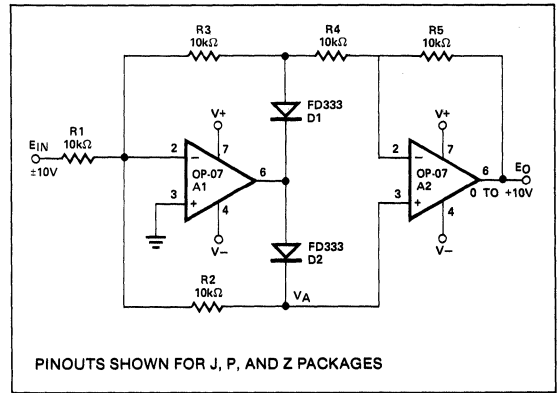
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



MAXIMUM OUTPUT SWING vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

POWER CONSUMPTION vs POWER SUPPLY

OUTPUT SHORT-CIRCUIT CURRENT vs TIME

UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE

TRIMMED OFFSET VOLTAGE vs TEMPERATURE

OFFSET VOLTAGE STABILITY vs TIME

TYPICAL APPLICATIONS
HIGH SPEED, LOW V_{OS} , COMPOSITE AMPLIFIER

ADJUSTMENT-FREE PRECISION SUMMING AMPLIFIER


TYPICAL APPLICATIONS
HIGH-STABILITY THERMOCOUPLE AMPLIFIER

PRECISION ABSOLUTE-VALUE CIRCUIT

APPLICATIONS INFORMATION

OP-07 series units may be substituted directly into 725, 108A/308A* and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-07 may be used in unnulling 741-type sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero through use of a potentiometer (see offset nulling circuit diagram).

The OP-07 provides stable operation with load capacitance of up to 500pF and $\pm 10V$ swings; larger capacitances should be decoupled with a 50 Ω decoupling resistor.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

*TO-99 Package only



OP-08

PRECISION LOW-INPUT-CURRENT OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Offset Voltage 150 μ V Max
- Low Offset Voltage Drift 2.5 μ V/ $^{\circ}$ C Max
- Five Times PM108A Output Current 5mA Min
- Low Offset Current 200pA Max
- Low Bias Current 2nA Max
- Low Power Consumption 18mW Max @ \pm 15V
- High Common-Mode Input Range \pm 13.5V Min
- MIL-STD-883 Class B Processing Available
- Silicon-Nitride Passivation
- 125 $^{\circ}$ C Temperature-Tested Dice

ORDERING INFORMATION†

$T_A = 25^{\circ}$ C V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	DIP 8-PIN	PLASTIC DIP 8-PIN	
0.15	OP08AJ*	OP08AZ*		MIL
0.15	OP08EJ	OP08EZ	OP08EP	COM
1.0	OP08CJ*	OP08CZ*		MIL
1.0	OP08GJ	OP08GZ	OP08GP	COM

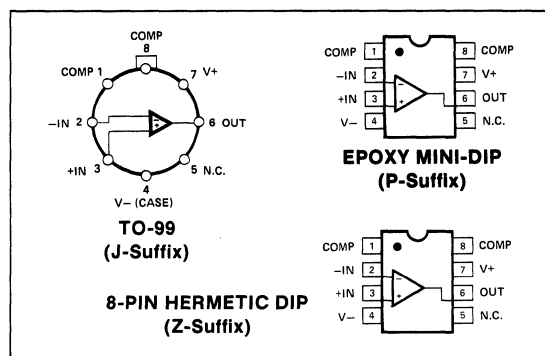
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

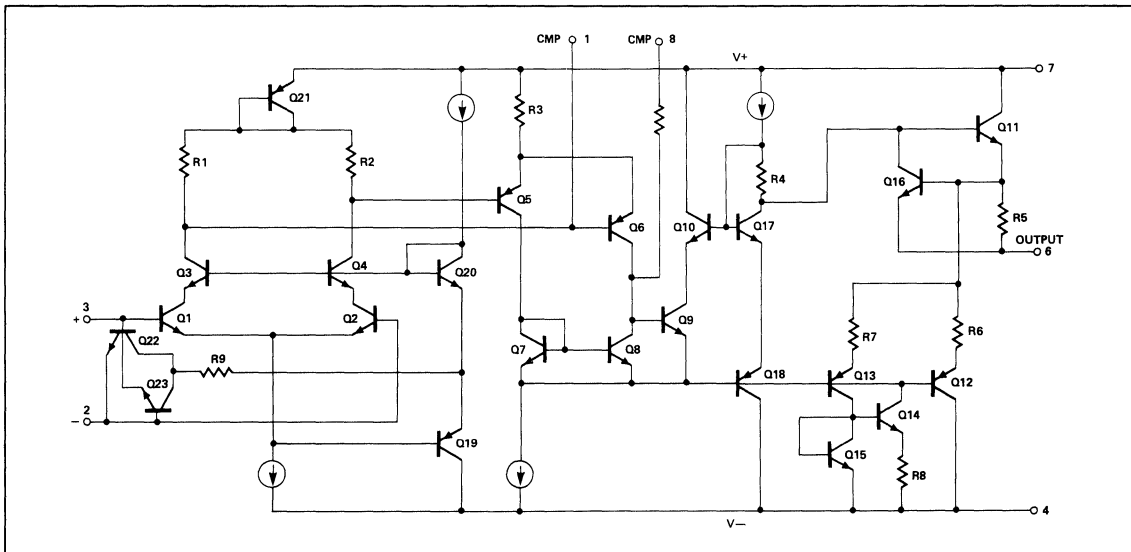
GENERAL DESCRIPTION

The PMI OP-08 is an improved version of the popular LM108A low-power op amp. Excellent performance is achieved by applying PMI's ion-implanted super-beta process and on-chip-zener-zap trimming. The OP-08 has a three-times lower offset voltage and a two-times lower offset voltage drift. Worst-case input offset voltage over -55° C to $+125^{\circ}$ C for the OP-08 is only 350 μ V. In addition, the OP-08 has five times the output current capability of the 108A. For an op amp with identical specifications plus internal frequency compensation, see the OP-12 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



5

OPERATIONAL AMPLIFIERS

**ABSOLUTE MAXIMUM RATINGS** (Note 4)

Supply Voltage	OP-08A, OP-08E (All DICE except GR)	$\pm 20\text{V}$
	OP-08C, OP-08G (GR DICE Only)	$\pm 18\text{V}$
Internal Power Dissipation (Note 1)		500mW
Differential Input Current (Note 2)		$\pm 10\text{mA}$
Input Voltage (Note 3)		$\pm 15\text{V}$
Output Short-Circuit Duration		Indefinite
Operating Temperature Range		
	OP-08A, OP-08C	-55°C to $+125^{\circ}\text{C}$
	OP-08E, OP-08G	0°C to $+70^{\circ}\text{C}$
Storage Temperature Range (J, Z)		-65°C to $+150^{\circ}\text{C}$
Storage Temperature Range (P)		-65°C to $+125^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)		300°C
DICE Junction Temperature (T_j)		-65°C to $+150^{\circ}\text{C}$

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	$7.1\text{mW}/^{\circ}\text{C}$
8-Pin Plastic DIP (P)	36°C	$5.6\text{mW}/^{\circ}\text{C}$
8-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^{\circ}\text{C}$

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs without some limiting resistance.
3. For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $T_A = +25^{\circ}\text{C}$, $V_S = \pm 20\text{V}$ for A and E Grades, $V_S = \pm 15\text{V}$ for C and G Grades, unless otherwise noted. Compensation capacitor = 30pF.

PARAMETER	SYMBOL	CONDITIONS	OP-08A/E			OP-08C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.80	2.0	—	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10\text{Hz}$	—	22	—	—	22	—	$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 100\text{Hz}$	—	21	—	—	21	—	
		$f_o = 1000\text{Hz}$	—	20	—	—	20	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10\text{Hz}$	—	0.15	—	—	0.15	—	$\text{pA}/\sqrt{\text{Hz}}$
		$f_o = 100\text{Hz}$	—	0.14	—	—	0.14	—	
		$f_o = 1000\text{Hz}$	—	0.13	—	—	0.13	—	
Input Resistance — Differential Mode	R_{IN}	(Note 1)	26	70	—	10	50	—	M Ω
Input Voltage Range	IVR	$V_S = \pm 15\text{V}$	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5\text{V}$	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	—	1	7	—	2	63	$\mu\text{V}/\text{V}$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10\text{k}\Omega$, $V_O = \pm 10\text{V}$	80	300	—	40	250	—	V/mV
		$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$, $V_S = \pm 15\text{V}$	50	150	—	—	100	—	
Output Voltage Swing	V_O	$R_L \geq 10\text{k}\Omega$, $V_S = \pm 15\text{V}$ $R_L \geq 2\text{k}\Omega$, $V_S = \pm 15\text{V}$	± 13	± 14	—	± 13	± 14	—	V
Slew Rate	SR	$R_L \geq 2\text{k}\Omega$	—	0.12	—	—	0.12	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.8	—	—	0.8	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	200	—	—	200	—	Ω
Power Consumption	P_d	$V_S = \pm 15\text{V}$	—	9	18	—	12	24	mW
		$V_S = \pm 5\text{V}$	—	3	6	—	4	8	

NOTE:

1. Guaranteed by input bias current.



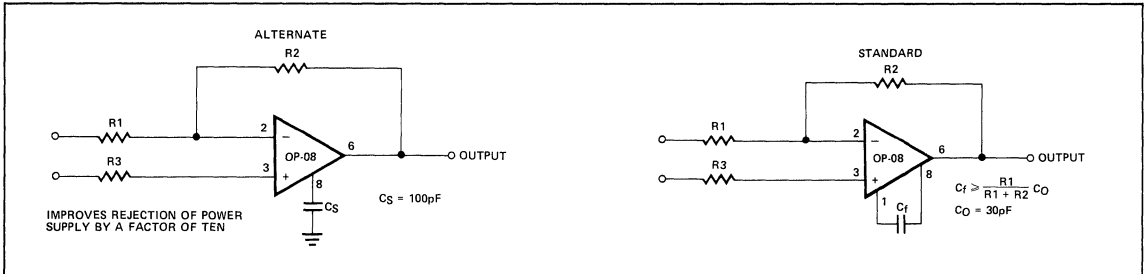
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for C Grade and $V_S = \pm 20V$ for A Grade, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08A			OP-08C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.12	0.35	—	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.5	10	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.12	0.40	—	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	$\mu A/^\circ C$
Input Bias Current	I_B		—	1.2	3.0	—	1.8	10	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	100	110	—	80	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	4	10	—	5	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 5k\Omega$, $V_O = \pm 10V$ $V_S = \pm 15V$	40	120	—	15	80	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$ $R_L \geq 5k\Omega$, $V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	V
Power Consumption	P_d	$V_S = \pm 15V$	—	9	18	—	15	24	mW

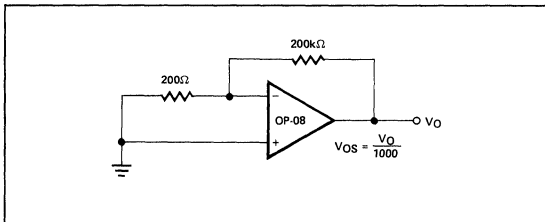
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OPERATIONAL AMPLIFIERS

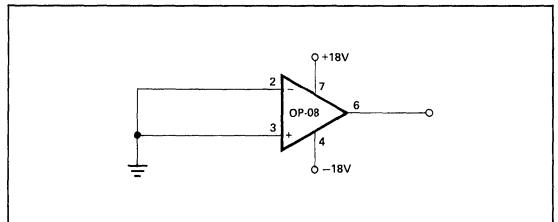
COMPENSATION CIRCUITS



OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT

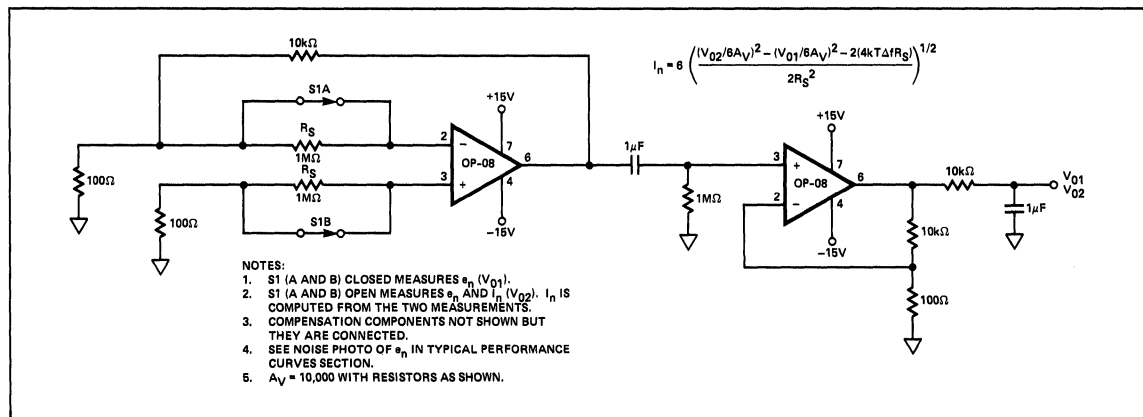


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for G Grade and $V_S = \pm 20V$ for E Grade, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08E			OP-08G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.50	2.5	—	1.5	10	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.12	6.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	0.50	2.5	—	2.0	50	$pA/^\circ C$
Input Bias Current	I_B		—	1.0	2.6	—	1.4	6.5	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	2	10	—	3	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	100	—	—	80	—	V/mV
		$R_L \geq 10k\Omega$, $V_O = \pm 10V$, $V_S = \pm 15V$	60	200	—	25	150	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	V
		$R_L \geq 2k\Omega$, $V_S = \pm 15V$	± 10	± 12	—	± 10	± 12	—	
Power Consumption	P_d	$V_S = \pm 15V$	—	9	18	—	15	24	mW

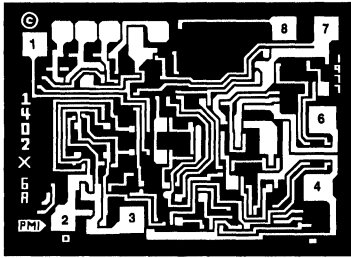
NOTE:

1. Sample tested.

LOW-FREQUENCY NOISE TEST CIRCUIT (0.1 to 10Hz)




DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.058 × 0.042 Inch, 2436 sq. mils (1.47 × 1.07mm, 1.57 sq. mm)

1. COMPENSATION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V⁻
6. OUTPUT
7. V⁺
8. COMPENSATION

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 20V$, $T_A = 25^\circ C$ for OP-08N and OP-08G devices; $V_S = \pm 20V$, $T_A = 125^\circ C$ for OP-08NT and OP-08GT devices; $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-08GR devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08NT LIMIT	OP-08N LIMIT	OP-08GT LIMIT	OP-08G LIMIT	OP-08GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.15	0.6	0.3	1.0	mV MAX
Input Offset Current	I_{OS}		0.2	0.2	0.4	0.2	0.5	nA MAX
Input Bias Current	I_B		2	2	4	2	5	nA MAX
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13.5	± 13.5	± 13.5	± 13.5	± 13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$ $V_S = \pm 15V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	$\mu V/V$ MAX
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 5k\Omega$	± 13 — ± 10	± 13 ± 10 —	± 13 — ± 10	± 13 ± 10 —	± 13 ± 10 —	V MIN
Large-Signal Voltage Gain ($V_O = \pm 10V$)	A_{VO}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$, $V_S = \pm 15V$ $R_L \geq 5k\Omega$, $V_S = \pm 15V$	— — 40	80 50 —	— 50 40	80 50 —	40 — —	V/mV MIN
Input Resistance	R_{IN}	(Note 2)	—	25	—	25	10	M Ω MIN
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_S = \pm 15V$ $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

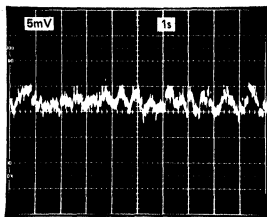
NOTES:

1. For 25°C characteristics of NT & GT devices, see N & G characteristics, respectively.
2. Guaranteed by input bias current.

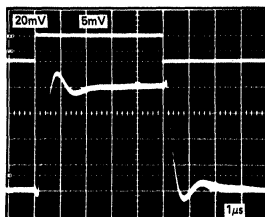
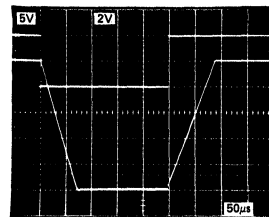
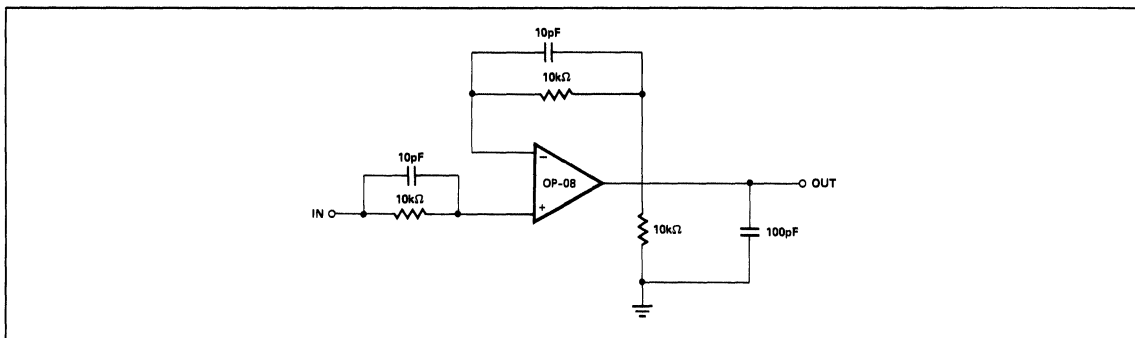
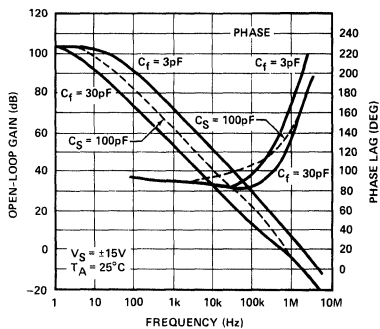
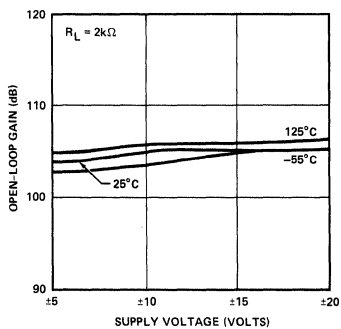
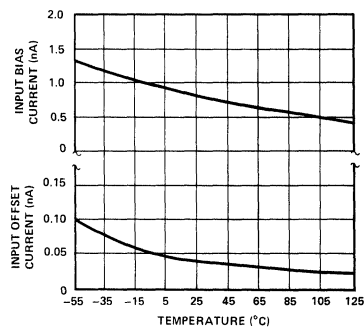
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

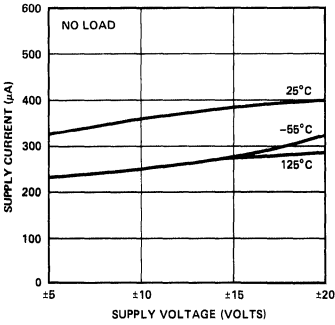
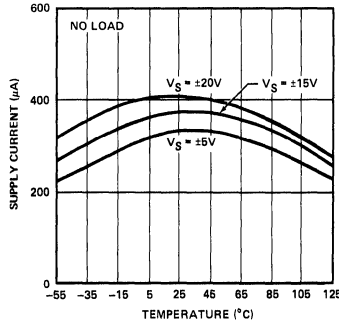
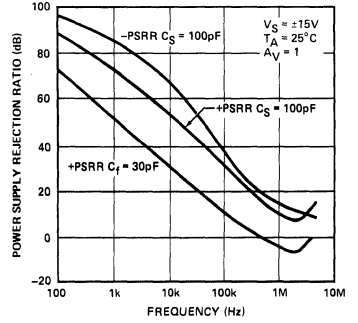
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08NT TYPICAL	OP-08N TYPICAL	OP-08GT TYPICAL	OP-08G TYPICAL	OP-08GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	0.5	0.5	1.0	pA/°C

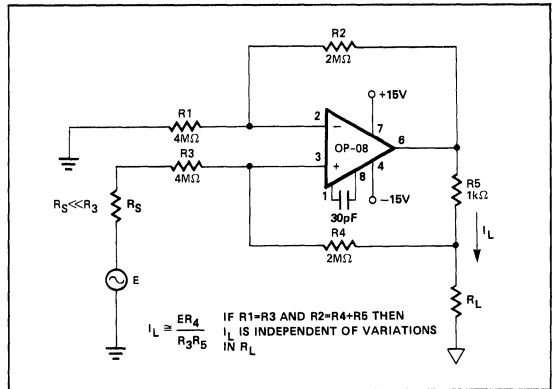
TYPICAL PERFORMANCE CHARACTERISTICS
LOW FREQUENCY NOISE


$R_S = 0$, $BW = 0.1\text{Hz TO } 10\text{Hz}$
 5mV/DIV AT READOUT
 0.5 μ V/DIV REFERRED TO INPUT

SMALL-SIGNAL TRANSIENT RESPONSE

LARGE-SIGNAL TRANSIENT RESPONSE

TRANSIENT RESPONSE TEST CIRCUIT

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

OPEN-LOOP GAIN vs SUPPLY VOLTAGE

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE


TYPICAL PERFORMANCE CHARACTERISTICS
SUPPLY CURRENT vs SUPPLY VOLTAGE

SUPPLY CURRENT vs TEMPERATURE

POWER SUPPLY REJECTION RATIO (PSRR) vs FREQUENCY

APPLICATIONS INFORMATION

The OP-08 series has very low input offset and bias currents; the user is cautioned that printed circuit board leakage currents can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is needed to take full advantage of the OP-08 performance. Board leakage is minimized by encircling the input pins with a guard ring maintained at the same potential as the inputs. This guard ring should be driven by a low impedance source, such as an amplifier's output or ground.

TYPICAL APPLICATION
BILATERAL CURRENT SOURCE


Precision Monolithics Inc.

FEATURES

- Guaranteed V_{OS} 500 μ V Max
- Guaranteed Matched CMRR 94dB Min
- Guaranteed Matched V_{OS} 750 μ V Max
- RC/RM4136 Direct Replacement (OP-09)
- LM148/LM348 Direct Replacement (OP-11)
- Low Noise
- Silicon-Nitride Passivation
- Internal Frequency Compensation
- Low Crossover Distortion
- Continuous Short-Circuit Protection
- Low Input Bias Current

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	EPOXY DIP 14-PIN	LCC	OPERATING TEMPERATURE RANGE
0.5	OP-09AY* OP-11AY*		OP11ARC/883	MIL
0.5	OP-09EY OP-11EY	OP-11EP		COM
2.5	OP-09BY* OP-11BY*			MIL
2.5	OP-09FY OP-11FY	OP-09FP OP-11FP		COM
5.0	OP-11CY*			MIL
5.0	OP-11GY	OP-11GP		COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-09 and OP-11 provide four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-11 is pin compatible with the LM148, LM348, RM4156, and HA4741 amplifiers. The OP-09 is pin compatible with the RM4136 and RC4136. The amplifiers are matched for common-mode rejection ratio and offset voltage which is very important in designing instrumentation amplifiers. In addition, the ampli-

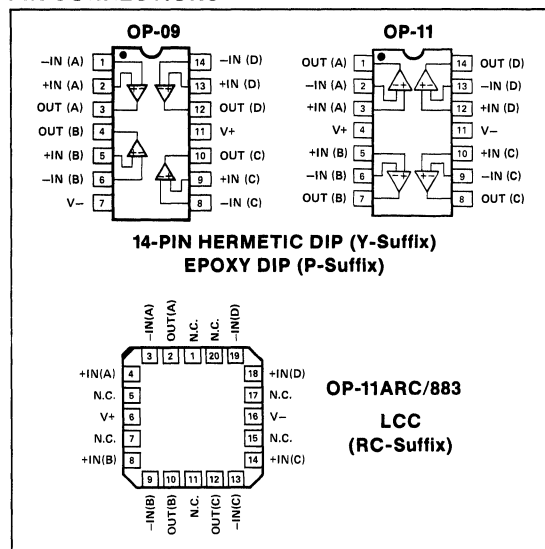
fier is designed to have equal positive-going and negative-going slew rates. This is an important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift, and excellent long-term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise", provides high reliability, and assures long-term stability of parameters.

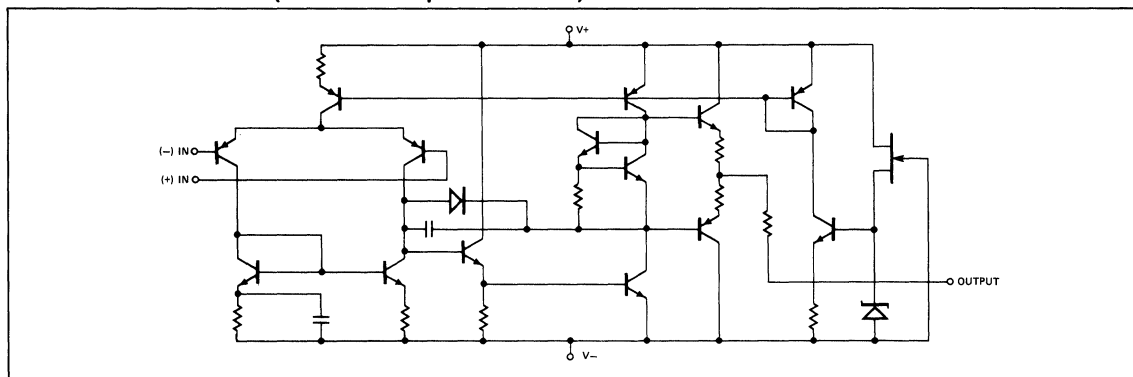
The OP-09 and OP-11 are ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance.

OP-09's and OP-11's with processing per the requirements of MIL-STD-883 are available. For dual-741-type versions, see the OP-04/14 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of Four Amplifiers is Shown)





ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage $\pm 22V$
 OP-09GR and OP-11GR (Only) $\pm 18V$
 Internal Power Dissipation (Note 1)
 RC, Y-Package 800mW
 P-Package 500mW
 Differential Input Voltage $\pm 30V$
 Input Voltage Supply Voltage
 Output Short-Circuit Duration Continuous
 (One Amplifier Only)
 Storage Temperature Range
 RC, Y-Package $-65^{\circ}C$ to $+150^{\circ}C$
 P-Package $-65^{\circ}C$ to $+125^{\circ}C$
 Lead Temperature Range (Soldering, 60 sec) $300^{\circ}C$
 DICE Junction Temperature (T_j) $-65^{\circ}C$ to $+150^{\circ}C$
 Operating Temperature Range
 OP-09A, OP-09B $-55^{\circ}C$ to $+125^{\circ}C$
 OP-09E, OP-09F $0^{\circ}C$ to $+70^{\circ}C$

OP-11A, OP-11B,
 OP-11C, OP-11ARC $-55^{\circ}C$ to $+125^{\circ}C$
 OP-11E, OP-11F, OP-11G $0^{\circ}C$ to $+70^{\circ}C$

NOTES:

- See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	70°C	10.0mW/°C
14-Pin Plastic DIP (P)	42°C	6mW/°C
LCC (RC)	70°C	7.8mW/°C

- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^{\circ}C$, $R_S \leq 100\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.5	0.75	—	0.8	2.0	mV
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 12V$ $V_{CM} = \pm 12V$	—	1	20	—	1	20	$\mu V/V$ dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for OP-09A, OP-09B, OP-11A and OP-11B, $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for OP-09E, OP-09F, OP-11E and OP-11F, $R_S \leq 100\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.6	1.0	—	1.0	2.5	mV
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 12V$ $V_{CM} = \pm 12V$	—	3.2	20	—	3.2	20	$\mu V/V$ dB

5
OPERATIONAL AMPLIFIERS

**ELECTRICAL CHARACTERISTICS (Each Amplifier)** at $V_S = \pm 15V$ $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A/E OP-11A/E			OP-09B/F OP-11B/F			OP-11C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.3	0.5	—	0.6	2.5	—	1.2	5.0	mV
Input Offset Current	I_{OS}		—	5.5	20	—	25	50	—	75	200	nA
Input Bias Current	I_B		—	180	300	—	300	500	—	300	500	nA
Input Resistance Differential Mode	R_{IN}	(Note 3)	0.17	0.29	—	0.1	0.17	—	0.1	0.17	—	M Ω
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V, R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V,$ $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	$\mu V/V$
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11	± 13	—	± 11	± 13	—	± 11	± 13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \leq 2k\Omega, V_O = \pm 10V$	100	650	—	100	650	—	50	500	—	V/mV
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	105	180	—	123	180	—	210	340	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.7	—	—	0.7	—	—	0.7	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	18	—	—	18	—	—	18	—	nV/ \sqrt{Hz}
		$f_O = 100Hz$	—	14	—	—	14	—	—	14	—	
		$f_O = 1000Hz$	—	12	—	—	12	—	—	12	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	17	—	—	17	—	—	17	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.8	—	—	1.8	—	—	1.8	—	pA/\sqrt{Hz}
		$f_O = 100Hz$	—	1.5	—	—	1.5	—	—	1.5	—	
		$f_O = 1000Hz$	—	1.2	—	—	1.2	—	—	1.2	—	
Channel Separation	CS		100	130	—	100	130	—	—	130	—	dB
Slew Rate (Note 2)	SR		0.7	1.0	—	0.7	1.0	—	0.7	1.0	—	V/ μs
Large-Signal Bandwidth (Note 2)		$V_O = 20V_{p-p}$	11	16	—	11	16	—	11	16	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1.0$	2.4	3.0	—	2.4	3.0	—	2.4	3.0	—	MHz
Risetime (Note 2)	t_r	$A_V = +1, V_{IN} = 50mV$	—	110	145	—	110	145	—	110	145	ns
Overshoot (Note 2)	OS		—	15	25	—	15	25	—	15	25	%

NOTES:

1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed by input bias current.
4. Guaranteed by risetime.

**ELECTRICAL CHARACTERISTICS (Each Amplifier)** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A OP-11A			OP-09B OP-11B			OP-11C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.4	1.0	—	1.0	3.5	—	1.5	6.0	mV
Average Input Offset Voltage Drift (Note 3)	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	20	40	—	40	80	—	250	300	nA
Average Input Offset Current Drift (Note 3)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	$nA/^\circ C$
Input Bias Current	I_B		—	200	375	—	400	650	—	400	800	nA
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11	± 13	—	± 11	± 13	—	± 11	± 13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09E OP-11E			OP-09F OP-11F			OP-11G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.4	0.8	—	0.8	3.0	—	1.5	6.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	14	30	—	40	60	—	250	300	nA
Average Input Offset Current Drift (Note 3)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	$nA/^\circ C$
Input Bias Current	I_B		—	200	350	—	400	550	—	400	800	nA
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11	± 13	—	± 11	± 13	—	± 11	± 13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

NOTES:

1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed but not tested.

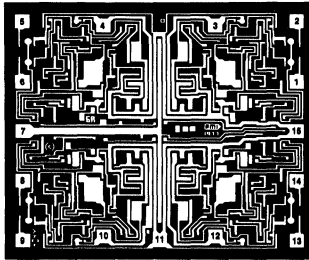
5

OPERATIONAL AMPLIFIERS



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)

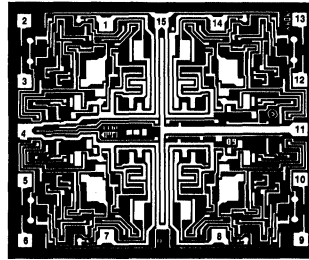
OP-09



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. OUTPUT (A)
4. OUTPUT (B)
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. V-
8. INVERTING INPUT (C)
9. NONINVERTING INPUT (C)
10. OUTPUT (C)
11. V+
12. OUTPUT (D)
13. NONINVERTING INPUT (D)
14. INVERTING INPUT (D)
15. V+

**DIE SIZE 0.085 × 0.070 inch, 5950 sq. mils
(2.16 × 1.78 mm, 3.84 sq. mm)**

OP-11



1. OUTPUT (A)
2. INVERTING INPUT (A)
3. NONINVERTING INPUT (A)
4. V-
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. OUTPUT (B)
8. OUTPUT (C)
9. INVERTING INPUT (C)
10. NONINVERTING INPUT (C)
11. V-
12. NONINVERTING INPUT (D)
13. INVERTING INPUT (D)
14. OUTPUT (D)
15. V+

**DIE SIZE 0.085 × 0.070 inch, 5950 sq. mils
(2.16 × 1.78 mm, 3.84 sq. mm)**

NOTE:

Either or both V+ pads may be used without any change in performance.

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-09/11N, OP-09/11G and OP-09/11GR devices; $T_A = 125^\circ C$ for OP-09/11NT and OP-09/11GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09NT	OP-09N	OP-09GT	OP-09GR	UNITS
			OP-11NT	OP-11N	OP-11GT	OP-11GR	
			LIMIT	LIMIT	LIMIT	LIMIT	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	1.0	0.5	3.5	2.5	5.0 mV MAX
Input Offset Current	I_{OS}		20	20	50	50	200 nA MAX
Input Bias Current	I_B		300	300	500	500	500 nA MAX
Input Voltage Range	IVR		± 12	± 12	± 12	± 12	± 12 V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$ $R_S \leq 10k\Omega$	100	100	100	100	70 dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$ $R_S \leq 10k\Omega$	32	32	32	32	100 $\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L = 2k\Omega$	± 11 ± 11	± 12 ± 11	± 11 ± 11	± 12 ± 11	± 11 ± 11 V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	50	100	50 V/mV MIN
Power Consumption (Four Amplifiers)	P_d	$V_{OUT} = 0$ No Load	200	180	200	180	340 mW MAX

NOTES:

For 25°C characteristics of NT & GT devices, see N & G characteristics, respectively.

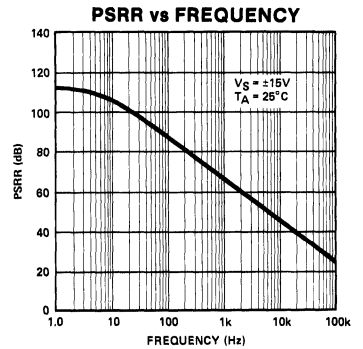
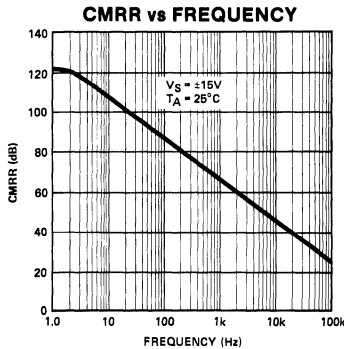
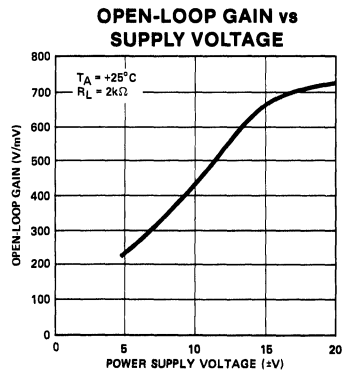
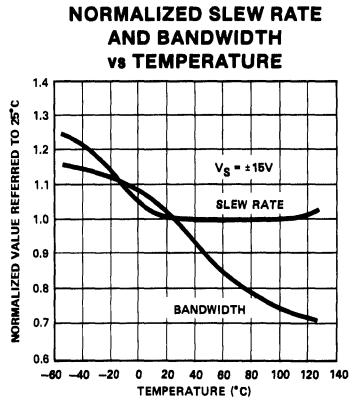
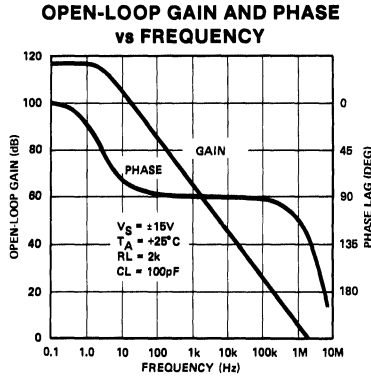
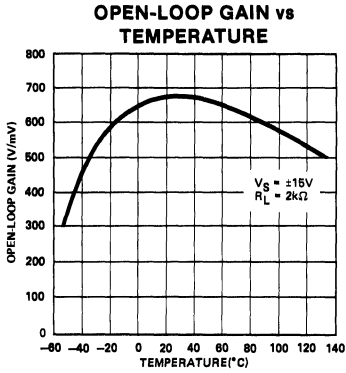
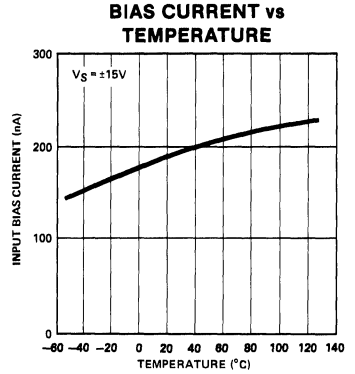
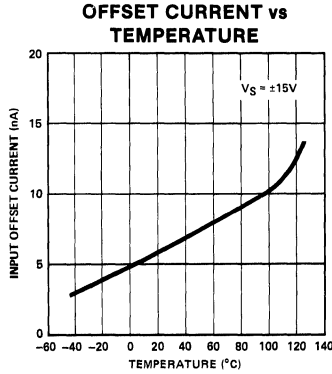
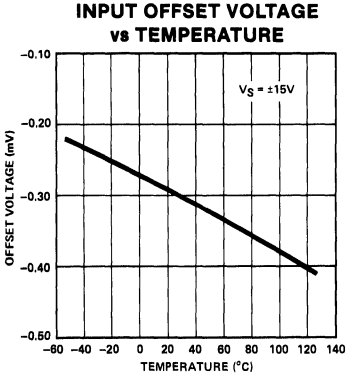
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09NT	OP-09N	OP-09GT	OP-09GR	UNITS
			OP-11NT	OP-11N	OP-11GT	OP-11GR	
			TYPICAL	TYPICAL	TYPICAL	TYPICAL	
Slew Rate	SR	$A_V = 1$ $R_L \geq 2k\Omega$	1	1	1	1	1 V/ μs
Unity Gain Bandwidth	GBW		2	2	2	2	2 MHz
Channel Separation	CS	$A_V = 100$ $f = 10kHz$ $R_S = 1k\Omega$	130	130	130	130	130 dB

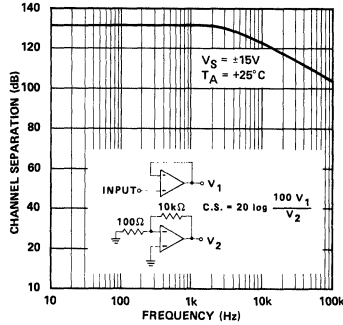


TYPICAL PERFORMANCE CHARACTERISTICS

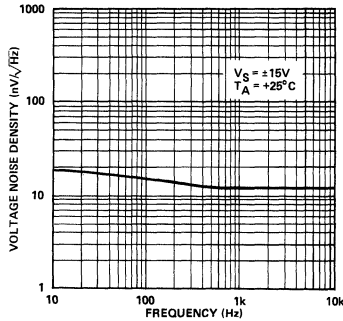


TYPICAL PERFORMANCE CHARACTERISTICS

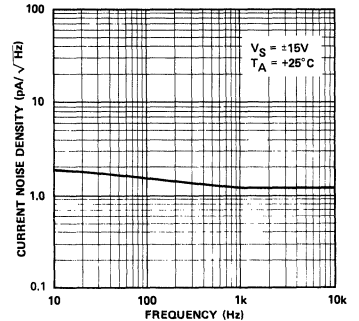
CHANNEL SEPARATION vs FREQUENCY



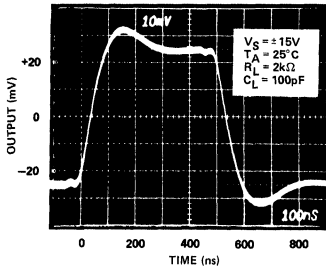
NOISE VOLTAGE DENSITY vs FREQUENCY



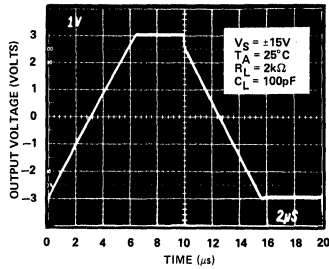
NOISE CURRENT DENSITY vs FREQUENCY



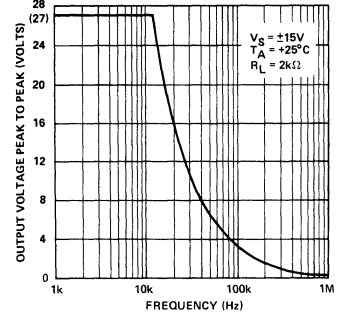
TRANSIENT RESPONSE



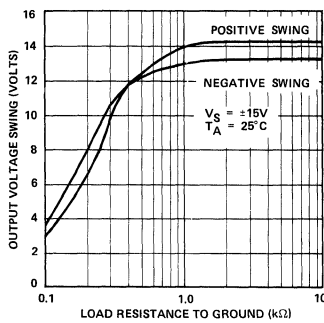
VOLTAGE FOLLOWER PULSE RESPONSE



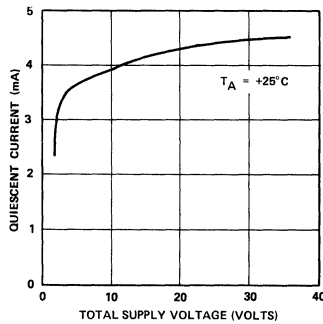
MAXIMUM OUTPUT SWING vs FREQUENCY



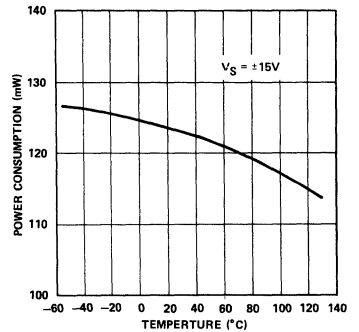
OUTPUT VOLTAGE vs LOAD RESISTANCE



QUIESCENT CURRENT vs SUPPLY VOLTAGE



POWER CONSUMPTION vs TEMPERATURE



Precision Monolithics Inc.

FEATURES

- **Extremely Tight Matching**
- **Excellent Individual Amplifier Parameters**
- **Offset Voltage Match** **0.18mV Max**
- **Offset Voltage Match vs Temp.** **0.8 μ V/ $^{\circ}$ C Max**
- **Common-Mode Rejection Match** **114dB Min**
- **Power Supply Rejection Match** **100dB Min**
- **Bias Current Match** **3.0nA Max**
- **Low Noise** **0.6 μ V_{p-p} Max**
- **Low Bias Current** **3.0nA Max**
- **High Common-Mode Input Impedance** **200G Ω Typ**
- **Excellent Channel Separation** **126dB Min**

ORDERING INFORMATION†

$T_A = 25^{\circ}\text{C}$ V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.5	OP10AY*	MIL
0.5	OP10EY	COM
0.5	OP10Y*	MIL
0.5	OP10CY	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

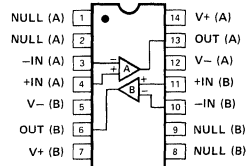
The OP-10 series of dual-matched instrumentation operational amplifiers consists of two independent monolithic high-performance operational amplifiers in a single 14-pin dual-in-line package. Tight matching of critical parameters

is provided between channels of the dual operational amplifier.

The excellent specifications of the individual amplifiers and tight matching over temperature enable construction of high-performance instrumentation amplifiers. The designer can achieve the guaranteed specifications because the common package eliminates temperature differentials which occur in designs using separately housed amplifiers.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode and power-supply rejection ratios. The individual amplifiers feature extremely low offset voltage, offset voltage drift, low noise voltage, low bias current, internal compensation and input/output protection.

PIN CONNECTIONS

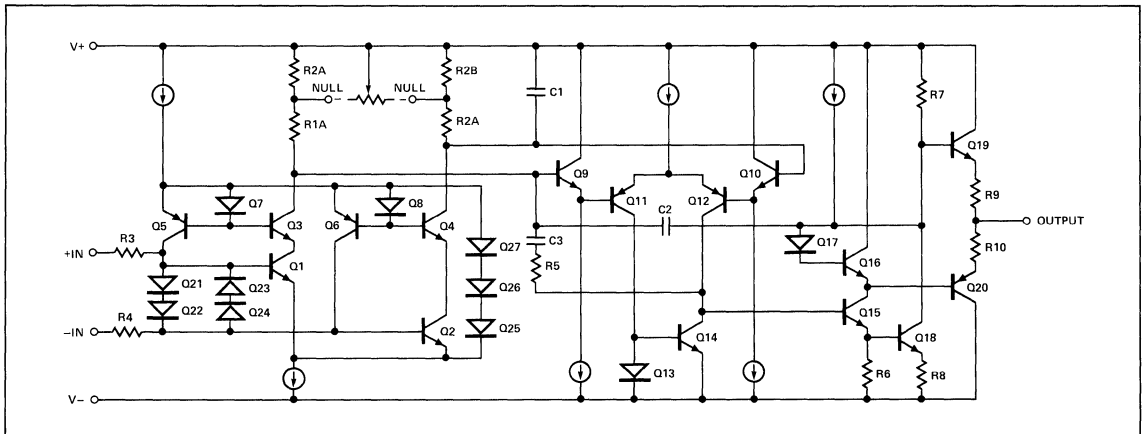


**14-PIN CERAMIC DIP
(Y-Suffix)**

NOTE:

Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.

SIMPLIFIED SCHEMATIC (1/2 OP-10)





ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-10A, OP-10	-55°C to +125°C
OP-10E, OP-10C	0°C to +70°C

DICE Junction Temperature (T_j) -65°C to +150°C
 Lead Temperature Range (Soldering, 60 sec) 300°C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
Dual-in-Line (Y)	106°C	11.3mW/°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. For supply voltages less than +22V, the absolute maximum input voltage is equal to the supply voltage.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Notes 1, 2)	—	0.25	1.0	—	0.25	1.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	1.0	2.8	—	1.0	2.8	nA
Input Bias Current	I_B		—	±1	±3	—	±1	±3	nA
Input Noise Voltage	e_{np-p}	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	20	60	—	20	60	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	G Ω
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 3)	150	500	—	150	500	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier	—	90	120	—	90	120	mW
		$V_S = \pm 3V$	—	4	6	—	4	6	
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.3	0.7	—	0.3	0.7	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	0.7	2.0	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.0	—	0.3	1.0	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1.8	5.6	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	50	—	8	50	$\mu A/^\circ C$
Input Bias Current	I_B		—	± 2	± 6	—	± 2	± 6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	50	—	13	50	$\mu A/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 12.0	± 12.6	—	V

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	ΔV_{OS}		—	0.07	0.18	—	0.12	0.5	mV
Average Noninverting Bias Current	I_{B+}		—	± 1.0	± 3.0	—	± 1.3	± 4.5	nA
Noninverting Offset Current	I_{OS+}		—	0.8	2.8	—	1.1	4.5	nA
Inverting Offset Current	I_{OS-}		—	0.8	2.8	—	1.1	4.5	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	114	123	—	106	120	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	3	10	—	4	20	$\mu V/V$
Channel Separation	CS	(Note 2)	126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.1	0.3	—	0.2	0.9	mV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 2)	—	0.45	1.3	—	0.9	2.5	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 3) Channel A only	—	0.3	0.8	—	0.4	1.2	$\mu V/^\circ C$

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

 5
 OPERATIONAL AMPLIFIERS

**MATCHING CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Average Noninverting Bias Current	I_{B^+}		—	± 2.0	± 6.0	—	± 2.4	± 8.0	nA
Average Drift of Noninverting Bias Current	TCI_{B^+}	(Note 2)	—	10	40	—	15	—	$\mu A/^\circ C$
Noninverting Offset Current	I_{OS^+}		—	2.0	6.5	—	2.4	9.0	nA
Average Drift of Noninverting Offset Current	TCI_{OS^+}	(Note 2)	—	12	50	—	18	—	$\mu A/^\circ C$
Inverting Offset Current	I_{OS^-}		—	2.0	6.5	—	2.4	9.0	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	108	120	—	103	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	6	20	—	7	32	$\mu V/V$

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/Time$	(Notes 1, 2)	—	0.3	1.5	—	0.5	—	$\mu V/Mo$
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	± 1.2	± 4.0	—	± 1.8	± 7.0	nA
Input Noise Voltage	e_{np-p}	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	10.3	18.0	—	10.5	20.0	nV/\sqrt{Hz}
		(Note 2) $f_O = 100Hz$	—	10.0	13.0	—	10.2	13.5	
		$f_O = 1000Hz$	—	9.6	11.0	—	9.8	11.5	
Input Noise Current	i_{np-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	0.32	0.80	—	0.35	0.90	pA/\sqrt{Hz}
		(Note 2) $f_O = 100Hz$	—	0.14	0.23	—	0.15	0.27	
		$f_O = 1000Hz$	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	10	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 3)	150	500	—	100	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.0	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 11.5	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.5	± 12.0	—	—	± 12.0	—	

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0, I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier $V_S = \pm 3V$	—	90	120	—	95	150	mW
Offset Adjustment Range		$R_p = 20k\Omega$	—	± 4	—	—	± 4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	1.2	4.5	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$ (Note 3)	—	0.3	1.0	—	0.4	1.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	50	—	12	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1.5	± 5.5	—	± 2.2	± 9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	50	—	18	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O = \pm 10V$	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 11.0	± 12.6	—	V

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

**MATCHING CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.12	0.5	—	0.3	—	mV
Average Noninverting Bias Current	I_{B^+}		—	± 1.3	± 4.5	—	± 2.0	—	nA
Noninverting Offset Current	I_{OS^+}		—	1.1	4.5	—	1.8	—	nA
Inverting Offset Current	I_{OS^-}		—	1.1	4.5	—	1.8	—	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	106	120	—	—	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	5	—	$\mu V/V$
Channel Separation	CS	(Note 1)	126	140	—	120	137	—	dB

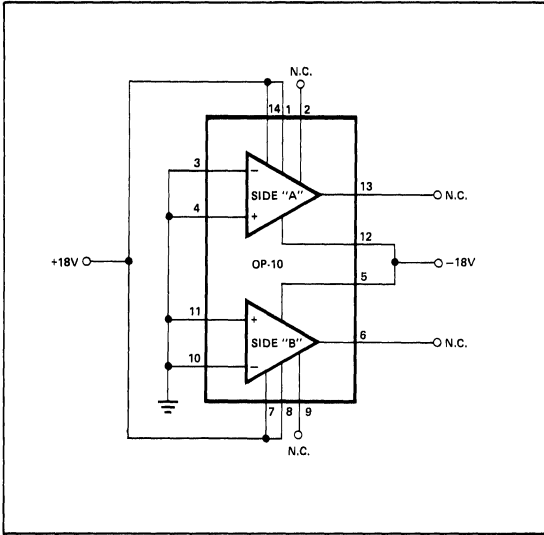
MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.18	0.7	—	0.4	—	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.9	2.3	—	1.3	—	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_L = 20k\Omega$ Channel A Only (Note 2)	—	0.3	0.9	—	0.6	—	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B^+}		—	± 2.0	± 6.0	—	± 2.8	—	nA
Average Drift of Noninverting Bias Current	TCI_{B^+}	(Note 1)	—	12	40	—	18	—	$pA/^\circ C$
Noninverting Offset Current	I_{B^+}		—	2.0	6.0	—	2.8	—	nA
Average Drift of Noninverting Offset Current	TCI_{OS^+}	(Note 1)	—	15	50	—	20	—	$pA/^\circ C$
Input Offset Current	I_{OS^-}		—	2.0	6.0	—	2.8	—	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	103	117	—	—	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	6	32	—	8	—	$\mu V/V$

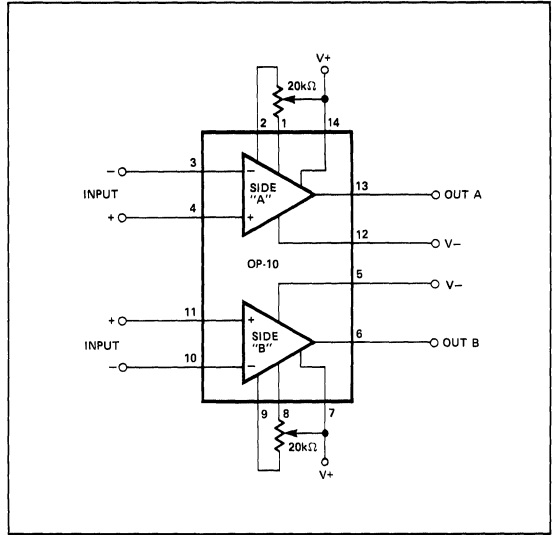
NOTES:

1. Sample tested.
2. Guaranteed by design.

BURN-IN CIRCUIT

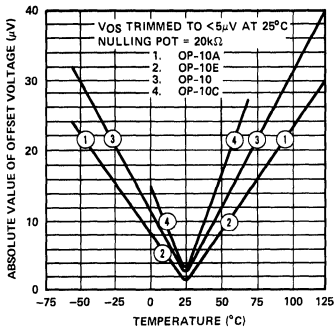


OFFSET NULLING CIRCUIT

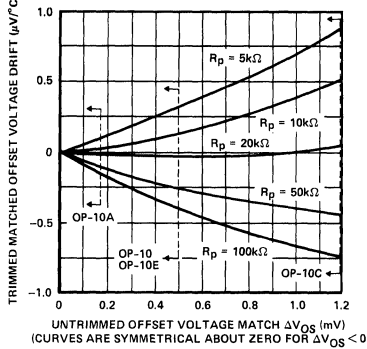


TYPICAL PERFORMANCE CHARACTERISTICS

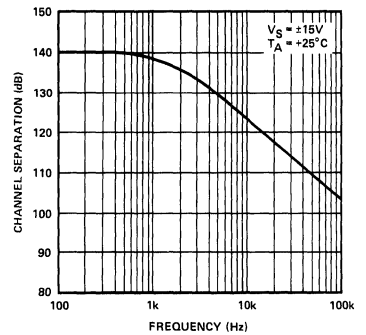
**MATCHING CHARACTERISTICS
TRIMMED OFFSET VOLTAGE
MATCH vs TEMPERATURE**



**MATCHING CHARACTERISTICS
TRIMMED MATCHED OFFSET
VOLTAGE DRIFT AS A
FUNCTION OF TRIMMING POT
(R_p) SIZE AND ΔV_{OS}**

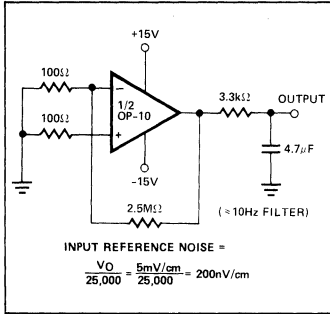


**MATCHING CHARACTERISTICS
CHANNEL SEPARATION
vs FREQUENCY**

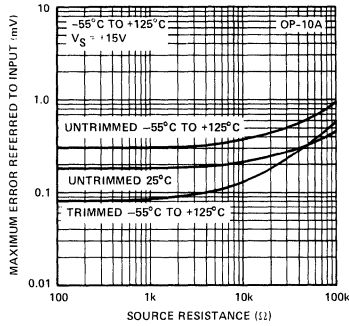


TYPICAL PERFORMANCE CHARACTERISTICS

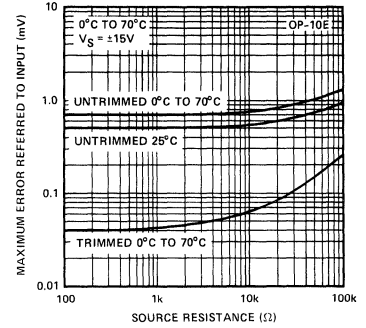
TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



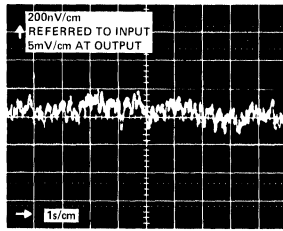
MATCHING CHARACTERISTIC
MAXIMUM INPUT ERROR vs
SOURCE RESISTANCE



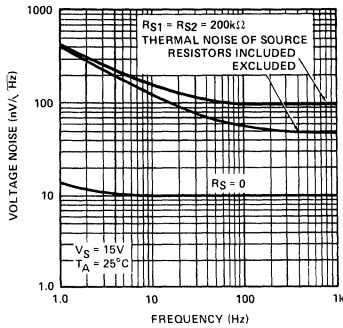
MATCHING CHARACTERISTIC
MAXIMUM INPUT ERROR vs
SOURCE RESISTANCE



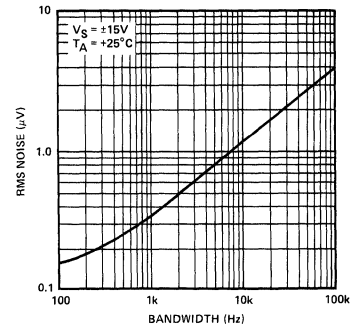
OP-10 LOW FREQUENCY NOISE



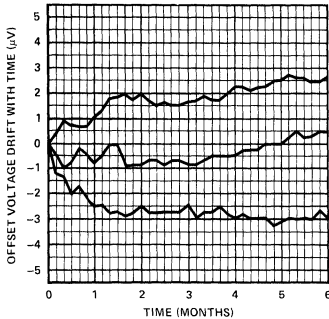
VOLTAGE DENSITY
vs FREQUENCY



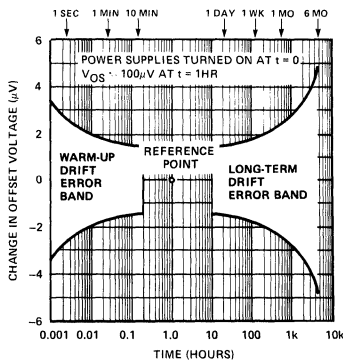
INPUT WIDEBAND NOISE
vs BANDWIDTH
(0.1Hz TO FREQUENCY
INDICATED)



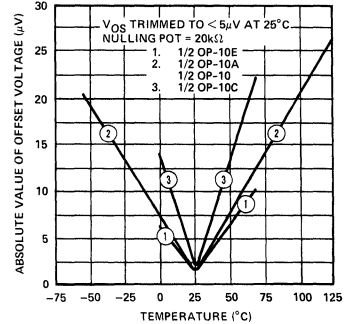
TYPICAL OFFSET VOLTAGE
STABILITY vs TIME



OFFSET VOLTAGE DRIFT
WITH TIME



TRIMMED OFFSET VOLTAGE
vs TEMPERATURE

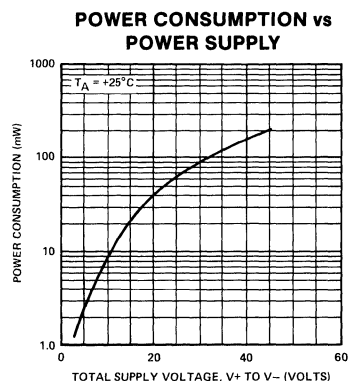
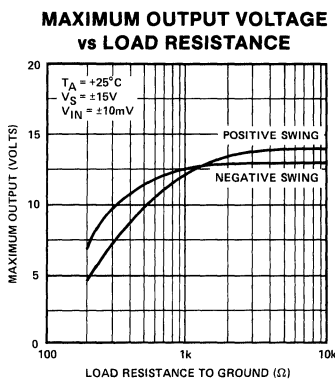
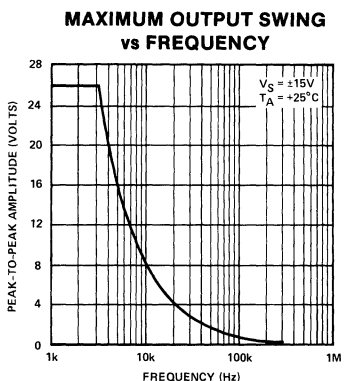
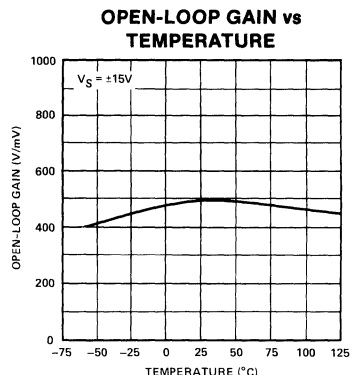
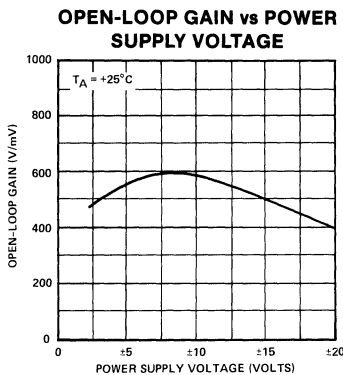
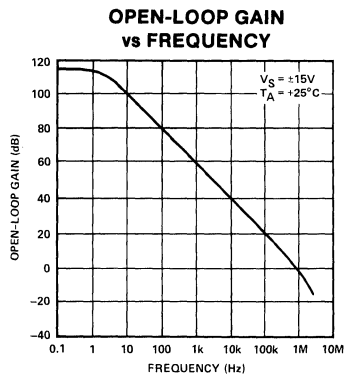
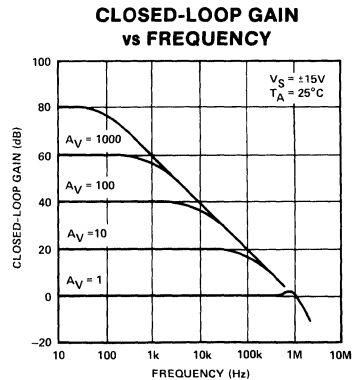
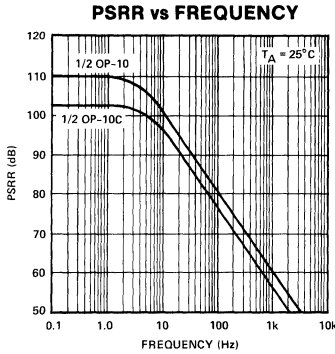
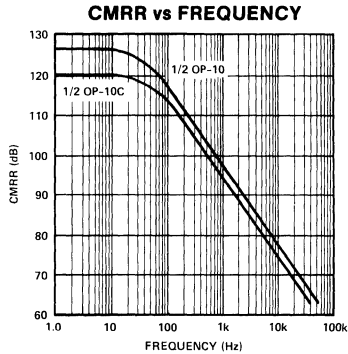


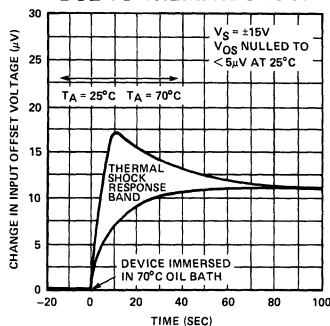
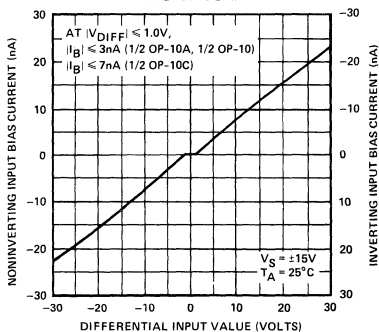
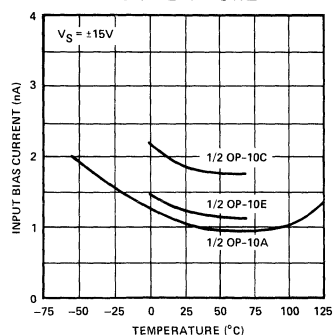


TYPICAL PERFORMANCE CHARACTERISTICS

5

OPERATIONAL AMPLIFIERS



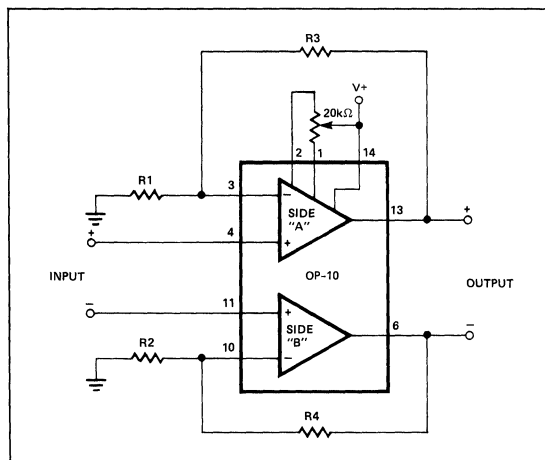
TYPICAL PERFORMANCE CHARACTERISTICS
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK

INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

INPUT BIAS CURRENT vs TEMPERATURE

APPLICATIONS INFORMATION
ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references and many other demanding applications. These designs all require good matching between two operational amplifiers.

The adjacent circuit, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the **difference** between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made very high; this is especially important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature.

For example, consider the case of two op amps, each with 80dB ($100\mu\text{V}/\text{V}$) CMRR. If the CMRR of one device is $+100\mu\text{V}/\text{V}$ while CMRR of the other is $-100\mu\text{V}/\text{V}$, then the net

CMRR will be $200\mu\text{V}/\text{V}$, a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.

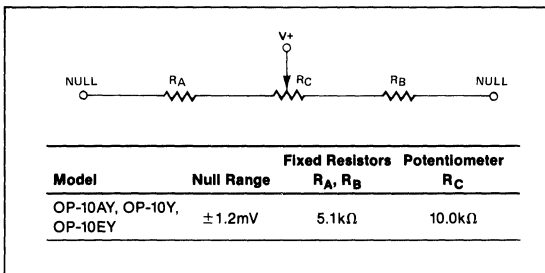

POWER SUPPLIES

The $V+$ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The $V-$ supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset trimming terminals are provided for each amplifier of the OP-10. Guaranteed performance over temperature is obtained by trimming only one side (side A) to match the offset of the other; a net differential offset of zero results. This procedure is used during factory testing of the devices; however, essentially the same results may be obtained by trimming side B to match side A, or by nulling each side individually.

The OP-10 provides lowest drift when trimmed with a 20kΩ potentiometer; this value provides about ±4mV of adjustment range which should be more than adequate for most applications. Where finer trimming resolution is desired, or where unwanted changes in potentiometer position with time and temperature could create unacceptable offsets, the adjustment sensitivity may be reduced by using the circuit shown below.

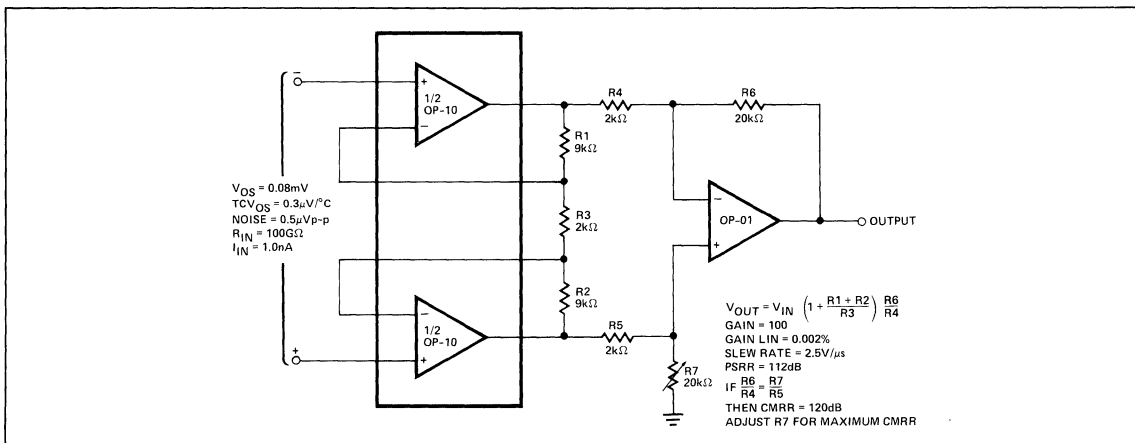

INSTRUMENTATION AMPLIFIERS USING OP-10

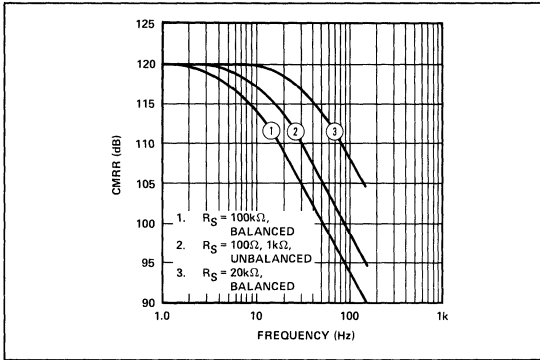
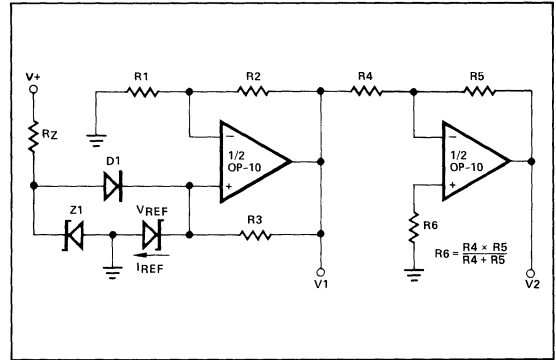
Instrumentation amplifiers with excellent performance can be easily built using the OP-10. Typical performance for a two and three-amplifier design, while more complex, has the advantages of simple gain adjustment by trimming a single resistor (R_3) and

wide common-mode voltage capability at any gain, plus improved gain linearity. Slew rate, small-signal bandwidth, and full power bandwidth are also superior. Speed will be improved by using an OP-01 for the output stage.

TYPICAL PERFORMANCE OF INSTRUMENTATION AMPLIFIERS GAIN = 100

PARAMETER	2 OP AMP DESIGN	3 OP AMP DESIGN
Gain Nonlinearity	0.004%	0.001% (OP-05) 0.002% (OP-01)
Initial Input Offset Voltage	70μV	75μV
vs. Temperature (amplifier A nulled with 20k pot)	0.3μV/°C	0.3μV/°C
vs. Time	3.5μV/month	3.5μV/month
Input Bias Current	± 1nA	± 1nA
vs. Temperature	10pA/°C	10pA/°C
Input Offset Current	0.8nA	0.8nA
vs. Temperature	12pA/°C	12pA/°C
Input Impedance Differential	80GΩ	100GΩ
Common-Mode	100GΩ	100GΩ
Input Noise Voltage (0.1 to 10Hz)	0.5μV _{p-p}	0.5μV _{p-p}
Input Noise Current (0.1 to 10Hz)	14pA _{p-p}	14pA _{p-p}
Common-Mode Rejection	120dB	120dB
Power Supply Rejection	112dB	112dB
Frequency Response		
Small-Signal (-3dB)	6.0Hz	26kHz (OP-05) 85kHz (OP-01)
Full Power	2.5Hz	4.3kHz (OP-05) 43kHz (OP-01)
Slew Rate	0.17V/μs	0.17V/μs (OP-05) 4.0V/μs (OP-01)

5
OPERATIONAL AMPLIFIERS
TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER


**CMRR vs FREQUENCY
INSTRUMENTATION AMPLIFIER (3 OP-AMP DESIGN)**

**PRECISION DUAL TRACKING VOLTAGE REFERENCES
USING OP-10**

**PRECISION DUAL TRACKING VOLTAGE REFERENCES
USING OP-10**

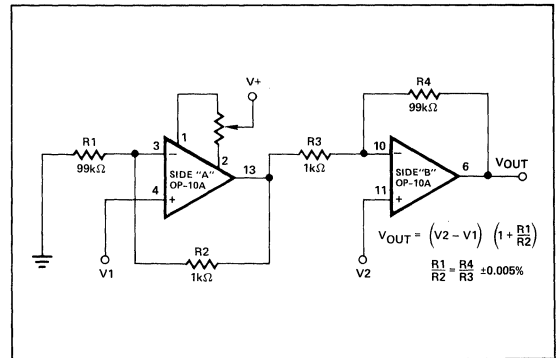
Precision dual tracking voltage references using a single reference source are easily constructed using OP-10. These references exhibit low noise, excellent stability vs. temperature and time, and have excellent power supply rejection.

In the circuit shown, R_3 should be adjusted to set I_{REF} to operate V_{REF} at its minimum temperature coefficient current. Proper circuit start-up is assured by R_Z , Z_1 , and D_1 .

$$V_{Z1} \leq V_{REF} + 2V \qquad V1 = V_{REF} \left(1 + \frac{R2}{R1} \right)$$

$$I_{REF} = (V1 - V_{REF}) / R3 \qquad V2 = V1 \left(\frac{-R5}{R4} \right)$$

Output Impedance ($\Delta I_L: 1.0mA-5.0mA$) $0.25 \times 10^{-3}\Omega$

INSTRUMENTATION AMPLIFIER (2 OP-AMP DESIGN)




OP-12

PRECISION LOW-INPUT-CURRENT OPERATIONAL AMPLIFIER (INTERNALLY COMPENSATED)

Precision Monolithics Inc.

FEATURES

- Low Offset Voltage 150 μ V Max
- Low Offset Voltage Drift 2.5 μ V/ $^{\circ}$ C Max
- Load Current Capability 5mA Min
- Internal Frequency Compensation
- 125 $^{\circ}$ C Temperature Tested Die
- Low Offset Current 200pA Max
- Low Bias Current 2.0nA Max
- Low Power Consumption 18mW Max @ \pm 15V
- High Common-Mode Input Range \pm 13V Min
- MIL-STD-883 Class B Processing Available
- Silicon-Nitride Passivation

GENERAL DESCRIPTION

The PMI OP-12 is an improved version of the popular LM108A low-power op amp. The OP-12 is internally compensated and its chip dimensions are only 42 X 58 mils. Offset voltage is lower; the total worst-case input offset voltage over -55° C to $+125^{\circ}$ C for the OP-12A is only 350 μ V. In addition, the OP-12 drives a 2k Ω load which is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super-beta process and on-chip zener-zap trimming capabilities. The internal compensation makes this op amp ideal for hybrid assembly applications.

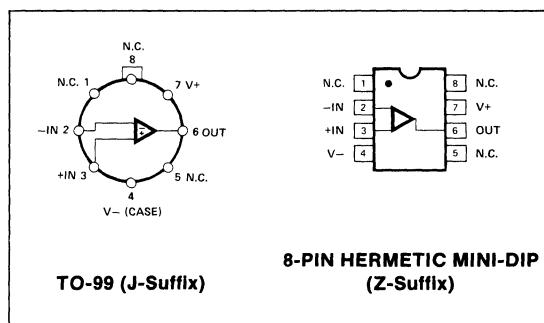
ORDERING INFORMATION†

$T_A = 25^{\circ}$ C V_{OS} MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	
0.15	OP12AJ*	OP12AZ*	MIL
0.15	OP12EJ	OP12EZ	COM
0.30	OP12BJ*	OP12BZ*	MIL
0.30	OP12FJ	OP12FZ	COM
1.0	OP12CJ*	OP12CZ*	MIL
1.0	OP12GJ	OP12GZ	COM

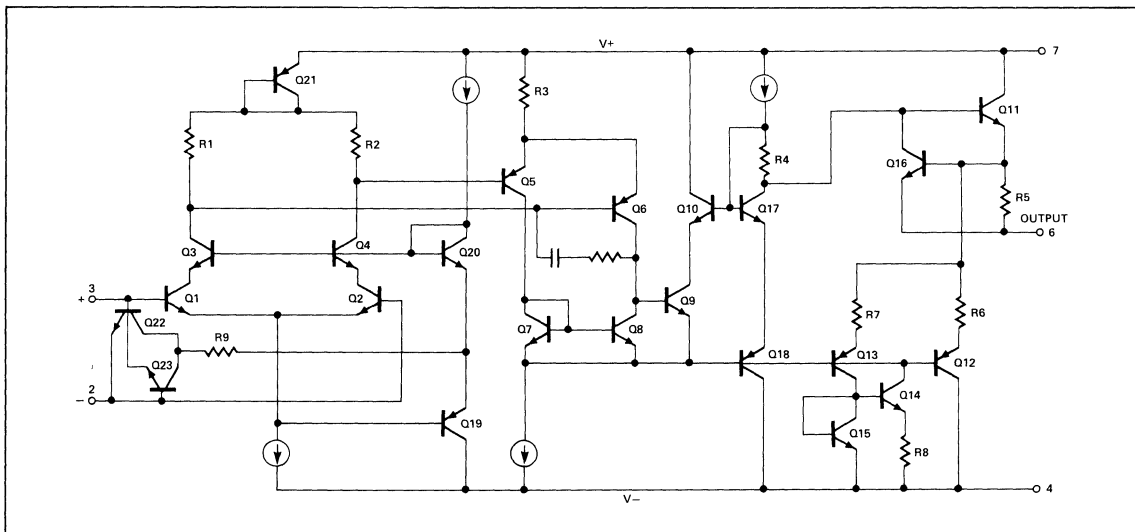
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



OPERATIONAL AMPLIFIERS

5



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage
 OP-12A, OP-12B,
 OP-12E, OP-12F, All DICE except GR ±20V
 OP-12C, OP-12G, GR DICE Only ±18V

Operating Temperature Range
 OP-12A, OP-12B, OP-12C -55°C to +125°C
 OP-12E, OP-12F, OP-12G 0°C to +70°C

Storage Temperature Range -65°C to +150°C
 Lead Temperature Range (Soldering, 60 sec) 300°C
 Internal Power Dissipation (Note 1) 500mW
 Differential Input Current (Note 2) ±10mA
 Input Voltage (Note 3) ±15V
 Output Short-Circuit Duration Indefinite
 DICE Junction Temperature (T_j) -65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±20V and T_A = 25°C for A, B, E and F grades, V_S = ±15V, and T_A = 25°C for C and G grades, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12A/E			OP-12B/F			OP-12C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}		—	0.07	0.15	—	0.18	0.30	—	0.25	1.0	mV
Input Offset Current	I _{OS}		—	0.05	0.20	—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I _B		—	0.8	2.0	—	0.8	2.0	—	1.0	5.0	nA
Input Resistance — Differential-Mode	R _{IN}	(Note 1)	26	70	—	26	70	—	10	50	—	MΩ
Input Voltage Range	IVR	V _S = ±15V	±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±13V	104	120	—	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±5V to ±15V	—	1	7	—	1	7	—	4	63	μV/V
Output Voltage Swing	V _O	R _L ≥ 10kΩ, V _S = ±15V R _L ≥ 2kΩ, V _S = ±15V	±13	±14	—	±13	±14	—	±13	±14	—	V
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 10kΩ V _O = ±10V	80	300	—	80	300	—	40	250	—	V/mV
		R _L ≥ 2kΩ V _O = ±10V	50	150	—	50	150	—	—	100	—	
Power Consumption	P _d	V _S = ±15V, No Load V _S = ±5V, No Load	—	9	18	—	9	18	—	12	24	mW
Input Noise Voltage	e _{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	—	0.9	—	μV _{p-p}
Input Noise Voltage Density	e _n	f _O = 10Hz	—	22	—	—	22	—	—	22	—	nV/√Hz
		f _O = 100Hz	—	21	—	—	21	—	—	21	—	
		f _O = 1000Hz	—	20	—	—	20	—	—	20	—	
Input Noise Current	i _{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	—	3	—	pA _{p-p}
Input Noise Current Density	i _n	f _O = 10Hz	—	0.15	—	—	0.15	—	—	0.15	—	pA/√Hz
		f _O = 100Hz	—	0.14	—	—	0.14	—	—	0.14	—	
		f _O = 1000Hz	—	0.13	—	—	0.13	—	—	0.13	—	
Slew Rate	SR	R _L ≥ 2kΩ	—	0.12	—	—	0.12	—	—	0.12	—	V/μs
Closed-Loop Bandwidth	BW	A _{VCL} = +1	—	0.80	—	—	0.80	—	—	0.80	—	MHz
Open-Loop Output Resistance	R _O	V _O = 0, I _O = 0	—	200	—	—	200	—	—	200	—	Ω

NOTE:

1. Guaranteed by input bias current.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, for C grade, $V_S = \pm 20V$ for A and B grades, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12A			OP-12B			OP-12C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.12	0.35	—	0.28	0.80	—	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.12	0.40	—	0.12	0.40	—	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	0.50	2.5	—	1.0	5.0	$pA/^\circ C$
Input Bias Current	I_B		—	1.2	3.0	—	1.2	3.0	—	1.8	10	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$	—	4	10	—	4	10	—	6	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 5k\Omega$ $V_O = \pm 10V$	40	120	—	40	120	—	15	80	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
		$R_L \geq 5k\Omega$, $V_S = \pm 15V$	± 10	± 13	—	± 10	± 13	—	± 10	± 12	—	
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	9	18	—	9	18	—	15	24	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for G grade, $V_S = \pm 20V$ for E and F grades, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

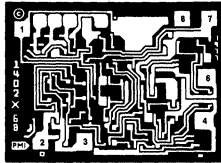
PARAMETER	SYMBOL	CONDITIONS	OP-12E			OP-12F			OP-12G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.23	0.45	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.11	0.60	—	0.12	0.70	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	—	1.0	5.0	$pA/^\circ C$
Input Bias Current	I_B		—	1.0	2.6	—	1.2	5.2	—	1.4	6.5	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$	—	4	10	—	4	10	—	6	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$ $V_O = \pm 10V$	60	200	—	60	200	—	25	150	—	V/mV
		$R_L \geq 2k\Omega$ $V_O = \pm 10V$	25	100	—	25	100	—	—	80	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
		$R_L \geq 5k\Omega$ $V_S = \pm 15V$	± 10	± 12	—	± 10	± 12	—	± 10	± 12	—	
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	9	18	—	9	18	—	15	24	mW

For typical performance characteristics, see OP-08 data sheet. Assume $C_C = 30pF$.

5



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.058 × 0.042 inch, 2436 sq. mils
(1.47 × 1.07 mm, 1.57 sq. mm)

1. NO CONNECTION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V⁻
6. OUTPUT
7. V⁺
8. NO CONNECTION

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-12N, OP-12G and OP-12GR devices; $T_A = 125^\circ C$ for OP-12NT and OP-12GT devices, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	OP-12NT LIMIT	OP-12N LIMIT	OP-12GT LIMIT	OP-12G LIMIT	OP-12GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.15	0.6	0.3	1	mV MAX
Input Offset Current	I_{OS}		0.2	0.2	0.2	0.2	0.5	nA MAX
Input Bias Current	I_B		2	2	2	2	5	nA MAX
Input Voltage Range	IVR		± 13	± 13	± 13	± 13	± 13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 13	± 13	± 13	± 13	± 13	V MIN
		$R_L \geq 2k\Omega$	—	± 10	—	± 10	± 10	
		$R_L \geq 5k\Omega$	± 10	—	± 10	—	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	80	80	80	80	40	V/mV MIN
		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	—	50	—	50	—	
		$R_L \geq 5k\Omega$, $V_O = \pm 10V$	40	—	40	—	—	
Input Resistance	R_{IN}	(Note 1)	26	26	26	26	10	M Ω MIN
Supply Current	I_{SV}	$I_{OUT} = 0$ $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

NOTES:

1. Guaranteed by design.

2. For 25°C specifications of OP-12NT and OP-12GT, see OP-12N and OP-12G, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12NT TYPICAL	OP-12N TYPICAL	OP-12GT TYPICAL	OP-12G TYPICAL	OP-12GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	1.0	1.0	1.0	pA/°C



OP-15/OP-16/OP-17

PRECISION JFET-INPUT OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

FEATURES (All Devices)

- Significant Performance Advantages over LF155, 156 and 157 Devices.
- Low Input Offset Voltage 500 μ V Max
- Low Input Offset Voltage Drift 2.0 μ V/ $^{\circ}$ C
- Minimum Slew Rate Guaranteed on All Models
- Temperature-Compensated Input Bias Currents
- Guaranteed Input Bias Current @ 125 $^{\circ}$ C
- Bias Current Specified WARMED UP Over Temperature
- Internal Compensation
- Low Input Noise Current 0.01pA/ $\sqrt{\text{Hz}}$
- High Common-Mode Rejection Ratio 100dB
- Models With MIL-STD-883 Processing Available
- 125 $^{\circ}$ C Temperature Tested DICE

OP-15

- 156 Speed With 155 Dissipation (80mW Typ)
- Wide Bandwidth 6MHz
- High Slew Rate 13V/ μ s
- Fast Settling to \pm 0.1% 1200ns

OP-16

- Higher Slew Rate 25V/ μ s
- Faster Settling to \pm 0.1% 900ns
- Wider Bandwidth 8MHz

OP-17

- Highest Slew Rate 60V/ μ s
- Fastest Settling to \pm 0.1% 600ns
- Highest Gain Bandwidth Product 30MHz

GENERAL DESCRIPTION

The PMI JFET-input series of devices offer clear advantages over industry-generic devices and are superior in both cost and performance to many dielectrically-isolated and hybrid

op amps. All devices offer offset voltages as low as 0.5mV with TCV_{OS} guaranteed to 5 μ V/ $^{\circ}$ C. A unique input bias cancellation circuit reduces the I_{B} by a factor of 10 over conventional designs. In addition, PMI specifies I_{B} and I_{OS} with the devices warmed up and operating at 25 $^{\circ}$ C ambient.

These devices were designed to provide real precision performance along with high speed. Although they can be nulled, the design objective was to provide low offset-voltage without nulling. Systems generally become more cost effective as the number of trim circuits is decreased. PMI achieves this performance by use of an improved Bipolar compatible JFET process coupled with on-chip, zener-zap offset trimming.

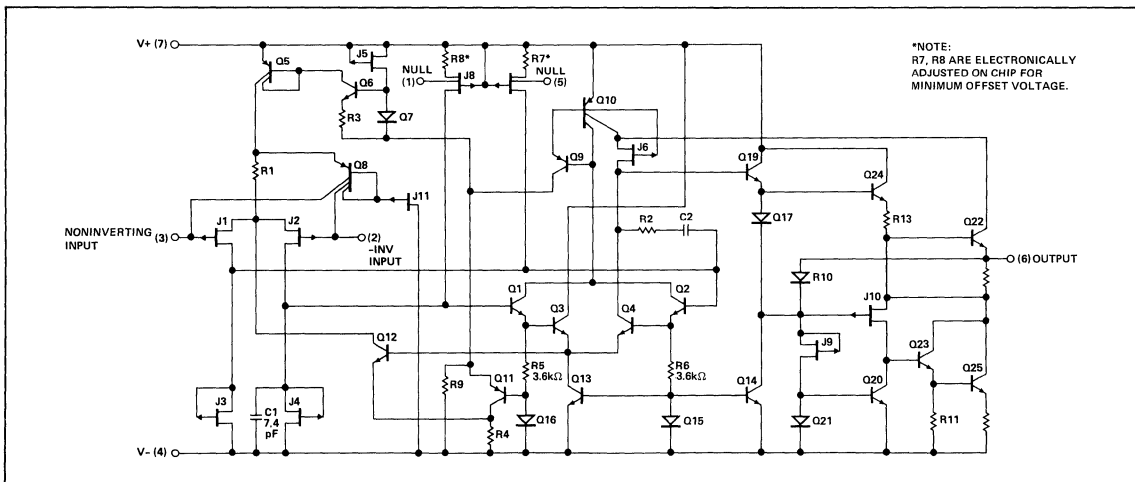
The OP-15 provides an excellent combination of high speed and low input offset voltage. In addition, the OP-15 offers the speed of the 156A op amp with the power dissipation of a 155A. The combination of a low input offset voltage of 500 μ V, slew rate of 13V/ μ s, and settling time of 1200ns to 0.1% makes the OP-15 an op amp of both precision and speed. The additional features of low supply current coupled with an input bias current of 9nA at 125 $^{\circ}$ C ambient (not junction) temperature makes the OP-15 ideal for a wide range of applications.

The OP-16 features a slew rate of 25V/ μ s and a settling time of 900ns to 0.1% which represents a significant improvement in speed over the 156. Also, the OP-16 has all the DC features of the OP-15.

The OP-17 has a slew rate of 60V/ μ s and is the best choice for applications requiring high closed-loop gain with high speed. Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell amplifiers.

See the OP-215 data sheet for a dual configuration of the OP-15.

SIMPLIFIED SCHEMATIC





ORDERING INFORMATION†

T _A = 25° C V _{OS} MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	8-PIN HERMETIC DIP	
0.5	OP15AJ* OP16AJ* OP17AJ*	OP15AZ* OP16AZ* OP17AZ*	MIL
0.5	OP15EJ OP16EJ OP17EJ	OP15EZ OP16EZ OP17EZ	COM
1.0	OP15BJ* OP16BJ* OP17BJ*	OP15BZ* OP16BZ* OP17BZ*	MIL
1.0	OP15FJ OP16FJ OP17FJ	OP15FZ OP16FZ OP17FZ	COM
3.0	OP15CJ* OP16CJ* OP17CJ*	OP15CZ* OP16CZ* OP17CZ*	MIL
3.0	OP15GJ OP16GJ OP17GJ	OP15GZ OP16GZ OP17GZ	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage

All Devices Except C, G (Packaged) & GR Grades .. ±22V
 C, G (Packaged) & GR Grades ±18V
 Internal Power Dissipation (Note 1) 500mW

Operating Temperature

A, B, & C Grades -55° C to +125° C
 E, F & G Grades 0° C to +70° C

Maximum Junction Temperature +150° C

DICE Junction Temperature (T_j) -65° C to +150° C

Differential Input Voltage

All Devices Except C, G (Packaged) & GR Grades .. ±40V
 C, G (Packaged) & GR Grades ±30V

Input Voltage (Note 3)

All Devices Except C, G (Packaged) & GR Grades .. ±20V
 C, G (Packaged) & GR Grades ±16V

Input Voltage

OP-15A, OP-15B, OP-15E, OP-15F ±20V
 OP-15C, OP-15G ±16V
 OP-16A, OP-16B, OP-16E, OP-16F ±20V
 OP-16C, OP-16G ±16V
 OP-17A, OP-17B, OP-17E, OP-17F ±20V
 OP-17C, OP-17G ±16V

Output Short-Circuit Duration Indefinite

Storage Temperature Range -65° C to +150° C

Lead Temperature Range (Soldering, 60 sec) +300° C

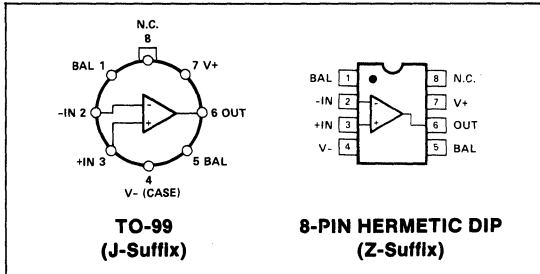
NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
Hermetic 8-Pin Dip (Z)	75° C	6.7mW/° C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power-supply voltage.

PIN CONNECTIONS



**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15A/E OP-16A/E OP-17A/E			OP-15B/F OP-16B/F OP-17B/F			OP-15C/G OP-16C/G OP-17C/G			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.2	0.5	—	0.4	1.0	—	0.5	3.0	mV	
Input Offset Current	I_{OS}	$T_J = 25^\circ C$ (Note 1) Device Operating	OP-15	—	3	10	—	6	20	—	12	50	pA
		$T_J = 25^\circ C$ (Note 1) Device Operating	OP-016/OP-17	—	3	10	—	6	20	—	12	50	
		$T_J = 25^\circ C$ (Note 1) Device Operating	OP-016/OP-17	—	5	25	—	10	50	—	20	125	
Input Bias Current	I_B	$T_J = 25^\circ C$ (Note 1) Device Operating	OP-15	—	± 15	± 50	—	± 30	± 100	—	± 60	± 200	pA
		$T_J = 25^\circ C$ (Note 1) Device Operating	OP-16/OP-17	—	± 18	± 110	—	± 40	± 200	—	± 80	± 400	
		$T_J = 25^\circ C$ (Note 1) Device Operating	OP-16/OP-17	—	± 15	± 50	—	± 30	± 100	—	± 60	± 200	
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	240	—	75	220	—	50	200	—	V/mV	
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V	
Supply Current	I_{SY}		OP-15	—	2.7	4.0	—	2.7	4.0	—	2.8	5.0	mA
			OP-16/OP-17	—	4.6	7.0	—	4.6	7.0	—	4.8	8.0	
Slew Rate	SR	$A_{VCL} = +1$ (Note 3)	OP-15	10	13	—	7.5	11	—	5	9	—	V/ μs
		$A_{VCL} = +1$ (Note 3)	OP-16	18	25	—	12	21	—	9	17	—	
		$A_{VCL} = +5$ (Note 3)	OP-17	45	60	—	35	50	—	25	40	—	
Gain Bandwidth Product	GBW	(Note 3)	OP-15	4.0	6.0	—	3.5	5.7	—	3.0	5.4	—	MHz
			OP-16	6.0	8.0	—	5.5	7.6	—	5.0	7.2	—	
			OP-17	20	30	—	15	28	—	11	26	—	
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	—	14	—	—	13	—	—	12	—	MHz
		$A_{VCL} = +1$	OP-16	—	19	—	—	18	—	—	17	—	
		$A_{VCL} = +5$	OP-17	—	11	—	—	10	—	—	9	—	
Settling Time	t_S	to 0.01%	OP-15	—	4.5	—	—	4.5	—	—	4.7	—	μs
		to 0.05% (Note 2)	OP-15	—	1.5	—	—	1.5	—	—	1.6	—	
		to 0.10%	OP-15	—	1.2	—	—	1.2	—	—	1.3	—	
		to 0.01%	OP-16	—	3.8	—	—	3.8	—	—	4.0	—	
		to 0.05% (Note 2)	OP-16	—	1.2	—	—	1.2	—	—	1.3	—	
		to 0.10%	OP-16	—	0.9	—	—	0.9	—	—	1.0	—	
Settling Time	t_S	to 0.01%	OP-17	—	1.5	—	—	1.5	—	—	1.6	—	μs
		to 0.05% (Note 4)	OP-17	—	0.7	—	—	0.7	—	—	0.8	—	
		to 0.10%	OP-17	—	0.6	—	—	0.6	—	—	0.7	—	
Input Voltage Range	IVR		± 10.5	—	—	± 10.5	—	—	± 10.3	—	—	V	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.5V$ $V_{CM} = \pm 10.3V$	86	100	—	86	100	—	—	—	—	dB	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$ $V_S = \pm 10V$ to $\pm 15V$	—	10	51	—	10	51	—	—	80	$\mu V/V$	
Input Noise Voltage Density	e_n	$f_O = 100Hz$ $f_O = 1000Hz$	—	20	—	—	20	—	—	20	—	nV/\sqrt{Hz}	
Input Noise Current Density	i_n	$f_O = 100Hz$ $f_O = 1000Hz$	—	0.01	—	—	0.01	—	—	0.01	—	pA/\sqrt{Hz}	
Input Capacitance	C_{IN}		—	3	—	—	3	—	—	3	—	pF	

NOTES:

- Input bias current is specified for two different conditions. The $T_J = 25^\circ C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at $25^\circ C$ ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_J and I_B vs T_A . PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Settling time is defined here for a unity gain inverter connection using $2k\Omega$ resistors. It is the time required for the error voltage (the voltage at the

inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.

- Sample tested.
- Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15A OP-16A OP-17A			OP-15B OP-16B OP-17B			OP-15C OP-16C OP-17C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.4	0.9	—	0.7	2.0	—	0.9	4.5	mV	
Average Input Offset Voltage Drift (Note 2)													
Without External Trim	TCV_{OS}		—	2	5	—	3	10	—	4	15	$\mu V/^\circ C$	
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	2	—	—	3	—	—	4	—		
Input Offset Current (Note 1)	I_{OS}	$T_j = 125^\circ C$	OP-15	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
		$T_A = 125^\circ C$		—	0.8	7.0	—	1.2	11	—	1.5	17	
		Device Operating		—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	
		Device Operating		—	1.0	8.5	—	1.3	14.5	—	1.7	22	
Input Bias Current (Note 1)	I_B	$T_j = 125^\circ C$	OP-15	—	± 1.2	± 5.0	—	± 1.5	± 7.5	—	± 1.8	± 10	nA
		$T_A = 125^\circ C$		—	± 1.7	± 9.0	—	± 2.2	± 14	—	± 2.7	± 19	
		Device Operating		—	± 1.2	± 5.0	—	± 1.5	± 7.5	—	± 1.8	± 10	
		Device Operating		—	± 2.0	± 11	—	± 2.5	± 18	—	± 3.0	± 25	
Input Voltage Range	IVR		± 10.4	—	—	± 10.4	—	—	± 10.25	—	—	V	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$	85	97	—	85	97	—	—	—	—	dB	
		$V_{CM} = \pm 10.25V$	—	—	—	—	—	—	80	93	—		
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	15	57	—	15	57	—	—	—	$\mu V/V$	
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	23	100		
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	35	120	—	30	110	—	25	100	—	V/mV	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V	

NOTES:

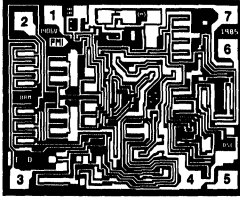
- Input bias current is specified for two different conditions. The $T_j = 25^\circ C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at $25^\circ C$ ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A . PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Sample tested.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15E OP-16E OP-17E			OP-15F OP-16F OP-17F			OP-15G OP-16G OP-17G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.3	0.75	—	0.55	1.5	—	0.7	3.8	mV
Average Input												
Offset Voltage Drift												
(Note 2)												
Without External Trim	TCV_{OS}		—	2	5	—	3	10	—	4	15	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	2	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = 70^\circ C$	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = 70^\circ C$	—	0.06	0.55	—	0.08	0.80	—	0.10	1.2	
		Device Operating	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	
		Device Operating	—	0.07	0.70	—	0.10	1.1	—	0.15	1.7	
Input Bias Current (Note 1)	I_B	$T_J = 70^\circ C$	—	± 0.10	± 0.40	—	± 0.12	± 0.60	—	± 0.14	± 0.80	nA
		$T_A = 70^\circ C$	—	± 0.13	± 0.75	—	± 0.16	± 1.1	—	± 0.19	± 1.5	
		Device Operating	—	± 0.10	± 0.40	—	± 0.12	± 0.60	—	± 0.14	± 0.80	
		Device Operating	—	± 0.15	± 0.90	—	± 0.20	± 1.4	—	± 0.25	± 2.0	
Input Voltage Range	IVR		± 10.4	—	—	± 10.4	—	—	± 10.25	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$	85	98	—	85	98	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$	—	—	—	—	—	—	80	94	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	13	57	—	13	57	—	—	—	$\mu V/V$
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	20	100	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	65	200	—	50	180	—	35	160	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

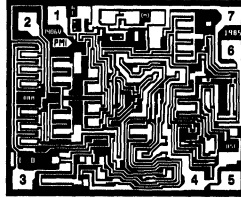
NOTES:

- Input bias current is specified for two different conditions. The $T_J = 25^\circ C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at $25^\circ C$ ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_J and I_B vs T_A . PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)
OP-15


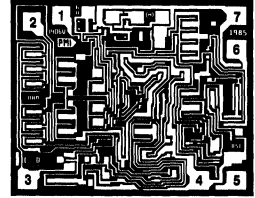
DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils
(1.73 × 1.42mm, 2.46 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
5. BALANCE
6. OUTPUT
7. V+

OP-16


DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils
(1.73 × 1.42mm, 2.46 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
5. BALANCE
6. OUTPUT
7. V+

OP-17


DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils
(1.73 × 1.42mm, 2.46 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
5. BALANCE
6. OUTPUT
7. V+

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-15/16/17N, OP-15/16/17G and OP-15/16/17GR devices; $T_A = 125^\circ C$ for OP-15/16/17NT and OP-15/16/17GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15NT	OP-15N	OP-15GT	OP-15G	OP-15GR	UNITS
			OP-16NT	OP-16N	OP-16GT	OP-16G	OP-16GR	
			LIMIT	LIMIT	LIMIT	LIMIT	LIMIT	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	0.9	0.5	2.0	1.0	3.0	mV MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 2k\Omega$	35	100	30	75	50	V/mV MIN
Input Voltage Range	IVR		± 10.4	± 10.5	± 10.4	± 10.5	± 10.3	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	86	85	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$ $V_S = \pm 10V$ to $\pm 15V$	57	51	57	51	—	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12 —	± 12 ± 11	± 12 —	± 12 ± 11	± 12 ± 11	V MIN
Supply Current	I_{SV}	OP-15 OP-16, OP-17	— —	4 7	— —	4 7	5 8	mA MAX
Input Bias Current	I_B	OP-15 OP-16, OP-17	± 9 ± 11	— —	± 14 ± 18	— —	— —	nA MAX
Input Offset Current	I_{OS}	OP-15 OP-16, OP-17	7.0 8.5	— —	11.0 14.5	— —	— —	nA MAX

NOTES:

For 25°C characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

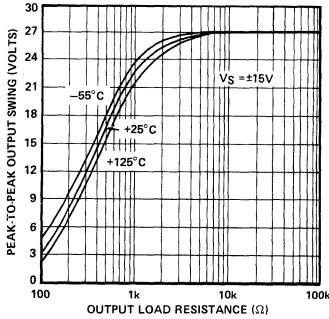
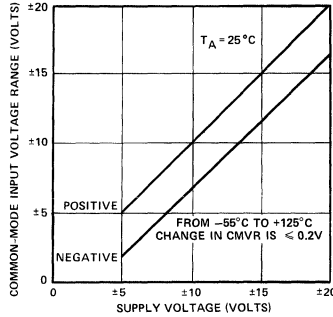
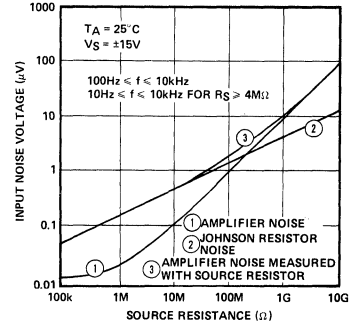
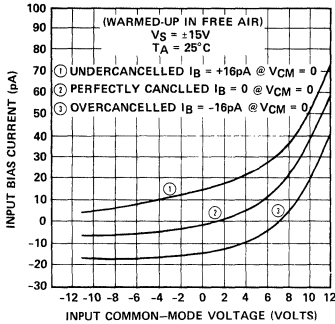
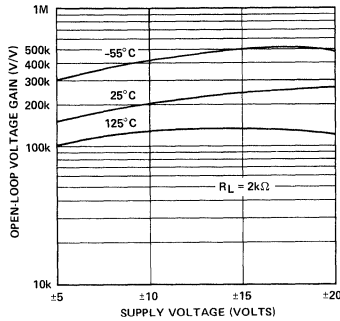
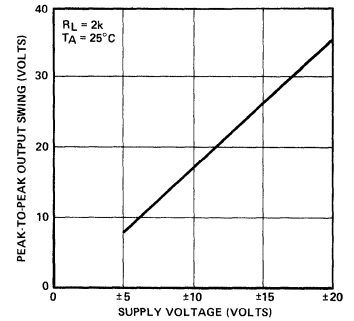
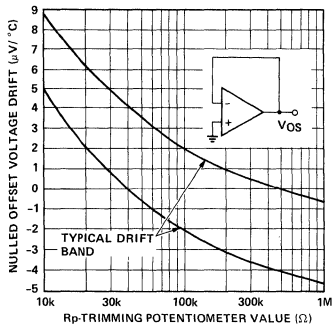
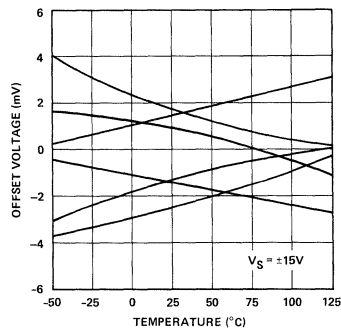
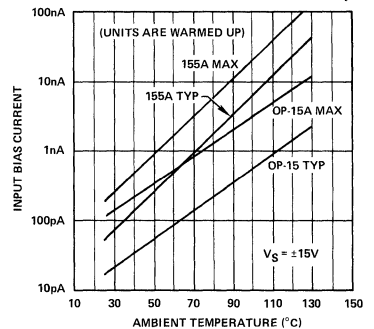
PARAMETER	SYMBOL	CONDITIONS	OP-15NT	OP-15N	OP-15GT	OP-15G	OP-15GR	UNITS	
			OP-16NT OP-17NT TYPICAL	OP-16N OP-17N TYPICAL	OP-16GT OP-17GT TYPICAL	OP-16G OP-17G TYPICAL	OP-16GR OP-17GR TYPICAL		
Average Input Offset Drift Unnullled	TCV_{OS}		2	2	3	3	4	$\mu V/^\circ C$	
Average Input Offset Drift Nullled	TCV_{OSn}	$R_P = 100k\Omega$	2	2	3	3	4	$\mu V/^\circ C$	
Input Offset Current	I_{OS}		3	3	3	3	3	pA	
Input Bias Current	I_B		± 15	± 15	± 15	± 15	± 15	pA	
Slew Rate	SR	$A_{VCL} = +1$	OP-15	13	13	11	11	9	$V/\mu s$
			OP-16	25	25	21	21	17	
		$A_{VCL} = +5$	OP-17	60	60	50	50	40	
Settling Time (see settling time test circuits)	t_s	to 0.01%	OP-15	4.5	4.5	4.5	4.5	4.7	μs
			OP-16	1.5	1.5	1.5	1.5	1.6	
			OP-17	1.2	1.2	1.2	1.2	1.3	
		to 0.05%	OP-15	1.5	1.5	1.5	1.5	1.6	
			OP-16	1.2	1.2	1.2	1.2	1.3	
			OP-17	0.9	0.9	0.9	0.9	1.0	
to 0.10%	OP-15	1.5	1.5	1.5	1.5	1.6			
	OP-16	0.7	0.7	0.7	0.7	0.8			
	OP-17	0.6	0.6	0.6	0.6	0.7			
Gain Bandwidth Product	GBW		OP-15	6.0	6.0	5.7	5.7	5.4	MHz
			OP-16	8.0	8.0	7.6	7.6	7.2	
			OP-17	30	30	28	28	26	
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	14	14	13	13	12	MHz
			OP-16	19	19	18	18	17	
		$A_{VCL} = +5$	OP-17	11	11	10	10	9	
Input Noise Voltage Density	e_n	$f = 100Hz$		20	20	20	20	20	nV/\sqrt{Hz}
		$f = 1000Hz$		15	15	15	15	15	
Input Noise Current Density	i_n	$f = 100Hz$		0.01	0.01	0.01	0.01	0.01	pA/\sqrt{Hz}
		$f = 1000Hz$		0.01	0.01	0.01	0.01	0.01	
Input Capacitance	C_{IN}		3	3	3	3	3	pF	

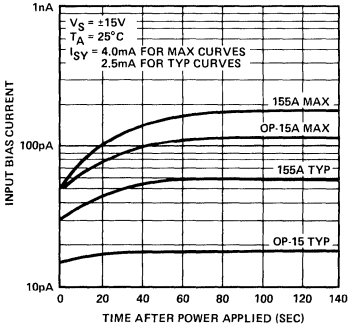
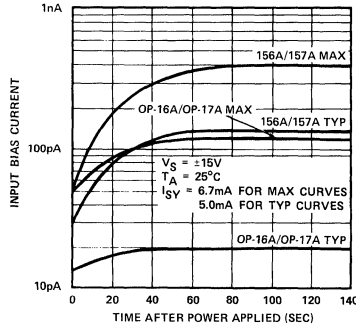
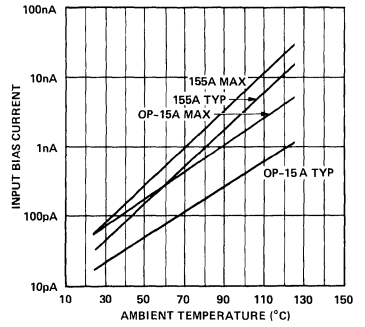
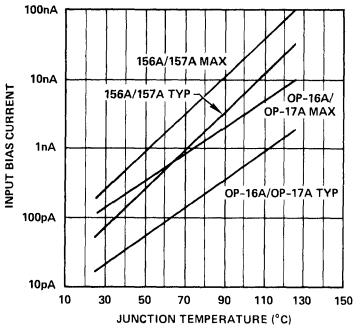
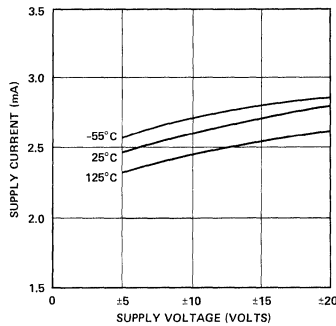
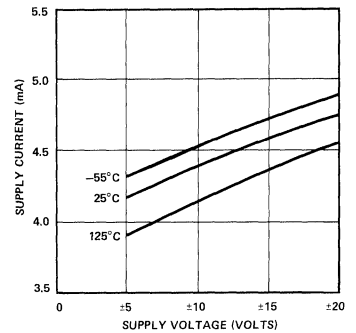
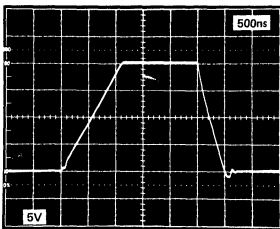
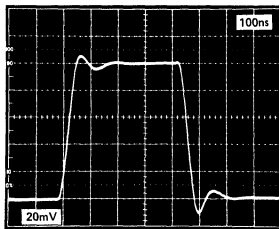
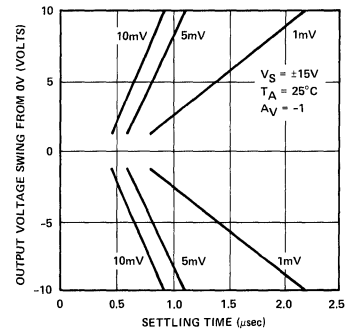
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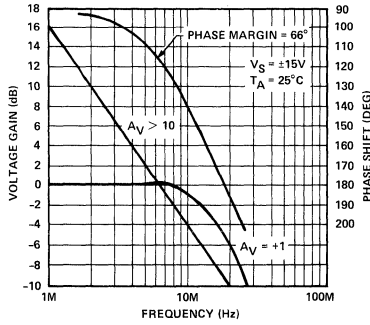
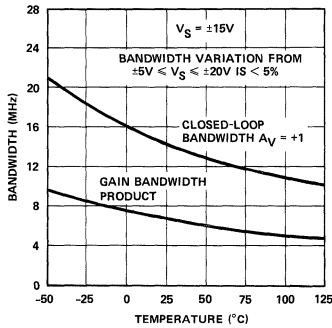
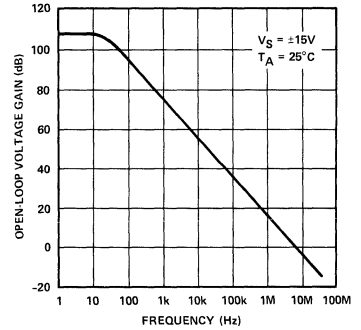
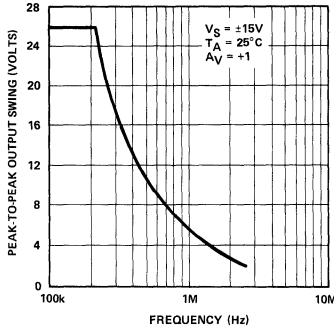
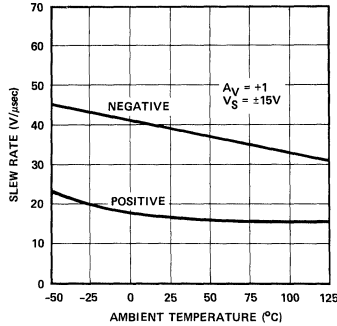
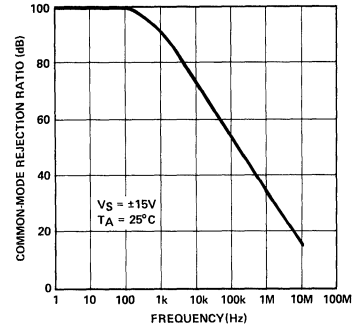
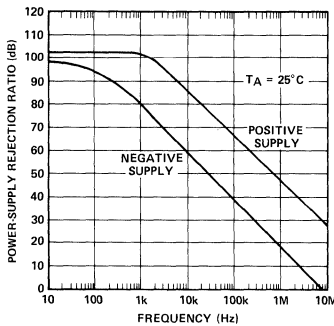
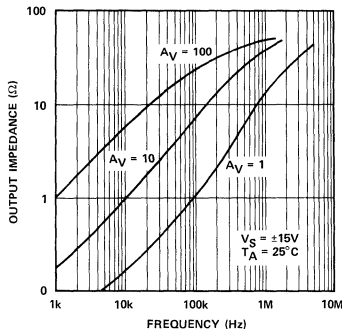
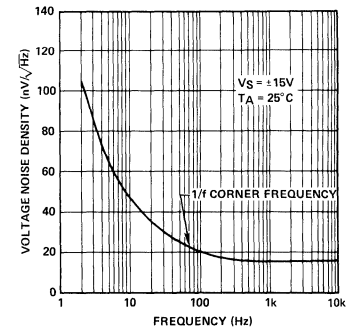
For $25^\circ C$ characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

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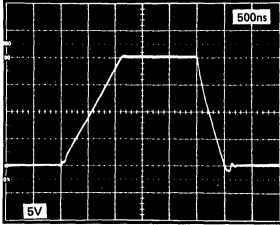
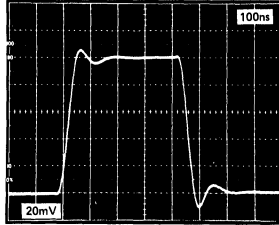
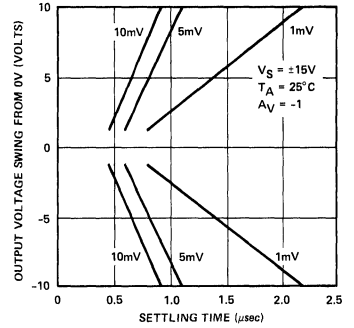
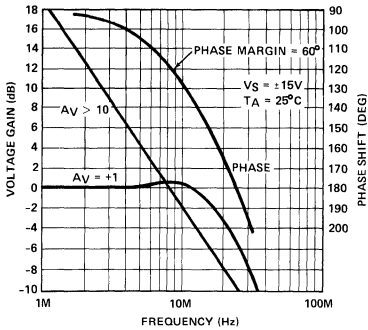
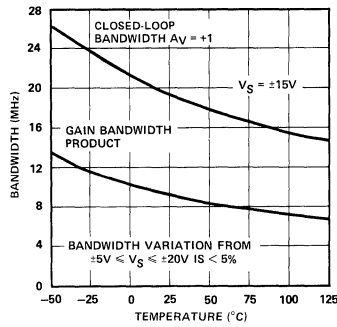
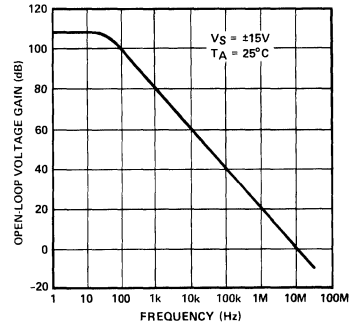
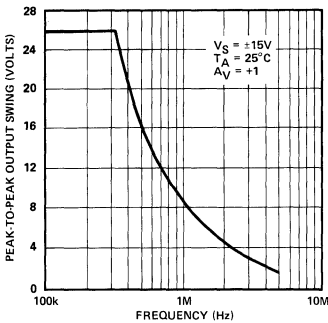
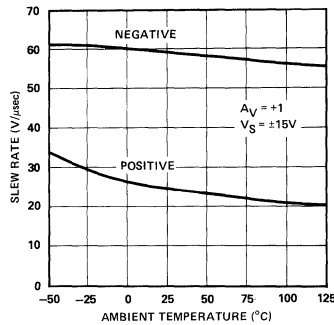
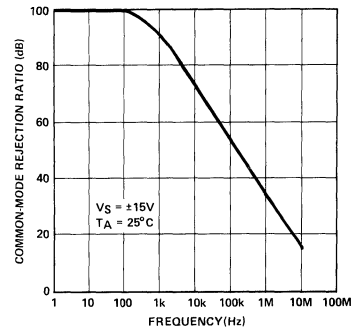
OPERATIONAL AMPLIFIERS

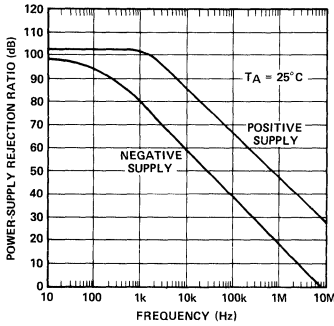
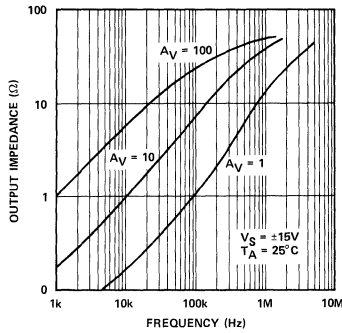
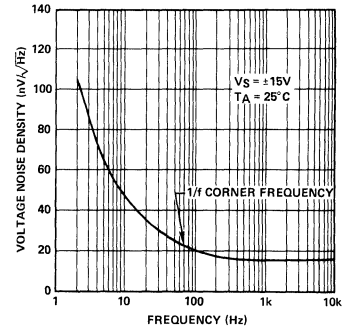
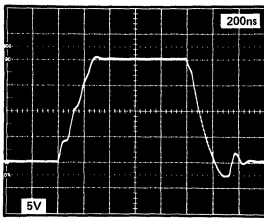
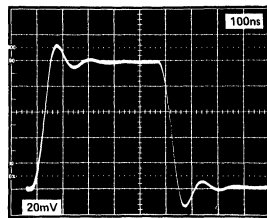
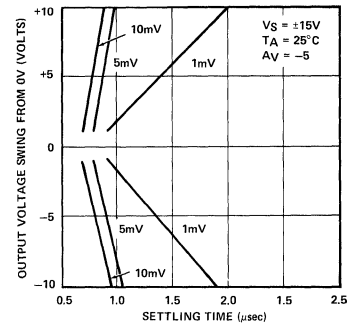
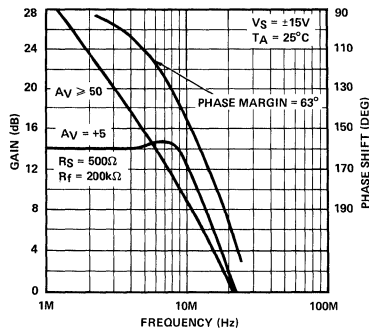
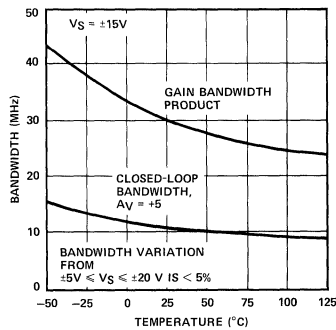
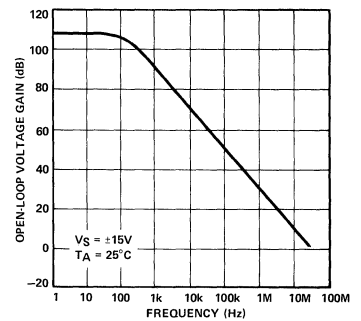
TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)
MAXIMUM OUTPUT SWING vs LOAD RESISTANCE

COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

VOLTAGE NOISE vs SOURCE RESISTANCE

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

NULLED OFFSET VOLTAGE DRIFT vs POTENTIOMETER SIZE

OFFSET VOLTAGE DRIFT vs TEMPERATURE OF REPRESENTATIVE UNITS

INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR)


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)
**BIAS CURRENT vs TIME
IN FREE AIR
(OP-15)**

**BIAS CURRENT vs TIME
IN FREE AIR
(OP-16/OP-17)**

**INPUT BIAS CURRENT vs
AMBIENT TEMPERATURE (UNITS
ARE WARMED-UP IN FREE AIR)
(OP-15)**

**INPUT BIAS CURRENT vs
AMBIENT TEMPERATURE (UNITS
ARE WARMED-UP IN FREE AIR)
(OP-16/OP-17)**

**SUPPLY CURRENT
vs SUPPLY VOLTAGE
(OP-15)**

**SUPPLY CURRENT
vs SUPPLY VOLTAGE
(OP-16/OP-17)**

TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)
**LARGE-SIGNAL
TRANSIENT RESPONSE**

**SMALL-SIGNAL
TRANSIENT RESPONSE**

SETTLING TIME


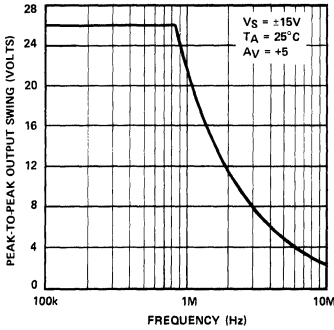
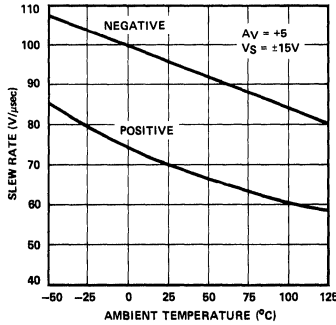
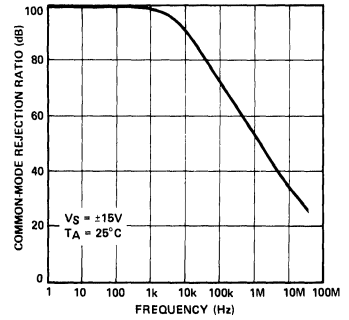
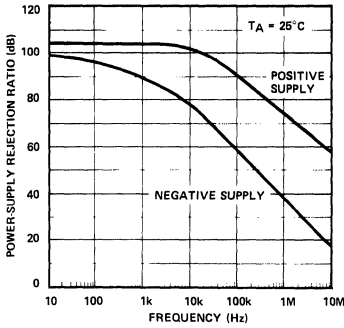
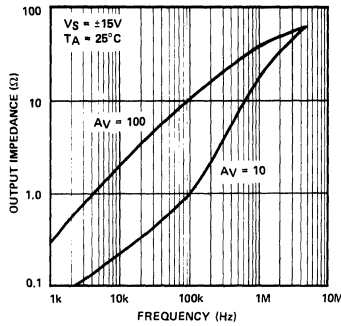
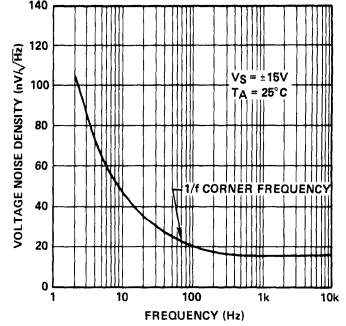
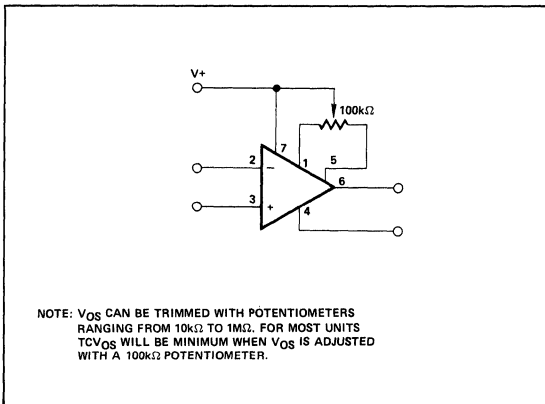
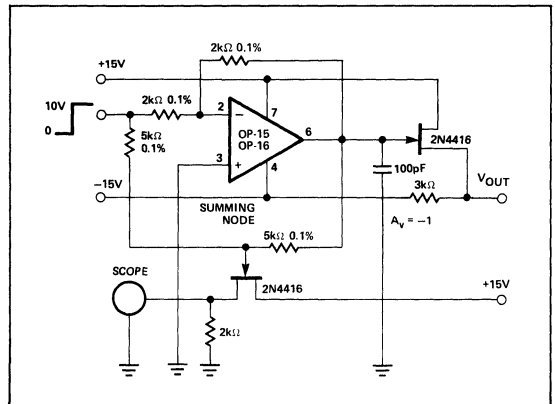
TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY

BANDWIDTH vs TEMPERATURE

OPEN-LOOP GAIN vs FREQUENCY

MAXIMUM OUTPUT SWING vs FREQUENCY

SLEW RATE vs TEMPERATURE

COMMON-MODE REJECTION RATIO vs FREQUENCY

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

OUTPUT IMPEDANCE vs FREQUENCY

VOLTAGE NOISE DENSITY vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)

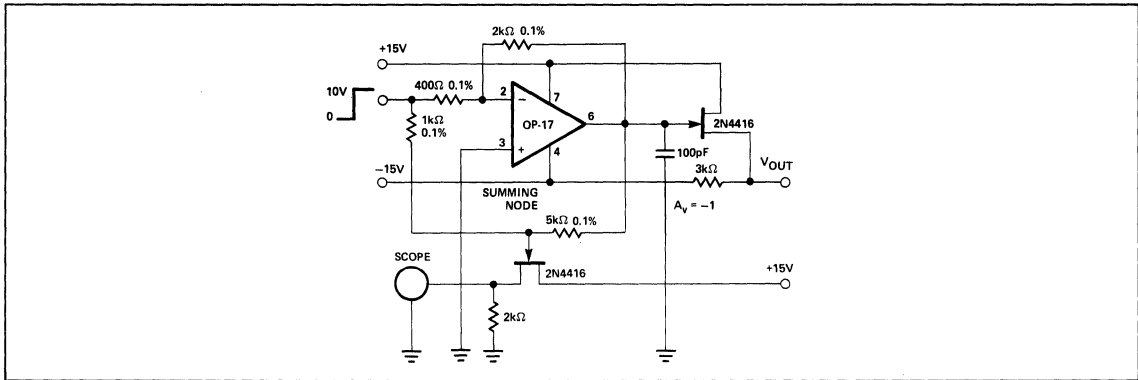
**LARGE-SIGNAL
TRANSIENT RESPONSE**

**SMALL-SIGNAL
TRANSIENT RESPONSE**

SETTLING TIME

**CLOSED-LOOP BANDWIDTH
AND PHASE SHIFT
vs FREQUENCY**

**BANDWIDTH vs
TEMPERATURE**

**OPEN-LOOP GAIN
vs FREQUENCY**

**MAXIMUM OUTPUT SWING
vs FREQUENCY**

**SLEW RATE
vs TEMPERATURE**

**COMMON-MODE REJECTION
RATIO vs FREQUENCY**


TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)
POWER-SUPPLY REJECTION RATIO vs FREQUENCY

OUTPUT IMPEDANCE vs FREQUENCY

VOLTAGE NOISE DENSITY vs FREQUENCY

TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)
LARGE-SIGNAL TRANSIENT RESPONSE

SMALL-SIGNAL TRANSIENT RESPONSE

SETTLING TIME

CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY

BANDWIDTH vs TEMPERATURE

OPEN-LOOP FREQUENCY RESPONSE


TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)

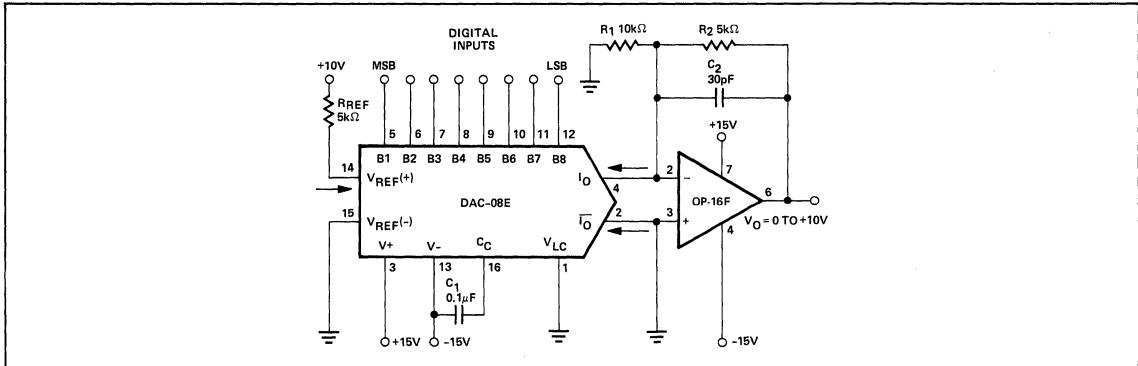
MAXIMUM OUTPUT SWING vs FREQUENCY

SLEW RATE vs TEMPERATURE

COMMON-MODE REJECTION RATIO vs FREQUENCY

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

OUTPUT IMPEDANCE vs FREQUENCY

VOLTAGE NOISE vs FREQUENCY

BASIC CONNECTIONS
INPUT OFFSET VOLTAGE NULLING

SETTLING-TIME TEST CIRCUIT — OP-15/OP-16

 5
 OPERATIONAL AMPLIFIERS

SETTLING-TIME TEST CIRCUIT — OP-17



TYPICAL APPLICATIONS

CURRENT-TO-VOLTAGE AMPLIFIER OUTPUT



APPLICATIONS INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance

from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time-constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback pole time constant.



OP-20

MICROPOWER OPERATIONAL AMPLIFIER (SINGLE OR DUAL SUPPLY)

Precision Monolithics Inc.

FEATURES

- Low Supply Current 55µA Max
- Single-Supply Operation +5V to +30V
- Dual-Supply Operation ±2.5V to ±15V
- Low Input Offset Voltage 250µV Max
- Low Input Offset Voltage Drift 1.5µV/°C Max
- High Common-Mode Input Range ... V- to V+ (-1.5V)
- High CMRR and PSRR 100dB Min
- High Open-Loop Gain 120dB Min
- No External Components Required
- 741 Pinout and Nulling

ORDERING INFORMATION†

T _A = 25° C V _{OS} MAX (µV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	
250	OP20BJ*	OP20BZ*		MIL
250	OP20FJ	OP20FZ		IND
250			OP20FP	COM
500	OP20CJ*	OP20CZ*		MIL
500	OP20GJ	OP20GZ		IND
500			OP20GP	COM
1000	OP20HJ	OP20HZ	OP20HP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

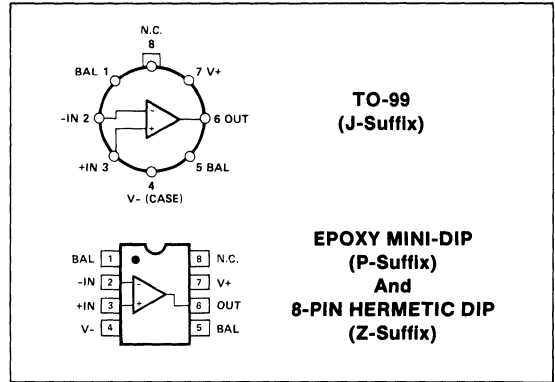
GENERAL DESCRIPTION

The OP-20 is a monolithic micropower operational amplifier that can be operated from a single power supply of +5V to

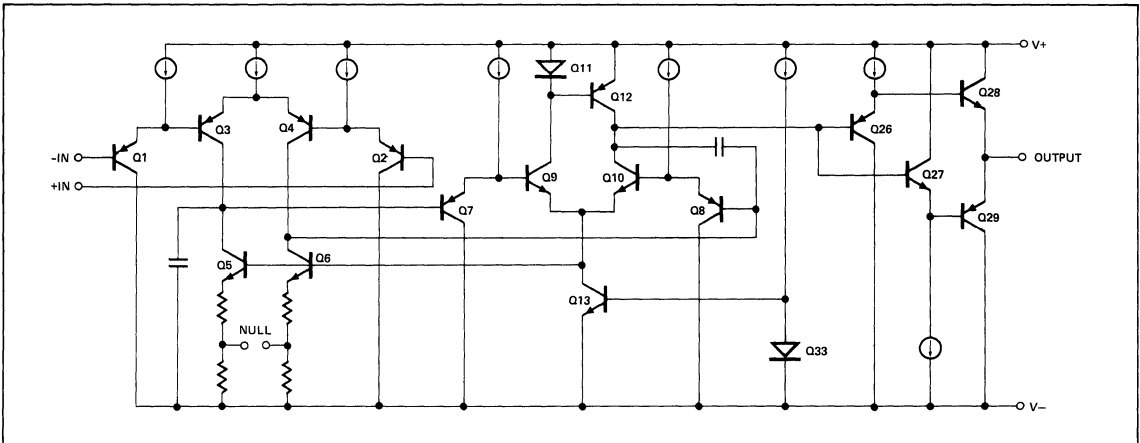
+30V, or from dual supplies of ±2.5V to ±15V. The input voltage range extends to the negative rail, therefore input signals down to zero volts can be accommodated when operating from a single supply.

Precision performance in high-gain applications is readily obtained when using the OP-20. The B/F grade features a maximum input offset voltage of 250µV, minimum CMRR of 95dB, and open-loop gain of over 500,000. Quiescent supply current is a maximum of only 55µA at ±2.5V or 80µA at ±15V. The low input offset, high gain, and low power consumption brings precision performance to portable instruments, satellites, missile control systems, and many other battery-powered applications.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



5 OPERATIONAL AMPLIFIERS

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	±18V
Power Dissipation	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J and Z Packages	-65° C to +150° C
P Package	-65° C to +125° C

Operating Temperature Range

OP-20B, OP-20C (J or Z package)	... -55° C to +125° C
OP-20F, OP-20G (J or Z package) -25° C to +85° C
OP-20FP, OP-20GP, OP-20HP	
OP-20HJ, OP-20HZ 0° C to +70° C
Lead Temperature Range (Soldering, 60 sec) 300° C
DICE Junction Temperature -65° C to +150° C

NOTE:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-20B/F			OP-20C/G			OP-20H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	55	250	—	150	500	—	300	1000	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.15	1.5	—	0.2	2.5	—	0.3	4.0	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	25	—	14	30	—	16	40	nA
Input Voltage Range	IVR	$V^+ = +5V, V^- = 0V$	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	-15/13.5	—	—	-15/13.5	—	—	-15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	$V^+ = +5V, V^- = 0V$ $0V \leq V_{CM} \leq 3.5V$	95	105	—	90	95	—	85	90	—	dB
		$V_S = \pm 15V$ $-15V \leq V_{CM} \leq 13.5V$	100	110	—	94	105	—	90	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and $V^- = 0V$, $V^+ = 5V$ to $30V$	—	4	6	—	6	10	—	10	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V^+ = +5V, V^- = 0V$ $1V \leq V_O \leq 3.5V$	300	500	—	200	500	—	—	500	—	V/mV
		$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 25k\Omega$	1000	2000	—	800	2000	—	500	1000	—	
Output Voltage Swing	V_O	$V^+ = 5V, V^- = 0V$ $R_L = 10k\Omega$	0.6/4.1	—	—	0.7/4.1	—	—	0.8/4.0	—	—	V
		$V_S = \pm 15V$, $R_L = 25k\Omega$	±14.1	—	—	±14.1	—	—	±14.0	—	—	
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	—	100	—	—	100	—	—	100	—	kHz
Slew Rate	SR	$V_S = \pm 15V$ $R_L = 25k\Omega$	—	0.05	—	—	0.05	—	—	0.05	—	V/ μs
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	40	55	—	44	63	—	45	70	μA
		$V_S = \pm 15V$, No Load	—	55	80	—	57	85	—	60	95	



ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-20BJ/BZ and OP-20CJ/CZ, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-20FJ/FZ and OP-20GJ/GZ, and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-20FP, OP-20GP, OP-20HP, OP-20HZ and OP-20HJ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-20B/F			OP-20C/G			OP-20H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnull'd	—	0.75	1.5	—	1.0	3.0	—	1.5	7.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	155	400	—	250	800	—	500	1700	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	2.5	—	1.0	3.5	—	1.5	5.0	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	27	—	14	33	—	16	45	nA
Input Voltage Range	IVR	$V_+ = +5V, V_- = 0V$ $V_S = \pm 15V$	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_+ = +5V, V_- = 0V$ $0V \leq V_{CM} \leq 3.2V$ $V_S = \pm 15V$	90	100	—	85	90	—	80	85	—	dB
		$-15V \leq V_{CM} \leq 13.2V$	96	110	—	90	105	—	85	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	4	10	—	6	18	—	10	32	$\mu V/V$
		$V_- = 0V,$ $V_+ = 5V$ to $30V$	—	4	10	—	6	18	—	10	57	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 50k\Omega$	500	700	—	400	600	—	250	400	—	V/mV
Output Voltage Swing	V_O	$V_+ = 5V, V_- = 0V,$ $R_L = 50k\Omega$	0.8/4.0	—	—	0.9/3.9	—	—	1.0/3.8	—	—	V
		$V_S = \pm 15V,$ $R_L = 50k\Omega$	± 14.0	—	—	± 13.9	—	—	± 13.9	—	—	
Supply Current	I_{SY}	$V_S = \pm 2.5V,$ No Load or $+5V, 0V$	—	50	65	—	53	75	—	55	85	μA
		$V_S = \pm 15V,$ No Load	—	64	95	—	68	100	—	72	115	

NOTE:

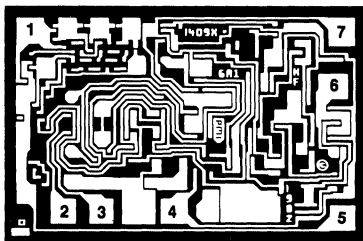
1. Sample tested.

5

OPERATIONAL AMPLIFIERS



DICE CHARACTERISTICS



DIE SIZE 0.068 × 0.045 Inch, 3060 sq. mils
(1.73 × 1.14 mm, 1.97 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
5. BALANCE
6. OUTPUT
7. V+

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

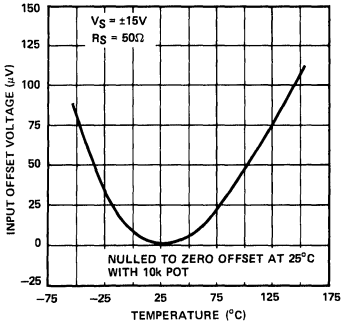
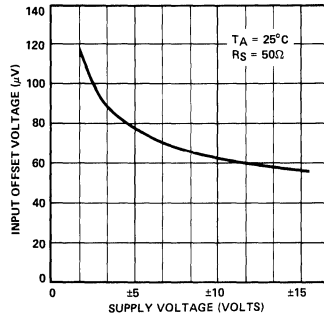
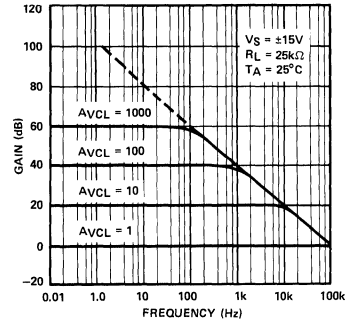
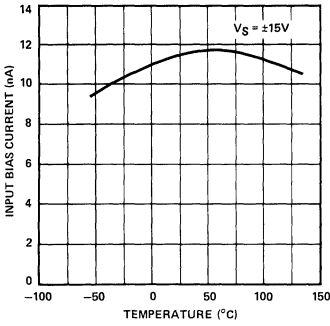
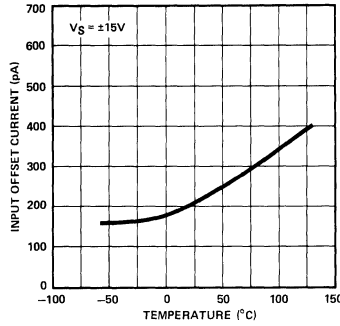
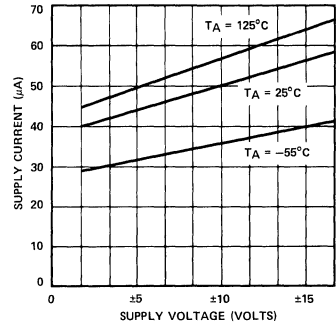
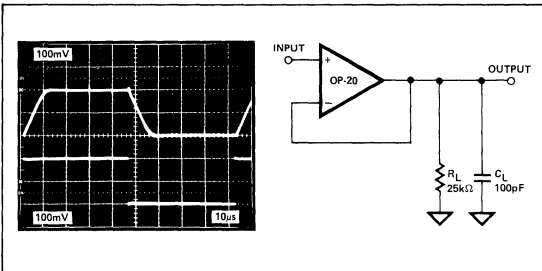
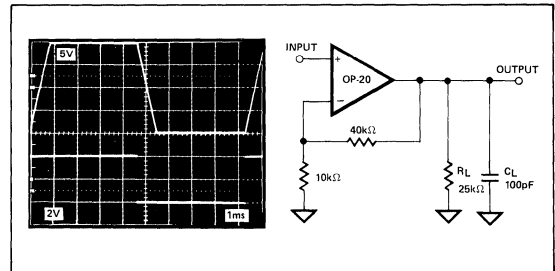
PARAMETER	SYMBOL	CONDITIONS	OP-20N LIMIT	OP-20G LIMIT	OP-20GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	600	1000	μV MAX
Input Offset Current	I_{OS}		1.5	2.5	4.0	nA MAX
Input Bias Current	I_B		25	30	40	nA MAX
Input Voltage Range	IVR	$V_+ = +5V, V_- = 0V$ $V_S = \pm 15V$	0/3.5 -15/13.5	0/3.5 -15/13.5	0/3.5 -15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_+ = +5V, V_- = 0V, 0V \leq V_{CM} \leq +3.5V$ $V_S = \pm 15V, -15V \leq V_{CM} \leq +13.5V$	95 100	90 94	85 90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V_- = 0V, V_+ = +5V$ to $+30V$	6	10	32	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$ $V_O = \pm 10V$	1000	800	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega, V_+ = +5V, V_- = 0V$ $R_L = 25k\Omega, V_S = \pm 15V$	0.7/4.1 ± 14.1	0.8/4.1 ± 14.1	0.9/4.0 ± 14.0	V MIN
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	55 80	63 85	70 95	μA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

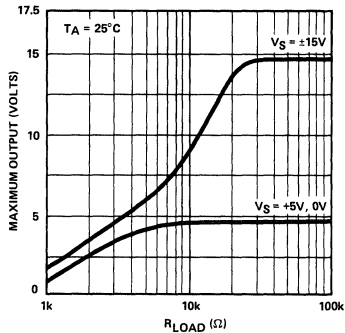
PARAMETER	SYMBOL	CONDITIONS	OP-20N TYPICAL	OP-20G TYPICAL	OP-20GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} TCV_{OSn}	Unnulled Nulled, $R_P = 10k\Omega$	1.0 1.0	1.5 1.5	2.5 2.5	$\mu V/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	2000	1000	V/mV

TYPICAL PERFORMANCE CHARACTERISTICS
TRIMMED OFFSET VOLTAGE vs TEMPERATURE

INPUT OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE

CLOSED-LOOP GAIN vs FREQUENCY

INPUT BIAS CURRENT vs TEMPERATURE

INPUT OFFSET CURRENT vs TEMPERATURE

SUPPLY CURRENT vs SUPPLY VOLTAGE

SMALL-SIGNAL TRANSIENT RESPONSE

LARGE-SIGNAL TRANSIENT RESPONSE


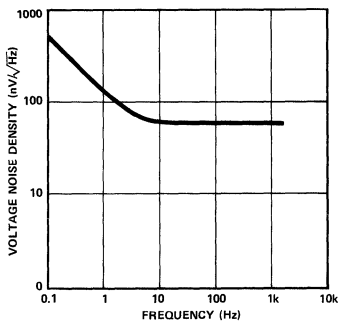


TYPICAL PERFORMANCE CHARACTERISTICS

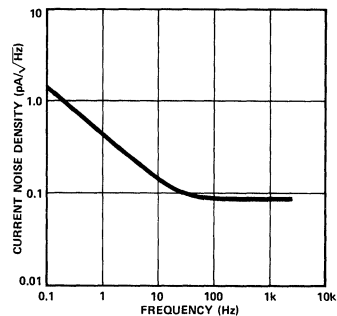
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



VOLTAGE NOISE DENSITY vs FREQUENCY

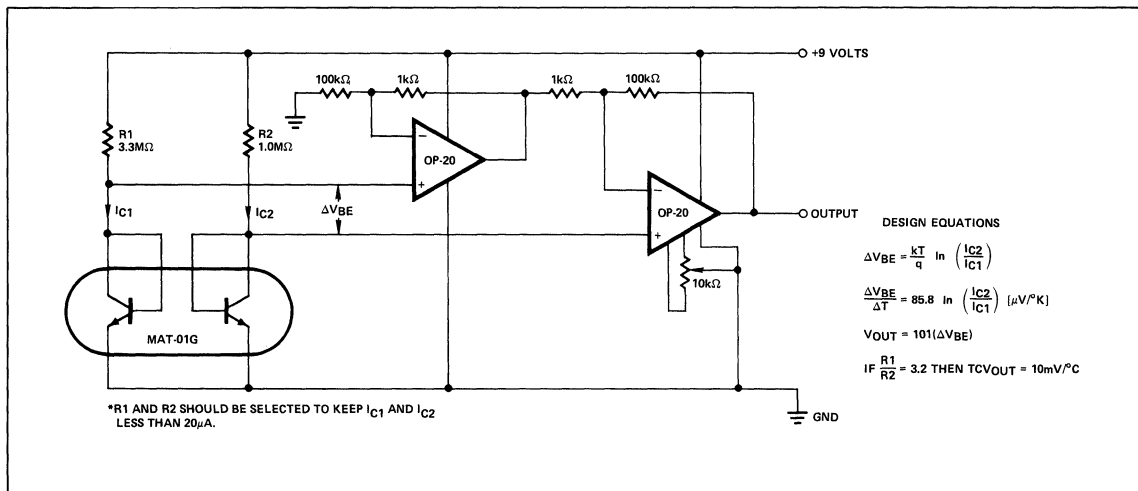


CURRENT NOISE DENSITY vs FREQUENCY



TYPICAL APPLICATIONS

TEMPERATURE SENSOR





OP-21

LOW-POWER
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Supply Current 230 μ A Max
- Wide Supply Range $\pm 2.5V$ to $\pm 15V$
- Low Input Offset Voltage 100 μ V Max
- Low Input Offset Voltage Drift 1.0 μ V/ $^{\circ}$ C Max
- High Common-Mode Input Range $V^- (+0.5V)$ to $V^+ (-1.5V)$
- High CMRR and PSRR 100dB Min
- High Open-Loop Gain 1000V/mV Min
- 125 $^{\circ}$ C Temperature Tested Dice

GENERAL DESCRIPTION

The OP-21 is a precision low-power operational amplifier offering the benefits of low offset voltage and high slew rate with the advantages of low power. A supply range of $\pm 2.5V$ to $\pm 15V$ allows a wide range of applications.

Two military temperature range models and three industrial temperature range models are available in TO-99 cans and 8-Pin hermetic DIPs. Industrial temperature range models are also available in 8-Pin epoxy DIPs. See OP-221 for dual and OP-421 for quad versions of the OP-21.

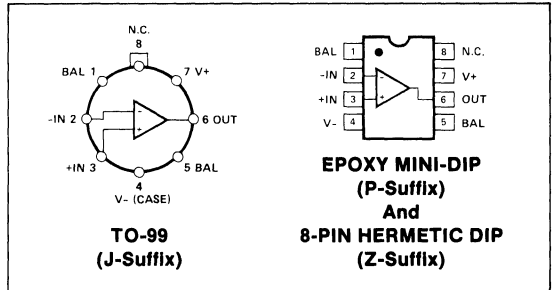
ORDERING INFORMATION†

T _A - 25 $^{\circ}$ C V _{OS} MAX (μ V)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC PLASTIC DIP 8-PIN	PLASTIC DIP 8-PIN	
100	OP21AJ*	OP21AZ*		MIL
100	OP21EJ	OP21EZ	OP21EP	IND
200	OP21BJ*	OP21BZ*		MIL
200	OP21FJ	OP21FZ	OP21FP	IND
500	OP21GJ	OP21GZ	OP21GP	IND

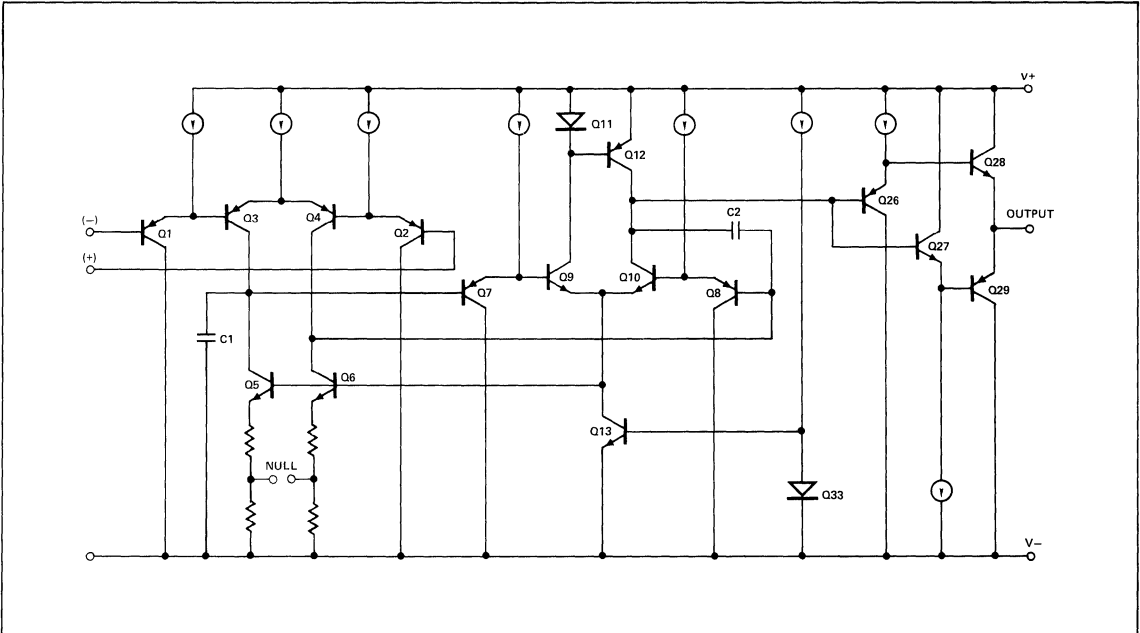
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



OPERATIONAL AMPLIFIERS

5



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J and Z Packages	-65°C to +125°C
P Package	-65°C to +125°C
Operating Temperature Range	
OP-21A, OP-21B	-55°C to +125°C
OP-21E, OP-21F, OP-21G	-25°C to +85°C

DICE Junction Temperature (T_J) -65°C to +150°C
 Lead Temperature Range (Soldering, 60 sec) 300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

ELECTRICAL CHARACTERISTICS at V_S = ±2.5V to ±15V and T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21A/E			OP-21B/F			OP-21G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	V _S = ±15V	—	40	100	—	150	200	—	300	500	μV
Input Offset Current	I _{OS}	V _{CM} = 0	—	0.6	4	—	0.8	5	—	1.2	6	nA
Input Bias Current	I _B	V _{CM} = 0	—	50	100	—	60	120	—	70	150	nA
Input Voltage Range	IVR	V _S = ±15V	-14.5/13.5	—	—	-14.5/13.5	—	—	-14.5/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	V _S = ±15V, No Load -14.5V ≤ V _{CM} ≤ 13.5V	100	110	—	90	105	—	84	100	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±2.5V to ±15V, No Load	—	2	6	—	4	10	—	10	32	μV/V
Large-Signal Voltage Gain	A _{VO}	V _S = ±15V, R _L = 10kΩ, V _O ±10V	1000	2000	—	500	1500	—	500	1000	—	V/mV
Output Voltage Swing	V _O	V _S = ±15V, R _L = 10kΩ	-13.7/14.0	—	—	-13.7/13.9	—	—	-13.6/13.8	—	—	V
Slew Rate	SR	C _L = 100pF, R _L = 25kΩ	—	0.25	—	—	0.25	—	—	0.25	—	V/μs
Closed-Loop Bandwidth	BW	A _{VCL} = +1, R _L = 10kΩ	—	600	—	—	600	—	—	600	—	kHz
Supply Current	I _{SY}	V _S = ±2.5V, No Load	—	170	230	—	180	275	—	190	300	μA
		V _S = ±15V, No Load	—	230	300	—	235	360	—	250	420	



ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-21A and OP-21B, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-21E, OP-21F and OP-21G, unless otherwise noted.

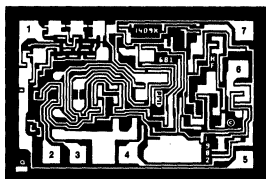
PARAMETER	SYMBOL	CONDITIONS	OP-21A/E			OP-21B/F			OP-21G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Notes 1, 2)	TCV_{OS}	Unnulled	—	0.5	1.0	—	1.0	2.0	—	2.5	5.0	$\mu V/^\circ C$
	TCV_{OSn}	Nulled	—	—	—	—	—	—	—	—	—	—
Input Offset Voltage	V_{OS}		—	75	200	—	200	500	—	500	1000	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.7	5	—	0.7	6	—	0.8	8	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	50	110	—	60	130	—	70	165	nA
Input Voltage Range	IVR		-14.3/13.2	—	—	-14.3/13.2	—	—	-14.3/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	No Load, $V_S = \pm 15V$, $-14.5V \leq V_{CM} \leq 13.2V$	96	105	—	86	100	—	80	95	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$, No Load	—	4	10	—	6	18	—	18	57	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 20k\Omega$, $V_O = \pm 10V$	500	1500	—	250	1300	—	250	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 20k\Omega$	-13.5/13.8	—	—	-13.5/13.7	—	—	-13.5/13.6	—	—	V
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	205	275	—	215	330	—	230	360	μA
		$V_S = \pm 15V$, No Load	—	275	360	—	285	430	—	300	500	

NOTE:

- Sample tested.
- TCV_{OSn} is guaranteed by unnullled TCV_{OS} and device design.

5

OPERATIONAL AMPLIFIERS

**DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)**

DIE SIZE 0.068 × 0.045 inch, 3060 sq. mils
(1.73 × 1.14 mm, 1.974 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V⁻
5. BALANCE
6. OUTPUT
7. V⁺

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-21N, OP-21G and OP-21GR devices; $T_A = 125^\circ C$ for OP-21NT and OP-21GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21NT LIMIT	OP-21N LIMIT	OP-21GT LIMIT	OP-21G LIMIT	OP-21GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	100	500	200	500	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	4	4	5	5	6	nA MAX
Input Bias Current	I_B	$V_{CM} = 0$	100	100	120	120	150	nA MAX
Input Voltage Range	IVR		-14.3 +13.5	-14.5 +13.5	-14.3 +13.5	-14.5 +13.5	-14.5 +13.5	V MIN
Common-Mode Rejection Ratio	CMRR	No Load CMVR = IVR	96	100	86	90	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ No Load	10	6	18	10	32	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$, $V_O = \pm 10V$	500	1000	250	500	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$	-13.5 +13.8	-13.7 +14.0	-13.5 +13.8	-13.7 +13.9	-13.6 +13.8	V MIN
Supply Current	I_{SY}	No Load	300	300	360	360	420	μA MAX

NOTES:

For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

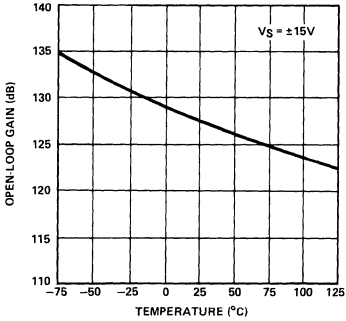
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21NT TYPICAL	OP-21N TYPICAL	OP-21GT TYPICAL	OP-21G TYPICAL	OP-21GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled	0.5	0.5	1	1	2.5	$\mu V/^\circ C$
Nullled Input Offset Voltage Drift	TCV_{OSn}	Nullled, $R_p = 10k\Omega$	0.5	0.5	1	1	2.5	$\mu V/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$	2000	2000	1500	1500	1000	V/mV
Slew Rate	SR	$R_L = 25k\Omega$ $C_L = 100pF$	0.25	0.25	0.25	0.25	0.25	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ $R_L = 10k\Omega$	600	600	600	600	600	kHz

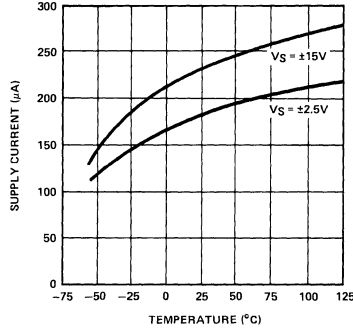


TYPICAL PERFORMANCE CHARACTERISTICS

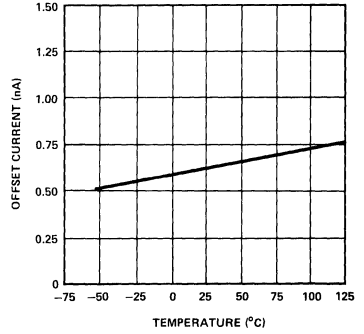
OPEN-LOOP GAIN vs TEMPERATURE



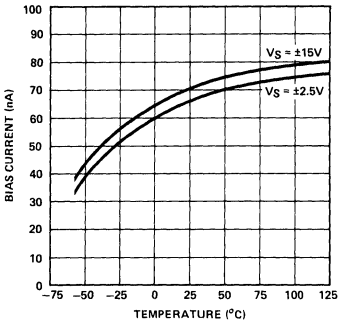
SUPPLY CURRENT vs TEMPERATURE



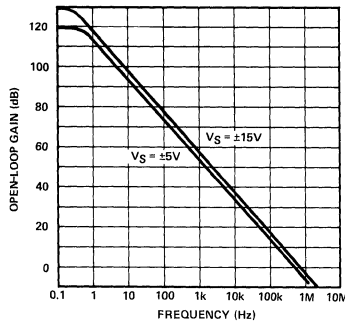
OFFSET CURRENT vs TEMPERATURE



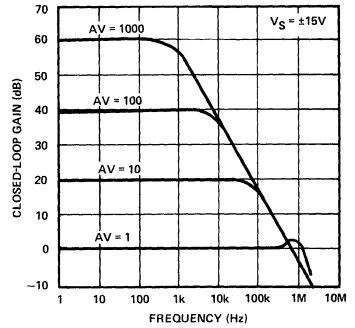
BIAS CURRENT vs TEMPERATURE



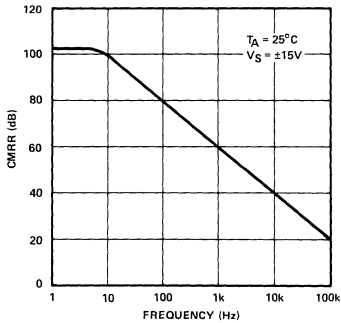
OPEN-LOOP GAIN vs FREQUENCY



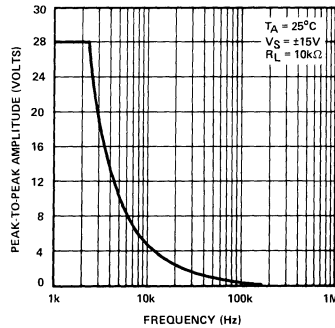
CLOSED-LOOP GAIN vs FREQUENCY

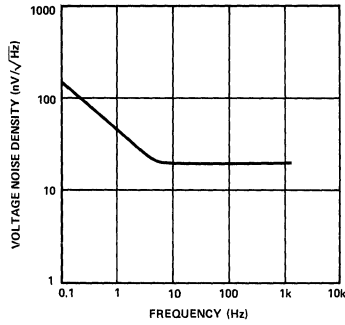
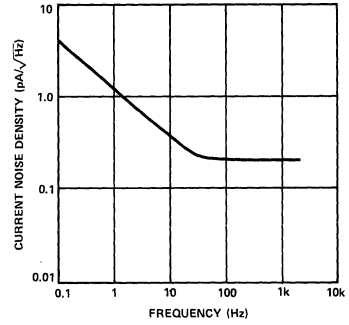
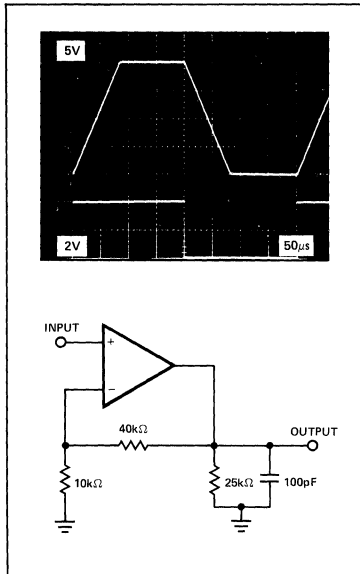
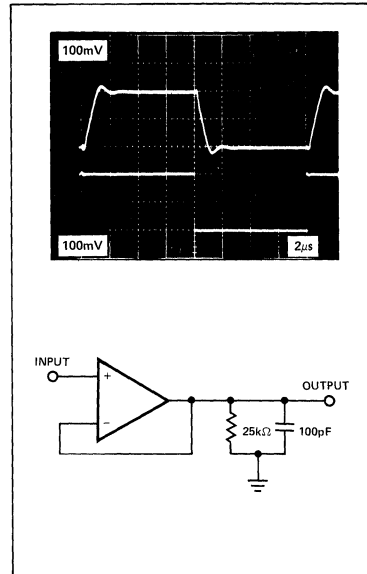


CMRR vs FREQUENCY



MAXIMUM OUTPUT SWING vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS
VOLTAGE NOISE DENSITY vs FREQUENCY

CURRENT NOISE DENSITY vs FREQUENCY

NONINVERTING LARGE-SIGNAL RESPONSE

NONINVERTING SMALL-SIGNAL RESPONSE


Precision Monolithics Inc.

FEATURES

- Programmable Supply Current $1\mu\text{A}$ to $400\mu\text{A}$
- Single Supply Operation $+3\text{V}$ to $+30\text{V}$
- Dual Supply Operation $\pm 1.5\text{V}$ to $\pm 15\text{V}$
- Low Input Offset Voltage $100\mu\text{V}$
- Low Input Offset Voltage Drift $0.75\mu\text{V}/^\circ\text{C}$
- High Common-Mode Input Range ... $\text{V}-$ to $\text{V}+$ (-1.5V)
- High CMRR and PSRR 115dB
- High Open-Loop Gain $1800\text{V}/\text{mV}$
- $\pm 30\text{V}$ Input Overvoltage Protection
- Unity-Gain Stable
- LM4250 Pinout and Nulling

GENERAL DESCRIPTION

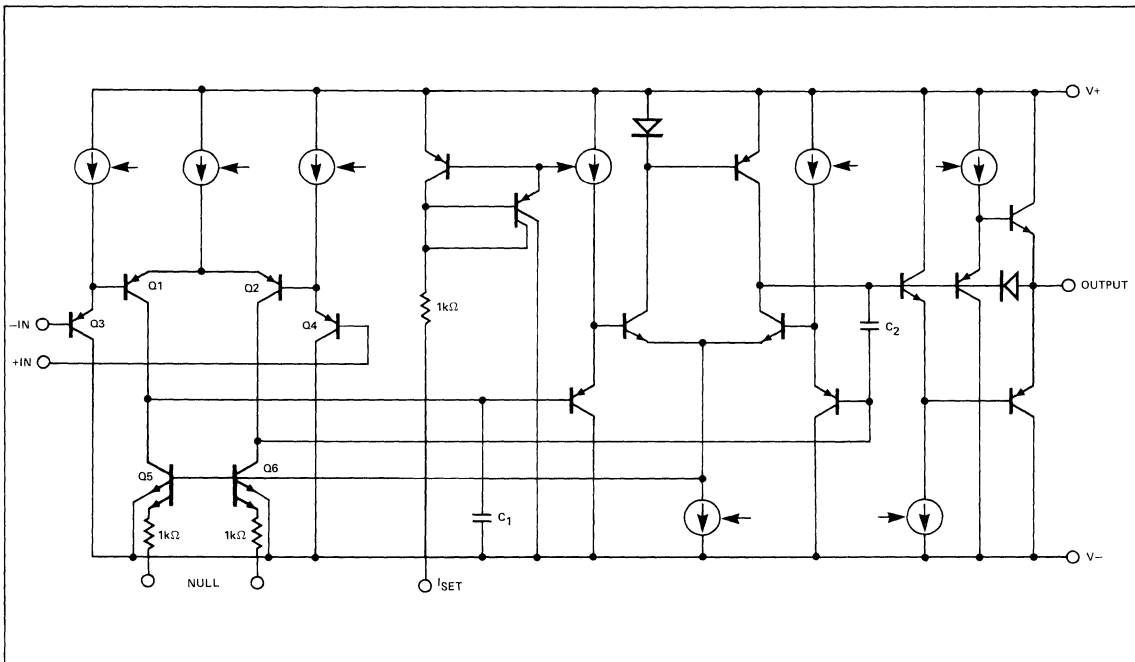
The OP-22 is a monolithic micropower operational amplifier designed to provide excellent accuracy in high-gain applications. Offsets are very low which generally eliminates any need for external nulling of V_{OS} . The OP-22 is internally compensated and unity-gain stable. It also features high open-loop gain, CMRR, and PSRR. This assures good gain accuracy and rejection of power supply variations even when

used in circuits with high closed-loop gain. The low offsets and high gain accuracy of the OP-22 bring precision performance to the micropower field.

The OP-22 is a versatile op amp designed for operation from battery or solar-cell power sources. Supply current is programmable over a range of $1\mu\text{A}$ to $400\mu\text{A}$ with a single external resistor. Input voltage range is very wide and extends down to the negative rail, thus the common-mode input voltage range includes ground when operating from a single supply voltage. This ability to provide high DC performance over a wide input range is particularly useful in single-battery applications. In addition, the OP-22 is characterized over a wide supply range of $\pm 1.5\text{V}$ to $\pm 15\text{V}$, or $+3\text{V}$ to $+30\text{V}$ for single supply.

The OP-22 pin-out and offset nulling are identical to the LM4250 and many other micropower operational amplifiers. This functional commonality allows easy upgrading of system performance. By selection of set resistor value, the circuit designer can readily use the OP-22 in place of such amplifiers as the LM108, LM112, LM4250, $\mu\text{A}776$, and ICL8021 in high-gain, low-frequency applications.

SIMPLIFIED SCHEMATIC



5
OPERATIONAL AMPLIFIERS

**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Storage Temperature Range	
J and Z Packages	-65°C to +150°C
Operating Temperature Range	
OP-22A, OP-22B (J or Z package)	-55°C to +125°C
OP-22E, OP-22F (J or Z package)	-25°C to +85°C
OP-22HJ, OP-22HZ	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to +150°C

NOTES:

- See table for maximum ambient temperature rating.
- Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

	MAXIMUM AMBIENT TEMPERATURE $V_S = \pm 15V$ and $I_{SET} = 10\mu A$	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	124°C	—
8-Pin Hermetic DIP (Z)	124°C	—

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 10\mu A$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22A/E			OP-22B/F			OP-22H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	—	0.5	3	nA
Input Bias Current	I_B	$I_{SET} = 1\mu A, V_{CM} = 0$	—	2.6	5	—	3.0	7.5	—	4.0	10	nA
		$I_{SET} = 10\mu A, V_{CM} = 0$	—	19	30	—	24	35	—	30	50	
Input Voltage Range	IVR	$V_+ = +5V,$ $V_- = 0V.$	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	-15/+13.5	—	—	-15/+13.5	—	—	-15/+13.5	—	—	
Common-Mode Rejection Ratio	CMRR (Note 2)	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.5V$	100	115	—	95	105	—	85	95	—	dB
Power Supply Rejection Ratio (Note 1)	PSRR (Note 2)	$V_S = \pm 1.5V$ to $\pm 15V;$ and $V_- = 0V,$ $V_+ = 3V$ to $30V.$	—	1.8	6	—	6	18	—	10	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V,$ $I_{SET} = 1\mu A,$ $R_L = 100k\Omega.$	1000	1800	—	500	900	—	250	500	—	V/mV
		$V_S = \pm 15V,$ $I_{SET} = 10\mu A,$ $R_L = 10k\Omega.$	1000	1800	—	500	900	—	300	500	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5V,$ $I_{SET} = 1\mu A, R_L = 100k\Omega$ & $I_{SET} = 10\mu A, R_L = 10k\Omega.$	±0.8	±0.82	—	±0.8	±0.82	—	±0.75	±0.8	—	V
		$V_S = \pm 15V,$ $I_{SET} = 1\mu A, R_L = 100k\Omega$ & $I_{SET} = 10\mu A, R_L = 10k\Omega.$	±14	±14.2	—	±14	±14.2	—	±13.5	±14	—	V
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0,$ $V_S = \pm 15V,$ $I_{SET} = 10\mu A, R_L = 10k\Omega.$	—	250	—	—	250	—	—	250	—	kHz
Slew Rate	SR	$V_S = \pm 15V,$ $I_{SET} = 10\mu A,$ $R_L = 10k\Omega.$	—	0.08	—	—	0.08	—	—	0.08	—	V/ μs
Supply Current No Load	I_{SY}	$V_S = \pm 15V, I_{SET} = 1\mu A.$	—	15	17	—	16	19	—	18	21	μA
		$V_S = \pm 15V, I_{SET} = 10\mu A.$	—	150	170	—	160	190	—	180	210	μA
		$V_S = \pm 1.5V, I_{SET} = 1\mu A.$	—	10.5	12.5	—	14	16	—	17	20	μA
		$V_S = \pm 1.5V, I_{SET} = 10\mu A.$	—	105	125	—	140	160	—	170	200	μA

NOTES:

- Sample tested for single-supply operation, 100% tested for dual-supply operation.
- Measured with V_{OS} unnullled and I_{SET} constant.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 10\mu A$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-22AJ/AZ and OP-22BJ/BZ, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-22EJ/EZ and OP-22FJ/FZ, and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-22HJ and OP-22HZ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22A/E			OP-22B/F			OP-22H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.75	1.5	—	1.0	2.0	—	1.5	3.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	175	400	—	350	600	—	500	1200	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	—	0.5	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	2	10	—	3	15	—	5	25	$pA/^\circ C$
Input Bias Current	I_B	$I_{SET} = 1\mu A, V_{CM} = 0$ $I_{SET} = 10\mu A, V_{CM} = 0$	—	2.8	5	—	3.3	7.5	—	4.5	10	nA
Input Voltage Range	IVR	$V^+ = +5V, V^- = 0V$ $V_S = \pm 15V$	0/3.2 -15/+13.2	—	—	0/3.2 -15/+13.2	—	—	0/3.2 -15/+13.2	—	—	V
Common-Mode Rejection Ratio	CMRR (Note 3)	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.2V$ $I_{SET} = 1\mu A$ $I_{SET} = 10\mu A$	80 90	105 115	—	80 86	99 105	—	80 80	90 90	—	dB
Power Supply Rejection Ratio	PSRR (Note 3)	$V_S = \pm 1.5V$ to $\pm 15V$ & $V^- = 0V,$ $V^+ = 3V$ to $30V$ (Note 2)	—	3.2	10	—	10	32	—	32	56	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V,$ $I_{SET} = 1\mu A, R_L = 100k\Omega.$ $V_S = \pm 15V,$ $I_{SET} = 10\mu A, R_L = 10k\Omega.$	200 500	400 1000	—	200 300	400 750	—	100 150	250 300	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5V,$ $I_{SET} = 1\mu A, R_L = 100k\Omega$ & $I_{SET} = 10\mu A, R_L = 10k\Omega.$ $V_S = \pm 15V,$ $I_{SET} = 1\mu A, R_L = 100k\Omega$ & $I_{SET} = 10\mu A, R_L = 10k\Omega.$	± 0.65 ± 13.6	± 0.75 ± 13.8	—	± 0.65 ± 13.6	± 0.75 ± 13.8	—	± 0.6 ± 13.0	± 0.7 ± 13.5	—	V
Supply Current No Load	I_{SY}	$V_S = \pm 15V, I_{SET} = 1\mu A.$ $V_S = \pm 15V, I_{SET} = 10\mu A.$ $V_S = \pm 1.5V, I_{SET} = 1\mu A.$ $V_S = \pm 1.5V, I_{SET} = 10\mu A.$	— — — —	16 160 12 120	18 180 14 140	— — — —	17 170 15 150	20 200 18 180	— — — —	20 200 19 190	25 250 25 250	μA

NOTES:

- Sample tested.
- $V_{CM} = 1.5V$
- Measured with V_{OS} unnulled and I_{SET} constant.

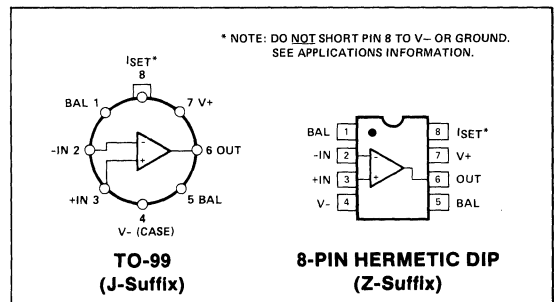
ORDERING INFORMATION†

$T_A = 25^\circ C$ V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	
300	OP22AJ*	OP22AZ*	MIL
300	OP22EJ	OP22EZ	IND
500	OP22BJ*	OP22BZ*	MIL
500	OP22FJ	OP22FZ	IND
1000	OP22HJ	OP22HZ	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

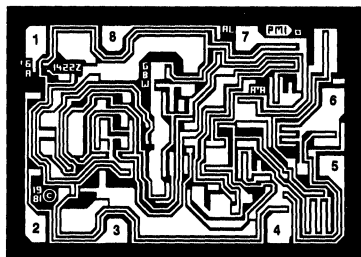
† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

PIN CONNECTIONS





DICE CHARACTERISTICS



DIE SIZE 0.069 × 0.049 Inch, 3381 sq. mils
(1.75 × 1.24 mm, 2.18 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V⁻
5. BALANCE
6. OUTPUT
7. V⁺
8. I_{SET}

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22N LIMIT	OP-22G LIMIT	OP-22GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	500	1000	μV MAX
Input Offset Current	I_{OS}	(Note 1)	1	2	3	nA MAX
Input Bias Current	I_B	$I_{SET} = 1\mu A$	5	7.5	10	nA MAX
		$I_{SET} = 10\mu A$ (Note 1)	30	35	50	
Input Voltage Range	IVR	$V^+ = +5V, V^- = 0V$	0/3.5	0/3.5	0/3.5	V MIN
		$V_S = \pm 15V$	-15/+13.5	-15/+13.5	-15/+13.5	
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V, -15V \leq V_{CM} \leq +13.5V$ (Note 2)	100	95	85	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$	6	18	32	$\mu V/V$ MIN
		$V^- = 0V, V^+ = 3V$ to $30V$ (Note 2)				
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V,$ $I_{SET} = 1\mu A, R_L = 100k\Omega.$	1000	500	250	V/mV MIN
		$V_S = \pm 15V,$ $I_{SET} = 10\mu A, R_L = 10k\Omega.$	1000	500	300	V/mV MIN
Output Voltage Swing	V_O	$V_S = \pm 1.5V,$ $I_{SET} = 1\mu A, R_L = 100k\Omega$ & $I_{SET} = 10\mu A, R_L = 10k\Omega.$	± 0.8	± 0.8	± 0.75	V MIN
		$V_S = \pm 15V,$ $I_{SET} = 1\mu A, R_L = 100k\Omega$ & $I_{SET} = 10\mu A, R_L = 10k\Omega.$	± 14	± 14	± 13.5	V MIN
Supply Current No Load	I_{SY}	$V_S = \pm 15V, I_{SET} = 1\mu A.$	17	19	21	μA MAX
		$V_S = \pm 15V, I_{SET} = 10\mu A.$	170	190	210	μA MAX
		$V_S = \pm 1.5V, I_{SET} = 1\mu A.$	12.5	16	20	μA MAX
		$V_S = \pm 1.5V, I_{SET} = 10\mu A.$	125	160	200	μA MAX

NOTES:

1. $V_{CM} = 0$
2. Measured with V_{OS} unnullled and I_{SET} held constant.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

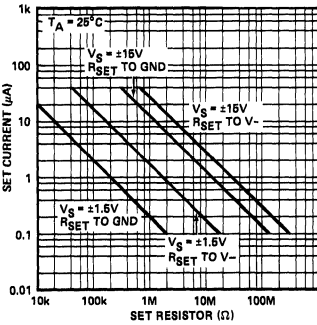
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 10\mu A$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22N TYPICAL	OP-22G TYPICAL	OP-22GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnullled	1.0	1.5	2.5	$\mu V/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $I_{SET} = 1\mu A, R_L = 100k\Omega$ & $I_{SET} = 10\mu A, R_L = 10k\Omega$	1800	900	500	V/mV

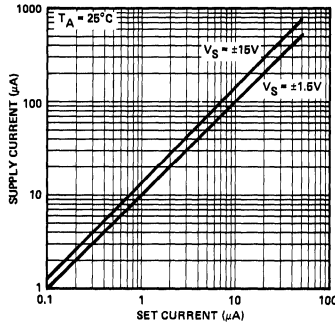


TYPICAL PERFORMANCE CHARACTERISTICS

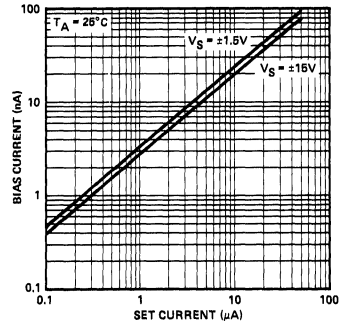
SET CURRENT vs SET RESISTOR



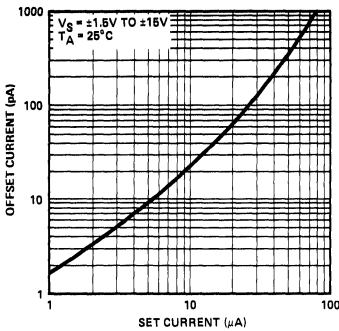
SUPPLY CURRENT vs SET CURRENT



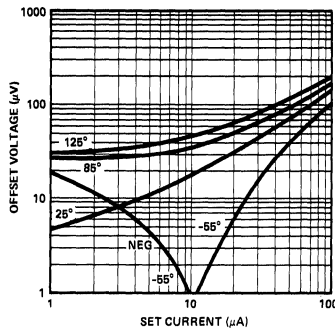
BIAS CURRENT vs SET CURRENT



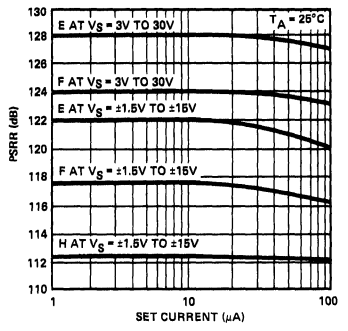
OFFSET CURRENT vs SET CURRENT



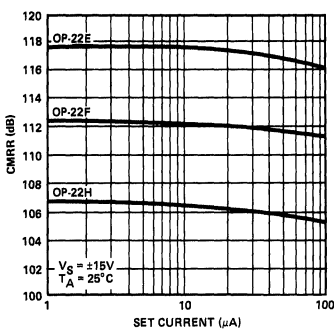
OFFSET VOLTAGE vs SET CURRENT



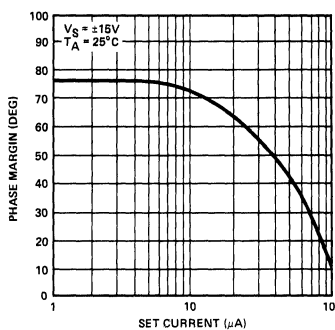
POWER SUPPLY REJECTION vs SET CURRENT



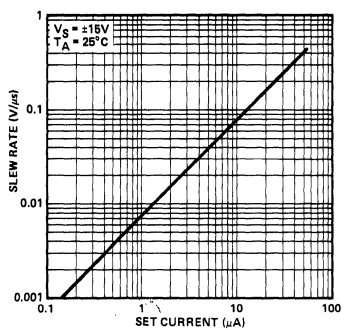
COMMON-MODE REJECTION vs SET CURRENT



PHASE MARGIN vs SET CURRENT



SLEW RATE vs SET CURRENT



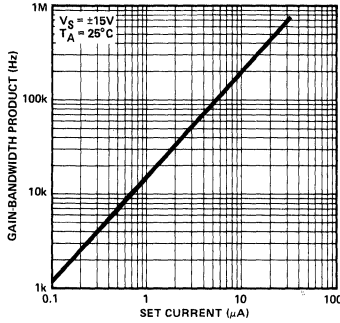
5

OPERATIONAL AMPLIFIERS

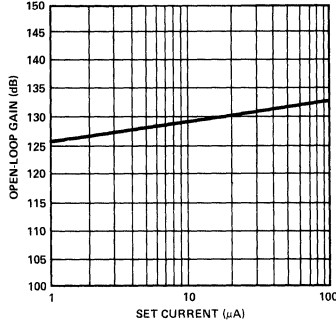


TYPICAL PERFORMANCE CHARACTERISTICS

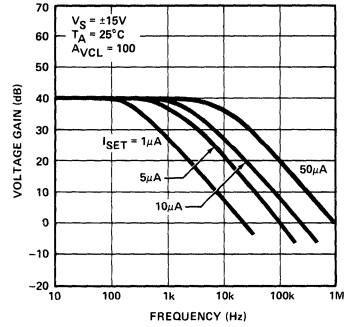
GAIN-BANDWIDTH PRODUCT vs SET CURRENT



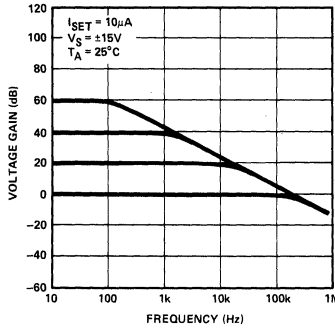
OPEN-LOOP GAIN vs SET CURRENT



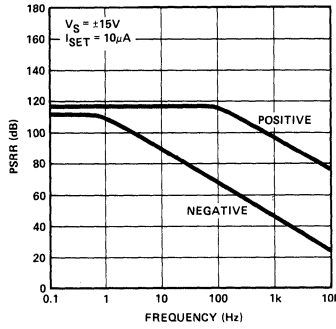
FREQUENCY RESPONSE vs SET CURRENT



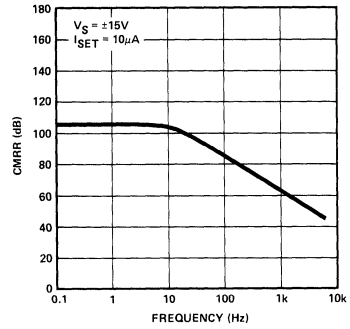
CLOSED-LOOP FREQUENCY RESPONSE



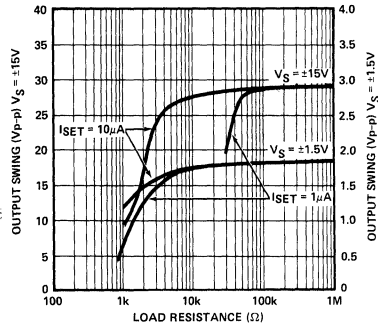
POWER SUPPLY REJECTION vs FREQUENCY



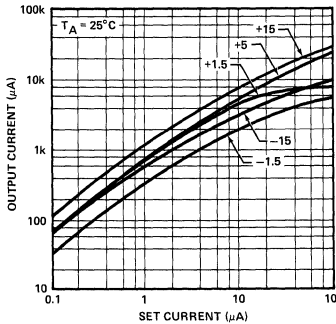
COMMON-MODE REJECTION vs FREQUENCY



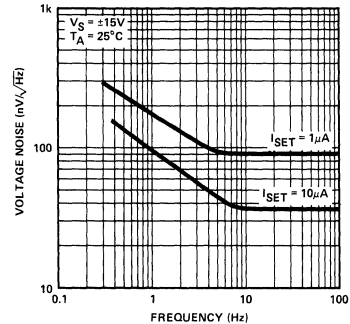
PEAK-TO-PEAK OUTPUT SWING vs LOAD RESISTANCE



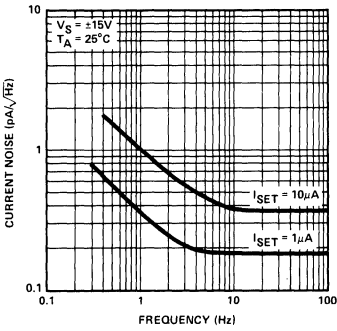
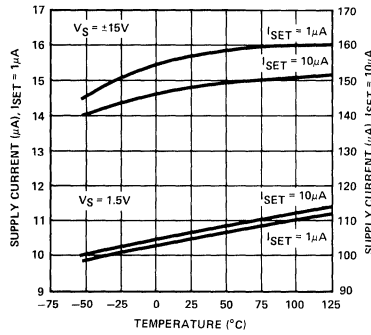
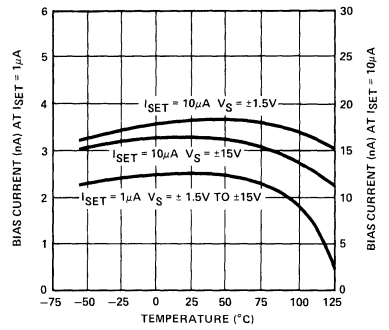
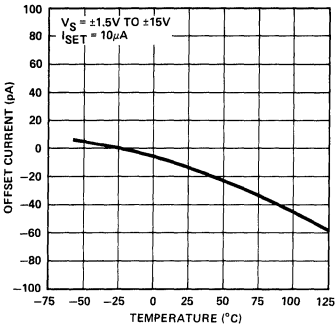
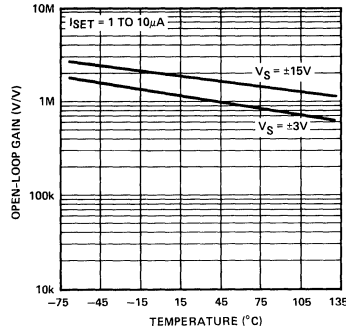
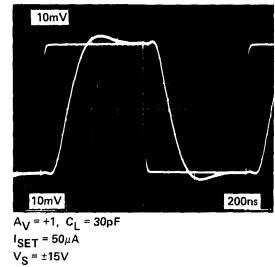
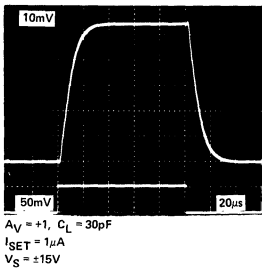
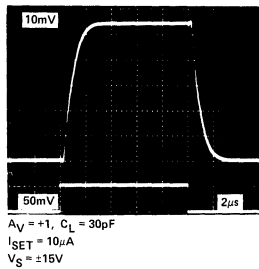
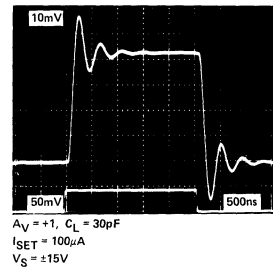
MAXIMUM OUTPUT CURRENT vs SET CURRENT AT V_S = ±15V, +5 AND ±1.5



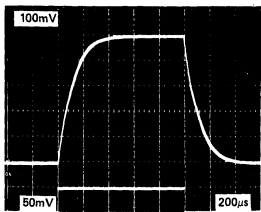
VOLTAGE NOISE vs FREQUENCY

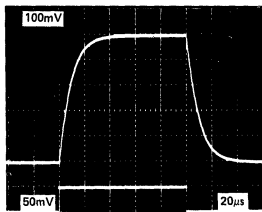


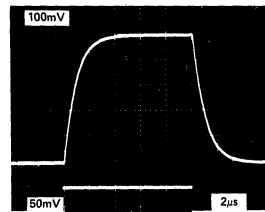
TYPICAL PERFORMANCE CHARACTERISTICS

CURRENT NOISE vs FREQUENCY

SUPPLY CURRENT vs TEMPERATURE

BIAS CURRENT vs TEMPERATURE

OFFSET CURRENT vs TEMPERATURE

OPEN-LOOP GAIN vs TEMPERATURE

SMALL-SIGNAL TRANSIENT RESPONSE

SMALL-SIGNAL TRANSIENT RESPONSE

SMALL-SIGNAL TRANSIENT RESPONSE

SMALL-SIGNAL TRANSIENT RESPONSE

 5
 OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS

 SMALL-SIGNAL
TRANSIENT RESPONSE

 $A_V = +10, C_L = 30\text{pF}$
 $I_{SET} = 1\mu\text{A}$
 $V_S = \pm 15\text{V}$

 SMALL-SIGNAL
TRANSIENT RESPONSE

 $A_V = +10, C_L = 30\text{pF}$
 $I_{SET} = 10\mu\text{A}$
 $V_S = \pm 15\text{V}$

 SMALL-SIGNAL
TRANSIENT RESPONSE

 $A_V = +10, C_L = 30\text{pF}$
 $I_{SET} = 100\mu\text{A}$
 $V_S = \pm 15\text{V}$

APPLICATIONS INFORMATION

OP-22 series units may be inserted directly into LM4250, $\mu\text{A}776$ and ICL8021 sockets with or without removal of external nulling components. The value of set resistor for a given supply current varies between types and the manufacturer's data sheets should be consulted for this information. Table 1 compares set resistor values for the OP-22 and the LM4250. (R_{SET} connected to V^-).

TABLE 1
 Supply Current vs. Set Resistor for OP-22 and LM4250

V_{SUPPLY}	$I_{SY} = 10\mu\text{A}$		$I_{SY} = 30\mu\text{A}$		$I_{SY} = 100\mu\text{A}$	
	OP-22	LM4250	OP-22	LM4250	OP-22	LM4250
$\pm 1.5\text{V}$	2.2M Ω	1.3M Ω	680k Ω	430k Ω	220k Ω	120k Ω
$\pm 3.0\text{V}$	6.8M Ω	2.7M Ω	2.2M Ω	910k Ω	680k Ω	270k Ω
$\pm 5.0\text{V}$	13M Ω	4.7M Ω	4.3M Ω	1.5M Ω	1.3M Ω	470k Ω
$\pm 12\text{V}$	33M Ω	12M Ω	11M Ω	3.9M Ω	3.3M Ω	1.2M Ω
$\pm 15\text{V}$	43M Ω	15M Ω	15M Ω	5.1M Ω	4.3M Ω	1.5M Ω
I_{SET}	0.67 μA	1.8 μA	2.0 μA	6.0 μA	6.7 μA	20 μA

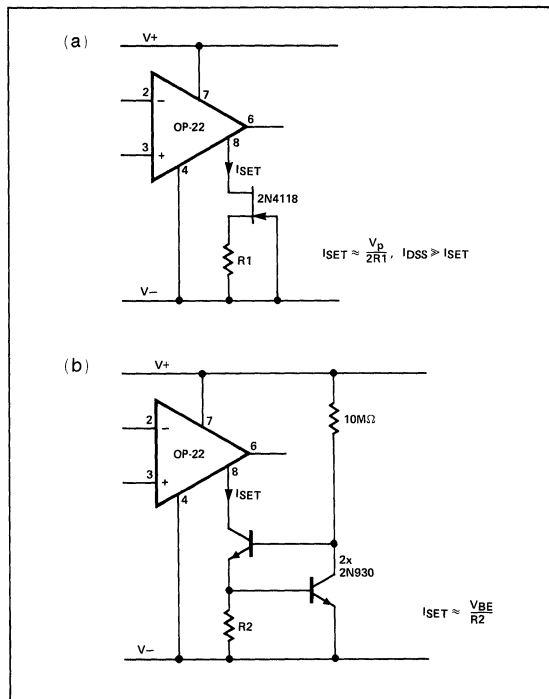
SET-RESISTOR SELECTION

The value of set resistor for selected supply current may be calculated using the "Supply current vs. Set current" curve and the formula;

$$R_{SET} = \frac{(V_{SUPPLY} - 2V_{BE})}{I_{SET}} \quad (1)$$

Alternatively, the "Supply Current vs. Set Current" graph may be used in conjunction with the "Set Current vs. Set Resistor" graph. V_{SUPPLY} in formula (1) refers to the total supply voltage with R_{SET} connected between pin 8 and negative supply. R_{SET} may be connected to ground in which case V_{SUPPLY} in (1) is the positive supply.

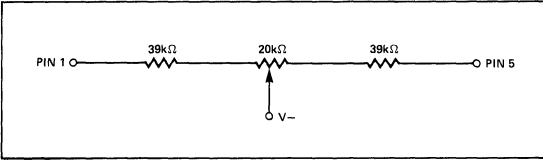
Biasing the OP-22 with a fixed resistor produces a supply current approximately proportional to supply voltage. In applications where a constant drain is required with varying supply, R_{SET} can be replaced by current generators. Two suggested arrangements are shown below:



CAUTION: Shorting of pin 8 to negative supply or ground will cause excessive I_{SET} which in turn will cause excessive supply current to flow. I_{SET} should always be limited.

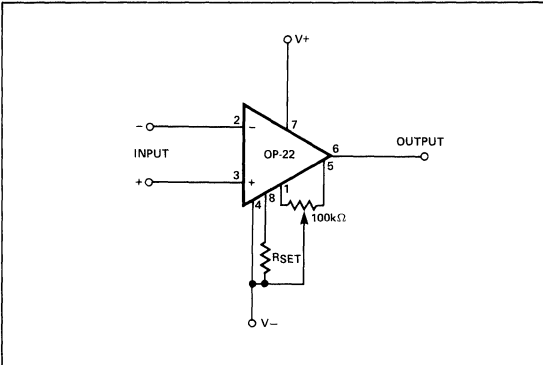
OFFSET VOLTAGE ADJUSTMENT

The offset voltage can be trimmed to zero using a 100k Ω potentiometer (see offset nulling circuit). Adjustment range is approximately $\pm 5\text{mV}$. Resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors as shown below.

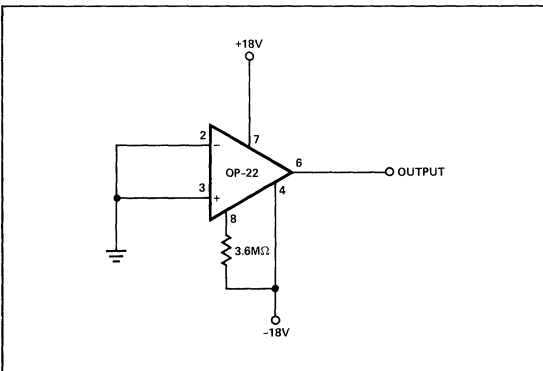


This arrangement has a $\pm 500\mu\text{V}$ adjustment range. Offset nulling of the OP-22 has negligible effect on the value of TCV_{OS} .

OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT*



*Other circuits may apply at PMI's discretion.

APPLICATIONS CIRCUITS

A micropower bandgap voltage reference operating at a quiescent current of $15\mu\text{A}$ may be constructed using an OP-22 and a MAT-01 dual transistor (see Figure 1). The circuit provides a 1.23V reference with better performance than micropower I.C. shunt regulators and has the advantages of being a series regulator.

MICROPOWER 1.23 VOLT BANDGAP REFERENCE

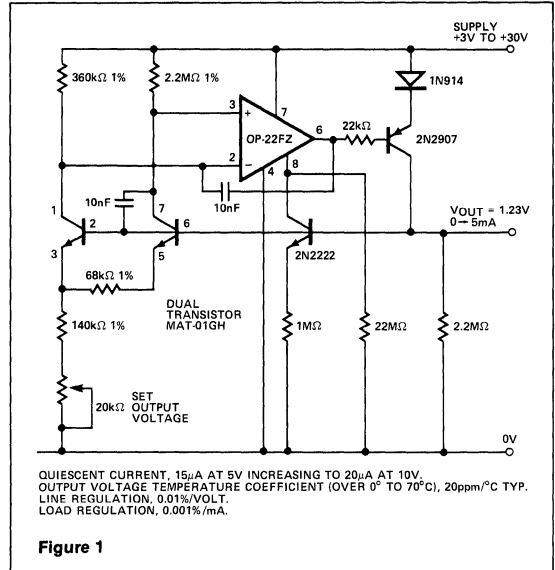


Figure 1

GATED MICROPOWER AMPLIFIER

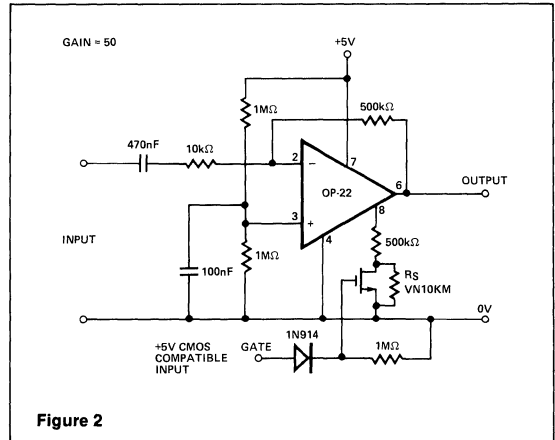
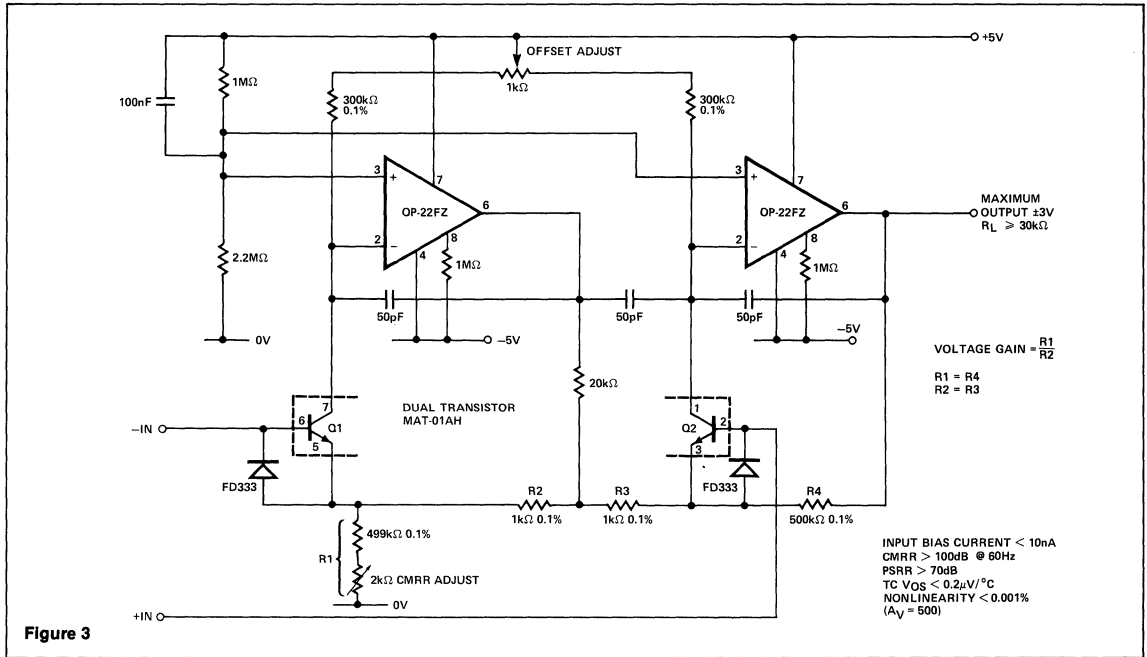


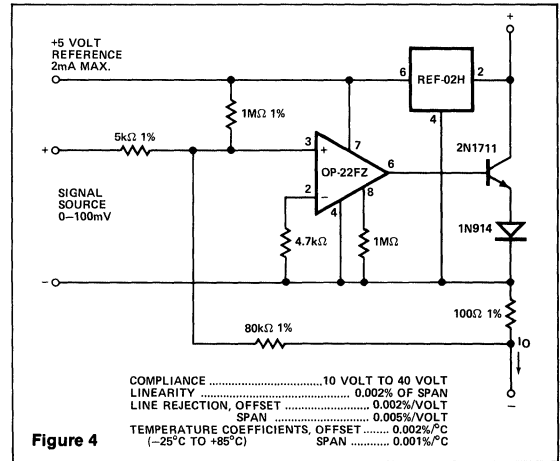
Figure 2

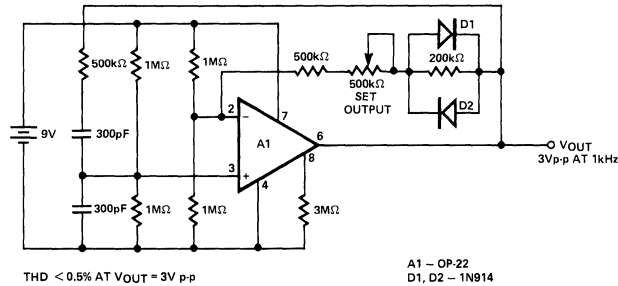
MICROPOWER INSTRUMENTATION AMPLIFIER — POWER DRAIN $\leq 3\text{mW}$ WITH $\pm 5\text{V}$ SUPPLIES


In Figure 2, the OP-22 is used as a gated amplifier where power consumption and bandwidth are controllable. R_S can be selected for a specific lower-power operation or omitted so the amplifier can be completely shut down.

A micropower instrumentation amplifier that consumes less than 3mW with $\pm 5\text{V}$ supplies is shown in Figure 3. Offset voltage drift is less than $0.2\mu\text{V}/^\circ\text{C}$ and common-mode input range is $\pm 3\text{V}$ with CMRR of over 100dB at 60Hz.

Process control systems use two-wire 4-20mA current transmitters when sending analog signals through noisy environments. The "zero" or "offset" current of 4mA may be used to power the transmitter signal conditioning amplifiers and/or excite a d.c. transducer. This allows remote signal conditioning without having a remote power source. Power is provided at the receiving end where the signal current is monitored by a precision 50Ω resistor. The 4-20mA transmitter shown in Figure 4 has high stability, excellent linearity, and generates the 4-20mA current output. A 5V reference is available for powering transducers and micropower amplifiers at a maximum current of 2mA.

TWO TERMINAL 4-20mA TRANSMITTER


MICROPOWER WIEN-BRIDGE OSCILLATOR ($P_d < 500\mu W$)

Figure 5
MICROPOWER 5 VOLT REGULATOR

QUIESCENT CURRENT $\sim 50\mu A$ AT 9V
 LOAD REGULATION, 0.001% / mA
 LINE REGULATION, 0.01% / VOLT
 TEMPERATURE COEFFICIENT, 40ppm / °C (-25°C TO +85°C)

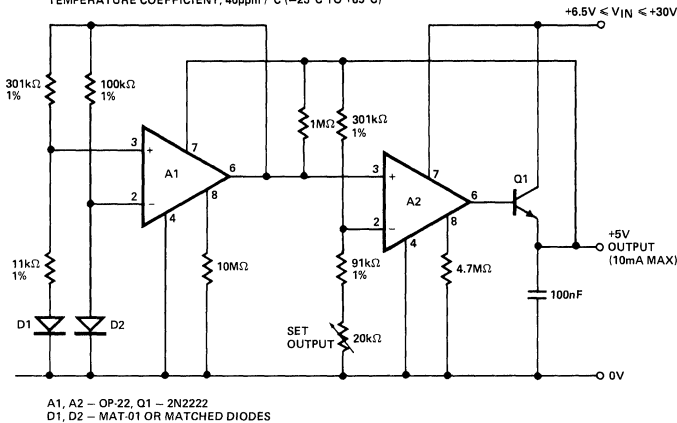

Figure 6

Figure 5 shows a micropower Wien-bridge oscillator designed for battery-powered instrumentation. Output level is controlled by nonlinear elements D1 and D2. When adjusted for 3V p-p output, the distortion level is below 0.5% at 1kHz.

The 5 volt regulator in Figure 6 is intended for instrumentation requiring good power efficiency. Low-power 3-terminal

IC regulators typically draw 2mA to 5mA quiescent current compared to only $50\mu A$ with this discrete implementation. Maximum load current is 10mA as shown, and can be increased by changing Q1 to a power transistor and proportionately increasing the set current of A2.

Precision Monolithics Inc.

FEATURES

- **Low Noise** { ... $80nV_{p-p}$ (0.1Hz to 10Hz)
..... $3nV/\sqrt{Hz}$
- **Low Drift** $0.2\mu V/^\circ C$
- **High Speed** { $2.8V/\mu s$ Slew Rate
..... 8MHz Gain Bandwidth
- **Low V_{OS}** $10\mu V$
- **Excellent CMRR** 126dB at V_{CM} of $\pm 11V$
- **High Open-Loop Gain** 1.8 Million
- **Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets**

ORDERING INFORMATION†

$T_A = 25^\circ C$ $V_{OS} \text{ MAX}$ (μV)	PACKAGE				OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	LCC	
25	OP27AJ*	OP27AZ*			MIL
25	OP27EJ	OP27EZ	OP27EP		IND/COM
60	OP27BJ*	OP27BZ*		OP27BRC/883	MIL
60	OP27FJ	OP27FZ	OP27FP		IND/COM
100	OP27CJ*	OP27CZ*			MIL
100	OP27GJ	OP27GZ	OP27GP		IND/COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

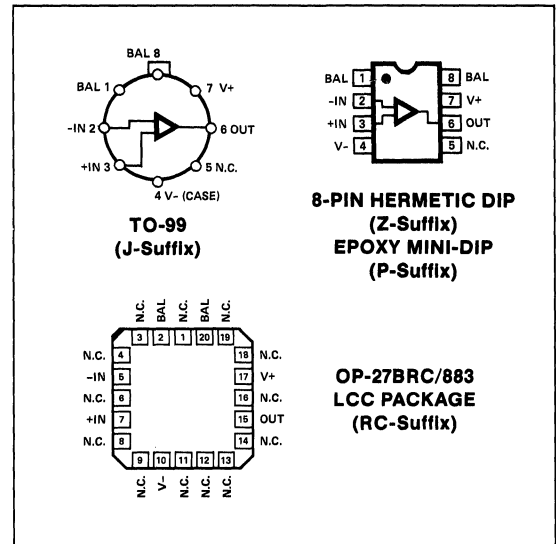
The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high-speed and low-noise. Offsets down to $25\mu V$ and drift of $0.6\mu V/^\circ C$ maximum make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, $e_n = 3.5nV/\sqrt{Hz}$, at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8MHz and a $2.8V/\mu sec$ slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of $\pm 10nA$ is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to $\pm 20nA$ and $15nA$ respectively.

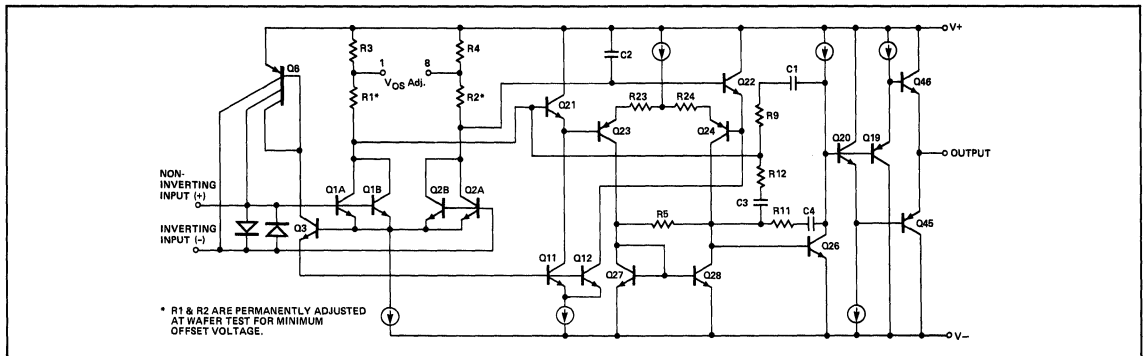
The output stage has good load driving capability. A guaranteed swing of $\pm 10V$ into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of $0.2\mu V/month$, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	-65°C to +150°C

Operating Temperature Range

OP-27A, OP-27B, OP-27C (J, Z, RC)	... -55°C to +125°C
OP-27E, OP-27F, OP-27G (J, Z)	... -25°C to +85°C
OP-27E, OP-27F, OP-27G (P)	... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	... 300°C
DICE Junction Temperature	... -65°C to +150°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C
LCC	80°C	7.8mW/°C

- The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
- For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E			OP-27B/F			OP-27C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	$\mu Vp-p$
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	nV/\sqrt{Hz}
		$f_O = 30\text{Hz}$ (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		$f_O = 1000\text{Hz}$ (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Notes 3, 6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	pA/\sqrt{Hz}
		$f_O = 30\text{Hz}$ (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		$f_O = 1000\text{Hz}$ (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	G Ω
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.0 ±10.0	±13.8 ±11.5	—	±12.0 ±10.0	±13.8 ±11.5	—	±11.5 ±10.0	±13.5 ±11.5	—	V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/ μs

5
OPERATIONAL AMPLIFIERS

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E			OP-27B/F			OP-27C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0, I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	V_O	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	± 4.0	—	—	± 4.0	—	—	± 4.0	—	mV

NOTES:

- Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
- Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$ — refer to typical performance curve.
- Sample tested.
- Guaranteed by design.
- See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
- See test circuit for current noise measurement.
- Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A			OP-27B			OP-27C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	± 20	± 60	—	± 28	± 95	—	± 35	± 150	nA
Input Voltage Range	IVR		± 10.3	± 11.5	—	± 10.3	± 11.5	—	± 10.2	± 11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.5	± 13.5	—	± 11.0	± 13.2	—	± 10.5	± 13.0	—	V

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-27J and OP-27Z, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-27P, unless otherwise noted.

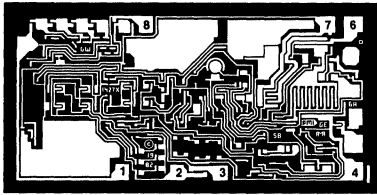
PARAMETER	SYMBOL	CONDITIONS	OP-27E			OP-27F			OP-27G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	± 14	± 60	—	± 18	± 95	—	± 25	± 150	nA
Input Voltage Range	IVR		± 10.5	± 11.8	—	± 10.5	± 11.8	—	± 10.5	± 11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.7	± 13.6	—	± 11.4	± 13.5	—	± 11.0	± 13.3	—	V

NOTES:

- Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
- The TCV_{OS} performance is within the specifications unnullled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
- Guaranteed by design.



DICE CHARACTERISTICS

DIE SIZE 0.054 × 0.108 inch, 5832 sq. mils
(1.37 × 2.74mm, 3.76 sq. mm)

1. NULL
2. (-) INPUT
3. (+) INPUT
4. V-
6. OUTPUT
7. V+
8. NULL

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-27N, OP-27G, and OP-27GR devices; $T_A = 125^\circ C$ for OP-27NT and OP-27GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27NT LIMIT	OP-27N LIMIT	OP-27GT LIMIT	OP-27G LIMIT	OP-27GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		± 60	± 40	± 95	± 55	± 80	nA MAX
Input Voltage Range	IVR		± 10.3	± 11	± 10.3	± 11	± 11	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = IVR$	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	10	—	10	20	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	600 —	1000 800	500 —	1000 800	700 600	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	± 11.5 —	± 12.0 ± 10.0	± 11.0 —	± 12.0 ± 10.0	± 11.5 ± 10.0	V MIN
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTE:

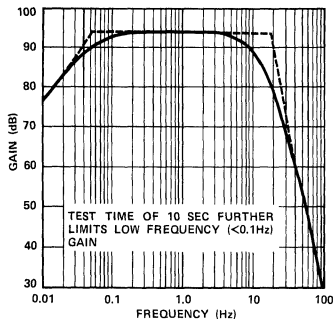
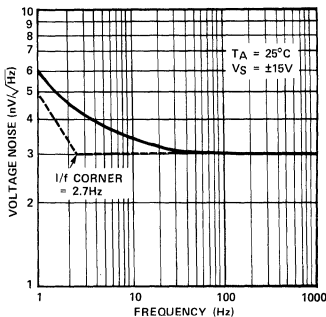
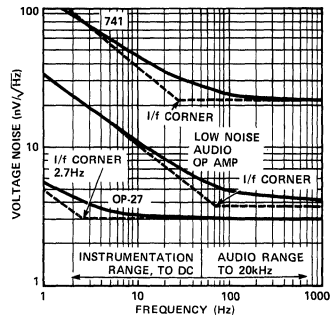
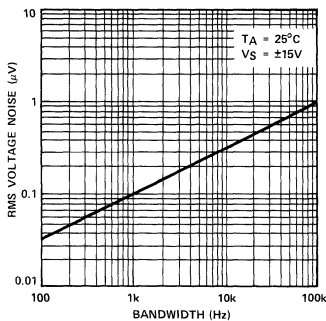
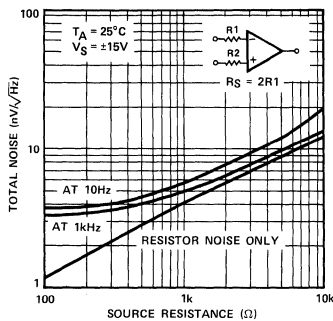
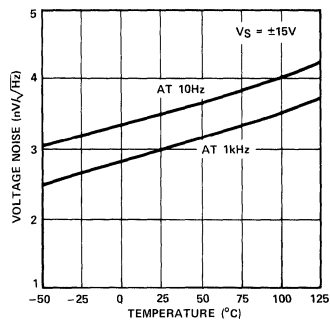
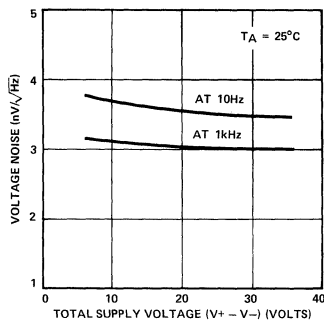
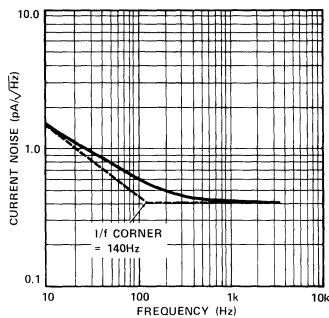
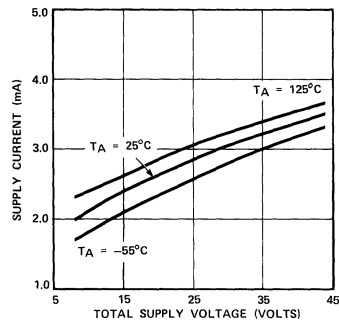
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N TYPICAL	OP-27G TYPICAL	OP-27GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nullled or Unnullled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.3	0.4	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		80	130	180	$pA/^\circ C$
Average Input Bias Current Drift	TCI_B		100	160	200	$pA/^\circ C$
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	nV/\sqrt{Hz}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	pA/\sqrt{Hz}
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.09	$\mu Vp-p$
Slew Rate	SR	$R_L \geq 2k\Omega$	2.8	2.8	2.8	V/ μs
Gain Bandwidth Product	GBW		8	8	8	MHz

NOTE:

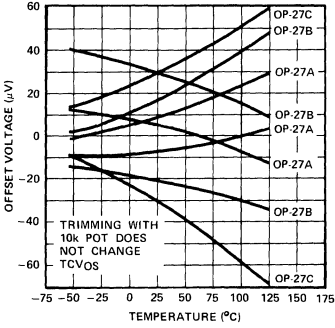
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS
**0.1Hz TO 10Hz_{p-p} NOISE TESTER
FREQUENCY RESPONSE**

**VOLTAGE NOISE DENSITY
vs FREQUENCY**

**A COMPARISON OF
OP AMP VOLTAGE
NOISE SPECTRA**

**INPUT WIDEBAND VOLTAGE
NOISE vs BANDWIDTH (0.1Hz
TO FREQUENCY INDICATED)**

**TOTAL NOISE vs SOURCE
RESISTANCE**

**VOLTAGE NOISE DENSITY
vs TEMPERATURE**

**VOLTAGE NOISE DENSITY
vs SUPPLY VOLTAGE**

**CURRENT NOISE DENSITY
vs FREQUENCY**

**SUPPLY CURRENT vs
SUPPLY VOLTAGE**


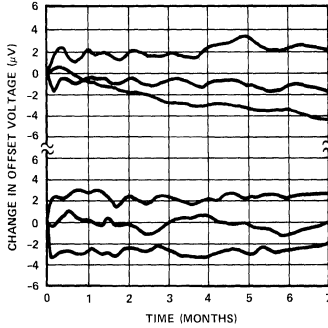


TYPICAL PERFORMANCE CHARACTERISTICS

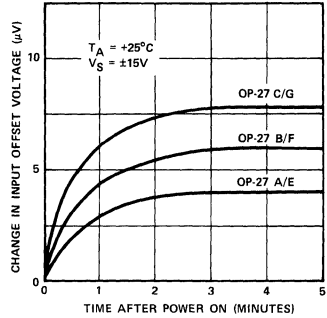
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



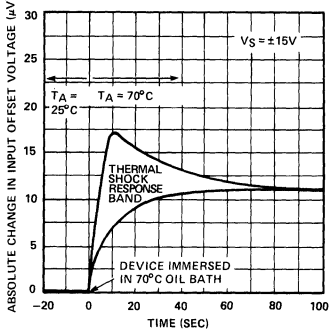
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



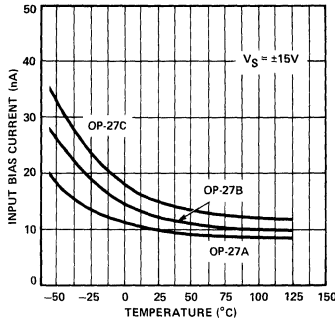
WARM-UP OFFSET VOLTAGE DRIFT



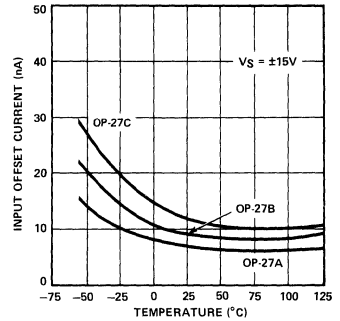
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



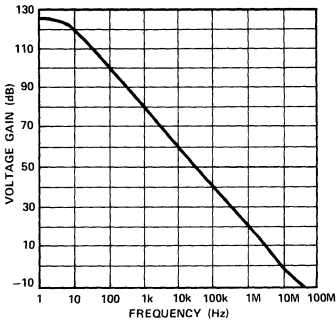
INPUT BIAS CURRENT vs TEMPERATURE



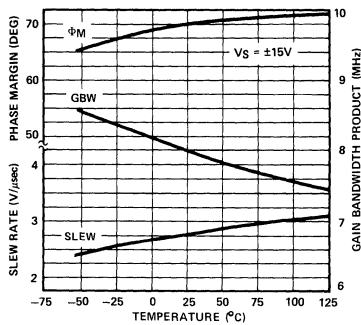
INPUT OFFSET CURRENT vs TEMPERATURE



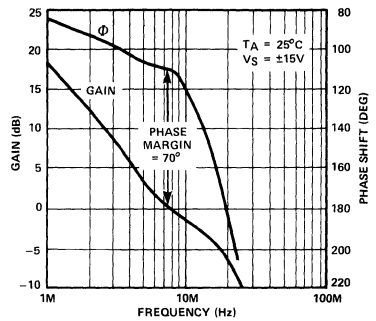
OPEN-LOOP GAIN vs FREQUENCY

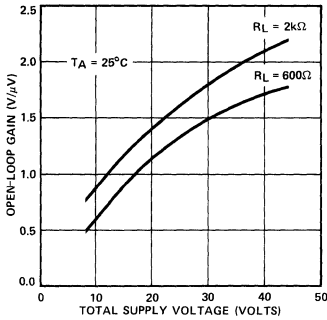
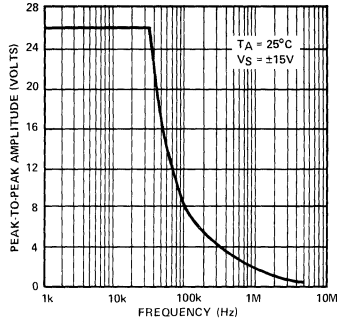
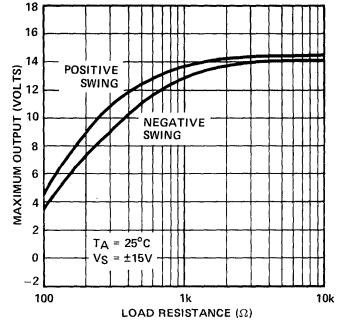
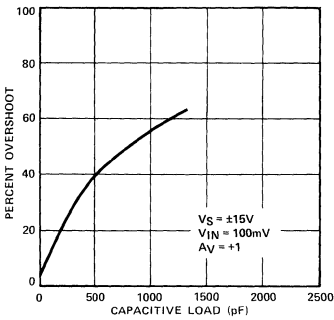
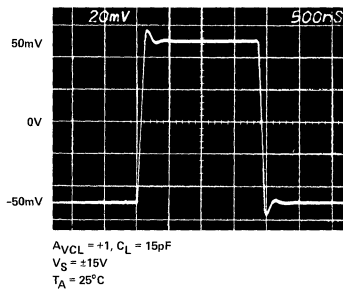
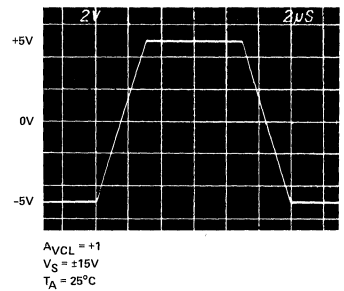
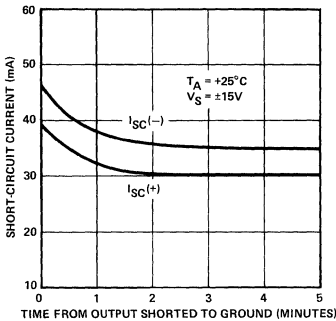
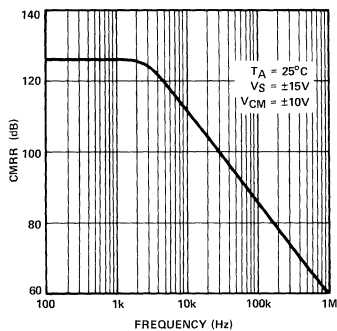
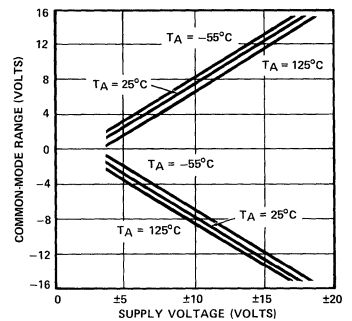


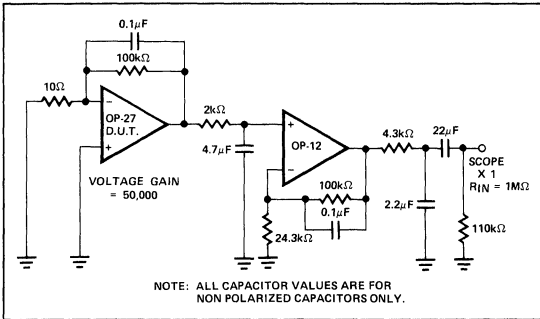
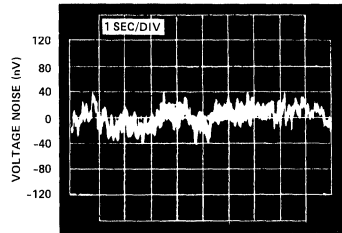
SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



GAIN, PHASE SHIFT vs FREQUENCY

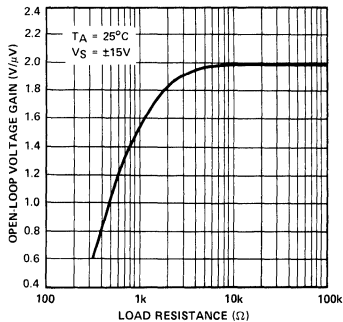
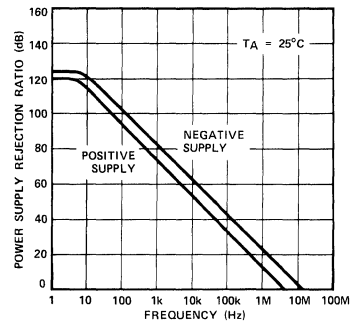


TYPICAL PERFORMANCE CHARACTERISTICS
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE

MAXIMUM OUTPUT SWING vs FREQUENCY

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

SMALL-SIGNAL TRANSIENT RESPONSE

LARGE-SIGNAL TRANSIENT RESPONSE

SHORT-CIRCUIT CURRENT vs TIME

CMRR vs FREQUENCY

COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE


TYPICAL PERFORMANCE CHARACTERISTICS
VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz)

LOW-FREQUENCY NOISE


0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE:
Observation time limited to 10 seconds.

OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE

PSRR vs FREQUENCY

APPLICATIONS INFORMATION

OP-27 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-27 may be fitted to unnullified 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-27 operation. OP-27 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see Offset Nulling Circuit).

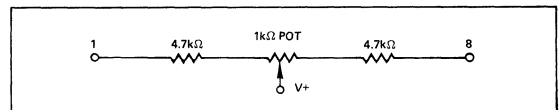
The OP-27 provides stable operation with load capacitances of up to 2000pF and $\pm 10V$ swings; larger capacitances should be decoupled with a 50 Ω resistor inside the feedback loop. The OP-27 is unity-gain stable.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-27 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10k Ω trim potentiometer may be used. TCV_{OS} is not degraded

(see Offset Nulling Circuit). Other potentiometer values from 1k Ω to 1M Ω can be used with a slight degradation (0.1 to 0.2 $\mu V/^{\circ}C$) of TCV_{OS} . Trimming to a value other than zero creates a drift of approximately ($V_{OS}/300$) $\mu V/^{\circ}C$. For example, the change in TCV_{OS} will be 0.33 $\mu V/^{\circ}C$ if V_{OS} is adjusted to 100 μV . The offset-voltage adjustment range with a 10k Ω potentiometer is $\pm 4mV$. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjunction with fixed resistors. For example, the network below will have a $\pm 280\mu V$ adjustment range.


NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-27 in the 0.1Hz to 10Hz range, the following precautions must be observed:

- (1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage

typically changes $4\mu\text{V}$ due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.

- (2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.
- (3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
- (4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.
- (5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the $1/f$ corner frequency.

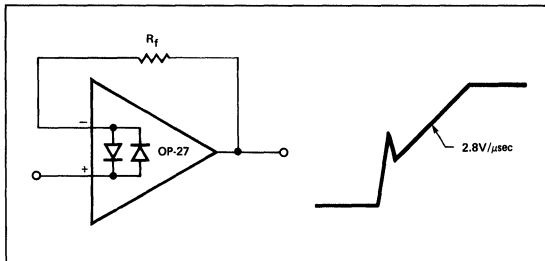
UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse ($>1\text{V}$), the output waveform will look as shown in the pulsed operation diagram below.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20\text{mA}$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 2\text{k}\Omega$, a pole will be created with R_f and the amplifier's input capacitance (8pF) that creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f will eliminate this problem.

PULSED OPERATION



COMMENTS ON NOISE

The OP-27 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-27 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-

bias-current cancellation circuit. The OP-27A/E has I_B and I_{OS} of only $\pm 40\text{nA}$ and 35nA respectively at 25°C . This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers prefer to use direct coupling. The high I_B , V_{OS} , TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-27's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-27 observed total noise with the noise performance of other devices in different circuit applications.

$$\text{Total noise} = [(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$$

Figure 1 shows noise-versus-source-resistance at 1000Hz . The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

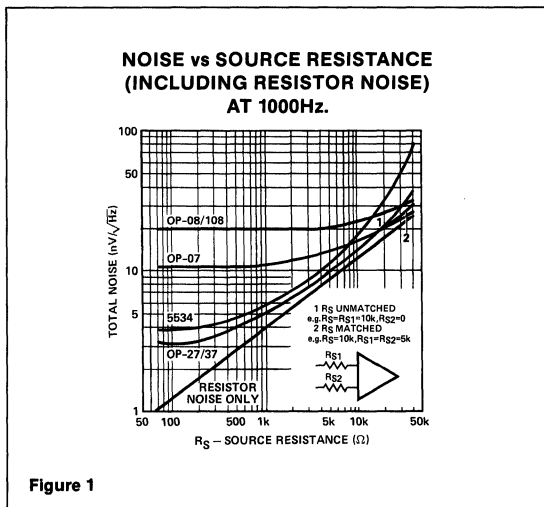


Figure 1

At $R_S < 1\text{k}\Omega$, the OP-27's low voltage noise is maintained. With $R_S > 1\text{k}\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of $20\text{k}\Omega$ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-27 and OP-07 and OP-08 noise occurs in the 15 -to- $40\text{k}\Omega$ region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3 -to- $5\text{k}\Omega$ range depending on whether balanced or unbalanced source resistors are used (at $3\text{k}\Omega$ the I_B , I_{OS} error also can be three times the V_{OS} spec.).

PEAK-TO-PEAK NOISE (0.1 to 10Hz) vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE).

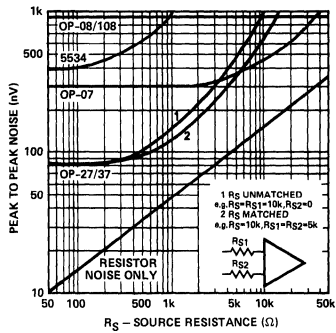


Figure 2

10Hz NOISE vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE).

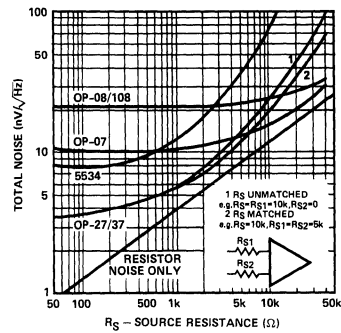


Figure 3

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-27 I_B can be neglected.
Magnetic differential phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-27 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

OPEN-LOOP GAIN

FREQUENCY AT:	OP-07	OP-27	OP-37
3Hz	100dB	124dB	125dB
10Hz	100dB	120dB	125dB
30Hz	90dB	110dB	124dB

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1 ; R_1 - R_2 - C_1 - C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.¹

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.⁴ (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values.)

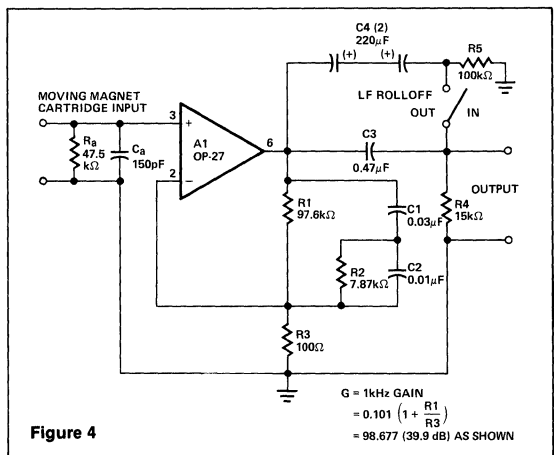


Figure 4

5 OPERATIONAL AMPLIFIERS

The OP-27 brings a $3.2nV/\sqrt{Hz}$ voltage noise and $0.45 pA/\sqrt{Hz}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω , which generates a voltage noise of $1.3nV/\sqrt{Hz}$. The noise increases the $3.2nV/\sqrt{Hz}$ of the amplifier by only 0.7dB. With a $1k\Omega$ source, the circuit noise measures 63dB below a $1mV$ reference level, unweighted, in a $20kHz$ noise bandwidth.

Gain (G) of the circuit at $1kHz$ can be calculated by the expression:

$$G = 0.101 \left(1 + \frac{R_1}{R_3} \right)$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3 , but gains higher than 40dB will show more equalization errors because of the $8MHz$ gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to $7V$ rms. At $3V$ output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to $20kHz$.

Capacitor C_3 and resistor R_4 form a simple -6dB-per-octave rumble filter, with a corner at $22Hz$. As an option, the switch-selected shunt capacitor C_4 , a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

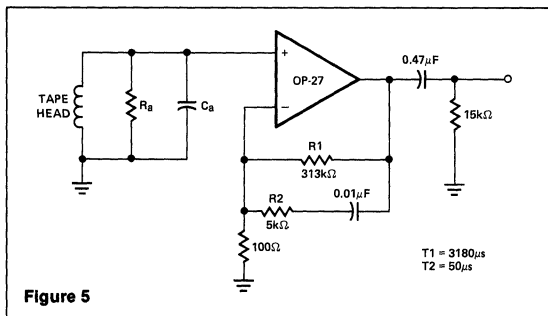


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above $3kHz$ ($T_2 = 50\mu s$), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.⁵

The network values of the configuration yield a $50dB$ gain at $1kHz$, and the dc gain is greater than $70dB$. Thus, the worst-case output offset is just over $500mV$. A single $0.47\mu F$ output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of $80nA$ with a $400mH$, $100 \mu in.$ head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below $1k\Omega$. For this configuration, the bias-current-induced offset voltage can be greater than the $100\mu V$ maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by $50dB$, and has an input impedance of $2k\Omega$. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be $110kHz$. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p , may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a $4nV/\sqrt{Hz}$ noise, while the op amp generates a $3.2nV/\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about $6nV/\sqrt{Hz}$, equivalent to $0.9\mu V$ in a $20kHz$ noise bandwidth, or nearly $61dB$ below a $1mV$ input signal. Measurements confirm this predicted performance.

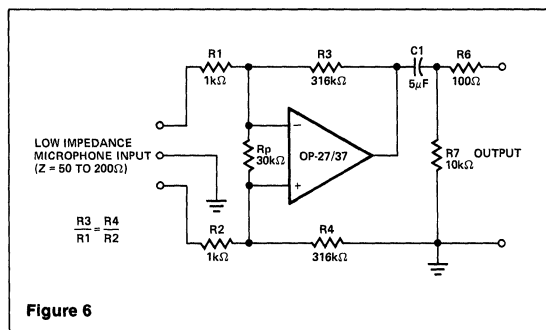


Figure 6

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally-compensated OP-27. T_1 is a JE-115K-E 150 Ω /15k Ω transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

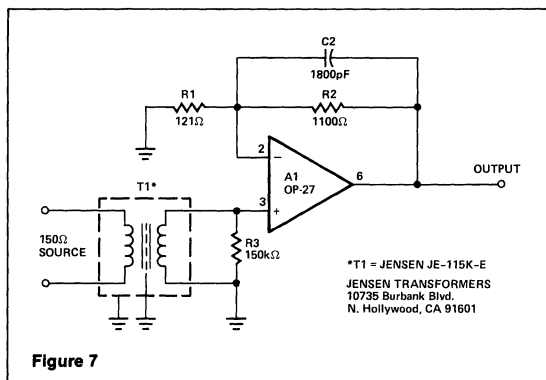


Figure 7

Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1 . Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a 40dB gain. The typical output blocking capacitor can be

eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

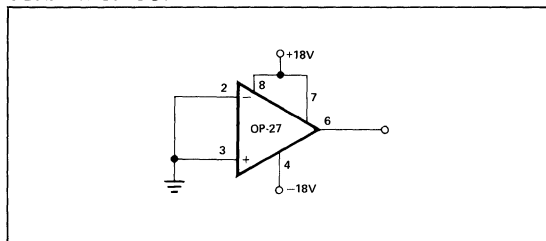
Capacitor C_2 and resistor R_2 form a 2 μ s time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2 μ s time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150 Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or -69.5 referenced to 1mV).

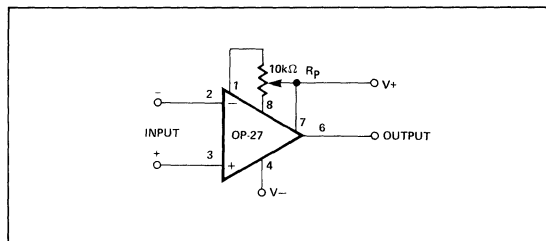
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3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Ota, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



5 OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

FEATURES

- Programmable Supply Current $1\mu A$ to $2mA$
- Single Supply Operation $+3V$ to $+30V$
- Dual Supply Operation $\pm 1.5V$ to $\pm 15V$
- Low Input Offset Voltage $100\mu V$
- Low Input Offset Voltage Drift $0.5\mu V/^\circ C$
- High Common-Mode Input Range ... $V-$ to $V+$ ($-1.5V$)
- High CMRR and PSRR $115dB$
- High Open-Loop Gain $2000V/mV$
- $\pm 30V$ Input Overvoltage Protection
- Fast $1V/\mu s$ @ $I_{SY} = 300\mu A$
- LM4250 Pinout
- Compensated for Minimum Gain of 10

ORDERING INFORMATION†

$T_A = 25^\circ C$ $V_{OS} \text{ MAX}$ (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	EPOXY DIP 8-PIN	HERMETIC DIP 8-PIN	
300	—	OP32AZ*	MIL
300	OP32EP	OP32EZ	IND
500	—	OP32BZ*	MIL
500	OP32FP	OP32FZ	IND
1000	OP32GP	OP32GZ	IND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-32 is a high-speed, high-gain programmable operational amplifier. Both offset voltage and offset current are

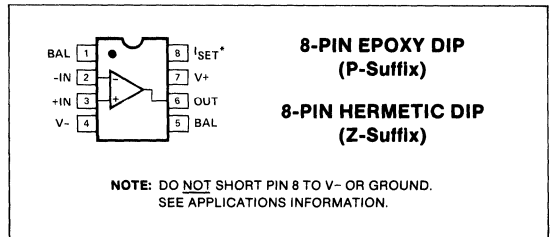
low, and both are stable with changes in temperature, supply voltage, and set current. High CMRR and PSRR ensure precision performance when the OP-32 is used with an unregulated battery or vehicular electrical system.

The wide input voltage range, including the negative supply or ground, allows use in single-battery applications. The OP-32 is characterized over a wide supply range of $\pm 1.5V$ to $\pm 15V$. This guarantees predictable performance with any commonly available supply.

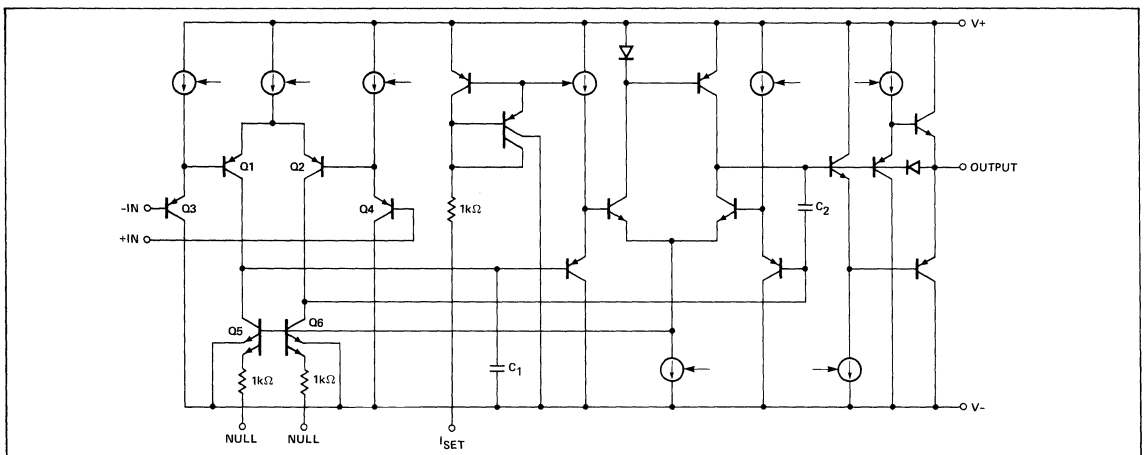
The ability to operate at relatively high speed with low power consumption makes this amplifier ideal for remote applications where power is limited. The programmability allows each amplifier in a system to be set for the minimum power consumption necessary for each specific application. Programmability also makes it possible to adjust the bandwidth and phase shift.

The OP-32 pinout is identical to the LM4250 and many other micropower operational amplifiers. This allows easy upgrading of system performance.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±18V
Power Dissipation	500mW
Differential Input Voltage	±30
Input Voltage	Supply Voltage
Storage Temperature Range	
Z Package	-65°C to +150°C
P Package	-55°C to +125°C

Operating Temperature Range

OP-32A, B (Z package)	-55°C to +125°C
OP-32E, F & G (Z or P package)	-25°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to +150°C

NOTE:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32A/E			OP-32B/F			OP-32G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	μV
Input Offset current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	—	—	3	nA
Input Bias Current (Note 1)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	—	5	10	nA
		$I_{SY} = 150\mu A$	—	20	35	—	24	35	—	30	50	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	—	80	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15.0/13.5	—	—	-15.0/13.5	—	—	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 2)	CMRR	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.5V$	100	115	—	95	110	—	85	100	—	dB
Power Supply Rejection Ratio (Note 2)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$; and $V_- = 0V$, $V_+ = 3V$ to $30V$.	—	1	6	—	3	12	—	10	25	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	1000	2000	—	750	1500	—	500	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	$\pm 0.8 \pm 0.88$			$\pm 0.8 \pm 0.88$			$\pm 0.75 \pm 0.85$			V
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	$\pm 14 \pm 14.2$			$\pm 14 \pm 14.2$			$\pm 13.8 \pm 14.2$			V
Gain-Bandwidth Product		$I_{SY} = 15\mu A$, $R_L = 100k\Omega$	—	100	—	—	100	—	—	100	—	kHz
		$I_{SY} = 450\mu A$, $R_L = 10k\Omega$	—	4500	—	—	4500	—	—	4500	—	
Slew Rate	SR	$V_S = \pm 15V$, $I_{SY} = 450\mu A$, $R_L = 10k\Omega$	—	1.5	—	—	1.5	—	—	1.5	—	V/ μs
Supply Current No Load (Note 3)	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	15	17	—	15	19	—	15	21	μA
		$I_{SET} = 10\mu A$	—	150	170	—	150	190	—	150	200	
		$I_{SET} = 30\mu A$	—	450	525	—	450	600	—	450	650	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	10.5	12.5	—	11	15	—	11	18	μA
		$I_{SET} = 10\mu A$	—	105	125	—	110	150	—	110	180	
		$I_{SET} = 30\mu A$	—	350	400	—	350	450	—	350	500	

NOTES:

1. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. PSRR and CMRR measured with V_{OS} unnullled and I_{SET} held constant.
3. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V_+) - (V_-)}{6}$$

The range of I_{SY}/I_{SET} is approximately 10.5 to 15 over the specified operating range of $V_S = \pm 1.5V$ to $V_S = \pm 15V$.

5
OPERATIONAL AMPLIFIERS



ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32A			OP-32B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnull'd	—	0.5	2.0	—	1.0	2.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	175	400	—	350	600	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	nA
Average Input Offset Current Drift	TCI_{OS}	(Notes 1, 2)	—	1	10	—	3	15	$pA/^\circ C$
Input Bias Current (Note 2)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	nA
		$I_{SY} = 150\mu A$	—	20	35	—	25	35	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15.0/13.5	—	—	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.5V$							dB
		$I_{SET} = 10\mu A$	90	110	—	86	105	—	
		$I_{SET} = 1\mu A$	80	90	—	80	90	—	
Power Supply Rejection Ratio (Note 3)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V_- = 0V$, $V_+ = 3V$ to $30V$ ($V_{CM} = 1.5V$)	—	2	10	—	2.5	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	200	400	—	200	500	—	V/mV
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	500	1000	—	300	750	—	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 0.65	± 0.75	—	± 0.65	± 0.75	—	V
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$							
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 13.6	± 14.0	—	± 13.0	± 13.5	—	V
Supply Current No Load (Note 4)	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	16	18	—	16	20	μA
		$I_{SET} = 10\mu A$	—	160	180	—	160	200	
		$I_{SET} = 30\mu A$	—	450	550	—	450	600	μA
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	12	14	—	12	17	
		$I_{SET} = 10\mu A$	—	120	140	—	120	170	μA
		$I_{SET} = 30\mu A$	—	360	450	—	360	500	μA

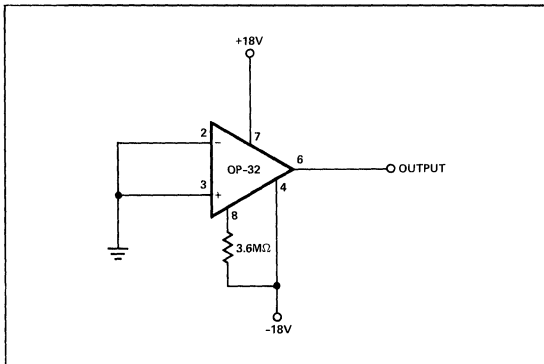
NOTES:

1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.
3. PSRR and CMRR measured with V_{OS} unnull'd and I_{SET} held constant.

4. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V_+) - (V_-)}{6}$$

BURN-IN CIRCUIT*



*Other circuits may apply at PMI's discretion.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

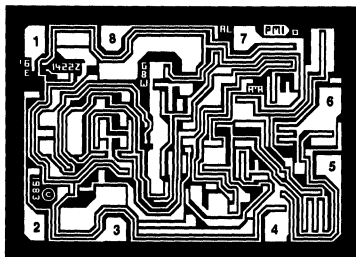
PARAMETER	SYMBOL	CONDITIONS	OP-32E			OP-32F			OP-32G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnull'd	—	0.5	1.5	—	1.0	2.0	—	1.5	3.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	100	400	—	200	600	—	500	1200	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	—	—	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Notes 1, 2)	—	2	10	—	3	15	—	5	25	$pA/^\circ C$
Input Bias Current (Note 2)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	—	5	10	nA
		$I_{SY} = 150\mu A$	—	20	35	—	24	35	—	30	50	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	—	80	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15.0/13.5	—	—	-15.0/13.5	—	—	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$V_S = \pm 15V$ & $-15V \leq V_{CM} \leq +13.5V$	95	110	—	90	105	—	80	100	—	dB
Power Supply Rejection Ratio (Note 3)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V_- = 0V$, $V_+ = 3V$ to $30V$	—	3.2	10	—	10	32	—	32	56	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	750	1000	—	500	1000	—	400	1000	—	V/mV
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	750	1000	—	500	1000	—	400	1000	—	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	± 0.70	± 0.75	—	± 0.65	± 0.75	—	± 0.6	± 0.7	—	V
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	± 13.8	± 14.1	—	± 13.6	± 14.1	—	± 13.0	± 14.0	—	V
Supply Current No Load (Note 4)	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	16	18	—	16	20	—	16	25	μA
		$I_{SET} = 10\mu A$	—	160	180	—	160	200	—	160	250	
		$I_{SET} = 30\mu A$	—	450	550	—	450	600	—	450	650	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	12	14	—	12	17	—	12	25	
		$I_{SET} = 10\mu A$	—	120	140	—	120	170	—	120	200	μA
		$I_{SET} = 30\mu A$	—	360	450	—	360	500	—	360	550	

NOTES:

- Sample tested.
- I_B and I_{OS} are measured at $V_{CM} = 0$.
- PSRR and CMRR measured with V_{OS} unnull'd and I_{SET} held constant.
- The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V_+) - (V_-)}{6}$$

5
OPERATIONAL AMPLIFIERS

DICE CHARACTERISTICS


**DIE SIZE 0.069 × 0.049 inch, 3381 sq. mils
(1.75 × 1.24 mm, 2.18 sq. mm)**

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
5. BALANCE
6. OUTPUT
7. V+
8. ISET

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32N LIMIT	OP-32G LIMIT	OP-32GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	500	1000	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	2	2	3	nA MAX
Input Bias Current (Note 1)	I_B	$I_{SY} = 15\mu A$	5	7.5	10	nA MAX
		$I_{SY} = 150\mu A$	35	35	50	
		$I_{SY} = 450\mu A$	90	100	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio (Note 2)	CMRR	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.5V$	100	95	85	dB MIN
Power Supply Rejection Ratio (Note 2)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V_- = 0V, V_+ = 3V$ to $30V$	6	12	25	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega, I_{SY} = 15\mu A$	1000	750	500	V/mV MIN
		$R_L = 10k\Omega, 150\mu A \leq I_{SY} \leq 450\mu A$	1000	750	500	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega, I_{SY} = 15\mu A$	± 0.8	± 0.8	± 0.75	V MIN
		$R_L = 10k\Omega, 150\mu A \leq I_{SY} \leq 450\mu A$				
		$V_S = \pm 15V$ $R_L = 100k\Omega, I_{SY} = 15\mu A$	± 14	± 14	± 13.8	V MIN
Supply Current No Load (Note 3)	I_{SY}	$V_S = \pm 1.5V, I_{SET} = 1\mu A$	12.5	15	18	μA MAX
		$I_{SET} = 10\mu A$	125	150	180	
		$I_{SET} = 30\mu A$	400	450	500	
		$V_S = \pm 15V, I_{SET} = 1\mu A$	17	19	21	
		$I_{SET} = 10\mu A$	170	190	200	μA MAX
		$I_{SET} = 30\mu A$	525	600	650	

NOTES:

1. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. PSRR and CMRR measured with V_{OS} unnullled and I_{SET} held constant.
3. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

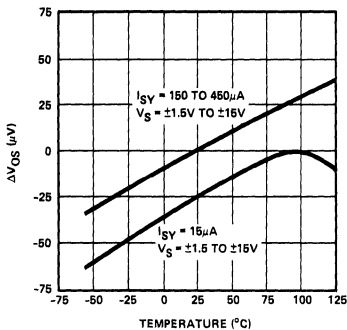
$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V_+) - (V_-)}{6}$$

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

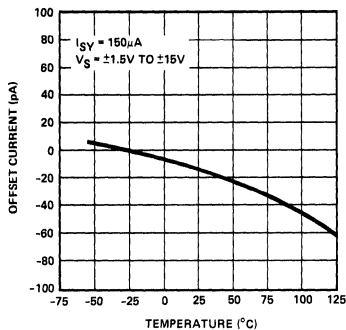


TYPICAL DC PERFORMANCE CHARACTERISTICS

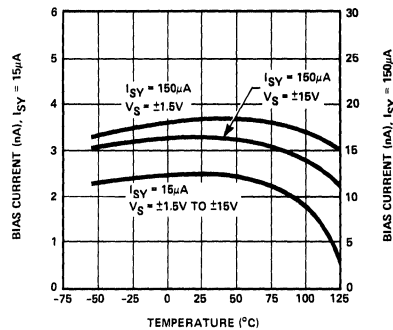
OFFSET VOLTAGE vs TEMPERATURE



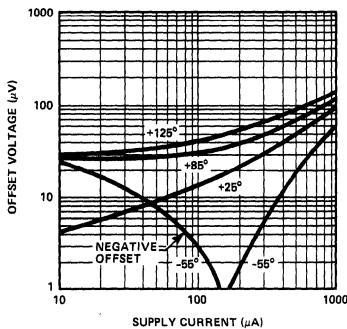
OFFSET CURRENT vs TEMPERATURE



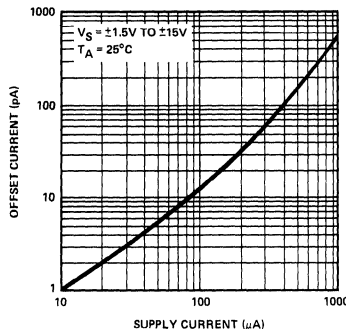
BIAS CURRENT vs TEMPERATURE



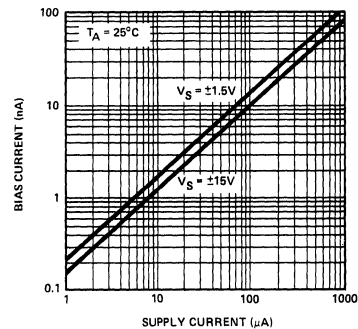
OFFSET VOLTAGE vs SUPPLY CURRENT



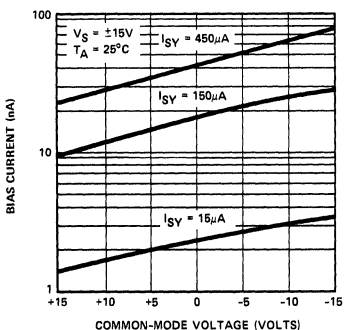
OFFSET CURRENT vs SUPPLY CURRENT



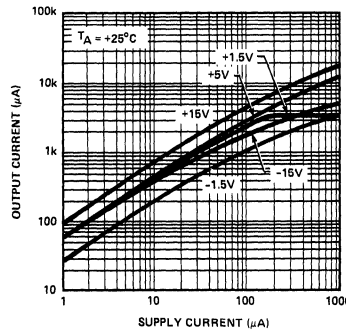
BIAS CURRENT vs SUPPLY CURRENT



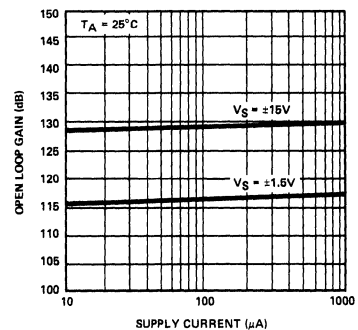
BIAS CURRENT vs COMMON-MODE VOLTAGE



MAXIMUM OUTPUT CURRENT vs SUPPLY CURRENT AT VS = ±15V, +5V AND ±1.5V

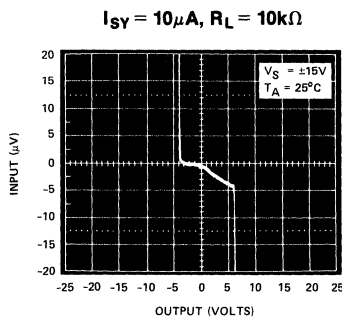
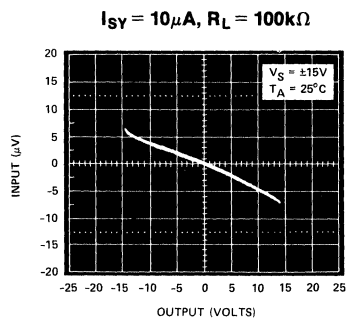
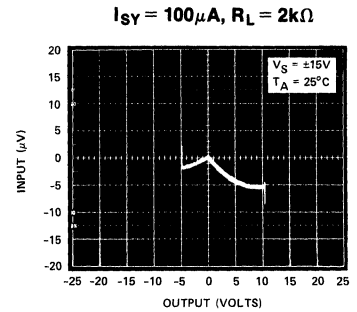
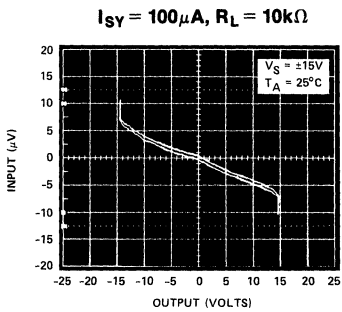
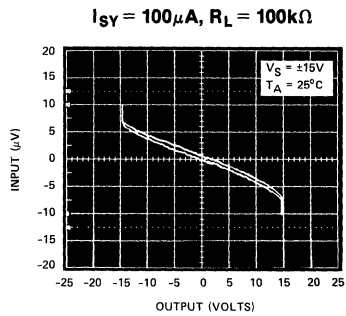
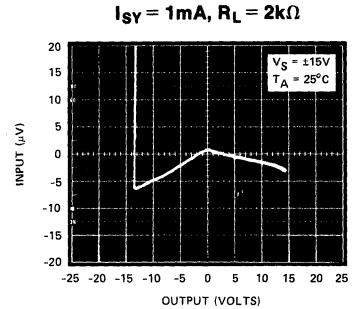
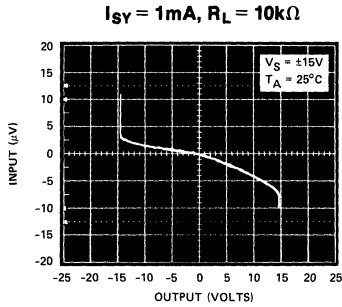
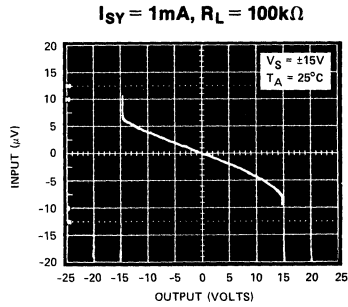


OPEN-LOOP GAIN vs SUPPLY CURRENT

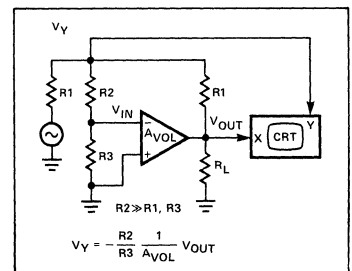


5 OPERATIONAL AMPLIFIERS

TYPICAL DC OPEN-LOOP INPUT-OUTPUT CHARACTERISTICS

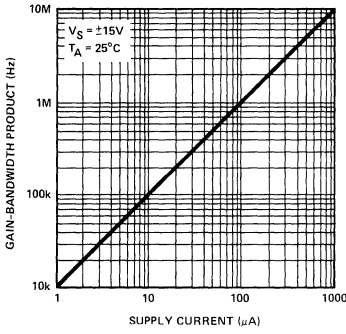


TEST CIRCUIT

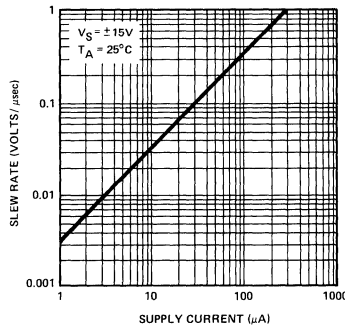


TYPICAL AC PERFORMANCE CHARACTERISTICS

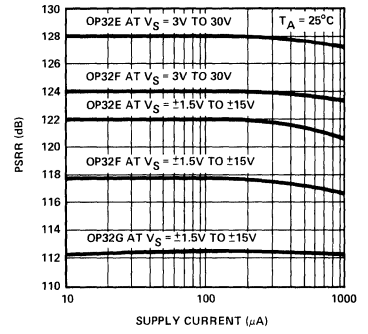
GAIN-BANDWIDTH PRODUCT vs SUPPLY CURRENT



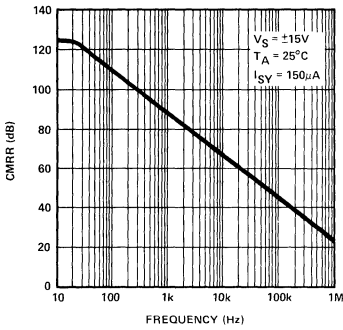
SLEW RATE vs SUPPLY CURRENT



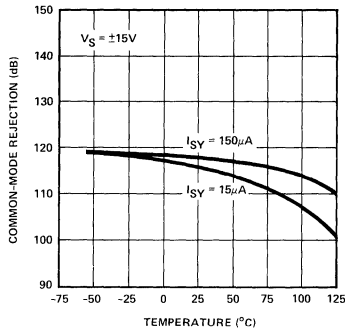
POWER SUPPLY REJECTION vs SUPPLY CURRENT



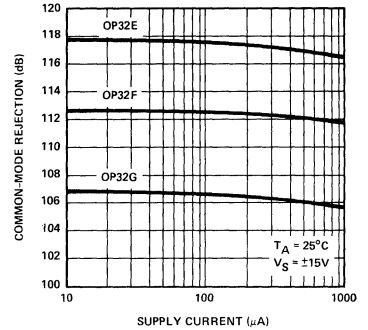
COMMON-MODE REJECTION vs FREQUENCY



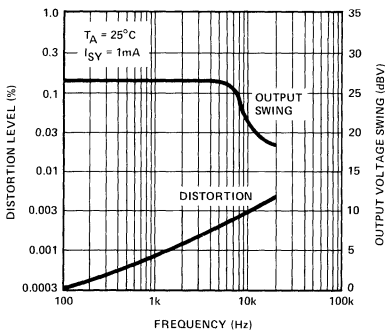
COMMON-MODE REJECTION vs TEMPERATURE



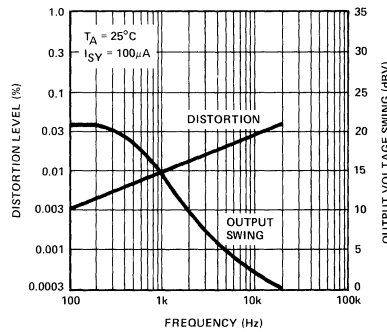
COMMON-MODE REJECTION vs SUPPLY CURRENT



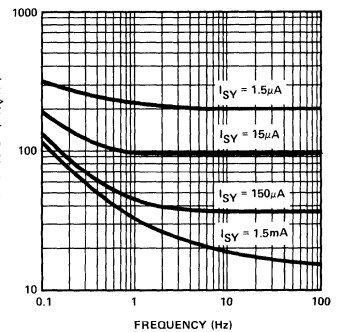
TOTAL HARMONIC DISTORTION vs FREQUENCY



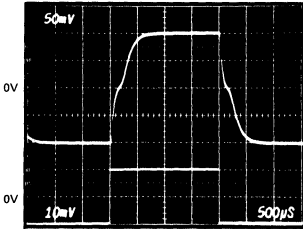
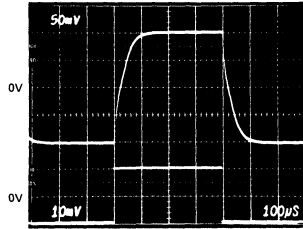
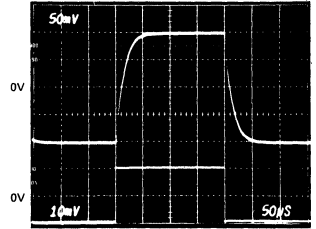
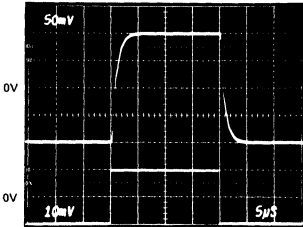
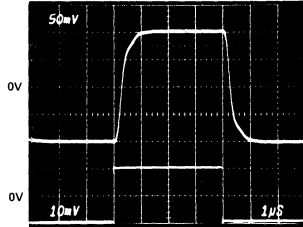
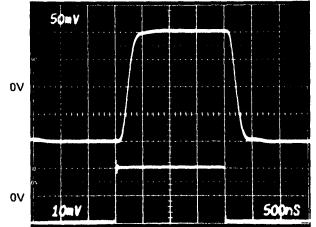
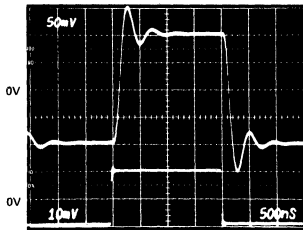
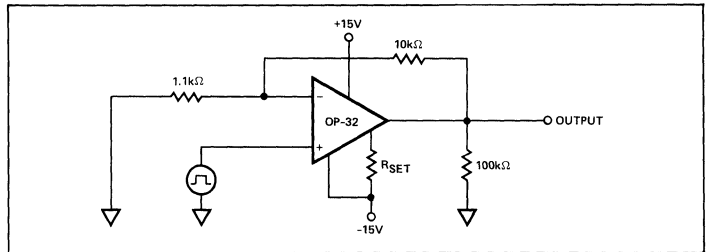
TOTAL HARMONIC DISTORTION vs FREQUENCY



VOLTAGE NOISE vs FREQUENCY

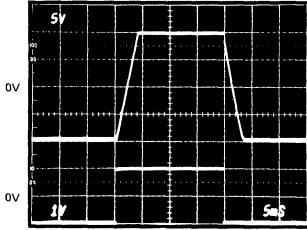
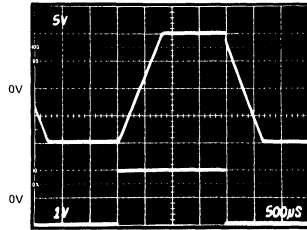
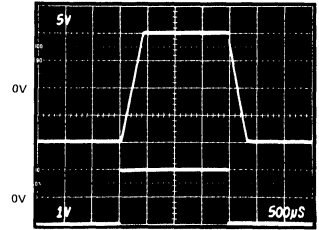
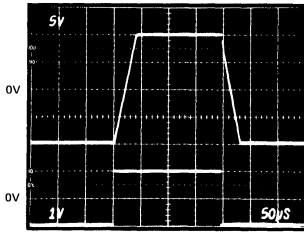
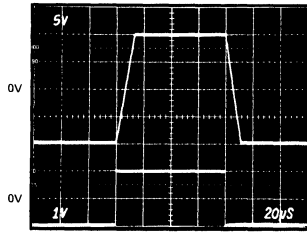
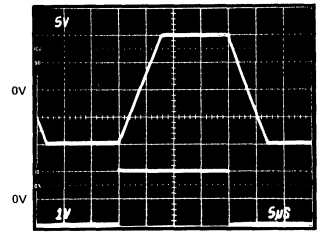
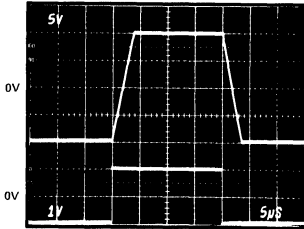
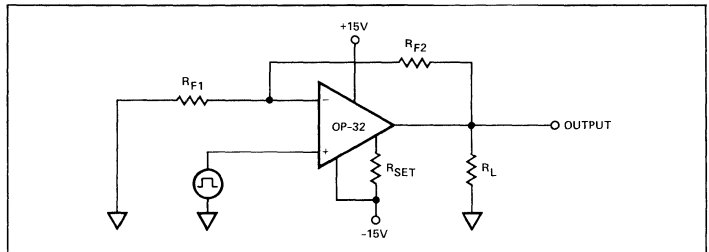


TYPICAL AC PERFORMANCE CHARACTERISTICS
SMALL-SIGNAL TRANSIENT RESPONSE vs SUPPLY CURRENT

 $I_{SY} = 1.5\mu A$

 $I_{SY} = 7.5\mu A$

 $I_{SY} = 15\mu A$

 $I_{SY} = 150\mu A$

 $I_{SY} = 450\mu A$

 $I_{SY} = 750\mu A$

 $I_{SY} = 1.5mA$

TEST CIRCUIT


TYPICAL AC PERFORMANCE CHARACTERISTICS

LARGE-SIGNAL TRANSIENT RESPONSE vs SUPPLY CURRENT

 $I_{SY} = 1.5\mu A$

 $R_{F1} = 110k\Omega, R_{F2} = 1M\Omega, R_L = OPEN$
 $I_{SY} = 7.5\mu A$

 $R_{F1} = 11k\Omega, R_{F2} = 100k\Omega, R_L = 1M\Omega$
 $I_{SY} = 15\mu A$

 $R_{F1} = 11k\Omega, R_{F2} = 100k\Omega, R_L = 1M\Omega$
 $I_{SY} = 150\mu A$

 $R_{F1} = 1.1k\Omega, R_{F2} = 10k\Omega, R_L = 100k\Omega$
 $I_{SY} = 450\mu A$

 $R_{F1} = 1.1k\Omega, R_{F2} = 10k\Omega, R_L = 100k\Omega$
 $I_{SY} = 750\mu A$

 $R_{F1} = 1.1k\Omega, R_{F2} = 10k\Omega, R_L = 100k\Omega$
 $I_{SY} = 1.5mA$

 $R_{F1} = 1.1k\Omega, R_{F2} = 10k\Omega, R_L = 100k\Omega$
TEST CIRCUIT


APPLICATIONS INFORMATION

SETTING SUPPLY CURRENT

The op amp power supply current is determined by the current flowing out of pin 8. Pin 8 is at the $V+$ voltage less two diode drops, which is approximately $V+$ minus 1.1V. Do not connect pin 8 to ground or $V-$ without a set resistor in series or excessive supply current will be drawn which may damage the OP-32.

The set resistor value is selected to make the power supply current optimum for the specific application. Adjusting the OP-32 power supply current determines the slew-rate, bandwidth, and the output current limits (see Performance Characteristics). The supply current is nominally 15 times the set current and the set resistor value is calculated from:

$$R_S = \frac{(V_{\text{SUPPLY}} - 1.1V)}{I_{\text{SET}}}, \text{ where } I_{\text{SY}} \approx 15 I_{\text{SET}} \quad (\text{See graph below})$$

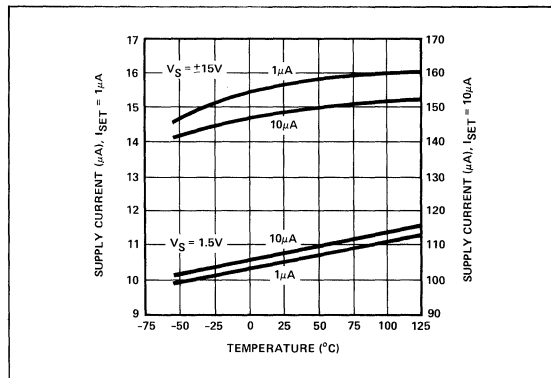
Note that the set resistor can go to either negative supply or to ground. If the set resistor goes to negative supply, then $V_{\text{SUPPLY}} = (V+) - (V-)$. For a single-supply circuit, V_{SUPPLY} is simply $(V+)$. If the supply voltage varies widely, set current can be stabilized with circuits (a), (b), or (c).

The relationship between supply voltage, supply current and set current can be approximated by:

$$\frac{I_{\text{SY}}}{I_{\text{SET}}} \approx 10 + \frac{(V+) - (V-)}{6} \quad (T_A = 25^\circ\text{C})$$

The ratio $\frac{I_{\text{SY}}}{I_{\text{SET}}}$ increases with temperature by approximately 0.05%/°C.

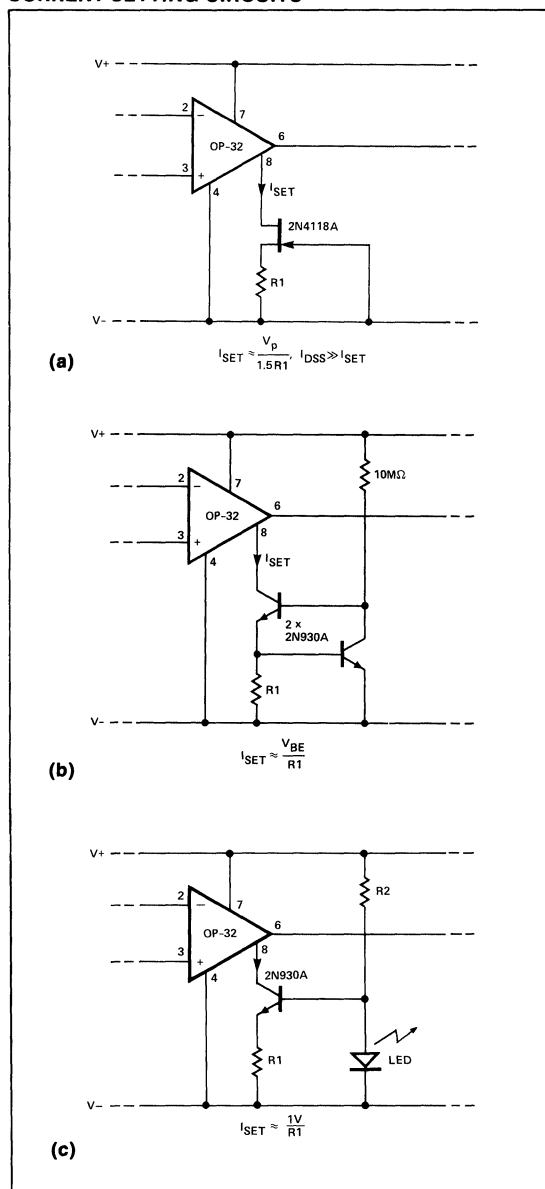
SUPPLY CURRENT vs TEMPERATURE

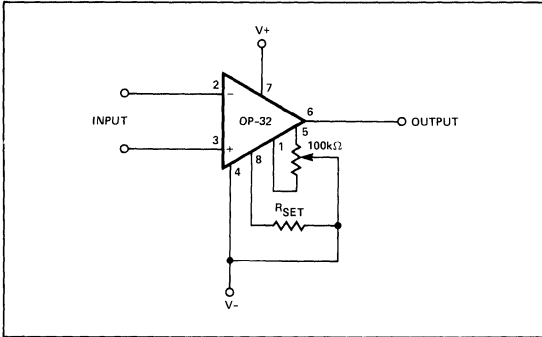


INPUT BIAS CURRENT

Input bias current varies directly with set current. The set current required for a given supply current ranges from $I_{\text{SY}}/10.5$ at $\pm 1.5V$ supply voltage to $I_{\text{SY}}/15$ at $\pm 15V$. Therefore, I_B will be highest at the minimum supply voltage condition of $\pm 1.5V$ (or 3V) for any given supply current.

CURRENT SETTING CIRCUITS



OFFSET NULLING CIRCUIT

OFFSET VOLTAGE ADJUSTMENT

The offset voltage can be trimmed to zero using a 100kΩ potentiometer (see offset nulling circuit). Adjusting the pot wiper towards pin 5 causes the output to go positive. Adjustment range is approximately $\pm 5\text{mV}$ at $V_S = \pm 15\text{V}$. The V_{OS} adjust range is proportional to supply voltage. Resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors.

If power supply voltages vary widely and the set current is established by a resistor, the op amp supply currents will vary in proportion to the supply voltage changes. V_{OS} will remain almost constant with supply current changes if the null pins (1 and 5) are not used. If a V_{OS} adjust pot is used, current variations may flow through the offset pot causing an apparent V_{OS} change. If a V_{OS} adjust pot is used in combination with widely-varying supply voltages, a set-current stabilizer circuit as shown in (a), (b), or (c) is recommended.

APPLICATIONS EXAMPLE
BATTERY-POWERED, GAIN-OF-100 AMPLIFIER

The simple noninverting amplifier circuit shown in Figure 1 provides an accurate gain-of-100 while operating from a pair of 9V batteries. The circuit requires only $15\mu\text{A}$ of supply current. Slew-rate is approximately $0.06\text{V}/\mu\text{sec}$ and output swing is $\pm 8\text{V}$.

A value of $500\text{k}\Omega$ was chosen for R_2 . For a gain of 100, R_1 is calculated as:

$$A_{VCL} = 1 + \frac{R_2}{R_1}$$

$$100 = 1 + \frac{500\text{k}\Omega}{R_1}$$

$$\therefore R_1 = 5.05\text{k}\Omega$$

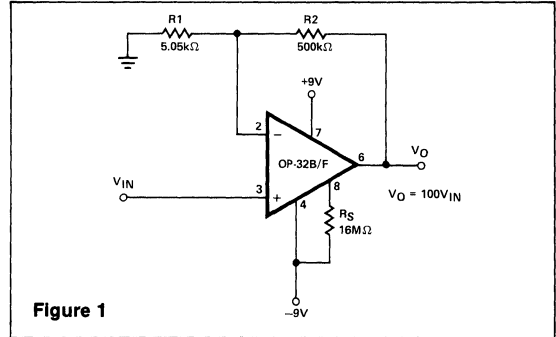
BATTERY-POWERED, GAIN-OF-100 AMPLIFIER


Figure 1

Using an OP-32B/F, we can expect an $I_B + I_{OS}/2$ of less than 8.5nA when operating at I_{SY} of $15\mu\text{A}$, so the input offset caused by $I_B R_1$ will be negligible ($8.5\text{nA} \times 5.05\text{k}\Omega \sim 43\mu\text{V}$).

The set resistor R_S needed for a supply current of $15\mu\text{A}$ is calculated from:

$$R_S = \frac{V_{SUPPLY} - 1.1\text{V}}{I_{SY}/15} = \frac{18\text{V} - 1.1\text{V}}{1\mu\text{A}}$$

$$\therefore R_S = 16.9\text{M}\Omega$$

Offset voltage adjustment is optional. An OP-32B/F has maximum input offset voltage of $500\mu\text{V}$ which would cause an output offset voltage of 50mV . Drift over temperature is very low, typically less than $1.0\mu\text{V}/^\circ\text{C}$, and is guaranteed to be less than $2.0\mu\text{V}/^\circ\text{C}$. PSRR is also low, only $6\mu\text{V}/\text{V}$, so battery voltage change has negligible effect on offset.

Most micropower programmable op amps lose open-loop gain and CMRR at low supply currents. The OP-32 design overcomes these limitations so accuracy is maintained at supply currents of only a few microamps. The OP-32B/F used in this example has a minimum open-loop gain of over 117dB. Gain error due to finite open-loop gain will be less than $100/750,000$, which is only 133PPM. CMRR will typically be 110dB, an error of 3PPM. Gain accuracy of the circuit is almost entirely dependent on the accuracy of the R_1/R_2 ratio; the op amp contributes less than 0.015% gain error.

Considering all error sources, this simple $\times 100$ battery-powered circuit using an OP-32B/F is capable of achieving excellent accuracy. Without external adjustments of any kind, output offset will be less than 54mV and gain accuracy will be better than $\pm 0.015\%$ (exclusive of R_2/R_1 error). Gain linearity, slew-rate symmetry, and stability over temperature are all excellent with the OP-32, making circuit performance very predictable.

Precision Monolithics Inc.

FEATURES

- **Low Noise** 80nV p-p (0.1Hz to 10Hz) $3nV/\sqrt{Hz}$ at 1kHz
- **Low Drift** $0.2\mu V/^\circ C$
- **High Speed** 17V/ μs Slew Rate 63MHz Gain Bandwidth
- **Low Input Offset Voltage** 10 μV
- **Excellent CMRR** ... 126dB (Common-Voltage of $\pm 11V$)
- **High Open-Loop Gain** 1.8 Million
- **Replaces 725, OP-05, OP-06, OP-07, AD510, AD517, SE5534 in Gains > 5**

ORDERING INFORMATION†

$T_A = 25^\circ C$ $V_{OS} \text{ MAX}$ (μV)	PACKAGE				OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	LCC	
25	OP37AJ*	OP37AZ*			MIL
25	OP37EJ	OP37EZ	OP37EP		IND/COM
60	OP37BJ*	OP37BZ*		OP37BRC/883	MIL
60	OP37FJ	OP37FZ	OP37FP		IND/COM
100	OP37CJ*	OP37CZ*			MIL
100	OP37GJ	OP37GZ	OP37GP		IND/COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-37 provides the same high performance as the OP-27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17V/ μs and gain-bandwidth product to 63MHz.

The OP-37 provides the low offset and drift of the OP-07 plus higher speed and lower noise. Offsets down to 25 μV and drift of 0.6 $\mu V/^\circ C$ maximum make the OP-37 ideal for precision instrumentation applications. Exceptionally low noise

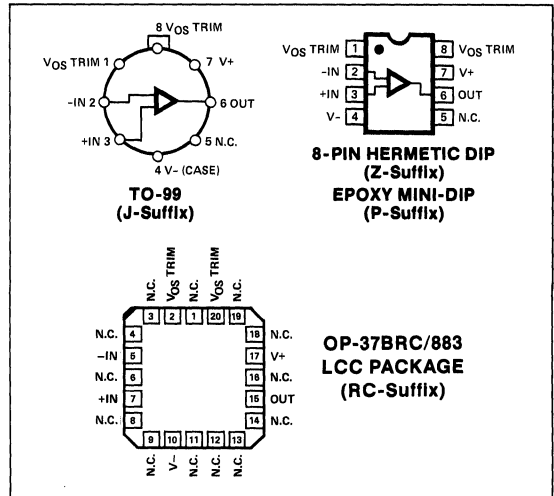
($e_n = 3.5nV/\sqrt{Hz}$ at 10Hz), a low 1/f noise corner frequency of 2.7Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low-level signals.

The low input bias current of $\pm 10nA$ and offset current of 7nA are achieved by using a bias-current-cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to $\pm 20nA$ and 15nA respectively.

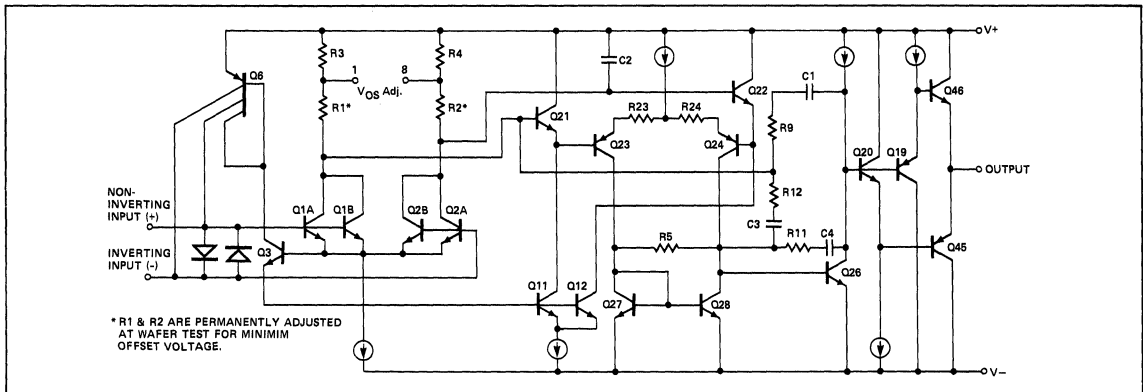
The output stage has good load driving capability. A guaranteed swing of $\pm 10V$ into 800 Ω and low output distortion make the OP-37 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2 μV /month, allow the circuit

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the OP-37 is achieved by using on-chip zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tape-head, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	-65°C to +150°C

Operating Temperature Range

OP-37A, OP-37B, OP-37C (J, Z, RC) -55°C to +125°C
OP-37E, OP-37F, OP-37G (J, Z) -25°C to +85°C
OP-37E, OP-37F, OP-37G (P) 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) 300°C
DICE Junction Temperature -65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C
LCC	80°C	7.8mW/°C

- The OP-37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
- For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37A/E			OP-37B/F			OP-37C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	$V_{OS}/Time$	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	$\mu Vp-p$
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	nV/\sqrt{Hz}
		$f_O = 30Hz$ (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		$f_O = 1000Hz$ (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	$f_O = 10Hz$ (Notes 3, 6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	pA/\sqrt{Hz}
		$f_O = 30Hz$ (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		$f_O = 1000Hz$ (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	G Ω
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSSR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 1k\Omega$, $V_O = \pm 10V$	800	1500	—	800	1500	—	400	1500	—	
		$R_L = 600\Omega$, $V_O = \pm 1V$, $V_S = \pm 4V$, (Note 4)	250	700	—	250	700	—	200	500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.0 ±10.0	±13.8 ±11.5	—	±12.0 ±10.0	±13.8 ±11.5	—	±11.5 ±10.0	±13.5 ±11.5	—	V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	11	17	—	11	17	—	11	17	—	V/ μs
Gain Bandwidth Prod.	GBW	$f_O = 10kHz$ (Note 4)	45	63	—	45	63	—	45	63	—	MHz
		$f_O = 1MHz$	—	40	—	—	40	—	—	40	—	

5
OPERATIONAL AMPLIFIERS



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-37A/E			OP-37B/F			OP-37C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Open-Loop Output Resistance	R_O	$V_O = 0, I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	$V_O = 0$	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_p = 10k\Omega$	—	± 4.0	—	—	± 4.0	—	—	± 4.0	—	mV

NOTES:

- Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
- Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$ — refer to typical performance curve.
- Sample tested.
- Guaranteed by design.
- See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
- See test circuit for current noise measurement.
- Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37A			OP-37B			OP-37C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	± 20	± 60	—	± 28	± 95	—	± 35	± 150	nA
Input Voltage Range	IVR		± 10.3	± 11.5	—	± 10.3	± 11.5	—	± 10.2	± 11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.5	± 13.5	—	± 11.0	± 13.2	—	± 10.5	± 13.0	—	V

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-37J and OP-37Z, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-37P, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37E			OP-37F			OP-37G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	± 14	± 60	—	± 18	± 95	—	± 25	± 150	nA
Input Voltage Range	IVR		± 10.5	± 11.8	—	± 10.5	± 11.8	—	± 10.5	± 11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.7	± 13.6	—	± 11.4	± 13.5	—	± 11.0	± 13.3	—	V

NOTES:

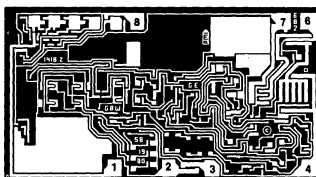
- Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
- The TCV_{OS} performance is within the specifications unnullled or when nullled with $R_p = 8k\Omega$ to $20k\Omega$. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
- Guaranteed by design.



DICE CHARACTERISTICS

DIE SIZE 0.054 × 0.096 inch, 5184 sq. mils
(1.37 × 2.44 mm, 3.35 sq. mm)

For additional DICE information refer to
1986 Data Book, Section 2.



1. NULL
2. (-) INPUT
3. (+) INPUT
4. V-
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-37N, OP-37G and OP-37GR devices; $T_A = 125^\circ C$ for OP-37NT and OP-37GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37NT LIMIT	OP-37N LIMIT	OP-37GT LIMIT	OP-37G LIMIT	OP-37GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		± 60	± 40	± 95	± 55	± 80	nA MAX
Input Voltage Range	IVR		± 10.3	± 11	± 10.3	± 11	± 11	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$T_A = 25^\circ C$, $V_S = \pm 4V$ to $\pm 18V$	10	10	10	10	20	$\mu V/V$ MAX
		$T_A = 125^\circ C$, $V_S = \pm 4.5V$ to $\pm 18V$	16	—	20	—	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1000	500	1000	700	V/mV MIN
		$R_L \geq 1k\Omega$, $V_O = \pm 10V$	—	800	—	800	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.5	± 12.0	± 11.0	± 12.0	± 11.5	V MIN
		$R_L \geq 600\Omega$	—	± 10.0	—	± 10.0	± 10.0	
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTES:

For $25^\circ C$ characteristics of OP-37NT and OP-37GT devices, see OP-37N and OP-37G characteristics, respectively.

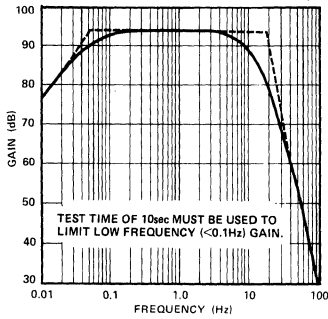
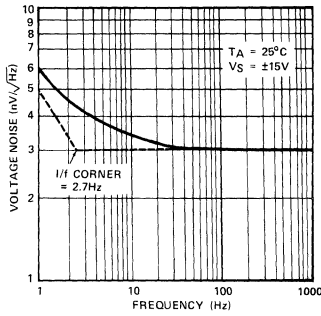
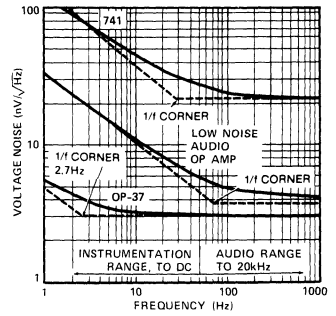
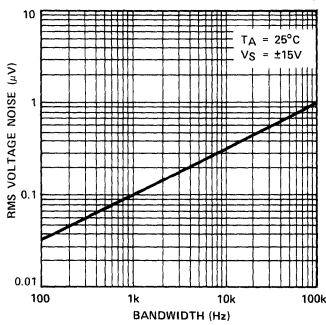
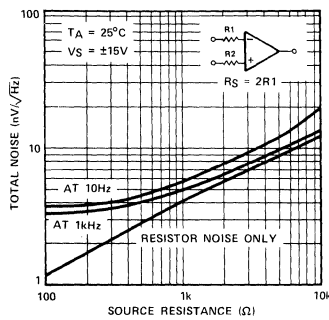
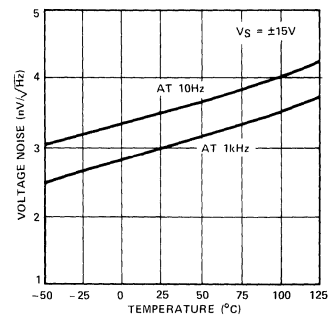
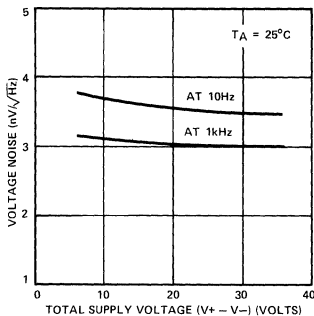
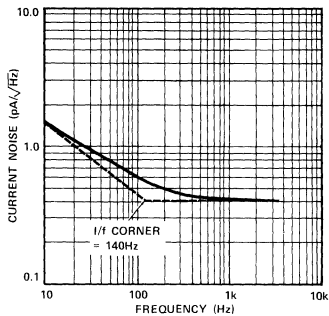
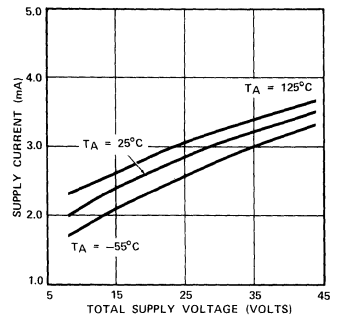
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

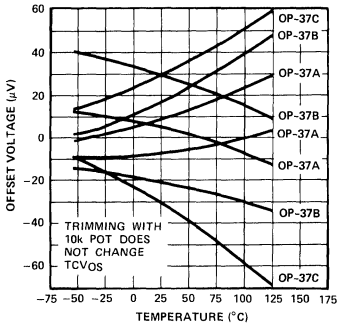
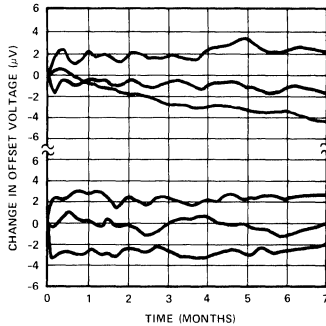
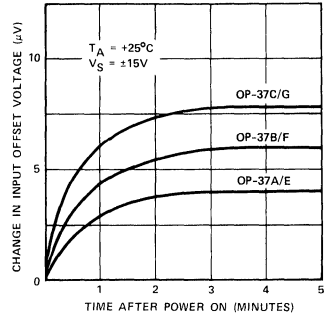
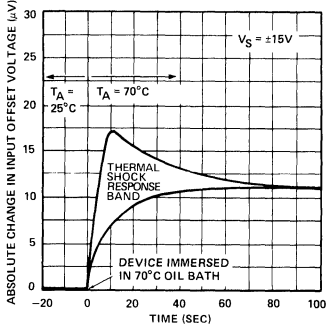
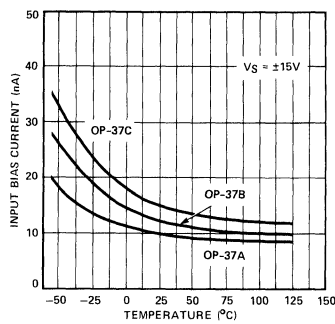
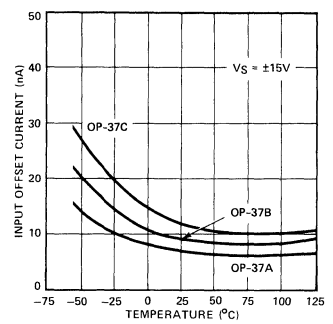
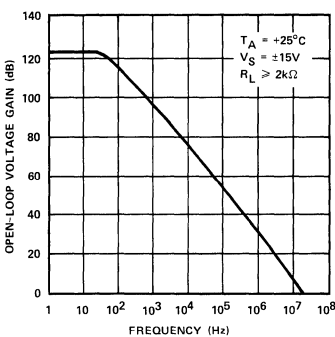
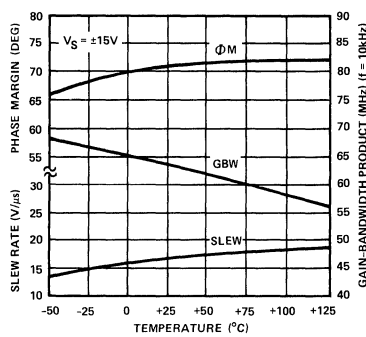
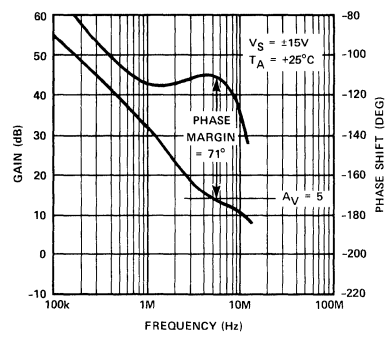
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

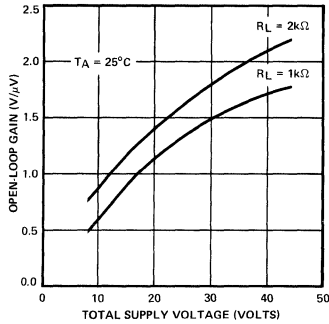
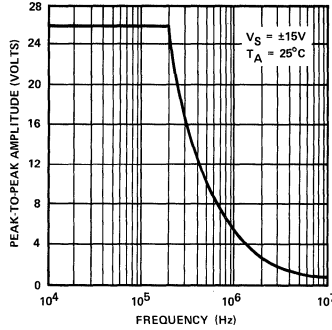
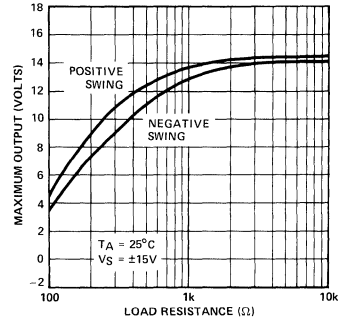
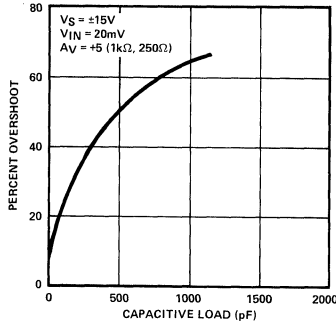
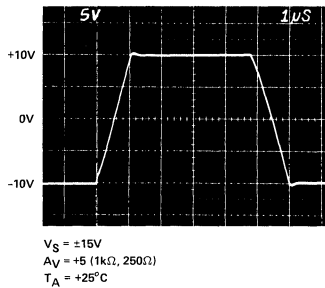
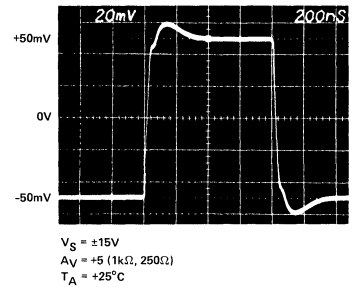
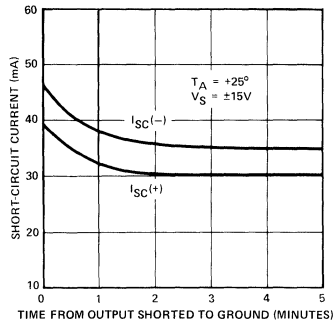
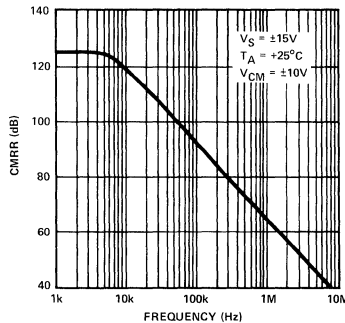
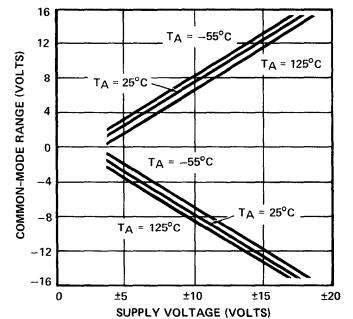
PARAMETER	SYMBOL	CONDITIONS	OP-37NT TYPICAL	OP-37N TYPICAL	OP-37GT TYPICAL	OP-37G TYPICAL	OP-37GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nullled or Unnullled $R_p = 8k\Omega$ to $20k\Omega$	0.2	0.2	0.3	0.3	0.4	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		80	80	130	130	180	$pA/^\circ C$
Average Input Bias Current Drift	TCI_B		100	100	160	160	200	$pA/^\circ C$
Input Noise Voltage Density	e_n	$f_o = 10Hz$	3.5	3.5	3.5	3.5	3.8	nV/\sqrt{Hz}
		$f_o = 30Hz$	3.1	3.1	3.1	3.1	3.3	
		$f_o = 1000Hz$	3.0	3.0	3.0	3.0	3.2	
Input Noise Current Density	i_n	$f_o = 10Hz$	1.7	1.7	1.7	1.7	1.7	pA/\sqrt{Hz}
		$f_o = 30Hz$	1.0	1.0	1.0	1.0	1.0	
		$f_o = 1000Hz$	0.4	0.4	0.4	0.4	0.4	
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.08	0.08	0.09	μV_{p-p}
Slew Rate	SR	$R_L \geq 2k\Omega$	17	17	17	17	17	$V/\mu s$
Gain Bandwidth Product	GBW	$f_o = 10kHz$	63	63	63	63	63	MHz

NOTE:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

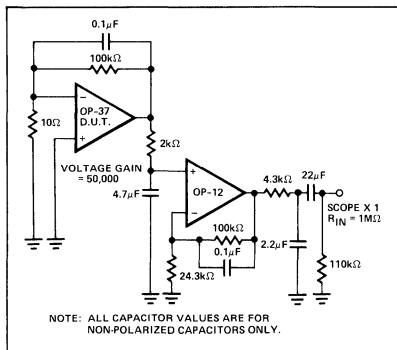
TYPICAL PERFORMANCE CHARACTERISTICS
NOISE-TESTER FREQUENCY RESPONSE (0.1Hz TO 10Hz)

VOLTAGE NOISE DENSITY vs FREQUENCY

A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA

INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

TOTAL NOISE vs SOURCE RESISTANCE

VOLTAGE NOISE DENSITY vs TEMPERATURE

VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE

CURRENT NOISE DENSITY vs FREQUENCY

SUPPLY CURRENT vs SUPPLY VOLTAGE


TYPICAL PERFORMANCE CHARACTERISTICS
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE

LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS

WARM-UP OFFSET VOLTAGE DRIFT

OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK

INPUT BIAS CURRENT vs TEMPERATURE

INPUT OFFSET CURRENT vs TEMPERATURE

OPEN-LOOP GAIN vs FREQUENCY

SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

GAIN, PHASE SHIFT vs FREQUENCY


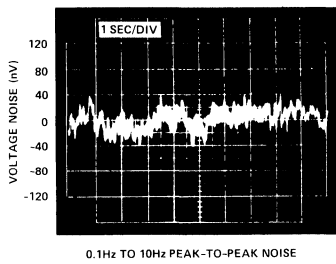
TYPICAL PERFORMANCE CHARACTERISTICS
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE

MAXIMUM OUTPUT SWING vs FREQUENCY

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

LARGE-SIGNAL TRANSIENT RESPONSE

SMALL-SIGNAL TRANSIENT RESPONSE

SHORT-CIRCUIT CURRENT vs TIME

CMRR vs FREQUENCY

COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE


TYPICAL PERFORMANCE CHARACTERISTICS

NOISE TEST CIRCUIT (0.1Hz TO 10Hz)

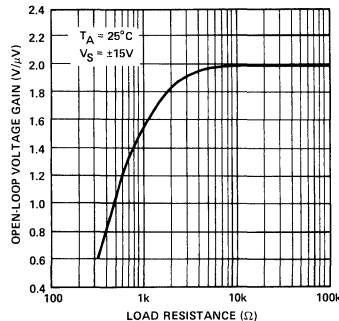


LOW-FREQUENCY NOISE

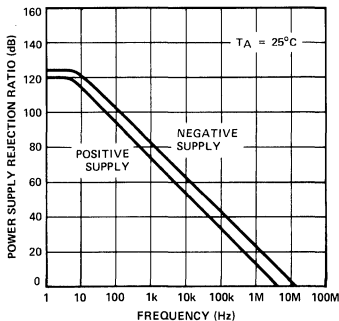


NOTE: Observation time limited to 10 seconds.

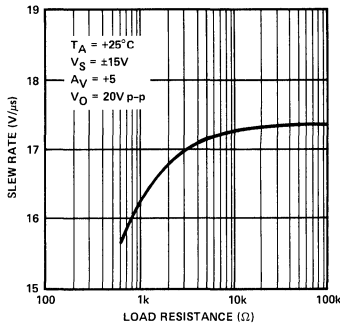
OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



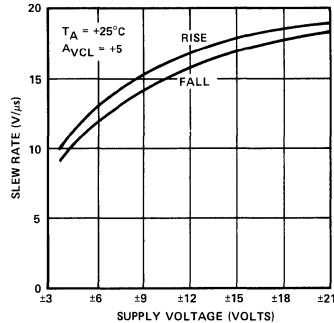
PSRR vs FREQUENCY



SLEW RATE vs LOAD



SLEW RATE vs SUPPLY VOLTAGE



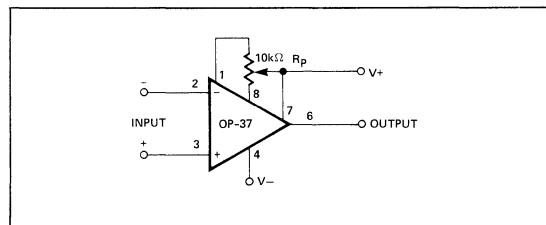
APPLICATIONS INFORMATION

OP-37 Series units may be inserted directly into 725, OP-06, OP-07, and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-37 may be fitted to unnullled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-37 operation. OP-37 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see offset nulling circuit).

The OP-37 provides stable operation with load capacitances of up to 1000pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. Closed-loop gain must be at least five. For closed-loop gain between five to ten, the designer should consider both the OP-27 and the OP-37. For gains above ten, the OP-37 has a clear advantage over the unity-gain-stable OP-27.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

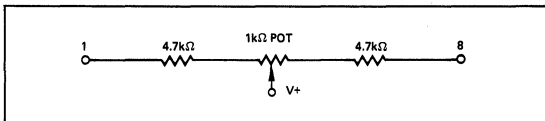
OFFSET NULLING CIRCUIT



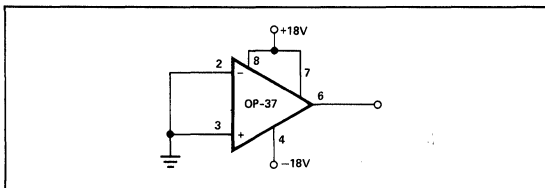
OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-37 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see offset nulling circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to $0.2\mu V/^{\circ}C$) of TCV_{OS} . Trimming to a value other than zero creates a drift of approximately $(V_{OS}/300)\mu V/^{\circ}C$. For exam-

ple, the change in TCV_{OS} will be $0.33\mu V/^{\circ}C$ if V_{OS} is adjusted to $100\mu V$. The offset-voltage adjustment range with a $10k\Omega$ potentiometer is $\pm 4mV$. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjunction with fixed resistors. For example, the network below will have a $\pm 280\mu V$ adjustment range.



BURN-IN CIRCUIT



NOISE MEASUREMENTS

To measure the $80nV$ peak-to-peak noise specification of the OP-37 in the 0.1Hz to 10Hz range, the following precautions must be observed:

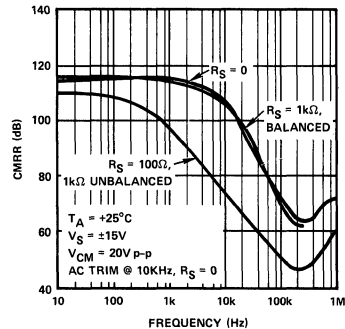
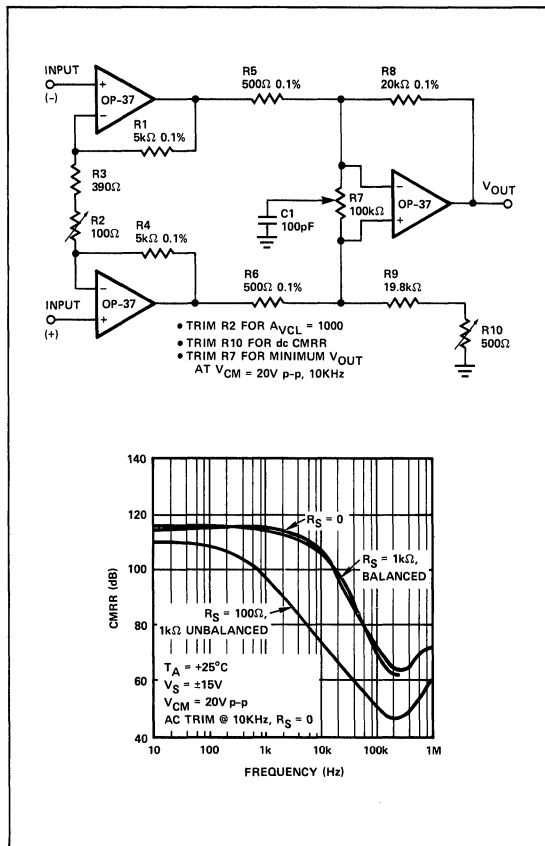
- (1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes $4\mu V$ due to increasing chip temperature after power-up. In the 10 second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
- (2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.
- (3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
- (4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.
- (5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the $1/f$ corner frequency.

OPTIMIZING LINEARITY

Best linearity will be obtained by designing for the minimum output current required for the application. High gain and excellent linearity can be achieved by operating the op amp with a peak output current of less than $\pm 10mA$.

INSTRUMENTATION AMPLIFIER

A three-op-amp instrumentation amplifier provides high gain and wide bandwidth. The input noise of the circuit below is $4.9nV/\sqrt{Hz}$. The gain of the input stage is set at 25 and the gain of the second stage is 40; overall gain is 1000. The amplifier bandwidth of 800kHz is extraordinarily good for a precision instrumentation amplifier. Set to a gain of 1000, this yields a gain-bandwidth product of 800MHz. The full-power bandwidth for a $20V_{p-p}$ output is 250kHz. Potentiometer R7 provides quadrature trimming to optimize the instrumentation amplifier's AC common-mode rejection.



COMMENTS ON NOISE

The OP-37 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-37 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-37A/E has I_B and I_{OS} of only $\pm 40nA$ and $35nA$ respectively at $25^{\circ}C$. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers

**NOISE vs SOURCE RESISTANCE
(INCLUDING RESISTOR NOISE)
AT 1000Hz**

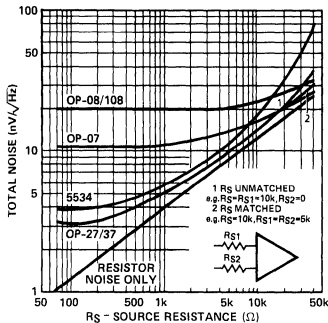


Figure 1

**10Hz NOISE vs
SOURCE RESISTANCE
(INCLUDES RESISTOR NOISE)**

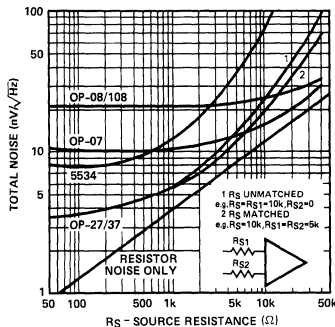


Figure 3

**PEAK-TO-PEAK NOISE (0.1 to
10Hz) vs SOURCE RESISTANCE
(INCLUDES RESISTOR NOISE)**

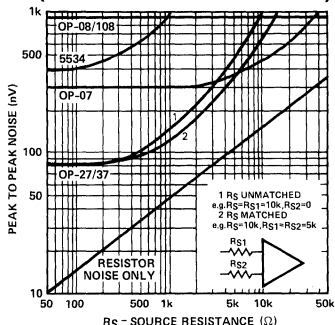


Figure 2

prefer to use direct coupling. The high I_B , TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-37's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-37 observed total noise with the noise performance of other devices in different circuit applications.

$$\text{Total noise} = \left[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise}^2) \right]^{1/2}$$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

At $R_S < 1k\Omega$, the OP-37's low voltage noise is maintained. With $R_S > 1k\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only

beyond R_S of 20k Ω that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-37 and OP-07 and OP-08 noise occurs in the 15-to-40k Ω region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to 5k Ω range depending on whether balanced or unbalanced source resistors are used (at 3k Ω the I_B , I_{OS} error also can be three times the V_{OS} spec.).

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500 Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500 Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-37 I_B can be neglected.
Magnetic phonograph cartridges	<1500 Ω	Similar need for low I_B in direct coupled applications. OP-37 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500 Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

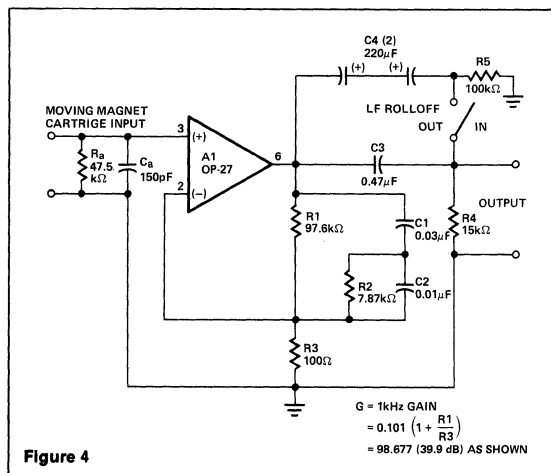


Figure 4

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A₁; R₁-R₂-C₁-C₂ form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75 μs.¹

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.⁴ (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values or where space is at a premium.)

The OP-27 brings a $3.2\text{nV}/\sqrt{\text{Hz}}$ voltage noise and $0.45\text{ pA}/\sqrt{\text{Hz}}$ current noise to this circuit. To minimize noise from other sources, R₃ is set to a value of 100 Ω, which generates a voltage noise of $1.3\text{nV}/\sqrt{\text{Hz}}$. The noise increases the $3.2\text{nV}/\sqrt{\text{Hz}}$ of the amplifier by only 0.7 dB. With a 1 kΩ source, the circuit noise measures 63 dB below a 1 mV reference level, unweighted, in a 20 kHz noise bandwidth.

Gain (G) of the circuit at 1 kHz can be calculated by the expression:

$$G = 0.101 \left(1 + \frac{R_1}{R_3} \right)$$

For the values shown, the gain is just under 100 (or 40 dB). Lower gains can be accommodated by increasing R₃, but gains higher than 40 dB will show more equalization errors because of the 8 MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7 V rms. At 3 V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20 kHz.

Capacitor C₃ and resistor R₄ form a simple -6 dB-per-octave rumble filter, with a corner at 22 Hz. As an option, the switch-selected shunt capacitor C₄, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

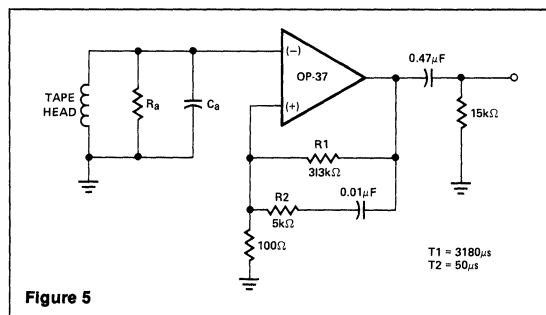


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3 kHz ($T_2 = 50\text{ μs}$), the amplifier need not be stabilized for unity gain. The uncompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R₁ and R₂ to optimize frequency response for nonideal tape-head performance and other factors.⁵

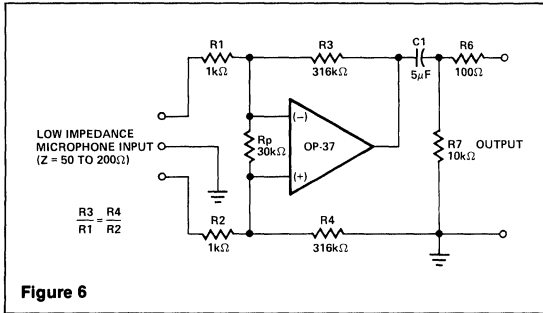
The network values of the configuration yield a 50 dB gain at 1 kHz, and the dc gain is greater than 70 dB. Thus, the worst-case output offset is just over 500 mV. A single 0.47 μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 85 nA with a 400 mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1 kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 170 μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2k Ω . Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

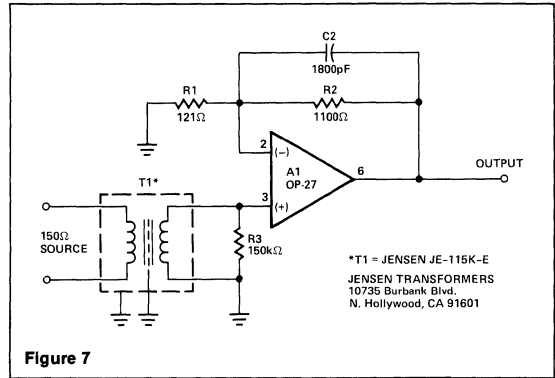


Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R₄ should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R₁ and R₂ than by the op amp, as R₁ and R₂ each generate a 4nV/ $\sqrt{\text{Hz}}$ noise, while the op amp generates a 3.2nV/ $\sqrt{\text{Hz}}$ noise. The rms sum of these predominant noise sources will be about 6nV/ $\sqrt{\text{Hz}}$, equivalent to 0.9 μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally compensated OP-27. T₁ is a JE-115K-E 150 Ω /15k Ω transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

Gain may be trimmed to other levels, if desired, by adjusting R₂ or R₁. Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a



40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

Capacitor C₂ and resistor R₂ form a 2 μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C₂ in use, A₁ must have unity-gain stability. For situations where the 2 μs time constant is not necessary, C₂ can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150 Ω resistor and R₁ and R₂ gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T₁ specified, the additional noise degradation will be close to 3.6dB (or -69.5 referenced to 1mV).

References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.



OP-41

LOW-BIAS-CURRENT JFET OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Bias Current 5pA Max
- Low Current Consumption 1.0mA Max
- High Gain 1000V/mV Min
- High Common-Mode Rejection 100dB Min
- Symmetrical Slew-Rates $\pm 1.0V/\mu s$ Min
- Fast Overload Recovery Time 6 μs Typ
- Low Harmonic Distortion <0.01% at 5kHz

ORDERING INFORMATION†

T _A = 25° C V _{OS} MAX (μV)	PACKAGE		
	TO-99 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
500	OP-41AJ*	—	MIL
500	OP-41EJ	—	IND
1000	OP-41BJ*	—	MIL
1000	OP-41FJ	—	IND
1500	—	OP-41GP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

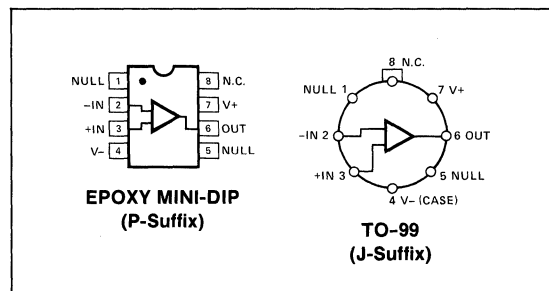
† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

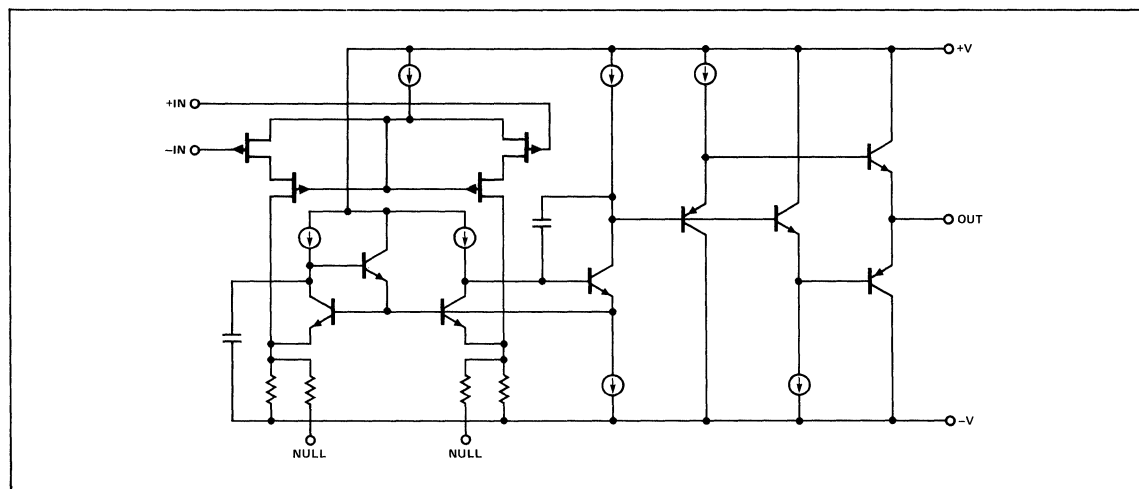
The OP-41 JFET op amp features a 5pA max bias current with an open-loop gain of over 1 million, and is targeted at price-sensitive applications. The device is unity-gain stable and highly tolerant of capacitive loads. At unity-gain, the output is guaranteed to drive 250pF without oscillation. Transient response is considerably improved over industry standard JFETs.

The OP-41's cascode input stage boosts CMR to over 100dB, improves CMR linearity, and stabilizes bias current with changing common-mode voltage. The linear common-mode rejection of 100dB min is unusually good for a FET input amplifier. The OP-41 consumes only 750 μA supply current and has a power-supply rejection ratio of 25 $\mu V/V$, making it an ideal choice for battery-operated systems. Despite the low supply-drain, the slew-rate is a respectable 1.3V/ μs , and symmetrical. Using zener-zap trimming techniques, offset voltage is adjusted to below 500 μV which eliminates the need for external nulling in many applications. The OP-41's guaranteed gain of 1 million into a 2k Ω load, combined with the linear 100dB minimum CMR, vastly improves linearity over competitive low-cost devices. Linearity is excellent in both low-gain and high-gain amplifier configurations. In voltage follower applications CMR effects dominate linearity, and in high-gain applications open-loop gain dominates linearity, hence the performance advantage of the OP-41.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Manufactured under the following U.S. patent: 4,538,115.

The device exhibits rapid recovery from signal overload. Following saturation at the positive supply, the output recovers in only 6μs, and from a negative overdrive in only 100ns.

The combination of low-power, low bias current, and high-gain, plus the superior CMR and PSRR performance of the OP-41, make it suitable in a wide variety of demanding applications. The device makes an excellent output amplifier for CMOS DACs. Where low-power consumption is needed in portable instrumentation, the OP-41 permits high-gain and high-accuracy amplification with good speed performance. The low and stable bias current makes it an excellent choice as a photodiode amplifier in medical applications.

A standard 741 pin-out allows existing JFET designs and low-power bipolar designs to be upgraded by switching to the OP-41.

ABSOLUTE MAXIMUM RATINGS

(Note 3)

Supply Voltage	±20V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 2)	±20V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±20V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-41A, B (J)	-55°C to +125°C
OP-41E, F (J)	-25°C to +85°C
OP-41G (P)	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Junction Temperature	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

2. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.

3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41A/E			OP-41B/F			OP-41G*			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	200	500	—	400	1000	—	500	1500	μV
Offset Current	I_{OS}	(Note 1)	—	0.04	1	—	0.05	2	—	0.05	5	pA
Bias Current	I_B	(Note 1)	—	3.0	5	—	3.5	10	—	3.5	25	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	300	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.3	±12.6	—	±12.0	±12.6	—	±11	±12.6	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.0	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	±11	+15 -11.5	—	±11	+15 -11.5	—	±11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	5	25	—	10	80	—	10	80	μV/V
Noise Voltage Density Referred to Input	e_n	1kHz	—	32	—	—	32	—	—	32	—	nV/√Hz
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±12	+20 -18	±36	±12	+20 -18	±36	±6	+20 -18	±36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	1	1.3	—	V/μs
Gain Bandwidth	GBW		—	500	—	—	500	—	—	500	—	kHz
Power Bandwidth	BW_p		—	20	—	—	20	—	—	20	—	kHz

5
OPERATIONAL AMPLIFIERS

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-41A/E			OP-41B/F			OP-41G*			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time	t_s	10V Step $A_V = -1$ to 0.1% to 0.01%	—	10	—	—	10	—	—	10	—	μs
			—	12	—	—	12	—	—	12	—	
Overload Recovery		Positive Going	—	0.1	—	—	0.1	—	—	0.1	—	μs
		Negative Going	—	6.0	—	—	6.0	—	—	6.0	—	
Capacitive Load Stability		$A_V = +1$ (Note 3)	250	>1000	—	250	>1000	—	250	>1000	—	pF
Open-Loop Output Resistance	R_O		—	150	—	—	150	—	—	150	—	Ω

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

*OP-41G SPECIFICATIONS ARE SUBJECT TO CHANGE AT TIME OF INTRODUCTION

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -55^\circ C/+125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41A			OP-41B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	400	1000	—	600	2000	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	2.5	5	—	3.5	10	$\mu V/^\circ C$
Offset Current	I_{OS}	(Note 1)	—	40	1000	—	50	2000	pA
Bias Current	I_B	(Note 1)	—	4000	7500	—	4500	15000	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.0	± 12.5	—	± 11.5	± 12.5	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11	+15 -11.5	—	± 11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	105	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	5	40	—	10	100	$\mu V/V$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6	+12 -17	± 36	± 6	+12 -17	± 36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	V/ μs
Gain Bandwidth	GBW		—	500	—	—	500	—	kHz
Power Bandwidth	BW _P		—	20	—	—	20	—	kHz
Capacitive Load Stability		$A_V = +1$ (Note 3)	100	>1000	—	100	>1000	—	pF

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -25^\circ C/+85^\circ C$ for E/F grades and $0^\circ C/70^\circ C$ for G grade, unless otherwise noted.

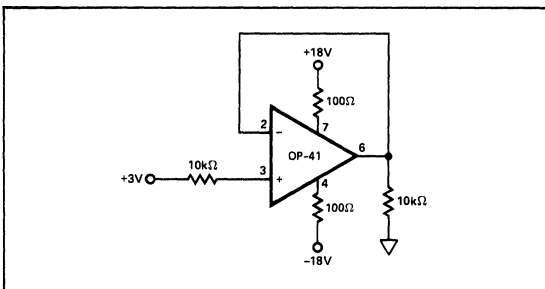
PARAMETER	SYMBOL	CONDITIONS	OP-41E			OP-41F			OP-41G*			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	250	1000	—	500	2000	—	500	2000	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	3.5	8	—	7.5	—	—	7.5	—	$\mu V/^\circ C$
Offset Current	I_{OS}	(Note 1)	—	5	100	—	10	200	—	20	—	pA
Bias Current	I_B	(Note 1)	—	240	500	—	300	1000	—	100	500	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	300	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.0	± 12.6	—	± 11.5	± 12.5	—	± 11	± 12.6	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.2	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11.0	+15 -11.5	—	± 11	+15 -11.5	—	± 11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	110	—	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	5	40	—	10	100	—	10	100	$\mu V/V$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6	+16 -18	± 36	± 6	+16 -18	± 36	± 6	+20 -18	± 36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	1	1.3	—	V/ μs
Gain Bandwidth	GBW		—	500	—	—	500	—	—	500	—	kHz
Power Bandwidth	BW_p		—	20	—	—	20	—	—	20	—	kHz
Capacitive Load Stability		$A_V = +1$ (Note 3)	100	>1000	—	100	>1000	—	100	>1000	—	pF

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

*OP-41G SPECIFICATIONS ARE SUBJECT TO CHANGE AT TIME OF INTRODUCTION

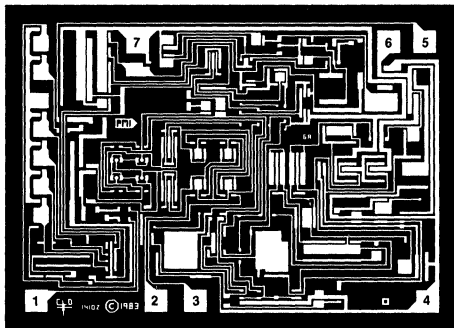
BURN-IN CIRCUIT



5
OPERATIONAL AMPLIFIERS



DICE CHARACTERISTICS



DIE SIZE 0.103 × 0.074 inch, 7622 sq. mils
(2.62 × 1.88mm, 4.92 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41N LIMIT	UNITS
Offset Voltage	V_{OS}		1000	μV MAX
Bias Current	I_B	(Note 1)	20	pA MAX
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12	V MIN
Supply Current	I_{SY}	$V_O = 0V$	1.2	mA MAX
Input Voltage Range	IVR	(Note 2)	± 11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	80	$\mu V/V$ MAX
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6 ± 36	mA MIN mA MAX
Slew Rate	SR		1	V/ μs MIN
Capacitive Load Stability	$A_V = +1$	(Note 3)	250	pF MIN

NOTES:

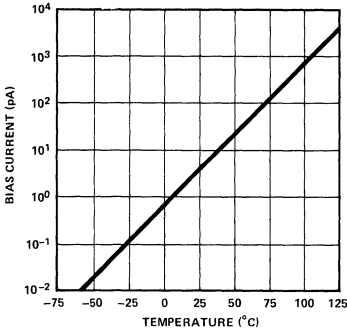
1. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

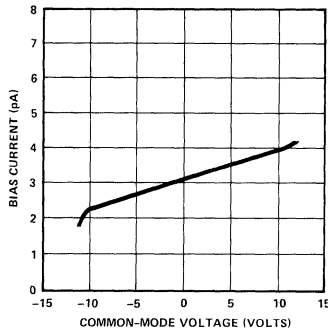


TYPICAL PERFORMANCE CHARACTERISTICS

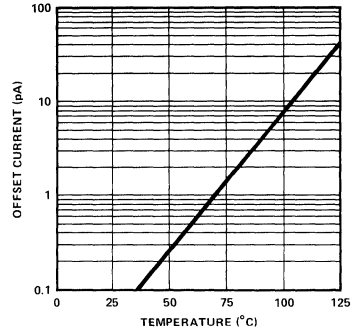
BIAS CURRENT vs TEMPERATURE



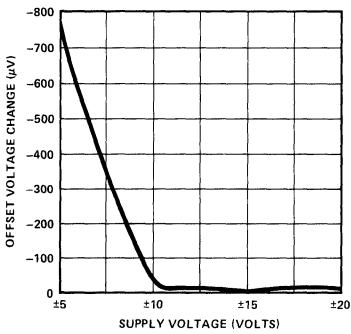
BIAS CURRENT vs COMMON-MODE VOLTAGE



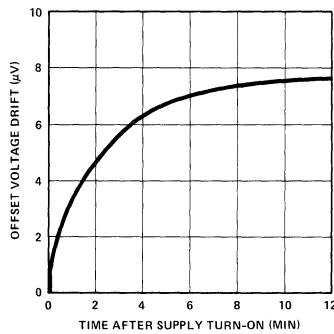
OFFSET CURRENT vs TEMPERATURE



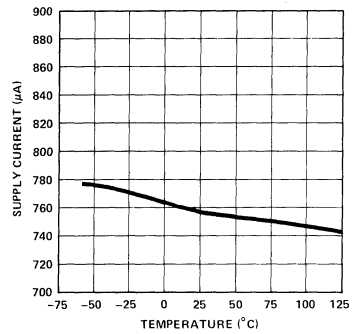
OFFSET VOLTAGE vs SUPPLY VOLTAGE



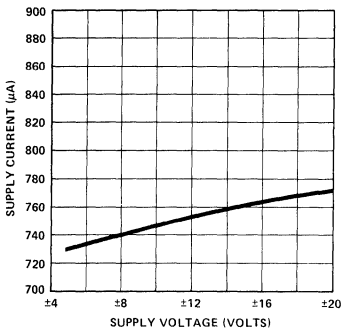
WARM-UP DRIFT vs TIME



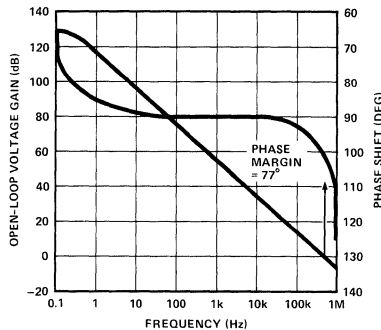
SUPPLY CURRENT vs TEMPERATURE



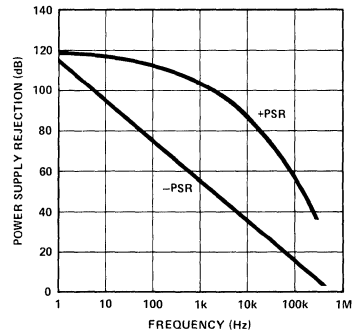
SUPPLY CURRENT vs SUPPLY VOLTAGE

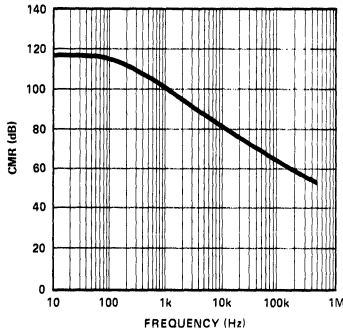
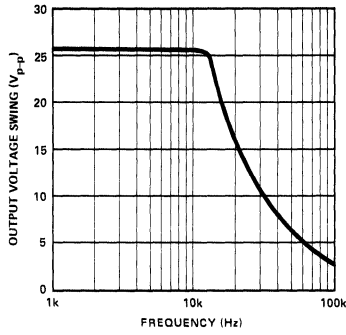
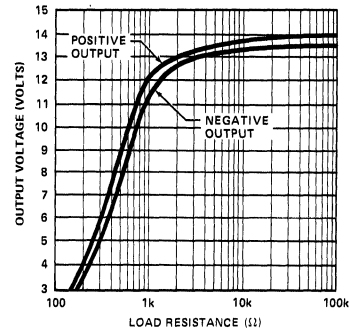
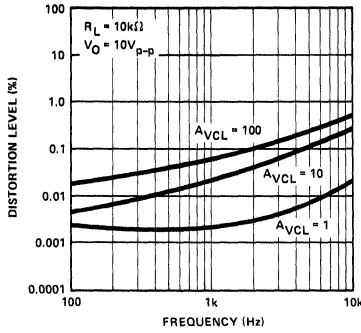
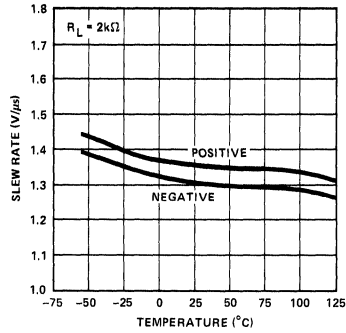
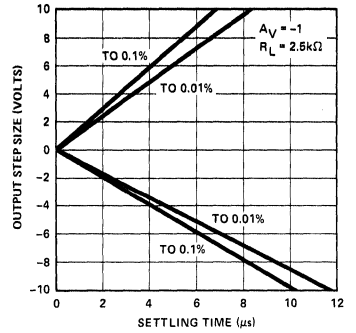
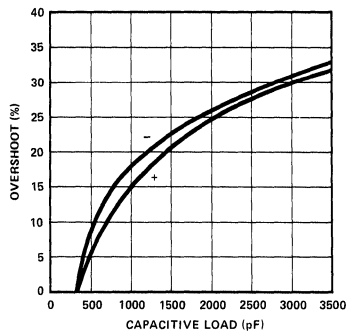


OPEN-LOOP GAIN AND PHASE vs FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS
COMMON-MODE REJECTION vs FREQUENCY

MAXIMUM OUTPUT SWING vs FREQUENCY

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

TOTAL HARMONIC DISTORTION vs FREQUENCY

SLEW RATE vs TEMPERATURE

SETTLING TIME

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD


OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted by a potentiometer of 10kΩ to 100kΩ resistance. This potentiometer should be connected between pins 1 and 5 with the wiper connected to the V₋ supply. (See Figure 1.) Nulling V_{OS} will change TCV_{OS} by no more than 5μV/°C per millivolt of V_{OS} change.

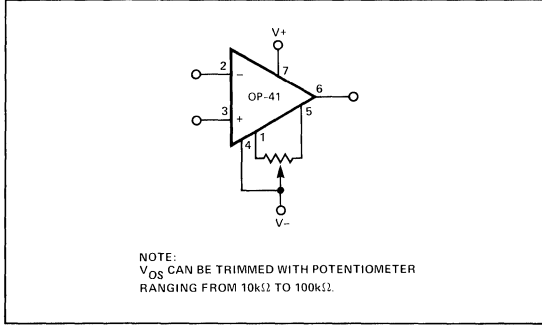
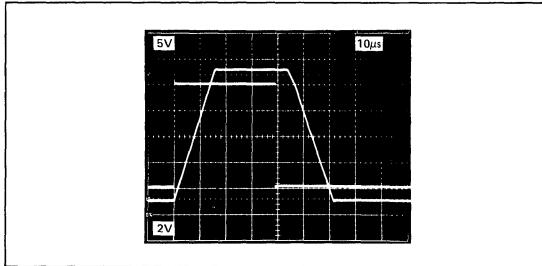
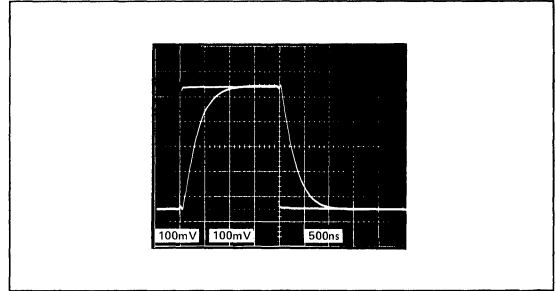
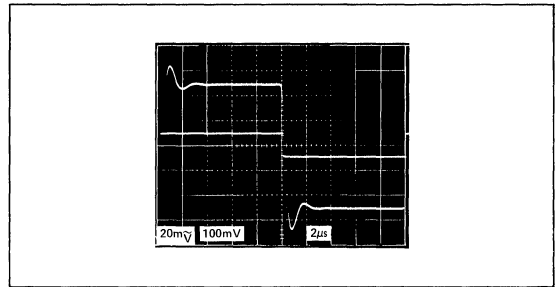
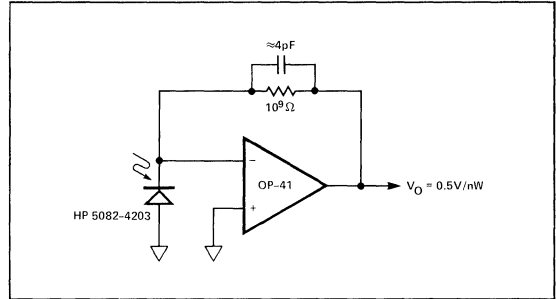
FIGURE 1: INPUT OFFSET VOLTAGE NULLING

APPLICATIONS INFORMATION
TYPICAL AC PERFORMANCE CHARACTERISTICS

Figure 2 shows the overload recovery time after the output saturates at each supply. A high degree of slew-rate symmetry is maintained even during severe input overload. The photo also shows the well controlled linear characteristics of the amplifier and freedom from oscillations. The OP-41's symmetry greatly reduces the generation of large DC components in the output when the amplifier is overdriven. This significantly reduces system recovery time after an overload.

Figure 3 shows the unity-gain small-signal transient response of the OP-41. Note the clean symmetrical waveform.

Figure 4 illustrates the high degree of stability even when loaded with 1000pF at unity-gain. Heavy capacitive loading will cause stability problems with many amplifiers.

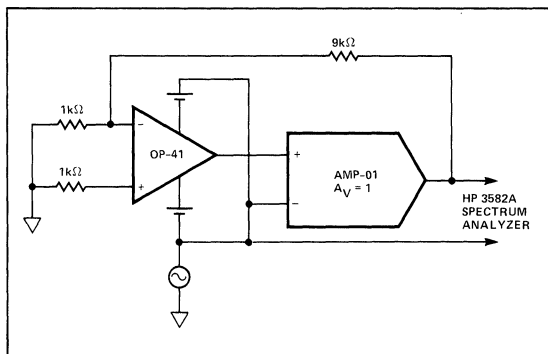
Figure 5 illustrates the use of the OP-41 in a high sensitivity, wide-dynamic-range light detector. This circuit will produce an output voltage proportional to the light input over a 60dB range.

FIGURE 2: OVERLOAD RECOVERY TIME AT A_V = 10

FIGURE 3: SMALL-SIGNAL TRANSIENT RESPONSE

FIGURE 4: SMALL-SIGNAL TRANSIENT RESPONSE WITH 1000pF LOAD

FIGURE 5: WIDE-DYNAMIC-RANGE LIGHT DETECTOR

CMR MEASUREMENT METHODS

Two separate methods are used to measure the CMR. The first method is used over the range of 10Hz to 20kHz. This method grounds the input circuitry and applies the common-mode signal to the remainder of the op amp, Figure 6.

The AMP-01 eliminates loading on the output stage. This assures that the OP-41 output is not required to deliver current into the feedback circuit. The effects of the DUT open-loop gain changing with frequency are therefore significantly reduced. The circuit does not require tight resistor matching. DC data sheet limits may be verified using this method. Circuit accuracy is dependent on the high CMR of the AMP-01.

FIGURE 6: CIRCUIT USED TO MEASURE CMR FROM 10kHz TO 20kHz

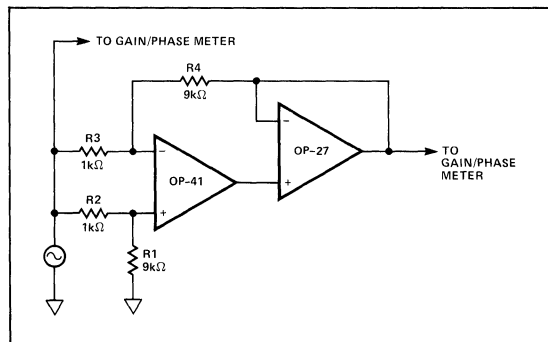


An alternate circuit may be used to make high-frequency measurements from 2kHz to 500kHz, Figure 7. The 2kHz to 20kHz data overlap can be used to verify the accuracy of the respective test methods.

This method drives the input stage with the test signal and requires an accurate ratio of resistors, $R4/R3 = R1/R2$. To measure CMR to 100dB requires ratio matching to better than 10ppm. For this reason, it is not practical to use the second method at low frequencies where CMR is greater than 80-100dB.

The DUT output is normally connected directly to R4 which may cause problems. If the DUT is not buffered with a broadband low-output-impedance amplifier, the frequency-dependent output impedance of the DUT, in series with R4, rapidly unbalances the resistor ratios. This causes frequency dependent errors. The OP-27 provides good performance over the range of frequencies used.

FIGURE 7: CIRCUIT USED TO MEASURE CMR FROM 2kHz TO 500kHz



GUARDING AND SHIELDING

In applications where the input is at high impedance, careful shielding is required to prevent hum pickup from power line sources or detection of RF from radio stations and nearby radar

transmitters. Loss of accuracy can also occur from surface and bulk leakages in printed circuit boards. Both of these conditions can be avoided by the following methods.

Hum and RF pickup are eliminated or reduced by keeping all high impedance leads, including feedback resistor leads, inside shielded enclosures. In addition to shielding, power supply lines should be bypassed where they pass through the shielding. This will prevent noise from being retransmitted from the power supply lines inside the shielded enclosure.

Noise can also be created by the flexing of coax cable. These signals can be caused by mechanical vibrations inside or outside the shielding. Prevention consists of securely supporting all high-impedance shielded lines to prevent motion.

Printed circuit board leakage currents can easily exceed the OP-41 bias currents or the incoming signal. Leakage currents can be minimized by using Teflon insulators to support wires instead of using PC traces. An alternate method is guarding the high impedance traces. When the OP-41 is in the inverting mode, the signal traces should have grounded guard traces on both sides, Figure 8. The opposite side of the board should be used as a ground plane and shield, if not otherwise used. A ground plane is implemented by leaving copper on all areas that are not being used for signal or power conduction. Ground connection should be made to all areas of isolated copper. In the noninverting configuration, the OP-41's output signal or a portion of it should be used to drive the guard traces, Figure 9. When the guard drive voltage is equal to the input signal, leakage currents will be effectively eliminated.

FIGURE 8: CURRENT-TO-VOLTAGE CONVERTER

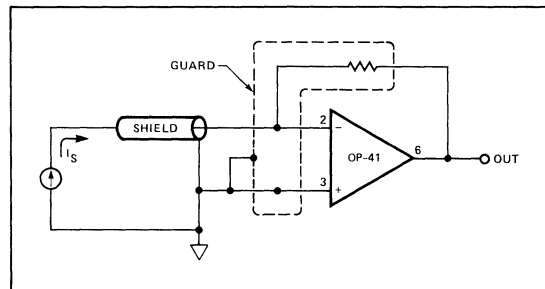
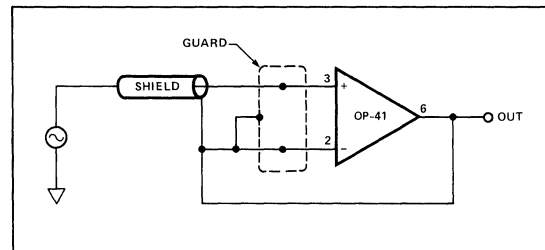
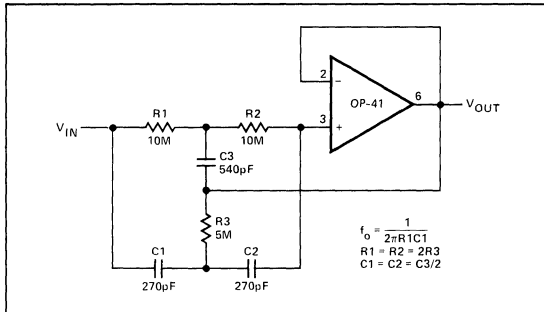


FIGURE 9: VERY HIGH IMPEDANCE NONINVERTING AMPLIFIER



The High Q Notch Filter benefits from the low bias current and high input impedance of the OP-41, Figure 10. These features enable small value capacitors and large resistors to be used in this 60Hz notch filter. The 5pA bias current only develops 100μV across R1 and R2.

FIGURE 10: HIGH Q NOTCH FILTER



Low power consumption, low bias current, and low offset voltage make the OP-41 an ideal current-to-voltage converter, Figure 11.

In this application, the PM-7541 and the OP-41 provide complete 12-bit digital-to-analog conversion with less than 3mA supply current.

FIGURE 11: DAC CIRCUIT USING THE OP-41

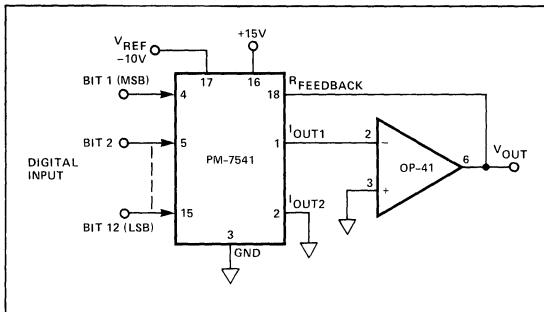
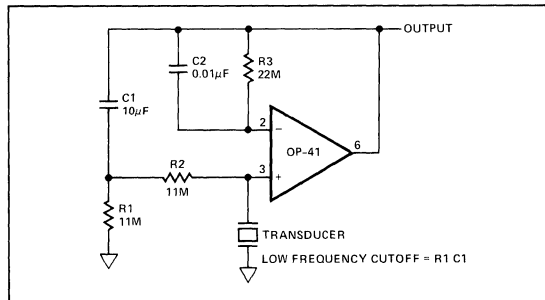


Figure 12 shows an amplifier for high-impedance ac transducers like a piezoelectric accelerometer. These sensors normally require a high-input-resistance amplifier. The OP-41 can provide input resistance in the range of 10¹²Ω, however, a dc return for bias current is needed. To maintain a high R_{IN}, large value resistors above 22MΩ are often required. These may not be practicable.

Using the circuit in Figure 12, input resistances that are orders of magnitude greater than the values of the dc return resistors can be obtained. This is accomplished by bootstrapping the resistors to the output. With this arrangement, the lower cutoff frequency is determined more by the RC product of R1 and C1 than it is by resistor values and the equivalent capacitance of the transducer.

FIGURE 12: AMPLIFIER FOR PIEZOELECTRIC TRANSDUCERS



WIDE RANGE LOW-CURRENT AMMETER

The circuit shown in Figure 13 can measure currents from 100pA to 100μA without the use of high value resistors. Accuracy is better than 1% over most of the range, depending upon the accuracy of the divider resistor and the input bias current of the op amp. Using the OP-41 as the input amplifier allows low end measurement down to a few pA due to the 3.5pA input bias current.

One of the requirements for a good current meter is low series voltage drop. Since the voltage across the inputs of an op amp is forced to virtually zero, it makes a good choice for the input of a current meter. Amplifier A1 is used as an inverting amplifier for the input. This ensures less than 500μV drop at any current level.

Feedback around the op amp is accomplished with a transistor, rather than a resistor. The op amp forces the collector current of Q1A to equal the input current. This causes the emitter-base voltage of Q1A to be proportional to the log of the input current. Resistors R1, R2, R3 and capacitors C1, C2 frequency compensate the log circuit since Q1A provides gain in the feedback loop.

The output of the log amplifier is taken from the emitter of Q1A to drive Q1B. Q1B anti-logs the output and drives the meter. The output of Q1B is proportional to the log of the input current scaled by a constant, which is proportional to the voltage from the divider, selected by S1. For transistors operating at different current levels, the V_{be} difference equals:

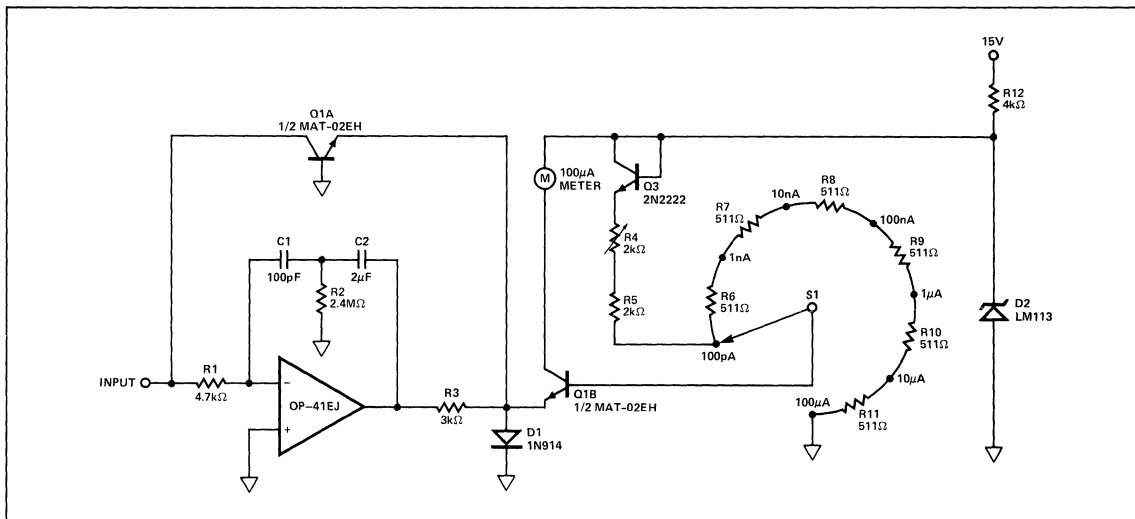
$$\Delta V_{be} = \frac{kT}{q} \ln \frac{IC2}{IC1}$$

solving for IC2

$$IC2 = IC1 e^{\left(\frac{\Delta V_{be} q}{kT}\right)}$$

Where IC1 and IC2 are the collector currents of Q1A and Q1B; Q is the charge of an electron; k is Boltzmann's constant; T is temperature in degrees Kelvin; and V_{be} is the voltage applied to the base of Q1B. If V_{be} varies as absolute temperature, the exponent will be a constant.

FIGURE 13: WIDE RANGE LOW-CURRENT AMMETER



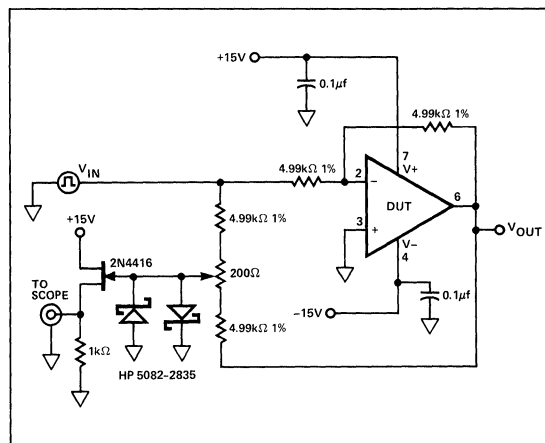
The voltage driving the divider is obtained from a 1.22V low voltage reference diode (LM113) through a 2N2222 transistor and resistor string. The voltage across the divider varies with absolute temperature, keeping the multiplier constant.

Calibration is simple, requiring only one adjustment. R4 is used to adjust full scale deflection with a 1μA input current. This will give maximum accuracy over the operating range of currents.

The low V_{OS} and exceptionally good log conformance of the MAT-02 assure high accuracy over the full 6 decade operating range.

Figure 14 is the test circuit used to measure the settling time. This circuit uses the "false sum-node" technique. When the system is initially set up, the 200Ω pot is adjusted until the DC output voltage to the scope is unchanged when the input is changed from +10V to -10V. The 2N4416 FET buffer isolates the sum node from the scope probe load capacitance. The pulse generator must be properly terminated and have ringing below the expected error signal. (2.5mV in a 5V pulse for 0.1% overshoot measurement.)

FIGURE 14: SETTLING-TIME TEST CIRCUIT





OP-43

LOW-BIAS-CURRENT, FAST JFET OPERATIONAL AMPLIFIER ($A_{VCL} \geq 2$)

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Low Bias Current 5pA Max
- High Slew-Rate $\pm 5V/\mu s$ Min
- Low Current Consumption 1.0mA Max
- High Gain 1000V/mV Min
- High Common-Mode Rejection 100dB Min
- Power Bandwidth 100kHz Typ
- Fast Overload Recovery Time 3.5 μs Typ
- Low Harmonic Distortion <0.01% at 5kHz

ORDERING INFORMATION†

$T_A = 25^\circ C$ V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	PLASTIC DIP 8-PIN	
250	OP-43AJ*	—	MIL
250	OP-43EJ	—	IND
750	OP-43BJ*	—	MIL
750	OP-43FJ	—	IND
1500	—	OP-43GP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

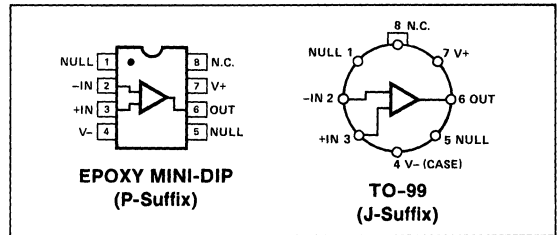
GENERAL DESCRIPTION

The OP-43 JFET operational amplifier is a high-speed version of the OP-41, featuring a slew rate of 6V/ μs , gain-bandwidth product of 2.4MHz, and power bandwidth of 100kHz. Its high speed is achieved without compromising the low supply current, which is typically 750 μA . The OP-43 has a bias current of only 5pA, and an open-loop gain of over 1 million. The

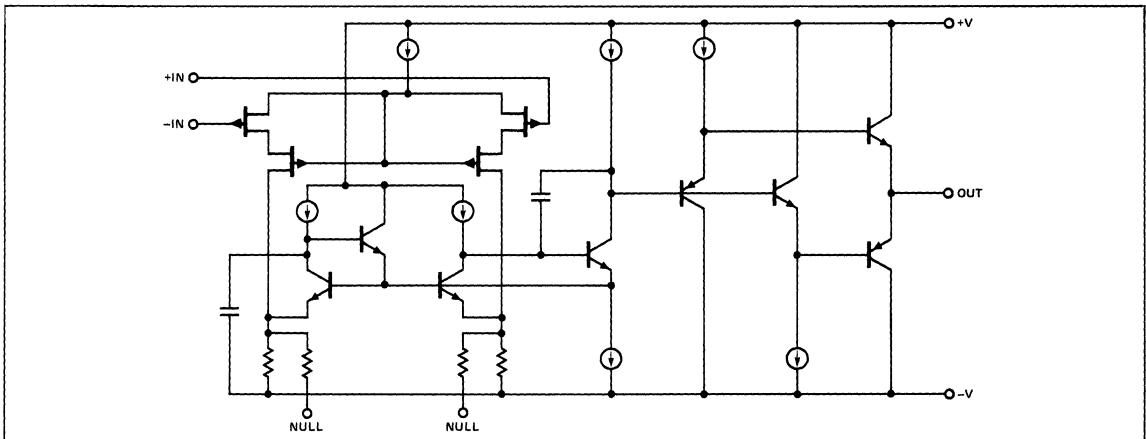
common-mode rejection is an outstanding 115dB, far beyond that available with most FET op amps. The OP-43 is stable with minimum gains of +2 and -1. It is ideal for price-sensitive applications requiring low power consumption combined with high speed and high accuracy. OP-41 circuits, in which more speed is required and unity gain stability is not a criterion, are easily upgraded with the OP-43.

The cascode input stage gives the OP-43 its exceptional CMR while improving CMR linearity with changing common-mode voltage. This input stage also stabilizes the bias current over the common-mode range. With its low power-consumption and a power-supply rejection ratio of 25 $\mu V/V$, the OP-43 is an ideal choice for battery-operated systems. Using zener-zap trimming techniques, offset voltage is adjusted to below 250 μV , thus eliminating the need for external nulling in many applications. In noninverting amplifier configurations, the outstanding CMR of the OP-43 insures linearity, while in high-gain configurations, linearity and accuracy are insured by the OP-43's guaranteed gain of 1 million into a 2k Ω load. Although the OP-43 is a high speed device, it is still capable of handling moderate capacitive loads and with a gain of -1 is guaranteed stable with at least 100pF.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Manufactured under the following U.S. patent: 4,538,115.

This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



The OP-43 exhibits rapid recovery from signal overload. Following saturation at the positive supply, the output recovers in only 3.5 μ s. Recovery from saturation at the negative supply is even faster.

The combination of low-power, low bias current, high speed, and high gain plus the superior CMR and PSRR performance of the OP-43, makes the device suitable for a wide range of demanding applications. Where low power-consumption is required in battery-powered or portable instrumentation, the OP-43 permits high-gain and high-accuracy amplification along with high-speed. The low and stable bias current, combined with its high input impedance, makes it an excellent choice for interfacing with high impedance transducers or low-level current sources.

In applications where speed is not essential, and superb capacitive load driving capabilities are required, the OP-41 is recommended.

The standard "741" pin-out allows existing JFET designs and low-power bipolar designs to be upgraded by direct replacement with the OP-43.

ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage	$\pm 20V$
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 2)	$\pm 20V$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	$\pm 20V$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature Range	
OP-43A, B (J)	$-55^{\circ}C$ to $+125^{\circ}C$
OP-43E, F (J)	$-25^{\circ}C$ to $+85^{\circ}C$
OP-43G (P)	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature Range (Soldering, 60 sec)	$300^{\circ}C$
Junction Temperature	$-65^{\circ}C$ to $+150^{\circ}C$

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

2. For supply voltages less than $\pm 20V$, the absolute maximum input voltage is equal to the supply voltage.
3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-43A/E			OP-43B/F			OP-43G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	200	250	—	400	750	—	500	1500	μV
Offset Current	I_{OS}	(Note 1)	—	0.04	1	—	0.05	2	—	0.05	5	pA
Bias Current	I_B	(Note 1)	—	3.0	5	—	3.5	10	—	3.5	25	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	300	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.3	± 12.6	—	± 12.0	± 12.6	—	± 11	± 12.6	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.0	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11	+15 -11.5	—	± 11	+15 -11.5	—	± 11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	5	25	—	10	80	—	10	80	$\mu V/V$
Noise Voltage Density Referred to Input	e_n	1kHz	—	32	—	—	32	—	—	32	—	nV/\sqrt{Hz}
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 12	+20 -18	± 36	± 12	+20 -18	± 36	± 6	+20 -18	± 36	mA
Slew Rate	SR		5	6	—	5	6	—	5	6	—	V/ μ s
Gain Bandwidth	GBW		—	2.4	—	—	2.4	—	—	2.4	—	MHz
Power Bandwidth	BW_p		—	100	—	—	100	—	—	100	—	kHz

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-43A/E			OP-43B/F			OP-43G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time	t_s	10V Step $A_V = -1$ to 0.1%	—	3	—	—	3	—	—	3	—	μs
		to 0.01%	—	6	—	—	6	—	—	6	—	
Overload Recovery		Positive Going	—	1	—	—	1	—	—	1	—	μs
		Negative Going	—	3.5	—	—	3.5	—	—	3.5	—	
Capacitive Load Stability		$A_V = -1$ (Note 3)	100	250	—	100	250	—	100	250	—	pF
Open-Loop Output Resistance	R_O		—	150	—	—	150	—	—	150	—	Ω

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -55^\circ C/+125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-43A			OP-43B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	400	750	—	600	1750	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	2.5	5	—	3.5	10	$\mu V/^\circ C$
Offset Current	I_{OS}	(Note 1)	—	40	1000	—	50	2000	pA
Bias Current	I_B	(Note 1)	—	4000	7500	—	4500	15000	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.0	± 12.5	—	± 11.5	± 12.5	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11	+15 -11.5	—	± 11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	105	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	5	40	—	10	100	$\mu V/V$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6	+12 -17	± 36	± 6	+12 -17	± 36	mA
Slew Rate	SR		5	6	—	5	6	—	V/ μs
Gain Bandwidth	GBW		—	2.4	—	—	2.4	—	MHz
Power Bandwidth	BW_P		—	100	—	—	100	—	kHz
Capacitive Load Stability		$A_V = -1$ (Note 3)	100	250	—	100	250	—	pF

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -25^\circ C/+85^\circ C$ for E/F grades and $0^\circ C/70^\circ C$ for G grade, unless otherwise noted.

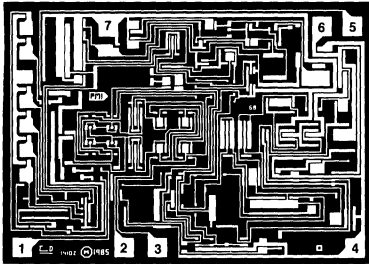
PARAMETER	SYMBOL	CONDITIONS	OP-43E			OP-43F			OP-43G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	250	750	—	500	1750	—	500	2000	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	3.5	8	—	7.5	—	—	7.5	—	$\mu V/^\circ C$
Offset Current	I_{OS}	(Note 1)	—	5	100	—	10	200	—	20	—	pA
Bias Current	I_B	(Note 1)	—	240	500	—	300	1000	—	100	500	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	300	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.0	± 12.6	—	± 11.5	± 12.5	—	± 11	± 12.6	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.2	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11.0	+15 -11.5	—	± 11	+15 -11.5	—	± 11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	110	—	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	5	40	—	10	100	—	10	100	$\mu V/V$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6	+16 -18	± 36	± 6	+16 -18	± 36	± 6	+20 -18	± 36	mA
Slew Rate	SR		5	6	—	5	6	—	5	6	—	V/ μs
Gain Bandwidth	GBW		—	2.4	—	—	2.4	—	—	2.4	—	MHz
Power Bandwidth	BW_p		—	100	—	—	100	—	—	100	—	kHz
Capacitive Load Stability		$A_V = -1$ (Note 3)	100	250	—	100	250	—	100	250	—	pF

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.



DICE CHARACTERISTICS



DIE SIZE 0.103 × 0.074 inch, 7622 sq. mils
(2.62 × 1.88mm, 4.92 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-43N LIMIT	UNITS
Offset Voltage	V_{OS}		750	μV MAX
Bias Current	I_B	(Note 1)	20	pA MAX
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12	V MIN
Supply Current	I_{SY}	$V_O = 0V$	1.2	mA MAX
Input Voltage Range	IVR	(Note 2)	± 11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	80	$\mu V/V$ MAX
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6	mA MIN
Slew Rate	SR		5	V/ μs MIN
Capacitive Load Stability	$A_V = -1$	(Note 3)	100	pF MIN

NOTES:

1. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

Precision Monolithics Inc.

FEATURES

- Open-Loop Gain 10,000,000V/V Min
- Low Input Offset Voltage 25 μ V Max
- Low Input Bias Current 5nA Max
- Excellent TCV_{OS} 0.3 μ V/ $^{\circ}$ C Max
- High CMRR 126dB Min
- High PSRR 126dB Min
- Low Noise 5.5nV/ $\sqrt{\text{Hz}}$ @ f = 10Hz
4.5nV/ $\sqrt{\text{Hz}}$ @ f = 1kHz
- High Output Current ± 50 mA
- Drives Capacitive Loads up to 10nF
- On-Board Thermal Shutdown Circuit

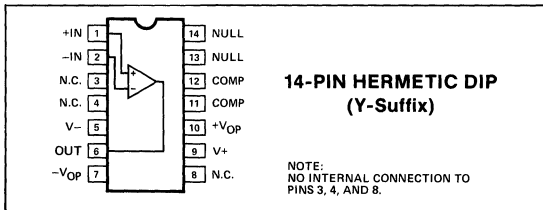
ORDERING INFORMATION†

$T_A = 25^{\circ}\text{C}$ V_{OS} MAX (μV)	PACKAGE	OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	
25	OP-50AY*	MIL
100	OP-50BY*	MIL
25	OP-50EY	IND
100	OP-50FY	IND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

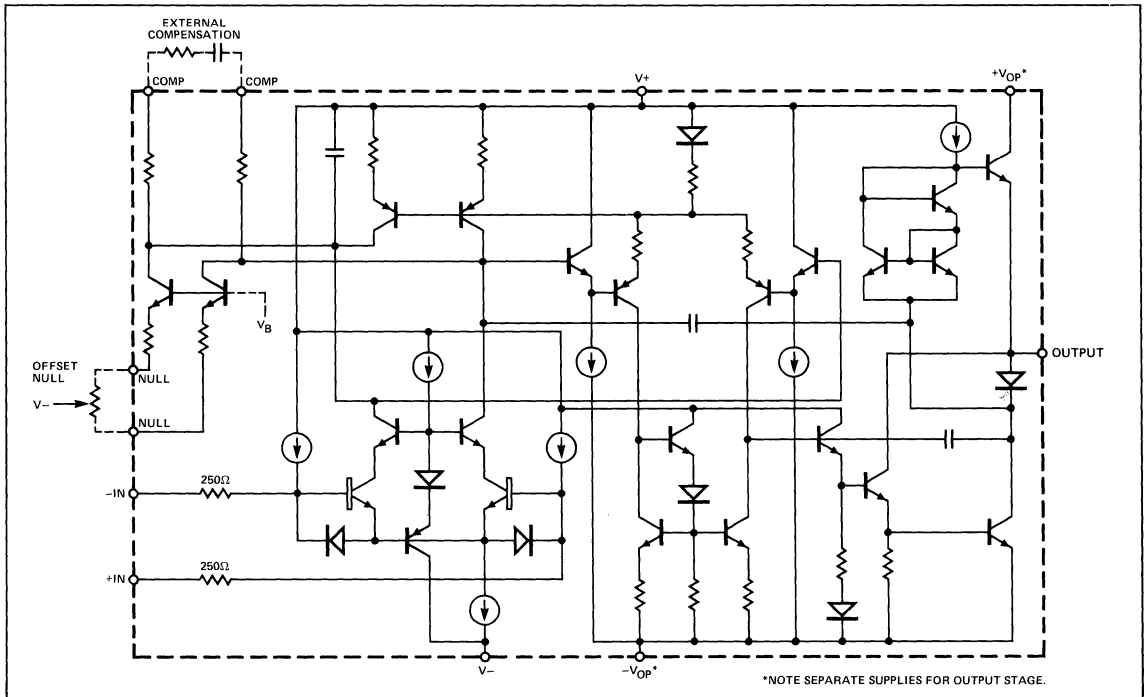
PIN CONNECTIONS



GENERAL DESCRIPTION

The OP-50 eliminates the need for an output buffer in applications which require high load-driving capability coupled with premium amplifier performance. The output stage can drive ± 50 mA into 50 Ω loads. In addition, the output is stable with capacitive loads of up to 10nF. This load driving ability makes the OP-50 ideal for amplifying small signals for transmission through long cables. The amplifier features open-loop voltage gain of over 10 million with common-mode rejection and power supply rejection of greater than 126dB (A/E grades).

SIMPLIFIED SCHEMATIC



Manufactured under the following patents: 4,471,321 and 4,503,381.



The OP-50 is stable for closed-loop gains above 50, and can be externally compensated for closed-loop gains in the range of 5 to 50. The amplifier is designed for use in high-gain and/or high-output-current applications. For example, an OP-07 coupled with an output buffer can be replaced by a single OP-50 amplifier.

Ion-implanted superbeta transistors, combined with a patented input bias current cancellation circuit, provide an input bias current of only 5nA and input offset current of 1nA. Over the full military temperature range, input bias current and input offset current for an A-grade device does not exceed 8nA and 3nA, respectively. Input offset voltages are trimmed to a maximum of 25µV (A/E grades) and 100µV (B/F grades) using PMI's zener-zapping technique. This low offset eliminates the need for an offset trimpot in most applications.

Low voltage-noise, typically 4.5nV/√Hz at 1kHz, is achieved in the OP-50 with minimum sacrifice of input protection. Overload protection is provided by input resistors of 250Ω and emitter-base diodes. The input resistors provide current limit protection against differential inputs of up to ±10V; and the diodes prevent avalanche breakdown which could degrade the I_B, I_{OS}, and matching of the input stage transistors. External resistors can be added to the input to guard against higher input voltages; however, the added resistors will degrade noise voltage performance. When minimum noise voltage is required, source resistance should be kept below a few hundred ohms.

Separate output-stage power supply pins are provided on the OP-50 to allow control of device power dissipation and output voltage swing. The maximum voltage which may be applied across the power supply pins is ±18V. The guaranteed specifications are based on operating both stages at ±15V; however, there is minimal effect on DC performance when the main amplifier is operated at ±15V and the output stage is operated at a reduced voltage. When operating both the main amplifier and the output stage at the same voltages, the corresponding power supply pins may be tied together. Decoupling capacitors are recommended between the power supply pins and analog ground. It is necessary to use decoupling capacitors on each power supply pin when operating the output stage at supply voltages less than the amplifier supply voltage. Do not operate the output-stage negative power supply pin at a more negative voltage than the negative supply pin (V-).

A thermally-symmetric die layout, which differs from other op amp designs by the positioning of more devices along the center line, provides the OP-50 with a thermal drift of less than 0.3µV/°C. This layout feature is critical to the maintenance of high open-loop gain when driving large-current loads and dissipating hundreds of milliwatts in the device. The use of a heatsink is recommended to reduce internal temperature rise when operating at high output power levels. The use of standard dual-in-line package heatsinks will help to dissipate heat to the environment. Other techniques, such as the use of external voltage-dropping resistors, allow heat to be dissipated **outside** of the package. See Figure 5, "Driving 50Ω Loads", in the applications section.

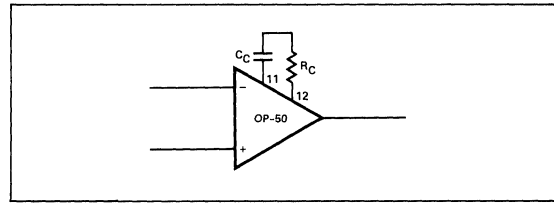
A thermal-shutdown circuit protects the OP-50 from overdisipation. When the die temperature reaches approximately 165°C, the output stage automatically shuts down. The amplifier input stage remains fully operational, thereby protecting the signal source from any loading changes caused by a complete shutdown.

COMPENSATION FOR GAINS BETWEEN 5 AND 50

The OP-50 can be compensated for inverting gains between 5 and 50 using a series resistor and capacitor. These values can be adjusted to minimize overshoot for a given application. The recommended compensation is:

GAIN RANGE	R _C	C _C
5 ≤ A _{VCL} ≤ 20	560Ω	4.7nF
20 ≤ A _{VCL} ≤ 50	3.3kΩ	1nF
A _{VCL} ≥ 50	No compensation required	

COMPENSATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2)	±18V
Internal Power Dissipation (Note 3)	500mW
Input Voltage	Supply Voltage
Differential Input Voltage (Note 4)	±10V
Differential Input Current (Note 4)	±20mA
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-50A, B	-55°C to +125°C
OP-50E, F	-25°C to +85°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T _J)	-65°C to +150°C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	106°C	11.3mW/°C

NOTES:

- Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
- Supply voltage rating applies to all power supply pins. No device pins should be connected to a voltage more negative than the supply to V-, pin 5.
- See table for maximum ambient temperature rating and derating factor.
- The OP-50's inputs are protected by 250Ω series resistors and protection diodes. If the differential input voltage exceeds ±10V, the input current must be limited to ±20mA.

5
OPERATIONAL AMPLIFIERS



ELECTRICAL CHARACTERISTICS at $V_+ = +V_{OP} = +15V$, $V_- = -V_{OP} = -15V$, $T_A = 25^\circ C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50A/E			OP-50B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	10	25	—	50	100	μV
Input Bias Current	I_B		—	± 1	± 5	—	± 1	± 10	nA
Input Offset Current	I_{OS}		—	0.1	1	—	0.1	3	nA
Input Voltage Range	IVR	CMRR $\geq 100dB$	± 12	—	—	± 12	—	—	V
Output Voltage Swing	V_O	$R_L \geq 500\Omega$ $R_L \geq 50\Omega$ (Note 1)	± 13 ± 2.5	± 13.4 ± 4.0	—	± 13 ± 2.5	± 13.4 ± 4.0	—	V
Output Voltage Swing	V_O	$V_+ = +V_{OP} = +5V$, $V_- = -V_{OP} = -5V$ $R_L = 500\Omega$ $R_L = 50\Omega$	± 3.5 ± 2.5	± 3.8 ± 2.8	—	± 3.5 ± 2.5	± 3.8 ± 2.8	—	V
Slew Rate	SR	$R_L \geq 2k\Omega$ $R_C = 560\Omega$ $C_C = 4.7nF$	2.5	3.0	—	2.5	3.0	—	V/ μs
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	126	140	—	110	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	0.1	0.5	—	0.5	1	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 1k\Omega$	10	20	—	7.5	15	—	V/ μV
Gain-Bandwidth Product	GBW	$A_{VCL} = 50$ (Note 2)	15	25	—	15	25	—	MHz
Offset Voltage Range Adjust		$R_P = 100k\Omega$	± 1.0	± 2.5	—	± 1.0	± 2.5	—	mV
Input Noise Voltage	e_{np-p}	$f = 0.1Hz$ to 10Hz	—	0.12	—	—	0.12	—	μV_{p-p}
Noise Voltage Density	e_n	$f = 10Hz$ $f = 1kHz$ (Note 3)	—	5.5 4.5	8.5 6.0	—	5.5 4.5	8.5 6.0	nV/\sqrt{Hz}
Noise Current	i_{np-p}	$f = 0.1Hz$ to 10Hz	—	2	—	—	2	—	pA_{p-p}
Noise Current Density	i_n	$f = 100Hz$ $f = 1kHz$	—	0.3 0.23	—	—	0.3 0.23	—	pA/\sqrt{Hz}
Quiescent Supply Current	I_{SY}	No Load	—	2.6	3.3	—	2.6	3.3	mA
Positive Current Limit	$+I_{SC}$	Output shorted to Ground	60	95	120	60	95	120	mA
Negative Current Limit	$-I_{SC}$	Output shorted to Ground	60	85	120	60	85	120	mA
Differential-Mode Input Resistance	R_{IND}		—	2	—	—	2	—	M Ω
Common-Mode Input Resistance	R_{INCM}		—	20	—	—	20	—	G Ω
Capacitive Load Capability	C_L	$A_{VCL} \geq 5$ $R_C = 560\Omega$ (Note 2) $C_C = 4.7nF$	10	—	—	10	—	—	nF
Settling-Time	t_s	Settling to 0.01%, $V_O = 20V_{p-p}$ $A_{VCL} = 500$ $A_{VCL} = 1000$	—	30 60	—	—	30 60	—	μs

NOTES:

1. Guaranteed by current limit tests.
2. Guaranteed by design.
3. Sample tested.



ELECTRICAL CHARACTERISTICS at $V_+ = +V_{OP} = +15V$, $V_- = -V_{OP} = -15V$, $-25^\circ C \leq T_A \leq +85^\circ C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50E			OP-50F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	20	45	—	50	150	μV
Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.15	0.3	—	0.3	1	$\mu V/^\circ C$
Input Bias Current	I_B		—	± 2	± 7	—	± 2	± 25	nA
Input Offset Current	I_{OS}		—	0.2	2.5	—	0.2	20	nA
Input Offset Current Drift	TCI_{OS}		—	3	—	—	5	—	$\mu A/^\circ C$
Input Bias Current Drift	TCI_B		—	20	—	—	50	—	$\mu A/^\circ C$
Input Voltage Range	IVR	$CMRR \geq 100dB$	± 11.5	—	—	± 11.5	—	—	V
Output Voltage Swing	V_O	$R_L \geq 500\Omega$	± 12	± 13.4	—	± 12	± 13.4	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	120	130	—	105	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	0.5	1.25	—	0.5	1.25	$\mu V/V$
Quiescent Supply Current	I_{SY}	No Load	—	2.8	4	—	2.8	4	mA
Open-Loop Gain	A_{VO}	$V_{OUT} = \pm 10V$, $R_L = 1k\Omega$ (Note 2)	4	15	—	4	15	—	$V/\mu V$

NOTES:

1. TCV_{OS} tested on E grade, guaranteed by design on F grade specification.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_+ = +V_{OP} = +15V$, $V_- = -V_{OP} = -15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, no compensation, unless otherwise noted.

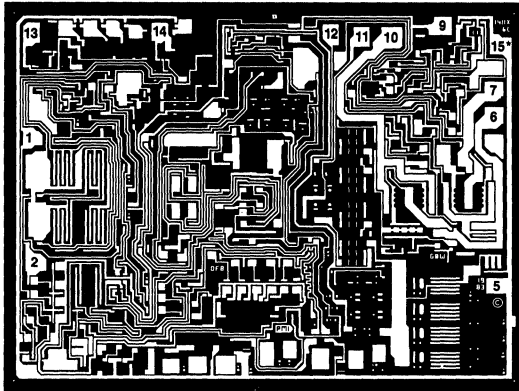
PARAMETER	SYMBOL	CONDITIONS	OP-50A			OP-50B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	20	55	—	50	200	μV
Input Offset Voltage Drift	TCV_{OS}		—	0.15	0.3	—	0.3	1	$\mu V/^\circ C$
Input Bias Current	I_B		—	± 2	± 8	—	± 2	± 20	nA
Input Offset Current	I_{OS}		—	0.5	3	—	0.5	12	nA
Input Offset Current Drift	TCI_{OS}		—	3	—	—	5	—	$\mu A/^\circ C$
Input Bias Current Drift	TCI_B		—	20	—	—	50	—	$\mu A/^\circ C$
Input Voltage Range	IVR	$CMRR \geq 100dB$	± 11.5	—	—	± 11.5	—	—	V
Output Voltage Swing	V_O	$R_L \geq 500\Omega$	± 12	± 13.2	—	± 12	± 13.2	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	120	130	—	105	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	0.5	1.25	—	0.5	1.25	$\mu V/V$
Quiescent Supply Current	I_{SY}	No Load	—	2.8	4	—	2.8	4	mA
Open-Loop Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 1k\Omega$ (Note 1)	4	10	—	4	10	—	$V/\mu V$

NOTE:

1. Tested at $+125^\circ C$, guaranteed by design at $-55^\circ C$.



DICE CHARACTERISTICS



DIE SIZE 0.110 × 0.148 inch, 16,280 sq. mils
(2.79 × 3.76 mm, 10.50 sq. mm)

1. NONINVERTING INPUT
2. INVERTING INPUT
5. V^-
6. OUTPUT
7. $-V_{OP}$
9. V^+
10. $+V_{OP}$
11. COMPENSATION
12. COMPENSATION
13. NULL
14. NULL
15. V^- (OPTIONAL BONDING PAD)*

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V^+ = +V_{OP} = +15V$, $V^- = -V_{OP} = -15V$, $T_A = 25^\circ C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50G LIMIT	UNITS
Input Offset Voltage	V_{OS}		100	μV MAX
Input Bias Current	I_B		± 10	nA MAX
Input Offset Current	I_{OS}		3	nA MAX
Output Voltage Swing	V_O	$R_L \geq 500\Omega$	± 13	V MIN
Output Voltage Swing	V_O	$V^+ = +V_{OP} = +5V$, $V^- = -V_{OP} = -5V$ $R_L = 500\Omega$ $R_L = 50\Omega$	± 3.5 ± 2.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	1	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 1k\Omega$	7.5	$V/\mu V$ MIN
Positive Current Limit	$+I_{SC}$	Output shorted to Ground	60	mA MIN
Negative Current Limit	$-I_{SC}$	Output shorted to Ground	60	mA MIN
Quiescent Supply Current	I_{SY}	No Load	3.3	mA MAX

NOTE:

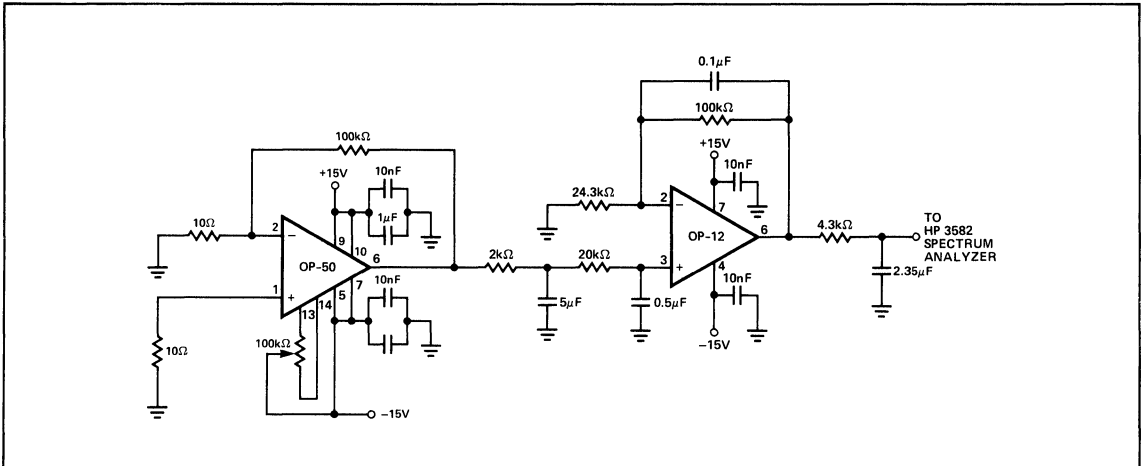
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



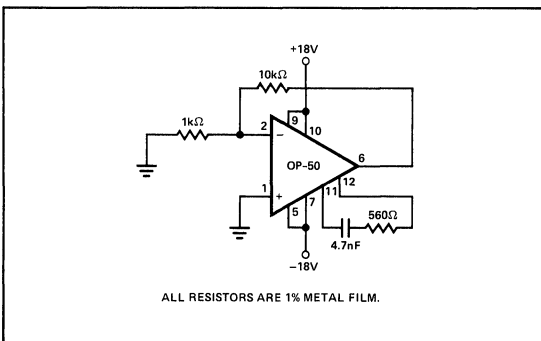
TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = +V_{OP} = +15V$, $V_- = -V_{OP} = -15V$, $T_A = 25^\circ C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50G TYPICAL	UNITS
Slew Rate	SR	$R_L \geq 2k\Omega$ $R_C = 560\Omega$ $C_C = 4.7nF$	3	V/ μs
Noise Voltage Density	e_n	$f = 10Hz$ $f = 1kHz$	5.5 4.5	nV/ \sqrt{Hz}
Input Noise Voltage	e_{np-p}	$f = 0.1Hz$ to 10Hz	0.12	μV_{p-p}
Noise Current Density	i_n	$f = 10Hz$ $f = 1kHz$	0.2 0.15	pA/ \sqrt{Hz}
Capacitive Load Capability	C_L	$A_{VOL} \geq 5$ $R_C = 560\Omega$ $C_C = 4.7nF$	10	nF

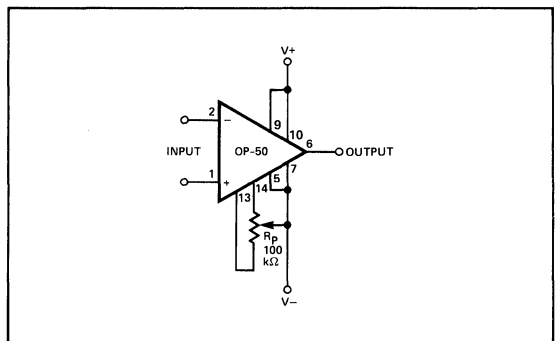
NOISE TEST CIRCUIT (0.1 TO 10Hz)



BURN-IN CIRCUIT

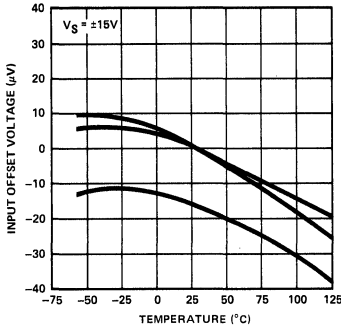
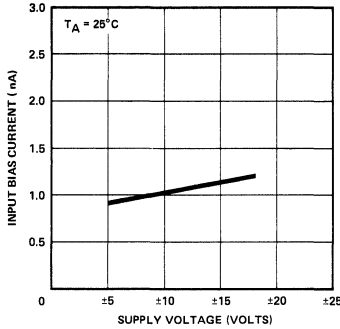
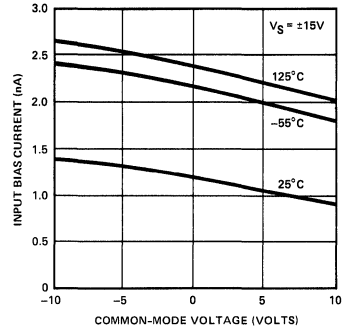
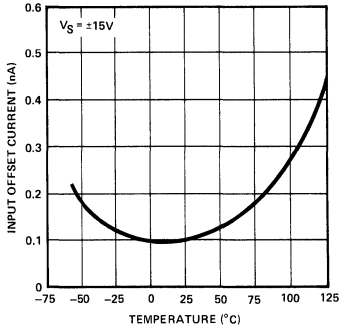
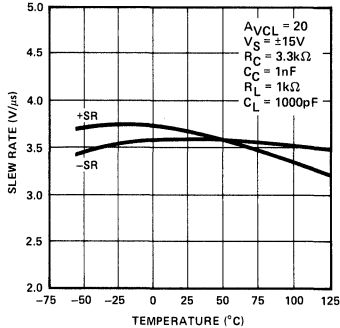
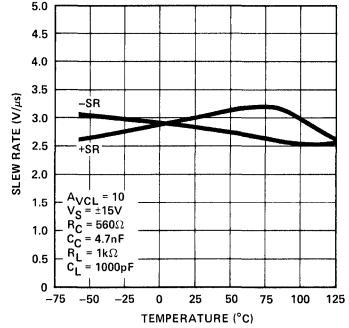
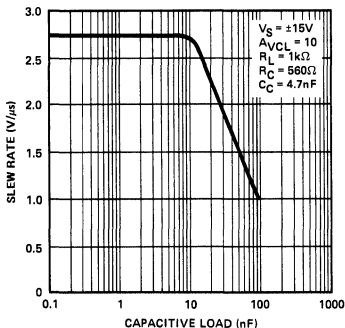
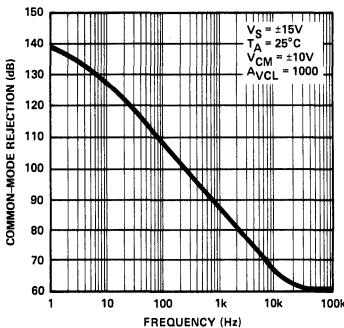
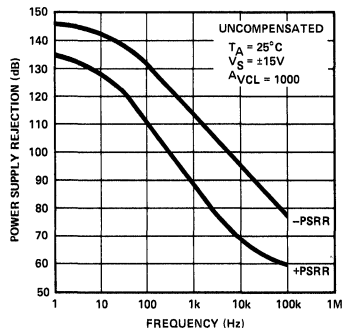


OFFSET NULLING CIRCUIT



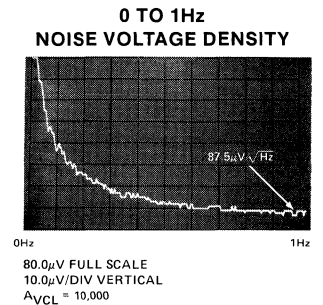
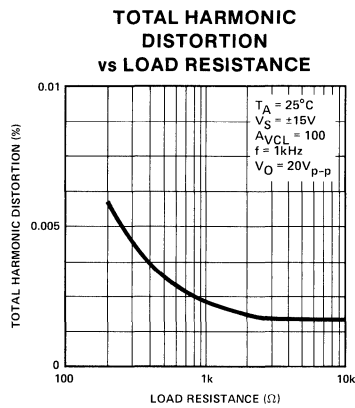
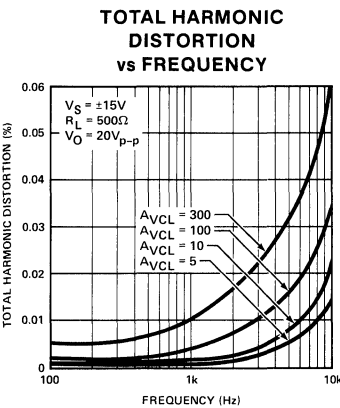
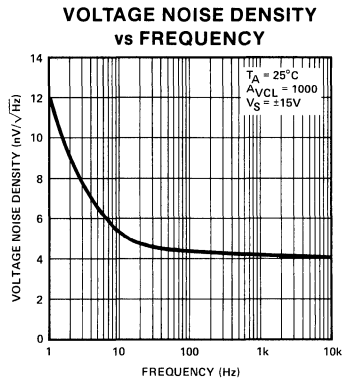
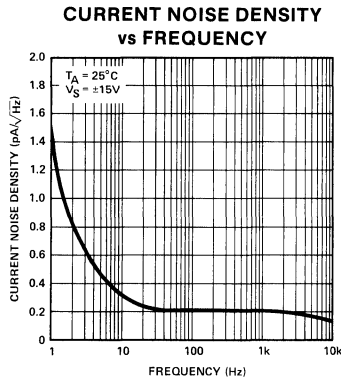
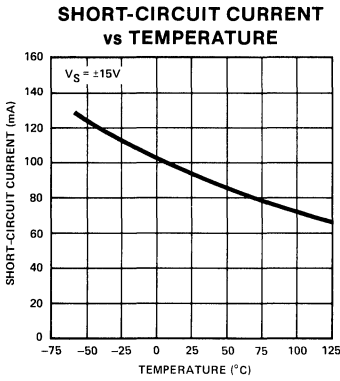
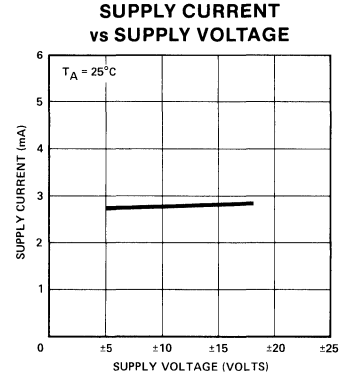
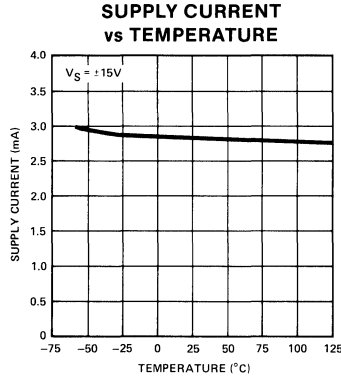
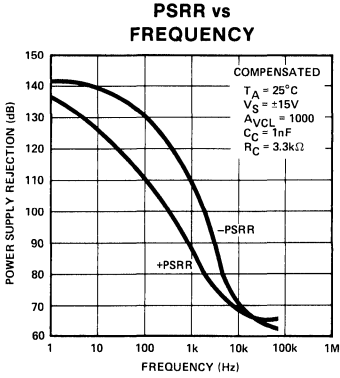
5
OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT OFFSET VOLTAGE vs TEMPERATURE

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

INPUT OFFSET CURRENT vs TEMPERATURE

SLEW RATE vs TEMPERATURE

SLEW RATE vs TEMPERATURE

SLEW RATE vs CAPACITIVE LOAD

CMRR vs FREQUENCY

PSRR vs FREQUENCY

NOTE:

The symbol $\pm V_S$ is used to indicate the supply voltages when the main amplifier and the output stage are being operated at the same voltages.

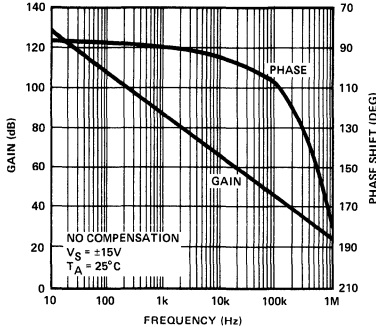
TYPICAL PERFORMANCE CHARACTERISTICS



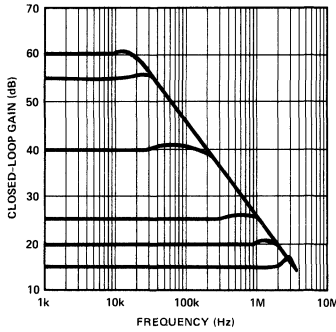


TYPICAL PERFORMANCE CHARACTERISTICS

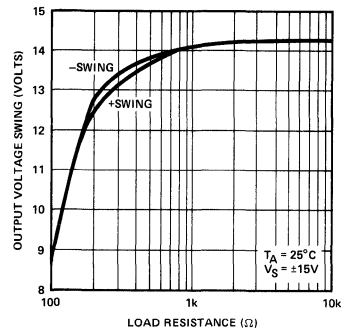
GAIN, PHASE SHIFT vs FREQUENCY



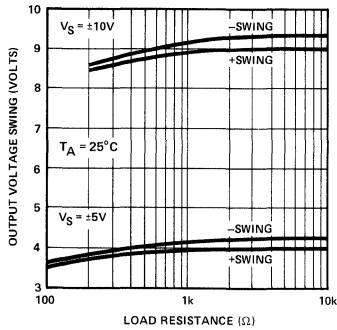
CLOSED-LOOP GAIN vs FREQUENCY



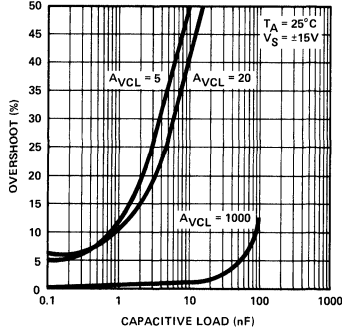
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



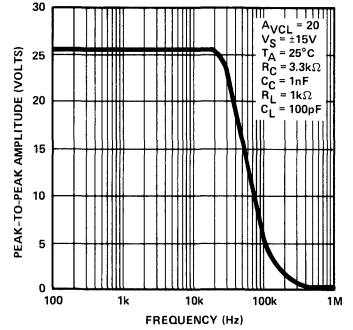
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



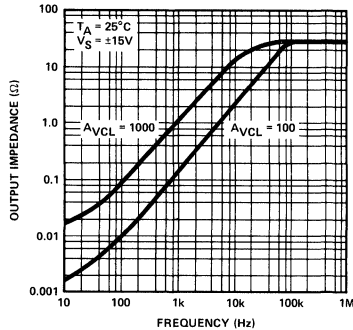
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

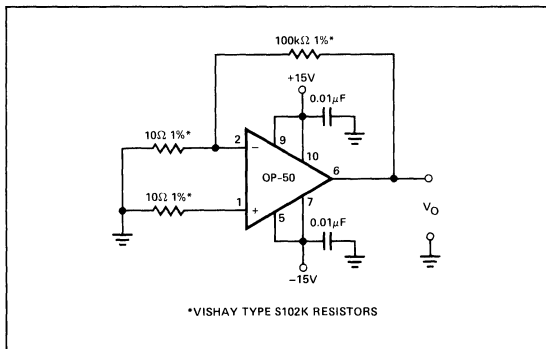


MAXIMUM OUTPUT SWING vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY



TCV_{OS} TEST CIRCUIT


overdriving of the long-tailed transistor pair and stop saturation of the output transistor. Power supply voltage is set to $\pm 5V$ to lower the quiescent power dissipation and minimize thermal feedback due to output stage dissipation. Operating from $\pm 5V$ supplies also reduces the OP-50 rise and fall times as the output slews over a reduced voltage range. This, in turn, reduces the output response time.

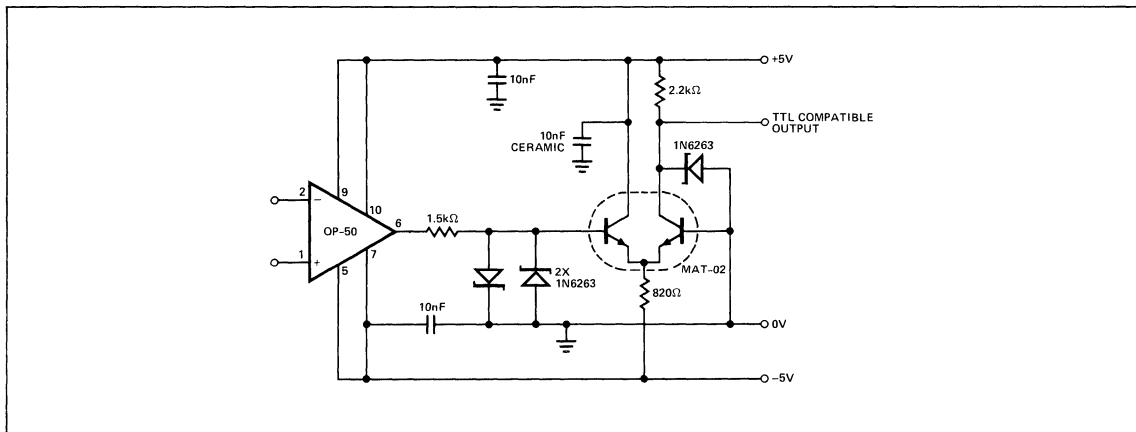
It is common practice with voltage comparators to ground one input terminal and to use a single-ended input. The historic reason is poor common-mode rejection on the input stage. In contrast, the OP-50 has very high common-mode rejection and is capable of detecting microvolt level differences in the presence of large common-mode signals.

The comparator is not fast, but it is very sensitive and can detect signal differences as low as $0.3\mu V$. With large input overdrives, the circuit responds in approximately $3\mu s$. If sharp transitions are needed, the use of a TTL Schmitt-trigger input is recommended. A table of Response Time vs. Input Overdrive is shown below.

APPLICATIONS INFORMATION
HIGH-SENSITIVITY VOLTAGE COMPARATOR

A comparator capable of resolving a submicrovolt difference signal is shown in Figure 1. The OP-50, operating without feedback, drives a second gain stage which generates a TTL-compatible output signal. Schottky-clamp diodes prevent

INPUT OVERDRIVE	100mV	10mV	1mV	100 μ V	10 μ V
Positive Output Delay	3.2 μ s	5 μ s	40 μ s	340 μ s	2.4ms
Negative Output Delay	1.8 μ s	5 μ s	50 μ s	380 μ s	4.5ms


FIGURE 1: HIGH-SENSITIVITY VOLTAGE COMPARATOR

INTEGRATOR AND UNITY-GAIN BUFFER

Figure 2 shows a method of obtaining unity-gain in a buffer configuration. The R1 and C1 network provides input compensation to circumvent the minimum gain requirement. Figure 3 shows the same technique applied in the inverting mode to form a high precision integrator.

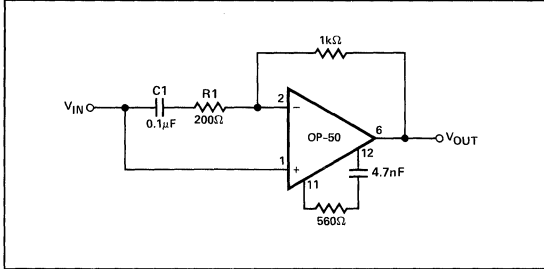


FIGURE 2: UNITY GAIN BUFFER

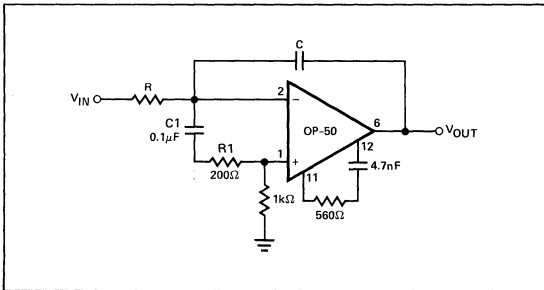


FIGURE 3: INTEGRATOR

20mA CURRENT SOURCE

The 20mA current source exploits the high output current and high linearity capabilities of the OP-50. Five precision resistors and a trim potentiometer are required in this circuit configuration, known as the Howland Current Pump. The trim potentiometer is used to balance the resistive feedback dividers. This maximizes the current-source output impedance. Compensation is selected for a voltage gain of 10.

Compliance is better than $\pm 11V$ at an output current of 20mA and the trimmed output resistance is typically $2M\Omega$ with $R_L \leq 500\Omega$. The transfer function is given by:

$$I_{OUT} = \frac{V_{IN(DIFF)} \times 10.1}{101} \text{ Amps}$$

$V_{IN(DIFF)}$ is the differential input voltage. For the resistor values shown in Figure 4, the maximum $V_{IN(DIFF)}$ is 200mV.

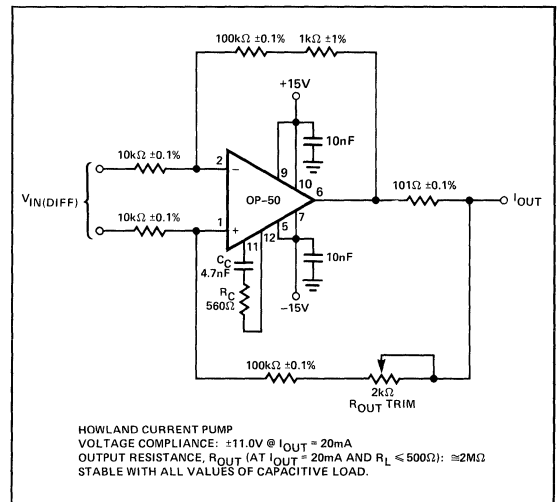


FIGURE 4: 20mA CURRENT SOURCE

DRIVING 50Ω LOADS

The OP-50 can provide up to 50mA into a 50Ω load and up to 26mA into a 500Ω load. The output is stable driving capacitive loads of up to 10nF.

Applications that make use of the high output current capability of the OP-50 will cause increased power dissipation in the amplifier. To reduce internal dissipation in these applications, external voltage dropping resistors can be connected in series with the output-stage power supply pins. As shown in Figure 5, 130Ω resistors can be attached to pin 7 ($-V_{OP}$) and to pin 10 ($+V_{OP}$). To maintain stability and specified performance levels, 0.047μF decoupling capacitors should be used as indicated from pin 7 and pin 10 to ground.

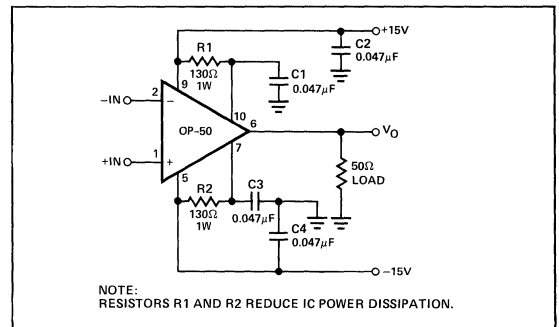


FIGURE 5: DRIVING 50Ω LOADS

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Outstanding Gain Linearity
- Ultra High Gain 5000V/mV Min
- Low V_{OS} 25 μ V Max
- Excellent TCV_{OS} 0.3 μ V/ $^{\circ}$ C Max
- High PSRR 3 μ V/V Max
- High CMRR 1.0 μ V/V Max
- Low Power Consumption 60mW Max
- Fits OP-07, 725, 108A/308A, 741 Sockets

ORDERING INFORMATION†

PACKAGE			OPERATING TEMPERATURE RANGE
TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	
OP77AJ*	OP77AZ*		MIL
OP77EJ	OP77EZ	OP77EP	IND
OP77BJ*	OP77BZ*		MIL
OP77FJ	OP77FZ	OP77FP	IND
	OP77GZ	OP77GP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-77 significantly advances the state-of-the-art in precision op amps. The OP-77's outstanding gain of 10,000,000 or more is maintained over the full ± 10 V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps, and provides superior performance in high closed-loop-gain applications.

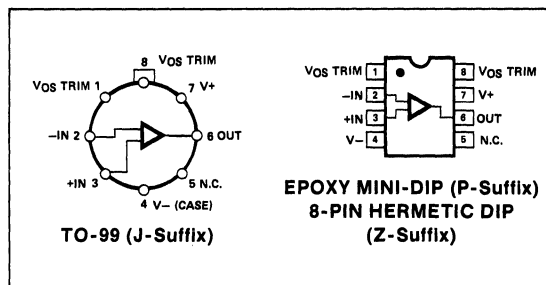
Low initial V_{OS} drift and rapid stabilization time, combined with only 50mW power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional TCV_{OS} of 0.3 μ V/ $^{\circ}$ C maximum and the low V_{OS} of 25 μ V maximum, eliminates the need for V_{OS} adjustment and increases system accuracy over temperature.

PSRR of 3 μ V/V (110dB) and CMRR of 1.0 μ V/V maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP-77 ideally suited for high-resolution instrumentation and other tight error budget systems.

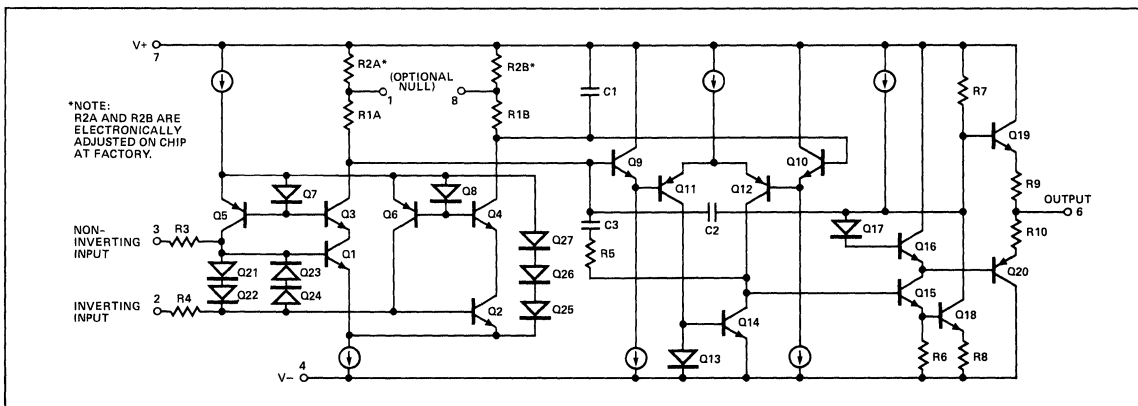
This product is available in five standard grades and three standard packages: the TO-99 can and the 8-pin mini-dip in ceramic or epoxy.

The OP-77 is a direct or upgrade replacement for the OP-07, OP-05, 725, or 108A op amps. 741-types can be replaced by eliminating the V_{OS} adjust pot.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range	
OP-77A, OP-77B	-55°C to +125°C
OP-77E, OP-77F	-25°C to +85°C
OP-77G	0°C to 70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T _j)	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77A			OP-77B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}		—	10	25	—	20	60	μV
Long-Term Input Offset Voltage Stability	ΔV _{OS} /Time	(Note 1)	—	0.2	—	—	0.2	—	μV/Mo
Input Offset Current	I _{OS}		—	0.1	1.5	—	0.1	2.8	nA
Input Bias Current	I _B		-0.2	1.2	2.0	-0.2	1.2	2.8	nA
Input Noise Voltage	e _{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	μV _{p-p}
Input Noise Voltage Density	e _n	f _O = 10Hz (Note 2)	—	10.3	18.0	—	10.3	18.0	nV/√Hz
		f _O = 100Hz (Note 2)	—	10.0	13.0	—	10.0	13.0	
		f _O = 1000Hz (Note 2)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i _{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	pA _{p-p}
Input Noise Current Density	i _n	f _O = 10Hz (Note 2)	—	0.32	0.80	—	0.32	0.80	pA/√Hz
		f _O = 100Hz (Note 2)	—	0.14	0.23	—	0.14	0.23	
		f _O = 1000Hz (Note 2)	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R _{IN}	(Note 3)	26	45	—	18.5	45	—	MΩ
Input Resistance — Common-Mode	R _{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±13V	—	0.1	1.0	—	0.1	1.6	μV/V
Power Supply Rejection Ratio	PSRR	V _S = ±3V to ±18V	—	1.0	3	—	1.0	3	μV/V
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2kΩ, V _O = ±10V	5000	12000	—	2000	8000	—	V/mV
		R _L ≥ 10kΩ	±13.5	±14.0	—	±13.5	±14.0	—	V
		R _L ≥ 2kΩ	±12.5	±13.0	—	±12.5	±13.0	—	
Output Voltage Swing	V _O	R _L ≥ 1kΩ	±12.0	±12.5	—	±12.0	±12.5	—	
Slew Rate	SR	R _L ≥ 2kΩ (Note 2)	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	A _{VCL} = +1 (Note 2)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R _O	V _O = 0, I _O = 0	—	60	—	—	60	—	Ω
Power Consumption	P _d	V _S = ±15V, No Load	—	50	60	—	50	60	mW
		V _S = ±3V, No Load	—	3.5	4.5	—	3.5	4.5	
Offset Adjustment Range		R _P = 20kΩ	—	±3	—	—	±3	—	mV

NOTES:1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.

2. Sample tested.

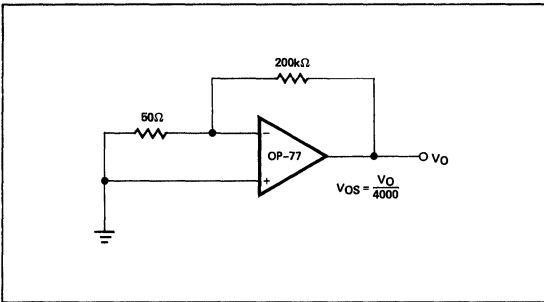
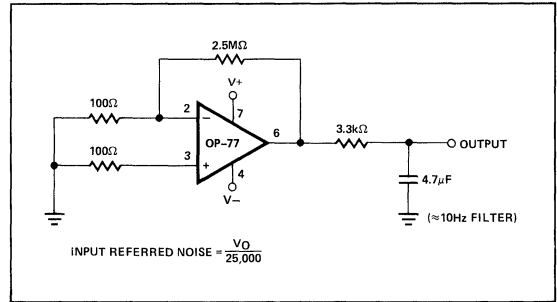
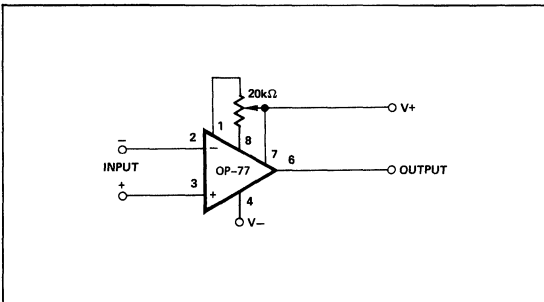
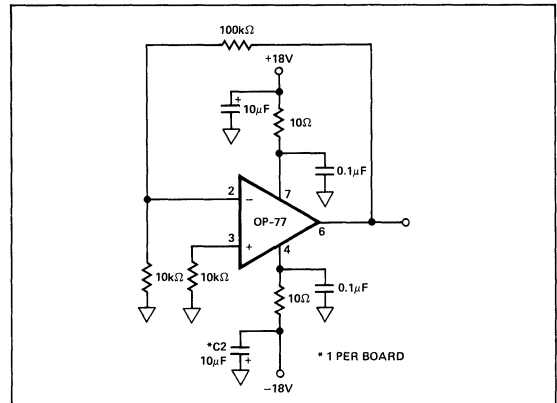
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77A			OP-77B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	25	60	—	45	120	μV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.1	0.3	—	0.2	0.6	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.1	2.2	—	0.1	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	0.5	25	—	0.5	50	$pA/^\circ C$
Input Bias Current	I_B		-0.2	2.4	4	-0.2	2.4	6	nA
Average Input Bias Current Drift	TCI_B	(Note 1)	—	8	25	—	15	35	$pA/^\circ C$
Input Voltage Range	IVR		± 13	± 13.5	—	± 13	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	3	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	1	3	—	1	5	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	2000	6000	—	1000	4000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 12.5	—	± 12	± 12.5	—	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	60	75	—	60	75	mW

NOTES:

1. Sample tested.
2. Guaranteed by design.

TYPICAL OFFSET VOLTAGE TEST CIRCUIT

TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT

OPTIONAL OFFSET NULLING CIRCUIT

BURN-IN CIRCUIT


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77E			OP-77F/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	10	25	—	20	60	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 1)	—	0.3	—	—	0.4	—	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	0.1	1.5	—	0.1	2.8	nA
Input Bias Current	I_B		-0.2	1.2	2.0	-0.2	1.2	2.8	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	10.0	13.0	—	10.2	13.5	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.35	0.90	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	0.14	0.23	—	0.15	0.27	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	26	45	—	18.5	45	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	1.6	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	1.0	3.0	—	1.0	3.0	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	5000	12000	—	2000	6000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
		$R_L \geq 2k\Omega$	± 12.5	± 13.0	—	± 12.5	± 13.0	—	
		$R_L \geq 1k\Omega$	± 12.0	± 12.5	—	± 12.0	± 12.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 2)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	50	60	—	50	60	mW
		$V_S = \pm 3V$, No Load	—	3.5	4.5	—	3.5	4.5	
Offset Adjustment Range		$R_p = 20k\Omega$	—	± 3	—	—	± 3	—	mV

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$.
2. Sample tested.
3. Guaranteed by design.

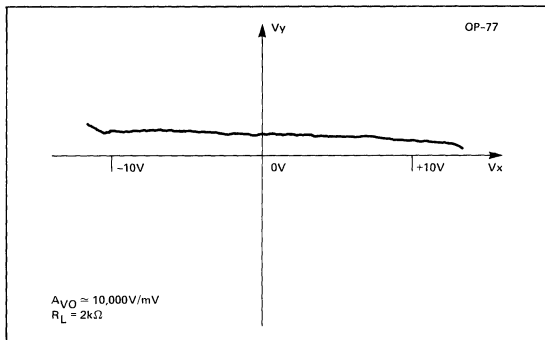
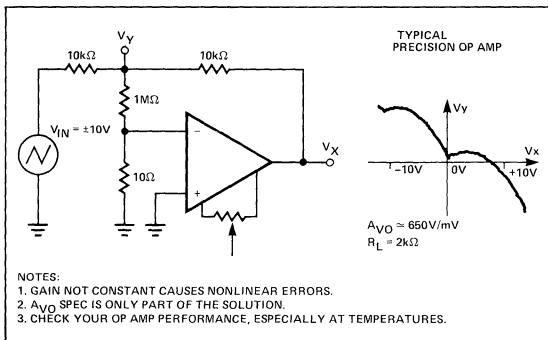
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-77E/F, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-77G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77E			OP-77F/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	10	45	—	20	100	μV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.1	0.3	—	0.2	0.6	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.1	2.2	—	0.1	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	0.5	40	—	0.5	85	$pA/^\circ C$
Input Bias Current	I_B		-0.2	2.4	4.0	-0.2	2.4	6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 1)	—	8	40	—	15	60	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	3.0	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	1.0	3.0	—	1.0	5.0	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	2000	6000	—	1000	4000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13.0	—	± 12	± 13.0	—	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	60	75	—	60	75	mW

NOTES:

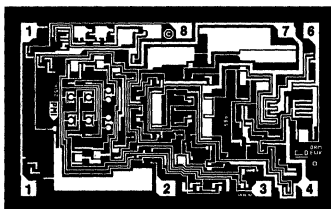
1. Sample tested.
2. Guaranteed by design.

OPEN-LOOP GAIN LINEARITY



Actual open-loop voltage can vary greatly at various output voltages. All automated testers use end-point testing and therefore only show the average gain. This causes errors in high closed-loop gain circuits. Since this is so difficult for manufacturers to test, you should make your own evaluation. This simple test circuit makes it easy. An ideal op amp would show a horizontal scope trace.

This is the output gain linearity trace for the new OP-77. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. The average open-loop gain is truly impressive — approximately 10,000,000.

DICE CHARACTERISTICS


1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
6. OUTPUT
7. V+
8. BALANCE

DIE SIZE 0.100 × 0.061 inch, 6100 sq. mils
(2.54 × 1.55 mm, 3.935 sq. mm)

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-77N/G devices.

PARAMETER	SYMBOL	CONDITIONS	OP-77N LIMIT	OP-77G LIMIT	UNITS
Input Offset Voltage	V_{OS}		40	75	μV MAX
Input Offset Current	I_{OS}		2.0	2.8	nA MAX
Input Bias Current	I_B		± 2	± 2.8	nA MAX
Input Resistance Differential-Mode	R_{IN}	(Note 1)	26	17	M Ω MIN
Input Voltage Range	IVR		± 13	± 13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	1	1.6	$\mu V/V$ MAX
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	3	3	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	± 13.5 ± 12.5 ± 12.0	± 13.5 ± 12.5 ± 12.0	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	2000	1000	V/mV MIN
Differential Input Voltage			± 30	± 30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	60	60	mW MAX

NOTES:

1. Guaranteed by design.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77N TYPICAL	OP-77G TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	0.1	0.2	$\mu V/^\circ C$
Nullled Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, $R_P = 20k\Omega$	0.1	0.2	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	$pA/^\circ C$
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	MHz



OP-90

LOW-VOLTAGE MICROPOWER OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- **Single/Dual Supply Operation** +1.6V to +36V
..... ±0.8V to ±18V
- **Input and Output Swing to Ground in Single Supply Operation**
- **Low Supply Current** 18µA Max
- **High Output Drive** 5mA Min
- **Low Input Offset Voltage** 50µV Max
- **High Open-Loop Gain** 2000V/mV Min

ORDERING INFORMATION†

T _A = 25°C V _{OS} Max (µV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	
50	OP90AZ*		MIL
50	OP90EZ	OP90EP	IND
100	OP90BZ*		MIL
100	OP90FZ	OP90FP	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

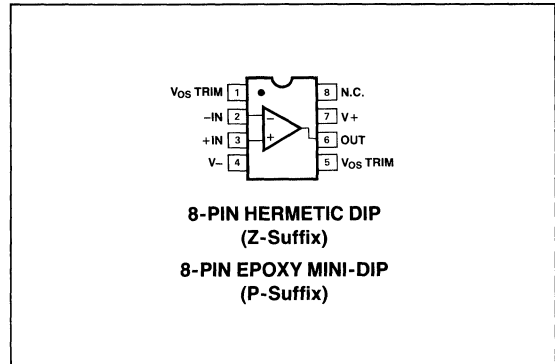
GENERAL DESCRIPTION

The OP-90 is a high-performance micropower op amp operable from a single supply of +1.6V to +36V or from dual supplies of ±0.8V to ±18V. Input voltage range extends to the negative rail allowing the OP-90 to accommodate input signals down to zero volts in single supply operation. The OP-90's output will swing to ground when operating from a single supply, enabling "zero in-zero out" operation.

The OP-90 draws only 12µA of quiescent supply current, while able to deliver over 5mA of output current to a load. The extremely low input offset voltage of less than 50µV virtually eliminates any need for external V_{OS} nulling. It has an open-loop gain of over 2 million, a CMRR above 110dB, and a PSRR that is under 10µV/V. The OP-90 features a noise voltage density of 35nV/√Hz at 30Hz, a very low value in comparison to other micropower op amps.

With its low offset voltage and high gain, the OP-90 brings precision performance to micropower applications. The low supply voltage requirements of the OP-90 combined with its minimal power consumption enables it to be powered by batteries or solar cells and is ideal for applications in portable instruments, remote sensors, and satellites.

PIN CONNECTIONS



5 OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-90A/E			OP-90B			OP-90F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	V _S = ±15V	—	—	150	—	—	250	—	—	250	µV
		V ₊ = +5V, V ₋ = -5V	—	—	50	—	—	100	—	—	100	
Input Offset Current	I _{OS}		—	—	1	—	—	2	—	—	2.5	nA
Input Bias Current	I _B		—	—	10	—	—	15	—	—	20	nA
Input Noise Voltage Density	e _n	f ₀ = 30Hz	—	35	—	—	35	—	—	40	—	nV/√Hz
Input Voltage Range	IVR	V _S = ±15V	-15/+14.2	—	—	-15/+14.0	—	—	-15/+14.0	—	—	V
		V ₊ = +5V, V ₋ = 0V	0/+4.2	—	—	0/+4.0	—	—	0/+4.0	—	—	
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±14V	110	—	—	107	—	—	104	—	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±1V to ±15V	—	—	10	—	—	15	—	—	15	µV/V

This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-90A/E			OP-90B			OP-90F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 100k\Omega$	2000	—	—	1000	—	—	1000	—	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 100k\Omega$ $V_S = \pm 15V$ $V+ = +5V, V- = 0V$	± 14.2 0/+4.2	—	—	± 14.0 0/+4.0	—	—	± 14.0 0/+4.0	—	—	V
Gain Bandwidth Product	GBW		—	25	—	—	25	—	—	25	—	kHz
Supply Current	I_{SY}	No Load	—	—	18	—	—	18	—	—	20	μA
Slew Rate	SR		—	8	—	—	8	—	—	8	—	V/ms

Precision Monolithics Inc.

FEATURES

- Low V_{OS} **100 μ V Max**
- Offset Voltage Match **90 μ V Max**
- Offset Voltage Match vs. Temp. **1.0 μ V/ $^{\circ}$ C Max**
- Common-Mode Rejection Match **103dB Min**
- Bias Current Match **3.5nA Max**
- Low Noise **0.6 μ V_{p-p} Max**
- Low Bias Current **3.0nA Max**
- High Channel Separation **126dB Min**

ORDERING INFORMATION†

$T_A = 25^{\circ}$ C V_{OS} MAX (μ V)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
100	OP207AY*	MIL
100	OP207EY	COM
200	OP207BY*	MIL
200	OP207FY	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

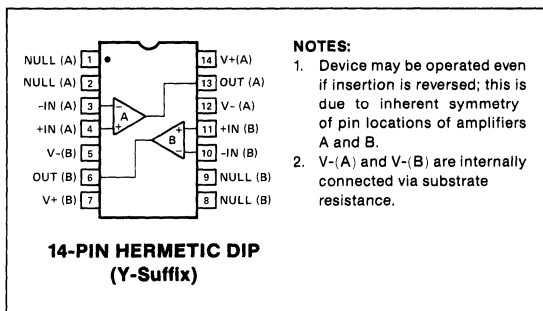
The OP-207 series of dual matched operational amplifiers consists of two independent OP-07 high performance operational amplifiers in a single 14-pin dual-in-line package. Exceptionally low offset voltage and tight matching of critical

parameters is provided between the channels of this dual operational amplifier.

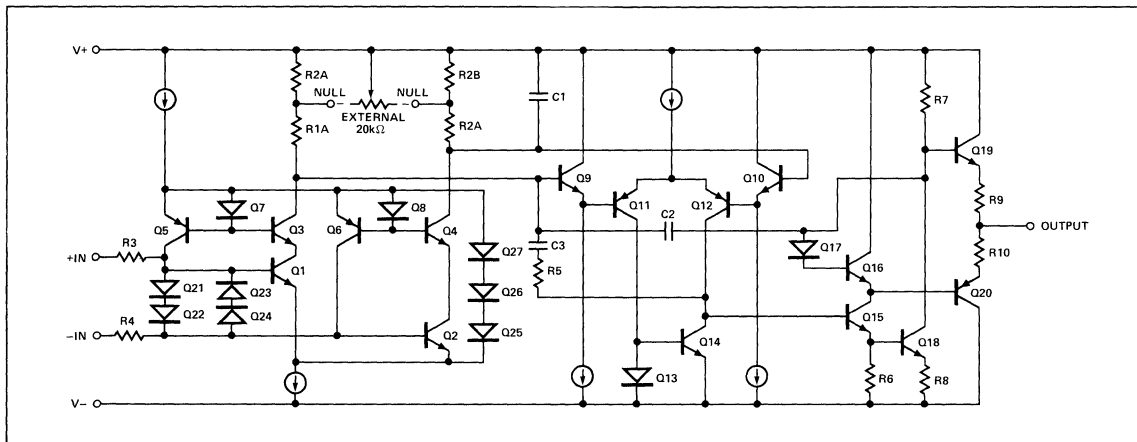
The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. Each amplifier is fully compensated and protected.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode rejection.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/2 OP-207)



5
OPERATIONAL AMPLIFIERS

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	$\pm 22V$
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	$\pm 30V$
Input Voltage (Note 2)	$\pm 22V$
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature Range	
OP-207A, OP-207B	$-55^{\circ}C$ to $+125^{\circ}C$
OP-207E, OP-207F	$0^{\circ}C$ to $+70^{\circ}C$

Lead Temperature (Soldering, 60 sec) $300^{\circ}C$ **NOTES:**

- See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP	$106^{\circ}C$	$11.3mW/^{\circ}C$

- For supply voltages less than $\pm 22V$, the absolute maximum input voltage is equal to the supply voltage.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A/E			OP-207B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	30	90	—	50	280	μV
Average Noninverting Bias Current	I_{B+}		—	± 1.5	± 3.5	—	± 1.5	± 6.0	nA
Noninverting Offset Current	I_{OS+}		—	± 0.7	± 3.5	—	± 1.0	± 6.0	nA
Inverting Offset Current	I_{OS-}		—	± 0.7	± 3.5	—	± 1.0	± 6.0	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	103	120	—	96	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Channel Separation			126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A			OP-207B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	70	180	—	180	450	μV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	—	0.9	1.5	$\mu V/^{\circ}C$
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 1)	—	0.3	1.0	—	0.4	1.3	
Average Noninverting Bias Current	I_{B+}		—	± 2	± 6	—	± 3	± 12	nA
Average Drift of Non-inverting Bias Current	TCI_{B+}		—	10	—	—	12	—	$pA/^{\circ}C$
Noninverting Offset Current	I_{OS+}		—	2	6.5	—	3	12	nA
Average Drift of Non-inverting Offset Current	TCI_{OS+}		—	12	—	—	15	—	$pA/^{\circ}C$
Inverting Offset Current	I_{OS-}		—	2	6.5	—	3	12	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	100	117	—	94	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	—	16	100	$\mu V/V$

NOTE:

- Sample tested.



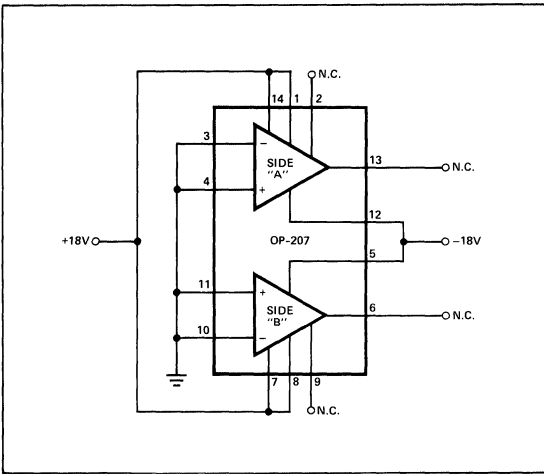
MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	60	150	—	120	350	μV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	—	0.9	1.5	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 1)	—	0.3	1.0	—	0.4	1.3	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B+}		—	± 2	± 5	—	± 3	± 10	nA
Average Drift of Non-inverting Bias Current	TCI_{B+}		—	10	—	—	12	—	$pA/^\circ C$
Noninverting Offset Current	I_{OS+}		—	2	5	—	3	10	nA
Average Drift of Non-inverting Offset Current	TCI_{OS+}		—	12	—	—	15	—	$pA/^\circ C$
Inverting Offset Current	I_{OS-}		—	2	5	—	3	10	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	100	117	—	94	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	—	16	100	$\mu V/V$

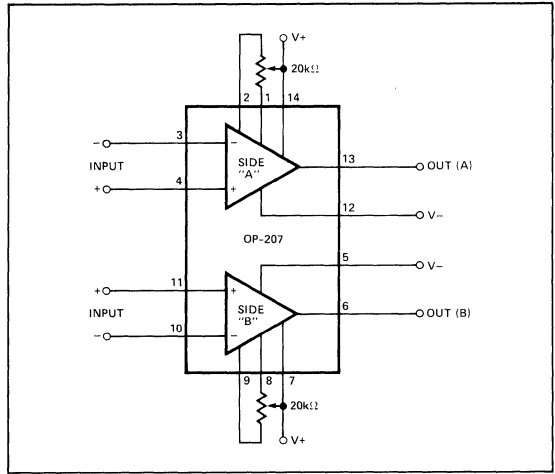
NOTE:

1. Sample tested.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A/E			OP-207B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	35	100	—	60	200	μV
Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)	—	0.3	1.5	—	0.4	2.0	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	0.9	2.8	—	1.5	6.0	nA
Input Bias Current	I_B		—	± 1	± 3	—	± 2	± 7	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 2)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000\text{Hz}$ (Note 2)	—	9.6	—	—	9.6	—	
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	μA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Note 2)	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000\text{Hz}$ (Note 2)	—	0.12	—	—	0.12	—	
Input Resistance — Differential Mode	R_{IN}	(Note 3)	20	60	—	8	30	—	M Ω
Input Resistance — Common-Mode	$R_{IN\text{ CM}}$		—	200	—	—	120	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.5	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 12.0	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.0	± 12.0	—	± 10.0	± 12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.2	—	—	0.2	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No Load, Both Amplifiers	—	180	240	—	200	300	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	± 4	—	—	± 4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$. Parameter is sample tested.
2. Sample tested.
3. Guaranteed by design.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A			OP-207B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	75	230	—	100	400	μV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_P = 20k\Omega$ (Notes 1, 2)	—	0.4	1.3	—	0.7	1.8	$\mu V/^\circ C$
With External Trim	TCV_{OSn}		—	0.4	—	—	0.7	—	
Input Offset Current	I_{OS}		—	1.8	5.6	—	3.0	12.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	—	12	—	$pA/^\circ C$
Input Bias Current	I_B		—	± 3.0	± 5.6	—	± 4.0	± 14.0	nA
Average Input Bias Current Drift	TCI_B		—	12	—	—	18	—	$pA/^\circ C$
Input Voltage Range	IVR		± 13	± 13.5	—	± 13	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	97	117	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	400	—	120	350	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 12.0	± 12.8	—	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	60	200	—	90	350	μV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_P = 20k\Omega$ (Notes 1, 2)	—	0.4	1.3	—	0.7	1.8	$\mu V/^\circ C$
With External Trim	TCV_{OSn}		—	0.4	—	—	0.7	—	
Input Offset Current	I_{OS}		—	1.4	5	—	2.5	10	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	—	12	—	$pA/^\circ C$
Input Bias Current	I_B		—	± 2	± 5	—	± 3	± 11	nA
Average Input Bias Current Drift	TCI_B		—	12	—	—	18	—	$pA/^\circ C$
Input Voltage Range	IVR		± 13	± 13.5	—	± 13	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	97	117	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	400	—	120	350	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 12.0	± 12.8	—	V

NOTES:

- Exclude first hour of operation to allow for stabilization of external circuitry.
- Sample tested.

APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references, and many other demanding applications. These designs all require good matching between two operational amplifiers.

The circuit below, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents,

common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made exceptionally high; this is very important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature. For example, consider the case of two op amps, each with 80dB ($100\mu\text{V/V}$) CMRR. If the CMRR of one device is $+100\mu\text{V/V}$ CMRR and the other is $-100\mu\text{V/V}$, then the net CMRR will be $200\mu\text{V/V}$, a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.

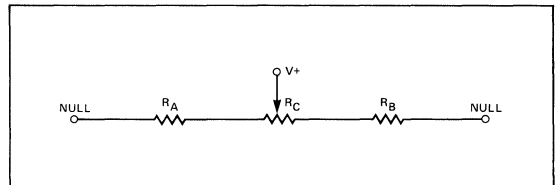
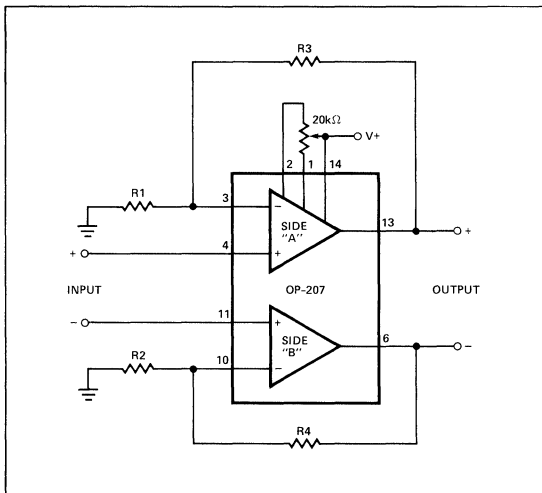
POWER SUPPLIES

The $V+$ supply terminals are completely independent and may be powered by separate supplies if desired. However, this approach would sacrifice the advantages of the power-supply-rejection-ratio matching. The $V-$ supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset voltage trimming is provided for each amplifier. Guaranteed performance over temperature is obtained by trimming one side (side A) to match the offset of the other. A net differential offset of zero results. This procedure is used during factory testing of the devices. The same results are obtained by trimming side B to match side A or by nulling each side individually.

The OP-207 is designed to provide best drift performance when trimmed with a $20\text{k}\Omega$ potentiometer; this value provides about $\pm 4\text{mV}$ of adjustment range which is adequate for most applications. Trimming resolution can be increased by use of the circuit shown below.



Precision Monolithics Inc.

FEATURES

- High Slew Rate 10V/ μ s Min
- Fast Settling Time 0.9 μ s to 0.1% Typ
- Low Input Offset Voltage Drift 10 μ V/ $^{\circ}$ C Max
- Wide Bandwidth 3.5MHz Min
- Temperature-Compensated Input Bias Currents
- Guaranteed Input Bias Current 18nA Max (125 $^{\circ}$ C)
- Bias Current Specified Warm-Up Over Temperature
- Low Input Noise Current 0.01pA/ $\sqrt{\text{Hz}}$ Typ
- High Common-Mode Rejection Ratio 86dB Min
- Pin Compatible With Standard Dual Pinouts
- 125 $^{\circ}$ C Temperature Tested DICE
- Models With MIL-STD-883 Class B Processing Available

ORDERING INFORMATION†

T _A = 25 $^{\circ}$ C V _{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 14-PIN	
1.0	OP215AJ*	OP215AZ*	OP215AY*	MIL
1.0	OP215EJ	OP215EZ	OP215EY	COM
2.0	OP215BJ*	OP215BZ*	OP215BY*	MIL
2.0	OP215FJ	OP215FZ	OP215FY	COM
4.0	OP215CJ*	OP215CZ*	OP215CY*	MIL
6.0	OP215GJ	OP215GZ	OP215GY	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

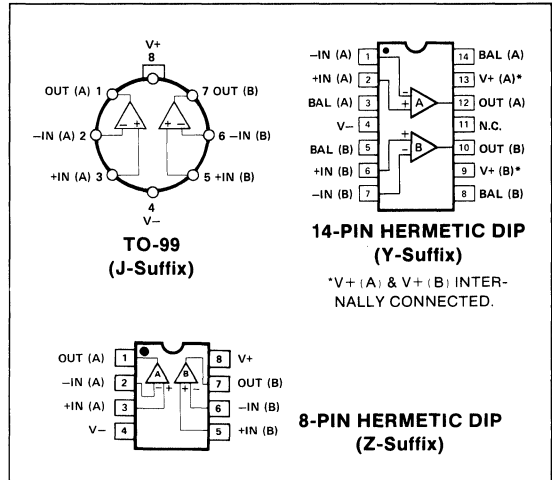
The OP-215 offers the proven JFET-input performance advantages of high speed and low input bias current with the tracking and convenience advantages of a dual op-amp configuration.

Low input offset voltages, low input currents, and low drift are featured in these high-speed amplifiers.

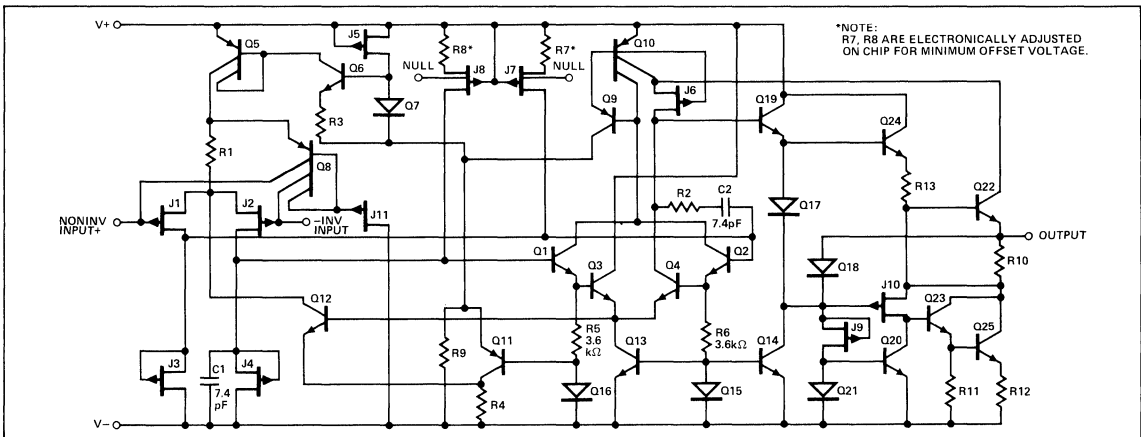
On-chip zener-zap trimming is used to achieve low V_{OS} while a bias-current compensation scheme gives a low input bias current at elevated temperatures. Thus the OP-215 features an input bias current of 18nA at 125 $^{\circ}$ C ambient (not junction) temperature which greatly extends the application usefulness of this device.

Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP-15/16/17 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/2 OP-215)



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage

OP-215A, OP-215B, OP-215E, OP-215F

(All DICE except GR) $\pm 22\text{V}$ OP-215C, OP-215G (GR DICE only) $\pm 18\text{V}$

Internal Power Dissipation (Note 1) 500mW

Operating Temperature Range

OP-215A, OP-215B, OP-215C -55°C to $+125^\circ\text{C}$ OP-215E, OP-215F, OP-215G 0°C to $+70^\circ\text{C}$ Maximum Junction Temperature (T_j) $+150^\circ\text{C}$

Differential Input Voltage

OP-215A, OP-215B, (All DICE except GR) $\pm 40\text{V}$ OP-215E, OP-215F, (All DICE except GR) $\pm 30\text{V}$ OP-215C, OP-215G (GR DICE only) $\pm 30\text{V}$

Input Voltage

OP-215A, OP-215B, (All DICE except GR) $\pm 20\text{V}$ OP-215E, OP-215F, (All DICE except GR) $\pm 20\text{V}$ OP-215C, OP-215G (GR DICE only) $\pm 16\text{V}$

(Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short-Circuit Duration Indefinite

Storage Temperature Range -65°C to $+150^\circ\text{C}$ Lead Temperature (Soldering, 60 sec) 300°C DICE Junction Temperature (T_j) -65°C to $+150^\circ\text{C}$ **NOTES:**

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	$10.0\text{mW}/^\circ\text{C}$
TO-99 (J)	80°C	$7.1\text{mW}/^\circ\text{C}$
8-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^\circ\text{C}$

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215A/E			OP-215B/F			OP-215C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$ 'G' Grade	—	0.2	1.0	—	0.8	2.0	—	2.0	4.0	mV
			—	—	—	—	—	—	—	2.5	6.0	
Input Offset Current	I_{OS}	$T_j = 25^\circ\text{C}$ (Note 1) Device Operating	—	3	50	—	3	50	—	3	100	μA
			—	5	100	—	5	100	—	5	200	
Input Bias Current	I_B	$T_j = 25^\circ\text{C}$ (Note 1) Device Operating	—	± 15	± 100	—	± 15	± 200	—	± 15	± 300	μA
			—	± 18	± 300	—	± 18	± 400	—	± 18	± 600	
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	—	10^{12}	Ω	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10\text{V}$	150	500	—	75	220	—	50	200	—	V/mV
			—	—	—	—	—	—	—	—	—	—
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
			± 11	± 12.7	—	± 11	± 12.7	—	± 11	± 12.7	—	—
Supply Current	I_{SY}	'G' Grade	—	6.0	8.5	—	6.0	8.5	—	7.0	10.0	mA
			—	—	—	—	—	—	—	7.0	12.0	
Slew Rate	SR	$A_{VCL} = +1$	10	18	—	7.5	18	—	5	15	—	V/ μs
Gain Bandwidth Product	GBW	(Note 3)	3.5	5.7	—	3.5	5.7	—	3.0	5.4	—	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	—	13	—	—	13	—	—	12	—	MHz
Settling Time	t_S	to 0.01% to 0.05% (Note 2) to 0.10%	—	2.3	—	—	2.3	—	—	2.4	—	μs
			—	1.1	—	—	1.1	—	—	1.2	—	
			—	0.9	—	—	0.9	—	—	1.0	—	
Input Voltage Range	IVR		+10.2	+14.8	—	+10.2	+14.8	—	+10.1	+14.8	—	V
			-10.2	-11.5	—	-10.2	-11.5	—	-10.1	-11.5	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$ A, B, C Grades E, F, G Grades	86	100	—	86	100	—	82	96	—	dB
			82	100	—	82	100	—	80	96	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10\text{V}$ to $\pm 16\text{V}$ $V_S = \pm 10\text{V}$ to $\pm 15\text{V}$	—	10	51	—	10	80	—	—	—	$\mu\text{V}/\text{V}$
			—	—	—	—	—	—	—	16	100	
Input Noise Voltage Density	e_n	$f_O = 100\text{Hz}$ $f_O = 1000\text{Hz}$	—	20	—	—	20	—	—	20	—	$\text{nV}/\sqrt{\text{Hz}}$
			—	15	—	—	15	—	—	15	—	
Input Noise Current Density	i_n	$f_O = 100\text{Hz}$ $f_O = 1000\text{Hz}$	—	0.01	—	—	0.01	—	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
			—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}		—	3	—	—	3	—	—	3	—	pF

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215A			OP-215B			OP-215C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.5	2.0	—	1.5	3.0	—	3.0	6.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	10	—	3	10	—	6	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = +125^\circ C$ $T_A = +125^\circ C$, Device Operating	—	0.8	8	—	0.8	8	—	1.0	12	nA
Input Bias Current (Note 1)	I_B	$T_J = +125^\circ C$ $T_A = +125^\circ C$, Device Operating	—	± 1.5	± 10	—	± 1.5	± 10	—	± 1.8	± 15	nA
Input Voltage Range	IVR		+10.2	+14.6	—	+10.2	+14.6	—	+10.1	+14.6	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	97	—	82	97	—	80	93	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$ $V_S = \pm 10V$ to $\pm 15V$	—	10	100	—	15	100	—	—	—	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	110	—	30	110	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

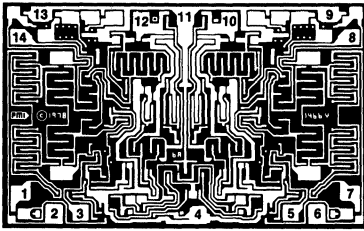
PARAMETER	SYMBOL	CONDITIONS	OP-215E			OP-215F			OP-215G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.4	1.65	—	1.4	2.65	—	3.5	8.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	15	—	3	15	—	6	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = +70^\circ C$ $T_A = +70^\circ C$, Device Operating	—	0.06	0.45	—	0.06	0.45	—	0.08	0.65	nA
Input Bias Current (Note 1)	I_B	$T_J = +70^\circ C$ $T_A = +70^\circ C$, Device Operating	—	± 0.12	± 0.70	—	± 0.12	± 0.70	—	± 0.14	± 0.9	nA
Input Voltage Range	IVR		+10.2	+14.7	—	+10.2	+14.7	—	+10.1	+14.7	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	80	98	—	80	98	—	76	94	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$ $V_S = \pm 10V$ to $\pm 15V$	—	13	100	—	13	100	—	—	—	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	180	—	50	180	—	35	130	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

NOTES:

- Input bias current is specified for two different conditions. The $T_J = 25^\circ C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at $25^\circ C$ ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs. T_J and I_B vs. T_A . PMI has a bias current compensation circuit which gives improved bias current and bias current over temperature vs. standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Settling time is defined here for a unity gain inverter connection using $2k\Omega$ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a $10V$ step input is applied to the inverter. See settling time test circuit.
- Sample tested.



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



- | | |
|---------------------------|------------------------|
| 1. INVERTING INPUT (A) | 8. NULL (B) |
| 2. NONINVERTING INPUT (A) | 9. V+ |
| 3. NULL (A) | 10. V _O (B) |
| 4. V- | 11. V+ |
| 5. NULL (B) | 12. V _O (A) |
| 6. NONINVERTING INPUT (B) | 13. V+ |
| 7. INVERTING INPUT (B) | 14. NULL (A) |

ALL V+ PADS ARE INTERNALLY CONNECTED.

DIE SIZE 0.059 × 0.093 inch, 5487 sq. mils (1.50 × 2.36 mm, 3.54 sq. mm)

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-215N, OP-215G and OP-215GR devices; $T_A = 125^\circ C$ for OP-215NT and OP-215GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215NT LIMIT	OP-215N LIMIT	OP-215GT LIMIT	OP-215G LIMIT	OP-215GR LIMIT	UNITS	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	2	1	3	2	6	mV MAX	
Input Bias Current	I_B		±18	—	±18	—	—	nA MAX	
Input Offset Current	I_{OS}		14	—	14	—	—	nA MAX	
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 2k\Omega$	30	150	30	75	50	V/mV MIN	
Input Voltage Range	IVR		±10.2	±10.2	±10.2	±10.2	±10.1	V MIN	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	86	82	86	82	dB MIN	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10$ to $\pm 16V$ $V_S = \pm 10$ to $\pm 15V$	100	51	100	80	—	— 100	— $\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12	±12	±12	±12	±12	— ±11	— V MIN
Supply Current	I_{SV}		—	8.5	—	8.5	12.0	—	— mA MAX

NOTES:

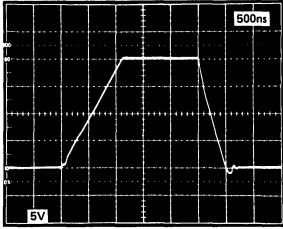
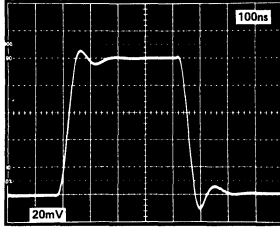
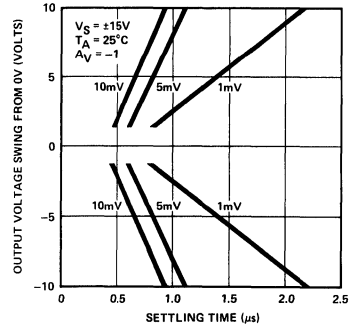
For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

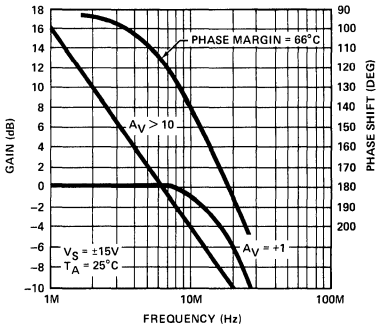
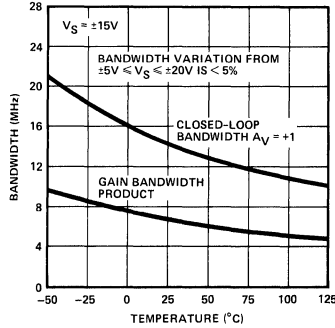
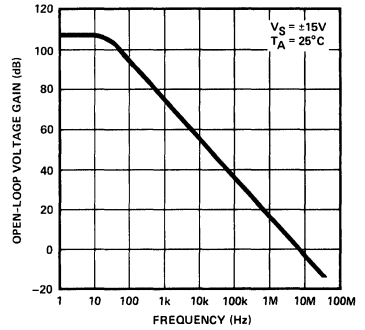
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215NT TYPICAL	OP-215N TYPICAL	OP-215GT TYPICAL	OP-215G TYPICAL	OP-215GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled $R_P = 100k\Omega$	2	2	3	3	4	$\mu V/^\circ C$
Average Input Offset Voltage Drift	TCV_{OSn}	Nulled $R_P = 100k\Omega$	0.5	0.5	1	1	2	$\mu V/^\circ C$
Input Offset Current	I_{OS}		3	3	3	3	3	pA
Input Bias Current	I_B		±15	±15	±15	±15	±15	pA
Slew Rate	SR	$A_{VCL} = +1$	17	17	16	16	15	V/ μs
Settling Time	t_S	to 0.01%	2.2	2.2	2.3	2.3	2.4	μs
		to 0.05%	1.1	1.1	1.1	1.1	1.2	
		to 0.10%	0.9	0.9	0.9	0.9	1.0	
Gain Bandwidth Product	GBW		6.0	6.0	5.7	5.7	5.4	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	14	14	13	13	12	MHz
Input Noise Voltage Density	e_n	$f_O = 100Hz$	20	20	20	20	20	nV/\sqrt{Hz}
		$f_O = 1000Hz$	15	15	15	15	15	
Input Noise Current Density	i_n	$f_O = 100Hz$	0.01	0.01	0.01	0.01	0.01	pA/\sqrt{Hz}
		$f_O = 1000Hz$	0.01	0.01	0.01	0.01	0.01	
Input Capacitance	C_{IN}		3	3	3	3	3	pF

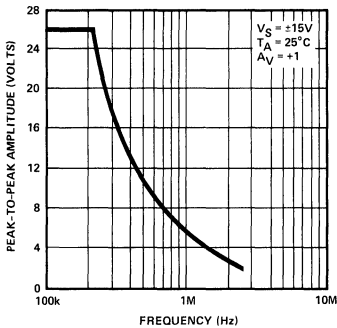
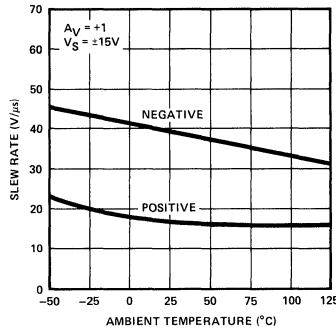
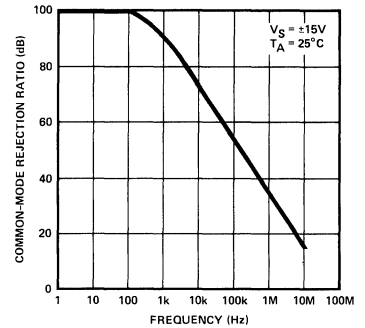
TYPICAL PERFORMANCE CHARACTERISTICS

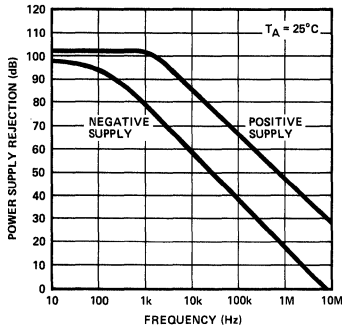
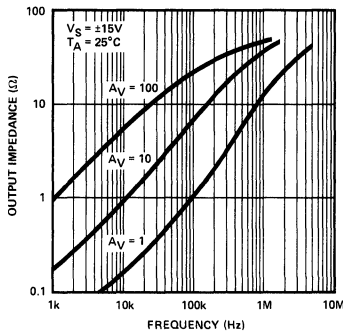
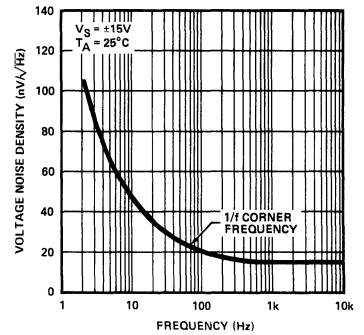
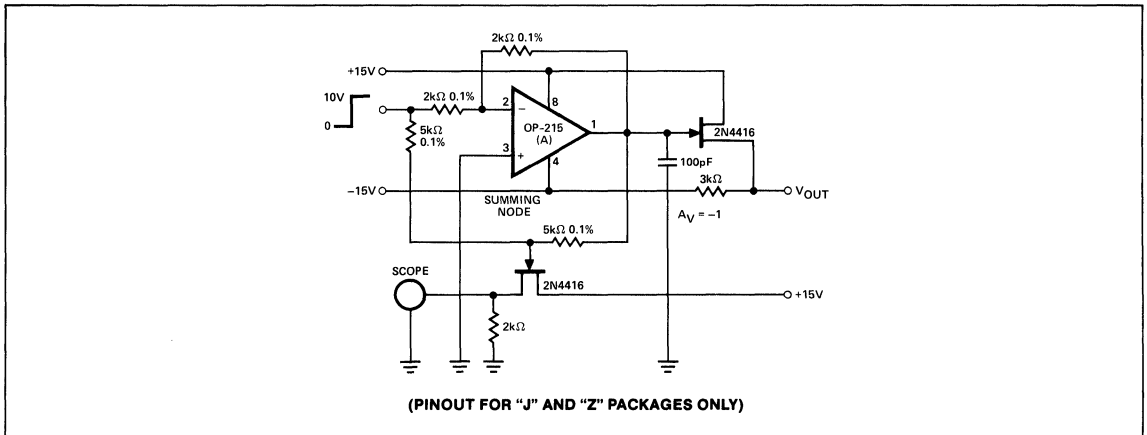
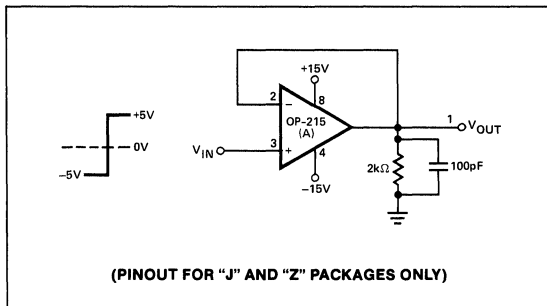
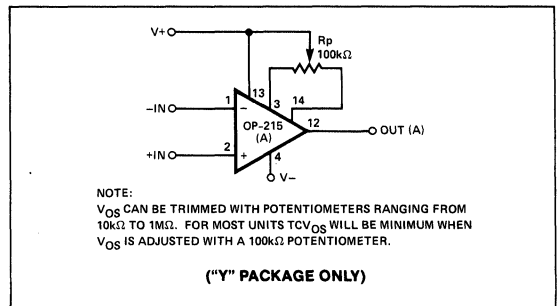
**LARGE-SIGNAL
TRANSIENT RESPONSE**

**SMALL-SIGNAL
TRANSIENT RESPONSE**

SETTLING TIME


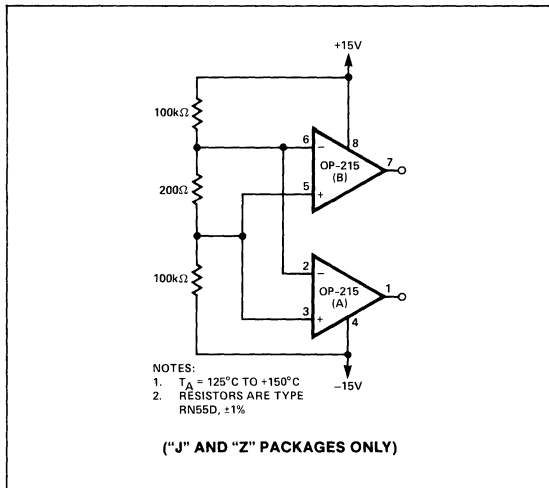
5

**CLOSED-LOOP
BANDWIDTH AND
PHASE SHIFT vs FREQUENCY**

BANDWIDTH vs TEMPERATURE

**OPEN-LOOP
FREQUENCY RESPONSE**


OPERATIONAL AMPLIFIERS

**MAXIMUM OUTPUT SWING
vs FREQUENCY**

SLEW RATE vs TEMPERATURE

**COMMON-MODE REJECTION
RATIO vs FREQUENCY**


TYPICAL PERFORMANCE CHARACTERISTICS
POWER SUPPLY REJECTION vs FREQUENCY

OUTPUT IMPEDANCE vs FREQUENCY

VOLTAGE NOISE DENSITY vs FREQUENCY

BASIC CONNECTIONS
SETTLING TIME TEST CIRCUIT

SLEW RATE TEST CIRCUIT

INPUT OFFSET VOLTAGE NULLING


BASIC CONNECTIONS
TYPICAL BURN-IN CIRCUIT

APPLICATIONS INFORMATION
DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback-pole time constant.

5
 OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

FEATURES

- Excellent TCV_{OS} Match $2\mu V/^{\circ}C$ Max
- Low Input Offset Voltage $150\mu V$ Max
- Low Supply Current $100\mu A$
- Single-Supply Operation $+5V$ to $+30V$
- Low Input Offset Voltage Drift $0.75\mu V/^{\circ}C$
- High Open-Loop Gain $2000V/mV$
- High PSRR $3\mu V/V$
- Low Input Bias Current $12nA$
- Wide Common-Mode Voltage Range $V-$ to within $1.5V$ of $V+$
- Pin Compatible with 1458, LM158, LM2904

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	
150	OP220AJ*	OP220AZ*	MIL
150	OP220EJ	OP220EZ	IND
300	OP220BJ*	OP220BZ*	MIL
300	OP220FJ	OP220FZ	IND
750	OP220CJ*	OP220CZ*	MIL
750	OP220GJ	OP220GZ	IND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

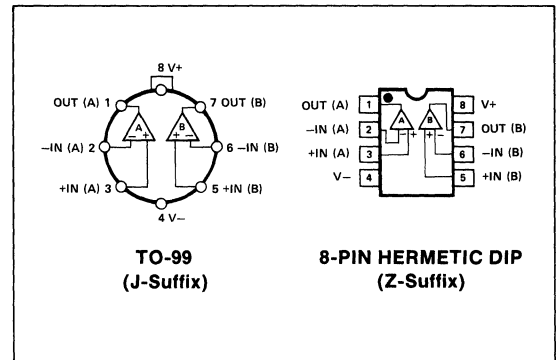
The OP-220 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The low

offset voltage, and input offset voltage tracking as low as $1.0\mu V/^{\circ}C$, make this the first micropower precision dual operational amplifier.

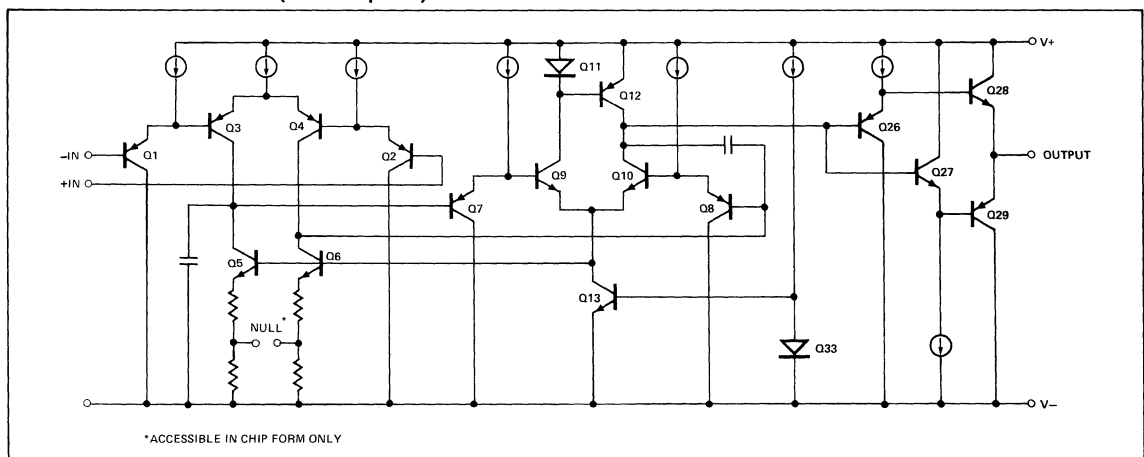
The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provides high performance in instrumentation amplifier designs. The individual amplifiers feature extremely low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection ratios.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (Each Amplifier)



*ACCESSIBLE IN CHIP FORM ONLY

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	±18V
Power Dissipation	500mW
Differential Input Voltage	30V or Supply Voltage
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-220A, B, C	-55°C to +125°C
OP-220E, F, G	-25°C to +85°C

Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_j)	-65°C to +150°C

NOTE:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	120	150	—	250	300	—	500	750	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.15	1.5	—	0.2	2	—	0.2	3.5	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	20	—	13	25	—	14	30	nA
Input Voltage Range	IVR	$V^+ = 5V, V^- = 0V,$ $V_S = \pm 15V$	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V^+ = 5V, V^- = 0V,$ $0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V,$ $-15V \leq V_{CM} \leq 13.5V$	90	100	—	85	90	—	75	85	—	dB
Common-Mode Rejection Ratio	CMRR	$V^+ = 5V, V^- = 0V,$ $0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V,$ $-15V \leq V_{CM} \leq 13.5V$	90	100	—	85	90	—	75	85	—	dB
		$V^+ = 5V, V^- = 0V,$ $0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V,$ $-15V \leq V_{CM} \leq 13.5V$	95	100	—	90	95	—	80	90	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	3	10	—	10	32	—	32	100	$\mu V/V$
		$V^- = 0V, V^+ = 5V$ to 30V	—	6	18	—	18	57	—	57	180	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V^+ = 5V, V^- = 0V, R_L = 100k\Omega$ $1V \leq V_O \leq 3.5V$ $V_S = \pm 15V, R_L = 25k\Omega$ $V_O = \pm 10V$	500	1000	—	500	800	—	300	500	—	V/mV
		$V^+ = 5V, V^- = 0V,$ $R_L = 10k\Omega$ $V_S = \pm 15V, R_L = 25k\Omega$ $V_O = \pm 10V$	1000	2000	—	1000	2000	—	800	1600	—	V/mV
Output Voltage Swing	V_O	$V^+ = 5V, V^- = 0V,$ $R_L = 10k\Omega$ $V_S = \pm 15V, R_L = 25k\Omega$	0.7/4	—	—	0.7/4	—	—	0.8/4	—	—	V
Slew Rate	SR	$R_L = 25k\Omega,$ (Note 1)	—	0.05	—	—	0.05	—	—	0.05	—	V/ μs
Bandwidth	BW	$A_{VCL} = +1, R_L = 25k\Omega$	—	200	—	—	200	—	—	200	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V,$ No Load	—	100	115	—	115	125	—	125	135	μA
		$V_S = \pm 15V,$ No Load	—	140	170	—	150	190	—	205	220	μA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-220A, B, and C, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-220E, F, and G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$V_S = \pm 15V$	—	0.75	1.5	—	1.2	2	—	2	3	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	200	300	—	400	500	—	1000	1300	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	2	—	0.6	2.5	—	0.8	5	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	25	—	13	30	—	14	40	nA
Input Voltage Range	IVR	$V^+ = 5V, V^- = 0V,$ $V_S = \pm 15V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V^+ = 5V, V^- = 0V,$ $0V \leq V_{CM} \leq 3.2V$ $V_S = \pm 15V$ $-15V \leq V_{CM} \leq 13.2V$	85	90	—	80	85	—	70	80	—	dB
Common-Mode Rejection Ratio	CMRR	$V^+ = 5V, V^- = 0V,$ $0V \leq V_{CM} \leq 3.2V$ $V_S = \pm 15V$ $-15V \leq V_{CM} \leq 13.2V$	85	90	—	80	85	—	70	80	—	dB
		$V^+ = 5V, V^- = 0V,$ $0V \leq V_{CM} \leq 3.2V$ $V_S = \pm 15V$ $-15V \leq V_{CM} \leq 13.2V$	90	95	—	85	90	—	75	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	6	18	—	18	57	—	57	180	$\mu V/V$
		$V^- = 0V, V^+ = 5V$ to 30V	—	10	32	—	32	100	—	100	320	$\mu V/V$



ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-220A, B, and C, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-220 E, F, and G, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 50k\Omega$ $V_O = \pm 10V$	500	1000	—	500	800	—	400	500	—	V/mV
Output Voltage Swing	V_O	$V_+ = 5V$, $V_- = 0V$, $R_L = 20k\Omega$ $V_S = \pm 15V$, $R_L = 50k\Omega$	0.9/3.8	—	—	0.9/3.8	—	—	1/3.8	—	—	V
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	—	135	170	—	155	185	—	170	210	μA

NOTE: 1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	150	300	—	250	500	—	300	600	μV
Average Noninverting Bias Current	I_{B^+}	$V_{CM} = 0$	—	10	20	—	15	25	—	20	30	nA
Noninverting Offset Current	I_{OS^+}	$V_{CM} = 0$	—	0.7	1.5	—	1	2	—	1.4	2.5	nA
Common-Mode Rejection Ratio Match (Note 1)	$\Delta CMRR$	$V_{CM} = -15V$ to $+13.5V$	92	100	—	87	95	—	72	85	—	dB
Power Supply Rejection Ratio Match (Note 2)	$\Delta PSRR$	$V_S = \pm 2.5V$ to $\pm 15V$	—	6	14	—	18	44	—	57	140	$\mu V/V$

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-220A, B and C; $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-220 E, F and G, unless otherwise noted. Grades E, F, and G are sample tested.

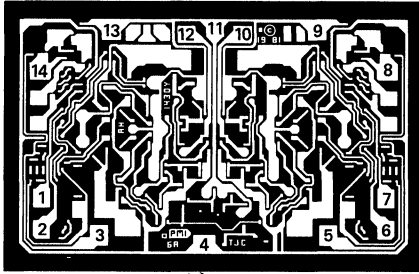
PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	250	500	—	400	800	—	800	1800	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	(Note 3)	—	1	2	—	1.5	3	—	1.5	5	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B^+}	$V_{CM} = 0$	—	10	25	—	15	30	—	22	40	nA
Average Drift of Noninverting Bias Current	TCI_{B^+}	$V_{CM} = 0$ (Note 3)	—	15	25	—	15	30	—	30	50	$pA/^\circ C$
Noninverting Offset Current	I_{OS^+}	$V_{CM} = 0$	—	0.7	2	—	1	2.5	—	2.5	5	nA
Average Drift of Noninverting Offset Current	TCI_{OS^+}	$V_{CM} = 0$ (Note 3)	—	7	15	—	12	22.5	—	15	30	$pA/^\circ C$
Common-Mode Rejection Ratio Match (Note 1)	$\Delta CMRR$	$V_{CM} = -15V$ to $+13V$	87	98	—	82	96	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	$\Delta PSRR$	$V_S = \pm 2.5V$ to $\pm 15V$	—	10	26	—	30	78	—	57	250	$\mu V/V$

NOTES:

- $\Delta CMRR$ is $20 \log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
- $\Delta PSRR$ is: $\frac{\text{Input-referred differential error}}{\Delta V_S}$
- Sample tested.



DICE CHARACTERISTICS



DIE SIZE 0.096 × 0.061 inch, 5856 sq. mils
(2.438 × 1.549 mm, 3.78 sq. mm)

NOTE: All V+ PADS ARE INTERNALLY CONNECTED.

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V-
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUT (B)
11. V+
12. OUT (A)
13. V+
14. BALANCE (A)

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25^\circ C$ for OP-220N, OP-220G and OP-220GR devices; $T_A = 125^\circ C$ for OP-221NT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220NT LIMIT	OP-220N LIMIT	OP-220G LIMIT	OP-220GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		350	200	500	1000	μV MAX
Input Offset Voltage Match	ΔV_{OS}		500	300	500	600	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	2.5	2	3.5	5	nA MAX
Input Bias Current	I_B	$V_{CM} = 0$	30	25	30	40	nA MAX
Input Voltage Range	IVR	$V_S = \pm 15V$	-15/13.5	-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V^- = 0V, V^+ = 5V, 0V \leq V_{CM} \leq 3.5V$	83	88	83	75	dB MIN
		$-15V \leq V_{CM} \leq 13.5V, V_S = \pm 15V$	88	93	88	80	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	22	12.5	40	100	$\mu V/V$ MAX
		$V^- = 0V, V^+ = 5V$ to 30V	36	22.5	70	180	
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega, V_S = \pm 15V$ $V_O = \pm 10V$	—	1000	800	500	V/mV MIN
		$V_S = \pm 15V, R_L = 50k\Omega$ $V_O = \pm 10V$	500	—	—	—	
Output Voltage Swing	V_O	$V^+ = 5V, V^- = 0V, R_L = 10k\Omega$ $V_S = \pm 15V, R_L = 25k\Omega$	—	0.7/4	0.8/4	0.8/3.8	V MIN
		$V^+ = 5V, V^- = 0V,$ $R_L = 20k\Omega$	0.9/3.8	—	—	—	
		$V_S = \pm 15V, R_L = 50k\Omega$	± 13.8	—	—	—	
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	170	125	135	170	μA MAX
		$V_S = \pm 15V$, No Load	250	190	220	300	

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

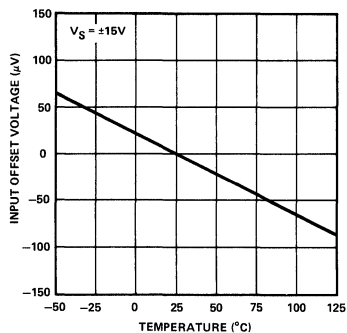
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220NT TYPICAL	OP-220N TYPICAL	OP-220G TYPICAL	OP-220GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		1.5	1.5	2	3	$\mu V/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	2000	1600	800	V/mV

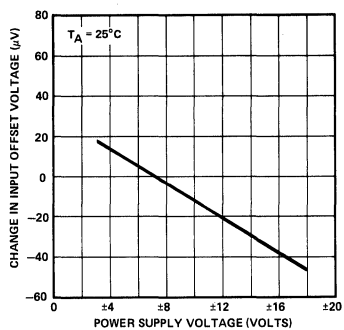


TYPICAL PERFORMANCE CHARACTERISTICS

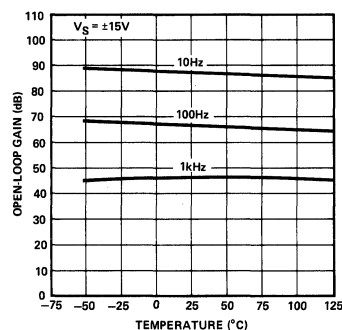
NORMALIZED OFFSET VOLTAGE vs TEMPERATURE



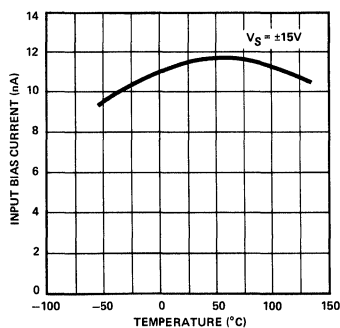
INPUT OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE



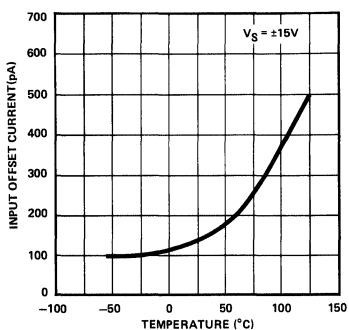
OPEN-LOOP GAIN vs TEMPERATURE



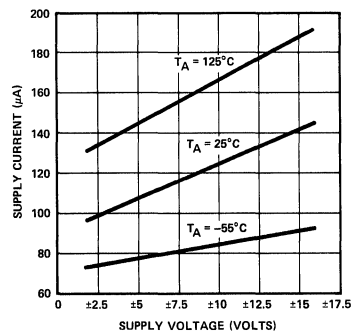
INPUT BIAS CURRENT vs TEMPERATURE



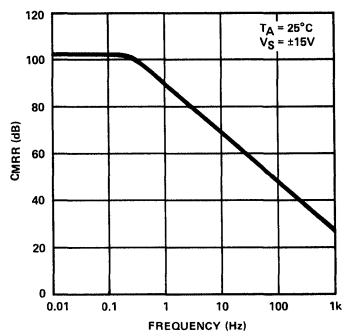
INPUT OFFSET CURRENT vs TEMPERATURE



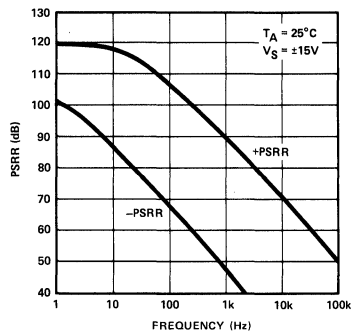
SUPPLY CURRENT vs SUPPLY VOLTAGE



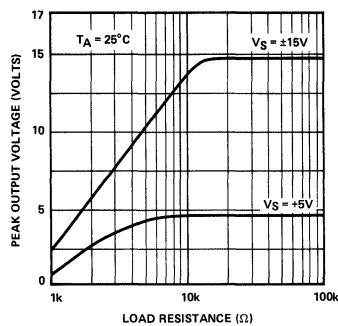
CMRR vs FREQUENCY



PSRR vs FREQUENCY

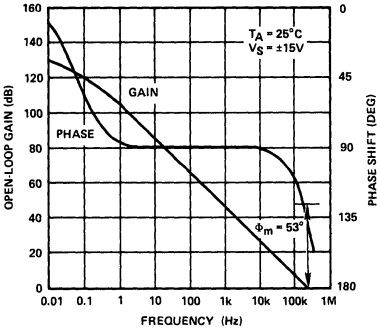


MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

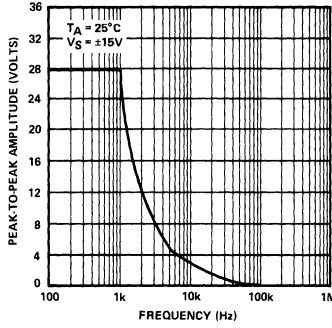


TYPICAL PERFORMANCE CHARACTERISTICS

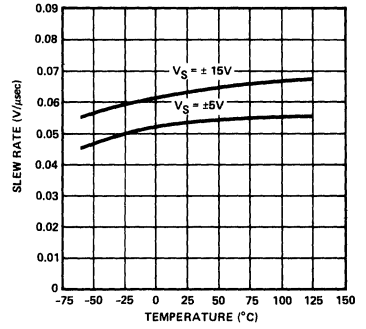
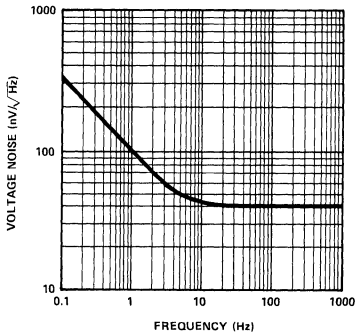
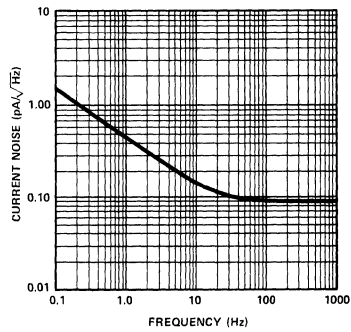
OPEN-LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY



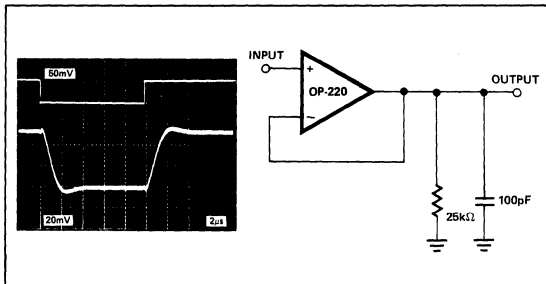
MAXIMUM OUTPUT SWING vs FREQUENCY



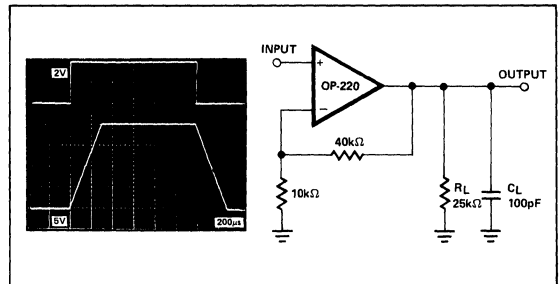
SLEW RATE vs TEMPERATURE


 VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY

 CURRENT NOISE DENSITY (i_n) vs FREQUENCY


SMALL-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE



INSTRUMENTATION AMPLIFIER APPLICATIONS OF THE OP-220

TWO-OP-AMP CONFIGURATION

The excellent input characteristics of the OP-220 make it ideal for use in *instrumentation amplifier* configurations where low-level differential signals are to be amplified. The low-noise, low input offsets, low drift, and high gain combined with excellent CMRR provide the characteristics needed for high-performance instrumentation amplifiers. In addition, the power supply current drain is very low.

The circuit of Figure 1 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two-op-amp instrumentation amplifier features *independent* adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to noninverting op amp inputs.

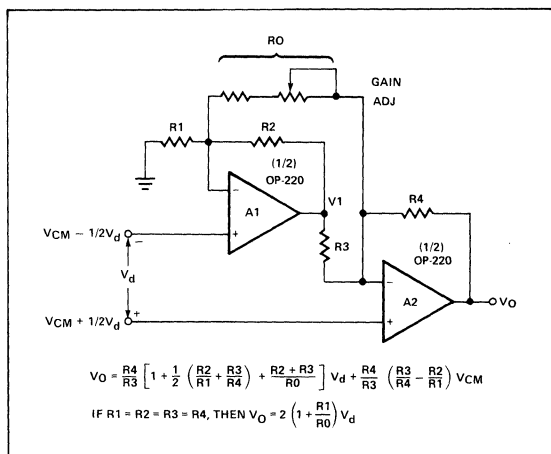


Figure 1. Two-Op-Amp Instrumentation Amplifier Configuration

The input voltages are represented as a common-mode input V_{CM} plus a differential input V_d . The ratio R_3/R_4 is made equal to the ratio R_2/R_1 to reject the common-mode input V_{CM} . The differential signal V_d is then amplified according to:

$$V_O = \frac{R_4}{R_3} \left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_O} \right) V_d, \text{ where } \frac{R_3}{R_4} = \frac{R_2}{R_1}$$

Note that gain can be independently varied by adjusting R_O . From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R_1 , R_2 , R_3 , and R_4 approximately equal. Designating R_1 , R_2 , R_3 , and R_4 as R_N allows the output equation to be further simplified:

$$V_O = 2 \left(1 + \frac{R_N}{R_O} \right) V_d, \text{ where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2; the output of A1 is:

$$V_1 = - \left(1 + \frac{R_N}{R_O} \right) V_d + 2 V_{CM}$$

If the instrumentation amplifier were designed for a gain of 10 and maximum V_d of $\pm 1V$, then R_N/R_O would need to be four and V_O would be a maximum of $\pm 10V$. Amplifier A1 would have a maximum output of $\pm 5V$ plus $2V_{CM}$, thus a limit of $\pm 10V$ on the output of A1 would imply a limit of $\pm 2.5V$ on V_{CM} .

A nominal value of $100k\Omega$ for R_N is suitable for most applications. A range of 200Ω to $25k\Omega$ for R_O will then provide a gain range of 10 to 1000. The current through R_O is V_d/R_O , so the amplifiers must supply $\pm 10mV/200\Omega$ when the gain is at the maximum value of 1000 and V_d is at $\pm 10mV$.

Rejecting common-mode inputs is most important in accurately amplifying low-level differential signals. Two factors determine the CMR of this instrumentation amplifier configuration (assuming infinite gain):

- (1) CMRR of the op amps
- (2) Matching of the resistor network ($R_3/R_4 = R_2/R_1$)

In this instrumentation amplifier configuration, error due to CMRR effect is directly proportional to the *differential* CMRR of the op amps. For the OP-220A/E, this combined CMRR is a minimum of 98dB. A combined CMRR value of 100dB and common-mode input range of $\pm 2.5V$ indicates a peak input-referred error of only $\pm 25\mu V$.

Resistor matching is the other factor affecting CMRR. Defining A_d as the differential gain of the instrumentation amplifier and assuming that R_1 , R_2 , R_3 and R_4 are approximately equal (R_N will be the nominal value), then CMRR will be approximately A_d divided by $4\Delta R/R_N$. CMRR at differential gain of 100 would be 88dB with resistor matching of 0.1%. Trimming R_1 to make the ratio R_3/R_4 equal to R_2/R_1 will directly raise the CMRR until it is limited by linearity and resistor stability considerations.

The high open-loop gain of the OP-220 is very important in achieving high accuracy in the two-op-amp instrumentation amplifier configuration. Gain error can be approximated by:

$$\text{Gain Error} \sim \frac{1}{1 + \frac{A_d}{A_{O2}}} \cdot \frac{A_d}{2 A_{O1} A_{O2}} \ll 1$$

where A_d is the instrumentation amplifier differential gain and A_{O2} is the open-loop gain of op amp A2. This analysis assumes equal values of R_1 , R_2 , R_3 , and R_4 . For example, consider an OP-220 with A_{O2} of 700V/mV. If the differential gain A_d were set to 700, the gain error would be 1/1.001 which is approximately 0.1%.

Another effect of finite op amp gain is undesired feedthrough of common-mode input. Defining A_{O1} as the open-loop gain of op amp A1, then the common-mode error (CME) at the output due to this effect will be approximately

$$\text{CME} \sim \frac{2 A_d}{1 + \frac{A_d}{A_{O1}}} \cdot \frac{1}{A_{O1}} V_{CM}$$

For $A_d/A_{01} \ll 1$, this simplifies to $(2 A_d/A_{01}) \times V_{CM}$. If the op amp gain is 700V/mV, V_{CM} is 2.5V, and A_d is set to 700, then the error at the output due to this effect will be approximately 5mV.

The OP-220 offers a unique combination of excellent dc performance, wide input range, and low supply current drain that is particularly attractive for instrumentation amplifier design.

THREE-OP-AMP CONFIGURATION

A three-op-amp instrumentation amplifier configuration using the OP-220 and OP-22 is recommended for applications requiring high accuracy over a wide gain range. This

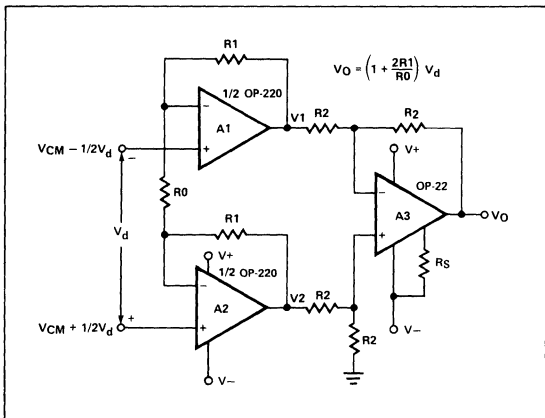


Figure 2. Three-Op-Amp Instrumentation Amplifier Using OP-220 and OP-22

circuit provides excellent CMR over a wide input range. As with the two-op-amp instrumentation amplifier circuits, tight matching of the two op amps provides a real boost in performance. The OP-22 is a micropower op-amp featuring programmable supply current.

A simplified schematic is shown in Figure 2. The input stage (A1 and A2) serves to amplify the differential input V_d without amplifying the common-mode voltage V_{CM} . The output stage then rejects the common-mode input. With ideal op-amps and no resistor matching errors, the outputs of each amplifier will be:

$$V_1 = -\left(1 + \frac{2R_1}{R_O}\right) \frac{V_d}{2} + V_{CM}$$

$$V_2 = \left(1 + \frac{2R_1}{R_O}\right) \frac{V_d}{2} + V_{CM}$$

$$V_O = V_2 - V_1 = \left(1 + \frac{2R_1}{R_O}\right) V_d$$

$$V_O = A_d V_d$$

The differential gain A_d is $1 + 2R_1/R_O$ and the common-mode input V_{CM} is rejected.

This three-op-amp instrumentation amplifier configuration using an OP-220 at the input and an OP-22 at the output provides excellent performance over a wide gain range with very low power consumption. A gain range of 1 to 2000 is practical and CMR of over 120dB is readily achievable.

Precision Monolithics Inc.

FEATURES

- Excellent TCV_{OS} Match $2\mu V/^{\circ}C$ Max
- Low Input Offset Voltage $150\mu V$ Max
- Low Supply Current $550\mu A$ Max
- Single Supply Operation $+5V$ to $+30V$
- Low Input Offset Voltage Drift $0.75\mu V/^{\circ}C$
- High Open-Loop Gain $1500V/mV$ Min
- High PSRR $3\mu V/V$
- Wide Common-Mode Voltage Range $V-$ to within $1.5V$ of $V+$
- Pin Compatible with 1458, LM158, LM2904

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	
150	OP221AJ*	OP221AZ*	MIL
150	OP221EJ	OP221EZ	IND
300	OP221BJ*	OP221BZ*	MIL
300	OP221FJ	OP221FZ	IND
500	OP221CJ*	OP221CZ*	MIL
500	OP221GJ	OP221GZ	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

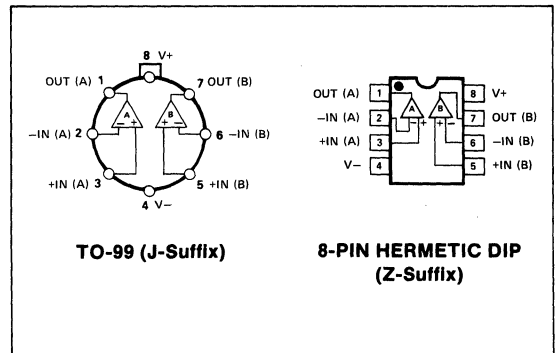
† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

wide supply voltage range, wide input voltage range, and low supply current drain of the OP-221 make it well-suited for operation from batteries or unregulated power supplies.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection.

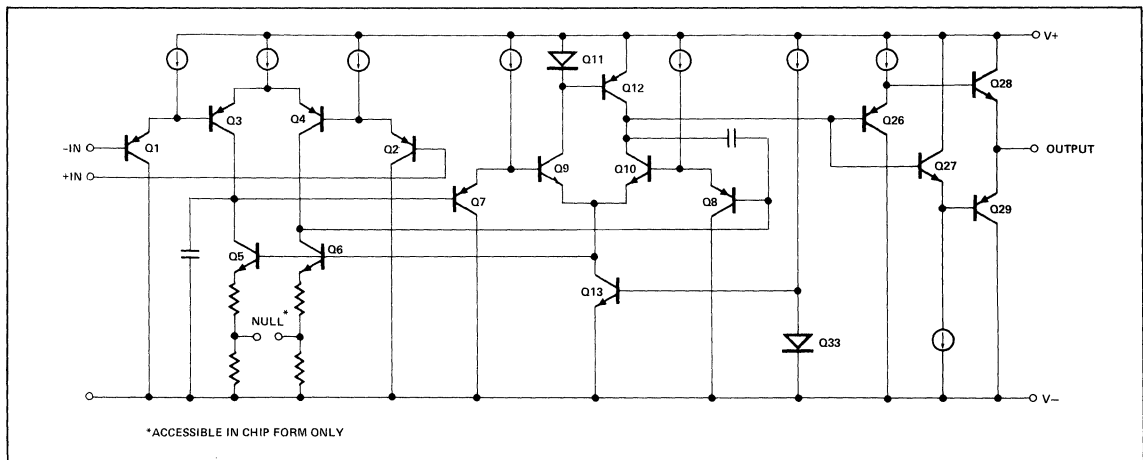
PIN CONNECTIONS



GENERAL DESCRIPTION

The OP-221 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The

SIMPLIFIED SCHEMATIC (Each Amplifier)





ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	30V or Supply Voltage
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-221A, B, C	-55°C to +125°C
OP-221E, F, G	-25°C to +85°C

Lead Temperature (Soldering, 60 sec.)	300°C
DICE Junction Temperature (T_j)	-65°C to +150°C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B/F			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	75	150	—	150	300	—	250	500	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	3	—	1	5	—	1.5	7	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	50	80	—	60	100	—	70	120	nA
Input Voltage Range	IVR	$V_+ = 5V, V_- = 0V$ $V_S = \pm 15V$	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_+ = 5V, V_- = 0V$ $0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V$	90	100	—	85	90	—	75	85	—	dB
		$-15V \leq V_{CM} \leq 13.5V$	95	100	—	90	95	—	80	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	3	10	—	10	32	—	32	100	$\mu V/V$
		$V_- = 0V, V_+ = 5V$ to 30V	—	6	18	—	18	57	—	57	180	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, R_L = 10k\Omega$ $V_O = \pm 10V$	1500	—	—	1000	—	—	800	—	—	V/mV
Output Voltage Swing	V_O	$V_+ = 5V, V_- = 0V,$ $R_L = 10k\Omega$	0.7/4.1	—	—	0.7/4.1	—	—	0.8/4	—	—	V
		$V_S = \pm 15V, R_L = 10k\Omega$	± 13.8	—	—	± 13.8	—	—	± 13.5	—	—	
Slew Rate	SR	$R_L = 10k\Omega, (Note 1)$	0.2	0.3	—	0.2	0.3	—	0.2	0.3	—	V/ μs
Bandwidth	BW		—	600	—	—	600	—	—	600	—	kHz
Supply Current (Both Amplifiers)	I_{SV}	$V_S = \pm 2.5V, No Load$	—	450	550	—	500	600	—	550	650	μA
		$V_S = \pm 15V, No Load$	—	600	800	—	800	850	—	850	900	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V, -55^\circ C \leq T_A \leq +125^\circ C$ for OP-221A, B and C; $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-221E, F and G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B/F			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	0.75	1.5	—	1.2	2	—	2	3	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	150	300	—	250	450	—	400	700	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	1	5	—	1.5	7	—	2	10	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	55	100	—	65	120	—	80	140	nA
Input Voltage Range	IVR	$V_+ = 5V, V_- = 0V$ $V_S = \pm 15V$	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_+ = 5V, V_- = 0V$ $0V \leq V_{CM} \leq 3.2V$ $V_S = \pm 15V$	85	90	—	80	85	—	70	80	—	dB
		$-15V \leq V_{CM} \leq 13.2V$	90	95	—	85	90	—	75	85	—	

5
OPERATIONAL AMPLIFIERS



ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-221A, B and C; $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-221E, F and G, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B/F			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V^- = 0V$, $V^+ = 5V$ to $30V$	—	6	18	—	18	57	—	57	180	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_O = \pm 10V$	1000	—	—	800	—	—	600	—	—	V/mV
Output Voltage Swing	V_O	$V^+ = 5V$, $V^- = 0V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.8/3.8	—	—	0.8/3.8	—	—	0.9/3.7	—	—	V
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	—	500	650	—	550	700	—	600	750	μA
			—	700	900	—	900	950	—	950	1000	

NOTE:

1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B/F			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	50	200	—	150	400	—	250	600	μV
Average Noninverting Bias Current	I_{B^+}		—	—	80	—	—	100	—	—	120	nA
Noninverting Input Offset Current	I_{OS^+}		—	2	5	—	2	5	—	4	10	nA
Common-Mode Rejection Ratio Match (Note 1)	$\Delta CMRR$	$V_{CM} = -15V$ to $+13.5V$	92	—	—	87	—	—	72	—	—	dB
Power Supply Rejection Ratio Match (Note 2)	$\Delta PSRR$	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	14	—	—	44	—	—	140	$\mu V/V$

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-221A, B and C; $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-221E, F and G, unless otherwise noted. Grades E, F, and G are sample tested.

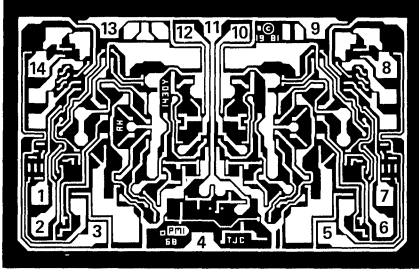
PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B/F			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	100	400	—	250	600	—	400	800	μV
Average Noninverting Bias Current	I_{B^+}	$V_{CM} = 0$	—	—	100	—	—	120	—	—	140	nA
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	(Note 3)	—	1	2	—	1	3	—	3	5	$\mu V/^\circ C$
Noninverting Input Offset Current	I_{OS^+}	$V_{CM} = 0$	—	3	7	—	3	7	—	6	12	nA
Common-Mode Rejection Ratio Match (Note 1)	$\Delta CMRR$	$V_{CM} = -15V$ to $+13.2V$	87	90	—	82	85	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	$\Delta PSRR$		—	—	26	—	—	78	—	—	250	$\mu V/V$

NOTE:

1. $\Delta CMRR$ is $20 \log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
2. $\Delta PSRR$ is:
$$\frac{\text{Input-Referred Differential Error}}{\Delta V_S}$$
3. Sample tested.



DICE CHARACTERISTICS



DIE SIZE 0.096 × 0.061 Inch, 5856 sq. mils
(2.44 × 1.55 mm, 3.78 sq. mm)

NOTE: All V+ PADS ARE INTERNALLY CONNECTED.

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V-
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUT (B)
11. V+
12. OUT (A)
13. V+
14. BALANCE (A)

For additional DICE information refer to
1986 Data Book, Section 2.

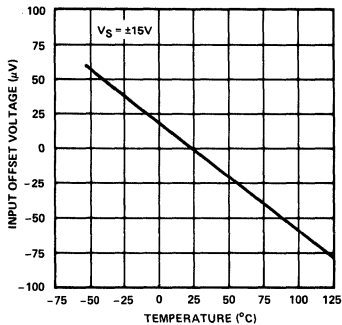
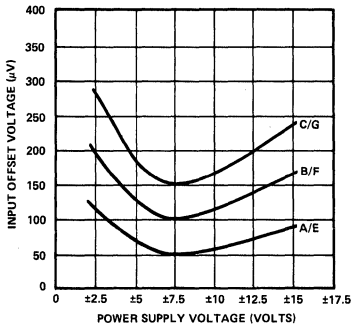
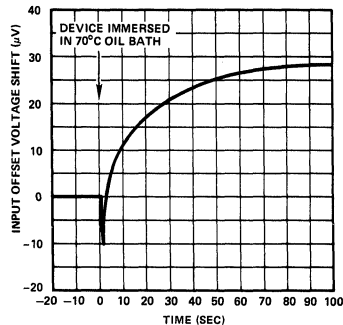
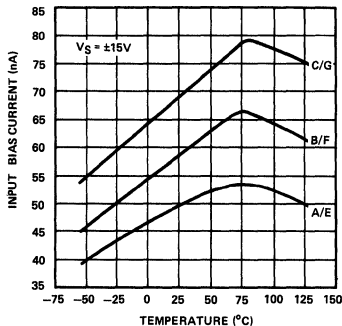
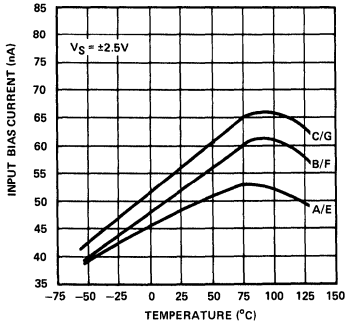
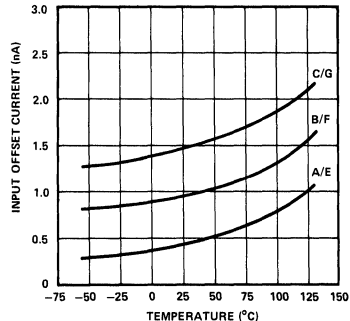
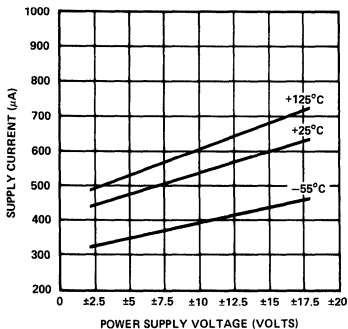
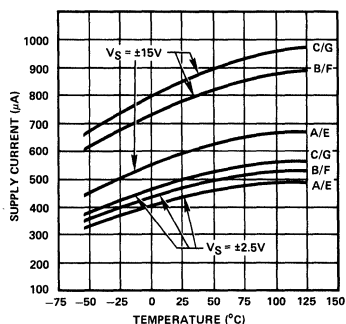
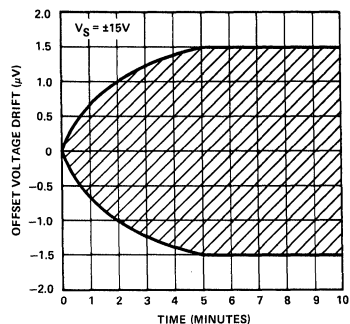
WAFER TEST LIMITS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221N LIMIT	OP-221G LIMIT	OP-221GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	350	500	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	3.5	5.5	7	nA MAX
Input Bias Current	I_B	$V_{CM} = 0$	85	105	120	nA MAX
Input Voltage Range	IVR	$V_+ = 5V, V_- = 0V$ $V_S = \pm 15V$	0/3.5 -15/13.5	0/3.5 -15/13.5	0/3.5 -15/13.5	V MIN/MAX V MIN
Common-Mode Rejection Ratio	CMRR	$V_- = 0V, V_+ = 5V, 0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V, -15V \leq V_{CM} \leq 13.5V$	88 93	83 88	75 80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V_- = 0V, V_+ = 5V$ to $30V$	12.5 22.5	40 70	100 180	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $R_L = 10k\Omega$	1500	1000	800	V/mV MIN
Output Voltage Swing	V_O	$V_+ = 5V, V_- = 0V, R_L = 10k\Omega$ $V_S = \pm 15V, R_L = 10k\Omega$	0.7/4.1 ± 13.8	0.7/4.1 ± 13.8	0.8/4 ± 13.5	V MIN/MAX V MIN
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	560 810	610 860	650 900	μA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

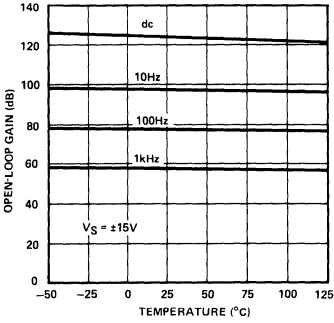
TYPICAL PERFORMANCE CHARACTERISTICS

NORMALIZED INPUT OFFSET VOLTAGE vs TEMPERATURE

INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

OFFSET VOLTAGE SHIFT DUE TO THERMAL SHOCK

INPUT BIAS CURRENT vs TEMPERATURE

INPUT BIAS CURRENT vs TEMPERATURE

INPUT OFFSET CURRENT vs TEMPERATURE

SUPPLY CURRENT vs SUPPLY VOLTAGE FOR OP-221A/E

SUPPLY CURRENT vs TEMPERATURE AT V_S = ±15V AND ±2.5V

INITIAL OFFSET VOLTAGE DRIFT vs TIME


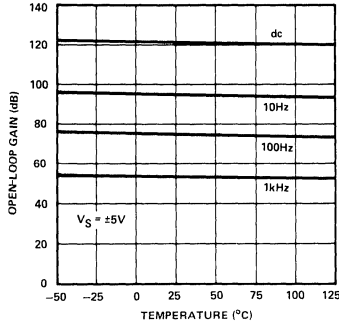


TYPICAL PERFORMANCE CHARACTERISTICS

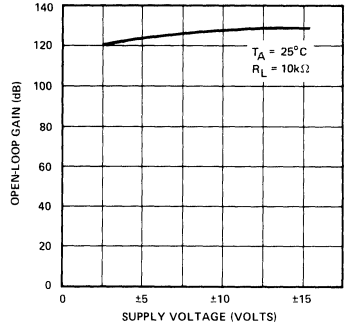
OPEN-LOOP GAIN AT ±15V vs TEMPERATURE



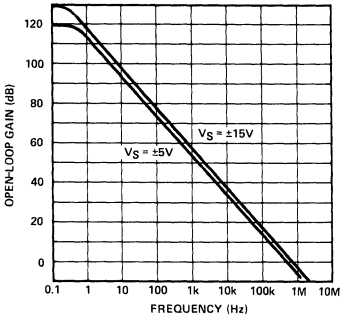
OPEN-LOOP GAIN AT ±5V vs TEMPERATURE



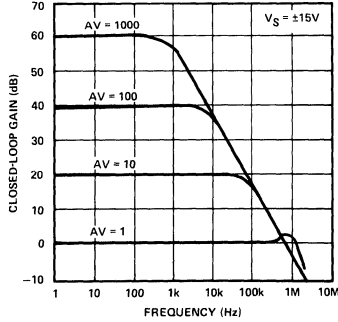
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



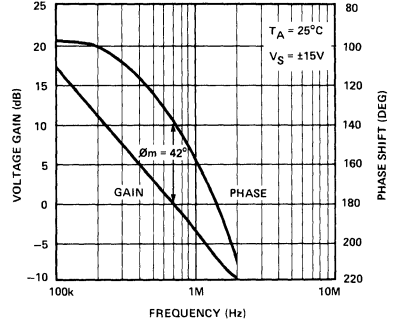
OPEN-LOOP GAIN vs FREQUENCY



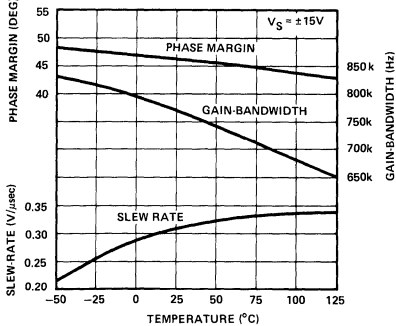
CLOSED-LOOP GAIN vs FREQUENCY



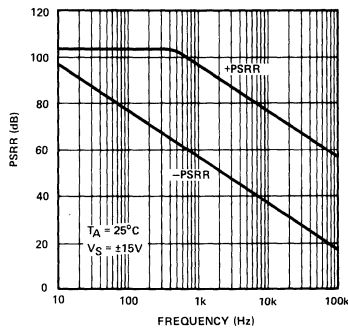
GAIN AND PHASE SHIFT vs FREQUENCY



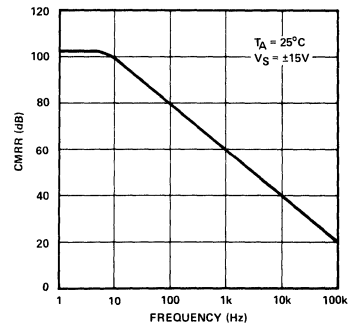
PHASE MARGIN, GAIN-BANDWIDTH, AND SLEW RATE vs TEMPERATURE

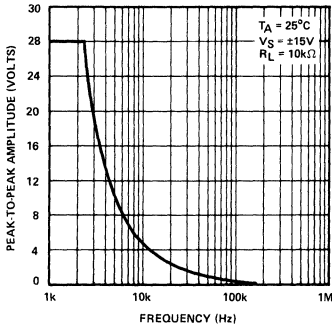
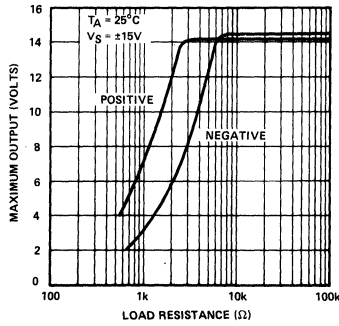
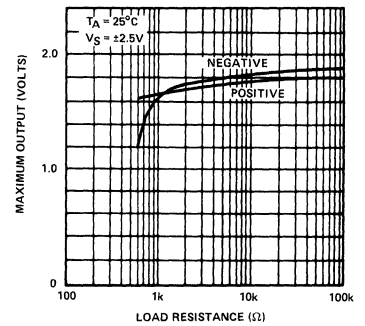
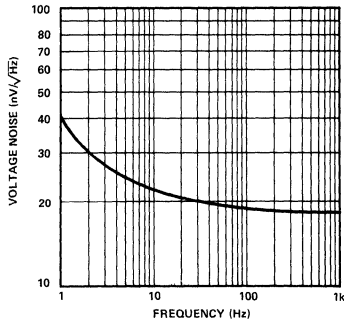
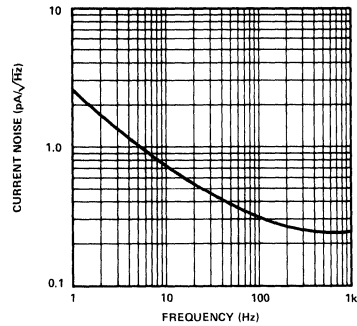
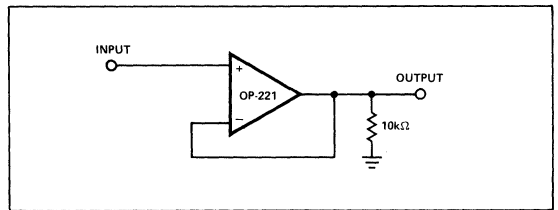
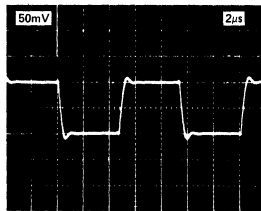
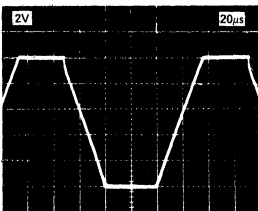
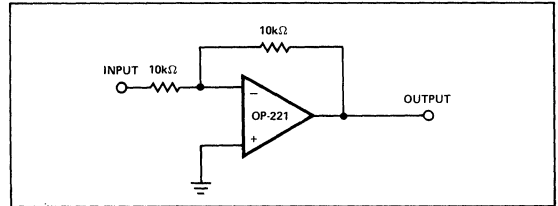
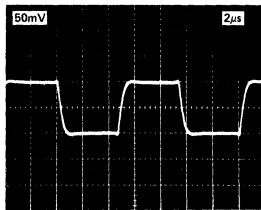
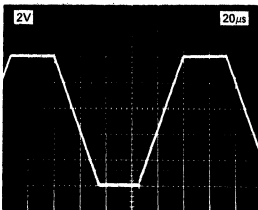


PSRR vs FREQUENCY



CMRR vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS
MAXIMUM OUTPUT SWING vs FREQUENCY

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY

CURRENT NOISE DENSITY (i_n) vs FREQUENCY

NONINVERTING STEP RESPONSE

INVERTING STEP RESPONSE


SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MONOLITHIC OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide the engineer with a powerful tool for designing instrumentation amplifiers and many other differential-input circuits. These designs are based on the principle that careful matching between two operational amplifiers can minimize the effect of DC errors in the individual amplifiers.

Reference to the circuit shown in Figure 1, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical. If the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifier's output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are high and tightly matched, an important feature not practical with single operational amplifier circuits.

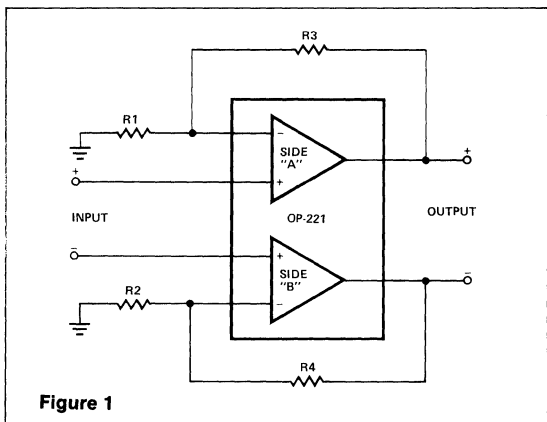


Figure 1

INSTRUMENTATION AMPLIFIER APPLICATIONS

Two-Op-Amp Configuration

The two-op-amp circuit (Figure 2), is recommended where the common-mode input voltage range is relatively limited; the common-mode and differential voltage both appear at V₁.

The high open-loop gain of the OP-221 is very important in achieving good CMRR in this configuration. Finite open-loop gain of A₁ (A₀₁) causes undesired feedthrough of the common-mode input. For A_d/A₀₁ ≪ 1, the common-mode error (CME) at the output due to this effect is approximately (2 A_d/A₀₁) × V_{CM}. This circuit features independent adjustment of CMRR and differential gain.

Three-Op-Amp Configuration

The three-op-amp circuit (Figure 3), has increased common-mode voltage range because the common-mode voltage is not amplified as it is in Figure 2. The CMR of this amplifier is directly proportional to the match of the CMR of the input op amps. CMRR can be raised even further by trimming the output stage resistors.

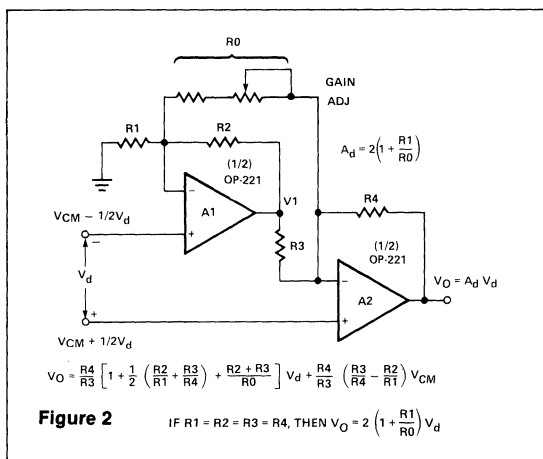


Figure 2

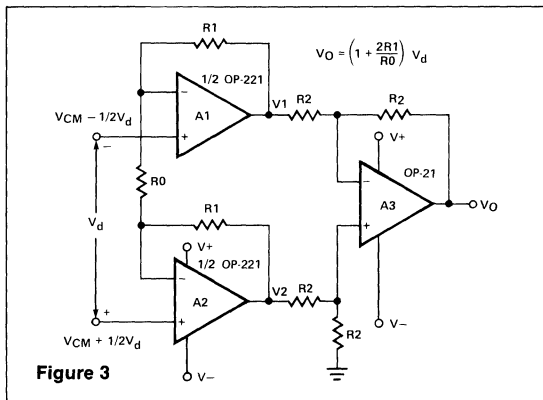


Figure 3



Precision Monolithics Inc.

FEATURES

- Excellent Individual Amplifier Parameters
- Low V_{OS} **80 μ V Max**
- Offset Voltage Match **80 μ V Max**
- Offset Voltage Match vs Temperature **1 μ V/ $^{\circ}$ C Max**
- Stable V_{OS} vs Time **1 μ V/Mo Max**
- Low Voltage Noise **3.9nV/ \sqrt Hz Max**
- Fast **2.8V/ μ s Typ**
- High Gain **1.8 Million Typ**
- High Channel Separation **154dB Typ**

ORDERING INFORMATION†

$T_A = 25^{\circ}$ C V_{OS} MAX (μ V)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
80	OP227AY*	MIL
80	OP227EY	IND
120	OP227BY*	MIL
120	OP227FY	IND
180	OP227CY*	MIL
180	OP227GY	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-227 is the first dual amplifier to offer a combination of low offset, low noise, high speed and guaranteed amplifier matching characteristics in one device. The OP-227 with a V_{OS} match of 25 μ V typical, a TCV_{OS} match of 0.3 μ V/ $^{\circ}$ C typical, and a 1/f corner of only 2.7Hz is an excellent choice for precision low noise designs. These D.C. characteristics, coupled with a slew rate of 2.8V/ μ s typical and a small-signal bandwidth of 8MHz typical, allow the designer to achieve AC performance previously unattainable with op-amp-based instrumentation designs.

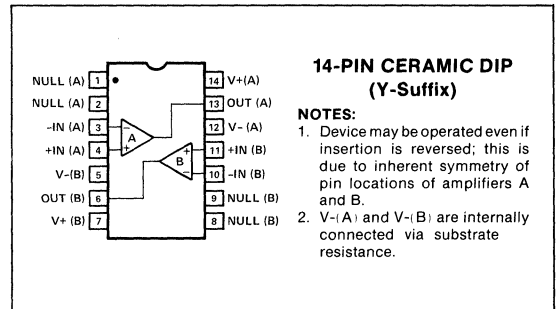
When used in a three-op-amp instrumentation amplifier configuration, the OP-227 can achieve a CMRR in excess of 100dB at 10kHz. In addition, this device has an open-loop gain of 1.5M typical with a 1k Ω load. The OP-227 also features an I_B of \pm 10nA typical, an I_{OS} of 7nA typical, and guaranteed matching of input currents between amplifiers. These outstanding input current specifications are realized through the use of a unique input current-cancellation-circuit which typically holds I_B and I_{OS} to \pm 20nA and 15nA respectively over the full military temperature range.

Other sources of input-referred errors, such as PSRR and CMRR, are reduced by factors in excess of 120dB for the individual amplifiers. D.C. stability is assured by a long-term drift specification of 1.0 μ V/month.

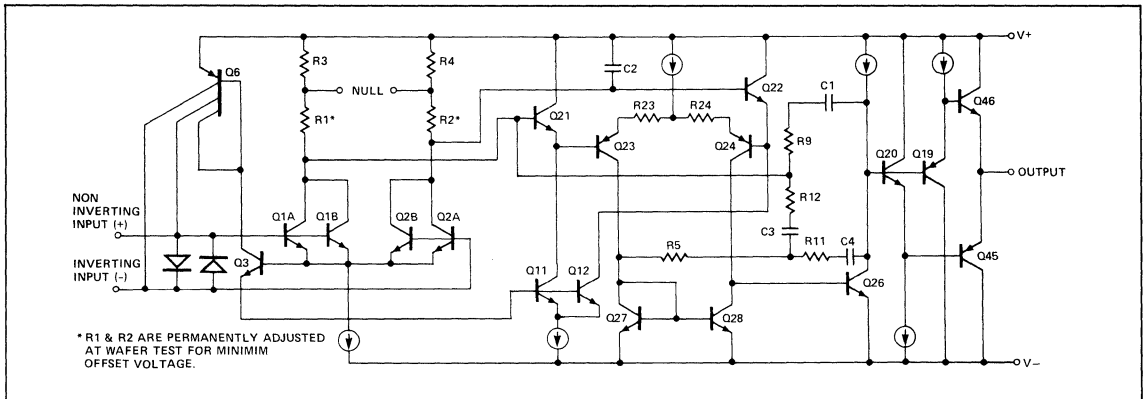
Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias current, CMRR, and power supply rejection ratio. This unique dual amplifier allows the elimination of external components for offset nulling and frequency compensation.

The OP-227 is pin compatible with the OP-10 and OP-207.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/2 OP-227)





ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature	
OP-227A, OP-227B, OP-227C	-55°C to +125°C
OP-227E, OP-227F, OP-227G	-25°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	300°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.

PACKAGE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin (Y)	106°C	11.3mW/°C

- The OP-227's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
- For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A/E			OP-227B/F			OP-227C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	20	80	—	40	120	—	60	180	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 4)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.20	—	0.08	0.20	—	0.09	0.28	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 3)	—	3.5	6.0	—	3.5	6.0	—	3.8	9.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 30\text{Hz}$ (Note 3)	—	3.1	4.7	—	3.1	4.7	—	3.3	5.9	
		$f_O = 1000\text{Hz}$ (Note 3)	—	3.0	3.9	—	3.0	3.9	—	3.2	4.6	
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Notes 3, 6)	—	1.7	4.5	—	1.7	4.5	—	1.7	—	$pA/\sqrt{\text{Hz}}$
		$f_O = 30\text{Hz}$ (Notes 3, 6)	—	1.0	2.5	—	1.0	2.5	—	1.0	—	
		$f_O = 1000\text{Hz}$ (Notes 3, 6)	—	0.4	0.7	—	0.4	0.7	—	0.4	0.7	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	G Ω
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/ μs
Gain Bandwidth Prod.	GBW	(Note 4)	5	8	—	5	8	—	5	8	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	Each Amplifier	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range	$R_P = 10k\Omega$		—	±4	—	—	±4	—	—	±4	—	mV

NOTES:

- Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grade specifications are guaranteed fully warmed up.
- Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30

- days are typically 2.5 μV — refer to typical performance curve.
- Sample tested.
- Parameter is guaranteed by design.
- See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
- See test circuit for current noise measurement.
- Guaranteed by input bias current.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** for $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A			OP-227B			OP-227C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	60	180	—	80	270	—	110	350	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Notes 2, 3)	—	0.3	1.0	—	0.4	1.5	—	0.5	1.8	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	± 20	± 60	—	± 28	± 95	—	± 35	± 150	nA
Input Voltage Range	IVR		± 10.0	± 11.5	—	± 10.0	± 11.5	—	± 10.0	± 11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.5	± 13.5	—	± 11.0	± 13.2	—	± 10.5	± 13.0	—	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS for $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227E			OP-227F			OP-227G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	40	140	—	60	200	—	85	280	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2)	—	0.5	1.0	—	0.4	1.5	—	0.5	1.8	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	± 14	± 60	—	± 18	± 95	—	± 25	± 150	nA
Input Voltage Range	IVR		± 10.0	± 11.8	—	± 10.0	± 11.8	—	± 10.0	± 11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.7	± 13.6	—	± 11.4	± 13.5	—	± 11.0	± 13.3	—	V

NOTES:

- Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
- The TCV_{OS} performance is within the specifications unnullled or when nullled with $R_P = 8k\Omega$ to $20k\Omega$, optimum performance is obtained with $R_P = 8k\Omega$.
- Sample tested.

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A/E			OP-227B/F			OP-227C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	25	80	—	35	150	—	55	300	μV
Average Noninverting Bias Current	I_{B+}	$I_{B+} = \frac{I_{B+A} + I_{B+B}}{2}$	—	± 10	± 40	—	± 12	± 55	—	± 15	± 90	nA
Noninverting Offset Current	I_{OS+}	$I_{OS+} = I_{B+A} - I_{B+B}$	—	± 12	± 60	—	± 15	± 80	—	± 20	± 130	nA
Inverting Offset Current	I_{OS-}	$I_{OS-} = I_{B-A} - I_{B-B}$	—	± 12	± 60	—	± 15	± 80	—	± 20	± 130	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 11V$	110	123	—	103	120	—	97	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 4V$ to $\pm 18V$	—	2	10	—	2	10	—	2	20	$\mu V/V$
Channel Separation	CS	(Note 1)	126	154	—	126	154	—	126	154	—	dB



MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = -55^\circ C$ to $+125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A			OP-227B			OP-227C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	55	180	—	75	300	—	100	480	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nullled or Unnullled (Note 2)	—	0.3	1.0	—	0.4	1.5	—	0.5	1.8	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B^+}	$I_{B^+} = \frac{I_{B^+A} + I_{B^+B}}{2}$	—	± 20	± 60	—	± 28	± 95	—	± 35	± 170	nA
Average Drift of Non-inverting Bias Current	TCI_{B^+}		—	100	—	—	160	—	—	200	—	$pA/^\circ C$
Noninverting Offset Current	I_{OS^+}	$I_{OS^+} = I_{B^+A} - I_{B^+B}$	—	± 25	± 90	—	± 35	± 140	—	± 45	± 250	nA
Average Drift of Non-inverting Offset Current	TCI_{OS^+}		—	130	—	—	200	—	—	250	—	$pA/^\circ C$
Inverting Offset Current	I_{OS^-}	$I_{OS^-} = I_{B^-A} - I_{B^-B}$	—	± 25	± 90	—	± 35	± 140	—	± 45	± 250	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$	105	118	—	97	114	—	90	110	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	3	20	—	4	51	$\mu V/V$

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = -25^\circ C$ to $+85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227E			OP-227F			OP-227G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	40	140	—	65	210	—	90	400	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nullled or Unnullled (Note 1)	—	0.3	1.0	—	0.4	1.5	—	0.5	1.8	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B^+}	$I_{B^+} = \frac{I_{B^+A} + I_{B^+B}}{2}$	—	± 14	± 60	—	± 18	± 95	—	± 25	± 170	nA
Average Drift of Non-inverting Bias Current	TCI_{B^+}		—	80	—	—	140	—	—	180	—	$pA/^\circ C$
Noninverting Offset Current	I_{OS^+}	$I_{OS^+} = I_{B^+A} - I_{B^+B}$	—	± 20	± 90	—	± 25	± 140	—	± 35	± 250	nA
Average Drift of Non-inverting Offset Current	TCI_{OS^+}		—	130	—	—	200	—	—	250	—	$pA/^\circ C$
Inverting Offset Current	I_{OS^-}	$I_{OS^-} = I_{B^-A} - I_{B^-B}$	—	± 20	± 90	—	± 25	± 140	—	± 35	± 250	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$	106	120	—	98	117	—	90	112	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	3	32	$\mu V/V$

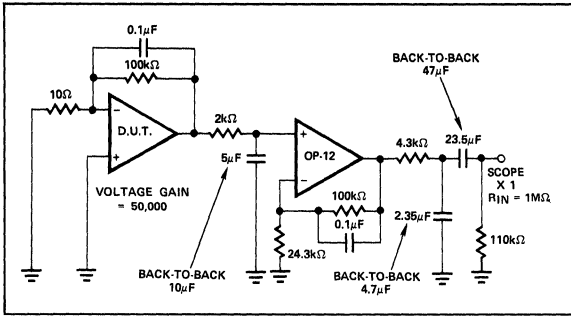
NOTES:

1. Sample tested.
2. Guaranteed by design.

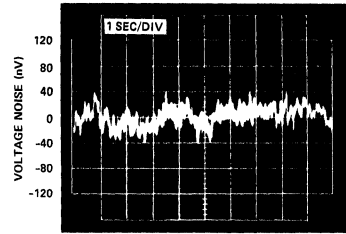
5
OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz_{p-p})



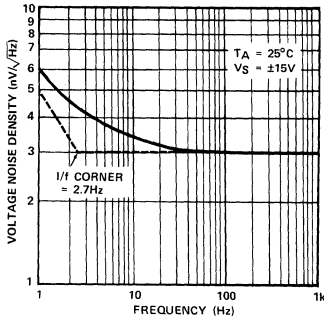
LOW-FREQUENCY NOISE



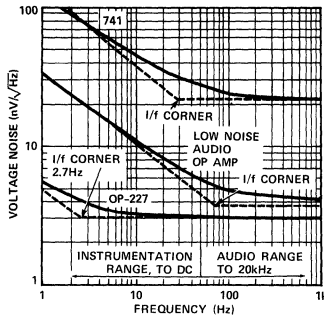
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE: OBSERVATION TIME MUST BE LIMITED TO 10 SECONDS TO ENSURE 0.1Hz CUTOFF.

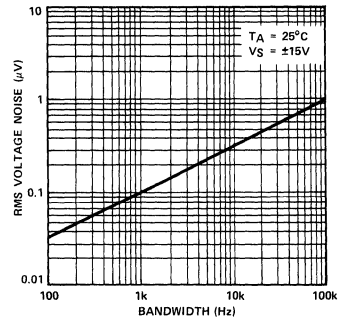
VOLTAGE NOISE DENSITY vs FREQUENCY



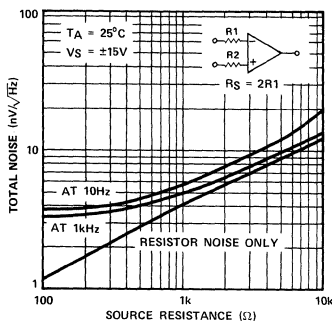
COMPARISON OF OP-AMP VOLTAGE NOISE SPECTRA



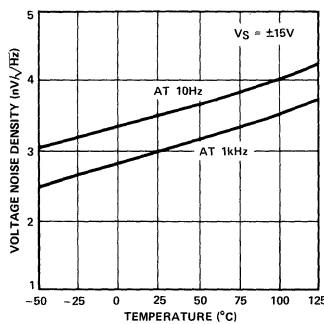
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



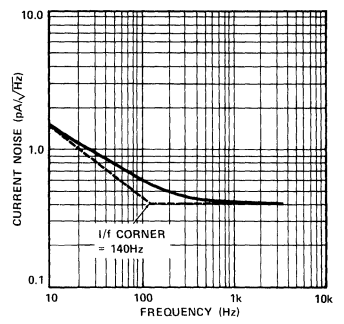
TOTAL NOISE vs SOURCE RESISTANCE



VOLTAGE NOISE DENSITY vs TEMPERATURE



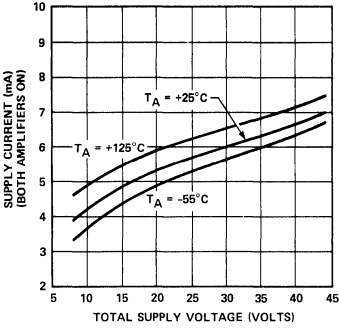
CURRENT NOISE DENSITY vs FREQUENCY



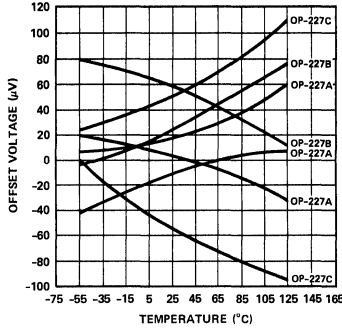


TYPICAL PERFORMANCE CHARACTERISTICS

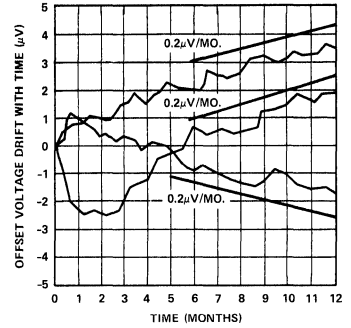
SUPPLY CURRENT vs SUPPLY VOLTAGE



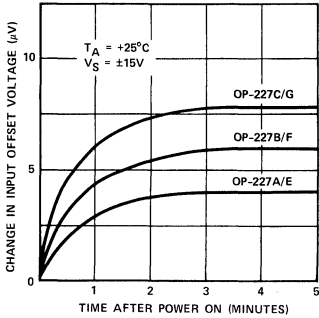
OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS



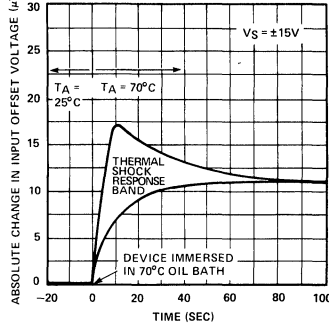
OFFSET VOLTAGE STABILITY WITH TIME



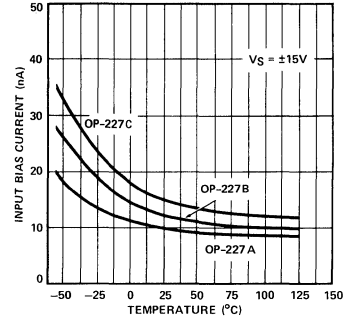
WARM-UP DRIFT



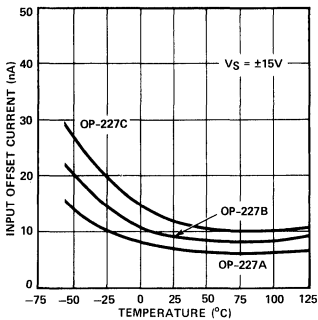
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



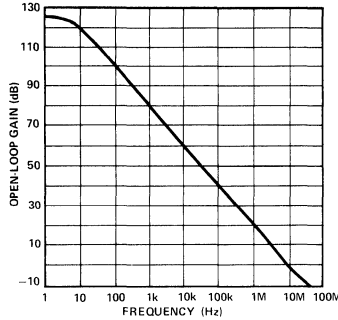
INPUT BIAS CURRENT vs TEMPERATURE



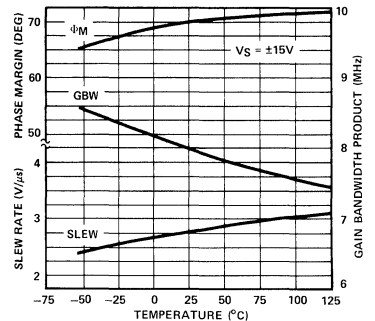
INPUT OFFSET CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs FREQUENCY

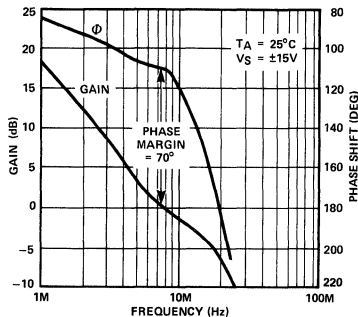
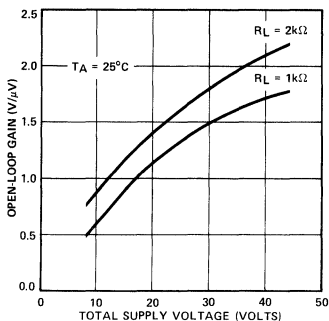
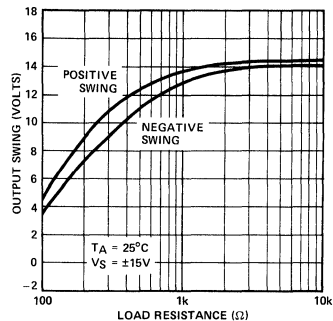
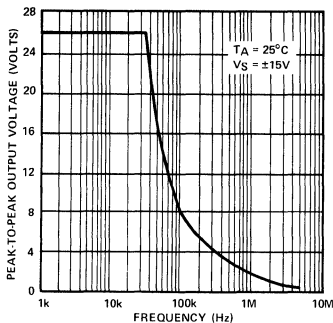
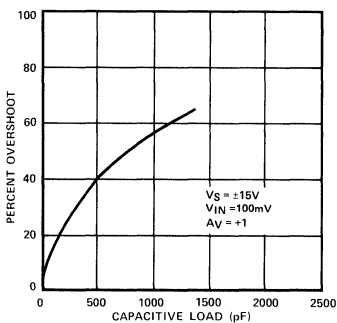
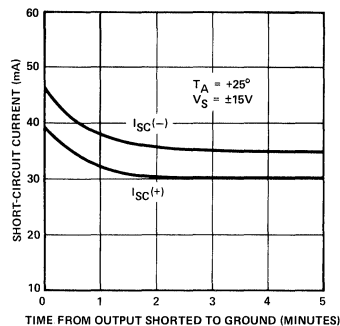
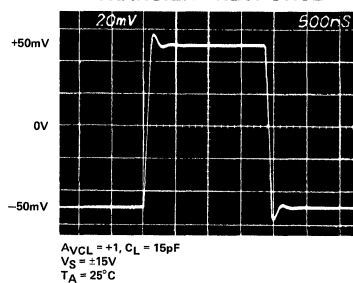
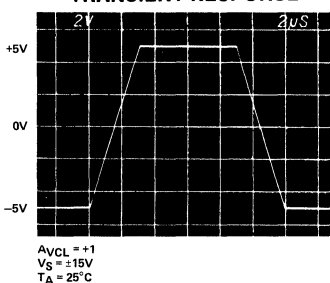
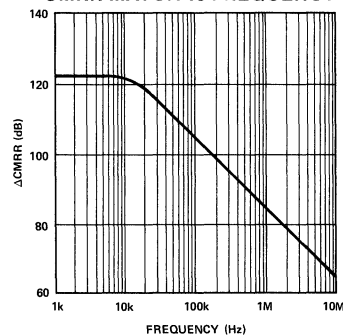


SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



5 OPERATIONAL AMPLIFIERS

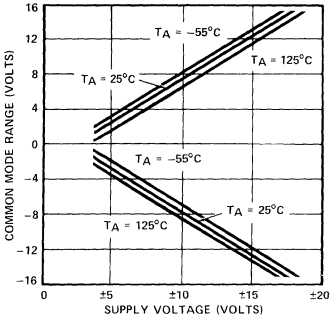
TYPICAL PERFORMANCE CHARACTERISTICS

GAIN, PHASE SHIFT vs FREQUENCY

OPEN-LOOP GAIN vs SUPPLY VOLTAGE

OUTPUT SWING vs RESISTIVE LOAD

MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

SHORT-CIRCUIT CURRENT vs TIME

SMALL-SIGNAL TRANSIENT RESPONSE

LARGE-SIGNAL TRANSIENT RESPONSE

MATCHING CHARACTERISTIC CMRR MATCH vs FREQUENCY


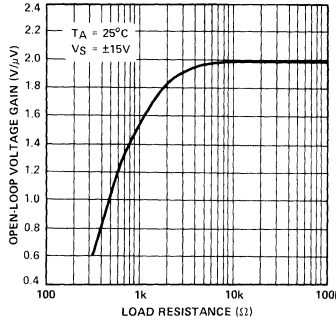


TYPICAL PERFORMANCE CHARACTERISTICS

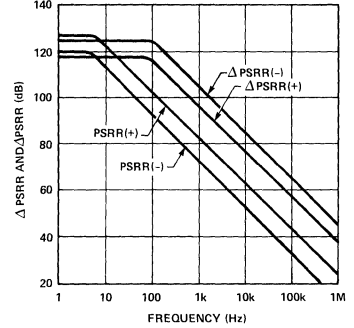
COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE



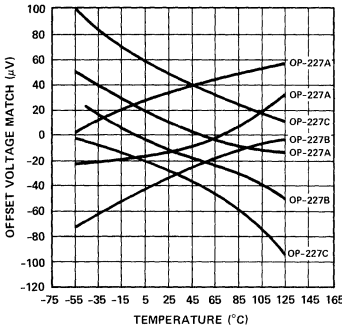
OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



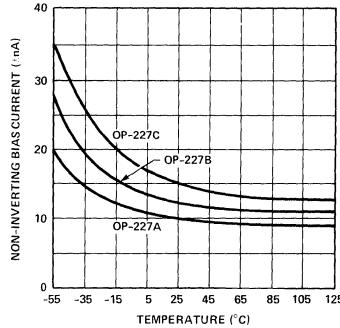
PSRR AND ΔPSRR vs FREQUENCY



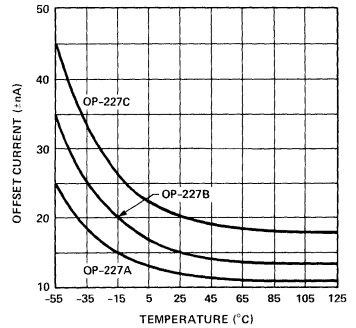
MATCHING CHARACTERISTIC; DRIFT OF OFFSET VOLTAGE MATCH OF REPRESENTATIVE UNITS



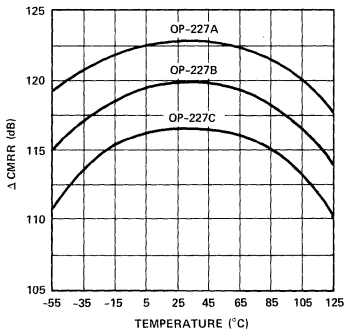
MATCHING CHARACTERISTIC; AVERAGE NONINVERTING BIAS CURRENT vs TEMPERATURE



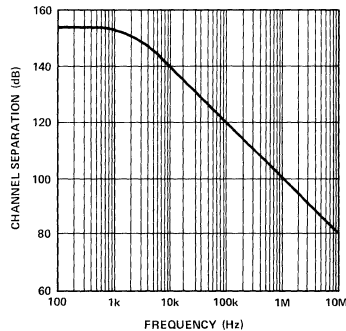
MATCHING CHARACTERISTIC; AVERAGE OFFSET CURRENT vs TEMPERATURE (INVERTING OR NONINVERTING)



MATCHING CHARACTERISTIC; CMRR MATCH vs TEMPERATURE



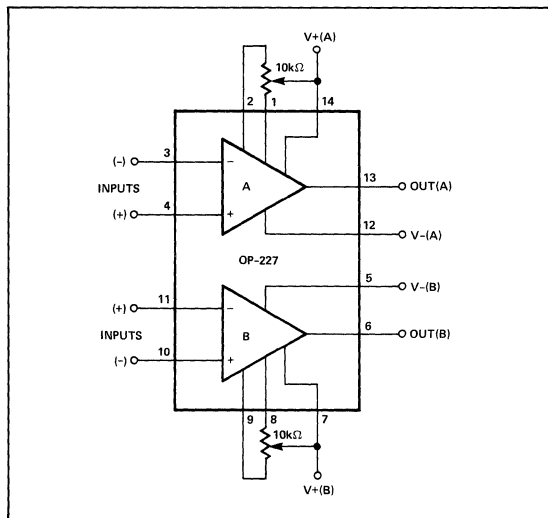
CHANNEL SEPARATION vs FREQUENCY



5 OPERATIONAL AMPLIFIERS

BASIC CONNECTIONS

OFFSET NULLING CIRCUIT



APPLICATIONS INFORMATION

NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-227 in the 0.1Hz to 10Hz range, the following precautions must be observed:

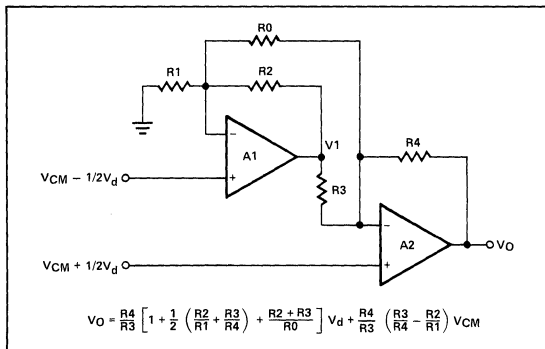
- (1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes $4\mu\text{V}$ due to increasing chip temperature after power-up. In the 10-second measurement interval these temperature-induced effects can exceed tens-of-nanovolts.
- (2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.
- (3) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.
- (4) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.
- (5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the $1/f$ corner frequency.

INSTRUMENTATION AMPLIFIER APPLICATIONS OF THE OP-227

The excellent input characteristics of the OP-227 make it ideal for use in *instrumentation amplifier* configurations where low-level differential signals are to be amplified. The low-noise, low input offsets, low drift, and high gain combined with excellent CMR provides the characteristics needed for high-performance instrumentation amplifiers. In addition, CMR vs. frequency is very good due to the wide gain-bandwidth of these op amps.

The circuit of Figure 1 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two-op-amp instrumentation amplifier features *independent* adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to non-inverting op amp inputs.

FIGURE 1: Two-Op-Amp Instrumentation Amplifier Configuration



The output voltage V_O , assuming ideal op amps, is given in Fig. 1. The input voltages are represented as a common-mode input V_{CM} plus a differential input V_d . The ratio R_3/R_4 is made equal to the ratio R_2/R_1 to reject the common-mode input V_{CM} . The differential signal V_d is then amplified according to:

$$V_O = \frac{R_4}{R_3} \left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_0} \right) V_d, \text{ where } \frac{R_3}{R_4} = \frac{R_2}{R_1}$$

Note that gain can be independently varied by adjusting R_0 . From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R_1 , R_2 , R_3 , and R_4 approximately equal. Designating R_1 , R_2 , R_3 , and R_4 as R_N allows the output equation to be further simplified:

$$V_O = 2 \left(1 + \frac{R_N}{R_0} \right) V_d, \text{ where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2; the output of A1 is:

$$V_1 = - \left(1 + \frac{R_N}{R_0} \right) V_d + 2 V_{CM}$$

If the instrumentation amplifier were designed for a gain of 10 and maximum V_d of $\pm 1V$, then R_N/R_O would need to be four and V_O would be a maximum of $\pm 10V$. Amplifier A1 would have a maximum output of $\pm 5V$ plus $2V_{CM}$, thus a limit of $\pm 10V$ on the output of A1 would imply a limit of $\pm 2.5V$ on V_{CM} . A nominal value of $10k\Omega$ for R_N is suitable for most applications. A range of 20Ω to $2.5k\Omega$ for R_O will then provide a gain range of 10 to 1000. The current through R_O is V_d/R_O , so the amplifiers must supply $\pm 10mV/20\Omega$ (or $\pm 0.5mA$) when the gain is at the maximum value of 1000 and V_d is at $\pm 10mV$.

Rejecting common-mode inputs is important in accurately amplifying low-level differential signals. Two factors determine the CMR in this instrumentation amplifier configuration (assuming infinite gain):

- (1) CMR of the op amps
- (2) Matching of the resistor network ratios ($R_3/R_4 = R_2/R_1$)

In this instrumentation amplifier configuration, error due to CMR effect is directly proportional to the CMR match of the op amps. For the OP-227 this ΔCMR is a minimum of 97dB for the "G" and 110dB for the "E" grade. A ΔCMR value of 100dB and common-mode input range of $\pm 2.5V$ indicates a peak input-referred error of only $\pm 25\mu V$. Resistor matching is the other factor affecting CMR. Defining A_d as the differential gain of the instrumentation amplifier and assuming that R_1 , R_2 , R_3 and R_4 are approximately equal (R_N will be the nominal value), then CMR for this instrumentation amplifier configuration will be approximately A_d divided by $4\Delta R/R_N$. CMR at differential gain of 100 would be 88dB with resistor matching of 0.1%. Trimming R_1 to make the ratio R_3/R_4 equal to R_2/R_1 will raise the CMR until limited by linearity and resistor stability considerations.

The high open-loop gain of the OP-227 is very important to achieving high accuracy in the two op-amp instrumentation amplifier configuration. Gain error can be approximated by

$$\text{Gain Error} \sim \frac{1}{1 + \frac{A_d}{A_{O2}}} \quad , \quad \frac{A_d}{2 A_{O1} A_{O2}} \ll 1$$

where A_d is the instrumentation amplifier differential gain and A_{O2} is the open-loop gain of op amp A2. This analysis assumes equal values of R_1 , R_2 , R_3 , and R_4 . For example, consider an OP-227 with A_{O2} of 700V/mV. If the differential gain A_d were set to 700, then the gain error would be 1/1.001 which is approximately 0.1%.

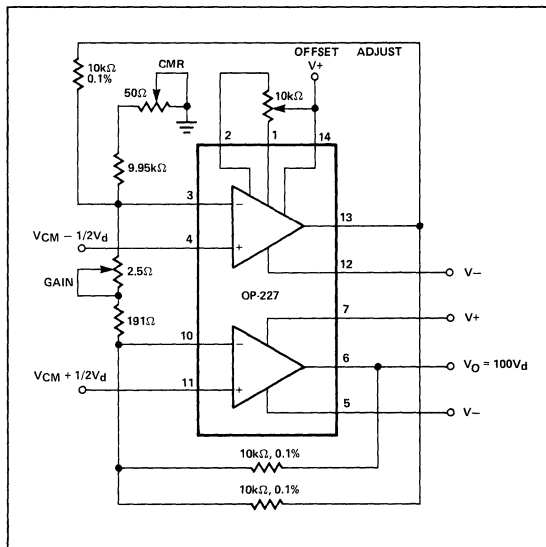
Another effect of finite op amp gain is undesired feedthrough of common-mode input. Defining A_{O1} as the open-loop gain of op amp A1, then the common-mode error (CME) at the output due to this effect will be approximately

$$\text{CME} \sim \frac{2 A_d}{1 + \frac{A_d}{A_{O1}}} \cdot \frac{1}{A_{O1}} V_{CM}$$

For $A_d/A_{O1} \ll 1$, this simplifies to $(2A_d/A_{O1}) \times V_{CM}$. If the op amp gain is 700V/mV, V_{CM} is 2.5V, and A_d is set to 700, then the error at the output due to this effect will be approximately 5mV.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 2. It has provision for trimming input offset voltage, CMR, and gain. Performance is excellent due to the high gain, high CMR, and low noise of the individual amplifiers combined with the tight matching characteristics of the OP-227 dual.

FIGURE 2: Two-Op-Amp Instrumentation Amplifier Using OP-227 Dual



A three-op-amp instrumentation amplifier configuration using the OP-227 and OP-27 is recommended for applications requiring high accuracy over a wide gain range. This circuit provides excellent CMR over a wide frequency range. As with the two-op-amp instrumentation amplifier circuits, the tight matching of the two op-amps within the OP-227 package provides a real boost in performance. Also, the low-noise, low offset, and high gain of the individual op-amps minimize errors.

A simplified schematic is shown in Figure 3. The input stage (A1 and A2) serves to amplify the differential input V_d without amplifying the common-mode voltage V_{CM} . The output stage then rejects the common-mode input. With ideal op-amps and no resistor matching errors, then the outputs of each amplifier will be:

$$V_1 = -\left(1 + \frac{2R_1}{R_O}\right) \frac{V_d}{2} + V_{CM}$$

$$V_2 = \left(1 + \frac{2R_1}{R_O}\right) \frac{V_d}{2} + V_{CM}$$

$$V_O = V_2 - V_1 = \left(1 + \frac{2R_1}{R_O}\right) V_d$$

$$V_O = A_d V_d$$

5
OPERATIONAL AMPLIFIERS

The differential gain A_d is $1 + 2R_1/R_O$ and the common-mode input V_{CM} is rejected.

While output error due to input offsets and noise are easily determined, the effects of finite gain and common-mode rejection are more subtle. CMR of the complete instrumentation amplifier is directly proportioned to the *match* in CMR of the input op-amps. This match varies from 97dB to 110dB minimum for the OP-227. Using 100dB, then the output response to a common-mode input V_{CM} would be:

$$[V_O]_{CM} = A_d V_{CM} \times 10^{-5}$$

CMRR of the instrumentation amplifier, which is defined as $20 \log_{10} A_d/A_{CM}$, is simply equal to the Δ CMRR of the OP-227. While this Δ CMRR is already high, overall CMRR of the complete amplifier can be raised by trimming the output stage resistor network.

Finite gain of the input op-amps causes a scale factor error and a small degradation in CMR. Designating the open-loop gain of op-amp A_1 as A_{O1} , and op-amp A_2 as A_{O2} , then the following equation approximates the output:

$$V_O \sim \frac{1}{1 + \frac{R_1}{R_O} \left(\frac{1}{A_{O1}} + \frac{1}{A_{O2}} \right)} \left[A_d V_d + \frac{2R_1}{R_O} \left(\frac{1}{A_{O1}} - \frac{1}{A_{O2}} \right) V_{CM} \right]$$

This can be simplified by defining A_O as the nominal open-loop gain and ΔA_O as the differential open-loop gain. Then

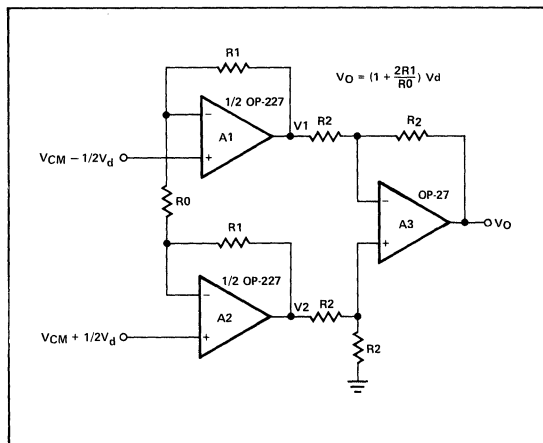
$$V_O \sim \frac{1}{1 + \frac{2R_1}{R_O} \frac{1}{A_O}} \left[A_d V_d + \frac{2R_1}{R_O} \frac{\Delta A_O}{A_O^2} V_{CM} \right]$$

The high open-loop gain of each amplifier within the OP-227 (700,000 minimum at 25° C into $R_L \geq 2k$) assures good gain accuracy even at high values of A_d . The effect of finite open-loop gain on CMR can be approximated by:

$$CMRR \sim \frac{A_O^2}{\Delta A_O}$$

If $\Delta A_O/A_O$ were 6% and A_O were 600,000, then the CMRR due to finite gain of the input op-amps would be approximately 140dB.

FIGURE 3: Three-Op-Amp Instrumentation Amplifier Using OP-227 and OP-27



The unity-gain output stage contributes negligible error to the overall amplifier. However, matching of the four-resistor R_2 -network is critical to achieving high CMR. Consider a worst-case situation where each R_2 resistor has an error of $\pm \Delta R_2$. If the resistor ratio is high on one side and low on the other, then the common-mode gain will be $2\Delta R_2/R_2$. Since the output stage gain is unity, CMRR will then be $R_2/2\Delta R_2$. It is common practice to trim the R_2 resistor connected to ground to maximize overall CMRR for the total instrumentation amplifier circuit.

This three-op-amp instrumentation amplifier configuration provides excellent performance over a wide gain range. A gain range of 1 to 2000 is practical and CMR of over 120dB is achievable.



OP-400

QUAD LOW-OFFSET LOW-POWER OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Low Input Offset Voltage 100 μ V Max
- Low Input Offset Voltage Drift 0.5 μ V/ $^{\circ}$ C Max
- High Open-Loop Gain 2000V/mV Min
- Low Input Bias Current 1nA Max
- Low Noise Voltage Density 12nV/ $\sqrt{\text{Hz}}$ at 1kHz
- Low Supply Current (per Amplifier) 700 μ A Max
- Pin Compatible to LM148, LM348, RM4156, and HA4741 with Improved Performance

ORDERING INFORMATION†

T _A = 25°C V _{OS} Max (μ V)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC DIP 14-PIN	PLASTIC DIP 14-PIN	
100	OP400AY*		MIL
100	OP400EY	OP400EP	IND
300	OP400BY*		MIL
300	OP400FY	OP400FP	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

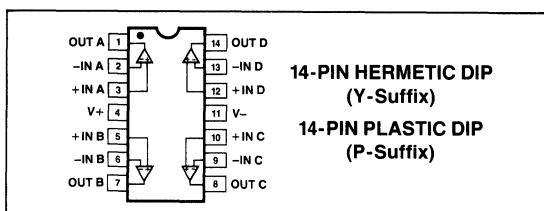
† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-400 is a monolithic quad operational amplifier that combines precision performance and low power consumption. This precision is guaranteed by an input offset voltage of less than 100 μ V with a drift of under 0.5 μ V/ $^{\circ}$ C, an input offset current below 0.2nA, and an open-loop gain of over 2 million into a 2k Ω load. In addition, the OP-400 has an input bias current of less than 1nA and a CMRR and PSRR of over 115dB. The OP-400 meets low power requirements by drawing less than 700 μ A of supply current per amplifier. Voltage noise density of the OP-400 is a low 12nV/ $\sqrt{\text{Hz}}$ at 1kHz.

The OP-400 is pin compatible with the LM148, LM348, RM4156, and HA4741 op amps and can be used to improve systems using these devices. It is an ideal choice for applications where multiple op amps are required and precision performance and low power consumption is critical.

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS at V_S = \pm 15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-400A/E			OP-400B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}		—	—	100	—	—	300	μ V
Input Offset Current	I _{OS}		—	—	0.2	—	—	0.5	nA
Input Bias Current	I _B		—	—	1	—	—	3	nA
Input Noise Voltage Density	e _n	f ₀ = 1kHz	—	12	—	—	12	—	nV/ $\sqrt{\text{Hz}}$
Input Voltage Range	IVR		\pm 12	—	—	\pm 12	—	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = \pm 12V	115	—	—	115	—	—	dB
Power Supply Rejection Ratio	PSRR	V _S = \pm 5V to \pm 18V	1.8	—	—	1.8	—	—	μ V/V
Large-Signal Voltage Gain	A _{VO}	R _L \geq 10k Ω	5000	—	—	2500	—	—	V/mV
		R _L \geq 2k Ω	2000	—	—	1000	—	—	

This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-400A/E			OP-400B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	—	—	± 12	—	—	V
Gain Bandwidth Product	GBW		—	1	—	—	1	—	MHz
Supply Current (All Amplifiers)	I_{SY}	No Load	—	2	2.8	—	2	2.8	mA
Slew Rate	SR		—	0.3	—	—	0.3	—	V/ μs



OP-420

QUAD MICROPOWER OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Supply Current 200 μ A Max @ $V_S = +5V$
- Single-Supply Operation +5V to +30V
- Dual-Supply Operation $\pm 2.5V$ to $\pm 15V$
- Low Input Offset Voltage 500 μ V Typ
- Low Input Offset Voltage Drift 5 μ V/ $^{\circ}$ C Typ
- High Common-Mode Input Range ... V- to (V+ - 1.5V)
- High CMRR 100dB Typ
- High Open-Loop Gain 1100V/mV Typ
- LM 148 Pinout

ORDERING INFORMATION†

$T_A = 25^{\circ}$ C V_{OS} MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC DIP 14-PIN	LCC	
2.5	OP420BY*		MIL
2.5	OP420FY		IND
4.0	OP420CY*	OP420CRC/883	MIL
4.0	OP420GY		IND
6.0	OP420HY		COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

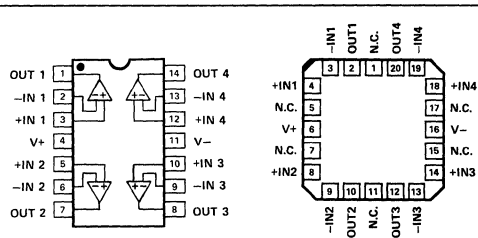
GENERAL DESCRIPTION

The OP-420 quad micropower operational amplifier is a single-chip quad patterned after the OP-20 precision micro-

power single operational amplifier. A Darlington PNP input stage allows the input common-mode voltage to include V-. The wide input range combined with low power-supply drain ($\sim 40\mu$ A/section at 5V), provides a unique solution for designs requiring high functional density and portable operation. Applications include two-wire transmitters for process control loops, battery-operated remote-line filters, signal preconditioning amplifiers, and a variety of multiple-gain block arrays.

For micropower applications requiring offset nulling, see the OP-20, OP-21 and OP-22 data sheets.

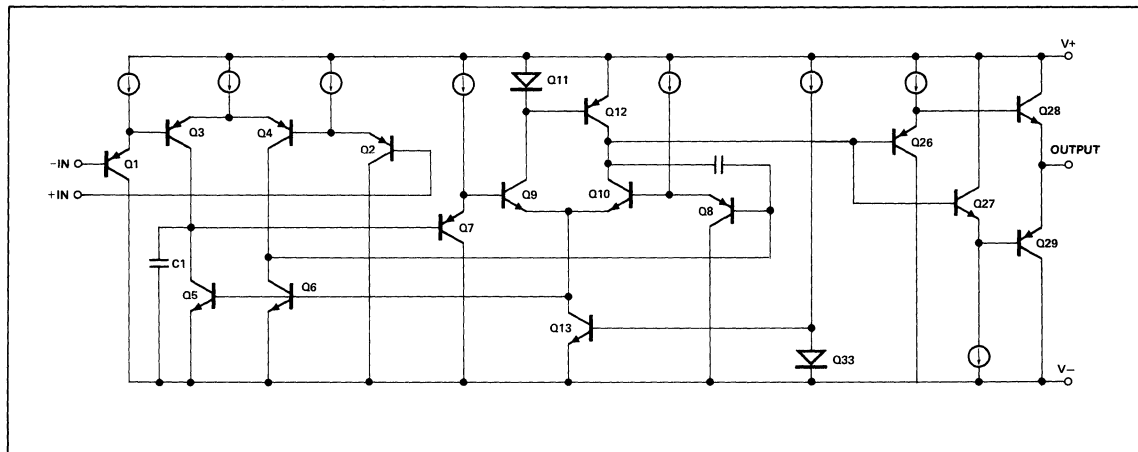
PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)

OP-420CRC/883
20-LEAD LCC
(RC-Suffix)

SIMPLIFIED SCHEMATIC (1/4 Shown)



OPERATIONAL AMPLIFIERS

5



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage $\pm 18V$
 Internal Power Dissipation (Note 1) 500mW
 Differential Input Voltage $\pm 30V$
 Input Voltage Supply Voltage
 Output Short-Circuit Duration Continuous
 (One Amplifier Only)
 Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature Range (Soldering, 60 sec) $300^{\circ}C$
 Operating Temperature Range
 OP-420BY, OP-420CY $-55^{\circ}C$ to $+125^{\circ}C$
 OP-420FY, OP-420GY $-25^{\circ}C$ to $+85^{\circ}C$

OP-420HY $0^{\circ}C$ to $+70^{\circ}C$
 DICE Junction Temperature (T_j) $-65^{\circ}C$ to $+150^{\circ}C$

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-420B OP-420F			OP-420C OP-420G			OP-420H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current (Note 1)	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	1.5	—	0.8	2.5	—	1.2	6	nA
Input Bias Current (Note 1)	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	9	20	—	12	30	—	18	40	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$	—	50	—	—	50	—	—	50	—	nV/ \sqrt{Hz}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$	—	0.12	—	—	0.12	—	—	0.12	—	pA/ \sqrt{Hz}
Input Voltage Range	IVR	$V+ = +5V, V- = 0V$ $V_S = \pm 15V$	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V+ = +5V, V- = 0V$ $0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V$	83	100	—	80	96	—	76	90	—	dB
		$-15V \leq V_{CM} \leq 13.5V$	83	100	—	80	96	—	76	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & $V- = 0V, V+ = 5V$ to $30V$	—	10	30	—	20	50	—	30	80	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$, $V_O = \pm 10V$	600	1100	—	400	900	—	200	800	—	V/mV
Slew Rate	SR		—	0.05	—	—	0.05	—	—	0.05	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	—	150	—	—	150	—	—	150	—	kHz
Output Voltage Swing	V_O	$V+ = 5V, V- = 0V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 25k\Omega$	0.7/4.1	—	—	0.8/4.0	—	—	0.9/3.8	—	—	V
			± 14.0	—	—	± 14.0	—	—	± 13.8	—	—	
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	140	200	—	170	300	—	200	400	μA
		$V_S = \pm 15V$, No Load	—	330	360	—	360	460	—	390	600	

NOTE:

1. I_B and I_{OS} are measured at $V_{CM} = 0$.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-420B and OP-420C, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-420F and OP-420G, and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-420H, unless otherwise noted.

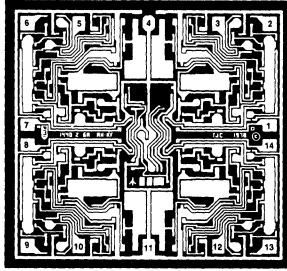
PARAMETER	SYMBOL	CONDITIONS	OP-420B OP-420F			OP-420C OP-420G			OP-420H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	5	10	—	8	15	—	15	25	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3.5	—	—	5.5	—	—	7.5	mV
Input Offset Current (Note 2)	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3	—	—	4	—	—	8	nA
Input Bias Current (Note 2)	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	30	—	—	40	—	—	60	nA
Input Voltage Range	IVR	$V^+ = +5V, V^- = 0V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	-15/13.2	—	—	-15/13.2	—	—	-15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	$V^+ = +5V, V^- = 0V,$ $0V \leq V_{CM} \leq 3.2V$	76	96	—	73	92	—	73	86	—	dB
		$V_S = \pm 15V,$ $-15V \leq V_{CM} \leq 13.2V$	76	96	—	73	92	—	73	86	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and $V^- = 0V, V^+ = 5V$ to 30V	—	15	50	—	25	80	—	40	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, R_L = 50k\Omega,$ $V_O = \pm 10V$	300	800	—	200	650	—	100	400	—	V/mV
Output Voltage Swing	V_O	$V^+ = 5V, V^- = 0V,$ $R_L = 20k\Omega$	0.9/3.9	—	—	1.0/3.8	—	—	1.1/3.6	—	—	V
		$V_S = \pm 15V,$ $R_L = 50k\Omega$	± 13.8	—	—	± 13.8	—	—	± 13.6	—	—	
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V, \text{No Load}$	—	170	300	—	210	400	—	250	600	μA
		$V_S = \pm 15V, \text{No Load}$	—	390	500	—	420	640	—	500	800	

NOTES:

- Sample tested.
- I_B and I_{OS} are measured at $V_{CM} = 0$.



DICE CHARACTERISTICS



DIE SIZE 0.092 × 0.086 inch, 7912 sq. mils
(2.34 × 2.18 mm, 5.10 sq. mm)

1. OUTPUT 1
2. INVERTING INPUT 1
3. NONINVERTING INPUT 1
4. V+
5. NONINVERTING INPUT 2
6. INVERTING INPUT 2
7. OUTPUT 2
8. OUTPUT 3
9. INVERTING INPUT 3
10. NONINVERTING INPUT 3
11. V-
12. NONINVERTING INPUT 4
13. INVERTING INPUT 4
14. OUTPUT 4

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-420N LIMIT	OP-420G LIMIT	OP-420GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	2.5	4	6	mV MAX
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$, (Note 1)	1.5	2.5	6	nA MAX
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$, (Note 1)	20	30	40	nA MAX
Input Voltage Range	IVR		-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_+ = +5V$, $V_- = 0V$	83	80	76	dB MIN
		$0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.5V$	83	80	76	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V_- = 0V$, $V_+ = +5V$ to $+30V$	30	50	80	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$, $V_O = \pm 10V$	600	400	200	V/mV MIN
Output Voltage Swing	V_O	$V_+ = +5V$, $V_- = 0V$ $R_L = 10k\Omega$ $V_S = \pm 15V$	0.7/4.1	0.8/4.0	0.9/3.8	V MAX
		$R_L = 25k\Omega$	± 14.0	± 14.0	± 13.8	V MIN
Supply Current	I_{SY}	No Load, (Four Amplifiers)	360	460	600	μA MAX

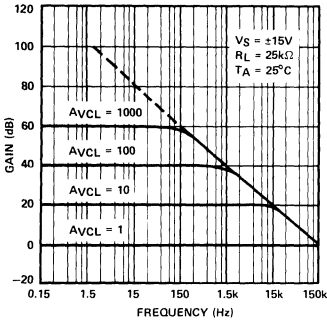
NOTES:

1. I_B and I_{OS} are measured at $V_{CM} = 0$.

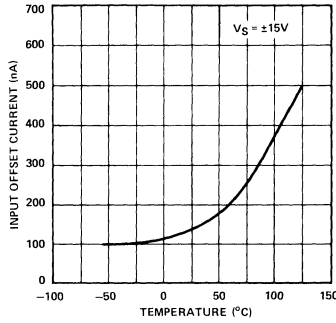
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

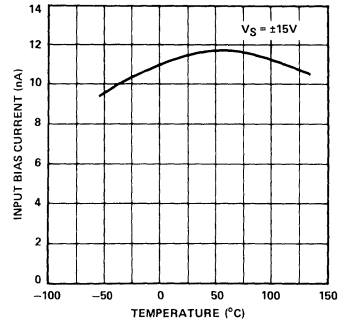
CLOSED-LOOP GAIN vs FREQUENCY



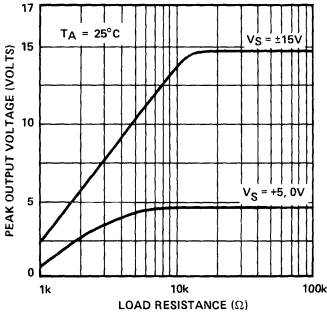
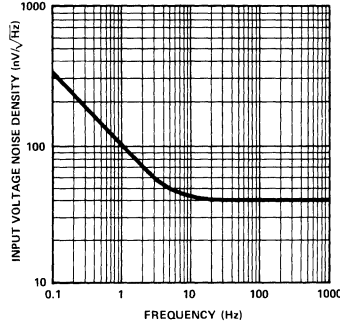
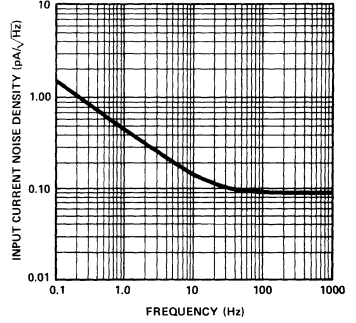
INPUT OFFSET CURRENT vs TEMPERATURE



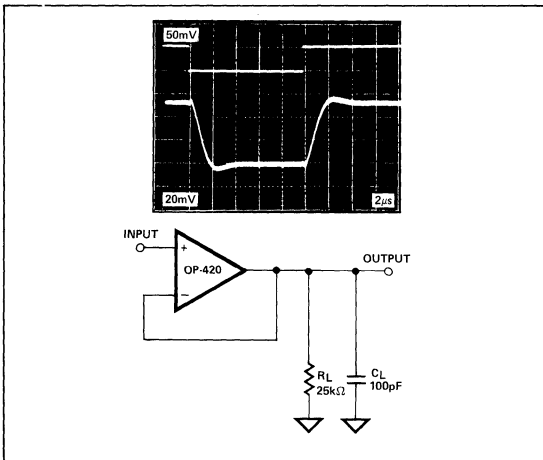
INPUT BIAS CURRENT vs TEMPERATURE



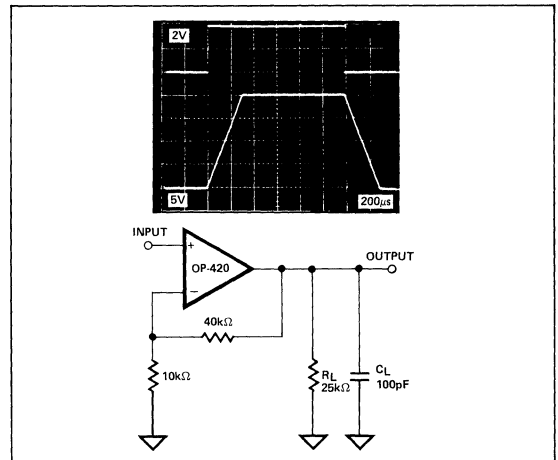
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE


 INPUT VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY

 INPUT CURRENT NOISE DENSITY (i_n) vs FREQUENCY


SMALL-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE



Precision Monolithics Inc.

FEATURES

- Low Supply Current 1mA Max
- Slew Rate 0.25V/ μ s Min
- Single Supply Operation +5V to +30V
- Low Input Offset Voltage 500 μ V Typ
- Low Input Offset Voltage Drift 10 μ V/ $^{\circ}$ C Max
- High Common-Mode Input Range ... V- to V+ (-1.5V)
- High CMRR 100dB Typ
- High Open-Loop Gain 400V/mV Typ
- Single-Chip Monolithic Construction
- Pin Compatible With LM124, LM148, and OP-11

ORDERING INFORMATION†

T _A = 25 $^{\circ}$ C V _{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
2.5	OP421BY*	MIL
2.5	OP421FY	IND
4	OP421CY*	MIL
4	OP421GY	IND
6	OP421HY	COM

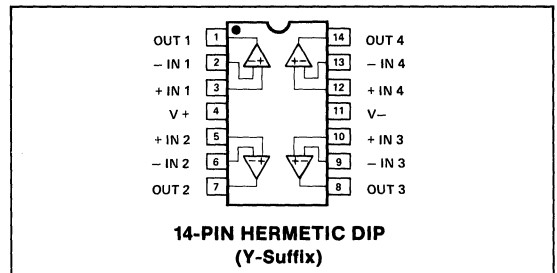
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

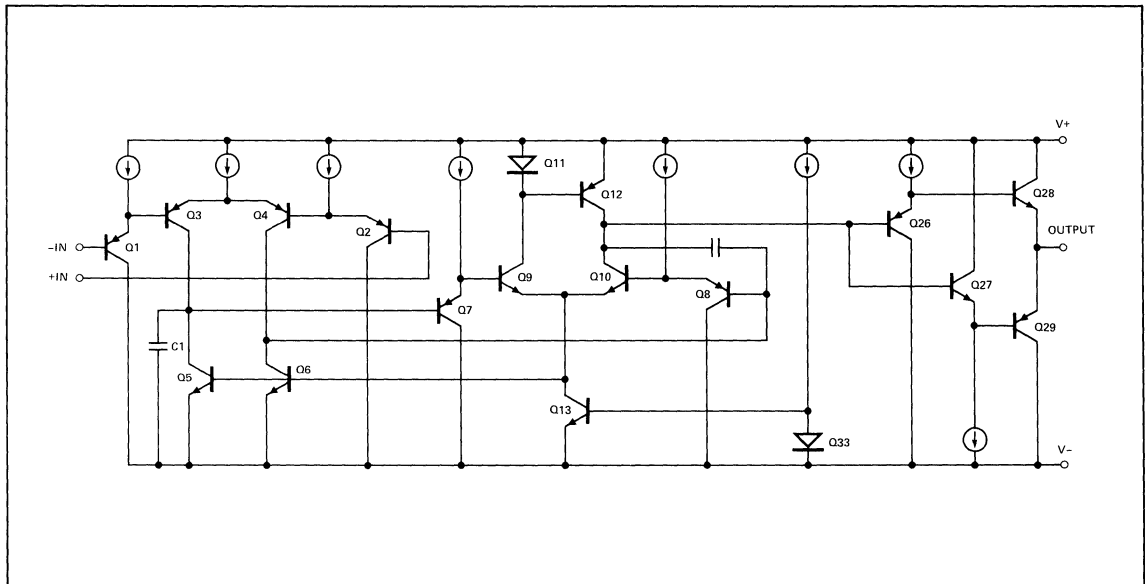
GENERAL DESCRIPTION

The OP-421 quad low-power operational amplifier is a single-chip quad patterned after the OP-21 single operational amplifier. The PNP input stage allows the input common-mode voltage to include V-. Featuring a low power-supply current (150 μ A/section typical at 5V), the OP-421 offers a unique solution for designs requiring a combination of high function density, wide bandwidth, and low-power operation. Applications for the OP-421 include low-power active filters, battery-operated remote line filters, and signal preconditioning amplifiers. In addition, the ever-present problem of crossover distortion in low-power devices is eliminated by a unique double-buffered output section.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/4 Shown)





ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ±18V
 Internal Power Dissipation (Note 1) 500mW
 Differential Input Voltage ±30V
 Input Voltage Supply Voltage
 Output Short-Circuit Duration Continuous
 (One Amplifier Only)
 Storage Temperature Range -65°C to +150°C
 Lead Temperature Range (Soldering, 60 sec) 300°C
 Operating Temperature Range
 OP-421BY, OP-421CY -55°C to +125°C
 OP-421FY, OP-421GY -25°C to +85°C
 OP-421HY 0°C to +70°C

DICE Junction Temperature (T_j) -65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421B OP-421F			OP-421C OP-421G			OP-421H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.6	5.0	—	2.0	10	—	5.0	20	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	20	50	—	50	80	—	100	150	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 1)	—	20	40	—	20	40	—	20	40	nV/\sqrt{Hz}
		$f_O = 100Hz$ (Note 1)	—	15	30	—	15	30	—	15	30	
Input Noise Current Density	i_n	$f_O = 10Hz$ (Note 1)	—	0.3	0.6	—	0.3	0.6	—	0.3	0.6	pA/\sqrt{Hz}
		$f_O = 100Hz$ (Note 1)	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	
Input Voltage Range	IVR	$V+ = +5V, V- = 0V$	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	-15/13.5	—	—	-15/13.5	—	—	-15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	$V+ = +5V, V- = 0V,$ $0V \leq V_{CM} \leq +3.5V$	83	100	—	80	96	—	76	90	—	dB
		$V_S = \pm 15V,$ $-15V \leq V_{CM} \leq +13.5V$	83	100	—	80	96	—	76	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & $V- = 0V, V+ = 5V$ to $30V$	—	10	30	—	20	50	—	30	80	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$	200	400	—	100	200	—	100	200	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V, V- = 0V$ $R_L = 5k\Omega$	0.7/4.0	—	—	0.8/3.9	—	—	0.9/3.8	—	—	V
		$V_S = \pm 15V,$ $R_L = 10k\Omega$	± 14	—	—	± 13.9	—	—	± 13.8	—	—	
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0,$ $R_L = 10k\Omega$	1.0	1.9	—	1.0	1.9	—	1.0	1.9	—	MHz
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V, \text{No Load}$	—	0.6	1.0	—	0.7	1.5	—	0.9	2.0	mA
		$V_S = \pm 15V, \text{No Load}$	—	1.2	1.8	—	1.4	2.3	—	1.8	3.0	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/ μs
Channel Separation	CS	(Note 1)	100	120	—	100	120	—	100	120	—	dB

NOTES:

1. Sample tested.
2. Guaranteed by design.

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OPERATIONAL AMPLIFIERS



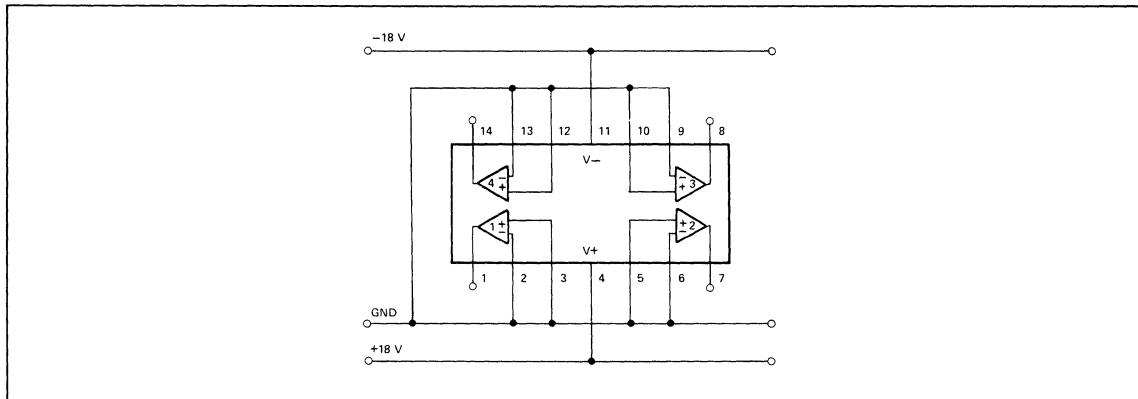
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-421B and OP-421C, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-421F and OP-421G, and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-421H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421B OP-421F			OP-421C OP-421G			OP-421H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	5	10	—	8	15	—	10	15	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1	3.5	—	1.8	5.5	—	3	7.5	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1.6	8	—	3.0	15	—	6.0	30	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	25	70	—	60	125	—	140	230	nA
Input Voltage Range	IVR	$V_+ = +5V, V_- = 0V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	-15/13.2	—	—	-15/13.2	—	—	-15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	$V_+ = +5V, V_- = 0V,$ $0V \leq V_{CM} \leq +3.2V$	78	96	—	74	94	—	73	86	—	dB
		$V_S = \pm 15V,$ $-15V \leq V_{CM} \leq +13.2V$	78	96	—	74	94	—	73	86	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & $V_- = 0V, V_+ = 5V$ to $30V$	—	15	50	—	25	80	—	40	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = 10V$ $R_L = 20k\Omega$	100	200	—	50	100	—	50	100	—	V/mV
		$V_+ = 5V, V_- = 0V$ $R_L = 10k\Omega$ $V_S = \pm 15V,$ $R_L = 20k\Omega$	0.8/3.9	—	—	0.9/3.8	—	—	1.0/3.7	—	—	
Output Voltage Swing	V_O	$V_+ = 5V, V_- = 0V$ $R_L = 10k\Omega$ $V_S = \pm 15V,$ $R_L = 20k\Omega$	± 13.8	—	—	± 13.7	—	—	± 13.7	—	—	V
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	1.2	1.5	—	1.5	2.0	—	2.0	3.0	mA
		$V_S = \pm 15V$, No Load	0.68	2.0	2.5	0.68	2.5	3.2	0.68	3.2	4.0	

NOTE:

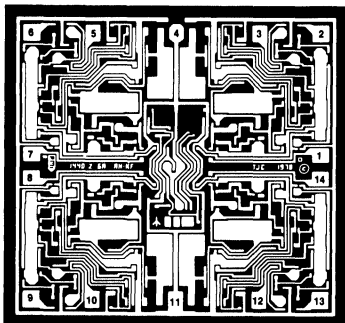
- 1. Sample tested.

BURN-IN CIRCUIT





DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.092 Inch, 7912 sq. mils
(2.34 × 2.18 mm, 5.10 sq. mm)

1. OUTPUT 1
2. INVERTING INPUT 1
3. NONINVERTING INPUT 1
4. V+
5. NONINVERTING INPUT 2
6. INVERTING INPUT 2
7. OUTPUT 2
8. OUTPUT 3
9. INVERTING INPUT 3
10. NONINVERTING INPUT 3
11. V-
12. NONINVERTING INPUT 4
13. INVERTING INPUT 4
14. OUTPUT 4

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

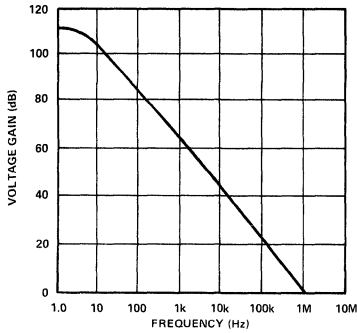
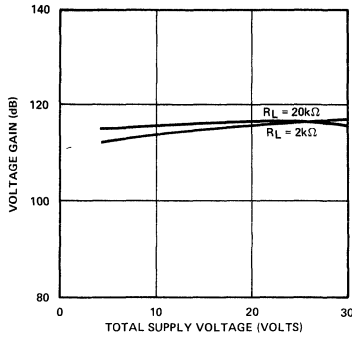
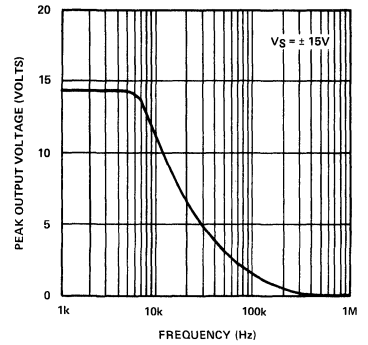
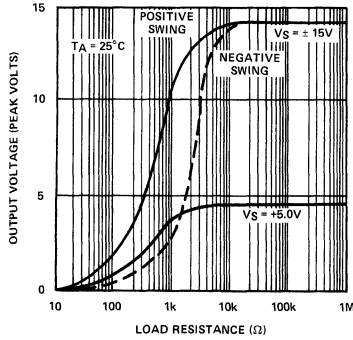
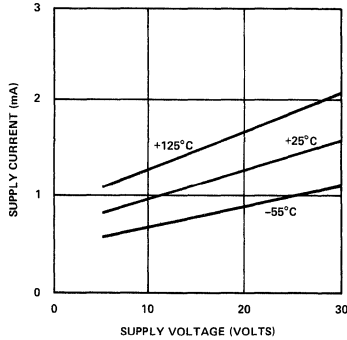
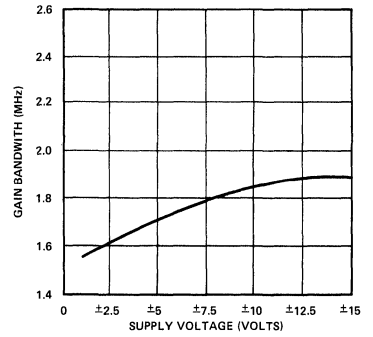
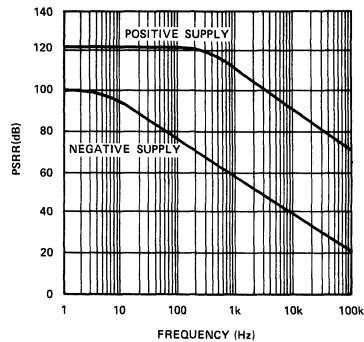
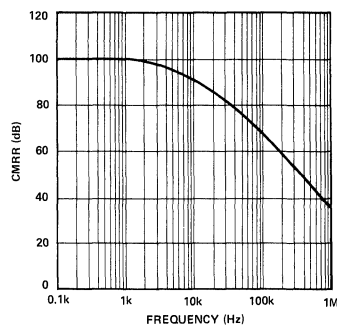
PARAMETER	SYMBOL	CONDITIONS	OP-421N LIMIT	OP-421G LIMIT	OP-421GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	2.5	4	6	mV MAX
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	5	10	20	nA MAX
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	50	80	150	nA MAX
Input Voltage Range	IVR		-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_+ = +5V$, $V_- = 0V$ $0V \leq V_{CM} \leq +3.5V$ $V_S = \pm 15V$, $-15V \leq V_{CM} \leq +13.5V$	83	80	76	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; and $V_- = 0V$, $V_+ = +5V$ to $30V$	30	50	80	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 20k\Omega$	200	200	100	V/mV MIN
Output Voltage Swing	V_O	$V_+ = +5V$, $V_- = 0V$, $R_L = 5k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.7/4.0 ± 14	0.8/3.9 ± 13.9	0.9/3.8 ± 13.8	V MIN
Supply Current (Four Amplifiers)	I_{SV}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	1.0 1.8	1.5 2.3	2.0 3.0	mA MAX

NOTE:

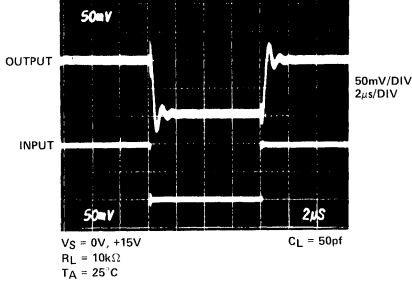
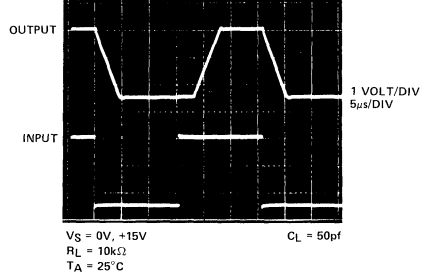
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

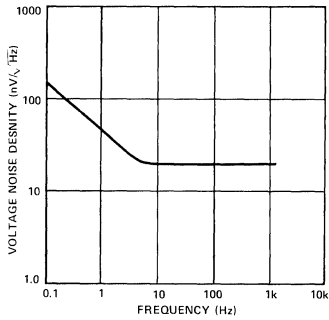
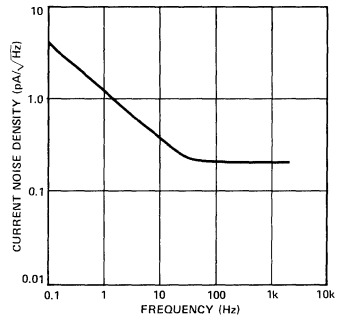
PARAMETER	SYMBOL	CONDITIONS	OP-421N TYPICAL	OP-421G TYPICAL	OP-421GR TYPICAL	UNITS
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$	20 15	20 15	20 15	nV/\sqrt{Hz}
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	1.9	1.9	1.9	MHz
Slew Rate	SR		0.5	0.5	0.5	V/ μs
Channel Separation	CS		120	120	120	dB

TYPICAL PERFORMANCE CHARACTERISTICS
**OPEN-LOOP
FREQUENCY RESPONSE**

**OPEN-LOOP GAIN
vs POWER SUPPLY VOLTAGE**

**OUTPUT SWING
vs FREQUENCY**

**OUTPUT SWING vs
OUTPUT LOAD**

**SUPPLY CURRENT vs
SUPPLY VOLTAGE**

**GAIN BANDWIDTH vs
SUPPLY VOLTAGE**

**POWER SUPPLY REJECTION
RATIO vs FREQUENCY**

**COMMON-MODE REJECTION
RATIO vs FREQUENCY**


TYPICAL PERFORMANCE CHARACTERISTICS

**VOLTAGE FOLLOWER
SMALL-SIGNAL RESPONSE**

**VOLTAGE FOLLOWER
LARGE-SIGNAL RESPONSE**


NOISE CHARACTERISTICS

**INPUT NOISE VOLTAGE
DENSITY vs FREQUENCY**

**INPUT NOISE CURRENT
DENSITY vs FREQUENCY**




PM-108A/PM-2108A

LOW-INPUT-CURRENT OPERATIONAL AMPLIFIERS

PM-108A/PM-208A/PM-308A/PM-108/PM-208/PM-308/PM-2108A/PM-2108

Precision Monolithics Inc.

FEATURES

- Low Offset Current 200pA Max
- Low Bias Current 2nA Max
- Low Power Consumption 18mW Max @ ±15V
- Wide Supply Range ±3V to ±20V
- High Power-Supply Rejection Ratio 96dB Min
- Low Offset Voltage Drift 5μV/°C Max
- High Common-Mode Input Range ±13.5V Min
- High Common-Mode Rejection Ratio 96dB Min
- MIL-STD-883 Processing Models Available
- Silicon-Nitride Passivation

GENERAL DESCRIPTION

The PM-108A series of precision operational amplifiers feature very low input offset and bias currents. Although

directly interchangeable with industry-standard types, Precision Monolithics' advanced processing provides the PM-108A series with a significant improvement in input noise voltage. Low supply current drain over a wide power-supply range makes the PM-108A attractive in battery operated and other low-power applications. The low bias current provides excellent performance with piezoelectric and capacitive transducers and in such high-impedance circuits as long-period integrators and sample-and-holds. For improved performance see OP-08, OP-12, OP-20, OP-21, and OP-22.

The PM-2108A contains two superbeta, PM-108A op amps in a single 16-pin DIP. Compared to the single PM-108A types, this model offers higher packaging density, closer thermal tracking between the two amplifiers, and reduced insertion cost.

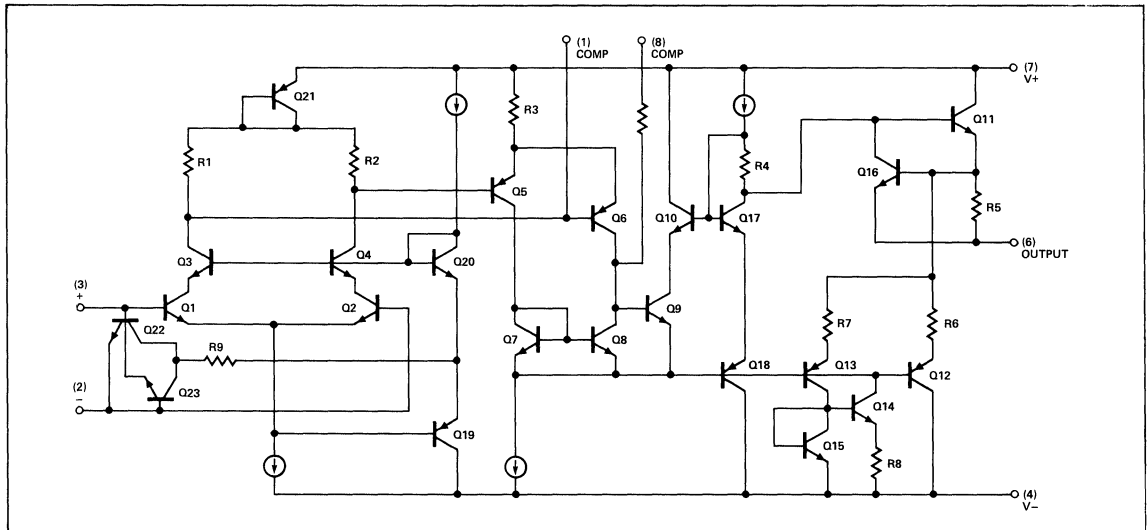
ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (mV)	PACKAGE					OPERATING TEMPERATURE RANGE
	HERMETIC			PLASTIC DIP 8-PIN	LCC	
	TO-99 8-PIN	DIP				
		8-PIN	16-PIN			
0.5	PM108AJ*	PM108AZ*	PM2108AQ*		PM108ARC/883	MIL
0.5	PM208AJ	PM208AZ				IND
0.5	PM308AJ	PM308AZ		PM308AP		COM
2.0	PM108J*	PM108Z*	PM2108Q*			MIL
2.0	PM208J	PM208Z				IND
7.5	PM308J	PM308Z				COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

SIMPLIFIED SCHEMATIC (Pin numbers for PM-108 only. Circuit is 1/2 2108.)





ABSOLUTE MAXIMUM RATINGS

Supply Voltage
 PM-108A, PM-108, PM-208A, PM-208,
 PM-2108A, PM-2108, PM-108ARC $\pm 20V$
 PM-308A, PM-308 $\pm 18V$
 Internal Power Dissipation (Note 1) 500mW
 Differential Input Current (Note 2) $\pm 10mA$
 Input Voltage (Note 3) $\pm 15V$
 Output Short-Circuit Duration Indefinite
 Operating Temperature Range
 PM-108A, PM-108, PM-2108A,
 PM-2108, PM-108ARC $-55^{\circ}C$ to $+125^{\circ}C$
 PM-208A, PM-208 $-25^{\circ}C$ to $+85^{\circ}C$
 PM-308A, PM-308 $0^{\circ}C$ to $+70^{\circ}C$
 Storage Temperature Range
 (Q-, J-, Z- or ARC-Package) $-65^{\circ}C$ to $+150^{\circ}C$
 (P-Package) $-65^{\circ}C$ to $+125^{\circ}C$
 Lead Temperature Range (Soldering, 60 sec) $300^{\circ}C$

NOTES:

1. Maximum package power dissipation vs. ambient temperature.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
Plastic 8-Pin DIP (P)	36°C	5.6mW/°C
Hermetic 8-Pin DIP (Z)	75°C	6.7mW/°C
Hermetic 16-Pin DIP (Q)	100°C	10.0mW/°C
LCC (RC)	80°C	7.8mW/°C

2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.
 3. For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at $\pm 5V \leq V_S \leq \pm 20V$ and $T_A = 25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-108A/PM-2108A PM-208A			PM-108/PM-2108 PM-208			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	0.7	2.0	mV
Input Offset Current	I_{OS}		—	0.05	0.2	—	0.05	0.2	nA
Input Bias Current	I_B		—	0.8	2.0	—	0.8	2.0	nA
Input Resistance	R_{IN}	(Note 1)	30	70	—	30	70	—	MΩ
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_{OUT} = \pm 10V, R_L \geq 10k\Omega$	80	300	—	50	300	—	V/mV
Supply Current	I_{SY}	$I_{OUT} = 0, V_{OUT} = 0, \text{ Each Amplifier}$	—	0.3	0.6	—	0.3	0.6	mA

ELECTRICAL CHARACTERISTICS at $\pm 5V \leq V_S \leq \pm 20V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$ for PM-108A, PM-108, PM-2108A and PM-2108, $-25^{\circ}C \leq T_A \leq +85^{\circ}C$ for PM-208A, PM-208, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-108A/PM-2108A PM-208A			PM-108/PM-2108 PM-208			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.4	1.0	—	1.0	3.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 2)	—	1	5	—	3	15	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}		—	0.1	0.4	—	0.1	0.4	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	0.5	2.5	—	0.5	2.5	$pA/^{\circ}C$
Input Bias Current	I_B		—	1	3	—	1	3	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_{OUT} = \pm 10V, R_L \geq 10k\Omega$	40	200	—	25	200	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V, R_L = 10k\Omega$	± 13	± 14	—	± 13	± 14	—	V
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13.5	—	—	± 13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V, V_{CM} = \pm 13.5V$	96	110	—	85	100	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$	—	3	15	—	15	100	$\mu V/V$
Supply Current	I_{SY}	$V_{OUT} = 0, T_A = \text{MAX}, \text{ Each Amplifier}$	—	0.15	0.4	—	0.15	0.4	mA

NOTES:

1. Guaranteed by input bias current.
 2. Sample tested.

**ELECTRICAL CHARACTERISTICS** at $\pm 5V \leq V_S \leq \pm 20V$ and $T_A = 25^\circ C$, unless otherwise noted.

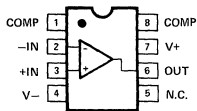
PARAMETER	SYMBOL	CONDITIONS	PM-308A			PM-308			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	2.0	7.5	mV
Input Offset Current	I_{OS}		—	0.2	1.0	—	0.2	1.0	nA
Input Bias Current	I_B		—	1.5	7.0	—	1.5	7.0	nA
Input Resistance	R_{IN}	(Note 1)	10	40	—	10	40	—	M Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_{OUT} = \pm 10V,$ $R_L \geq 10k\Omega$	80	300	—	25	300	—	V/mV
Supply Current	I_{SV}	$I_{OUT} = 0, V_{OUT} = 0,$ Each Amplifier	—	0.3	0.8	—	0.3	0.8	mA

ELECTRICAL CHARACTERISTICS at $\pm 5V \leq V_S \leq \pm 15V$ and $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

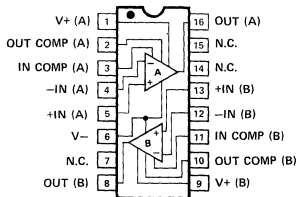
PARAMETER	SYMBOL	CONDITIONS	PM-308A			PM-308			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.4	0.73	—	3.0	10.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	1	5	—	6	30	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	1.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	2	10	—	2	10	$\mu A/^\circ C$
Input Bias Current	I_B		—	2	10	—	2	10	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_{OUT} = \pm 10V,$ $R_L \geq 10k\Omega$	60	200	—	15	100	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V, R_L = 10k\Omega$	± 13	± 14	—	± 13	± 14	—	V
Input Voltage Range	IVR	$V_S = \pm 15V$	± 14	—	—	± 13	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	96	110	—	80	100	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	3	15	—	15	100	$\mu V/V$
Supply Current	I_{SV}	$V_{OUT} = 0, T_A = MAX,$ Each Amplifier	—	0.23	—	—	0.23	—	mA

NOTE:

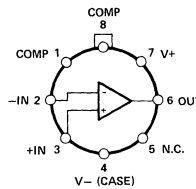
- Guaranteed by input bias current.

PIN CONNECTIONS

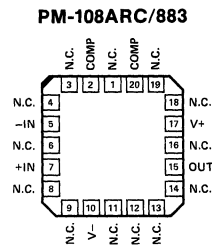
**EPOXY MINI-DIP
(P-Suffix)
AND
8-PIN HERMETIC DIP
(Z-Suffix)**



**16-PIN HERMETIC DIP
(Q-Suffix)**



**TO-99
(J-Suffix)**



**LCC PACKAGE
(RC-Suffix)**

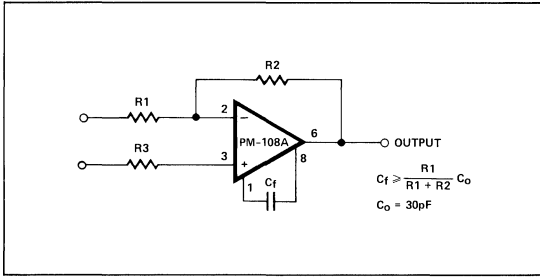
APPLICATIONS INFORMATION

The PM-108A series has very low input offset and bias currents; the user is cautioned that printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to achieve the PM-108A's

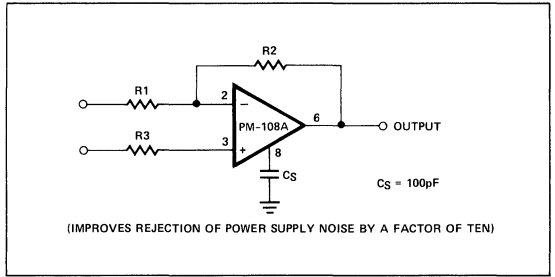
rated performance. It is suggested that board leakage be minimized by encircling the input pins with a guard ring maintained at a potential close to that of the inputs. The guard ring should be driven by a low impedance source such as an amplifier's output or ground.

COMPENSATION CIRCUITS

STANDARD



ALTERNATE





PM-146/PM-246

PROGRAMMABLE QUAD
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Wide Supply Range $\pm 1.2V$ to $\pm 22V$
- Programmable Operation
Supply Current (per Amplifier) $3.5\mu A$ to $1.75mA$
Gain-Bandwidth Product $10kHz$ to $4MHz$
- High Gain $100dB$ Min*
- Low Noise $28nV/\sqrt{Hz}$ Typ*
- High Power-Supply Rejection $80dB$ Min*
- Excellent Channel Separation $120dB$ Typ*

* At $I_{SET} = 10\mu A$.

CROSS REFERENCE

PMI	NATIONAL	EXAR
PM146Q	LM146J	XR-146M
PM246Q	LM246J	XR-246N

ORDERING INFORMATION†

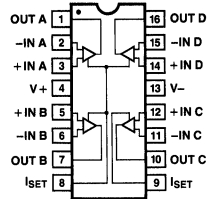
$T_A = 25^\circ C$ V_{OS} MAX (mV)**	CERAMIC DIP PACKAGE	OPERATING TEMPERATURE RANGE
5	PM146Q*	MIL
6	PM246Q	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

** At $I_{SET} = 10\mu A$.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

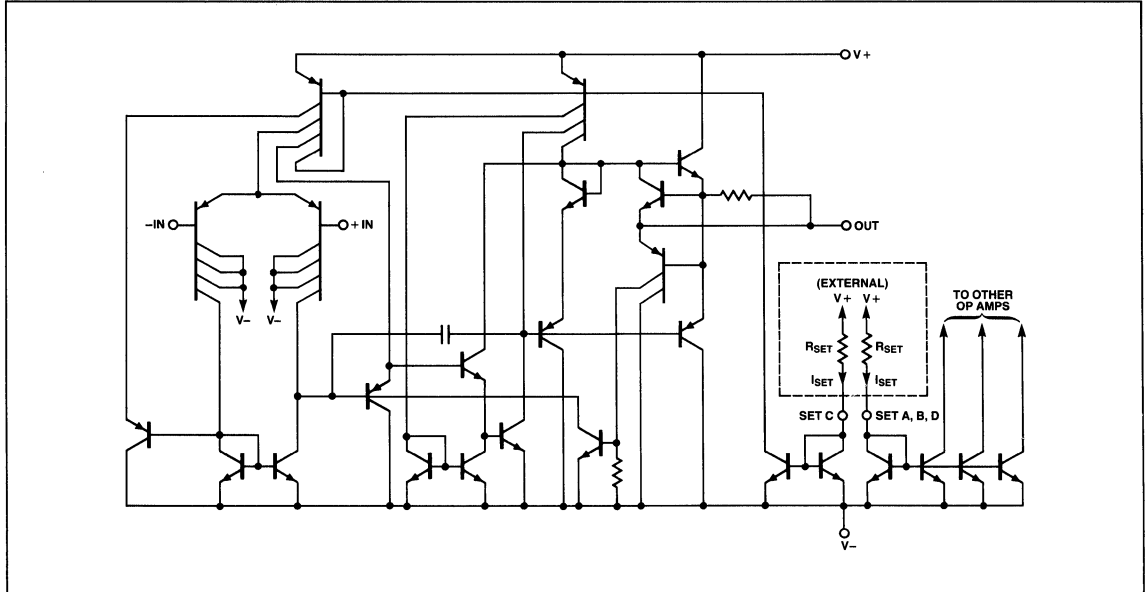
PIN CONNECTIONS



16-PIN CERAMIC DIP
(Q-Suffix)

16-PIN EPOXY DIP
(P-Suffix)

SIMPLIFIED SCHEMATIC



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**GENERAL DESCRIPTION**

The PM-146 monolithic quad operational amplifier incorporates four independent programmable low-power amplifiers. Using two external resistors, the supply currents may be programmed for the optimal combination of bias and offset currents, gain-bandwidth product, slew rate, input noise, and output currents. By means of this capability, the user can achieve the required level of speed and performance while maintaining the minimum possible power consumption.

Gain-bandwidth products of 2MHz with slew rates of $1V/\mu s$, at a supply current drain of 1mA per amplifier, are achieved using a programming ("set") current of $30\mu A$. At the other end of the spectrum, bias currents of 1nA at a supply drain of only $3.5\mu A$ per amplifier are obtained with a set current of $0.1\mu A$ for applications where speed is not important.

The PM-146 operates with a supply voltage down to $\pm 1.5V$, which makes the amplifier well-suited to applications utilizing battery or solar-cell supplies. Since speed is controlled by the programming current, the slew rate and gain-bandwidth of the PM-146 remain relatively unchanged with varying supply voltages. The extreme versatility afforded by the PM-146's programmability allows the device to be tailored to a wide variety of applications, including active filters, oscillators, and general-purpose amplifiers.

The pin configuration of the PM-146 matches the OP-11 pin-out, with the addition of the two programming pins on one end. These pins are internally protected to survive a momentary short to the power supply rails.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{SET} = 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-146Q			PM-246Q			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 50\Omega$ (Note 1)	—	0.5	5	—	0.5	6	mV
Input Offset Current	I_{OS}	(Note 1)	—	2	20	—	2	100	nA
Input Bias Current	I_B	(Note 1)	—	50	100	—	50	250	nA
Supply Current (4 Op Amps)	I_{SY}		—	1.4	2.0	—	1.4	2.5	mA
Open Loop Voltage Gain	A_{VO}	$R_L = 10k\Omega$, $\Delta V_{OUT} = \pm 10V$	100	1000	—	50	1000	—	V/mV
Input Voltage Range	IVR	(Note 2)	± 13.5	± 14	—	± 13.5	± 14	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$, $R_S \leq 10k\Omega$	80	100	—	70	100	—	dB
Power-Supply Rejection	PSR	$R_S \leq 10k\Omega$	80	100	—	74	100	—	dB
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 14	—	± 12	± 14	—	V
Short-Circuit Output Current	I_{SC}		5	20	35	5	20	35	mA
Gain-Bandwidth Product	GBW		0.8	1.2	—	0.5	1.2	—	MHz
Phase Margin	ϕ_o		—	60	—	—	60	—	Degrees
Slew Rate	SR		—	0.4	—	—	0.4	—	$V/\mu s$
Input Noise Voltage Density	e_n	$f = 1kHz$	—	28	—	—	28	—	nV/\sqrt{Hz}
Channel Separation	CS	$R_L = 10k\Omega$, $\Delta V_{OUT} = 0V$ to $\pm 12V$	—	120	—	—	120	—	dB
Input Resistance	R_{IN}		—	1.0	—	—	1.0	—	M Ω
Input Capacitance	C_{IN}		—	2.0	—	—	2.0	—	pF

NOTES:

- $V_{CM} = 0V$.
- Guaranteed by CMR test.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{SET} = 10\mu A$, $-55^\circ C \leq T_A \leq +125^\circ C$ for PM-146Q, $-25^\circ C \leq T_A \leq +85^\circ C$ for PM-246Q, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-146Q			PM-246Q			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 50\Omega$ (Note 1)	—	0.5	6	—	0.5	7.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	2	25	—	2	100	nA
Input Bias Current	I_B	(Note 1)	—	50	100	—	50	250	nA
Supply Current (4 Op Amps)	I_{SY}		—	1.5	2.0	—	1.5	2.5	mA
Open Loop Voltage Gain	A_{VO}	$R_L = 10k\Omega$, $\Delta V_{OUT} = \pm 10V$	50	1000	—	25	1000	—	V/mV
Input Voltage Range	IVR	(Note 2)	± 13.5	± 14	—	± 13.5	± 14	—	V
Common-Mode Rejection	CMR	$R_S \leq 50\Omega$ $V_{CM} = \pm 13.5V$	70	100	—	70	100	—	dB
Power-Supply Rejection	PSR	$R_S \leq 50\Omega$	76	100	—	74	100	—	dB
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 14	—	± 12	± 14	—	V

NOTES:

- $V_{CM} = 0V$.
- Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{SET} = 1\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-146Q			PM-246Q			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 50\Omega$ (Note 1)	—	0.5	5	—	0.5	7	mV
Input Bias Current	I_B	(Note 1)	—	7.5	20	—	7.5	100	nA
Supply Current (4 Op Amps)	I_{SY}		—	140	250	—	140	300	μA
Gain-Bandwidth Product	GBW		80	100	—	50	100	—	kHz

NOTE:

- $V_{CM} = 0V$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$, $I_{SET} = 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-146Q			PM-246Q			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 50\Omega$ (Note 1)	—	0.5	5	—	0.5	7	mV
Input Voltage Range	IVR	(Note 2)	± 0.7	—	—	± 0.7	—	—	V
Common-Mode Rejection	CMR	$R_S \leq 50\Omega$ $V_{CM} = \pm 0.7V$	—	80	—	—	80	—	dB
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 0.6	—	—	± 0.6	—	—	V

NOTES:

- $V_{CM} = 0V$.
- Guaranteed by CMR test.



PM-155A/PM-156A/PM-157A

MONOLITHIC JFET-INPUT
OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

LOW SUPPLY CURRENT — PM-155A/PM-355A/PM-155
GENERAL PURPOSE — PM-156A/PM-356A/PM-156
WIDE-BANDWIDTH — PM-157A/PM-357A/PM-157

FEATURES

All Devices

- Low Input Bias and Offset Currents
- Low Input Offset Voltage 1.0mV
- Low Input Offset Voltage Drift $3.0\mu\text{V}/^\circ\text{C}$
- Low Input Noise Current $0.01\text{pA}/\sqrt{\text{Hz}}$
- High Common-Mode Rejection Ratio 100dB

- PM-155 (Only) LF155 Replacement
- Low Supply Current 2mA

- PM-156 (Only) LF156 Replacement
- High Slew Rate $12\text{V}/\mu\text{sec}$
- Fast Settling to $\pm 0.01\%$ 4.0 μsec

- PM-157 (Only) LF157 Replacement
- Wide-Bandwidth Decompensated ($A_{VCL} = 5 \text{ Min}$) ... 20MHz
- High Slew Rate $45\text{V}/\mu\text{sec}$
- Fast Settling to $\pm 0.01\%$ 4.0 μsec

GENERAL DESCRIPTION

The PM JFET-input series provides low input current, high slew rate, and direct interchangeability with LF155, 156, and 157 types. These operational amplifiers use a new process which allows fabrication of matched JFET transistors and standard bipolar transistors on the same chip. High accuracy and low cost make the PM JFET-input series useful in new designs and as replacements for modular and hybrid types. Unlike many designs, nulling the input offset voltage does not degrade common-mode rejection ratio or input offset voltage drift. Low input voltage noise and current noise plus a low 1/f noise corner frequency allow these amplifiers to be used in a variety of low noise, wide-bandwidth applications.

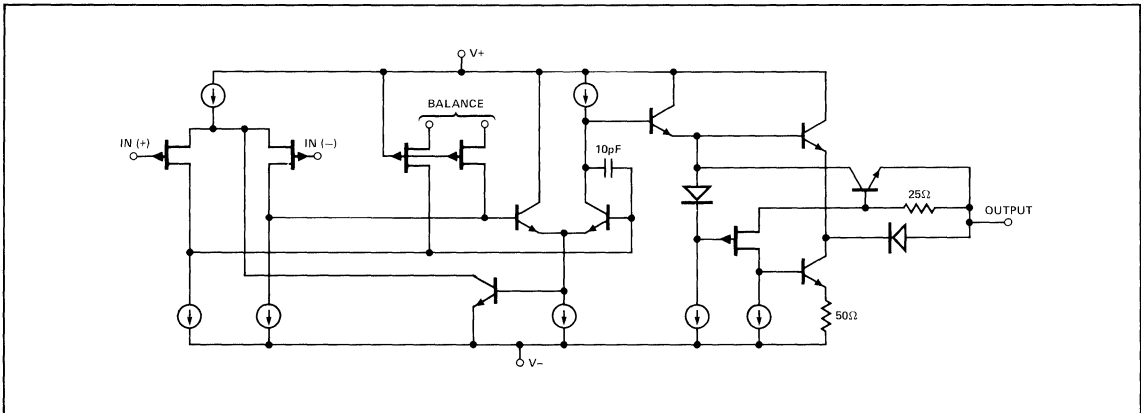
Dynamic specifications for the PM-155 include a slew rate of $5\text{V}/\mu\text{s}$, a 2.5MHz gain bandwidth product, and settling time to within $\pm 0.01\%$ of final value in 5.0 μs . The PM-156 has a slew rate of $12\text{V}/\mu\text{s}$ and a settling time of 4.0 μs to $\pm 0.01\%$ of final value.

The PM-157 is a very fast decompensated device. This results in a $45\text{V}/\mu\text{s}$ slew rate, a 20MHz gain bandwidth product, and a settling time of 4.0 μs . Decompensation requires a minimum closed-loop gain of five because of stability considerations.

For improved performance, see the OP-15/OP-16/OP-17 data sheet. For duals, see the OP-215 data sheet.

5
OPERATIONAL AMPLIFIERS

SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS

Supply Voltage
 PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157,
 PM-355A, PM-356A, PM-357A ±22V

Internal Power Dissipation
 PM-155A, PM-156A, PM-157, PM-155, PM-156,
 PM-157 670mW
 PM-355A, PM-356A, PM-357A 500mW
 (Derate based on a thermal resistance of 150°C/W
 junction to ambient or 45°C/W junction to case.)

Operating Temperature Range
 PM-155A, PM-156A, PM-157A, PM-155, PM-156,
 PM-157 -55°C to +125°C
 PM-355A, PM-356A, PM-357A 0°C to +70°C

Maximum Junction Temperature (T_j)
 PM-155A, PM-156A, PM-157A, PM-155, PM-156,
 PM-157 +150°C
 PM-355A, PM-356A, PM-357A +100°C

Differential Input Voltage
 PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157,
 PM-355A, PM-356A, PM-357A ±40V

Input Voltage
 PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157,
 PM-355A, PM-356A, PM-357A ±20V

NOTE:
 The absolute maximum negative input voltage is equal to the negative power supply voltage.

Output Short-Circuit Duration Indefinite
 Storage Temperature Range -65°C to +150°C
 Lead Temperature Range (Soldering, 60 sec) +300°C

ELECTRICAL CHARACTERISTICS at ±15V ≤ V_S ≤ ±20V, -55°C ≤ T_A ≤ +125°C and T_{HIGH} = +125°C for PM-155A, PM-156A and PM-157A, 0°C ≤ T_A ≤ +70°C and T_{HIGH} = +70°C for PM-355A, PM-356A and PM-357A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155A/ PM-156A/ PM-157A			PM-355A/ PM-356A/ PM-357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S = 50Ω	—	1.4	2.5	—	1.2	2.3	mV
Input Offset Voltage Drift	TCV _{OS}	R _S = 50Ω	—	3	5	—	3	5	μV/°C
Change in Input Offset Drift with V _{OS} Adjust	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	R _S = 50Ω	—	0.5	—	—	0.5	—	μV/°C per mV
Input Offset Current	I _{OS}	T _j ≤ T _{HIGH} (Note 1)	—	4.0	10	—	0.4	1.0	nA
Input Bias Current	I _B	T _j ≤ T _{HIGH} (Note 1)	—	±10	±25	—	±2	±5	nA
Large-Signal Voltage Gain	A _{VO}	V _S = ±15V, V _O = ±10V, R _L = 2kΩ	25	75	—	25	75	—	V/mV
Output Voltage Swing	V _O	V _S = ±15V, R _L = 10kΩ	±12	±13	—	±12	±13	—	V
		V _S = ±15V, R _L = 2kΩ	±10	±12	—	±10	±12	—	
Input Voltage Range	IVR	V _S = ±15V	±10.4	+15.1 -12.0	—	±10.4	+15.1 -12.0	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±IVR	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	—	10	57	μV/V

- NOTES:**
- PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at V_{CM} = 0.
 - Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

**ELECTRICAL CHARACTERISTICS** at $\pm 15V \leq V_S \leq \pm 20V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		PM-155A/ PM-156A/ PM-157A			PM-355A/ PM-356A/ PM-357A			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	1	2	—	1	2	mV
Input Offset Current	I_{OS}	$T_J = 25^\circ C$ (Note 1)		—	3	10	—	3	10	pA
Input Bias Current	I_B	$T_J = 25^\circ C$ (Note 1)		—	± 30	± 50	—	± 30	± 50	pA
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$		50	200	—	50	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm 15V$	PM-155	—	2	4	—	2	4	mA
			PM-156/PM-157	—	5	7	—	5	7	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	3	5	—	3	5	—	V/ μs
			PM-156	10	12	—	10	12	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	40	45	—	40	45	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	—	2.5	—	—	2.5	—	MHz
			PM-156	4.0	4.5	—	4.0	4.5	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	15	20	—	15	20	—	
Settling Time (to $\pm 0.01\%$)	t_S	$V_S = \pm 15V$ (Note 2)	PM-155	—	5.0	—	—	4.0	—	μs
			PM-156	—	4.0	—	—	1.5	—	
		$V_S = \pm 15V$ (Note 3)	PM-157	—	4.0	—	—	1.5	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, $f = 100Hz$	PM-155	—	25	—	—	25	—	nV/\sqrt{Hz}
		$R_S = 100\Omega$, $f = 1000Hz$		—	20	—	—	20	—	
		$R_S = 100\Omega$, $f = 100Hz$	PM-156/PM-157	—	15	—	—	15	—	
		$R_S = 100\Omega$, $f = 1000Hz$		—	12	—	—	12	—	
Input Noise Current	i_n	$f = 100Hz$, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	pA/\sqrt{Hz}
		$f = 1000Hz$, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}			—	3	—	—	3	—	pF

NOTES:

- PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Settling time is defined here for a unity gain inverter connection using $2k\Omega$ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
- Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

**ELECTRICAL CHARACTERISTICS** at $T_A = +25^\circ\text{C}$, $\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$ for PM-155, PM-156 and PM-157, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155 PM-156 PM-157			UNITS	
			MIN	TYP	MAX		
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	3	5	mV	
Input Offset Current	I_{OS}	$T_j = 25^\circ\text{C}$ (Note 1)	—	3	20	pA	
Input Bias Current	I_B	$T_j = 25^\circ\text{C}$ (Note 1)	—	± 30	± 100	pA	
Input Resistance	R_{IN}		—	10^{12}	—	Ω	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	50	200	—	V/mV	
Supply Current	I_{SY}	$V_S = \pm 15\text{V}$	PM-155	—	2	4	mA
			PM-156/PM-157	—	5	7	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15\text{V}$	PM-155	—	5	—	V/ μs
		$A_{VCL} = +5$, $V_S = \pm 15\text{V}$	PM-156 PM-157	7.5 30	12 40	— —	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15\text{V}$	PM-155	—	2.5	—	MHz
			PM-156	—	5	—	
			PM-157	—	20	—	
Settling Time (to $\pm 0.01\%$)	t_S	$V_S = \pm 15\text{V}$ (Note 2)	PM-155	—	5	—	μs
			PM-156	—	4	—	
			PM-157	—	4	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, $f = 100\text{Hz}$	PM-155	—	25	—	$\text{nV}/\sqrt{\text{Hz}}$
		$R_S = 100\Omega$, $f = 1000\text{Hz}$		—	20	—	
		$R_S = 100\Omega$, $f = 100\text{Hz}$	PM-156/PM-157	—	15	—	
		$R_S = 100\Omega$, $f = 1000\text{Hz}$		—	12	—	
Input Noise Current	i_n	$f = 100\text{Hz}$, $V_S = \pm 15\text{V}$ $f = 1000\text{Hz}$, $V_S = \pm 15\text{V}$	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$	
Input Capacitance	C_{IN}		—	3	—	pF	

NOTES:

- PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Settling time is defined here for a unity gain inverter connection using $2\text{k}\Omega$ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
- Settling time is defined here for a $A_V = -5$ connection with $R_F = 2\text{k}\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.



ELECTRICAL CHARACTERISTICS at $\pm 15V \leq V_S \leq \pm 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$ and $T_{HIGH} = +125^\circ C$ for PM-155, PM-156 and PM-157, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155 PM-156 PM-157			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	4	7	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	5	—	$\mu V/^\circ C$
Change In Input Offset Drift With V_{OS} Adjust.	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	$R_S = 50\Omega$	—	0.5	—	$\mu V/^\circ C$ per mV
Input Offset Current	I_{OS}	$T_J \leq T_{HIGH}$ (Note 1)	—	8	20	nA
Input Bias Current	I_B	$T_J \leq T_{HIGH}$ (Note 1)	—	± 2	± 50	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 2k\Omega$	25	75	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V, R_L = 10k\Omega$ $V_S = \pm 15V, R_L = 2k\Omega$	± 12 ± 10	± 13 ± 12	—	V
Input Voltage Range	IVR	$V_S = \pm 15V$	± 10.4	+15.1 -12.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	$\mu V/V$

NOTES:

- PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0, T_J = +125^\circ C$.
- Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

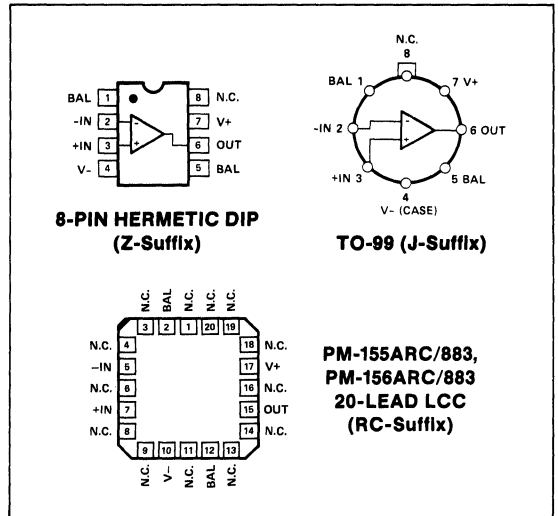
ORDERING INFORMATION†

$T_A = 25^\circ C$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	8-PIN HERMETIC DIP	LCC	
2.0	PM155AJ*	PM155AZ*	PM155ARC/883	MIL
	PM156AJ*	PM156AZ*	PM156ARC/883	
	PM157AJ*	PM157AZ*		
2.0	PM355AJ	PM355AZ		COM
	PM356AJ	PM356AZ		
	PM357AJ	PM357AZ		
5.0	PM155J*	PM155Z		MIL
	PM156J*	PM156Z		
	PM157J*	PM157Z		

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

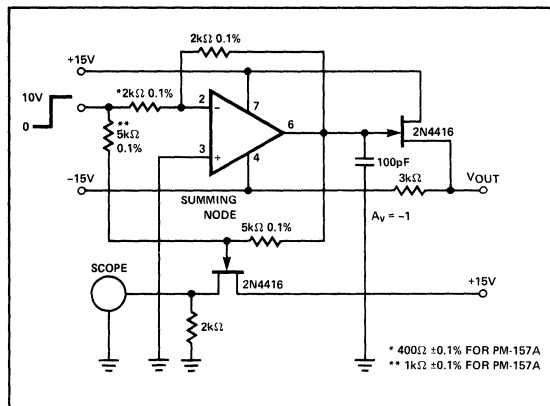
PIN CONNECTIONS



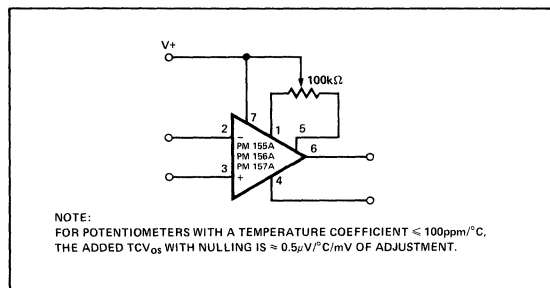
5
OPERATIONAL AMPLIFIERS

BASIC CONNECTIONS

SETTLING-TIME TEST CIRCUIT



INPUT OFFSET VOLTAGE NULLING



APPLICATIONS INFORMATION

INPUT VOLTAGE CONSIDERATIONS

The PM series JFET input stages can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than V_- can result in a destroyed unit.

If both inputs exceed the negative common-mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common-mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common-mode voltage range.

Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

POWER SUPPLY CONSIDERATIONS

Power supply polarity reversal can result in a destroyed unit.

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input. This minimizes "pick-up" and increases the frequency of the feedback pole by minimizing the capacitance from input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device to AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain. Consequently, the pole has negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the inverting input of the op amp. The capacitor value should be such that the RC time constant of the capacitor and feedback resistor is greater than, or equal to, the original feedback-pole time constant.



PM-725

INSTRUMENTATION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Extremely High Gain 3M Typ
- Low Offset Voltage and Offset Current
- Low Drift with Temperature
- High Common-Mode Rejection 110dB Min
- High Power Supply Rejection 10 μ V/V Max
- Silicon-Nitride Passivation
- Differential-Input Overvoltage Protection

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (mV)	PACKAGE			
	HERMETIC		PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	DIP 8-PIN		
1.0	PM725J*	PM725Z*	PM725CP	MIL COM
2.5	PM725CJ	PM725CZ		

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

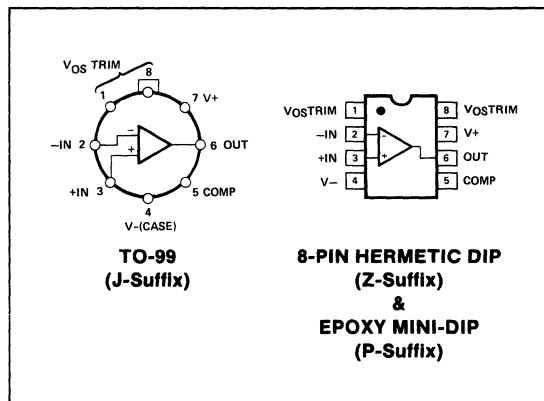
†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

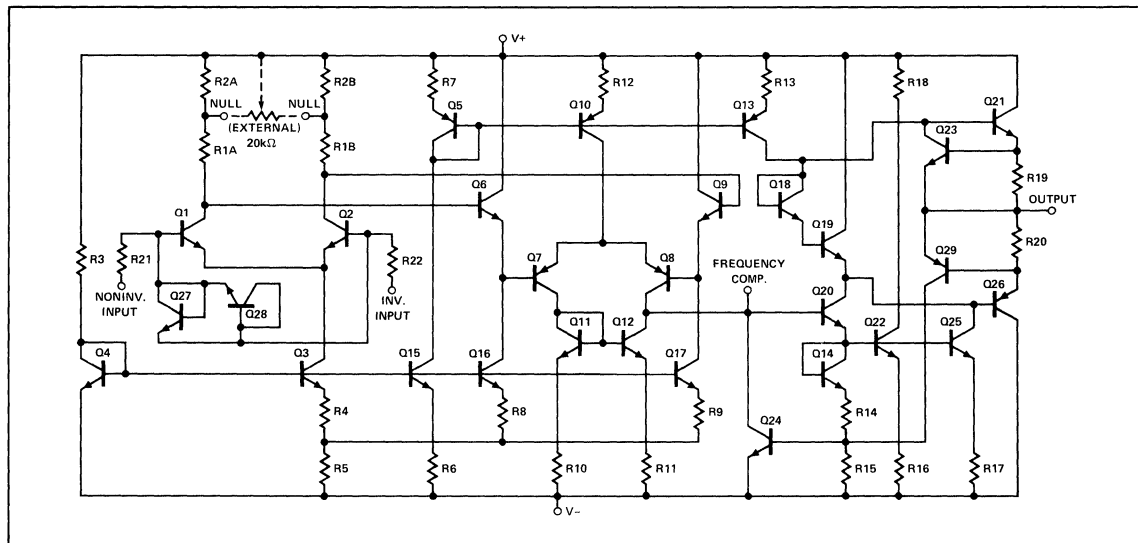
The PM-725 series of monolithic instrumentation operational amplifiers provide industry-standard 725 specifications. In

addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process minimizes "popcorn noise" and provides maximum reliability and long-term stability. For improved specifications, refer to the OP-06 series data sheet. For devices with internal frequency compensation, refer to the OP-05 instrumentation amplifier and OP-07 ultra-low offset voltage operational amplifier data sheets.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



5
OPERATIONAL AMPLIFIERS

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	±22V
Internal Power Dissipation (see note)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J and Z Packages	-65° C to +150° C
P Package	-65° C to +125° C
Operating Temperature Range	
PM-725	-55° C to +125° C

PM-725C 0° C to +70° C
 Lead Temperature Range (Soldering, 60 sec) 300° C

NOTE:

1. See table for maximum ambient temperature rating and derating factor.

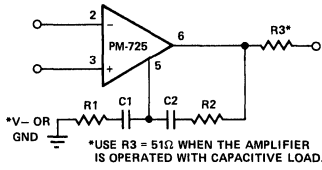
PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Plastic DIP (P)	36° C	5.6mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-725			PM-725C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.5	1.0	—	0.5	2.5	mV
Input Offset Current	I_{OS}		—	2	20	—	2	35	nA
Input Bias Current	I_B		—	42	100	—	42	125	nA
Input Noise Voltage	e_n	$f_O = 10Hz$	—	15	—	—	15	—	nV/\sqrt{Hz}
		$f_O = 100Hz$	—	9	—	—	9	—	
		$f_O = 1000Hz$	—	8	—	—	8	—	
Input Resistance	R_{IN}		—	1.5	—	—	1.5	—	MΩ
Input Voltage Range	IVR		±13.5	±14	—	±13.5	±14	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1,000	3,000	—	250	3,000	—	V/mV
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, $V_{CM} = \pm 13.5V$	110	120	—	94	120	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$, $V_S = \pm 5V$ to $\pm 15V$	—	2	10	—	2	35	$\mu V/V$
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.0	±13.5	—	±12.0	±13.5	—	V
		$R_L \geq 2k\Omega$	±10.0	±13.5	—	±10.0	±13.5	—	
Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	150	—	—	150	—	Ω
Power Consumption	P_d	No Load	—	80	105	—	80	150	mW



COMPENSATION CIRCUIT



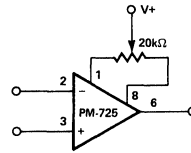
COMPENSATION COMPONENT VALUES

A _v	R ₁ (Ω)	C ₁ (μF)	R ₂ (Ω)	C ₂ (μF)
10,000	10k	50pF		
1,000	470	0.001		
100	47	0.01		
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

*FOR MAXIMUM PSRR VS FREQUENCY COMPENSATION NETWORK SHOULD BE RETURNED TO V-

PINOUTS FOR J, Z, AND P PACKAGES.

OFFSET VOLTAGE NULL CIRCUIT



PINOUTS FOR J, Z, AND P PACKAGES.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for PM-725, $0^\circ C \leq T_A \leq +70^\circ C$ for PM-725C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-725			PM-725C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	—	1.5	—	—	3.5	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$, Unnulled (Note 1)	—	2	5	—	2	—	$\mu V/^\circ C$
Average Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, Nulled	—	0.6	—	—	0.6	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$T_A = MAX$ $T_A = MIN$	—	1.2	20	—	1.2	35	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	35	150	—	10	—	$\mu A/^\circ C$
Input Bias Current	I_B	$T_A = MAX$ $T_A = MIN$	—	20	100	—	30	125	nA
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $T_A = MAX$ $R_L \geq 2k\Omega$, $T_A = MIN$	1,000	—	—	125	—	—	V/mV
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, $V_{CM} = \pm 13.5V$	100	—	—	—	115	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$, $V_S = \pm 5V$ to $\pm 15V$	—	—	20	—	20	—	$\mu V/V$
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 10	—	—	± 10	—	—	V

NOTE: 1. Sample tested.



PM-741

COMPENSATED OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Industry Standard 741 Specifications
- Internal Frequency Compensation
- Continuous Short-Circuit Protection
- Silicon-Nitride Passivation
- Low Noise

ORDERING INFORMATION†

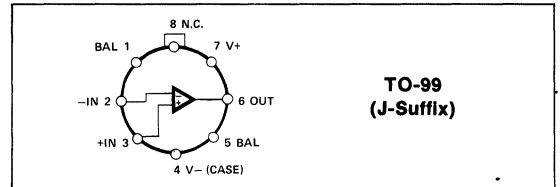
$T_A = 25^\circ\text{C}$ $V_{OS} \text{ MAX}$ (mV)	PACKAGE TO-99 8-PIN	OPERATING TEMPERATURE RANGE
5.0	PM741J	MIL
6.0	PM741CJ	COM

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

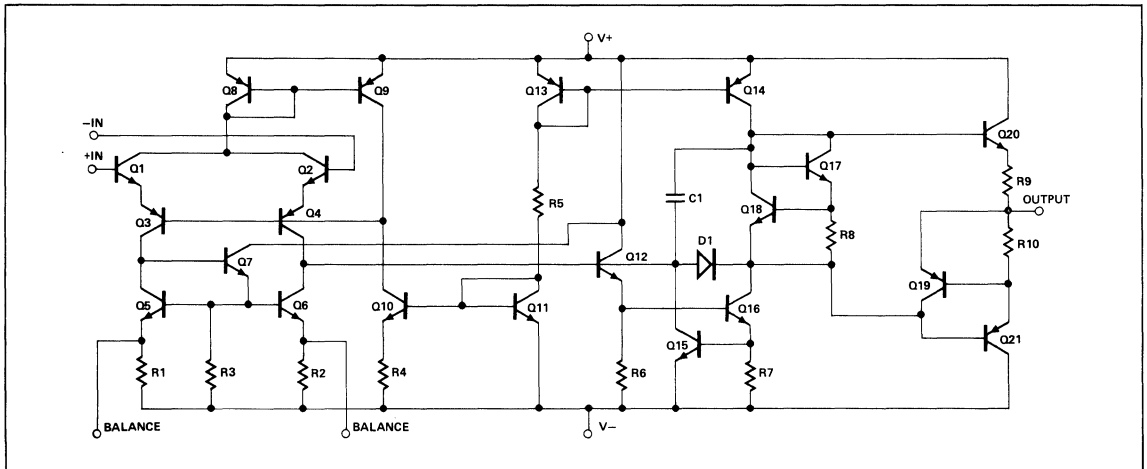
GENERAL DESCRIPTION

The PM-741 series of internally-compensated operational amplifiers provide industry-standard 741 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process provides high reliability and long-term stability of parameters. For higher performance general purpose op amps, refer to the OP-02 data sheet. See the OP-04/OP-14 data sheet for duals.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
PM-741	±22V
PM-741C	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

PM-741	-55°C to +125°C
PM-741C	0°C to +70°C

NOTE:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C



ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-741			PM-741C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10\text{k}\Omega$	—	—	5.0	—	—	6.0	mV
Input Offset Current	I_{OS}		—	—	200	—	—	200	nA
Input Bias Current	I_B		—	—	500	—	—	500	nA
Input Resistance	R_{IN}	(Note 1)	0.3	—	—	0.3	—	—	M Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	50,000	—	—	25,000	—	—	V/V
Supply Current	I_{SY}	$V_{OUT} = 0$	—	—	2.8	—	—	2.8	mA

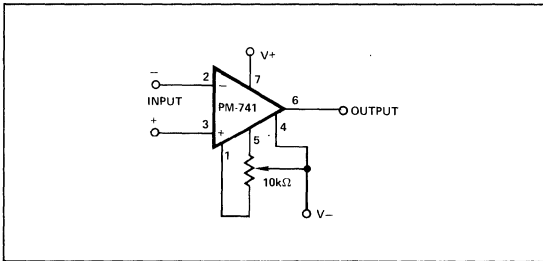
ELECTRICAL CHARACTERISTICS at $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for PM741, $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ for PM741C, $V_S = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-741			PM-741C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10\text{k}\Omega$	—	—	6.0	—	—	7.5	mV
Input Offset Current	I_{OS}		—	—	500	—	—	300	nA
Input Bias Current	I_B		—	—	1.5	—	—	0.8	μA
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	25,000	—	—	15,000	—	—	V/V
Output Voltage Swing	V_O	$R_L \geq 10\text{k}\Omega$ $R_L \geq 1\text{k}\Omega$	± 12 ± 10	—	—	± 12 ± 10	—	—	V
Input Voltage Range	IVR		± 12	—	—	± 12	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10\text{V}$	70	—	—	70	—	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10\text{k}\Omega$	—	—	142	—	—	142	$\mu\text{V/V}$

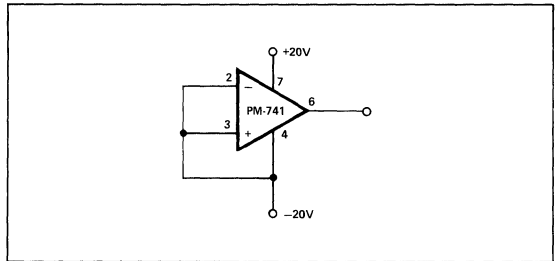
NOTE:

1. Guaranteed by design.

TYPICAL OFFSET NULLING CIRCUIT



TYPICAL BURN-IN CIRCUIT



5
OPERATIONAL AMPLIFIERS



PM-747

DUAL COMPENSATED OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Dual PM-741 Internally-Compensated Operational Amplifier
- Internal Frequency Compensation
- Low Power Consumption
- Continuous Short-Circuit Protection
- Silicon-Nitride Passivation

ORDERING INFORMATION†

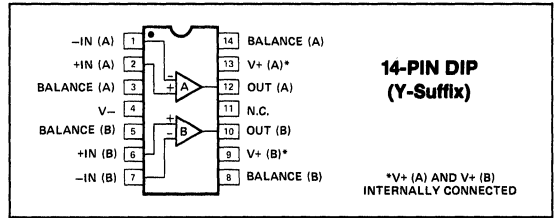
$T_A = 25^\circ\text{C}$ $V_{OS} \text{ MAX}$ (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
	HERMETIC DIP 14-PIN	
5.0	PM747Y	MIL
6.0	PM747CY	COM

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

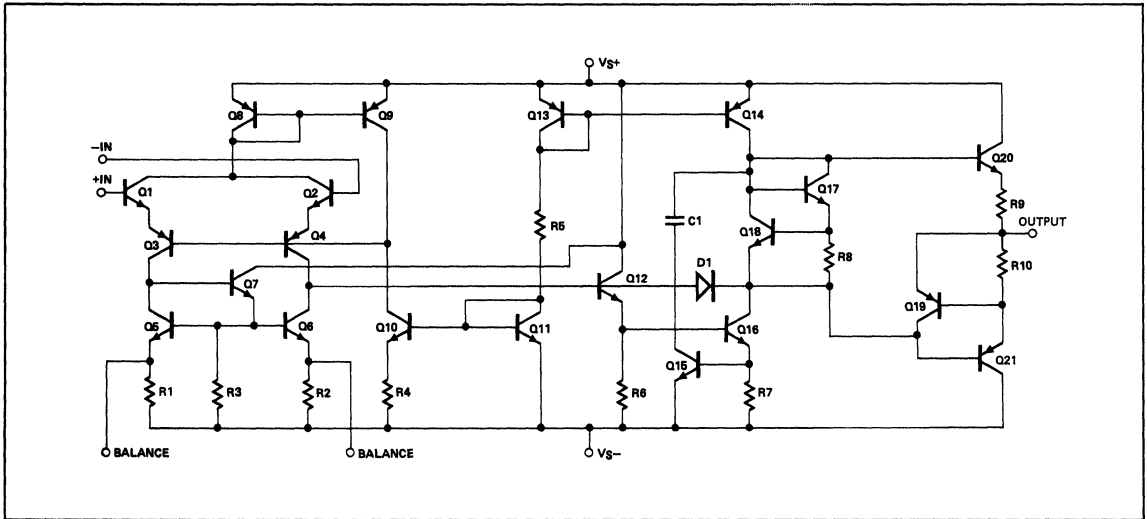
GENERAL DESCRIPTION

The PMI series of internally-compensated operational amplifiers provides industry-standard 747 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process provides maximum reliability and long-term stability of parameters for lowest overall system operating cost.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/2 of Circuit Shown)



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	
PM-747	±22V
PM-747C	±18V
Internal Power Dissipation (Note 1)	
Y Package	670mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

PM-747	-55°C to +125°C
PM-747C	0°C to +70°C

NOTE:

- See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	83°C	10.0mW/°C

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-747			PM-747C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20\text{k}\Omega$	—	1.0	5.0	—	1.0	6.0	mV
Input Offset Current	I_{OS}		—	20	200	—	20	200	nA
Input Bias Current	I_B		—	80	500	—	80	500	nA
Input Resistance	R_{IN}	(Note 1)	0.22	2.0	—	0.3	2.0	—	M Ω
Input Capacitance	C_{IN}		—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range			—	±15	—	—	±15	—	mV
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	50	200	—	25	200	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10\text{k}\Omega$ $R_L \geq 2\text{k}\Omega$	±12 ±10	±14 ±13	—	±12 ±10	±14 ±13	—	V
Output Resistance	R_O		—	75	—	—	75	—	Ω
Output Short-Circuit Current	I_{SC}		—	25	—	—	25	—	mA
Supply Current	I_{SY}	Per Amplifier, No Load	—	1.7	2.8	—	1.7	2.8	mA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 20\text{k}\Omega$, $V_{CM} = \pm 10\text{V}$	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{V}$ to $\pm 20\text{V}$ $V_S = \pm 5\text{V}$ to $\pm 18\text{V}$	—	30	150	—	—	—	$\mu\text{V/V}$
Power Consumption	P_d	Per Amplifier, No Load	—	50	85	—	50	85	mW
Transient Response, Unity Gain	Risetime Overshoot	$V_{IN} = 20\text{mV}$, $R_L = 2\text{k}\Omega$ $C_L \leq 100\text{pF}$	—	0.3	—	—	0.3	—	μs %
Slew Rate	SR	$R_L \geq 2\text{k}\Omega$	—	0.7	—	—	0.7	—	V/ μs
Channel Separation	CS		—	120	—	—	120	—	dB

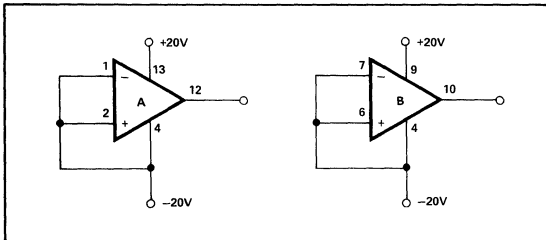
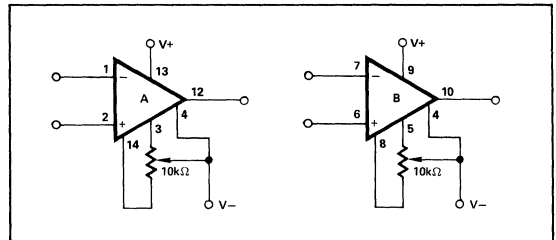
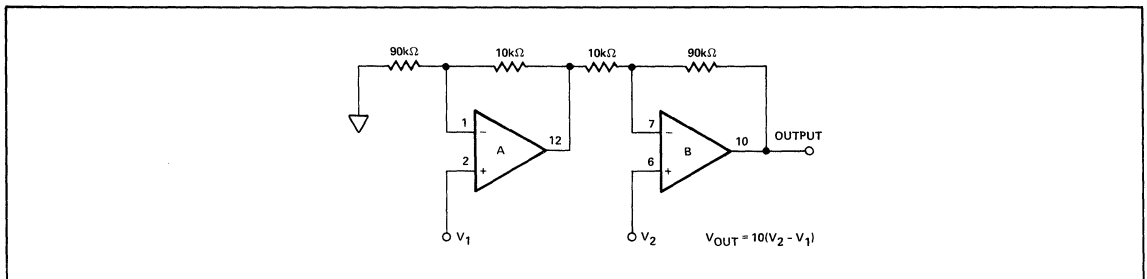
NOTE:

- Guaranteed by input bias current.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for PM-747, $0^\circ C \leq T_A \leq +70^\circ C$ for PM-747C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-747			PM-747C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	1.0	6.0	—	1.0	7.5	mV
Input Offset Current	I_{OS}	$T_A = MAX$	—	7	200	—	7	200	nA
		$T_A = MIN$	—	85	500	—	30	300	
Input Bias Current	I_B	$T_A = MAX$	—	0.03	0.5	—	0.03	0.5	μA
		$T_A = MIN$	—	0.3	1.5	—	0.10	0.8	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 14	—	± 12	± 14	—	V
		$R_L \geq 2k\Omega$	± 10	± 13	—	± 10	± 13	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	50	—	15	25	—	V/mV
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 20k\Omega$, $V_{CM} = \pm 10V$	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 20k\Omega$, $V_S = \pm 5V$ to $\pm 20V$	—	30	150	—	—	—	$\mu V/V$
		$V_S = \pm 5V$ to $\pm 18V$	—	—	—	—	30	150	
Supply Current	I_{SY}	$T_A = MAX$ Per Amplifier,	—	1.5	2.5	—	1.5	2.5	mA
		$T_A = MIN$ No Load	—	2.0	3.3	—	2.0	3.3	
Power Consumption	P_d	$T_A = MAX$ Per Amplifier,	—	45	75	—	45	75	mW
		$T_A = MIN$ No Load	—	60	100	—	60	100	
Channel Separation	CS		—	120	—	—	120	—	dB

BURN-IN CIRCUIT**TYPICAL OFFSET NULLING CIRCUIT****TYPICAL APPLICATION****HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER**



JM38510/10104

JAN SINGLE LOW-INPUT-CURRENT
OPERATIONAL AMPLIFIER (EXTERNALLY COMPENSATED)

Precision Monolithics Inc.

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low input-current, externally-compensated operational amplifier as specified in MIL-M-38510/101 for device type 04. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/101 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

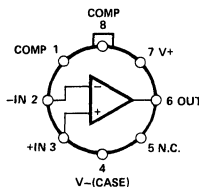
Military Device Type
04

Generic-Industry Type
LM108A

CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline A-1 (8 Lead Can). Package Type Designator "G".

PIN CONNECTIONS AND ORDERING INFORMATION



TO-99 (J-Suffix)

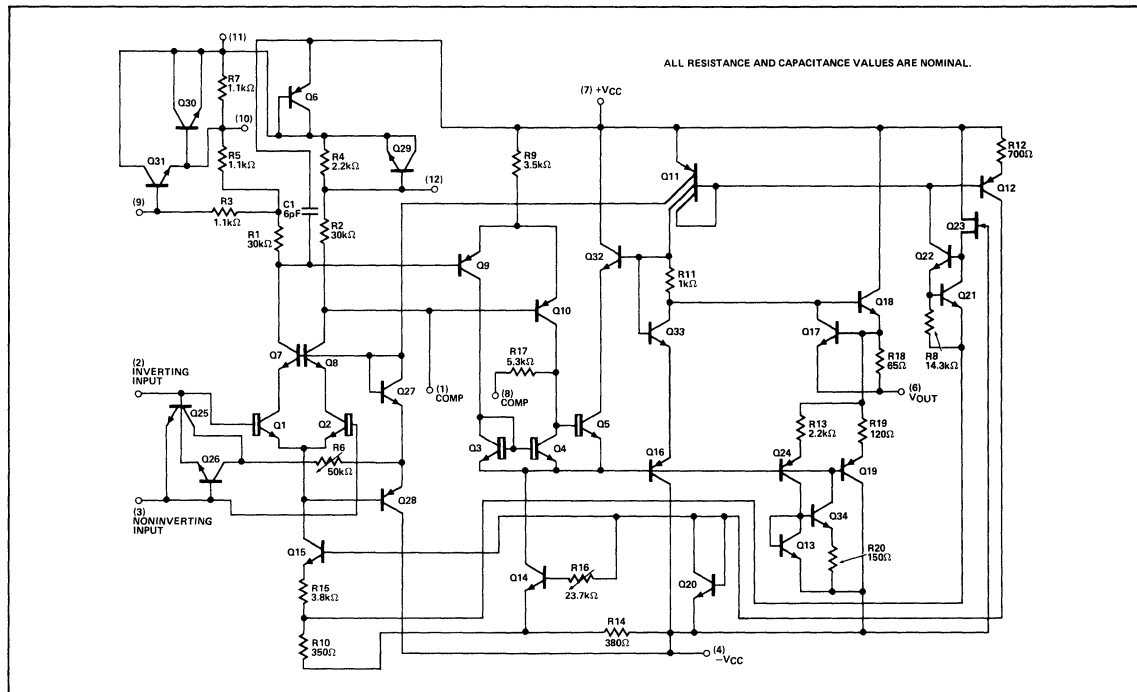
Jan Device **PMI Device Type**
JM38510/10104BGC PM108AJ1/38510

NOTE: Lead Finish: Gold Plate.
Check with factory for other qualified lead finishes.

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{J-C}	Maximum θ_{J-A}
8 Lead Can (TO-99)	G	330mW at $T_A = 125^\circ\text{C}$	40°C/W	150°C/W

SIMPLIFIED SCHEMATIC



**ELECTRICAL CHARACTERISTICS** at $5V \leq \pm V_{CC} \leq 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	(Note 2) $T_A = 25^\circ C$ $R_S = 50\Omega$ $-55^\circ C \leq T_A \leq 125^\circ C$	-0.5	+0.5	mV
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from $-55^\circ C$ to $+25^\circ C$ ΔT_A from $+25^\circ C$ to $+125^\circ C$	-5.0	+5.0	$\mu V/^\circ C$
Input Offset Current	I_{IO}	(Note 2) $T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq 125^\circ C$	-0.2	+0.2	nA
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from $-55^\circ C$ to $+25^\circ C$ ΔT_A from $+25^\circ C$ to $+125^\circ C$	-2.5	+2.5	$\mu A/^\circ C$
Input Bias Current	$+I_{IB}$	(Note 2) $25^\circ C \leq T_A \leq 125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	-0.1	+2.0	nA
	$-I_{IB}$	(Note 2) $25^\circ C \leq T_A \leq 125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	-0.1	+2.0	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 10V$ $R_S = 50\Omega$ $T_A = 25^\circ C$ $-V_{CC} = 20V$ $-55^\circ C \leq T_A \leq 125^\circ C$	-16	+16	$\mu V/V$
Power Supply Rejection Ratio	-PSRR	$+V_{CC} = 20V$ $R_S = 50\Omega$ $T_A = 25^\circ C$ $-V_{CC} = -10V$ $-55^\circ C \leq T_A \leq 125^\circ C$	-16	+16	$\mu V/V$
Input Voltage Common-Mode Rejection	CMR	$\pm V_{CC} = 20V$ $V_{IN} = \pm 15V$ $R_S = 50\Omega$	96	—	dB
Adjustment For Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Adjustment For Input Offset Voltage	V_{IO} ADJ (-)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Output Short-Circuit Current (For Positive Output)	$I_{OS (+)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	15	—	mA
Output Short-Circuit Current (For Negative Output)	$I_{OS (-)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	—	15	mA
Supply Current	I_{CC}	$T_A = -55^\circ C$	—	0.8	mA
		$T_A = +25^\circ C$	—	0.6	
		$T_A = +125^\circ C$	—	0.6	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = 20V, R_L = 10k\Omega$	± 16	—	V
		$\pm V_{CC} = 20V, R_L = 2k\Omega$	—	—	
Open-Loop Voltage Gain (Single Ended) (Note 1)	$A_{VS (\pm)}$	$\pm V_{CC} = 20V$ $T_A = 25^\circ C$ $R_L = 10k\Omega$ $-55^\circ C \leq T_A \leq 125^\circ C$ $V_{OUT} = \pm 15V$	80	—	V/mV
Open-Loop Voltage Gain (Single Ended) (Note 1)	A_{VS}	$\pm V_{CC} = 5V$ $R_L = 10k\Omega$ $V_{OUT} = \pm 2V$	20	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$C_F = 10pF$	—	1000	nsec
Transient Response Overshoot	$TR_{(OS)}$	$C_F = 10pF$	—	50	%
Noise (Referred to Input) Broadband	$N_I (BB)$	$V_{CC} = 20V$ $T_A = 25^\circ C$ Bandwidth = 5kHz	—	15	μV rms
Noise (Referred to Input) Popcorn	$N_I (PC)$	$\pm V_{CC} = 20V$ $T_A = 25^\circ C$ Bandwidth = 5kHz	—	40	μV peak

NOTES:

1. Note that gain is not specified at $V_{IO (ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO (ADJ)}$ extremes. For closed-loop applications (closed-loop gain less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements

exist (positive open-loop gain or open-loop gain linearity), they should be specified in the individual procurement document as additional requirements.

2. Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
3. Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75^\circ C$ will cause T_J to exceed the maximum of $175^\circ C$.

ELECTRICAL CHARACTERISTICS at $5V \leq \pm V_{CC} \leq 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted. (Continued)

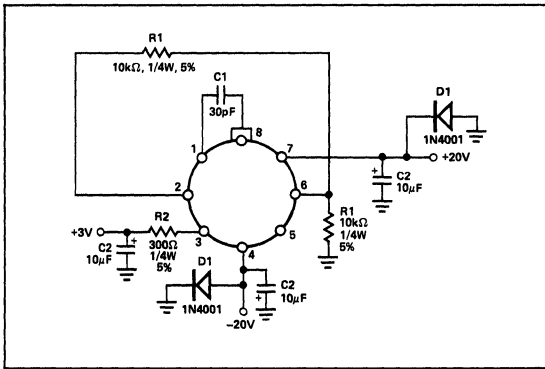
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	
Slew Rate	SR (+)	$A_V = 1$	$-55^\circ C \leq T_A \leq 25^\circ C$	0.05	—	V/ μ sec
		$V_{IN} = +5V$	$T_A = 125^\circ C$	0.05	—	
Slew Rate	SR (-)	$A_V = 1$	$-55^\circ C \leq T_A \leq 25^\circ C$	0.05	—	V/ μ sec
		$V_{IN} = \pm 5V$	$T_A = 125^\circ C$	0.05	—	

NOTES:

- Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed-loop applications (closed-loop gain less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity), they should be

specified in the individual procurement document as additional requirements.

- Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
- Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75^\circ C$ will cause T_J to exceed the maximum of $175^\circ C$.

For Other Test Circuit Diagrams, See MIL-M-38510/101
BURN-IN CIRCUIT




JM38510/10106

JAN DUAL LOW-INPUT-CURRENT OPERATIONAL AMPLIFIER (EXTERNALLY COMPENSATED)

Precision Monolithics Inc.

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a dual low input-current, externally-compensated operational amplifier as specified in MIL-M-38510/101 for device type 06.

Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/101 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The generic industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

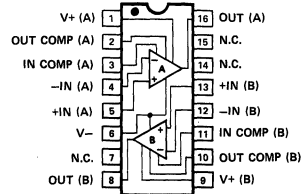
Military Device Type
06

Generic Industry Type
LM2108A

CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline D-2 (16-pin DIP). Package Type Designator "E".

PIN CONNECTIONS AND ORDERING INFORMATION



16-PIN HERMETIC DIP (Q-Suffix)

Jan Device Type
JM38510/10106BEB

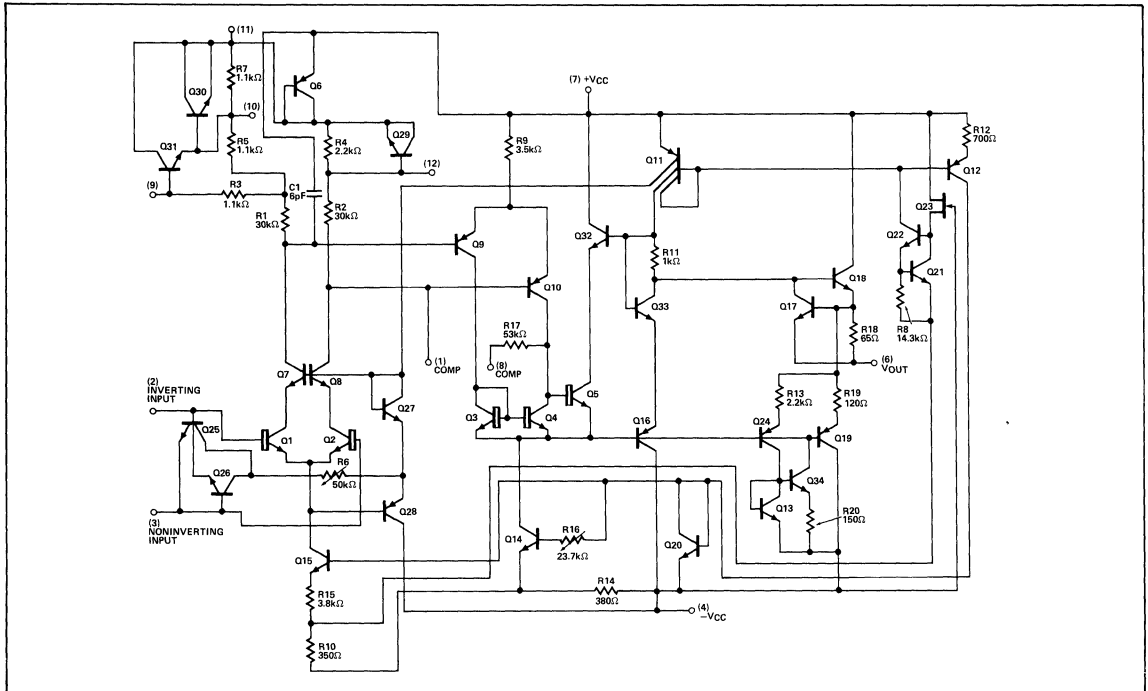
PMI Device Type
PM2108AQ2/38510

NOTE: Lead finish: Acid Tin Plate
Check with factory for other qualified lead finishes.

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{J-C}	Maximum θ_{J-A}
Dual-in-line	E	400mW at $T_A = 125^\circ\text{C}$	35°C/W	120°C/W

SIMPLIFIED SCHEMATIC (Each Amplifier)



**ELECTRICAL CHARACTERISTICS** at $5V \leq V_{CC} \leq 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	(Note 2) $T_A = 25^\circ C$ $R_S = 50\Omega$ $-55^\circ C \leq T_A \leq 125^\circ C$	-0.5 -1.0	+0.5 +1.0	mV
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from $-55^\circ C$ to $+25^\circ C$ ΔT_A from $+25^\circ C$ to $+125^\circ C$	-5.0 -5.0	+5.0 +5.0	$\mu V/^\circ C$
Input Offset Current	I_{IO}	(Note 2) $T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq 125^\circ C$	-0.2 -0.4	+0.2 +0.4	nA
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from $-55^\circ C$ to $+25^\circ C$ ΔT_A from $+25^\circ C$ to $+125^\circ C$	-2.5 -2.5	+2.5 +2.5	$pA/^\circ C$
Input Bias Current	$+I_{IB}$	(Note 2) $25^\circ C \leq T_A \leq 125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	-0.1 -0.1	+2.0 +3.0	nA
	$-I_{IB}$	(Note 2) $25^\circ C \leq T_A \leq 125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	-0.1 -0.1	+2.0 +3.0	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 10V$ $R_S = 50\Omega$ $T_A = 25^\circ C$ $-V_{CC} = -20V$ $-55^\circ C \leq T_A \leq 125^\circ C$	-16 -16	+16 +16	$\mu V/V$
Power Supply Rejection Ratio	-PSRR	$+V_{CC} = 20V$ $R_S = 50\Omega$ $T_A = 25^\circ C$ $-V_{CC} = -10V$ $-55^\circ C \leq T_A \leq 125^\circ C$	-16 -16	+16 +16	$\mu V/V$
Input Voltage Common-Mode Rejection	CMR	$\pm V_{CC} = 20V$ $V_{IN} = \pm 15V$ $R_S = 50\Omega$	96	—	dB
Adjustment For Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Adjustment For Input Offset Voltage	V_{IO} ADJ (-)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Output Short-Circuit Current (For Positive Output)	$I_{OS (+)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	15	—	mA
Output Short-Circuit Current (For Negative Output)	$I_{OS (-)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	—	15	mA
Supply Current	I_{CC}	$\pm V_{CC} = 15V$ $T_A = -55^\circ C$	—	0.8	mA
		$T_A = +25^\circ C$	—	0.6	
		$T_A = +125^\circ C$	—	0.6	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = 20V, R_L = 10k\Omega$ $\pm V_{CC} = 20V, R_L = 2k\Omega$	± 16 —	— —	V
Open-Loop Voltage Gain (Single Ended) (Note 1)	$A_{VS (\pm)}$	$\pm V_{CC} = 20V$ $T_A = 25^\circ C$ $R_L = 10k\Omega$ $-55^\circ C \leq T_A \leq 125^\circ C$ $V_{OUT} = \pm 15V$	80 40	— —	V/mV
Open-Loop Voltage Gain (Single Ended) (Note 1)	A_{VS}	$\pm V_{CC} = 5V$ $R_L = 10k\Omega$ $V_{OUT} = \pm 2V$	20	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$C_F = 10pF$	—	1000	nsec
Transient Response Overshoot	$TR_{(OS)}$	$C_F = 10pF$	—	50	%
Noise (Referred to Input) Broadband	$N_I (BB)$	$V_{CC} = 20V$ $T_A = 25^\circ C$ Bandwidth = 5kHz	—	15	μV rms
Noise (Referred to Input) Popcorn	$N_I (PC)$	$\pm V_{CC} = 20V$ $T_A = 25^\circ C$ Bandwidth = 5kHz	—	40	μV peak

NOTES:

- Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed-loop applications (closed-loop gain less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity), they should be specified in the individual procurement document as additional requirements.
- Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
- Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75^\circ C$ will cause T_J to exceed the maximum of $175^\circ C$. For dual devices, I_{OS} is measured one channel at a time.

ELECTRICAL CHARACTERISTICS at $5V \leq \pm V_{CC} \leq 20V$ and $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Slew Rate	SR (+)	$A_V = 1$	0.05	—	$V/\mu\text{sec}$
		$V_{IN} = +5V$	0.05	—	
Slew Rate	SR (-)	$A_V = 1$	0.05	—	$V/\mu\text{sec}$
		$V_{IN} = \pm 5V$	0.05	—	
Settling Time	$t_s (+)$	$T_A = 25^{\circ}C$	—	—	ns
		$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	—	—	
	$t_s (-)$	$T_A = 25^{\circ}C$	—	—	ns
		$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	—	—	
Channel Separation	CS	$\pm V_{CC} = 20V$ $T_A = 25^{\circ}C$	80	—	dB

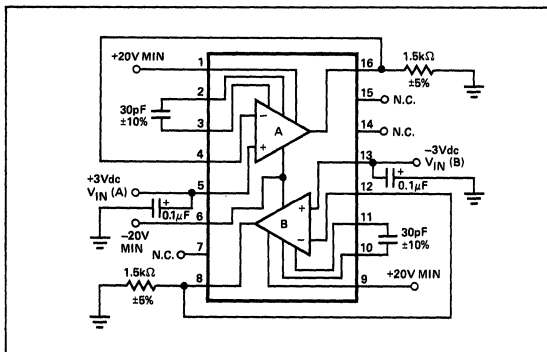
NOTES:

- Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed-loop applications (closed-loop gain is less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity), they should be

specified in the individual procurement document as additional requirements.

- Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
- Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75^{\circ}C$ will cause T_j to exceed the maximum of $175^{\circ}C$. For dual devices, I_{OS} is measured one channel at a time.

For other Test Circuit Diagrams, See MIL-M-38510/101

BURN-IN CIRCUIT




JM38510/11004

JAN QUAD 741-TYPE
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Broadband Noise $5\mu V_{rms}$ Max
- RM-4136 Direct Replacement
- Silicon-Nitride Passivation
- Low Crossover Distortion
- Continuous Short-Circuit Protection
- MIL-M-38510 Processed

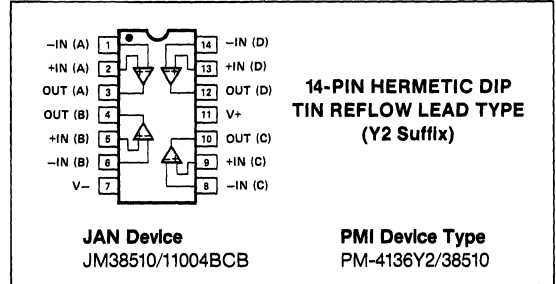
The generic industry device may not have identical operational performance characteristics across the Military temperature range, or reliability factors equivalent to the 38510 device.

For an 883-processed device with improved electrical specifications, review the OP-09 data sheet.

ORDERING INFORMATION

JAN SLASH SHEET	PMI DEVICE
JM38510/11004BCB	PM-4136Y2/38510

PIN CONNECTIONS



GENERAL DESCRIPTION

The PM-4136Y2/38510 provides four matched 741-type operational amplifiers in a 14-pin hermetic dual-in-line package. The device is manufactured to meet or exceed all terms and conditions of the MIL-M-38510/110A slash sheet, under the requirements of the MIL-M-38510 general microcircuit specifications. Complete device specifications, test configurations, and manufacturing requirements are found in the slash sheet and general specifications.

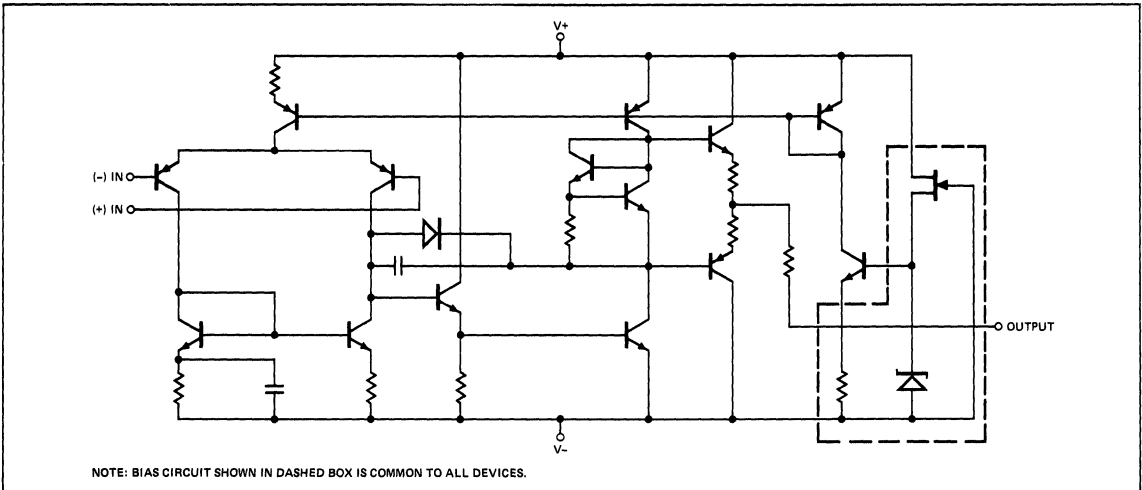
POWER AND THERMAL CHARACTERISTICS

Case Outline	Package	Maximum Allowable Power Dissipation	Maximum θ_{JC}	Maximum θ_{JA}
Y	Dual-In-Line	400mW @ $T_A = 125^\circ C$	35° C/W	120° C/W

GENERIC CROSS-REFERENCE INFORMATION

The PM-4136Y2/38510 is PMI's product name for the JM38510/11004BCB. The PM-4136Y2/38510 is a 38510-processed version of the industry-standard RM4136.

SIMPLIFIED SCHEMATIC (One of Four Amplifiers is Shown)



5
OPERATIONAL AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (Note 1)	±22V
Input Voltage Range (Note 2)	±22V
Differential Input Voltage Range (Note 3)	±30V
Input Current Range	10 to 0.1mA
Storage Temperature Range	-65°C to +150°C
Output Short-Circuit Duration (Note 4)	Unlimited
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature (T _j) (Note 5)	175°C

NOTES:

1. Voltages in excess of these may be applied for short-term tests if voltage difference does not exceed 44 volts.
2. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.

3. The differential input voltage range shall not exceed the supply voltage range.
4. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
5. For short-term test (in the specific burn-in and life-test configuration where required and up to 168 hours maximum) T_j = 275°C.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	±5V to ±20V
Ambient Temperature Range	-55° to +125°C

ELECTRICAL CHARACTERISTICS at ±5V ≤ V_{CC} ≤ ±20V and -55°C ≤ T_A ≤ 125°C, R_S = 50Ω, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	04 LIMITS		UNITS
			MIN	MAX	
Input Offset Voltage	V _{IO}	T _A = 25°C	-5	5	mV
		-55°C ≤ T _A ≤ 125°C (Note 1)	-6	6	
Input Offset Voltage Temperature Sensitivity	ΔV _{IO} /ΔT	-55°C ≤ T _A ≤ 125°C	-25	25	μV/°C
Input Offset Current	I _{IO}	25°C ≤ T _A ≤ 125°C, R _S = 20kΩ (Note 1)	-75	75	nA
		T _A = -55°C, R _S = 20kΩ (Note 1)	-150	150	
Input Offset Current Temperature Sensitivity	ΔI _{IO} /ΔT	-55°C ≤ T _A ≤ 25°C	-1000	1000	pA/°C
		25°C ≤ T _A ≤ 125°C	-500	500	
Input Bias Current	+I _{IB}	R _S = 20kΩ, 25°C ≤ T _A ≤ 125°C	-250	-1	nA
		T _A = -55°C (Note 1)	-400	-1	
	-I _{IB}	R _S = 20kΩ, 25°C ≤ T _A ≤ 125°C	-250	-1	
		T _A = -55°C (Note 1)	-400	-1	
Power Supply Rejection Ratio	+PSRR	+V _{CC} = 10V, -V _{CC} = -20V	-100	100	μV/V
	-PSRR	+V _{CC} = 20V, -V _{CC} = -10V	-100	100	
Input Voltage Common-Mode Rejection	CMR	Common-Mode Range = 30V (Note 2)	76	—	dB
Output Short Circuit Current	I _{OS(+)}	±V _{CC} = ±15V, 25°C ≤ T _A ≤ 125°C (Note 3)	-80	—	mA
Output Short Circuit Current	I _{OS(-)}	±V _{CC} = ±15V, T _A = -55°C (Note 3)	—	80	
Supply Current	I _{CC}	V _{CC} = ±15V, T _A = -55°C	—	13	mA
		(Note 4), T _A = 25°C	—	11	
		T _A = 125°C	—	11	
Output Voltage Swing (Maximum)	+V _{OP}	V _{CC} = ±20V, R _L = 10kΩ, R _L = 2kΩ	+16	—	V
	-V _{OP}	V _{CC} = ±20V, R _L = 10kΩ, R _L = 2kΩ	+15	—	
			—	-16	
			—	-15	

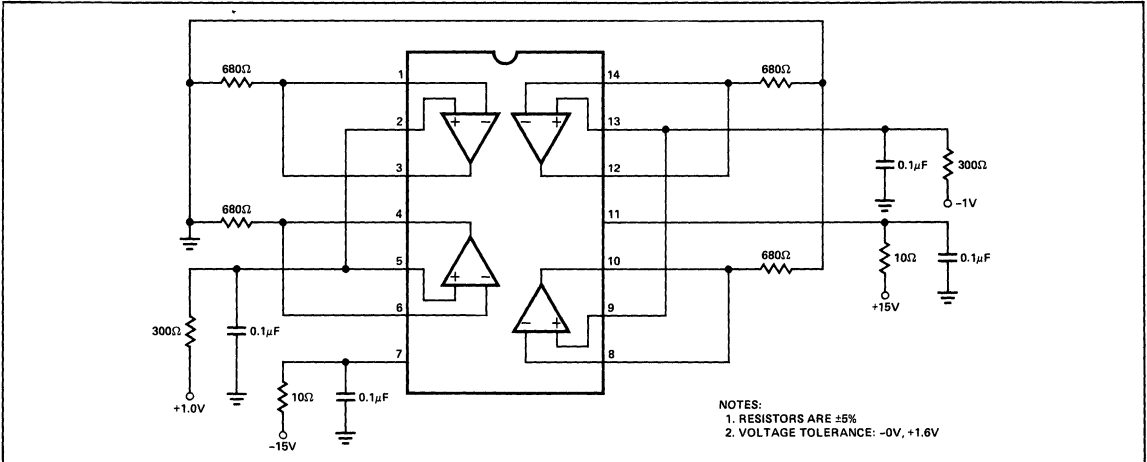
**ELECTRICAL CHARACTERISTICS** at $\pm 5V \leq V_{CC} \leq \pm 20V$ and $-55^\circ C \leq T_A \leq 125^\circ C$, $R_S = 50\Omega$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	04 LIMITS		UNITS
			MIN	MAX	
Open-Loop Voltage Gain (Single Ended)	$A_{VS(+)}$	$R_L = 10k\Omega$, $\pm V_O = \pm 15V$, $T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq 125^\circ C$	50 25	— —	
	$A_{VS(-)}$	$R_L = 2k\Omega$, $\pm V_O = \pm 15V$, $T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq 125^\circ C$	50 25	— —	V/mV
	A_{VS}	$R_L = 10k\Omega$, $T_A = 25^\circ C$ $R_L = 2k\Omega$, $\pm V_{CC} = \pm 5V$, $-55^\circ C \leq T_A \leq 125^\circ C$	10 10	— —	
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 20V$, $A_V = 1$	—	0.3	μs
Transient Response Overshoot	$TR_{(OS)}$	$\pm V_{CC} = \pm 20V$	—	50	μs
Slew Rate	$SR(+)$	$\pm V_{CC} = \pm 20V$, $A_V = 1$	0.6	—	V/ μs
Noise (Broadband)	$N_I(BB)$	$T_A = 25^\circ C$, $\pm V_{CC} = \pm 20V$, $R_S = 50\Omega$	—	5	μV_{rms}
Noise (Popcorn)	$N_I(PC)$	$T_A = 25^\circ C$, $\pm V_{CC} = \pm 20V$, $R_S = 20k\Omega$	—	50	μV_{pk}
Channel Separation	CS	$T_A = 25^\circ C$	80	—	dB

NOTES:

- Tested at $V_{CM} = 0$, +15V and -15V with $\pm V_{CC} = \pm 20V$; and at $V_{CM} = 0V$ and -2.5V with $\pm V_{CC} = \pm 5V$.
- CMR is determined by measuring input offset voltage as follows:
 - Only one amplifier shorted to ground at one time, $0 \leq t \leq 25ms$. Continuous limits will be considerably lower and apply for $-55^\circ C \leq T_A \leq 25^\circ C$.
 - I_{CC} limits are the total for all four amplifiers at no load, connected as follows with the noninverting inputs grounded.

OFFSET VOLTAGE CONDITION	+V _{CC}	-V _{CC}	V _O
1	35V	-5V	15V
2	5V	-35V	-15V

BURN-IN CIRCUIT

5 OPERATIONAL AMPLIFIERS



JM38510/11401/11402/11403/ 11404/11405/11406

JAN JFET-INPUT
OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low-power, internally-compensated JFET-input operational amplifier as specified in MIL-M-38510/114 for device types O1 to O6. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/114 for Class B processed devices.

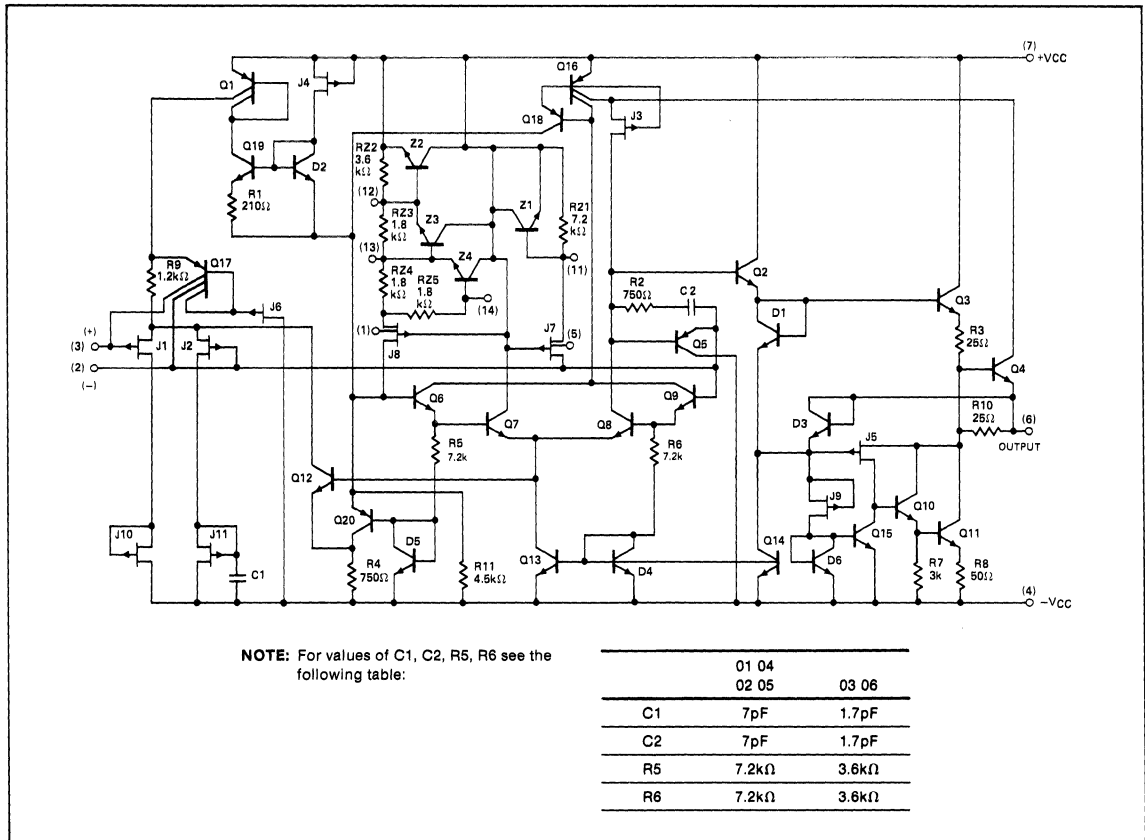
GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The generic-industry types listed may

not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic-Industry Type
O1	LF-155
O4	LF-155A
O2	LF-156
O5	LF-156A
O3	LF-157
O6	LF-157A

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage Range	±2V
Input Voltage Range (Note 1)	±20V
Differential Input Voltage Range	±40V
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	$T_j = 175^\circ\text{C}$ (Note 3)
Storage Temperature Range	-65°C to +150°C
Output Short-Circuit Duration	Unlimited (Note 2)

- Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
- For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), $T_j = 275^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	±5 to ±20 VDC
Ambient Temperature Range	-55°C to +125°C

NOTES:

- The absolute maximum negative input voltage is equal to the negative power supply voltage.

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = -55°C to +125°C and figure 1, unless otherwise noted.

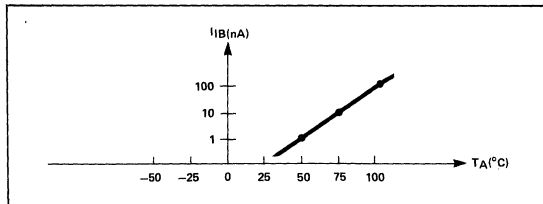
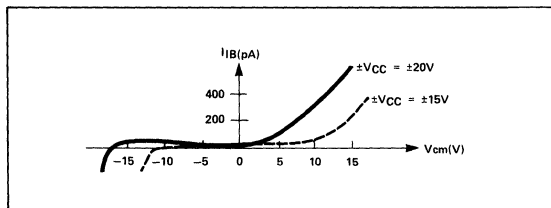
PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		04 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V, V_{CM} = 0V$ $T_A = 25^\circ\text{C}$	-5	5	-2	2	mV
		$\pm V_{CC} = \pm 20V$ $V_{CM} = \pm 15V, 0V$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-7	7	-2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$ $V_{CM} = 0V$	-30	30	-10	10	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V, V_{CM} = 0V,$ $T_j = 25^\circ\text{C}$	-20	20	-20	20	pA
		$T_j = 125^\circ\text{C}$	-20	20	-20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$ $-I_{IB}$	$\pm V_{CC} = \pm 20V, V_{CM} = +15V$ $T_j = 25^\circ\text{C}$	-100	3500	-100	3500	pA
		$t \leq 25\text{ms}$ $T_j = 125^\circ\text{C}$	-10	60	-10	60	nA
		$\pm V_{CC} = \pm 15V, V_{CM} = +10V$ $T_j = 25^\circ\text{C}$	-100	300	-100	300	pA
		$t \leq 25\text{ms}$ $T_j = 125^\circ\text{C}$	-10	50	-10	50	nA
		$\pm V_{CC} = \pm 20V, -15V \leq V_{CM} \leq 0V$ $T_j = 25^\circ\text{C}$	-100	100	-100	100	pA
		$t \leq 25\text{ms}$ $T_j = 125^\circ\text{C}$	-10	50	-10	50	nA
Power Supply Rejection Ratio	+PSRR -PSRR	$+V_{CC} = 10V, -V_{CC} = -20V$	85	—	85	—	dB
		$+V_{CC} = 20V, -V_{CC} = -10V$					
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$ $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	$V_{IO} \text{ ADJ}(+)$ $V_{IO} \text{ ADJ}(-)$	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
		$\pm V_{CC} = \pm 20V$	—	-8	—	-8	
Output Short-Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25\text{ms}$ (Short Circuit to Ground)	-50	—	-50	—	mA
Output Short-Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25\text{ms}$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55^\circ\text{C}$	—	6	—	6	mA
		$\pm V_{CC} = \pm 15V, T_A = +25^\circ\text{C}$	—	4	—	4	
		$T_A = +125^\circ\text{C}$	—	4	—	4	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V, R_L = 10k\Omega$	±16	—	±16	—	V
		$\pm V_{CC} = \pm 20V, R_L = 2k\Omega$	±15	—	±15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$ $A_{VS(-)}$	$\pm V_{CC} = \pm 20V, V_{OUT} = \pm 15V$ $R_L = 2k\Omega, T_A = 25^\circ\text{C}$	50	—	50	—	V/mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$ $R_L = 2k\Omega$ $V_{OUT} = \pm 2V$	10	—	10	—	V/mV

ELECTRICAL CHARACTERISTICS at V_{CC} from $\pm 5V$ to $\pm 20V$; source resistance = 50 ohm; ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$ and figure 1, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		04 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	150	—	150	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	40	—	40	%
Slew Rate	$SR_{(+)}$ and $SR_{(-)}$	$V_{IN} = \pm 5V$, $\pm V_{CC} = \pm 15V$ $A_V = 1$, See Figure 2 $T_A = 25^{\circ}C$ $T_A = -55^{\circ}C$, $+125^{\circ}C$	2 1	—	3 1.5	—	$V/\mu s$
	Settling Time	$ts_{(+)}$ and $ts_{(-)}$	—	4000	—	4000	ns
Noise (Referred to Input) Broadband	$N_{I(BB)}$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_{I(PC)}$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

- Bias currents are actually junction leakage currents which double (approximately) for each $10^{\circ}C$ increase in junction temperature T_j . Measurement of bias current is specified at T_j rather than T_A , since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms or 5 loop time constants after power is first applied to the device for test. Measurement at $T_A = -55^{\circ}C$ is not necessary since expected values are too small for typical test systems.
- Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:



- Negative I_B minimum limits reflect the characteristics of device with bias current compensation.
- CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and $-15V$.
- Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_j(max) \leq 175^{\circ}C$.
- Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline A-1 (8 Lead Can). Package Type Designator "G".

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{J-C}	Maximum θ_{J-A}
8 Lead Can (TO-99)	G	330mW at $T_A = 125^{\circ}C$	40°C/W	150°C/W

PIN CONNECTIONS AND ORDERING INFORMATION

<p>Jan Device</p> <p>JM38510/11401BGC JM38510/11404BGC JM38510/11402BGC JM38510/11405BGC JM38510/11403BGC JM38510/11406BGC</p>	<p>PMI Device Type</p> <p>PM155J1/38510 PM155AJ1/38510 PM156J1/38510 PM156AJ1/38510 PM157J1/38510 PM157AJ1/38510</p>
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NOTE: Lead Finish-Gold Plate.
Check with factory for other qualified lead finishes.

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage Range	±22V
Input Voltage Range (Note 1)	±20V
Differential Input Voltage Range	±40V
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	$T_j = 175^\circ\text{C}$ (Note 3)
Storage Temperature Range	-65°C to +150°C
Output Short-Circuit Duration	Unlimited (Note 2)

- Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
- For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), $T_j = 275^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	±5 to ±20 VDC
Ambient Temperature Range	-55°C to +125°C

NOTES:

- The absolute maximum negative input voltage is equal to the negative power supply voltage.

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = -55°C to +125°C and figure 1, unless otherwise noted.

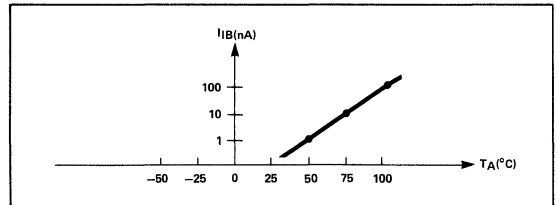
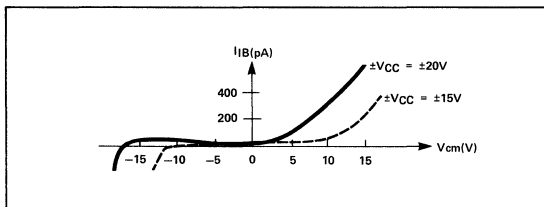
PARAMETER	SYMBOL	CONDITIONS	02 LIMITS		05 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V, V_{CM} = 0V$ $T_A = 25^\circ\text{C}$	-5	5	-2	2	mV
		$\pm V_{CC} = \pm 20V$ $V_{CM} = \pm 15V, 0V$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-7	7	-2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$ $V_{CM} = 0V$	-30	30	-10	10	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V, V_{CM} = 0V,$ $T_j = 25^\circ\text{C}$	-20	20	-20	20	pA
		$T_j = 125^\circ\text{C}$	-20	20	-20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC} = \pm 20V, V_{CM} = +15V$ $T_j = 25^\circ\text{C}$ $t \leq 25\text{ms}$ $T_j = 125^\circ\text{C}$	-100	3500	-100	3500	pA
		$\pm V_{CC} = \pm 15V, V_{CM} = +10V$ $T_j = 25^\circ\text{C}$	-10	60	-10	60	nA
	$-I_{IB}$	$\pm V_{CC} = \pm 20V, V_{CM} = +10V$ $T_j = 25^\circ\text{C}$	-100	300	-100	300	pA
		$T_j = 125^\circ\text{C}$	-10	50	-10	50	nA
	$\pm V_{CC} = \pm 20V, -15V \leq V_{CM} \leq 0V$ $T_j = 25^\circ\text{C}$	-100	100	-100	100	pA	
	$T_j = 125^\circ\text{C}$	-10	50	-10	50	nA	
Power Supply Rejection Ratio	+PSRR -PSRR	$+V_{CC} = 10V, -V_{CC} = -20V$	85	—	85	—	dB
		$+V_{CC} = 20V, -V_{CC} = -10V$	—	—	—	—	
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$ $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	$V_{IO\ ADJ(+)}$ $V_{IO\ ADJ(-)}$	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
		$\pm V_{CC} = \pm 20V$	—	-8	—	-8	
Output Short-Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25\text{ms}$ (Short Circuit to Ground)	-50	—	-50	—	mA
Output Short-Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25\text{ms}$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55^\circ\text{C}$	—	11	—	11	mA
		$\pm V_{CC} = \pm 15V, T_A = +25^\circ\text{C}$	—	7	—	7	
		$T_A = +125^\circ\text{C}$	—	7	—	7	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V, R_L = 10\text{k}\Omega$	±16	—	±16	—	V
		$\pm V_{CC} = \pm 20V, R_L = 2\text{k}\Omega$	±15	—	±15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$ $A_{VS(-)}$	$\pm V_{CC} = \pm 20V, V_{OUT} = \pm 15V$ $R_L = 2\text{k}\Omega, T_A = 25^\circ\text{C}$	50	—	50	—	V/mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$ $R_L = 2\text{k}\Omega$ $V_{OUT} = \pm 2V$	10	—	10	—	V/mV

ELECTRICAL CHARACTERISTICS at V_{CC} from $\pm 5V$ to $\pm 20V$; source resistance = 50 ohm; ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$ and figure 1, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	02 LIMITS		05 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	100	—	100	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	40	—	40	%
Slew Rate	$SR_{(+)}$ and $SR_{(-)}$	$V_{IN} = \pm 5V$, $\pm V_{CC} = \pm 15V$ $A_V = 1$, See Figure 2 $T_A = 25^{\circ}C$	7.5	—	10	—	$V/\mu s$
		$T_A = -55^{\circ}C$, $+125^{\circ}C$	5	—	7	—	
Settling Time	$ts_{(+)}$ and $ts_{(-)}$	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25^{\circ}C$, $A_V = -1$ See Figure 3	—	1500	—	1500	ns
Noise (Referred to Input) Broadband	$N_I(BB)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_I(PC)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

- Bias currents are actually junction leakage currents which double (approximately) for each $10^{\circ}C$ increase in junction temperature T_j . Measurement of bias current is specified at T_j rather than T_A , since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms or 5 loop time constants after power is first applied to the device for test. Measurement at $T_A = -55^{\circ}C$ is not necessary since expected values are too small for typical test systems.
- Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:



- Negative I_B minimum limits reflect the characteristics of device with bias current compensation.
- CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and $-15V$.
- Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_j(max) \leq 175^{\circ}C$.
- Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage Range	±22V
Input Voltage Range (Note 1)	±20V
Differential Input Voltage Range	±40V
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	$T_J = 175^\circ\text{C}$ (Note 3)
Storage Temperature Range	-65°C to +150°C
Output Short-Circuit Duration	Unlimited (Note 2)

- Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
- For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), $T_J = 275^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	±5 to ±20 VDC
Ambient Temperature Range	-55°C to +125°C

NOTES:

- The absolute maximum negative input voltage is equal to the negative power supply voltage.

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = -55°C to +125°C and figure 1, unless otherwise noted.

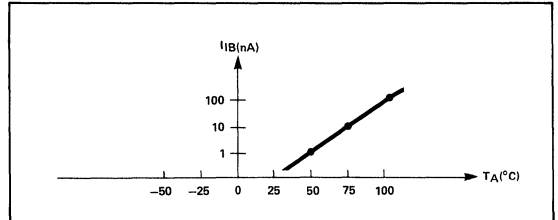
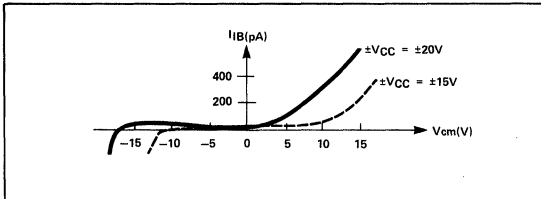
PARAMETER	SYMBOL	CONDITIONS	03 LIMITS		06 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V, V_{CM} = 0V$ $T_A = 25^\circ\text{C}$	-5	5	-2	2	mV
		$\pm V_{CC} = \pm 20V$ $V_{CM} = \pm 15V, 0V$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-7	7	-2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$ $V_{CM} = 0V$	-30	30	-10	10	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V, V_{CM} = 0V,$ $T_J = 25^\circ\text{C}$	-20	20	-20	20	μA
		$T_J = 125^\circ\text{C}$	-20	20	-20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC} = \pm 20V, V_{CM} = +15V$ $T_J = 25^\circ\text{C}$	-100	3500	-100	3500	μA
		$t \leq 25\text{ms}$ $T_J = 125^\circ\text{C}$	-10	60	-10	60	nA
	$-I_{IB}$	$\pm V_{CC} = \pm 15V, V_{CM} = +10V$ $T_J = 25^\circ\text{C}$	-100	300	-100	300	μA
		$t \leq 25\text{ms}$ $T_J = 125^\circ\text{C}$	-10	50	-10	50	nA
		$\pm V_{CC} = \pm 20V, -15V \leq V_{CM} \leq 0V$ $T_J = 25^\circ\text{C}$	-100	100	-100	100	μA
		$t \leq 25\text{ms}$ $T_J = 125^\circ\text{C}$	-10	50	-10	50	nA
Power Supply Rejection Ratio	+PSRR -PSRR	$+V_{CC} = 10V, -V_{CC} = -20V$	85	—	85	—	dB
		$+V_{CC} = 20V, -V_{CC} = -10V$	—	—	—	—	
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$ $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	$V_{IO\ ADJ(+)}$	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
	$V_{IO\ ADJ(-)}$	$\pm V_{CC} = \pm 20V$	—	-8	—	-8	
Output Short-Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25\text{ms}$ (Short Circuit to Ground)	-50	—	-50	—	mA
Output Short-Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25\text{ms}$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55^\circ\text{C}$	—	11	—	11	mA
		$\pm V_{CC} = \pm 15V, T_A = +25^\circ\text{C}$	—	7	—	7	
		$T_A = +125^\circ\text{C}$	—	7	—	7	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V, R_L = 10k\Omega$	±16	—	±16	—	V
		$\pm V_{CC} = \pm 20V, R_L = 2k\Omega$	±15	—	±15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$ $A_{VS(-)}$	$\pm V_{CC} = \pm 20V, V_{OUT} = \pm 15V$ $R_L = 2k\Omega, T_A = 25^\circ\text{C}$	50	—	50	—	V/mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$ $R_L = 2k\Omega$ $V_{OUT} = \pm 2V$	10	—	10	—	V/mV

ELECTRICAL CHARACTERISTICS at V_{CC} from $\pm 5V$ to $\pm 20V$; source resistance = 50 ohm; ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$ and figure 1, unless otherwise noted. (Continued)

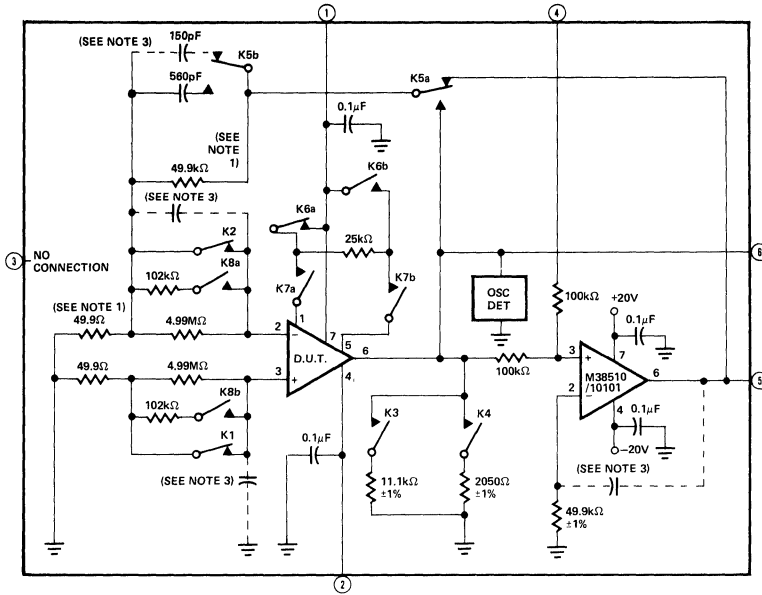
PARAMETER	SYMBOL	CONDITIONS	03 LIMITS		06 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 5$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	450	—	450	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 5$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	25	—	25	%
Slew Rate	$SR(+)$ and $SR(-)$	$V_{IN} = \pm 1V$, $\pm V_{CC} = \pm 15V$ $A_V = 5$, See Figure 2 $T_A = 25^{\circ}C$ $T_A = -55^{\circ}C$, $+125^{\circ}C$	30 20	— —	40 25	— —	$V/\mu s$
	Settling Time	$ts(+)$ and $ts(-)$	—	800	—	800	ns
Noise (Referred to Input) Broadband	$N_i(BB)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_i(PC)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

- Bias currents are actually junction leakage currents which double (approximately) for each $10^{\circ}C$ increase in junction temperature T_j . Measurement of bias current is specified at T_j rather than T_A , since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms or 5 loop time constants after power is first applied to the device for test. Measurement at $T_A = -55^{\circ}C$ is not necessary since expected values are too small for typical test systems.
- Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:



- Negative I_B minimum limits reflect the characteristics of device with bias current compensation.
- CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and $-15V$.
- Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_j(max) \leq 175^{\circ}C$.
- Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

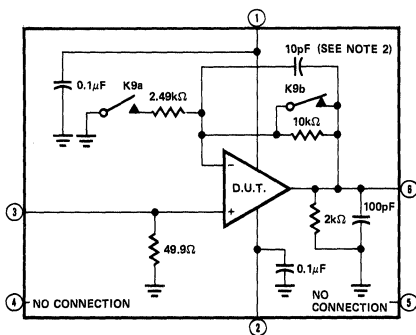

NOTES:

1. All resistors are $\pm 0.1\%$ tolerance and all capacitors are $\pm 10\%$ tolerance, unless otherwise specified.
2. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and change of state of relays (i.e. disable voltage supplies, current limit $\pm V_{CC}$, etc.).
3. Compensation capacitors should be added as required for test circuit stability. Two general methods for stability compensation exist. One method is with a capacitor for nulling amp feedback. The other method is with a capacitor in parallel with the $49.9k\Omega$ closed-loop feedback resistor. Both methods should not be used simultaneously. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations, etc. Loop response and

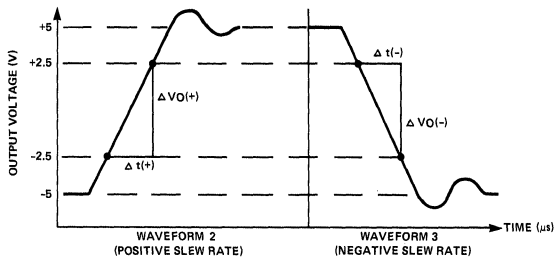
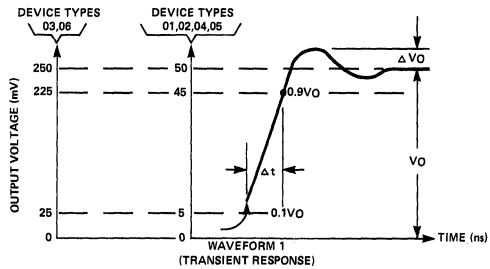
settling time shall be consistent with the test rate such that any value has settled for at least five loop time constants before the value is measured.

4. Adequate settling time should be allowed such that each parameter has settled to within 5% of its final value.
5. All relays are shown in the normal de-energized state.
6. The nulling amplifier shall be a M38510/10101XXX. Saturation of the nulling amplifier is not allowed on tests where the E (Pin 5) value is measured.
7. The load resistors 2050Ω and $11.1k\Omega$ yield effective load resistances of $2k\Omega$ and $10k\Omega$ respectively.
8. Any oscillation greater than 300mV in amplitude (peak-to-peak) shall be cause for device failure.

Figure 1. Test Circuit for Static Tests


NOTES:

1. Resistors are $\pm 1.0\%$ tolerance and capacitors are $\pm 10\%$ tolerance.
2. This capacitance includes the actual measured value with stray and wire capacitance.
3. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.



PARAMETER SYMBOL	DEVICE TYPE	INPUT PULSE SIGNAL AT $t_p \leq 50\text{ns}$	OUTPUT PULSE SIGNAL	EQUATION
TR (t_r)	ALL	+50mV	WAVEFORM 1	TR (t_r) = Δt
TR (O_S)	ALL	+50mV	WAVEFORM 1	TR (O_S) = $100 (\Delta V_O / V_O) \%$
SR (+)	01, 02, 04, 05 03, 06	-5V to +5V STEP -1V to +1V STEP	WAVEFORM 2 WAVEFORM 2	SR (+) = $\Delta V_O(+)/\Delta t(+)$
SR (-)	01, 02, 04, 05 03, 06	+5V to -5V STEP -1V to +1V STEP	WAVEFORM 3 WAVEFORM 3	SR (-) = $\Delta V_O(-)/\Delta t(-)$

Figure 2. Test Circuit for Transient Response and Slew Rate.

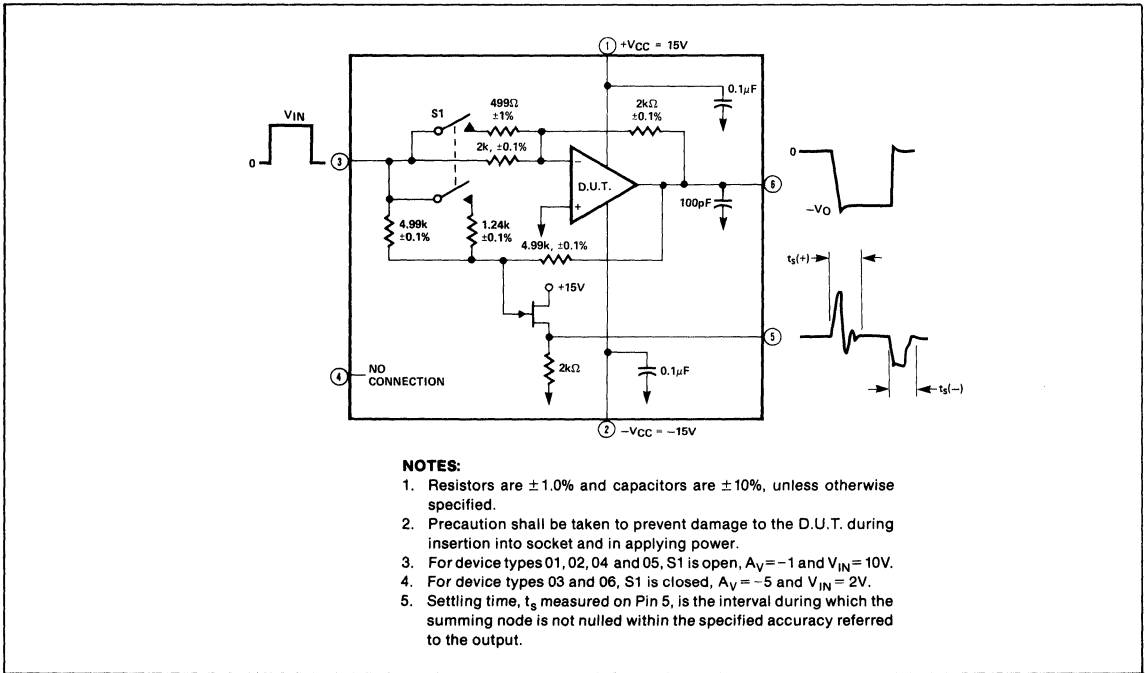


Figure 3. Test Circuit for Settling Time

BURN-IN

Devices supplied by PMI have been subjected to burn-in per Method 1015 of MIL-STD-883 using test condition C with circuit shown on Figure 4 or test condition F using circuit shown on Figure 5.

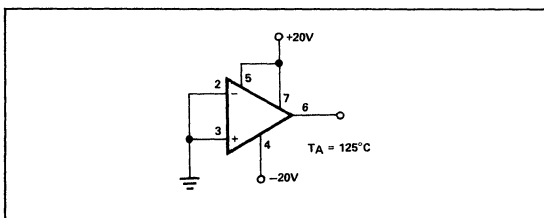


Figure 4. Test Circuit, Burn-In (Steady-State Power and Reverse Bias) and Operating Life Test

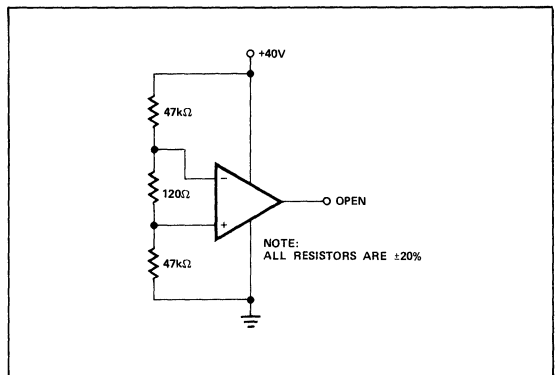


Figure 5. Accelerated Burn-In and Life Test Circuit

Precision Monolithics Inc.

FEATURES

- Low V_{OS} $25\mu V$
- Low V_{OS} Drift $0.6\mu V/^\circ C$
- Low Noise $0.6\mu V_{p-p}$
- Wide Supply Voltage Range $\pm 4.5V$ to $\pm 20V$

ORDERING INFORMATION

JAN SLASH SHEET	PMI DEVICE
JM38510/13501BPB	OP07AZ2/38510
JM38510/13502BPB	OP07Z2/38510
JM38510/13501BGC	OP07AJ1/38510
JM38510/13501BGA	OP07AJ3/38510
JM38510/13502BGC	OP07J1/38510

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low offset voltage, internally-compensated operational amplifier as specified in MIL-M-38510/135 for device type 01 and 02. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/135 for Class B processed devices.

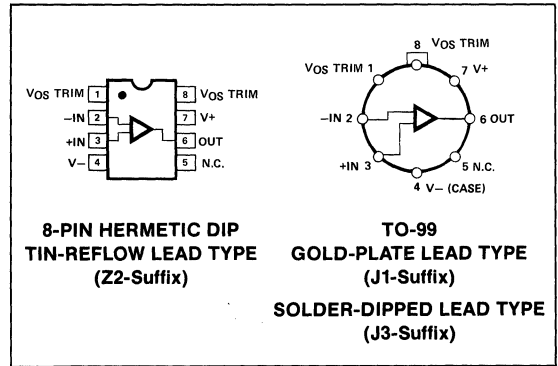
GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

MILITARY DEVICE TYPE	GENERIC-INDUSTRY TYPE
01	OP07A
02	OP07

For an 833-processed device with improved electrical specifications, review the OP-07 data sheet.

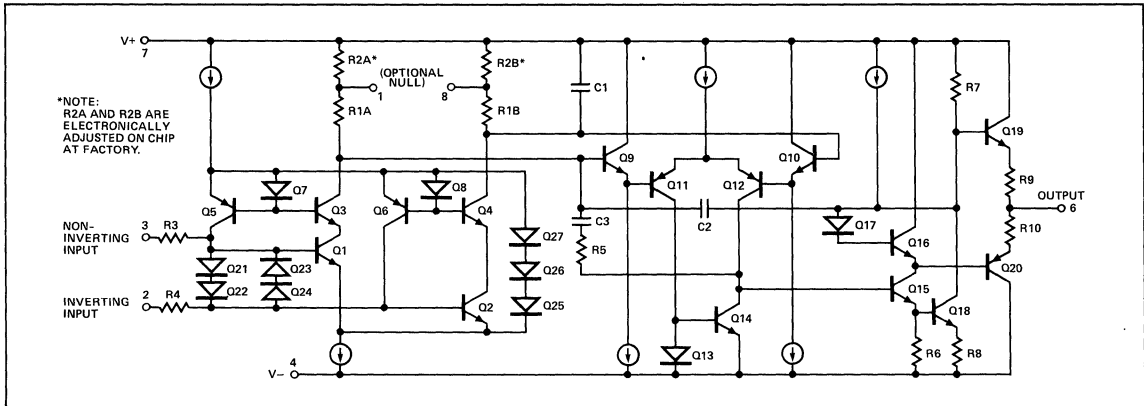
PIN CONNECTIONS



POWER AND THERMAL CHARACTERISTICS

Case Outline	Package	Maximum Allowable Power Dissipation	Maximum θ_{JC}	Maximum θ_{JA}
P	Dual-In-Line	208mW @ $T_A = 125^\circ C$	50°C/W	120°C/W
G	8-Lead CAN	167mW @ $T_A = 125^\circ C$	60°C/W	150°C/W

SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) $\pm 22V$
 Input Voltage Range (V_{IN}) $\pm V_{CC}$
 Differential Input Voltage Range $\pm 30V$
 Output Short-Circuit Duration (Note 1)
 Lead Temperature (Soldering, 60 sec) $+300^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Junction Temperature (T_J) $+150^{\circ}C$
 Maximum Power Dissipation (P_D) (Note 2) 500mW

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range $\pm 4.5V$ to $\pm 20V$
 Ambient Temperature Range $-55^{\circ}C$ to $+125^{\circ}C$

NOTES:

- Output may be shorted to ground indefinitely at $V_S = \pm 15V$, $T_A = 25^{\circ}C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.
- Maximum power dissipation versus ambient temperature.

ELECTRICAL CHARACTERISTICS at $\pm 4.5V \leq V_{CC} \leq \pm 20V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, $R_S = 50\Omega$ unnullified, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	$T_A = 25^{\circ}C$ (Notes 1, 2)	-25 -60	25 60	-75 -200	75 200	μV
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}/\Delta T$		-0.6	0.6	-1.3	1.3	$\mu V/^{\circ}C$
Input Bias Current	$+I_{IB}$	$T_A = 25^{\circ}C$ (Note 1)	-2 -4	2 4	-3 -6	3 6	nA
	$-I_{IB}$	$T_A = 25^{\circ}C$ (Note 1)	-2 -4	2 4	-3 -6	3 6	
Input Offset Current	I_{IO}	$T_A = 25^{\circ}C$ (Note 1)	-2 -4	2 4	-2.8 -5.6	2.8 5.6	nA
	$+PSRR$	$+V_{CC} = 20V$ to $5V$, $-V_{CC} = -15V$ $T_A = 25^{\circ}C$	—	10	—	10	
Power Supply Rejection Ratio	$-PSRR$	$+V_{CC} = 15V$, $-V_{CC} = -20V$ to $-5V$ $T_A = 25^{\circ}C$	—	10	—	10	$\mu V/V$
	$+PSRR$	$+V_{CC} = 20V$ to $5V$, $-V_{CC} = -15V$	—	20	—	20	
	$-PSRR$	$+V_{CC} = 15V$, $-V_{CC} = -20V$ to $-5V$	—	20	—	20	
	$PSRR$	$V_{CC} = \pm 4.5V$ to $\pm 20V$ $T_A = 25^{\circ}C$	—	10	—	10	
		$V_{CC} = \pm 4.5V$ to $\pm 20V$	—	20	—	20	

NOTES:

- Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
- Due to the inherent warm-up drift, testing shall occur no sooner than three (3) minutes after application of power.

5

OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS at $\pm 4.5V \leq V_{CC} \leq \pm 20V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, $R_S = 50\Omega$ unnullled, unless otherwise noted.
(Continued)

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$, $T_A = 25^{\circ}C$, $V_{CC} = \pm 15V$	110	—	110	—	dB
		$V_{CM} = \pm 13V$	106	—	106	—	
Adjustment for Input Offset	V_{IO} Adj (+)	$T_A = 25^{\circ}C$ (Note 1)	0.5	—	0.5	—	mV
	V_{IO} Adj (-)	$T_A = 25^{\circ}C$ (Note 1)	—	-0.5	—	-0.5	
Output Short-Circuit Current	$I_{OS(+)}$	$t \leq 25ms$ (Note 1, 3)	-65	—	-65	—	mA
		$t \leq 25ms$ (Note 1, 3)	—	65	—	65	
Supply Current	I_{CC}	$T_A = 25^{\circ}C$ (Note 1)	—	4	—	4	mA
			—	5	—	5	
Output Voltage Swing (Minimum)	V_{OP}	$R_L = 1k\Omega$, (Note 1)	-10	10	-10	10	V
		$R_L = 2k\Omega$, (Note 1)	-12	12	-12	12	
Open Loop Voltage Gain (Single-Ended)	A_{VS}	$T_A = 25^{\circ}C$ (Note 2)	300	—	200	—	V/mV
			200	—	150	—	
Slew Rate	$SR(+)$, $SR(-)$	$V_{IN} = 10V$, $T_A = 25^{\circ}C$, (Note 1)	.08	—	.08	—	V/ μ s
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	18	—	18	nV/ \sqrt{Hz}
		$f_O = 100Hz$	—	14	—	14	
		$f_O = 1kHz$	—	12	—	12	
Low Frequency Input Noise Voltage	e_{np-p}	$f = 0.1Hz$ to $10Hz$, $T_A = 25^{\circ}C$, (Note 1)	—	0.6	—	0.6	μ V _{p-p}

NOTES:

1. Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
2. $V_{OUT} = 0$ to $+10V$ for $A_{VS}(+)$ and $V_{OUT} = 0$ to $-10V$ for $A_{VS}(-)$. $R_L = 2,000\Omega$.
3. Continuous short-circuit limits are considerably less than the indicated test limits, since maximum power dissipation cannot be exceeded.



JM38510/13503

LOW-NOISE PRECISION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low V_{OS} $25\mu V$
- Low V_{OS} Drift $0.6\mu V/^\circ C$
- High Speed $1.7V/\mu s$
- Low Noise $0.18\mu V_{p-p}$
- High Gain **1.0 Million**
- Wide Supply Voltage Range $\pm 4.5V$ to $\pm 18V$

ORDERING INFORMATION

JAN SLASH SHEET	PMI DEVICE
JM38510/13503BPC	OP27AZ2/38510
JM38510/13503BGC	OP27AJ1/38510

GENERAL DESCRIPTION

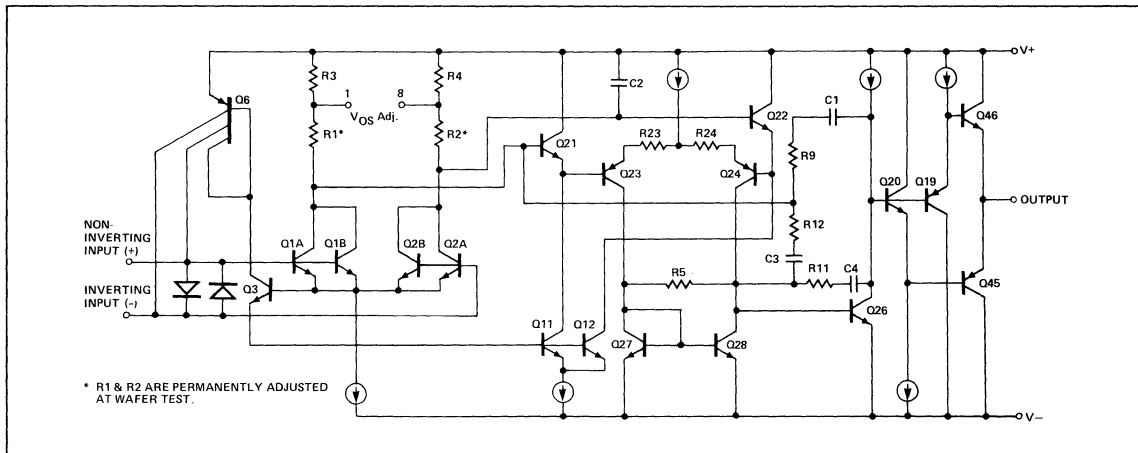
This data sheet covers the electrical requirements for a monolithic, low offset voltage, internally-compensated operational amplifier as specified in MIL-M-38510/135 for device type 03. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/135 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

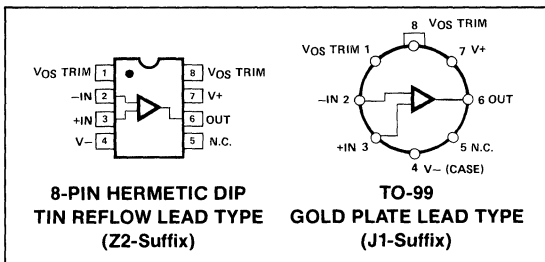
SIMPLIFIED SCHEMATIC



MILITARY DEVICE TYPE	GENERIC-INDUSTRY TYPE
03	OP27A

For an 833-processed device with improved electrical specifications, review the OP-27 data sheet.

PIN CONNECTIONS



POWER AND THERMAL CHARACTERISTICS

Case Outline	Package	Maximum Allowable Power Dissipation	Maximum θ_{JC}	Maximum θ_{JA}
P	Dual-In-Line	208mW @ $T_A = 125^\circ C$	50°C/W	120°C/W
G	8-Lead CAN	167mW @ $T_A = 125^\circ C$	60°C/W	150°C/W

5
OPERATIONAL AMPLIFIERS

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (V_{CC})	$\pm 22V$
Input Voltage Range (V_{IN})	$\pm V_{CC}$
Differential Input Voltage Range	$\pm 0.7V$
Output Short-Circuit Duration (Note 1)	
Lead Temperature (Soldering, 60 sec)	$+300^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature (T_J)	$+150^{\circ}C$
Maximum Power Dissipation (P_D) (Note 2)	500mW

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	$\pm 4.5V$ to $\pm 18V$
Ambient Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$

NOTES:

- Output may be shorted to ground indefinitely at $V_S = \pm 15V$, $T_A = 25^{\circ}C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.
- Maximum power dissipation versus ambient temperature.

ELECTRICAL CHARACTERISTICS at $\pm 4.5V \leq V_{CC} \leq \pm 20V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, $R_S = 50\Omega$ unnull'd, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	03 LIMITS		UNITS
			MIN	MAX	
Input Offset Voltage	V_{IO}	$T_A = 25^{\circ}C$ (Notes 1, 2)	-25 -60	25 60	μV
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}/\Delta T$		-0.6	0.6	$\mu V/^{\circ}C$
Input Bias Current	$+I_{IB}$	$T_A = 25^{\circ}C$ (Note 1)	-40 -60	40 60	nA
	$-I_{IB}$	$T_A = 25^{\circ}C$ (Note 1)	-40 -60	40 60	
Input Offset Current	I_{IO}	$T_A = 25^{\circ}C$ (Note 1)	-35 -50	35 50	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 18V$ to $5V$, $-V_{CC} = -15V$ $T_A = 25^{\circ}C$	—	10	$\mu V/V$
	-PSRR	$+V_{CC} = 15V$, $-V_{CC} = -18V$ to $-5V$ $T_A = 25^{\circ}C$	—	10	
	+PSRR	$+V_{CC} = 18V$ to $5V$, $-V_{CC} = -15V$	—	16	
	-PSRR	$+V_{CC} = 15V$, $-V_{CC} = -18V$ to $-5V$	—	16	
	PSRR	$V_{CC} = \pm 4.5V$ to $\pm 18V$ $T_A = 25^{\circ}C$	—	10	
		$V_{CC} = \pm 4.5V$ to $\pm 18V$	—	16	

NOTES:

- Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
- Due to the inherent warm-up drift, testing shall occur no sooner than three (3) minutes after application of power.



ELECTRICAL CHARACTERISTICS at $\pm 4.5V \leq V_{CC} \leq \pm 20V$ and $-55^\circ C \leq T_A \leq 125^\circ C$, $R_S = 50\Omega$ unnullled, unless otherwise noted.
(Continued)

PARAMETER	SYMBOL	CONDITIONS	03 LIMITS		UNITS
			MIN	MAX	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$, $T_A = 25^\circ C$, $V_{CC} = \pm 15V$	114	—	dB
		$V_{CM} = \pm 11V$, $V_{CC} = \pm 15V$	108	—	
Adjustment for Input Offset	V_{IO} Adj (+)	$T_A = 25^\circ C$, (Note 1)	0.5	—	mV
	V_{IO} Adj (-)	$T_A = 25^\circ C$, (Note 1)	—	-0.5	
Output Short-Circuit Current	$I_{OS(+)}$	$t \leq 25ms$, (Note 1,3)	-60	—	mA
	$I_{OS(-)}$	$t \leq 25ms$, (Note 1,3)	—	70	
Supply Current	I_{CC}	$T_A = 25^\circ C$	—	4	mA
		(Note 1)	—	5	
Output Voltage Swing (Minimum)	V_{OP}	$R_L = 600\Omega$, (Note 1)	-10	10	V
		$R_L = 2k\Omega$, (Note 1)	-11.5	11.5	
Open Loop Voltage Gain (Single-Ended)	A_{VS}	$T_A = 25^\circ C$	1000	—	V/mV
		(Note 2)	600	—	
Slew Rate	$SR(+)$, $SR(-)$	$V_{IN} = 10V$, $T_A = 25^\circ C$, (Note 1)	1.7	—	V/ μs
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	5.5	nV/ \sqrt{Hz}
		$f_O = 100Hz$	—	4.0	
		$f_O = 1kHz$	—	3.8	
Low Frequency Input Noise Voltage	e_{np-p}	$f = 0.1Hz$ to $10Hz$ $T_A = 25^\circ C$, (Note 1)	—	0.18	μV_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	4.0	pA/ \sqrt{Hz}
		$f_O = 100Hz$	—	1.5	
		$f_O = 1kHz$	—	0.8	

NOTES:

1. Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
2. $V_{OUT} = 0$ to $+10V$ for $A_{VS}(+)$ and $V_{OUT} = 0$ to $-10V$ for $A_{VS}(-)$. $R_L = 2,000\Omega$.
3. Continuous short-circuit limits are considerably less than the indicated test limits, since maximum power dissipation cannot be exceeded.

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



INSTRUMENTATION AMPLIFIER

Precision Monolithics Inc.

6-3 Introduction

6-3 Definitions

6-5 **AMP-01**

Low-Noise Precision
Instrumentation Amplifier

6-27 **AMP-05**

Fast-Settling JFET
Instrumentation Amplifier



INSTRUMENTATION AMPLIFIER

Precision Monolithics Inc.

INTRODUCTION

An instrumentation amplifier is a committed gain block that amplifies a differential input voltage by a precisely set gain. Voltages common to both inputs are rejected. Differential gain is set by one or two external resistors, usually over a range of 1 to 1000. Instrumentation amplifiers are designed to have very high input impedance; this assures that the gain will not be affected by signal-source impedances (R_S). Input bias current must be low to minimize input offset voltages due to $I_B \times R_S$. In the output stage, low output impedance keeps the output voltage from being affected by the load impedance. Instrumentation amplifiers employ heavy negative feedback which provides excellent gain linearity even at high gains.

Most instrumentation amplifiers have an output sense pin (SENSE) and a reference input pin (REFERENCE). As shown in Figure 1, the load is usually connected between SENSE and REFERENCE points. The amplifier will make $V_{OUT} = G V_{IN}$ despite voltage drops between OUTPUT and LOAD, or from REFERENCE to GROUND. The SENSE and REFERENCE inputs are particularly useful for driving remote loads with high currents. The essential characteristics of instrumentation amplifiers—high input impedance, low output impedance, low offset, high linearity, stable gain, and ability to reject common-mode inputs—make them very useful for amplifying low-level transducer outputs. Transducers such as thermocouples, strain-gage bridges, biological probes, and current shunts produce small differential signals superimposed on common-mode bias voltages. In addition, common-mode ground noise is usually prevalent. Instrumentation amplifiers are gain blocks that have been optimized for preamplifying low-level transducer signals in the presence of common-mode noise.

The PMI AMP-01 instrumentation amplifier has all the features needed for use in high-accuracy data-acquisition systems and high-performance instruments:

- Wide Gain Range ($0.1 \leq G \leq 10,000$)
- High Input Impedance

- Low Input Bias Current
- Low Offsets
- Excellent Linearity

Unlike conventional instrumentation amplifiers, the AMP-01 has high output drive capability; it can supply $\pm 10V$ at $\pm 50mA$. This enhanced output drive capability enables the AMP-01 to drive unusually large capacitive loads without encountering stability problems.

Gain of the AMP-01 is set by the ratio of two external resistors according to:

$$V_{OUT} = \left(\frac{20 \times R_{SCALE}}{R_{GAIN}} \right) V_{IN}$$

Output sense and reference points are provided. The AMP-01 is unusually versatile, and can be connected as a precision current source or high-performance op amp as well as a conventional instrumentation amplifier.

The AMP-05 JFET instrumentation amplifier supports high-speed applications, such as analog-multiplexed data acquisition and fast analog signal processing. The design offers a $10\mu s$ maximum settling-time to 12 bits at gains up to 1000, and with 14-bit linearity. The AMP-05 also provides on-board circuits for guard driving, which maximizes input signal speed, and a precision current source for transducer or reference excitation.

AMP-05 features include:

- Input bias current, 25pA max.
- High gain-bandwidth product, 200MHz
- $6V/\mu s$ output slew-rate with a 1000pF load
- High common-mode rejection, 110dB min.

DEFINITIONS

Voltage Offsets — Offset at the output of an instrumentation amplifier consists of two terms, a gain-dependent input-offset-voltage and a gain-independent output-offset-voltage. Total offset is the sum of the unity-gain-output-offset (V_{OOS}) plus input-offset (V_{IOS}) multiplied by the gain (Output Offset = $V_{OOS} + G V_{IOS}$). At high gain, the input offset term dominates. For the AMP-01 and AMP-05, both input and output offsets can be trimmed externally if desired.

6

INSTRUMENTATION AMPLIFIERS

Power Supply Rejection — Offset changes with variations in the power supply voltages. The ability of the instrumentation amplifier to reject fluctuations in power supply voltage is referred to as “power supply rejection”. It varies with gain and is different for the positive and negative supplies. The offset change referred-to-input (RTI) is usually specified in dB form. For example, a PSR of 100dB at a gain of 1000 would imply an input-offset-voltage change of $10\mu\text{V}$ -per-volt of power supply change. The output offset change-per-volt of power-supply change would be 10mV. PSR in the specification tables is measured at DC.

Input Bias Current — The input bias currents are currents flowing into (or out of) the two inputs of the amplifier. The value given in the specification table is the maximum current into either input. Input offset current is the difference between the two input bias currents.

Input Voltage Range — The linear operating range of the amplifier is referred to as the “input voltage range”. When operating at high gains with small differential inputs, this input range is the common-mode input voltage range.

Common-Mode Rejection — Common-mode rejection (CMR) specifies the amplifiers ability

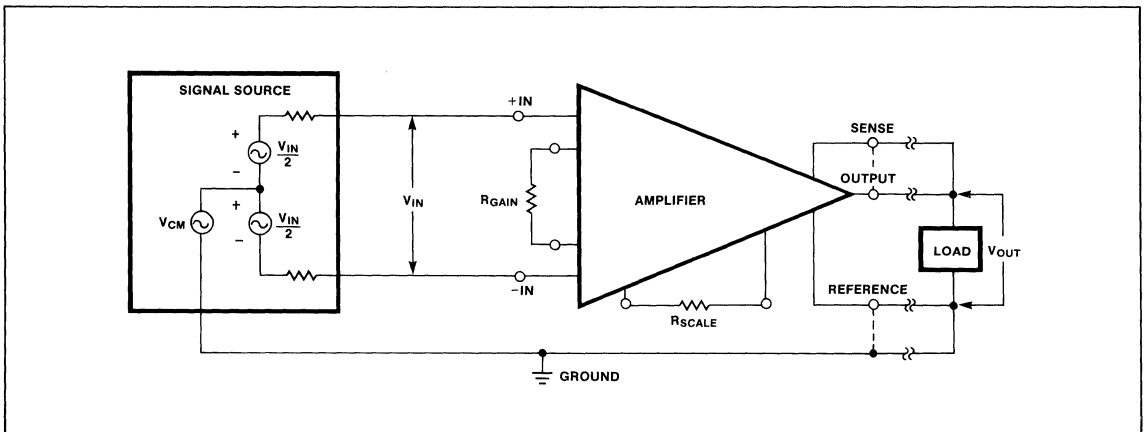
to reject common-mode inputs. The ratio of change in output voltage to a change in common-mode input voltage is the common-mode gain ($\Delta V_O/\Delta V_{CM}$). The ratio of differential gain (G) to common-mode gain (A_{CM}) is defined as common-mode rejection ratio (CMRR). The CMR is conventionally specified in log form; $\text{CMR} = 20 \log_{10} \text{CMRR}$.

Since instrumentation amplifiers are designed to amplify differential signals while rejecting common-mode inputs, common-mode gain stays essentially independent of gain setting. Therefore, CMRR increases almost directly with the gain setting.

As an example, consider a CMR of 120dB at a gain of 1000 with a common-mode input range of $\pm 10\text{V}$. The 120dB of CMR implies a CMRR of $1000/A_{CM} = 1,000,000$, or a common-mode gain of $1/1000$. A $\pm 10\text{V}$ common-mode input will cause an output change of $\pm 10\text{mV}$ for this example ($\text{CMR} = 120\text{dB}$, $G = 1000$).

Gain Equation Accuracy — Differential gain is given as a function of the two external resistors. For the AMP-01 and AMP-05, the relationship is ideally $20 \times R_S/R_G$. The specified accuracy limits indicate the accuracy of the amplifier given an exact ratio of R_S/R_G .

INSTRUMENTATION AMPLIFIER FUNCTIONAL DIAGRAM

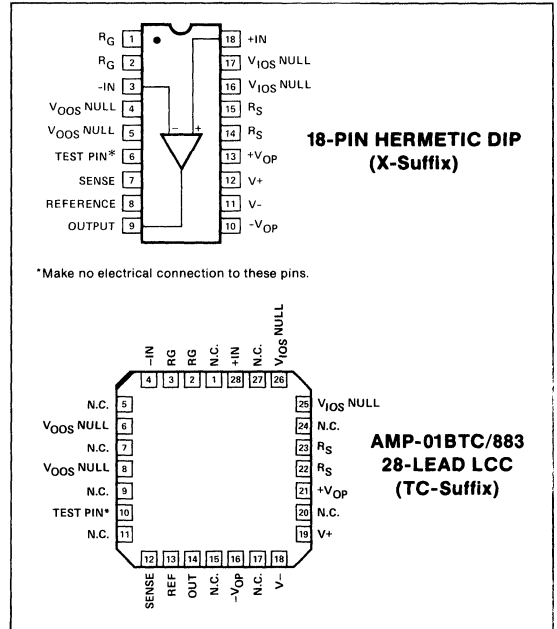


Precision Monolithics Inc.

FEATURES

- Low Offset Voltage 50 μ V Max
- Very Low Offset Voltage Drift 0.3 μ V/ $^{\circ}$ C Max
- Low Noise 0.12 μ V_{p-p} (0.1Hz to 10Hz)
- Excellent Output Drive \pm 10V at \pm 50mA
- Capacitive Load Stability to 1 μ F
- Gain Range 0.1 to 10,000
- Excellent Linearity 16-Bit at G = 1000
- High CMR 125dB Min (G = 1000)
- Low Bias Current 3nA Max
- May be Configured as a Precision Op-Amp
- Output-Stage Thermal Shutdown

PIN CONNECTIONS



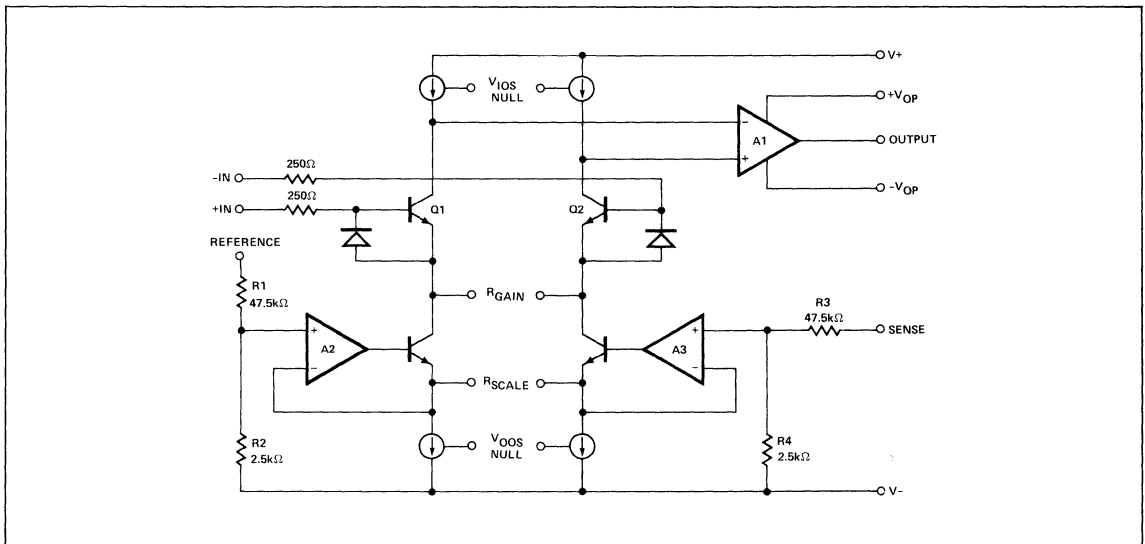
ORDERING INFORMATION†

PACKAGE		OPERATING TEMPERATURE RANGE
CERDIP 18-PIN	LCC	
AMP01AX*	AMP01BTC/883	MIL
AMP01BX*		MIL
AMP01EX		IND
AMP01FX		IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

SIMPLIFIED SCHEMATIC



Manufactured under the following U.S. patents: 4,471,321 and 4,503,381.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A			AMP-01B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	20	50	—	40	100	μV
Input Offset Voltage Drift	TCV_{IOS}	$-55^\circ C \leq T_A \leq +125^\circ C$	—	0.15	0.3	—	0.3	1.0	$\mu V/^\circ C$
Output Offset Voltage	V_{OOS}	$T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	1	3	—	2	6	mV
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$ (Note 3) $-55^\circ C \leq T_A \leq +125^\circ C$	—	20	50	—	50	120	$\mu V/^\circ C$
Offset Referred to Input vs. Positive Supply $V_+ = +5V$ to $+15V$	PSR	$G = 1000$	120	130	—	110	120	—	dB
		$G = 100$	110	130	—	100	120	—	
		$G = 10$	95	110	—	90	100	—	
		$G = 1$	75	90	—	70	80	—	
Offset Referred to Input vs. Negative Supply $V_- = -5V$ to $-15V$	PSR	$G = 1000$	110	125	—	105	115	—	dB
		$G = 100$	95	105	—	90	95	—	
		$G = 10$	75	85	—	70	75	—	
		$G = 1$	55	65	—	50	60	—	
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	± 6	—	—	± 6	—	mV
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	± 100	—	—	± 100	—	mV
INPUT CURRENT									
Input Bias Current	I_B	$T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	1	3	—	2	6	nA
Input Bias Current Drift	TCI_B	$-55^\circ C \leq T_A \leq +125^\circ C$	—	40	—	—	50	—	$pA/^\circ C$
Input Offset Current	I_{OS}	$T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	0.2	1.0	—	0.5	2.0	nA
Input Offset Current Drift	TCI_{OS}	$-55^\circ C \leq T_A \leq +125^\circ C$	—	3	—	—	5	—	$pA/^\circ C$
INPUT									
Input Resistance	R_{IN}	Differential, $G = 1000$	—	1	—	—	1	—	G Ω
		Differential, $G \leq 100$	—	10	—	—	10	—	
		Common-Mode, $G = 1000$	—	20	—	—	20	—	
Input Voltage Range	IVR	$T_A = 25^\circ C$ (Note 2)	± 10.5	—	—	± 10.5	—	—	V
		$-55^\circ C \leq T_A \leq +125^\circ C$	± 10.0	—	—	± 10.0	—	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$, $1k\Omega$ source imbalance							dB
		$G = 1000$	125	130	—	115	125	—	
		$G = 100$	120	130	—	110	125	—	
		$G = 10$	100	120	—	95	110	—	
		$G = 1$	85	100	—	75	90	—	
		$-55^\circ C \leq T_A \leq +125^\circ C$							
		$G = 1000$	120	125	—	110	120	—	dB
		$G = 100$	115	125	—	105	120	—	
		$G = 10$	95	115	—	90	105	—	
		$G = 1$	80	95	—	75	90	—	

NOTES:

1. V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS} , respectively.

2. Refer to section on common-mode rejection.

3. AMP-01AX specification changed from $100\mu V/^\circ C$ to $50\mu V/^\circ C$, effective January, 1985.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01E			AMP-01F			UNITS		
			MIN	TYP	MAX	MIN	TYP	MAX			
OFFSET VOLTAGE											
Input Offset Voltage	V_{IOS}	$T_A = 25^\circ C$ $-25^\circ C \leq T_A \leq +85^\circ C$	—	20	50	—	40	100	μV		
Input Offset Voltage Drift	TCV_{IOS}	$-25^\circ C \leq T_A \leq +85^\circ C$, (Note 2)	—	0.15	0.3	—	0.3	1.0	$\mu V/^\circ C$		
Output Offset Voltage	V_{OOS}	$T_A = 25^\circ C$ $-25^\circ C \leq T_A \leq +85^\circ C$	—	1	3	—	2	6	mV		
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$, (Note 2) $-25^\circ C \leq T_A \leq +85^\circ C$	—	20	100	—	50	120	$\mu V/^\circ C$		
Offset Referred to Input vs. Positive Supply $V+ = +5V$ to $+15V$	PSR	$G = 1000$	120	130	—	110	120	—	dB		
		$G = 100$	110	130	—	100	120	—			
		$G = 10$	95	110	—	90	100	—			
		$G = 1$	75	90	—	70	80	—			
				$-25^\circ C \leq T_A \leq +85^\circ C$	120	130	—	110	120	—	dB
				$G = 100$	110	130	—	100	120	—	
				$G = 10$	95	110	—	90	100	—	
				$G = 1$	75	90	—	70	80	—	
Offset Referred to Input vs. Negative Supply $V- = -5V$ to $-15V$	PSR	$G = 1000$	110	125	—	105	115	—	dB		
		$G = 100$	95	105	—	90	95	—			
		$G = 10$	75	85	—	70	75	—			
		$G = 1$	55	65	—	50	60	—			
				$-25^\circ C \leq T_A \leq +85^\circ C$	110	125	—	105	115	—	dB
				$G = 100$	95	105	—	90	95	—	
				$G = 10$	75	85	—	70	75	—	
				$G = 1$	55	65	—	50	60	—	
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	± 6	—	—	± 6	—	mV		
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	± 100	—	—	± 100	—	mV		
INPUT CURRENT											
Input Bias Current	I_B	$T_A = 25^\circ C$ $-25^\circ C \leq T_A \leq +85^\circ C$	—	1	3	—	2	6	nA		
Input Bias Current Drift	TCI_B	$-25^\circ C \leq T_A \leq +85^\circ C$	—	40	—	—	50	—	$pA/^\circ C$		
Input Offset Current	I_{OS}	$T_A = 25^\circ C$ $-25^\circ C \leq T_A \leq +85^\circ C$	—	0.2	1.0	—	0.5	2.0	nA		
Input Offset Current Drift	TCI_{OS}	$-25^\circ C \leq T_A \leq +85^\circ C$	—	3	—	—	5	—	$pA/^\circ C$		
INPUT											
Input Resistance	R_{IN}	Differential, $G = 1000$	—	1	—	—	1	—	G Ω		
		Differential, $G \leq 100$	—	10	—	—	10	—			
		Common-Mode, $G = 1000$	—	20	—	—	20	—			
Input Voltage Range	IVR	$T_A = 25^\circ C$ (Note 3)	± 10.5	—	—	± 10.5	—	—	V		
		$-25^\circ C \leq T_A \leq +85^\circ C$	± 10.0	—	—	± 10.0	—	—			
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$, $1k\Omega$ source imbalance							dB		
		$G = 1000$	125	130	—	115	125	—			
		$G = 100$	120	130	—	110	125	—			
		$G = 10$	100	120	—	95	110	—			
				$G = 1$	85	100	—	75	90	—	dB
				$-25^\circ C \leq T_A \leq +85^\circ C$	120	125	—	110	120	—	
				$G = 100$	115	125	—	105	120	—	
				$G = 10$	95	115	—	90	105	—	
		$G = 1$	80	95	—	75	90	—			

NOTES:

- V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS} , respectively.
- Sample tested.
- Refer to section on common-mode rejection.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E			AMP-01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
GAIN									
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$ Accuracy Measured from $G = 1$ to 1000	—	0.3	0.6	—	0.5	0.8	%
Gain Range	G		0.1	—	10k	0.1	—	10k	V/V
Nonlinearity		G = 1000	—	0.0007	0.005	—	0.0007	0.005	%
		G = 100 (Note 1)	—	—	0.005	—	—	0.005	
		G = 10	—	—	0.005	—	—	0.007	
		G = 1	—	—	0.010	—	—	0.015	
Temperature Coefficient	G_{TC}	$1 \leq G \leq 1000$ (Notes 1, 2)	—	5	10	—	5	15	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	± 13.0	± 13.8	—	± 13.0	± 13.8	—	V
		$R_L = 500\Omega$	± 13.0	± 13.5	—	± 13.0	± 13.5	—	
		$R_L = 50\Omega$	± 2.5	± 4.0	—	± 2.5	± 4.0	—	
		$R_L = 2k\Omega$ Over Temp. $R_L = 500\Omega$ (Note 3)	± 12.0	± 13.8	—	± 12.0	± 13.8	—	
Positive Current Limit		Output-to-Ground Short	60	100	120	60	100	120	mA
Negative Current Limit		Output-to-Ground Short	60	90	120	60	90	120	mA
Capacitive Load Stability		$1 \leq G \leq 1000$ No Oscillations, (Note 1)	0.1	1	—	0.1	1	—	μF
Thermal Shutdown Temperature		Junction Temperature	—	165	—	—	165	—	°C
NOISE									
Voltage Density, RTI	e_n	$f_O = 1kHz$	—	5	—	—	5	—	nV/\sqrt{Hz}
		G = 1000	—	10	—	—	10	—	
		G = 100	—	59	—	—	59	—	
		G = 10	—	540	—	—	540	—	
		G = 1	—	540	—	—	540	—	
Noise Current Density, RTI	i_n	$f_O = 1kHz, G = 1000$	—	0.15	—	—	0.15	—	pA/\sqrt{Hz}
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.12	—	—	0.16	—	μV_{p-p}
		G = 1000	—	0.16	—	—	0.16	—	
		G = 100	—	1.4	—	—	1.4	—	
		G = 10	—	13	—	—	13	—	
		G = 1	—	13	—	—	13	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz, G = 1000	—	2	—	—	2	—	pA_{p-p}
DYNAMIC RESPONSE									
Small-Signal Bandwidth (-3dB)	BW	G = 1	—	570	—	—	570	—	kHz
		G = 10	—	100	—	—	100	—	
		G = 100	—	82	—	—	82	—	
		G = 1000	—	26	—	—	26	—	
		G = 1000	—	26	—	—	26	—	
Slew Rate	SR	G = 10	3.5	4.5	—	3.0	4.5	—	V/ μs
Settling Time	t_s	To 0.01%, 20V step	—	12	—	—	12	—	μs
		G = 1	—	13	—	—	13	—	
		G = 10	—	15	—	—	15	—	
		G = 100	—	50	—	—	50	—	
		G = 1000	—	50	—	—	50	—	

NOTES:

- Guaranteed by design.
- Gain tempco does not include the effects of gain and scale resistor tempco match.
- $-55^\circ C \leq T_A \leq +125^\circ C$ for A/B grades, $-25^\circ C \leq T_A \leq +85^\circ C$ for E/F grades.

6
INSTRUMENTATION AMPLIFIERS



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

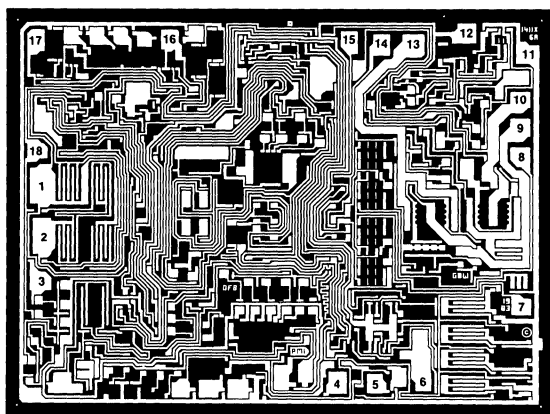
PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E			AMP-01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SENSE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	$k\Omega$
Input Current	I_{IN}	Referenced to V^-	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	-10.5	—	+15	-10.5	—	+15	V
REFERENCE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	$k\Omega$
Input Current	I_{IN}	Referenced to V^-	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	-10.5	—	+15	-10.5	—	+15	V
Gain to Output			—	1	—	—	1	—	V/V
POWER SUPPLY $-25^\circ C \leq T_A \leq +85^\circ C$ for E/F Grades, $-55^\circ C \leq T_A \leq +125^\circ C$ for A/B Grades									
Supply Voltage Range	V_S	+V linked to V_{OP} -V linked to $-V_{OP}$	± 4.5	—	± 18	± 4.5	—	± 18	V
Quiescent Current	I_Q	+V linked to V_{OP} -V linked to $-V_{OP}$	—	3.0	4.8	—	3.0	4.8	mA

NOTE:

1. Guaranteed by design.



DICE CHARACTERISTICS



DIE SIZE 0.110 × 0.148 inch, 16,280 sq. mils
(2.79 × 3.76 mm, 10.50 sq. mm)

- | | |
|-------------------|--------------------|
| 1. R_G | 10. V^- (OUTPUT) |
| 2. R_G | 11. V^- |
| 3. $-$ INPUT | 12. V^+ |
| 4. V_{OOS} NULL | 13. V^+ (OUTPUT) |
| 5. V_{OOS} NULL | 14. R_S |
| 6. TEST PIN* | 15. R_S |
| 7. SENSE | 16. V_{IOS} NULL |
| 8. REFERENCE | 17. V_{IOS} NULL |
| 9. OUTPUT | 18. $+$ INPUT |

* Make no electrical connection

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01NBC LIMIT	AMP-01GBC LIMIT	UNITS
Input Offset Voltage	V_{IOS}		60	120	μV MAX
Output Offset Voltage	V_{OOS}		4	8	mV MAX
Offset Referred to Input vs. Positive Supply	PSR	$V^+ = +5V$ to $+15V$			
		$G = 1000$	120	110	dB MIN
		$G = 100$	110	100	
		$G = 10$	95	90	
$G = 1$	75	70			
Offset Referred to Input vs. Negative Supply	PSR	$V^- = -5V$ to $-15V$			
		$G = 1000$	110	105	dB MIN
		$G = 100$	95	90	
		$G = 10$	75	70	
$G = 1$	55	50			
Input Bias Current	I_B		4	8	nA MAX
Input Offset Current	I_{OS}		1	3	nA MAX
Input Voltage Range	IVR	Guaranteed by CMR Tests	± 10	± 10	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$			
		$G = 1000$	125	115	dB MIN
		$G = 100$	120	110	
		$G = 10$	100	95	
$G = 1$	85	75			
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$	0.6	0.8	% MAX
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	± 13	± 13	V MIN
		$R_L = 500\Omega$	± 13	± 13	
		$R_L = 50\Omega$	± 2.5	± 2.5	
Output-Current Limit		Output-to-Ground Short	± 60	± 60	mA MIN
Output-Current Limit		Output-to-Ground Short	± 120	± 120	mA MAX
Quiescent Current	I_Q	$+V$ Linked to $+V_{OP}$ $-V$ Linked to $-V_{OP}$	4.8	4.8	mA MAX

NOTE:

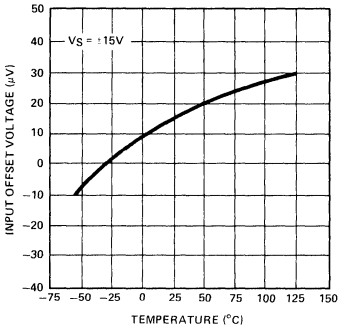
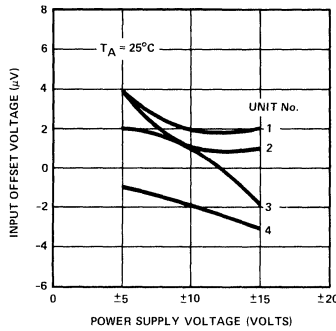
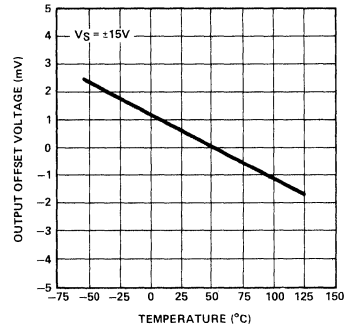
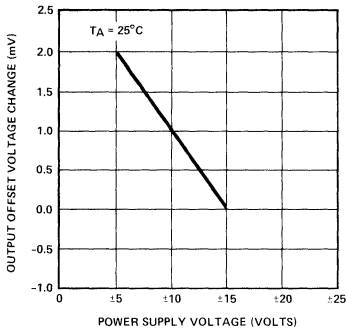
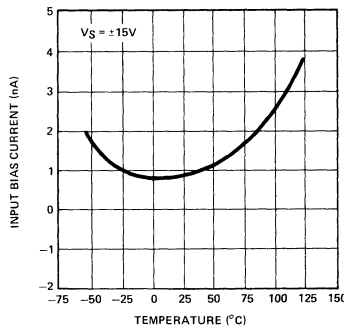
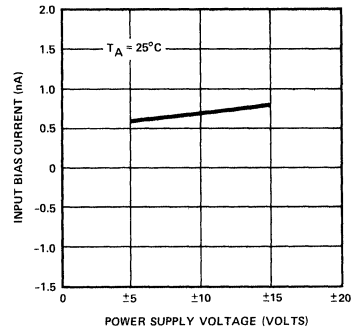
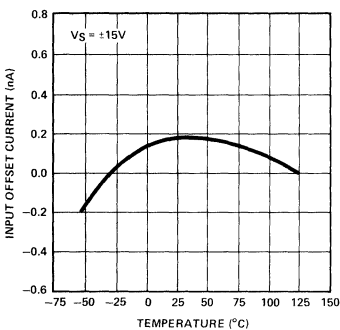
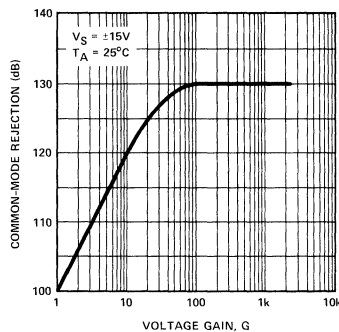
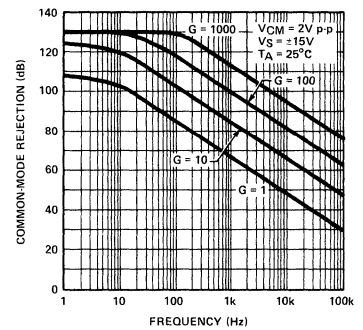
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01NBC TYPICAL	AMP-01GBC TYPICAL	UNITS
Input Offset Voltage Drift	TCV_{IOS}		0.15	0.30	$\mu V/^\circ C$
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$	20	50	$\mu V/^\circ C$
Input Bias Current Drift	TCI_B		40	50	$pA/^\circ C$
Input Offset Current Drift	TCI_{OS}		3	5	$pA/^\circ C$
Nonlinearity		$G = 1000$	0.0007	0.0007	%
Voltage Noise Density	e_n	$G = 1000$ $f_G = 1kHz$	5	5	nV/\sqrt{Hz}
Current Noise Density	i_n	$G = 1000$ $f_G = 1kHz$	0.15	0.15	pA/\sqrt{Hz}
Voltage Noise	e_{np-p}	$G = 1000$ 0.1Hz to 10Hz	0.12	0.12	μV_{p-p}
Current Noise	i_{np-p}	$G = 1000$ 0.1Hz to 10Hz	2	2	pA_{p-p}
Small-Signal Bandwidth (-3dB)	BW	$G = 1000$	26	26	kHz
Slew Rate	SR	$G = 10$	4.5	4.5	$V/\mu s$
Settling Time	t_s	To 0.01%, 20V Step $G = 1000$	50	50	μs

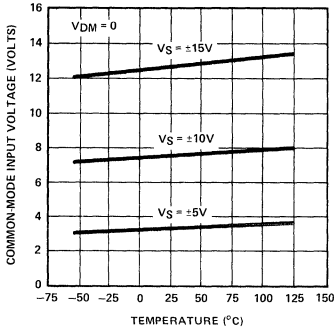
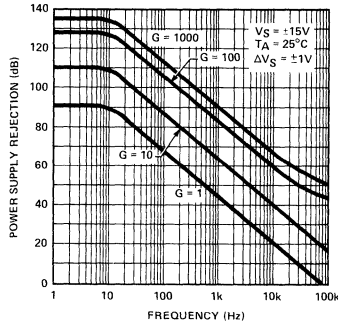
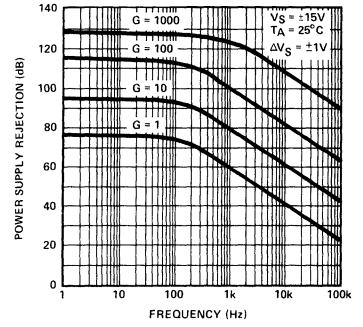
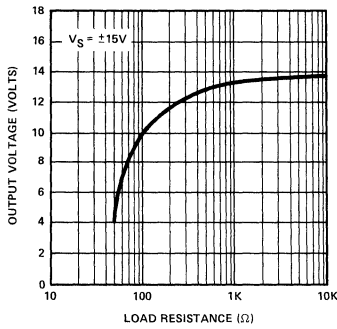
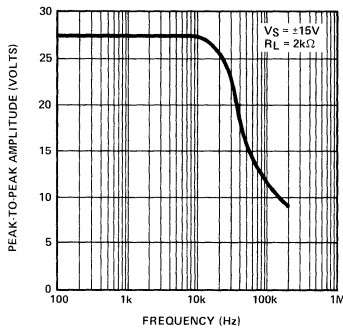
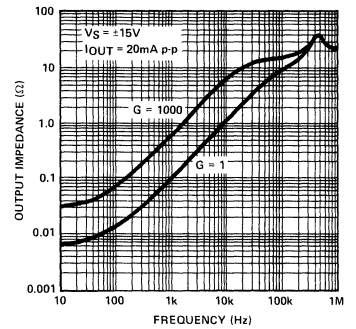
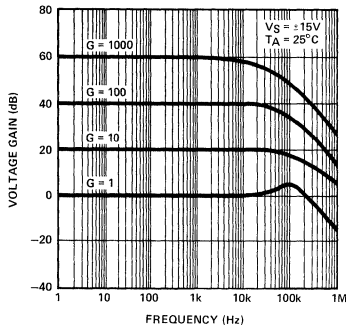
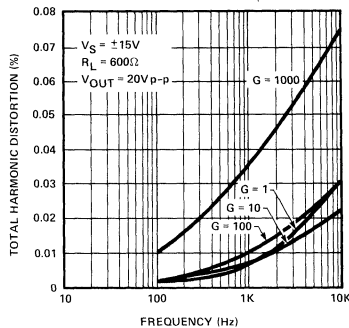
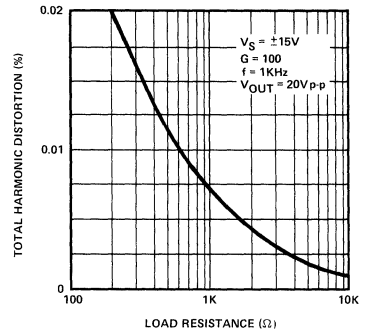
TYPICAL PERFORMANCE CHARACTERISTICS

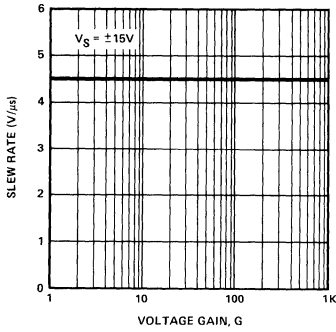
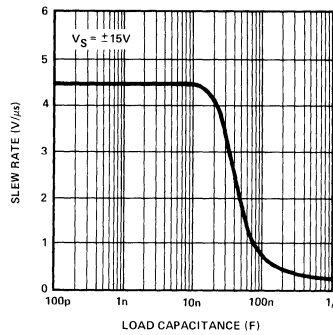
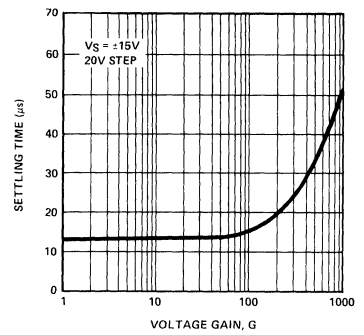
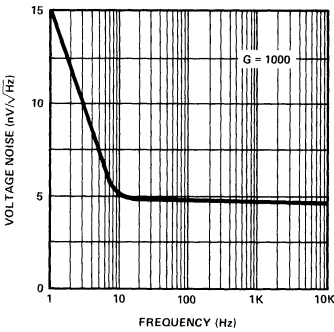
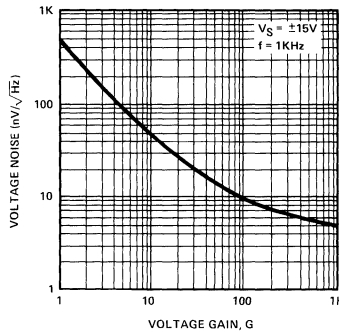
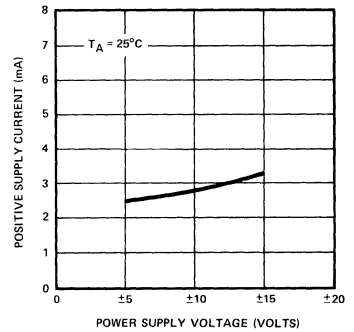
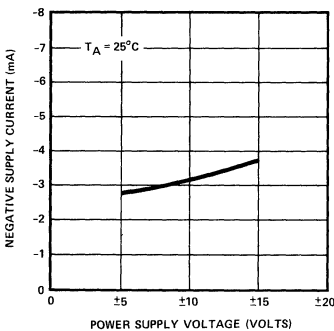
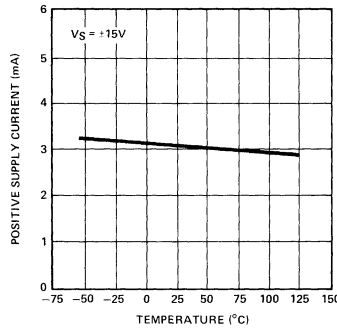
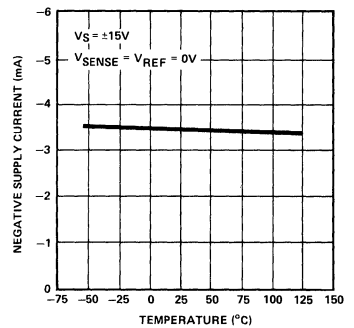
INPUT OFFSET VOLTAGE vs TEMPERATURE

INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

OUTPUT OFFSET VOLTAGE vs TEMPERATURE

OUTPUT OFFSET VOLTAGE CHANGE vs SUPPLY VOLTAGE

INPUT BIAS CURRENT vs TEMPERATURE

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

INPUT OFFSET CURRENT vs TEMPERATURE

COMMON-MODE REJECTION vs VOLTAGE GAIN

COMMON-MODE REJECTION vs FREQUENCY


6

INSTRUMENTATION AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS

COMMON-MODE VOLTAGE RANGE vs TEMPERATURE

POSITIVE PSR vs FREQUENCY

NEGATIVE PSR vs FREQUENCY

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

MAXIMUM OUTPUT SWING vs FREQUENCY

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

CLOSED-LOOP VOLTAGE GAIN vs FREQUENCY

TOTAL HARMONIC DISTORTION vs FREQUENCY

TOTAL HARMONIC DISTORTION vs LOAD RESISTANCE


TYPICAL PERFORMANCE CHARACTERISTICS
SLEW RATE vs VOLTAGE GAIN

SLEW RATE vs LOAD CAPACITANCE

SETTLING TIME TO 0.01% vs VOLTAGE GAIN

VOLTAGE NOISE DENSITY vs FREQUENCY

RTI VOLTAGE NOISE DENSITY vs GAIN

POSITIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

NEGATIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

POSITIVE SUPPLY CURRENT vs TEMPERATURE

NEGATIVE SUPPLY CURRENT vs TEMPERATURE

INSTRUMENTATION AMPLIFIERS

INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. While the initial offsets may be adjusted to zero, temperature variations will cause shifts in offsets. Systems with auto-zero can correct for offset errors, so initial adjustment would be unnecessary. However, many high-gain applications don't have auto zero. For these applications, both offsets can be nulled, which has minimal effect on TCV_{IOS} and TCV_{OOS} .

The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain, output-offset-errors dominate, while at high gain, input-offset-errors dominate. Overall offset voltage, V_{OS} , referred to the output (RTO) is calculated as follows;

$$V_{OS}(RTO) = (V_{IOS} \times G) + V_{OOS} \quad (1)$$

where V_{IOS} and V_{OOS} are the input and output offset voltage specifications and G is the amplifier gain. Input offset nulling alone is recommended with amplifiers having fixed gain above 50. Output offset nulling alone is recommended when gain is fixed at 50 or below.

In applications requiring both initial offsets to be nulled, the input offset is nulled first by short-circuiting R_G , then the output offset is nulled with the short removed.

The overall offset voltage drift TCV_{OS} , referred to the output, is a combination of input and output drift specifications. Input offset voltage drift is multiplied by the amplifier gain, G , and summed with the output offset drift;

$$TCV_{OS}(RTO) = (TCV_{IOS} \times G) + TCVOOS \quad (2)$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage specification. Frequently, the amplifier drift is referred back to the input (RTI) which is then equivalent to an input signal change;

$$TCV_{OS}(RTI) = TCVOOS + \frac{TCV_{OOS}}{G} \quad (3)$$

For example, the maximum input-referred drift of an AMP-01EX set to $G = 1000$ becomes;

$$TCV_{OS}(RTI) = 0.3\mu V/^{\circ}C + \frac{100\mu V/^{\circ}C}{1000} = 0.4\mu V/^{\circ}C \text{ max.}$$

INPUT BIAS AND OFFSET CURRENTS

Input transistor bias currents are additional error sources which can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an IA will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces a non-trimmable error. The magnitude of the error is the offset current times the source resistance.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

GAIN

The AMP-01 uses two external resistors for setting voltage gain over the range 0.1 to 10,000. The magnitudes of the scale resistor, R_S , and gain-set resistor, R_G , are related by the formula: $G = 20 \times R_S / R_G$, where G is the selected voltage gain (Refer to Figure 1).

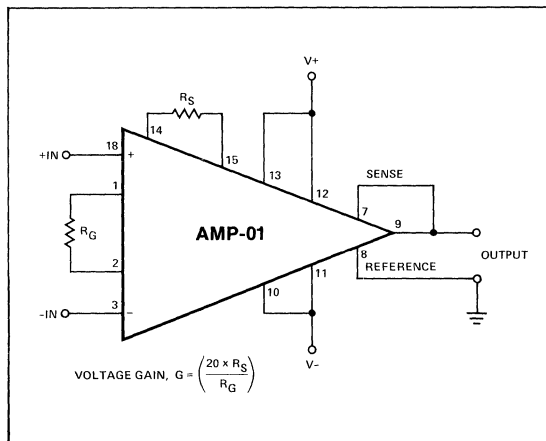
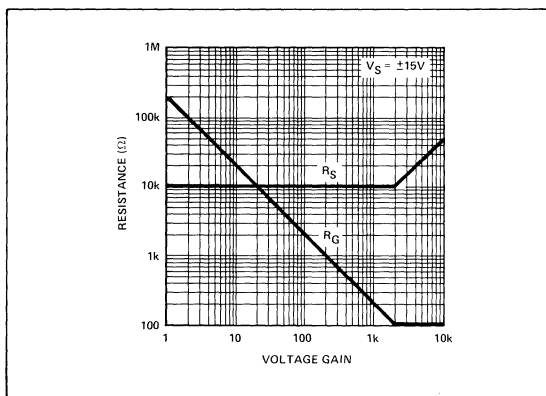


Figure 1. Basic AMP-01 connections for gains 0.1 to 10,000.

The magnitude of R_S affects linearity and output referred errors. Circuit performance is characterized using $R_S = 10k\Omega$ when operating on ± 15 volt supplies and driving a ± 10 volt output. R_S may be reduced to $5k\Omega$ in many applications particularly when operating on ± 5 volt supplies or if the output voltage swing is limited to ± 5 volts. Bandwidth is improved with $R_S = 5k\Omega$ and this also increases common-mode rejection by approximately 6dB at low gain. Lowering the value below $5k\Omega$ can cause instability in some circuit configurations and usually has no advantage. High voltage gains between two and ten thousand would require very low values of R_G . For $R_S = 10k\Omega$ and $A_V = 2000$ we get $R_G = 100\Omega$; this value is the practical lower limit for R_G . Below 100Ω , mismatch of wirebond and resistor temperature coefficients will introduce significant gain tempco errors. Therefore, for gains above 2,000, R_G should be kept constant at 100Ω and R_S increased. The maximum gain of 10,000 is obtained with R_S set to $50k\Omega$.

Metal-film or wirewound resistors are recommended for best results. The absolute values and TC's are not too important, only the ratiometric parameters.

AC amplifiers require good gain stability with temperature and time, but DC performance is unimportant. Therefore, low cost metal-film types with TC's of $50ppm/^{\circ}C$ are usually adequate for R_S and R_G . Realizing the full potential of the AMP-01's offset voltage and gain stability requires precision metal-film or wirewound resistors. Achieving a $15ppm/^{\circ}C$ gain tempco at all gains requires R_S and R_G temperature coefficient matching to $5ppm/^{\circ}C$ or better.



R_G AND R_S SELECTION

Gain accuracy is determined by the ratio accuracy of R_S and R_G combined with the gain equation error of the AMP-01 (0.6% max for A/E grades).

All instrumentation amplifiers require attention to layout so thermocouple effects are minimized. Thermocouples formed between copper and dissimilar metals can easily destroy the TC_{VOS} performance of the AMP-01 which is typically 0.15μV/°C. Resistors themselves can generate thermoelectric EMF's when mounted parallel to a thermal gradient. "Vishay" resistors are recommended because a maximum value for thermoelectric generation is specified. However, where thermal gradients are low and gain TC's of 20-50ppm are sufficient, general-purpose metal-film resistors can be used for R_G and R_S.

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. CMR specifications are normally measured with a full-range input voltage change and a specified source resistance unbalance.

The current-feedback design used in the AMP-01 inherently yields high common-mode rejection. Unlike resistive feedback designs, typified by the three-op-amp IA, the CMR is not degraded by small resistances in series with the reference input. A slight, but trimmable, output offset voltage change results from resistance in series with the reference input.

The common-mode input voltage range, CMVR, for linear operation may be calculated from the formula:

$$CMVR = \pm \left(IVR - \frac{|V_{OUT}|}{2G} \right) \dots (4)$$

IVR is the data sheet specification for input voltage range; V_{OUT} is the maximum output signal; and G is the chosen

voltage gain. For example, at 25°C, IVR is specified as ±10.5 volt minimum with ±15 volt supplies. Using a ±10 volt maximum swing output and substituting the figures in (4) simplifies the formula to:

$$CMVR = \pm \left(10.5 - \frac{5}{G} \right) \dots (5)$$

For all gains greater than or equal to 10, CMVR is ±10 volt minimum; at gains below 10, CMVR is reduced.

ACTIVE GUARD DRIVE

Rejection of common-mode noise and line pick-up can be improved by using shielded cable between the signal source and the IA. Shielding reduces pick-up, but increases input capacitance, which in turn degrades the settling-time for signal changes. Further, any imbalance in the source resistance between the inverting and noninverting inputs, when capacitively loaded, converts the common-mode voltage into a differential voltage. This effect reduces the benefits of shielding. AC common-mode rejection is improved by "bootstrapping" the input cable capacitance to the input signal, a technique called "guard driving". This technique effectively reduces the input capacitance. A single guard-driving signal is adequate at gains above 100 and should be the average value of the two inputs. The value of external gain resistor R_G is split between two resistors R_{G1} and R_{G2}; the center tap provides the required signal to drive the buffer amplifier (Figure 2).

GROUNDING

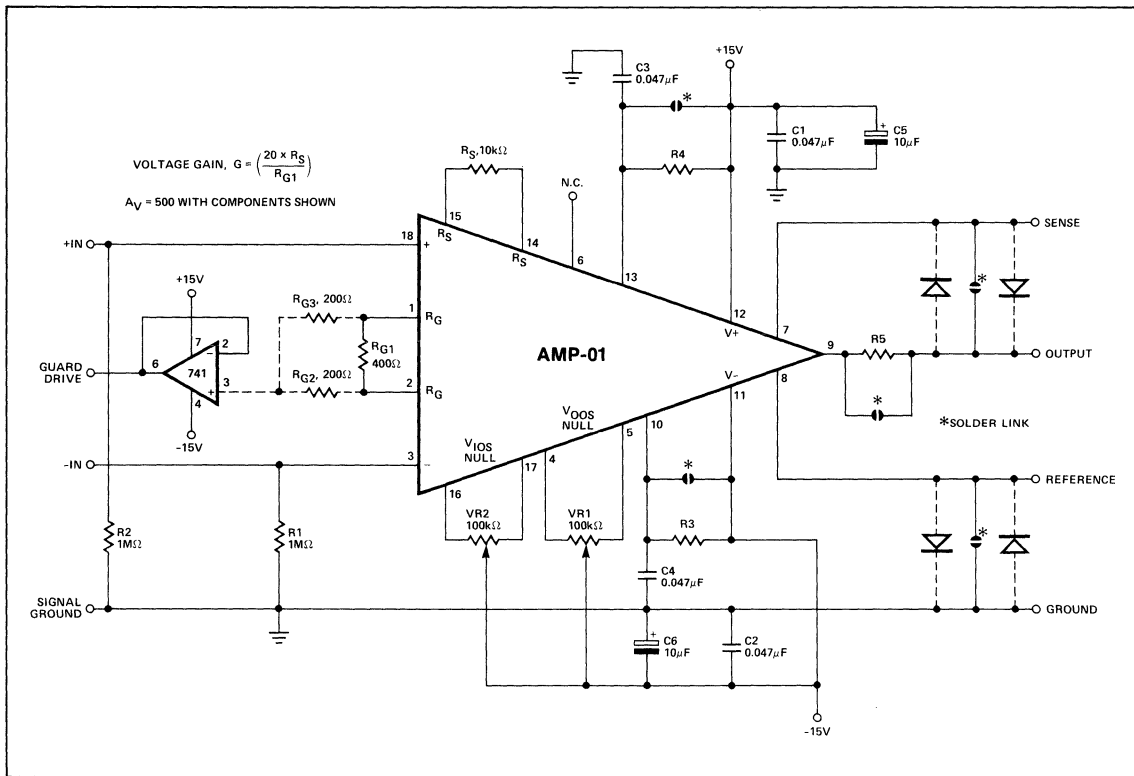
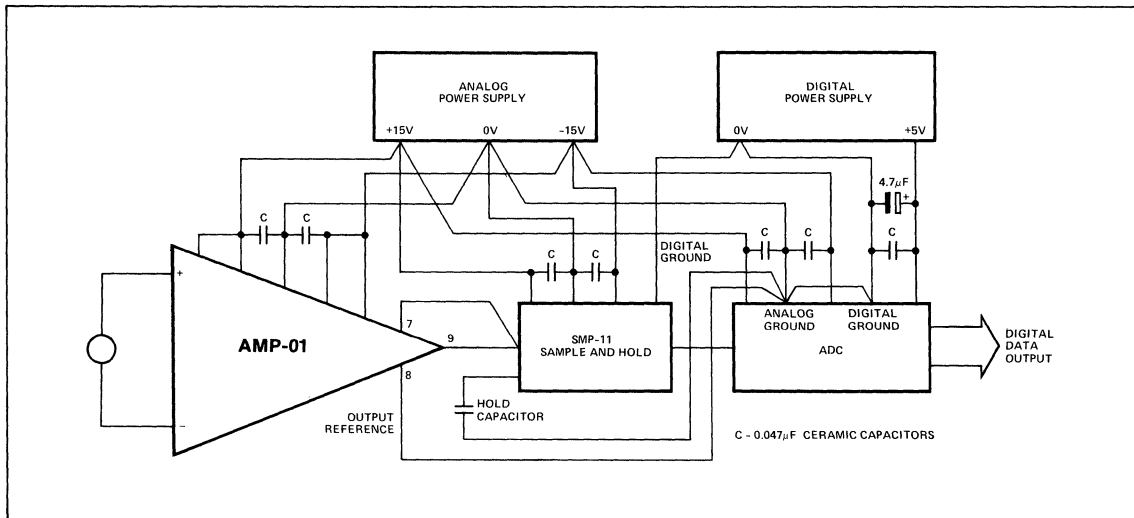
The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds which will be tied together at one point, usually the analog power-supply ground. In addition, the digital and analog grounds may be joined, normally at the analog ground pin on the A-to-D converter. Following this basic grounding practice is essential for good circuit performance (Figure 3).

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates do not interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

SENSE AND REFERENCE TERMINALS

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground.


Figure 2. AMP-01 evaluation circuit showing guard-drive connection.

Figure 3. Basic grounding practice.



If heavy output currents are expected and the load is situated some distance from the amplifier, voltage drops due to track or wire resistance will cause errors. Voltage drops are particularly troublesome when driving 50Ω loads. Under these conditions, the sense and reference terminals can be used to "remote sense" the load as shown in Figure 4. This method of connection puts the I×R drops inside the feedback loop and virtually eliminates the error. An unbalance in the lead resistances from the sense and reference pins does not degrade CMR, but will change the output offset voltage. For example, a large unbalance of 3Ω will change the output offset by only 1mV.

DRIVING 50Ω LOADS

Output currents of 50mA are guaranteed into loads of up to 50Ω and 26mA into 500Ω. In addition, the output is stable and free from oscillation even with a high load capacitance. The combination of these unique features in an instrumentation amplifier allows low-level transducer signals to be condi-

tioned and directly transmitted through long cables in voltage or current form. Increased output current brings increased internal dissipation, especially with 50Ω loads. For this reason, the power-supply connections are split into two pairs; pins 10 and 13 connect to the output stage only and pins 11 and 12 provide power to the input and following stages. Dual supply pins allow dropper resistors to be connected in series with the output stage so excess power is dissipated outside the package. Additional decoupling is necessary between pins 10 and 13 to ground to maintain stability when dropper resistors are used. Figure 5 shows a complete circuit for driving 50Ω loads.

HEATSINKING

To maintain high reliability, the die temperature of any IC should be kept as low as practicable, preferably below 100°C. Although most AMP-01 application circuits will produce very little internal heat — little more than the quiescent dissipation of 90mW — some circuits will raise that

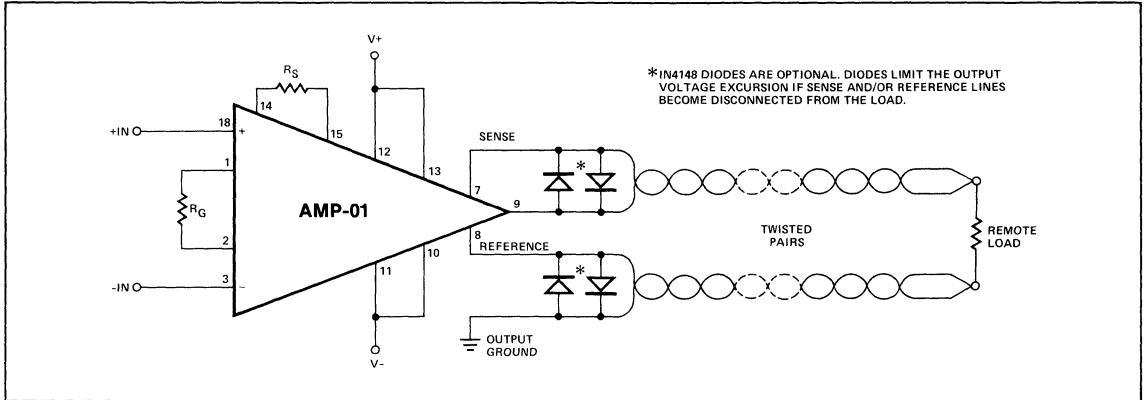


Figure 4. Remote load sensing.

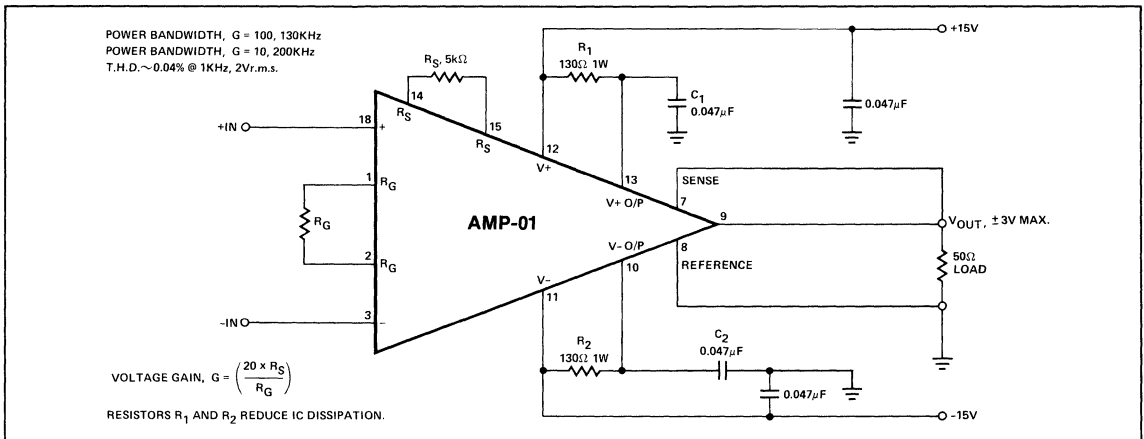


Figure 5. Driving 50Ω loads.

to several hundred milliwatts (for example, the 4-20mA current transmitter application, Figure 8). Excessive dissipation will cause thermal shutdown of the output stage thus protecting the device from damage. A heatsink is recommended in power applications to reduce the die temperature.

Several appropriate heatsinks are available; the Thermalloy 6010B is especially easy to use and is inexpensive. Intended for dual-in-line packages, the heatsink may be attached with a cyanoacrylate adhesive. This heatsink reduces the thermal resistance between the junction and ambient environment to approximately 80° C/W. Junction (die) temperature can then be calculated by using the relationship:

$$P_d = \frac{T_j - T_a}{\theta_{ja}}$$

where T_j and T_a are the junction and ambient temperatures respectively, θ_{ja} is the thermal resistance from junction to ambient, and P_d is the device's internal dissipation.

OVERVOLTAGE PROTECTION

Instrumentation amplifiers invariably sit at the front end of instrumentation systems where there is a high probability of exposure to overloads. Voltage transients, failure of a transducer, or removal of the amplifier power supply while the signal source is connected may destroy or degrade the performance of an unprotected amplifier. Although it is impractical to protect an IC internally against connection to power lines, it is relatively easy to provide protection against typical system overloads.

The AMP-01 is internally protected against overloads for gains of up to 100. At higher gains, the protection is reduced and some external measures may be required. Limited internal overload protection is used so that noise performance would not be significantly degraded.

AMP-01 noise level approaches the theoretical noise floor of the input stage which would be $4nV/\sqrt{\text{Hz}}$ at 1kHz when the gain is set at 1000. Noise is the result of shot noise in the input devices and Johnson noise in the resistors. Resistor noise is calculated from the values of R_G (200Ω at a gain of 1000) and the input protection resistors (250Ω). Active loads for the input transistors contribute less than $1nV/\sqrt{\text{Hz}}$ of noise. The measured noise level is typically $5nV/\sqrt{\text{Hz}}$.

Diodes across the input transistor's base-emitter junctions, combined with 250Ω input resistors and R_G , protect against differential inputs of up to ±20V for gains of up to 100. The diodes also prevent avalanche breakdown that would degrade the I_B and I_{OS} specifications. Decreasing the value of R_G for gains above 100 limits the maximum input overload protection to ±10V. External series resistors could be added to guard against higher voltage levels at the input, but resistors alone increase the input noise and degrade the signal-to-noise ratio, especially at high gains.

Protection can also be achieved by connecting back-to-back 9.1V zener diodes across the differential inputs. This technique does not affect the input noise level and can be used down to a gain of 2 with minimal increase in input current. Although voltage-clamping elements look like short circuits at the limiting voltage, the majority of signal sources provide less than 50mA, producing power levels that are easily handled by low-power zeners.

Simultaneous connection of the differential inputs to a low-impedance signal above 10V during normal circuit operation is unlikely. However, additional protection involves adding 100Ω current-limiting resistors in each signal path prior to the voltage clamp; the resistors increase the input noise level to just $5.4nV/\sqrt{\text{Hz}}$ (refer to Figure 6).

Input components, be they multiplexers or resistors, should be carefully selected to prevent the formation of thermocouple junctions which would degrade the input signal.

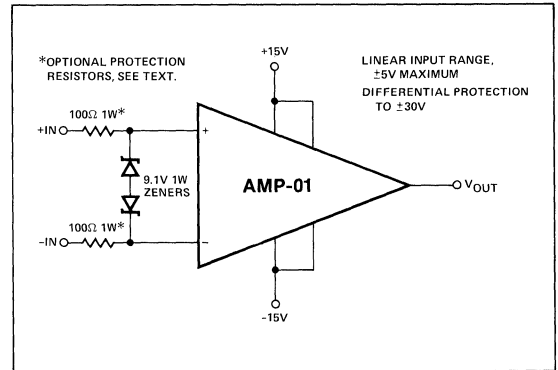


Figure 6. Input overvoltage protection for gains 2 to 10,000.

POWER SUPPLY CONSIDERATIONS

Achieving the rated performance of precision amplifiers in a practical circuit requires careful attention to external influences. For example, supply noise and changes in the nominal voltage directly affect the input offset voltage. A PSR of 80dB means that a change of 100mV on the supply, not an uncommon value, will produce a 10μV input offset change. Consequently, care should be taken in choosing a power unit that has a low output noise level, good line and load regulation, and good temperature stability.

APPLICATIONS INFORMATION

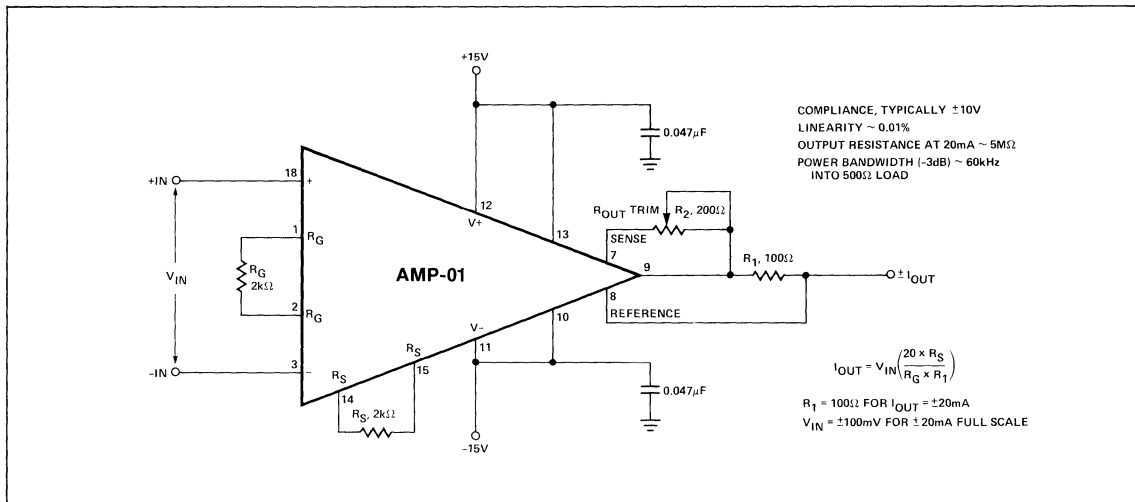


Figure 7. High-compliance bipolar current source with 13-bit linearity.

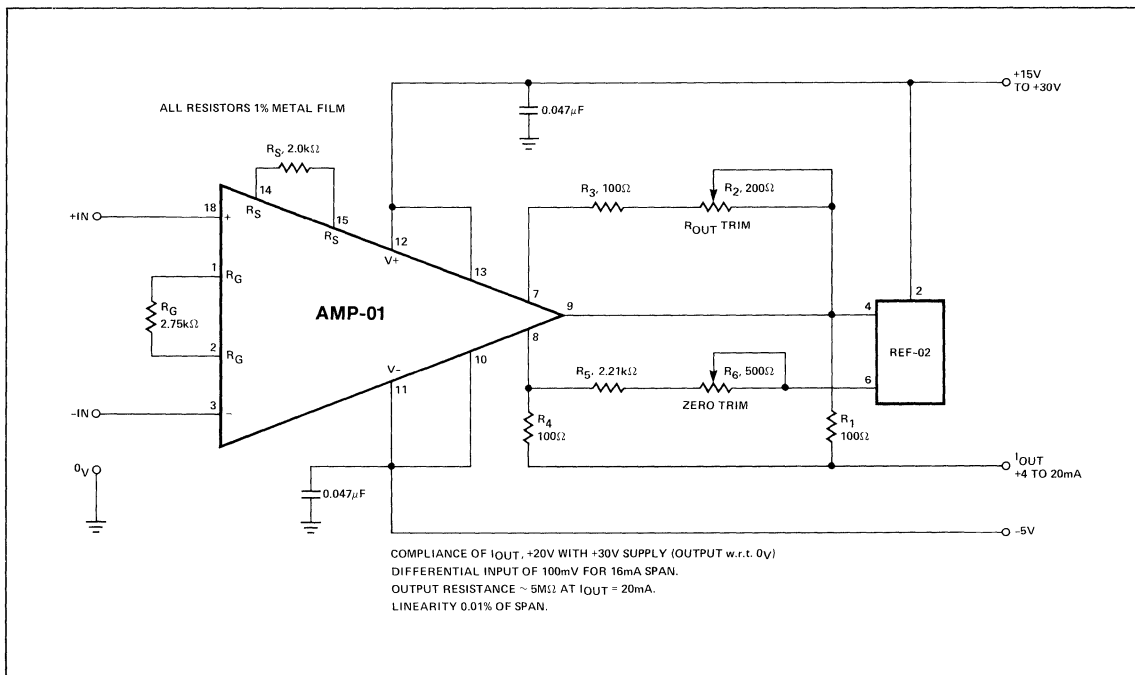


Figure 8. 13-bit linear 4-20mA transmitter constructed by adding a voltage reference. Thermocouple signals can be accepted without preamplification.

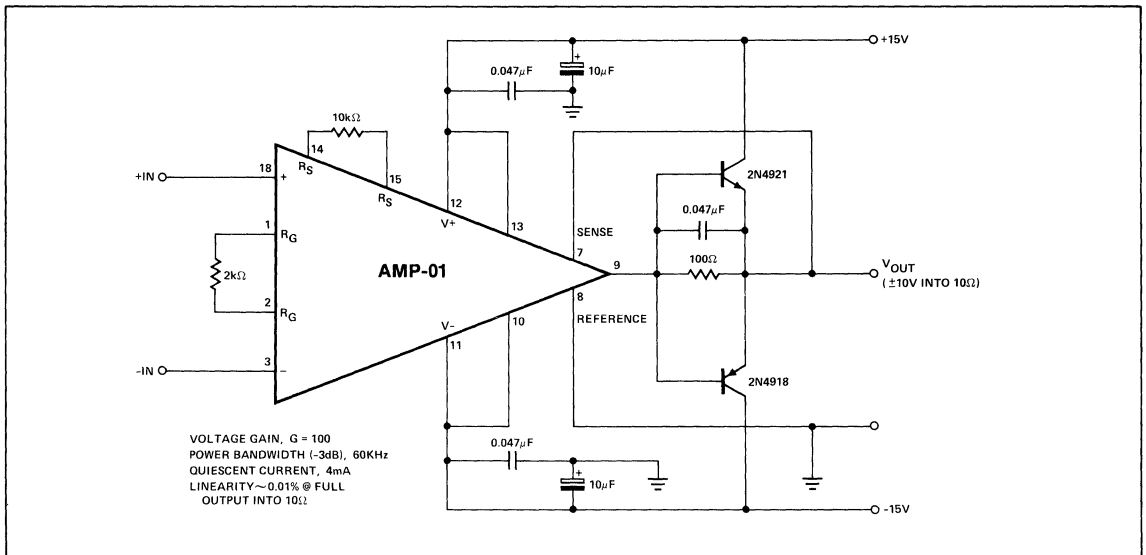


Figure 9. Adding two transistors increases output current to $\pm 1A$ without affecting the quiescent current of 4mA. Power bandwidth is 60kHz.

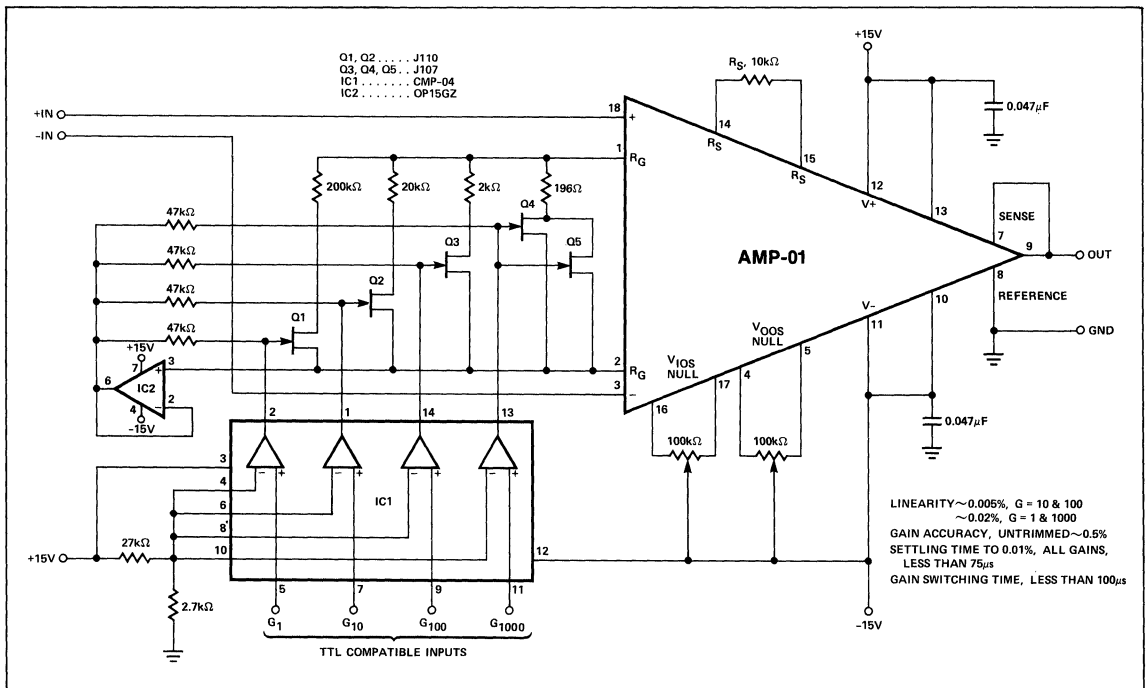


Figure 10. The AMP-01 makes an excellent programmable-gain instrumentation amplifier. Combined gain-switching and settling time to 13-bits falls below 100μs. Linearity is better than 12-bits over a gain range 1 to 1000.

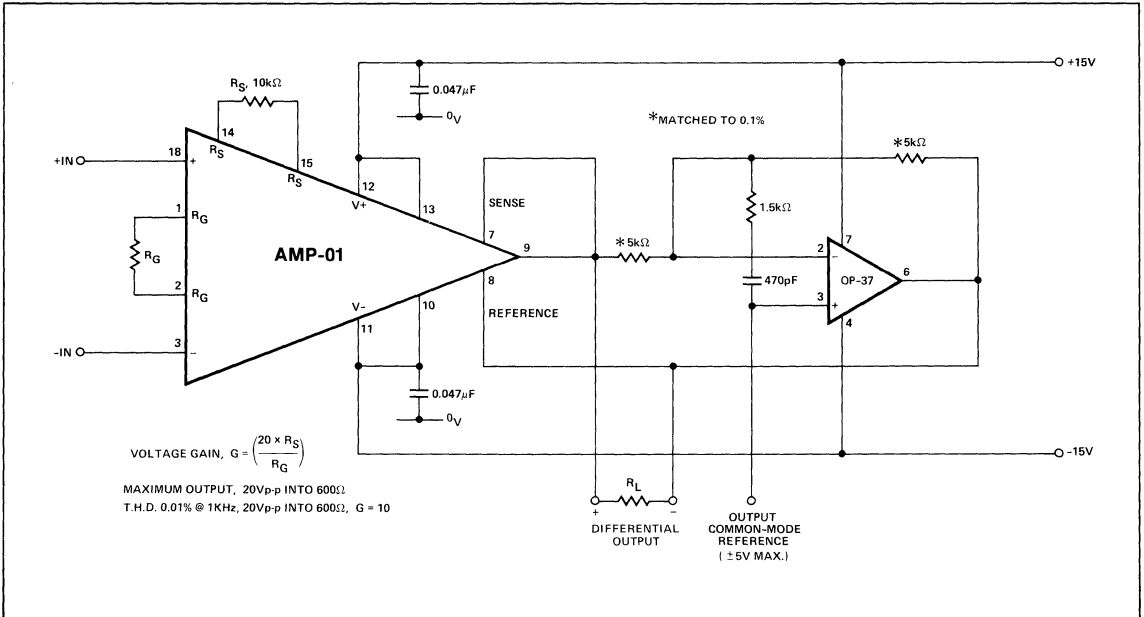


Figure 11. A differential input instrumentation amplifier with differential output replaces a transformer in many applications. The output will drive a 600Ω load at low distortion, (0.01%).

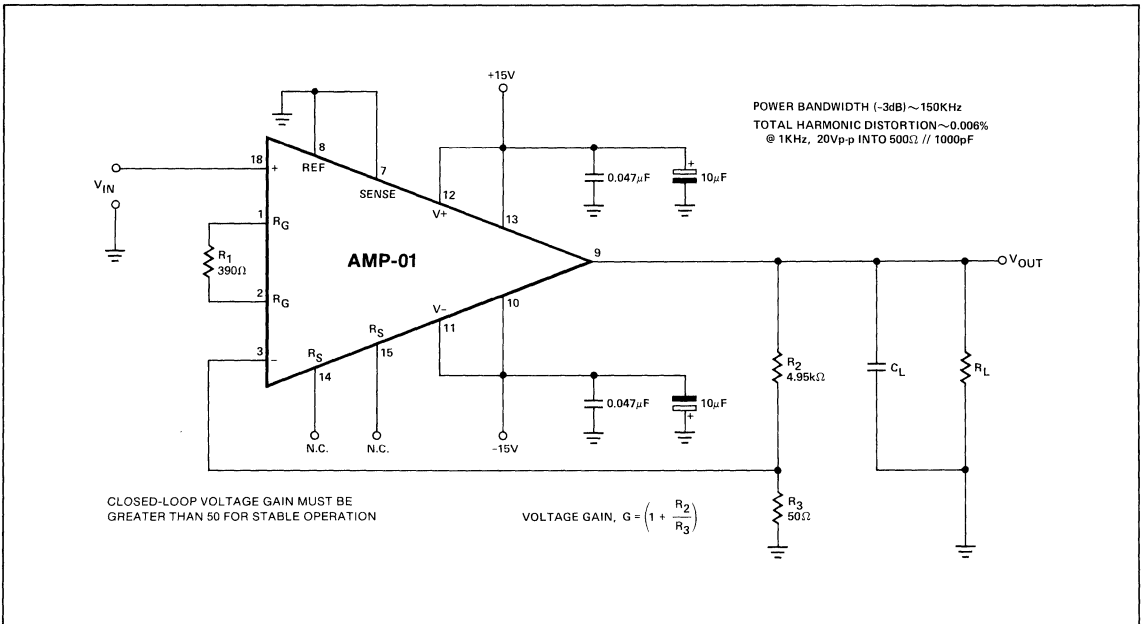


Figure 12. Configuring the AMP-01 as a noninverting operational amplifier provides exceptional performance. The output handles low load impedances at very low distortion, 0.006%.

6 INSTRUMENTATION AMPLIFIERS

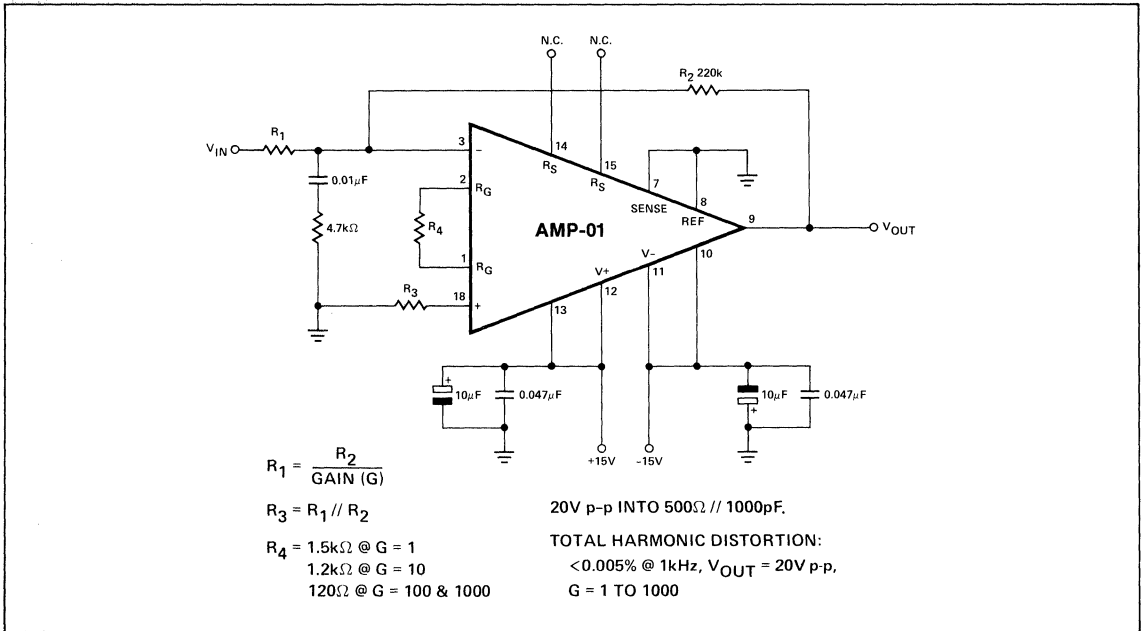


Figure 13. The inverting operational amplifier configuration has excellent linearity over the gain range 1 to 1000, typically 0.005%. Offset voltage drift at unity gain is improved over the drift in the instrumentation amplifier configuration.

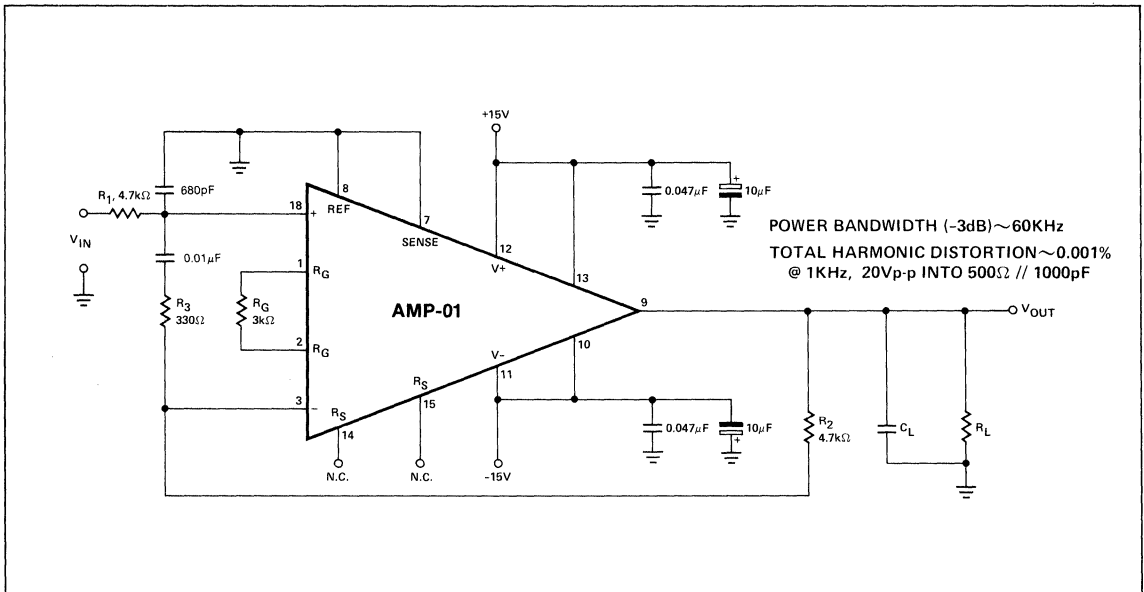
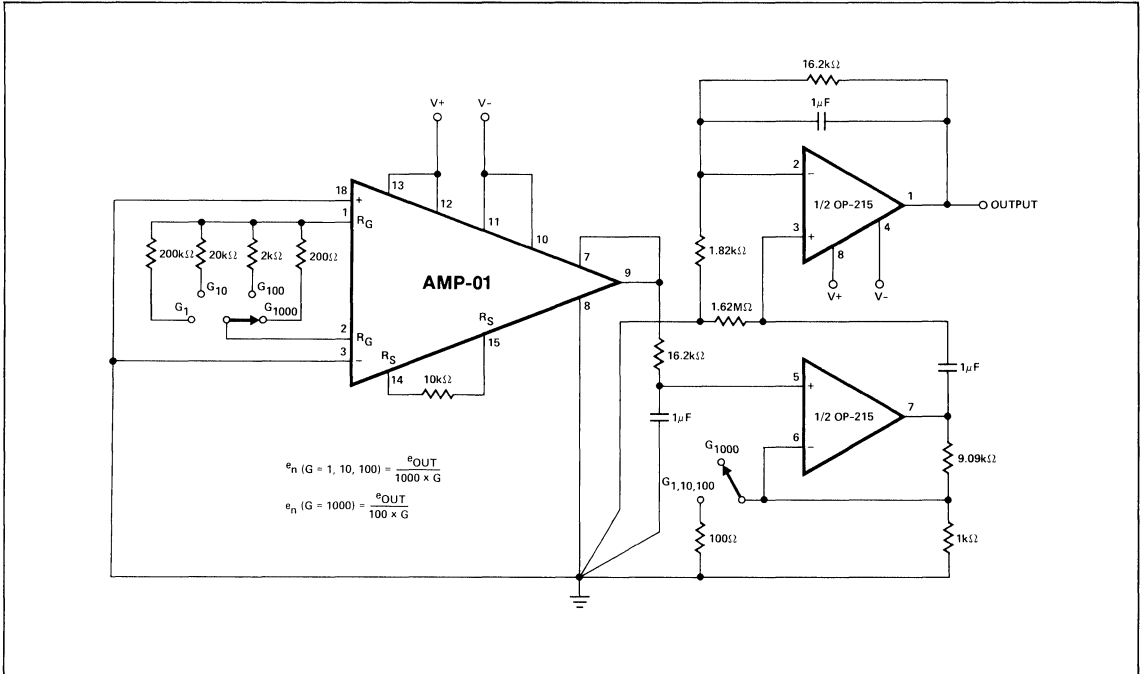
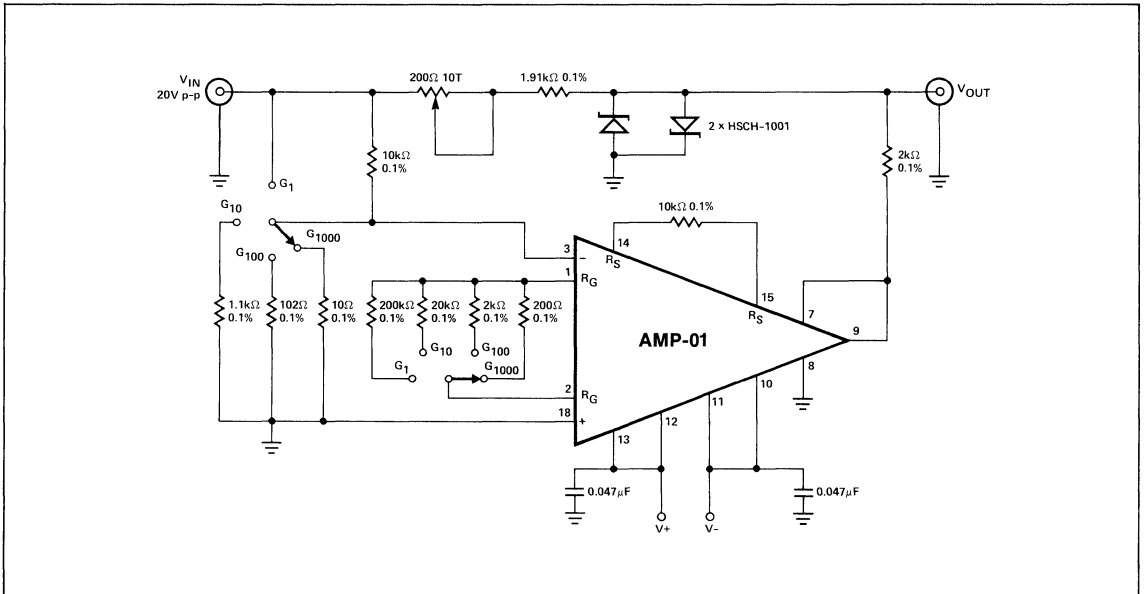
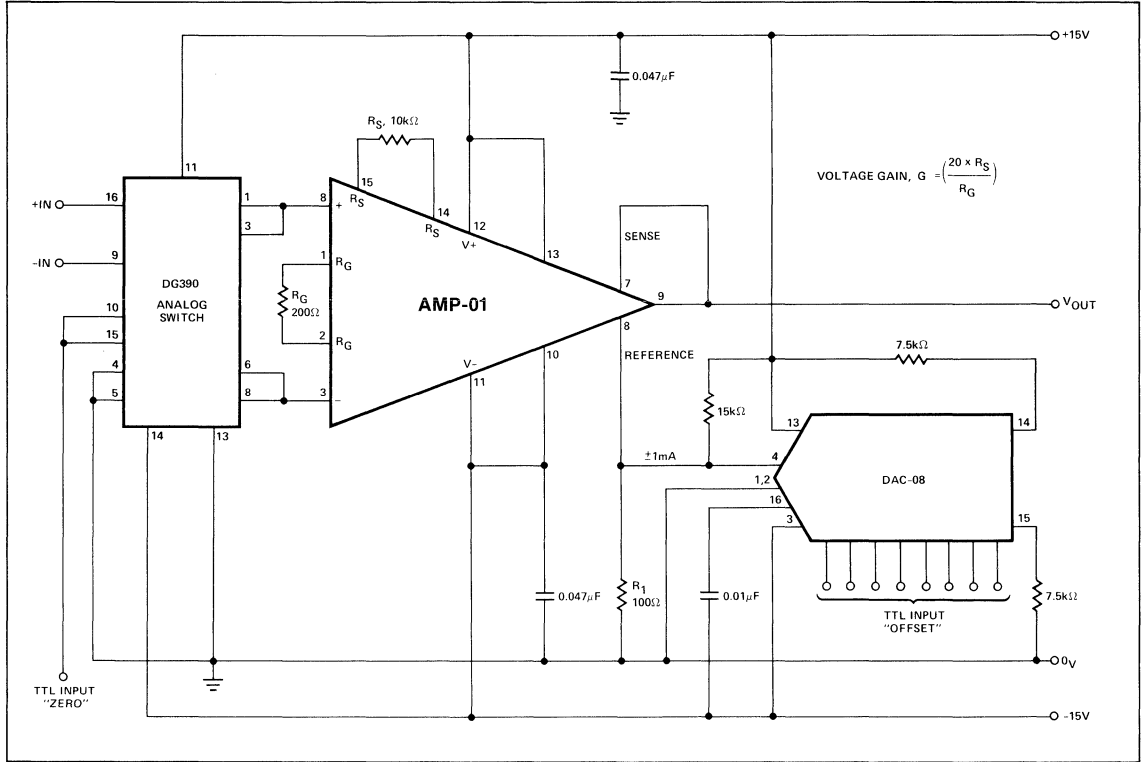


Figure 14. Stability with large capacitive loads combined with high output current capability make the AMP-01 ideal for line driving applications. Offset voltage drift approaches the TCV_{IOS} limit, (0.3µV/°C).

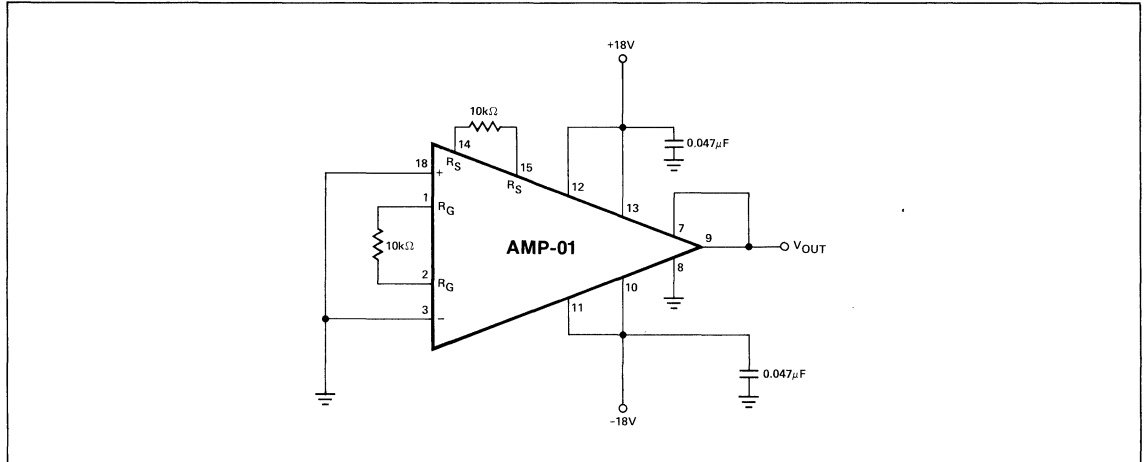
NOISE TEST CIRCUIT (0.1Hz to 10Hz)

SETTLING-TIME TEST CIRCUIT




INSTRUMENTATION AMPLIFIER WITH AUTO-ZERO



BURN-IN CIRCUIT





AMP-05

FAST-SETTLING JFET
INSTRUMENTATION AMPLIFIER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Settling-Time to 12-Bit Accuracy, $G \leq 1000 \dots 12\mu\text{s Max}$
- 14-Bit Gain Linearity at $G \leq 1000$
- On-Board Dual Guard Drivers
- On-Board 100 μA Precision Current Source
- Low Bias Current $\dots 50\text{pA Max @ } 25^\circ\text{C}$
 $\dots 20\text{nA Max @ } 125^\circ\text{C}$
- Temperature Stable CMR
 $\dots 105\text{dB Min Over } -55^\circ\text{C to } +125^\circ\text{C}$
- High Slew-Rate with 500pF Load $\dots 5\text{V}/\mu\text{s Min}$

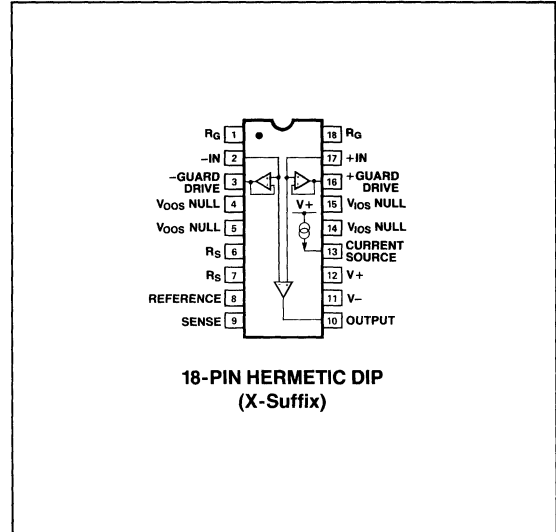
ORDERING INFORMATION†

CERDIP 18-PIN PACKAGE	OPERATING TEMPERATURE RANGE
AMP05AX*	MIL
AMP05BX*	MIL
AMP05EX	IND
AMP05FX	IND

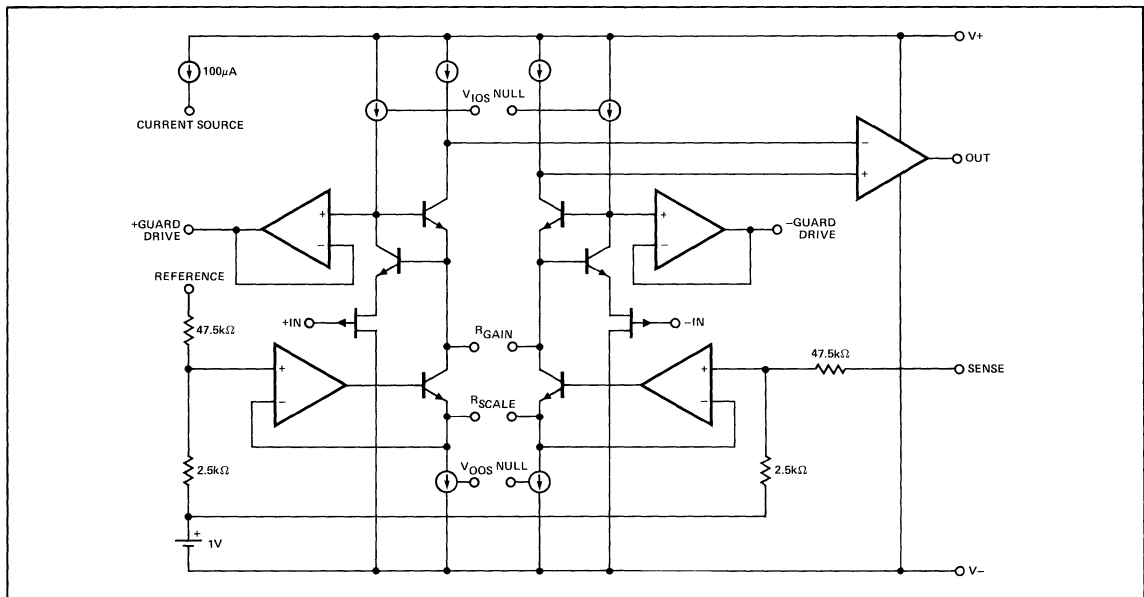
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

6
INSTRUMENTATION AMPLIFIERS

GENERAL DESCRIPTION

The AMP-05 is a fast JFET instrumentation amplifier designed for high-speed analog signal-processing and analog-multiplexed data acquisition systems. Settling-time to 12-bits is $12\mu\text{s}$ maximum, with better than 14-bit linearity at all gains up to 1000. Two functions are added to the instrumentation amplifier that reduce external component count in many applications. On-board dual guard drivers maintain good settling-time and common-mode rejection performance when shielded cable connects the input signal to the AMP-05. A precision $100\mu\text{A}$ current source is also provided for transducer excitation, powering a low-current voltage reference, and other functions.

The AMP-05 employs a current-feedback technique which provides a high and stable common-mode rejection, 105dB minimum over the military temperature range. JFET inputs reduce bias current to 50pA maximum at 25°C and only 20nA maximum at 125°C ; low bias current reduces errors due to signal-source

resistance. Internal input protection allows a 30V differential overload at all gain settings. AMP-05 voltage gain is set by the ratio of two external resistors over the range 0.1 to 2000 and a low gain temperature-coefficient of $20\text{ppm}/^\circ\text{C}$ is achievable in the range 1 to 1000.

The AMP-05's outputs can all drive large capacitive loads without oscillation. The amplifier output is guaranteed stable with loads up to 2,000pF and the guard drivers can tolerate up to 10,000pF without oscillation.

Sense and reference pins complete the output feedback-loop and provide an output ground reference, respectively. The reference pin may be used for zeroing system offsets, where auto-zero hardware is employed. Resistance, in series with the reference terminal, does not degrade common-mode rejection on PMI's AMP-05, which is a significant problem with instrumentation amplifiers employing the three op-amp configuration.

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



VOLTAGE FOLLOWERS/BUFFERS

Precision Monolithics Inc.

7-3 Introduction

7-4 **BUF-03**

High-Speed Voltage Follower/Buffer



VOLTAGE FOLLOWERS/BUFFERS

Precision Monolithics Inc.

INTRODUCTION

The function of a unity-gain buffer is to accurately reproduce the input signal under widely-varying load conditions. To do this, buffers must have high input impedance, wide bandwidth, and high output drive. Offsets and gain error need to be minimized.

The buffer function can be implemented by use of general-purpose operational amplifiers connected as unity-gain voltage followers, but higher performance can be obtained by optimizing a circuit specifically for buffering. A design dedicated to unity-gain buffering and using no

feedback can provide better frequency response. In addition, output current can be increased substantially beyond that of conventional IC operational amplifiers.

The BUF-03 is a high-speed, unity-gain IC that is optimized for the buffer function. A FET input provides high input impedance. On-chip zener-zap trimming is used to reduce the offset voltage. The output stage is designed to supply approximately 70mA of peak current. These features combine to make the BUF-03 an IC analog buffer of unique capability.

7

VOLTAGE FOLLOWERS/BUFFERS



BUF-03

HIGH-SPEED VOLTAGE FOLLOWER/BUFFER

Precision Monolithics Inc.

FEATURES

- Very High Slew Rate 220V/ μ sec Min
- Wide Bandwidth 63MHz
- Load Drive Current 70mA Peak
- Easily Drives Large Capacitive Loads Without Oscillation
- High Input Resistance $5 \times 10^{11}\Omega$
- Low Output Resistance 2 Ω
- Very Low Bias Current (Warmed-Up) 400pA Max
- Low Offset Voltage 6mV Max
- Unity Gain 0.997V/V
- Excellent Gain Linearity 0.015%

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ $V_{OS}\text{ MAX}$ (mV)	PACKAGE TO-99 8-PIN	OPERATING TEMPERATURE RANGE
6	BUF03AJ*	MIL
6	BUF03EJ	COM
15	BUF03BJ*	MIL
15	BUF03FJ	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

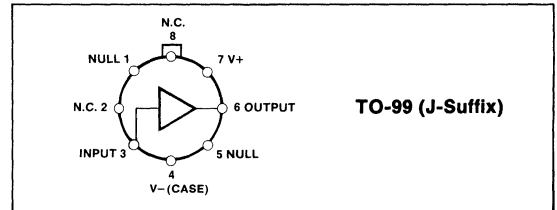
GENERAL DESCRIPTION

The BUF-03 is the first very high-speed monolithic voltage follower. Featuring performance previously unobtainable in a monolithic unit, it offers a combination of both exceptional speed and excellent input/output specifications. Implemented

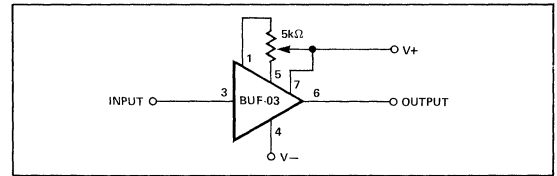
in an open-loop circuit employing source followers and emitter followers, the BUF-03 utilizes a quasi-quad FET input structure to optimize both speed and D.C. input characteristics. On-chip zener-zap trimming is used to achieve low offset voltage while careful biasing throughout results in excellent gain linearity over the full input voltage range.

Applications for which the BUF-03 is well-suited include high-speed line drivers, isolation amplifiers for driving reactive loads, and high-speed sample-hold circuits.

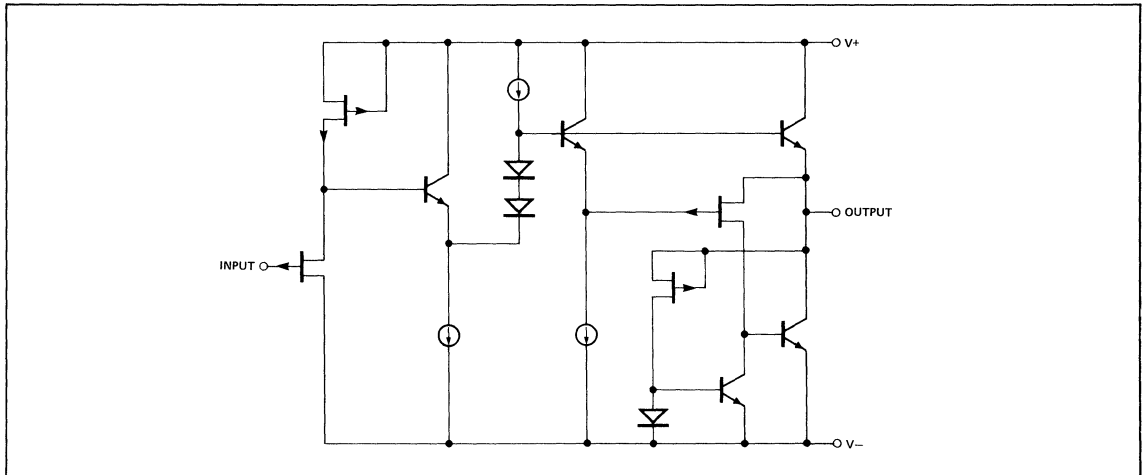
PIN CONNECTIONS



OPTIONAL OFFSET NULLING CIRCUIT



SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS (Note)

Supply Voltage (V+ to V-) 36V
 Internal Power Dissipation (Pd) (see curves)
 in still air, no heat sink 1.05W
 with heat sink, $\theta_{JA} = 90^\circ\text{C/W}$ 1.40W
 Input Voltage (for $V_S < \pm 18\text{V}$, maximum input
 voltage is equal to supply) $\pm 18\text{V}$
 Continuous Output Current 70mA
 Peak Output Current 100mA
 Short-Circuit Protection (Maximum Pd or Tj
 not to be exceeded) Indefinite at 80mA

Maximum Junction Temperature (Tj) 175°C
 Storage Temperature Range -65°C to +175°C
 Operating Temperature Range
 BUF-03A, BUF-03B -55°C to +125°C
 BUF-03E, BUF-03F 0°C to +70°C
 Lead Temperature (Soldering, 60 sec) 300°C
 DICE Junction Temperature (Tj) -65°C to +175°C

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$, $T_{\text{CHIP}} = 75^\circ\text{C}$, device fully warmed-up, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	BUF-03A/E			BUF-03B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC SPECIFICATIONS									
Slew Rate	SR	$R_L \geq 2\text{k}\Omega$, $C_L = 50\text{pF}$	220	250	—	180	250	—	V/ μsec
Power Bandwidth	PBW	$V_{IN} = 10V_{P-P}$, $R_L \geq 2\text{k}\Omega$	—	9	—	—	8	—	MHz
Bandwidth	BW	$\Delta V_{IN} \leq 2V_{P-P}$	—	63	—	—	50	—	MHz
Settling Time	t _S	To 0.1%, $\pm 10\text{V}$ step	—	90	—	—	100	—	nsec
Capacitive Load Capability	C _{LOAD}	No Oscillations	—	1	—	—	1	—	μF
Propagation Delay	t _d	Step Input	—	7	—	—	7	—	nsec
Rise Time	t _r	$\Delta V = 0.5\text{V}$	—	7	—	—	7	—	nsec
Wide Band Input Noise Voltage	V _n	DC to 50MHz	—	350	—	—	400	—	μVRMS
Input Noise Voltage Density	e _n	f = 10kHz	—	50	—	—	60	—	nV/ $\sqrt{\text{Hz}}$
DC SPECIFICATIONS									
Input Offset Voltage	V _{OS}	$R_S \leq 20\text{k}\Omega$	—	2	6	—	4	15	mV
Input Bias Current	I _B		—	150	400	—	180	700	pA
Input Resistance	R _{IN}		—	5×10^{11}	—	—	4×10^{11}	—	Ω
Voltage Gain ($V_{IN} = \pm 10\text{V}$)	A _{VO}	$R_L \geq 10\text{k}\Omega$	0.9960	0.9975	—	0.9940	0.9970	—	V/V
		$R_L \geq 2\text{k}\Omega$	0.9945	0.9960	—	0.9930	0.9950	—	
		$R_L \geq 1\text{k}\Omega$	0.9925	0.9945	—	0.9905	0.9930	—	
			0.9925	0.9945	—	0.9905	0.9930	—	
Nonlinearity (Note 2)	NL	$V_{IN} = \pm 10\text{V}$, $R_L \geq 2\text{k}\Omega$	—	0.015	0.023	—	0.017	0.03	%F.S.
		$V_{IN} = \pm 7\text{V}$, $R_L \geq 1\text{k}\Omega$	—	0.013	0.023	—	0.015	0.03	
Maximum Output Error	OUT _{error}	$V_{IN} = +10\text{V}$, 0V, -10V $R_S = 0$ to 20k Ω $R_L \geq 2\text{k}\Omega$ in all combinations	—	40	60	—	50	85	mV
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6\text{V}$ to $\pm 18\text{V}$	—	0.10	0.71	—	0.15	1.42	mV/V
Supply Current	I _{SY}	No Load	—	19	25	—	19	25	mA
Peak Load Current	I _{L(PK)}		—	70	—	—	70	—	mA
Output Resistance	R _O		—	2	—	—	2	—	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1\text{k}\Omega$	—	± 80	—	—	± 80	—	mV
Input Voltage Range (Reduced Accuracy)	IVR		—	± 11.5	—	—	± 11.5	—	V

NOTES:

1. The BUF-03 package thermal resistance, in still air, is 145°C/W (45°C/W junction-to-case, 100°C/W case-to-ambient). The chip temperature of 75°C is achieved by reducing the case-to-ambient thermal resistance to 45°C/W. An inexpensive heat sink, such as the Thermalloy 2271B or 6203, is recommended for use in this application. In addition, if the device is operated in a forced-air environment, or is attached to a PC board which has good thermal conductivity, the chip temperature may be further reduced.

If no heat sinking is used, the chip temperature (in still air) may exceed 105°C. The effect of this elevated temperature will be to increase the input bias current by a factor of eight, increase the V_{OS} specification by TC_{V_{OS}} × 30°C, and reduce device speed by 10%.

2. Nonlinearity is computed using linear regression techniques with data from five points (e.g., -10V, -5V, 0V, +5V, and +10V for $\pm 10\text{V}$ full-scale linearity).

7

VOLTAGE FOLLOWERS/BUFFERS



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, $T_{CHIP}(MAX) = +165^\circ C$, device fully warmed-up, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	BUF-03A			BUF-03B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	—	220	—	—	220	—	V/ μ sec
Input Offset Voltage	V_{OS}	$R_S \leq 2k\Omega$	—	6	20	—	10	35	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 2k\Omega$, (Note 2)	—	50	100	—	90	170	$\mu V/^\circ C$
Input Bias Current	I_B	$T_A = +125^\circ C$	—	25	75	—	30	90	nA
Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_{IN} = \pm 10V$	0.9920	0.9955	—	0.9902	0.9942	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/ $^\circ C$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.15	1.26	—	0.20	2.24	mV/V
Supply Current	I_{SY}	$T_A = +125^\circ C$	—	18	24	—	18	24	mA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, $T_{CHIP}(MAX) = +120^\circ C$, device fully warmed-up, unless otherwise noted.

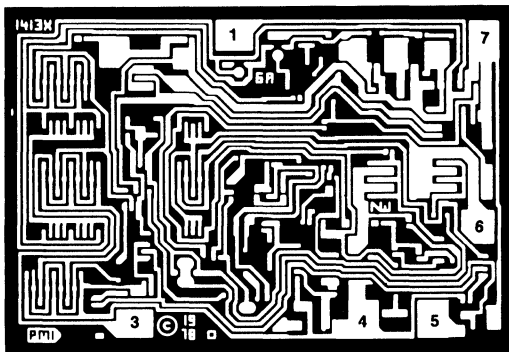
PARAMETER	SYMBOL	CONDITIONS	BUF-03E			BUF-03F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	240	—	—	240	—	V/ μ sec
Input Offset Voltage	V_{OS}	$R_S \leq 2k\Omega$, $C_L = 50pF$	—	4	14	—	7	28	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 2k\Omega$, (Note 2)	—	40	90	—	80	150	$\mu V/^\circ C$
Input Bias Current	I_B	$T_A = +70^\circ C$	—	1.5	5	—	1.8	8	nA
Voltage Gain ($V_{IN} = \pm 10V$)	A_{VO}	$R_L \geq 2k\Omega$	0.9935	0.9958	—	0.9918	0.9946	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/ $^\circ C$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.12	1	—	0.16	1.78	mV/V
Supply Current	I_{SY}	$T_A = +70^\circ C$	—	19	25	—	19	25	mA

NOTES:

- In order to operate the device at an ambient temperature of $+125^\circ C$, more extensive heat sinking must be used to ensure that the chip temperature never exceeds the absolute maximum of $+175^\circ C$. The chip temperature of $+165^\circ C$ is achieved by reducing the case-to-ambient thermal resistance to $30^\circ C/W$ (e.g., Thermalloy 2227).
- Guaranteed by design.



DICE CHARACTERISTICS



- 1. NULL
- 3. INPUT
- 4. NEGATIVE SUPPLY
- 5. NULL
- 6. OUTPUT
- 7. POSITIVE SUPPLY

DIE SIZE 0.070 × 0.048 inch, 3360 sq. mils
(1.78 × 1.22 mm, 2.17 sq. mm)

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_j = 25^\circ C$, unless otherwise noted.

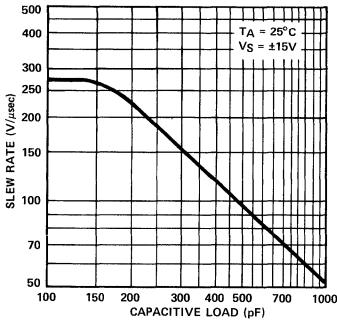
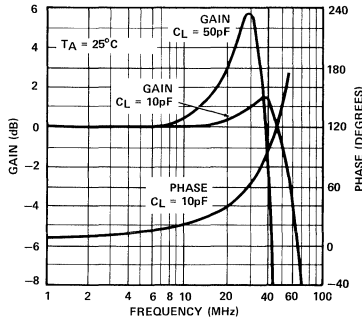
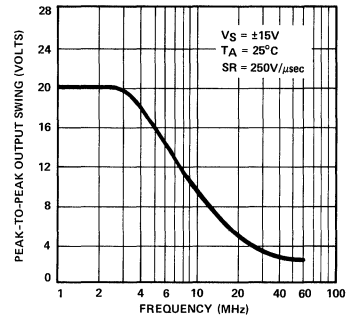
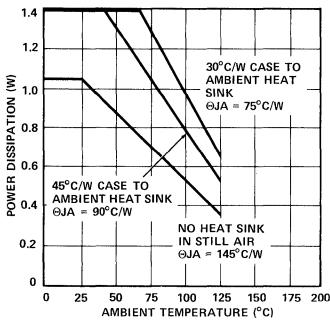
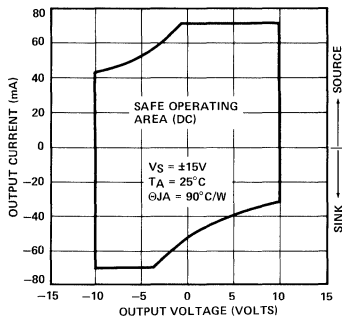
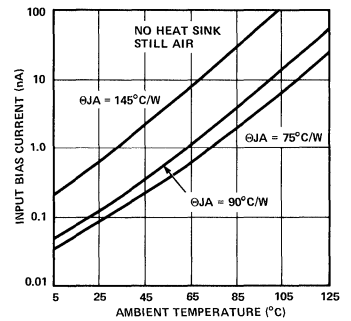
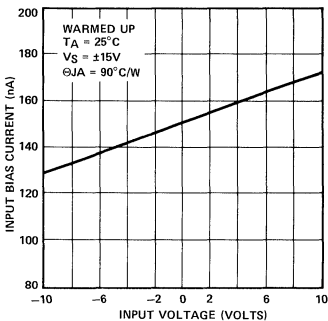
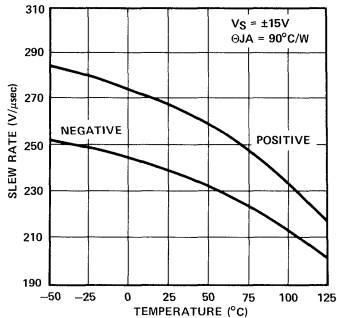
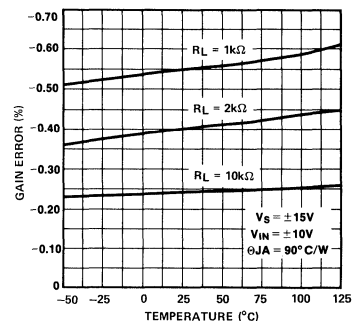
PARAMETER	SYMBOL	CONDITIONS	BUF-03N LIMIT	BUF-03G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	6	15	mV MAX
Slew Rate (Note 1)	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	220	180	V/ μ sec MIN
Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_{IN} = \pm 10V$	0.9960	0.9940	V/V MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6V$ to $\pm 18V$	0.71	1.42	mV/V MAX
Supply Current	I_{SY}	No Load	25	25	mA MAX

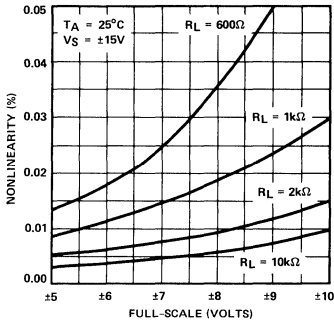
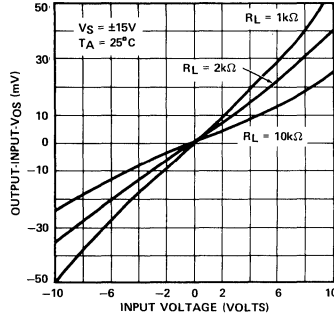
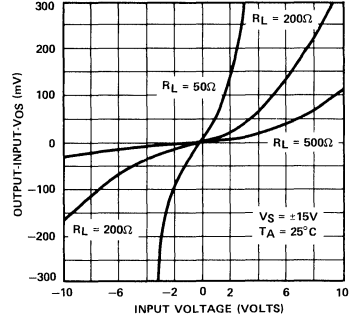
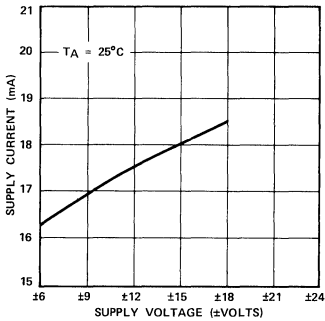
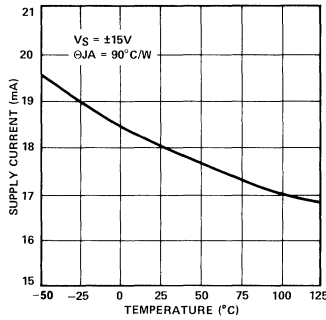
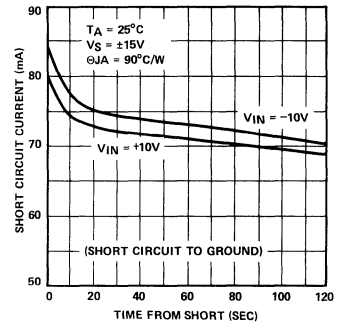
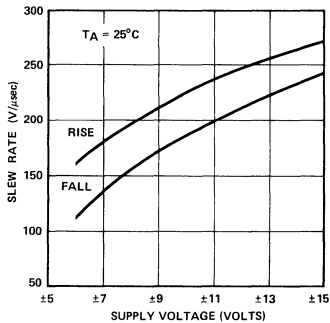
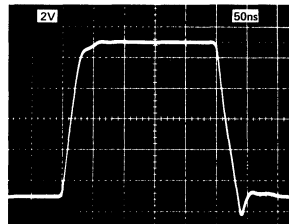
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_j = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-03N TYPICAL	BUF-03G TYPICAL	UNITS
Peak Load Current	$I_L(PK)$		70	70	mA
Input Bias Current	I_B		40	60	pA
Input Resistance	R_{IN}		5×10^{11}	5×10^{11}	Ω
Output Resistance	R_O		2	2	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	± 80	± 80	mV
Input Voltage Range (Reduced Accuracy)	IVR		± 11.5	± 11.5	V
Power Bandwidth	PBW	$V_{IN} = 10V_{P-P}$, $R_L \geq 2k\Omega$	9	8	MHz
Bandwidth	BW	$\Delta V_{IN} \leq 2V_{P-P}$	63	55	MHz
Settling Time	t_S	To 0.1%, $\pm 10V$ step	90	100	ns
Capacitive Load Capacity	C_{LOAD}	No Oscillations	1	1	μF
Propagation Delay	t_d	Step Input	7	7	ns
Rise Time	t_r	$\Delta V_{IN} = 0.5V$	7	7	ns
Wide Band Input Noise Voltage	V_n	DC to 50MHz	350	400	μV_{RMS}
Input Noise Voltage Density	e_n	$f = 10kHz$	50	60	nV/\sqrt{Hz}

NOTE:
1. Sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS
SLEW RATE vs CAPACITIVE LOAD

GAIN AND PHASE RESPONSE vs FREQUENCY

LARGE-SIGNAL FREQUENCY RESPONSE

MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE

OUTPUT CURRENT vs OUTPUT VOLTAGE

INPUT BIAS CURRENT vs TEMPERATURE (WARMED-UP)

INPUT BIAS CURRENT vs INPUT VOLTAGE

SLEW RATE vs TEMPERATURE

GAIN ERROR vs TEMPERATURE


TYPICAL PERFORMANCE CHARACTERISTICS
NONLINEARITY vs FULL-SCALE VOLTAGE

GAIN ERROR vs INPUT VOLTAGE

GAIN ERROR vs INPUT VOLTAGE

SUPPLY CURRENT vs SUPPLY VOLTAGE

SUPPLY CURRENT vs TEMPERATURE

OUTPUT SHORT-CIRCUIT CURRENT vs TIME

SLEW RATE vs SUPPLY VOLTAGE

SLEW RATE


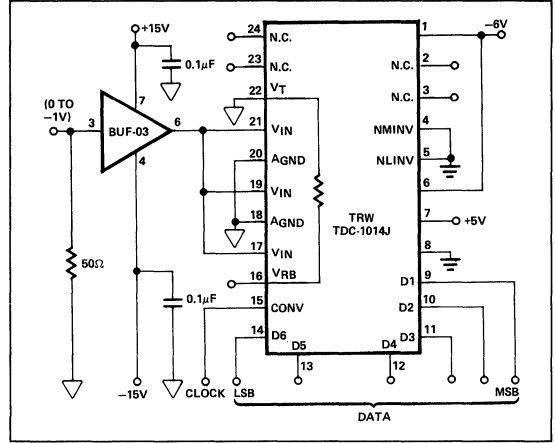


APPLICATIONS INFORMATION

OPERATING THE BUF-03 AT REDUCED POWER SUPPLIES

In most video applications the signal levels are significantly lower than the 20V peak-to-peak capability of the BUF-03. This suggests operating the BUF-03 at reduced power supplies; for example, at $\pm 6V$ supplies $\pm 2V$ signals can be handled. The obvious advantage of reduced supplies is the accompanying decrease in power dissipation: from a typical $540mW (= 30V \times 18mA)$ to $195mW (= 12V \times 16.2mA)$ at $\pm 6V$. At lower supply voltages heat sinking is no longer necessary. However, as shown on the slew rate vs supply voltage curve, slew rate does degrade at lower supplies. This occurs because of higher internal node capacitances at lower voltages and because of the slightly decreased operating current.

HIGH-SPEED 6-BIT A/D BUFFER



HIGH-SPEED SAMPLE/HOLD AMPLIFIER

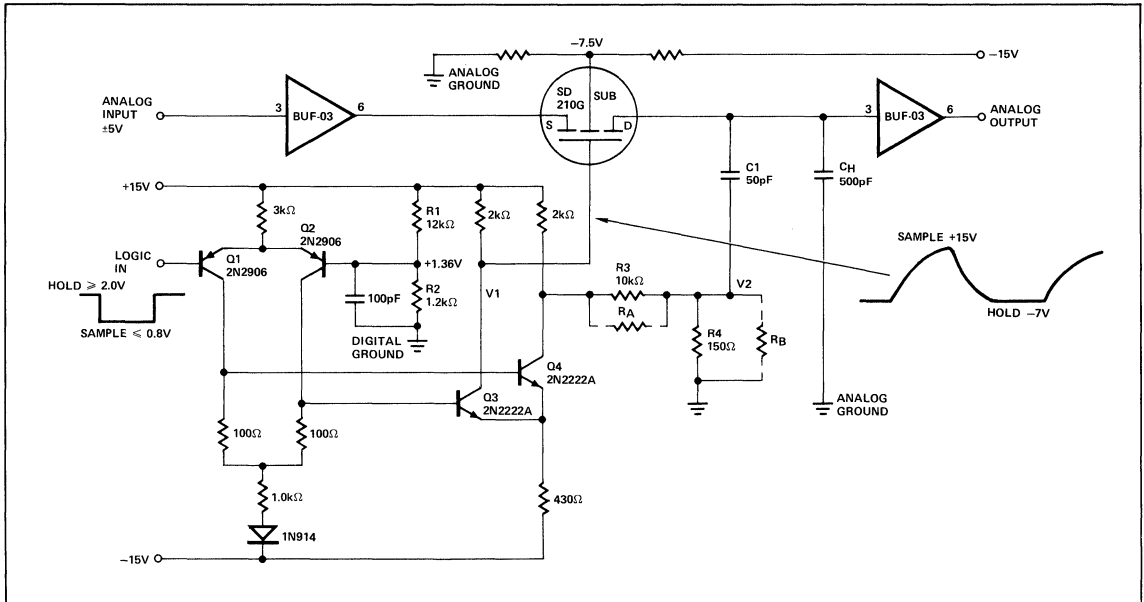


Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



VOLTAGE COMPARATORS

Precision Monolithics Inc.

8-3	Introduction	8-37	CMP-07
8-3	Definitions		Very High-Speed Comparator
8-6	CMP-01	8-40	CMP-404
	Fast Precision Comparator		Quad Low-Power Precision Comparator
8-14	CMP-02	8-48	PM-111/PM-211
	Low-Input-Current Precision Comparator		Precision Voltage Comparators
8-22	CMP-04	8-54	PM-119/PM-219/PM-319
	Quad Low-Power Precision Comparator		Dual Comparators
8-30	CMP-05	8-56	PM-139/PM-139A/PM-339A
	High-Speed Precision Comparator		Quad Low-Power Voltage Comparators



VOLTAGE COMPARATORS

Precision Monolithics Inc.

INTRODUCTION

A comparator provides a logic output indicating the amplitude relationship between two analog signal inputs.

When selecting a comparator, certain device parameters must be considered for proper design and application. These parameters are:

- V_{OS} (Input Offset Voltage)
- Response Time
- Slew Rate
- PSRR (Power Supply Rejection Ratio)
- I_B (Input Bias Current)
- CMVR (Common-Mode Voltage Range)
- Output Configuration
- Voltage Gain

The input offset voltage (V_{OS}) for a comparator should be as small as possible because in a high gain circuit it is the dominating factor that determines the exact threshold level. For this reason, comparators should be nulled or a Precision Comparator used so that the input differential voltage is as close to zero as practical when the output is at the logic switching threshold.

The voltage gain (A_V) determines the sensitivity and threshold accuracy of a comparator. For the ideal comparator, the gain could be considered infinite; and an extremely small voltage applied between the two inputs will cause a change in the output. In practice, some minimum voltage variation will be required at the input to effect a change in the output state. This minimum sensitivity will be determined from the voltage gain of the comparator. The relationship is as follows:

$$\Delta V_{IN(MIN)} = \frac{\Delta V_O}{A_V}$$

The quantity ΔV_O which is the difference between the high and low state of the output is generally chosen to be 2.5V to insure the matching of the comparator with the TTL load.

Precision Monolithics' comparator product line now spans high precision, low power and high speed comparators.

The CMP-01 is a fast precision comparator with low offset voltage. The CMP-02 offers the CMP-01's offset voltage performance along with lower input bias currents.

The quad CMP-04 offers both low power and low offset voltages. Existing "139" type applications can be upgraded by the pin compatible CMP-04. For very low power applications the CMP-404 drops into the "139" pinout, immediately reducing power consumption to 1.5 milliwatts. The PM-139/239/339 devices provide equal performance to "139/239/339" type comparators.

The CMP-05 brings together superior input specifications with very fast response times. This combination makes the CMP-05 the ideal choice in high-accuracy 10 and 12-bit data systems.

The latest addition to the PMI comparator line is the very high speed ECL output CMP-07 which offers 5 nanosecond response time in the industry standard "685" pinout.

DEFINITIONS

Average Offset Current Drift (TCI_{OS}) — The ratio of the change in the input offset current to the change in temperature producing it.

Average Offset Voltage Drift (TCV_{OS}) — The ratio of the change in the input offset voltage to the change in temperature producing it.

Average Offset Voltage Drift With External Trimming (TCV_{OSN}) — The ratio of the change in the input offset voltage to the change in temperature producing it, with the input offset voltage trimmed to zero at room temperature.

Common-Mode Rejection Ratio (CMRR) — The ratio of differential voltage gain to common-mode voltage gain, expressed in dB. CMRR is measured as the ratio of the change in common-mode voltage divided by the change in input offset voltage.

$$CMRR = 20 \log \left(\frac{A_{V(DIFF)}}{A_{V(CM)}} \right) = 20 \log \left(\frac{\Delta CMV}{\Delta V_{OS}} \right)$$

Common-Mode Voltage Range (CMVR) — The range of common-mode voltage on the input terminals for which operation within specifications is assured.

8
VOLTAGE COMPARATORS

Differential Input Resistance (R_{IN}) — The resistance looking into either input terminal with the other grounded.

Differential Input Voltage — The range of voltage between the input terminals for which operation within specifications is assured.

Input Bias Current (I_B) — The average of the two input currents, with the inputs tied together.

Input Offset Current (I_{OS}) — The difference between the currents into the two input terminals when the output is within a specified voltage range.

Input Offset Voltage (V_{OS}) — The voltage applied between the input terminals to obtain a specified output voltage range.

Input Slew Rate — The maximum rate of change in differential and/or common-mode input voltage which the input stage can follow.

Input To Output High Propagation Delay (t_{pd+}) — The time measured between the input signal's V_{OS} crossing and the output voltage's 50% low-to-high transition point. Specified for a given input voltage step size and overdrive.

Input To Output Low Propagation Delay (t_{pd-}) — The time measured between the input signal's V_{OS} crossing and the output voltage's 50% high-to-low transition point. Specified for a given input voltage step size and overdrive.

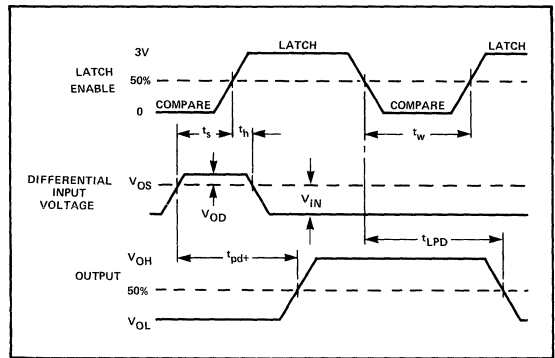
Latch Disable Propagation Delay (t_{LDD}) — The time measured between the 50% transition points of the latch enable signal and the output signal transition point.

Latch Hold Time (t_h) — The amount of time measured from 50% of the latch enable signal to the comparator-input trip-point crossing.

Latch Pulse Width (t_w) — The width of the latch enable pulse measured between the 50% points of the rising and falling pulse edges.

Latch Set-Up Time (t_s) — The amount of time measured from the comparator-input trip-point crossing to 50% of the latch enable control.

Switching Time Waveforms



Offset Voltage Adjustment Range — The change in offset voltage that can be obtained by adjusting a specified external nulling potentiometer.

Output Leakage Current (I_{LEAK}) — The current into the output terminal with a given output voltage and input drive equal to or greater than a specified value.

Output Sink Current (I_{SINK}) — The maximum negative current that can be delivered by the comparator.

Overdrive (V_{OD}) — The input step voltage (V_{IN}) of specified size drives the comparator from some initial input voltage to an input level just barely in excess of that required to bring the output from its high or low state to the logic threshold voltage. This excess is defined as the voltage overdrive.

Positive Output Voltage (V_{OH}) — The high output voltage level with a given load and an input drive equal to a specified value.

Power Supply Rejection Ratio (PSRR) — The ratio of the maximum change in input offset voltage to the specified change in power supply voltage.

Response Time (t_r) — The interval between the application of an input step function and the time when the output crosses the logic thresh-



Precision Monolithics Inc.

VOLTAGE COMPARATORS

old voltage. Logic threshold is defined as the voltage at the output of the comparator at which the loading logic circuitry changes its digital state, or, as 1.4V when the loading logic circuitry is not used.

Saturation Voltage (V_{OL}) — The low output voltage level with a given sink current and an input drive equal to a specified value.

Supply Currents — The currents required from the positive or negative supplies to operate the comparator without a load.

Voltage Gain (A_V) — The ratio of the change in output voltage (over a specified range) to the change in differential input voltage producing it.

∞

VOLTAGE COMPARATORS

FEATURES

- **Fast Response Time** 180ns Max
- **High Input Slew Rate** 92V/ μ s
- **Low Offset Voltage** 0.3mV Typical, 0.8mV Max
- **Low Offset Current** 4nA Typical, 25nA Max
- **Low Offset Drift** 1 μ V/ $^{\circ}$ C, 30pA/ $^{\circ}$ C
- **Standard Power Supplies** +5V or \pm 5V to \pm 18V
- **Guaranteed Operation from Single +5V Supply**
- **No Pull-Up Resistor Required for TTL Drive**
- **Wired OR Capability**
- **Fits 111, 106, 710 Sockets**
- **Easy Offset Nulling** Single 2k Ω Potentiometer
- **Easy to Use** Free from Oscillations

ORDERING INFORMATION†

+25 $^{\circ}$ C V _{OS} (mV)	PACKAGE		PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
	HERMETIC			
	TO-99 8-PIN	DIP 8-PIN		
0.8	CMP01J*	CMP01Z*	—	MIL
0.8	CMP01EJ	CMP01EZ	CMP01EP	COM
2.8	CMP01CJ	CMP01CZ	CMP01CP	COM

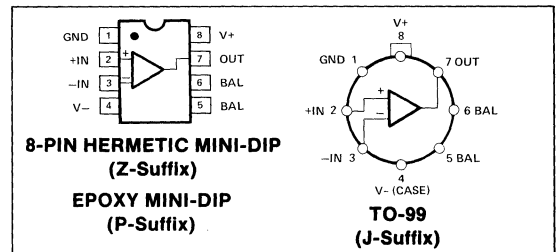
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

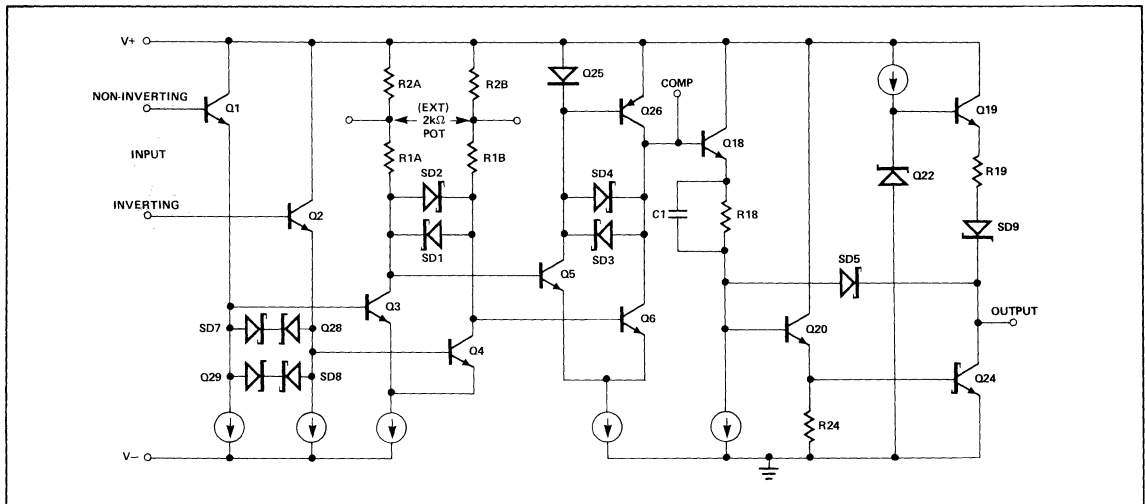
GENERAL DESCRIPTION

The CMP-01 is a monolithic fast precision voltage comparator using an advanced NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The CMP-01 is capable of operating over a wide range of supply voltages including single ended 5 volt supply. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13-bit A/D converters. The CMP-01 is pin-compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to the CMP-02 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ELECTRICAL CHARACTERISTICS** at $V_{S+} = 5V$, $V_{S-} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01 CMP-01E			CMP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	3	21	—	4	65	nA
Input Bias Current	I_B		—	250	500	—	300	720	nA
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive	—	150	—	—	150	—	ns
		5k Ω to 5V (Pull-Up) TTL Fan-Out = 4, 5k Ω to 5V (Pull-Up)	—	150	—	—	150	—	
Input Voltage Range	CMVR		1.8	1.7-3.8	3.5	1.8	1.7-3.8	3.5	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	—	2.3	3.2	—	2.4	3.8	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	11.5	16	—	12	19	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1) $V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.5	1.6	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	
With External Trim	TCV_{OSn}		—	1	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$T_A = +125^\circ C$, (Note 1) $T_A = -55^\circ C$, (Note 1)	—	4	25	nA
Average Input Offset Current Drift	TCI_{OS}	$+25^\circ C \leq T_A \leq +125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	—	12	—	
Input Bias Current	I_B	$T_A = +125^\circ C$ $T_A = -55^\circ C$	—	330	600	nA
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	
Response Time	t_r	100mV Step, 5mV Overdrive, (Note 2) $T_A = +125^\circ C$, No Load $T_A = -55^\circ C$, No Load	—	220	—	ns
Input Voltage Range	CMVR		± 12	± 13	—	
Common-Mode Rejection Ratio	CMRR		88	106	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	75	96	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$ $V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.20	0.4	V
			—	0.32	0.5	

NOTES:

- These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

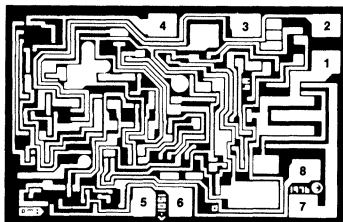
PARAMETER	SYMBOL	CONDITIONS	CMP-01E			CMP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.4	—	0.5	3.5	mV
		$V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.5	2.4	—	0.6	4.3	
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	$\mu V/^\circ C$
			—	1.0	—	—	1.2	—	
With External Trim	TCV_{OSn}		—	—	—	—	—	—	
			—	—	—	—	—	—	
Input Offset Current	I_{OS}	$T_A = +70^\circ C$, (Note 1)	—	4	25	—	5	80	nA
		$T_A = 0^\circ C$, (Note 1)	—	5	45	—	6	120	
Average Input Offset Current Drift	TCI_{OS}	$+25^\circ C \leq T_A \leq +70^\circ C$ $0^\circ C \leq T_A \leq +25^\circ C$	—	12	—	—	12	—	$\mu A/^\circ C$
			—	35	—	—	40	—	
Input Bias Current	I_B	$T_A = +70^\circ C$	—	330	600	—	340	900	nA
		$T_A = 0^\circ C$	—	400	950	—	450	1200	
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive $T_A = +70^\circ C$, No Load $T_A = 0^\circ C$, No Load	—	150	—	—	150	—	ns
			—	100	—	—	100	—	
Input Voltage Range	CMVR		± 12.0	± 13.3	—	± 12.0	± 13.3	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0$	—	0.17	0.4	—	0.17	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.3	0.5	—	0.31	0.5	

NOTES:

- These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.



DICE CHARACTERISTICS



**DIE SIZE 0.065 × 0.042 inch, 2730 sq. mils
(1.651 × 1.069 mm, 1.761 sq. mm)**

1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	0.8	2.8	mV MAX
Input Offset Current	I_{OS}	(Note 1)	25	80	nA MAX
Input Bias Current	I_B		600	900	nA MAX
Differential Input Resistance	R_{IN}	(Note 2)	150	100	k Ω MIN
Input Voltage Range	CMVR		± 12.5	± 12.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S \leq 18V$ $-18V \leq V_S \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4 —	— 2.4	V MIN
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	2	8	μA MAX
Positive Supply Current	I+	$V_{IN} \leq -10mV$	8.0	8.5	mA MAX
Negative Supply Current	I-	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

WAFER TEST LIMITS at $V_S + = 5V$ and $V_S - = 0V$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		21	65	nA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

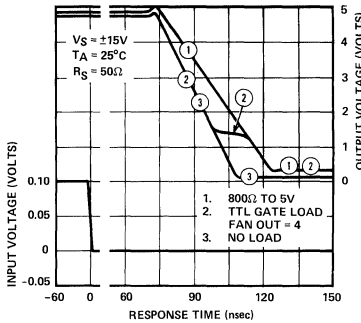
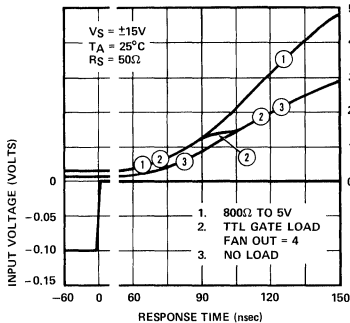
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N TYPICAL	CMP-01GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		35	40	pA/°C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25^\circ C$	110	110	ns

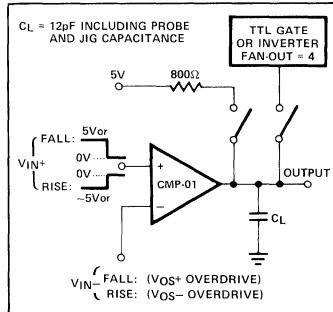


TYPICAL PERFORMANCE CHARACTERISTICS

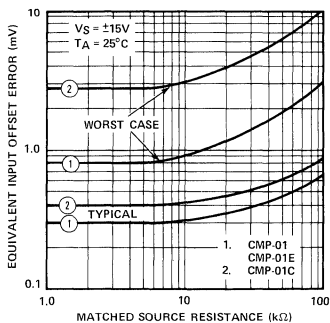
RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



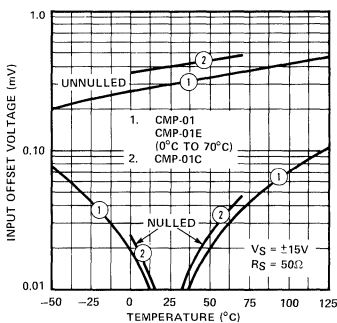
RESPONSE TIME TEST CIRCUIT



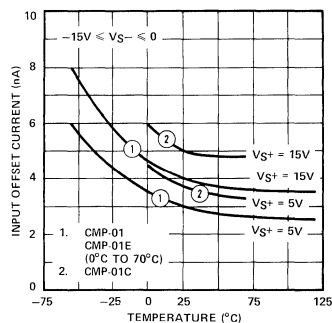
INPUT OFFSET ERROR vs SOURCE RESISTANCE



OFFSET VOLTAGE vs TEMPERATURE

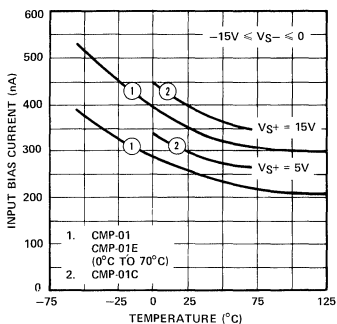


INPUT OFFSET CURRENT vs TEMPERATURE

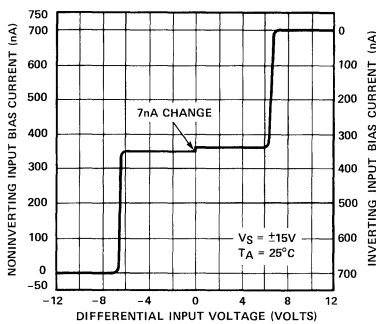


VOLTAGE COMPARATORS

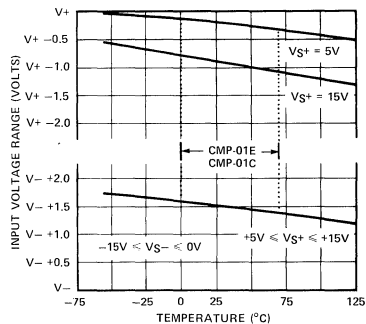
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

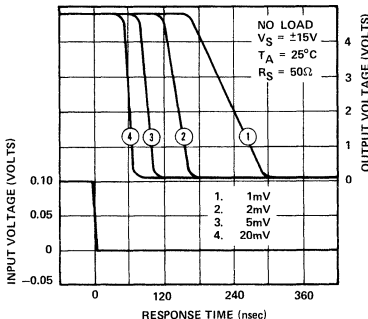
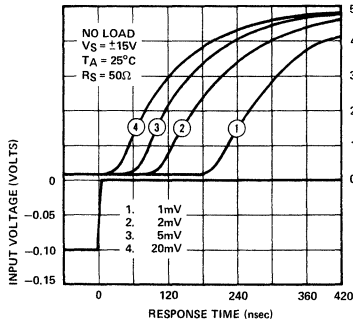


INPUT VOLTAGE RANGE vs TEMPERATURE

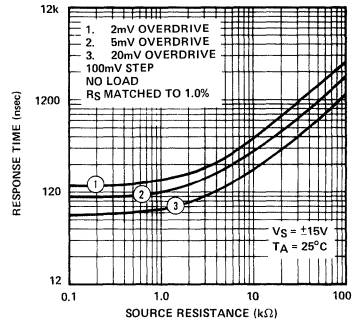


TYPICAL PERFORMANCE CHARACTERISTICS

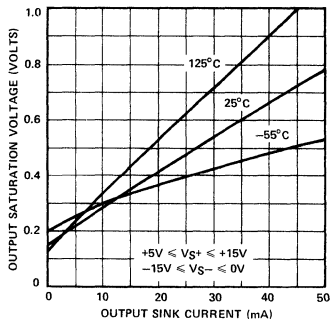
RESPONSE TIME FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES



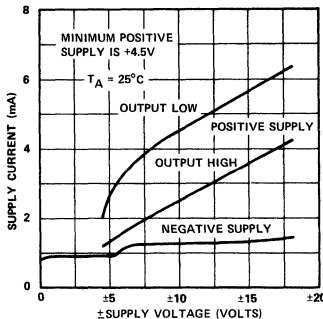
RESPONSE TIME vs SOURCE RESISTANCE



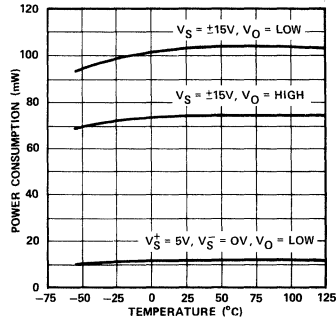
SATURATION VOLTAGE vs SINK CURRENT



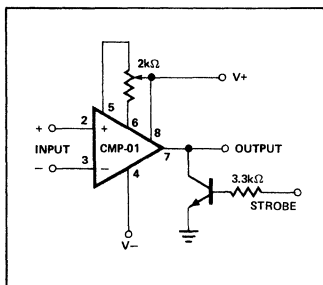
SUPPLY CURRENT vs SUPPLY VOLTAGE



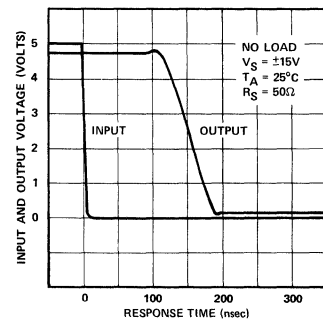
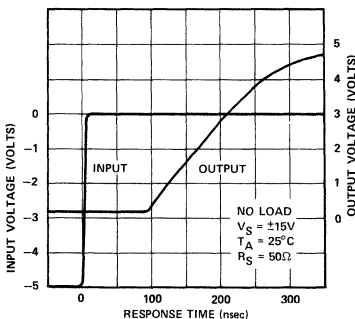
POWER CONSUMPTION vs TEMPERATURE



OFFSET TRIMMING AND STROBE CIRCUIT



RESPONSE TIME FOR 5V STEP AND 5mV OVERDRIVE





APPLICATIONS INFORMATION

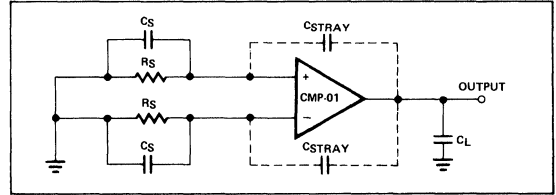
The CMP-01 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-01 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading (C_L). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

and if $C_S \geq 20pF$ $\left(\begin{matrix} \text{maximum step size} \\ \text{minimum overdrive} \end{matrix} \right)$

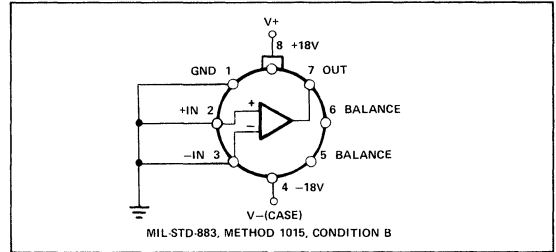
the response time will approximate the response time for low values of R_S . It should be noted that the offset nulling terminals do not require bypassing for stability. As with all

wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

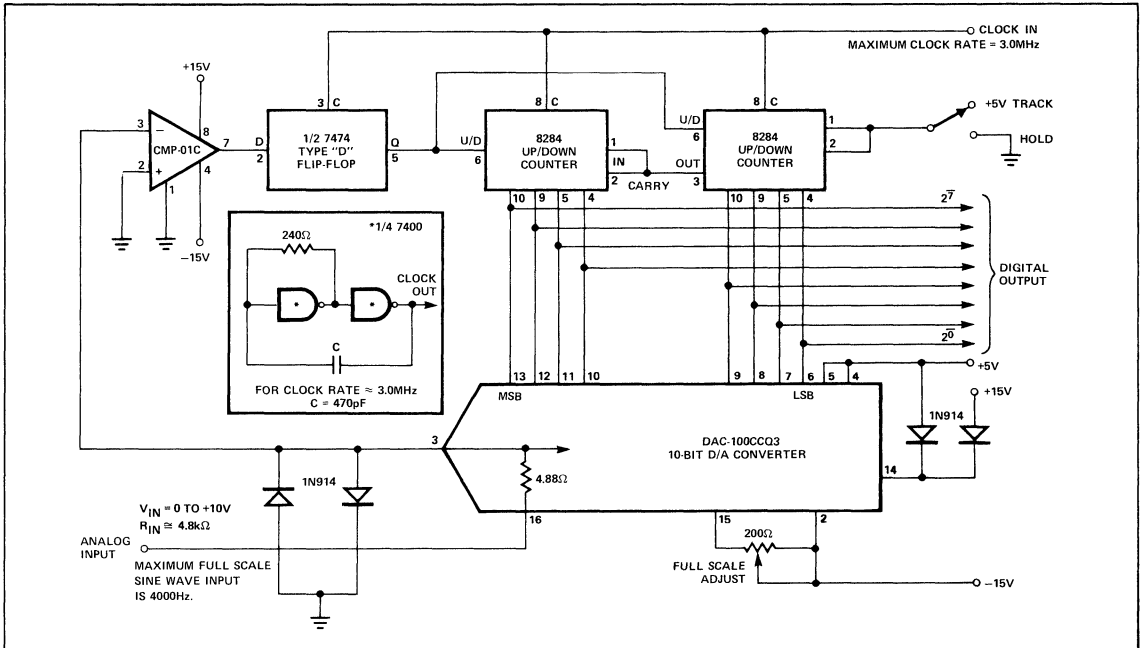
MINIMIZING OSCILLATION



BURN-IN CIRCUIT



8-BIT TRACKING A/D CONVERTER



VOLTAGE COMPARATORS



CMP-02

LOW-INPUT-CURRENT
PRECISION COMPARATOR

Precision Monolithics Inc.

FEATURES

- **Low Offset Voltage** 0.3mV Typ, 0.8mV Max
- **Low Offset Current** 0.3nA Typ, 3nA Max
- **Low Bias Current** 28nA Typ, 50nA Max
- **Low Offset Drift** 1 μ V/ $^{\circ}$ C, 4pA/ $^{\circ}$ C
- **High Gain** 200,000 Min
- **High CMRR** 110dB Typ, 94dB Min
- **High Input Impedance** 16M Ω
- **Fast Response Time** 190ns Typ, 270ns Max
- **Standard Power Supplies** +5V or \pm 5V to \pm 18V
- **Guaranteed Operation from Single +5V**
- **No Pull-Up Resistor Required for TTL Drive**
- **Wired OR Capability**
- **Fits 111, 106, 710 Sockets**
- **Easy Offset Nulling** Single 2k Ω Potentiometer
- **Easy to Use** Free from Oscillations

ORDERING INFORMATION†

+25 $^{\circ}$ C V _{OS} (mV)	PACKAGE			
	HERMETIC		PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	DIP 8-PIN		
0.8	CMP02J*	CMP02Z*	—	MIL
2.8	CMP02EJ	CMP02EZ	CMP02EP	COM
	CMP02CJ	CMP02CZ	CMP02CP	COM

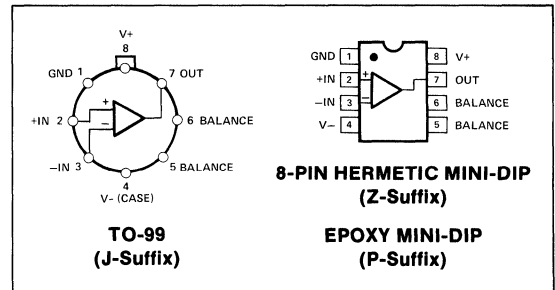
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

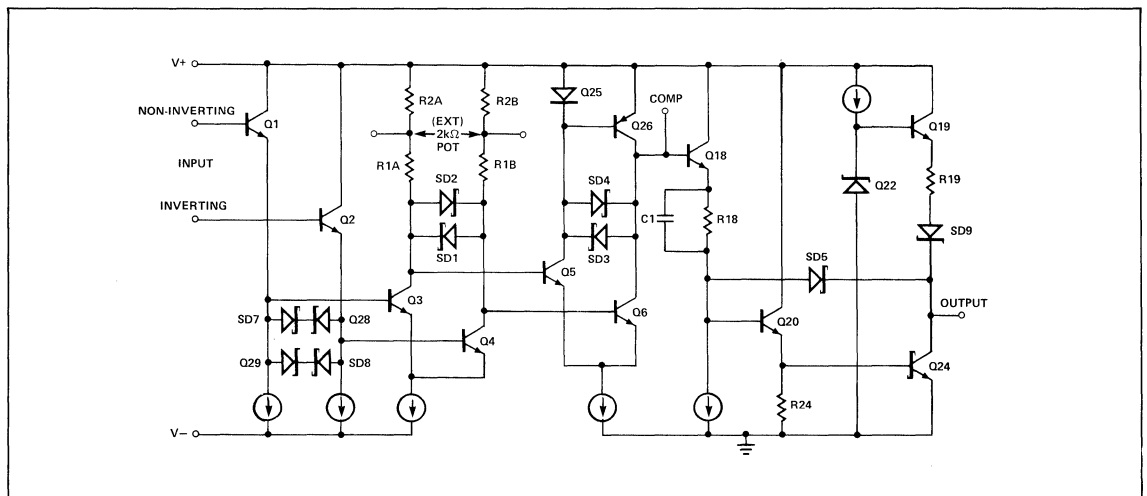
GENERAL DESCRIPTION

The CMP-02 is a monolithic low input current comparator using an advanced NPN-Schottky Barrier Diode process. It features superior input characteristics with extremely low offset voltage, offset current, bias current and temperature drift. High common-mode and power supply rejection plus good response time contribute to excellent performance in the most demanding applications. The balanced offset nulling, large output drive, and wired-OR capability combined with internal pull-up maximize application convenience. The CMP-02 is capable of operating over a wide range of supply voltages, including single plus 5 volt supply operation, and is pin-compatible to earlier 111, 106, and 710 types. For applications requiring faster response time, please refer to the CMP-01 fast precision comparator data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ELECTRICAL CHARACTERISTICS** at $V_S = 5V$, $V_{S-} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02			CMP-02C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.25	3	—	0.35	14	nA
Input Bias Current	I_B		—	24	45	—	30	90	nA
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive	—	250	—	—	250	—	ns
		5k Ω to 5V (Pull-Up) TTL Fan-Out = 4, 5k Ω to 5V	—	250	—	—	250	—	
Input Voltage Range	CMVR		1.8-3.5	1.7-3.8	—	1.8-3.5	1.7-3.8	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -3.5mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	—	2.2	3	—	2.3	3.6	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	11	15	—	11.5	18	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.6	mV
		$V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.5	2.8	
Average Input Offset Voltage Drift						
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	—	1.0	—	
Input Offset Current	I_{OS}	$T_A = +125^\circ C$, (Note 1)	—	0.3	4	nA
		$T_A = -55^\circ C$, (Note 1)	—	0.4	12	
Average Input Offset Current Drift	TCI_{OS}	$+25^\circ C \leq T_A \leq +125^\circ C$	—	2	—	$pA/^\circ C$
		$-55^\circ C \leq T_A \leq +25^\circ C$	—	4	—	
Input Bias Current	I_B	$T_A = +125^\circ C$	—	25	50	nA
		$T_A = -55^\circ C$	—	45	120	
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive	—	310	—	ns
		$T_A = +125^\circ C$, No Load $T_A = -55^\circ C$, No Load	—	155	—	
Input Voltage Range	CMVR		± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR		88	106	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	75	96	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$	—	0.20	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.32	0.5	

NOTES:

- These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.
- Sample tested.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02E			CMP-02C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.4	—	0.5	3.5	mV
		$V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.5	2.4	—	0.6	4.3	
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	—	1	—	—	1.2	—	
Input Offset Current	I_{OS}	$T_A = +70^\circ C$, (Note 1)	—	0.3	3	—	0.4	15	nA
		$T_A = 0^\circ C$, (Note 1)	—	0.4	6	—	0.5	25	
Average Input Offset Current Drift	TCI_{OS}	$+25^\circ C \leq T_A \leq +70^\circ C$	—	2	—	—	3	—	$\mu A/^\circ C$
		$0^\circ C \leq T_A \leq +25^\circ C$	—	4	—	—	5	—	
Input Bias Current	I_B	$T_A = +70^\circ C$	—	26	50	—	33	100	nA
		$T_A = 0^\circ C$	—	34	80	—	42	160	
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive	—	225	—	—	225	—	ns
		$T_A = +70^\circ C$, No Load	—	180	—	—	180	—	
		$T_A = 0^\circ C$, No Load	—	180	—	—	180	—	
Input Voltage Range	CMVR		± 12.0	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0$	—	0.17	0.4	—	0.17	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.30	0.5	—	0.31	0.5	

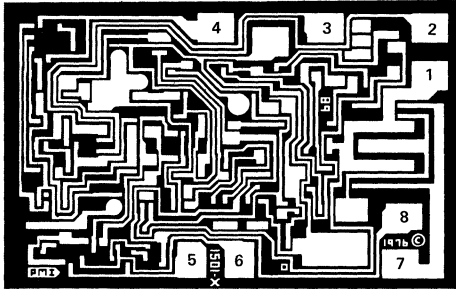
NOTES:

1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.





DICE CHARACTERISTICS



1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

For additional DICE information refer to 1986 Data Book, Section 2.

DIE SIZE 0.065 × 0.042 inch, 2730 sq. mils
(1.651 × 1.069 mm, 1.761 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ $R_S \leq 50k\Omega$	0.8	2.8	mV MAX
			0.9	3	
Input Offset Current	I_{OS}		3	15	nA MAX
Input Bias Current	I_B		50	100	nA MAX
Differential Input Resistance	R_{IN}		1.7	0.9	M Ω MIN
Input Voltage Range	CMVR		± 12.5	± 12.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S + \leq 18V$ $-18V \leq V_S - \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4	—	V MIN
			—	2.4	
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	2	8	μA MAX
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	8	8.5	mA MAX
Negative Supply Current	I_-	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

WAFER TEST LIMITS at $V_S + = 5V$ and $V_S - = 0V$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		3	14	nA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

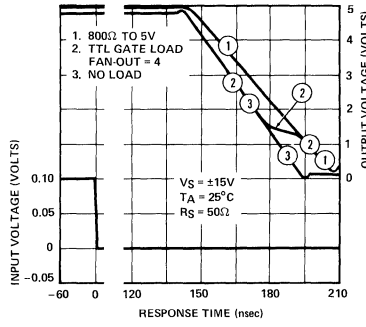
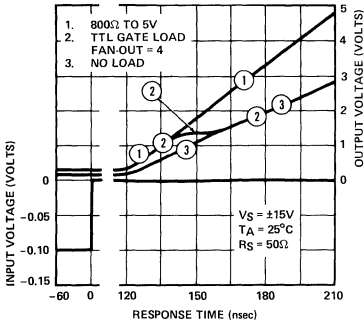
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N TYPICAL	CMP-02GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		4	5	pA/ $^\circ C$
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25^\circ C$	190	190	ns

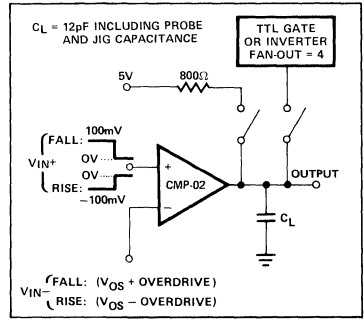


TYPICAL PERFORMANCE CHARACTERISTICS

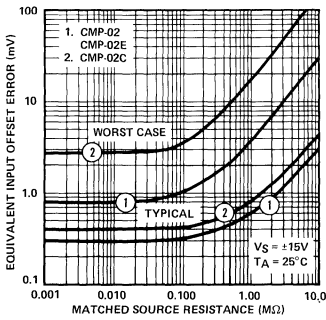
RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



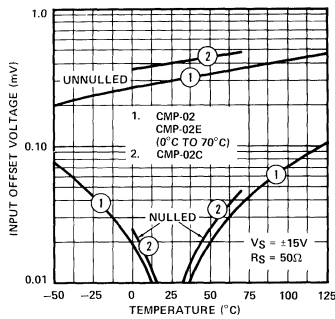
RESPONSE TIME TEST CIRCUIT



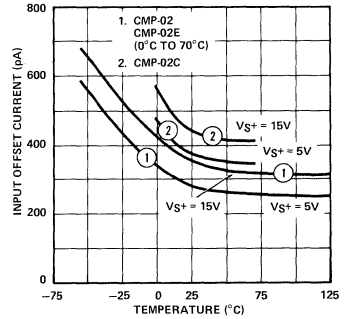
INPUT OFFSET ERROR vs SOURCE RESISTANCE



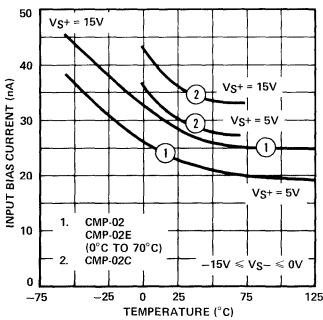
OFFSET VOLTAGE vs TEMPERATURE



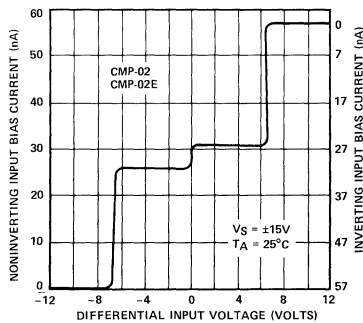
INPUT OFFSET CURRENT vs TEMPERATURE



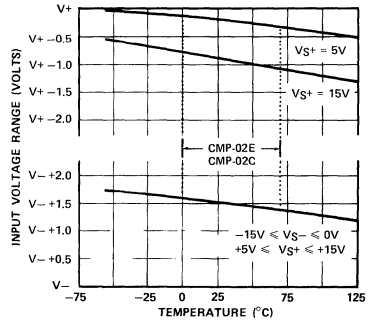
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT VOLTAGE RANGE vs TEMPERATURE

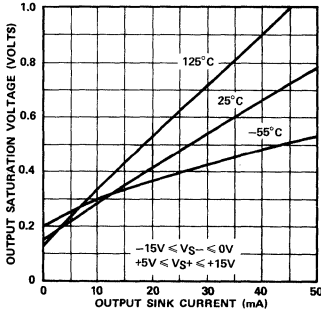


VOLTAGE COMPARATORS

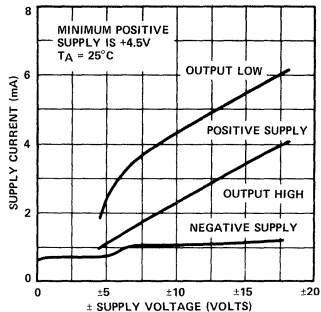


TYPICAL PERFORMANCE CHARACTERISTICS

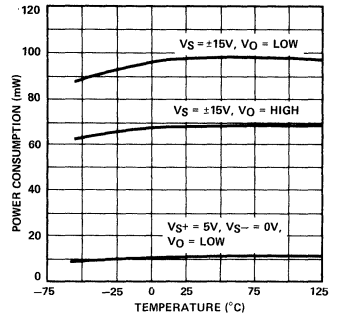
SATURATION VOLTAGE vs SINK CURRENT



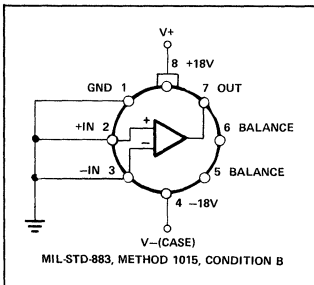
SUPPLY CURRENT vs SUPPLY VOLTAGE



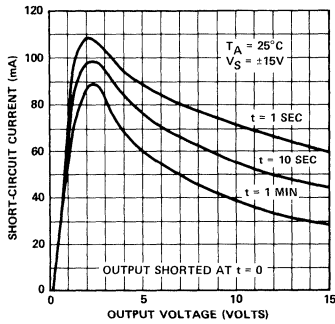
POWER CONSUMPTION vs TEMPERATURE



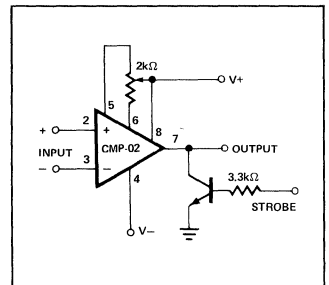
STANDARD BURN-IN CIRCUIT



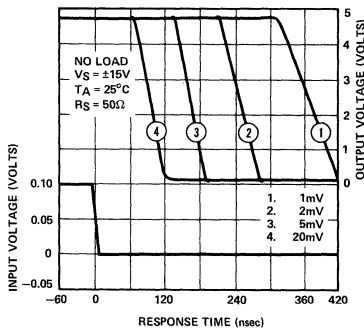
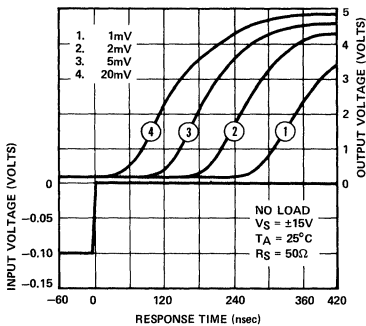
OUTPUT SHORT-CIRCUIT CURRENT vs OUTPUT VOLTAGE



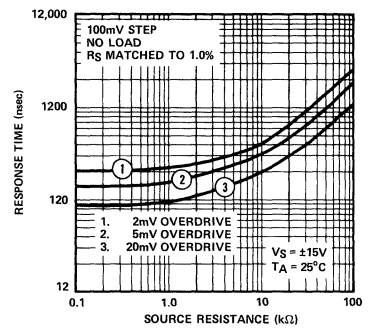
OFFSET TRIMMING AND STROBE CIRCUITS



RESPONSE TIME, 100mV STEP AND VARIOUS INPUT OVERDRIVES



RESPONSE TIME vs SOURCE RESISTANCE



APPLICATIONS INFORMATION

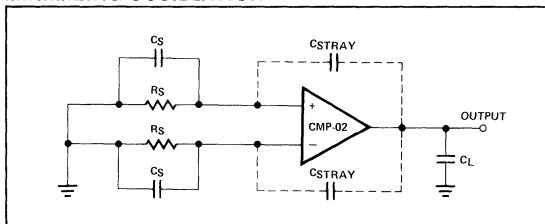
The CMP-02 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-02 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading (C_L). The capacitive loading techniques will eliminate the oscillations, but result in slower

response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

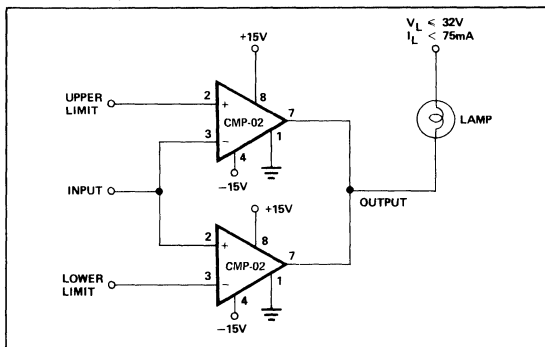
$$\text{and if } C_S \geq 20\text{pF} \left(\frac{\text{maximum step size}}{\text{minimum overdrive}} \right)$$

the response time will approximate the response time for low values of R_S . It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

MINIMIZING OSCILLATION



PRECISION, DUAL LIMIT, GO/NO GO TESTER



Precision Monolithics Inc.

FEATURES

- High Gain 200V/mV Typ
- Single or Dual Supply Operation
- Input Voltage Range Includes Ground
- Low Power Consumption (1.5mW/Comparator)
- Low Input Bias Current 100nA Max
- Low Input Offset Current 10nA Max
- Low Offset Voltage 1mV Max
- Low Output Saturation Voltage 250mV @ 4mA
- Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS
- Directly Replaces LM139/239/339 Comparators

ORDERING INFORMATION†

25° C V _{OS} (mV)	DIP PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC 14-PIN	PLASTIC 14-PIN	
1	CMP04BY*	—	MIL
1	CMP04FY	—	IND
1	—	CMP04FP	COM

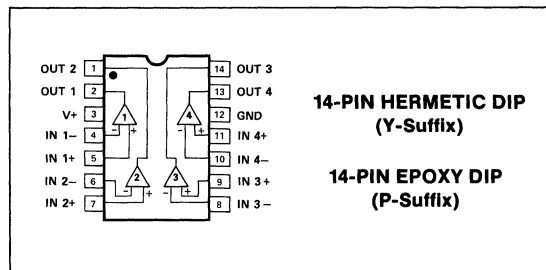
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP-04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V⁻ for split supplies. A low power supply current of 2mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

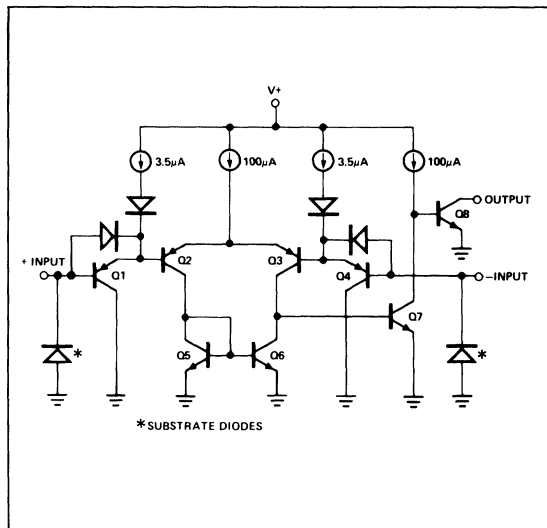
PIN CONNECTIONS



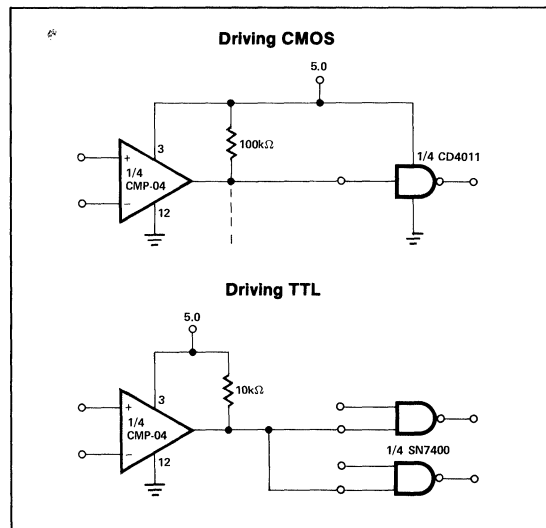
14-PIN HERMETIC DIP
(Y-Suffix)

14-PIN EPOXY DIP
(P-Suffix)

SIMPLIFIED SCHEMATIC (1/4 CMP-04)



TYPICAL INTERFACE



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	36V or ±18V
Differential Input Voltage	36V _{DC}
Input Voltage	-0.3V to +36V
Power Dissipation (Note 1)	500mW
Operating Temperature Range	
CMP-04FY	-25°C to +85°C
CMP-04BY	-55°C to +125°C
CMP-04FP	0°C to +70°C
DICE Junction Temperature (T _j)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
P-Suffix	-65°C to +125°C

Input Current (V _{IN} < -3.0V)	50mA
Output Short-Circuit to GND	Continuous
Lead Temperature (Soldering, 60 sec)	300°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
Hermetic DIP (Y)	100°C	10mW/°C
Plastic DIP (P)	50°C	6mW/°C

ELECTRICAL CHARACTERISTICS at V₊ = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S = 0Ω, R _L = 5.1kΩ V _O = 1.4V, (Note 1)	—	0.4	1	mV
Input Offset Current	I _{OS}	I _{IN(+)} = I _{IN(-)} R _L = 5.1kΩ V _O = 1.4V	—	2	10	nA
Input Bias Current	I _B	I _{IN(+)} or I _{IN(-)}	—	25	100	nA
Voltage Gain	A _V	R _L ≥ 15kΩ, V ₊ = 15V, (Note 5)	80	200	—	V/mV
Large-Signal Response Time	t _r	V _{IN} = TTL Logic Swing V _{REF} = 1.4V, (Note 4) V _{RL} = 5V, R _L = 5.1kΩ	—	300	—	ns
Small-Signal Response Time	t _r	V _{IN} = 100mV Step, (Note 4) 5mV Overdrive V _{RL} = 5V, R _L = 5.1kΩ	—	1.3	—	μs
Input Voltage Range	CMVR	(Note 2)	0	—	V+ - 1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	80	100	—	dB
Power Supply Rejection Ratio	PSRR	V ₊ = +5V to 18V, (Note 5)	80	100	—	dB
Saturation Voltage	V _{OL}	V _{IN(-)} ≥ 1V, V _{IN(+)} = 0, I _{SINK} ≤ 4mA	—	250	400	mV
Output Sink Current	I _{SINK}	V _{IN(-)} ≥ 1V, V _{IN(+)} = 0, V _O ≤ 1.5V	6	16	—	mA
Output Leakage Current	I _{LEAK}	V _{IN(+)} ≥ 1V, V _{IN(-)} = 0, V _O = 30V	—	0.1	100	nA
Supply Current	I ₊	R _L = ∞, All Comps V ₊ = 30V	—	0.8	2.0	mA

NOTES:

- At output switch point, V_O = 1.4V, R_S = 0Ω with V₊ from 5V; and over the full input common-mode range (0V to V₊ - 1.5V).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V₊ - 1.5V, but either or both inputs can go to +30V without damage.
- R_L ≥ 15kΩ, V₊ = 15V, V_{CM} = 1.5V to 13.5V.
- Sample tested.
- Guaranteed by design.


VOLTAGE COMPARATORS



ELECTRICAL CHARACTERISTICS at $V+ = +5V$. For CMP-04BY, $-55^{\circ}C \leq T_A \leq 125^{\circ}C$. For CMP-04FY, $-25^{\circ}C \leq T_A \leq 85^{\circ}C$. For CMP-04FP, $0^{\circ}C \leq T_A \leq 70^{\circ}C$, unless otherwise noted.

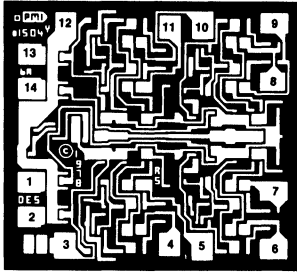
PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F (Note 3)			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	—	1	2	mV
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	—	4	20	nA
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$	—	40	200	nA
Voltage Gain	A_V	$R_L \geq 15k\Omega$, $V+ = 15V$, (Note 5)	70	125	—	V/mV
Large-Signal Response Time	t_r	$V_{IN} =$ TTL Logic Swing $V_{REF} = 1.4V$, (Note 4) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	300	—	ns
Small-Signal Response Time	t_r	$V_{IN} = 100mV$ Step, (Note 4) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	1.3	—	μs
Input Voltage Range	CMVR	(Note 2)	0	—	$V+ - 1.5$	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	60	100	—	dB
Power Supply Rejection Ratio	PSRR	$V+ = +5V$ to 18V	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$	—	250	700	mV
Output Sink Current	I_{SINK}	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $V_O \leq 1.5V$	5	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0$, $V_O = 30V$	—	0.1	200	nA
Supply Current	$I+$	$R_L = \infty$, All Comps $V+ = 30V$	—	1.2	3.0	mA

NOTES:

- At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with $V+$ from 5V; and over the full input common-mode range (0V to $V+ - 1.5V$).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V+ - 1.5V$, but either or both inputs can go to +30V without damage.
- $R_L \geq 15k\Omega$, $V+ = 15V$, $V_{CM} = 1.5V$ to 13.5V.
- Sample tested.
- Guaranteed by design.



DICE CHARACTERISTICS

DIE SIZE 0.052 × 0.056 inch, 2912 sq. mils
(1.32 × 1.42 mm, 1.88 sq. mm)

- | | |
|---------------------------|----------------------------|
| 1. OUTPUT (2) | 8. INVERTING INPUT (3) |
| 2. OUTPUT (1) | 9. NONINVERTING INPUT (3) |
| 3. POSITIVE SUPPLY | 10. INVERTING INPUT (4) |
| 4. INVERTING INPUT (1) | 11. NONINVERTING INPUT (4) |
| 5. NONINVERTING INPUT (1) | 12. GROUND (SUBSTRATE) |
| 6. INVERTING INPUT (2) | 13. OUTPUT (4) |
| 7. NONINVERTING INPUT (2) | 14. OUTPUT (3) |

For additional DICE information refer to
1986 Data Book, Section 2.WAFER TEST LIMITS at $V_+ = +5V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N LIMIT	CMP-04G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	1	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	10	25	nA MAX
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$, (Note 1)	100	100	nA MAX
Voltage Gain	A_V	$R_L \geq 15k\Omega$, $V_+ = 15V$, (Note 3)	80	50	V/mV MIN
Input Voltage Range	CMVR	(Notes 2, 3)	$V_+ - 1.5$	$V_+ - 1.5$	V MAX
Common-Mode Rejection Ratio	CMRR	(Note 4)	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_+ = 5V$ to $+18V$	80	80	dB MIN
Saturation Voltage	V_{OL}	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$	400	400	mV MAX
Output Sink Current	I_{SINK}	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $V_O \leq 1.5V$	6	6	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0$, $V_O = 30V$	100	100	nA MAX
Supply Current	I_+	$R_L = \infty$, All Comps $V_+ = 30V$	2	2	mA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = +5V$, unless otherwise noted.

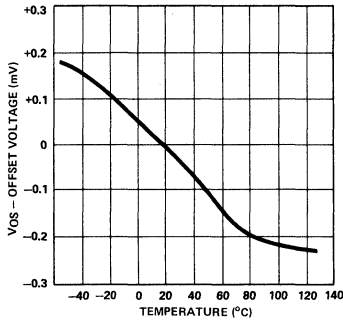
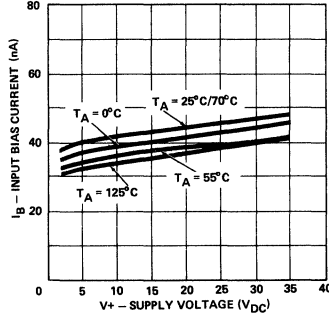
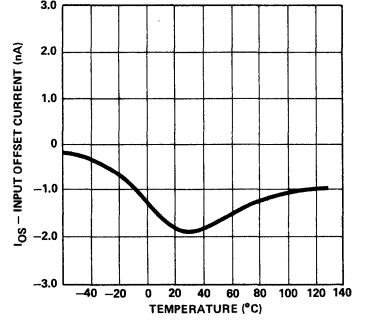
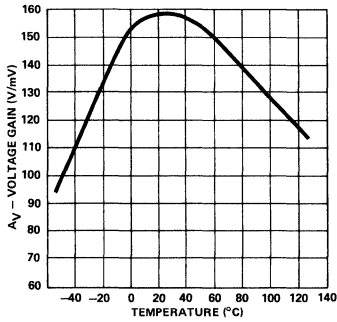
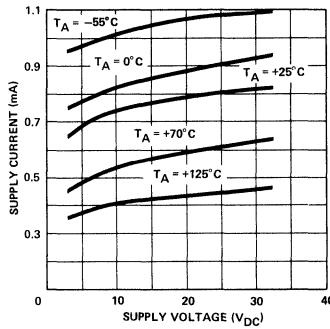
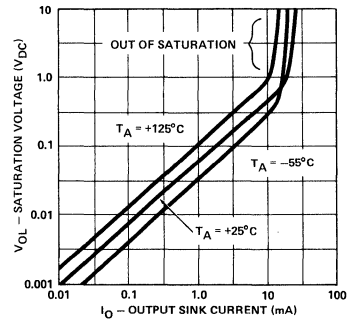
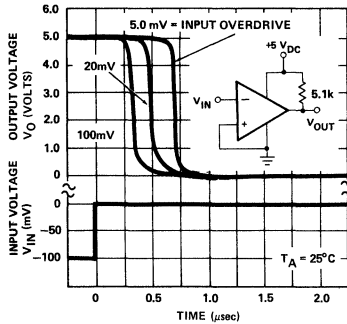
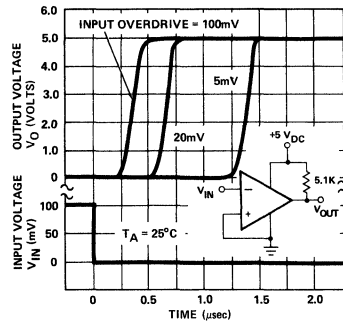
PARAMETER	SYMBOL	CONDITIONS	CMP-04N TYPICAL	CMP-04G TYPICAL	UNITS
Large-Signal Response Time	t_r	$V_{IN} =$ TTL Logic Swing $V_{REF} = 1.4V$, (Note 5) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	600	600	ns
Small-Signal Response Time	t_r	$V_{IN} = 100mV$ Step, (Note 5) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	1.3	1.3	μs

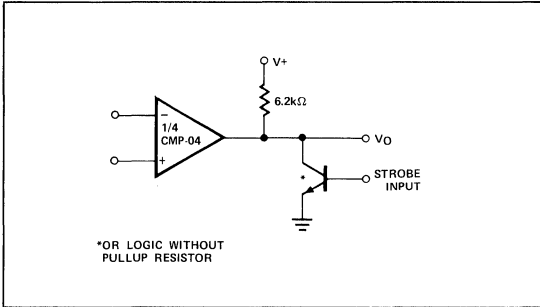
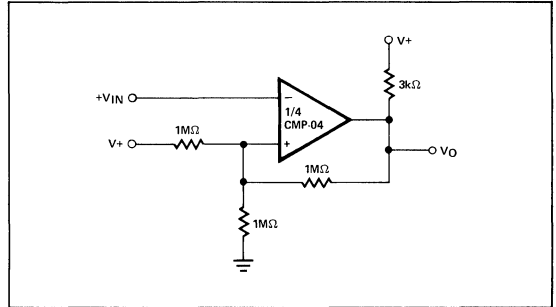
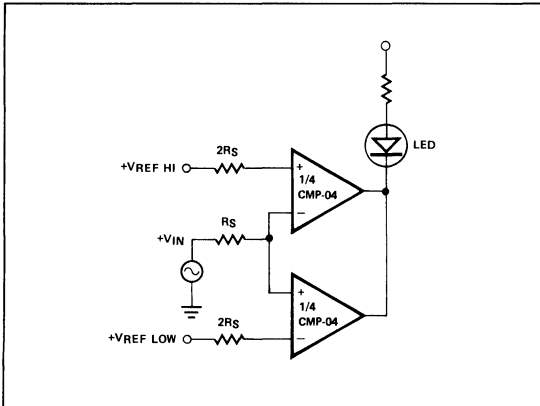
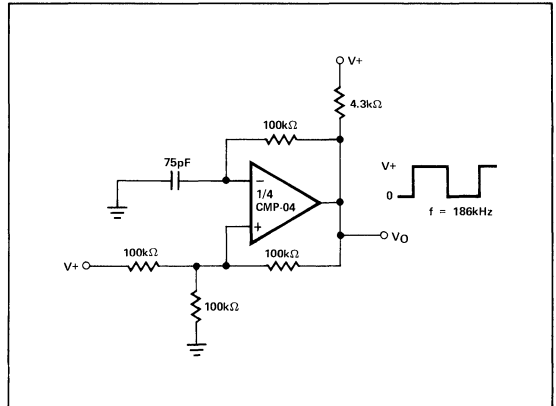
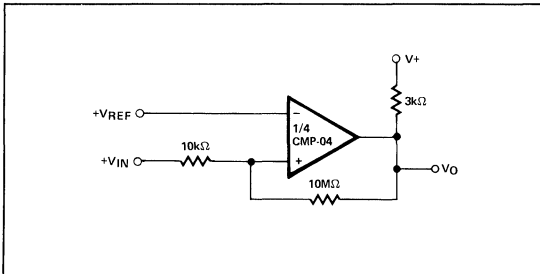
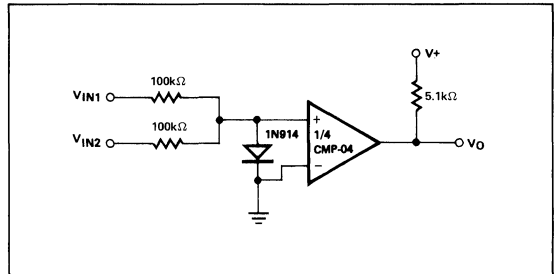
NOTES:

- At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V_+ from 5V; and over the full input common-mode range (0V to $V_+ - 1.5V$).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the

common-mode voltage range is $V_+ - 1.5V$, but either or both inputs can go to $+30V$ without damage.

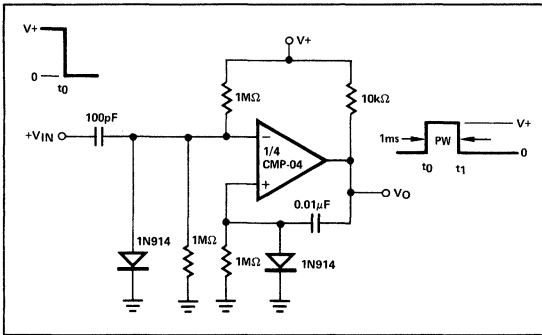
- Guaranteed by design.
- $R_L \geq 15k\Omega$. $V_{CM} = 1.5V$ to $13.5V$.
- Sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS
OFFSET VOLTAGE vs TEMPERATURE

INPUT BIAS CURRENT vs V+ AND TEMPERATURE

INPUT OFFSET CURRENT vs TEMPERATURE

VOLTAGE GAIN vs TEMPERATURE

SUPPLY CURRENT vs SUPPLY VOLTAGE

OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION


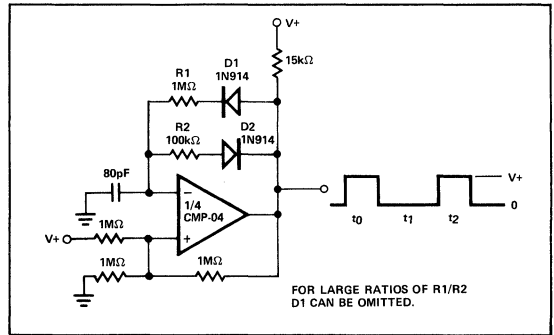
TYPICAL APPLICATIONS
OUTPUT STROBING

INVERTING COMPARATOR WITH HYSTERESIS

LIMIT COMPARATOR

SQUAREWAVE OSCILLATOR

NONINVERTING COMPARATOR WITH HYSTERESIS

COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY




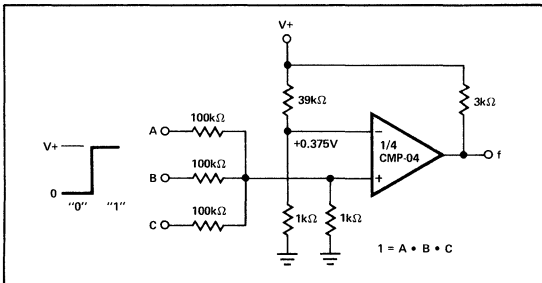
ONE-SHOT MULTIVIBRATOR



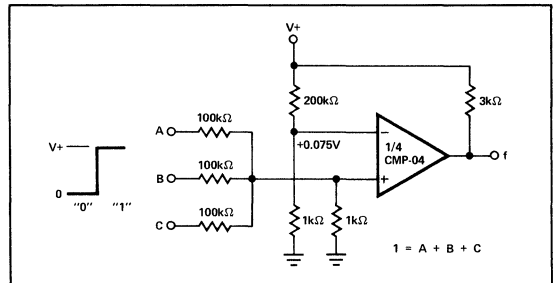
PULSE GENERATOR



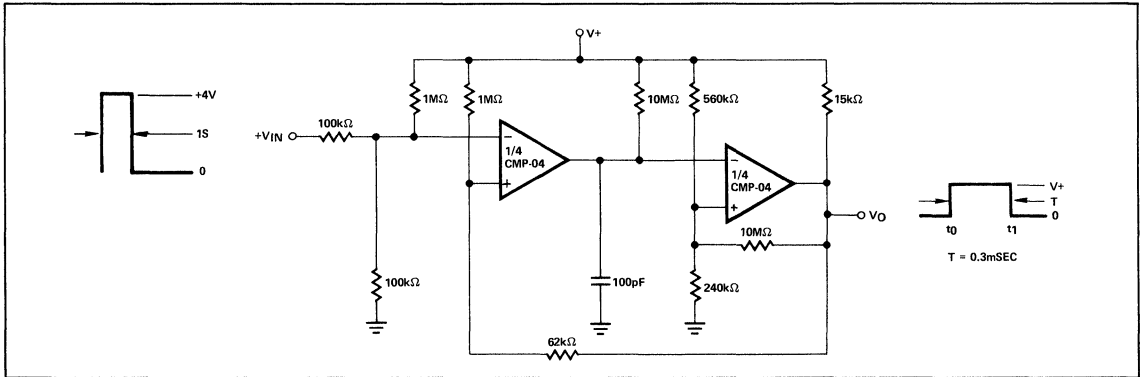
AND GATE



OR GATE



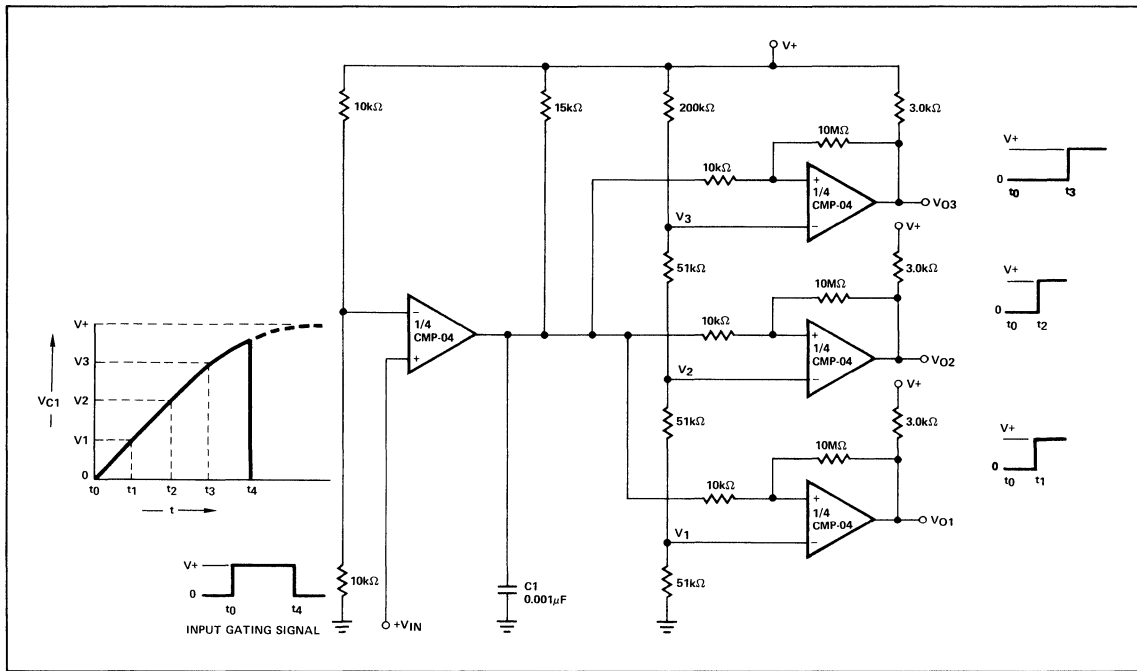
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT



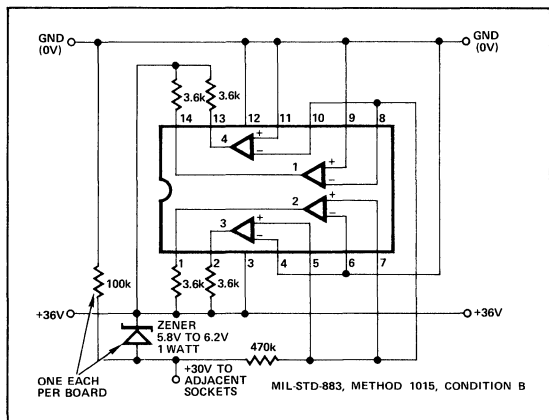


TYPICAL APPLICATIONS

TIME DELAY GENERATOR



BURN-IN CIRCUIT





CMP-05

HIGH-SPEED PRECISION COMPARATOR (WITH LATCH CIRCUIT)

Precision Monolithics Inc.

FEATURES

- Precision Input Stage
Input Offset Voltage **150 μ V**
Input Offset Current **15nA**
- Fast Response Time (5mV Overdrive) **38ns**
- High Voltage Gain **16,000V/V**
- Latch Function with TTL Compatible Input
- TTL Compatible Output
- Available in Hermetic Mini-DIP Package

ORDERING INFORMATION†

25° C V _{OS} (μ V)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC		PLASTIC	
	TO-99 8-PIN	DIP 8-PIN	DIP 8-PIN	
600	CMP05BJ*	CMP05BZ*	—	MIL
600	CMP05FJ	CMP05FZ	—	IND
1000	CMP05CJ*	CMP05CZ*	—	MIL
1000	CMP05GJ	CMP05GZ	—	IND
1000	—	—	CMP05GP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

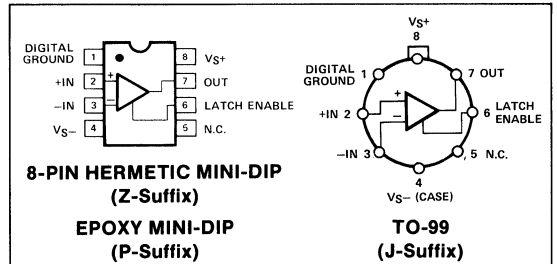
GENERAL DESCRIPTION

The CMP-05's very high speed and precision input specifications make it the ideal comparator in systems needing 12-bit

accuracy along with high speed. An exceptionally fast response time of 60nsec is possible with only 1/2 LSB overdrive (12-bit, 10-volt system).

The CMP-05 design makes it the ideal component in systems requiring high speed with excellent low-level analog signal resolution. High-speed 12-bit successive approximation A/D converters, zero crossing detectors and logic threshold detectors are typical system applications.

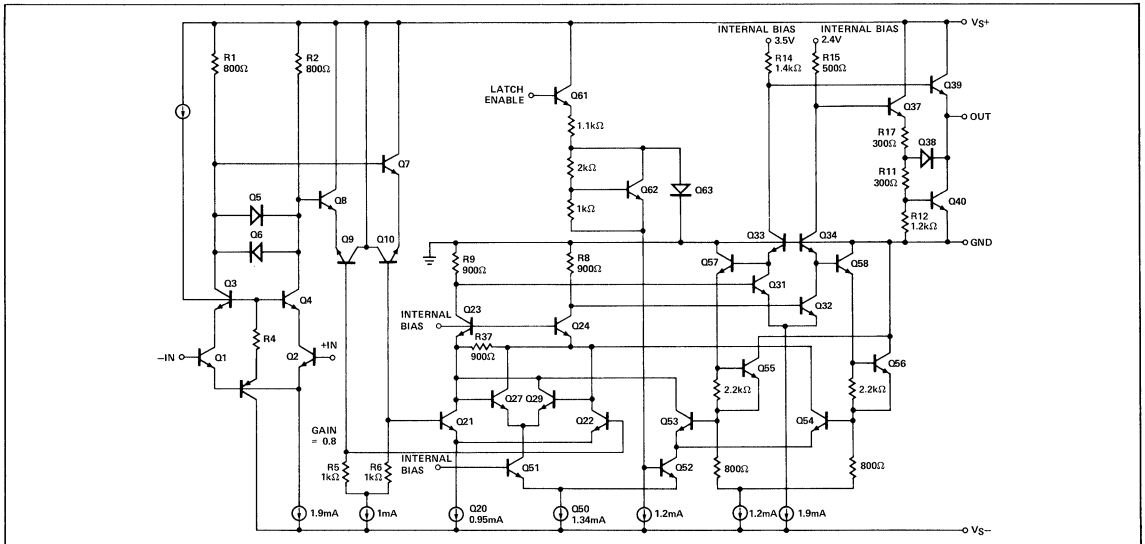
PIN CONNECTIONS



LOGIC TABLE

LATCH ENABLE	OUT
0 or NC	Comparing
1	Latched

SIMPLIFIED SCHEMATIC DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Positive Supply Voltage	+6V
Negative Supply Voltage	-18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±5V
Latch Enable Input Voltage	-0.5V to V+ Supply
Operating Temperature Range	
CMP-05B/C (J or Z Package)	
(Note 3)	-55°C to +125°C
CMP-05F/G (J or Z Package)	-25°C to +85°C
CMP-05G (P Package)	0°C to +70°C
DICE Junction Temperature (T _J)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
P-Suffix	-65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

Output Short-Circuit Duration — to ground Indefinite
 — to V+ = 5.0V ... 1 Minute

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
Epoxy Mini-DIP (P)	36°C	5.6mW/°C
Hermetic Mini-DIP (Z)	75°C	6.7mW/°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
- Latch is functional for -55°C ≤ T_A ≤ +85°C.

ELECTRICAL CHARACTERISTICS at V_{S+} = 5.0V, V_{S-} = -5.0V, T_A = 25°C and Latch Enable grounded, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05B/F			CMP-05C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S = 50Ω	—	150	600	—	400	1000	μV
Input Offset Current	I _{OS}		—	15	80	—	30	150	nA
Input Bias Current	I _B		—	0.6	1.2	—	0.8	1.8	μA
Voltage Gain	A _{VO}	(Note 1)	8	16	—	7	14	—	V/mV
Input Voltage Range	CMVR	(Note 1)	±3.0	±3.3	—	±3.0	±3.3	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±3.0V, (Note 1)	86	91	—	84	89	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±4.75V to V _S = ±5.25V	—	51	126	—	64	126	μV/V
		P Package	—	—	—	—	120	360	
		V _{S+} = 5V, V _{S-} = -5V to -15V	—	15	51	—	18	63	
		P Package	—	—	—	—	36	180	
Output High Voltage	V _{OH}	V _{IN} ≥ 10mV, I _O = 0μA	2.4	2.9	—	2.4	2.9	—	V
		V _{IN} ≥ 10mV, I _O = 320μA	2.4	2.9	—	—	—	—	
		V _{IN} ≥ 10mV, I _O = 200μA	—	—	—	2.4	2.9	—	
Saturation Voltage	V _{SAT}	V _{IN} ≤ -10mV, I _{SINK} = 0mA	—	0.13	0.40	—	0.13	0.40	V
		V _{IN} ≤ -10mV, I _{SINK} = 8mA	—	—	—	—	0.28	0.40	
		V _{IN} ≤ -10mV, I _{SINK} = 12.8mA	—	0.32	0.40	—	—	—	
Positive Supply Current	I _{S+}	V _O ≤ 2.4V, (Note 1)	—	7.5	11	—	8.0	12	mA
		V _O ≤ 0.4V	—	10	15	—	11	16	
Negative Supply Current	I _{S-}	V _O ≤ 0.4V	—	11	16	—	12	18	mA
Power Dissipation	P _d	V _O ≤ 0.4V	—	105	155	—	115	170	mW
Latch Input Voltage									
Logic 1	V _{LH}	Over Operating Temp. Range Latch Enabled, (Note 1)	2.0	—	—	2.0	—	—	V
Logic 0	V _{LL}	Over Operating Temp. Range Latch Disabled, (Note 1)	—	—	0.8	—	—	0.8	
Latch Input Current									
Logic 1	I _{LH}	V _{LH} = 3.0V, (Note 1)	—	10	45	—	10	45	μA
Logic 0	I _{LL}	V _{LL} = 0.8V, (Note 1)	—	6	25	—	6	25	
Input to Output High Response Time	t _{pd+}	V _{OD} = 1.2mV, (Note 2)	—	60	—	—	60	—	ns
		V _{OD} = 5.0mV, (Notes 2, 4)	—	41	55	—	41	55	
Input to Output Low Response Time	t _{pd-}	V _{OD} = 1.2mV, (Note 2)	—	60	—	—	60	—	ns
		V _{OD} = 5.0mV, (Notes 2, 4)	—	37	55	—	37	55	
Latch Disable Time	t _{LPD}	(Notes 3, 4)	—	50	65	—	50	65	ns

NOTES:

- Guaranteed by design.
- Times are for 100mV step inputs. See switching time waveforms.
- See switching time waveforms.
- Sample tested.





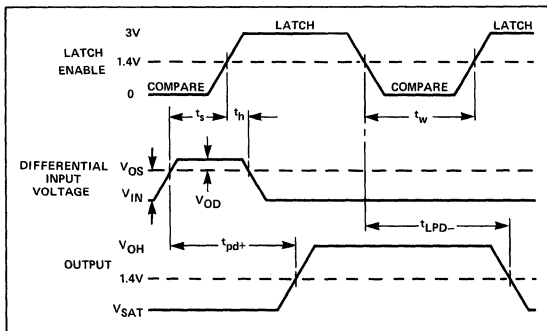
ELECTRICAL CHARACTERISTICS at $V_{S+} = 5.0V$, $V_{S-} = -5.0V$, and Latch Enable grounded. For CMP-05B/C, $-55^{\circ}C \leq T_A \leq 125^{\circ}C$. For CMP-05F/G, $-25^{\circ}C \leq T_A \leq 85^{\circ}C$ (J, Z Packages) and $0^{\circ}C \leq T_A \leq 70^{\circ}C$ (P Package), unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05B/F			CMP-05C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.3	1.5	—	0.55	2.0	mV
Input Offset Voltage Drift	TCV_{OS}		—	1.5	7.5	—	2.5	15	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}		—	40	250	—	70	400	nA
Input Bias Current	I_B		—	1.1	2.5	—	1.5	3.8	μA
Voltage Gain	A_{VO}	(Note 1)	6	11	—	5	10	—	V/mV
Input Voltage Range	CMVR	(Note 1)	± 2.9	± 3.2	—	± 2.9	± 3.2	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$, (Note 1)	83	90	—	80	88	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 4.75V \leq V_S \leq \pm 5.25V$ P Package	—	63	178	—	80	252	$\mu V/V$
Output High Voltage	V_{OH}	$V_{IN} \geq 10mV$, $I_O = 0\mu A$	2.4	—	—	2.4	—	—	V
		$V_{IN} \geq 10mV$, $I_O = 240\mu A$	2.4	—	—	—	—	—	
		$V_{IN} \geq 10mV$, $I_O = 160\mu A$	—	—	—	2.4	—	—	
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV$, $I_{SINK} = 0mA$	—	0.18	0.40	—	0.20	0.40	V
		$V_{IN} \leq -10mV$, $I_{SINK} = 9.6mA$	—	0.2	0.40	—	—	—	
		$V_{IN} \leq -10mV$, $I_{SINK} = 6.4mA$	—	—	—	—	0.30	0.40	
Positive Supply Current	I_{S+}	$V_O \leq 0.4V$	—	11	16	—	12	17	mA
Negative Supply Current	I_{S-}	$V_O \leq 0.4V$	—	12	17	—	13	19	mA
Power Dissipation	P_d	$V_O \leq 0.4V$	—	115	165	—	125	180	mW
Latch Input Current									
Logic 1	I_{LH}	$V_{LH} = 3V$, (Notes 1, 4)	—	18	90	—	18	90	μA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, (Notes 1, 4)	—	10	50	—	10	50	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Notes 1, 2)	—	125	—	—	125	—	ns
		$V_{OD} = 5.0mV$, (Notes 2, 5)	—	92	—	—	92	—	
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Notes 1, 2)	—	115	—	—	115	—	ns
		$V_{OD} = 5.0mV$, (Notes 2, 5)	—	88	—	—	88	—	
Latch Disable Time	t_{LPD+}	(Notes 2, 4, 5)	—	56	—	—	56	—	ns
	t_{LPD-}		—	30	—	—	30	—	

NOTES:

- Guaranteed by design.
- Times are for 100mV step inputs. See switching time waveforms.
- A high on the latch enable input will cause the latch to assume the state of the comparator and not follow subsequent inputs.
- Latch is functional for $-55^{\circ}C \leq T_A \leq +85^{\circ}C$.
- Sample tested.

SWITCHING TIME WAVEFORMS



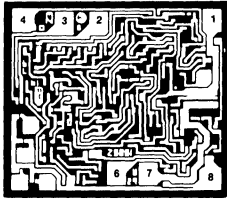
Minimum Input Timing Requirements*

Parameter	Minimum Limit	Units
t_S Setup Time	35	ns
t_h Hold Time	10	
t_w Latch Pulse Width	25	

* t_S , t_h , t_w are tested with $V_{IN} = 100mV$ and $V_{OD} = 5mV$.



DICE CHARACTERISTICS



DIE SIZE 0.051×0.045 inch, 2295 sq. mils
(1.295×1.143 mm, 1.481 sq. mm)

1. DIGITAL GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
6. LATCH ENABLE
7. OUTPUT
8. POSITIVE SUPPLY

For additional DICE information refer to
1984 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 5V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	1000	μV MAX
Input Offset Current	I_{OS}		150	nA MAX
Input Bias Current	I_B		1.8	μA MAX
Voltage Gain	A_{VO}	(Note 1)	7	V/mV MIN
Input Voltage Range	CMVR	(Note 1)	± 3.0	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$ (Note 1)	80	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 4.75 \leq V_S \leq \pm 5.25$ $V_{S+} = 5V, V_{S-} = -5V$ to $-15V$	178 63	$\mu V/V$ MAX
Positive Output Voltage	V_{OH}	$V_{IN} \geq 10mV, I_O = 0\mu A$	2.4	V MIN
Saturation Voltage	V_{SAT}	$V_{IN} \leq 10mV, I_O = 0\mu A$	0.4	V MAX
Positive Supply Current	I_+	$V_O \leq 0.4V$	16	mA MAX
Negative Supply Current	I_-	$V_O \leq 0.4V$	18	mA MAX
Negative Supply Current	I_-	$V_- = -15V, V_O \leq 0.4V$	20	mA MAX
Latch Input Voltage				
Logic 1	V_{LH}	Latch Enabled	2.0	V MIN
Logic 0	V_{LL}	Latch Disabled	0.8	V MAX
Latch Input Current				
Logic 1	I_{LH}	$V_{LH} = 3.0V$, (Notes 1, 4)	45	μA MAX
Logic 0	I_{LL}	$V_{LL} = 0.8V$, (Notes 1, 4)	25	μA MAX
Input to Output High Response Time	t_{pd+}	$V_{OD} = 5.0mV$, (Notes 1, 2)	60	ns MAX
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 5.0mV$, (Notes 1, 2)	60	ns MAX

NOTE:

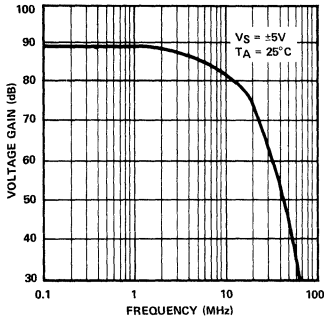
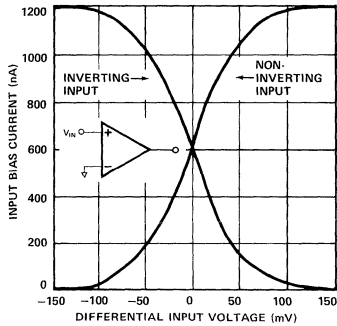
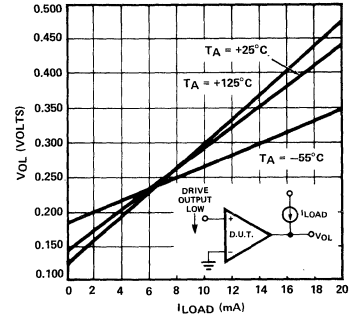
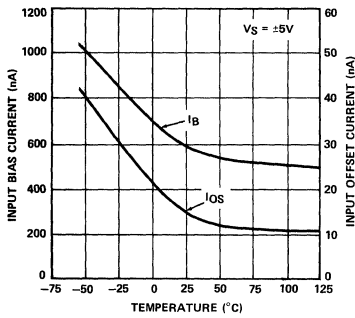
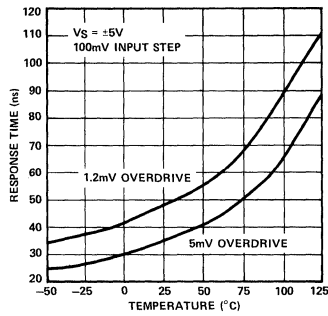
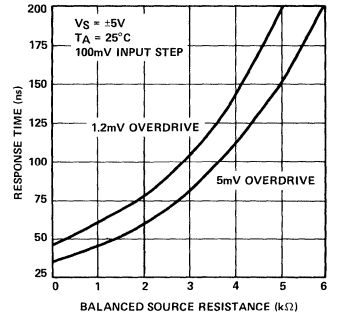
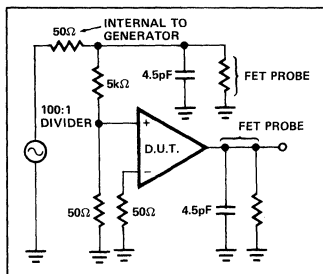
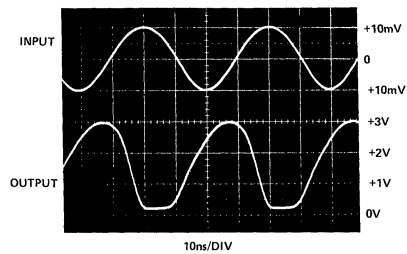
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 5V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05G TYPICAL	UNITS
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2)	41	ns
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2)	37	ns
Latch Disable Time	t_{LPD}	(Notes 3, 4)	50	ns

NOTES:

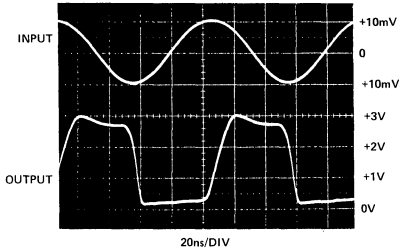
1. Guaranteed by design.
2. Times are for 100mV step inputs.
3. See switching time waveforms.
4. Latch is functional for $-55^\circ C \leq T_A \leq 85^\circ C$.

TYPICAL PERFORMANCE CHARACTERISTICS
VOLTAGE GAIN vs FREQUENCY

INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

V_{SAT} vs LOAD CURRENT

INPUT CURRENTS vs TEMPERATURE

RESPONSE TIME vs TEMPERATURE

RESPONSE TIME vs BALANCED SOURCE RESISTANCE

RESPONSE PHOTOGRAPH TEST SET-UP

RESPONSE TO 25MHz SINE WAVE


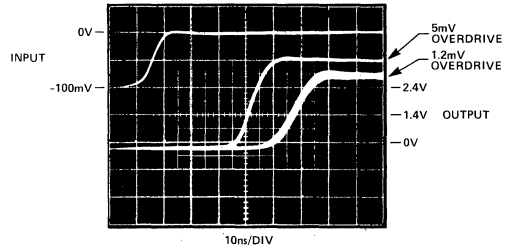


TYPICAL PERFORMANCE CHARACTERISTICS

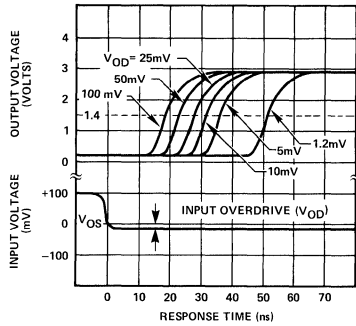
RESPONSE TO 10MHz SINE WAVE



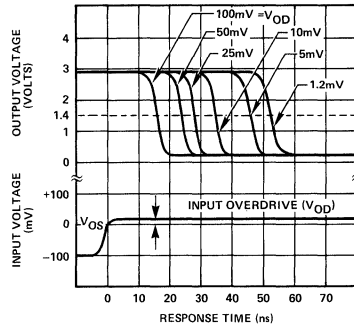
RESPONSE TIME TO 5mV AND 1.2mV (= 1/2 LSB) OVERDRIVES



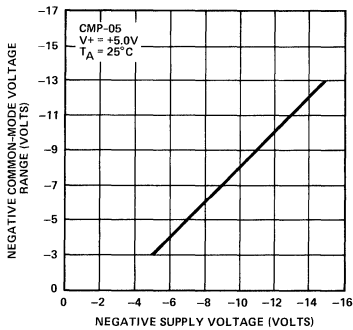
t_{pd+} RESPONSE TIME



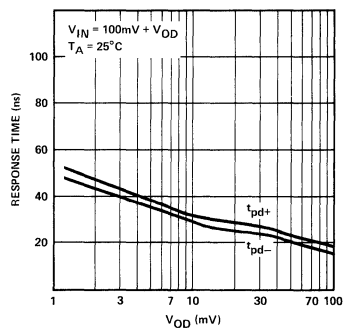
t_{pd-} RESPONSE TIME



CMP-05 NEGATIVE COMMON-MODE INPUT RANGE vs NEGATIVE SUPPLY



RESPONSE TIME vs OVERDRIVE VOLTAGE





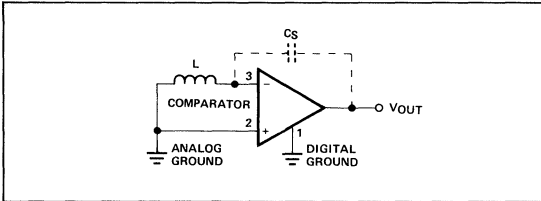
APPLICATION INFORMATION

The CMP-05 is a very accurate device providing fast response time even with small—Microvolt level—overdrives. To achieve this performance requires high gain at high frequencies. As shown in the voltage gain versus frequency curve, the gain—bandwidth product of the CMP-05 is 1.5×10^{11} Hz. It maintains its full gain to approximately 8MHz and rolls off at a very fast rate beyond that frequency due to the fact that five poles occur in the 30 to 60MHz range. At 30MHz the gain of the comparator is still 2000. Therefore, in the transition region small values of source lead inductance and stray feedback capacitance can cause an oscillatory condition.

For example (in the figure below) with $L = 0.1\mu\text{H}$, $C_S = 0.15\text{pF}$, the closed-loop gain of the circuit at 30MHz is:

$$A_V = \frac{1}{LC_S\omega^2} = \frac{1}{10^{-7} \times 0.15 \times 10^{-12} \times (2\pi \times 30 \times 10^6)^2} = 1880$$

POTENTIAL FEEDBACK SOURCES



With the open-loop gain at 2000 oscillation will occur since the phase shift exceeds 180° . To minimize these problems power supplies should be decoupled, lead lengths should be kept as short as possible, and a ground plane should be used to reduce the stray feedback capacitance. In addition, a ground plane substantially diminishes the possibility of the output current spike coupling back to the inputs through the ground lead. Keeping a separate digital ground (pin 1) and analog ground (to which the inputs are referenced) also reduces the magnitude of the problem.

Fortunately, in high-speed circuitry the comparator inputs will be driven at a fast rate, in which case no transition region oscillations will occur. As the minimum slew rate versus source resistance curve indicates, if the input is driven at a rate exceeding $6\text{mV}/\mu\text{sec}$, no oscillations will occur with source resistors of less than $1\text{k}\Omega$. Examples of "clean" transitions can be observed in the photographs of the response time with 5mV and 1.2mV overdrives, and the response to the 10 and 25MHz input signals.

In order to not degrade its speed the CMP-05's inputs are not internally clamped. If large differential voltages are present it is recommended that the inputs be clamped with high speed, low capacitance diodes such as the H.P. 5082-2835, which is a Schottky Diode.

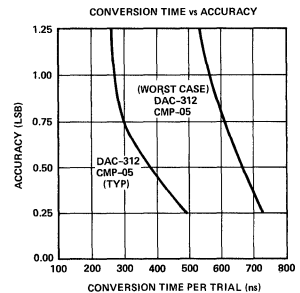
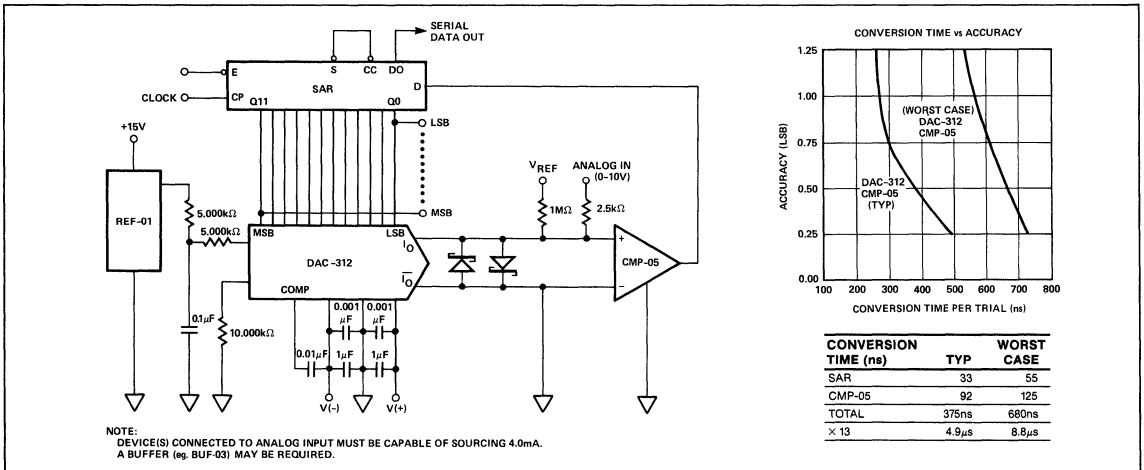
As in all high-speed devices, it is to the user's advantage to keep the source impedances low and matched.

LATCH

The CMP-05 has a latch feature which functions over -55°C to $+85^\circ\text{C}$. When the latch is enabled, the output stays in its existing logic state regardless of the input signal. The input timing requirements of the latch are presented in the Switching Time Waveforms. The latch opens up a broader applications area at no sacrifice in total system speed. Effectively, the latch allows high speed sampling of comparison decisions. This is important in automatic test equipment limit comparators, in measuring pods used in logic analyzers and other similar synchronous measurement circuitry needing fast clocking frequencies. The latch pulse width t_w allows sampling of input signals to take place in 25nsec.

The latch prevents self oscillation (due to positive feedback) from taking place when slowly-moving high-source-impedance signals pass thru the linear amplification region of the comparator. This is successfully accomplished by rapidly strobing the comparator near its minimum t_w time which prevents self oscillation from making a complete cycle since t_w is shorter than the total response time t_{pd} through the comparator.

12-BIT FAST A/D CONVERTER



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375ns	680ns
× 13	4.9μs	8.8μs



CMP-07

VERY HIGH-SPEED COMPARATOR
(WITH LATCH CIRCUIT)

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- **Input-to-Output Propagation**
Delay at 5mV Overdrive 6.5ns Max
- **Latch-to-Output Propagation**
Delay at 5mV Overdrive 5.5ns Max
- **Latch Pulse Width** 2ns Min
- **Low Power Dissipation** 200mW Max
- **ECL Compatible Complementary Outputs and Latch Input**
- **50 Ohm Line Driving Capability**
- **Pin Compatible with Am685**

ORDERING INFORMATION†

PACKAGE		OPERATING TEMPERATURE RANGE
TO-100	DIP	
CMP07BK*	CMP07BQ*	MIL
CMP07FK	CMP07FQ	IND

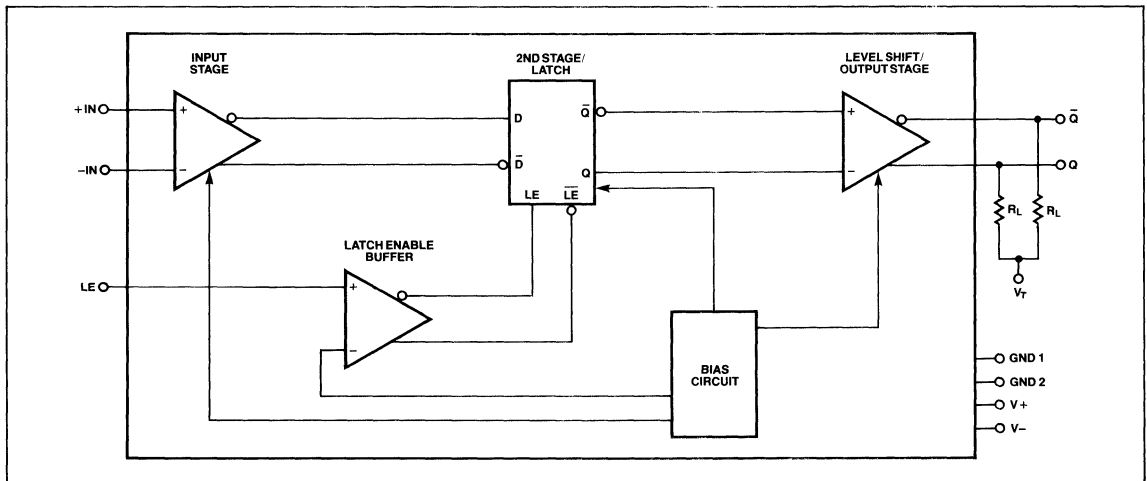
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The CMP-07 is a very high-speed comparator with complementary ECL output logic compatibility. It offers the same propagation delay specifications as the Am685, at 66% of the Am685's power consumption, reducing heat generation and improving reliability.

BLOCK DIAGRAM



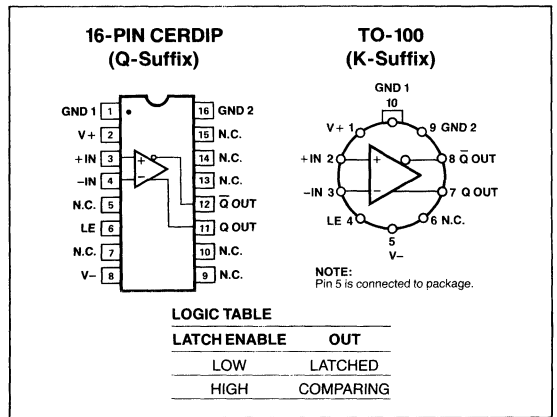
This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

Latch timing is also faster than the Am685, resulting in less uncertainty when used as a sampling comparator.

The CMP-07 is specified for operation with a standard -5.2V ECL power supply and a +6V supply. The circuit operates with a +5V supply with some reduction in input voltage range. The output stage directly drives 50Ω transmission lines.

The CMP-07 electrical characteristics are ideally suited for use in data conversion systems, logic analyzer probes, automatic test equipment, pulse detectors, and simple flash converters.

PIN CONNECTIONS



VOLTAGE COMPARATORS

**ABSOLUTE MAXIMUM RATINGS**

Positive Supply Voltage	+7V
Negative Supply Voltage	-7V
Power Dissipation	500mW
Input Voltage	±4V
Differential Input Voltage	±6V
Latch Enable Input Voltage	V- Supply to +1V

Operating Temperature Range

CMP-07F	-30°C to +85°C
CMP-07B	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Minimum Operating Voltage (V+ to V-)	+9.7V

ELECTRICAL CHARACTERISTICS at V+ = 6V, V- = -5.2V, VT = -2V, RL = 50Ω; -55°C ≤ TA ≤ +125°C for CMP-07B, -30°C ≤ TA ≤ +85°C for CMP-07F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS (Notes 1, 2)	CMP-07F		CMP-07B		UNITS
			MIN	MAX	MIN	MAX	
Input Offset Voltage	VOS	RS = 100Ω, TA = 25°C RS = 100Ω, TMIN < TA < TMAX	-2.0	+2.0	-2.0	+2.0	mV
Average Temperature Coefficient of Input Offset Voltage	TCVOS	RS = 100Ω	-10	+10	-10	+10	μV/°C
Input Offset Current	IOS	TA = 25°C TMIN < TA < TMAX	-1.0	+1.0	-1.0	+1.0	μA
Input Bias Current	IB	TA = 25°C TMIN < TA < TMAX	—	10	—	10	μA
Input Voltage Range	VCMR	TMIN < TA < TMAX	-2.7	+3.4	-2.7	+3.4	V
Common-Mode Rejection Ratio	CMRR	RS = 100Ω	80	—	80	—	dB
Power Supply Rejection Ratio	PSRR	RS = 100Ω, ΔVS = ±5%	70	—	70	—	dB
Output High Voltage	VOH	TA = 25°C TA = TMIN TA = TMAX	-0.960	-0.810	-0.960	-0.810	V
Output Low Voltage	VOL	TA = 25°C TA = TMIN TA = TMAX	-1.850	-1.650	-1.850	-1.650	V
Positive Supply Current	I+	TMIN < TA < TMAX	—	12	—	12	mA
Negative Supply Current	I-	TMIN < TA < TMAX	—	23	—	23	mA
Power Dissipation	Pd	TMIN < TA < TMAX	—	200	—	200	mW

SWITCHING CHARACTERISTICS

(Note 3)

Propagation Delay	t _{pd+} , t _{pd-}	TMIN < TA < 25°C TA = TMAX	4.5	6.5	4.5	6.5	ns
Latch Enable Propagation Delay	t _{pd+} (E), t _{pd-} (E)	TMIN < TA < 25°C TA = TMAX	4.0	5.5	4.0	5.5	ns
Setup Time	ts	TMIN < TA < 25°C TA = TMAX	—	4.0	—	4.0	ns
Hold Time	th	TMIN < TA < TMAX	—	1.0	—	1.0	ns
Latch Enable Pulse Width	t _{pw} (E)	TMIN < TA < 25°C TA = TMAX	—	2.0	—	2.0	ns

NOTES:

- The specifications for VOS, IOS, IB, CMRR, PSRR, t_{pd+}, and t_{pd-} apply over the full VCMR range and for ±5% supply voltages.
- The CMP-07 is designed to meet all the above specifications after thermal equilibrium has been established with a transverse airflow of 500 LFPM or more.
- All speed/switching characteristics are for a 100mV step with 5mV overdrive beyond the input switching threshold.

DEFINITION OF SWITCHING TERMS

INPUT TO OUTPUT HIGH DELAY (t_{pd+}) — The propagation delay measured from the time the input signal crosses the input switching threshold, to the 50% point of the output LOW to HIGH transition.

INPUT TO OUTPUT LOW DELAY (t_{pd-}) — The propagation delay measured from the time the input signal crosses the input switching threshold, to the 50% point of the output HIGH to LOW transition.

LATCH ENABLE TO OUTPUT HIGH DELAY ($t_{pd+(E)}$) — The propagation delay measured from the 50% point of the Latch Enable LOW to HIGH transition, to the 50% point of the output LOW to HIGH transition.

LATCH ENABLE TO OUTPUT LOW DELAY ($t_{pd-(E)}$) — The propagation delay measured from the 50% point of the Latch Enable LOW to HIGH transition, to the 50% point of the output HIGH to LOW transition.

MINIMUM SETUP TIME (t_s) — The minimum time before the Latch Enable falling-edge 50% point that an input signal change must be present to be acquired and held at the outputs.

MINIMUM HOLD TIME (t_h) — The minimum time after the Latch Enable falling-edge 50% point that the input signal must remain unchanged to be acquired and held at the outputs.

MINIMUM LATCH-ENABLE PULSE WIDTH ($t_{pw(E)}$) — The minimum time that the Latch Enable input must remain HIGH to acquire and hold an input signal change. Measured between the 50% point of the Latch Enable rising-edge and the 50% point of the Latch Enable falling-edge.

APPLICATIONS INFORMATION

As with any high speed circuit, proper layout, impedance matching, ground planes, and bypassing must be used. A parallel combination of a $1\mu\text{F}$ tantalum and a $0.01\mu\text{F}$ ceramic capacitor, located close to the device's power supply pins, provides good supply bypassing. If latch operation is not required, the Latch Enable (LE) input should be tied to digital ground.

The GND1 pin is internally connected to the collectors of the emitter-follower output transistors (Q and \bar{Q}). GND2 is internally connected to the rest of the comparator circuitry.

Grounding of the CMP-07 requires good R.F. layout practice. Use of a double-sided P.C. board is recommended; one side of the board should be a solid ground plane, with GND1 and GND2 connected directly to the ground plane. The CMP-07 should be soldered in place (avoid using a socket). All N.C. pins should be tied to ground to increase pin-to-pin isolation.

TIMING DIAGRAM

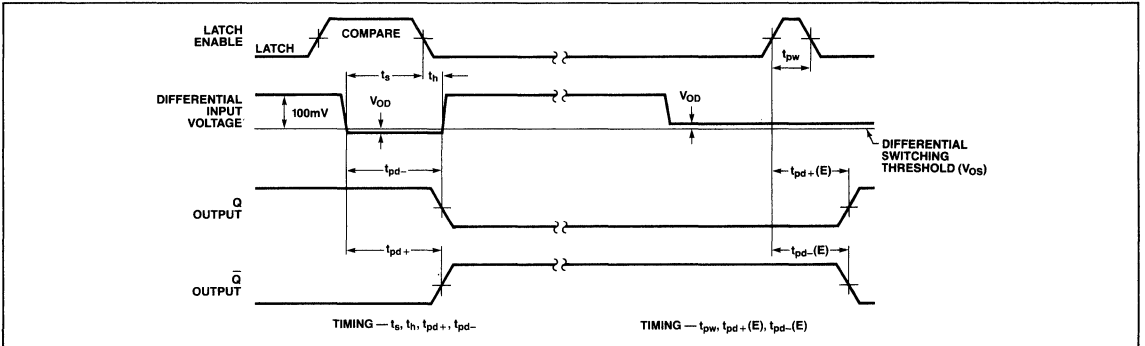


FIGURE 1: 30ns One Shot

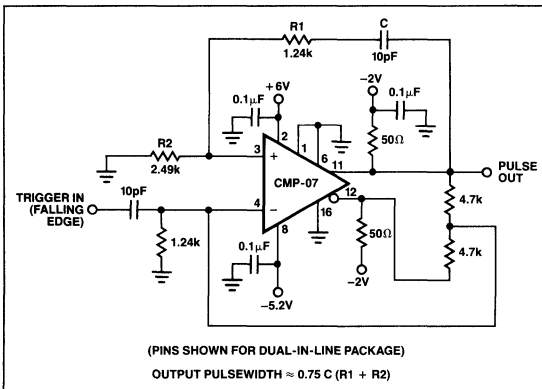
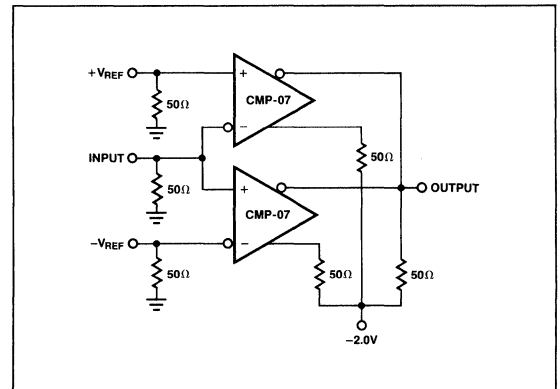


FIGURE 2: High-Speed Window Detector





CMP-404

QUAD LOW-POWER
PRECISION COMPARATOR

Precision Monolithics Inc.

FEATURES

- Very Low Power Consumption 1.5mW Max
- Low Input Offset Voltage 1mV Max
- Very Low Drift 3 μ V/ $^{\circ}$ C Typ
- High Output-Drive Current 25mA Typ
- Single or Dual Supply Operation
- Ideal for CMOS Logic Interface
- LM139 Pinout

ORDERING INFORMATION†

25 $^{\circ}$ C V _{OS} (mV)	HERMETIC DIP PACKAGE	OPERATING TEMPERATURE RANGE
1	CMP404AY*	MIL
2	CMP404BY*	MIL
1	CMP404EY	IND
2	CMP404FY	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

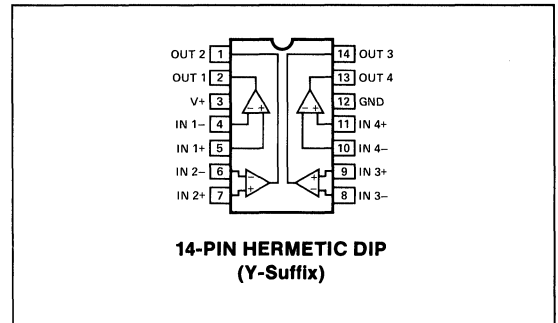
GENERAL DESCRIPTION

Four precision-input comparators provide excellent speed with low power consumption through use of a novel Schottky-clamped design. These open-collector output comparators only consume 365 microwatts each, yet they make accurate 5mV decisions in only four microseconds. In addition, they can drive load currents of 25mA. This output stage is ideal for driving relays, lamps, and LEDs.

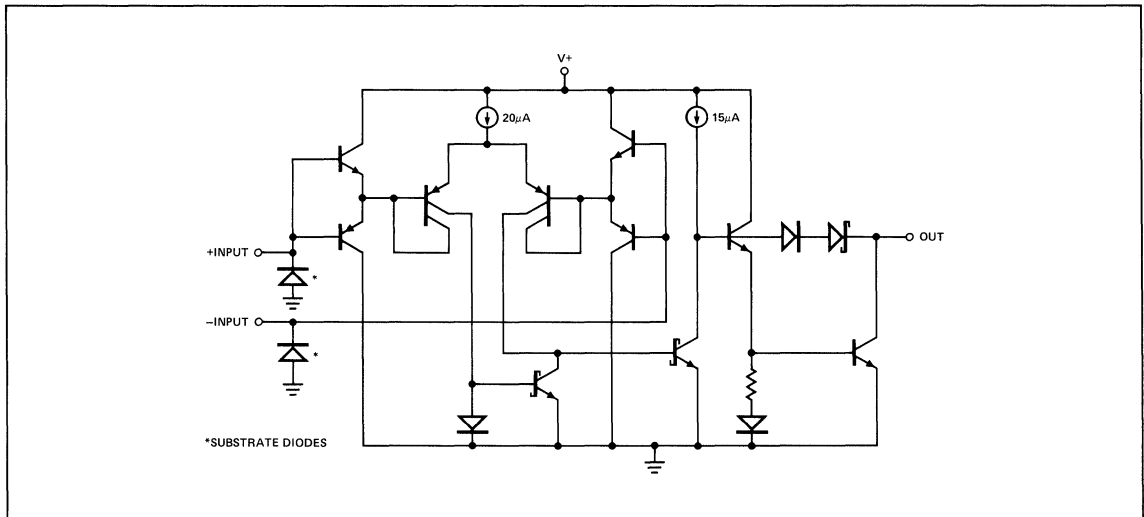
The low input-offset-voltage makes the CMP-404 an ideal companion to CMOS logic when the stability and accuracy of a bipolar technology is needed along with low power consumption. The open-collector outputs with pull-up resistors provide CMOS interface with excellent noise immunity. Improved isolation between comparators was achieved by use of an independent bias circuit for each comparator. This is especially important when one comparator is detecting low-level signals while an adjacent comparator is being driven by a high-level signal. In single-supply operation, the inputs can operate at ground. The CMP-404 can operate from 5 to 30 volts single supply or ± 2.5 to ± 15 volts dual supply.

Window comparators, limit comparators, multivibrators, one shots, voltage-controlled oscillators, and set-point detectors are common applications.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/4 OF CMP-404)



**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	36V or $\pm 18V$
Input Voltage	$-0.3V$ to $V+$
Output Voltage	$-0.3V$ to $36V$
Power Dissipation	500mW
Derate Above 100°C by	10mW/°C
Thermal Resistance (θ_{JA})	100°C/W
Operating Temperature Range	
CMP-404EY/FY	$-25^{\circ}C$ to $+85^{\circ}C$
CMP-404AY/BY	$-55^{\circ}C$ to $+125^{\circ}C$
DICE Junction Temperature (T_J)	$-65^{\circ}C$ to $+150^{\circ}C$

Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Input Current (Note 2)	20mA
Output Short-Circuit to $V+$ (Note 3)	50mA
Lead Temperature (Soldering, 60 sec)	300°C

NOTE:

1. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
2. Limit for input current that flows when input voltage signals exceed $V+$ or GND forward biasing internal junctions.
3. Short circuits to $V+$ can cause excessive heating and eventual destruction. The maximum output current is 50mA.

ELECTRICAL CHARACTERISTICS at $V+ = 5V$, $R_L = 5.1k\Omega$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ for CMP-404AY/BY; $-25^{\circ}C \leq T_A \leq 85^{\circ}C$ for CMP-404 EY/FY, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-404A/E			CMP-404B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$, $T_A = 25^{\circ}C$	—	—	1	—	—	2	mV
		$R_S = 50\Omega$, Full Temp	—	—	2	—	—	3	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	3	—	—	3	—	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25^{\circ}C$	—	3	10	—	3	25	nA
		$I_{IN(+)} - I_{IN(-)}$, Full Temp	—	—	50	—	—	100	nA
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25^{\circ}C$	—	10	50	—	10	100	nA
		$I_{IN(+)}$ or $I_{IN(-)}$, Full Temp	—	—	100	—	—	200	nA
Voltage Gain	A_V	$R_L = 15k\Omega$	50	400	—	50	400	—	V/mV
Small-Signal Response Time	t_r	$V_{OD} = 5mV$, $V_{STEP} = 100mV$ $R_L = 5.1k\Omega$, $T_A = 25^{\circ}C$ (Note 4)	—	3.5	5	—	3.5	5	μs
Large-Signal Response Time	t_r	$V_{IN} =$ TTL Logic Swing $V_{REF} = 1.4V$, $R_L = 5.1k\Omega$	—	0.8	—	—	0.8	—	μs
Input Voltage Range	CMVR	$T_A = 25^{\circ}C$	0	—	$V+ - 1.5$	0	—	$V+ - 1.5$	V
		$T_A =$ Full Temp	0	—	$V+ - 2$	0	—	$V+ - 2$	V
Common-Mode Rejection Ratio	CMRR	$R_L = 15k\Omega$, (Note 6)	75	85	—	75	85	—	dB
Saturation Voltage	V_{OL}	$T_A = 25^{\circ}C$, (Note 2)	—	0.32	0.4	—	0.32	0.4	V
		Full Temp, (Note 2)	—	—	0.5	—	—	0.5	V
Output Sink Current	I_{SINK}	$V_{IN(-)} = 1V$ $V_{IN(+)} = 0V$, $V_O = 2V$, (Note 5)	10	25	—	10	25	—	mA
Output Leakage Current	I_{LEAK}	$T_A = 25^{\circ}C$, (Note 3)	—	0.01	0.1	—	0.01	0.1	μA
		Full Temp, (Note 3)	—	—	0.4	—	—	0.4	μA
Power Supply Rejection Ratio	PSRR	$V+ = 5V$ to $30V$, $R_L = 15k\Omega$	75	100	—	65	100	—	dB
Supply Current	$I+$	$R_L = \infty$	—	220	300	—	220	350	μA

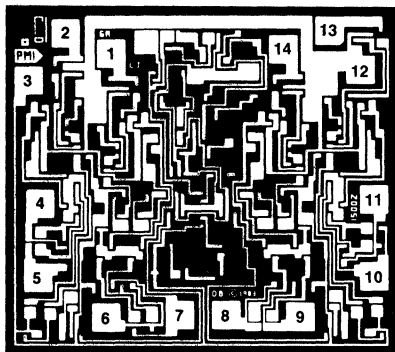
NOTES:

1. Typical values are reported for $T_A = 25^{\circ}C$.
2. $I_{SINK} = 1mA$, $V_{IN(-)} = 1V$, $V_{IN(+)} = 0V$
3. $V_{IN(-)} = 0V$, $V_{IN(+)} = 1V$, $V_O = 30V$
4. Guaranteed by design. See response-time test circuit.
5. Output Sink Current should be limited to 50mA by external resistance.
6. Applies over the CMVR range.

 8
 VOLTAGE COMPARATORS



DICE CHARACTERISTICS



DIE SIZE 0.068 × 0.076 inch, 5168 sq. mils
(1.727 × 1.93 mm, 3.33 sq. mm)

- | | |
|---------------------------|----------------------------|
| 1. OUTPUT (2) | 8. INVERTING INPUT (3) |
| 2. OUTPUT (1) | 9. NONINVERTING INPUT (3) |
| 3. POSITIVE SUPPLY | 10. INVERTING INPUT (4) |
| 4. INVERTING INPUT (1) | 11. NONINVERTING INPUT (4) |
| 5. NONINVERTING INPUT (1) | 12. GROUND |
| 6. INVERTING INPUT (2) | 13. OUTPUT (4) |
| 7. NONINVERTING INPUT (2) | 14. OUTPUT (3) |

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 5V$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-404G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$	25	nA MAX
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$	100	nA MAX
Voltage Gain	A_V	$R_L = 15k\Omega$	50	V/mV MIN
Input Voltage Range	CMVR		$V_+ - 1.5$	V MAX
Common-Mode Rejection Ratio	CMRR	$R_L = 15k\Omega$	75	dB MIN
Power Supply Rejection Ratio	PSRR	$V_+ = 5V$ to $30V$, $R_L = 15k\Omega$	65	dB MIN
Saturation Voltage	V_{OL}	$I_{SINK} = 1mA$	0.4	V MAX
Output Sink Current	I_{SINK}	$V_{IN(-)} = 1V$ $V_{IN(+)} = 0V$, $V_O = 2V$	10	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN(-)} = 0V$ $V_{IN(+)} = 1V$, $V_O = 30V$	0.1	μA MAX
Supply Current	I_+	$R_L = \infty$	300	μA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

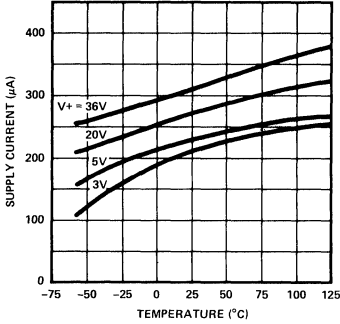
TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = 5V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-404G TYPICAL	UNITS
Large-Signal Response Time	t_r	$V_{IN} =$ TTL Logic Swing $V_{REF} = 1.4V$, $R_L = 5.1k\Omega$	0.8	μs
Small-Signal Response Time	t_r	$V_{OD} = 5mV$, $V_{STEP} = 100mV$ $R_L = 5.1k\Omega$	3.5	μs

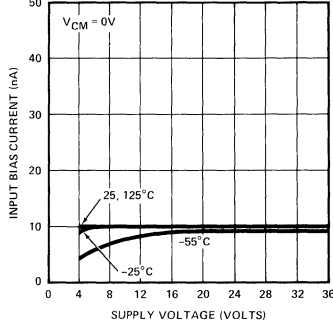


TYPICAL PERFORMANCE CHARACTERISTICS

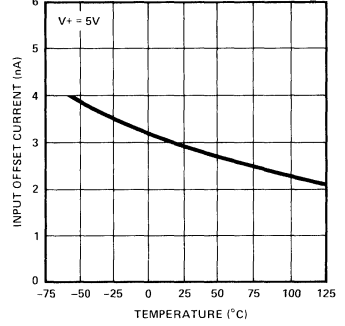
SUPPLY CURRENT vs TEMPERATURE



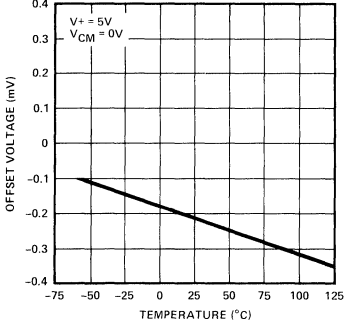
INPUT BIAS CURRENT vs SUPPLY VOLTAGE



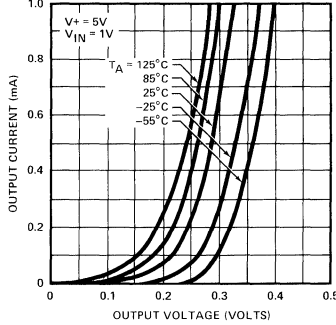
INPUT OFFSET CURRENT vs TEMPERATURE



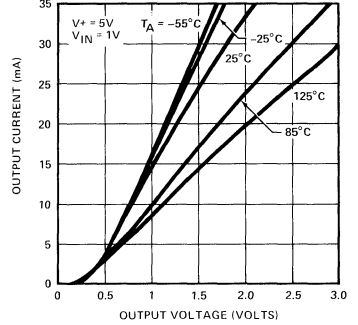
OFFSET VOLTAGE vs TEMPERATURE



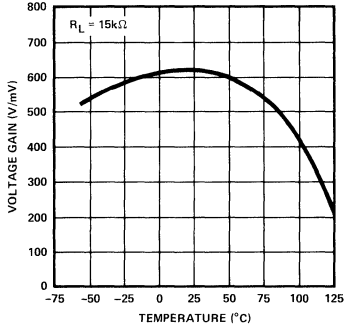
OUTPUT CURRENT vs OUTPUT VOLTAGE



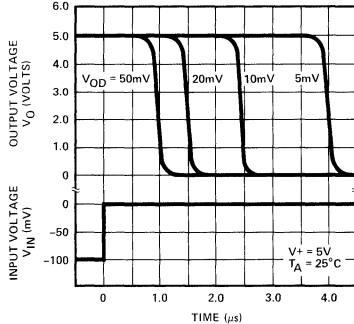
OUTPUT CURRENT vs OUTPUT VOLTAGE



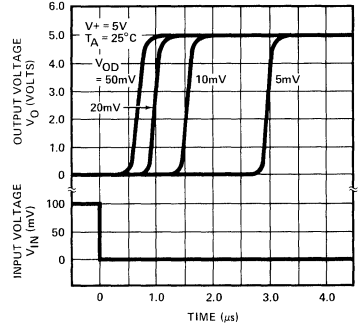
OPEN-LOOP GAIN vs TEMPERATURE



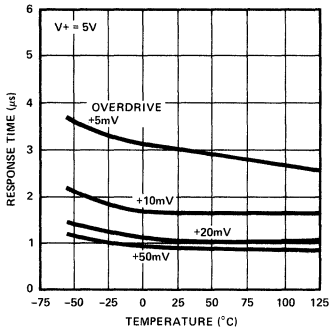
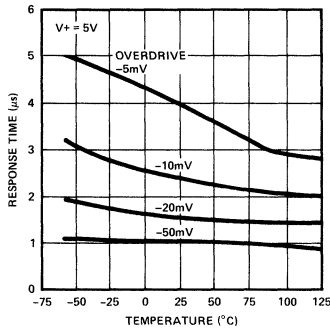
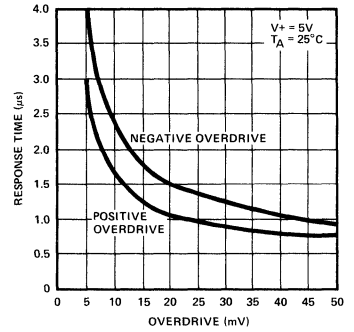
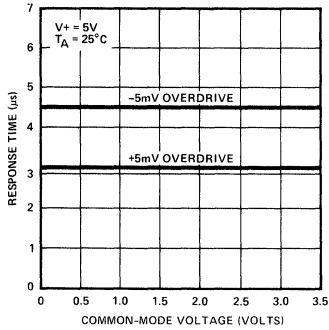
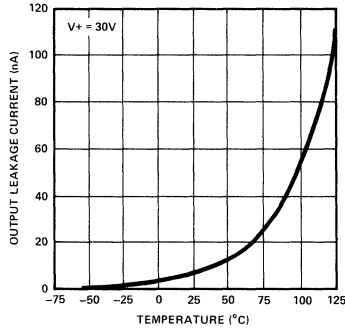
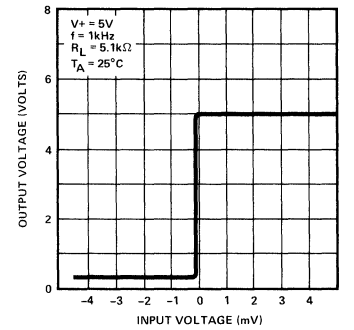
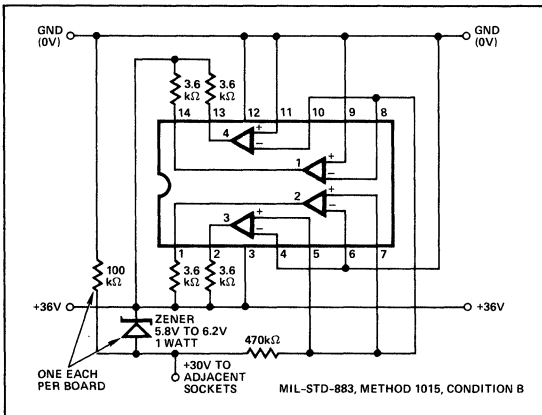
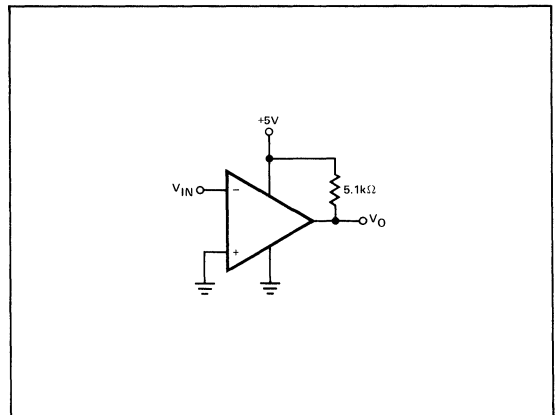
NEGATIVE RESPONSE TIME vs OVERDRIVE



POSITIVE RESPONSE TIME vs OVERDRIVE



VOLTAGE COMPARATORS

TYPICAL PERFORMANCE CHARACTERISTICS
POSITIVE RESPONSE TIME vs TEMPERATURE

NEGATIVE RESPONSE TIME vs TEMPERATURE

RESPONSE TIME vs OVERDRIVE

RESPONSE TIME vs COMMON-MODE VOLTAGE

OUTPUT LEAKAGE vs TEMPERATURE

INPUT-OUTPUT TRANSFER CHARACTERISTIC

BURN-IN CIRCUIT

RESPONSE-TIME TEST CIRCUIT




APPLICATIONS INFORMATION

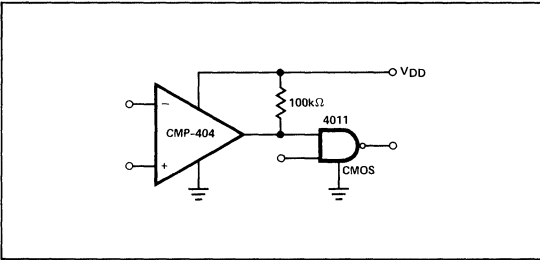
The use of non-saturated switching within the CMP-404 design results in optimized response time. The high-gain output stage drives large load currents with a minimum saturation voltage (V_{OL}). This provides excellent noise margin when driving LSTTL loads. An independent bias network for each comparator inside the CMP-404 minimizes crosstalk between comparators. This proves especially important when one comparator is detecting low-level signals while adjacent comparators are making transitions.

Input signals should be confined to between the power supply rails. Input signals exceeding either $V+$ or GND will forward-bias internal junctions. Input current during forward bias should be limited to 20mA.

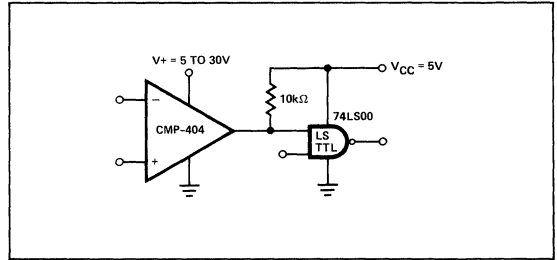
Exceeding the positive end of the common-mode input-voltage-range will cause the comparator output transistor to turn on, thus resulting in a continuous logic-low output state.

The open-collector output stage can be easily wire-OR-ed to make window comparators. The open-collector output also simplifies shifting of logic levels between different supply levels. The output transistors easily drive high-current loads, which is especially useful in fault-detector circuits for driving high-level enunciators (piezo horns, relays, lamps, or red LEDs).

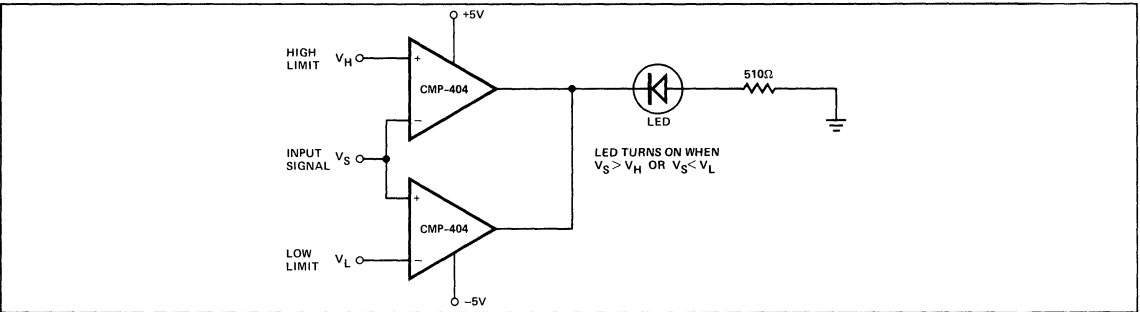
CMOS INTERFACING



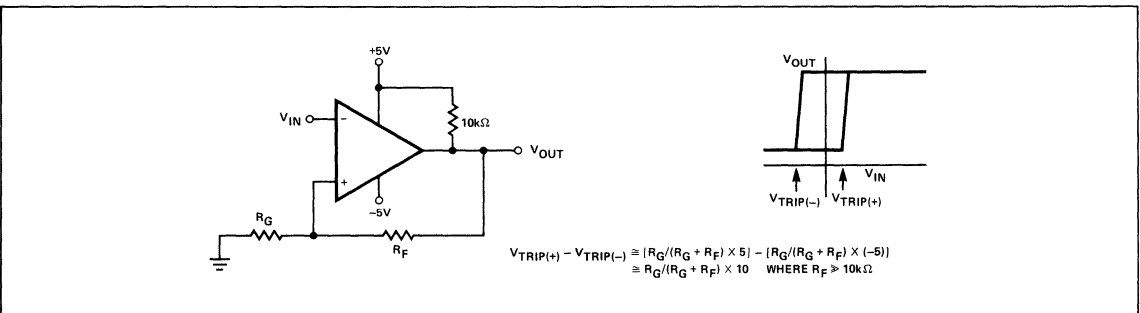
TTL INTERFACING



LIMIT DETECTOR (WINDOW COMPARATOR)

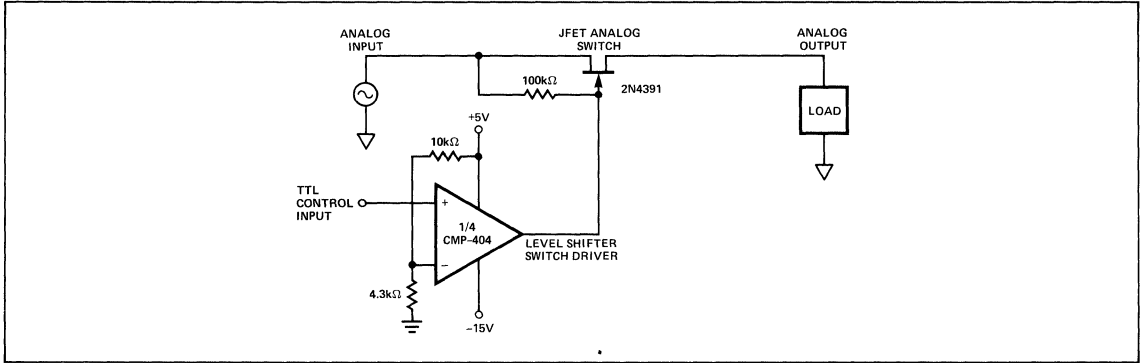


SETTING UP HYSTERESIS

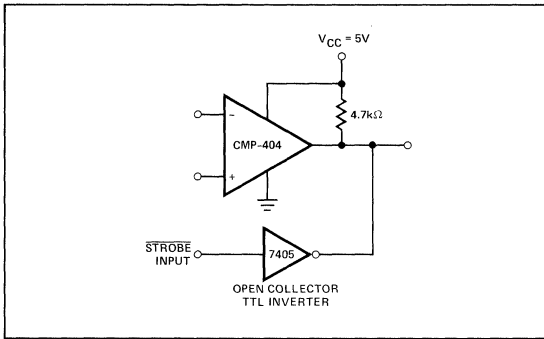


VOLTAGE COMPARATORS

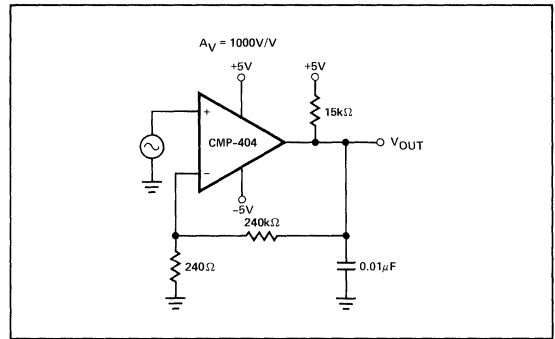
TTL-COMPATIBLE ANALOG SWITCH



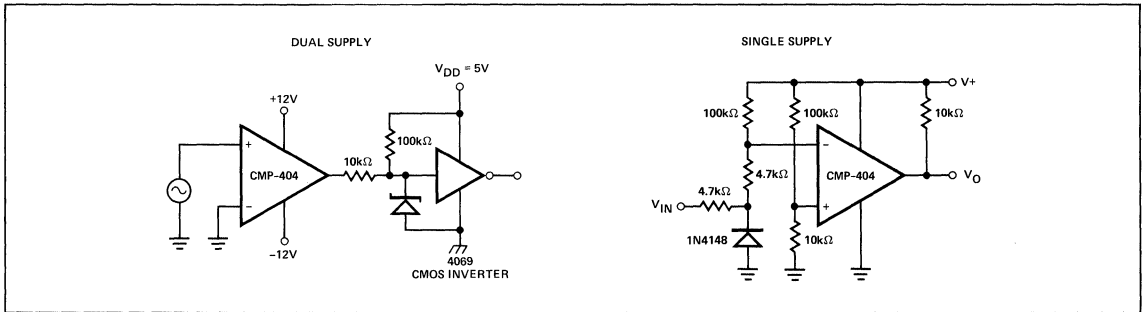
OUTPUT STROBING



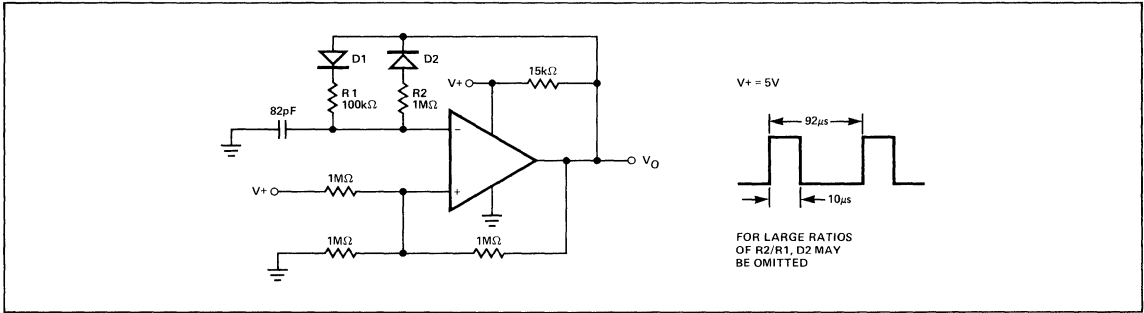
LOW-FREQUENCY OPERATIONAL AMPLIFIER



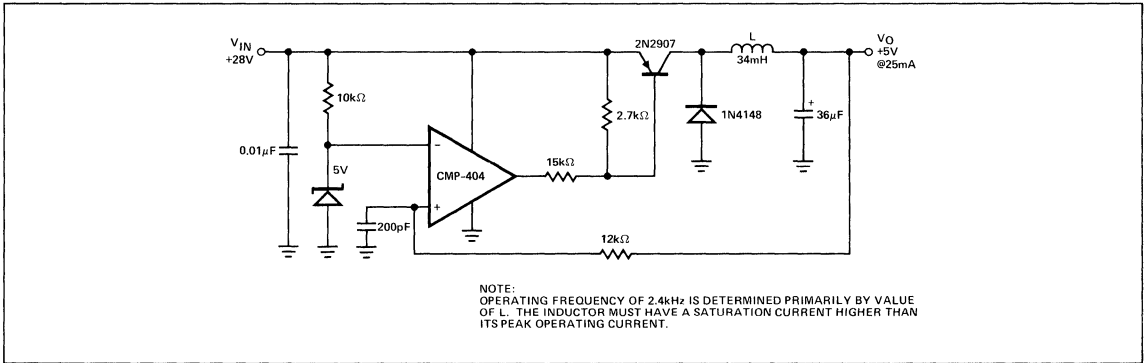
ZERO-CROSSING DETECTOR CIRCUITS



PULSE GENERATOR



REGULATED DC-TO-DC CONVERTER





PM-111/PM-211

PRECISION VOLTAGE COMPARATORS

Precision Monolithics Inc.

FEATURES

- High Output Drive 50mA
- Low Input Bias Current 50nA Max
- Low Offset Voltage 3mV Max
- Differential Input Voltage Range $\pm 30V$
- Logic Outputs Compatible with Bipolar and CMOS
- Fully-Specified at All Temperatures

ORDERING INFORMATION†

V _{OS} MAX (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 14-PIN	HERMETIC DIP 8-PIN	LCC 20-PIN	
3.0	PM111J*	PM111Y*	PM111Z*	PM111RC/883	MIL
3.0	PM211J	PM211Y	PM211Z	—	IND

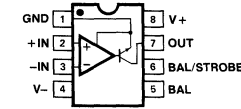
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1984 Data Book, Section 2.

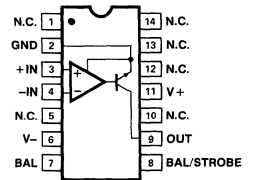
GENERAL DESCRIPTION

The PM-111/PM-211 are voltage comparators featuring low input bias and offset currents, high-differential voltage ranges, and wide-supply voltage ranges. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply voltage. Strobing and offset balancing are available and the outputs can be wire OR'ed.

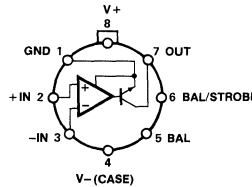
PIN CONNECTIONS



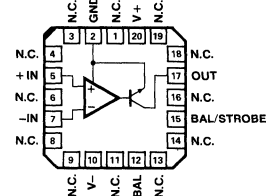
HERMETIC MINI-DIP
(Z-Suffix)



14-PIN HERMETIC DIP
(Y-Suffix)

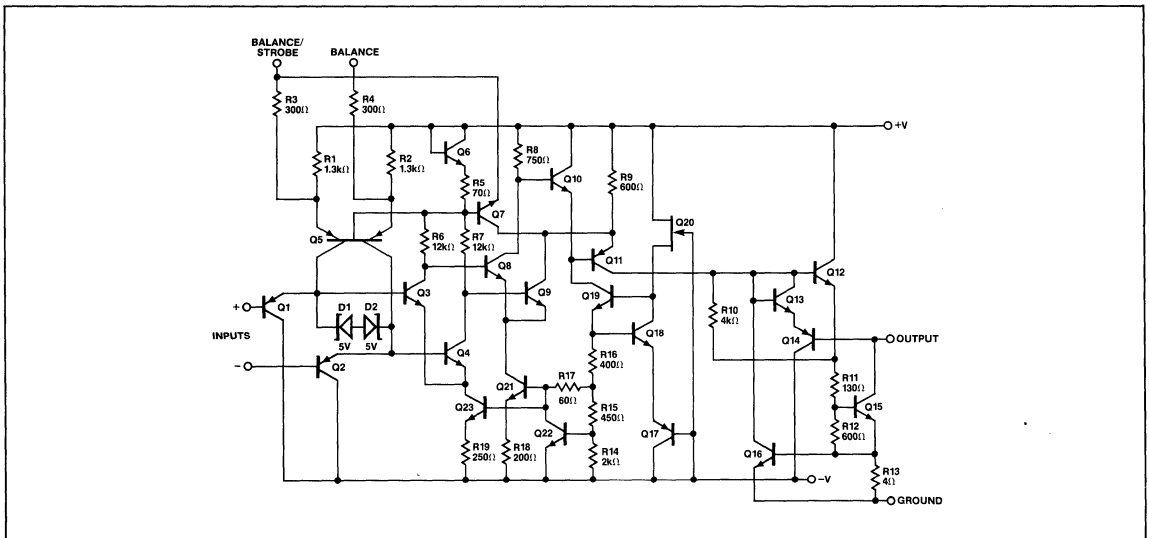


TO-99
(J-Suffix)



PM-111RC/883
LCC
(RC-Suffix)

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Total Supply Voltage, V_+ to V_-	36V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Strobe Pin Voltage	$V_+ - 5V$
Differential Input Voltage	$\pm 30V$
Input Voltage (Note 2)	$\pm 15V$
Power Dissipation (Note 3)	500mW
Output Short-Circuit Duration	10s
Operating Temperature Range	
PM-111	-55°C to $+125^\circ\text{C}$
PM-211	-25°C to $+85^\circ\text{C}$
DICE Junction Temperature (T_J)	-65°C to $+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering, 10 sec)	300°C

NOTES:

1. Absolute Maximum Ratings apply to both packaged parts and DICE, unless otherwise noted.
2. Rating applies to $V_S = \pm 15V$. The positive input-voltage limit is 30V above the negative supply. The negative input-voltage limit is equal to the negative supply or 30V below the positive supply, whichever is less.
3. Maximum package power-dissipation vs. ambient temperature.

PACKAGE TYPE	MAXIMUM AMBIENT	DERATE ABOVE
	TEMPERATURE FOR RATING	MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	75°C	$6.8\text{mW}/^\circ\text{C}$
Hermetic DIP (Z)	75°C	$6.7\text{mW}/^\circ\text{C}$
Hermetic DIP (Y)	95°C	$9.0\text{mW}/^\circ\text{C}$
LCC (RC)	88°C	$8.1\text{mW}/^\circ\text{C}$

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pin at ground and $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-111/PM-211			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	0.75	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	5.0	nA
Input Bias Current	I_B	(Note 1)	—	25	50	nA
Voltage Gain (Emitter)	A_{VE}	(Note 2)	—	75	—	V/mV
Voltage Gain (Collector)	A_{VC}		—	200	—	V/mV
Response Time	t_r	$R_L = 500\Omega$ (tied to V_+) $V_{OD} = 5\text{mV}$ (Note 3)	—	180	—	ns
Saturation Voltage	V_{OL}	$V_{IN} \leq -5\text{mV}$ $I_{OUT} = 50\text{mA}$	—	0.68	1.0	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5\text{mV}$ $V_{OUT} = 50V$	—	5	15	nA
Positive Supply Current	I_{SY+}		—	3.3	5	mA
Negative Supply Current	I_{SY-}		—	2.4	4	mA

NOTES:

1. The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a $7.5k\Omega$ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
2. Average of A_{V+} and A_{V-} over a $\pm 10V$ output range measured at the emitter.
3. The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge. The slowest response occurs at the highest temperature of operation.

8

VOLTAGE COMPARATORS

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, ground pin at ground and $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-211			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	0.8	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	7	nA
Input Bias Current	I_B	(Note 1)	—	25	100	nA
Voltage Gain (Emitter)	A_{VE}	(Note 2)	—	35	—	V/mV
Response Time	t_r	$R_L = 500\Omega$ (tied to V^+) $V_{OD} = 5mV$ (Note 3)	—	240	—	ns
Saturation Voltage	V_{OL}	$V_{IN} \leq -5mV$ $I_{OUT} = 50mA$	—	0.8	1.5	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5mV$ $V_{OUT} = 50V$	—	10	100	nA
Positive Supply Current	I_{SY^+}		—	4	6	mA
Negative Supply Current	I_{SY^-}		—	2.8	5	mA
Input Voltage Range	IVR		± 13	± 14	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pin at ground and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

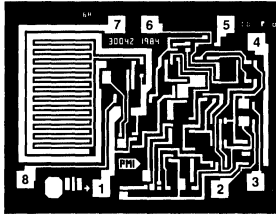
PARAMETER	SYMBOL	CONDITIONS	PM-111			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	0.8	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	10	nA
Input Bias Current	I_B	(Note 1)	—	25	100	nA
Voltage Gain (Emitter)	A_{VE}	(Note 2)	—	20	—	V/mV
Response Time	t_r	$R_L = 500\Omega$ (tied to V^+) $V_{OD} = 5mV$ (Note 3)	—	420	—	ns
Saturation Voltage	V_{OL}	$V_{IN} \leq -5mV$ $I_{OUT} = 50mA$	—	0.62	1.5	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5mV$ $V_{OUT} = 50V$	—	145	500	nA
Positive Supply Current	I_{SY^+}		—	4.2	6	mA
Negative Supply Current	I_{SY^-}		—	3	5	mA
Input Voltage Range	IVR		± 13	± 14	—	V

NOTES:

- The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5k Ω load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
- Average of A_{V^+} and A_{V^-} over a $\pm 10V$ output range measured at the emitter.
- The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge. The slowest response occurs at the highest temperature of operation.



DICE CHARACTERISTICS



DIE SIZE 0.066 × 0.050 inch, 3300 sq. mils
(1.68 × 1.27mm, 2.13 sq. mm)

1. GROUND
2. +IN
3. -IN
4. V-
5. BALANCE
6. BALANCE/STROBE
7. OUTPUT
8. V+

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ and ground pin at ground for PM-111GBC, $T_A = 125^\circ C$ for PM-111GTBC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-111GTBC	PM-111GBC	UNITS
			LIMIT	LIMIT	
Input Offset Voltage	V_{OS}	(Note 1)	3	3	mV
Input Offset Current	I_{OS}	(Note 1)	10	5	nA
Input Bias Current	I_B	(Note 1)	100	50	nA
Saturation Voltage	V_{OL}		1.5	1.0	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5mV$ $V_{OUT} = 50V$	500	15	nA
Input Voltage Range	IVR		± 13	—	V
Positive Supply Current	I_{SY+}		6	5	mA
Negative Supply Current	I_{SY-}		5	4	mA

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$ and ground pin at ground for PM-111GBC, $T_A = 125^\circ C$ for PM-111GTBC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-111GTBC	PM-111GBC	UNITS
			TYPICAL	TYPICAL	
Voltage Gain (Emitter)	A_{VE}	(Note 2)	20	75	V/mV
Response Time	t_r	(Note 3)	420	180	ns

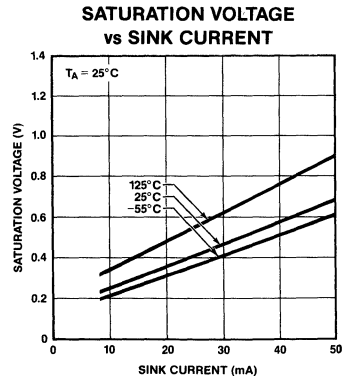
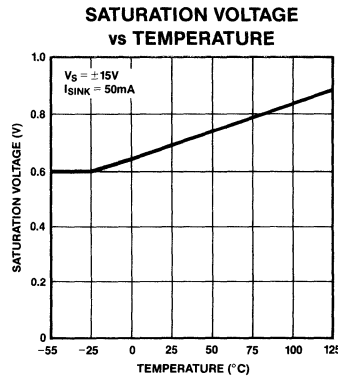
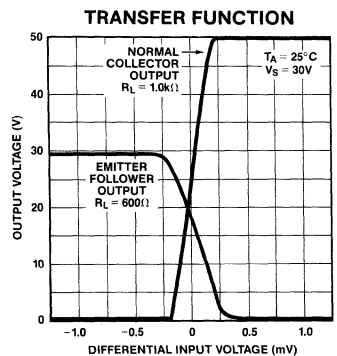
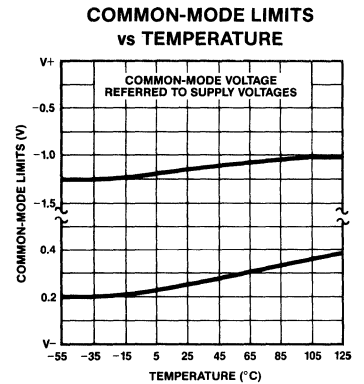
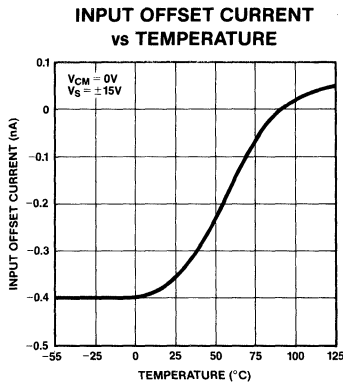
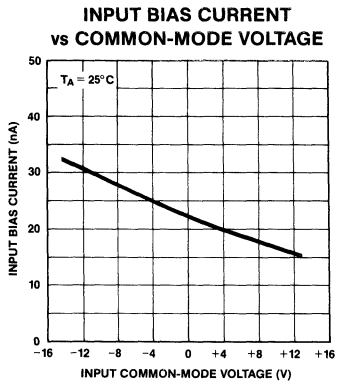
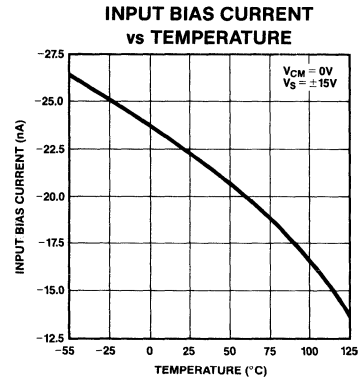
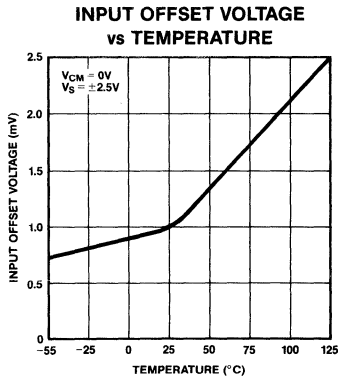
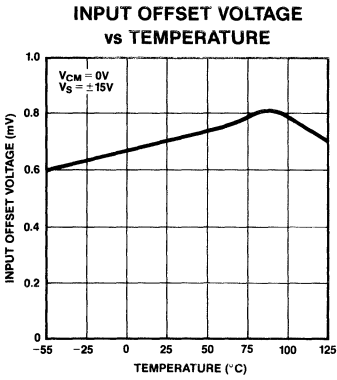
NOTES:

1. The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5k Ω load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
2. Average of A_{V+} and A_{V-} over a $\pm 10V$ output range measured at the emitter.
3. The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge. The slowest response occurs at the highest temperature of operation.


 VOLTAGE COMPARATORS



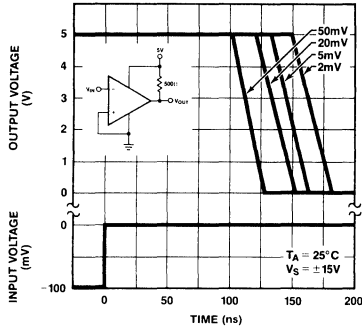
TYPICAL PERFORMANCE CHARACTERISTICS



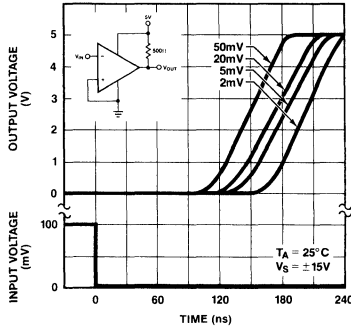


TYPICAL PERFORMANCE CHARACTERISTICS

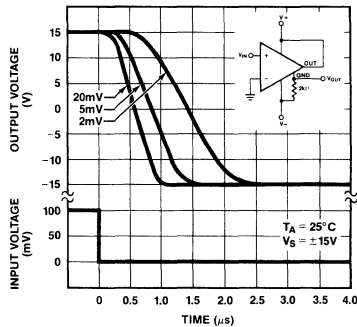
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



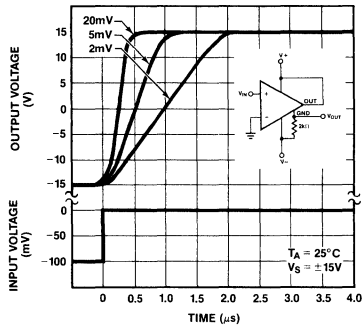
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



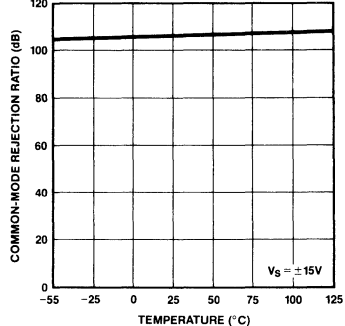
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



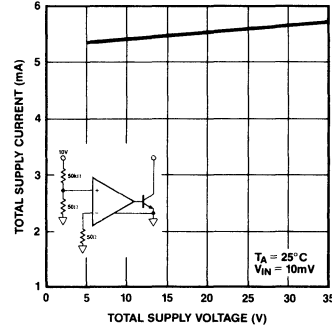
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



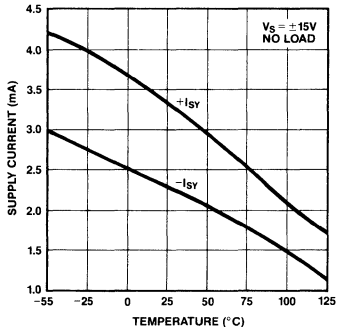
COMMON-MODE REJECTION RATIO vs TEMPERATURE



TOTAL SUPPLY CURRENT vs TOTAL SUPPLY VOLTAGE



SUPPLY CURRENT vs TEMPERATURE



VOLTAGE COMPARATORS



PM-119/PM-219/PM-319

DUAL
COMPARATORS

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Fast Response Time 80ns Typ
- High Output Drive Current 25mA
- Single or Dual Supply Operation +5V to $\pm 15V$
- Open Collector Outputs Up to +35V
- Inputs and Outputs Can Be Isolated from System Ground
- Two Independent Comparators

allowing output swings of up to +35V. High output drive capability facilitates RTL, DTL, and TTL interfacing, as well as relay and lamp driving at currents up to 25mA. Typical response time of 80ns with $\pm 15V$ power supplies makes the PM-119 ideal for application in fast A/D converters, level shifters, oscillators, and multivibrators.

ORDERING INFORMATION†

TO-100 10-PIN	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC DIP 14-PIN	EPOXY DIP 14-PIN	
PM119K*	PM119Y*	—	MIL
PM219K	PM219Y	—	IND
—	PM319Y	PM319P	COM

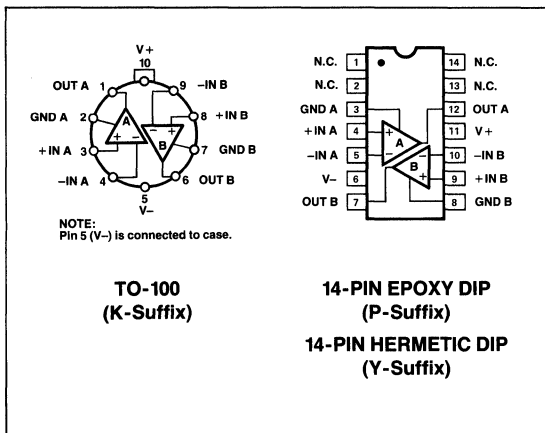
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

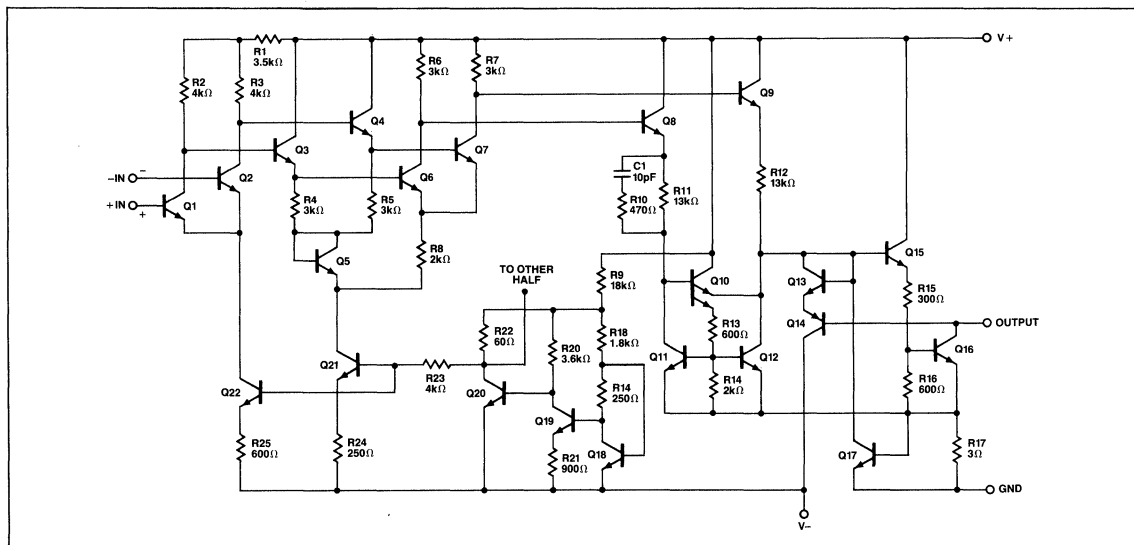
GENERAL DESCRIPTION

The PM-119 is a dual high-speed voltage comparator designed to operate from a single +5V supply up to $\pm 15V$ dual supplies. Open-collector outputs are provided for logic interface flexibility,

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (Each Comparator)



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pin at ground and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-119/PM-219			PM-319			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	—	0.7	4.0	—	2.0	8.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	30	75	—	80	200	nA
Input Bias Current	I_B	(Note 1)	—	150	500	—	250	1000	nA
Voltage Gain (Collector)	A_{VC}	(Note 2)	10	40	—	8	40	—	V/mV
Response Time	t_r	$V_{IN} = 100mV$ Step $V_{OD} = 5mV$ (Note 3)	—	80	—	—	80	—	ns
Positive Supply Current	I_{SY}	$V_S = +5V, 0V$	—	4.3	—	—	4.3	—	mA
Positive Supply Current	I_{SY+}	$V_S = \pm 15V$	—	8	11.5	—	8	11.5	mA
Negative Supply Current	I_{SY-}	$V_S = \pm 15V$	—	3	4.5	—	3	4.5	mA

NOTES:

1. The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a $7.5k\Omega$ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
2. Average of A_{V+} and A_{V-} over a $\pm 10V$ output range measured at the emitter.
3. The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge.





PM-139/PM-139A/PM-339A

QUAD LOW-POWER VOLTAGE COMPARATORS

Precision Monolithics Inc.

FEATURES

- Single or Dual Supply Operation
- Input Voltage Range Includes Ground
- Low Power Consumption (2mW/Comparator)
- Low Input Bias Current 25nA
- Low Input Offset Current $\pm 5nA$
- Low Offset Voltage $\pm 2mV$
- Low Output Saturation Voltage (250mV @ 4mA)
- Logic Outputs Compatible with TTL, DTL, ECL, MOS and CMOS
- Directly replaces LM139 and LM139A/339A Comparators

ORDERING INFORMATION†

+25°C V _{OS} (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	14-PIN HERMETIC DIP	LCC	
$\pm 2^*$	PM139AY*	PM139ARC/883	MIL
$\pm 5^*$	PM139Y*		MIL
± 2	PM339AY		COM

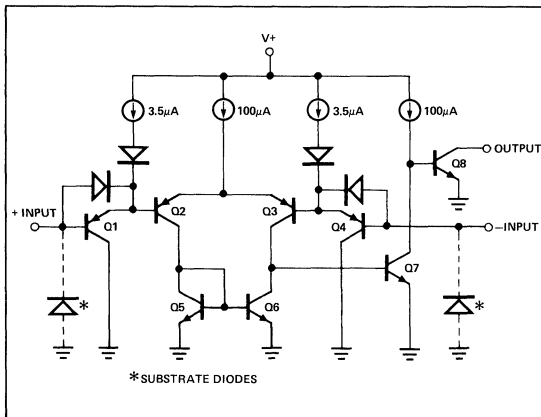
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

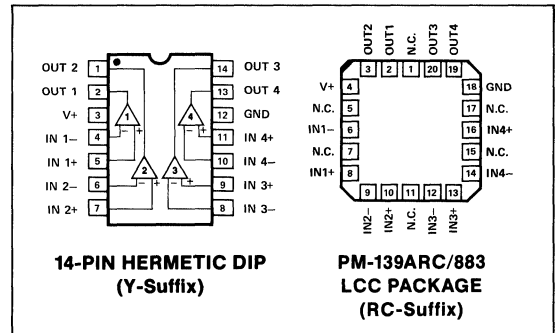
The PM-139 has four independent voltage comparators, each with precision DC specifications. Low offset voltage, bias current, power consumption and output saturation voltage

SIMPLIFIED SCHEMATIC (ONE COMPARATOR)

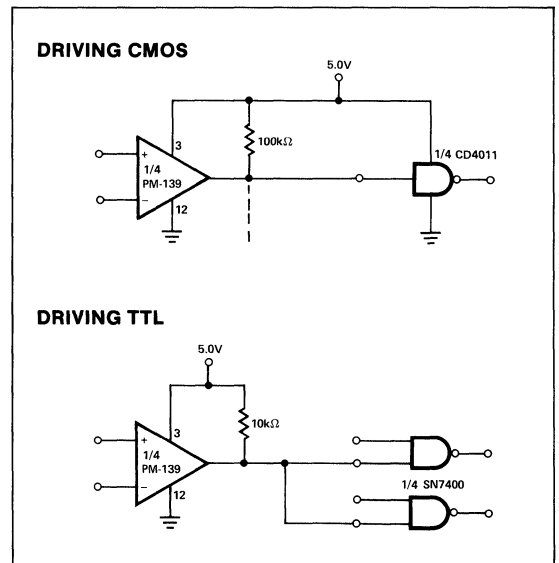


are offered in a design that features single power supply operation. The input voltage range includes ground for convenient single supply operation. The 2mA power supply current, independent of supply voltage — coupled with the single supply operation, makes this comparator ideal for low power applications. Open collector outputs allow maximum applications flexibility.

PIN CONNECTIONS



TYPICAL INTERFACE



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, V+	36V or ±18V	Input Current (V _{IN} < -0.3V)	50mA
Differential Input Voltage	36V	Operating Temperature Range	
Input Voltage	-0.3V to +36V	PM-339A	0°C to +70°C
Power Dissipation Hermetic DIP	500mW	PM-139A/139/139ARC	-55°C to +125°C
Derate Above 100°C	10mW/°C	Storage Temperature Range	-65°C to +150°C
Output Short-Circuit to Ground	Continuous	Lead Temperature (Soldering, 60 sec)	300°C

ELECTRICAL CHARACTERISTICS at V+ = +5V, T_A = 25°C, unless otherwise noted.

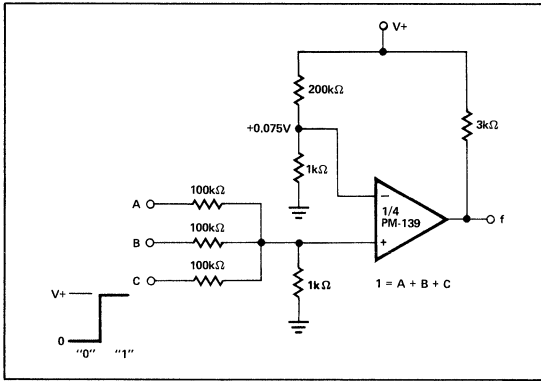
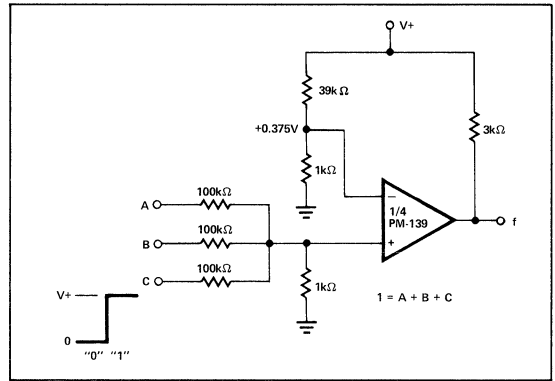
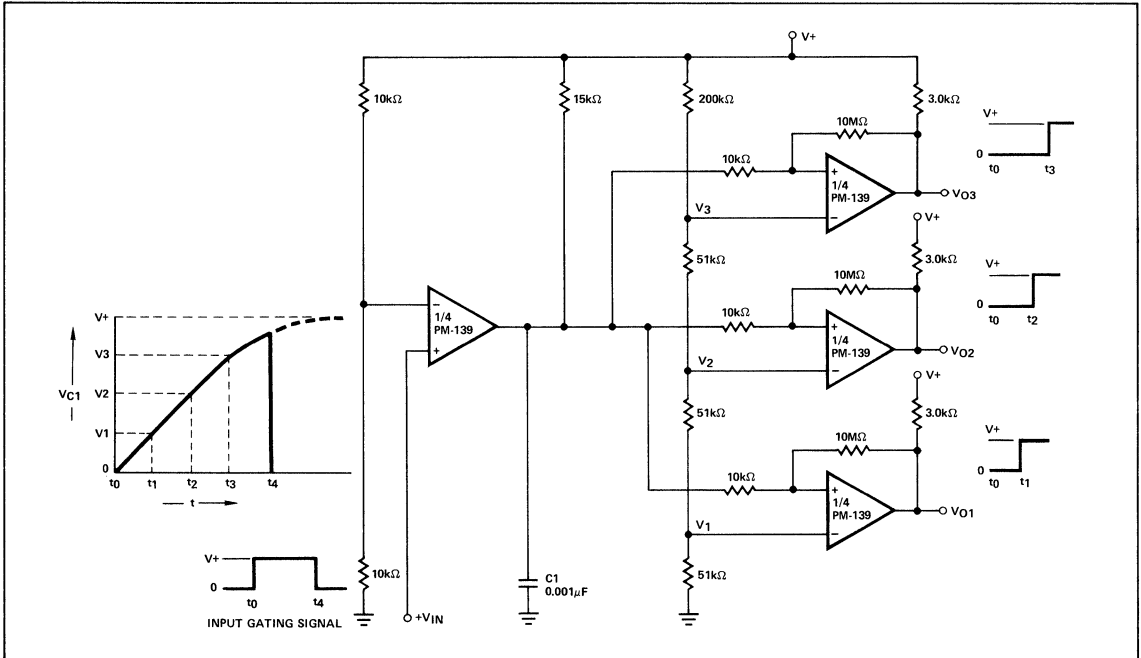
PARAMETER	SYMBOL	CONDITIONS	PM-139A			PM-339A			PM-139			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	(Note 1)	—	1	2	—	1	2	—	2	5	mV
Input Bias Current	I _B	I _{IN(+)} or I _{IN(-)} with Output in Linear Range	—	25	100	—	25	250	—	25	100	nA
Input Offset Current	I _{OS}	I _{IN(+)} or I _{IN(-)}	—	3	25	—	5	50	—	3	25	nA
Input Common-Mode Voltage Range	CMVR	(Notes 2, 5, 6)	0	—	3.5	0	—	3.5	0	—	3.5	V
Supply Current	I _S	R _L = ∞ on all Comparators V+ = 30V	—	0.8	2	—	0.8	2	—	0.8	2	mA
Voltage Gain	A _{VO}	R _L ≥ 15kΩ, V+ = 15V (to support large V _O swing) (Note 5)	50	200	—	50	200	—	50	200	—	V/mV
Large-Signal Response Time	t _r	V _{IN} = TTL Logic Swing, V _{REF} = 1.4V, V _{RL} = 5V, R _L = 5.1kΩ, (Note 4)	—	300	—	—	300	—	—	300	—	ns
Response Time	t _r	V _{RL} = 5V, R _L = 5.1kΩ (Notes 3, 4)	—	1.3	—	—	1.3	—	—	1.3	—	μs
Output Sink Current	I _{SINK}	V _{IN(-)} ≥ 1V, V _{IN(+)} = 0, V _O ≤ 1.5V	6	16	—	6	16	—	6	16	—	mA
Saturation Voltage	V _{OL}	V _{IN(-)} ≥ 1V, V _{IN(+)} = 0, I _{SINK} ≤ 4mA	—	250	400	—	250	400	—	250	400	mV
Output Leakage Current	I _{LEAK}	V _{IN(+)} ≥ 1V, V _{IN(-)} = 0, V _O = 30V	—	0.1	—	—	0.1	—	—	0.1	—	nA

ELECTRICAL CHARACTERISTICS at V+ = +5V, -55°C ≤ T_A ≤ +125°C for PM-139/139A and 0°C ≤ T_A ≤ +70°C for PM-339A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-139A			PM-339A			PM-139			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	(Note 1)	—	—	4	—	—	4	—	—	9	mV
Input Offset Current	I _{OS}	I _{IN(+)} or I _{IN(-)}	—	—	100	—	—	150	—	—	100	nA
Input Bias Current	I _B	I _{IN(+)} OR I _{IN(-)} with Output in Linear Range	—	—	300	—	—	400	—	—	300	nA
Input Common-Mode Voltage Range	CMVR	(Notes 3, 5)	0	—	V+ - 2	0	—	V+ - 2	0	—	V+ - 2	V
Saturation Voltage	V _{OL}	V _{IN(-)} ≥ 1V, V _{IN(+)} = 0, I _{SINK} ≤ 4mA	—	—	700	—	—	700	—	—	700	mV
Output Leakage Current	I _{LEAK}	V _{IN(+)} ≥ 1V, V _{IN(-)} = 0, V _O = 30V	—	—	1	—	—	1	—	—	1	μA
Differential Input Voltage		Keep All V _{INs} ≥ 0V	—	—	36	—	—	36	—	—	36	V

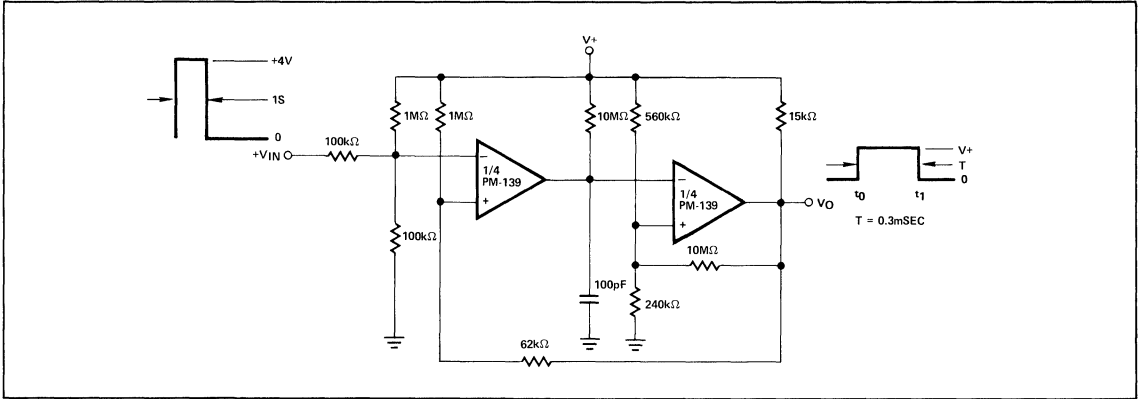
NOTES:

- At output switch point, V_O = 1.4V, R_S = 0Ω with V+ from 5V, and over the full input common-mode range (0V to V+ - 1.5V).
- The input common-mode voltage or either input voltage signal should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ - 1.5V, but either or both inputs can go to +30V without damage.
- The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained. See characteristics section.
- Sample tested.
- Guaranteed by design.
- Positive CMVR limit equals V+ - 1.5V for supply voltages other than 5V.

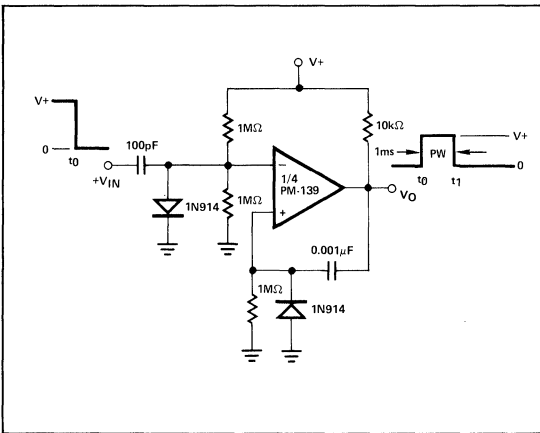
TYPICAL APPLICATIONS
OR GATE

AND GATE

TIME DELAY GENERATOR


TYPICAL APPLICATIONS

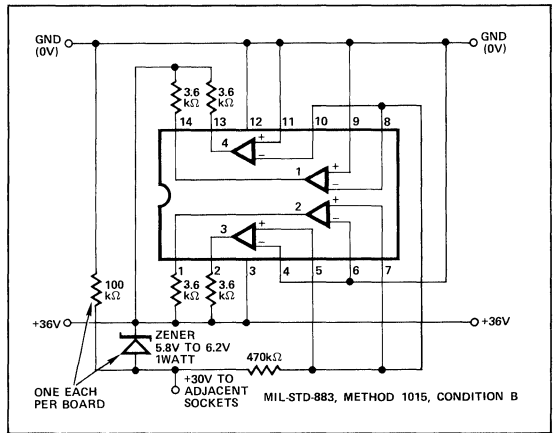
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK-OUT



ONE-SHOT MULTIVIBRATOR



BURN-IN CIRCUIT



VOLTAGE COMPARATORS

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



MATCHED TRANSISTOR ARRAYS

Precision Monolithics Inc.

9-3	Introduction
9-3	Definitions
9-4	Parameter Comparison Tables
9-5	MAT-01
	Matched Monolithic Dual Transistor
9-11	MAT-02
	Low-Noise, Matched Dual Monolithic Transistor
9-23	MAT-04
	Matched Monolithic Quad Transistor



MATCHED TRANSISTOR ARRAYS

Precision Monolithics Inc.

INTRODUCTION

Monolithic dual and quad transistor arrays feature inherently close matching of electrical parameters and very low thermal differentials. In addition, PMI arrays are specifically designed for low offset voltage, low offset voltage drift, low noise, and high gain, specified over a wide range of collector currents. Monolithic duals are optimized for amplifier input use and provide the best possible input stage performance. The dual and quad transistors are excellent for use in high-performance audio systems, high-gain instrumentation amplifiers, and precision current mirrors.

Both the dual and quad transistors are also designed for minimal base-to-emitter resistance which makes log conformity excellent. For an ideal transistor, the base-to-emitter voltage is equal to $(kT/q) \ln(I_C/I_S)$. An added term, $I_C r_{BE}$, causes departure from this idealized logarithmic relationship. The MAT-02 and new MAT-04 have very low r_{BE} over a wide range of collector current. Circuits for squaring, RMS-to-DC conversion, and logarithmic amplification can be accurately implemented through use of these low- r_{BE} products. The MAT-04 preliminary data sheet is shown in the Advanced Products Section.

The well-defined relationship between V_{BE} and collector current can also be used for temperature sensing or for generating bandgap-reference voltages. The low noise, low offsets, and high gain combined with a wide operating range for collector current make these monolithic arrays very useful for a diverse range of applications.

DEFINITIONS

Average Offset Current Drift (TCI_{OS}) — The ratio of the change in I_{OS} to the change in temperature producing it.

Average Offset Voltage Drift (TCV_{OS}) — The ratio of the change in V_{OS} to the change in temperature producing it.

Bias Current (I_B) — The average of the base currents at a specified collector voltage and current.

Broadband Noise Voltage (e_{nRMS}) — The root-mean-square noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Current Gain Match (Δh_{FE}) — The difference in h_{FE} between the transistors at a specified voltage and current, expressed as a percentage of the lower of the two h_{FE} 's.

$$\left(1 - \frac{h_{FE1}}{h_{FE2}}\right) \times 100$$

Excess Emitter Resistance (r_{BE}) — The effective resistance between the base and emitter terminals of each transistor.

Noise Voltage (e_{np-p}) — The peak-to-peak noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Noise Voltage Density (e_n) — The rms noise voltage referred to the input in a 1Hz band surrounding a specified frequency, measured at a specified collector voltage and current.

Offset Current (I_{OS}) — The difference between the base currents at a specified collector voltage and current.

Offset Current Change ($\Delta I_{OS}/\Delta V_{CB}$) — The ratio of the change in offset current to the change in collector-base voltage producing it.

Offset Voltage (V_{OS}) — The difference between the base-emitter voltages ($V_{BE1}-V_{BE2}$) at a specified collector voltage and current.

9

MATCHED TRANSISTORS



MATCHED TRANSISTOR ARRAYS

Precision Monolithics Inc.

Parameter Comparison Table ($I_C = 10\mu A$) for MAT-02

Device	BV_{CEO} Min (V)	V_{OS} Max (mV)	TCV_{OS} Max ($\mu V/^\circ C$)	h_{FE} Min	I_{OS} Max (nA)	TCI_{OS} Max ($\mu A/^\circ C$)
MAT-02A/E**	40	.05	0.3	400	0.5	90
MAT-02B/F**	40	.15	1	300	1.3	150
LM194	40	.05	0.3	300	0.7	N.C.
LM394	40	.15	1	200	2.0	N.C.
MAT-01AH	45	0.1	0.5	500	0.6	90
MAT-01GH	45	0.5	1.8	250	3.2	150
LM114A	45	0.5	2.0	500	2.0	—
LM114	45	2.0	10	250	10	—
LM115A	60	0.5	2.0	250	2.0	—
LM115	60	2.0	10	250	10	—
AD810*	35	3.0	15	100	2.0	600
AD811*	45	1.5	7.5	200	10	300
AD812*	35	1.0	5.0	400	2.5	300
AD813*	45	0.5	2.5	200	5	300
AD818*	20	1.0	5.0	200	10	300

* Discontinued

** Temperature range for A-grade and B-grade is $-55^\circ C$ to $+125^\circ C$; temperature range for E-grade and F-grade is $-25^\circ C$ to $+85^\circ C$.

Parameter Comparison Table ($I_C = 10\mu A$) for MAT-01 to 2N-Types

Device	BV_{CEO} Min (V)	V_{OS} Max (mV)	TCV_{OS} Max ($\mu V/^\circ C$)	h_{FE} Min	% h_{FE} Match Max	I_{OS} Max (nA)	TCI_{OS} Max ($\mu A/^\circ C$)
MAT-01GH	45	0.5	1.8	250	8	3.2	150
2N2639	45	5.0	10	50	10	20	1000
2N2640	45	10	20	50	20	40	2000
2N2642	45	5.0	10	100	10	10	500
2N2643	45	10	20	100	20	20	375
2N2915	45	3.0	10	60	10	17	600
2N2915A	45	2.0	5.0	60	15	26	900
2N2916	45	5.0	10	150	10	7	N.C.
2N2916A	45	2.0	5.0	150	15	10	300
2N2917	45	10	20	60	20	17	1450
2N2918	45	5.0	20	150	20	7	750
2N2919	60	3.0	10	60	10	17	600
2N2919A	60	1.5	5.0	60	10	17	600
2N2920	60	3.0	10	150	10	7	N.C.
2N2920A	60	1.5	5.0	150	10	7	300
2N2060	60	5.0	10	25	10	40	N.C.
2N2060A	60	3.0	5.0	25	10	40	N.C.
2N2060B	60	1.5	5.0	25	10	40	N.C.

Notes: 1. TCI_{OS} Max and I_{OS} Max calculated from published data.

2. N.C. = Insufficient published data to calculate.

3. All of above are physically interchangeable pin-for-pin with MAT-01 and MAT-02 series.



MAT-01

MATCHED MONOLITHIC
DUAL TRANSISTOR

Precision Monolithics Inc.

FEATURES

- Low V_{OS} (V_{BE} Match) **40 μ V Typ**
100 μ V Max
- Low $TC_{V_{OS}}$ **0.5 μ V/ $^{\circ}$ C Max**
- High h_{FE} **500 Min**
- Excellent h_{FE} Linearity from 10nA to 10mA
- Low Noise Voltage **0.23 μ V $_{p-p}$ — 0.1Hz to 10Hz**
- High Breakdown **45V Min**

ORDERING INFORMATION†

$T_A = 25^{\circ}$ C V_{OS} MAX (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
0.1	MAT01AH*	MIL
0.5	MAT01GH*	MIL

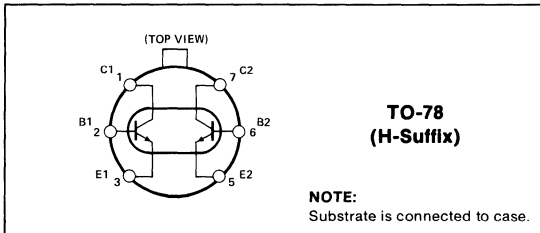
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The MAT-01 is a monolithic dual NPN transistor. An exclusive Silicon Nitride "Triple-Passivation" process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of 40 μ V, temperature drift of 0.15 μ V/ $^{\circ}$ C, and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at a collector current of only 10nA. The high gain at low collector current makes the MAT-01 ideal for use in low-power, low-level input stages.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (Note 4)

Collector-Base Voltage (BV_{CBO})	45V
MAT-01AH, GH, N	
Collector-Emitter Voltage (BV_{CEO})	45V
MAT-01AH, GH, N	
Collector-Collector Voltage (BV_{CC})	45V
MAT-01AH, GH, N	
Emitter-Emitter Voltage (BV_{EE})	45V
MAT-01AH, GH, N	
Emitter-Base Voltage (BV_{EBO}) (Note 1)	5V
Collector Current (I_C)	25mA
Emitter Current (I_E)	25mA
Total Power Dissipation	
Case Temperature $\leq 40^{\circ}$ C (Note 2)	1.8W
Ambient Temperature $\leq 70^{\circ}$ C (Note 3)	500mW
Operating Ambient Temperature	-55° C to $+125^{\circ}$ C
Operating Junction Temperature	-55° C to $+150^{\circ}$ C
Storage Temperature	-65° C to $+150^{\circ}$ C
Lead Temperature (Soldering, 60 sec)	300 $^{\circ}$ C
DICE Junction Temperature	-65° C to $+150^{\circ}$ C

NOTES:

1. Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5V rating shown.
2. Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/ $^{\circ}$ C for case temperatures above 40 $^{\circ}$ C.
3. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/ $^{\circ}$ C for ambient temperatures above 70 $^{\circ}$ C.
4. Absolute maximum ratings apply to both DICE and packaged devices.

9

MATCHED TRANSISTORS

**ELECTRICAL CHARACTERISTICS** at $V_{CB} = 15V$, $I_C = 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

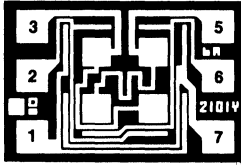
PARAMETER	SYMBOL	CONDITIONS	MAT-01AH			MAT-01GH			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Breakdown Voltage	BV_{CEO}	$I_C = 100\mu A$	45	—	—	45	—	—	V
Offset Voltage	V_{OS}		—	0.04	0.1	—	0.10	0.5	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)	—	2.0	—	—	2.0	—	$\mu V/\text{Mo}$
Long-Term		(Note 2)	—	0.2	—	—	0.2	—	
Offset Current	I_{OS}		—	0.1	0.6	—	0.2	3.2	nA
Bias Current	I_B		—	13	20	—	18	40	nA
Current Gain	h_{FE}	$I_C = 10nA$ $I_C = 10\mu A$ $I_C = 10mA$	—	590	—	—	430	—	
			500	770	—	250	560	—	
			—	840	—	—	610	—	
Current Gain Match	Δh_{FE}	$I_C = 10\mu A$ $100nA \leq I_C \leq 10mA$	—	0.7	3.0	—	1.0	8.0	%
			—	0.8	—	—	1.2	—	
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.23	0.4	—	0.23	0.4	μV_{p-p}
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	—	0.60	—	—	0.60	—	μV_{RMS}
Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 3) $f_O = 100\text{Hz}$ (Note 3) $f_O = 1000\text{Hz}$ (Note 3)	—	7.0	9.0	—	7.0	9.0	$nV/\sqrt{\text{Hz}}$
			—	6.1	7.6	—	6.1	7.6	
			—	6.0	7.5	—	6.0	7.5	
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	—	0.5	3.0	—	0.8	8.0	$\mu V/V$
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	—	2	15	—	3	70	pA/V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 30V$, $I_E = 0$ (Note 4)	—	15	50	—	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 30V$, $V_{BE} = 0$ (Notes 4, 6)	—	50	200	—	90	400	pA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = 30V$, (Note 6)	—	20	200	—	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 0.1mA$, $I_C = 1mA$ $I_B = 1mA$, $I_C = 10mA$	—	0.12	0.20	—	0.12	0.25	V
			—	0.8	—	—	0.8	—	
Gain-Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 10mA$	—	450	—	—	450	—	MHz
Output Capacitance	C_{ob}	$V_{CB} = 15V$, $I_E = 0$	—	2.8	—	—	2.8	—	pF
Collector-Collector Capacitance	C_{CC}	$V_{CC} = 0$	—	8.5	—	—	8.5	—	pF

ELECTRICAL CHARACTERISTICS at $V_{CB} = 15V$, $I_C = 10\mu A$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01AH			MAT-01GH			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	0.06	0.15	—	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 7)	—	0.15	0.50	—	0.35	1.8	$\mu V/^\circ C$
Offset Current	I_{OS}		—	0.9	8.0	—	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 5)	—	10	90	—	15	150	$pA/^\circ C$
Bias Current	I_B		—	28	60	—	36	130	nA
Current Gain	h_{FE}		167	400	—	77	300	—	
Collector-Base Leakage Current	I_{CBO}	$T_A = 125^\circ C$, $V_{CB} = 30V$, $I_E = 0$ (Note 4)	—	15	80	—	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	$T_A = 125^\circ C$, $V_{CE} = 30V$, $V_{BE} = 0$ (Notes 4, 6)	—	50	300	—	90	400	nA
Collector-Collector Leakage Current	I_{CC}	$T_A = 125^\circ C$, $V_{CC} = 30V$ (Note 6)	—	30	200	—	50	400	nA



DICE CHARACTERISTICS



DIE SIZE 0.035 × 0.025 inch, 875 sq. mils
(0.89 × 0.64 mm, 0.58 sq. mm)

1. COLLECTOR (1)
2. BASE (1)
3. EMITTER (1)
5. EMITTER (2)
6. BASE (2)
7. COLLECTOR (2)

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_{CB} = 15V$ and $I_C = 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}	$I_C = 100\mu A$	45	V MIN
Offset Voltage	V_{OS}		0.5	mV MAX
Offset Current	I_{OS}		3.2	nA MAX
Bias Current	I_B		40	nA MAX
Current Gain	h_{FE}		250	MIN
Current Gain Match	Δh_{FE}		8.0	% MAX
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	8.0	$\mu V/V$ MAX
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	70	pA/V MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 0.1mA, I_C = 1mA$	0.25	V MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_{CB} = 15V$ and $I_C = 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

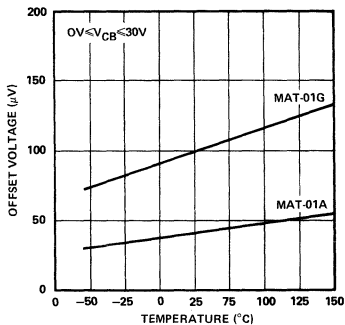
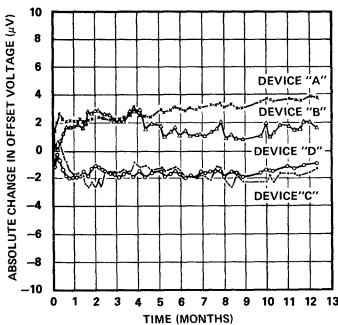
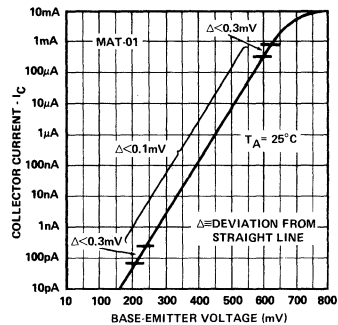
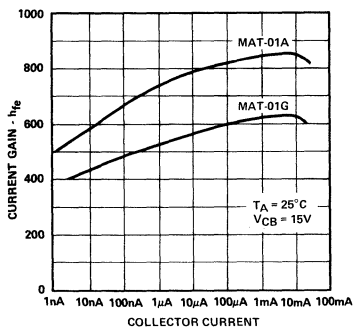
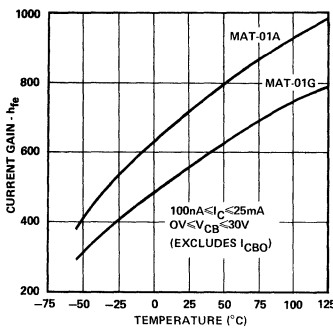
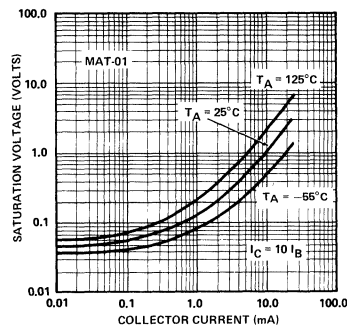
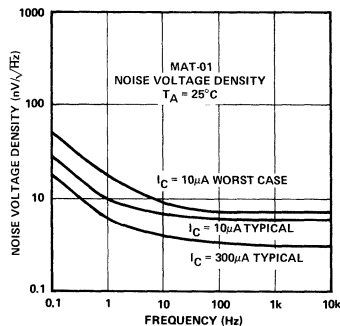
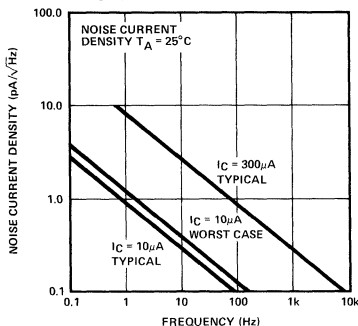
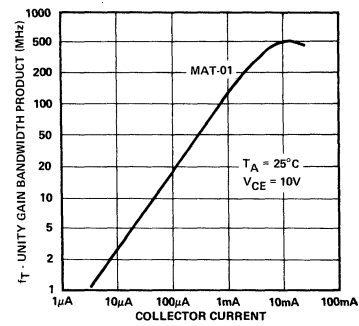
PARAMETER	SYMBOL	CONDITIONS	MAT-01N TYPICAL	UNITS
Average Offset Voltage Drift	TCV_{OS}		0.35	$\mu V/^\circ C$
Average Offset Current Drift	TCI_{OS}		15	pA/°C
Collector-Emitter-Leakage Current	I_{CES}	$V_{CE} = 30V, V_{BE} = 0$	90	pA
Collector-Base-Leakage Current	I_{CBO}	$V_{CB} = 30V, I_E = 0$	25	pA
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 10mA$	450	MHz
Offset Voltage Stability	$\Delta V_{OS}/T$	First Month (Note 1)	2.0	$\mu V/Mo$
		Long-Term (Note 2)	0.2	

NOTES:

1. Exclude first hour of operation to allow for stabilization.
2. Parameter describes long-term average drift after first month of operation.
3. Sample tested.
4. The collector-base (I_{CBO}) and collector-emitter (I_{CES}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.
5. Guaranteed by I_{OS} test limits over temperature.
6. I_{CC} and I_{CES} are guaranteed by measurement of I_{CBO} .
7. Guaranteed by V_{OS} test ($TCV_{OS} \approx \frac{V_{OS}}{T}$ for $V_{OS} \ll V_{BE}$) $T = 298^\circ K$ for $T_A = 25^\circ C$.

9

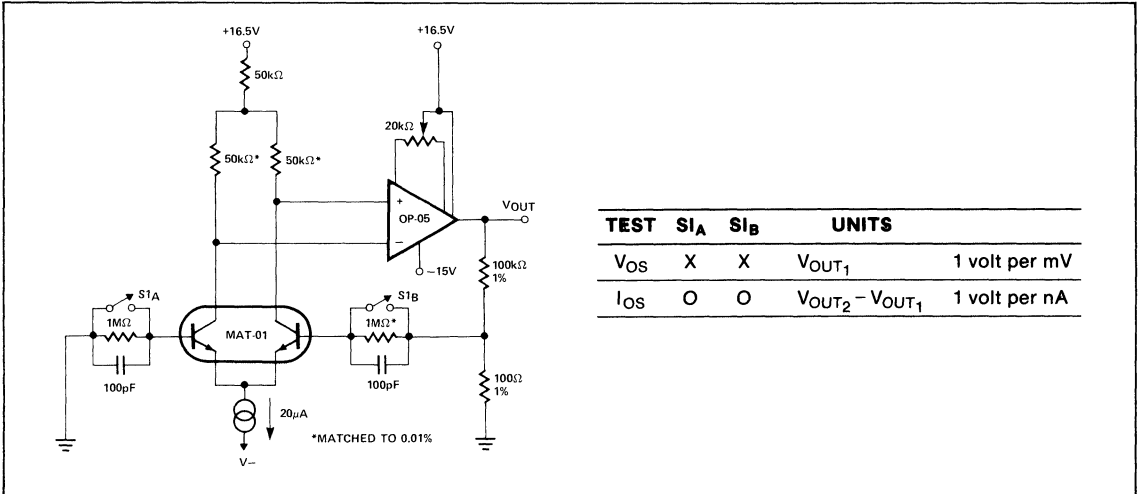
MATCHED TRANSISTORS

TYPICAL PERFORMANCE CHARACTERISTICS
OFFSET VOLTAGE vs TEMPERATURE

OFFSET VOLTAGE vs TIME

BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT

CURRENT GAIN vs COLLECTOR CURRENT

CURRENT GAIN vs TEMPERATURE

SATURATION VOLTAGE vs COLLECTOR CURRENT

NOISE VOLTAGE

NOISE CURRENT DENSITY

GAIN-BANDWIDTH vs COLLECTOR CURRENT


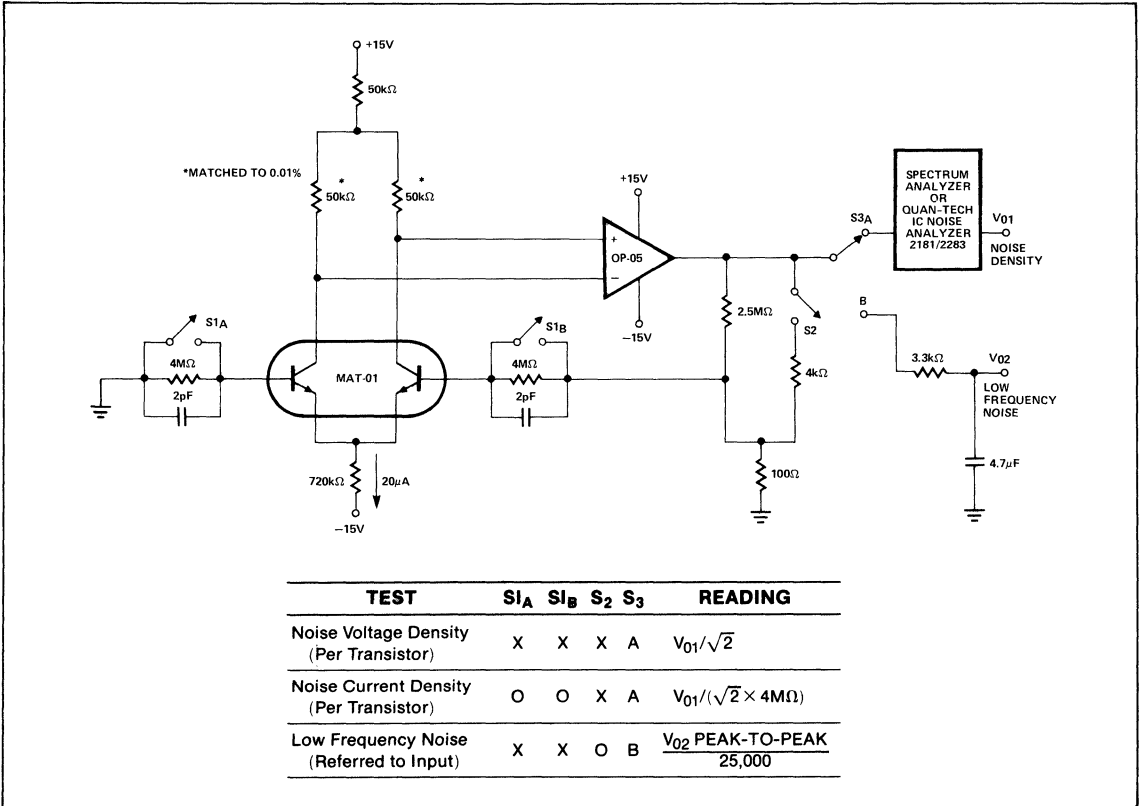


MAT-01 TEST CIRCUITS

MAT-01 MATCHING MEASUREMENT CIRCUIT



MAT-01 NOISE MEASUREMENT CIRCUIT



MATCHED TRANSISTORS

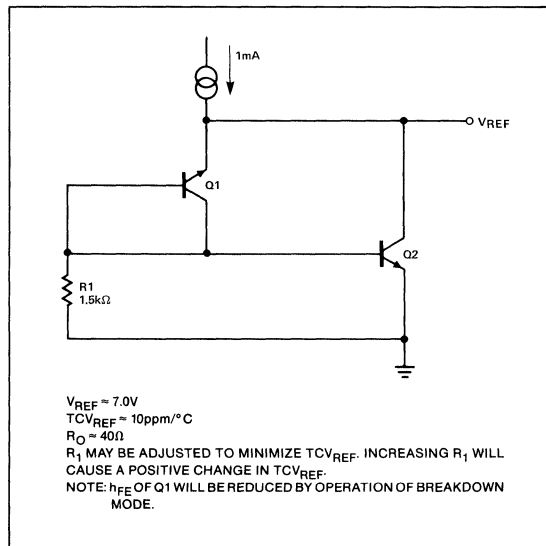
APPLICATION NOTES

Application of reverse bias voltages to the emitter-base junctions in excess of ratings (5V) may result in degradation of h_{FE} and h_{FE} matching characteristics. Circuit designs should be checked to ensure that reverse bias voltages above 5V cannot be applied during such transient conditions as at circuit turn-on and turn-off.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the predicted drift performance. Both input terminals should be maintained at the same temperature, preferably close to the temperature of the device's package.

TYPICAL APPLICATIONS

PRECISION REFERENCE



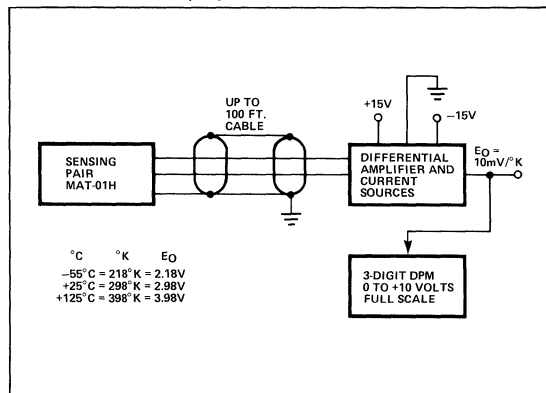
PRECISION OPERATIONAL AMPLIFIERS

*MATCH TO 0.1%
 **SEE TABLE FOR SPECIFIC DEVICE TYPE

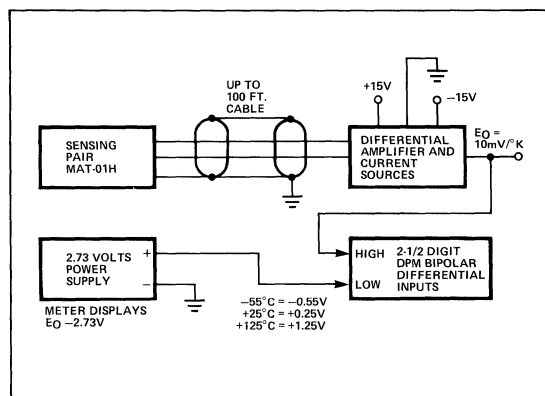
THIS CONFIGURATION CAN ALSO BE USED WITH THE LOW POWER OP-21 OR MICROPOWER OP-22 TO ACHIEVE A LOW NOISE AND LOW POWER PRECISION OP-AMP.

	MAT-01AH OP-02A	MAT-01AH OP-02A	MAT-01GH OP-02	MAT-01GH OP-02
V_{os} Maximum	0.15mV	0.27mV	0.65mV	1.2mV
TCV_{os} Maximum	$0.6\mu V/^{\circ}C$	$1\mu V/^{\circ}C$	$2\mu V/^{\circ}C$	$4\mu V/^{\circ}C$
I_{os} Maximum	0.8nA	0.1nA	3.2nA	0.32nA
I_b Maximum	20nA	2nA	40nA	4nA
Gain Minimum	2,000,000	2,000,000	800,000	800,000
I_s	$20\mu A$	$2\mu A$	$20\mu A$	$2\mu A$
R_L	$100k\Omega$	$1M\Omega$	$100k\Omega$	$1M\Omega$

BASIC DIGITAL THERMOMETER READOUT IN DEGREES KELVIN ($^{\circ}K$)



DIGITAL THERMOMETER WITH READOUT IN $^{\circ}C$





MAT-02

LOW-NOISE, MATCHED DUAL MONOLITHIC TRANSISTOR

Precision Monolithics Inc.

FEATURES

- Low Offset Voltage 50 μ V Max
- Low Noise Voltage at 100Hz, 1mA ... 1.0nV/ $\sqrt{\text{Hz}}$ Max
- High Gain (h_{FE}) 500 Min at $I_C = 1\text{mA}$
..... 300 Min at $I_C = 1\mu\text{A}$
- Excellent Log Conformance $r_{BE} \approx 0.3\Omega$
- Low Offset Voltage Drift 0.1 $\mu\text{V}/^\circ\text{C}$ Max
- Improved Direct Replacement for LM194/394

ORDERING INFORMATION

$T_A = 25^\circ\text{C}$ V_{OS} Max (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-78 6-PIN	LCC	
50	MAT02AH*		MIL
50	MAT02EH		IND
150	MAT02BH*	MAT02BRC/883	MIL
150	MAT02FH		IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

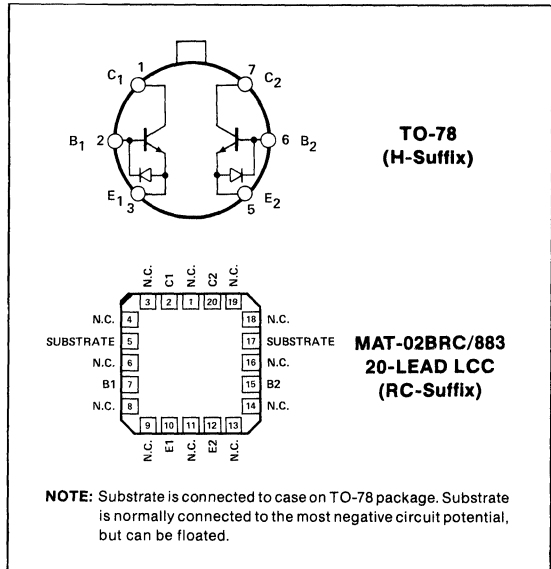
GENERAL DESCRIPTION

The design of the MAT-02 series of NPN dual monolithic transistors is optimized for very low noise, low drift, and low r_{BE} . Precision Monolithics' exclusive Silicon Nitride "Triple-Passivation" process stabilizes the critical device parameters over wide ranges of temperature and elapsed time. Also, the high current gain (h_{FE}) of the MAT-02 is maintained over a wide range of collector current. Exceptional characteristics of the MAT-02 include offset voltage of 50 μV max (A/E grades) and 150 μV max (B/F grades). Device performance is specified over the full military temperature range as well as at 25 $^\circ\text{C}$.

Input protection diodes are provided across the emitter-base junctions to prevent degradation of the device characteristics due to reverse-biased emitter current. The substrate is clamped to the most negative emitter by the parasitic isolation junction created by the protection diodes. This results in complete isolation between the transistors.

The MAT-02 should be used in any application where low noise is a priority. The MAT-02 can be used as an input stage to make an amplifier with noise voltage of less than 1.0nV/ $\sqrt{\text{Hz}}$ at 100Hz. Other applications, such as log/anti-log circuits, may use the excellent logging conformity of the MAT-02. Typical bulk resistance is only 0.3 Ω to 0.4 Ω . The MAT-02 electrical characteristics approach those of an ideal transistor when operated over a collector current range of 1 μA to 10mA. For applications requiring multiple devices see MAT-04 Quad Matched Transistor data sheet.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (Note 3)

Collector-Base Voltage (V_{CBO})	40V
MAT-02AH, BH, EH, FH	40V
Collector-Emitter Voltage (V_{CEO})	40V
MAT-02AH, BH, EH, FH	40V
Collector-Collector Voltage (V_{CC})	40V
MAT-02AH, BH, EH, FH	40V
Emitter-Emitter Voltage (V_{EE})	40V
MAT-02AH, BH, EH, FH	40V
Collector Current (I_C)	20mA
Emitter Current (I_E)	20mA
Total Power Dissipation	
Case Temperature $\leq 40^\circ\text{C}$ (Note 1)	1.8W
Ambient Temperature $\leq 70^\circ\text{C}$ (Note 2)	500mW
Operating Ambient Temperature	-55 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Operating Junction Temperature	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Storage Temperature	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300 $^\circ\text{C}$
DICE Junction Temperature	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$

NOTES:

1. Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/ $^\circ\text{C}$ for case temperature above 40 $^\circ\text{C}$.
2. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/ $^\circ\text{C}$ for ambient temperature above 70 $^\circ\text{C}$.
3. Absolute maximum ratings apply to both DICE and packaged devices.



MATCHED TRANSISTORS

**ELECTRICAL CHARACTERISTICS** at $V_{CB} = 15V$, $I_C = 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02A/E			MAT-02B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$I_C = 1mA$ (Note 1)	500	605	—	400	605	—	
		$I_C = 100\mu A$	500	590	—	400	590	—	
		$I_C = 10\mu A$	400	550	—	300	550	—	
		$I_C = 1\mu A$	300	485	—	200	485	—	
Current Gain Match	Δh_{FE}	$10\mu A \leq I_C \leq 1mA$, (Note 2)	—	0.5	2	—	0.5	4	%
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\mu A \leq I_C \leq 1mA$	—	10	50	—	80	150	μV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq V_{MAX}$, (Note 6) $1\mu A \leq I_C \leq 1mA$	—	10	25	—	10	50	μV
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	$V_{CB} = 0V$ $1\mu A \leq I_C \leq 1mA$	—	5	25	—	5	50	μV
Offset Current Change vs V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq V_{MAX}$	—	30	70	—	30	70	pA/V
Bulk Resistance	r_{BE}	$10\mu A \leq I_C \leq 10mA$	—	0.3	0.5	—	0.3	0.5	Ω
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$	—	25	200	—	25	400	pA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$, (Notes 3, 5)	—	35	200	—	35	400	pA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}$, (Notes 3, 5) $V_{BE} = 0$	—	35	200	—	35	400	pA
Noise Voltage Density	e_n	$I_C = 1mA$, $V_{CB} = 0$, (Note 4)	—	1.6	2	—	1.6	3	nV/\sqrt{Hz}
		$f_O = 10Hz$	—	0.9	1	—	0.9	2	
		$f_O = 100Hz$	—	0.85	1	—	0.85	2	
		$f_O = 1kHz$	—	0.85	1	—	0.85	2	
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1mA$ $I_B = 100\mu A$	—	0.05	0.1	—	0.05	0.2	V
Input Bias Current	I_B	$I_C = 10\mu A$	—	—	25	—	—	34	nA
Input Offset Current	I_{OS}	$I_C = 10\mu A$	—	—	0.6	—	—	1.3	nA
Breakdown Voltage	BV_{CEO}		40	—	—	40	—	—	V
Gain-Bandwidth Product	f_T	$I_C = 10mA$, $V_{CE} = 10V$	—	200	—	—	200	—	MHz
Output Capacitance	C_{OB}	$V_{CB} = 15V$, $I_E = 0$	—	23	—	—	23	—	pF
Collector-Collector Capacitance	C_{CC}	$V_{CC} = 0$	—	35	—	—	35	—	pF

NOTES:

- Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
- Current Gain Match (Δh_{FE}) is defined as:
- Guaranteed by design.
- Sample tested.
- I_{CC} and I_{CES} are verified by measurement of I_{CBO} .
- This is the maximum change in V_{OS} as V_{CB} is swept from 0V to 40V.

$$\Delta h_{FE} = \frac{100 (\Delta I_B) (h_{FE} \text{ min})}{I_C}$$



ELECTRICAL CHARACTERISTICS $V_{CB} = 15V, -25^{\circ}C \leq T_A \leq +85^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02E			MAT-02F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\mu A \leq I_C \leq 1mA$	—	—	70	—	—	220	μV
Average Offset Voltage Drift	TCV_{OS}	$10\mu A \leq I_C \leq 1mA, 0 \leq V_{CB} \leq V_{MAX}$, (Note 1) V_{OS} Trimmed to Zero, (Note 3)	—	0.08	0.3	—	0.08	1	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}	$I_C = 10\mu A$	—	—	8	—	—	13	nA
Input Offset Current Drift	TCI_{OS}	$I_C = 10\mu A$, (Note 4)	—	40	90	—	40	150	$pA/^{\circ}C$
Input Bias Current	I_B	$I_C = 10\mu A$	—	—	45	—	—	50	nA
Current Gain	h_{FE}	$I_C = 1mA$, (Note 2)	325	—	—	300	—	—	
		$I_C = 100\mu A$	275	—	—	250	—	—	
		$I_C = 10\mu A$	225	—	—	200	—	—	
		$I_C = 1\mu A$	200	—	—	150	—	—	
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$	—	2	—	—	3	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}, V_{BE} = 0$	—	3	—	—	4	—	nA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$	—	3	—	—	4	—	nA

ELECTRICAL CHARACTERISTICS $V_{CB} = 15V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02A			MAT-02B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\mu A \leq I_C \leq 1mA$	—	—	80	—	—	250	μV
Average Offset Voltage Drift	TCV_{OS}	$10\mu A \leq I_C \leq 1mA, 0 \leq V_{CB} \leq V_{MAX}$, (Note 1) V_{OS} Trimmed to Zero, (Note 3)	—	0.08	0.3	—	0.08	1	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}	$I_C = 10\mu A$	—	—	9	—	—	15	nA
Input Offset Current Drift	TCI_{OS}	$I_C = 10\mu A$, (Note 4)	—	40	90	—	40	150	$pA/^{\circ}C$
Input Bias Current	I_B	$I_C = 10\mu A$	—	—	60	—	—	70	nA
Current Gain	h_{FE}	$I_C = 1mA$, (Note 2)	275	—	—	250	—	—	
		$I_C = 100\mu A$	225	—	—	200	—	—	
		$I_C = 10\mu A$	175	—	—	150	—	—	
		$I_C = 1\mu A$	150	—	—	100	—	—	
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$ $T_A = 125^{\circ}C$	—	15	—	—	25	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}, V_{BE} = 0$ $T_A = 125^{\circ}C$	—	50	—	—	50	—	nA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$ $T_A = 125^{\circ}C$	—	30	—	—	40	—	nA

NOTES:

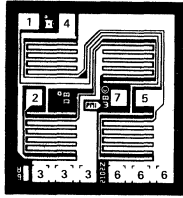
- Guaranteed by V_{OS} test ($TCV_{OS} = \frac{V_{OS}}{T}$ for $V_{OS} \ll V_{BE}$) $T = 298k$ for $T_A = 25^{\circ}C$.
- Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
- The initial zero offset voltage is established by adjusting the ratio of I_{C1} to I_{C2} at $T_A = 25^{\circ}C$. This ratio must be held to 0.003% over the entire temperature range. Measurements are taken at the temperature extremes and $25^{\circ}C$.
- Guaranteed by design.



MATCHED TRANSISTORS



DICE CHARACTERISTICS



1. COLLECTOR 1
2. BASE 1
3. EMITTER 1
4. COLLECTOR 2
5. BASE 2
6. EMITTER 2
7. SUBSTRATE

DIE SIZE 0.060 × 0.056 inch, 3,360 sq. mils
(1.520 × 1.420: 216 sq. mm)

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at 25°C for $V_{CB} = 15V$ and $I_C = 10\mu A$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}		40	V MIN
Offset Voltage	V_{OS}	$10\mu A \leq I_C \leq 1mA$	150	μV MAX
Input Offset Current	I_{OS}		1.2	nA MAX
Input Bias Current	I_B	$V_{CB} = 0V$	34	nA MAX
Current Gain	h_{FE}	$I_C = 1mA, V_{CB} = 0V$ $I_C = 10\mu A, V_{CB} = 0V$	400 300	MIN
Current Gain Match	Δh_{FE}	$10\mu A \leq I_C \leq 1mA, V_{CB} = 0V$	4	% MAX
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$0V \leq V_{CB} \leq 40V$ $10\mu A \leq I_C \leq 1mA$	50	μV MAX
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	$V_{CB} = 0$ $10\mu A \leq I_C \leq 1mA$	50	μV MAX
Bulk Resistance	r_{BE}	$100\mu A \leq I_C \leq 10mA$	0.5	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1mA$ $I_B = 100\mu A$	0.2	V MAX

NOTE:

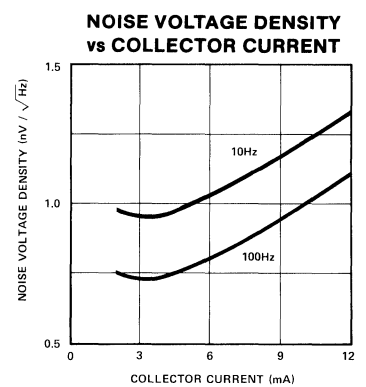
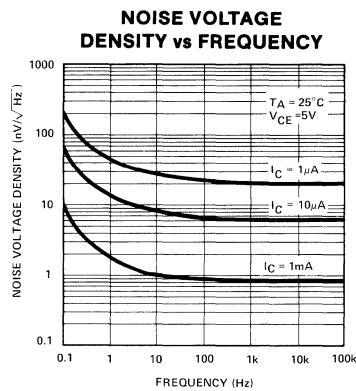
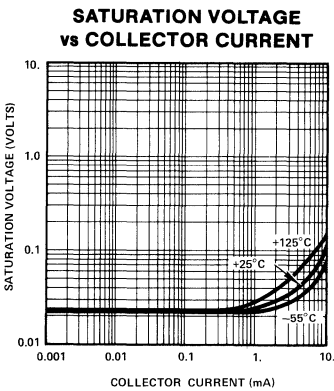
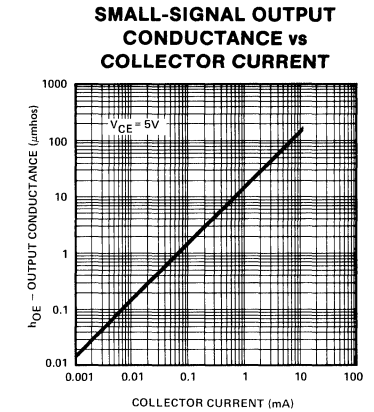
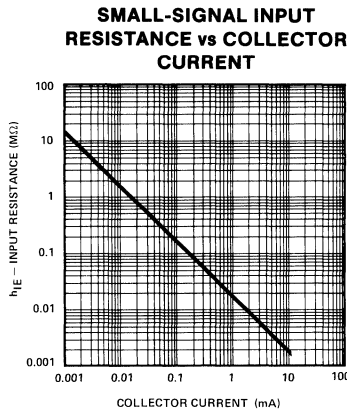
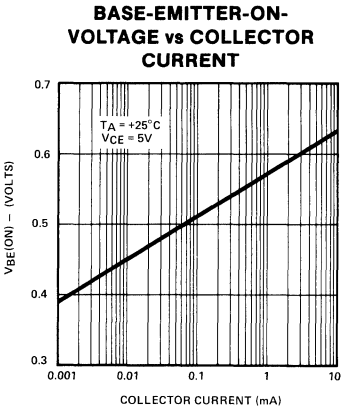
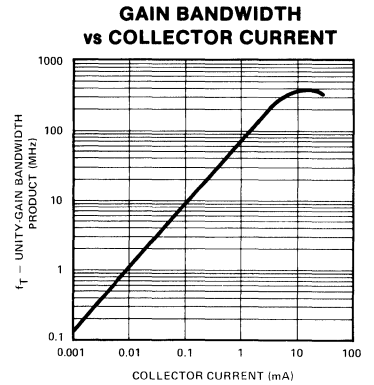
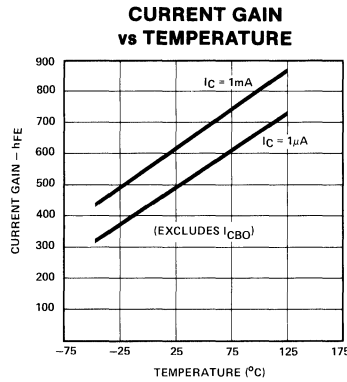
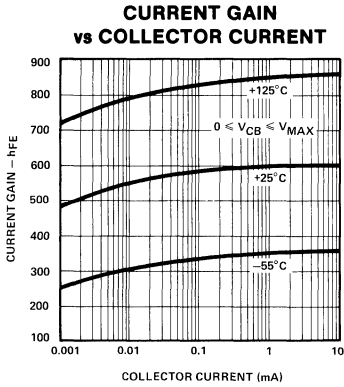
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS $V_{CB} = 15V$, $I_C = 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

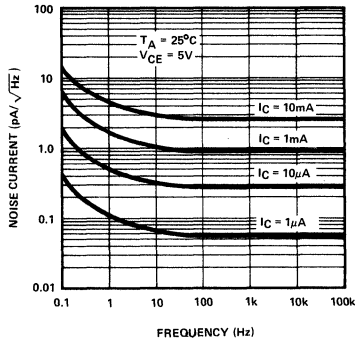
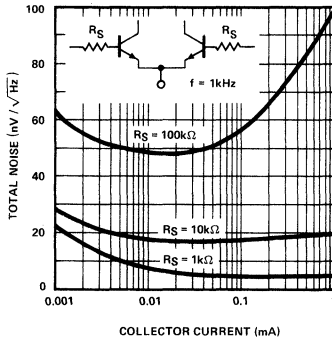
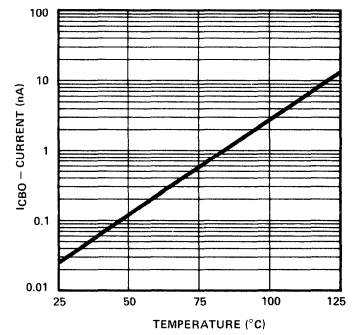
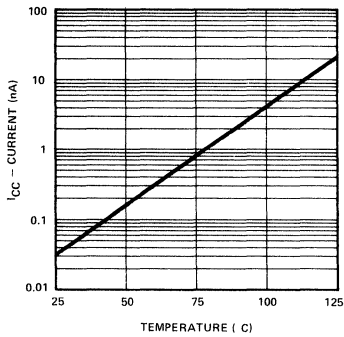
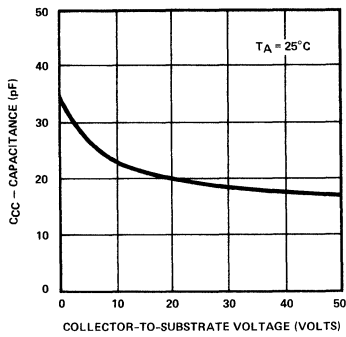
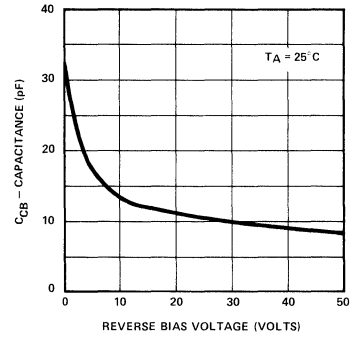
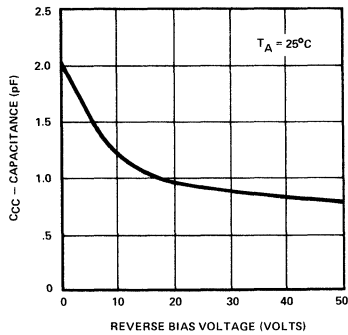
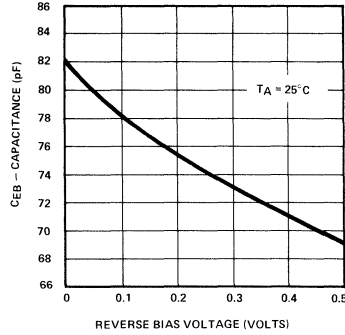
PARAMETER	SYMBOL	CONDITIONS	MAT-02N TYPICAL	UNITS
Average Offset Voltage Drift	TCV_{OS}	$10\mu A \leq I_C \leq 1mA$ $0 \leq V_{CB} \leq V_{MAX}$	0.08	$\mu V/^\circ C$
Average Offset Current Drift	TCI_{OS}	$I_C = 10\mu A$	40	$pA/^\circ C$
Gain-Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 10mA$	200	MHz
Offset Current Change vs V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 40V$	70	pA/V

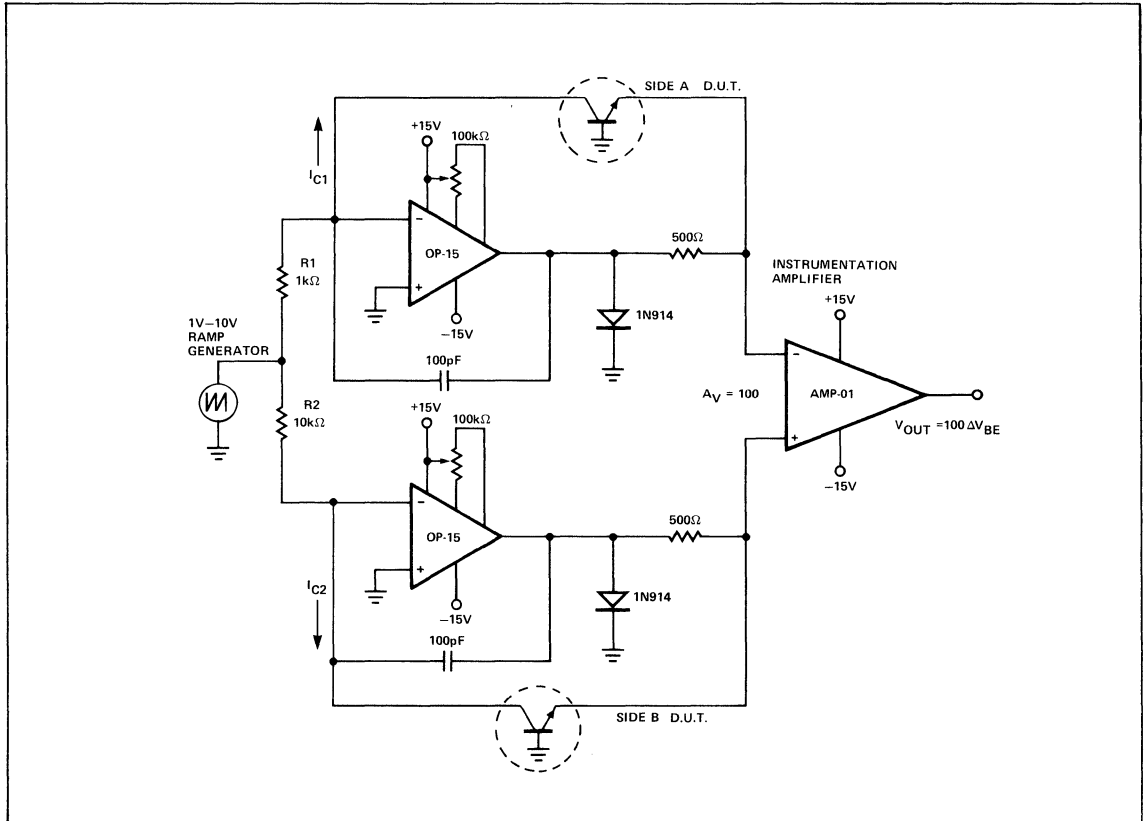


TYPICAL PERFORMANCE CHARACTERISTICS



MATCHED TRANSISTORS

TYPICAL PERFORMANCE CHARACTERISTICS
NOISE CURRENT DENSITY vs FREQUENCY

TOTAL NOISE vs COLLECTOR CURRENT

COLLECTOR-TO-BASE LEAKAGE vs TEMPERATURE

COLLECTOR-TO-COLLECTOR LEAKAGE vs TEMPERATURE

COLLECTOR-TO-COLLECTOR CAPACITANCE vs COLLECTOR-TO-SUBSTRATE VOLTAGE

COLLECTOR-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE

COLLECTOR-TO-COLLECTOR CAPACITANCE vs REVERSE BIAS VOLTAGE

EMITTER-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE


LOG CONFORMANCE TEST CIRCUIT

LOG CONFORMANCE TESTING

The log conformance of the MAT-02 is tested using the circuit shown above. The circuit employs a dual transdiode logarithmic converter operating at a fixed ratio of collector currents that are swept over a 10:1 range. The output of each transdiode converter is the V_{BE} of the transistor plus an error term which is the product of the collector current and r_{BE} , the bulk emitter resistance. The difference of the V_{BE} is amplified at a gain of $\times 100$ by the AMP-01 instrumentation amplifier. The differential emitter-base voltage (ΔV_{BE}) consists of a temperature-dependent DC level plus an AC error voltage which is the deviation from true log conformity as the collector currents vary.

The output of the transdiode logarithmic converter comes from the idealized intrinsic transistor equation (for silicon):

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} \quad \text{where} \quad (1)$$

k = Boltzmann's Constant ($1.38062 \times 10^{-23} \text{ J/}^\circ\text{K}$)

q = Unit Electron Charge ($1.60219 \times 10^{-19} \text{ C}$)

T = Absolute Temperature, $^\circ\text{K}$ ($= ^\circ\text{C} + 273.2$)

I_S = Extrapolated Current for $V_{BE} = 0$

I_C = Collector Current

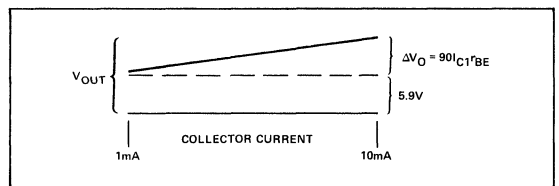
An error term must be added to this equation to allow for the bulk resistance (r_{BE}) of the transistor. Error due to the op amp input current is limited by use of the OP-15 BIFET-input op amp. The resulting AMP-01 input is:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{I_{C1}}{I_{C2}} + I_{C1} r_{BE1} - I_{C2} r_{BE2} \quad (2)$$

A ramp function which sweeps from 1V to 10V is converted by the op amps to a collector current ramp through each transistor. Because I_{C1} is made equal to $10 I_{C2}$, and assuming $T_A = 25^\circ\text{C}$, the previous equation becomes:

$$\Delta V_{BE} = 59\text{mV} + 0.9 I_{C1} r_{BE} \quad (\Delta r_{BE} \sim 0)$$

As viewed on an oscilloscope, the change in ΔV_{BE} for a 10:1 change in I_C is then displayed as shown below:



With the oscilloscope AC coupled, the temperature dependent term becomes a DC offset and the trace represents the deviation from true log conformity. The bulk resistance can be calculated from the voltage deviation ΔV_O and the change in collector current (9mA):

$$r_{BE} = \frac{\Delta V_O}{9\text{mA}} \times \frac{1}{100} \quad (3)$$

This procedure finds r_{BE} for Side A. Switching R_1 and R_2 will provide the r_{BE} for Side B. Differential r_{BE} is found by making $R_1 = R_2$.

APPLICATIONS: NONLINEAR FUNCTIONS

MULTIPLIER/DIVIDER CIRCUIT

The excellent log conformity of the MAT-02 over a very wide range of collector current makes it ideal for use in log-antilog circuits. Such nonlinear functions as multiplying, dividing, squaring, and square-rooting are accurately and easily implemented with a log-antilog circuit using two MAT-02 pairs (see Figure 1). The transistor circuit accepts three input currents (I_1 , I_2 , and I_3) and provides an output current I_O according to $I_O = I_1 I_2 / I_3$. All four currents must be positive in the log-antilog circuit, but negative input voltages can be

easily accommodated by various offsetting techniques. Protective diodes across each base-to-emitter junction would normally be needed, but these diodes are built into the MAT-02. External protection diodes are therefore not needed.

For the circuit shown in Figure 1, the operational amplifiers make $I_1 = V_X/R_1$, $I_2 = V_Y/R_2$, $I_3 = V_Z/R_3$, and $I_O = V_O/R_O$. The output voltage for this one-quadrant, log-antilog multiplier/divider is ideally:

$$V_O = \frac{R_3 R_O}{R_1 R_2} \frac{V_X V_Y}{V_Z} \quad (V_X, V_Y, V_Z > 0) \quad (4)$$

If all the resistors (R_O , R_1 , R_2 , R_3) are made equal, then $V_O = V_X V_Y / V_Z$. Resistor values of 50k Ω to 100k Ω are recommended assuming an input range of 0.1V to +10V.

ERROR ANALYSIS

The base-to-emitter voltage of the MAT-02 in its forward-active operation is:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} + r_{BE} I_C, \quad V_{CB} \sim 0 \quad (5)$$

The first term comes from the idealized intrinsic transistor equation previously discussed (see equation (1)).

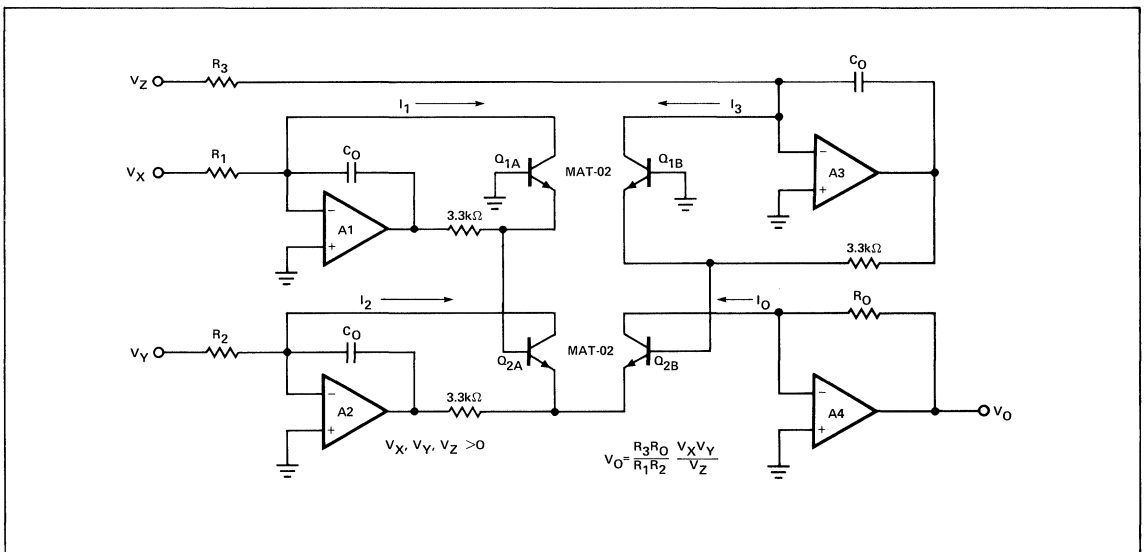
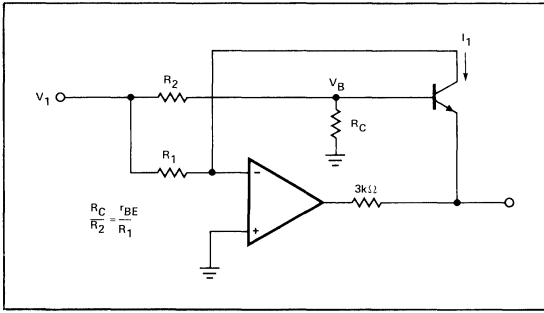


Figure 1. One-Quadrant Multiplier/Divider


Figure 2. Compensation of Bulk Resistance Error

Extrinsic resistive terms and the Early effect cause departure from the ideal logarithmic relationship. For small V_{CB} , all of these effects can be lumped together as a total effective bulk resistance r_{BE} . The $r_{BE}I_C$ term causes departure from the desired logarithmic relationship. The r_{BE} term for the MAT-02 is less than 0.5Ω and Δr_{BE} between the two sides is negligible.

Returning to the multiplier/divider circuit of Figure 1 and using Equation (4):

$$V_{BE1A} + V_{BE2A} - V_{BE2B} - V_{BE1B} + (I_1 + I_2 - I_O - I_3) r_{BE} = 0$$

If the transistor pairs are held to the same temperature, then:

$$\frac{kT}{q} \ln \frac{I_1 I_2}{I_3 I_O} = \frac{kT}{q} \ln \frac{I_{S1A} I_{S2A}}{I_{S1B} I_{S2B}} + (I_1 + I_2 - I_O - I_3) r_{BE} \quad (6)$$

If all the terms on the right-hand side were zero, then we would have $\ln(I_1 I_2 / I_3 I_O)$ equal to zero which would lead directly to the desired result:

$$I_O = \frac{I_1 I_2}{I_3}, \text{ where } I_1, I_2, I_3, I_O > 0 \quad (7)$$

Note that this relationship is temperature independent. The right-hand side of Equation (6) is near zero and the output current I_O will be approximately $I_1 I_2 / I_3$. To estimate error, define ϕ as the right-hand side terms of Equation (6):

$$\phi = \ln \frac{I_{S1A} I_{S2A}}{I_{S1B} I_{S2B}} + \frac{q}{kT} (I_1 + I_2 - I_O - I_3) r_{BE} \quad (8)$$

For the MAT-02, $\ln(I_{SA}/I_{SB})$ and $I_C r_{BE}$ are very small. For small ϕ , $e^\phi \sim 1 + \phi$ and therefore:

$$\begin{aligned} \frac{I_1 I_2}{I_3 I_O} &= 1 + \phi \\ I_O &\sim \frac{I_1 I_2}{I_3} (1 - \phi) \end{aligned} \quad (9)$$

The $\ln(I_{SA}/I_{SB})$ terms in ϕ cause a fixed gain error of less than $\pm 0.6\%$ from each pair when using the MAT-02, and this gain error is easily trimmed out by varying R_O . The $I_C r_{BE}$ terms are more troublesome because they vary with signal levels and are multiplied by absolute temperature. At 25°C , kT/q is

approximately 26mV and the error due to an $r_{BE}I_C$ term will be $r_{BE}I_C/26\text{mV}$. Using an r_{BE} of 0.4Ω for the MAT-02 and assuming a collector-current range of up to $200\mu\text{A}$, then a peak error of 0.3% could be expected for an $r_{BE}I_C$ error term when using the MAT-02. Total error is dependent on the specific application configuration (multiply, divide, square, etc.) and the required dynamic range. An obvious way to reduce $I_C r_{BE}$ error is to reduce the maximum collector current, but then op amp offsets and leakage currents become a limiting factor at low input levels. A design range of no greater than $10\mu\text{A}$ to 1mA is generally recommended for most nonlinear function circuits.

A powerful technique for reducing error due to $I_C r_{BE}$ is shown in Figure 2. A small voltage equal to $I_C r_{BE}$ is applied to the transistor base. For this circuit:

$$V_B = \frac{R_C}{R_2} V_1 \text{ and } I_C r_{BE} = \frac{r_{BE}}{R_1} V_1 \quad (10)$$

The error from $r_{BE}I_C$ is cancelled if R_C/R_2 is made equal to r_{BE}/R_1 . Since the MAT-02 bulk resistance is approximately 0.39Ω , an R_C of 3.9Ω and R_2 of $10R_1$ will give good error cancellation.

In more complex circuits, such as the circuit in Figure 1, it may be inconvenient to apply a compensation voltage to each individual base. A better approach is to sum all compensation to the bases of Q1. The "A" side needs a base voltage of $(V_O/R_O + V_Z/R_3) r_{BE}$ and the "B" side needs a base voltage of $(V_X/R_1 + V_Y/R_2) r_{BE}$. Linearity of better than $\pm 0.1\%$ is readily achievable with this compensation technique.

Operational amplifier offsets are another source of error. In Figure 2, the input offset voltage and input bias current will cause an error in collector current of $(V_{OS}/R_1) + I_B$. A low offset op amp, such as the OP-07 with less than $75\mu\text{V}$ of V_{OS} and I_B of less than $\pm 3\text{nA}$, is recommended. The OP-22/32, a programmable micropower op amp, should be considered if low power consumption or single-supply operation is needed. The value of frequency-compensating capacitor (C_O) is dependent on the op amp frequency response and peak collector current. Typical values for C_O range from 30pF to 300pF .

FOUR-QUADRANT MULTIPLIER

A simplified schematic for a four-quadrant log/antilog multiplier is shown in Figure 3. As with the previously discussed one-quadrant multiplier, the circuit makes $I_O = I_1 I_2 / I_3$. The two input currents, I_1 and I_2 , are each offset in the positive direction. This positive offset is then subtracted out at the output stage. Assuming ideal op amps, the currents are:

$$I_1 = \frac{V_X}{R_1} + \frac{V_R}{R_2}, \quad I_2 = \frac{V_Y}{R_1} + \frac{V_R}{R_2} \quad (11)$$

$$I_O = \frac{V_X}{R_1} + \frac{V_Y}{R_1} + \frac{V_R}{R_2} + \frac{V_O}{R_O}, \quad I_3 = \frac{V_R}{R_2}$$

From $I_O = I_1 I_2 / I_3$, the output voltage will be:

$$V_O = \frac{R_O R_2}{R_1^2} \frac{V_X V_Y}{V_R} \quad (12)$$

 9
MATCHED TRANSISTORS

Collector-current range is the key design decision. The inherently low r_{BE} of the MAT-02 allows the use of a relatively high collector current. For input scaling of $\pm 10V$ full-scale and using a 10V reference, we have a collector-current range for I_1 and I_2 of:

$$\left(\frac{-10}{R_1} + \frac{10}{R_2}\right) \leq I_C \leq \left(\frac{10}{R_1} + \frac{10}{R_2}\right) \quad (13)$$

Practical values for R_1 and R_2 would range from 50k Ω to 100k Ω . Choosing an R_1 of 82k Ω and R_2 of 62k Ω provides a collector-current range of approximately 39 μA to 283 μA . An R_O of 108k Ω will then make the output scale factor 1/10 and $V_O = V_X V_Y / 10$. The output, as well as both inputs, are scaled for $\pm 10V$ full-scale.

Linear error for this circuit is substantially improved by the small correction voltage applied to the base of Q1 as shown in Figure 3. Assuming an equal bulk emitter resistance for each MAT-02 transistor, then the error is nulled if:

$$(I_1 + I_2 - I_3 - I_O) r_{BE} + \rho V_O = 0$$

The currents are known from the previous discussion, and the relationship needed is simply:

$$V_O = \frac{r_{BE}}{R_O} V_O \quad (14)$$

The output voltage is attenuated by a factor of r_{BE}/R_O and applied to the base of Q1 to cancel the summation of voltage drops due to $r_{BE}I_C$ terms. This will make $\ln(I_1 I_2 / I_3 I_O)$ more nearly zero which will thereby make $I_O = I_1 I_2 / I_3$ a more accurate relationship. Linearity of better than 0.1% is readily achievable with this circuit if the MAT-02 pairs are carefully kept at the same temperature.

MULTIFUNCTION CONVERTER

The multifunction converter circuit provides an accurate means of squaring, square rooting, and of raising ratios to arbitrary powers. The excellent log conformity of the MAT-02 allows a wide range of exponents. The general transfer function is:

$$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m \quad (15)$$

V_X , V_Y , and V_Z are input voltages and the exponent "m" has a practical range of approximately 0.2 to 5. Inputs V_X and V_Y are often taken from a fixed reference voltage. With a REF-01 providing a precision +10V to both V_X and V_Y , the transfer function would simplify to:

$$V_O = 10 \left(\frac{V_Z}{10}\right)^m \quad (16)$$

As with the multiplier/divider circuits, assume that the transistor pairs have excellent matching and are at the same temperature. The $\ln I_{SA}/I_{SB}$ will then be zero. In the circuit of Figure 4, the voltage drops across the base-emitter junctions of Q1 provide:

$$\frac{R_B}{R_B + KR_A} V_A = \frac{kT}{q} \ln \frac{I_Z}{I_X} \quad (17)$$

I_Z is V_Z/R_1 and I_X is V_X/R_1 . Similarly, the relationship for Q2 is:

$$\frac{R_B}{R_B + (1-K)R_A} V_A = \frac{kT}{q} \ln \frac{I_O}{I_Y} \quad (18)$$

I_O is V_O/R_O and I_Y is V_Y/R_1 . These equations for Q1 and Q2 can then be combined.

$$\frac{R_B + KR_A}{R_B + (1-K)R_A} \ln \frac{I_Z}{I_X} = \ln \frac{I_O}{I_Y} \quad (19)$$

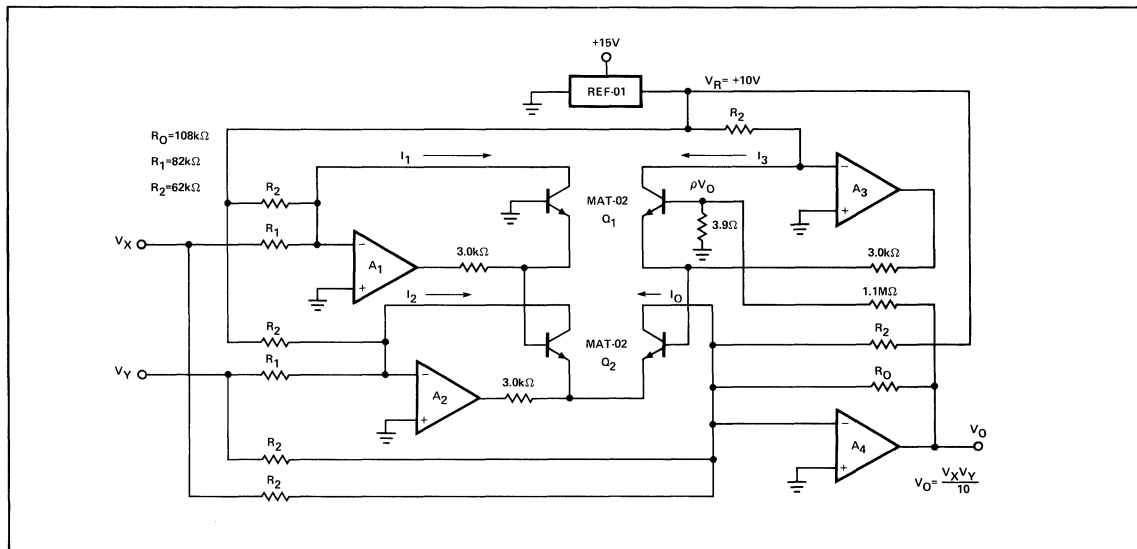


Figure 3. Four-Quadrant Multiplier

Substituting in the voltage relationships and simplifying leads to:

$$V_O = \frac{R_O}{R_1} V_Y \left(\frac{V_Z}{V_X} \right)^m, \text{ where} \quad (20)$$

$$m = \frac{R_B + KR_A}{R_B + (1-K)R_A}$$

The factor "K" is a potentiometer position and varies from zero to 1.0, so "m" ranges from $R_B/(R_A + R_B)$ to $(R_B + R_A)/R_B$. Practical values are 125Ω for R_B and 500Ω for R_A ; these values will provide an adjustment range of 0.2 to 5.0. A value of $100k\Omega$ is recommended for the R_1 resistors assuming a full-scale input range of 10V. As with the one-quadrant multiplier/divider circuit previously discussed, the V_X , V_Y , and V_Z inputs must all be positive.

The op amps should have the lowest possible input offsets. The OP-07 is recommended for most applications, although such programmable micropower op amps as the OP-22 or OP-32 offer advantages in low-power or single-supply circuits. The micropower op amps also have very low input-bias-current drift, an important advantage in log/antilog circuits. External offset nulling may be needed, particularly for applications requiring a wide dynamic range. Frequency-compensating capacitors, on the order of 50pF, may be required for A2 and A3. Amplifier A1 is likely to need a larger capacitor, typically $0.0047\mu F$, to assure stability.

Accuracy is limited at the higher input levels by bulk emitter resistance, but this is much lower for the MAT-02 than for other transistor pairs. Accuracy at the lower signal levels primarily depends on the op amp offsets. Accuracies of

better than 1% are readily achievable with this circuit configuration and can be better than $\pm 0.1\%$ over a limited operating range.

FAST LOGARITHMIC AMPLIFIER

The circuit of Figure 5 is a modification of a standard logarithmic amplifier configuration. Running the MAT-02 at 2.5mA per side (full-scale) allows a fast response with wide dynamic range. The circuit has a 7 decade current range, a 5 decade voltage range, and is capable of 2.5µsec settling time to 1% with a 1 to 10V step.

The output follows the equation:

$$V_O = \frac{R_3 + R_2}{R_2} \frac{kT}{q} \ln \frac{V_{REF}}{V_{in}} \quad (21)$$

The output is inverted with respect to the input, and is nominally -1V/decade using the component values indicated.

LOW-NOISE $\times 1000$ AMPLIFIER

The MAT-02 noise voltage is exceptionally low, only $1nV/\sqrt{Hz}$ at 10Hz when operated over a collector-current range of 1 to 4mA. A single-ended $\times 1000$ amplifier that takes advantage of this low MAT-02 noise level is shown in Figure 6. In addition to low noise, the amplifier has very low drift and high CMRR. An OP-32 programmable low-power op amp is used for the second stage to obtain good speed with minimal power consumption. Small-signal bandwidth is 1MHz, slew-rate is $2.4V/\mu s$, and total supply current is approximately 2.8mA.

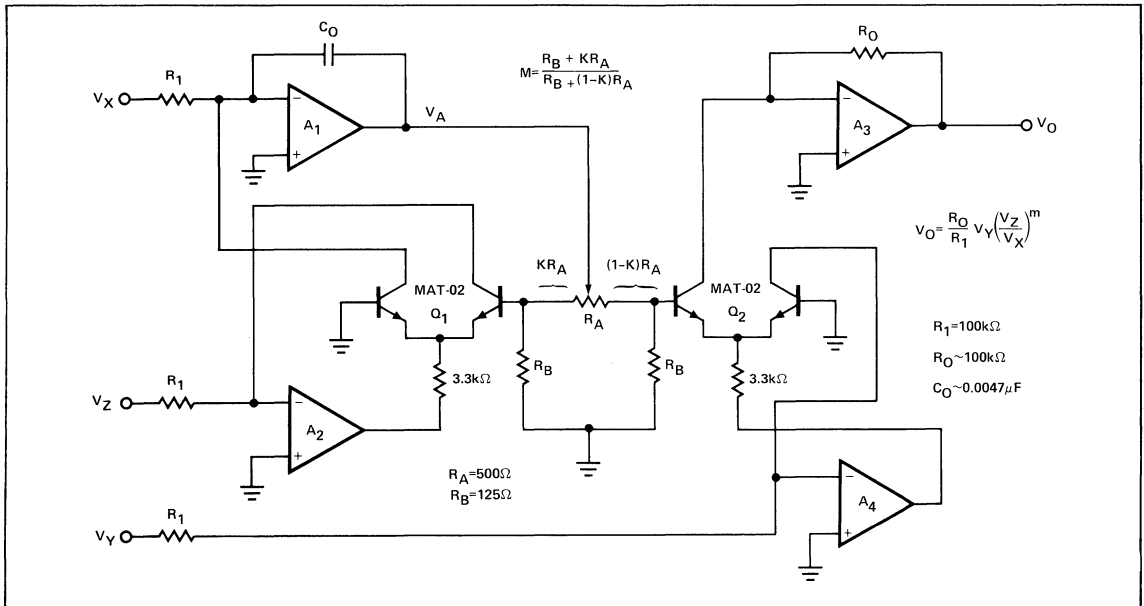


Figure 4. Multifunction Converter



MAT-04

MATCHED MONOLITHIC
QUAD TRANSISTOR

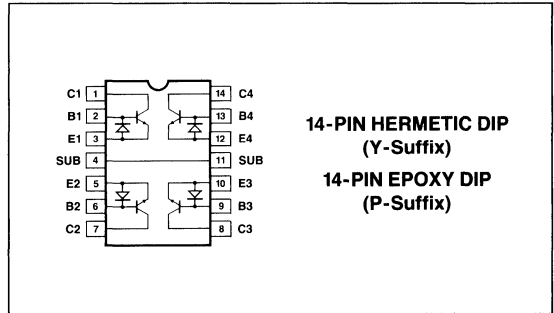
Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Low Offset Voltage 150 μ V Max
- High Current Gain 400 Min
- Excellent Current Gain Match 2% Max
- Low Noise Voltage at 100Hz, 1mA 2.5nV/ $\sqrt{\text{Hz}}$ Max
- Excellent Log Conformance $r_{BE} = 0.6\Omega$ Max
- Matching Guaranteed for All Transistors

PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)

14-PIN EPOXY DIP
(P-Suffix)

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ $V_{OS\text{ MAX}}$ (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC DIP 14-PIN	EPOXY** DIP 14-PIN	
150 μV	MAT04AY*		MIL
150 μV	MAT04EY	MAT04EP	IND
300 μV	MAT04BY*		MIL
300 μV	MAT04FY	MAT04FP	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

**Epoxy packaged devices available in 1st Quarter, 1986.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The MAT-04 is a quad monolithic NPN transistor that offers excellent parametric matching for precision amplifier and non-linear circuit applications. Performance characteristics of the MAT-04 include high gain (400 minimum) over a wide range of collector current, low noise (2.5nV/ $\sqrt{\text{Hz}}$ maximum at 100Hz, $I_C = 1\text{mA}$) and excellent logarithmic conformance. The MAT-04 also features a low offset voltage of 150 μV and tight current gain matching, to within 2%. Each transistor of the MAT-04 is individually tested to data sheet specifications. For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are verified to meet stated limits. Device performance is guaranteed at 25 $^\circ\text{C}$ and over the industrial and military temperature ranges.

The long-term stability of matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias base-emitter current.

The superior logarithmic conformance and accurate matching characteristics of the MAT-04 makes it an excellent choice for use in log and antilog circuits. The MAT-04 is an ideal choice in applications where low noise and high gain are required.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector-Base Voltage (BV_{CBO})	40V
Collector-Emitter Voltage (BV_{CEO})	40V
Collector-Collector Voltage (BV_{CC})	40V
Emitter-Emitter Voltage (BV_{EE})	40V
Collector Current	30mA
Emitter Current	30mA
Substrate (Pin-4 to Pin-11) Current	30mA
Total Power Dissipation (Note 2)	500mW
Operating Temperature Range	
MAT-04AY, BY	-55 $^\circ\text{C}$ to +125 $^\circ\text{C}$
MAT-04EY, FY, EP, FP	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
Storage Temperature	
Y Package	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
P Package	-65 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300 $^\circ\text{C}$

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged devices.
2. The table below lists maximum ambient temperature ratings and derating factors.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100 $^\circ\text{C}$	10mW/ $^\circ\text{C}$
14-Pin Epoxy DIP (P)	42 $^\circ\text{C}$	6mW/ $^\circ\text{C}$

This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS} , I_{OS} , Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04A/E			MAT-04B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 1)	400	800	—	300	600	—	
Current Gain Match	Δh_{FE}	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 2)	—	0.5	2	—	1	4	%
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	50	150	—	100	300	μV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0\text{V}$	—	5	25	—	10	50	μV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	50	100	—	100	200	μV
Bulk Emitter Resistance	r_{BE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0\text{V}$	—	0.4	0.6	—	0.4	0.6	Ω
Input Bias Current	I_B	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	125	250	—	165	330	nA
Input Offset Current	I_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	0.6	5	—	2	13	nA
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu\text{A}$	40	—	—	40	—	—	V
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 100\mu\text{A}$ $I_C = 1\text{mA}$	—	0.03	0.06	—	0.03	0.06	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40\text{V}$	—	5	—	—	5	—	pA
Noise Voltage Density	e_n	$V_{CB} = 0\text{V}$ $f_O = 10\text{Hz}$ $I_C = 1\text{mA}$ $f_O = 100\text{Hz}$ (Note 3) $f_O = 1\text{kHz}$	—	2	3	—	2	4	$\text{nV}/\sqrt{\text{Hz}}$
Gain Bandwidth Product	f_T	$I_C = 1\text{mA}$ $V_{CE} = 10\text{V}$	—	300	—	—	300	—	MHz
Output Capacitance	C_{OBO}	$V_{CB} = 15\text{V}$ $I_E = 0$ $f = 1\text{MHz}$	—	10	—	—	10	—	pF
Input Capacitance	C_{EBO}	$V_{BE} = 0\text{V}$ $I_C = 0$ $f = 1\text{MHz}$	—	40	—	—	40	—	pF

NOTES:

- Current gain measured at $I_C = 10\mu\text{A}$, $100\mu\text{A}$ and 1mA .
- Current gain match is defined as: $\Delta h_{FE} = \frac{100(\Delta I_B)(h_{FE \text{ min}})}{I_C}$
- Sample tested.



ELECTRICAL CHARACTERISTICS at $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS} , I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04E			MAT-04F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 1)	225	625	—	200	500	—	
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	60	210	—	120	420	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$ (Note 2)	—	0.2	1	—	0.4	2	$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current	I_B	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	160	445	—	200	500	nA
Input Offset Current	I_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	4	20	—	8	40	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	50	—	—	100	—	$\text{pA}/^{\circ}\text{C}$
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu\text{A}$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40\text{V}$	—	0.5	—	—	0.5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40\text{V}$	—	5	—	—	5	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40\text{V}$	—	0.7	—	—	0.7	—	nA

ELECTRICAL CHARACTERISTICS at $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS} , I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

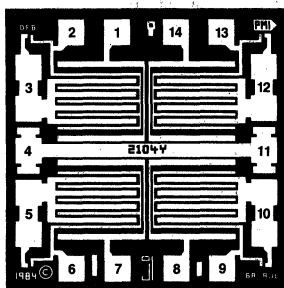
PARAMETER	SYMBOL	CONDITIONS	MAT-04A			MAT-04B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 1)	175	475	—	125	425	—	
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	70	250	—	140	500	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$ (Note 2)	—	0.2	1	—	0.4	2	$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current	I_B	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	210	570	—	235	800	nA
Input Offset Current	I_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	6	30	—	12	60	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	50	—	—	100	—	$\text{pA}/^{\circ}\text{C}$
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu\text{A}$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40\text{V}$	—	5	—	—	5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40\text{V}$	—	100	—	—	100	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40\text{V}$	—	7	—	—	7	—	nA

NOTES:

1. Current gain measured at $I_C = 10\mu\text{A}$, $100\mu\text{A}$ and 1mA .
2. Guaranteed by V_{OS} test ($TCV_{OS} \leq V_{OS}/T$ for $V_{OS} \ll V_{BE}$) $T = 298^{\circ}\text{K}$ for $T_A = 25^{\circ}\text{C}$.



DICE CHARACTERISTICS



DIE SIZE 0.059 × 0.059 inch, 3481 sq. mils
(1.50 × 1.50 mm, 2.25 sq. mm)

1. Q1 COLLECTOR
2. Q1 BASE
3. Q1 EMITTER
4. SUBSTRATE
5. Q2 EMITTER
6. Q2 BASE
7. Q2 COLLECTOR
8. Q3 COLLECTOR
9. Q3 BASE
10. Q3 EMITTER
11. SUBSTRATE
12. Q4 EMITTER
13. Q4 BASE
14. Q4 COLLECTOR

For additional DICE information refer to
1986 Data Book, Section 2.

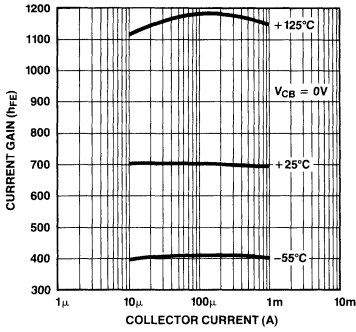
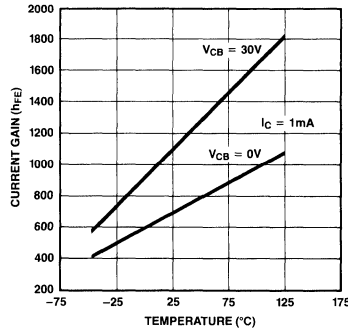
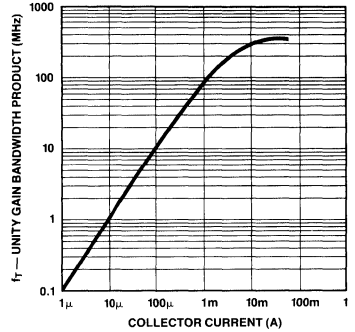
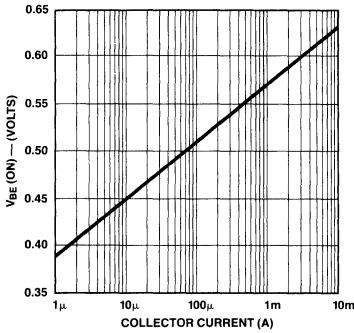
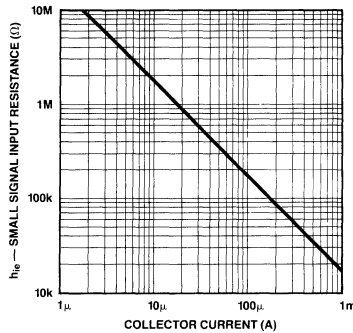
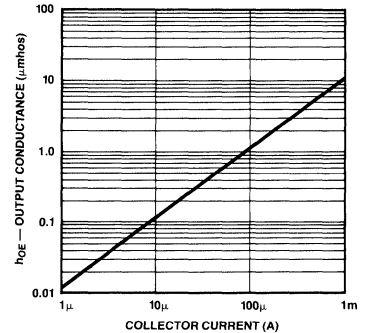
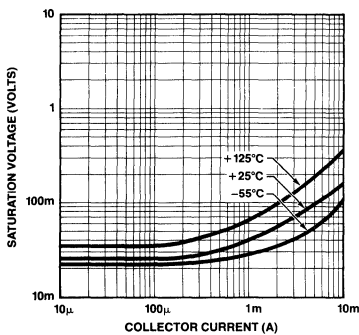
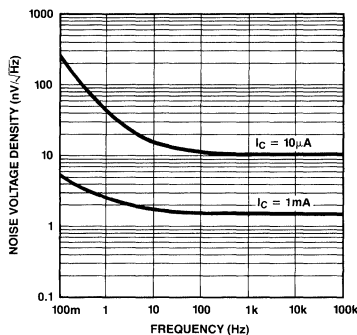
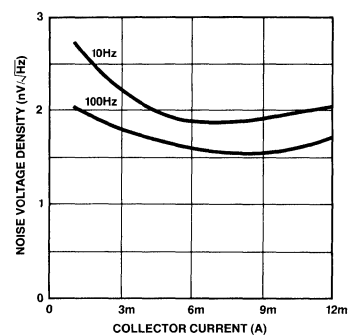
WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS} , I_{OS} , Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04N LIMITS	UNITS
Current Gain	h_{FE}	$I_C = 100\mu\text{A}$ $0V \leq V_{CB} \leq 30V$	300	MIN
Current Gain Match	Δh_{FE}	$I_C = 100\mu\text{A}$, $V_{CB} = 0V$	4	% MAX
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0V \leq V_{CB} \leq 30V$	300	μV MAX
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0V$	50	μV MAX
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0V \leq V_{CB} \leq 30V$	200	μV MAX
Bulk Emitter Resistance	r_{BE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0V$	0.6	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 100\mu\text{A}$ $I_C = 1\text{mA}$	0.06	V MAX
Input Bias Current	I_B	$I_C = 100\mu\text{A}$ $0V \leq V_{CB} \leq 30V$	330	nA MAX
Input Offset Current	I_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0V$	13	nA MAX
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu\text{A}$	40	V MIN

NOTE:

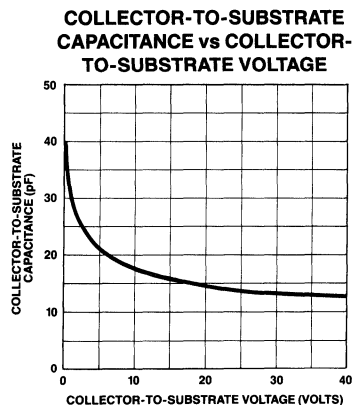
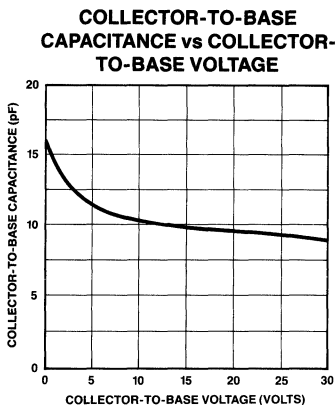
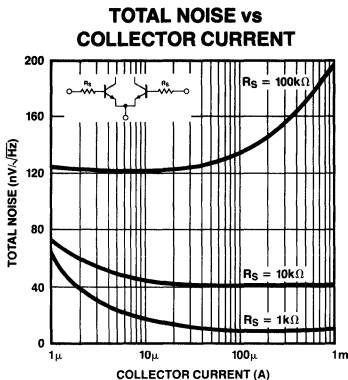
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

CURRENT GAIN vs COLLECTOR CURRENT

CURRENT GAIN vs TEMPERATURE

GAIN BANDWIDTH vs COLLECTOR CURRENT

BASE-EMITTER-ON-VOLTAGE vs COLLECTOR CURRENT

SMALL SIGNAL INPUT RESISTANCE (h_{ie}) vs COLLECTOR CURRENT

SMALL SIGNAL OUTPUT CONDUCTANCE vs COLLECTOR CURRENT

SATURATION VOLTAGE vs COLLECTOR CURRENT

NOISE VOLTAGE vs FREQUENCY

NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT


MATCHED TRANSISTORS

TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATION NOTES

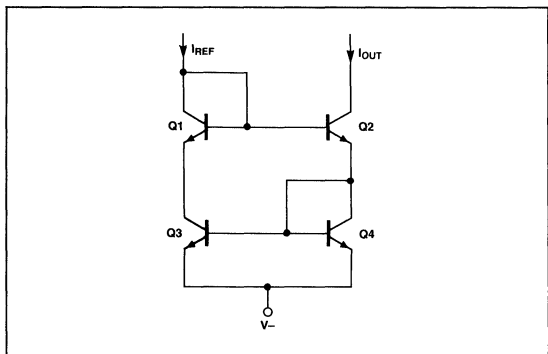
It is recommended that one of the substrate pins (Pins 4 and 11) be tied to the most negative circuit potential to minimize coupling between devices. Pins 4 and 11 are internally connected.

APPLICATIONS

CURRENT SOURCES

The MAT-04 can be used to implement a variety of high impedance current mirrors as shown in Figures 1, 2, and 3. These current mirrors can be used as biasing elements and load devices for amplifier stages.

FIGURE 1: Unity Gain Current Mirror, $I_{OUT} = I_{REF}$



The unity-gain current mirror of Figure 1, using a MAT-04AY, has an accuracy of better than 1% and an output impedance of over 100MΩ at 100μA. Figures 2 and 3 show modified current mirrors designed for a current gain of two, and one-half respectively. The accuracy of these mirrors is reduced from that of the unity-gain source due to base current errors but is still better than 2%.

FIGURE 2: Current Mirror, $I_{OUT} = 2 (I_{REF})$

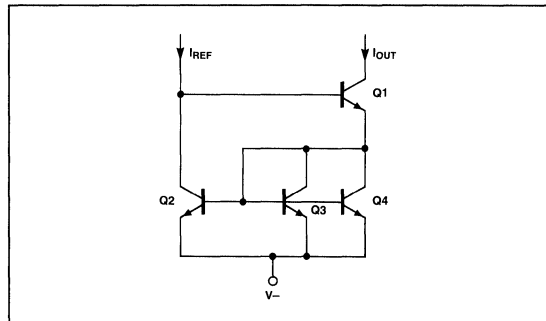


FIGURE 3: Current Mirror, $I_{OUT} = 1/2 (I_{REF})$

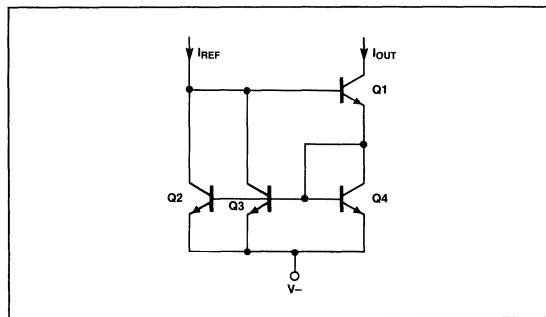
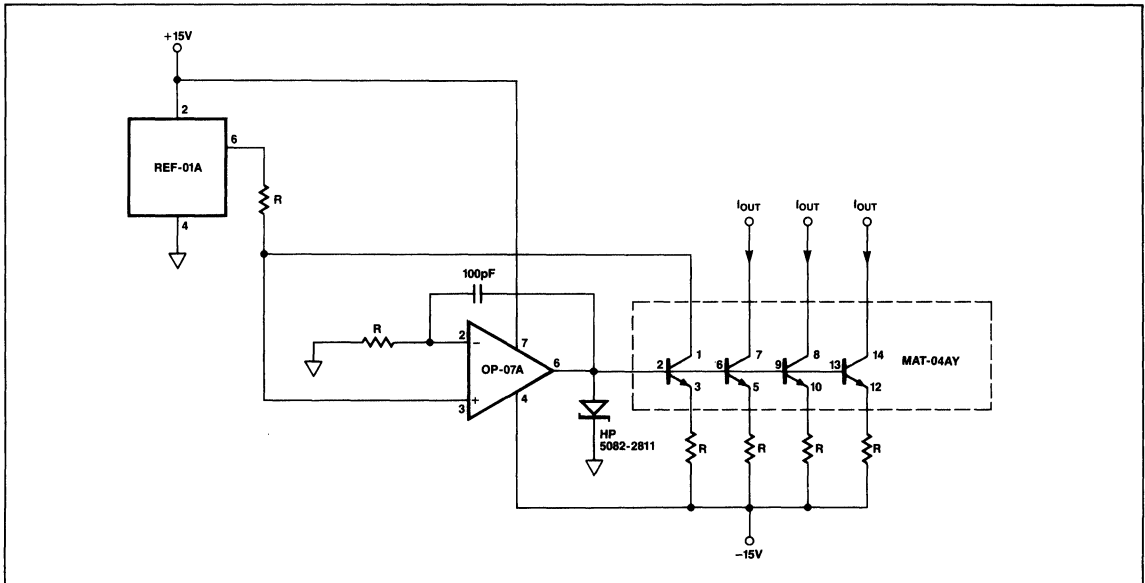


Figure 4 is a temperature independent current sink that has an accuracy of better than 1% over the military temperature range at an output current of 100μA to 1mA. The Schottky diode acts as a clamp to insure correct circuit start-up at power on. The resistors used in this circuit should be 1% metal-film type.

FIGURE 4: Temperature Independent Current Sink, $I_{OUT} = 10V/R\Omega$


NONLINEAR FUNCTIONS

An application where precision matched-transistors are a powerful tool is in the generation of nonlinear functions. These circuits are based on the transistor's logarithmic property which takes the following idealized form:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S}$$

The MAT-04, with its excellent logarithmic conformance, maintains this idealized function over many decades of collector current. This, in addition to the stringent parametric matching of the MAT-04, enables the implementation of extremely accurate log/antilog circuits.

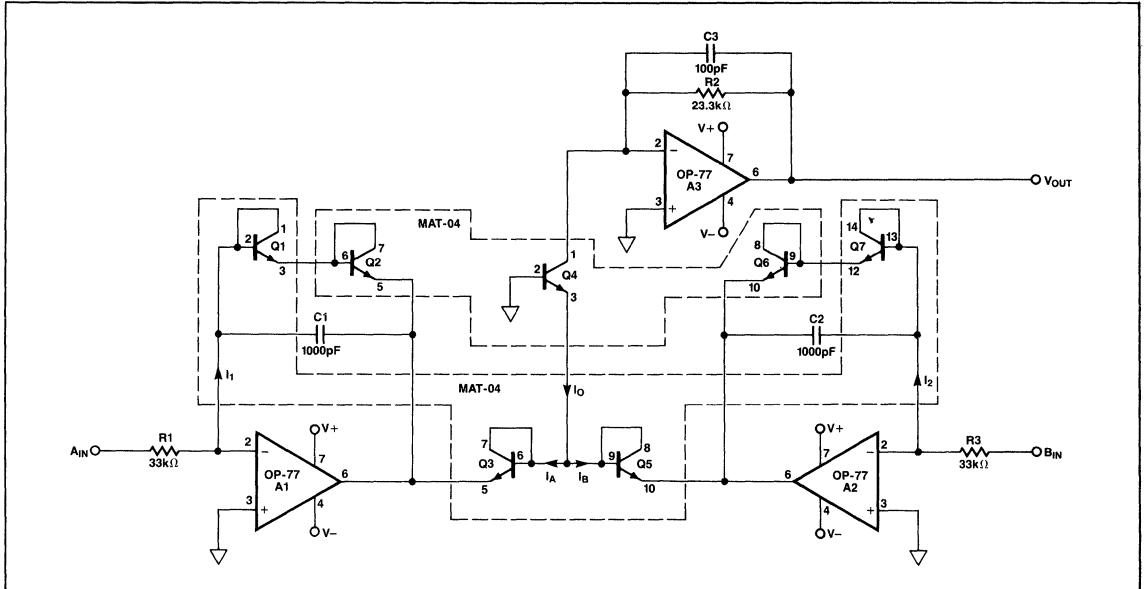
The circuit of Figure 5 is a vector summer that adds and subtracts logged inputs to generate the following transfer function:

$$V_{OUT} = \frac{1}{\sqrt{2}} \sqrt{V_A^2 + V_B^2}$$

This circuit uses two MAT-04AYs and maintains an accuracy of better than 0.5% over an input range of 10mV to 10V. The layout of the MAT-04s reduces errors due to matching and temperature differences between the two precision quad matched-transistors.

Op amps A1 and A2 translate the input voltages into logarithmic valued currents (I_A and I_B in Figure 5) that flow through transistor Q_3 and Q_5 . These currents are summed by transistor Q_4 ($I_O = I_A + I_B = \sqrt{I_1^2 + I_2^2}$) which feeds the current-to-voltage converter consisting of op amp A3. To maintain accuracy, 1% metal-film resistors should be used.



FIGURE 5: Vector Summer

LOW NOISE, HIGH SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 6 is a very low noise, high speed amplifier, ideal for use in precision transducer and professional audio applications. The performance of the amplifier is summarized in Table I. Figure 7 shows the input referred spot noise over the 0-25kHz bandwidth to be flat at $1.2\text{nV}/\sqrt{\text{Hz}}$. Figure 8 highlights the low $1/f$ noise corner at 2Hz.

The circuit uses a high speed op amp, the OP-17, preceded by an input amplifier. This consists of a precision dual matched-transistor, the MAT-02, and a feedback V-to-I converter, the MAT-04. The arrangement of the MAT-04 is known as a "linearized cross quad" which performs the voltage-to-current conversion. The OP-17 acts as an overall nulling amplifier to complete the feedback loop. Resistors R1, R2, and R3, R4 form voltage dividers that attenuate the output voltage swing since the "cross quad" arrangement has a limited input range. Biasing for the input stage is set by zener diode Z1. At low currents the effective zener voltage is about 3.3V due to the soft knee characteristic of the zener diode. This results in a bias current of $530\mu\text{A}$ per side for the input stage. The gain equation for this amplifier is:

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(\frac{R_{10} R_{11}}{R_{10} + R_{11}} \right) \left(\frac{R_4 + R_3}{R_3} \right) \frac{1}{R_G}$$

and for the values shown in Figure 6 this equation becomes:

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{33000}{R_G}$$

TABLE I: Instrumentation Amplifier Characteristics

Input Noise	G = 1000	$1.2\text{nV}/\sqrt{\text{Hz}}$
Voltage Density	G = 100	$3.6\text{nV}/\sqrt{\text{Hz}}$
	G = 10	$30\text{nV}/\sqrt{\text{Hz}}$
Bandwidth	G = 500	400kHz
	G = 100	1MHz
	G = 10	1.2MHz
Slew Rate		$40\text{V}/\mu\text{s}$
Common-Mode Rejection	G = 1000	130dB
Distortion	G = 100 $f = 20\text{Hz to } 20\text{kHz}$	0.03%
Settling Time	G = 1000	$10\mu\text{s}$
Power Consumption		350mW

FIGURE 6: Low Noise, High Speed Instrumentation Amplifier

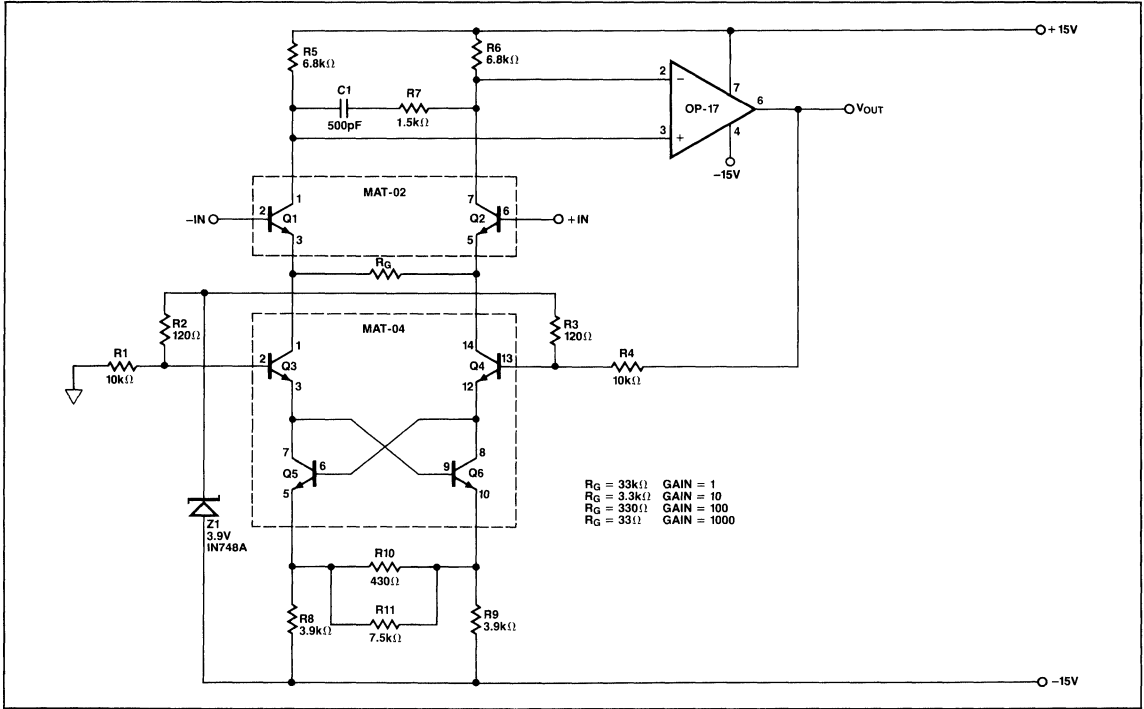


FIGURE 7: Spot Noise of the Instrumentation Amplifier from 0-25kHz at a Gain of 1000

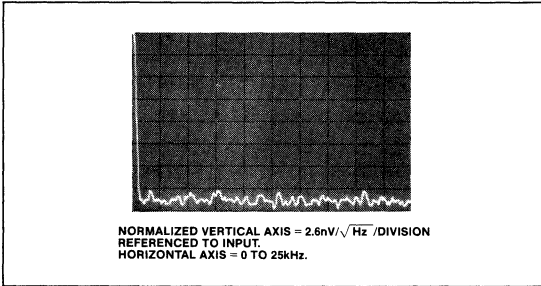


FIGURE 8: Low Frequency Noise Spectrum Showing Low 2Hz Noise Corner. Gain = 1000.

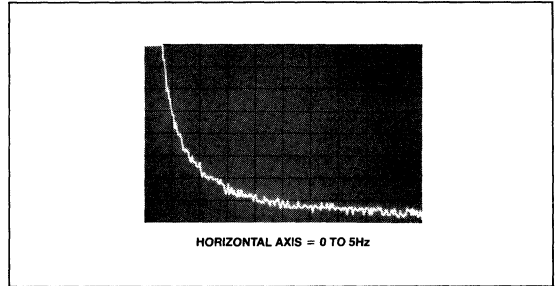
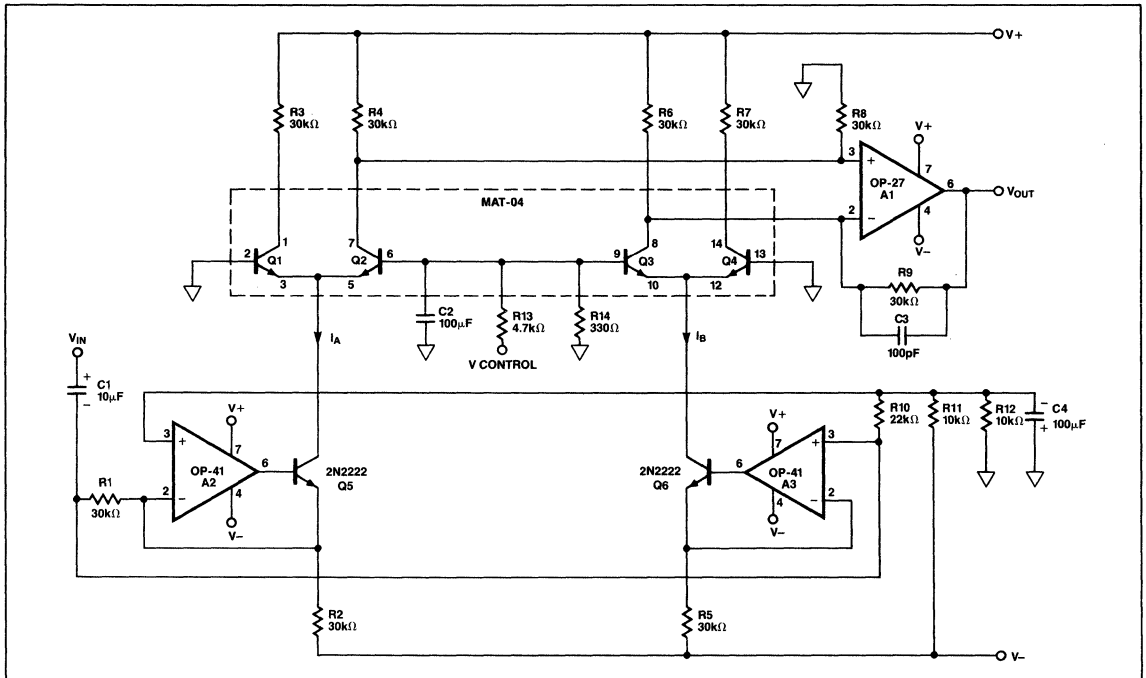


FIGURE 9: Voltage-Controlled Attenuator

VOLTAGE-CONTROLLED ATTENUATOR

The voltage-controlled attenuator (VCA) of Figure 9, widely used in professional audio circles, can easily be implemented using a MAT-04. The excellent matching characteristics of the MAT-04 enables the VCA to have a distortion level of under 0.03% over a wide range of control voltages. The VCA accepts a 3V RMS input and easily handles the full 20Hz-20kHz audio bandwidth as shown in Figure 10. Noise level for the VCA is more than 110dB below maximum output.

In the voltage-controlled attenuator, the input signal modulates the stage current of each differential pair. Op amps A2 and A3 in conjunction with transistors Q5 and Q6 form voltage-to-current converters that transform a single input voltage into differential currents which form the stage currents of each differential pair. The control voltage shifts the current between each side of the two differential pairs, regulating the signal level reaching the output stage which consists of op amp A1. Figure 11 shows the increase in signal attenuation as the control voltage becomes more negative.

The ideal transfer function for the voltage-controlled attenuator is:

$$V_{OUT}/V_{IN} = \frac{2}{1 + \exp\left((-V_{control})\left(\frac{R_{14}}{R_{13} + R_{14}}\right)\left(\frac{kT}{q}\right)\right)}$$

Where k = Boltzmann constant $1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$
 T = temperature in $^\circ\text{K}$
 q = electronic charge = $1.602 \times 10^{-19} \text{ C}$

From the transfer function it can be seen that the maximum gain of the circuit is 2 (6dB).

To insure best performance, resistors R2 through R7 should be 1% metal film resistors. Since capacitor C2 can see small amounts of reverse bias when the control voltage is positive, it may be prudent to use a nonpolarized tantalum capacitor.

FIGURE 10: Voltage-Controlled Attenuator,
Attenuation vs Frequency

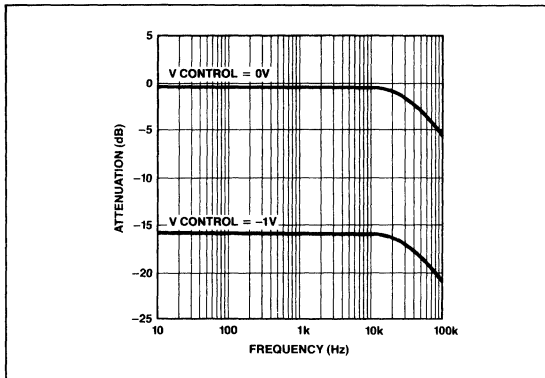


FIGURE 11: Voltage-Controlled Attenuator,
Attenuation vs Control Voltage

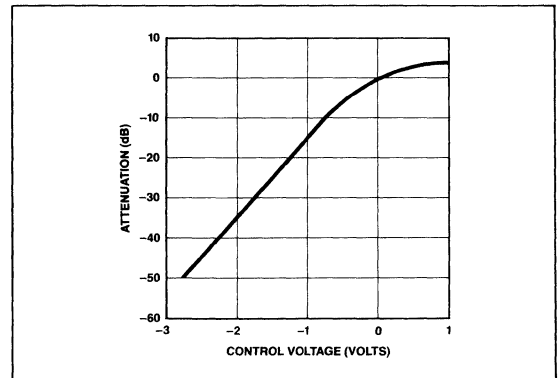


Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



VOLTAGE REFERENCES

Precision Monolithics Inc.

10-3 Introduction

10-3 Definitions

10-4 **REF-01**

+10V Precision Voltage Reference

10-11 **REF-02**

+5V Precision Voltage
Reference/Temperature Transducer

10-19 **REF-03**

+2.5V Precision Voltage Reference

10-21 **REF-05**

+5V Precision Voltage Reference

10-22 **REF-10**

+10V Precision Voltage Reference

INTRODUCTION

Voltage references provide a constant output voltage irrespective of changes in input voltage, output current, or temperature. References are needed in such diverse equipment as power supplies, panel meters, calibration standards, precision current sources, data conversion systems, and control set-point circuits.

Line regulation, load regulation (output impedance), and temperature coefficient specifications indicate how close a reference will be to an ideal voltage source. Line regulation specifies reference-output-voltage vs. input-voltage changes. Output voltage changes due to load current variations are reflected by load regulation specifications. Temperature coefficient specifications indicate output voltage variation over temperature.

PMI references use the bandgap principle which sums voltages with negative and positive temperature coefficients to yield a stable output voltage over temperature. A transistor base-emitter-junction voltage (V_{BE}) exhibits a negative temperature coefficient. Two transistors operating with unequal current densities will have different V_{BE} s and the difference, ΔV_{BE} , exhibits a positive temperature coefficient. When ΔV_{BE} is amplified and added to V_{BE} , a near-zero temperature coefficient results if the sum equals 1.23V. The 1.23V level is then amplified to provide stable output voltages of +5.00V or +10.00V. The bandgap technique has the advantages of low power consumption, low noise, and excellent long-term stability.

PMI's zener-zapping technique allows for trimming of the ΔV_{BE} amplification factor to ensure low output voltage temperature coefficients. Additional zapping trims the output's absolute value to within specified limits.

The REF-01 and REF-02 are stable +10.00V and +5.00V monolithic bandgap voltage references. Output voltages are adjustable with small effect on output-voltage temperature coefficients. The REF-02 provides an additional output voltage that has a linear temperature dependence.

The REF-05 and REF-10 are premium versions of the REF-01 and REF-02 that have guaranteed long-term stability and MIL-STD-883 process-

ing. Extensive testing over a long period of time, combined with tight control of processing, has enabled PMI to specify limits on output change with time.

DEFINITIONS

Line Regulation — The ratio of the change in output voltage to the change in input (line) voltage producing it. It includes the effects of self-heating.

Load Regulation — The ratio of the change in output voltage to the change in load current. It includes the effects of self-heating.

Output Change With Temperature (ΔV_{OT}) — The absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of the typical output voltage.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{V_O \text{ (Typical)}} \right| \times 100$$

Output Temperature Coefficient (TCV_O) — The ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C. For example, TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e.,

$$TCV_O(0^\circ\text{C to } +70^\circ\text{C}) = \frac{\Delta V_{OT}(0^\circ\text{C to } +70^\circ\text{C})}{70^\circ\text{C}}$$

$$\text{and } TCV_O(-55^\circ\text{C to } +125^\circ\text{C}) =$$

$$\frac{\Delta V_{OT}(-55^\circ\text{C to } +125^\circ\text{C})}{180^\circ\text{C}}$$

Output Turn-On Settling Time (t_{ON}) — The time required for the output voltage to reach its final value within a specified error band after application of V_{IN} .

Output Voltage Noise (e_{np-p}) — The peak-to-peak output noise voltage within a specified frequency band.

Quiescent Supply Current (I_{SQ}) — The current required from the supply to operate the device with no load.

Precision Monolithics Inc.

FEATURES

- 10 Volt Output $\pm 0.3\%$ Max
- Adjustment Range $\pm 3\%$ Min
- Excellent Temperature Stability $8.5\text{ppm}/^\circ\text{C}$ Max
- Low Noise $30\mu\text{V}_{\text{p-p}}$ Max
- Low Supply Current 1.4mA Max
- Wide Input Voltage Range 13V to 33V
- High Load-Driving Capability 20mA
- No External Components
- Short-Circuit Proof
- MIL-STD-883 Screening Available

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ ΔV_O MAX (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	PLASTIC DIP 8-PIN	PLASTIC DIP 8-PIN	LCC	
± 30	REF01AJ*	REF01AZ*			MIL
± 30	REF01EJ	REF01EZ			COM
± 50	REF01J*	REF01Z*		REF01RC/883	MIL
± 50	REF01HJ	REF01HZ	REF01HP		COM
± 100	REF01CJ	REF01CZ	REF01CP		COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

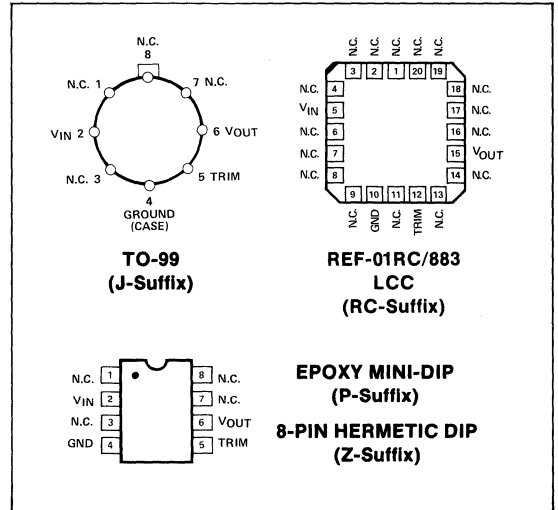
†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

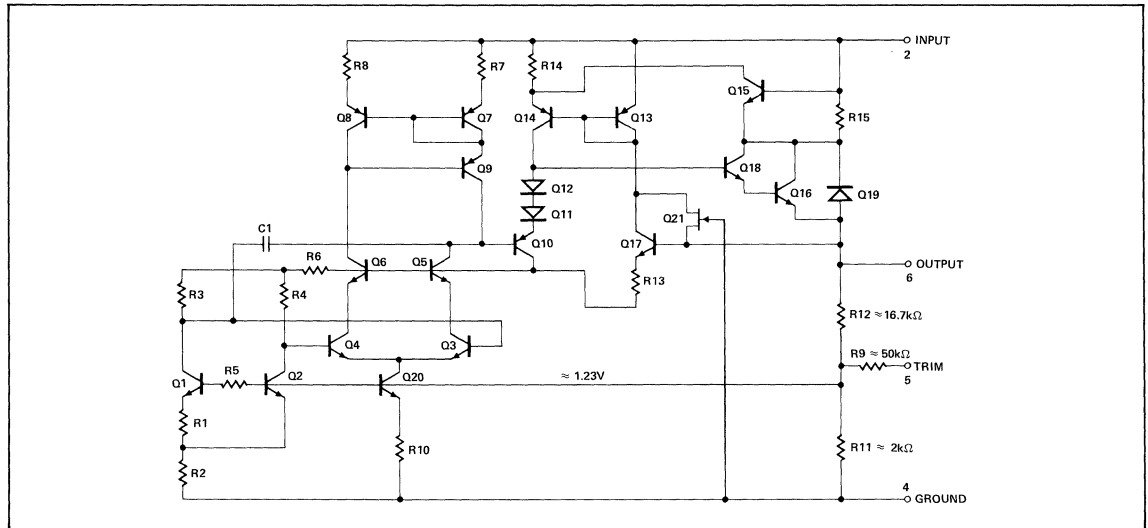
The REF-01 precision voltage reference provides a stable +10V output which can be adjusted over a $\pm 3\%$ range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 12V to 40V, low current

drawn of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-01 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. Full military temperature range devices with screening to MIL-STD-883 are available. For guaranteed long-term drift see the REF-10 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Input Voltage	
REF-01, A, E, H, RC, All DICE	40V
REF-01C	30V
Power Dissipation (Note 1)	500mW
Output Short-Circuit Duration (to Ground or V_{IN})	Indefinite
Storage Temperature Range	
J, RC, and Z Packages	-65° C to +150° C
P Package	-65° C to +125° C
Operating Temperature Range	
REF-01A, REF-01, REF-01RC	-55° C to +125° C
REF-01E, REF-01H,	
REF-01C	0° C to +70° C

DICE Junction Temperature (T_J) -65° C to +150° C
 Lead Temperature (Soldering, 60 sec.) 300° C

NOTES:

- See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C
8-Pin Plastic DIP (P)	36° C	5.6mW/° C
LCC (RC)	72° C	7.8mW/° C

- Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25° C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01A/E			REF-01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0$	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	$R_D = 10k\Omega$	± 3.0	± 3.3	—	± 3.0	± 3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	20	30	—	20	30	μV_{p-p}
Line Regulation (Note 4)		$V_{IN} = 13V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		$I_L = 0$ to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To $\pm 0.1\%$ of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55° C \leq T_A \leq +125° C$ and $I_L = 0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01A/E			REF-01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 1, 2)	ΔV_{OT}	$0° C \leq T_A \leq +70° C$	—	0.02	0.06	—	0.07	0.17	%
		$-55° C \leq T_A \leq +125° C$	—	0.06	0.15	—	0.18	0.45	
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/° C
Change in V_O Temperature Coefficient with Output Adjustment		$R_D = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 13V$ to 33V) (Note 4)		$0° C \leq T_A \leq +70° C$	—	0.007	0.012	—	0.007	0.012	%/V
		$-55° C \leq T_A \leq +125° C$	—	0.009	0.015	—	0.009	0.015	
Load Regulation ($I_L = 0$ to 8mA) (Note 4)		$0° C \leq T_A \leq +70° C$	—	0.006	0.010	—	0.007	0.012	%/mA
		$-55° C \leq T_A \leq +125° C$	—	0.007	0.012	—	0.009	0.015	

NOTES:

- ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

- ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
- TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O (0° \text{ to } +70° C) = \frac{\Delta V_{OT} (0° \text{ to } +70° C)}{70° C}$$

$$\text{and } TCV_O (-55° \text{ to } +125° C) = \frac{\Delta V_{OT} (-55° \text{ to } +125° C)}{180° C}$$

- Line and Load Regulation specifications include the effect of self heating.
- Guaranteed by design.
- Sample tested.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C			UNITS
			MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0mA$	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	± 2.7	± 3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	25	35	μV_{p-p}
Line Regulation (Note 4)		$V_{IN} = 13V$ to 30V	—	0.009	0.015	%/V
Load Regulation (Note 4)		$I_L = 0$ to 8mA $I_L = 0$ to 4mA	—	0.006	0.015	%/mA
Turn-on Settling Time	t_{ON}	To $\pm 0.1\%$ of final value	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S		-0.2	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	mA

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C			UNITS
			MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	20	65	ppm/ $^\circ C$
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	ppm/%
Line Regulation (Note 4)		$V_{IN} = 13V$ to 30V	—	0.011	0.018	%/V
Load Regulation (Note 4)		$I_L = 0$ to 5mA	—	0.008	0.018	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.

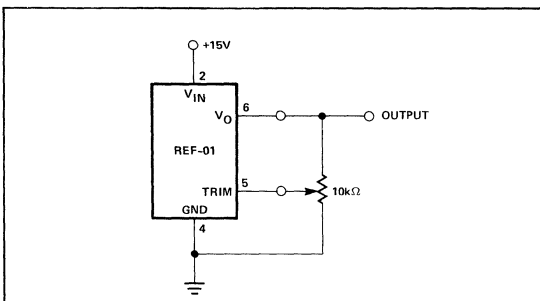
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70^\circ C}$$

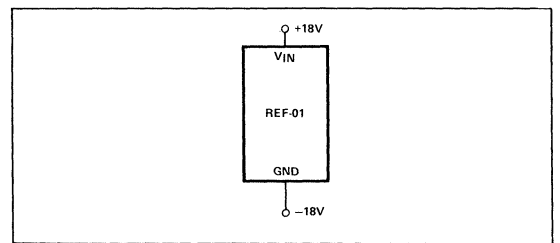
4. Line and Load Regulation specifications include the effect of self heating.

5. Guaranteed by design.

6. Sample tested.

OUTPUT ADJUSTMENT


The REF-01 trim terminal can be used to adjust the output voltage over a $10V \pm 300mV$ range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can

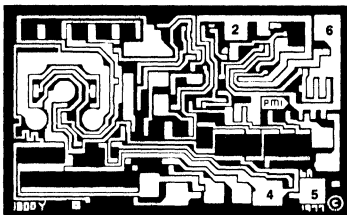
BURN-IN CIRCUIT


also be set to exactly 10.000V, or to 10.240V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/ $^\circ C$ for 100mV of output adjustment.



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

DIE SIZE 0.063 × 0.040 inch, 2520 sq. mils
(1.60 × 1.02 mm, 1.63 sq. mm)

2. INPUT VOLTAGE (V_{IN})
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_{IN} = +15V$, $T_A = 25^\circ C$ for REF-01N and REF-01G devices; $T_A = 125^\circ C$ for REF-01NT and REF-01GT devices, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	REF-01NT LIMIT	REF-01N LIMIT	REF-01GT LIMIT	REF-01G LIMIT	UNITS
Output Voltage	V_O	$I_L = 0$	10.05	10.03	10.10	10.05	V MAX
			9.95	9.97	9.90	9.95	V MIN
Output Adjustment Range	V_{trim}	$R_P = 10k\Omega$	—	± 3.0	—	± 3.0	% MIN
Line Regulation		$V_{IN} = 13V$ to $33V$	0.015	0.01	0.015	0.01	%/V MAX

NOTE:

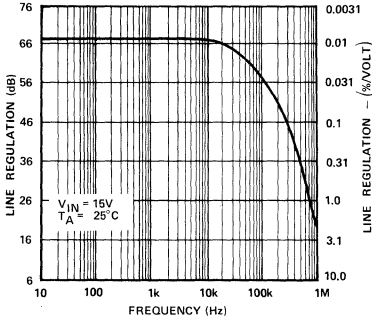
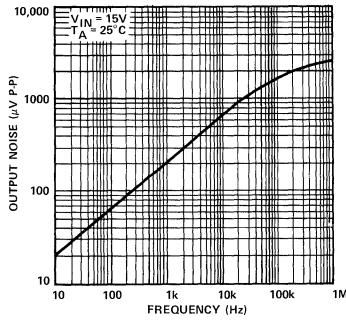
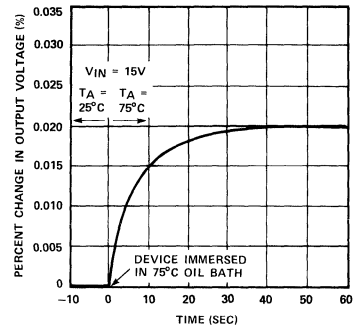
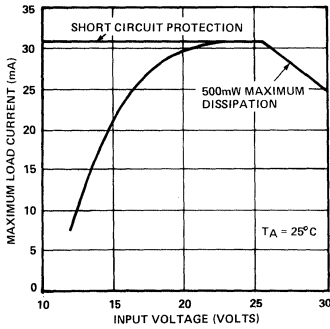
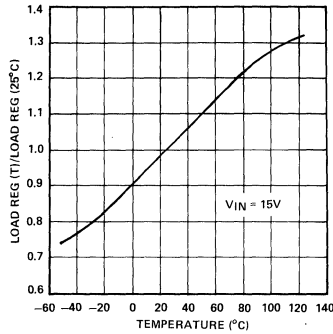
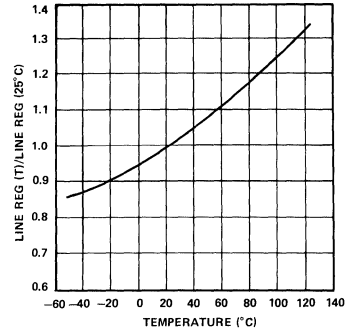
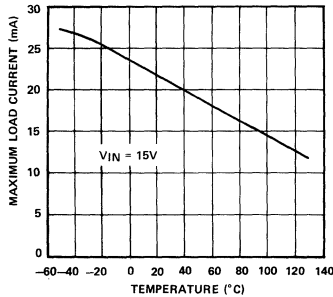
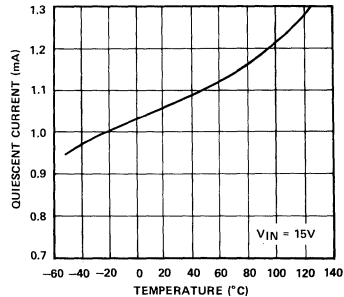
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01NT TYPICAL	REF-01N TYPICAL	REF-01GT TYPICAL	REF-01G TYPICAL	UNITS
Load Regulation		$I_L = 0$ to $10mA$	0.007	0.005	0.009	0.006	%/mA
		$I_L = 0$ to $8mA$, NT, GT @ $+125^\circ C$					
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	20	20	20	20	μV_{p-p}
Turn-On Settling Time	t_{ON}	To $\pm 0.1\%$ of Final Value NT, GT @ $+125^\circ C$	7.5	5.0	7.5	5.0	μs
Quiescent Current	I_{SY}	No Load, NT, GT @ $+125^\circ C$	1.4	1.0	1.4	1.0	mA
Load Current	I_L		21	21	21	21	mA
Sink Current	I_S		-0.5	-0.5	-0.5	-0.5	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	30	30	30	30	mA
Output Voltage Temperature Coefficient	TCV_O		10	10	10	10	ppm/ $^\circ C$

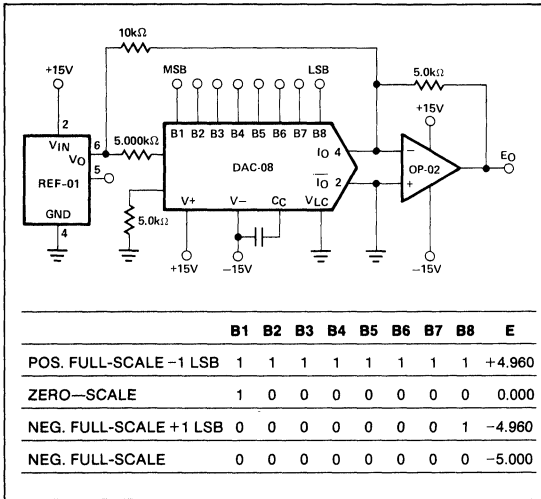
NOTE:

1. For $+25^\circ C$ specifications of REF-01NT and REF-01GT, see REF-01N and REF-01G respectively.

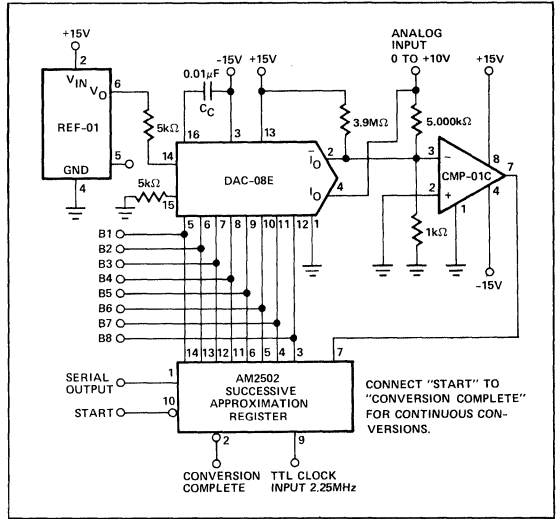
TYPICAL PERFORMANCE CHARACTERISTICS
LINE REGULATION vs FREQUENCY

OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

OUTPUT CHANGE DUE TO THERMAL SHOCK

MAXIMUM LOAD CURRENT vs INPUT VOLTAGE

NORMALIZED LOAD REGULATION ($\Delta I_L = 10mA$) vs TEMPERATURE

NORMALIZED LINE REGULATION vs TEMPERATURE

MAXIMUM LOAD CURRENT vs TEMPERATURE

QUIESCENT CURRENT vs TEMPERATURE


TYPICAL APPLICATIONS

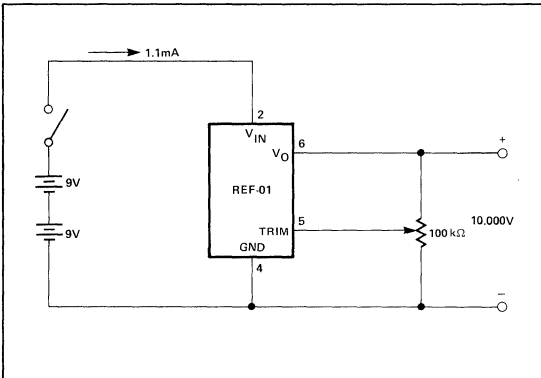
D/A CONVERTER REFERENCE



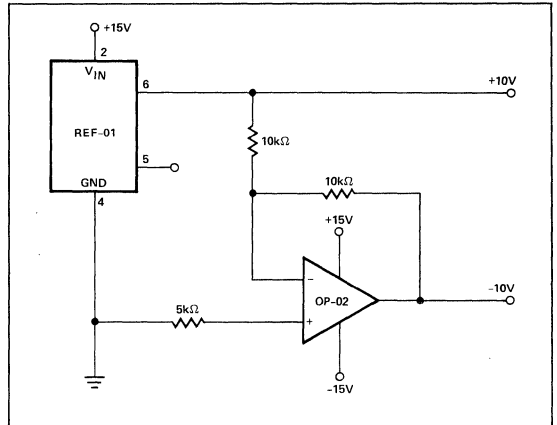
A/D CONVERTER REFERENCE



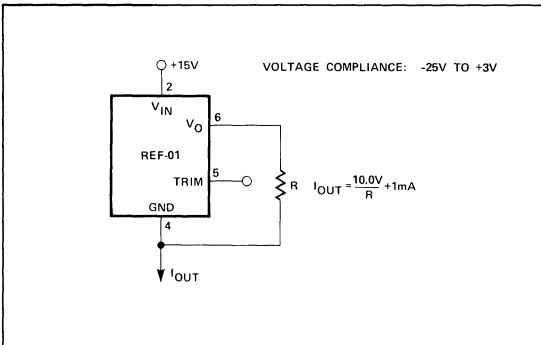
PRECISION CALIBRATION STANDARD



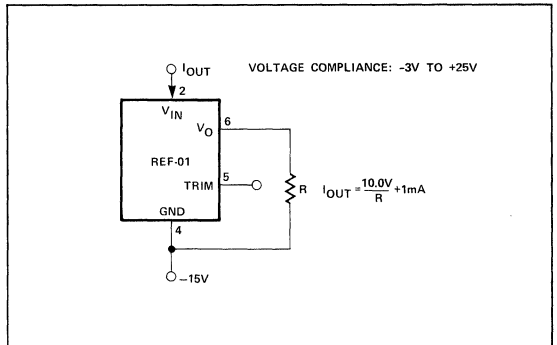
±10V REFERENCE



CURRENT SOURCE



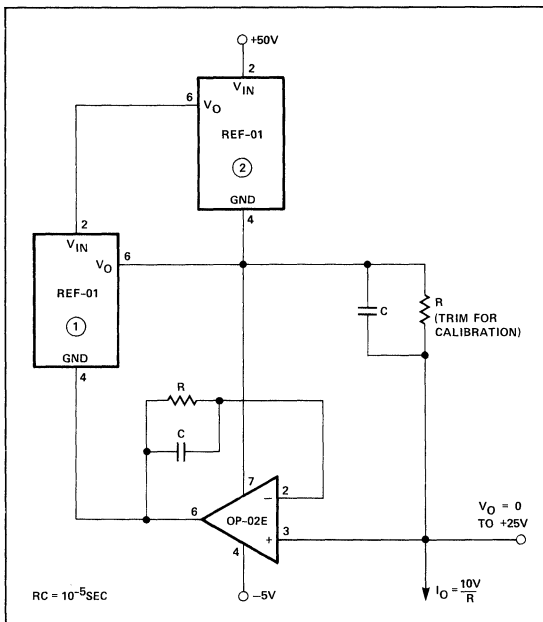
CURRENT SINK



PRECISION CURRENT SOURCE

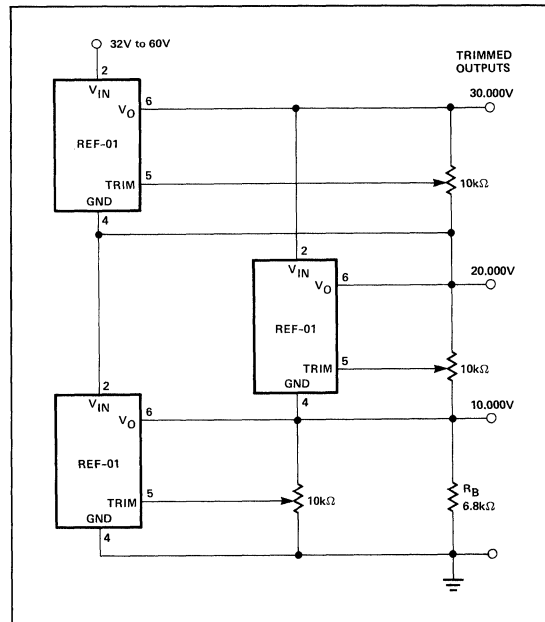
A current source with 25V output compliance and excellent output impedance can be obtained using this circuit. REF-01 (2) keeps the line voltage and power dissipation constant in device (1); the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical $3\mu\text{V}/\text{V}$ PSRR of the OP-02E will create an 8ppm change ($3\mu\text{V}/\text{V} \times 25\text{V}/10\text{V}$) in output current over a 25V range. For example, a 10mA current source can be built ($R = 1\text{k}\Omega$) with $300\text{M}\Omega$ output impedance.

$$R_O = \frac{25\text{V}}{8 \times 10^{-6} \times 10\text{mA}}$$


REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF-01's can be stacked to yield 10,000, 20,000, and 30,000V outputs. An additional advantage is near-perfect line regulation of the 10.0V and 20.0V output. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 20,000V regulator.

In general, any number of REF-01's can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30 . . . 100V. The line voltage can range from 105V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).





REF-02

+5V PRECISION VOLTAGE REFERENCE/TEMPERATURE TRANSDUCER

Precision Monolithics Inc.

FEATURES

- 5 Volt Output $\pm 0.3\%$ Max
- Temperature Voltage Output $2.1\text{mV}/^\circ\text{C}$
- Adjustment Range $\pm 3\%$ Min
- Excellent Temperature Stability $8.5\text{ppm}/^\circ\text{C}$ Max
- Low Noise $15\mu\text{V}_{\text{p-p}}$ Max
- Low Supply Current 1.4mA Max
- Wide Input Voltage Range 8V to 33V
- High Load-Driving Capability 20mA
- No External Components
- Short-Circuit Proof
- MIL-STD-883 Screening Available

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ ΔV_O MAX (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	LCC	
± 15	REF02AJ*	REF02AZ*			MIL
± 15	REF02EJ	REF02EZ			COM
± 25	REF02J*	REF02Z*		REF02RC/883	MIL
± 25	REF02HJ	REF02HZ	REF02HP		COM
± 50	REF02CJ	REF02CZ	REF02CP		COM
± 100	REF02DJ	REF02DZ	REF02DP		COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

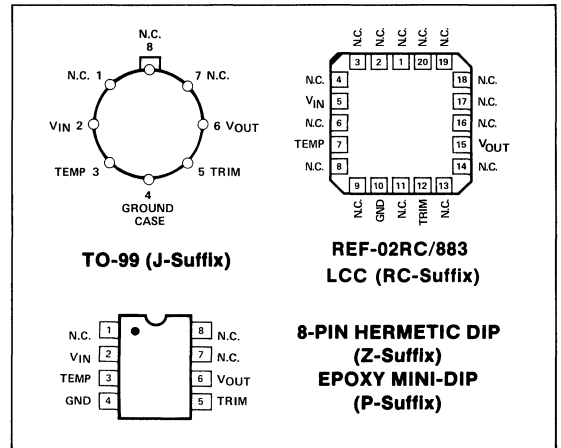
† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

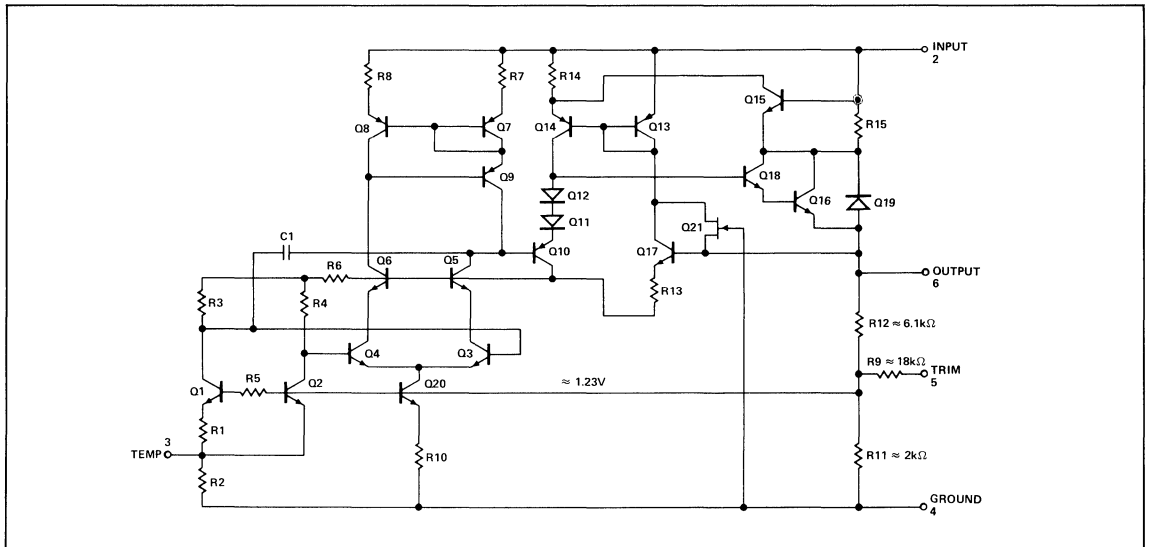
The REF-02 precision voltage reference provides a stable +5V output which can be adjusted over a $\pm 6\%$ range with

minimal effect on temperature stability. Single-supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-02 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-02 is enhanced by its use as a monolithic temperature transducer. For +10V references, see the REF-01 and REF-10 data sheets.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



VOLTAGE REFERENCES

10

**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Input Voltage	
REF-02 A, E, H, RC, All DICE	40V
REF-02 C, D	30V
Power Dissipation (Note 1)	500mW
Output Short-Circuit Duration (to Ground or V_{IN})	Indefinite
Storage Temperature Range	
J, RC, and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range	
REF-02A, REF-02, REF-02RC	-55°C to +125°C
REF-02E, REF-02H	0°C to +70°C
REF-02C, REF-02D	0°C to +70°C

Lead Temperature (Soldering, 60 sec) 300°C
 DICE Junction Temperature (T_j) -65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
LCC (RC)	72°C	7.8mW/°C

2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E			REF-02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0$	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	± 3	± 6	—	± 3	± 6	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 7)	—	10	15	—	10	15	μV_{p-p}
Line Regulation (Note 2)		$V_{IN} = 8V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		$I_L = 0$ to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To $\pm 0.1\%$ of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for REF-02A and REF-02, $0^\circ C \leq T_A \leq +70^\circ C$ for REF-02E and REF-02H, $I_L = 0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E			REF-02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 4, 5)	ΔV_{OT}	$0^\circ C \leq T_A \leq +70^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	0.02	0.06	—	0.07	0.17	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 8$ to 33V) (Note 2)		$0^\circ C \leq T_A \leq +70^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	0.007	0.012	—	0.007	0.012	%/V
Load Regulation ($I_L = 0$ to 8mA) (Note 2)		$0^\circ C \leq T_A \leq +70^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	0.006	0.010	—	0.007	0.012	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:

- Guaranteed by design.
- Line and Load Regulation specifications include the effect of self heating.
- Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
- ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

- ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
- TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70^\circ C}$$

- Sample Tested.

**ELECTRICAL CHARACTERISTICS** at $V_{IN} = +15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02C			REF-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0mA$	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	± 2.7	± 6.0	—	± 2.0	± 6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 7)	—	12	18	—	12	—	μV_{p-p}
Line Regulation (Note 2)		$V_{IN} = 8V$ to 30V	—	0.009	0.015	—	0.010	0.04	%/V
Load Regulation (Note 2)		$I_L = 0$ to 8mA $I_L = 0$ to 4mA	—	0.006	0.015	—	—	—	%/mA
Turn-on Setting Time	t_{ON}	To $\pm 0.1\%$ of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S		-0.2	-0.5	—	-0.2	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $0^\circ C \leq T_A \leq +70^\circ C$ and $I_L = 0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02C			REF-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	20	65	—	70	250	ppm/ $^\circ C$
Change in V_O Temperature Coefficient With Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 2)		$V_{IN} = 8V$ to 30V	—	0.011	0.018	—	0.012	0.05	%/V
Load Regulation (Note 2)		$I_L = 0$ to 5mA	—	0.008	0.018	—	0.016	0.05	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/ $^\circ C$

NOTES:

- Guaranteed by design.
- Line and Load Regulation specifications include the effect of self heating.
- Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
- ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

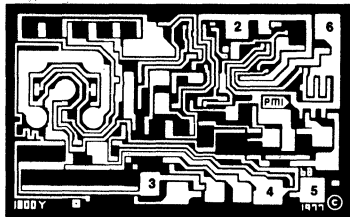
- ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
- TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70^\circ C}$$

- Sample Tested.



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.063 × 0.040 inch, 2520 sq. mils
(1.60 × 1.02 mm, 1.63 sq. mm)

2. INPUT VOLTAGE (V_{IN})
3. TEMPERATURE TRANSDUCER OUTPUT VOLTAGE (TEMP)
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_{IN} = +15V$, $T_A = 25^\circ C$ for REF-02N and REF-02G devices; $T_A = 125^\circ C$ for REF-02NT and REF-02GT devices, unless otherwise noted. (Note 3)

PARAMETER	SYMBOL	CONDITIONS	REF-02NT LIMIT	REF-02N LIMIT	REF-02GT LIMIT	REF-02G LIMIT	UNITS
Output Voltage	V_O	$I_L = 0$	4.975	4.985	4.950	4.975	V MIN
			5.025	5.015	5.050	5.025	V MAX
Output Adjustment Range	V_{trim}	$R_p = 10k\Omega$	—	±3	—	±3	% MIN
Line Regulation		$V_{IN} = 8V$ to 33V	0.015	0.01	0.015	0.01	%/V MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02NT TYPICAL	REF-02N TYPICAL	REF-02GT TYPICAL	REF-02G TYPICAL	UNITS
Temp. Voltage Output	V_T	(Notes 1, 2)	630	630	630	630	mV
Temp. Voltage Output Temp. Coefficient	TCV_T	(Notes 1, 2)	2.1	2.1	2.1	2.1	mV/°C
Output Voltage Temp. Coefficient	TCV_O		10	10	10	10	ppm/°C
Load Regulation		$I_L = 0$ to 10mA $I_L = 0$ to 8mA, NT, GT @ +125°C	0.007	0.005	0.009	0.006	%/mA
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	10	10	10	10	μV_{p-p}
Turn-On Settling Time	t_{ON}	To ±0.1% of final value, NT, GT @ +125°C	7.5	5.0	7.5	5.0	μs
Quiescent Supply Current	I_{SY}	No Load, NT, GT @ +125°C	1.4	1.0	1.4	1.0	mA
Load Current	I_L		21	21	21	21	mA
Sink Current	I_S		-0.5	-0.5	-0.5	-0.5	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	30	30	30	30	mA

NOTES:

1. See AN-18 for detailed REF-02 thermometer applications information.
2. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
3. For +25°C specifications of REF-02NT and REF-02GT, see REF-02N and REF-02G respectively.

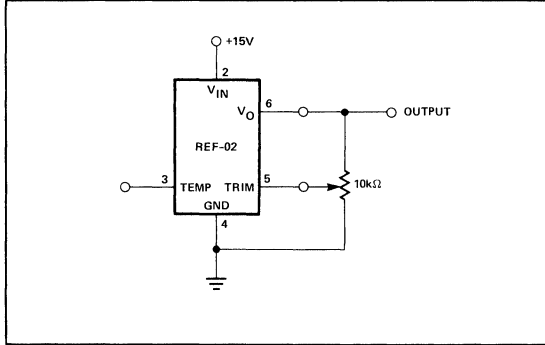


OUTPUT ADJUSTMENT

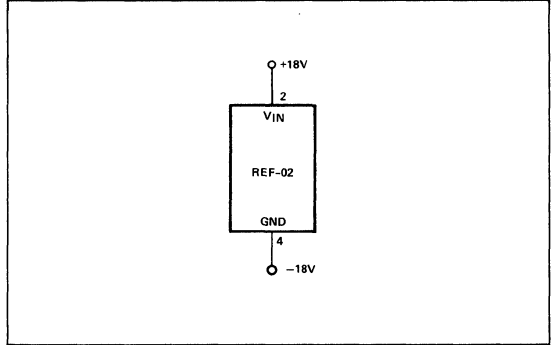
The REF-02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

OUTPUT ADJUSTMENT CIRCUIT

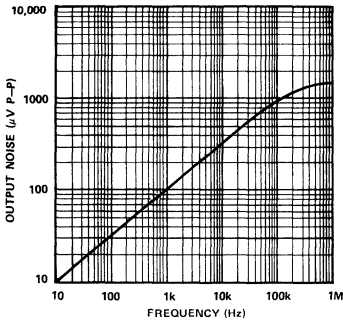


BURN-IN CIRCUIT

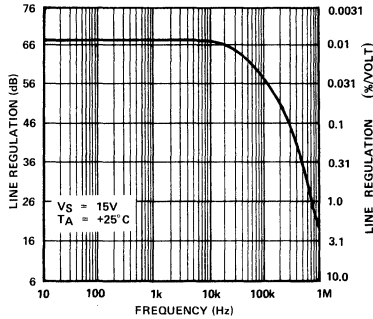


TYPICAL PERFORMANCE CHARACTERISTICS

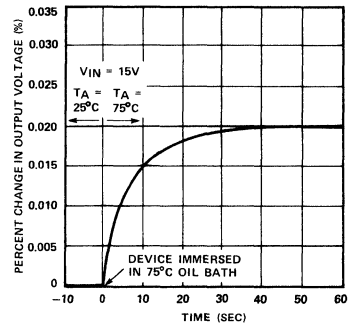
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

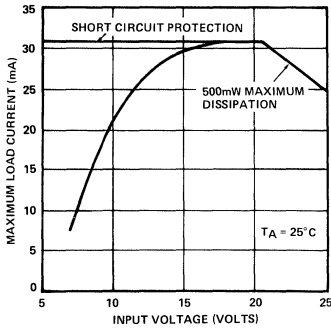
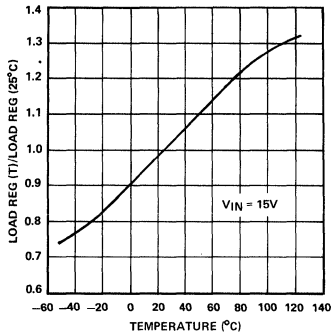
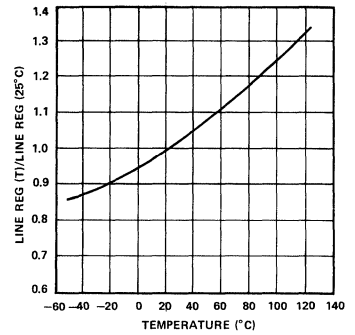
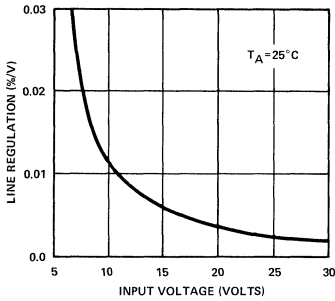
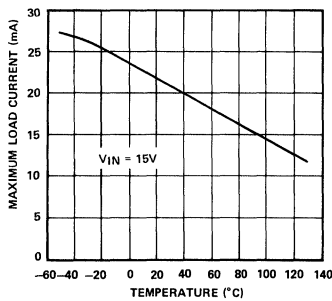
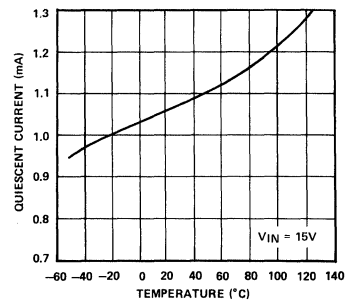
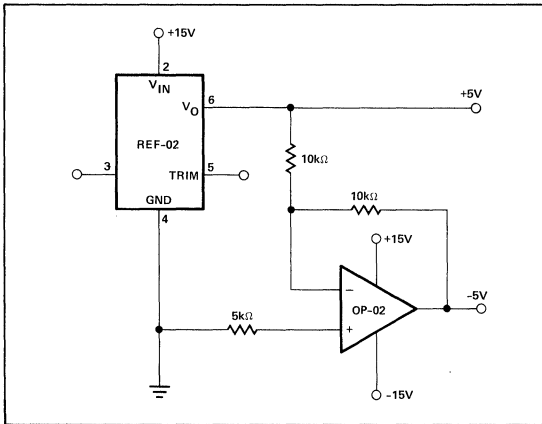
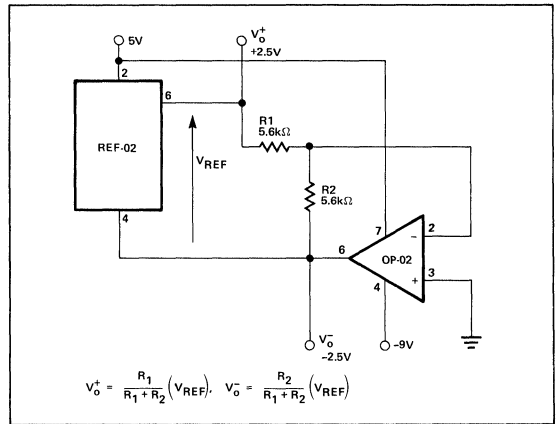


LINE REGULATION vs FREQUENCY



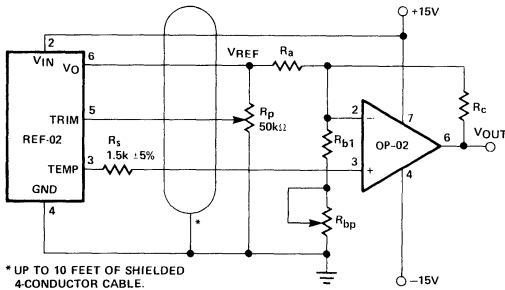
OUTPUT CHANGE DUE TO THERMAL SHOCK



TYPICAL PERFORMANCE CHARACTERISTICS
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE

NORMALIZED LOAD REGULATION ($\Delta I_L = 10\text{mA}$) vs TEMPERATURE

NORMALIZED LINE REGULATION vs TEMPERATURE

LINE REGULATION vs SUPPLY VOLTAGE

MAXIMUM LOAD CURRENT vs TEMPERATURE

QUIESCENT CURRENT vs TEMPERATURE

TYPICAL APPLICATIONS
±5V REFERENCE

±2.5V REFERENCE




PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR



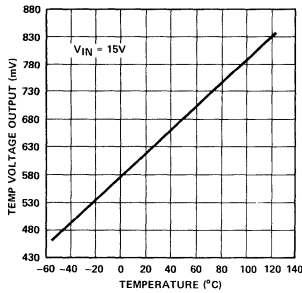
* UP TO 10 FEET OF SHIELDED 4-CONDUCTOR CABLE.

RESISTOR VALUES

TCV _{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	-55° C to +125° C	-55° C to +125° C	-67° F to +257° C
OUTPUT VOLTAGE RANGE	-0.55V to +1.25V	-5.5V to +12.5V*	-0.67V to +2.57V
ZERO-SCALE	0V @ 0° C	0V @ 0° C	0V @ 0° F
R _a (± 1% resistor)	9.09kΩ	15kΩ	7.5kΩ
R _{b1} (± 1% resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R _{bp} (Potentiometer)	200Ω	500Ω	200Ω
R _c (± 1% resistor)	5.11kΩ	84.5kΩ	8.25kΩ

*For 125°C operation, the op amp output must be able to swing to +12.5V, increase V_{IN} to +18V from +15V if this is a problem.

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-02A)

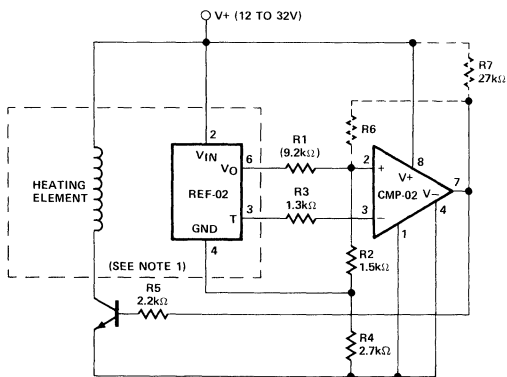


REFERENCE STACK WITH EXCELLENT LINE REGULATION

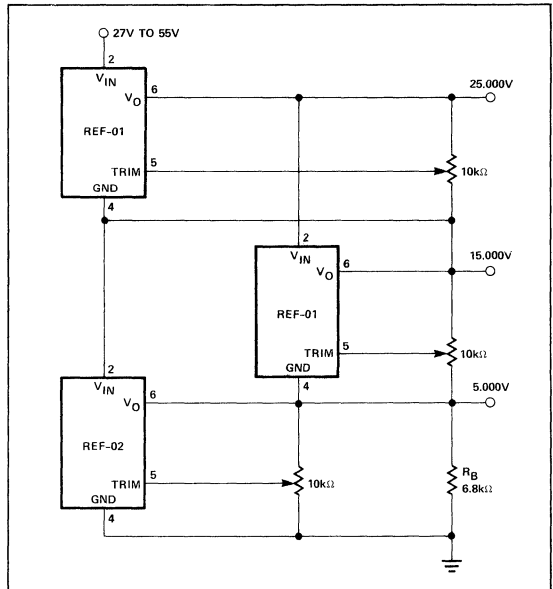
Two REF-01's and one REF-02 can be stacked to yield 5.000V, 15.000V and 25.000V outputs. An additional advantage of this circuit is near-perfect line regulation of the 5.0V and 15.0V outputs. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 15.000V regulator.

In general, any number of REF-01's and REF-02's can be stacked this way. For example, ten devices will yield ten outputs in 5V or 10V steps. The line voltage can range from 100V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).

TEMPERATURE CONTROLLER

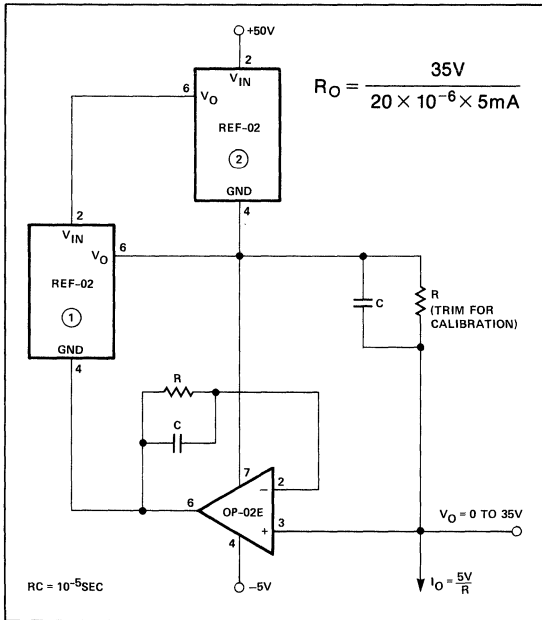
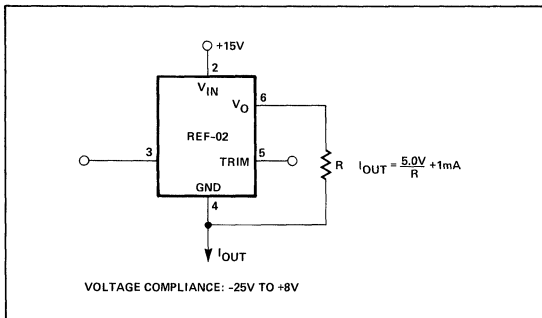
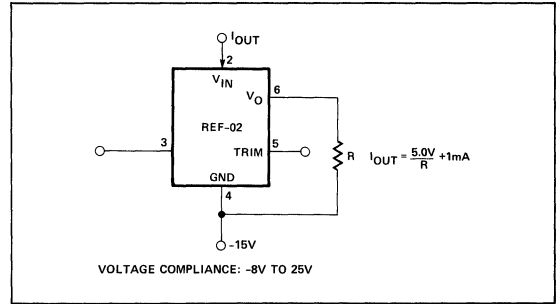
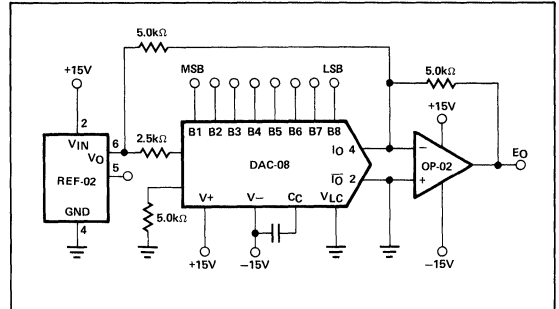
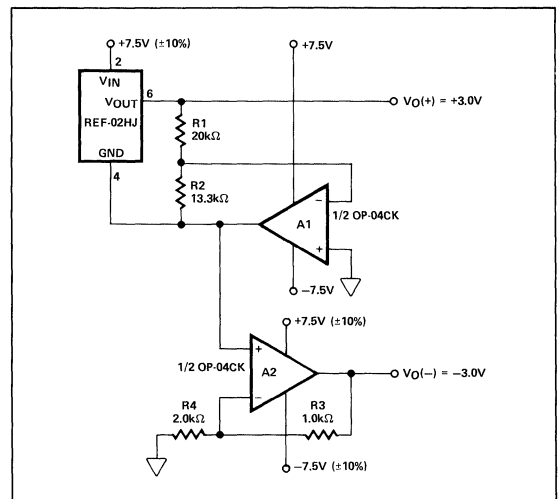


- NOTES:
- REF-02 SHOULD BE THERMALLY CONNECTED TO SUBSTANCE BEING HEATED.
 - NUMBERS IN PARENTHESES ARE FOR A SETPOINT TEMPERATURE OF 50° C.
 - R3 = R1R2/R6



PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-02 (2) keeps the line voltage and power dissipation constant in device (1); the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical $3\mu\text{V/V}$ PSRR of the OP-02E will create a 20ppm change ($3\mu\text{V/V} \times 35\text{V}/5\text{V}$) in output current over a 35V range. For example, a 5mA current source can be built ($R = 1\text{k}\Omega$) with $350\text{M}\Omega$ output impedance.


CURRENT SOURCE

CURRENT SINK

D/A CONVERTER REFERENCE

±3V REFERENCE




REF-03

+2.5V PRECISION
VOLTAGE REFERENCE

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- 2.5 Volt Output $\pm 0.3\%$
- Adjustment Range $\pm 3\%$
- Excellent Temperature Stability $3\text{ppm}/^\circ\text{C}$
- Low Noise $5\mu\text{V}_{\text{p-p}}$
- Low Supply Current 1.4mA Max
- Excellent in Single +5V Systems
- Wide Input Voltage Range $4.5\text{V to }33\text{V}$
- High Load-Driving Capability 20mA
- No External Components
- Short-Circuit Proof

ORDERING INFORMATION†

PACKAGE			
TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
REF03AJ*	REF03AZ*		MIL
REF03EJ	REF03EZ	REF03EP	IND
REF03BJ*	REF03BZ*		MIL
REF03FJ	REF03FZ	REF03FP	IND

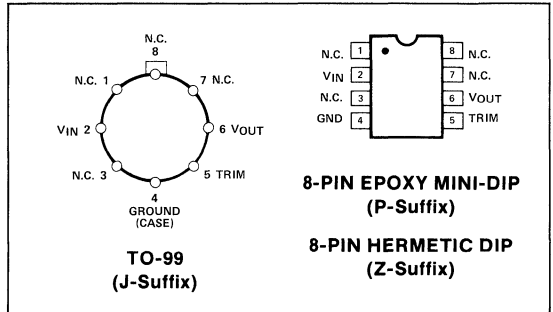
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

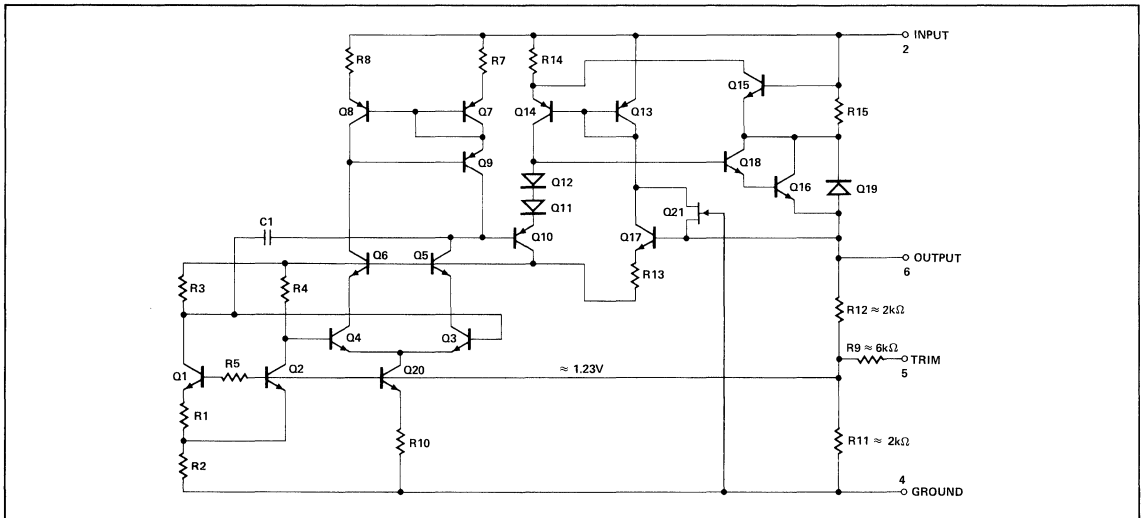
GENERAL DESCRIPTION

The REF-03 precision voltage reference provides a stable +2.5V output which can be adjusted over a $\pm 3\%$ range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 4.5V to 33V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-03 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. Full military temperature range devices with screening to MIL-STD-883 are available.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Input Voltage		
REF-03	40V
Power Dissipation (Note 1)	500mW
Output Short-Circuit Duration (to Ground or V_{IN})	Indefinite
Storage Temperature Range		
J, and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range		
REF-03A, REF-03B	-55°C to +125°C
REF-03E, REF-03F	-25°C to +85°C

DICE Junction Temperature (T_j) -65°C to +150°C
 Lead Temperature (Soldering, 60 sec.) 300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-03A/E			REF-03B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0$	2.493	2.500	2.508	2.485	2.500	2.515	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	5	7.5	—	5	7.5	μV_{p-p}
Line Regulation (Note 4)		$V_{IN} = 4.5V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		$I_L = 0$ to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of Final Value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ and $I_L = 0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-03A/E			REF-03B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 1, 2)	ΔV_{OT}	-25°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C	—	0.03	0.09	—	0.11	0.28	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 4.5V$ to 33V) (Note 4)		-25°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C	—	0.007	0.012	—	0.007	0.012	%/V
Load Regulation ($I_L = 0$ to 8mA) (Note 4)		-25°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C	—	0.006	0.010	—	0.007	0.012	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 2.5V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{2.5V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +2.500V or untrimmed.

3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O (-25^\circ \text{ to } +85^\circ \text{C}) = \frac{\Delta V_{OT} (-25^\circ \text{ to } +85^\circ \text{C})}{110^\circ \text{C}}$$

$$\text{and } TCV_O (-55^\circ \text{ to } +125^\circ \text{C}) = \frac{\Delta V_{OT} (-55^\circ \text{ to } +125^\circ \text{C})}{180^\circ \text{C}}$$

4. Line and Load Regulation specifications include the effect of self-heating.
 5. Sample tested.

Precision Monolithics Inc.

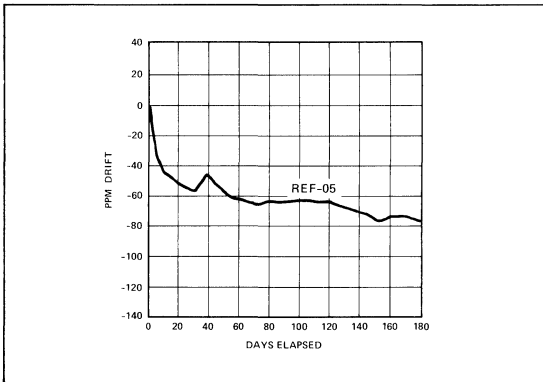
FEATURES

- 5 Volt Output
- Guaranteed Long-Term Stability 100ppm/1000 Hrs Max
- Excellent Temperature Stability 8.5ppm/°C Max
- Low Noise 15 μ V_{p-p} Max
- Low Supply Current 1.4mA Max
- Wide Input Voltage Range 8V to 33V
- High Load-Driving Capability 20mA
- Short-Circuit Proof
- Processed Per MIL-STD-883

GENERAL DESCRIPTION

The REF-05 precision voltage reference provides a stable +5V output which can be adjusted over a $\pm 6\%$ range with minimal

LONG-TERM DRIFT PLOT (Average of 20 Devices)

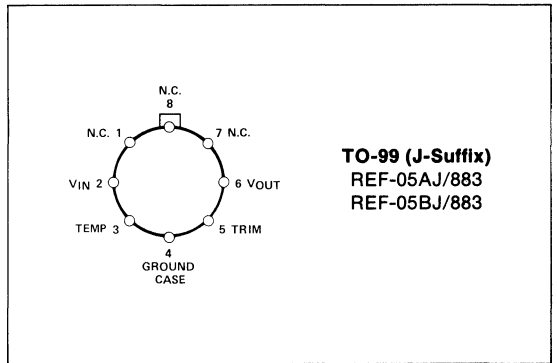


effect on temperature stability. Long-term drift is guaranteed at 100ppm/1000 hrs. maximum. Single-supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-05 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-05 is enhanced by its use as a monolithic temperature transducer. For +10V Precision Voltage References see the REF-10 data sheet.

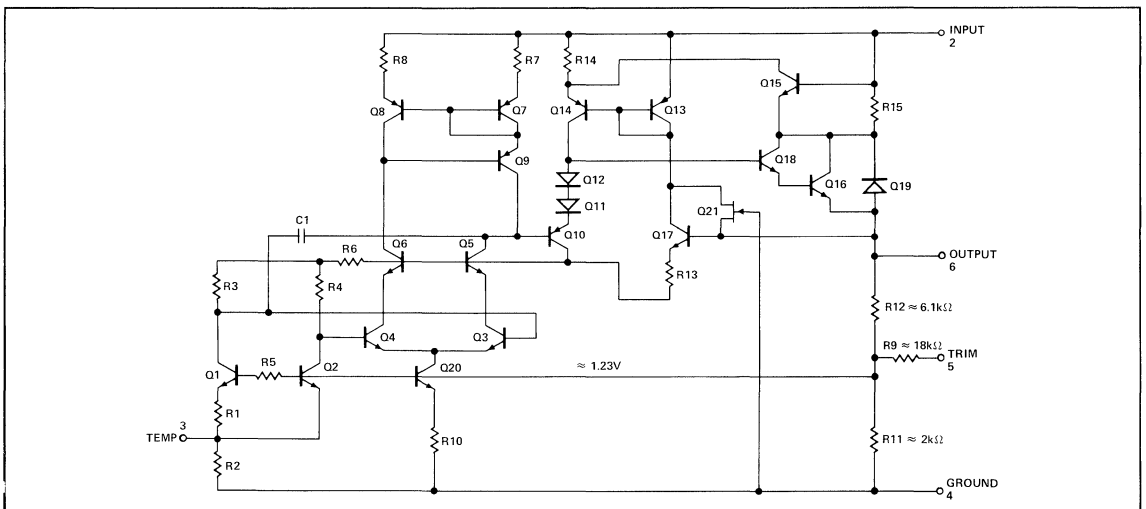
ELECTRICAL CHARACTERISTICS/ ABSOLUTE MAXIMUM RATINGS

Contact factory for 883 data sheet with full electrical specifications. Typical performance characteristics and applications information are provided in the REF-02 data sheet.

PIN CONNECTIONS & ORDERING INFORMATION



SIMPLIFIED SCHEMATIC

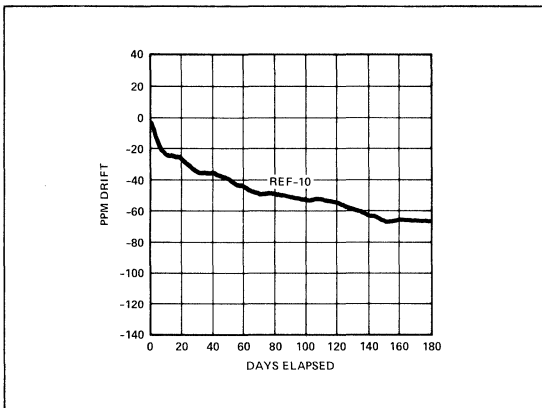


Precision Monolithics Inc.

FEATURES

- 10 Volt Output
- Guaranteed Long-Term Stability
..... 50ppm/1000 Hrs Max
- Excellent Temperature Stability 8.5ppm/°C Max
- Low Noise 30 μ V_{p-p} Max
- Low Supply Current 1.4mA Max
- Wide Input Voltage Range 13V to 40V
- High Load-Driving Capability 20mA
- Short-Circuit Proof
- Processed Per MIL-STD-883

LONG-TERM DRIFT PLOT (Average of 20 Devices)



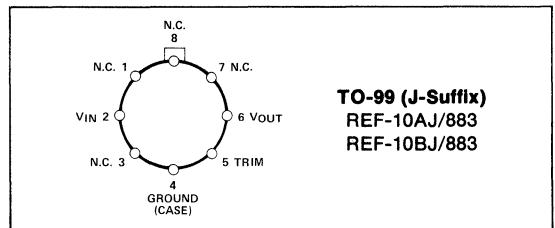
GENERAL DESCRIPTION

The REF-10 precision voltage reference provides a stable +10V output that can be adjusted over a $\pm 3\%$ range with minimal effect on temperature stability. Long-term drift is guaranteed at 50ppm/1000 hrs. maximum. Single-supply operation over an input voltage range of 13V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-10 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. For +5V precision voltage references, see the REF-05 data sheet.

ELECTRICAL CHARACTERISTICS/ ABSOLUTE MAXIMUM RATINGS

Contact factory for 883 data sheet with full electrical specifications. Typical performance characteristics and applications information are provided in the REF-01 data sheet.

PIN CONNECTIONS & ORDERING INFORMATION



SIMPLIFIED SCHEMATIC

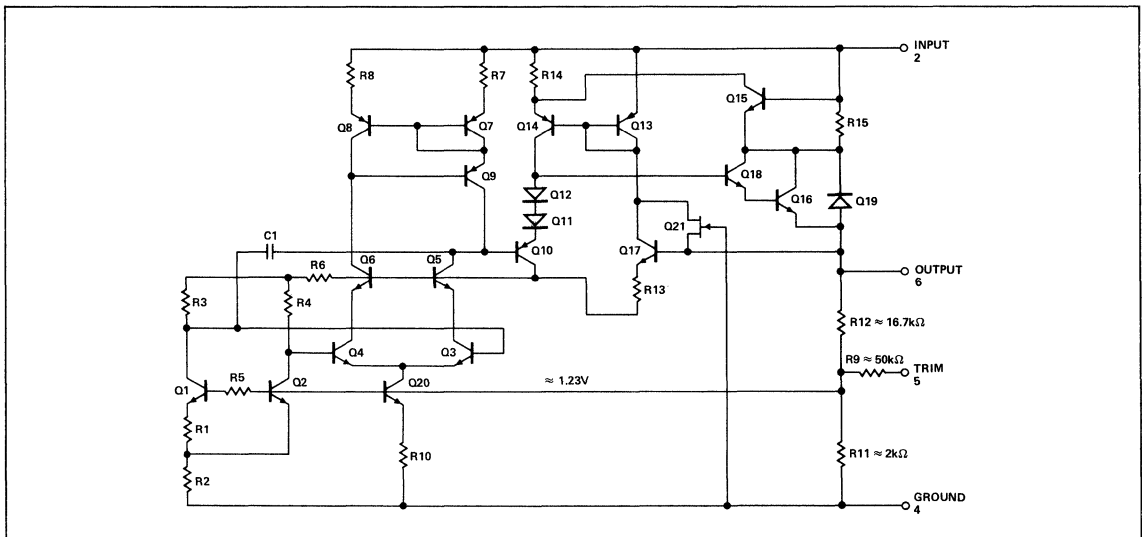


Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



D/A CONVERTERS

Precision Monolithics Inc.

- | | | | |
|-------|---|--------|---|
| 11-4 | Introduction | 11-84 | DAC-208
9-Bit Voltage-Output D/A Converter |
| 11-4 | Definitions | 11-88 | DAC-210
11-Bit Voltage-Output D/A Converter |
| 11-8 | Selection Guide | 11-92 | DAC-312
12-Bit High-Speed Multiplying D/A Converter |
| 11-10 | DAC-01
6-Bit Voltage-Output D/A Converter | 11-104 | DAC-888
BYTEDAC® 8-Bit High-Speed "Microprocessor Compatible" Multiplying D/A Converter |
| 11-14 | DAC-02/DAC-03/DAC-05
10-Bit-Plus-Sign Voltage-Output D/A Converters | 11-116 | DAC-1508A/1408A
8-Bit Multiplying D/A Converters |
| 11-19 | DAC-06
Two's-Complement 10-Bit Voltage-Output D/A Converter | 11-122 | DAC-8012
CMOS 12-Bit Multiplying D/A Converter "With Memory" |
| 11-23 | DAC-08
8-Bit High-Speed Multiplying D/A Converter | 11-131 | DAC-8212
Dual 12-Bit Buffered Multiplying CMOS D/A Converter |
| 11-34 | DAC-10
10-Bit High-Speed Multiplying D/A Converter | 11-136 | DAC-8408
Quad 8-Bit Multiplying CMOS D/A Converter With Memory |
| 11-42 | DAC-20
2-Digit BCD High-Speed Multiplying D/A Converter | 11-140 | PM-562
12-Bit Multiplying Current-Output D/A Converter |
| 11-50 | DAC-86
COMDAC® Companding D/A Converter | 11-148 | PM-565A
Complete High-Speed 12-Bit Monolithic D/A Converter |
| 11-58 | DAC-88
COMDAC® Companding D/A Converter | 11-149 | PM-7226
Quad 8-Bit CMOS D/A Converter With Voltage Output |
| 11-67 | DAC-89
COMDAC® Companding D/A Converter | | |
| 11-76 | DAC-100
10-Bit Current-Output D/A Converter | | |



D/A CONVERTERS

Precision Monolithics Inc.

11-150 **PM-7524**

CMOS 8-Bit Buffered Multiplying
D/A Converter

11-159 **PM-7528**

Dual 8-Bit Buffered Multiplying CMOS
D/A Converter

11-175 **PM-7533**

CMOS Low Cost 10-Bit Multiplying
D/A Converter

11-185 **PM-7541**

CMOS 12-Bit Monolithic Multiplying
D/A Converter

11-195 **PM-7542**

12-Bit Multiplying CMOS
D/A Converter

11-196 **PM-7543**

12-Bit Serial-Input Multiplying CMOS
D/A Converter

11-197 **PM-7545/PM-7645**

12-Bit Buffered Multiplying CMOS
D/A Converters

11-208 **PM-7548**

12-Bit Multiplying CMOS
D/A Converter

11-209 **JM38510/11301/11302**

JAN 8-Bit Multiplying D/A Converters

DIGITAL-TO-ANALOG CONVERTERS

INTRODUCTION

A D/A converter accepts a digital input and produces an analog output. The basic DAC consists of a voltage or current reference, binary-weighted precision resistors, a set of electronic switches, and a means of summing the weighted currents.

Three important criteria for selecting a good DAC are resolution, accuracy, and speed. Other essential requirements to be considered are temperature stability, input coding, output format, reference requirements, and power consumption.

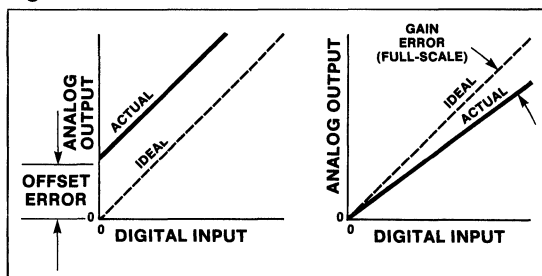
Since introducing the first monolithic D/A converter in 1970, PMI has continually improved and updated its DAC product line. Using both bipolar and CMOS technologies, PMI offers complete selections of parametric trade-offs available from these technologies. Very high speed, internal references and amplifiers are key features of the bipolar technology DACs. The CMOS technology DACs offer a much higher degree of logic interface function, while maintaining absolute minimums in power dissipation. A wide offering of microprocessor-interfaceable DACs simplify connection to 4, 8, and 16-bit microprocessor systems. The DAC with "memory" is another first offered by PMI to simplify system self-diagnosis of data path integrity.

The selection guides following the definitions will aid you in quickly locating the appropriate DAC for your application.

DEFINITIONS — LINEAR DIGITAL-TO-ANALOG CONVERTERS

Absolute Accuracy — The absolute accuracy of a DAC is the difference between the actual unadjusted analog output and the ideal output that is expected when a given digital code is applied. Sources of error include full-scale error (gain error), zero-scale error (offset error), nonlinearity errors, and the drift of all of these. Therefore, absolute accuracy includes all deviations from the ideal. (See Figure 11.1)

Figure 11.1 Gain and Offset Error Defined



A.C. Feedthrough — The ratio of the amplitude of signal at the DAC output to the reference input with all DAC switches off. This parameter is expressed in dBs.

BCD — The abbreviation BCD stands for binary-coded decimal. It is a binary code used to represent decimal numbers in which the digits 0 through 9 are coded, using the 4-bit binary 8-4-2-1 code.

Binary — A positive-weighted code in which a number is represented by:

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + \dots + a_n 2^n$$

where each coefficient "a_i" has a value of zero or one. Data converters use this code in its fractional form where:

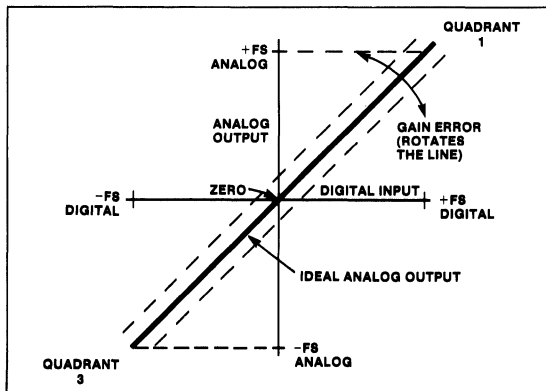
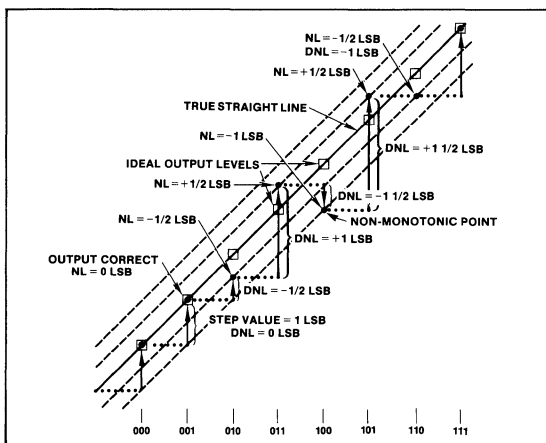
$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \dots + a_n 2^{-n}$$

and N has a fractional value between zero and one.

Bit — The unit of binary information. It can have the value of zero or one.

Bipolar Output — When the analog signal range includes both positive and negative values, the output is said to be bipolar. The transfer characteristic of an ideal 2-quadrant bipolar-output DAC is shown in Figure 11.2.

Differential Nonlinearity (DNL) — Differential nonlinearity is the worst case deviation of any adjacent analog outputs from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be nonmonotonic. Maximum DNL error is less than or equal to twice the maximum INL. (See Figure 11.3)

Figure 11.2 Bipolar Output Converter

Figure 11.3 Nonlinearity (NL) and Differential Nonlinearity (DNL)


Dynamic Range (DR) — The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For linear DACs, this ratio is 2^n , where n = number of bits of resolution.

DR (in dB) = $20 \log_{10} 2^n \approx 6n$ for linear DACs; (COMDACs® are 66 or 72dB.)

Endpoint Linearity — See Integral Nonlinearity.

Functional Compliance — The functional compliance of a DAC is the voltage range over which the current output can be driven and for which the DAC output current will maintain the

same relative accuracy (the output can change absolutely).

Full Scale (FS) — The full-scale output of a DAC is its maximum voltage or current. For a binary DAC, the full-scale output occurs when the digital inputs are all ones. The full-scale value is one LSB less than the reference value.

Full-Scale Gain Error (G_{FSE}) — See Gain Error.

Full-Scale Range (FSR) — The difference between the maximum analog output and the minimum analog output of a DAC.

Gain Drift (TC_{GFS}) — The variation of the full-scale value (voltage or current) measured over the operating temperature range is called gain drift. This parameter has units of %FS, ppmFS, or LSB. It may also be expressed % of FS/°C, ppmFS/°C, etc.

Gain Error (G_{FSE}) — The difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value (see Figure 11.1). It is the deviation in slope of the DAC transfer characteristic from ideal.

Glitch — A glitch is a switching transient appearing in the output during a code transition. Its value is expressed as a product of voltage ($V \times ns$) or current ($mA \times ns$) and time duration or charge transferred (in Picocoulombs).

Integral Nonlinearity (INL) or Nonlinearity (NL) — This is the single most important DAC specification. PMI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points, expressed as a percent of full-scale range or in terms of LSBs. (See Figure 11.5) For DACs, a specification of $\pm 1/2$ LSB INL guarantees monotonicity and ± 1 LSB maximum differential nonlinearity.

Least Significant Bit (LSB) — The analog value of the LSB is the smallest change that can occur in the output of a DAC. It corresponds to a one-bit change in the binary input. The analog value will be either a voltage or current.

$$LSB \text{ (Analog Value)} = \frac{FSR}{2^n}$$

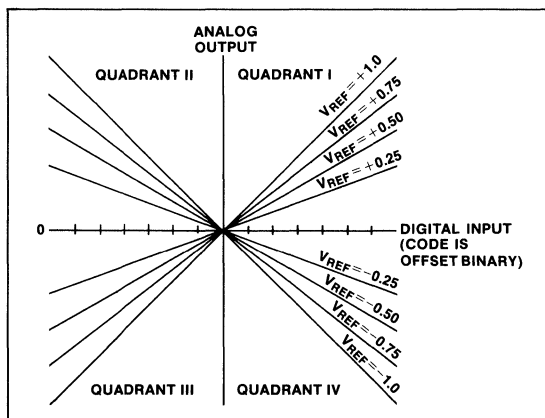
where FSR = Full-Scale Range
 n = number of bits

Most Significant Bit (MSB) — The analog value of the MSB is the largest incremental output change obtainable by switching a single input bit. The analog value will be either a voltage or current.

$$\text{MSB (Analog Value)} = \frac{\text{FSR}}{2}$$

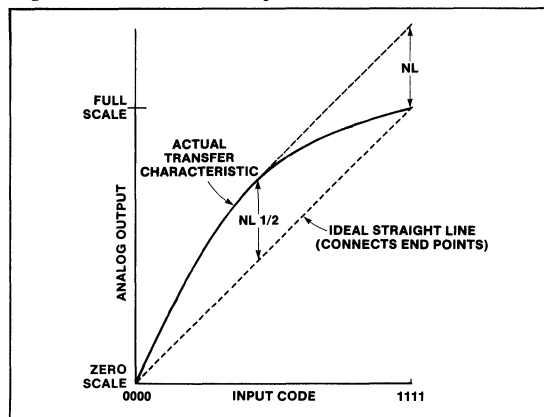
Monotonicity — A DAC is monotonic if the analog output either increases or remains the same for an increasing digital input code. If the DNL is less than or equal to ± 1 LSB, monotonicity is guaranteed. (See Figure 11.3)

Figure 11.4 DAC Transfer Curves



Multiplying DACs — The DAC multiplies an analog reference by a digital word. Some DACs can multiply only positive digital words by a positive reference. This is known as single quadrant operation (Quadrant I, see Figure 11.4). Two quadrant operation (Quadrants I and III) can be performed by a DAC that usually operates in Quadrant I by configuring the output for bipolar output operation. This is accomplished by offsetting the output by a negative MSB (1/2 of FSR), so that the MSB becomes the sign bit. CMOS DACs provide four quadrant operation by allowing the use of both positive and negative references. (Quadrants I, II, III, IV).

Figure 11.5 Nonlinearity



Nonlinearity (NL) — See Integral Nonlinearity.

Offset Drift (TCV_{OS}, TCI_{OS}) — The variation of the offset (voltage or current) measured over the operating temperature range. The offset drift is divided by the temperature range over which it is measured, and expressed in ppm per degree centigrade or percent of full-scale range. This parameter applies to DACs operating in the bipolar output mode. See zero-scale drift for DACs operating in the unipolar output mode.

Offset Error (V_{OS}, I_{OS}) — The offset error is the error at analog zero for a data converter operating in the bipolar mode.

Output Resistance (R_O) — Output resistance is the equivalent internal resistance for a current output D/A converter as seen at its output. It is measured as the change in output current ΔI with the change in output voltage ΔV . It is a direct measure of the true compliance.

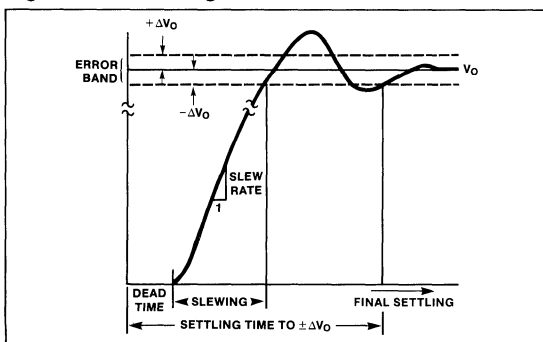
Power Supply Sensitivity (P_{SS}) — The change in the output of the converter due to a change in the power supply value. This may be expressed as a percent of full-scale range per one percent change in the power supply, or as a percent of full scale per volt of power supply change. Normally P_{SS} is specified at DC; it is sometimes specified over a given frequency range.

Relative Accuracy — See Integral Nonlinearity.

Resolution (n) — The resolution of a DAC is the number of states (2^n) that the FSR is divided (or resolved) into, where n is equal to the number of bits.

Settling Time — Settling time is the elapsed time for the analog output to reach its final value within a specified error band after a digital input code change. It is usually specified for a full-scale change and measured from the 50% point of the logic input change to the time the output reaches its final value within the specified error band. (See Figure 11.6)

Figure 11.6 Settling Time Measurement



Three-State Outputs — A digital output circuit that can be programmed to output a logic low, logic high, or a high output impedance state. These devices are generally connected to digital buses.

True Compliance — The true compliance of a DAC is the voltage range over which the current output can vary while the DAC maintains an absolute accuracy of $\pm 1/2$ LSB. The higher the DAC output impedance, the better the voltage compliance will be.

Unipolar Output — A DAC operates in the unipolar output mode when the analog output starts at zero, stopping at a full-scale positive or negative value, while the digital inputs are changed from zero to all-ones code. The analog output occurs in one quadrant.

Zero-Scale Error (V_{zse} , I_{zse}) — The zero-scale error is the error at analog zero for a data converter operating in the unipolar mode.

Zero-Scale Drift (TCV_{zs} , TCI_{zs}) — The variation of zero scale measured over the operating temperature. It is expressed in ppmFS/ $^{\circ}$ C, or %FS/ $^{\circ}$ C, etc.

Zero-Scale Symmetry Error (V_{zss}) — This definition applies only to sign-magnitude DACs. It is the change in the analog output produced by switching the sign bit with a zero-code input to the magnitude bits. It is expressed in units of voltage, current, or in fractions of an LSB.

DEFINITIONS — COMPANDING DACs

The companding (COMDAC[®]) DACs that PMI manufactures are the DAC-86, DAC-88, and the DAC-89. They are constructed such that the more significant bits of the digital input have a larger than binary relationship to the less significant bits. This decreases the resolution of the more significant bits, which increases the analog signal range. The effect of this is to compress more data into the more significant bits.

Chord — The mathematical formula, describing the DAC transfer function, is implemented by performing a piecewise linear approximation of the function. The straight line segments used in the approximation are called chords.

Chord Endpoints — The digital code corresponding to the maximum analog output for a given chord is called the chord endpoint.

Dynamic Range (DR) — The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For the COMDACs[®] this would be output ($I_{7,15}$) divided by output ($I_{0,1}$). This is then converted to dB using the formula:

$$DR = 20 \text{ Log}_{10} \left(\frac{I_{7,15}}{I_{0,1}} \right) \text{ (dB)}$$

Encode Current — The encode current is the difference between $I_{OE(+)}$ and $I_{OD (+)}$ or the difference between $I_{OE(-)}$ and $I_{OD (-)}$ at any code.

Full-Scale Symmetry Error — The full-scale symmetry error of a DAC is the difference between the maximum and the minimum analog output values. For the COMDACs[®] this is the difference between $I_{OD (-)}$ and $I_{OD (+)}$ or $I_{OE (+)}$ and $I_{OE (-)}$.



D/A CONVERTERS

Precision Monolithics Inc.

Output-Level Notation — Each output current level may be designated by the digital input code as $I_{c,s}$; where c = chord number and s = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of the first chord (C_0); and $I_{7,15}$ = full-scale current.

Steps — Each chord is divided into equal increments called steps.

Step Nonlinearity — This is the deviation of the actual step size from the ideal step size within a chord. In a linear DAC, it corresponds to differential nonlinearity.

DIGITAL-TO-ANALOG CONVERTER SELECTION GUIDE

PMI offers a complete line of digital-to-analog converters (DACs), all of which are guaranteed to be monotonic over their operating temperature ranges, and some which have become industry standards. The DACs have been arranged in a matrix, which highlights their primary characteristics so that the user can easily narrow the selection, according to specific requirements. More detailed specifications are then tabulated in each product group.

	Voltage Output						Current Output															
	DAC-01	DAC-208	DAC-210	DAC-02, DAC-03	DAC-05	DAC-06	DAC-08	DAC-20	DAC-10	DAC-100	DAC-312	PM-582	DAC-888	DAC-86	DAC-88, DAC-89	PM-7533	PM-7528	PM-7541	PM-7545, PM-7645	DAC-8012	PM-7524	
Resolution																						
6-Bits	●																					
8-Bits		●					●	●					●	●	●		●					●
10-Bits			●	●	●	●			●	●						●						
12-Bits											●	●						●	●	●		
Input Coding																						
BCD								●														
Binary							●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Complementary Binary	●								●													
Sign Magnitude		●	●	●	●																	
Input Latches μ P Compatible												●					●		●	●	●	
Two's Complement						●																
Complementary Current Outputs							●	●	●		●	●			●		●				●	
Internal Reference	●	●	●	●	●	●				●												
Logic Threshold Control							●	●	●	●	●	●	●	●								
JAN Qualified							●															
Operating Temperature Range																						
Military	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Industrial										●	●	●	●	●	●	●	●	●	●	●	●	●
Commercial	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●

*Companding



D/A CONVERTERS

Precision Monolithics Inc.

DIGITAL-TO-ANALOG CONVERTER SELECTION GUIDE

Six-Bit

DAC-01	6-Bit Voltage-Output D/A	3 μ s settling, includes ref., 250mW power dissipation
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Eight-Bit

DAC-08*	8-Bit High-Speed Multiplying D/A	85ns settling, 1LSB gain error, 0.1%INL
DAC-208	8-Bit Plus Sign Voltage-Output D/A	Includes ref., 0.1%INL, 750ns settling
DAC-888	8-Bit High-Speed μ P-Compatible D/A	8-bit input latch, 0.1%INL, 400ns settling
DAC-1508A/ 1408A	8-Bit Multiplying D/A	0.19%INL, 250ns settling, 157mW power dissipation
PM-7524	CMOS 8-Bit Multiplying D/A with Latches	1/2LSB INL, 1mW power dissipation, 10ppm/ $^{\circ}$ C gain drift
PM-7528	CMOS Dual 8-Bit Buffered Multiplying D/A	1% matching, +5V to +15V single supply, 0.5LSB INL
JM38510/ 11301-11302	JAN Qualified DAC-08	MIL-M-38510/113 device types 01 and 02

Eight-Bit Companding

DAC-86	Companding D/A Converter	μ 255 law, meets D3 specs, encode and decode
DAC-88	Companding D/A Converter	Improved accuracy and speed over DAC-86
DAC-89	Companding D/A Converter ('A' Law)	11-bit accuracy and resolution around zero

Ten-Bit and BCD

DAC-02/ 03/05	10-Bit-Plus-Sign Voltage-Out D/A	Includes ref., \pm 10V out, 2 μ s settling
DAC-06	Two's Complement 10-Bit Voltage-Out D/A	Includes ref., 1LSB INL, 1.5 μ s settling
DAC-10	10-Bit High-Speed Multiplying D/A	85ns settling, 10ppm/ $^{\circ}$ C drift, 0.05% INL
DAC-20	2-Digit BCD High-Speed Multiplying D/A	85ns settling, 0.25LSB gain error, 0.25LSB INL
DAC-100	10-Bit Current-Output D/A	Includes ref., 375ns settling, 15ppm/ $^{\circ}$ C drift
DAC-210	10-Bit-Plus-Sign Voltage-Output D/A	Includes ref., 0.05%INL, 1.5 μ s settling
PM-7533	CMOS Low-Cost 10-Bit Multiplying D/A	0.5LSB INL, 4-quadrant multiplying, 2mA I _{SY}

Twelve-Bit

DAC-312	12-Bit High-Speed Multiplying D/A	0.012%DNL, 0.025%INL, 250ns settling
DAC-8012	CMOS 12-Bit Multiplying D/A with Memory	Data readback, 0.5LSB INL, 2ppm/ $^{\circ}$ C TC
PM-562	12-Bit Multiplying D/A Converter	0.25LSB INL, 1.5 μ s settling, 0.5LSB DNL
PM-7541	CMOS 12-Bit Multiplying D/A	0.5LSB INL, 4-quadrant multiplying, 2mA I _{SY}
PM-7545/ 7645	CMOS 12-Bit Multiplying D/A with Latches	0.5LSB INL, 1LSB gain error, 2mA I _{SY}

* Indicates product available in LCC package (1986).

DIGITAL-TO-ANALOG CONVERTERS

11

Precision Monolithics Inc.

FEATURES

- **Fast** **3 μ s Settling Time Max**
- **Complete** **Includes Reference, Ladder, Op Amp**
- **Low Power Consumption** **250mW Max**
- **6-Bit Resolution** **7-Bit Accuracy**
- **3 Output Options** **+10V, \pm 5V, \pm 10V**
- **Standard Power Supplies** **\pm 12V to \pm 18V**
- **TTL — Compatible Logic Levels**
- **MIL-STD-883 Class B Processing Available From Stock**

ORDERING INFORMATION††

14-PIN HERMETIC DIP		
FULL TEMP. N.L. LSB	MILITARY TEMP.	COMMERCIAL TEMP.
\pm 1/8	DAC01AY* DAC01Y*	—
\pm 1/4	DAC01BY* DAC01FY*†	DAC01CY DAC01HY†
\pm 1/2	—	DAC01DY

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Unipolar only — all others unipolar or bipolar.

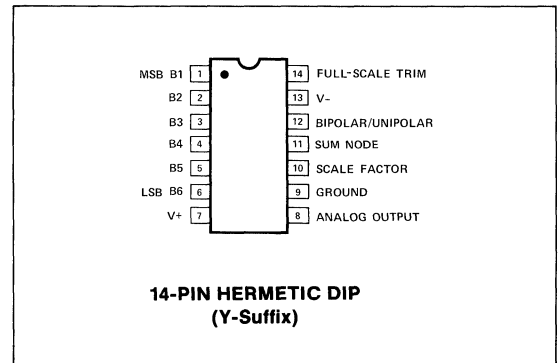
†† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

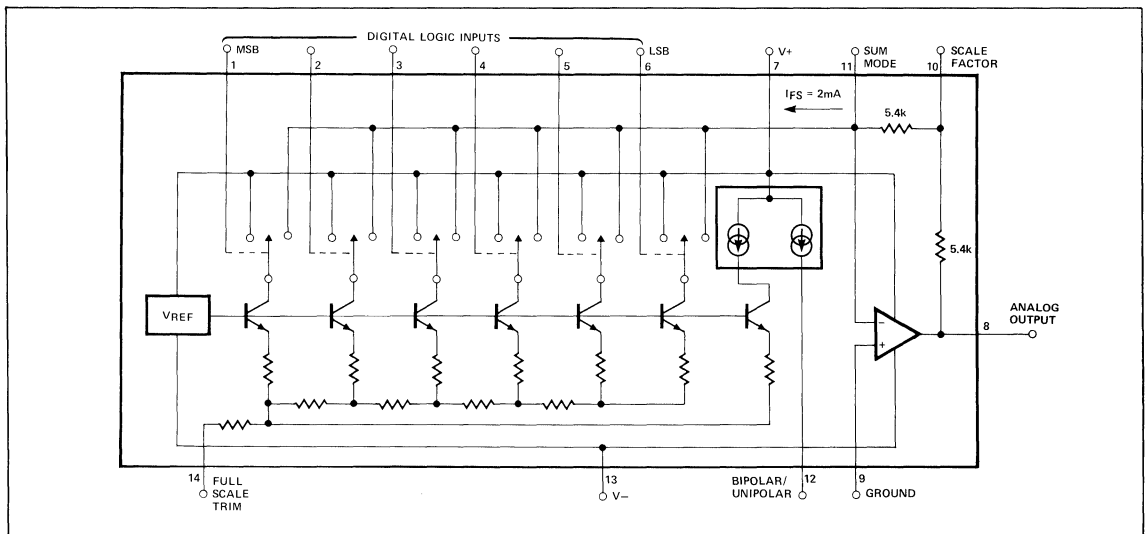
The DAC-01 is a complete monolithic 6-bit digital-to-analog converter. The device contains current steering logic, current sources, a diffused resistor ladder network, precision

voltage reference and fast summing op amp on one chip. Monolithic construction provides low power consumption and high reliability. Wide power supply range, three output voltage options, and three input code options assure flexibility for a wide variety of applications. A seventh bit may also be added for greater resolution. Introduced in 1970, the DAC-01 is still the fastest, lowest power, most accurate 6-bit complete monolithic DAC available. The DAC-01 is ideal for CRT deflection circuits, servo positioning controls, digitally programmed power supplies and pulse generators, modem and telephone system digitizing and demodulation circuits, digital filters, and 6-bit A/D converters.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (See Note 3)

Operating Temperature	
DAC-01A, DAC-01, DAC-01B,	
DAC-01F	-55°C to +125°C
DAC-01C, DAC-01H, DAC-01D	0°C to +70°C
DICE Junction Temperature (T_j)	-65°C to +150°C
V+ Supply Voltage to Ground	0 to +18V
V- Supply Voltage to Ground	0 to -18V
Logic Input to Ground	-0.7 to +6V
Internal Power Dissipation (Note 1)	500mW

Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 2)	Indefinite

NOTES:

- Rating applies to ambient temperatures of 100°C. For temperatures above 100°C, derate linearly at 10mW/°C.
- Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and over the rated operating temperature range, unless otherwise noted.

PARAMETER	SYMBOL	DAC-01A	DAC-01	DAC-01B	DAC-01F	DAC-01C	DAC-01H	DAC-01D	UNITS
Output Options		Unipolar Bipolar	Unipolar Bipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	
Temperature Range	T_A	-55/+125	-55/+125	-55/+125	-55/+125	0/+70	0/+70	0/+70	°C
Nonlinearity 25°C/Maximum	NL	±0.20	±0.40	±0.40	±0.40	±0.40	±0.40	±0.78	%FS
Nonlinearity Over Temperature — Maximum	NL	±0.30	±0.45	±0.45	±0.45	±0.45	±0.45	±0.78	%FS
Full-Scale Tempco — Maximum	T_C	±80	±80	±120	±80	±160	±160	±160	ppm/°C
Unipolar Zero-Scale Output Voltage — Maximum (Notes 1, 2)	V_{ZS}	25	25	25	40	25	40	50	mV

ELECTRICAL CHARACTERISTICS for all DAC-01 grades, $V_S = \pm 15V$ and over the rated operating temperature range unless otherwise noted.

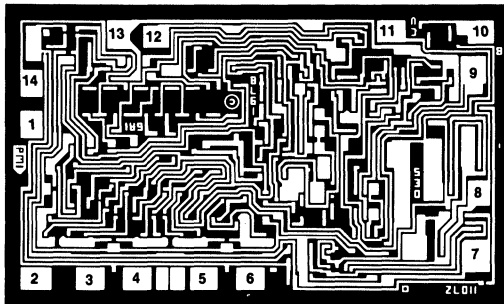
PARAMETER	SYMBOL	CONDITIONS	DAC-01			UNITS
			MIN	TYP	MAX	
Unipolar Full Range Output Voltage (Note 3)	V_{FR}	2k Ω load, logic $\leq 0.8V$, short pin 13 to pin 14. Short pin 12 to Ground and pin 10 to pin 11.	+10.0	—	+11.75	V
Bipolar Output Voltage (Note 3) ±5 Volt Range		2k Ω load, short pin 11 to pin 12. Short pin 13 to pin 14, short pin 10 to pin 11.				
	V_{FR+}	Logic Inputs $\leq 0.8V$	+4.93	—	+5.94	V
	V_{FR-}	Logic Inputs $\geq 2.0V$	-5.94	—	-4.93	V
±10 Volt Range		Open pin 10				
	V_{FR+}	Logic Inputs $\leq 0.8V$	+9.86	—	+11.89	V
	V_{FR-}	Logic Inputs $\geq 2.0V$	-11.89	—	-9.86	V
Bipolar Offset Voltage (Note 1) ±1/2 ($ V_{FR+} - V_{FR-} $)		±5 Volt Range	—	±40	±70	mV
		±10 Volt Range	—	±80	±140	mV
Resolution			6	—	—	Bits
Logic Input "0"	V_{INL}		—	—	0.8	V
Logic Input "1"	V_{INH}		2	—	—	V
Logic Input Current, Each Input	I_{IN}		—	±2	±8	μA
Power Supply Sensitivity	P_{SS}	$\pm 12V \leq V_S \leq \pm 18V$ $V_{FS} = 10.0V$	—	±0.01	±0.15	% V_{FS}/V
Power Consumption	P_d	No Load	—	200	250	mW
Supply Current	I^+	$V^+ = +15V$	—	—	7.3	mA
	I^-	$V^- = -15V$ Logic Inputs $\leq 0.8V$	—	—	9.3	mA
Setting Time to ±1/2 LSB (Note 4)	t_S	$2.0V \leq$ Logic Level $\leq 0.8V$ $T_A = 25^\circ C$	—	1.5	3	μs

NOTES:

- Zero-scale or bipolar offset voltage can be trimmed to zero volts or to the exact one's or two's complement condition with an external resistor network to pin 11.
- Logic input voltage $\geq 2.0V$.
- Full-scale is adjustable to precisely 10V for unipolar operation and 10V or 20V peak-to-peak bipolar operation with an external 500 Ω potentiometer from pin 14 to V-.
- Guaranteed by design.



DICE CHARACTERISTICS



1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6 (LSB)
7. V+
8. ANALOG OUTPUT
9. GROUND
10. SCALE FACTOR
11. SUM NODE
12. BIPOLAR/UNIPOLAR
13. V-
14. FULL-SCALE TRIM

DIE SIZE 0.092 × 0.054 inch, 4968 sq. mils (2.34 × 1.37 mm, 3.21 sq. mm)

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-01N BIPOLAR AND UNIPOLAR LIMIT	DAC-01G BIPOLAR AND UNIPOLAR LIMIT	UNITS
Nonlinearity	NL	$V_S = \pm 15\text{V}$	1/4	1/2	L.S.B. MAX
Zero-Scale Voltage	V_{ZS}	$V_S = \pm 15\text{V}$	25	35	mV MAX

WAFER TEST LIMITS at $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

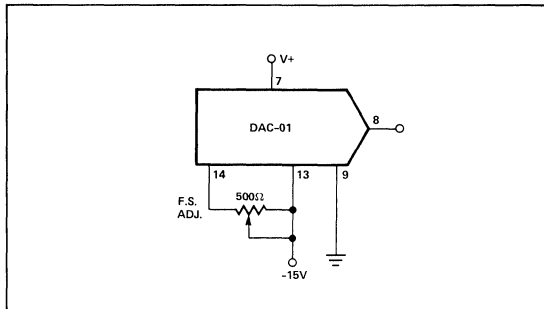
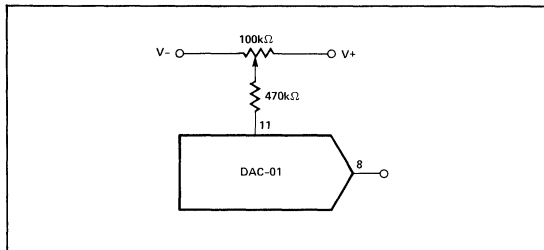
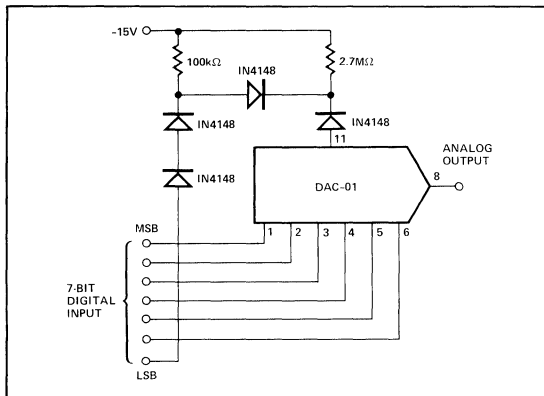
PARAMETER	SYMBOL	CONDITIONS	DAC-01 LIMIT	UNITS
Unipolar Full-Scale Output Voltage (All Models)	V_{FR}	2k Ω Load, Logic $\leq 0.8\text{V}$, Short V- to Full-Scale Trim, Unipolar/ Bipolar to Ground, and Scale Factor to Sum Node	10.00	V MIN
		2k Ω Load, Short Sum Node to Unipolar/Bipolar. Short V- to Full-Scale Trim and Scale Factor to Sum Node.	11.75	V MAX
Bipolar Output Voltage ± 5 Volt Range	V_{FR+} V_{FR-}	Logic Inputs $\leq 0.8\text{V}$	+4.93	V MIN
		Logic Inputs $\geq 2.0\text{V}$	-5.94	V MAX
± 10 Volt Range	V_{FR+} V_{FR-}	Open-Scale Factor Logic Inputs $\leq 0.8\text{V}$	+9.78	V MIN
		Logic Inputs $\geq 2.0\text{V}$	-11.89	V MAX
Bipolar Offset Voltage $\pm 1/2 (I_{V_{FR+}} - I_{V_{FR-}})$		± 5 Volt Range	$\pm 1/2$	LSB MAX
		± 10 Volt Range		
Resolution			6	Bits MAX
Logic Input "0"	V_{INL}		0.8	V MAX
Logic Input "1"	V_{INH}		2	V MIN
Logic Input Current, Each Input	V_{OV}		± 8	μA MAX
Power Supply Rejection	PSR	$\pm 12\text{V} \leq V_S \leq \pm 18\text{V}$, $V_S = 10.0\text{V}$	0.15	%FS/V MAX
Power Consumption	P_d	No Load	250	mW MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at 25°C .

PARAMETER	SYMBOL	CONDITIONS	DAC-01N TYPICAL	DAC-01G TYPICAL	UNITS
Settling Time	t_S	To $\pm 1/2$ LSB	1.5	1.5	μs
Full-Scale Tempco	TCV_{FS}	$V_S = \pm 15\text{V}$	60	90	ppm/ $^\circ\text{C}$

BASIC CIRCUIT CONNECTIONS
FULL-SCALE ADJUSTMENT TECHNIQUE

OPTIONAL ZERO-SCALE OR BIPOLAR OFFSET ADJUSTMENT

ADDITION OF 7th BIT

APPLICATIONS INFORMATION
INPUT CODES

The DAC-01 uses standard complementary binary coding for unipolar operation (all inputs logic high produces zero output voltage). One's complement coding may be implemented by shorting pin 11 to pin 12 and inverting the MSB (all other bits are not inverted). Complementary offset binary coding may be implemented by shorting pin 11 to pin 12, and injecting approximately $5\mu\text{A}$ into pin 11 (which is at ground potential) by using the "optional Zero-Scale or bipolar offset adjustment" circuit. Two's complement code is achieved when the MSB for complementary offset binary is inverted.

FULL-SCALE ADJUST

A 500Ω pot from pin 14 to V^- can be used to adjust the Full-Scale output voltage to exactly 10 volts in unipolar mode or 10 to 20 volts peak-to-peak in bipolar mode. If no pot is used, connect pin 14 to V^- .

SCALE FACTOR

For +10 volts or ± 5 volt outputs, short pin 10 to pin 11 (adjusts the feedback resistor around the output amplifier). For ± 10 volt output, leave pin 10 open. Intermediate output voltages may be obtained by placing a pot between pin 10 and pin 11. This will, however, seriously degrade the Full-Scale temperature coefficient due to the mismatch between the $+1150\text{ppm}/^\circ\text{C}$ tempco of the diffused resistors and the pot tempco.

CAPACITIVE LOADS

When driving capacitive loads greater than 50pF in Unipolar mode or 30pF in Bipolar mode a 100pF capacitor may be placed from pin 11 to ground for added stability.

LOWER RESOLUTION APPLICATIONS

When less than 6 bits of resolution is required, connect unused bits to a voltage level greater than +2.0 volts. The +5 volt logic supply is adequate.



DAC-02/DAC-03/DAC-05

10-BIT-PLUS-SIGN VOLTAGE-OUTPUT
D/A CONVERTERS

Precision Monolithics Inc.

FEATURES

- Complete Includes Reference and Op Amp
- Compact Single 18-Pin DIP Package
- Bipolar Output ($\pm 10V$) Sign-Magnitude Coding
- DAC-03 — Unipolar Only; +5V or +10V
- Monotonicity Guaranteed
- Nonlinearity ± 1 LSB
- Fast 2.0 μ s Settling Time
- Stable Full-Scale Tempco 60ppm/ $^{\circ}$ C
- Low Power Consumption 300mW Max
- TTL, CMOS Compatible Inputs
- MIL-STD-883 Class B Processing Available on DAC-05

ORDERING INFORMATION †

PACKAGE: 18-PIN HERMETIC DIP				
MONO-TONICITY BITS	MILITARY TEMP*	COMMERCIAL TEMP		
10	DAC05AX	DAC02ACX	DAC03ADX	DAC05EX
9	—	DAC02BCX	DAC03BDX	—
8	DAC05CX	DAC02CCX	DAC03CDX	DAC05GX
7	—	DAC02DDX	DAC03DDX	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

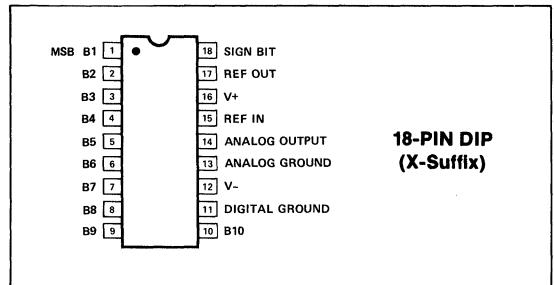
GENERAL DESCRIPTION

The DAC-02 and DAC-05 are complete 10-bit plus sign D/A converters on a single monolithic chip. All elements of a complete sign-magnitude DAC are included; precision vol-

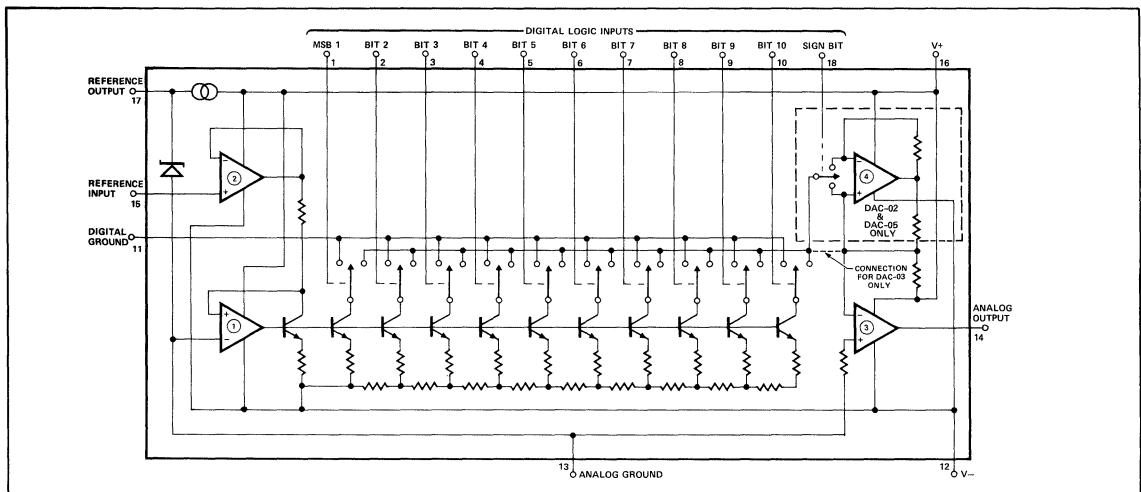
tage reference, current steering logic, current sources, R-2R resistor network, logic-controlled polarity switch, and high speed internally-compensated output op amp. Monotonicity guaranteed over the entire temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The wide power supply range, low power consumption, wide logic input compatibility and sign-magnitude coding assures utility in a wide range of applications including CRT displays, data acquisition systems, A/D converters, servo positioning controls, and audio digitizing/reconstruction systems.

The DAC-03 is similar in construction to the DAC-02/DAC-05 except for a unipolar only output. This device is intended for low cost, limited temperature range applications, with the same general specifications as its premium counterparts.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note)

Operating Temperature Range	
DAC-05A, C	-55°C to +125°C
DAC-02 and DAC-03, All	
DAC-05E, G	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
V+ Supply to Analog Ground	0 to +18V
V- Supply to Analog Ground	0 to -18V
Analog Ground to Digital Ground	0 to ±0.5V
Logic Inputs to Digital Ground	-5V to (V+ - 0.7V)
Internal Reference Output Current	300µA
Reference Input Voltage	0 to +10V
Internal Power Dissipation	500mW

Lead Temperature (Soldering, 60 sec) 300°C
 Output Short Circuit Duration Indefinite
 (Short circuit may be to ground or either supply.)

NOTE: For ambient temperatures above 100°C derate 100mW/°C.

OUTPUT VOLTAGE RANGE SELECTION TABLE

PRODUCT	OUTPUT VOLTAGE RANGE	ADD AS SUFFIX TO PART NO.
DAC02	±10V	1
DAC03	0 to +10V	1
DAC03	0 to +5V	2
DAC05	±10V	1

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0 \leq T_A \leq +70^\circ C$ for DAC-02 and DAC-05E & G, $T_A = 25^\circ C$ for DAC-03 and $-55 \leq T_A \leq +125^\circ C$ for DAC-05A & C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-02	DAC-03	DAC-05	MIN	TYP	MAX	UNITS
Monotonicity			AC	AD	A/E	10	—	—	Bits
			BC	BD		9	—	—	
			CC	CD	C/G	8	—	—	
			DD	DD		7	—	—	
Nonlinearity	NL		AC/BC	AD/BD		—	—	±0.1	% FS
			CC	CD	A/E	—	—	±0.2	
			DD	DD		—	—	±0.4	
Full-Scale Tempo	T _C	INT REF	AC/BC/CC	ALL	A	—	—	±60	ppm/°C
					E/G	—	±45	±100	
			DD	C	—	±60	±120		
						—	—	±150	
Full-Scale Tempo	T _C	EXT REF	ALL		ALL	—	±30	—	ppm/°C
				ALL	—	±40	—		
Settling Time	t _S	To 1/2 LSB, 10V Step (Note 4)	ALL	ALL	ALL	—	2	—	µs
Full Range Output Voltage (Note 1)	V _{FR}	V _{FR+} (SB High) V _{FR-} (SB Low) DAC-03 +10V +5V	ALL		ALL	+10	—	+11.5	Volts
			ALL		ALL	-11.5	—	-10	
			ALL	ALL	ALL	+10	—	+11.5	
Zero-Scale Offset	V _{ZS}	SB High. All other logic inputs low. T _A = 25°C		ALL	ALL	—	±1	±5	mV
			ALL		ALL	—	±1	±10	
			ALL		ALL	—	±5	±10	
Zero-Scale Symmetry	V _{ZSS}	(Note 2)	AC/BC/CC			—	±1	±5	mV
			DD	N/A		—	±1	±10	
			ALL		ALL	—	±4	±10	
Full Range Bipolar Symmetry	V _{FRS}	V _{FR+} - V _{FR-} (Note 3) T _A = Min or Max T _A = 25°C	AC/BC/CC	N/A		—	±30	±60	mV
			DD		ALL	—	±30	±80	
			ALL		ALL	—	±20	±70	
Reference Input Bias Current	I _B		ALL	ALL	ALL	—	100	—	nA
Reference Input Impedance	Z _{IN}		ALL	ALL	ALL	—	200	—	MΩ
Reference Input Slew Rate	SR		ALL	ALL	E/G	—	1.5	—	V/µs
			ALL	ALL	A/C	—	2	—	
Reference Output Voltage	V _{REF}		ALL	ALL	ALL	—	6.7	—	Volts

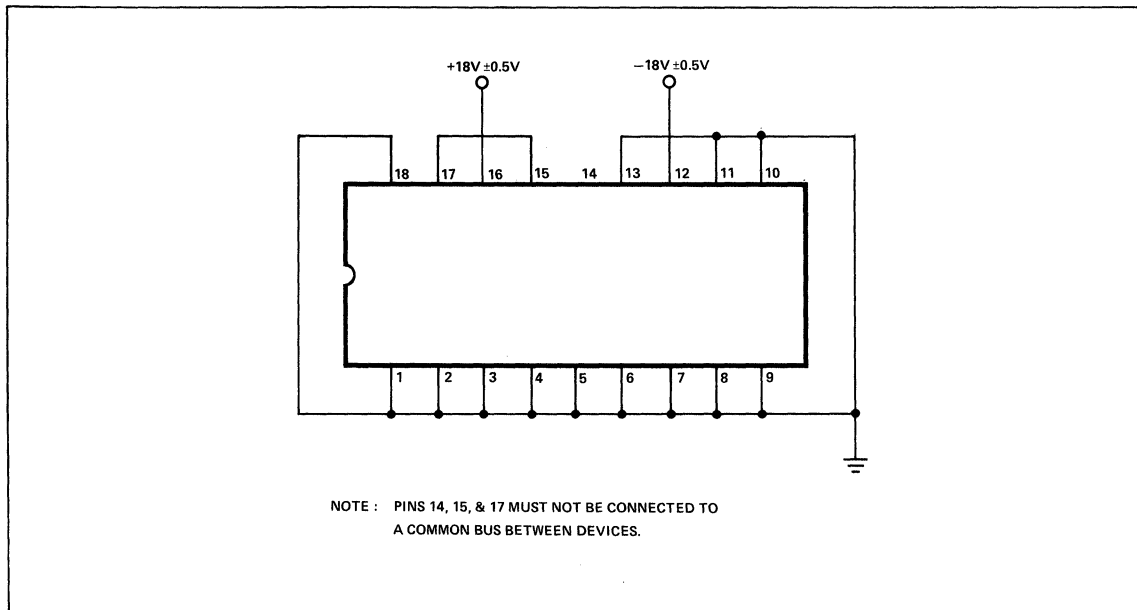


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0 \leq T_A \leq +70^\circ C$ for DAC-02 and DAC-05E & G, $T_A = 25^\circ C$ for DAC-03 and $-55 \leq T_A \leq +125^\circ C$ for DAC-05A & C, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-02	DAC-03	DAC-05	MIN	TYP	MAX	UNITS
Logic Input Current	I_{IN}	Each input -5V to (V+ - 0.7)V	ALL	ALL	ALL	—	± 1	± 10	μA
Logic Input 0	V_{INL}		ALL	ALL	ALL	—	—	0.8	Volts
Logic Input 1	V_{INH}		ALL	ALL	ALL	2	—	—	
Positive Supply Current	I^+	SB High. All other logic inputs low.	AC/BC/CC DD	ALL	ALL	—	+7	+10	mA
Negative Supply Current	I^-	SB High. All other logic inputs low.	AC/BC/CC DD	ALL	ALL	—	-9	-10	mA
Power Supply Sensitivity	P_{SS}	$V_S = \pm 12$ to $\pm 18V$ $T_A = \text{Min to Max}$ $T_A = 25^\circ C$	AC/BC/CC DD	ALL	ALL	—	± 0.015	± 0.05	% V_{FS}/V
Power Dissipation	P_d	$I_{OUT} = 0$ $T_A = 25^\circ C$ $T_A = \text{Min to Max}$	AC/BC/CC DD	ALL	ALL	—	225	300	mW
Output Drive Current	I_O	Guaranteed by V_{FR} test	ALL	ALL	ALL	—	—	5	mA

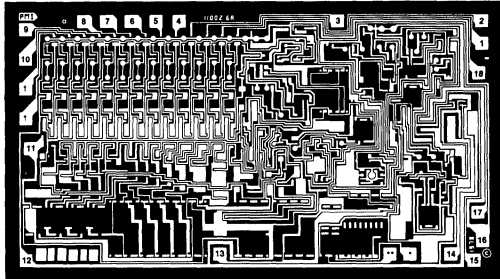
NOTES:

- Reference output terminal connected directly to reference input terminal, $R_L = 2k\Omega$ for 10V devices, $R_L = 1k\Omega$ for 5V devices, all logic inputs $\geq 2.0V$.
- Zero-scale symmetry is the change in the output voltage produced by switching the sign-bit with all logic bits low ($V_{ZS+} - V_{ZS-}$).
- Full-scale bipolar symmetry is the magnitude of the difference between V_{FR+} and $|V_{FR-}|$.
- Guaranteed by design.

BURN-IN TEST CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.163 × 0.090 inch; 14,670 sq. mils
(4.14 × 2.286 mm, 9.464 sq. mm)

- | | |
|--------------|--------------------|
| 1. BIT 1-MSB | 10. BIT 10 |
| 2. BIT 2 | 11. DIGITAL GROUND |
| 3. BIT 3 | 12. V- |
| 4. BIT 4 | 13. ANALOG GROUND |
| 5. BIT 5 | 14. ANALOG OUTPUT |
| 6. BIT 6 | 15. REF IN |
| 7. BIT 7 | 16. V+ |
| 8. BIT 8 | 17. REF OUT |
| 9. BIT 9 | 18. SIGN BIT |

For additional DICE information refer to 1986 Data Book, Section 2.

NOTE:

Voltage output range programmable by connecting *(10V) to analog output for 10 volt range. Jumps from ** (5V) to analog output for 5 volt range. † Bits 11 & 12 (not normally used)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ and +10V full-scale output, unless otherwise noted.

PARAMETER	CONDITIONS	DAC-02-N LIMIT	DAC-02-G LIMIT	UNITS
Resolution (Bits 11 and 12 Not Normally Used)	Bipolar Output	13	13	Bits MAX
	Unipolar Output	12	12	
Monotonicity		9	8	Bits MIN
Nonlinearity		±0.1	±0.2	% FS MAX
Zero-Scale Offset	Sign Bit High, All Other Inputs Low	±10	±10	mV MAX
Zero-Scale Symmetry	±10V Full-Scale	±5	±5	mV MAX
Full-Scale Bipolar Symmetry	±10V Full-Scale	±60	±60	mV MAX
Power Supply Rejection	$V_S = \pm 12V$ to $\pm 18V$	0.05	0.05	% V_{FS}/V MAX
Power Dissipation	$I_{OUT} = 0$	300	300	mW MAX
Logic Input "0"		0.8	0.8	V MAX
Logic Input "1"		2	2	V MIN
Full Range Output Voltage	Sign-Bit	±11.5	±11.5	V MAX
	High or Low	±10	±10	V MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and +10V full-scale output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-02-N TYPICAL	DAC-02-G TYPICAL	UNITS
Full-Scale Tempco	TCV_{FS}	Internal Reference	60	60	ppm/ $^\circ C$
Settling Time ($T_A = 25^\circ C$)	t_s	To $\pm 1/2$ LSB 10 Volt Step	2	2	μs
Logic Input Current	I_{IN}	$T_A = 25^\circ C$	1	1	μA

NOTE:

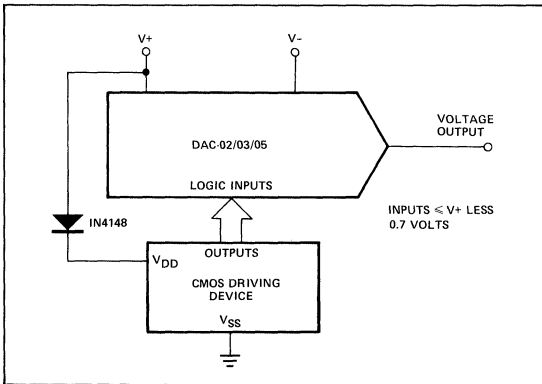
When ordering DICE in this series, use DAC-02 numbers and grades above.

TYPICAL APPLICATIONS

The DAC-02's, DAC-03's and DAC-05's logic input stages require about $1\mu\text{A}$ and are capable of operation with inputs between -5 volts and $V+$ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

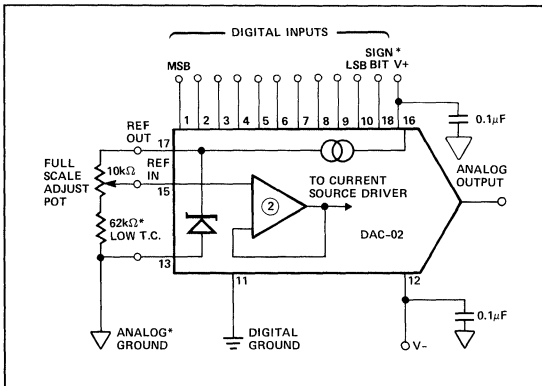
In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_D to $V+$ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-02, DAC-03 and DAC-05 require either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

CMOS LOGIC INTERFACE CIRCUIT



CONNECTION INFORMATION

FULL-SCALE ADJUSTMENT CIRCUIT



FULL-SCALE ADJUSTMENT

Full-scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results

will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of $\leq 72\text{k}\Omega$ may be used.

REFERENCE INPUT BYPASS

Lowest noise and fastest settling operation will be obtained by bypassing the reference input to analog ground with a $0.01\mu\text{F}$ disk capacitor.

GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably near the DAC-02, DAC-03 and DAC-05 package, so that the large digital currents do not flow through the analog ground path.

APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATIONS

For applications not requiring full 10-bit resolution, unused logic inputs should be tied to ground.

UNIPOLAR OPERATION

Operation as a 10-bit straight binary converter may be implemented by permanently tying the sign-bit to $+5\text{V}$ (for positive full-scale output) or to ground (for negative full-scale output). In the DAC-03 only, Pin 18 unipolar enable is tied to Pin 17.

POWER SUPPLIES

The DAC-02, DAC-03 and DAC-05 will operate within specifications for power supplies ranging from $\pm 12\text{V}$ to $\pm 18\text{V}$. Power supplies should be bypassed near the package with a $0.1\mu\text{F}$ disk capacitor.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF .

REFERENCE OUTPUT

For best results, reference output current should not exceed $100\mu\text{A}$.

USE WITH EXTERNAL REFERENCES

Positive-polarity external reference voltages referred to analog ground may be applied to the reference input terminal to improve full-scale tempco, to provide tracking to other system elements, or to slave a number of DAC-02's, DAC-03's and DAC-05's to the reference output of any one of them. This reference voltage should be between $+5\text{V}$ to $+7\text{V}$ for optimum performance.

SIGN PLUS MAGNITUDE CODING TABLE (DAC-02, DAC-03 and DAC-05)

	SIGN-BIT MSB										LSB
+ FULL SCALE	1	1	1	1	1	1	1	1	1	1	1
+ HALF-SCALE	1	1	0	0	0	0	0	0	0	0	0
ZERO-SCALE (+)	1	0	0	0	0	0	0	0	0	0	0
ZERO-SCALE (-)	0	0	0	0	0	0	0	0	0	0	0
- HALF-SCALE	0	1	0	0	0	0	0	0	0	0	0
- FULL-SCALE	0	1	1	1	1	1	1	1	1	1	1



DAC-06

TWO'S-COMPLEMENT 10-BIT VOLTAGE-OUTPUT D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- **Complete** Includes Reference and Op Amp
- **Compact** Single 18-Pin DIP Package
- **Bipolar Output** Two's Complement Coding
- **Monotonicity Guaranteed**
- **Nonlinearity** ± 1 LSB
- **Fast** $1.5\mu\text{s}$ Settling Time
- **Low Power Consumption** 300mW Max
- **TTL, CMOS Compatible Inputs**

ORDERING INFORMATION†

MONO-TONICITY BITS	PACKAGE 18-PIN HERMETIC DIP	
	MILITARY TEMP	COMMERCIAL TEMP
10	—	DAC-06EX
9	DAC-06BX*	DAC-06FX
8	DAC-06CX*	DAC-06GX

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

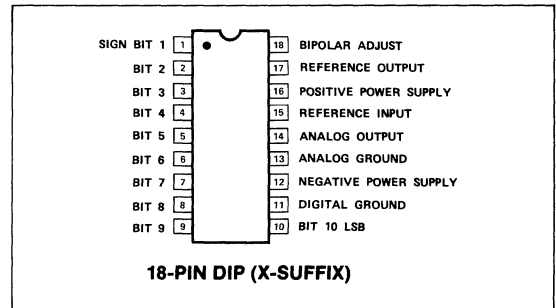
†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

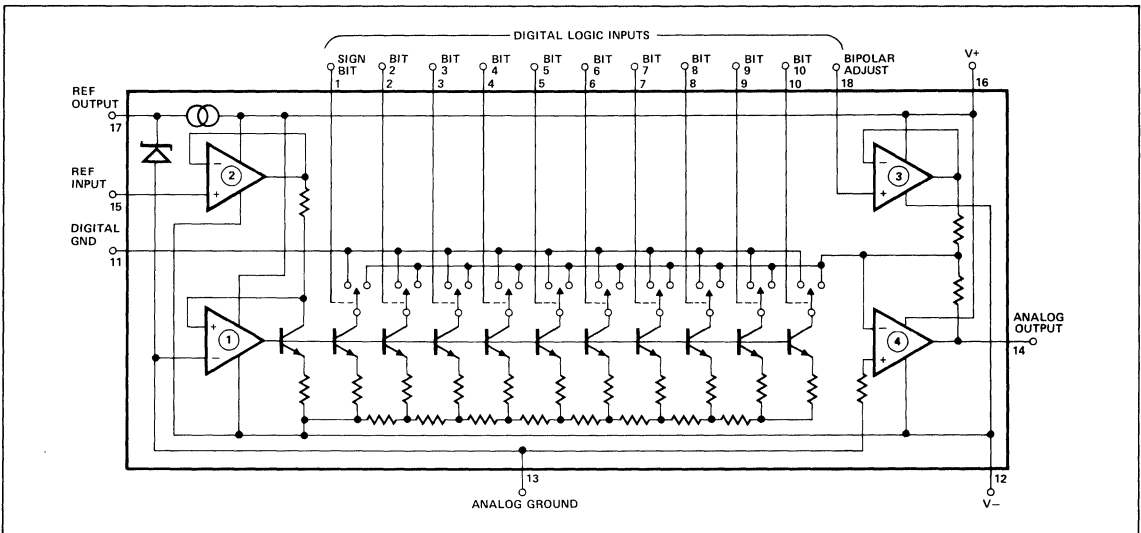
The DAC-06 is a complete 10-bit two's complement D/A converter on a single 90 x 163 mil monolithic chip. All elements of a complete bipolar output two's complement DAC

are included — precision voltage reference, current steering logic, current sources, R-2R resistor network, bipolar offset circuit and high speed internally compensated output op amp. Monotonicity guaranteed over the entire operating temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The user may also easily implement one's complement, straight offset binary, or unipolar operation. The $\pm 12\text{V}$ to $\pm 18\text{V}$ power supply range, low power consumption, TTL and CMOS compatibility, wide logic input compatibility and adaptable logic coding capability assure utility in a wide range of applications.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



DIGITAL-TO-ANALOG CONVERTERS

**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature Range	
DAC-06B, C	-55°C to +125°C
DAC-06E, F, G	0°C to +70°C
DICE Junction Temperature (T _j)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
V+ Supply to Analog Ground	0 to +18V
V- Supply to Analog Ground	0 to -18V
Analog Ground to Digital Ground	0 to ±0.5V

Logic Inputs to Digital Ground	-5V to (V+ - 0.7)V
Internal Reference Output Current	300μA
Reference Input Voltage	0 to +10V
Bipolar Offset Input Voltage	0 to +10V
Internal Power Dissipation	500mW
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration	Indefinite
(Short circuit may be to ground or either supply)	

ELECTRICAL CHARACTERISTICS at V_S = ±15V; -55°C ≤ T_A ≤ +125°C for DAC-06B & C; and 0°C ≤ T_A ≤ +70°C for DAC-06E, F & G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-06	MIN	TYP	MAX	UNITS	
Resolution			All	10	—	—	Bits	
Monotonicity			E	10	—	—	Bits	
			B/F	9	—	—		
			C/G	8	—	—		
Nonlinearity	NL	T _A = 25°C	E	—	—	±0.1	% FS	
			B/F	—	—	±0.2		
			C/G	—	—	±0.4		
		T _A = Full Temp.	E	—	—	±0.2		
			B/F	—	—	±0.3		
			C/G	—	—	±0.5		
Full-Scale Tempco	TCV _{FS}	Total Internal Ref Connected	B	—	±45	±90	ppm/°C	
			E/F/G	—	±45	±100		
		Zero Drift Ext Ref Applied	C	—	±60	±120		
			All	—	±30	—		
Settling Time	t _S	To ±1/2 LSB, 10V Step	All	—	1.5	—	μs	
Unipolar Zero-Scale Output	V _{ZS}	Short Pin 18 to Ground (Note 1)	T _A = 25°C	All	—	±1	±5	mV
			T _A = Full Temp.	All	—	±2	±10	mV
Bipolar Offset Voltage	BP Off	Connect Pins 15, 17 & 18 (Note 3)	All	-5	—	+2.5	% Range	
Full Range Output Voltage	V _{FR}	Connect Pin 15 to 17 (Note 2) R _L = 2kΩ	All	10	—	11.5	V	
Reference Input Bias Current	I _B		All	—	100	—	nA	
Reference Input Impedance	Z _{IN}		All	—	200	—	MΩ	
Reference Input Slew Rate	SR		All	—	1.5	—	V/μs	
Reference Output Voltage	V _{REF}		All	—	6.7	—	V	
Logic Input Current	I _{IN}	Each Input -5V to (V+ - 0.7)V	All	—	1	10	μA	
Logic Input "0"	V _{INL}		All	—	—	0.8	V	
Logic Input "1"	V _{INH}		All	2	—	—	V	
Power Supply Sensitivity	P _{SS}	V _S = ±12V to ±18V	T _A = 25°C	All	—	±0.02	±0.05	% FS/V
			T _A = Full Temp.	All	—	±0.02	±0.1	% FS/V
Supply Current	I+	T _A = 25°C	All	—	7	10	mA	
	I-		All	—	-9	-10	mA	
Power Dissipation	P _D		T _A = 25°C	All	—	250	300	mW
			T _A = Full Temp.	All	—	—	350	mW

NOTES:

- May be operated in the 0 to +10V unipolar mode by shorting Pin 18 to Ground.
- V_{FR} = |V_{FR+}| + |V_{FR-}| and is trimmable to exactly 10V range with the circuit shown in typical applications.
- Bipolar offset voltage is trimmable to exact two's or one's complement condition with the circuit shown in typical applications.

**TYPICAL APPLICATIONS****ADJUSTING FOR TWO'S COMPLEMENT CODING**

1. Connect Full-Scale Adjust and Bipolar Adjust Circuitry as shown in figure.
2. Turn all bits OFF ($V_{FS-} - 1\text{LSB}$) = 1000000000
3. Adjust Bipolar Pot for V_{FS} at output -5.000V
4. Turn all bits ON (V_{FR+}) = 0111111111
5. Adjust Full-Scale Pot for desired V_{FR+} value +4.990V
6. Check Zero-Scale Reading (V_{ZS}) = 0000000000
If this reading is outside desired V_{ZS} range, readjust Bipolar Pot until the output reads 0.0000V.

TWO'S COMPLEMENT CODING TABLE

	INPUT										IDEAL OUTPUT
	MSB									LSB	
$V_{FS+} - 1\text{LSB}$	0	1	1	1	1	1	1	1	1	1	+4.990V
$V_{FS+} - 2\text{LSB}$	0	1	1	1	1	1	1	1	1	0	+4.980V
+1LSB	0	0	0	0	0	0	0	0	0	1	+0.010V
Zero	0	0	0	0	0	0	0	0	0	0	0.000V
-1LSB	1	1	1	1	1	1	1	1	1	1	-0.010V
$V_{FS-} + 1\text{LSB}$	1	0	0	0	0	0	0	0	0	1	-4.990V
V_{FS-}	1	0	0	0	0	0	0	0	0	0	-5.000V

ADJUSTING FOR ONE'S COMPLEMENT CODING

1. Connect Full-Scale Adjust and Bipolar Adjust Circuitry as shown in above figure.
2. Turn all bits OFF (V_{FR-}) = 1000000000
3. Adjust Bipolar Pot for V_{FR-} at output -5.0000V
4. Turn all bits ON (V_{FR+}) = 0111111111
5. Adjust Full-Scale Pot for desired V_{FR+} value +5.0000V

ONE'S COMPLEMENT CODING TABLE

	INPUT										IDEAL OUTPUT
	MSB									LSB	
$V_{FS+} - 1\text{LSB}$	0	1	1	1	1	1	1	1	1	1	+5.000V
$V_{FS+} - 2\text{LSB}$	0	1	1	1	1	1	1	1	1	0	+4.990V
+0	0	0	0	0	0	0	0	0	0	0	+0.005V
-0	1	1	1	1	1	1	1	1	1	1	-0.005V
$V_{FS-} + 2\text{LSB}$	1	0	0	0	0	0	0	0	0	1	-4.990V
$V_{FS-} + 1\text{LSB}$	1	0	0	0	0	0	0	0	0	0	-5.000V

Note that two zero states will straddle ($\pm 1/2$ LSB) the true zero. Therefore the DAC will give symmetrical outputs for both positive and negative full-scale.

REFERENCE OUTPUT

For best results, reference output current should not exceed $100\mu\text{A}$.

POWER SUPPLIES

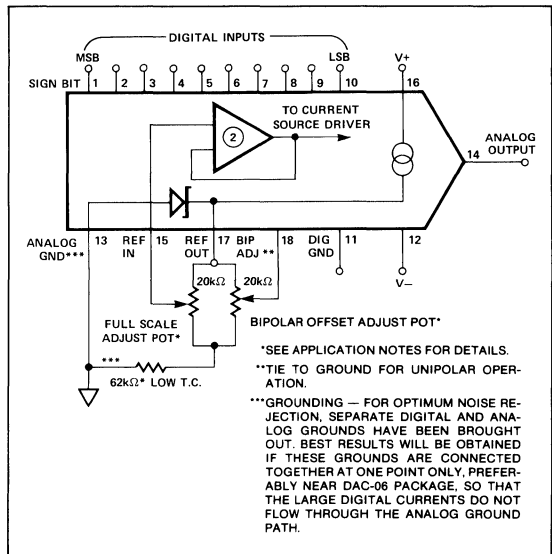
The DAC-06 will operate within specifications for power supplies ranging from $\pm 12\text{V}$ to $\pm 18\text{V}$. Power supplies should be bypassed near the package with a $0.1\mu\text{F}$ disk capacitor. Chip users should connect the substrate to $V-$.

GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the DAC-06 package, so that large digital currents do not flow through the analog ground path.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF .

FULL-SCALE OUTPUT RANGE AND BIPOLAR OFFSET ADJUSTMENT CIRCUIT**EXTERNAL ADJUSTMENT NETWORK**

Full-scale output range and bipolar offset may be adjusted by using the circuit shown in the figure above. Best results will be obtained when low tempco pots and resistors are used, or if pot and resistor tempcos match.

CODE CONVERSION TO OFFSET BINARY

Offset binary coding is exactly the same as two's complement coding except that the most significant bit occurs in true, rather than inverted form and the output states are relabeled. To convert the DAC-06 to offset binary code operation, simply place a logic inverter in series with the MSB input (Pin 1) and invert the MSB value shown in steps 2, 4 and 6 of the two's complement adjustment procedure shown above.

OFFSET BINARY CODING TABLE

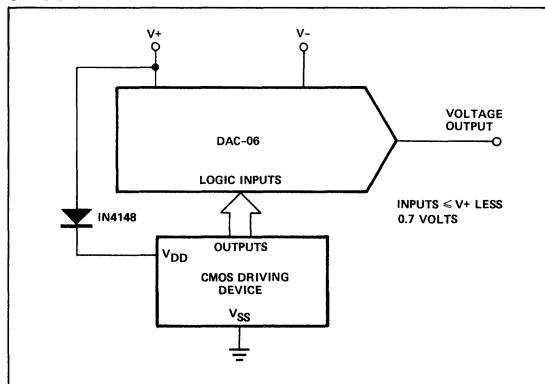
	INPUT										IDEAL	
	MSB									LSB	OUTPUT	
$V_{FS+} - 1\text{LSB}$	1	1	1	1	1	1	1	1	1	1	1	+4.990V
$V_{FS+} - 2\text{LSB}$	1	1	1	1	1	1	1	1	1	1	0	+4.980V
ZERO	1	0	0	0	0	0	0	0	0	0	0	0.00
-1LSB	0	1	1	1	1	1	1	1	1	1	1	-0.005V
$V_{FS-} + 1\text{LSB}$	0	0	0	0	0	0	0	0	0	0	1	-4.990V
V_{FS-}	0	0	0	0	0	0	0	0	0	0	0	-5.000V

INTERFACING WITH CMOS LOGIC

The DAC-06 logic input stages require about $1\mu\text{A}$ and are capable of operation with inputs between -5 volts and $V+$ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where

the CMOS logic and D/A converter must use the same positive power supply.

In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_D to $V+$ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-06 requires either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

CMOS LOGIC INTERFACE CIRCUIT




DAC-08

8-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

Precision Monolithics Inc.

FEATURES

- **Fast Settling Output Current** 85ns
- **Full-Scale Current Prematched to ± 1 LSB**
- **Direct Interface to TTL, CMOS, ECL, HTL, PMOS**
- **Nonlinearity to .0.1% Maximum Over Temperature Range**
- **High Output Impedance and Compliance** -10V to +18V
- **Complementary Current Outputs**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Low FS Current Drift** ± 10 ppm/ $^{\circ}$ C
- **Wide Power Supply Range** ± 4.5 V to ± 18 V
- **Low Power Consumption** 33mW @ ± 5 V
- **Low Cost**

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic digital-to-analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct

interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic input.

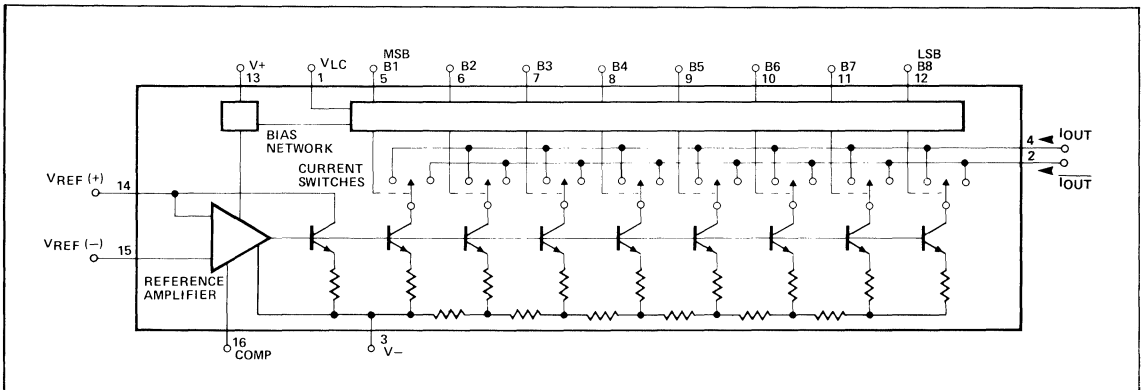
High voltage compliance complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as $\pm 0.1\%$ over the entire operating temperature range are available. Device performance is essentially unchanged over the ± 4.5 to ± 18 V power supply range, with 33mW power consumption attainable at ± 5 V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1μ s A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



DIGITAL-TO-ANALOG CONVERTERS

11

**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature	DAC-08AQ, Q	-55°C to +125°C
	DAC-08HQ, EQ, CQ, HP, EP, CP	0°C to +70°C
DICE Junction Temperature (T _J)		-65°C to +150°C
Storage Temperature Q Package		-65°C to +150°C
Storage Temperature P Package		-65°C to +125°C
Power Dissipation		500mW
Derate above 100°C		10mW/°C
Lead Temperature (Soldering, 60 sec)		300°C
V+ Supply to V- Supply		36V

Logic Inputs	V- to V+ plus 36V
V _{LC}	V- to V+
Analog Current Outputs (at V _S = 15V)	4.25mA
Reference Input (V ₁₄ to V ₁₅)	V- to V+
Reference Input Differential Voltage (V ₁₄ to V ₁₅)	±18V
Reference Input Current (I ₁₄)	5.0mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 2.0mA, -55°C ≤ T_A ≤ +125°C for DAC-08/08A, 0°C ≤ T_A ≤ +70°C for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT}.

PARAMETER	SYMBOL	CONDITIONS	DAC-08A/H			DAC-08/E			DAC-08C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			8	—	—	8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	8	—	—	Bits
Nonlinearity			—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time	t _S	To ±1/2 LSB, all bits switched ON or OFF, T _A = 25°C, (Note)	—	85	135	—	85	150	—	85	150	ns
Propagation Delay												
Each bit	t _{PLH}	T _A = 25°C	—	35	60	—	35	60	—	35	60	ns
All bits switched	t _{PHL}	(Note)	—	35	60	—	35	60	—	35	60	
Full-Scale Tempco (Note)	TC _{1FS}	DAC-08E	—	±10	±50	—	±10	±80	—	±10	±80	ppm/°C
Output Voltage Compliance (True Compliance)	V _{OC}	Full-Scale current change < 1/2 LSB, R _{OUT} > 20MΩ typical	-10	—	+18	-10	—	+18	-10	—	+18	Volts
Full Range Current	I _{FR4}	V _{REF} = 10.000V R ₁₄ , R ₁₅ = 5.000kΩ T _A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I _{FRS}	I _{FR4} - I _{FR2}	—	±0.5	±4	—	±1	±8	—	±2	±16	μA
Zero-Scale Current	I _{ZS}		—	0.1	1	—	0.2	2	—	0.2	4	μA
Output Current Range	I _{OR1} I _{OR2}	R ₁₄ , R ₁₅ = 5.000kΩ V _{REF} = +15.0V, V- = -10V V _{REF} = +25.0V, V- = -12V	2.1	—	—	2.1	—	—	2.1	—	—	mA
Output Current Noise		I _{REF} = 2mA	—	25	—	—	25	—	—	25	—	nA
Logic Input Levels												
Logic "0"	V _{IL}	V _{LC} = 0V	—	—	0.8	—	—	0.8	—	—	0.8	Volts
Logic Input "1"	V _{IL}		2	—	—	2	—	—	2	—	—	
Logic Input Current												
Logic "0"	I _{IL}	V _{LC} = 0V V _{IN} = -10V to +0.8V	—	-2	-10	—	-2	-10	—	-2	-10	μA
Logic Input "1"	I _{IH}	V _{IN} = 2.0V to 18V	—	0.002	10	—	0.002	10	—	0.002	10	
Logic Input Swing	V _{IS}	V- = -15V	-10	—	+18	-10	—	+18	-10	—	+18	Volts
Logic Threshold Range	V _{THR}	V _S = ±15V, (Note)	-10	—	+13.5	-10	—	+13.5	-10	—	+13.5	Volts
Reference Bias Current	I ₁₅		—	-1	-3	—	-1	-3	—	-1	-3	μA
Reference Input Slew Rate	dI/dt	R _{EQ} = 200Ω See fast pulsed R _L = 100Ω ref. info. C _C = 0pF following. (Note)	4	8	—	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	PSSI _{FS+} PSSI _{FS-}	V+ = 4.5V to 18V V- = -4.5V to -18V I _{REF} = 1.0mA	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	%ΔI _O /%ΔV+
			—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	%ΔI _O /%ΔV-

NOTE: Guaranteed by design.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $-55^\circ C \leq T_A \leq +125^\circ C$ for DAC-08/08A, $0^\circ C \leq T_A \leq +70^\circ C$ for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT-} . (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-08A/H			DAC-08/E			DAC-08C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Current	I+	$V_S = \pm 5V$, $I_{REF} = 1.0mA$	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
	I-		—	-4.3	-5.8	—	-4.3	-5.8	—	-4.3	-5.8	
	I+	$V_S = +5V$, $-15V$, $I_{REF} = 2.0mA$	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
	I-		—	-6.4	-7.8	—	-6.4	-7.8	—	-6.4	-7.8	
	I+	$V_S = \pm 15V$, $I_{REF} = 2.0mA$	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
	I-		—	-6.5	-7.8	—	-6.5	-7.8	—	-6.5	-7.8	
Power Dissipation	P_d	$\pm 5V$, $I_{REF} = 1.0mA$	—	33	48	—	33	48	—	33	48	mW
		$+5V$, $-15V$, $I_{REF} = 2.0mA$	—	108	136	—	103	136	—	108	136	
		$\pm 15V$, $I_{REF} = 2.0mA$	—	135	174	—	135	174	—	135	174	

NOTE: Guaranteed by design.

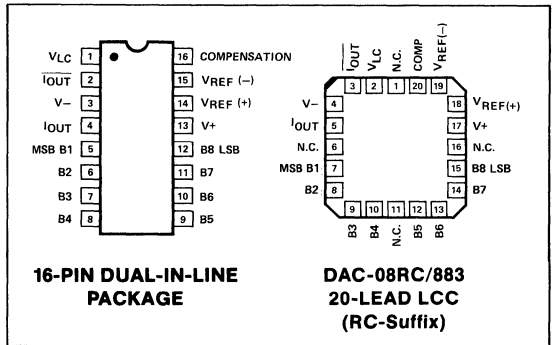
ORDERING INFORMATION†

NL	16-PIN DUAL-IN-LINE PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC	PLASTIC	LCC	
0.1%	DAC08AQ*			MIL
	DAC08HQ	DAC08HP		COM
0.19%	DAC08Q*		DAC08RC/883	MIL
	DAC08EQ	DAC08EP		COM
0.39%	DAC08CQ	DAC08CP		COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

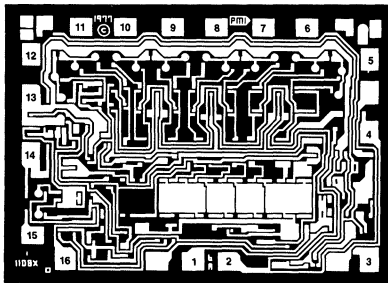
PIN CONNECTIONS



DIGITAL-TO-ANALOG CONVERTERS



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.085 × 0.062 inch, 5,270 sq. mils
(2.159 × 1.575 mm, 3.4 sq. mm)

- | | |
|----------------|-------------------|
| 1. V_{LC} | 9. BIT 5 |
| 2. I_{OUT} | 10. BIT 6 |
| 3. V^- | 11. BIT 7 |
| 4. I_{OUT} | 12. BIT 8 (LSB) |
| 5. BIT 1 (MSB) | 13. V^+ |
| 6. BIT 2 | 14. $V_{REF} (+)$ |
| 7. BIT 3 | 15. $V_{REF} (-)$ |
| 8. BIT 4 | 16. COMP |

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 125^\circ C$ for DAC-08NT, DAC-08GT devices; $T_A = 25^\circ C$ for DAC-08N, DAC-08G and DAC-08GR devices, unless otherwise noted. Output characteristics apply to both I_{OUT} and I_{OUT} .

PARAMETER	SYMBOL	CONDITIONS	DAC-08NT LIMIT	DAC-08N LIMIT	DAC-08GT LIMIT	DAC-08G LIMIT	DAC-08GR LIMIT	UNITS
Resolution			8	8	8	8	8	Bits MIN
Monotonicity			8	8	8	8	8	Bits MIN
Nonlinearity			± 0.1	± 0.1	± 0.19	± 0.19	± 0.39	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB	+18 -10	+18 -10	+18 -10	+18 -10	+18 -10	Volts MAX Volts MIN
Full-Scale Current	I_{FS4} or I_{FS2}	$V_{REF} = 10.000V$ $R_{14}, R_{15} = 5.000k\Omega$	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full-Scale Symmetry	I_{FSS}		± 8	± 8	± 8	± 8	± 16	μA MAX
Zero-Scale Current	I_{ZS}		2	2	4	4	4	μA MAX
Output Current Range	I_{FS1} or I_{FS2}	$V^- = -10V$, $V_{REF} = +15V$ $V^- = -12V$, $V_{REF} = +25V$ $R_{14}, R_{15} = 5.000k\Omega$	2.1 4.2	2.1 4.2	2.1 4.2	2.1 4.2	2.1 4.2	mA MIN mA MIN
Logic Input "0"	V_{IL}		0.8	0.8	0.8	0.8	0.8	V MAX
Logic Input "1"	V_{IH}		2	2	2	2	2	V MIN
Logic Input Current		$V_{LC} = 0V$						
Logic "0"	I_{IL}	$V_{IN} = -10V$ to $+0.8V$	± 10	± 10	± 10	± 10	± 10	μA MAX
Logic "1"	I_{IH}	$V_{IN} = 2.0V$ to $18V$	± 10	± 10	± 10	± 10	± 10	μA MAX
Logic Input Swing	V_{IS}	$V^- = -15V$	+18 -10	+18 -10	+18 -10	+18 -10	+18 -10	V MAX V MIN
Reference Bias Current	I_{15}		-3	-3	-3	-3	-3	μA MAX
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	$V^+ = 4.5V$ to $18V$ $V^- = -4.5V$ to $-18V$ $I_{REF} = 1.0mA$	0.01	0.01	0.01	0.01	0.01	%FS/%V MAX
Power Supply Current	I^+	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	3.8 -7.8	3.8 -7.8	3.8 -7.8	3.8 -7.8	3.8 -7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	174	174	174	174	174	mW MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

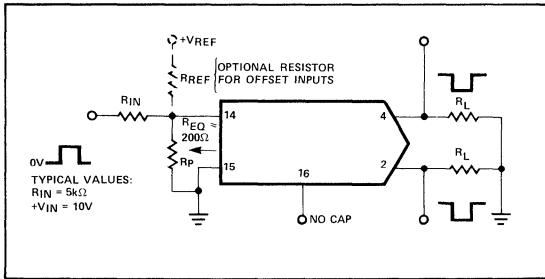


TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $I_{REF} = 2.0mA$, unless otherwise noted. Output characteristics apply to both I_{OUT} and I_{OUT} .

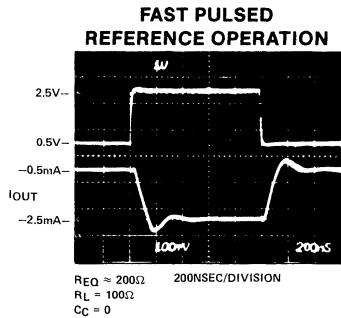
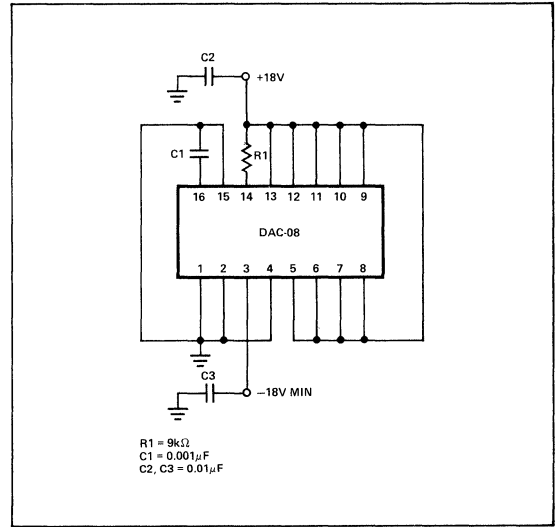
PARAMETER	SYMBOL	CONDITIONS	ALL GRADES	
			TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	$mA/\mu s$
Propagation Delay	t_{PLH}, t_{PHL}	$T_A = 25^\circ C$, Any Bit	35	ns
Settling Time	t_S	To $\pm 1/2$ LSB, All Bits Switched ON or OFF, $T_A = 25^\circ C$	85	ns

NOTE:
For DAC08NT & GT 25°C characteristics, see DAC08N & G characteristics respectively.

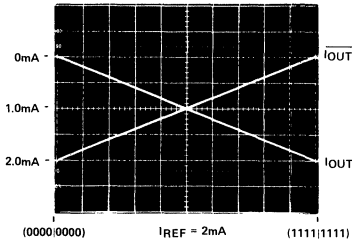
PULSED REFERENCE OPERATION



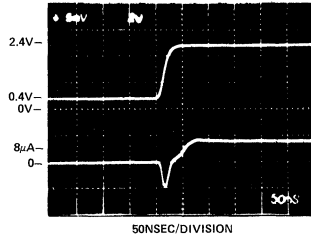
BURN-IN CIRCUIT



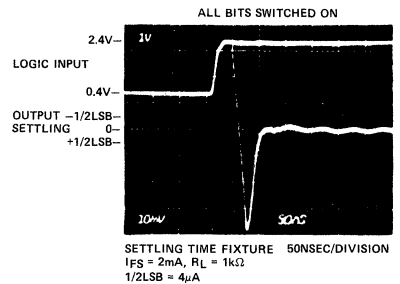
TRUE AND COMPLEMENTARY OUTPUT OPERATION



LSB SWITCHING



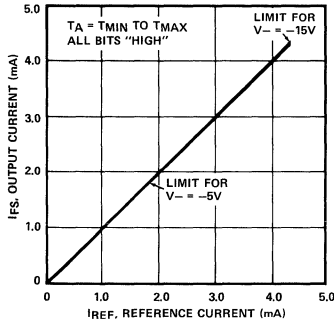
FULL-SCALE SETTLING TIME



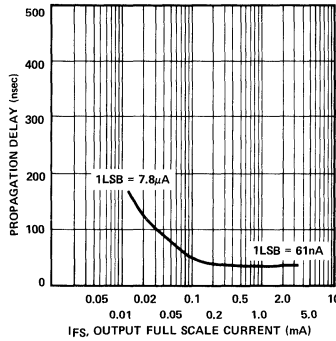


TYPICAL PERFORMANCE CHARACTERISTICS

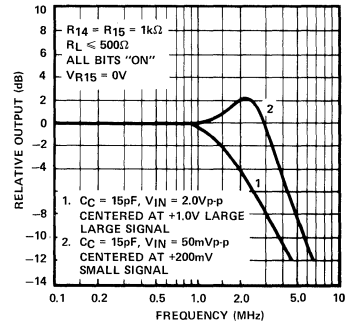
FULL-SCALE CURRENT vs REFERENCE CURRENT



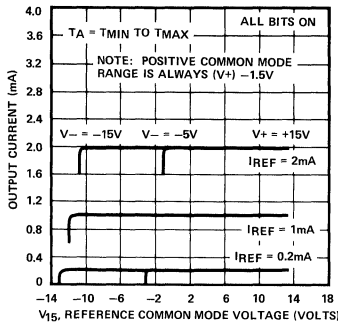
LSB PROPAGATION DELAY vs IFS



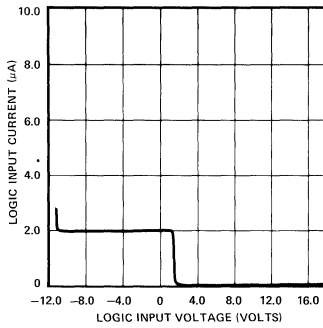
REFERENCE INPUT FREQUENCY RESPONSE



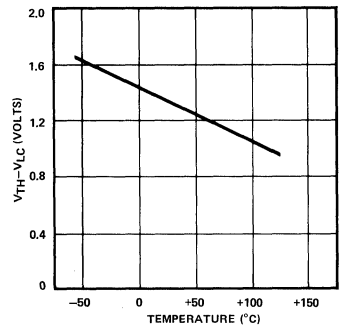
REFERENCE AMP COMMON-MODE RANGE



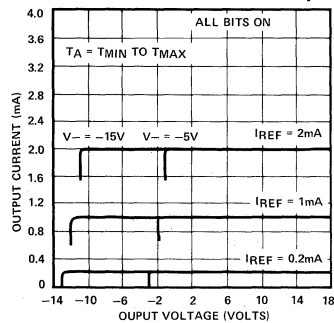
LOGIC INPUT CURRENT vs INPUT VOLTAGE



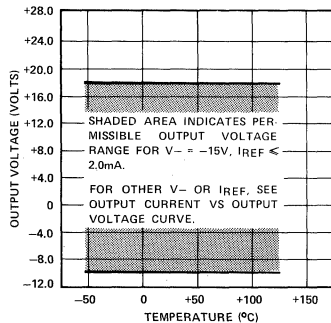
VTH - VLC vs TEMPERATURE



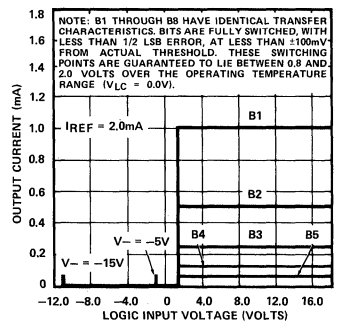
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



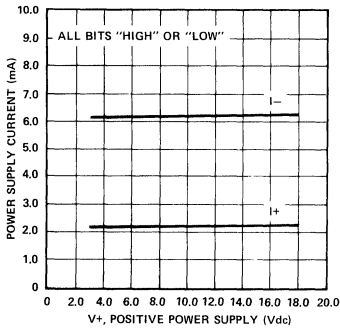
BIT TRANSFER CHARACTERISTICS



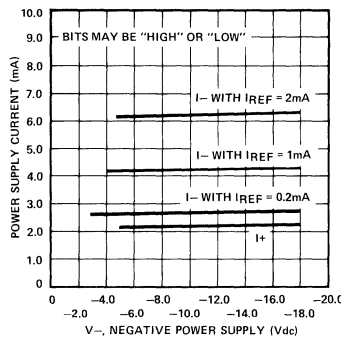


TYPICAL PERFORMANCE CHARACTERISTICS

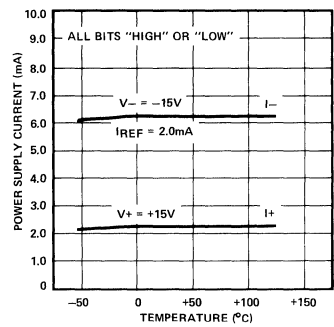
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V-

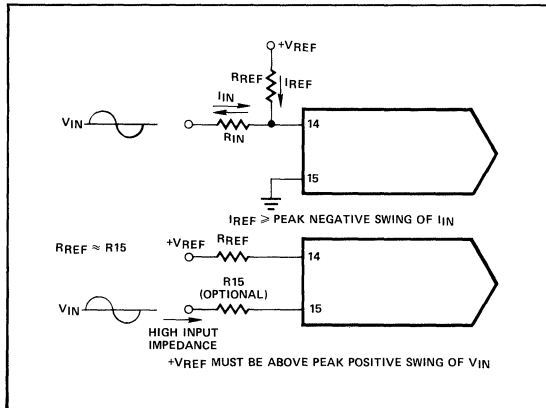


POWER SUPPLY CURRENT vs TEMPERATURE

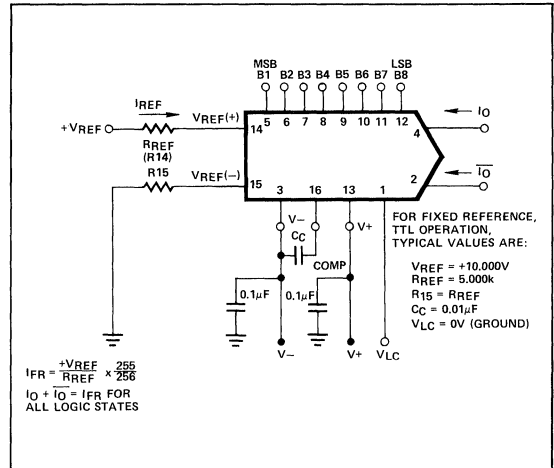


BASIC CONNECTIONS

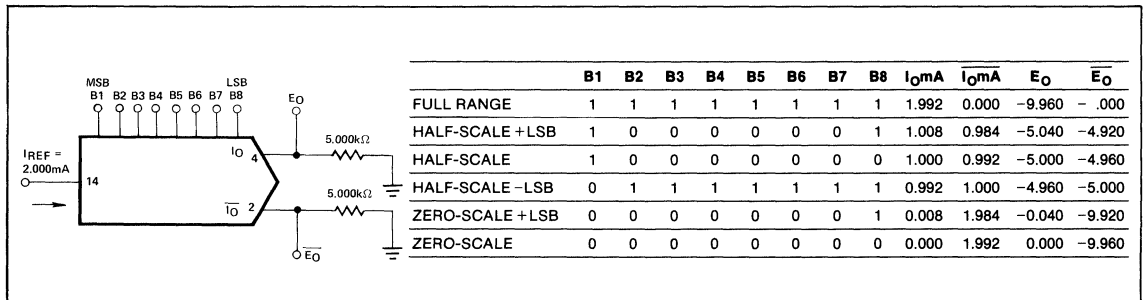
ACCOMODATING BIPOLAR REFERENCES



BASIC POSITIVE REFERENCE OPERATION



BASIC UNIPOLAR NEGATIVE OPERATION

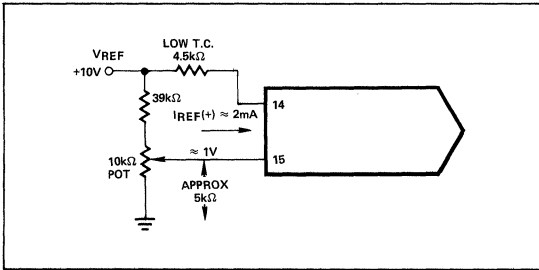
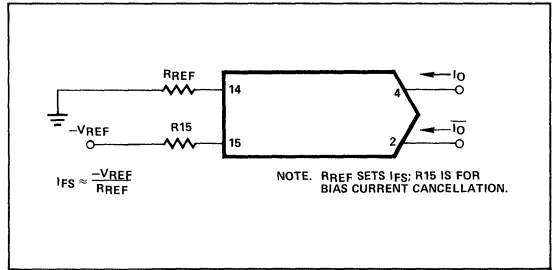


DIGITAL-TO-ANALOG CONVERTERS

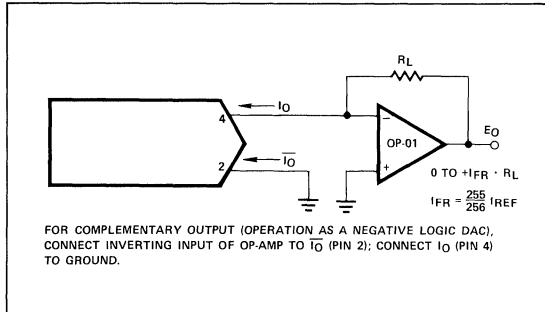
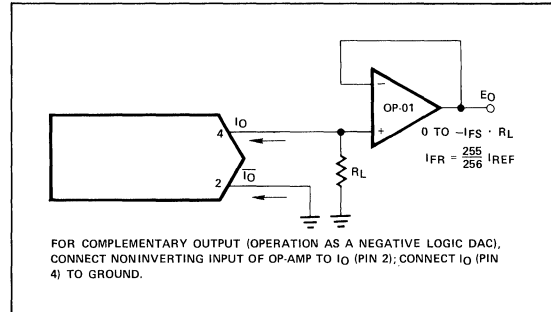
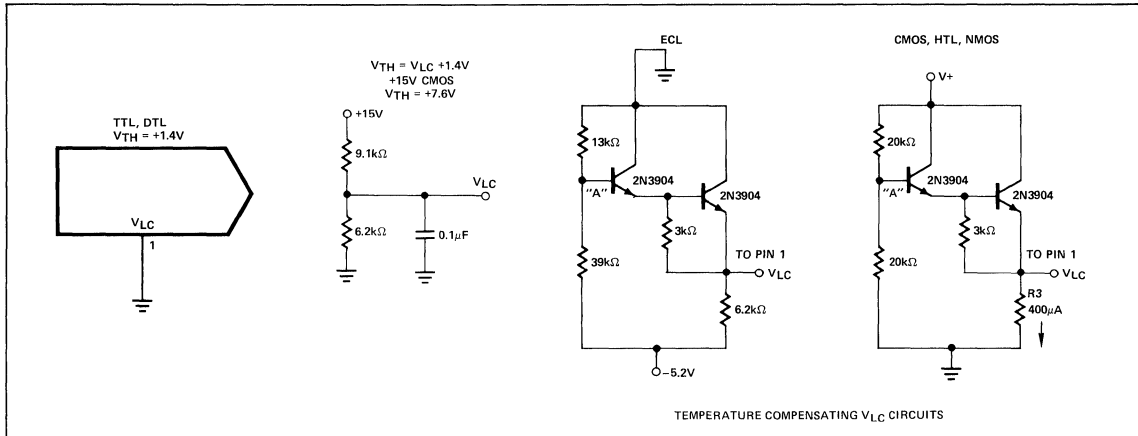
11

BASIC CONNECTIONS
BASIC BIPOLAR OUTPUT OPERATION

	B1	B2	B3	B4	B5	B6	B7	B8	E_0	\bar{E}_0
POS. FULL RANGE	1	1	1	1	1	1	1	1	- 9.920	+10.000
POS. FULL RANGE -LSB	1	1	1	1	1	1	1	0	- 9.840	+ 9.920
ZERO-SCALE +LSB	1	0	0	0	0	0	0	1	- 0.080	+ 0.160
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO-SCALE -LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG. FULL-SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	- 9.840
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	+10.000	- 9.920

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT

BASIC NEGATIVE REFERENCE OPERATION

OFFSET BINARY OPERATION

	B1	B2	B3	B4	B5	B6	B7	B8	E_0
POS. FULL RANGE	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	-4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	-5.000

BASIC CONNECTIONS
POSITIVE LOW IMPEDANCE OUTPUT OPERATION

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION

INTERFACING WITH VARIOUS LOGIC FAMILIES

APPLICATIONS INFORMATION
REFERENCE AMPLIFIER SET-UP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin

15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V - \text{plus } (I_{REF} \times 1k\Omega) \text{ plus } 2.5V$. The positive common-mode range is $V + \text{less } 1.5V$.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF} . If required, full-scale trimming may be accomplished by adjusting the value of R_{14} , or by using a potentiometer for R_{14} . An improved



method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full-scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V_- . The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0k Ω , minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin, such that the ratio of C_C (pF) to R_{14} (k Ω) = 15.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slow rate. For $R_{14} = 1k\Omega$ and $C_C = 15pF$, the reference amplifier slews at 4mA/ μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 200 Ω and $C_C = 0$. This yields a reference slew rate of 16mA/ μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2 μA logic input current and completely adjustable logic threshold voltage. For $V_- = -15V$, the logic inputs may swing between -10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V_- plus ($I_{REF} \times 1k\Omega$) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC} . For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an $I_{REF} = 1mA$ is recommended. For interfacing other logic families, see preceding page. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100 μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1k Ω divider, for example, it should be bypassed to ground by a 0.01 μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \bar{I}_O = I_{FS}$. Current appears at the "true" (I_O) output when a "1" (logic high) is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases \bar{I}_O as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must be connected to ground or to a point capable of sourcing I_{FS} ; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V_- and is independent of the positive supply. Negative compliance is given by V_- plus ($I_{REF} \times 1k\Omega$) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of $\pm 5V$ or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -4.5V with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I_+) (V_+) + (I_-) (V_-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically $\pm 10ppm/^\circ C$, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for min-



DAC-10

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

Precision Monolithics Inc.

FEATURES

- **Fast Settling** 85ns
- **Low Full-Scale Drift** 10ppm/°C
- **Nonlinearity to 0.05% Max Over Temp Range**
- **Complementary Current Outputs** 0 to 4mA
- **Wide Range Multiplying Capability** ... 1MHz Bandwidth
- **Wide Power Supply Range** .. +5, -7.5 Min to ±18V Max
- **Direct Interface to TTL, CMOS, ECL, PMOS, NMOS**

ORDERING INFORMATION†

NL LSB	18-PIN HERMETIC DUAL-IN-LINE PACKAGE	
	MILITARY TEMP.*	COMMERCIAL TEMP.
±1/2	DAC10BX*	DAC10FX
±1	DAC10CX*	DAC10GX

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The DAC-10 series of 10-bit monolithic multiplying digital-to-analog converters provide high-speed performance and full-scale accuracy.

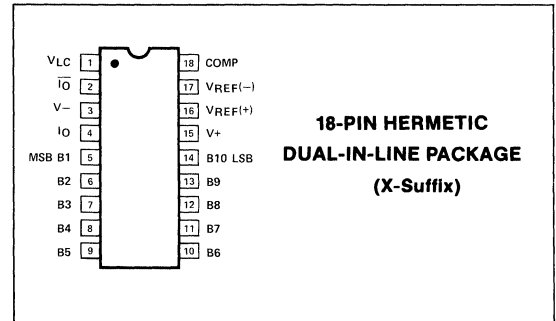
Advanced circuit design achieves 85ns settling times with very low 'glitch' energy and low power consumption. Direct interface to all-popular logic families with full noise immunity is provided by the high-swing, adjustable-threshold logic inputs.

All DAC-10 series models guarantee full 10-bit monotonicity, and nonlinearities as tight as ±0.05% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±18V power supply range, with 85mW power consumption attainable at lower supplies.

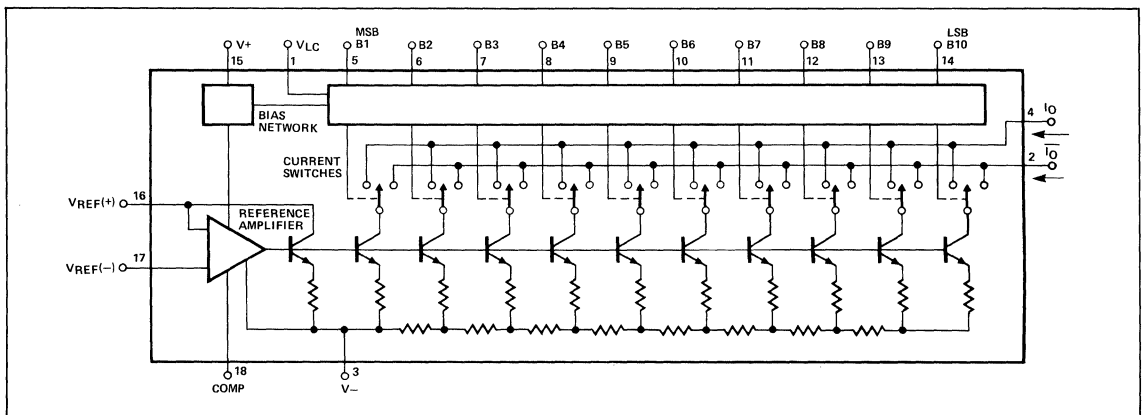
A highly stable, unique trim method is used, which selectively shorts zener diodes, to provide 1/2 LSB full-scale accuracy without the need for laser trimming.

Single-chip reliability coupled with low cost and outstanding flexibility make the DAC-10 device an ideal building block for A/D converters, Data Acquisition systems, CRT display, programmable test equipment, and other applications where low power consumption, input/output versatility, and long-term stability are required.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Manufactured under one or more of the following patents: 4,055,770; 4,056,740; 4,092,639



ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
DAC-10BX, CX	-55°C to +125°C
DAC-10FX, GX	0°C to +70°C
DICE Junction Temperature (T_j)	-65°C to +150°C
Storage Temperature	-65°C to +150°C
Power Dissipation	500mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
V+ Supply to V- Supply	36V

Logic Inputs	V- to V+ plus 36V
V_{LC}	V- to V+
Analog Current Outputs	+18V to -18V
Reference Inputs (V_{16} to V_{17})	V- to V+
Reference Input Differential Voltage (V_{16} to V_{17})	±18V
Reference Input Current (I_{16})	2.5mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2mA$; $-55^\circ C \leq T_A \leq 125^\circ C$ for DAC-10B and DAC-10C, $0^\circ C \leq T_A \leq 70^\circ C$ for DAC-10F and G, unless otherwise noted. Output characteristics apply to both I_{OUT} and \bar{I}_{OUT} .

PARAMETER	SYMBOL	CONDITIONS	DAC-10B/F			DAC-10C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1	—	0.7	—	LSB
Settling Time	t_S	All Bits Switched ON or OFF Settle to 0.05% of FS (See Note)	—	85	135	—	85	150	ns
Output Capacitance	C_O		—	18	—	—	18	—	pF
Propagation Delay	t_{PLH} t_{PHL}	All Bits Switched $R_L = 5k\Omega$ $R_L = 0$	—	50	—	—	50	—	ns
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1 LSB	—	-5.5	—	—	-5.5	—	V
Gain Tempco	TCI_{FS}	(See Note)	—	±10	±25	—	±10	±50	ppm/°C
Full-Scale Symmetry	I_{FSS}	$I_{FR} - \bar{I}_{FR}$	—	0.1	4	—	0.1	4	μA
Zero-Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA
Full-Scale Current	I_{FR}	(See Note)	3.960	3.996	4.032	3.920	3.996	4.072	mA
Reference Input Slew Rate	DI/dt		—	6	—	—	6	—	mA/μs
Reference Bias Current	I_B		—	-1	-3	—	-1	-3	μA
Power Supply Sensitivity	$PSSI_{FS+}$	$4.5V \leq V+ \leq 18V$	—	0.001	0.01	—	0.001	0.01	%Δ I_{FS} /%ΔV
	$PSSI_{FS-}$	$-18V \leq V- \leq -10V$	—	0.0012	0.01	—	0.0012	0.01	
Power Supply Current	$I+$	$V_S = \pm 15V$; $I_{REF} = 2mA$	—	2.3	4	—	2.3	4	mA
	$I-$		—	-9	-15	—	-9	-15	
	$I+$	$V_S = +5V/-7.5V$; $I_{REF} = 1mA$	—	1.8	4	—	1.8	4	
	$I-$		—	-5.9	-9	—	-5.9	-9	
Power Dissipation	P_d	$V_S = +5V/-7.5V$; $I_{REF} = 1mA$	—	231	276	—	231	276	mW
			—	85	107	—	85	107	
Logic Input Levels	V_{IL}	$V_{LC} = 0$	—	—	0.8	—	—	0.8	V
	V_{IH}		2	—	—	2	—	—	
Logic Input Currents	I_{IL}	$V_{LC} = 0$; $-5V \leq V_{IN} \leq 0.8V$ $2V \leq V_{IN} \leq 18V$	-10	-5	—	-10	-5	—	μA
	I_{IH}		—	0.001	10	—	0.001	10	

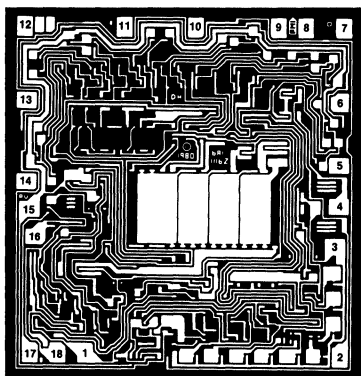
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2mA$; $T_A = 25^\circ C$, unless otherwise noted. Output characteristics apply to both I_{OUT} and \bar{I}_{OUT} .

PARAMETER	SYMBOL	CONDITIONS	DAC-10B/C/F			DAC-10G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1	—	0.7	—	LSB
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1 LSB	-5	-6/+18	+10	-5	-6/+15	+10	V
Full-Scale Current	I_{FS}	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 5.000k\Omega$	3.978	3.996	4.014	3.956	3.996	4.036	mA
Full-Scale Symmetry	I_{FSS}	$I_{FR} - \bar{I}_{FR}$	—	0.1	4	—	0.1	4	μA
Zero-Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA

NOTE: Guaranteed by design.



DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.090 inch, 7740 sq. mils
(2.184 × 2.286 mm, 4.993 sq. mm)

- | | |
|---------------------|-------------------|
| 1. V_{LC} (LOGIC) | 10. B6 |
| THRESHOLD CONTROL | 11. B7 |
| 2. \overline{I}_O | 12. B8 |
| 3. V^- | 13. B9 |
| 4. I_O | 14. B10 (LSB) |
| 5. B1 (MSB) | 15. V^+ |
| 6. B2 | 16. $V_{REF} (+)$ |
| 7. B3 | 17. $V_{REF} (-)$ |
| 8. B4 | 18. COMPENSATION |
| 9. B5 | |

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2mA$, $T_A = 25^\circ C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT} .

PARAMETER	SYMBOL	CONDITIONS	DAC-10N LIMIT	DAC-10G LIMIT	UNITS
Resolution			10	10	Bits MIN
Monotonicity			10	10	Bits MIN
Nonlinearity	NL		± 0.5	± 1	LSB MAX
Output Voltage Compliance	V_{OC}	True 1 LSB	+10 -5	+10 -5	V MAX V MIN
Output Current Range		$I_{FS} \pm 3.996 MA$	± 18	± 40	μA MAX
Zero-Scale Current	I_{ZS}	All Bits OFF	0.5	0.5	μA MAX
Logic Input "1"	V_{IH}	$I_{IN} = 100nA$	2	2	V MIN
Logic Input "0"	V_{IL}	V_{LC} @ Ground $I_{IN} = -100\mu A$	0.8	0.8	V MAX
Positive Supply Current	I^+	$V^+ = 15V$	4	4	mA MAX
Negative Supply Current	I^-	$V^- = -15V$	-15	-15	mA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

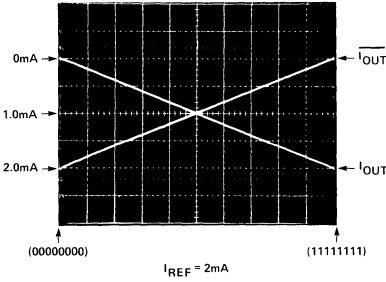
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $I_{REF} = 2mA$, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT} .

PARAMETER	SYMBOL	CONDITIONS	DAC-10N TYPICAL	DAC-10G TYPICAL	UNITS
Settling Time	t_s	To $\pm 1/2$ LSB When Output is Switched from 0 to FS	85	85	ns
Gain Temperature Coefficient (TC)		V_{REF} Tempco Excluded	± 10	± 10	ppm FS/ $^\circ C$
Output Capacitance			18	18	pF
Output Resistance			10	10	M Ω

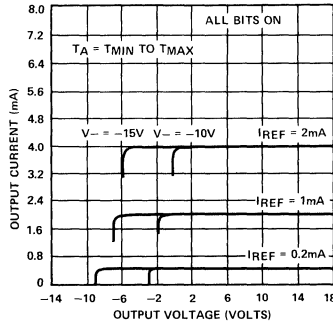


TYPICAL PERFORMANCE CHARACTERISTICS

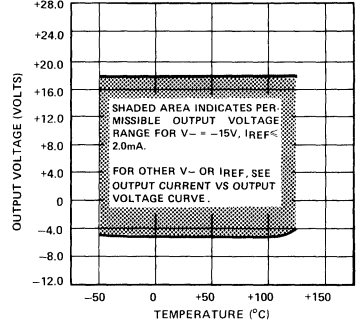
TRUE AND COMPLEMENTARY OUTPUT OPERATIONS



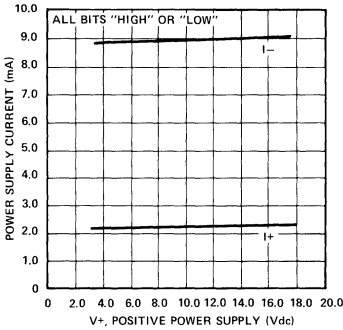
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



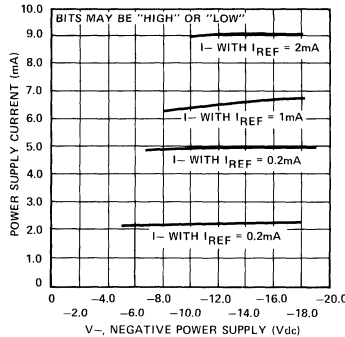
OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



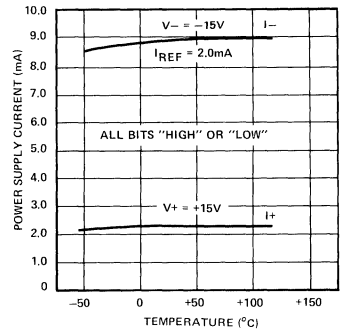
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V-

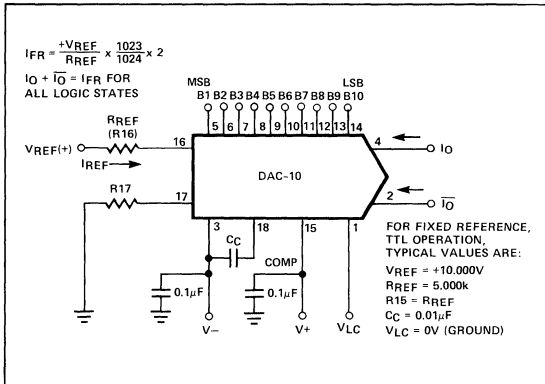


POWER SUPPLY CURRENT vs TEMPERATURE

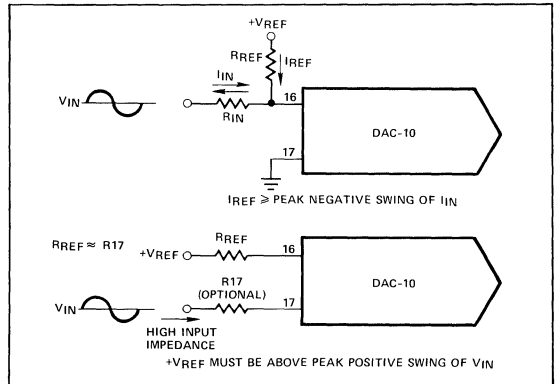


BASIC CONNECTIONS

BASIC POSITIVE REFERENCE OPERATION



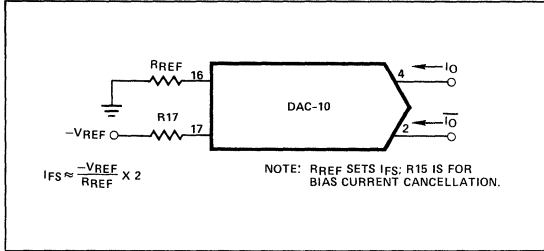
ACCOMMODATING BIPOLAR REFERENCES



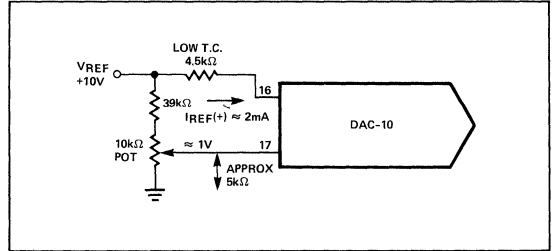
DIGITAL-TO-ANALOG CONVERTERS



BASIC NEGATIVE REFERENCE OPERATION



RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



BASIC UNIPOLAR NEGATIVE OPERATION

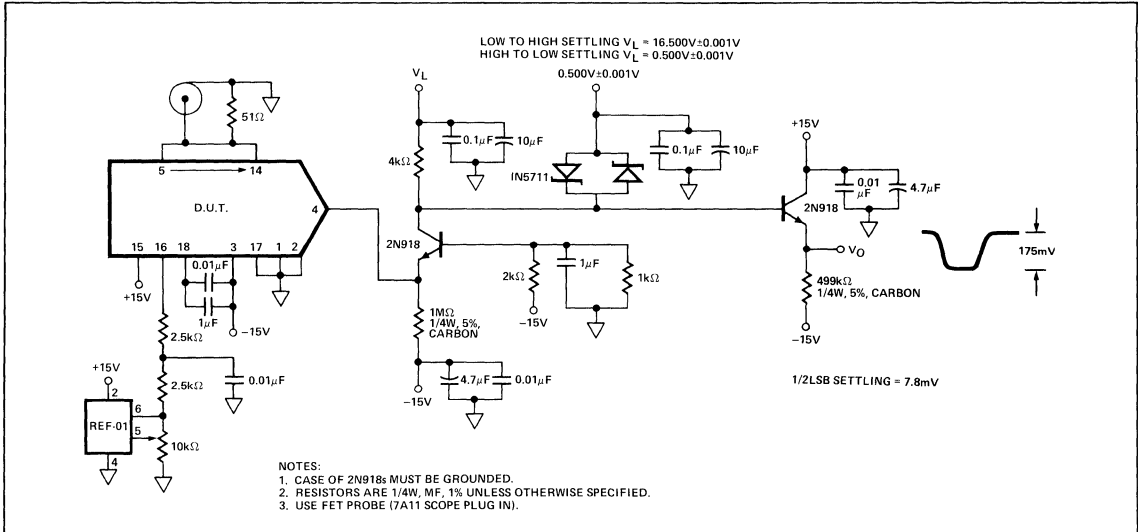
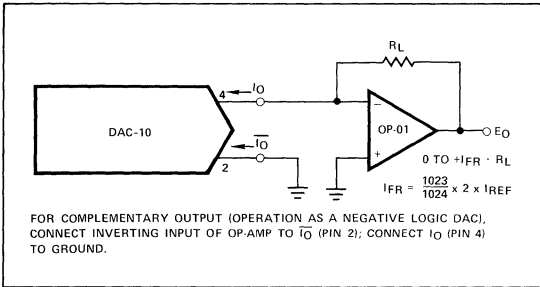
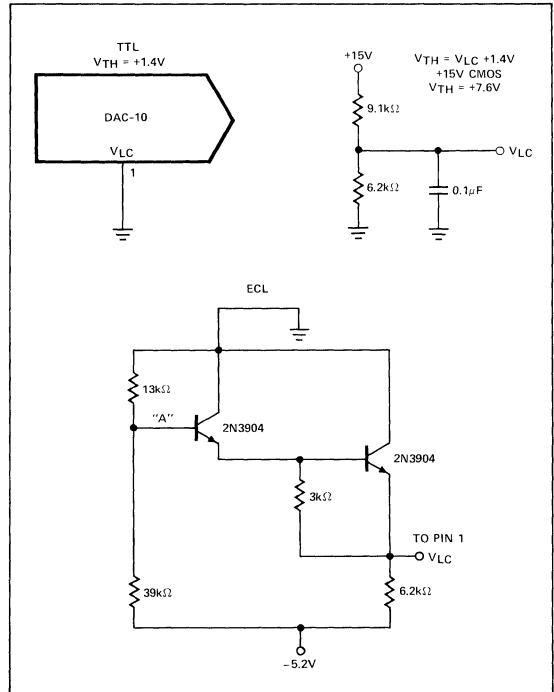
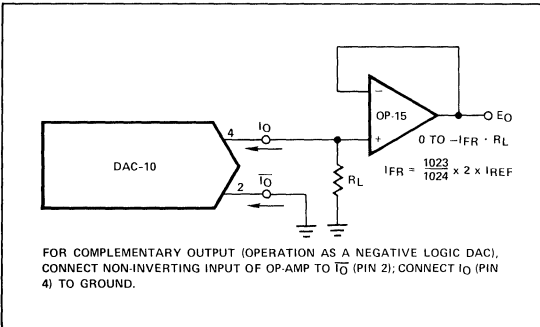
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	I ₀ mA	I ₀ mA	E ₀	E ₀
FULL RANGE	1	1	1	1	1	1	1	1	1	1	3.996	0.000	-4.995	-0.000
HALF-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	2.004	1.992	-2.505	-2.490
HALF-SCALE	1	0	0	0	0	0	0	0	0	0	2.000	1.996	-2.500	-2.495
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	1	1	1.996	2.000	-2.495	2.500
ZERO-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	0.004	3.992	-0.005	-4.990
ZERO-SCALE	0	0	0	0	0	0	0	0	0	0	0.000	3.996	-0.000	-4.995

BASIC BIPOLAR OUTPUT OPERATION

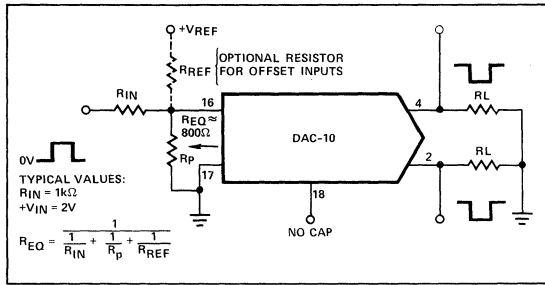
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E ₀	E ₀
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	-4.990	+5.000
POS FULL RANGE -LSB	1	1	1	1	1	1	1	1	1	0	-4.980	+4.990
ZERO-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	-0.010	+0.020
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.000	+0.010
ZERO-SCALE -LSB	1	1	1	1	1	1	1	1	1	1	+0.010	0.000
NEG FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	+4.990	-4.980
NEG FULL-SCALE	0	0	0	0	0	0	0	0	0	0	+5.000	-4.990

OFFSET BINARY OPERATION

	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E ₀
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	+4.990
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.00
NEG FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	-4.990
NEG FULL-SCALE	0	0	0	0	0	0	0	0	0	0	-5.000

SETTLING TIME MEASUREMENT

POSITIVE LOW IMPEDANCE OUTPUT OPERATION

INTERFACING WITH VARIOUS LOGIC FAMILIES

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


PULSED REFERENCE OPERATION



APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-10 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to 2mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{1023}{1024} \times 2 \times (I_{REF}) \text{ where } I_{REF} = I_{16}$$

In positive reference applications, an external positive reference voltage forces current through R16 into the $V_{REF(+)}$ terminal (pin 16) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 17; reference current flows from ground through R16 into $V_{(+)}$, as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 17. The voltage at pin 18 is equal to and tracks the voltage at pin 17 due to the high gain of the internal reference amplifier. R17 (nominally equal to R16) is used to cancel bias current errors; R17 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 17. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V_{-}$ plus $(I_{REF} \times 2k\Omega)$ plus 2V. The positive common-mode range is V_{+} less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R16 should be split into two resistors with the junction bypassed to ground with a 0.1 μ F capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF} . If required, full-scale trimming may be accomplished by adjusting the value of R16, or by using a potentiometer for R16. An improved method effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 18 to V_{-} . For fixed reference operation, a 0.01 μ F capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-10 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4 μ A. Monotonic operation is maintained over a typical range of I_{REF} from 100 μ A to 2mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 18 to V_{-} . The value of this capacitor depends on the impedance presented to pin 16 for R16 values of 1.0, 2.5 and 5.0k Ω , minimum values of C_C are 15, 37, and 75pF. Larger values of R16 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R16 enabling small C_C values should be used. If pin 16 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R16 = 1k Ω and $C_C = 15$ pF, the reference amplifier slews at 4mA/ μ s enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2$ mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 16 is 200 Ω and $C_C = 0$. This yields a reference slew rate of 16mA/ μ s which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-10 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2 μ A logic input current and completely adjustable logic threshold voltage. For $V_{-} = -15$ V, the logic inputs may swing between -5 and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-10 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V_{-} plus $(I_{REF} \times 2k\Omega)$ plus 3V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4V above V_{LC} . For TTL interface, simply ground pin 1. When interfacing ECL, an $I_{REF} = 1$ mA is recommended. For interfacing other logic families, see previous page. For general setup of the logic control circuit, it should be noted that pin 1 will sink 1.1mA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1k Ω divider, for example, it should be bypassed to ground by a 0.01 μ F capacitor.



ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \bar{I}_O = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases \bar{I}_O as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS} ; DO NOT LEAVE AN UNUSED OUTPUT PIN OPEN.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V_- and is independent of the positive supply. Negative compliance is +10V above V_- .

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-10 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating with V_- supplies of -10V or less, $I_{REF} \leq 1\text{mA}$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -9V with $I_{REF} = 2\text{mA}$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-10 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain within acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-10 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically $\pm 10\text{ppm}/^\circ\text{C}$, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-10 decrease approximately 10% at -55°C ; at $+125^\circ\text{C}$ an increase of about 15% is typical.

SETTLING TIME

The DAC-10 is capable of extremely fast settling times; typically 85ns at $I_{REF} = 2\text{mA}$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 10 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 130ns, thus determining the overall settling time of 85ns. Settling to 8-bit accuracy requires about 60 to 78ns. The output capacitance of the DAC-10 including the package is approximately 18pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve $\pm 2\mu\text{A}$, therefore a $4\text{k}\Omega$ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of schematic titled "Settling Time Measurement" uses a cascode design to permit driving a $4\text{k}\Omega$ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111 to 100000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within $\pm 0.2\%$ of the final value, and thus settling times may be observed at lower values of I_{REF} .

DAC-10 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 μF capacitors at the supply pins provide full transient protection.



DAC-20

2-DIGIT BCD HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

Precision Monolithics Inc.

FEATURES

- Fast Settling Output Current 85ns
- Full-Scale Current Prematched to ± 0.3 LSB
- Direct Interface to TTL, CMOS, ECL, PMOS, NMOS
- Nonlinearity to $\pm 1/2$ LSB Maximum Over Temp.
- High Output Impedance and Compliance $-10V$ to $+18V$
- Complementary Current Outputs
- Wide Range Multiplying Capability ... 1MHz Bandwidth
- Low FS Current Drift ± 10 ppm/ ΔC
- Wide Power Supply Range $\pm 4.5V$ to $\pm 18V$
- Low Power Consumption 37mW @ $\pm 5V$
- Low Cost

ORDERING INFORMATION†

NL LSB	16-PIN DUAL-IN-LINE PACKAGE COMMERCIAL TEMPERATURE RANGE	
	HERMETIC	PLASTIC
$\pm 1/2$	DAC20CQ	DAC20CP

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The DAC-20 series of 2-digit BCD monolithic multiplying digital to analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB

between reference and full-scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

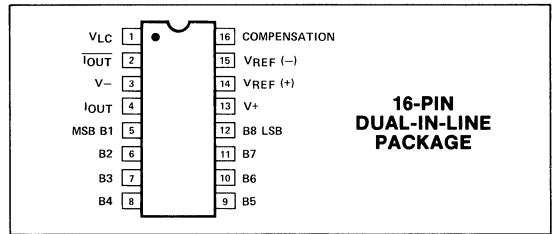
Complementary current outputs with $-10V$ to $+18V$ voltage compliance enable resistive termination, a voltage output without an external op amp.

Both DAC-20 models guarantee full 2-digit monotonicity, some have nonlinearity as tight as $\pm 1/2$ LSB over the entire operating temperature range. Nonlinearity is unchanged over the $\pm 4.5V$ to $\pm 18V$ power supply range, with 37mW power consumption attainable at $\pm 5V$ supplies.

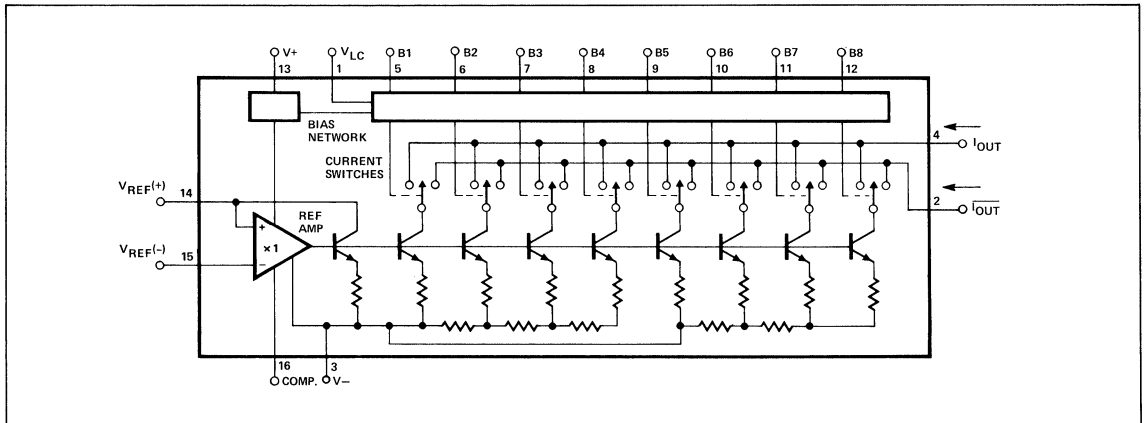
The compact size and low power consumption make the DAC-20 attractive for portable applications.

DAC-20 applications include A/D converters, audio attenuators, analog meter drivers, programmable power supplies, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

PIN CONNECTIONS



EQUIVALENT CIRCUIT



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Operating Temperature Range	DAC-20 CQ, CP	0°C to $+70^\circ\text{C}$
DICE Junction Temperature (T_j)		-65°C to $+150^\circ\text{C}$
Storage Temperature Range	Q Package	-65°C to $+150^\circ\text{C}$
	P Package	-65°C to $+125^\circ\text{C}$
Power Dissipation		500mW
	Derate above 100°C	10mW/ $^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)		300°C

V+ Supply to V- Supply	36V
Logic Inputs	V- to V- plus 36V
V_{LC}	V- to V+
Reference Inputs (V_{14}, V_{15})	V- to V+
Reference Input Differential Voltage (V_{14} to V_{15})	$\pm 18\text{V}$
Reference Input Current (I_{14})	5.0mA

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

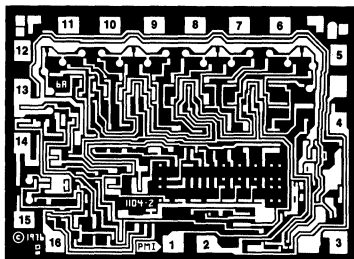
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $I_{REF} = 2.0\text{mA}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-20C			UNITS
			MIN	TYP	MAX	
Resolution		BCD 0 to 99 steps	2	—	—	Digits
Monotonicity		BCD 99 steps	2	—	—	Digits
Nonlinearity	NL	0000 0000 to 1001 1001	—	—	$\pm 1/2$	LSB
Settling Time	t_S	To $\pm 1/2$ LSB ($\pm 0.5\%$ FS) all bits switched ON or OFF, $T_A = 25^\circ\text{C}$ (Note 1)	—	85	150	ns
Propagation Delay						
Each Bit	t_{PLH}	$T_A = 25^\circ\text{C}$ (Note 1)	—	35	60	ns
All bits switched	t_{PHL}					
Full Tempo	TCI_{FS}	(Note 1)	—	± 10	± 80	ppm/ $^\circ\text{C}$
Output Voltage Compliance (True Compliance)	V_{OC}	Full-scale current change < 1/2 LSB (< 0.5% FS) $R_{OUT} > 20\text{M}\Omega$ typical $I_{REF} = 1\text{mA}$	-10	—	+18	V
Full Range Output (Digital Input 1001 1001)	I_{FR4}	$T_A = 25^\circ\text{C}$, $I_{REF} = 2\text{mA}$	1.92	1.98	2.04	mA
Zero-Scale Current	I_{ZS}		—	0.2	5	μA
Output Current Range	I_{OR}	$V_- = -10\text{V}$ $V_- = -12\text{V}$ to -18V	2.2	2	—	mA
			4.2	2	—	
Logic Input Levels						
Logic "0"	V_{IL}	$V_{LC} = 0\text{V}$	—	—	0.8	V
Logic "1"	V_{IH}		2	—	—	
Logic Input Current						
Logic "0"	I_{IL}	$V_{LC} = 0\text{V}$ $V_{IN} = -10\text{V}$ to $+0.8\text{V}$	—	-2	± 10	μA
Logic "1"	I_{IH}	$V_{IN} = 2\text{V}$ to 18V	—	0.002	± 10	
Logic Input Swing	V_{IS}	$V_- = -15\text{V}$	-10	—	+18	V
Logic Threshold Range	V_{THR}	$V_S = \pm 15\text{V}$ (Note 1)	-10	—	+13.5	V
Reference Bias Current	I_{15}		—	-1	-3	μA
Reference Input Slew Rate	dI/dt	(Note 1)	4	8	—	mA/ μs
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	$V_+ = 4.5\text{V}$ to 18V $V_- = -4.5\text{V}$ to -18V $I_{REF} = 1\text{mA}$	—	± 0.0003	± 0.03	$\% \Delta I_{FS}$ $\% \Delta V$
Power Supply Current	I_+ I_- I_+ I_-	$V_S = \pm 5\text{V}$, $I_{REF} = 1\text{mA}$ $V_S = \pm 15\text{V}$, $I_{REF} = 2\text{mA}$	—	2.3 -5.0 2.5 -7.8	3.8 -6.5 3.8 -9.1	mA
Power Dissipation	P_d	$V_S = \pm 5\text{V}$, $I_{REF} = 1\text{mA}$ $V_S = \pm 15\text{V}$, $I_{REF} = 2\text{mA}$	—	37 152	52 194	mW

NOTE:
1. Guaranteed by design.



DICE CHARACTERISTICS

DIE SIZE 0.085 × 0.065 inch, 5,525 sq. mils
(2.159 × 1.651 mm, 3.56 sq. mm)

- | | |
|----------------|-------------------|
| 1. V_{LC} | 9. BIT 5 |
| 2. I_{OUT} | 10. BIT 6 |
| 3. V^- | 11. BIT 7 |
| 4. I_{OUT} | 12. BIT 8 (LSB) |
| 5. BIT 1 (MSB) | 13. V^+ |
| 6. BIT 2 | 14. $V_{REF} (+)$ |
| 7. BIT 3 | 15. $V_{REF} (-)$ |
| 8. BIT 4 | 16. COMP |

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 25^\circ C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and \bar{I}_{OUT} .

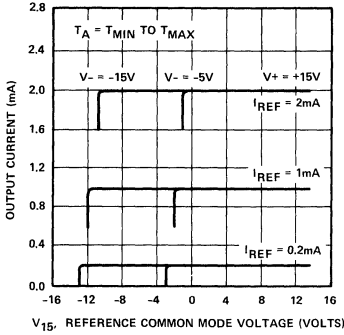
PARAMETER	SYMBOL	CONDITIONS	DAC-20G LIMIT	UNITS
Resolution		BCD 0 to 99 steps	2	Digits MIN
Monotonicity		BCD 99 steps	2	Digits MIN
Nonlinearity	NL	FS = 1001 1001	$\pm 1/2$	LSB MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1/2 LSB	+18 -10	V MAX V MIN
Full-Scale Current	I_{FS4}	$V_{REF} = 10V$ $R_{14}, R_{15} = 5k\Omega$	2.04 1.92	mA MAX mA MIN
Zero-Scale Current	I_{ZS}		5	μA MAX
Output Current Range	I_{OR}	$V^- = -10V$ $V^- = -12V$ to $-18V$	2.1 4.2	mA MIN
Logic "0" Input Level	V_{IL}		0.8	V MAX
Logic "1" Input Level	V_{IH}		2	V MIN
Logic Input Current				
Logic "0"	I_{IL}	$V_{IN} = -10V$ to $+0.8V$	± 10	μA MAX
Logic "1"	I_{IH}	$V_{IN} = 2V$ to $18V$	± 10	μA MAX
Logic Input Swing	V_{IS}	$V^- = -15V$	+18 -10	V MAX V MIN
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	$V^- = -4.5V$ to $-18V$ $V^- = -4.5V$ to $-18V$ $I_{REF} = 1mA$	± 0.03 ± 0.03	$\% \Delta I_{FS}$ MAX $\% \Delta V$
Power Supply Current	I^+ I^-	$V_S = \pm 18V$ $I_{REF} \leq 2mA$	3.8 -7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 18V$ $I_{REF} \leq 2mA$	194	mW MAX

NOTE:

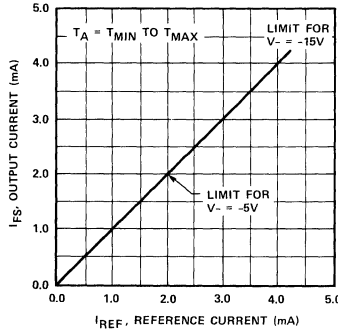
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, unless otherwise noted specified. Output characteristics refer to both I_{OUT} and \bar{I}_{OUT} .

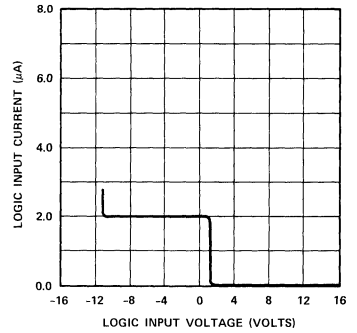
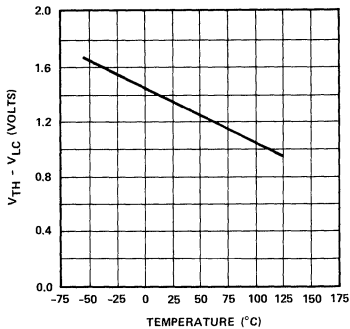
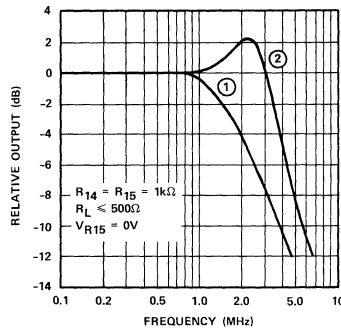
PARAMETER	SYMBOL	CONDITIONS	DAC-20G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	mA/ μs
Propagation Delay	t_{PLH} , t_{PHL}	$T_A = 25^\circ C$, Any Bit	35	ns
Settling Time	t_s	To $\pm 1/2$ LSB, All Bits Switched ON or OFF, $T_A = 25^\circ C$	85	ns

TYPICAL REFERENCE PERFORMANCE CHARACTERISTICS
**REFERENCE AMP
COMMON-MODE RANGE
(DIGITAL INPUT 1001 1001)**


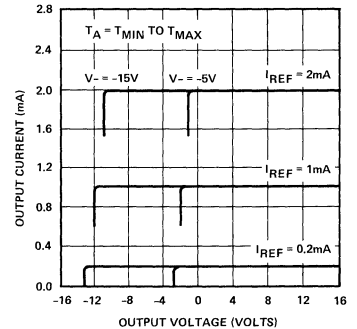
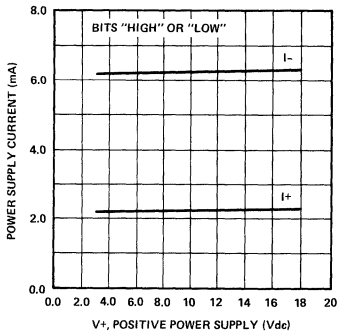
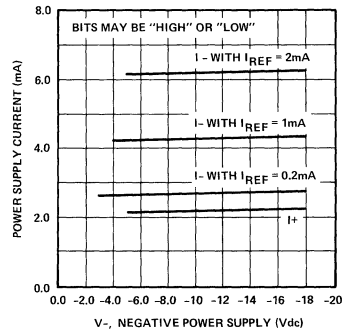
NOTE: POSITIVE COMMON MODE IS ALWAYS (V+) -1.5V;
NEGATIVE COMMON MODE RANGE IS V- PLUS
($I_{REF} \times 800\Omega$) PLUS 2.5V.

**FULL-SCALE CURRENT vs
REFERENCE CURRENT
(DIGITAL INPUT 1001 1001)**


NOTE: THE RECOMMENDED RANGE FOR OPERATION WITH
WITH A DC REFERENCE CURRENT IS +0.2mA
TO +4.0mA.

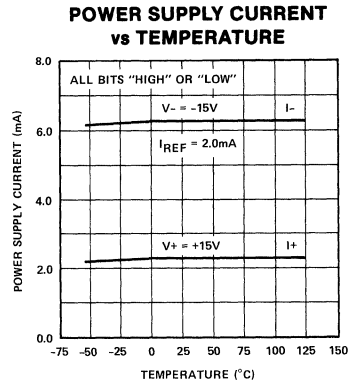
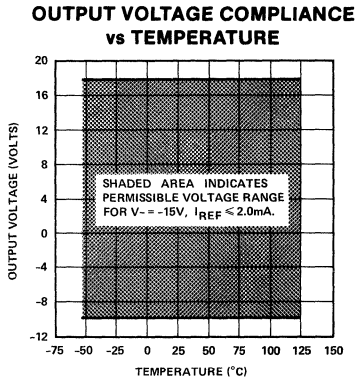
**LOGIC INPUT CURRENT
vs INPUT VOLTAGE**

 $V_{TH} - V_{LC}$ vs TEMPERATURE

**REFERENCE INPUT FREQUENCY
RESPONSE (DIGITAL INPUT
1001 1001)**


CURVE 1: $C_D = 15pF$, $V_{IN} = 2.0V_{p-p}$ CENTERED AT
+1.0V, LARGE SIGNAL.
CURVE 2: $C_D = 15pF$, $V_{IN} = 50mV_{p-p}$ CENTERED AT
+200mV, SMALL SIGNAL.

**OUTPUT CURRENT
vs OUTPUT VOLTAGE
(OUTPUT VOLTAGE COMPLIANCE)
(DIGITAL INPUT 1001 1001)**

**POWER SUPPLY
CURRENT vs V+**

**POWER SUPPLY
CURRENT vs V-**




TYPICAL REFERENCE PERFORMANCE CHARACTERISTICS



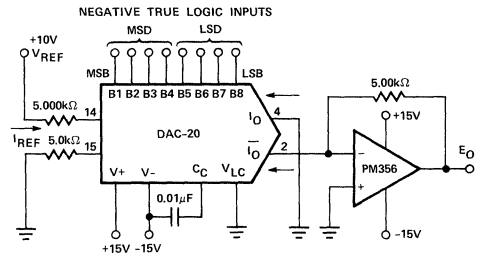
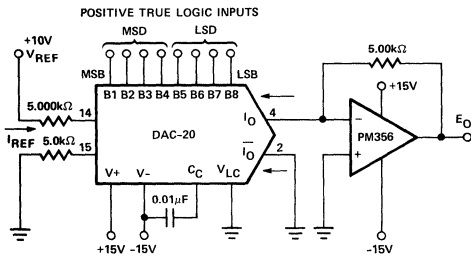
BASIC OUTPUT CONNECTIONS

With complementary current outputs, the DAC-20 may be used with either positive true or negative true (complementary) logic. Current appears at the "true" output (I_O) when a "1" is applied to a logic input. As the BCD-coded input increases, the sink current at Pin 4 increases proportionately, in the fashion of a "positive logic" D/A converter. When a "0" is applied to a logic input, that current is turned OFF at Pin 4 and ON at Pin 2 (\bar{I}_O) which is used for negative true or "negative logic" D/A converters.

The unused output must be connected to ground or some voltage source capable of sourcing 1.65 times I_{REF} . A detailed discussion of reference input operation begins on the next page.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V_- and is independent of the positive supply. Negative compliance is given by V_- plus $(I_{REF} \times 800\Omega)$ plus 2.5V.

POSITIVE VOLTAGE OUTPUT



DECIMAL INPUT	BCD INPUT		I_O	E_O
	MSD	LSD		
0	0000	0000	0	0
10	0001	0000	0.20mA	+1.0V
20	0010	0000	0.40mA	+2.0V
30	0011	0000	0.60mA	+3.0V
40	0100	0000	0.80mA	+4.0V
80	1000	0000	1.60mA	+8.0V
99	1001	1001	1.98mA	+9.9V

DECIMAL INPUT	BCD INPUT		\bar{I}_O	E_O
	MSD	LSD		
0	1111	1111	0	0
10	1110	1111	0.20mA	+1.0V
20	1101	1111	0.40mA	+2.0V
30	1100	1111	0.60mA	+3.0V
40	1011	1111	0.80mA	+4.0V
80	0111	1111	1.60mA	+8.0V
99	0110	0110	1.98mA	+9.9V



NEGATIVE VOLTAGE OUTPUT

POSITIVE TRUE LOGIC INPUTS

NEGATIVE TRUE LOGIC INPUTS

DECIMAL INPUT	BCD INPUT		I _o	E _o
	MSD	LSD		
0	0000	0000	0	0
10	0001	0000	0.20mA	-1.0V
20	0010	0000	0.40mA	-2.0V
30	0011	0000	0.60mA	-3.0V
40	0100	0000	0.80mA	-4.0V
80	1000	0000	1.60mA	-8.0V
99	1001	1001	1.98mA	-9.9V

DECIMAL INPUT	BCD INPUT		I _o	E _o
	MSD	LSD		
0	1111	1111	0	0
10	1110	1111	0.20mA	-1.0V
20	1101	1111	0.40mA	-2.0V
30	1100	1111	0.60mA	-3.0V
40	1011	1111	0.80mA	-4.0V
80	0111	1111	1.60mA	-8.0V
99	0110	0110	1.98mA	-9.9V

REFERENCE OPERATION

POSITIVE

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:
 VREF = +10.000V
 RREF = 5.000k
 R15 ≈ RREF
 Cc = 0.01μF
 V_{LC} = 0V (GROUND)

$$I_{FS} = \frac{V_{REF(+)} - V_{REF(-)}}{R_{REF}}$$

$$I_o + I_{iO} \approx I_{REF} \times 1.65$$

FOR ALL LOGIC INPUT STATES

NEGATIVE

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:
 VREF = +10.000V
 RREF = 5.000k
 R15 ≈ RREF
 Cc = 0.01μF
 V_{LC} = 0V (GROUND)

$$I_{FS} = \frac{V_{REF(-)} - V_{REF(+)}}{R_{REF}}$$

$$I_o + I_{iO} \approx I_{REF} \times 1.65$$

FOR ALL LOGIC INPUT STATES

REFERENCE AMPLIFIER SETUP

The DAC-20 is a multiplying converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = 99/100 \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

In positive reference applications an external positive reference voltage forces current through R₁₄ into the V_{REF}(+) terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF}(-) at Pin 15; reference current flows from ground through R₁₄ into V_{REF}(+), as in the positive reference case. This negative reference con-

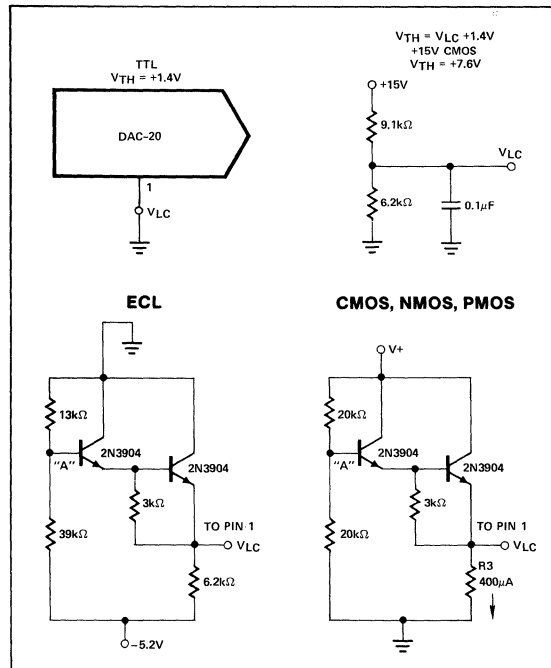
nection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

When a DC reference is used, a reference bypass capacitor is recommended. A 5V TTL logic supply is not recommended as reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1 μ F capacitor.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF} . If required, full-scale trimming may be accomplished by adjusting the value of R_{14} .

The reference amplifier must be compensated by using a capacitor from Pin 16 to V^- . For fixed reference operation, a 0.01 μ F capacitor is recommended. For variable reference applications, see section entitled "Multiplying Operation."

LOGIC INPUT OPERATION AND INTERFACING



LOGIC THRESHOLD CONTROL

The DAC-20 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2 μ A logic input current and completely adjustable logic threshold voltage.

For $V^- = -15V$, the logic inputs may swing between -10V and +18V. This enables direct interface with a +15V CMOS logic, even when the DAC-20 is powered from a +5V supply. Minimum logic threshold voltage are given by: V^- plus ($I_{REF} \times 800\Omega$) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 1, V_{LC}).

The logic input threshold is 1.4V above V_{LC} . For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an $I_{REF} = 1mA$ is recommended. For interfacing other logic families, see the figure. Pin 1 will source 100 μ A typically, so the external circuitry must be designed to accommodate this current. Note that the threshold voltage has the temperature dependence of two forward biased diodes. The two V_{LC} setting circuits shown, include temperature compensation.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1k Ω divider, for example, it should be bypassed to ground by a 0.01 μ F capacitor.

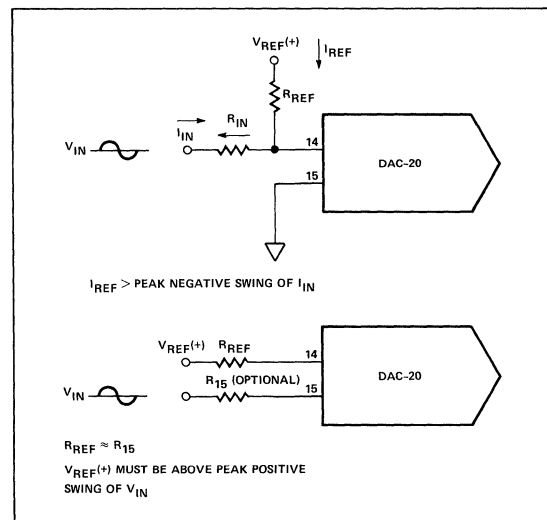
MULTIPLYING OPERATION

The DAC-20 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 2mA to 4 μ A. Monotonic operation is maintained over a typical range of I_{REF} from 100 μ A to 2mA.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V^-$ plus ($I_{REF} \times 800\Omega$) plus 2.5V. The positive common mode range is V^+ less 1.5V.

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V^- . The value of this capacitor depends on the impedance presented to Pin 14: for R_{14} values of 1.0, 2.5 and 5.0k Ω , minimum value of C_C are 15, 37, and 75pF. Larger values of R_{14} require

ACCOMMODATING BIPOLAR REFERENCES

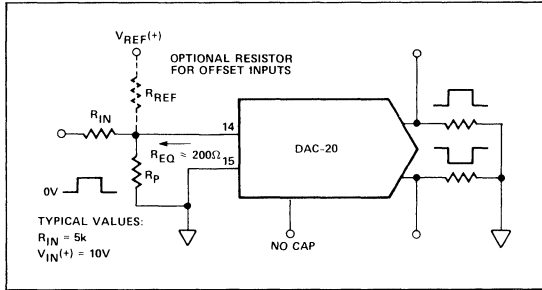


proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slow rate. For $R_{14} = 1k\Omega$ and $C_C = 15pF$, the reference amplifier slews at $4mA/\mu s$ enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by the alternate compensation scheme shown above. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier for a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at Pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of $16mV/\mu s$, which is relatively independent of R_{IN} and V_{IN} values.

PULSED REFERENCE OPERATION



POWER SUPPLY CONSIDERATIONS

The DAC-20 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of $\pm 5V$ or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at $-4.5V$ with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V total must be applied to insure turn-on of the internal bias network.

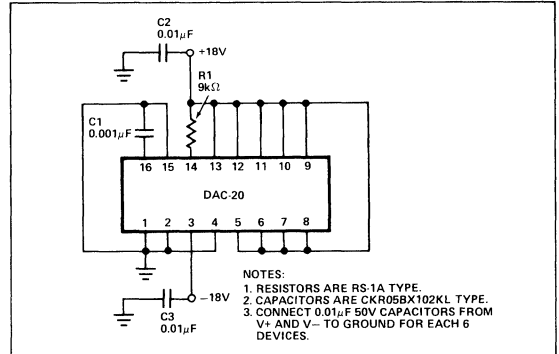
Symmetrical supplies are not required, as the DAC-20 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required:

however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power Consumption may be calculated as follows:

$P_d = (I+) \times (V+) + (I-) \times (V-)$. A useful feature of the DAC-20 design is that supply current is constant and independent of input logic states; this reduces the size of the power supply bypass capacitors.

BURN-IN CIRCUIT



TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specification of the DAC-20 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically $\pm 10ppm/^\circ C$, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift.

SETTLING TIME OPTIMIZATION

The DAC-20 is capable of extremely fast settling times, typically 85ns at $I_{REF} = 2.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The output capacitance of the DAC-20, including the package, is approximately 15pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; $0.1\mu F$ capacitors at the supply pins provide full transient protection.

Precision Monolithics Inc.

FEATURES

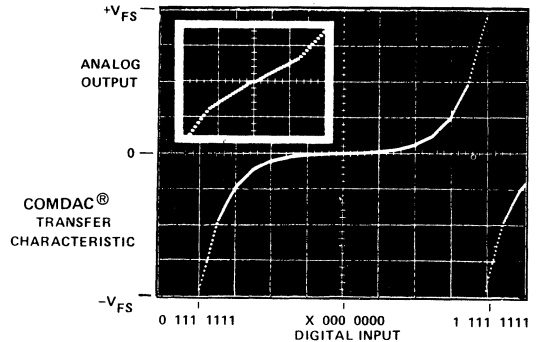
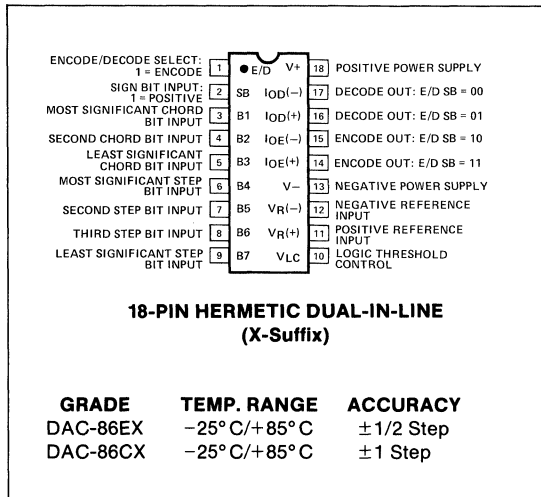
- Conforms With Bell System μ -255 Companding Law
- Meets D3 Compandor Tracking Specifications
- Both Encode and Decode Capability
- Tight Full-Scale Tolerance Eliminates Calibration
- Low Full-Scale Drift Over Temperature
- Extremely Low Noise Contribution
- Multiplying Reference Inputs
- Simplifies PCM System Design
- High Reliability
- Low Power Consumption and Low Cost
- Two Grades Available

GENERAL DESCRIPTION

The DAC-86 monolithic COMDAC® D/A Converter provides a 15 segment linear approximation to the Bell System μ -255 companding law. The law is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. A sign bit determines signal polarity, and an encode/decode input determines the mode of operation.

Accuracy is assured by specifying chord end point values, step nonlinearity, and monotonicity over the full operating temperature range. Typical applications include PCM carrier systems, digital PBX's intercom systems, and PCM recording. For CCITT "A" Law models, refer to the DAC-89 data sheet.

PIN CONNECTIONS & ORDERING INFORMATION



BELL μ -255 LAW TRANSFER CHARACTERISTIC

The DAC-86 transfer characteristic is a piecewise linear approximation to the Bell System μ -255 law expressed by:

$$Y(x) = \text{sgn}(x) \frac{\ln(1 + \mu |x|)}{\ln(1 + \mu)} - 1 \leq x \leq 1$$

for a normalized coding range of ± 1

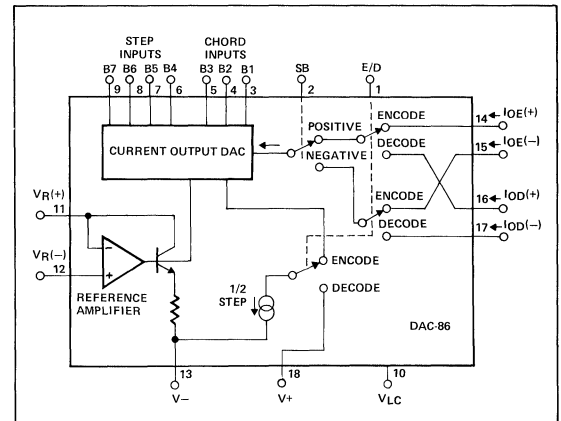
where: x = input signal level

Y = output compressed signal level

$\mu = 255$

This law is implemented with a eight chord (or segment) piecewise linear approximation with 16 linear steps in each chord. Dynamic range of 72dB in both polarities is achieved with eight-bit coding.

EQUIVALENT CIRCUIT





ABSOLUTE MAXIMUM RATINGS

V+ Supply to V- Supply 36V
 V_{LC} Swing V- plus 8V to V+
 Analog Current Outputs V- plus 8V to V- plus 36V
 Reference Inputs V- to V+
 Reference Input Differential Voltage ±18V
 Reference Input Current 1.25mA

Logic Inputs V- plus 8V to V- plus 36V
 Operating Temperature -25°C to +85°C
 Storage Temperature -65°C to +150°C
 Power Dissipation 500mW
 Derate Above 100°C 10mW/°C
 Lead Temperature (Soldering, 60 sec) 300°C

ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 528μA, -25°C ≤ T_A ≤ +85°C, for all 4 outputs, unless otherwise noted.

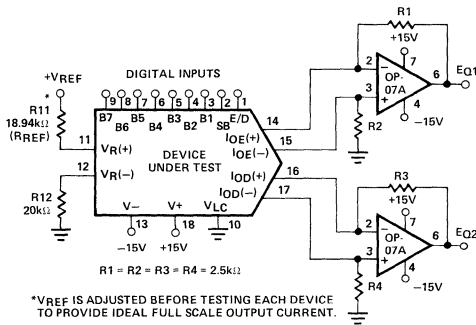
PARAMETER	SYMBOL	CONDITIONS	DAC-86E			DAC-86C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log (I _{7,15} /I _{0,1})	72	72	72	72	72	72	dB
Monotonicity		Sign-Bit + or -	128	-	-	128	-	-	Steps
Chord End-Point Accuracy All Chords		Error relative to ideal values at I _{FS} = 2007.75μA	-	-	±1/2	-	-	±1	Step
Encode Decision Level Current		Additional output encode/decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
Settling Time (Note 1)	t _S	To within ±1/2 step	-	1	-	-	1	-	μsec
Full-Scale Drift (C ₇) (Note 2)	ΔI _{FS}	Full temperature range	-	±1/16	±1/10	-	±1/10	±1/4	Step
Output Voltage Compliance	V _{OC}	Full-scale current change ≤ 1/2 step	-5	-	+18	-5	-	+18	Volts
Full-Scale Symmetry Error	I _{O(+)} - I _{O(-)}	Decode or encode pair Input Code 111 1111	-	±1/40	±1/8	-	±1/40	±1/4	Step
Zero-Scale Current (C ₀)	I _{ZS}	Measured at selected output with 000 0000 input	-	1/40	1/8	-	1/40	1/4	Step
Disable Current (All bits high)	I _{DIS}	Leakage of output disabled by E/D and SB	-	5	75	-	5	75	nA
Step Accuracy All Chords		Error relative to ideal values at I _{FS} = 2007.75μA	-	-	±1/2	-	-	±1	Step
Output Current Range	I _{FSR}		4.2	2.0	-	4.2	2.0	-	mA
Logic Input Levels, Logic "0"	V _{IL}	V _{LC} = 0V	-	-	0.8	-	-	0.8	Volts
Logic Input Levels, Logic "1"	V _{IH}	V _{LC} = 0V	2	-	-	2	-	-	Volts
Logic Input Current	I _{IN}	V _{IN} = -5V to +18V	-	-	120	-	-	120	μA
Logic Input Swing	V _{IS}	V- = -15V	-5	-	+18	-5	-	+18	Volts
Reference Bias Current	I ₁₂		-	-3	-12	-	-3	-12	μA
Reference Input Slew Rate	dI/dt		-	0.25	-	-	0.25	-	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	PSSI _{FS+} PSSI _{FS-}	V+ = 4.5V to 18V, V- = -15V V- = -10.8V to -18V, V+ = 15V	-	±1/20	±1/2	-	±1/20	±1/2	Step
Power Supply Current	I+	V _S = +5V, -15V, I _{FS} = 2.0mA	-	2.7	4.5	-	2.7	4.5	mA
	I-	V _S = +5V, -15V, I _{FS} = 2.0mA	-	-6.7	-9.3	-	-6.7	-9.3	
	I+	V _S = ±15V, I _{FS} = 2.0mA	-	2.7	4.5	-	2.7	4.5	
	I-	V _S = ±15V, I _{FS} = 2.0mA	-	-6.7	-9.3	-	-6.7	-9.3	
Power Dissipation	P _d	V _S = +5V, -15V, I _{FS} = 2.0mA V _S = ±15V, I _{FS} = 2.0mA	-	114 141	167 207	-	114 141	167 207	mW

NOTE:
 1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C₀) step size is 0.5μA, while in the last chord near full-scale (C₇) step size is 64μA. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading. In decode operation, the DAC-86

and OP-16 combination will decode eight channels. In the encode mode, the DAC-86 and CMP-01 combination will encode eight channels. Both encode and decode statements assume a 5.2μsec channel time.
 2. Guaranteed by design.



OUTPUT CURRENT DC TEST CIRCUIT



LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT
1	1	1	$I_{OE}(+)$ ($E_{O1}/R1$)
2	1	0	$I_{OE}(-)$ ($E_{O1}/R2$)
3	0	1	$I_{OD}(+)$ ($E_{O2}/R3$)
4	0	0	$I_{OD}(-)$ ($E_{O2}/R4$)

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonicity is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES ($I_{REF} = 528\mu A$)

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.5	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.25	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

NOTE:

These tables may be extended to include all of the encode/decode currents (ideal with $S I_{REF} = 528\mu A$) by multiplying any of the numbers in the normalized tables by $0.5\mu A$.

PARAMETER DEFINITIONS

FULL-SCALE DRIFT

The change in output current over the full operating temperature with $V_{REF} = 10.000V$, $R11 = 18.94k\Omega$, and $R12 = 20k\Omega$.

FULL-SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full-scale output.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes $< 1/2$ step change in output current.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord; used to specify accuracy.

STEPS

Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION

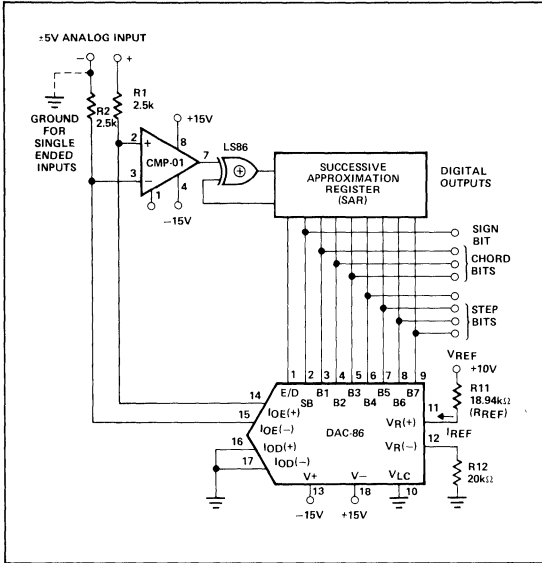
Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full-scale current.

DYNAMIC RANGE

Ratio of full-scale current to step size in chord zero, expressed in dB. This can be measured peak or peak-to-peak with the same result.



**BASIC ENCODE OPERATION
(COMPRESSING A/D CONVERSION)
BASIC ENCODE CONNECTIONS**



ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-86 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign-

magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear converter), the step size is a constant percentage of full-scale. In a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC) the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN-39 for detailed explanation.

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as a polarity detector. The encode/decode (E/D) input is held at a logic "0". In this mode, current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made.

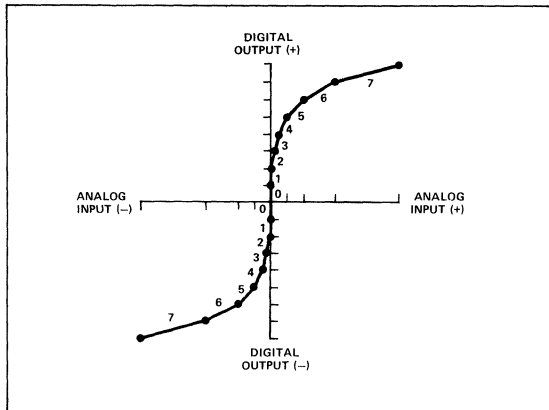
NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) ($I_{C,S} = 2\{2^C(S + 17) - 16.5\}$)

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256



**ENCODE TRANSFER CHARACTERISTICS
(A/D CONVERSION)**

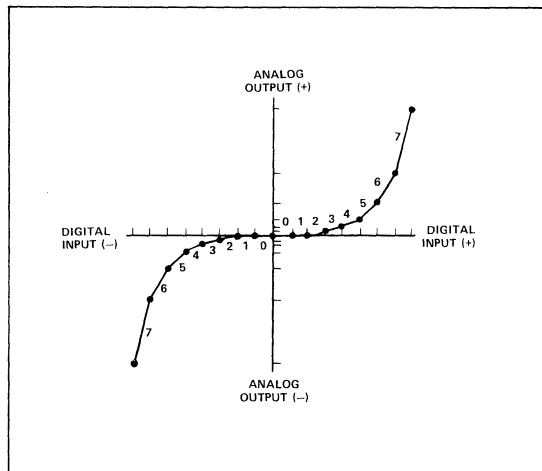


**BASIC DECODE OPERATION
(EXPANDING D/A CONVERSION)**

D/A conversion with the DAC-86 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the encode/decode input. This enables the $I_{OD(+)}$ or $I_{OD(-)}$ to be selected by the sign-bit input. When the sign-bit input is high, a logic "1", all of the output current flows into

$I_{OD(+)}$ forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", all of the output current flows into $I_{OD(-)}$ through R2 forcing a negative voltage output. The sign-bit steers current into $I_{OD(+)}$ or $I_{OD(-)}$, therefore the output will always be symmetrical, limited only by the matching of R1 and R2.

**DECODE TRANSFER CHARACTERISTIC
(D/A CONVERSION)**



NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) ($I_{C,S} = 2\{2^C(S + 16.5) - 16.5\}$)

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

NORMALIZED TABLES

The encode and decode tables are used to calculate the ideal output current at any point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. $343/8031 \times I_{FS} = 85.75\mu A$ ($I_{FS} = 2007.75\mu A$). Alternatively, use the condensed current tables and add up the number of steps.

BASIC REFERENCE CONSIDERATIONS

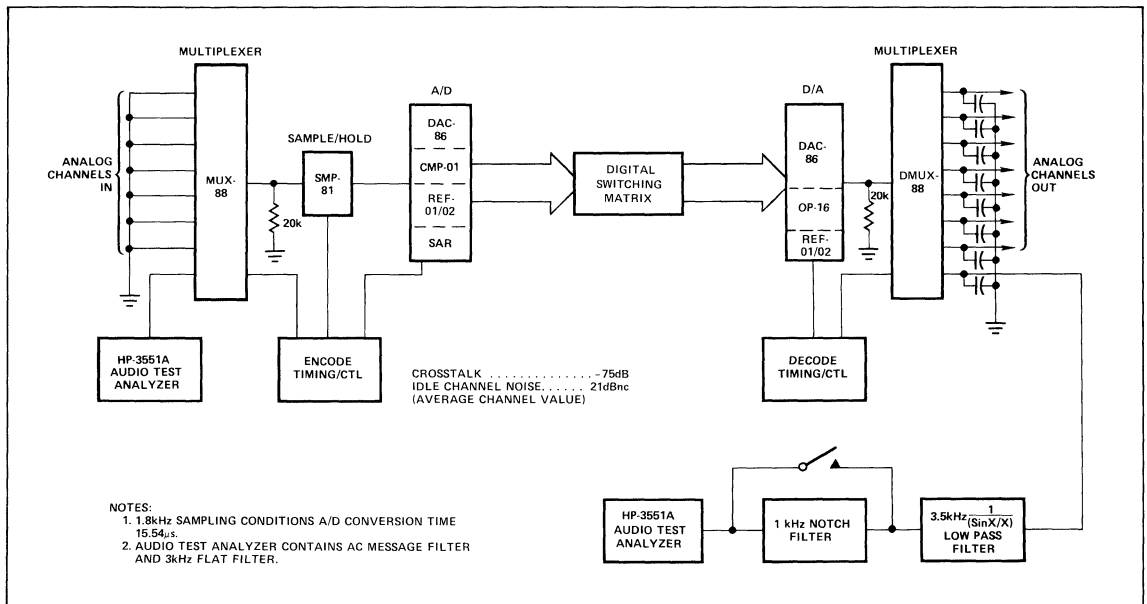
Full-scale output current is ideally $2007.75\mu A$ when the reference current is $528\mu A$ in the decode mode. In the encode mode $I_{FS} = 2039.75\mu A$ due to the additional 1/2 step ($32\mu A$). A percentage change in I_{REF} will produce the same percentage change in output current.

The large step size at full-scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with $V+ = 15V$, $R_{REF} = 15V/528\mu A$ or $28.4k\Omega$. When using a power supply as a reference, R11 becomes two resistors, R11A and R11B, and the junction bypassed to ground with a $0.1\mu F$ monolithic capacitor.

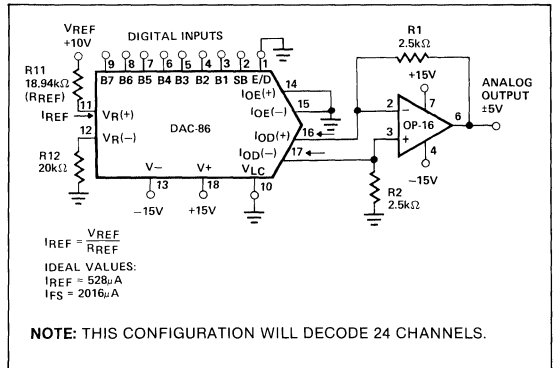
DECODE OUTPUT VOLTAGE

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	VOLT
POS FULL-SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0	0V
(-) ZERO-SCALE	0	0	0	0	0	0	0	0	0	0V
(-) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	0	1	-0.0012
NEG FULL-SCALE	0	0	1	1	1	1	1	1	1	-5.019V

SYSTEM TEST CIRCUIT



BASIC DECODE CONNECTIONS



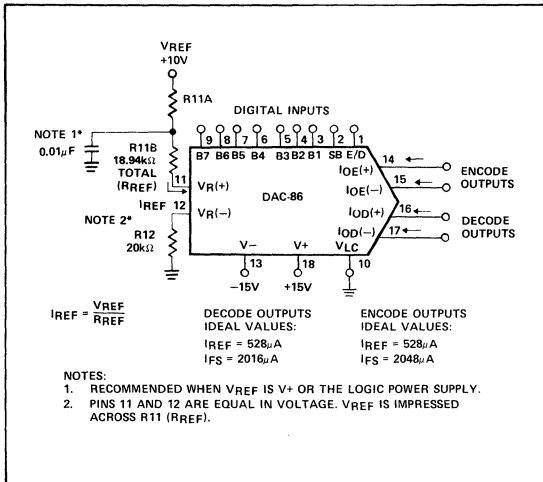
REFERENCE AMPLIFIER SETUP

The DAC-86 is a multiplying D/A converter. The output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full-scale output current is a linear function of the reference current.

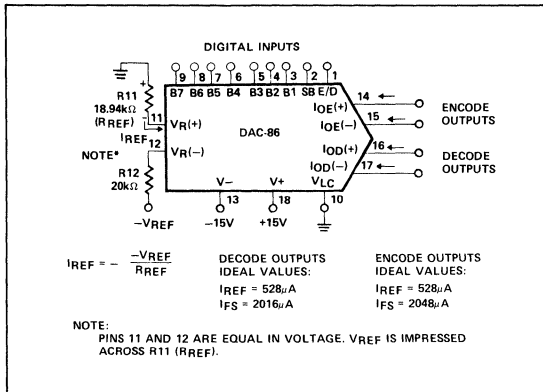
In external reference applications a positive reference voltage forces current through R11 in the $V_{R(+)}$ terminal (pin 11) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{R(-)}$ at pin 12; reference current flows from ground through R11 into $V_{R(+)}$. This negative reference connection has the advantage of presenting a very high impedance at pin 12. The voltage at pin 11 is equal to and tracks the voltage at pin 12 due to the high gain of the internal

reference amplifier. R12 (nominally equal to R11) is used to cancel bias current errors and may be eliminated with a minor increase in error.

POSITIVE REFERENCE OPERATION



NEGATIVE REFERENCE OPERATION



REFERENCE AMPLIFIER OPERATION

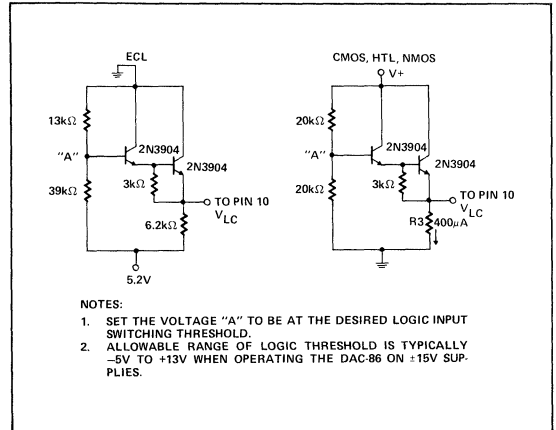
For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full-scale temperature performance. (This also minimizes the contributions of reference amplifier V_{OS} and TCV_{OS}). For most applications the tight relationship between I_{REF} and I_{FS} eliminates the need for trimming I_{REF} ; but if desired full-scale trimming is

accomplished by selecting R11 or by using a potentiometer for R11.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode voltage range. While the recommended operating range of DC reference current is 0.1mA to 1.0mA, monotonic operation is maintained over an even wider range.

LOGIC INPUT AND POWER SUPPLY CONSIDERATIONS

INTERFACING CIRCUIT FOR ECL, CMOS, HTL, AND NMOS LOGIC INPUTS



LOGIC INPUTS

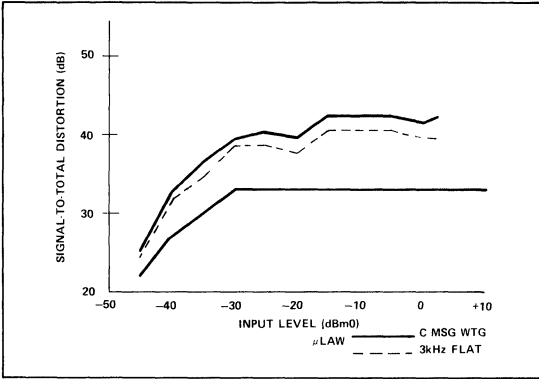
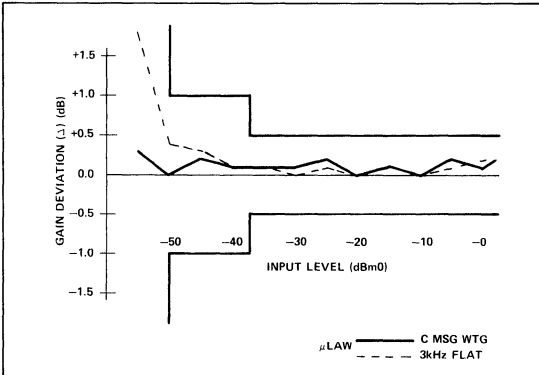
The DAC-86 interfaces with various logic families by referencing V_{LC} (pin 10) at a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at pin 10.

The negative voltage at the logic inputs must be limited to +10V with respect to $V-$ (pin 13).

POWER SUPPLIES

Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

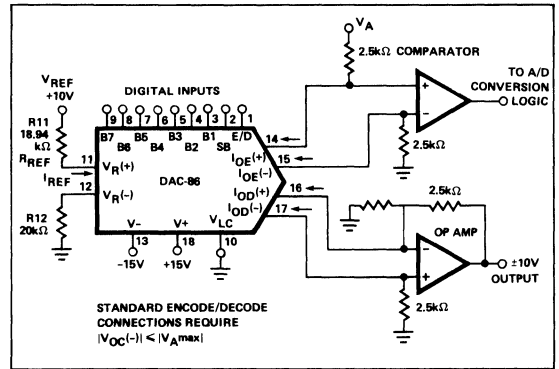
When operating with $V-$ between -15V and -11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common-mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between -15V and the $V-$ supply in use. Operation with $V+$ between +5V and +15V affects V_{LC} and the reference amplifier common-mode positive voltage range in the same manner.

SYSTEM PERFORMANCE CHARACTERISTICS
SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL

GAIN TRACKING

OUTPUT VOLTAGE COMPLIANCE

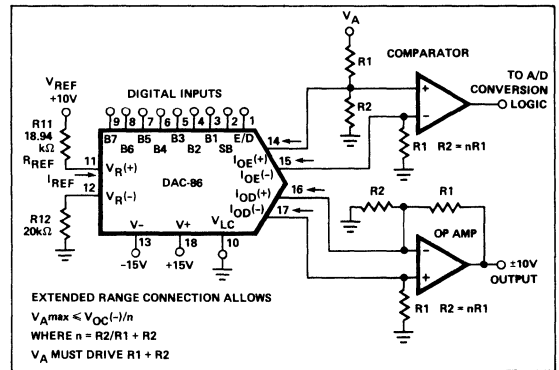
The DAC-86 has true current outputs with wide voltage compliance that enables single ended and balanced load drive capability. Positive voltage compliance is +18V and negative voltage compliance is -5.0V with $I_{REF} = 528\mu A$ and $V = -15V$. Negative voltage compliance $V_{OC(-)}$ for other values of I_{REF} and V may be obtained from the table, or calculated as follows:

$$V_{OC(-)} \text{ min} = (V-) + (2 I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the connections shown above.

STANDARD OUTPUT CONNECTIONS


STANDARD ENCODE/DECODE CONNECTIONS REQUIRE $|V_{OC(-)}| \leq |V_A \text{max}|$

OUTPUT COMPLIANCE EXTENSION CONNECTIONS


EXTENDED RANGE CONNECTION ALLOWS

$$V_A \text{max} \leq V_{OC(-)}/n$$

$$\text{WHERE } n = R2/R1 + R2$$

$$V_A \text{ MUST DRIVE } R1 + R2$$

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC(-)}$

V-	I_{FS}		
	1.0mA	2.0mA	4.0mA
-12V	-2.8V	-2.0V	-0.4V
-15V	-5.8V	-5.0V	-3.4V
-18V	-8.8V	-8.0V	-6.4V

MINIMUM NEGATIVE COMPLIANCE

$$V_{OC(-)} \text{ MIN} = (V-) + (2 I_{REF} 1.6k\Omega) + 8.4V$$

DICE

For applicable DICE information, see DAC-88 Data Sheet.

FEATURES

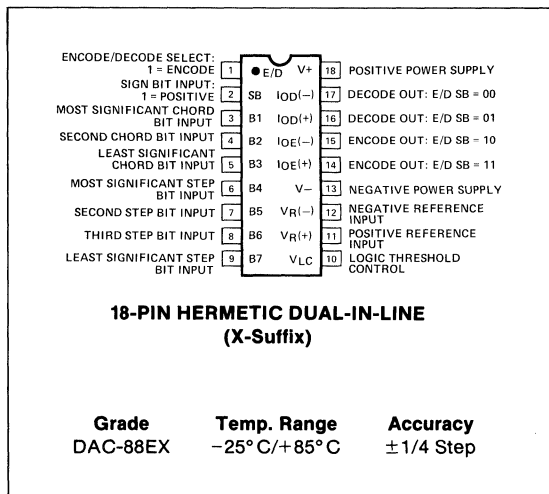
- IMPROVED ACCURACY over DAC-86
- IMPROVED SPEED over DAC-86
- Conforms With Bell System μ -255 Companding Law
- Meets D3 Compandor Tracking Specifications
- Both Encode and Decode Capability
- Tight Full-Scale Tolerance Eliminates Calibration
- Low Full-Scale Drift Over Temperature
- Extremely Low Noise Contribution
- Multiplying Reference Inputs
- Simplifies PCM System Design
- High Reliability
- Low Power Consumption and Low Cost
- Fully Specified Dice Available

GENERAL DESCRIPTION

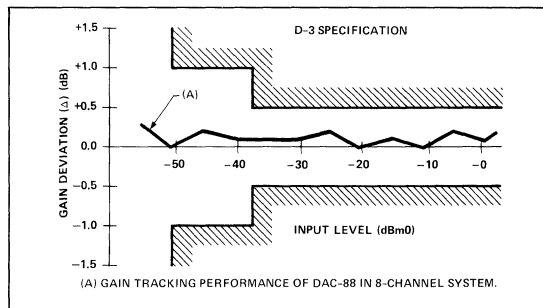
The DAC-88 monolithic COMDAC® D/A Converter provides a 15 segment linear approximation to the Bell System μ -255 companding law. The law is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. A sign bit determines signal polarity, and an encode/decode input determines the mode of operation.

Accuracy is assured by specifying chord end point values, step nonlinearity, and monotonicity over the full operating temperature range. Typical applications include PCM carrier systems, digital PBX's, intercom systems, and PCM recording. For CCITT "A" Law models, refer to the DAC-89 data sheet.

PIN CONNECTIONS & ORDERING INFORMATION



GAIN TRACKING



BELL μ -255 LAW TRANSFER CHARACTERISTIC

The DAC-88 transfer characteristic is a piecewise linear approximation to the Bell System μ 255 law expressed by:

$$Y(x) = \text{sgn}(x) \frac{\ln(1 + \mu |x|)}{\ln(1 + \mu)} \quad -1 \leq x \leq 1$$

for a normalized coding range of ± 1

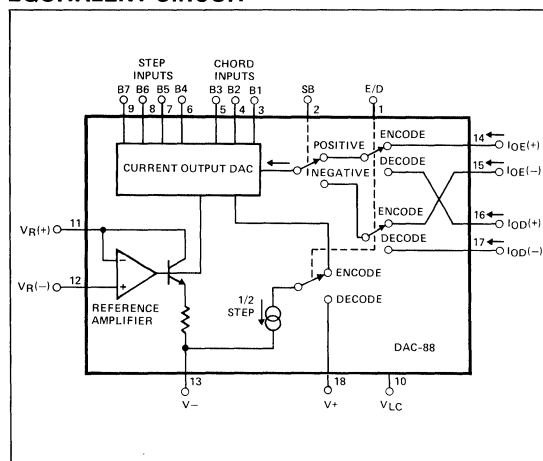
where: x = input signal level

Y = output compressed signal level

$\mu = 255$

This law is implemented with an eight chord (or segment) piecewise linear approximation with 16 linear steps in each chord. Dynamic range of 72dB in both polarities is achieved with eight-bit coding.

EQUIVALENT CIRCUIT



**ABSOLUTE MAXIMUM RATINGS**

V+ Supply to V- Supply	36V
V _{LC} Swing	V- plus 8V to V+
Analog Current Outputs	V- plus 8V to V- plus 36V
Reference Inputs	V- to V+
Reference Input Differential Voltage	± 18V
Reference Input Current	1.25mA
Logic Inputs	V- plus 8V to V- plus 36V

Operating Temperature	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Power Dissipation	500mW
Derate Above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ± 15V, I_{REF} = 528μA, -25°C ≤ T_A ≤ +85°C, all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-88E			UNITS
			MIN	TYP	MAX	
Resolution		8 chords with 16 steps each	± 128	± 128	± 128	Steps
Dynamic Range		20 log (I _{7,15} /I _{0,1})	72	72	72	dB
Monotonicity		Sign-Bit + or -	128	-	-	Steps
Chord End-Point Accuracy Chord Zero		Error relative to ideal values at I _{FS} = 2007.75μA	-	-	± 1/4	Step
Chord End-Point Accuracy All Chords Other Than Zero		Error relative to ideal values at I _{FS} = 2007.75μA	-	-	± 1/2	Step
Encode Decision Level Current		Additional output encode/decode = 1	3/8	1/2	5/8	Step
Settling Time (Note 1)	t _S	To within ± 1/2 step	-	500	-	ns
Settling Time in Chord Zero	T _{SCO}	To within ± 1/2 step	-	500	-	ns
Full-scale Drift (C ₇) (Note 3)	ΔI _{FS}	Full temperature range	-	± 1/16	± 1/10	Step
Output Voltage Compliance	V _{OC}	Full-Scale current change ≤ 1/2 step	-5	-	+18	Volts
Full-Scale Symmetry Error (Note 2)	I _{O(+)} - I _{O(-)}	Decode or encode pair Input Code 111 1111	-	± 1/40	± 1/8	Step
Zero-Scale Current (C ₀) (Note 2)	I _{ZS}	Measured at selected output with 000 0000 input	-	1/40	1/8	Step
Disable Current (All bits high) (Note 2)	I _{DIS}	Leakage of output disabled by E/D and SB	-	5	100	nA
Step Accuracy Chord Zero		Error relative to ideal values at I _{FS} = 2007.75μA	-	-	± 1/4	Step
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at I _{FS} = 2016μA	-	-	± 1/2	Step
Output Current Range	I _{FSR}		4.2	2.0	0	mA
Logic Input Levels, Logic "0"	V _{IL}	V _{LC} = 0V	-	-	0.8	Volts
Logic Input Levels, Logic "1"	V _{IH}	V _{LC} = 0V	2	-	-	Volts
Logic Input Current	I _{IN}	V _{IN} = -5V to +18V	-	-	120	μA
Logic Input Swing	V _{IS}	V- = -15V	-5	-	+18	Volts
Reference Bias Current	I ₁₂		-	-3	-12	μA
Reference Input Slew Rate	dI/dt		-	0.25	-	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	PSSI _{FS+} PSSI _{FS-}	V+ = 4.5V to 18V, V- = -15V V- = -10.8V to -18V, V+ = 15V	-	± 1/20 ± 1/10	± 1/2 ± 1/2	Step

NOTES:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C₀) step size is 0.5μA, while in the last chord near full-scale (C₇) step size is 64μA. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading. In decode operation, the DAC-88 and OP-16 combination will decode 24 channels. In the encode mode, the

DAC-88 and CMP-01 combination will encode eight channels. Both encode and decode statements assume a 5.2μs channel time.

- Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
- Guaranteed by design.



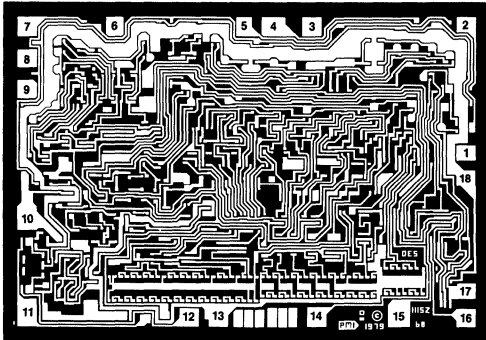
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25^\circ C \leq T_A \leq +85^\circ C$, all 4 outputs, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-88E			UNITS
			MIN	TYP	MAX	
Power Supply Current	I+	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	2.7	5.5	mA
	I-	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	-6.7	-12	
	I+	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	2.7	5.5	
	I-	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	-6.7	-12	
Power Dissipation	P_d	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	114	207	mW
		$V_S = \pm 15V, I_{FS} = 2.0mA$	—	141	262	
Full-Scale Current Deviation From Ideal Deviation (See Tables) (Note 2)	$I_{FS}(D)$	$V_{REF} 10.000V, T_A = 25^\circ C$	—	—	$\pm 1/2$	Step
	$I_{FS}(E)$	$R11 = 19.53k\Omega, R12 = 20k\Omega$	—	—	$\pm 1/2$	
Idle Current (Note 2)	I_I		—	10	—	μA

NOTE:

- Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.

DICE CHARACTERISTICS



- | | |
|----------------|------------------|
| 1. E/D | 10. V_{LC} |
| 2. SIGN-BIT | 11. $V_R (+)$ |
| 3. BIT 1 (MSB) | 12. $V_R (-)$ |
| 4. BIT 2 | 13. V^- |
| 5. BIT 3 | 14. $I_{OE} (+)$ |
| 6. BIT 4 | 15. $I_{OE} (-)$ |
| 7. BIT 5 | 16. $I_{OD} (+)$ |
| 8. BIT 6 | 17. $I_{OD} (-)$ |
| 9. BIT 7 (LSB) | 18. V^+ |

For additional DICE information refer to 1986 Data Book, Section 2.

DIE SIZE 0.123 × 0.085 inch, 10,455 sq. mils
(3.124 × 2.159 mm, 6.745 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25^\circ C$, all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-88N (NOTE 3) LIMIT	UNITS
Resolution		8 chords with 16 steps each	± 128	Steps MIN
Dynamic Range		$20 \log (I_{7, 15} / I_{0, 1})$	72	dB MIN
Monotonicity		Sign-Bit + or -	128	Steps MIN
Chord End-Point Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/4$	Step MAX
Chord End-Point Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/2$	Step MAX
Encode Decision Level Current		Additional output encode/decode = 1	3/8	Step MIN
			5/8	Step MAX
Output Voltage Compliance	V_{OC}	Full-scale current change $\leq 1/2$ step	-5	Volts MIN
			+18	Volts MAX



WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25^\circ C$, all 4 outputs, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-88N (NOTE 3) LIMIT	UNITS
Full-Scale Symmetry Error (Note 2)	$I_{O+} - I_{O-}$	Decode or encode pair Input Code 111 1111	$\pm 1/8$	Step MAX
Zero-Scale Current (Note 2)	I_{ZS}	Measured at selected output 000 0000 input	1/8	Step Max
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	100	nA MAX
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/4$	Step MAX
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	$\pm 1/2$	Step MAX
Output Current Range	I_{FSR}		4.2	mA MIN
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	0.8	Volts MAX
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2	Volts MIN
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	120	μA MAX
Logic Input Swing	V_{IS}	$V_- = -15V$	-5 +18	Volts MIN Volts MAX
Reference Bias Current	I_{12}		-12	μA MAX
Power Supply Sensitivity Over Supply Range	$PSSI_{FS-}$ $PSSI_{FS-}$	$V_+ = 4.5V$ to $18V$ $V_- = -10.8V$ to $-18V$	$\pm 1/2$ $\pm 1/2$	Step MAX Step MAX
Power Supply Current	I_+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.75	mA MAX
	I_-		-12.0	
	I_+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.75	mA MAX
	I_-		-12.0	
Full-Scale Current Deviation From Ideal Deviation (See Tables) (Note 2)	$I_{FS}D$	$V_{REF} 10.000V$, $T_A = 25^\circ C$	$\pm 1/2$	Step MAX
	$I_{FS}E$	$R_{11} = 19.53k\Omega$ $R_{12} = 20k\Omega$	$\pm 1/2$	Step MAX

NOTE:

Electrical tests performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $T_A = 25^\circ C$, unless otherwise noted.

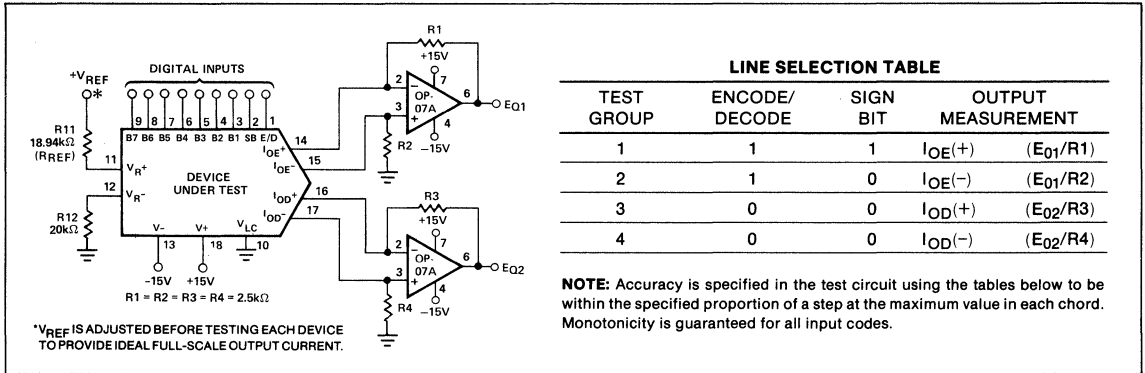
PARAMETER	SYMBOL	CONDITIONS	DAC-88N TYPICAL	UNITS
Settling Time (Note 1)	t_S	To within $\pm 1/2$ step	500	ns
Settling Time in Chord Zero	T_{SCO}	To within $\pm 1/2$ step	500	ns
Full-Scale Drift (C_7)	ΔI_{FS}	Full temperature range	$\pm 1/16$	Step
Reference Input Slew Rate	dI/dt		0.25	mA/ μs
Power Dissipation	P_D	$V_S + 5V$, $-15V$	114	mW
	P_D	$V_S = \pm 15V$	141	mW
Idle Current (Note 2)	I_I		10	μA

NOTES:

- In a companding DAC, the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is $0.5\mu A$. While in the last chord near full-scale (C_7) step size is $64\mu A$. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading.
- Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
- See DAC-88E for typical values.



OUTPUT CURRENT DC TEST CIRCUIT



LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT
1	1	1	$I_{OE}(+)$ ($E_{01}/R1$)
2	1	0	$I_{OE}(-)$ ($E_{01}/R2$)
3	0	0	$I_{OD}(+)$ ($E_{02}/R3$)
4	0	0	$I_{OD}(-)$ ($E_{02}/R4$)

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonicity is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES ($I_{REF} = 528\mu A$)

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.50	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

NOTE: These tables may be extended to include all of the encode/ decode currents (ideal with $I_{REF} = 528\mu A$) by multiplying any of the numbers in the normalized tables by 0.25 μA .

PARAMETER DEFINITIONS

FULL-SCALE DRIFT

The change in output current over the full operating temperature with $V_{REF} = 10.000V$, $R11 = 18.94k\Omega$, and $R12 = 20k\Omega$.

ENCODE CURRENT

The difference between $I_{OE}(+)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OD}(-)$ at any code.

FULL-SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full-scale output.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes < 1/2 step change in output current.

IDEAL OUTPUT CURRENT

The difference between the (+) and (-) currents (encode or decode) at any code.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord; used to specify accuracy.

STEPS

Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION

Each output current level may be designated by the code I_{CS} where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{1,15}$ = full-scale current.

DYNAMIC RANGE

Ratio of full scale current to step size in chord zero, expressed in dB.

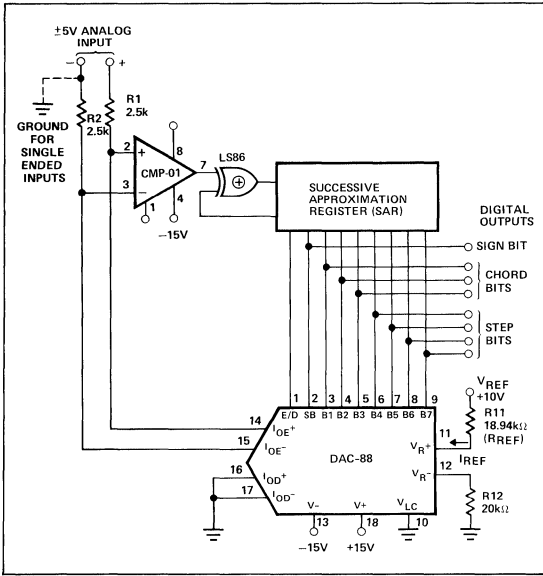


BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

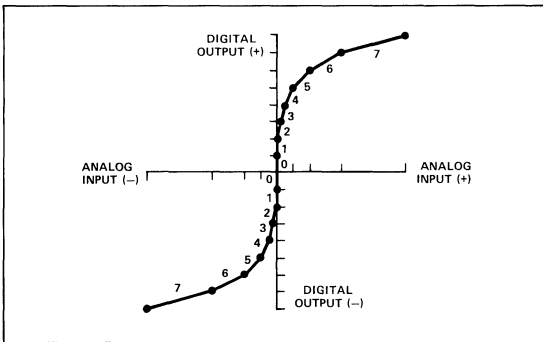
ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-88 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear converter), the step size is a constant percentage of full-scale. In a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

BASIC ENCODE CONNECTIONS



ENCODE TRANSFER CHARACTERISTICS (A/D CONVERSION)



When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC) the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN 39 for detailed explanation.

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as polarity detector only. The Encode/Decode (E/D) input is held at a logic "0". In this mode current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$.

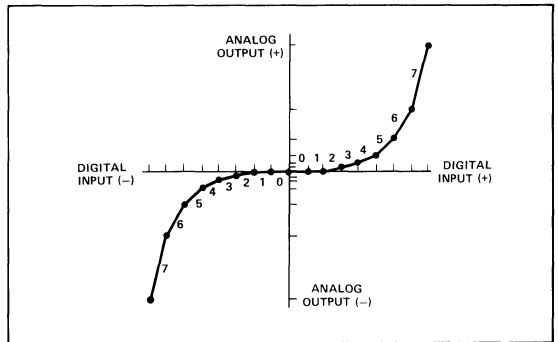
For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made.

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

D/A conversion with the DAC-88 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This mode enables the $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the sign-bit input. When the sign-bit input is high, a logic "1", all of the output current flows into

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)





$I_{OD(+)}$ forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", all of the output current flows into $I_{OD(-)}$ through R2 forcing a negative voltage output. The sign-bit steers current into $I_{OD(+)}$ or $I_{OD(-)}$, the output will therefore always be symmetrical, limited only by the matching of R1 and R2.

NORMALIZED TABLES

The encode and decode tables are used to calculate ideal output current at any point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. $343/8031 \times I_{FS} = 85.75\mu A$ ($I_{FS} = 2007.75\mu A$). Alternatively, use the condensed current tables and add up the number of steps.

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) ($I_{C,S} = 2[2^C(S + 17) - 16.5]$)

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

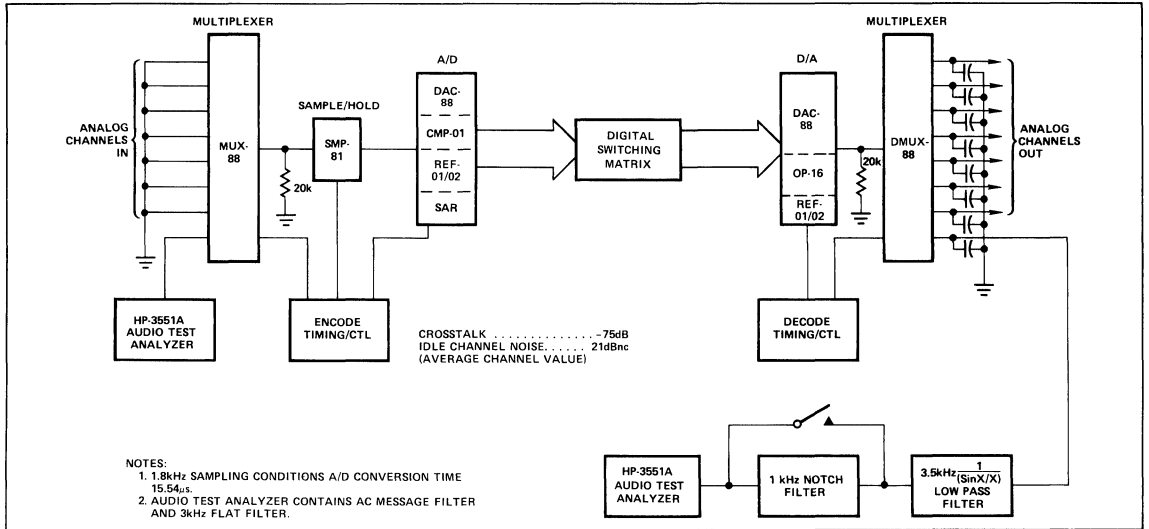
NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) ($I_{C,S} = 2[2^C(S + 16.5) - 16.5]$)

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4291
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	212	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256



SYSTEM TEST CIRCUIT



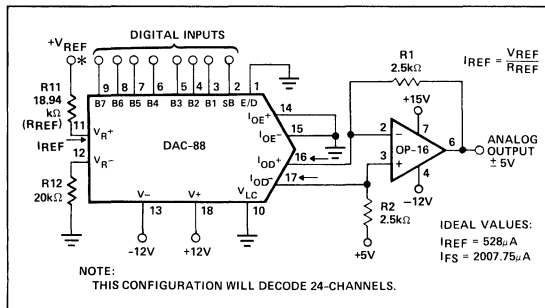
BASIC REFERENCE CONSIDERATIONS

Full-scale output current is ideally 2007.75 μ A when the reference current is 528 μ A in the decode mode. In the encode mode $I_{FS} = 2039.75\mu A$ due to the additional 1/2 step (32 μ A). A percentage change in I_{REF} will produce the same percentage change in output current.

DECODE OUTPUT VOLTAGE

	E/D	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL-SCALE	0	1	1	1	1	1	1	1	5.019V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	0.0012V
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0V
(-) ZERO-SCALE	0	0	0	0	0	0	0	0	0V
(-) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	1	-0.0012V
NEG FULL-SCALE	0	0	1	1	1	1	1	1	-5.019V

BASIC CONNECTIONS



The large step size at full-scale allows the use of inexpensive references in many applications. In some applications V_{REF} may even be the positive power supply. For example, with $V+ = 15V$, $R_{REF} = 15V/528\mu A$ or 28.4k Ω . When using a power supply as a reference, R11 becomes two resistors, R11A and R11B, and the junction bypassed to ground with a 0.1 μ F monolithic capacitor.

REFERENCE AMPLIFIER OPERATION

The DAC-88 is a multiplying D/A converter. The output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full-scale output current is a linear function of the reference current and is given for all four outputs in the figures above.

REFERENCE RECOMMENDATIONS

For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full-scale temperature performance.

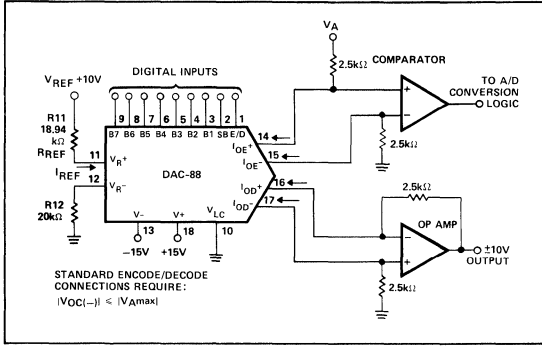
POWER SUPPLIES

Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

When operating with $V-$ between -15V and -11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common-mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between -15V and the $V-$ supply. Operation with $V+$ between +5V and +15V affects V_{LC} and the reference amplifier common-mode positive voltage range in the same manner.



STANDARD OUTPUT CONNECTIONS



capability. Positive voltage compliance is +18V and negative voltage compliance is -5.0V with $I_{REF} = 528\mu A$ and $V = -15V$. Negative voltage compliance $V_{OC(-)}$ for other values of I_{REF} and V may be obtained from the table, or calculated as follows:

$$V_{OC(-)} \text{ min} = (V-) + (2 I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the connections shown in the compliance extension diagram.

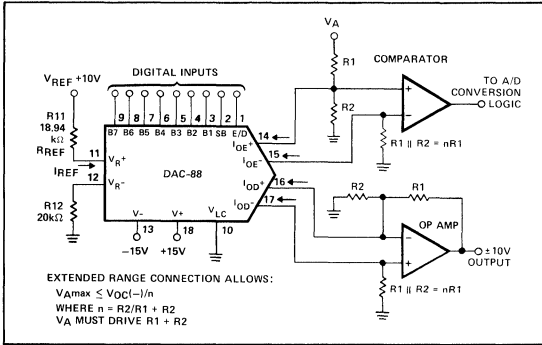
NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC(-)}$

V-	1.0mA	I_{FS} 2.0mA	4.0mA
-12V	-2.8V	-2.0V	-0.4V
-15V	-5.8V	-5.0V	-3.4V
-18V	-8.8V	-8.0V	-6.4V

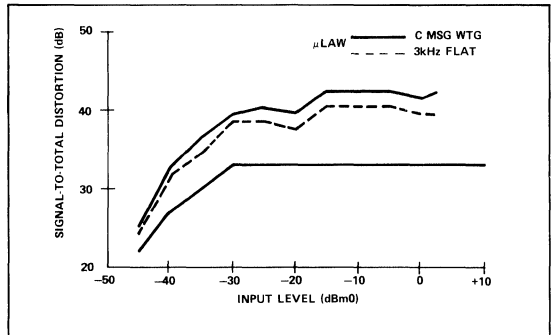
MINIMUM NEGATIVE COMPLIANCE

$$V_{OC(-)} \text{ MIN} = (V-) + (2 I_{REF} 1.6k\Omega) + 8.4V$$

COMPLIANCE EXTENSION CONNECTIONS



SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL

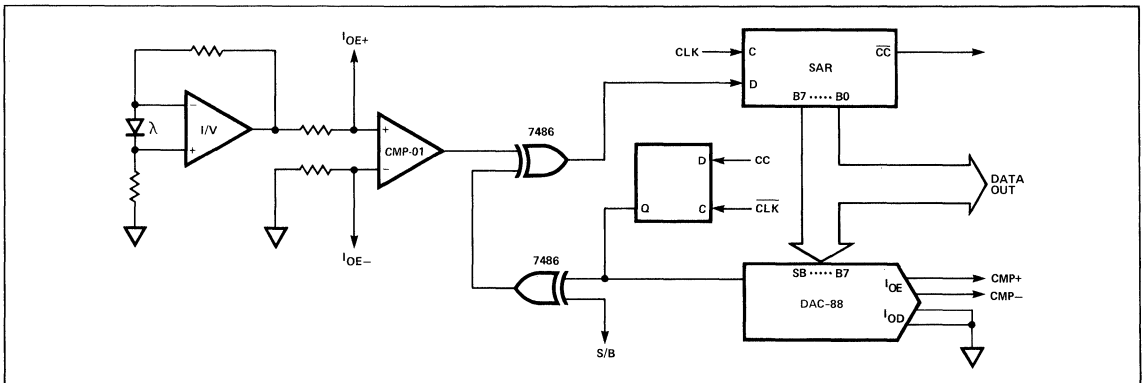


OUTPUT VOLTAGE COMPLIANCE

The DAC-88 has true current outputs with wide voltage compliance that enables single ended and balanced load driving

APPLICATIONS

PHOTODIODE LINEARIZING CIRCUIT



Precision Monolithics Inc.

FEATURES

- 11-Bit Accuracy and Resolution Around Zero
- Sign Plus 66dB Dynamic Range
- True Current Outputs: -5V to +18V Compliance
- Tight Full-Scale Tolerance Eliminates Calibration
- Low Full-Scale Drift Over Temperature
- Low Power Consumption and Low Cost
- Ideal for PCM and 8-Bit μ P Applications
- Outputs Multiplexed for Time Shared Applications
- Fully Specified Dice Available

GENERAL DESCRIPTION

The DAC-89 monolithic COMDAC® converter provides the complete decode function for "A" Law PCM CODECS. The DAC-89 may be configured in an encoder, decoder, or time-shared between encoding and decoding.

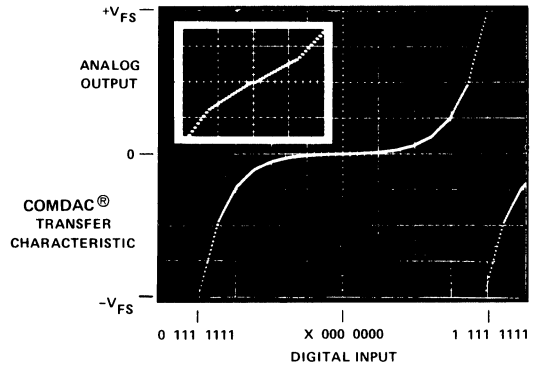
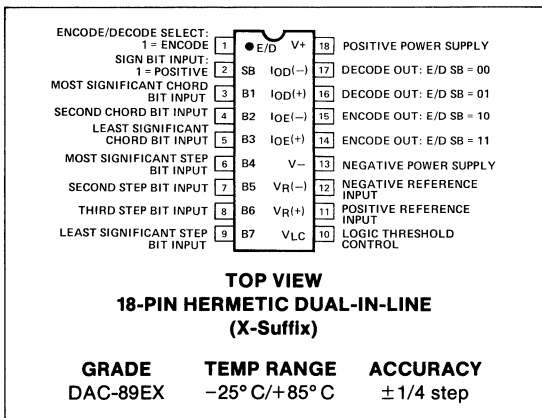
Specifying chord end-point values assures accuracy chord nonlinearity, and monotonicity over the full operating temperature range. For companding D/A converters with Bell μ -255 law conformance, refer to the DAC-88 data sheet. For industrial, process control, and audio applications, see the DAC-86 data sheet.

CCITT "A" LAW CHARACTERISTIC

The DAC-89 output is an approximation to the CCITT "A" law which can be expressed as:

$$Y = \frac{1 + \ln AX}{1 + \ln A} \quad 1/A \leq X \leq 1$$

PIN CONNECTIONS & ORDERING INFORMATION



$$Y = \frac{AX}{1 + \ln A} \quad 0 \leq X \leq 1/A \text{ where:}$$

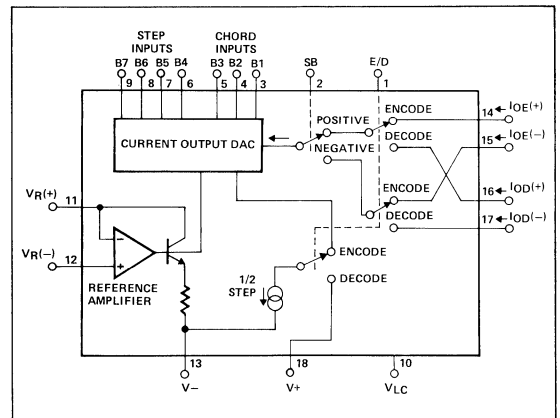
X = Normalized input signal level of the compressor (encoder), V_{IN}/V_{FS} .

Y = Output signal level of the compressor (encoder).

$$A = 87.6$$

The DAC-89 implements this law with an eight chord (or segment) piecewise linear approximation for each polarity with sixteen linear steps in each chord. The first two chords are co-linear and of equal step size, and may be considered as one chord of 32 steps. Step sizes of the remaining six chords are binarily related to the first chord.

EQUIVALENT CIRCUIT



**ABSOLUTE MAXIMUM RATINGS**

V+ Supply to V- Supply	36V
V _{LC} Swing	V- plus 8V to V+
Analog Current Outputs	V- plus 8V to V- plus 36V
Reference Inputs	V- to V+
Reference Input Differential Voltage	±18V
Reference Input Current	1.25mA
Logic Inputs	V- plus 8V to V- plus 36V

Operating Temperature Range	-25° C to +85° C
Storage Temperature Range	-65° C to +150° C
Power Dissipation	500mW
Derate Above 100° C	10mW/° C
Lead Temperature (Soldering, 60 sec)	300° C

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 512μA, -25° C ≤ T_A ≤ +85° C, all 4 outputs, unless otherwise noted. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C₀) step size is 1.0μA, while in the last chord near full-scale (C₇) step size is 64μA.

PARAMETER	SYMBOL	CONDITIONS	DAC-89E			UNITS
			MIN	TYP	MAX	
Resolution		8 chords with 16 steps each	±128	±128	±128	Steps
Dynamic Range		20 log (I _{7,15} /I _{0,0})	66	—	66	dB
Monotonicity		Sign Bit + or -	128	—	—	Steps
Chord End-Point Accuracy Chord Zero		Error relative to ideal values at I _{FS} = 2016μA	—	—	±1/4	Step
Chord End-Point Accuracy All Chords Other Than Zero		Error relative to ideal values at I _{FS} = 2016μA	—	—	±1/2	Step
Step Accuracy Chord Zero		Error relative to ideal values at I _{FS} = 2016μA	—	—	±1/4	Step
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at I _{FS} = 2016μA	—	—	±1/2	Step
Encode Decision Level Current		Additional output Encode/Decode = 1	1/4	1/2	3/4	Step
Settling Time (Note 1)	t _S	To within ±1/2 step	—	500	—	ns
Full-Scale Drift (Note 3)	ΔI _{FS}	Full temperature range	—	±1/20	±1/4	Step
Output Voltage Compliance	V _{OC}	Full-scale current change ≤ 1/2 step	-5	—	+18	Volts
Full-Scale Current Deviation from Ideal (See Tables) (Note 2)	I _{FS(D)} I _{FS(E)}	V _{REF} 10.000V T _A = 25° C R11 = 19.53kΩ, R12 = 20kΩ	—	—	±1/2	Step Step
Full-Scale Symmetry Error (Note 2)	I _{O(+)} - I _{O(-)}	Decode or Encode pair	—	±1/40	±1/8	Step
Zero-Scale Current (Note 2)	I _{ZS}	Measured at selected output with 000 0000 input	1/4	1/2	3/4	Step
Disable Current (Note 2)	I _{DIS}	Disabled by E/D and SB	—	5.0	100	nA
Idle Current (Note 2)	I _I		—	10	—	μA
Output Current Range	I _{FSR}	V _{REF} = 25.000V T _A = 25° C	4.2	2.0	0	mA
Logic Input Levels, Logic "0"	V _{IL}	V _{LC} = 0V	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V _{IH}	V _{LC} = 0V	2.0	—	—	Volts
Logic Input Current	I _{IN}	V _{IN} = -5V to +18V	—	—	120	μA
Logic Input Swing	V _{IS}	V- = -15V	-5	—	+18	Volts
Reference Bias Current	I _{I2}		—	-3	-12	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	PSSI _{FS+} PSSI _{FS-}	V+ = 4.5V to 18V, V- = -15V V- = -10.8V to -18V, V+ = 15V	—	±1/20 ±1/10	±1/2 ±1/2	Step

NOTES:

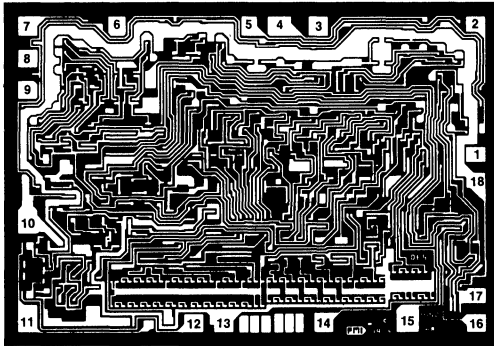
- Settling time varies for each of the chord bits and step bits and a maximum specification may be misleading. In decode operation, the DAC-89 and OP-16 combination will decode 8 channels. In the encode mode, the DAC-89 and CMP-01 combination will encode 8 channels. Both encode and decode statements assume a 3.9μs channel time.
- Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
- Guaranteed by design.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 512\mu A$, $-25^\circ C \leq T_A \leq +85^\circ C$, all 4 outputs, unless otherwise noted. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is $1.0\mu A$, while in the last chord near full-scale (C_7) step size is $64\mu A$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-89E			UNITS
			MIN	TYP	MAX	
Power Supply Current	I+	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	2.7	5.5	mA
	I-	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	-6.7	-12	
	I+	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	2.7	5.5	
	I-	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	-6.7	-12	
Power Dissipation	P_d	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	114	207	mW
		$V_S = \pm 15V, I_{FS} = 2.0mA$	—	141	262	

DICE CHARACTERISTICS



DIE SIZE 0.123 × 0.085 inch, 10.455 sq. mils
(3.124 × 2.159 mm, 6.745 sq. mm)

- | | |
|----------------|------------------|
| 1. E/D | 10. V_{LC} |
| 2. SIGN-BIT | 11. $V_R (+)$ |
| 3. BIT 1 (MSB) | 12. $V_R (-)$ |
| 4. BIT 2 | 13. V_- |
| 5. BIT 3 | 14. $I_{OE} (+)$ |
| 6. BIT 4 | 15. $I_{OE} (-)$ |
| 7. BIT 5 | 16. $I_{OD} (+)$ |
| 8. BIT 6 | 17. $I_{OD} (-)$ |
| 9. BIT 7 (LSB) | 18. V_+ |

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25^\circ C$, all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-89N (NOTE 3) LIMIT	UNITS
Resolution		8 chords with 16 steps each	± 128	Steps MIN
Dynamic Range		$20 \log (I_{7,15}/I_{0,1})$	66	dB MIN
Monotonicity		Sign-Bit + or -	128	Steps MIN
Chord End-point Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/4$	Step MAX
Chord End-point Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/2$	Step MAX
Encode Decision Level Current		Additional output encode/decode = 1	1/4 3/4	Step MIN Step MAX
Output Voltage Compliance	V_{OC}	Full-scale current change $\leq 1/2$ step	-5 +18	Volts MIN Volts MAX
Full-Scale Symmetry Error (Note 2)	$I_{O+} - I_{O-}$	Decode or encode pair Input Code 111 1111	$\pm 1/8$	Step MAX
Zero-Scale Current (Note 2)	I_{ZS}	Measured at selected output 000 0000 input	1/4	Step Max
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	100	nA MAX



WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25^\circ C$, all 4 outputs, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-89N (NOTE 3) LIMIT	UNITS
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/4$	Step MAX
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	$\pm 1/2$	Step MAX
Output Current Range	I_{FSR}	$V_{REF} = 25.000V$, $T_A = 25^\circ C$	4.2	mA MIN
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	0.8	Volts MAX
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2	Volts MIN
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	120	μA MAX
Logic Input Swing	V_{IS}	$V_- = -15V$	-5 +18	Volts MIN Volts MAX
Reference Bias Current	I_{12}		-12	μA MAX
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS-}$	$V_+ = 4.5V$ to $18V$	$\pm 1/2$	Step MAX
	$PSSI_{FS-}$	$V_- = 10.8V$ to $-18V$	$\pm 1/2$	Step MAX
Power Supply Current	I+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.5	mA MAX
	I-		-12.0	
	I+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.75	mA MAX
	I-		-12.0	
Full-Scale Current Deviation From Ideal Deviation (See Tables) (Note 2)	I_{FSD}	$V_{REF} = 10.000V$, $T_A = 25^\circ C$	$\pm 1/2$	Step MAX
	I_{FSE}	$R_{11} = 19.53k\Omega$ $R_{12} = 20k\Omega$	$\pm 1/2$	Step MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $T_A = 25^\circ C$, unless otherwise noted.

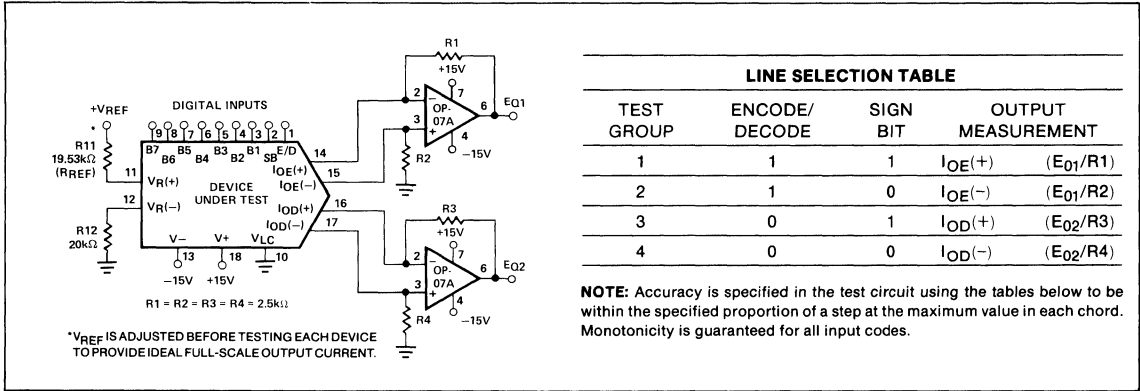
PARAMETER	SYMBOL	CONDITIONS	DAC-89N TYPICAL	UNITS
Settling Time (Note 1)	t_S	To within $\pm 1/2$ step	500	ns
Settling Time in Chord Zero	T_{SCO}	To within $\pm 1/2$ step	500	ns
Full-Scale Drift (C_7)	ΔI_{FS}	Full temperature range	$\pm 1/20$	Step
Reference Input Slew Rate	dI/dt		0.25	mA/ μs
Power Dissipation	P_D	$V_S + 5V$, $-15V$	114	mW
	P_D	$V_S = \pm 15V$	141	mW
Idle Current (Note 2)	I_I		10	μA

NOTES:

- In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is $0.5\mu A$. While in the last chord near full-scale (C_7) step size is $64\mu A$. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading.
- Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
- See DAC-89E for typical values.



OUTPUT CURRENT DC TEST CIRCUIT



LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT
1	1	1	IOE(+) (E01/R1)
2	1	0	IOE(-) (E01/R2)
3	0	1	IOD(+) (E02/R3)
4	0	0	IOD(-) (E02/R4)

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonicity is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	17	34	68	136	272	544	1088
15	1111	16	32	64	128	256	512	1024	2048
STEP SIZE		1	1	2	4	8	16	32	64

NOTE:

These tables may be extended to include all of the encode/decode currents (ideal with IREF = 512μA) by multiplying any of the numbers in the normalized tables by 0.5μA.

PARAMETER DEFINITIONS

STEP NONLINEARITY

Step size deviation from ideal within a chord.

ENCODE CURRENT

The difference between IOE(+) and IOD(+) or the difference between IOE(-) and IOD(-) at any code.

FULL-SCALE DRIFT

The change in output current over the full operating temperature with VREF = 10.000V, R11 = 19.53kΩ, and R12 = 20kΩ.

FULL-SCALE SYMMETRY ERROR

The difference between IOD(-) and IOD(+) or the difference between IOE(-) and IOE(+) at full-scale output.

IDEAL OUTPUT CURRENT

The difference between the (+) and (-) currents (encode or decode) at any code.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes < 1/2 step change in output current.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord; used to specify accuracy.

STEPS

Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION

Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full-scale current.

DYNAMIC RANGE

Ratio of full-scale current to step size in chord zero expressed in dB.

**BASIC ENCODE OPERATION
(COMPRESSING A/D CONVERSION)**

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as a polarity detector only. The Encode/Decode (E/D) input is held at logic "0". In this mode current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

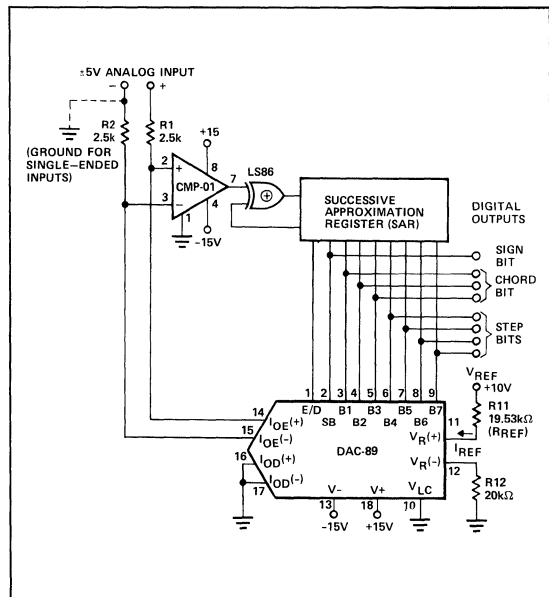
The bits are converted with a successive removal technique starting with a decision at the code 011 1111 and sequentially turning off bits until all decisions have been made.

ENCODE DECISION LEVELS

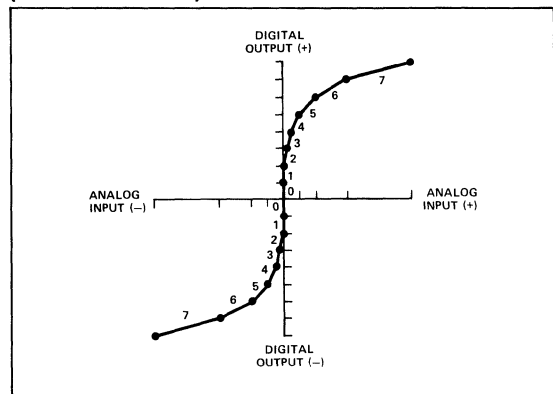
Compressing A/D conversion with the DAC-89 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign-magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear) converter, the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC), the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN 39 for detailed explanation.

BASIC DECODE CONNECTIONS



**ENCODE TRANSFER CHARACTERISTIC
(A/D CONVERSION)**



NORMALIZED ENCODE DECISION LEVELS (SIGN-BIT EXCLUDED)

NORMALIZED ENCODE DECISION

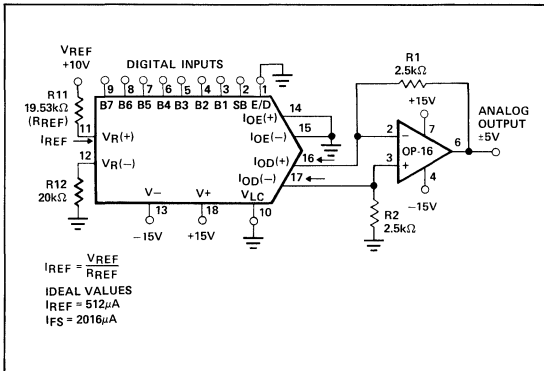
STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	36	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	*4096
STEP SIZE		2	2	4	8	16	32	64	128

*Virtual Decision Level

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

D/A conversion with the DAC-89 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This mode enables the I_{OD} outputs, disables the I_{OE} outputs, and allows I_{OD}(+) or I_{OD}(-) to be selected by the sign-bit input. When the sign-bit input is high, logic "1", the output current flows into I_{OD}(+) forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", the output current flows into I_{OD}(-) through R2 forcing a negative voltage output. The sign-bit steers current into I_{OD}(+) or I_{OD}(-), the output will therefore always be symmetrical, limited only by the matching of R1 and R2.

BASIC DECODE CONNECTIONS

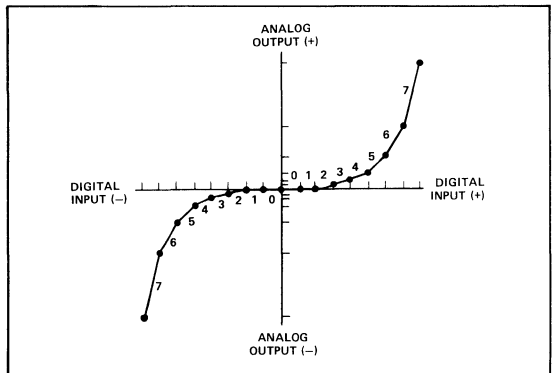


NORMALIZED TABLES

The encode and decode tables are used to calculate ideal output current at any code point. For example, in decode mode at I_{3,7} (011 0111) find 188. 188/4032 times I_{FS} of 2016μA equals 94μA.

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E ₀
POS FULL-SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0	0.004V
(-) ZERO-SCALE	0	0	0	0	0	0	0	0	0	0.004V
(-) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	0	1	-0.0012V
NEG FULL-SCALE	0	0	1	1	1	1	1	1	1	-5.040V

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



**NORMALIZED DECODE OUTPUT (SIGN-BIT EXCLUDED)****NORMALIZED DECODE OUTPUT**

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	472	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

BASIC REFERENCE CONSIDERATIONS

Full-scale output current is ideally $2016\mu\text{A}$ when the reference current is $512\mu\text{A}$ in the decode mode. In the encode mode $I_{\text{FS}} = 2048\mu\text{A}$ due to the additional one-half step ($32\mu\text{A}$). A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

The large step size at full scale allows the use of inexpensive references in many applications. In some applications V_{REF} may even be the positive power supply. For example, with $V^+ = 15\text{V}$, $R_{\text{REF}} = 15\text{V}/512\mu\text{A}$ or $29.3\text{k}\Omega$. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction bypassed to ground to provide decoupling.

OUTPUT VOLTAGE COMPLIANCE

The DAC-89 has true current outputs with wide voltage compliance that enables single ended and balanced load driving capability. Positive voltage compliance is $+18\text{V}$ and negative voltage compliance is -5.0V with $I_{\text{REF}} = 512\mu\text{A}$ and $V = -15\text{V}$. Negative voltage compliance $V_{\text{OC}}(-)$ for other values of I_{REF} and V^- may be obtained from the table, or calculated as follows:

$$V_{\text{OC}}(-) \text{ min} = (V^-) + (2 I_{\text{REF}} \times 1.6\text{k}\Omega) + 8.4\text{V}$$

Output voltage compliance can be extended in both encode and decode modes using the output compliance extension connections. (Figures 1 and 2).

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{\text{OC}}(-)$

V^-	1.0mA	I_{FS} 2.0mA	4.0mA
-12V	-2.8V	-2.0V	-0.4V
-15V	-5.8V	-5.0V	-3.4V
-18V	-8.8V	-8.0V	-6.4V

MINIMUM NEGATIVE COMPLIANCE

$$V_{\text{OC}}(-) \text{ MIN} = (V^-) + (2 I_{\text{REF}} 1.6\text{k}\Omega) + 8.4\text{V}$$

IDLE OUTPUT CURRENT

In the selected output state (encode or decode), equivalent idle currents are present on the (+) and (-) output leads. The output will be symmetrical with the external resistor matching determining the overall system accuracy.



OUTPUT COMPLIANCE EXTENSION CONNECTIONS

STANDARD ENCODE/DECODE CONNECTIONS

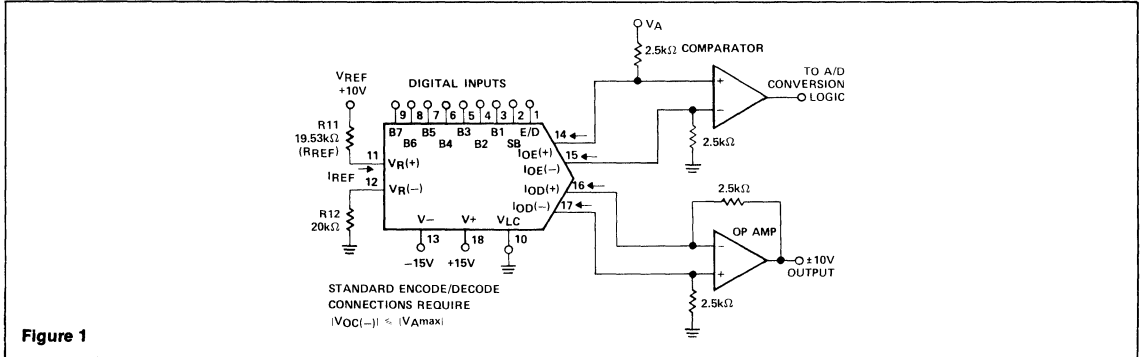


Figure 1

EXTENDED RANGE CONNECTIONS

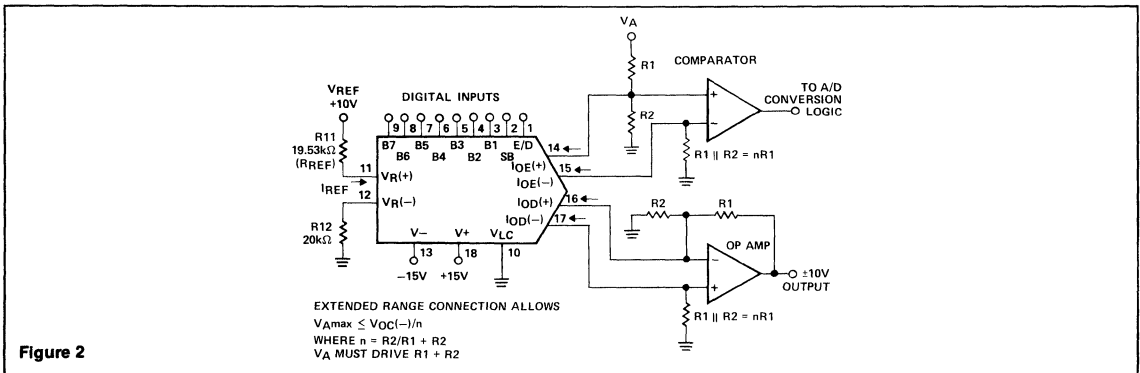


Figure 2

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN-BIT EXCLUDED)

IDEAL DECODE OUTPUT

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
1	0001	1.5	17.5	35	70	140	280	560	1120
2	0010	2.5	18.5	37	74	148	286	592	1184
3	0011	3.5	19.5	39	78	156	312	624	1248
4	0100	4.5	20.5	41	82	164	328	656	1312
5	0101	5.5	21.5	43	86	172	344	688	1376
6	0110	6.5	22.5	45	90	180	360	720	1440
7	0111	7.5	23.5	47	94	188	376	752	1504
8	1000	8.5	24.5	49	98	196	392	784	1568
9	1001	9.5	25.5	51	102	204	408	816	1632
10	1010	10.5	26.5	53	106	212	424	848	1696
11	1011	11.5	27.5	55	100	220	440	880	1760
12	1100	12.5	28.5	57	114	228	456	912	1824
13	1101	13.5	29.5	59	118	236	472	944	1888
14	1110	14.5	30.5	61	122	244	488	976	1952
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64



DAC-100

10-BIT CURRENT-OUTPUT D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- **Fast Settling** 225nsec (8 Bits), 375nsec (10 Bits)
- **Stable** Tempcos to $\pm 15\text{ppm}/^\circ\text{C}$ Max
- **Commercial, Industrial and Military Models Available**
- **TTL Compatible Logic Inputs**
- **Wide Supply Range** $\pm 6\text{V}$ to $\pm 18\text{V}$

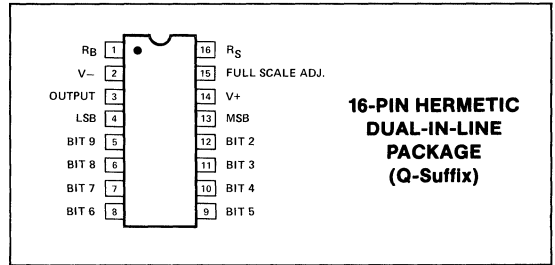
GENERAL DESCRIPTION

The DAC-100 is a complete 10-bit resolution digital-to-analog converter constructed on two monolithic chips in a single 16-pin DIP. Featuring excellent linearity vs. temperature performance, the DAC-100 includes a low tempco voltage reference, ten current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output, matched bipolar offset and feedback resistors. Resistors are included for use with an external op amp for voltage output applications.

Although all units have 10-bit resolution, a wide choice of linearity and temperature coefficient options are provided to allow price/performance optimization.

The small size, wide operating temperature range, and high reliability construction make the DAC-100 ideal for aerospace applications. Other applications include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power supplies, analog meter movement drivers, waveform generators and high speed analog-to-digital converters.

PIN CONNECTIONS



ORDERING INFORMATION†

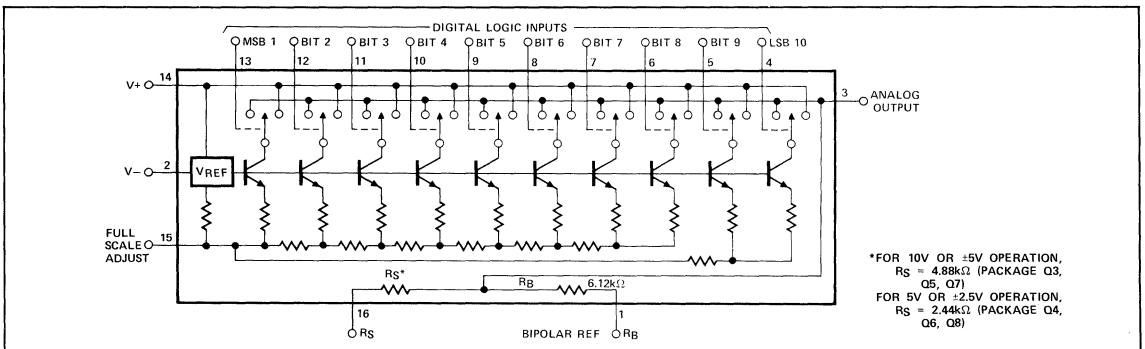
N.L.* %FS MAX	TEMPCO* ppm/°C MAX	MILITARY TEMPERATURE		INDUSTRIAL TEMPERATURE		COMMERCIAL TEMPERATURE	
		$V_O = \pm 5\text{V}/10\text{V}$	$V_O = \pm 2.5\text{V}/5\text{V}$	$V_O = \pm 5\text{V}/10\text{V}$	$V_O = \pm 2.5\text{V}/5\text{V}$	$V_O = \pm 5\text{V}/10\text{V}$	$V_O = \pm 2.5\text{V}/5\text{V}$
± 0.05	± 15	—	—	DAC100AAQ7	DAC100AAQ8	—	—
± 0.05	± 30	—	—	DAC100ABQ7	DAC100ABQ8	—	—
± 0.05	± 60	DAC100ACQ5/883	DAC100ACQ6/883	DAC100ACQ7	DAC100ACQ8	DAC100ACQ3	DAC100ACQ4
± 0.10	± 30	DAC100BBQ5/883	DAC100BBQ6/883	DAC100BBQ7	DAC100BBQ8	—	—
± 0.10	± 60	DAC100BCQ5/883	DAC100BCQ6/883	DAC100BCQ7	DAC100BCQ8	DAC100BCQ3	DAC100BCQ4
± 0.10	± 120	—	—	—	—	—	—
± 0.20	± 60	DAC100CCQ5/883	DAC100CCQ6/883	DAC100CCQ7	DAC100CCQ8	DAC100CCQ3	DAC100CCQ4
± 0.20	± 120	—	—	—	—	—	—
± 0.30	± 120	—	—	DAC100DDQ7	DAC100DDQ8	DAC100DDQ3	DAC100DDQ4

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

*Part number construction: The 1st letter following DAC-100 (A-D) refers to

the nonlinearity specification; the 2nd letter (A-D) refers to the full-scale tempco; the letter Q refers to the package; and the end numeral indicates the output voltage and temperature.

SIMPLIFIED SCHEMATIC



*FOR 10V OR $\pm 5\text{V}$ OPERATION,
 $R_S = 4.88\text{k}\Omega$ (PACKAGE Q3,
 Q5, Q7)
 FOR 5V OR $\pm 2.5\text{V}$ OPERATION,
 $R_S = 2.44\text{k}\Omega$ (PACKAGE Q4,
 Q6, Q8)

**ABSOLUTE MAXIMUM RATINGS** (Note 2)

V+ Supply to V- Supply	0 to +36V
V+ Supply to Output	0 to +18V
V- Supply to Output	0 to -18V
Logic Inputs to Output	-1V to +6V
Power Dissipation (Note 1)	500mW
Operating Temperature Range Q3, Q4	0°C to +70°C
Q5, Q6, Q7, Q8	-55°C to +125°C

DICE Junction Temperature	-25°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

NOTES:

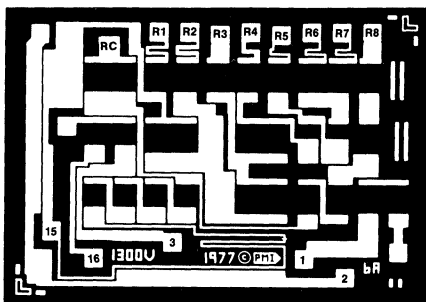
- Rating applies to ambient temperature of 100°C. Above 100°C, derate at 10mW/°C.
- Ratings apply to DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for Q7 and Q8 devices; $0^\circ C \leq T_A \leq +70^\circ C$ for Q3 and Q4; $-55^\circ C \leq T_A \leq +125^\circ C$ for Q5 and Q6 devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-100	MIN	TYP	MAX	UNITS
Resolution				10	—	—	Bits
Nonlinearity (For nonlinearity/tempco combinations, see Ordering Information)	NL	($\pm 1/2$ LSB - 10 bits)	A—	—	—	± 0.05	%FS
		($\pm 1/2$ LSB - 9 bits)	B—	—	—	± 0.1	
		($\pm 1/2$ LSB - 8 bits)	C—	—	—	± 0.2	
		($\pm 3/4$ LSB - 8 bits)	D—	—	—	± 0.3	
Full-Scale Tempco (See Full-Scale Test Circuit)	T _C		-A	—	—	± 15	ppm/°C
			-B	—	—	± 30	
			-C	—	—	± 60	
			-D	—	—	± 120	
Setting Time T _A = 25°C	t _S	to $\pm 0.05\%$ FS	ALL	—	—	375	ns
		to $\pm 0.1\%$ FS	ALL	—	—	300	
		to $\pm 0.2\%$ FS	ALL	—	—	225	
		to $\pm 0.4\%$ FS	ALL	—	—	150	
		to $\pm 0.8\%$ FS	ALL	—	—	100	
Full-Range Output Voltage (Limits guarantee adjustability to exact 10.0 (5.0)V with a 200Ω Trimpot® between Adjust and V-)	V _{FR}	Connect FS Adjust to V- 10V Models (Q3, Q5, Q7) (See Full-Scale Test Circuit) 5V Models (Q4, Q6, Q8) V _{IN} = 0.7V (See Basic Unipolar Voltage Output Circuit)		10	—	11.1	V
				5	—	5.55	
Zero-Scale Output Voltage	V _{ZS}	V _{IN} = 2.1V	ALL	—	—	0.013	%FS
Logic Inputs: High	V _{INH}	Measured with respect to output pin	ALL	2.1	—	—	V
Logic Inputs: Low	V _{INL}	Measured with respect to output pin	ALL	—	—	0.7	V
Logic Input Current, Each Input	I _{IN}	V _{IN} = 0 to +6V	ALL	—	—	5	μA
Logic Input Resistance	R _{IN}	V _{IN} = 0 to +6V	ALL	—	3	—	mΩ
Logic Input Capacitance	C _{IN}		ALL	—	2	—	pF
Output Resistance	R _O		ALL	—	500	—	kΩ
Output Capacitance	C _O		ALL	—	13	—	pF
Applied Power Supplies: V+			ALL	+6	—	+18	V
Applied Power Supplies: V-			ALL	-6	—	-18	V
Power Supply Sensitivity	P _{SS}	V _S = $\pm 6V$ to $\pm 18V$	ALL	—	—	± 0.10	% per Volt
Power Consumption	P _D	V _S = $\pm 15V$	Q3, Q4	—	200	300	mW
		V _S = $\pm 6V$	Q3, Q4	—	80	—	
		V _S = $\pm 15V$	Q5, Q6, Q7, Q8	—	200	250	
Positive Supply Current	I+	V _S = +15V	Q3, Q4	—	—	10	mA
		V _S = +15V	Q5, Q6, Q7, Q8	—	—	8.33	
Negative Supply Current	I-	V _S = -15V	Q3, Q4	—	—	-10	mA
		V _S = -15V	Q5, Q6, Q7, Q8	—	—	-8.33	

DICE CHARACTERISTICS

DAR-01



DIE SIZE 0.089 × 0.063 inch, 5607 sq. mils
(2.26 × 1.6 mm, 3.616 sq. mm)

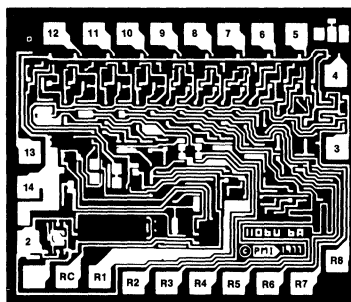
- 1. R_B
- 2. V^-
- 3. OUTPUT
- 15. FULL-SCALE ADJ
- 16. R_S

R — Pads are connected to similarly marked pads on DAI-01

Note: Pads 4 — 14, See DAI-01

These die versions are available on special order; contact your PMI sales office.

DAI-01



DIE SIZE 0.080 × 0.067 inch, 5360 sq. mils
(2.032 × 1.70 mm, 3.45 sq. mm)

- 2. V^-
- 3. OUTPUT
- 4. BIT 10 (LSB)
- 5. BIT 9
- 6. BIT 8
- 7. BIT 7
- 8. BIT 6
- 9. BIT 5
- 10. BIT 4
- 11. BIT 3
- 12. BIT 2
- 13. BIT 1 (MSB)
- 14. V^+

R — Pads are connected to similarly marked pads on DAR-01

Note: Pads 1, 2, 15, 16, See DAR-01

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$ for the R-2R Ladder Network comprised of R1—R8, R12, R23, R34, R45 and R56 when connected to an ideal DAI-01, unless otherwise noted.

PARAMETER	CONDITIONS	DAR-01-N			DAR-01-G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Nonlinearity	$VR1 = 3.2V$	—	—	± 0.035	—	—	± 0.05	%

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$, $VR1 = 3.2V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAR-01			UNITS
		MIN	TYP	MAX	
Resistance R1	Absolute Measurement	2.56	—	3.84	k Ω
Ratio RC1 to R1	Ideal = 1.00503 to 1	-1	—	+1	%
Ratio R1 to RS1	Ideal = 1.29959 to 1	-1	—	+1	%
Ratio R1 to RS2	Ideal = 1.29959 to 1	-1	—	+1	%
Ratio RB to R1	Ideal = 1.92211 to 1	-1	—	+1	%

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** in common to all grades.

PARAMETER	CONDITIONS	DAR-01			UNITS
		MIN	TYP	MAX	
Absolute Temperature Coefficient	All Resistors	—	±180	—	ppm/°C
Tracking Temperature Coefficient	All Resistors with Respect to R1	—	3	—	ppm/°C

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$ when connected to an ideal DAR-01, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAI-01-N			DAI-01-G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Nonlinearity	NL	$V_S = \pm 15\text{V}$	—	—	±0.05	—	—	±0.1	%
Internal Reference Voltage	V_{MCR}	$V_S = \pm 15\text{V}$	6.6	—	6.900	6.6	—	6.900	V

WAFER TEST LIMITS at $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ when connected to an ideal DAR-01, unless otherwise noted.

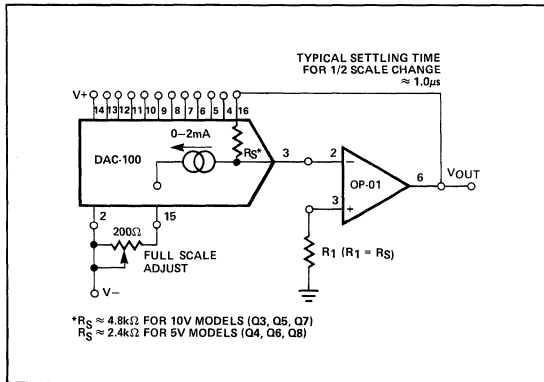
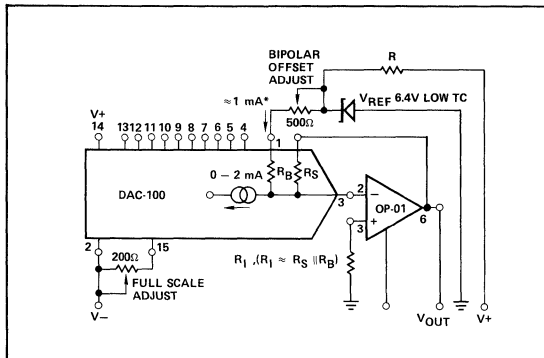
PARAMETER	CONDITIONS	DAI-01			UNITS
		MIN	TYP	MAX	
Resolution		10	—	10	Bits
Analog Output Current	All Bits Low, V_- Connected to FS Adjust	1840	—	2274	μA
Zero-Scale Output Current	All Bits High, V_- Connected to FS Adjust	—	—	±0.011	% I_{FS}
Logic Input "0"	Measured with Respect to Output	—	—	0.7	V
Logic Input "1"	Measured with Respect to Output	2.1	—	—	V
Supply Current	All Bits High, V_- Connected to FS Adjust	—	—	8.33	mA
Power Supply Rejection	$V_S = \pm 6\text{V}$ to $\pm 18\text{V}$	—	—	0.1	% I_{FS}/V

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, and when connected to an ideal DAR-01, unless otherwise noted.

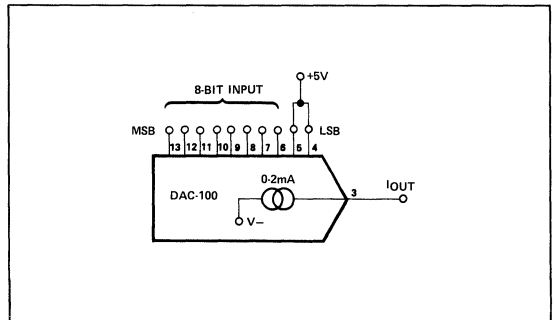
PARAMETER	CONDITIONS	DAI-01-N			DAI-01-G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Full-Scale Temperature Coefficient (Note)		—	±60	—	—	±60	—	ppm/°C

NOTE:
Full-Scale Temperature Coefficient is defined as the change in output voltage measured in the basic unipolar voltage output test circuit shown on the DAC-100 data sheet and is expressed in ppm between 25°C and either temperature extreme divided by the corresponding temperature change.

BASIC CONNECTIONS
BASIC UNIPOLAR VOLTAGE OUTPUT CIRCUIT

BASIC BIPOLAR VOLTAGE OUTPUT CIRCUIT

APPLICATIONS INFORMATION

FULL RANGE OUTPUT ADJUSTMENT — The output current of the DAC-100 may be reduced to produce an exact 10.000 (5.000) volt output by connecting a 200Ω adjustable resistance between the full-scale adjust pin and V-. Adjustment should be made with an input of all "zeroes."

LOWER RESOLUTION APPLICATIONS — The DAC-100 may be used in applications requiring less than 10 bits of resolution. All unused logic inputs **must** be tied to logic high for proper operation. "Floating" logic inputs can cause improper operation.

REDUCED RESOLUTION APPLICATION


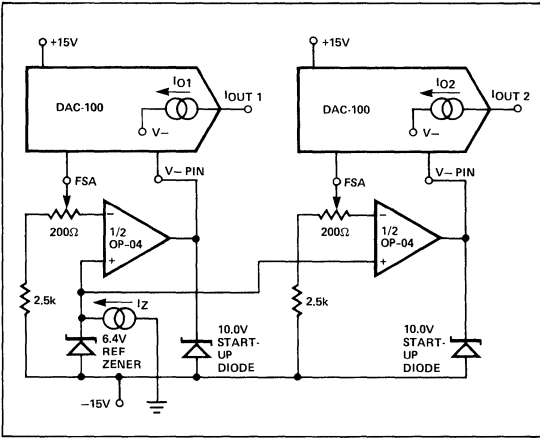
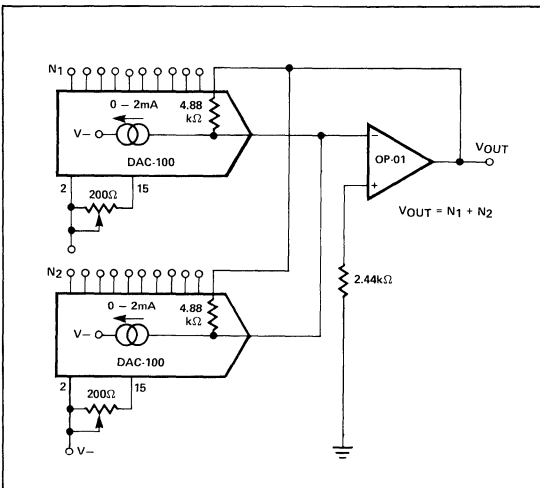
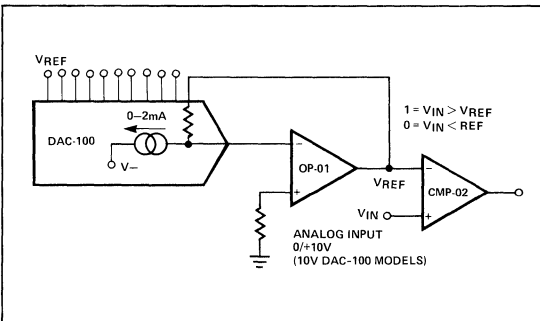
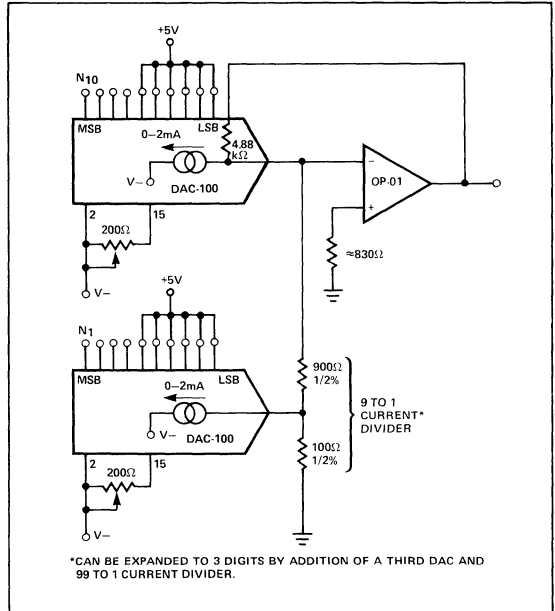
LOGIC CODING — The DAC-100 uses complementary or inverted binary logic coding, i.e., an all "zeroes" input produces a full range output, while an all "ones" input produces a zero-scale output. Each lesser significant bit's weight is one-half the previous more significant bit's value. High logic input turns the bit "OFF," low logic input level turns the bit "ON".

LOGIC COMPATIBILITY — The input logic levels are directly compatible with TTL logic and may also be used with CMOS logic powered from a single +5 volt supply.

NONLINEARITY (NL) — The maximum deviation from an ideal straight line drawn between the end points, expressed as a percent of full-scale range (FSR) or given in terms of LSB value. The end points are zero-scale output for unipolar operation and minus full-scale to positive full-scale for bipolar operation.

BIPOLAR OPERATION — The DAC-100 may be converted to bipolar operation by injecting a half-scale current into the output; this is accomplished by connecting the internal bipolar resistor to a +6.4 volt reference. Trimming of the zero output may be facilitated by placing a 500Ω adjustable resistance in series with the +6.4 volts.

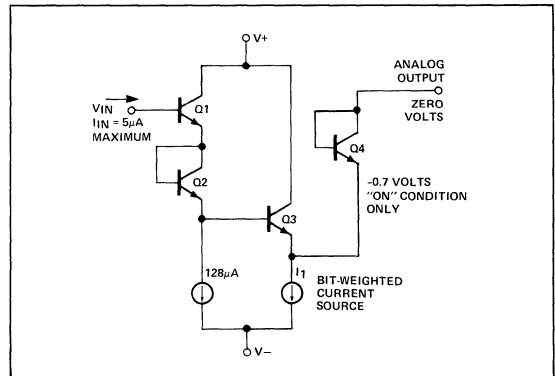
VOLTAGE AT OUTPUT PIN — The DAC-100 is designed to be operated with the voltage at the output pin held very close to zero volts. Input logic threshold levels are directly affected by output pin voltage changes; voltage swings at the output may cause loss of linearity due to improper switching of bits. Large voltage swings may cause permanent damage and should be avoided. Proper operation can be obtained with output voltages held within ±0.7 volts; a pair of back-to-back silicon diodes tied from the output to ground is a convenient way of clamping the output to this limit.

TYPICAL APPLICATIONS
EXTERNAL REFERENCE CONNECTION

ANALOG SUM OF TWO DIGITAL NUMBERS

DIGITALLY PROGRAMMED LEVEL DETECTOR

BINARY-CODED-DECIMAL D/A CONVERSION

INTERFACING WITH CMOS LOGIC

The DAC-100 requires only about $1\mu\text{A}$ of input current into each logic stage. This enables use with CMOS inputs as long as one rule is observed; logic input voltages should not exceed 6.5 volts or $V+$, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown below. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply ($V+$) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

DAC-100 — LOGIC INPUT STAGE


Switching is accomplished by forward biasing Q4, diode-connected transistor, for the bit "ON" condition and back biasing Q4 in the "OFF" condition. For the "ON" condition ($V_{IN} \leq 0.7$ volts), Q3 is "OFF" — all of the bit-weighted current, I_1 , flows from the analog output through Q4 and ultimately to V^- . In the "OFF" condition ($V_{IN} \geq 2.1$ volts), Q3 is "ON", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

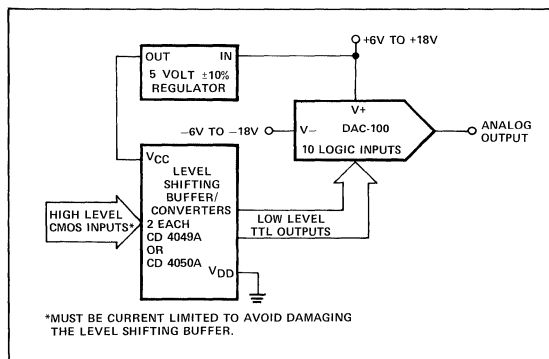
$$1) BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7 \text{ volts}$$

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limit is observed, DAC-100 operation with CMOS input is easily achieved.

±6 VOLT POWER SUPPLY OPERATION

This is the most convenient method of interfacing the DAC-100 with CMOS logic. At ±6 volts the DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

BLOCK DIAGRAM — CMOS TO DAC-100 INTERFACE



HIGH LEVEL CMOS INTERFACING

The block diagram below illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with the DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts — clearly satisfying the input stage voltage rule.

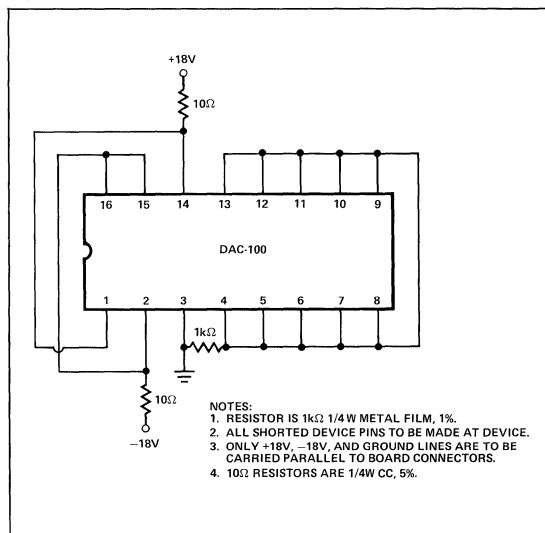
In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or non-inverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100 to CMOS interfacing method to be used in either type of application.

Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive three-terminal IC regulator can supply several level shifting devices.

NOTE:

For a more complete explanation and detailed circuit connections, refer to AN-14, "Interfacing PMI D/A's with CMOS Logic."

BURN-IN CIRCUIT





DAC-208

9-BIT VOLTAGE-OUTPUT D/A CONVERTER (8 BITS PLUS SIGN)

Precision Monolithics Inc.

FEATURES

- Complete Reference and Op Amp included
- Sign-Magnitude Coding
- Unipolar/Bipolar Selectable +5V or $\pm 10V$
- 8-Bit Linearity Maintained over Full Temp Range
- Fast 750ns Settling Time
- Multiplying Operation
- Guaranteed Monotonicity
- MIL-STD-883 Class B Processing Available

ORDERING INFORMATION†

NL %FS	18-PIN HERMETIC DUAL-IN-LINE	
	MILITARY TEMP	COMMERCIAL TEMP
0.1	DAC208AX*	DAC208EX
0.2	DAC208BX*	DAC208FX

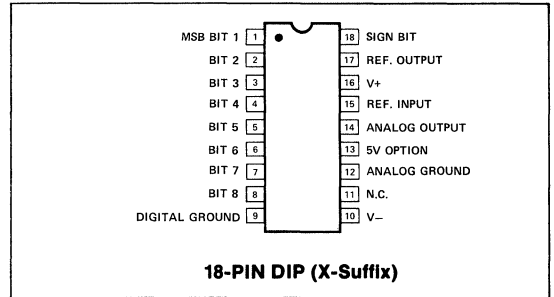
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

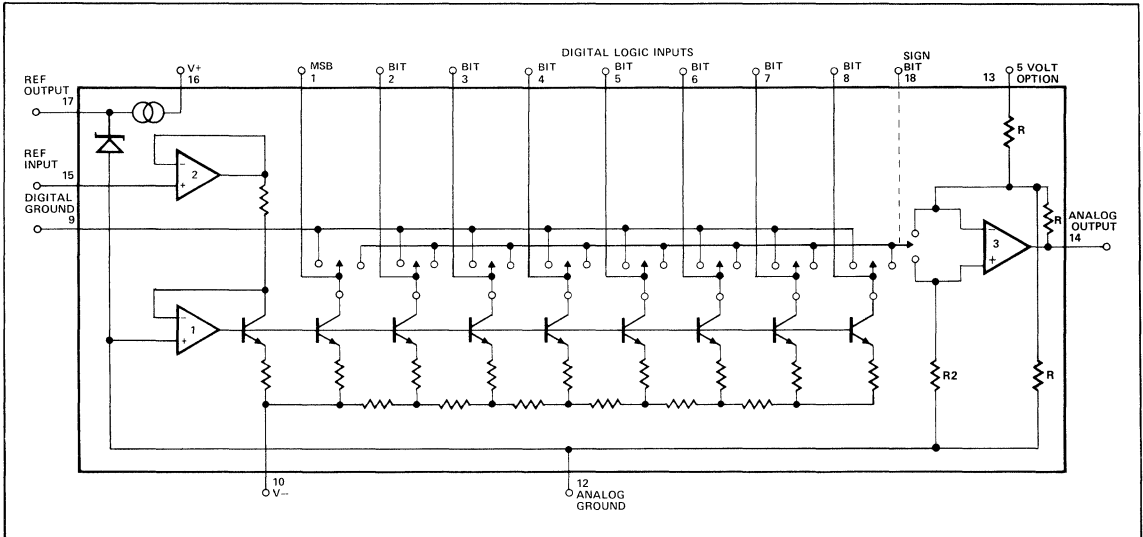
GENERAL DESCRIPTION

The DAC-208 is a complete, voltage output, 8-bit plus sign D/A converter. A precision voltage reference, logic controlled polarity switch, and high-speed (750 ns settling time) output op amp are included. Nonlinearity, monotonicity, and full-scale temperature coefficient are guaranteed over the full operating range. Enhanced reliability is achieved with monolithic construction and hermetic DIP packaging. Two low-cost 0°C/+70°C and two -55°C/+125°C grades are available in addition to MIL-STD-883 Class B processing. Monotonicity is guaranteed by design.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature Range	DAC-208A, B	-55°C to +125°C
	DAC-208E, F	0°C to +70°C
Storage Temperature Range		-65°C to +150°C
V+ Supply to Analog Ground		0 to +18V
V- Supply to Analog Ground		0 to -18V
Analog Ground to Digital Ground		0 to ±0.5V
V+ Supply to V- Supply		36V

Logic Inputs to Digital Ground	-5V to (V+ - 0.7V)
Internal Reference Output Current	300µA
Reference Input Voltage	0 to +10V
Internal Power Dissipation	500mW
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration	Indefinite

(Short circuit may be to ground or either supply.)

ELECTRICAL CHARACTERISTICS — MILITARY AND COMMERCIAL GRADES at $V_S = \pm 15V$, $T_A = -55^\circ C$ to $+125^\circ C$ for A and B grades, $T_A = 0^\circ C$ to $+70^\circ C$ for E and F grades, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-208A/E			DAC-208B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		Including Sign	9	9	9	9	9	9	Bits
Monotonicity			8	—	—	8	—	—	Bits
Nonlinearity	NL	$T_A = 25^\circ C$	—	—	±0.1	—	—	±0.2	%FS
		$T_A = 0^\circ C - 70^\circ C$ (E and F only)	—	—	±0.1	—	—	±0.2	
		$-55^\circ C \leq T_A \leq +125^\circ C$ (A + B Suffix Only)	—	—	±0.1	—	—	±0.2	
Zero-Scale Offset Voltage	V_{ZS}	$T_A = \text{Full Range}$	—	—	—	—	—	—	%FS
			—	—	±0.1	—	—	±0.15	
Bipolar Full Range Voltage Symmetry	V_{FRS}	$T_A = 25^\circ C$ ($V_{FR+} - V_{FR-}$)	—	—	60	—	—	70	mV
		$T_A = \text{Full Range}$	—	—	70	—	—	70	
Zero-Scale Voltage Symmetry	V_{ZSS}	($V_{ZS+} - V_{ZS-}$) $T_A = \text{Full Range}$	—	—	1	—	—	2	mV
Gain Tempco	T_C	Internal Reference	—	—	40	—	—	60	ppm/°C
		External Reference	—	15	—	—	30	—	
Output Voltage Range (Note 3)	V_{OR+} V_{OR-}	10V Option	+10.0	—	+11.5	+10.0	—	+11.5	V
		5V Option	+5.0	—	+5.75	+5.0	—	+5.75	
		10V Option	-11.5	—	-10.0	-11.5	—	-10.0	
Differential Nonlinearity	DNL	$T_A = 25^\circ C$	—	—	±1/2	—	—	1	LSB
Settling Time	t_S		—	750	—	—	750	—	ns
Reference Input Slew Rate	SR_{REF}		—	1.5	—	—	1.5	—	V/µs
Reference Input Impedance	Z_{IN}		—	200	—	—	200	—	MΩ
Reference Input Multiplying Range	IVR_m	For 0.1% Typical Nonlinearity (Note 1)	3	—	10	3	—	10	V
Reference Amplifier Bandwidth	BW		—	1	—	—	1	—	MHz
Reference Output Voltage	V_{REF}		—	7.6	—	—	7.6	—	V
DAC Output Current	I_O	(Note 2)	0	—	5	0	—	5	mA
Reference Output Current	I_{REF}		—	100	—	—	100	—	µA
Output Slew Rate	SR_O		—	10	—	—	10	—	V/µs
Logic Input Current	I_{IN}	$-5V \leq V_I \leq V+$	—	±2	±10	—	±2	±10	µA
Logic "0" Voltage	V_{INL}		—	—	0.8	—	—	0.8	V
Logic "1" Voltage	V_{INH}		2	—	—	2	—	—	V

NOTES:

1. These characteristics are for design guidance only and are not subject to test.

2. Guaranteed by V_{OR} test, $R_L = 2k\Omega$.
3. $R_L = 2k\Omega$.

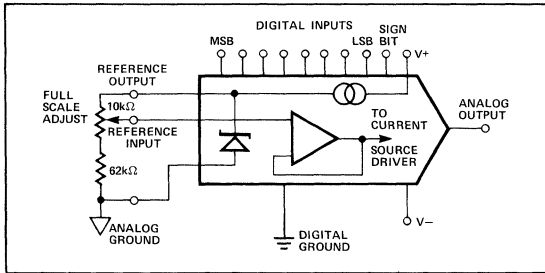


ELECTRICAL CHARACTERISTICS — MILITARY AND COMMERCIAL GRADES at $V_S = \pm 15V$, $T_A = -55^\circ C$ to $+125^\circ C$ for A and B grades, $T_A = 0^\circ C$ to $+70^\circ C$ for E and F grades, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-208A/E			DAC-208B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Sensitivity	P_{SS}	$T_A = \text{Full Range}$	—	0.03	0.15	—	0.03	0.15	$\% V_{FS}/V$
Positive Supply Current	I_+		—	7	9	—	7	9	mA
Negative Supply Current	I_-		—	10	12	—	10	12	mA

CONNECTION INFORMATION

FULL-SCALE ADJUSTMENT CIRCUIT



Full-Scale output voltage is trimmed using the circuit configuration shown above. Low tempcco metal-film resistors are recommended. External components should be mounted near the package to ensure good temperature tracking.

REFERENCE INPUT BYPASS

Low noise and fast settling operation can be obtained by bypassing the Reference Input to Analog Ground with a $0.01\mu F$ monolithic capacitor.

GROUNDING

Separate digital and analog grounds have been provided for optimum noise rejection. Best results will be obtained when analog and digital ground are connected together at one point only. This configuration ensures negligible digital currents flowing in analog ground.

APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATIONS

For applications requiring less than 8-Bit resolution, connect unused logic inputs to ground.

UNIPOLAR OPERATION

Operation as an 8-Bit binary converter may be implemented by connecting the Sign-Bit to +5V for positive Full-Scale output, and 0V for negative Full-Scale.

+5 VOLT OPTION

The output voltage range can be modified by connecting the 5V option pin (pin 13) to the analog output (pin 14). The 5V

option is for unipolar operation only. In this configuration the Sign-Bit should be held at logic high (+5V).

POWER SUPPLIES

The DAC-208 will operate within specification for power supplies ranging from $\pm 12V$ to $\pm 18V$ for unipolar positive operation; and from $\pm 13V$ to $\pm 18V$ for bipolar. Power supplies should be bypassed near the package with $0.1\mu F$ monolithic capacitors.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to $100pF$.

REFERENCE OUTPUT

Reference output current, I_{ref} , should not exceed $100\mu A$.

INTERFACING WITH CMOS LOGIC

The DAC-208 logic input stage requires approximately $1\mu A$, I_{in} , and is capable of operation with inputs between $-5V$ and $(V+ - 0.7 \text{ Volts})$. The wide input voltage range allows direct CMOS interface with no additional components required.

EXTERNAL REFERENCES

Positive external reference voltages may be applied to the reference input terminal to improve Full-Scale temperature coefficient. External references are used when cascading several converters or when tracking is required between system elements.

MULTIPLYING OPERATION

Two-quadrant multiplying operation is achieved by applying an analog input (0 to +10V) to the Reference input terminal. The DAC output is the scaled product of the input voltage and the digital code.

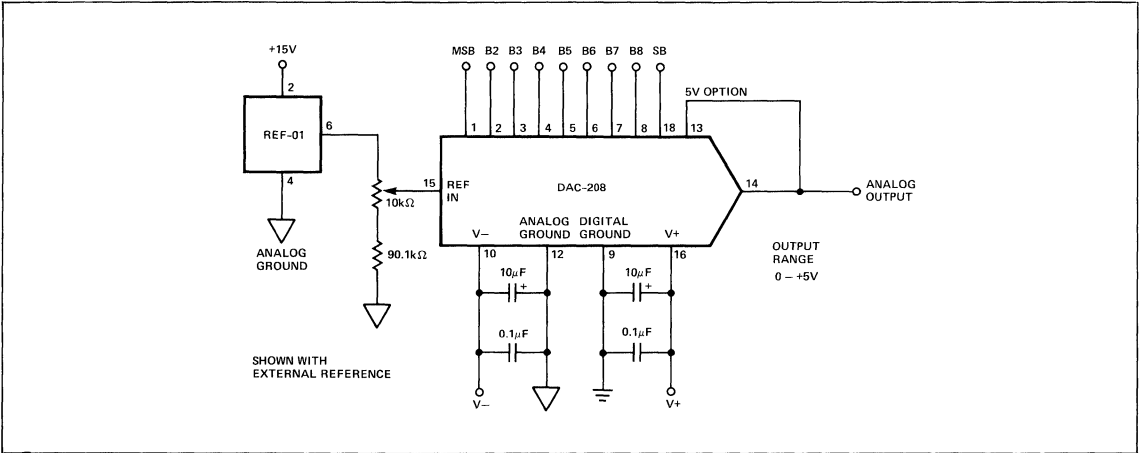
SIGN — MAGNITUDE CODING TABLE

	SIGN BIT	MSB	LSB					
+FULL-SCALE -1 LSB	1	1	1	1	1	1	1	1
+HALF-SCALE	1	1	0	0	0	0	0	0
ZERO-SCALE (+)	1	0	0	0	0	0	0	0
ZERO-SCALE (-)	0	0	0	0	0	0	0	0
-HALF-SCALE	0	1	0	0	0	0	0	0
-FULL-SCALE +1 LSB	0	1	1	1	1	1	1	1



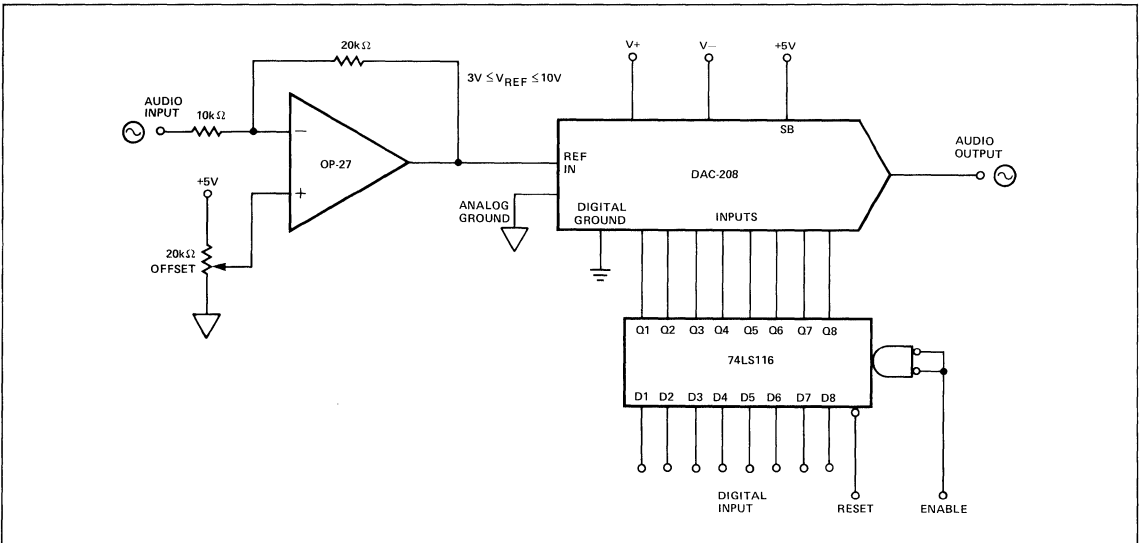
UNIPOLAR OPERATION

5V OPTION



APPLICATIONS

AUDIO ATTENUATOR



Precision Monolithics Inc.

FEATURES

- **Complete** Includes Reference and Op Amp
- **Bipolar Output** $\pm 10V$
- **Sign-Magnitude Coding**
- **No Bipolar Offset Adjustment Required**
- **10-Bit Linearity Maintained over Full Temperature**
- **Multiplying Operation**
- **Fast** 1.5 μs Settling Time
- **Monotonicity Guaranteed**
- **Reliable** 100% Burned-in
- **Models with MIL-STD-883 Class B Processing Available**

ORDERING INFORMATION†

TEMPCO (ppm/°C)	18-PIN HERMETIC DUAL IN-LINE PACKAGE		
	NL %FS	MILITARY	COMMERCIAL
± 40	± 0.05	DAC210AX*	DAC210EX
± 60	± 0.05	DAC210BX*	DAC210FX
± 30 Typ	± 0.10		DAC210GX

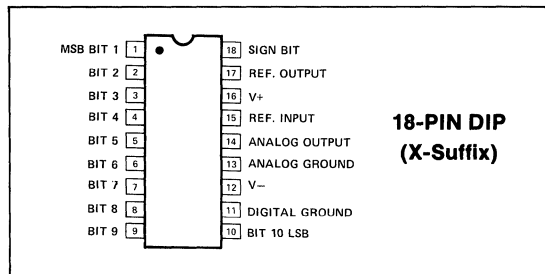
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

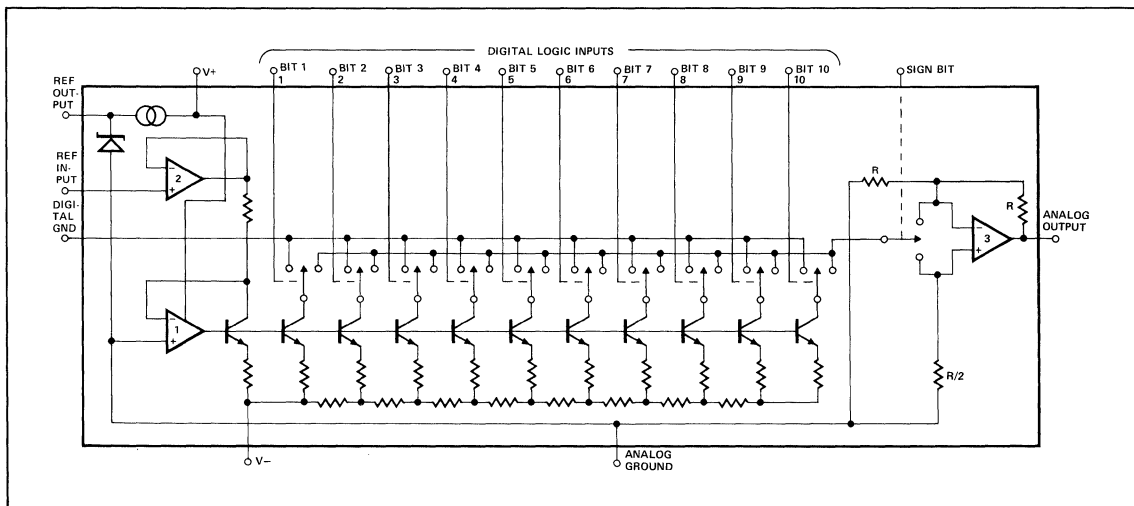
GENERAL DESCRIPTION

The DAC-210 is a complete, monolithic 10-bit plus sign DAC with a $\pm 10V$ output. A precision voltage reference, a logic controlled polarity switch and output amplifier are included. Linearity, monotonicity, and full-scale temperature coefficient are guaranteed over the full operating temperature range. Ease of application is achieved by the **total** D/A system specs given for nonlinearity and zero-scale offset. System specs eliminate the complex error budget analysis required by less "complete" DACs. Sign-magnitude coding minimizes the "major-carry" zero-code errors inherent in offset coding schemes. Reliability is enhanced by a monolithic design, 100% burn-in, and a hermetic DIP package. MIL-STD-883 Class B processing is available on $-55^{\circ}C$ to $+125^{\circ}C$ grades.

PIN CONNECTION



SIMPLIFIED SCHEMATIC





ELECTRICAL CHARACTERISTICS — MILITARY AND COMMERCIAL GRADES at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, for A and B grades. $0^\circ C \leq T_A \leq +70^\circ C$ for E, F and G grades, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-210A/E			DAC-210B/F			DAC-210G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		Including Sign	11	—	—	11	—	—	11	—	—	Bits
Monotonicity			10	—	—	10	—	—	9	—	—	Bits
Nonlinearity	NL	$T_A = 25^\circ C$	—	—	± 0.05	—	—	± 0.05	—	—	± 0.10	%FS
		$T_A = \text{Full Range}$	—	—	± 0.05	—	—	± 0.10	—	—	—	
		$T_A = \text{Full Range (A only)}$	—	—	± 0.075	—	—	—	—	—	—	
Zero-Scale Offset Voltage	V_{ZS}	$T_A = 25^\circ C$	—	—	± 0.05	—	—	± 0.1	—	—	—	%FS
		$T_A = \text{Full Range}$	—	—	± 0.06	—	—	± 0.1	—	—	—	
Bipolar Full Range Voltage Symmetry ($V_{FR+} - V_{FR-} $)	V_{FRS}	$T_A = 25^\circ C$	—	—	40	—	—	60	—	—	80	mV
		$T_A = \text{Full Range}$	—	—	50	—	—	70	—	50	—	
Zero-Scale Voltage Symmetry ($V_{ZS+} - V_{ZS-}$)	V_{ZSS}	$T_A = \text{Full Range}$	—	—	1	—	—	1	—	—	2	mV
Gain Tempco	T_C	Internal Reference	—	—	± 40	—	—	± 60	—	± 30	—	ppm/ $^\circ C$
		External Reference	—	± 15	—	—	± 30	—	—	± 30	—	
Output Voltage Range	V_{OR+} V_{OR-}	$R_L = 2k\Omega$	+10.0	—	+11.5	+10.0	—	+11.5	+10.0	—	+11.5	V
			-11.5	—	-10.0	-11.5	—	-10.0	-11.5	—	-10.0	
Differential Nonlinearity	DNL	$T_A = 25^\circ C$	—	—	± 1	—	—	± 1	—	± 1	—	LSB
Settling Time	T_S	(Note 4)	—	1.5	—	—	1.5	—	—	1.5	—	μs
Reference Input Slew Rate	SR_{REF}		—	1.5	—	—	1.5	—	—	1.5	—	V/ μs
Reference Input Impedance	Z_{IN}		—	200	—	—	200	—	—	200	—	M Ω
Reference Input Multiplying Range	IVR_m	For 0.1% Typical Nonlinearity (Note 1)	3	—	10	3	—	10	3	—	10	V
Reference Amplifier Bandwidth	BW		—	1	—	—	1	—	—	1	—	MHz
Reference Output Voltage	V_{REF}		—	7.6	—	—	7.6	—	—	7.6	—	V
DAC Output Current	I_O	(Note 3)	0	—	5	0	—	5	0	—	5	mA
Reference Output Current	I_{REF}		—	100	—	—	100	—	—	100	—	μA
Output Slew Rate	SR_O		—	10	—	—	10	—	—	10	—	V/ μs
Logic Input Current	I_{IN}	$-5V \leq V_I \leq V+$	—	± 2	± 10	—	± 2	± 10	—	± 2	± 10	μA
Logic "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	—	—	0.8	V
Logic "1" Input Voltage	V_{INH}		2.0	—	—	2.0	—	—	2.0	—	—	V
Power Supply Sensitivity (Note 2)	P_{SS}	$T_A = 25^\circ C$	—	0.015	0.05	—	0.015	0.05	—	0.015	0.1	% V_{FS}/V
		$T_A = \text{Full Range}$	—	0.015	0.1	—	0.015	0.1	—	0.015	0.1	
Positive Supply Current	$I+$		—	7	9	—	7	9	—	7	9	mA
Negative Supply Current	$I-$		—	-10	-12	—	-10	-12	—	-10	-12	mA

NOTES:

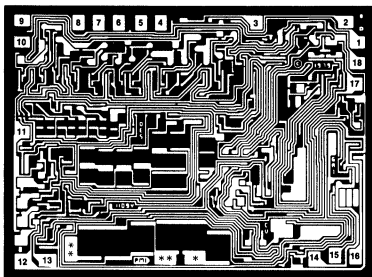
- Guaranteed by design.
- Power Supplies — The DAC-210 will operate within specifications for power supplies ranging from $\pm 12V$ to $\pm 18V$. Power supplies should be bypassed near the package with a $0.1\mu F$ disk capacitor.
- Guaranteed by V_{OR} test, $R_L = 2k\Omega$.
- To within $\pm 5mV$ of final settled value, (± 10 volt output step, $R_L = 2k\Omega$.)

**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature Range	
DAC-210A, B	-55°C to +125°C
DAC-210E, F, G	0°C to +70°C
DICE Junction Temperature (T_j)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
V+ Supply to Analog Ground	0 to +18V
Analog Ground to Digital Ground	0 to $\pm 0.5V$
Logic Inputs to Digital Ground	-5V to (V+ - 0.7V)

V+ Supply to V- Supply	36V
Internal Reference Output Current	300 μ A
Reference Input Voltage	0 to +10V
Internal Power Dissipation	500mW
Derate Above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration	Indefinite
(Short-circuit may be to ground or either supply.)	

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

DICE CHARACTERISTICS

- | | |
|-------------|----------------------|
| 1. B1 (MSB) | 10. B10 (LSB) |
| 2. B2 | 11. DIGITAL GROUND |
| 3. B3 | 12. V- |
| 4. B4 | 13. ANALOG GROUND |
| 5. B5 | 14. ANALOG OUTPUT |
| 6. B6 | 15. REFERENCE INPUT |
| 7. B7 | 16. V+ |
| 8. B8 | 17. REFERENCE OUTPUT |
| 9. B9 | 18. SIGN BIT |

NOTE: For 5 volt output option (+5V only) * is connected to analog output. ** is connected to analog ground.

DIE SIZE 0.117 × 0.086 inch, 10,062 sq. mils
(2.972 × 2.18 mm, 5.942 sq. mm)

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, +10V full-scale output, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC-210N LIMIT	DAC-210G LIMIT	DAC-210GR LIMIT	UNITS
Resolution	Bipolar Output	11	11	11	Bits MAX
	Unipolar Output	10	10	10	
Monotonicity		10	9	8	Bits MIN
Nonlinearity		± 0.05	± 0.1	± 0.2	%FS MAX
Zero-Scale Offset	Sign-Bit High, All Other Inputs Low	± 5	± 10	± 10	mV MAX
Zero-Scale Symmetry	$V_{ZS+} - V_{ZS-}$	± 1	± 2	± 2	mV MAX
Full-Scale Bipolar Symmetry	$\pm 10V$ Full-Scale	± 40	± 80	± 80	mV MAX
Power Supply Rejection	$V_S = \pm 12V$ to $\pm 18V$	0.05	0.05	0.1	% V_{FS}/V MAX
Power Consumption	$I_{OUT} = 0$	300	300	300	mW MAX
Logic Input "0"		0.8	0.8	0.8	V MAX
Logic Input "1"		2	2	2	V MIN
Analog Output Voltage (All Bits High)	V+ (Sign-Bit High)	11.5	11.5	11.5	V MAX
		10	10	10	V MIN
	V- (Sign-Bit Low)	-10	-10	-10	V MAX
		-11.5	-11.5	-11.5	V MIN
Differential Nonlinearity		± 1	± 1	± 1	LSB MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

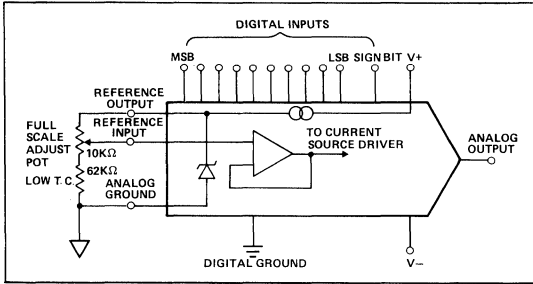
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and +10V full-scale output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-210N TYPICAL	DAC-210G TYPICAL	DAC-210GR TYPICAL	UNITS
Full-Scale Tempco	TCV_{FS}	Internal Reference	15	30	30	ppm/°C
Settling Time ($T_A = 25^\circ C$)	t_s	To $\pm 1/2$ LSB 10 Volt Step	1.5	1.5	1.5	μ s
Logic Input Current	I_{IN}	$T_A = 25^\circ C$	1	1	1	μ A

CONNECTION INFORMATION

FULL-SCALE ADJUSTMENT — Full-scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of $\geq 75k\Omega$ may be used.

FULL SCALE ADJUSTMENT CIRCUIT



REFERENCE INPUT BYPASS — Lowest noise and fastest settling operation will be obtained by bypassing the reference input to analog ground with a $0.01\mu\text{F}$ disk capacitor.

VARIABLE REFERENCES — Operation as a two-quadrant multiplying DAC is achieved by applying an analog input varying between 0 and +10V to the reference input terminal. The DAC output is then the scaled product of this voltage and the digital input.

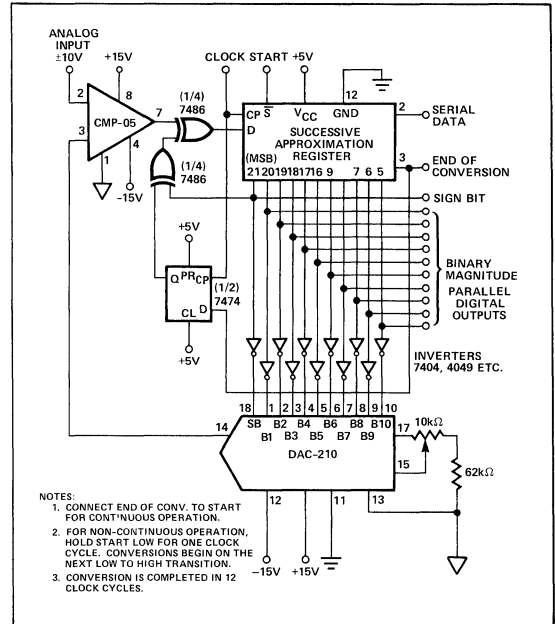
GROUNDING — For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the power supply, so that the large digital currents do not flow through the analog ground path.

SIGN — MAGNITUDE CODING TABLE

	SIGN-BIT	MSB	LSB
+ FULL-SCALE -1 LSB	1	1 1 1 1 1 1 1 1 1 1	1
+ HALF-SCALE	1	1 0 0 0 0 0 0 0 0 0	0
ZERO-SCALE (+)	1	0 0 0 0 0 0 0 0 0 0	0
ZERO-SCALE (-)	0	0 0 0 0 0 0 0 0 0 0	0
- HALF-SCALE	0	1 0 0 0 0 0 0 0 0 0	0
- FULL-SCALE +1 LSB	0	1 1 1 1 1 1 1 1 1 1	1

TYPICAL APPLICATIONS

10-BIT SIGN-MAGNITUDE ADC



APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATION — For applications not requiring full 10-bit resolution, unused logic inputs should be tied to ground.

CAPACITIVE LOADING — The output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE OUTPUT — For best results, reference output current should not exceed 100 μA .

INTERFACING WITH CMOS LOGIC — The DAC-210's logic input stages require about 1 μA and are capable of operation with inputs between -5 volts and V+. This wide input voltage range allows direct CMOS interface with no additional components.

USE WITH EXTERNAL REFERENCES — Positive polarity external reference voltages referred to analog ground may be applied to the reference input terminal to improve full-scale tempco, to provide tracking to other system elements, or to slave a number of DAC-210's to the reference output of any one of them.



DAC-312

12-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- **Guaranteed Differential Nonlinearity** **0.012%**
- **Nonlinearity** **0.025%**
- **Fast Settling Time** **250ns**
- **High Compliance** **-5V to +10V**
- **Differential Outputs** **0 to 4mA**
- **Guaranteed Monotonicity** **12 Bits**
- **Low Full-Scale Tempco** **10ppm/°C**
- **Circuit Interface to TTL, CMOS, ECL, PMOS/NMOS**
- **Low Power Consumption** **225mW**
- **Industry Standard AM6012 Pinout**

GENERAL DESCRIPTION

The DAC-312 series of 12-bit multiplying digital-to-analog converters provide high speed with guaranteed performance to 0.012% differential nonlinearity over the full commercial operating temperature range.

Based on the segmented design approach pioneered by PMI with the COMDAC® line of data converters, the DAC-312 combines a 9-bit master D/A converter with a 3-bit (MSB's) segment generator to form an accurate 12-bit D/A converter at low cost. This technique guarantees a very uniform step size (up to $\pm 1/2$ LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs. In order to provide the same performance with a 12-bit R-2R ladder design, an integral nonlinearity over temperature of 1/2 LSB (0.012%) would be required.

The 250ns settling time with low glitch energy and low power consumption are achieved by careful attention to the circuit design and stringent process controls. Direct interface with all popular logic families is achieved through the logic threshold terminal.

High compliance and low drift characteristics (as low as 10ppm/°C) are also features of the DAC-312 along with an

excellent power supply rejection ratio of $\pm 0.001\%$ FS/% Δ V. Operating over a power supply range of +5/-11V to ± 18 V the device consumes 225mW at the lower supply voltages with an absolute maximum dissipation of 375mW at the higher supply levels.

With their guaranteed specifications, single chip reliability and low cost, the DAC-312 device makes excellent building blocks for A/D converters, data acquisition systems, video display drivers, programmable test equipment and other applications where low power consumption and complete input/output versatility are required.

PIN CONNECTIONS & ORDERING INFORMATION†

**20-PIN HERMETIC
DUAL-IN-LINE
PACKAGE
(R-Suffix)**

MODEL	TEMP RANGE	DNL
DAC312BR	-55°C / +125°C	± 1 LSB
DAC312FR	0°C / +70°C	± 1 LSB
DAC312ER	0°C / +70°C	$\pm 1/2$ LSB

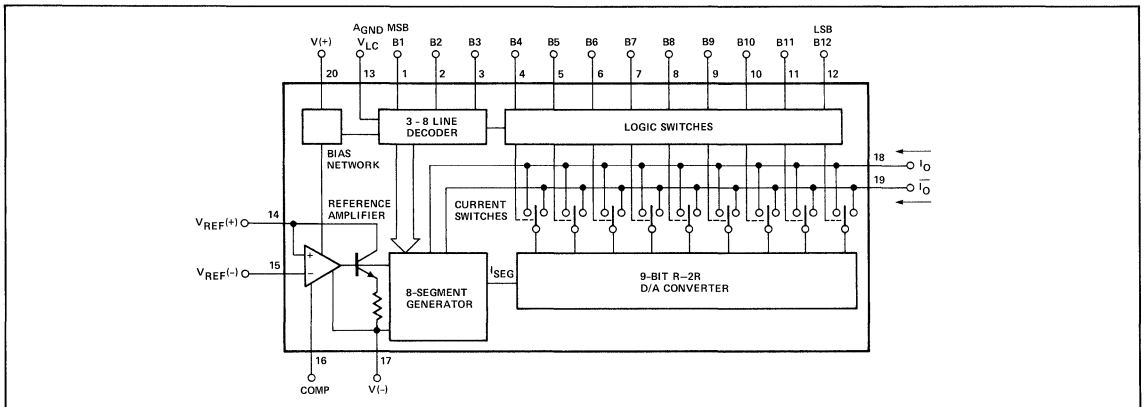
Military Temperature Range Devices
With MIL-STD-883 Class B Processing

MODEL	TEMP	DNL
DAC312BR/883	-55°C / +125°C	± 1 LSB

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

FUNCTIONAL DIAGRAM



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639

**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature	
DAC-312B	-55° C to +125° C
DAC-312E, DAC-312F	0° C to +70° C
DICE Junction Temperature	-65° C to +150° C
Storage Temperature (T _J)	-65° C to +125° C
Lead Temperature (Soldering, 60 sec)	300° C
Power Supply Voltage	±18V

Logic Inputs	-5V to +18V
Analog Current Outputs	-8V to +12V
Reference Inputs V ₁₄ , V ₁₅	V- to V+
Reference Input Differential Voltage (V ₁₄ to V ₁₅)	±18V
Reference Input Current (I ₁₄)	1.25mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

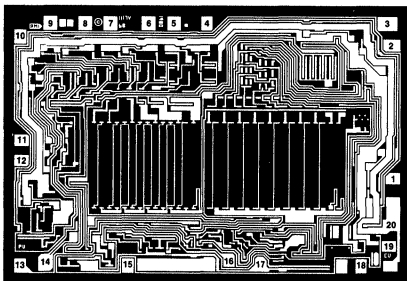
ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 1.0mA, -55° C ≤ T_A ≤ 125° C for DAC-312B, 0° C ≤ T_A ≤ 70° C for DAC-312E, DAC-312F, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT}.

PARAMETER	SYMBOL	CONDITIONS	DAC-312E			DAC-312B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			12	—	—	12	—	—	Bits
Monotonicity			12	—	—	12	—	—	Bits
Differential Nonlinearity	D.N.L.	Deviation from ideal step size	—	—	±0.0125	—	—	±0.0250	%FS
Nonlinearity	N.L.	Deviation from ideal straight line	—	—	±0.5	—	—	±1	LSB
Nonlinearity	N.L.	Deviation from ideal straight line	—	—	±0.05	—	—	±0.05	%FS
Full-Scale Current	I _{FS}	V _{REF} = 10.000V R ₁₄ = R ₁₅ = 10.000kΩ	3.967	3.999	4.031	3.935	3.999	4.063	mA
Full-Scale Tempco	TCI _{FS}		—	±10	±30	—	±10	±40	ppm/°C
			—	±0.001	±0.003	—	±0.001	±0.004	%FS/°C
Output Voltage Compliance	V _{OC}	D.N.L. Specification guaranteed over compliance range	-5	—	+10	-5	—	+10	Volts
Full-Scale Symmetry	I _{FSS}	I _{FS} - I _{FS}	—	±0.4	±1	—	±0.4	±2	μA
Zero-Scale Current	I _{ZS}		—	—	0.10	—	—	0.10	μA
Settling Time	t _S	To ±1/2 LSB, all bits switched ON or OFF (See Note)	—	250	500	—	250	500	ns
Propagation Delay — all bits	t _{PLH} t _{PHL}	All bits switched 50% point logic swing to 50% point output (See Note)	—	25	50	—	25	50	ns
Output Resistance	R _O		—	>10	—	—	>10	—	MΩ
Output Capacitance	C _{OUT}		—	20	—	—	20	—	pF
Logic Input Levels "0"	V _{IL}	V _{LC} = GND	—	—	0.8	—	—	0.8	Volts
Logic Input Levels "1"	V _{IH}	V _{LC} = GND	2	—	—	2	—	—	Volts
Logic Input Current	I _{IN}	V _{IN} = -5 to +18V	—	—	40	—	—	40	μA
Logic Input Swing	V _{IS}		-5	—	+18	-5	—	+18	Volts
Reference Bias Current	I ₁₅		0	-0.5	-2	0	-0.5	-2	μA
Reference Input Slew Rate	dI/dt	R _{14(eq)} = 800Ω C _C = 0pF (See Note)	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	PSSI _{FS+} PSSI _{FS-}	V+ = +13.5V to +16.5V, V- = -15V V- = -13.5V to -16.5V, V+ = +15V	—	±0.0005	±0.001	—	±0.0005	±0.001	%FS/%ΔV
			—	±0.00025	±0.001	—	±0.00025	±0.001	
Power Supply Range	V+ V-	V _{OUT} = 0V	4.5 -18	— —	18 -10.8	4.5 -18	— —	18 -10.8	Volts
Power Supply Current	I+ I- I+ I-	V+ = +5V, V- = -15V V+ = +15V, V- = -15V	— — — —	3.3 -13.9 3.9 -13.9	7 -18 7 -18	— — — —	3.3 -13.9 3.9 -13.9	7 -18 7 -18	mA
Power Dissipation	P _d	V+ = +5V, V- = -15V V+ = +15V, V- = -15V	— —	225 267	305 375	— —	225 267	305 375	mW

NOTE: Guaranteed by design.



DICE CHARACTERISTICS



DIE SIZE 0.140 × 0.095 inch, 13,300 sq. mils (3.56 × 2.41 mm, 8.58 sq. mm)

- | | |
|-------------|---------------------------------------|
| 1. B1 (MSB) | 11. B11 |
| 2. B2 | 12. B12 (LSB) |
| 3. B3 | 13. V _{LC} /A _{GND} |
| 4. B4 | 14. V _{REF} (+) |
| 5. B5 | 15. V _{REF} (-) |
| 6. B6 | 16. COMP |
| 7. B7 | 17. V- |
| 8. B8 | 18. I _O |
| 9. B9 | 19. I _O |
| 10. B10 | 20. V+ |

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 1.0mA$, $T_A = 25^\circ C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT-} .

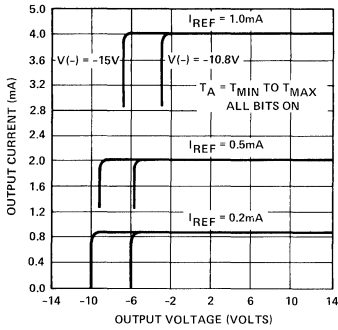
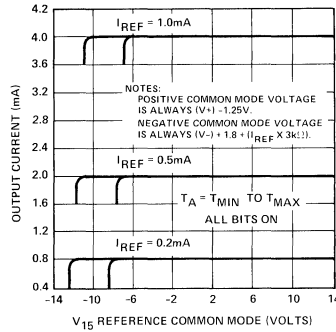
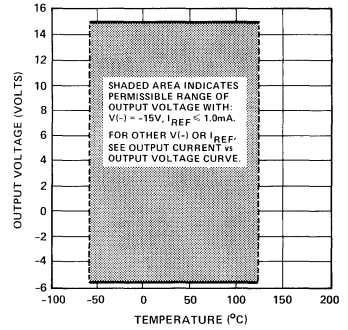
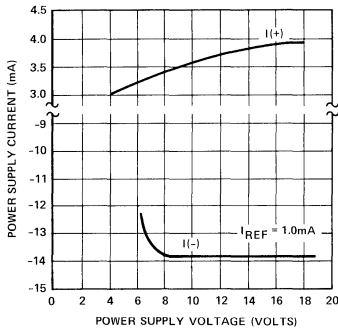
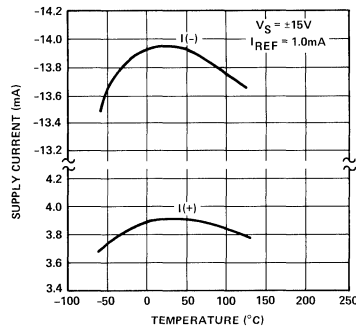
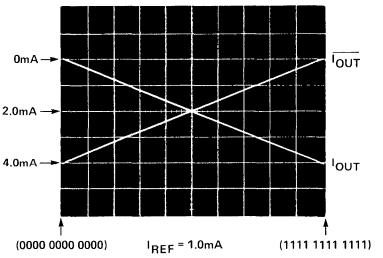
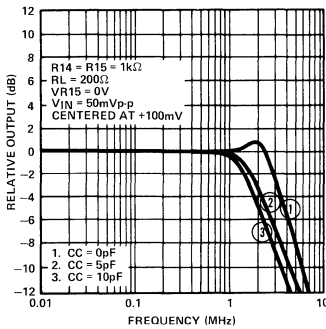
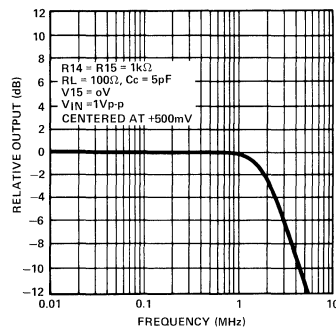
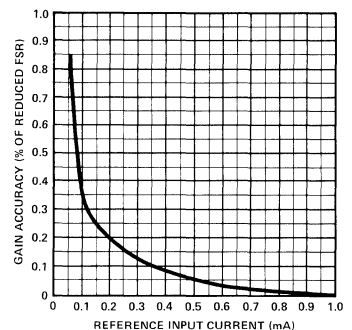
PARAMETER	SYMBOL	CONDITIONS	DAC-312N LIMIT	DAC-312G LIMIT	UNITS
Resolution			12	12	Bits MIN
Monotonicity			12	12	Bits MIN
Nonlinearity			± 0.05	± 0.05	%FS MAX
Output Voltage Compliance	V _{OC}	Full-Scale Current Change < 1/2 LSB	+10 -5	+10 -5	V MAX V MIN
Full-Scale Current		V _{REF} = 10.000V R ₁₄ , R ₁₅ = 10.000k Ω	4.031 3.967	4.063 3.935	mA MAX mA MIN
Full-Scale Symmetry	I _{FSS}		± 1	± 2	μA MAX
Zero-Scale Current	I _{ZS}		0.1	0.1	μA MAX
Differential Nonlinearity	DNL	Deviation from ideal step size	± 0.012 $\pm 1/2$	± 0.025 ± 1	%FS MAX Bits (LSB) MAX
Logic Input Levels "0"	V _{IL}	V _{LC} = GND	0.8	0.8	V MAX
Logic Input Levels "1"	V _{IH}	V _{LC} = GND	2	2	V MIN
Logic Input Swing	V _{IS}		+18 -5	+18 -5	V MAX V MIN
Reference Bias Current	I ₁₅		-2	-2	μA MAX
Power Supply Sensitivity	PSSI _{FS+} PSSI _{FS-}	V+ = +13.5V to +16.5V, V- = -15V V- = -13.5V to -16.5V, V+ = +15V	± 0.001 ± 0.001	± 0.001 ± 0.001	%/% MAX
Power Supply Current	I+ I-	V _S = $\pm 15V$ I _{REF} $\leq 1.0mA$	7 -18	7 -18	mA MAX
Power Dissipation	P _D	V _S = +15V I _{REF} $\leq 1.0mA$	375	375	mW MAX

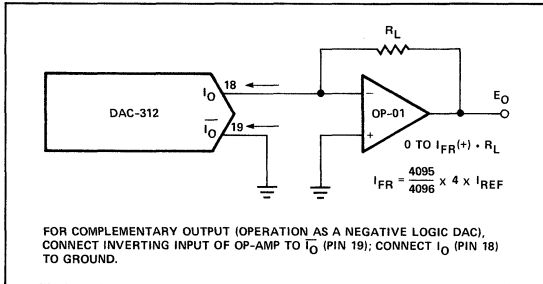
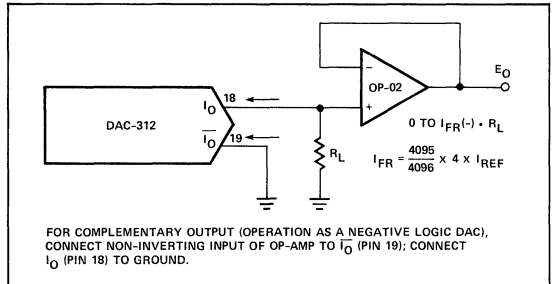
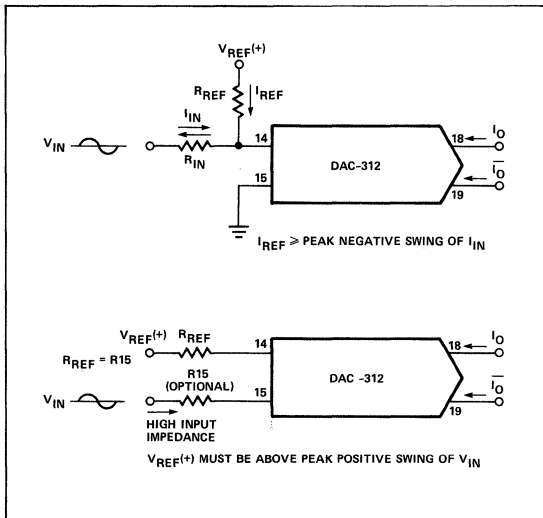
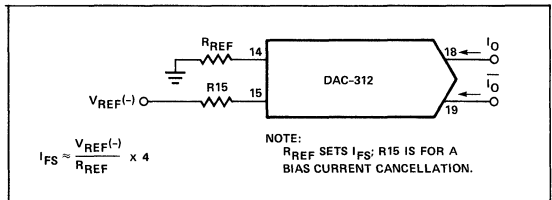
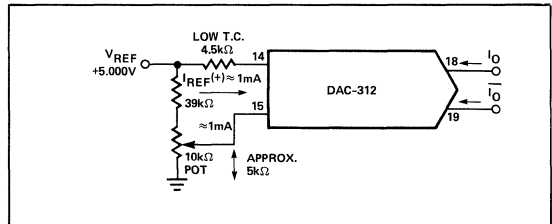
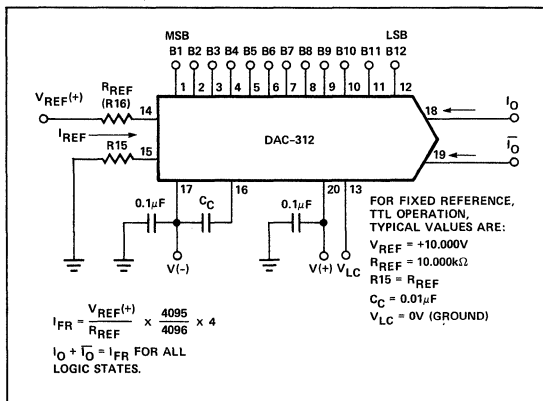
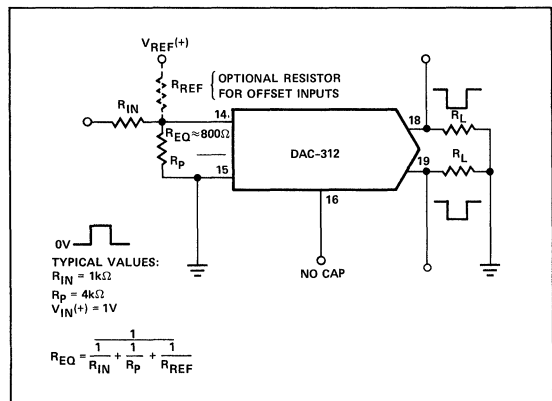
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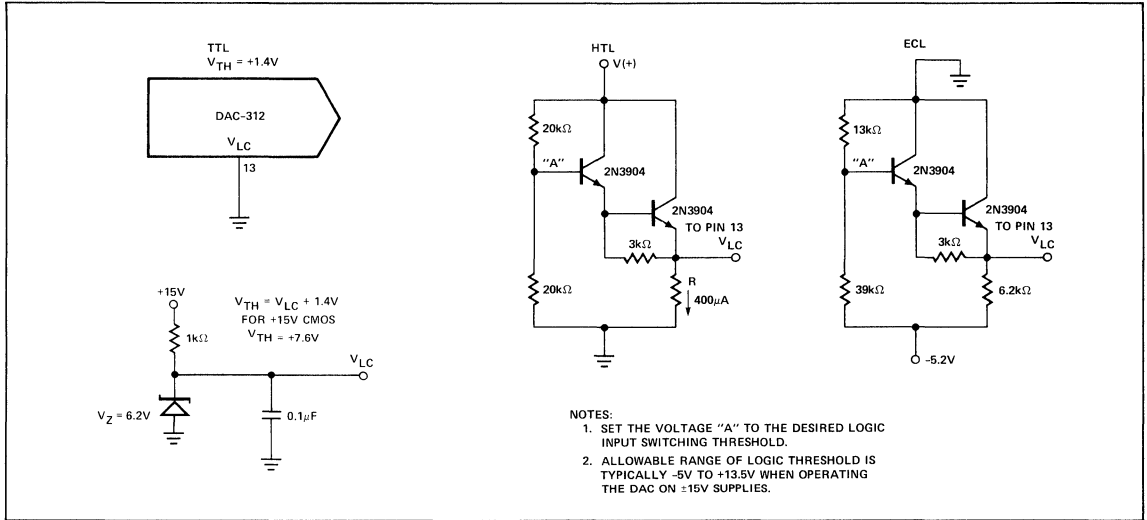
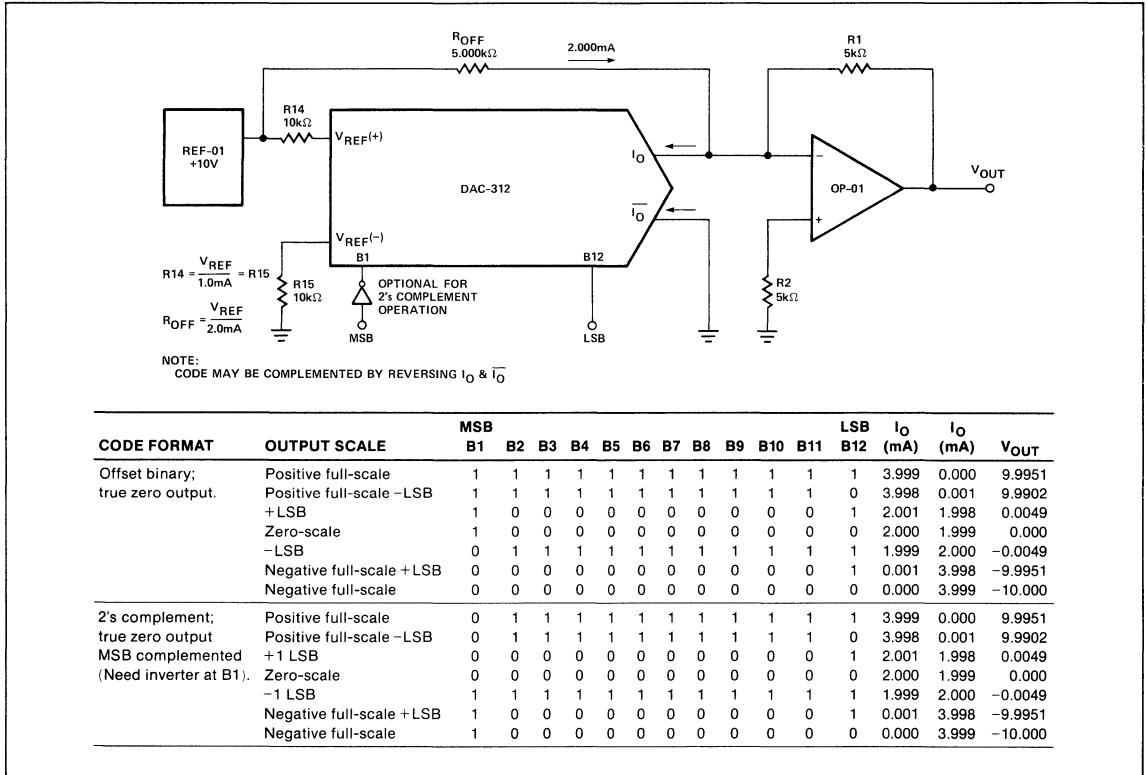
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at 25°C; V_S = $\pm 15V$, and I_{REF} = 1.0mA, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT-}.

PARAMETER	SYMBOL	CONDITIONS	DAC-312N TYPICAL	DAC-312G TYPICAL	UNITS
Reference Input Slew Rate	dl/dt		8	8	mA/ μs
Propagation Delay	t _{PLH} , t _{PHL}	Any Bit	25	25	ns
Settling Time	t _S	To $\pm 1/2$ LSB, All Bits Switched ON or OFF.	250	250	ns
Full-Scale	TC _{IFS}		± 10	± 10	ppm/ $^\circ C$

TYPICAL PERFORMANCE CHARACTERISTICS
**OUTPUT CURRENT vs
OUTPUT VOLTAGE
(OUTPUT VOLTAGE COMPLIANCE)**

**REFERENCE AMPLIFIER
COMMON-MODE RANGE**

**OUTPUT COMPLIANCE
vs TEMPERATURE**

**POWER SUPPLY CURRENT vs
POWER SUPPLY VOLTAGE**

**POWER SUPPLY CURRENT
vs TEMPERATURE**

**TRUE AND COMPLEMENTARY
OUTPUT OPERATION**

**REFERENCE AMPLIFIER
SMALL-SIGNAL
FREQUENCY RESPONSE**

**REFERENCE AMPLIFIER
LARGE-SIGNAL
FREQUENCY RESPONSE**

**GAIN ACCURACY vs
REFERENCE CURRENT**


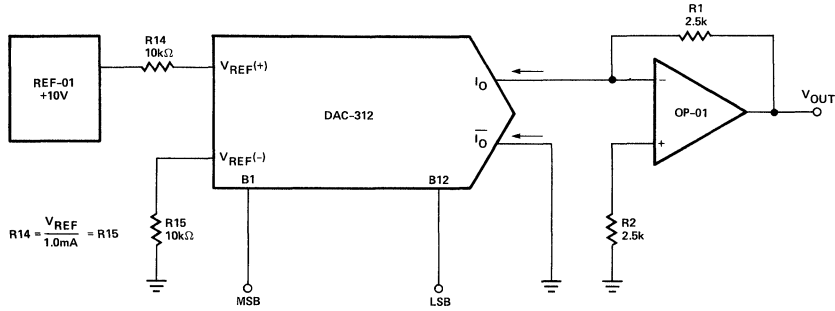
BASIC CONNECTIONS
NEGATIVE LOW IMPEDANCE OUTPUT OPERATION

POSITIVE LOW IMPEDANCE OUTPUT OPERATION

ACCOMMODATING BIPOLAR REFERENCES

BASIC NEGATIVE REFERENCE OPERATION

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT

BASIC POSITIVE REFERENCE OPERATION

PULSED REFERENCE OPERATION


BASIC CONNECTIONS
INTERFACING WITH VARIOUS LOGIC FAMILIES

BIPOLAR OFFSET (TRUE ZERO)




BASIC CONNECTIONS

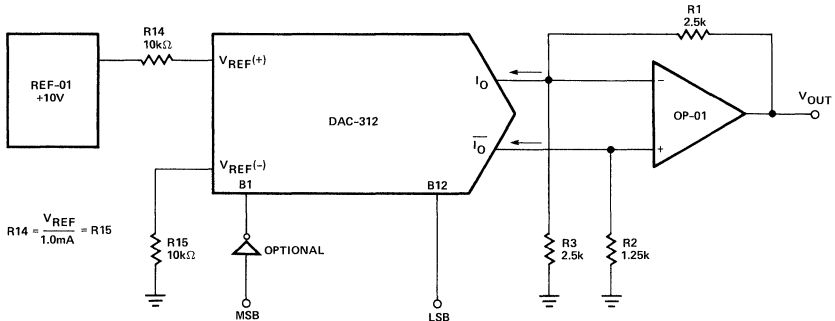
BASIC UNIPOLAR OPERATION



NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & \bar{I}_O

CODE FORMAT	OUTPUT SCALE	MSB												I_O (mA)	\bar{I}_O (mA)	V_{OUT}
		B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12			
Straight Binary; unipolar with true input code, true zero output.	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive full-scale -LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
	LSB	0	0	0	0	0	0	0	0	0	0	0	0	0.001	3.998	0.0024
Complementary binary; unipolar with complementary input code, true zero output.	Positive full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
	Positive full-scale -LSB	0	0	0	0	0	0	0	0	0	0	0	0	0.001	3.998	9.9951
	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
	Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

SYMMETRICAL OFFSET OPERATION



NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & \bar{I}_O

CODE FORMAT	OUTPUT SCALE	MSB												I_O (mA)	\bar{I}_O (mA)	V_{OUT}
		B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12			
Straight offset binary; symmetrical about zero, no true zero output.	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.00	9.9976
	Positive full-scale -LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
	(+) Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(-) Zero-scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
	Negative full-scale -LSB	0	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998
	Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976
1's complement; symmetrical about zero, no true zero output. MSB complemented (need inverter at B1).	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive full-scale -LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
	(+) Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(-) Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
	Negative full-scale -LSB	1	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998
	Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-312 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999 I_{REF}$$

$$\text{where } I_{REF} = I_{14}$$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V_-$ plus $(I_{REF} \times 3k\Omega)$ plus 1.23V. The positive common-mode range is V_+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1 μ F capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF} . If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 16 to V_- . For fixed reference operation, a 0.01 μ F capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-312 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1 μ A. Monotonic operation is maintained over a typical range of I_{REF} from 100 μ A to 1.0mA. Although some degradation of gain accuracy will be realized

at reduced values of I_{REF} . (See Gain Accuracy vs Reference Current).

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V_- . The value of this capacitor depends on the impedance presented to pin 14 for R14 values of 1.0, 2.5 and 5.0k Ω , minimum values of C_C are 5, 10, and 25pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1k Ω and C_C = 5pF, the reference amplifier slews at 4mA/ μ s enabling a transition from $I_{REF} = 0$ to $I_{REF} = 1$ mA in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800 Ω and $C_C = 0$. This yields a reference slew rate of 8mA/ μ s which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-312 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40 μ A logic input current, and completely adjustable logic threshold voltage. For $V_- = -15$ V, the logic inputs may swing between -5 and +10V. This enables direct interface with +15V CMOS logic, even when the DAC-312 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V_- plus $(I_{REF} \times 3k\Omega)$ plus 1.8V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC} . For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq 1$ mA is recommended. For interfacing other logic families, see block titled "Interfacing With Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 7mA typical; external circuitry should be designed to accommodate this current.



ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \bar{I}_O = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increases \bar{I}_O as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR} ; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V^- and is independent of the positive supply. Negative compliance is +10V above V^- .

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-312 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V^- supplies of -10V or less, $I_{REF} \leq 1\text{mA}$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -9V with $I_{REF} = 1\text{mA}$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-312 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-312 are guaranteed to apply over the entire rated operating temperature range. Full-Scale output current drift is tight, typically $\pm 10\text{ppm}/^\circ\text{C}$, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for min-

imum overall full-scale drift. Settling times of the DAC-312 decrease approximately 10% at -55°C ; at $+125^\circ\text{C}$ an increase of about 15% is typical.

SETTLING TIME

The DAC-312 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0\text{mA}$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the DAC-312 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of the settling time requires the ability to accurately resolve $\pm 1/2$ LSB of current, which is $\pm 500\text{nA}$ for 4mA FSR. In order to assure the measurement is of the actual settling time and not the R.C. time of the output network, the resistive termination on the output of the DAC must be 500 ohms or less. This does, however, place certain limitations on the testing apparatus. At I_{REF} values of less than 0.5mA, it is difficult to prevent RC damping of the output and maintain adequate sensitivity. Because the DAC-312 has 8 equal current sources for the 3 most significant bits, the major carry occurs at the code change of 000111111111 to 111000000000. The worst case settling time occurs at the zero to full-scale transition and it requires 9.2 time constants for the DAC output to settle to within $\pm 1/2$ LSB (0.0125%) of its final value.

The DAC-312 switching transients or "glitches" are on the order of 500mV-ns. This is most evident when switching through the major carry and may be further reduced by adding small capacitive loads at the output with a minor sacrifice in transition speeds.

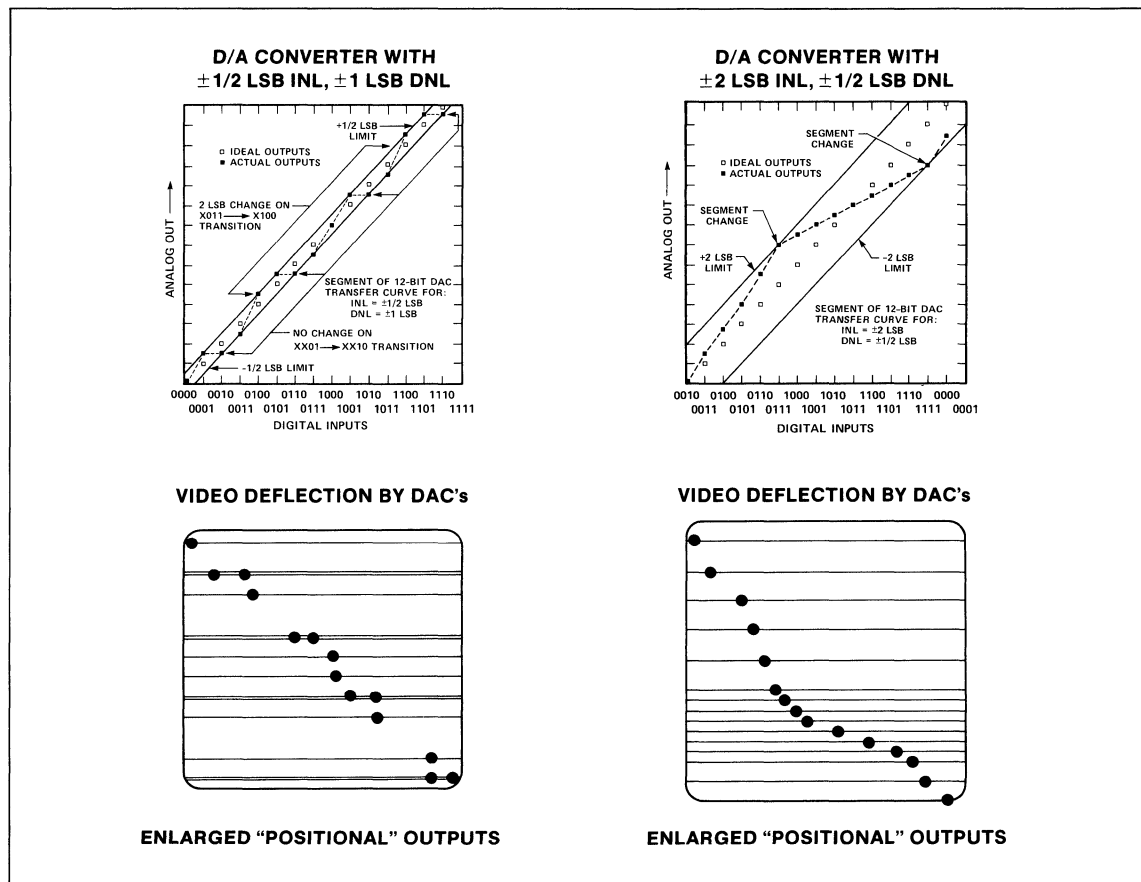
Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 μF capacitors at the supply pins provide full transient protection.

DIFFERENTIAL vs INTEGRAL NONLINEARITY

Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full-scale output or as fractional LSBs or both. The following figures define the manner in which these parameters are specified. The left figure shows a portion of the transfer curve of a DAC with 1/2 LSB INL and the (implied) DNL spec of 1 LSB. Below this is a graphic representation of the way this would appear on a CRT, for example, if the D/A Converter output were to be applied to the Y input of a CRT as shown in the application schematic titled "CRT Display Driver". On the right is a portion of the transfer curve of a DAC specified for 2 LSB INL with 1/2 LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e. the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2 LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, 2 LSB gaps can cause large errors at those input levels (assuming 1/2 LSB quantizing levels). It can be seen from the two figures that the DNL specified D/A converter will yield much finer grained data than the INL specified part, thus improving the ability of the A/D to resolve changes in the analog input.

DIFFERENTIAL LINEARITY COMPARISON



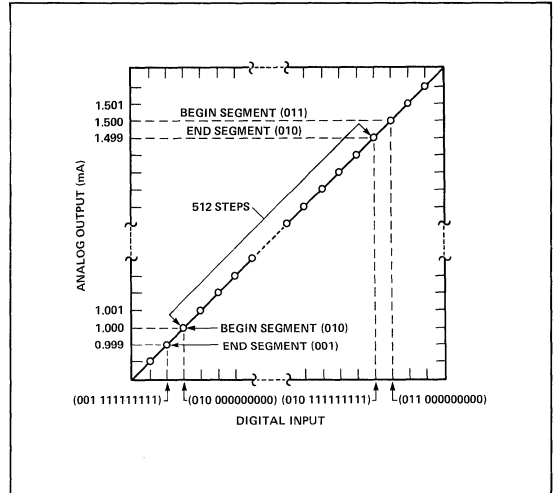


DESCRIPTION OF OPERATION

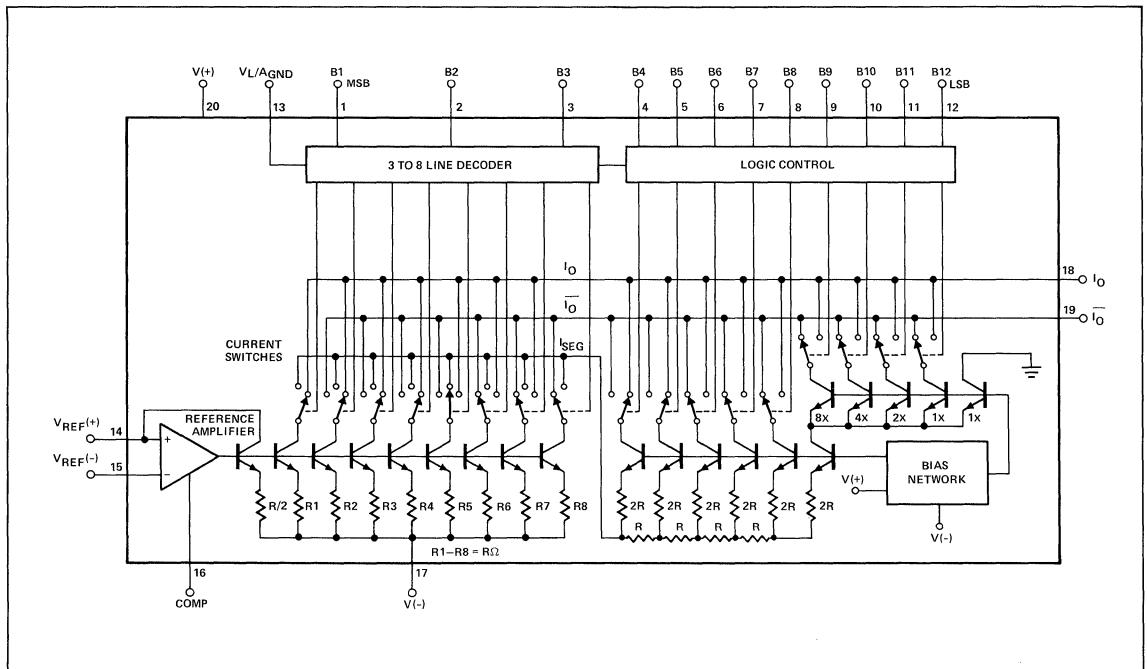
The DAC-312 is divided into two major sections, an 8-segment generator and a 9-bit master/slave D/A Converter. In operation the device performs as follows (See Simplified Schematic):

The three most significant bits (MSB's) are inputs to a 3-to-8 line decoder. The selected resistor (R5 in the figure) is connected to the master/slave 9-bit D/A Converter. All lower order resistors (R1 through R4) are summed into the I_O line, while all higher order resistors (R6 through R8) are summed into the I₀ line. The R5 current supplies 512 steps of current (0 to 0.499mA for a 1mA reference current) which are also summed into the I_O or I₀ lines depending on the bits selected. In the figure, the code selected is: 100 110000000. Therefore, 2mA (4 X 0.5mA/segment) + 0.375mA (from master/slave D/A Converter) are summed into I_O giving an I_O of 2.375mA. I₀ has a current of 1.625mA with this code. As the three MSB's are incremented, each successively higher code adds 0.5mA to I_O and subtracts 0.5mA from I₀, with the selected resistor feeding its current to the master/slave D/A Converter; thus each increment of the 3 MSB's allows the current in the 9-bit D/A Converter to be added to a pedestal consisting of the sum of all lower order currents from the segment generator. This configuration guarantees monotonicity.

EXPANDED TRANSFER CHARACTERISTIC SEGMENT (001 010 011)

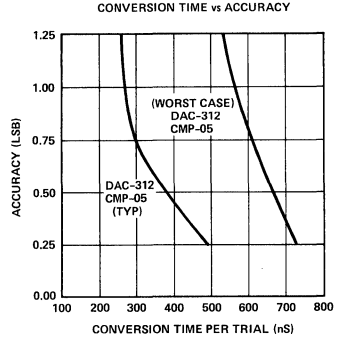
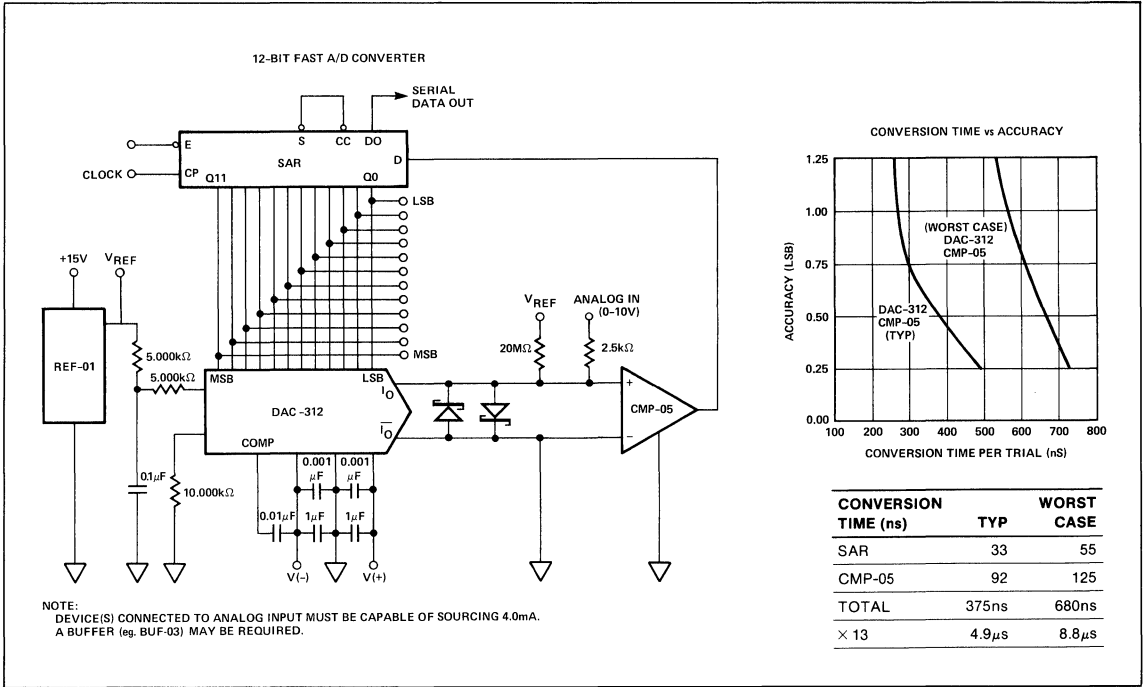


SIMPLIFIED SCHEMATIC





12-BIT FAST A/D CONVERTER



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375ns	680ns
× 13	4.9μs	8.8μs



DAC-888

BYTEDAC® 8-BIT HIGH-SPEED "MICROPROCESSOR COMPATIBLE" MULTIPLYING D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- 8-Bit Level Triggerged Latch
- 8-Bit μ P Compatible
- Easily Interfaced to All 8-Bit Processors
- TTL Logic Compatible
- \overline{CE} and \overline{WR} Inputs
- High Output Impedance and Compliance
- Proven DAC-08 Analog Flexibility and Reliability
- Nonlinearity to $\pm 0.1\%$ Max
- Low Power Dissipation 134mW

ORDERING INFORMATION†

18-PIN HERMETIC DUAL-IN-LINE PACKAGE

NL %FS	MILITARY TEMP.	INDUSTRIAL TEMP.
0.1	DAC888AX*	DAC888EX
0.19	DAC888BX*	DAC888FX

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

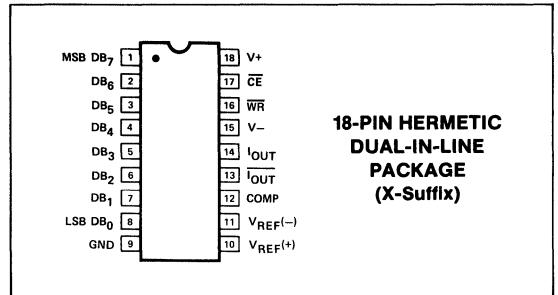
The BYTEDAC® DAC-888 is a buffered 8-bit digital-to-analog converter designed specifically for 8-bit bus oriented systems. The data inputs are connected to level-triggerged latches. Two active-low control pins are provided for ease of interface to virtually all available microprocessors. The

latches may also be operated in a transparent mode by holding both control pins low. Additionally, the DAC-888 has a data hold time requirement of zero nanoseconds.

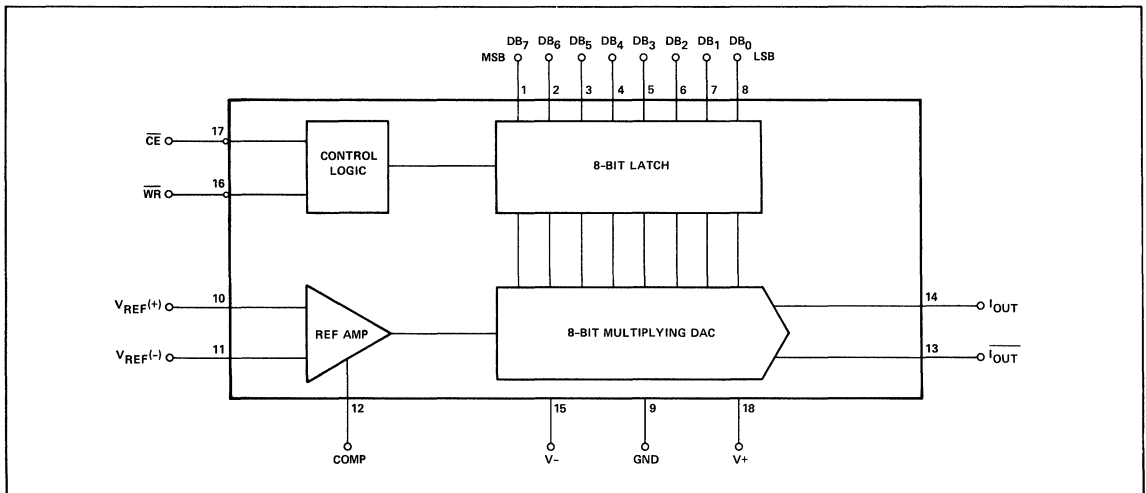
The Analog section consists of a "Field-Proven" DAC-08 D/A Converter. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates full-scale adjustment in most applications.

DAC-888 applications include graphic display drivers, high-speed modems, A/D converters, programmable waveform generators and power supplies, analog meter drivers, audio encoders and programmable attenuators; and other applications where low cost, high speed and buffered flexibility are required.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639



ABSOLUTE MAXIMUM RATINGS

Operating Temperature
 DAC-888 A/B -55° C to +125° C
 DAC-888 E/F -25° C to +85° C
 DICE Junction Temperature (T_j) -65° C to +150° C
 Storage Temperature -65° C to +150° C
 Power Dissipation 300mW
 Derate above 100° C 10mW/° C
 Lead Temperature (Soldering, 60 sec) 300° C
 V+ Supply to V- Supply 18.1V

Logic Inputs 0V to 5.5V
 Analog Current Outputs -5mA
 Reference Inputs (V₁₀ to V₁₁) V- to V+
 Reference Input Differential Voltage
 (V₁₀ to V₁₁) ±15V
 Reference Input Current 5mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = +5V, V- = -12V, I_{REF} = 2mA, T_A = -55° C to +125° C for DAC-888A/B, unless otherwise noted. T_A = 25° C to +85° C apply for DAC-888E/F. Output characteristics refer to both I_{OUT} and I_{OUT}.

PARAMETER	SYMBOL	CONDITIONS	DAC-888A/E			DAC-888B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	Bits
Nonlinearity			—	—	±0.1	—	—	±0.19	%FS
Full-Scale Tempco	TCI _{FS}	(See note)	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance	V _{OC}	Full-Scale Current Change < 1/2 LSB	-5	—	+5	-5	—	+5	V
Output Impedance	R _{OUT}		—	>20	—	—	>20	—	MΩ
Full Range Current	I _{FR}	V _{REF} = 5.00V R ₁₁ , R ₁₀ = 2.500kΩ T _A = 25° C	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I _{FRS}	I _{FR14} - I _{FR13}	—	±1	±8	—	±1	±8	μA
Zero-Scale Current	I _{ZS}		—	0.2	2	—	0.2	2	μA
Output Current Range	I _{FSR}	I _{REF} = 3mA	2.1	2.9	—	2.1	2.9	—	mA
Reference Bias Current	I _B		—	-1	-3	—	-1	-3	μA
Power Supply Sensitivity	PSSI _{FR+}	V+ = 4.5V to 5.5V	—	±0.0003	±0.01	—	±0.0003	±0.01	%ΔI _{FS} /%ΔV+
	PSSI _{FR-}	V- = -10.8V to -13.2V I _{REF} = 1mA	—	±0.0002	±0.01	—	±0.0002	±0.01	%ΔI _{FS} /%ΔV-
Power Supply Current	I+		—	12	16	—	12	16	mA
	I-	I _{REF} = 2mA	—	6	9	—	6	9	
Power Dissipation	P _d	I _{REF} = 2mA	—	134	190	—	134	190	mW
Logic Input Levels									
Logic Input "0"	V _{IL}		—	—	0.8	—	—	0.8	V
Logic Input "1"	V _{IH}		2	—	—	2	—	—	
Logic Input Current									
Logic Input "0"	I _{IL}	V _{IN} = 0.8V	—	-2	-10	—	-2	-10	μA
Logic Input "1"	I _{IH}	V _{IN} = 5.0V	—	0.1	1	—	0.1	1	

NOTE: Guaranteed by design.



ELECTRICAL CHARACTERISTICS — A.C. PARAMETERS $V_S = +5V, -12V, I_{REF} = 2mA, T_A = 25^\circ C.$

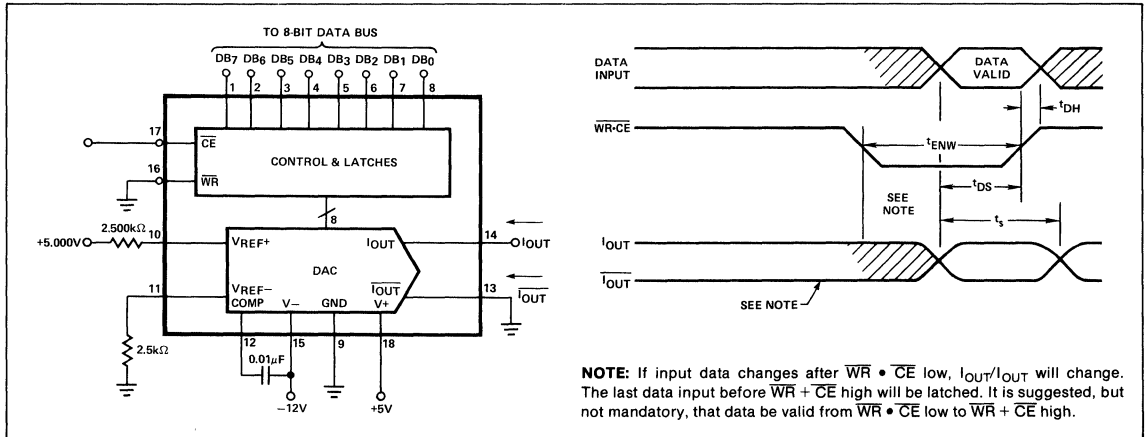
PARAMETER	SYMBOL	CONDITIONS	DAC-888A/E			DAC-888B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time	t_s	From \overline{CE} & \overline{WR} Negative Level to $\pm 1/2LSB$, All Bits Switched ON or OFF, (See note)	—	300	400	—	300	400	ns
Reference Input Slew Rate	dI/dt	(See Note)	4	8	—	4	8	—	$mA/\mu s$
Data Input Setup Time	t_{DS}	(See note)	150	—	—	150	—	—	ns
Data Input Hold Time	t_{DH}	(See note)	10	—	—	10	—	—	ns
Chip Enable/Write Pulse Width	t_{ENW}	(See note)	250	—	—	250	—	—	ns

NOTE: Guaranteed by design.

DAC-888 PIN DESCRIPTION

SYMBOL	DESCRIPTION	
$DB_0 - DB_7$	DATA BIT — Bits 0-7 are digital, active-high inputs. DB_7 is assigned as the MSB.	PINS 1-8
\overline{CE}	CHIP ENABLE — An active low input control which is the device enable input terminal.	PIN 17
\overline{WR}	WRITE CONTROL — An active low control which enables the microprocessor to write data to the DAC.	PIN 16
$I_{OUT+} \cdot I_{OUT-}$	CURRENT OUTPUT — Complementary current outputs, which when added, equal I_{FS} .	PINS 13-14
V_{REF+}, V_{REF-}	VOLTAGE REFERENCE — Differential inputs that accept a negative, positive, or bipolar input and are used to set I_{FS} .	PINS 10-11
COMP	COMPENSATION — The reference amplifier frequency compensating terminal.	PIN 12

FUNCTIONAL DIAGRAM AND TIMING DIAGRAM FOR 8-BIT OPERATION

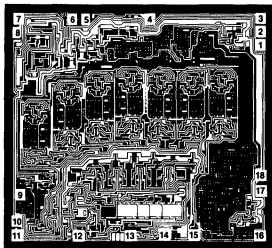


OPERATION TABLE

\overline{CE}	\overline{WR}	OUTPUT
1	X	NO CHANGE
0	1	NO CHANGE
0	0	UPDATE LATCHES (TRANSPARENT)



DICE CHARACTERISTICS



- | | |
|--------------|--------------------------|
| 1. DB7 (MSB) | 10. $V_{REF} (+)$ |
| 2. DB6 | 11. $V_{REF} (-)$ |
| 3. DB5 | 12. COMP |
| 4. DB4 | 13. $\overline{I_{OUT}}$ |
| 5. DB3 | 14. I_{OUT} |
| 6. DB2 | 15. V_- |
| 7. DB1 | 16. \overline{WR} |
| 8. DB0 (LSB) | 17. \overline{CE} |
| 9. GROUND | 18. V_+ |

For additional DICE information refer to 1986 Data Book, Section 2.

DIE SIZE 0.139 × 0.126 inch; 17, 514 sq. mils
(3.53 × 3.2mm.; 11.296 sq. mm.)

WAFER TEST LIMITS at $V_S = +5, -12V$, $I_{REF} = 2mA$, $T_A = 25^\circ C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-888N LIMIT	DAC-888G LIMIT	UNITS
Resolution			8	8	Bits MIN
Monotonicity			8	8	Bits MIN
Nonlinearity			±0.1	±0.19	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB $R_{OUT} > 20M\Omega$ Typ.	+5 -5	+5 -5	V MAX V MIN
Full Range Current	I_{FR14}	$V_{REF} = 5.00V$ $R_{11}, R_{10} = 2,500k\Omega$ $T_A = 25^\circ C$	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full Range Symmetry	I_{FRS}	$I_{FR14} - I_{FR13}$	±8	±8	µA MAX
Zero-Scale Current	I_{ZS}		2	2	µA MAX
Output Current Range	I_{FSR}	$I_{REF} = 3mA$	2.1	2.1	mA MIN
Reference Bias Current	I_B		-3	-3	µA MAX
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	$V_+ = 4.5V$ to $5.5V$ $V_- = -4.5V$ to $-12V$, $I_{REF} = 1mA$	±0.01 ±0.01	±0.01 ±0.01	% Δ /FS/% Δ V+ MAX % Δ /FS/% Δ V- MAX
Power Supply Current	I_+ I_-	$I_{REF} = 2mA$	16 9	16 9	mA MAX
Power Dissipation	P_d	$I_{REF} = 2mA$	190	190	mW MAX
Logic Input Levels					
Logic Input "0"	V_{IL}		0.8	0.8	V MAX
Logic Input "1"	V_{IH}		2	2	V MIN
Logic Input Current	I_{IL} I_{IH}	$V_{IN} = 0.8V$ $V_{IN} = 5.0V$	-10 1	-10 1	µA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS $V_+ = +5V$, $-12V$, $I_{REF} = 2mA$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-888 TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8.0	mA/µs
Settling Time	t_s	From \overline{CE} Negative Edge to ±1/2 LSB, All bits Switched ON or OFF	300	ns
Data Input Setup Time	t_{DS}		100	ns
Data Input Hold Time	t_{DH}		0	ns
Chip Enable Write Pulse Width	t_{ENW}		200	ns



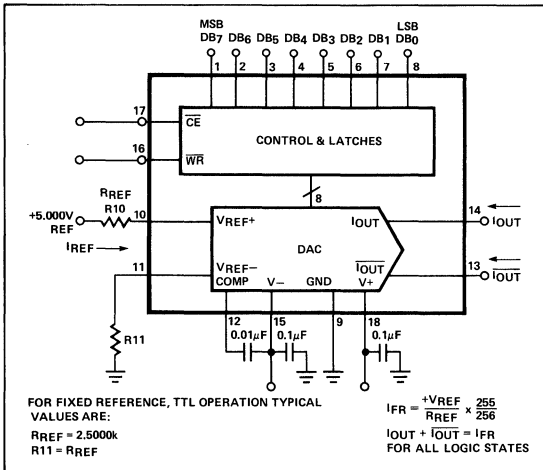
DIGITAL INFORMATION

The BYTEDAC® DAC-888 is a monolithic microprocessor compatible D/A converter consisting of an 8-bit level triggered latch, control circuitry and one 8-bit multiplying D/A converter housed in an 18-pin dual in line package (DIP).

The DAC-888 accepts 8-bit binary bytes at the data inputs. Data access is accomplished when \overline{WR} and \overline{CE} are low. During the low state of \overline{CE} and \overline{WR} , the latches are transparent, therefore, data should be valid from 100ns prior to \overline{WR} and \overline{CE} low until \overline{CE} or \overline{WR} high. When \overline{CE} or \overline{WR} goes high, the data stored in the latches will hold the selected output indefinitely.

ANALOG INFORMATION

BASIC POSITIVE REFERENCE OPERATION



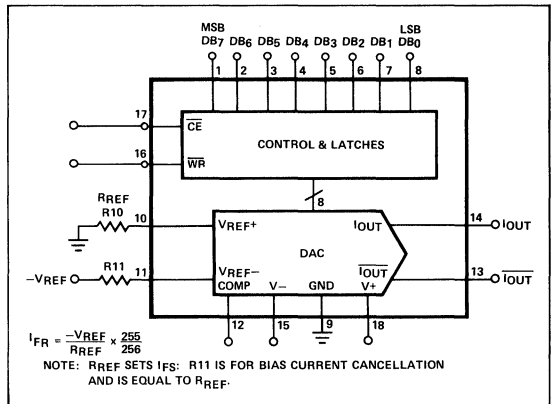
or may vary from nearly 0 to +4.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = 10$$

In positive reference applications, an external positive reference voltage current flows through R_{10} into the $V_{REF(+)}$ terminal of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$; reference current flows from ground through R_{10} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 11. The voltage at pin 10 is equal to and tracks the voltage at pin 11 due to the high gain of the internal reference amplifier. R_{11} (nominally equal to R_{10}) is used to cancel bias current errors; R_{11} may be eliminated with only a minor increase in error.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF} . If required, full-scale trimming may be accomplished by adjusting the value of R_{10} or by using a potentiometer for R_{10} . An improved method of full-scale trimming which eliminates potentiometer

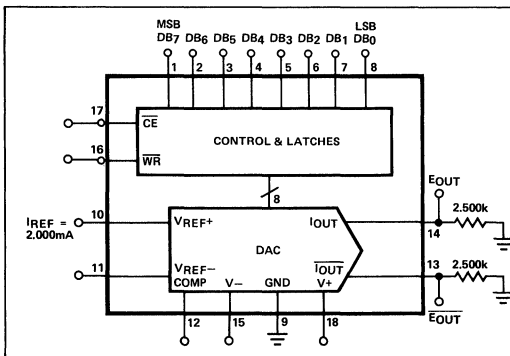
BASIC NEGATIVE REFERENCE OPERATION



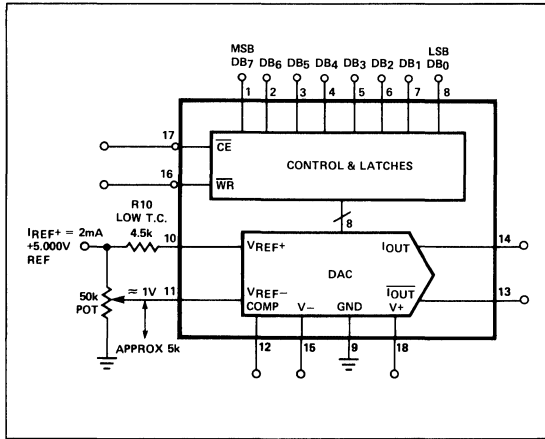
REFERENCE AMPLIFIER SET-UP

The DAC-888 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed

BASIC UNIPOLAR NEGATIVE OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	I_{0mA}	I_{0mA}	E_O	\overline{E}_O
FULL-SCALE	1	1	1	1	1	1	1	1	1.992	0.000	-4.980	0.000
FULL-SCALE -1 LSB	1	1	1	1	1	1	1	0	1.984	0.008	-4.960	-0.020
HALF-SCALE +1 LSB	1	0	0	0	0	0	0	1	1.008	0.984	-2.520	-2.460
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	0.992	-2.500	-2.480
HALF-SCALE -1 LSB	0	1	1	1	1	1	1	1	0.992	1.000	-2.480	-2.500
ZERO-SCALE +1 LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.020	-4.960
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	1.992	-0.000	-4.980

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT


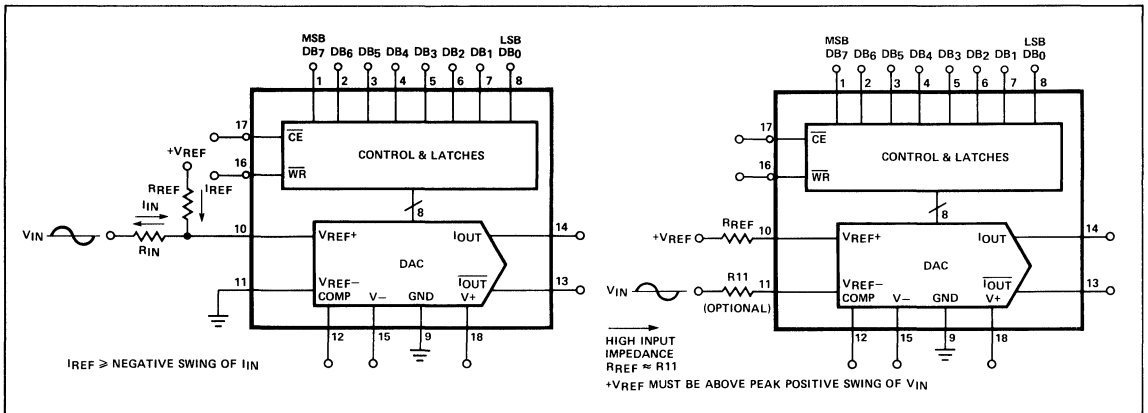
meter TC effects is shown in the Recommended Full Scale Adjustment Circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 12 to V-. For fixed reference operation a 0.01μF capacitor is recommended. For variable reference applications, see "Reference Amplifier Compensation for Multiplying Applications" section.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 12 to V-. The value of this capacitor depends on the impedance presented to pin 10 (see Table 1).

ACCOMMODATING BIPOLAR REFERENCES

TABLE 1. REFERENCE AMPLIFIER COMPENSATION

REF. INPUT RESISTANCE	SUGGESTED C_C
1kΩ	15pF
2.5kΩ	37pF
5kΩ	75pF

NOTE: A 0.01μF capacitor is suggested for fixed references.

For fastest response to a pulse, low values of R_{10} , enabling small C_C values, should be used. If pin 10 is driven by a high current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For $R_{10} = 1k\Omega$ and $C_C = 15pF$, the reference amplifier slews at 4mA/μs, enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns (see Figure, pulsed reference operation).

Bipolar references may be accommodated by offsetting V_{REF} or pin 11, as shown in Figure below. The negative common-mode range of the reference amplifier is given by $V_{CM} = V_-$ plus $(I_{REF} \times 1k\Omega)$ plus 2.5V. The positive common-mode range is V_+ less 1.5V.

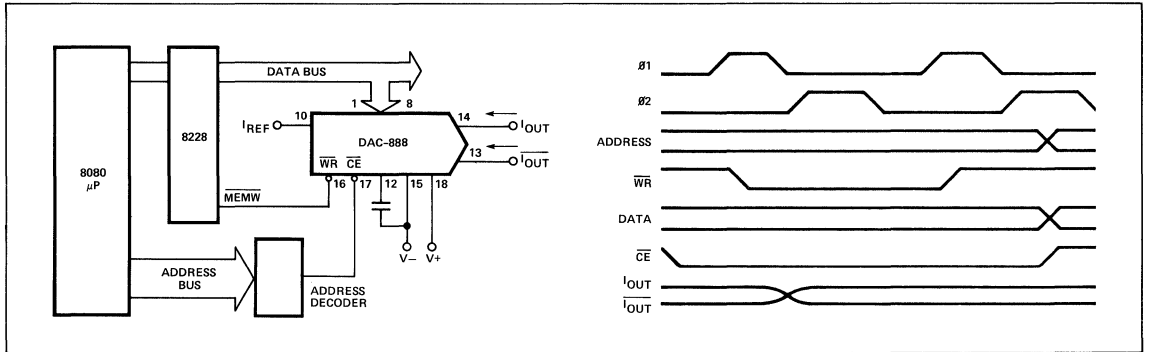
When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL Logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{10} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

ANALOG OUTPUT CURRENTS

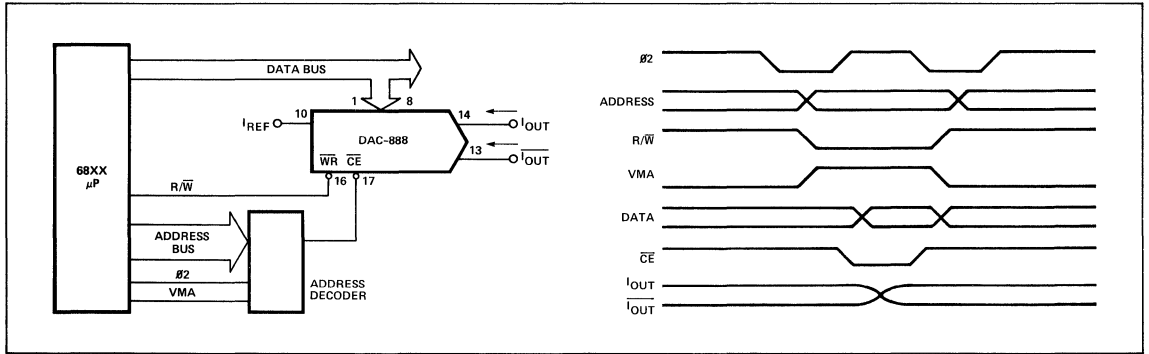
Both true and complemented output sink currents are provided, where $I_O + \bar{I}_O = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 14 increases proportionally in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 14 and turned on at pin 13. A decreasing logic count increases \bar{I}_O as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS} ; do not leave an unused output pin open.



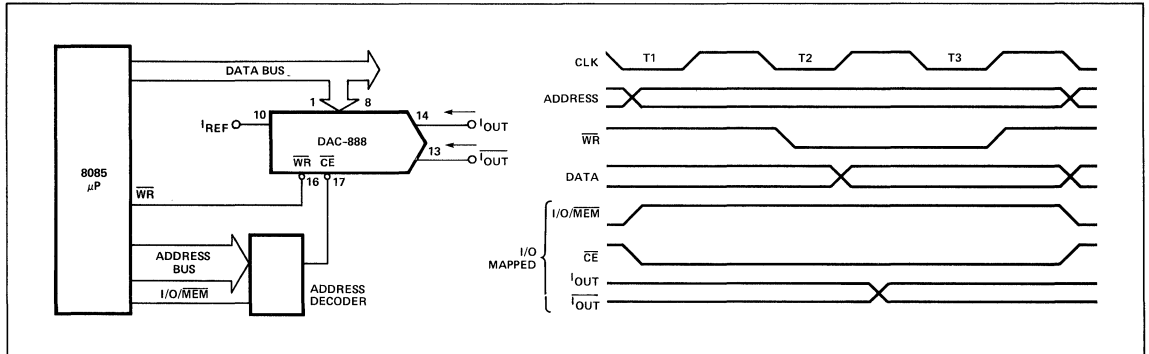
8080 INTERFACE

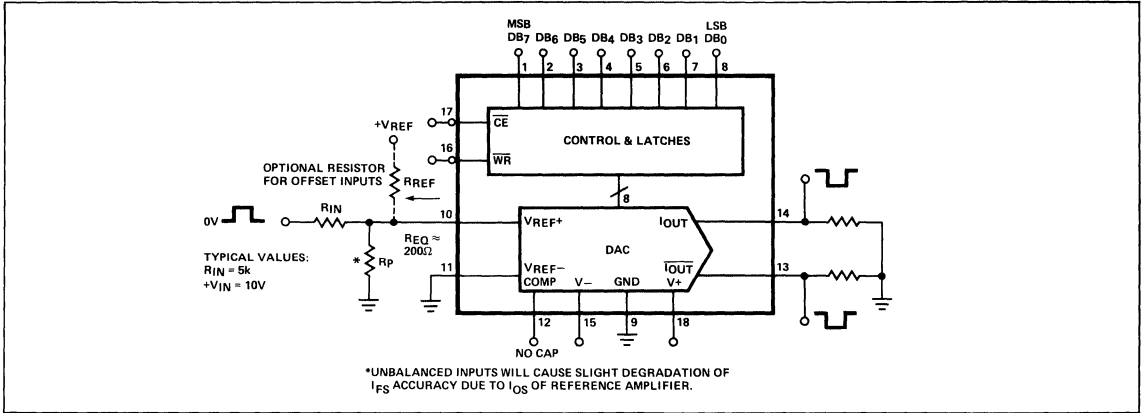
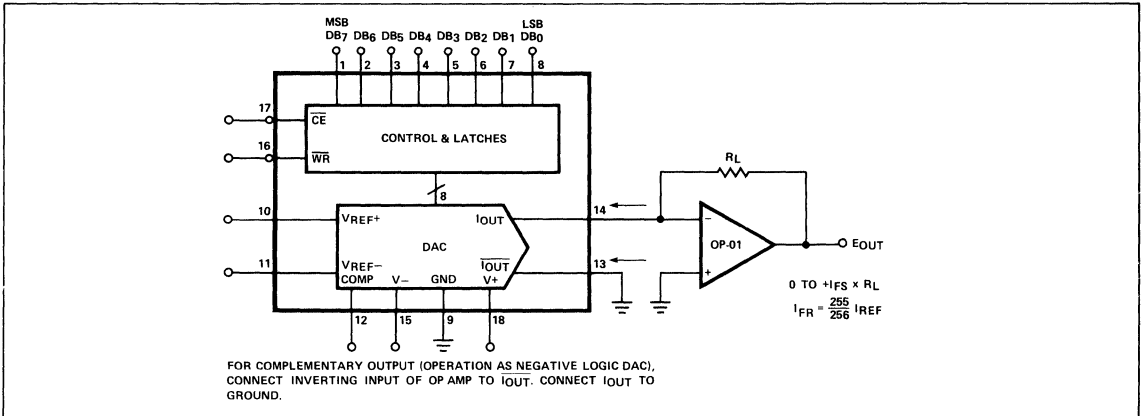
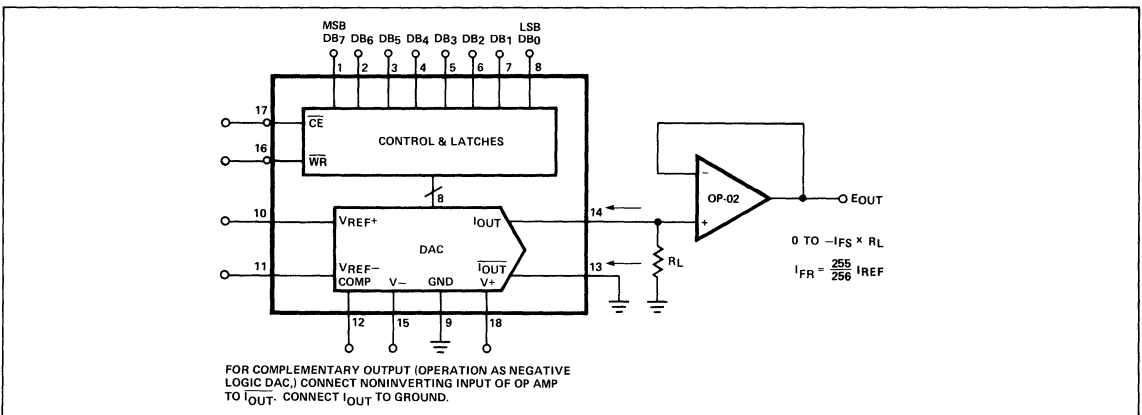


6800, 6801, 6809 INTERFACE



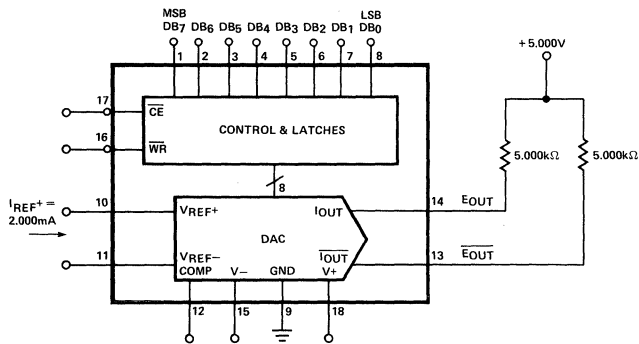
8085 INTERFACE



PULSED REFERENCE OPERATION

POSITIVE LOW IMPEDANCE OUTPUT OPERATION

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


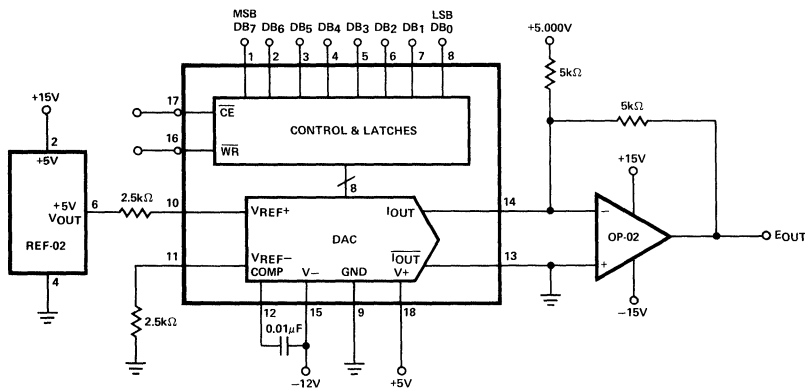


BASIC BIPOLAR OUTPUT OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O	\bar{E}_O
POSITIVE FULL-SCALE	1	1	1	1	1	1	1	1	-4.960	5.000
POSITIVE FULL-SCALE -1 LSB	1	1	1	1	1	1	1	0	-4.920	4.960
ZERO-SCALE +1LSB	1	0	0	0	0	0	0	1	-0.040	0.080
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	0.040
ZERO-SCALE -1LSB	0	1	1	1	1	1	1	1	0.040	0.000
NEGATIVE FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	4.900	-4.920
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	5.000	-4.960

OFFSET BINARY OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O
POSITIVE FULL-SCALE	1	1	1	1	1	1	1	1	4.960
POSITIVE FULL-SCALE -1LSB	1	1	1	1	1	1	1	0	4.920
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEGATIVE ZERO-SCALE +1LSB	0	0	0	0	0	0	0	1	-4.960
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	-5.000



BASIC BIPOLAR OUTPUT OPERATION

Both outputs have an extremely wide voltage compliance, enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 18V above V₋ and is independent of the positive supply. Negative compliance is given by V₋ plus (I_{REF} X 1kΩ) plus 2.5V.

POWER SUPPLIES

The DAC-888 operates over a wide range of power supply voltages from a total supply of 9V to 15V. When operating at supplies of ±5V or less, I_{REF} ≤ 1mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower

supplies is possible. However, at least 8V must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-888 is quite insensitive to variations in supply voltage.

Power consumption may be calculated as follows:

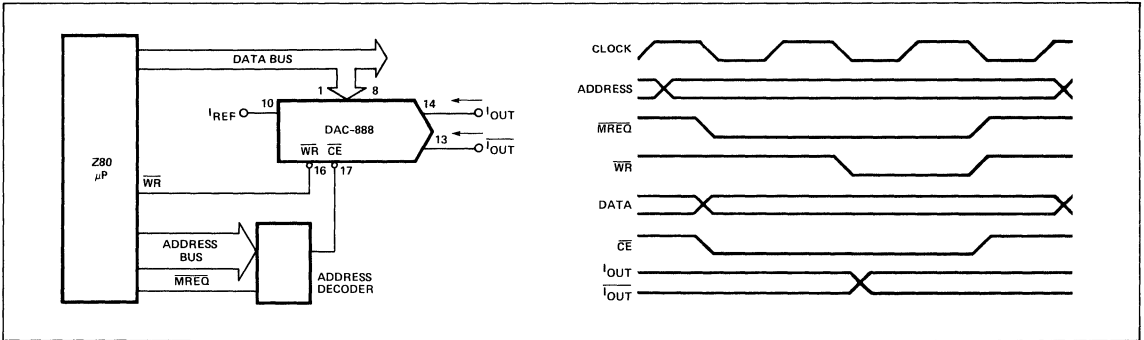
$$P_d = (I^+) (V^+) + (I^-) (V^-)$$

TEMPERATURE PERFORMANCE

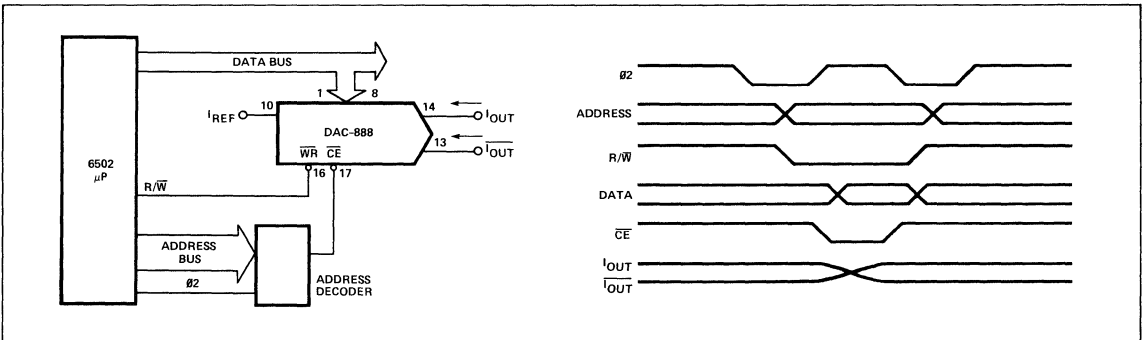
The nonlinearity and monotonicity specifications of the DAC-888 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R₁₀ should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-888 decrease approximately 10% at -55°C; at +125°C an increase of about 15% is typical.

Z-80 INTERFACE

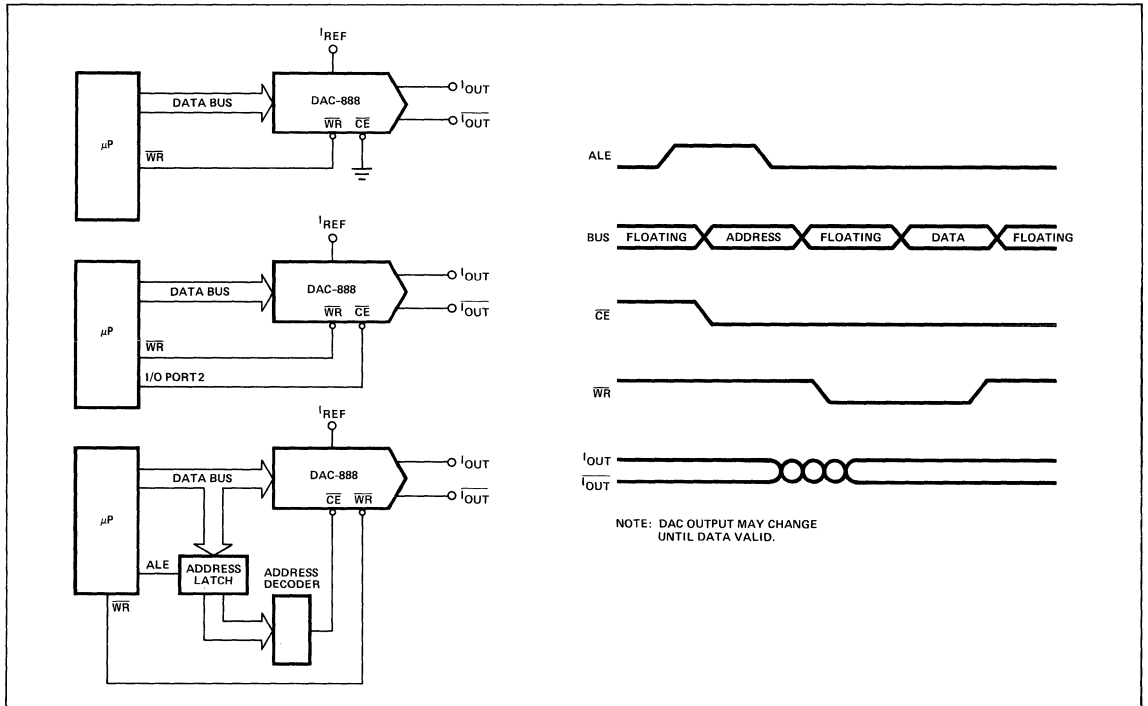


6502 INTERFACE

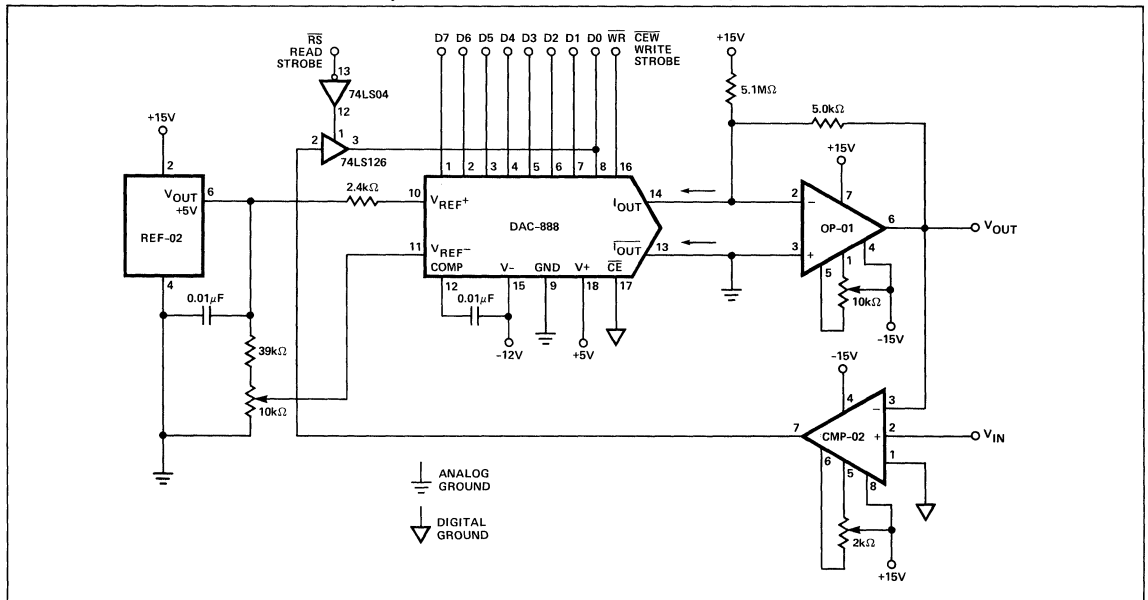




8048 INTERFACE



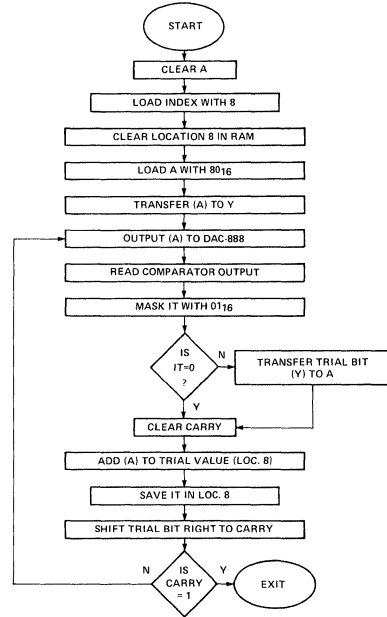
'SOFTWARE SAR' A/D CONVERTER (WITH 8048 MICROPROCESSOR)



SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERSION PROGRAM LISTING USING DAC-888 AND SYM 1 PCB WITH 6502μP WITH FLOW CHART

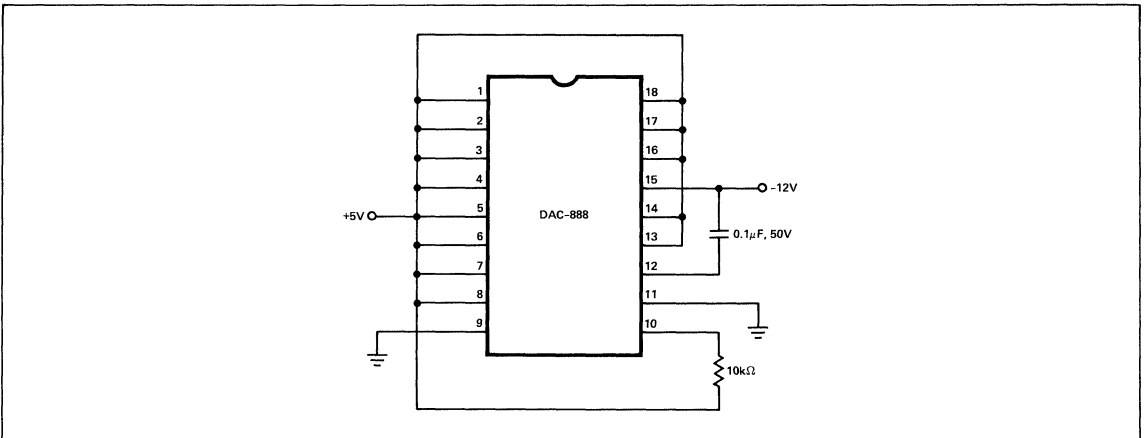
LOCATION	DATA	MNEMONIC	COMMENTS
500	A9 00	LDA #00	Clear
502	A2 08	LDX #08	Set Index Register
504	95 00	STA ,X	Clear Memory at 08 _H
506	A9 80	LDA #80	Trial Bit
508	A8	TAY	TO Y
509	8D 00 10	STA 1000 (Cont.)	Output
50C	AD 00 1C	LDA 1C00	Read Comp.
50F	29 01	AND A, #01	Mask it
511	F0 01	BEC * +1	Branch if CMP = 0
513	98	TYA	Get Trial Bit
514	18	CLC	Clear Carry
515	75 00	ADC ,X	Result Summed With Previous Test
517	95 00	STA ,X	Save it
519	98	TYA	Get Trial Value
51A	4A	LSR	Next Bit
51B	A8	TAY	Save it
51C	15 00	ORA ,X	Next Data
51E	90 E9	BCC *-23	Continue For 8 Trials
520	4C 00 05	JMP 500	Do Over

NOTE: 32 Bytes 260μs



DIGITAL-TO-ANALOG CONVERTERS

BURN-IN CIRCUIT





DAC-1508A/1408A

8-BIT MULTIPLYING
D/A CONVERTERS

Precision Monolithics Inc.

FEATURES

- Improved Direct Replacement for MC1508/MC1408
- 0.19% Nonlinearity Maximum Over Temperature Range
- Improved Settling Time 250ns, Typ
- Improved Power Consumption 157mW, Typ
- Compatible with TTL, CMOS Logic
- Standard Supply Voltages +5.0V and -5.0V to -15V
- Output Voltage Swing +0.5V to -5.0V
- High-Speed Multiplying Input 4.0mA/ μ s

ORDERING INFORMATION†

RELATIVE ACCURACY % FS	16-PIN DUAL-IN-LINE PACKAGE		
	HERMETIC MILITARY	COMMERCIAL	PLASTIC COMMERCIAL
$\pm 0.19\%$	DAC1508A-8Q*	DAC1408A-8Q	DAC1408A-8P
$\pm 0.39\%$	—	DAC1408A-7Q	DAC1408A-7P
$\pm 0.78\%$	—	DAC1408A-6Q	DAC1408A-6P

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

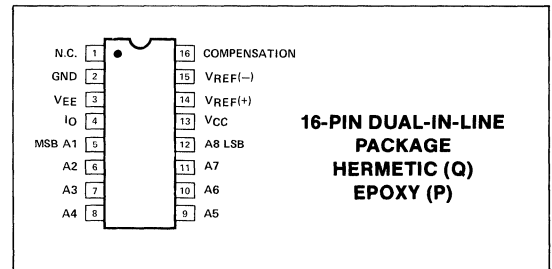
The DAC-1508A/1408A are 8-bit monolithic multiplying digital-to-analog converters consisting of a reference current amplifier, R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

The R-2R ladder divides the reference current into eight binarily-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full-scale output current of 1.992mA would result from a reference input current of 2.0mA.

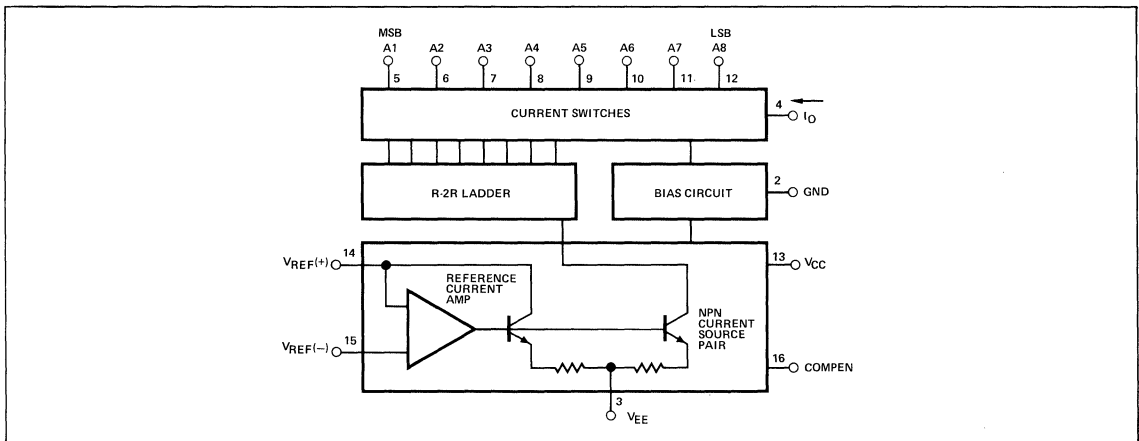
The DAC-1508A/1408A is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building tracking and successive approximation analog-to-digital converters.

For significantly improved speed and applications flexibility your attention is directed to the DAC-08 8-bit high-speed multiplying D/A converter data sheet. For D/A converters, which include precision voltage references on the chip, please refer to the DAC-210 or the DAC-100 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS**

Power Supply Voltage

V_{CC}	+5.5Vdc
V_{EE}	-16.5Vdc
Digital Input Voltage, V_5 through V_{12}	+5.5, 0Vdc
Applied Output Voltage	+0.5, -5.2Vdc
Reference Current, I_{14}	5mA
Power Dissipation (Package Limitation), P_d	
Ceramic Package (or Epoxy B Package)	100mW
Derate above $T_A = +25^\circ\text{C}$	6.7mW/ $^\circ\text{C}$

Derate above $T_A = +100^\circ\text{C}$ for

Epoxy B Package	5.3mW/ $^\circ\text{C}$
Operating Temperature Range, T_A	
DAC-1508A	-55°C to $+125^\circ\text{C}$
DAC-1408A	0°C to $+75^\circ\text{C}$
DICE Junction Temperature (T_j)	-65°C to 150°C
Storage Temperature Range, T_{stg}	-65°C to $+150^\circ\text{C}$
Plastic Package Only	-65°C to $+125^\circ\text{C}$

NOTE: Ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{CC} = +5\text{Vdc}$, $V_{EE} = -15\text{Vdc}$, $V_{REF}/R_{14} = 2\text{mA}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for DAC-1508A-8, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$ for DAC-1408A, unless otherwise noted. All digital inputs at logic high level.

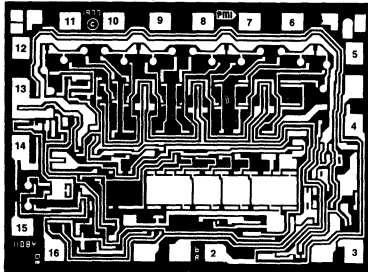
PARAMETER	SYMBOL	CONDITIONS	DAC-1508A/1408A			UNITS
			MIN	TYP	MAX	
Relative Accuracy (error relative to Full-Scale I_O)						
DAC-1508A-B, DAC-1408A-8			—	—	± 0.19	%IFS
DAC-1408A-7	E_r		—	—	± 0.39	
DAC-1408A-6			—	—	± 0.78	
Settling Time to within 1/2 LSB (includes t_{PLH})		t_s	$T_A = +25^\circ\text{C}$, (Note 1)	—	250	—
Propagation Delay Time	t_{PLH} , t_{PHL}	$T_A = +25^\circ\text{C}$, (Note 1)	—	30	100	ns
Output Full-Scale Current Drift	TCI_O		—	± 20	—	ppm/ $^\circ\text{C}$
Digital Input Logic Levels (MSB)						
High Level, Logic "1"	V_{IH}		2	—	—	Vdc
Low Level, Logic "1"	V_{IL}		—	—	0.8	
Digital Input Current (MSB)	I_{IH} I_{IL}	High Level, $V_{IH} = 5.0\text{V}$ Low Level, $V_{IL} = 0.8\text{V}$	— —	0 -0.4	0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	I_{15}		—	-1	-3	μA
Output Current Range	I_{OR}	$V_{EE} = -5\text{V}$ $V_{EE} = -15\text{V}$	0 0	2.0 2.0	2.1 4.2	mA
Output Current	I_O	$V_{REF} = 2.000\text{V}$, $R_{14} = 1000\Omega$	1.9	1.99	2.1	mA
Output Current	$I_{O(min)}$	All bits low	—	0	4	μA
Output Voltage Compliance ($E_r \leq 0.19\%$ at $T_A = +25^\circ\text{C}$)	V_O	$I_{REF} = 1\text{mA}$ $V_{EE} = -5\text{V}$ $V_{EE} = -10\text{V}$	-0.6 -5	— —	+0.5 +0.5	Vdc
Reference Current Slew Rate	SRI_{REF}		—	4	—	mA/ μs
Output Current Power Supply Sensitivity	$PSSI_{O-}$		—	0.5	2.7	$\mu\text{A}/\text{V}$
Power Supply Current	I_{CC} I_{EE}	All bits low	— —	+9 -7.5	+14 -13	mA
Power Supply Voltage	V_{CCR} V_{EER}	$T_A = +25^\circ\text{C}$	+4.5 -4.5	+5 -15	+5.5 -16.5	Vdc
Power Dissipation	P_d	All bits low $V_{EE} = -5\text{Vdc}$ $V_{EE} = -15\text{Vdc}$ All bits high $V_{EE} = -5\text{Vdc}$ $V_{EE} = -15\text{Vdc}$	— — — —	82 157 70 132	135 265 — —	mW

NOTE:

1. Guaranteed by design.



DICE CHARACTERISTICS



DIE SIZE 0.085 × 0.062 Inch, 5270 sq. mils
(2.16 × 1.58 mm, 3.39 sq. mm)

- | | |
|--------------------|--------------------------|
| 1. N.C. | 9. A5 |
| 2. GROUND | 10. A6 |
| 3. V _{EE} | 11. A7 |
| 4. I _O | 12. A8 (LSB) |
| 5. A1 (MSB) | 13. V _{CC} |
| 6. A2 | 14. V _{REF} (+) |
| 7. A3 | 15. V _{REF} (-) |
| 8. A4 | 16. COMP |

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at V₊ = 5V, V₋ = -15V, I_{REF} = 2mA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-1408A-G LIMIT	UNITS
Resolution			8	Bits MIN
Monotonicity			8	Bits MIN
Nonlinearity			±0.19	%FS MAX
Output Voltage Compliance	V _O	Full-Scale Current Change, I _{REF} = 1mA <1/2 LSB V ₋ = -5V V ₋ = -10V	+0.5 -0.6 -5	V MAX V MIN V MIN
Full-Scale Current	I _{FS}	V _{REF} = 2.000V, R ₁₄ , R ₁₅ = 1.000kΩ	2, ±0.1	mA MAX
Zero-Scale Current	I _{ZS}	(All Bits Low)	4	μA MAX
Output Current Range	I _{OR}	V ₋ = -5V V ₋ = -15V	2.1 4.2	mA MAX
Logic "0" Input Level	V _{IL}		0.8	V MAX
Logic "1" Input Level	V _{IH}		2	V MIN
Logic Input Current				
Logic "0"	I _{IL}	Low Level, V _{IL} = -0.8V	±10	μA MAX
Logic "1"	I _{IH}	High Level, V _{IH} = 5V	±10	μA MAX
Reference Bias Current	I ₁₅		-3	μA MAX
Output Current Power Supply Sensitivity	PSSI ₀₋		2.7	μA/V MAX
Power Supply Current	I ₊		+14	mA MAX
(All Bits Low)	I ₋		-13	mA MAX
Power Supply Voltage Range	V _{CCR} V _{EER}		+5, ±0.5 -16.5, -4.5	V MAX/MIN
Power Dissipation				
(All Bits Low)	P _d	V ₋ = 5V V ₋ = -15V	135 265	mW MAX

NOTE:

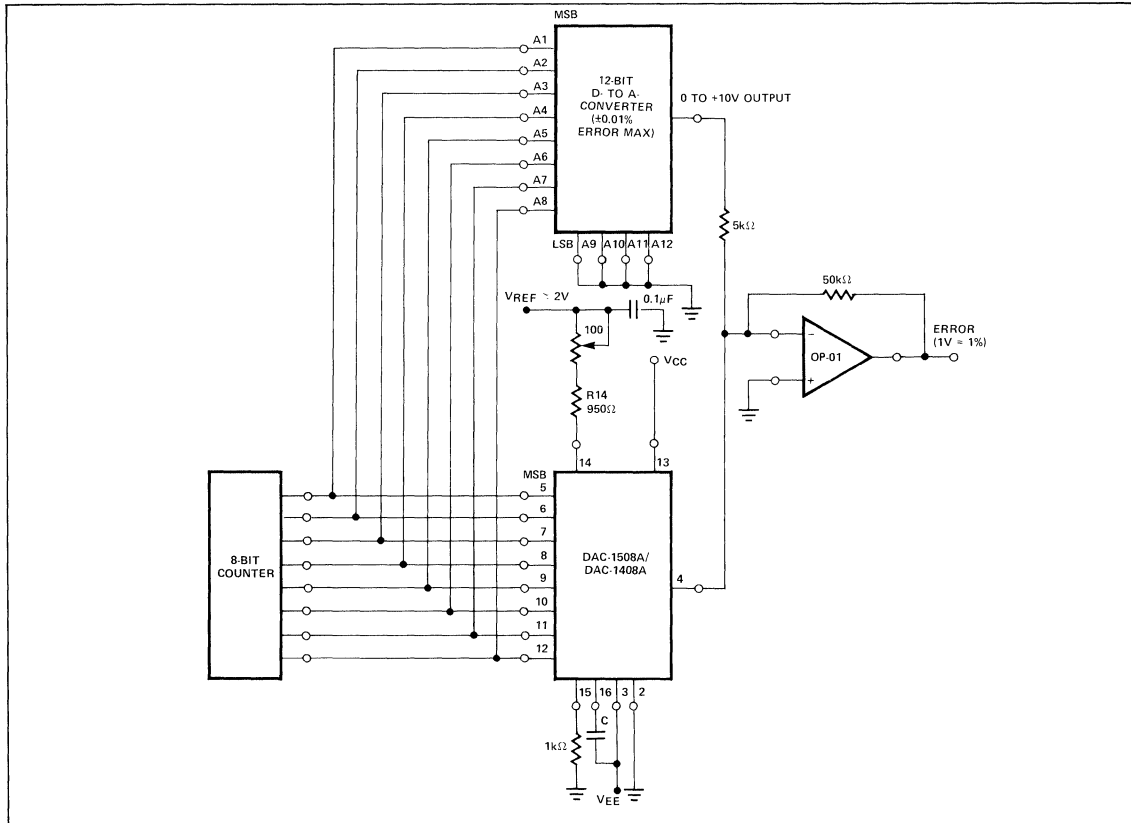
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V₊ = +5V, V₋ = -15V, T_A = 25°C, V_{LC} and I_{OUT} connected to ground, and I_{REF} = 2mA, unless otherwise noted. Output characteristics refer to I_{OUT} only.

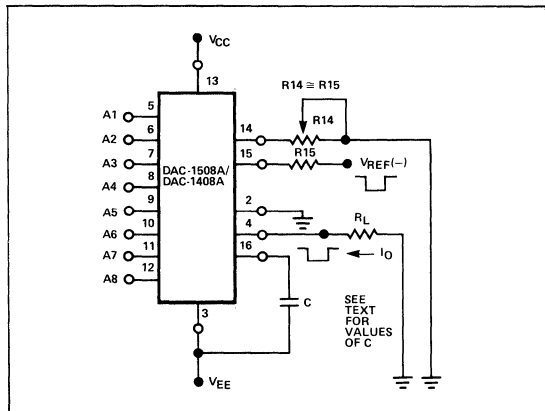
PARAMETER	SYMBOL	CONDITIONS	DAC-1408G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		4	mA/μs
Propagation Delay	t _{PLH} , t _{PHL}	Any Bit	30	ns
Settling Time	t _s	To ±1/2 LSB, All Bits Switched ON or OFF	250	ns

APPLICATIONS

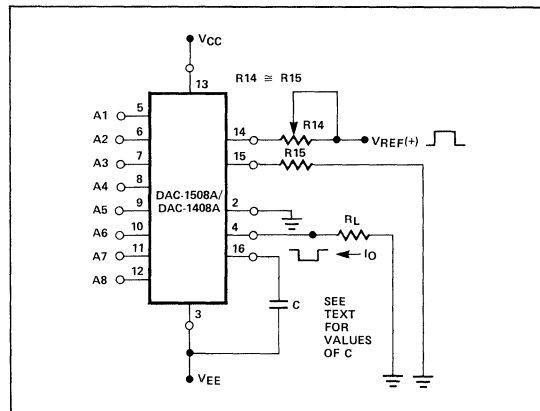
RELATIVE ACCURACY TEST CIRCUIT



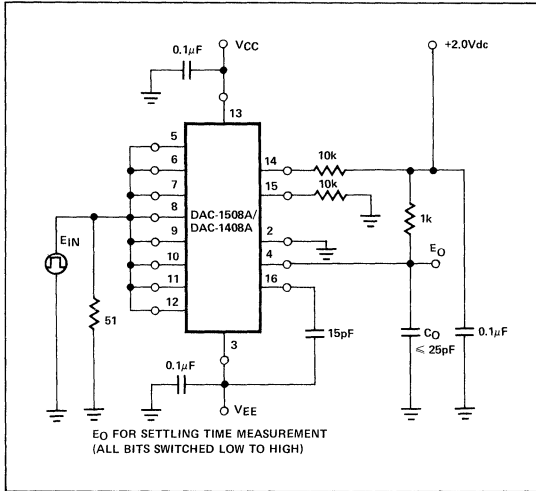
USE WITH NEGATIVE VREF



USE WITH POSITIVE VREF



TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT



Pin 14 regardless of the setup method or reference voltage polarity. Connections for a positive voltage are shown on the preceding page. The reference voltage source supplies the full current I_{14} . For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0k Ω , minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on Pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1 μ F to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

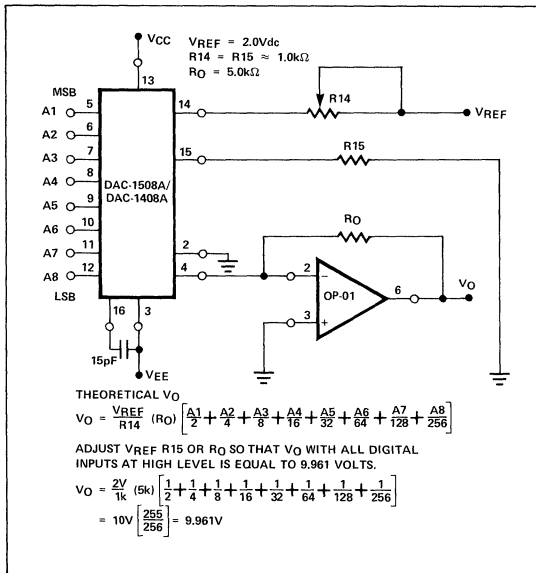
The voltage on Pin 4 is restricted to a range of -0.6V to +0.5V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC-1508A-8.

The negative output voltage compliance of the DAC-1508A-8 is extended to -5.0V where the negative supply voltage is more negative than -10V. Using a full-scale current of 1.992mA and load resistor of 2.5k Ω between Pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980V. The value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 Ω do not significantly affect performance but a 2.5k Ω load increases "worst case" settling time to 1.2 μ s (when all bits are switched on). Refer to the subsequent text section of Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than -7.0V, due to the increased voltage drop across the resistors in the reference current amplifier.

USE WITH CURRENT-TO-VOLTAGE CONVERTING OP AMP



GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at Pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14} , must always flow into

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC-1508A-8 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC-1508A-8 has a very low full-scale current drift with temperature.

The DAC-1508A-8/DAC-1408A series is guaranteed accurate to within $\pm 1/2$ LSB at a full-scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of one LSB ($8.0\mu\text{A}$), which is the ladder remainder shunted to ground. The input current to Pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. Testing relative accuracy is accomplished by the circuit labelled "Relative Accuracy Test Circuit". The 12-bit converter is calibrated for a full-scale output current of 1.992mA. This is an optional step since the DAC-1508A-8 accuracy is essentially the same between 1.5 and 2.5mA. Then the DAC-1508A-8 circuit's full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D/A converters may not be used to construct a 16-bit accuracy D/A converter. 16-bit accuracy implies a total error of $\pm 1/2$ of one part in 65,536, or $\pm 0.00076\%$ which is much more accurate than the $\pm 0.19\%$ specification provided by the DAC-1508A-8.

MULTIPLYING ACCURACY

The DAC-1508A-8 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from $16\mu\text{A}$ to 4.0mA, the additional error contributions are less than $1.6\mu\text{A}$. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC-1508A-8 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a DC reference current is 0.5 to 4.0mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "ON", which corresponds to a low-to-high transition for all bits. This time is typically 250ns for settling to within $\pm 1/2$ LSB, for 8-bit accuracy, and 200ns to $1/2$ LSB for 7 and 6-bit accuracy. The turn off is typically under 100ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25\text{pF}$.

The slowest single switch is the least significant bit. In applications where the D/A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250ns may be realized.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, $100\mu\text{F}$ supply bypassing for low frequencies, and a minimum scope lead length are all mandatory.



DAC-8012

CMOS 12-BIT MULTIPLYING D/A CONVERTER "WITH MEMORY"

Precision Monolithics Inc.

FEATURES

- Data Readback Capability
- 12-Bit Resolution and Linearity
- Low Gain Tempco: 2ppm/°C
- Fast TTL/CMOS Compatible Data Latches
- 3-State Outputs TTL/CMOS Compatible
- Single +5V to +15V Supply
- Small 20-Pin 0.3" DIP
- Low Cost
- Latch-Up Resistant
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION†

PACKAGE: 20-PIN*

RELATIVE ACCURACY	MAXIMUM GAIN ERROR	MILITARY** TEMP.	INDUSTRIAL TEMP.	COMMERCIAL TEMP.
	$T_A = +25^\circ\text{C}$ $V_{DD} = +5\text{V}$	-55°C to +125°C	-25°C to +85°C	0°C to +70°C
±1/2 LSB	±1 LSB	DAC-8012AR	DAC-8012ER	DAC-8012GP
±1 LSB	±3 LSB	DAC-8012BR	DAC-8012FR	DAC-8012HP

* Package Designation:

Suffix R: Hermetic DIP

Suffix P: Plastic DIP

Consult Factory for Dice Information

** For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

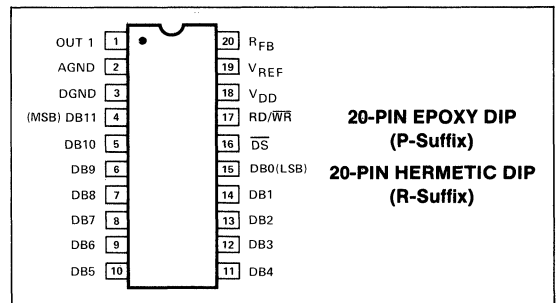
GENERAL DESCRIPTION

The DAC-8012 is a monolithic 12-bit CMOS Multiplying DAC with on-board data latches and three-state output buffers that

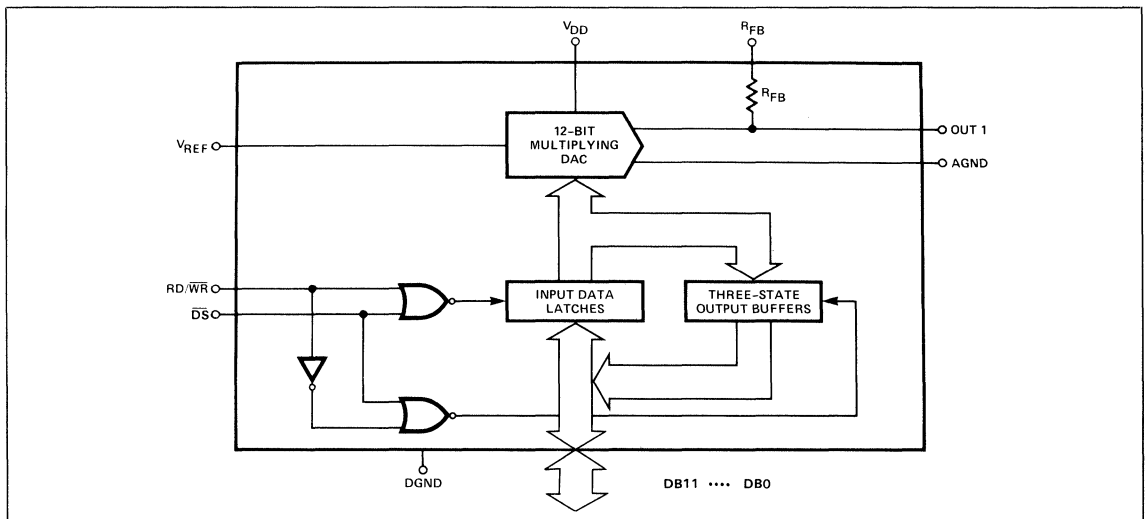
feature "memory" read-write operation. Data is loaded into the latches by a single 12-bit wide word, and can be read back on the same data lines. The DAC-8012 can be directly connected to 12-bit and 16-bit busses.

The readback function makes the DAC-8012 particularly well-suited for applications in automatic test equipment, industrial automation, and other multi-channel microprocessor-controlled systems that require keeping track of the current DAC output data without using an extra memory location for each channel. Low power dissipation and single-supply operation from +5V to +15V makes the DAC-8012 an excellent choice in low-power and remote systems and digital systems with a large number of analog outputs. Four-quadrant multiplying capability and 12-bit linearity allows the DAC-8012 to be used in low-noise, wide-bandwidth, low-distortion, digitally-controlled precision attenuator and filter applications.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM





ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C, unless otherwise noted.)

V _{DD} to DGND	-0.3V, +17V
Digital Input Voltage to DGND	-0.3V, V _{DD}
AGND to DGND	-0.3V, V _{DD}
V _{RFB} , V _{REF} to DGND	±25V
V _{FIN1} to DGND	-0.3V, V _{DD}
Power Dissipation (Any Package) to +75°C	450mW
Derates Above +75°C by	6mW/°C
Operating Temperature Range	
Military (AR, BR) Grades	-55°C to +125°C
Industrial (ER, FR) Grades	-25°C to +85°C
Commercial (GP, HP) Grades	0°C to +70°C
Dice Junction Temperature	+150°C

Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
- The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper anti-static handling procedures.
- Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF} = +10V, V_{O1}/I_{T1} = 0V, AGND = DGND = 0V; T_A = -55°C to +125°C apply for DAC-8012AR/BR, T_A = -25°C to +85°C apply for DAC-8012ER/FR, T_A = 0°C to +70°C apply for DAC-8012GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G			DAC-8012B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY									
Resolution			12	—	—	12	—	—	Bits
Relative Accuracy	INL	T _A = Full Temp. Range	—	—	±1/2	—	—	±1	LSB
Differential Nonlinearity (Note 1)	DNL	T _A = Full Temp. Range	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G _{FSE}	T _A = +25°C T _A = Full Temp. Range	—	—	±1 ±2	—	—	±3 ±4	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature (Notes 4, 5)	TCG _{FS}		—	—	±5	—	—	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV _{DD} (Note 4)	PSR	T _A = +25°C T _A = Full Temp. Range (ΔV _{DD} = ±5%)	—	—	0.002 0.004	—	—	0.002 0.004	%/%
Output Leakage Current at OUT 1	I _{LKG}	T _A = +25°C, RD/WR = DS = 0V, All digital inputs = 0V T _A = Full Temp. Range A/B Versions E/F/G/H Versions	—	—	10 200 25	—	—	10 200 25	nA
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 6, & 7)	t _{pD}	T _A = +25°C (OUT 1 Load = 100Ω, C _{EXT} = 13pF)	—	—	300	—	—	300	ns
Current Settling Time (Notes 4, 7)	t _s	T _A = Full Temp. Range (To 1/2 LSB) I _{OUT1} Load = 100Ω	—	—	1	—	—	1	μs
Glitch Energy (Note 4)	Q	T _A = +25°C T _A = Full Temp. Range V _{REF} = AGND	—	—	400 500	—	—	400 500	nVs
AC Feedthrough at I _{OUT1} (Notes 4, 11)	FT	T _A = Full Temp. Range V _{REF} = ±10V, f = 10kHz	—	—	5	—	—	5	mV _{p-p}
REFERENCE INPUT									
Input Resistance (Pin 19 to GND) (Note 12)	R _{REF}	T _A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF} = +10V$, $V_{OUT1} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8012AR/BR, $T_A = -25^\circ C$ to $+85^\circ C$ apply for DAC-8012ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8012GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G			DAC-8012B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUTS									
Output Capacitance (Note 4) C_{OUT1}	C_{OUT}	$V_{DD} = +5V$ or $+15V$ $T_A = \text{Full Temp. Range}$ DB0-DB11 = 0V, RD/WR = $\overline{DS} = 0V$ DB0-DB11 = V_{DD} , RD/WR = $\overline{DS} = 0V$	—	—	70	—	—	70	pF
			—	—	150	—	—	150	
DIGITAL INPUTS									
Input High Voltage	V_{INH}	$T_A = \text{Full Temp. Range}$	2.4	—	—	2.4	—	—	V
Input Low Voltage	V_{INL}		—	—	0.8	—	—	0.8	
Input Current (Note 8)	I_{IN}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	1	—	—	1	μA
			—	—	10	—	—	10	
Input Capacitance DB0-DB11 RD/WR, \overline{DS} (Note 4)	C_{IN}	$T_A = \text{Full Temp. Range}$	—	—	12	—	—	12	pF
			—	—	6	—	—	6	
DIGITAL OUTPUTS									
Output High Voltage	V_{OH}	$I_O = 400\mu A$	4.0	—	—	4.0	—	—	V
Output Low Voltage	V_{OL}	$I_O = -1.6mA$	—	—	0.4	—	—	0.4	V
Three-State Output Leakage Current			—	—	10	—	—	10	μA
SWITCHING CHARACTERISTICS (Note 9)		See Timing Diagram							
Write to Data Strobe Setup Time	t_{WSU}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
			0	—	—	0	—	—	
Data Strobe to Write Hold Time	t_{WH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
			0	—	—	0	—	—	
Read to Data Strobe Setup Time	t_{RSU}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
			0	—	—	0	—	—	
Data Strobe to Read Hold Time	t_{RH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
			0	—	—	0	—	—	
Write Mode Data Strobe Width	t_{WRS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	180	—	—	180	—	—	ns
			250	—	—	250	—	—	
Read Mode Data Strobe Width	t_{RDS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	220	—	—	220	—	—	ns
			290	—	—	290	—	—	
Data Setup Time	t_{DSU}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	210	—	—	210	—	—	ns
			250	—	—	250	—	—	
Data Hold Time	t_{DH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
			0	—	—	0	—	—	
Data Strobe to Output Valid Time (Note 13)	t_{CO}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	300	—	—	300	ns
			—	—	400	—	—	400	
Output Active Time from Deselection (Note 13)	t_{OTD}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	215	—	—	215	ns
			—	—	375	—	—	375	
POWER SUPPLY									
Supply Current	I_{DD}	$T_A = \text{Full Temp. Range}$ (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	$T_A = \text{Full Temp. Range}$ (All Digital Inputs 0V or V_{DD})	—	10	100	—	10	100	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $V_{OUT1} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8012AR/BR, $T_A = -25^\circ C$ to $+85^\circ C$ apply for DAC-8012ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8012GP/HP, unless otherwise noted.

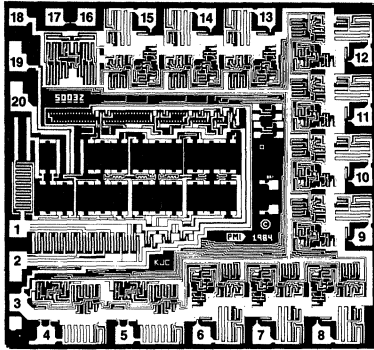
PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G			DAC-8012B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS									
Input High Voltage	V_{INH}	$T_A = \text{Full Temp. Range}$	13.5	—	—	13.5	—	—	V
Input Low Voltage	V_{INL}		—	—	1.5	—	—	1.5	V
Input Current (Note 8)	I_{IN}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	1 10	—	—	1 10	μA
Input Capacitance DB0-DB11 RD/WR, \overline{DS} (Note 4)	C_{IN}	$T_A = \text{Full Temp. Range}$	—	—	12 10	—	—	12 10	pF
DIGITAL OUTPUTS									
Output High Voltage	V_{OH}	$I_O = 3mA$	13.5	—	—	13.5	—	—	V
Output Low Voltage	V_{OL}	$I_O = -3mA$	—	—	1.5	—	—	1.5	V
Three-State Output Leakage Current			—	—	10	—	—	10	μA
SWITCHING CHARACTERISTICS (Note 9)		See Timing Diagram							
Write to Data Strobe Setup Time	t_{WSU}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Data Strobe to Write Hold Time	t_{WH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Read to Data Strobe Setup Time	t_{RSU}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Data Strobe to Read Hold Time	t_{RH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Write Mode Data Strobe Width	t_{WRS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	100 120	—	—	100 120	—	—	ns
Read Mode Data Strobe Width	t_{RDS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	110 150	—	—	110 150	—	—	ns
Data Setup Time	t_{DSU}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	90 120	—	—	90 120	—	—	ns
Data Hold Time	t_{DH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Data Strobe to Output Valid Time (Note 13)	t_{CO}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	— —	—	180 220	— —	—	180 220	ns
Output Active Time for Deselection (Note 13)	t_{OTD}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	— —	—	180 250	— —	—	180 250	ns
POWER SUPPLY									
Supply Current	I_{DD}	$T_A = \text{Full Temp. Range}$ (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	$T_A = \text{Full Temp. Range}$ (All Digital Inputs 0V or V_{DD})	—	10	100	—	10	100	μA

NOTES:

- 12-bit monotonic over full temperature range.
- Includes the effects of 5ppm max. gain T.C.
- Using internal R_{FB} , DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- GUARANTEED but NOT TESTED.
- Typical value is 2ppm/ $^\circ C$ for $V_{DD} = +5V$.
- From digital input change to 90% of final analog output.
- All digital inputs = 0V to V_{DD} ; or V_{DD} to 0V.
- Logic inputs are MOS gates, typical input current (at $+25^\circ C$) is less than 1nA.
- Sample tested at $+25^\circ C$ to ensure compliance.
- Feedthrough can further be reduced by connecting the metal lid on the sidebrazed package (Suffix R) to DGND.
- Resistor T.C. = $+100\text{ppm}/^\circ C$ max.
- $C_L = 100\text{pf}$.



DICE CHARACTERISTICS



DIE SIZE 0.121 × 0.112 inch, 13,552 sq. mils
(3.07 × 2.85 mm, 8.75 sq. mm)

- | | |
|---------------|----------------------|
| 1. OUT 1 | 11. DB4 |
| 2. AGND | 12. DB3 |
| 3. DGND | 13. DB2 |
| 4. DB11 (MSB) | 14. DB1 |
| 5. DB10 | 15. DB0 (LSB) |
| 6. DB9 | 16. DS |
| 7. DB8 | 17. RD/WR |
| 8. DB7 | 18. V _{DD} |
| 9. DB6 | 19. V _{REF} |
| 10. DB5 | 20. R _{FB} |

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at V_{DD} = +5V or +15V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND = 0V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012G	
			LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G _{FSE}	DAC Latches Loaded with 1111 1111 1111	±3	LSB MAX
Output Leakage	I _{LKG}	DAC Latches Loaded with 0000 0000 0000 Pad 1	±10	nA MAX
Input Resistance	R _{REF}	Pad 19	6/15	kΩ MIN/ kΩ MAX
Output High Voltage	V _{OH}	V _{DD} = 5V, I _O = 400μA	4.0	V MIN
Output Low Voltage	V _{OL}	V _{DD} = 5V, I _O = -1.6mA	0.4	V MAX
Digital Input High	V _{INH}	V _{DD} = 5V V _{DD} = 15V	2.4 13.5	V MIN
Digital Input Low	V _{INL}	V _{DD} = 5V V _{DD} = 15V	0.8 1.5	V MAX
Input Current	I _{IN}	V _{IN} = 0V or V _{DD}	±1	μA MAX
Supply Current	I _{DD}	All Digital Inputs V _{INL} or V _{INH} All Digital Inputs 0V or V _{DD}	2 0.1	mA MAX
DC Supply Rejection (ΔGain/ΔV _{DD})	PSRR	V _{DD} = ±5%	0.004	%% MAX

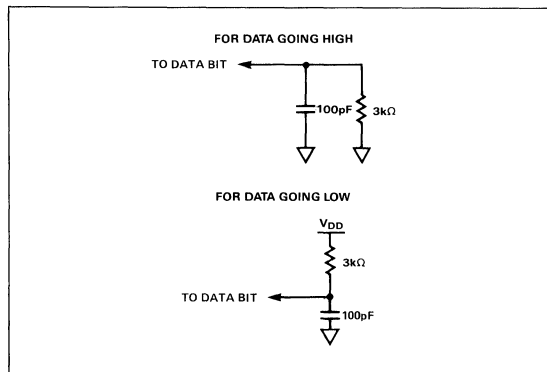
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF} = +10V, V_{OUT1} = 0V; T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012G	
			TYPICAL	UNITS
Digital Input Capacitance	C _{IN}		12	pF
Output Capacitance	C _{OUT1}	DAC Latches Loaded with 0000 0000 0000	70	pF
	C _{OUT1}	DAC Latches Loaded with 1111 1111 1111	150	pF
Propagation Delay	t _{pD}	V _{DD} = 15V V _{DD} = 5V	300	ns

LOAD CIRCUITS FOR SWITCHING TESTS



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

DIFFERENTIAL NONLINEARITY

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of ± 1 LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will not decrease for an increase in digital code applied).

GAIN ERROR

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is V_{REF} minus 1 LSB. The gain error is adjustable to zero using external resistance.

OUTPUT CAPACITANCE

The capacitance from OUT1 to AGND.

PROPAGATION DELAY

This is measured from the digital input change to the analog output current reaching 90% of its final value.

FEEDTHROUGH GLITCH ENERGY

This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with $V_{REF} = AGND$.

LOGIC INFORMATION

D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A Converter section of the DAC-8012, and Figure 2 gives an approximate equivalent switch circuit. R is typically 11k Ω .

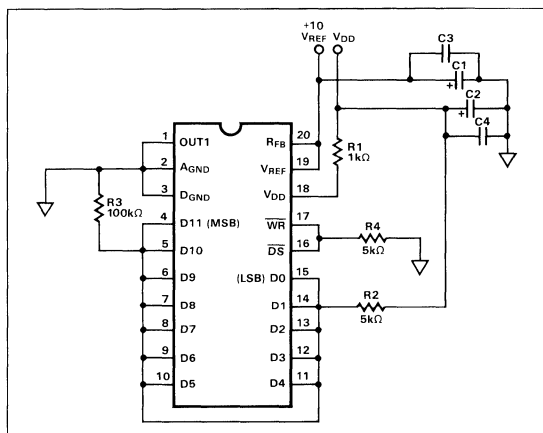
The binary-weighted currents are switched between OUT 1 and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT 1 terminal, $C_{OUT 1}$, is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT 1). One of the current switches is shown in Figure 2.

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristics resistance and is equal to value "R"). Since the input resistance at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} is recommended to define scale factor.)

The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however, when the circuit is not powered up the switch assumes an open state.

BURN-IN CIRCUIT



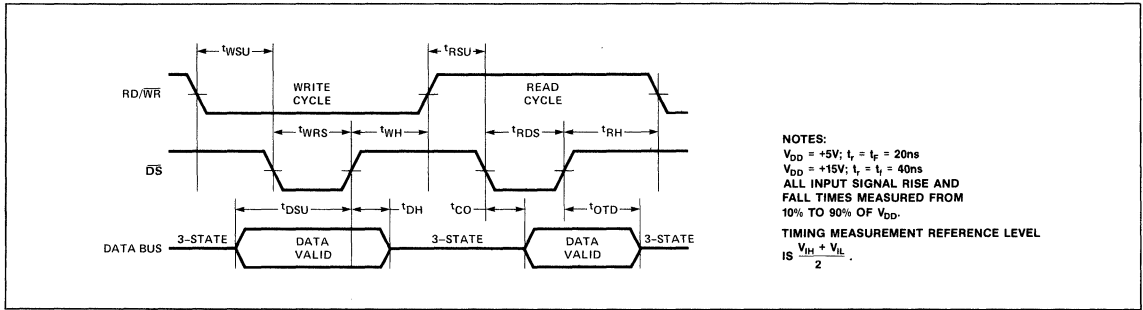
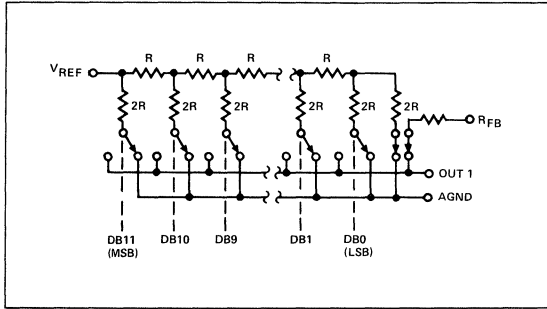
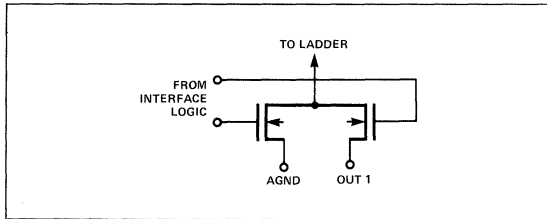
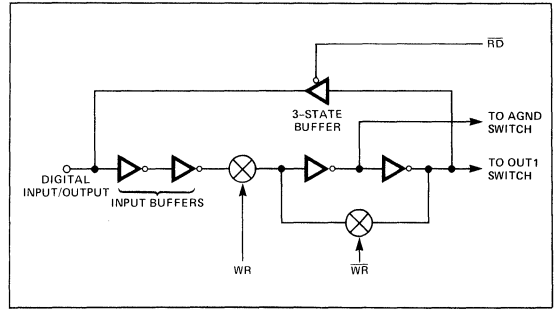
TIMING DIAGRAM

FIGURE 1: Simplified D/A Circuit of DAC-8012

FIGURE 2: N-Channel Current Steering Switch

DIGITAL SECTION

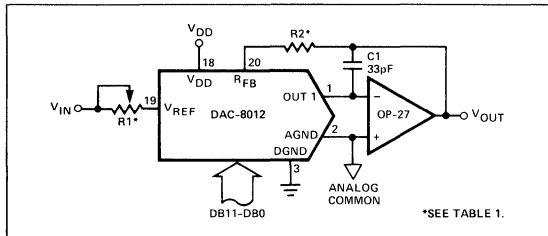
Figure 3 shows the digital I/O structure for one bit. When the data strobe (\overline{DS}) and the $\overline{RD}/\overline{WR}$ lines are held low, data at the digital input is fed through the input buffers and the data latches which control the DAC current output switches are transparent. Data is latched when either \overline{DS} or $\overline{RD}/\overline{WR}$ go high. When the data strobe \overline{DS} is held low and the $\overline{RD}/\overline{WR}$ line is held high, the three-state buffer becomes active and the data from the latches is

FIGURE 3: Digital Input/Output Structure


fed through the three-state buffers to the digital input/output lines. This is known as the Read Cycle, or data readback.

The input buffers are simple CMOS inverters designed such that when the DAC-8012 is operated with $V_{DD} = +5V$, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0V to 3.0V, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and D_{GND}) as is practically possible. The DAC-8012 may be operated with any supply voltage in the range $5V \leq V_{DD} \leq 15V$. With $V_{DD} = +15V$, the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

The three-state output buffers, in the active mode, provide TTL-compatible digital outputs with a fan-out of one TTL load when the DAC-8012 is operated with +5V power supply. When powered from +15V, the output buffers provide output logic levels of 1.5V and 13.5V. Three-state output leakage is typically 10nA.

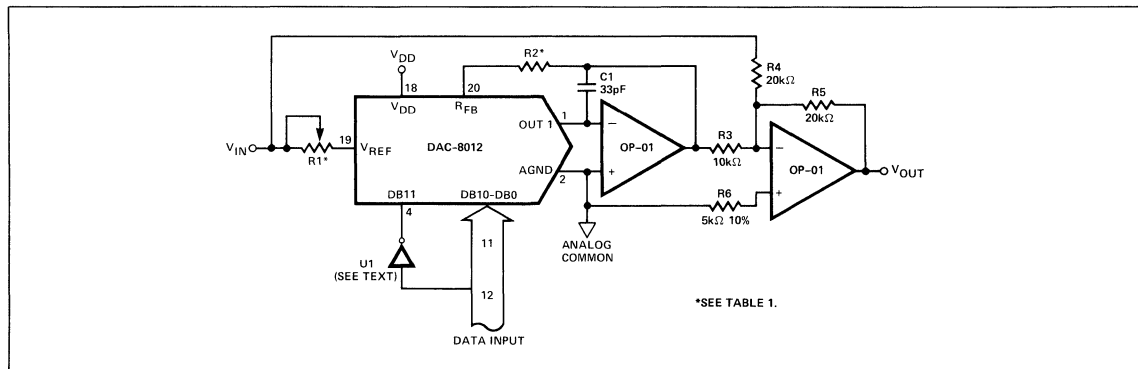
FIGURE 4: Unipolar Binary Operation

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the DAC-8012. Resistor R1 is used to trim for full scale. The following versions: DAC-8012AR, DAC-8012ER, DAC-8012GP, have a guaranteed maximum gain error of ± 1 LSB at $+25^\circ\text{C}$ and $V_{DD} = +5\text{V}$, and in many applications the gain trim resistors are not required. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (the inversion is introduced by the op amp); or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20\text{V} \leq V_{IN} \leq +20\text{V}$ (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD} . Table II shows the code relationship for the circuit of Figure 4.

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code, and inverter U₁ on the MSB line, converts 2's-complement input code to offset binary code. The inverter U₁ may be omitted if the inversion is done in software, using an exclusive OR instruction.

R3, R4 and R5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

FIGURE 5: Bipolar Operation (2's Complement Code)

TABLE I: Recommended Trim Resistor Value vs. Grades

TRIM RESISTOR	HP/FR/BR	GP/ER/AR
R1	100Ω	20Ω
R2	33Ω	6.8Ω

TABLE II: Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN} \cdot \left\{ \begin{matrix} 4095 \\ 4096 \end{matrix} \right\}$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN} \cdot \left\{ \begin{matrix} 2048 \\ 4096 \end{matrix} \right\} = -1/2 V_{IN}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{IN} \cdot \left\{ \begin{matrix} 1 \\ 4096 \end{matrix} \right\}$
0 0 0 0 0 0 0 0 0 0 0 0	0 Volts

TABLE III: 2's Complement Code Table for Circuit of Figure 5

DATA INPUT	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN} \cdot \left\{ \begin{matrix} 2047 \\ 2048 \end{matrix} \right\}$
0 0 0 0 0 0 0 0 0 0 0 1	$+V_{IN} \cdot \left\{ \begin{matrix} 1 \\ 2048 \end{matrix} \right\}$
0 0 0 0 0 0 0 0 0 0 0 0	0 Volts
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN} \cdot \left\{ \begin{matrix} 1 \\ 2048 \end{matrix} \right\}$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN} \cdot \left\{ \begin{matrix} 2048 \\ 2048 \end{matrix} \right\}$

APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is $0.67 V_{OS}$ where V_{OS} is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than 10% of 1 LSB over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the DAC-8012. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

Digital Glitches: When RD/WR and DS are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which RD/WR is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse RD/WR, so that it only occurs when data is valid, will eliminate the problem.

INTERFACING THE DAC-8012 TO MICROPROCESSORS

Figure 6 shows the interface configuration for the 68000 16-bit microprocessor. No external logic is required to write data into the DAC or to readback data from the DAC-8012 latches. Analog circuitry has been removed for clarity.

FIGURE 6: 68000 16-Bit Microprocessor to DAC-8012 Interface

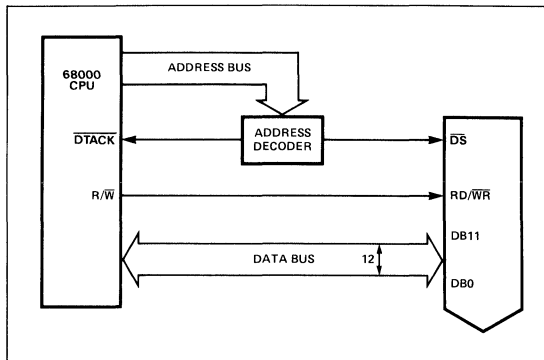
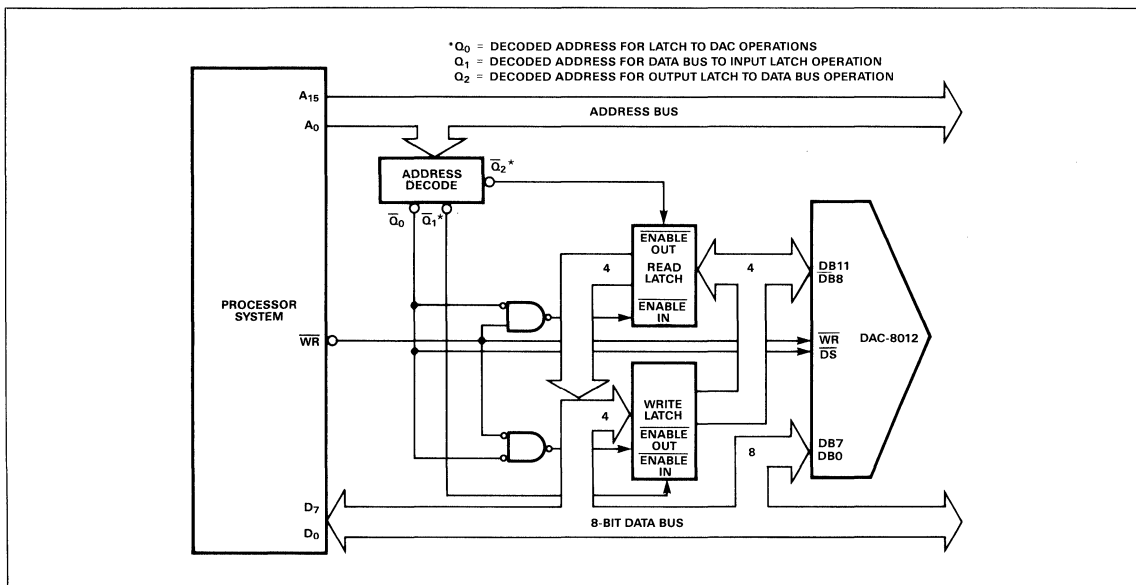


FIGURE 7: 8-Bit Processor to DAC-8012 Interface





DAC-8212

DUAL 12-BIT BUFFERED
MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Direct Parallel Load of All 12 Bits for High Data Throughput
- On Chip Latches for Both DACs
- 12-Bit Endpoint Linearity ($\pm 1/2$ LSB)
- +5V to +15V Single Supply Operation
- DACs Matched to 1%
- Four-Quadrant Multiplication
- Low Power Consumption

APPLICATIONS

- Automatic Test Equipment
- Robotics
- Programmable Instrumentation Equipment
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION†

RELATIVE ACCURACY	GAIN ERROR	PACKAGE: 24-PIN**		
		MILITARY* TEMPERATURE -55°C TO +125°C	INDUSTRIAL TEMPERATURE -25°C TO +85°C	COMMERCIAL TEMPERATURE 0°C TO +70°C
$\pm 1/2$ LSB	± 1 LSB	DAC8212AV	DAC8212EV	DAC8212GP
$\pm 1/2$ LSB	± 6 LSB	DAC8212BV	DAC8212FV	DAC8212HP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

** Package designation: Suffix V: Hermetic Dip; Suffix P: Plastic Dip

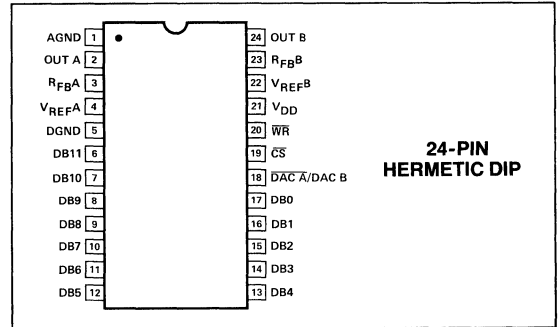
† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

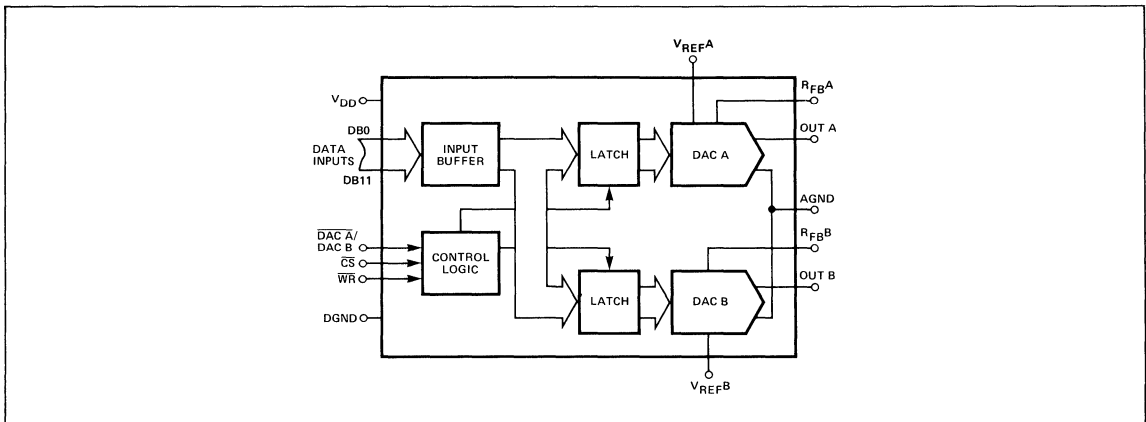
The DAC-8212 contains two 12-bit multiplying digital-to-analog converters. Excellent DAC-to-DAC matching and tracking results from monolithic construction. The DAC-8212 consists of two thin-film R-2R resistor-ladder networks, two 12-bit data latches, one 12-bit input buffer, and control logic. Operation from a +5 or +15 volt single power supply dissipates only 20mW of power.

Digital input data is directed into one of the DAC data latches determined by the DAC selection control line $\overline{\text{DAC A}}/\text{DAC B}$. The data load cycle is similar to the write cycle of a random access memory, activated by the $\overline{\text{WR}}$ and $\overline{\text{CS}}$ control inputs. With $\overline{\text{WR}}$ and $\overline{\text{CS}}$ lines logic low, the input latches are transparent, allowing input digital data to flow directly to the DAC selected by the $\overline{\text{DAC A}}/\text{DAC B}$ select input.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} to AGND	0V, +17V
V _{DD} to DGND	0V, +17V
AGND to DGND	V _{DD}
DGND to AGND	V _{DD}
Digital Input Voltage to DGND	-0.3V, V _{DD} + 0.3
V _{PIN 2} , V _{PIN 24} to AGND	-0.3V, V _{DD} + 0.3
V _{REF A} , V _{REF B} to AGND	±25V
V _{RFB A} , V _{RFB B} to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derate Above +75°C by	6mW/°C
Operating Temperature Range	
AV, BV Versions	-55°C to +125°C
EV, FV Versions	-25°C to +85°C
GP, HP Versions	0°C to +70°C

Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
- The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
- Do not insert this device into powered sockets; remove power before insertion or removal.
- Use proper anti-static handling procedures.
- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF A} = V_{REF B} = +10V, OUT A = OUT B = 0V; T_A = -55°C to +125°C apply for DAC-8212A/BV; T_A = -25°C to +85°C apply for DAC-8212EV/FV; T_A = 0°C to +70°C apply for DAC-8212GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
STATIC ACCURACY							
Specifications apply to both DAC A and DAC B							
Resolution	N		12	—	—	Bits	
Relative Accuracy	NL	Endpoint Linearity Error	—	—	±1/2	LSB	
Differential Nonlinearity	DNL	All Grades are Monotonic	—	—	±1	LSB	
Full Scale Gain Error (Note 1)	G _{FSE}	T _A = +25°C	DAC-8212A/E/G	—	—	±1	LSB
			DAC-8212B/F/H	—	—	±6	
		T _A = Full Temp. Range	DAC-8212A/E/G	—	—	±2	
			DAC-8212B/F/H	—	—	±7	
Output Leakage Current Out A (Pin 2)/Out B (Pin 24)	I _{LKG}	Data In 0000 0000 0000	T _A = +25°C	—	5	±50	nA
			T _A = Full Temp. Range	—	—	±400	
Input Resistance (V _{REF A} , V _{REF B})	R _{REF}			8	—	15	kΩ
V _{REF A} /V _{REF B} (Input Resistance Match)	ΔV _{REF A, B}			—	0.1	±1	%
DIGITAL INPUTS							
Digital Input High	V _{INH}	V _{DD} = +5V	2.4	—	—		V
		V _{DD} = +15V	13.0	—	—		
Digital Input Low	V _{INL}	V _{DD} = +5V	—	—	0.8		V
		V _{DD} = +15V	—	—	1.5		
Input Current	I _{IN}	V _{DBX} = 0V or V _{DD}	T _A = +25°C	—	.001	±1	μA
			T _A = Full Temp. Range	—	—	±10	
Input Capacitance (Note 2)	C _{IN}	DB0–DB11	—	—	10		pF
		WR, CS, DAC A/DAC B	—	—	15		



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8212AV/BV; $T_A = -25^\circ C$ to $+85^\circ C$ apply for DAC-8212EV/FV; $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8212GP/HP, unless otherwise noted. (Continued)

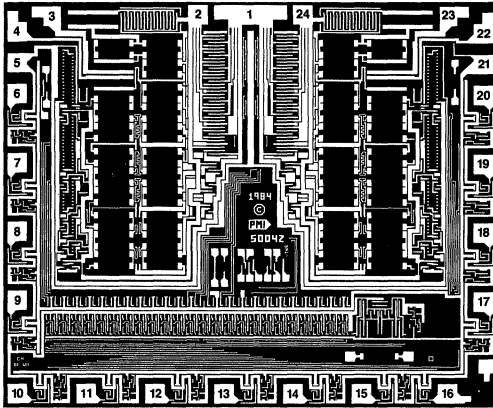
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
SWITCHING CHARACTERISTICS (Notes 2, 3)							
Chip Select to Write Set-Up Time	t_{CS}		230	—	—	ns	
Chip Select to Write Hold Time	t_{CH}		30	—	—	ns	
DAC Select to Write Set-Up Time	t_{AS}		230	—	—	ns	
DAC Select to Write Hold Time	t_{AH}		30	—	—	ns	
DAC Select Set-Up Write Time	t_{DSS}		10	—	—	ns	
Data Valid to Write Set-Up Time	t_{DS}		130	—	—	ns	
Data Valid to Write Hold Time	t_{DH}		0	—	—	ns	
Write Pulse Width	t_{WR}		200	—	—	ns	
POWER SUPPLY							
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	—	—	2	mA	
		All Digital Inputs 0V or V_{DD}	—	—	100	μA	
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSS	$\Delta V_{DD} = \pm 5\%$ $T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	0.02	%/%	
			—	—	0.04	%/%	
AC PERFORMANCE CHARACTERISTICS (Note 2)							
Propagation Delay (Note 4)	t_{pD}	$T_A = +25^\circ C$	—	—	220	ns	
Current Settling Time (Notes 5, 6)	t_s	$T_A = +25^\circ C$	—	—	2	μs	
			$C_{OUT A}$ $C_{OUT B}$	DAC Latches Loaded with 0000 0000 0000	—	—	90
$C_{OUT A}$ $C_{OUT B}$	DAC Latches Loaded with 1111 1111 1111	—	—	120			
AC Feedthrough	FT_A FT_B	$V_{REF A}$ to $OUT A$; $V_{REF A} = 20V_{p-p}$; $f = 100kHz$; $T_A = +25^\circ C$	—	—	-70	dB	
			$V_{REF B}$ to $OUT B$; $V_{REF B} = 20V_{p-p}$; $f = 100kHz$; $T_A = +25^\circ C$	—	—		-70

NOTES:

- Measured using internal $R_{FB A}$ and $R_{FB B}$. Both DAC latches loaded with 1111 1111 1111.
- Guaranteed by design.
- See timing diagram.
- From 50% of digital input to 90% of final analog output current. $V_{REF A} = V_{REF B} = +10V$; $OUT A$, $OUT B$ load = 100Ω , $C_{EXT} = 13pF$.
- WR , $CS = 0V$; $DB0-DB11 = 0V$ to V_{DD} or V_{DD} to $0V$.
- Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale. The output voltage is measured at the output of an external op amp.

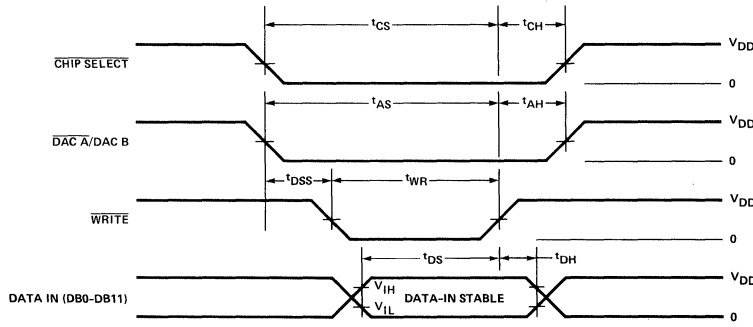


DICE CHARACTERISTICS



DIE SIZE 0.137 × 0.114 inch, 15,168 sq. mils
(3.49 × 2.89 mm, 10.11 sq. mm)

WRITE CYCLE TIMING DIAGRAM



- NOTES:
 1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD} :
 $V_{DD} = +5V, t_r = t_f = 20ns$;
 $V_{DD} = +15V, t_r = t_f = 40ns$.
 2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

APPLICATIONS INFORMATION

Each DAC of the DAC-8212 requires an external op amp for current-to-voltage conversion. Figure 1 shows DAC A connected for a 0 to -10 volt output unipolar operation. Using the internal feedback resistor R_{FBA} results in a correct full-scale output according to the transfer equation:

$$V_{OUT A} = -\frac{D}{4096} \times V_{REF A}$$

where D is a binary number.

V_{REF} may be a DC reference voltage or an AC input signal when used for multiplying applications.

The OUT A and OUT B terminals have full-scale output currents of V_{REF}/R_{REF} . The DAC output voltage should be kept within a tenth of an LSB of full-scale in order to maintain the linearity specification. A simplified circuit of one of the DACs is shown in Figure 2.

Input timing requirements are discussed in the Interface Logic Information section.

FIGURE 1: Circuit Connection for Unipolar Output Voltage

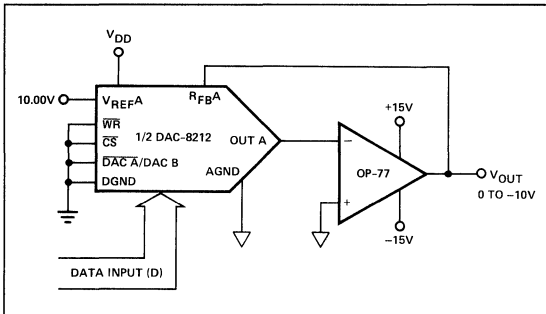
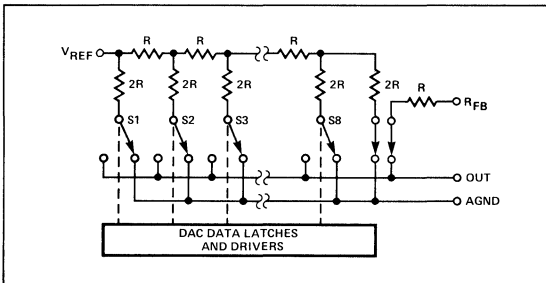


FIGURE 2: Simplified Functional Circuit for DAC A or DAC B



INTERFACE LOGIC INFORMATION

DAC SELECTION

Both DAC latches share a common 12-bit input port. The control input $\overline{DAC A}/\overline{DAC B}$ selects which DAC can accept data from the input port.

MODE SELECTION

The inputs \overline{CS} and \overline{WR} control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When \overline{CS} and \overline{WR} are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data on the data bit lines DB0-DB11.

HOLD MODE

The selected DAC latch retains the data which was present on the data lines just prior to \overline{CS} or \overline{WR} assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

MODE SELECTION TABLE

$\overline{DAC A}/\overline{DAC B}$	\overline{CS}	\overline{WR}	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State

H = High State

X = Don't Care



DAC-8408

QUAD 8-BIT MULTIPLYING CMOS
D/A CONVERTER WITH MEMORY

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Four DACs on a Single Chip
- $\pm 1/4$ LSB End-Point Linearity
- Guaranteed Monotonic
- DACs Matched to Within 1%
- Microprocessor Compatible
- Read/Write Capability (3-State Output)
- On-Board Data Latches
- TTL/CMOS Compatible
- Four-Quadrant Multiplication
- Single Supply Operation (+5V)
- Low Power Consumption
- Ideal for Battery-Operated Equipment
- Latch-Up Resistant

APPLICATIONS

- Automatic Test Equipment
- Systems Requiring Data Access for Self-Diagnostics
- Industrial Automation
- Multi-Channel Microprocessor-Controlled Systems
- Process Control
- Digital Attenuators
- X-Y Graphics

ORDERING INFORMATION†

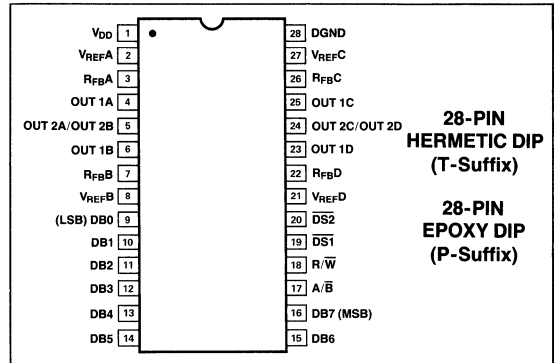
INL	GAIN ERROR	PACKAGE: 28-PIN**		
		COMMERCIAL TEMPERATURE 0°C to +70°C	INDUSTRIAL TEMPERATURE -25°C to +85°C	MILITARY* TEMPERATURE -55°C to +125°C
$\pm 1/4$	± 1 LSB	DAC8408GP	DAC8408ET	DAC8408AT

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

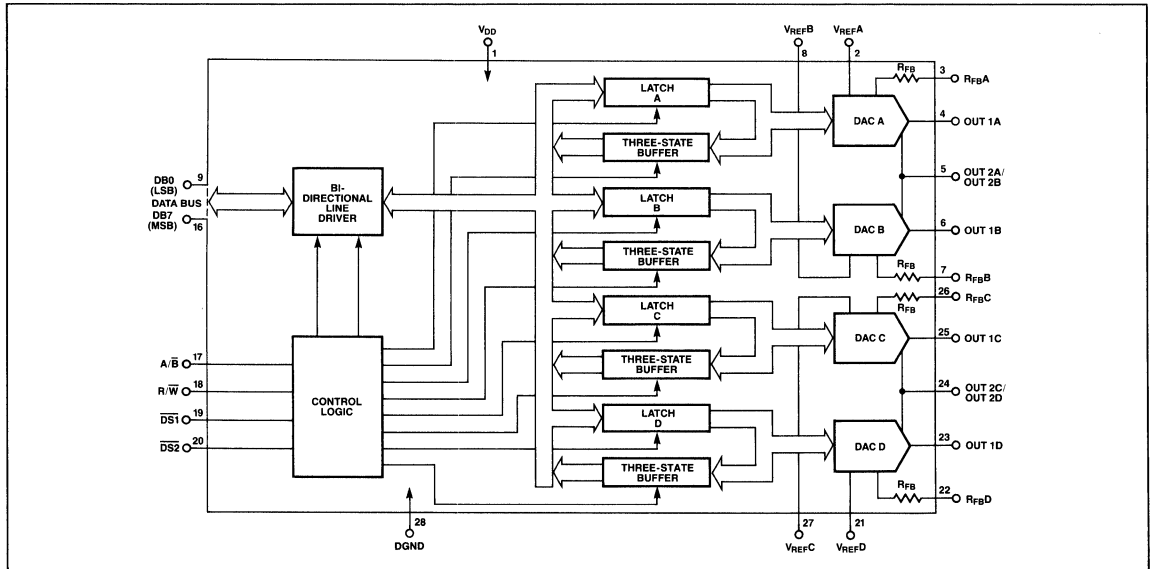
** Package Designation: Suffix T: Hermetic DIP; Suffix P: Plastic Dip.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



GENERAL DESCRIPTION

The DAC-8408 is a quad 8-bit multiplying digital-to-analog CMOS converter. Each DAC has its own reference input, feedback resistor, and on-board data latches that feature read/write capability. The readback function serves as memory for those systems requiring self-diagnostics.

A common 8-bit TTL/CMOS compatible input port is used to load data into any of the four DAC data-latches. Control lines $\overline{DS1}$, $\overline{DS2}$, and A/B determine which DAC will accept data. Data loading is similar to that of a RAM's write cycle. Data can be read back onto the same data bus with control line R/W. The DAC-8408 is bus compatible with most 8-bit microprocessors including the 6800, 8080, 8085, and Z80. The DAC-8408 operates on a single +5 volt supply and dissipates less than 20mW.

ABSOLUTE MAXIMUM RATINGS

($T_A = +25^\circ\text{C}$ unless otherwise noted.)

V_{DD} to OUT 2A, OUT 2B, OUT 2C, OUT 2D	0, +7V
V_{DD} to DGND	0, +7V
OUT 1A, OUT 1B,	
OUT 1C, OUT 1D to DGND	-0.3V to $V_{DD} + 0.3V$
OUT 2A, OUT 2B,	
OUT 2C, OUT 2D to DGND	-0.3V to $V_{DD} + 0.3V$

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = \pm 10V$; $V_{OUTA,B,C,D} = 0V$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for DAC-8408AT; $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ apply for DAC-8408ET; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for DAC-8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D.

PARAMETER	SYMBOL	CONDITIONS	DAC-8408A/E/G			UNITS
			MIN	TYP	MAX	
STATIC ACCURACY						
Resolution	N		8	—	—	Bits
Nonlinearity	INL	(Note 1)	—	—	$\pm 1/4$	LSB
Differential Nonlinearity	DNL	(Note 2)	—	—	$\pm 1/2$	LSB
Gain Error	G_{FSE}	(Using Internal R_{FB})	—	—	± 1	LSB
Gain Error Tempco (Note 3)	TC_{GFS}		—	2	—	ppm/ $^\circ\text{C}$
Power Supply Rejection ($\Delta V_{DD} = \pm 10\%$)	PSR	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	—	—	0.001 0.002	%FSR/%
Output Leakage Current	I_{LKG}	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	—	—	± 30 ± 60	nA
REFERENCE INPUT						
Input Voltage Range			—	—	± 20	V
Input Resistance Match (Note 4)		$R_{A/B/C/D}$	—	—	± 1	%
Input Resistance	R_{IN}		6	10	14	k Ω
DIGITAL INPUTS (Note 5)						
Digital Input Low	V_{IL}		—	—	0.8	V
Digital Input High	V_{IH}		2.4	—	—	
Input Leakage Current	I_{LKG}	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	—	—	± 1.0 ± 10.0	μA
Input Capacitance	C_{IN}	(Note 6)	—	—	8	pF

DB0 through DB7 to DGND	-0.3V to $V_{DD} + 0.3V$
Control Logic Input Voltage to DGND	-0.3V to $+V_{DD} + 0.3V$
V_{REFA} , V_{REFB} , V_{REFC} , V_{REFD} to	
OUT 2A, OUT 2B, OUT 2C, OUT 2D	$\pm 25V$
Power Dissipation (any package) to $+75^\circ\text{C}$	450mW
Derates Above $+75^\circ\text{C}$ by	6mW/ $^\circ\text{C}$
Operating Temperature Range	
Commercial Grade (GP)	0°C to $+70^\circ\text{C}$
Industrial Grade (ET)	-25°C to $+85^\circ\text{C}$
Military Grade (AT)	-55°C to $+125^\circ\text{C}$
Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$

CAUTION:

- Do not apply voltages higher than $V_{DD} + 0.3V$ or less than $-0.3V$ potential on any terminal except V_{REF} and R_{FB} .
- The digital control inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep in conductive foam at all times until ready to use.
- Use proper anti-static handling procedures.
- Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = \pm 10V$; $V_{OUTA,B,C,D} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8408AT; $T_A = -25^\circ C$ to $+85^\circ C$ apply for DAC-8408ET; $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D. (Continued)

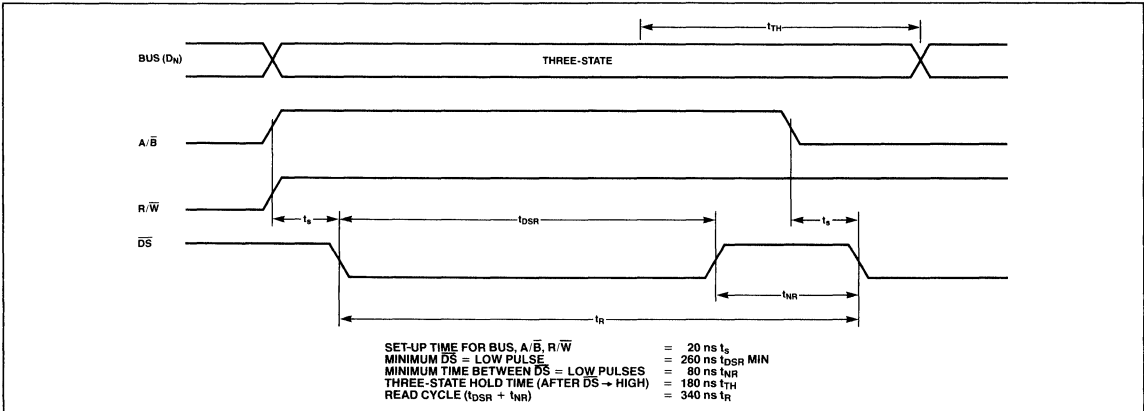
PARAMETER	SYMBOL	CONDITIONS	DAC-8408A/E/G			UNITS
			MIN	TYP	MAX	
DATA BUS OUTPUTS						
Digital Output Low	V_{OL}	1.6mA Sink	—	—	0.4	V
Digital Output High	V_{OH}	400 μ A Source	4	—	—	
Output Leakage Current	I_{LKG}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	± 1.0 ± 10.0	μA
DAC OUTPUTS						
Propagation Delay	t_{pD}	(Notes 7, 11)	—	150	170	ns
Settling Time (Notes 12, 13)	t_s		—	190	245	ns
Output Capacitance	C_{OUT}	DAC Latches All "0"s DAC Latches All "1"s"	—	—	30 50	pF
AC Feedthrough	FT	(20 V_{p-p} (ω : F = 100kHz)	—	—	-55	dB
SWITCHING CHARACTERISTICS (Notes 6, 10)						
Data Write Time	t_W	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	260 350	—	—	ns
Write Strobe	t_{DSW}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	180 250	—	—	ns
Data Hold Time	t_{DHD}		0	—	—	ns
Data Read Time	t_R	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	340 460	—	—	ns
Three-State Hold Time	t_{TH}	$T_A = 25^\circ C$ $T_A = \text{Full Temp. Range}$	180 250	—	—	ns
Read Strobe	t_{DSR}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	260 350	—	—	ns
POWER SUPPLY						
Voltage Range	V_{DD}		4.5	—	5.5	V
Supply Current	I_{DD}	(Note 8)	—	—	50	μA
Supply Current (Note 9)	I_{DD}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	500 1.0	μA mA

NOTES:

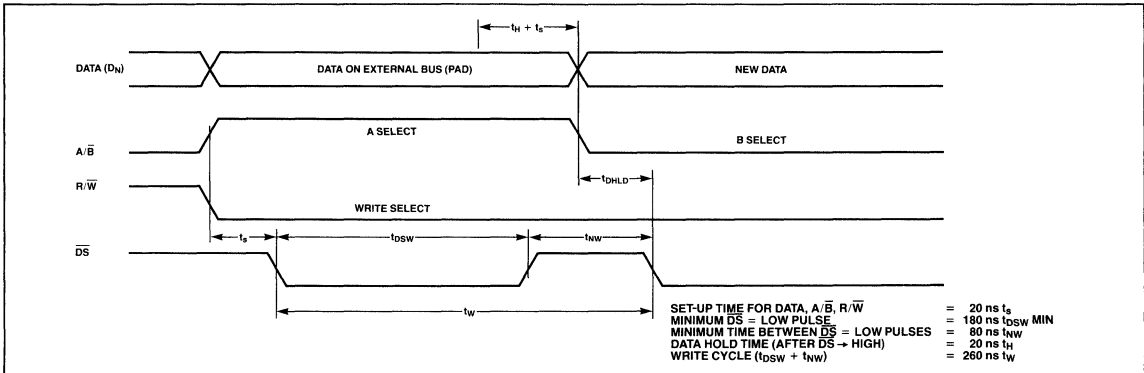
1. This is an end-point linearity specification.
2. All grades guaranteed to be monotonic over the full operating temperature range.
3. ppm/ $^\circ C$ of FSR (FSR = Full Scale Range).
4. Input Resistance Temperature Coefficient = +300ppm/ $^\circ C$.
5. Logic Inputs are MOS gates. Typical input current at $+25^\circ C$ is less than 1nA.
6. Guaranteed by design.
7. From Digital Input to 90% of final analog output current.
8. All Digital Inputs "0" or V_{DD} .
9. All Digital Inputs V_{IH} or V_{IL} .
10. See Timing Diagram.
11. These characteristics are for design guidance only and are not subject to test.
12. Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
13. Extrapolated: t_s (1/2 LSB) = $t_{pD} + 6.2\tau$, where τ = the measured first time constant of the final RC decay.



TIMING DIAGRAM READ CYCLE



TIMING DIAGRAM WRITE CYCLE



MODE SELECTION TABLE

DS1	DS2	A/B	R/W	DAC A	DAC B	DAC C	DAC D
H	H	X	X	HOLD	HOLD	HOLD	HOLD
L	H	H	L	WRITE	HOLD	HOLD	HOLD
L	L	H	L	WRITE	HOLD	WRITE	HOLD
L	H	H	H	READ	HOLD	HOLD	HOLD
L	L	H	H	HOLD	HOLD	HOLD	HOLD
L	H	L	L	HOLD	WRITE	HOLD	HOLD
L	L	L	L	HOLD	WRITE	HOLD	WRITE
L	H	L	H	HOLD	READ	HOLD	HOLD
L	L	L	H	HOLD	HOLD	HOLD	HOLD
H	L	H	L	HOLD	HOLD	WRITE	HOLD
H	L	H	H	HOLD	HOLD	READ	HOLD
H	L	L	L	HOLD	HOLD	HOLD	WRITE
H	L	L	H	HOLD	HOLD	HOLD	READ

L = Low State H = High State X = Irrelevant



PM-562

12-BIT MULTIPLYING CURRENT-OUTPUT D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- Nonlinearity $\pm 1/4$ LSB (Max)
- Settling Time $1.5 \mu\text{s}$ (Typ)
- No Laser Trimming Used in Fabrication
- Internal Range and Offset Scaling Resistors
- Guaranteed Monotonicity Over Temperature
- TTL or CMOS Logic Input Compatibility, Pin Selectable
- Low Power Consumption 130mW (Typ)
- Directly Pin Compatible with AD562

ORDERING INFORMATION†

NONLINEARITY @25°C (LSB)	PMI MODEL NO.	TEMP. RANGE
$\pm 1/4$	PM562AV*	-55°C/+125°C
$\pm 1/2$	PM562BV*	-55°C/+125°C
$\pm 1/2$	PM562FV	-25°C/+85°C
$\pm 1/4$	PM562GV	0°C/+70°C
$\pm 1/2$	PM562HV	0°C/+70°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1984 Data Book, Section 2.

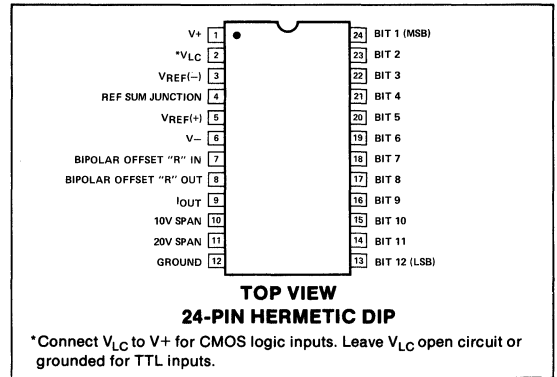
GENERAL DESCRIPTION

The PM-562 is a 12-bit monolithic multiplying digital-to-analog converter consisting of a reference current amplifier, an R-2R ladder network, range and offset scaling resistors, and 12 high-speed current switches. Improvements provided by the PM-562 include greater negative power supply range

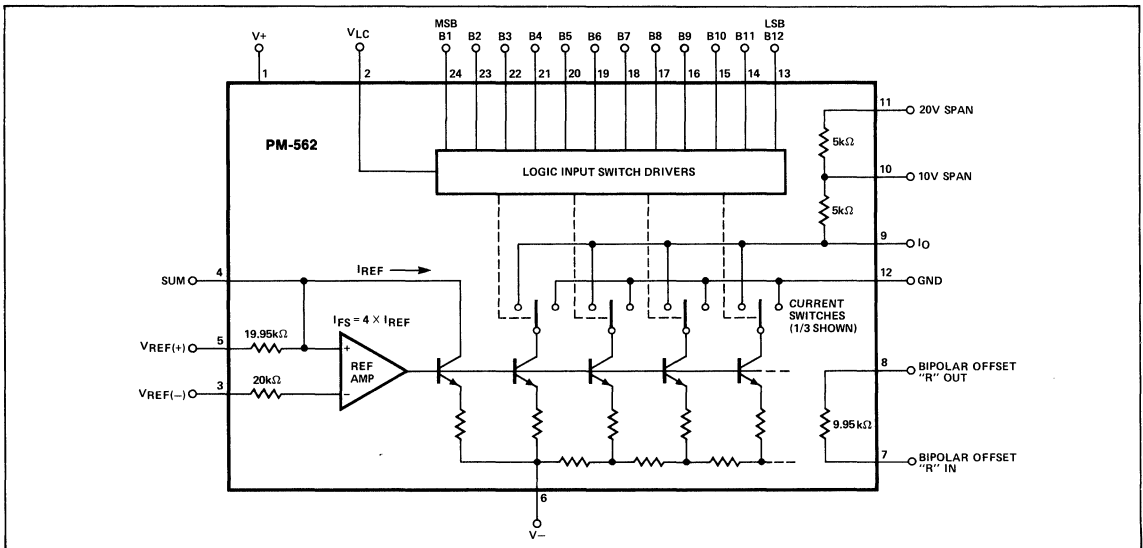
and increased output resistance. The PM-562 is pin compatible with the AD562.

A highly stable trim method; selective shorting of zener diodes, provides 13-bit accuracy without the need for laser trimming. Reliability of this trimming method has been proven in several other PMI products with many years of reliability history. Internal scaling resistors plus an external op amp simplifies construction in voltage output applications, while maintaining accuracy over wide operating temperature ranges. The PM-562 is recommended for 12-bit accuracy D/A applications where single-chip reliability, small size and low cost are primary considerations.

PIN CONNECTIONS



EQUIVALENT CIRCUIT



Manufactured under the following patent: 4,055,773.



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
PM-562A/B	-55° C to +125° C
PM-562F	-25° C to +85° C
PM-562G/H	0° C to +70° C
Storage Temperature Range	-65° C to +150° C
Power Dissipation at T _A = 125° C	1000mW
Lead Temperature (Soldering, 60 sec)	300° C

Supply Voltage (V ₊)	+18V
Supply Voltage (V ₋)	-18V
V ₊ to V ₋	36V
Logic Inputs	V ₋ to (V ₋ plus 36V)
Summing Junction (Pin 4)	V ₋ to V ₊
CMOS/TTL Threshold (Pin 2)	V ₋ to V ₊
I _{OUT} (Pin 9)	-5V to +18V
Span Resistors	36V

ELECTRICAL CHARACTERISTICS at V₊ = 5V, V₋ = -15V, V_{REF} (+) = +10.0000V, V_{REF} (-) = 0V, T_A = +25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562A/G			PM-562B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution	N	T _A = Full Range	12	—	—	12	—	—	Bits
Monotonicity		T _A = Full Range	12	—	—	12	—	—	Bits
Nonlinearity	NL		—	—	±1/4	—	—	±1/2	LSB
Differential Nonlinearity	DNL		—	—	±1/2	—	—	±1/2	LSB
Settling Time	t _S	To ±1/2 LSB, all bits ON or OFF	—	1.5	—	—	1.5	—	μs
Output Voltage Compliance	V _{OC}		—	+10/-1.5	—	—	+10/-1.5	—	V
Full-Scale Output Current Range	I _{FR}	V _{REF} (+) = +10.0000V R ₂ = 50Ω	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Zero-Scale Current	I _{ZS}	All bits OFF	—	.005	0.05	—	.005	0.05	%FS
Output Resistance	R _O		—	2	—	—	2	—	MΩ
Output Capacitance	C _O		—	30	—	—	30	—	pF
Reference Input Impedance	Z _{IN}	Pin 5	—	20	—	—	20	—	kΩ
Gain Error	I _{FSE}	R ₂ = 50Ω, (Note 1)	—	±0.2	—	—	±0.2	—	%FS
Bipolar Zero-Scale Error	I _{BZSE}	R ₁ = 50Ω, (Note 1)	—	±0.1	—	—	±0.1	—	%FS
Full-Scale Gain Adjustment Range	ΔI _{FSR}	R ₂ = 100Ω Trimpot, (Note 1)	—	±0.25	—	—	±0.25	—	%FS
Bipolar Zero-Scale Adjustment Range	ΔI _{BZSR}	R ₁ = 100Ω Trimpot, (Note 1)	—	±0.25	—	—	±0.25	—	%FS
Power Supply Gain Sensitivity	+P _{SS} -P _{SS}	V ₊ = 5V or V ₊ = 15V V ₋ = -15V	—	—	2 6	—	—	2 6	ppmFS/%
Supply Current	I ₊ I ₋	V ₊ = 4.75V to 15.8V V ₋ = -15V ± 10%	—	5 -7	18 -25	—	5 -7	18 -25	mA
TTL Logic Input Voltage	V _{IH} V _{IL}	Pin 2 Open Circuit	I _{IH} = 100nA I _{IL} = -100μA	2.0	—	—	2.0	—	—
CMOS Voltage Logic Input	V _{IH} V _{IL}	Pin 2 tied to Pin 1	I _{IH} = 100nA I _{IL} = -100μA	70	—	—	70	—	—
				—	—	30	—	—	30



ELECTRICAL CHARACTERISTICS at $V_+ = 5V$, $V_- = -15V$, $V_{REF(+)} = +10.0000V$, $V_{REF(-)} = 0V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for PM-562A/B, $-25^\circ C \leq T_A \leq +85^\circ C$ for PM-562F, $0^\circ C \leq T_A \leq +70^\circ C$ for PM-562G/H, unless otherwise noted.

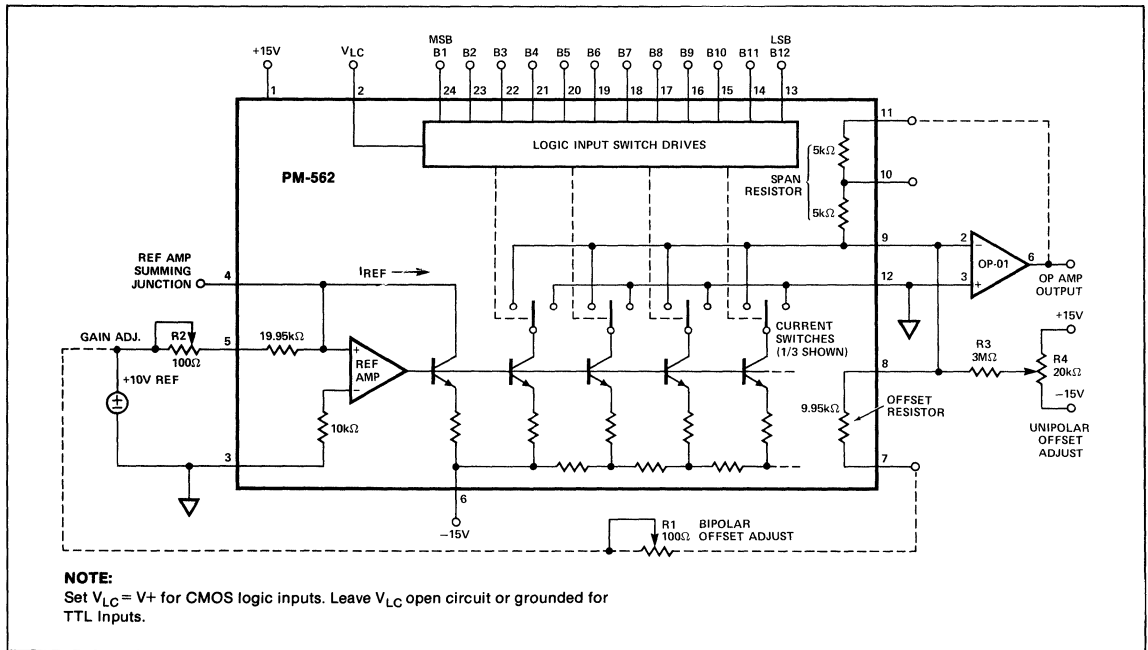
PARAMETER	SYMBOL	CONDITIONS	PM-562A/G			PM-562B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Zero-Scale Temperature Coefficient	$TC_{I_{ZS}}$	Unipolar Leakage Current Change (Note 2)	—	—	2	—	—	2	ppmFS/°C
Bipolar Zero-Scale Temperature Coefficient	$TC_{I_{BZS}}$	Bipolar (Note 2)	—	—	4	—	—	4	ppmFS/°C
Full-Scale Gain Temperature Coefficient	$TC_{I_{FS}}$	Excludes V_{REF} (Note 2)	—	—	5	—	—	5	ppmFS/°C
Differential Nonlinearity Temperature Coefficient	TC_{DNL}	(Note 2)	—	1	—	—	2	—	ppmFS/°C

NOTES:

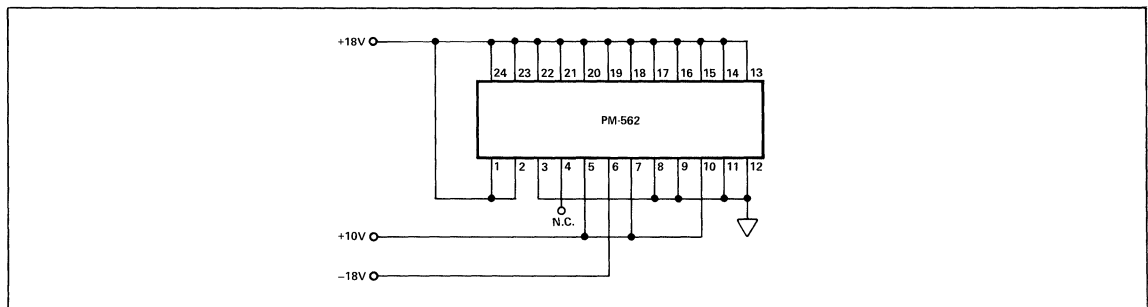
1. See connection diagram.

2. Guaranteed by design.

CONNECTION DIAGRAM

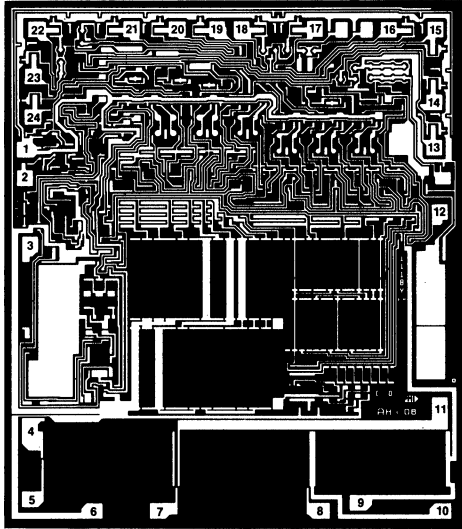


BURN-IN CONFIGURATION





DICE CHARACTERISTICS



DIE SIZE 0.141 × 0.162 Inch, 22842 sq. mils
(3.581 × 4.115 mm, 14.737 sq. mm)

- | | |
|---------------------------|------------------|
| 1. V+ | 13. BIT 12 (LSB) |
| 2. V _{LC} | 14. BIT 11 |
| 3. V _{REF} (-) | 15. BIT 10 |
| 4. REF SUM JUNCTION | 16. BIT 9 |
| 5. V _{REF} (+) | 17. BIT 8 |
| 6. V- | 18. BIT 7 |
| 7. BIPOLAR OFFSET "R" IN | 19. BIT 6 |
| 8. BIPOLAR OFFSET "R" OUT | 20. BIT 5 |
| 9. I _{OUT} | 21. BIT 4 |
| 10. 10V SPAN | 22. BIT 3 |
| 11. 20V SPAN | 23. BIT 2 |
| 12. GROUND | 24. BIT 1 (MSB) |

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at V+ = 5V, V- = -15V, V_{REF} = 10.0000V, T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562G LIMITS	UNITS
Nonlinearity	NL		±1/2	LSB
Differential Nonlinearity	DNL		±1/2	LSB
Zero-Scale Current	I _{ZS}	All Bits OFF	0.05	%FS
Full-Scale Output Current Range	I _{FR}	I _{REF} = 0.5mA Unipolar	-1.6/-2.4	mA
Logic Input High	V _{IH}	I _{IH} = 100nA	2	V
Logic Input Low	V _{IL}	I _{IL} = -100µA	0.8	V
Positive Supply Current	I+	V+ = 4.75 to 15.8V	18	mA
Negative Supply Current	I-	V- = -13.5 to -16.5V	-25	mA

NOTE: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications bases on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 5V, V- = -15V, V_{REF} = 10.0000V, T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562G TYPICAL	UNITS
Settling Time	t _S	to ±1/2 LSB, V _O = 0V	1.5	µs
Full-Scale Gain Temperature Coefficient	TCI _{FS}	Excludes V _{REF}	5	ppmFS/°C
Output Voltage Compliance	V _{OC}		-1.5/+10	V
Output Resistance	R _O		2	MΩ
Output Capacitance	C _O		30	pF
Power Supply Gain Sensitivity	+P _{SS}	V+ = +5V or +15V	2	ppmFS/%
Power Supply Gain Sensitivity	-P _{SS}	V- = -15V	6	ppmFS/%

APPLICATIONS INFORMATION

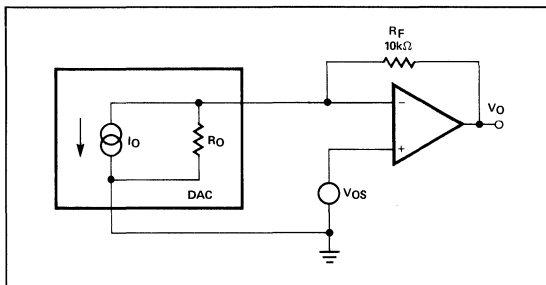
R_O EFFECT ON ACCURACY

The D/A converter equivalent circuit and output voltage equations show that a low output resistance (R_O) can provide a significant error term due to V_{OS} drift of the output amplifier. Note that the higher R_O (2MΩ) offered by the PM-562 gives an apparent V_{OS} drift that is one-half as large as that resulting from the 6.6kΩ R_O of the standard AD562 when using a 10kΩ span resistor (R_F).

$$\Delta V_O = \Delta I_O R_F + \Delta V_{OS}$$

Since: $\Delta I_O = \Delta V_{OS} / R_O$

Then: $\Delta V_O = \Delta V_{OS} (R_F / R_O + 1)$



LAYOUT SUGGESTIONS

Good layout practice appropriate for a 12-bit resolution analog system provides the overriding guideline. Power supplies should have small high frequency noise content. The V₋ (-15V) supply should be the cleanest since it has the most direct effect on I_{OUT}. The PM-562 should have bypass capacitors on both V₊ and V₋ supplies. A tantalum or electrolytic 1 to 10 micro Farad in parallel with a ceramic 0.01 micro Farad bypass capacitor adequately attenuate high frequency supply noise.

The ground line between Pin-3 and Pin-12 should not conduct any other current paths. Placing the common ground point at Pin-12 provides good results. Pin-9 is the most sensitive node to high frequency noise pickup. Keep the signal path between Pin-9 and the current-to-voltage converter (op amp or resistor) as short as possible.

LOGIC INTERFACING (TTL OR CMOS)

The PM-562 digital inputs (BIT 1 through BIT 12) can be programmed by the V_{LC} (Pin-2) for TTL or CMOS logic input compatibility.

For TTL input compatibility leave Pin-2 open circuit or ground it to Pin-12. The logic threshold trip point stays at 1.4V for V₊ set anywhere from 4.75 to 15.8V.

For CMOS input compatibility tie V_{LC} (Pin-2) to V₊. This establishes the CMOS Logic threshold trip point at 1/2 of V₊. Therefore V₊ should be set to the same V_{DD} voltage used by the CMOS driving logic.

MULTIPLYING MODE

The output current of the PM-562 is the product of the reference voltage input and the number represented by the digital input code divided by 4096. The reference voltage V_{REF (+)} must be positive with respect to V_{REF (-)}. The PM-562 typically maintains 12-bit linearity with reference voltages as small as one volt. Reference signal feedthrough is typically 60dB down at 10kHz with a digital input of zero. The DAC output typically takes 20 microseconds to settle to within 1/2 LSB for a 5 volt step on the reference input. The small signal bandwidth for a 100mVpp reference input signal is typically 65kHz, and the typical large signal bandwidth for a 5Vpp reference input signal is 20kHz.

UNIPOLAR OPERATION (0 to +10V OUTPUT)

Figure 1 shows the simplest unipolar setup for 0 to +10V operation. The output should be buffered since the output resistance is 5kΩ. The digital input code is complemented in this configuration. That is, binary "0" in produces +10V full-scale out. And all binary one's in produces 0V out.

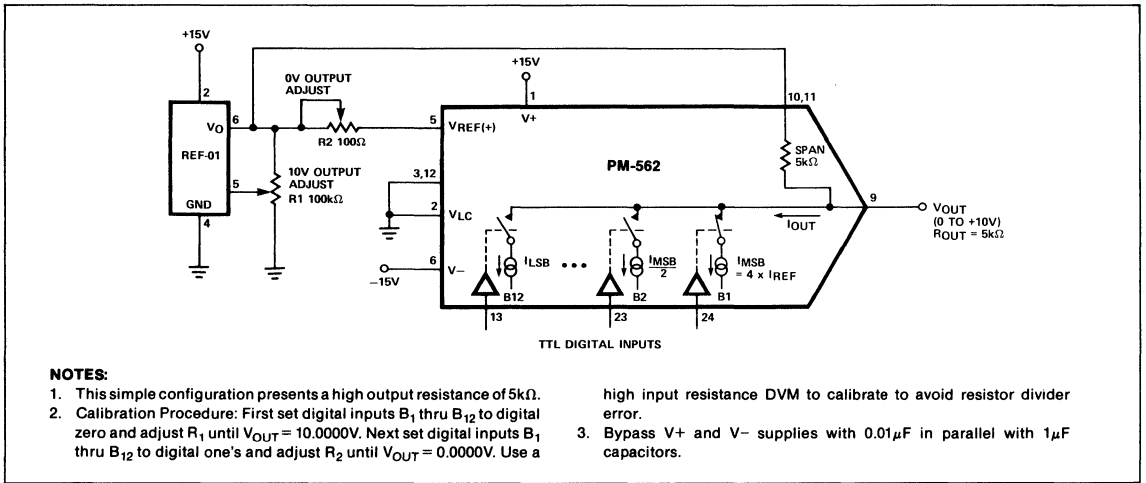
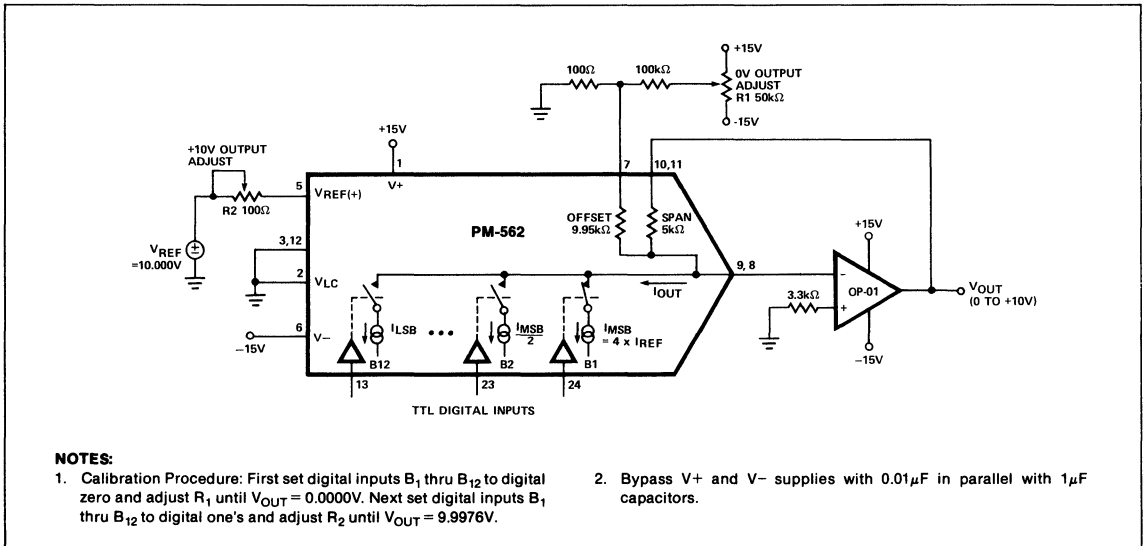
Figure 2 shows the best configuration to achieve a 0V to 10V output digital-to-analog converter. In this configuration digital "0" in produces 0V out. All one's in produces 10V out.

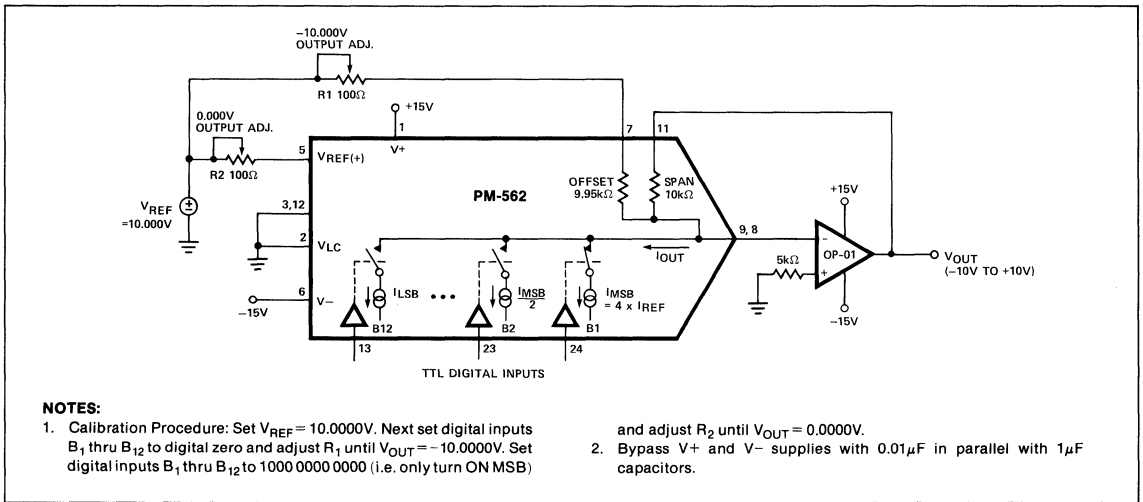
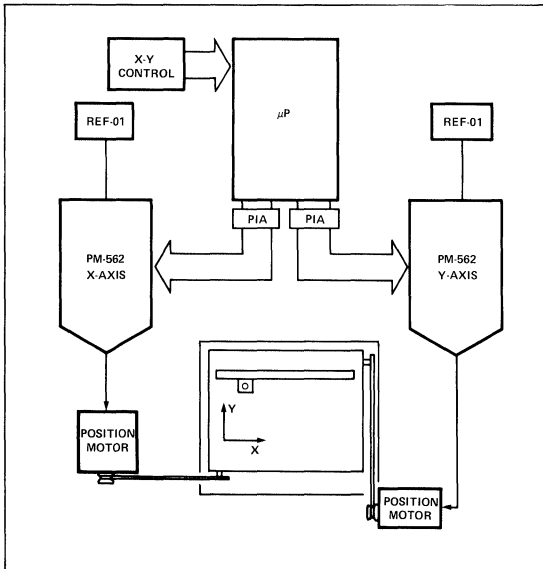
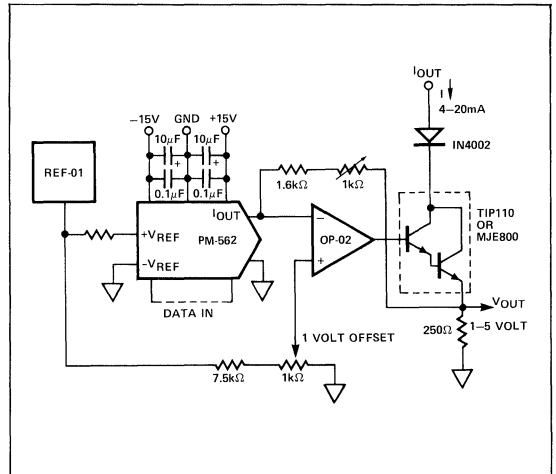
Calibration of Figure 2 is accomplished by placing digital "0" on all input bits and adjusting R1 until 0V appears at V_{OUT}. Next the span (or full-scale) is adjusted by R2 for an output voltage of 9.9976V.

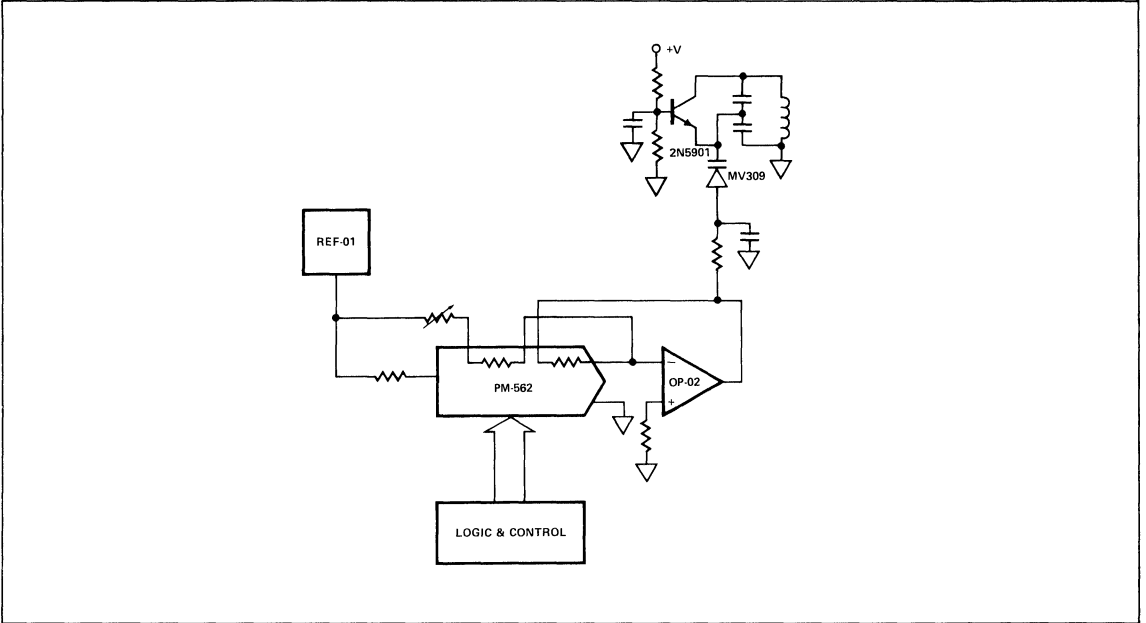
BIPOLAR OPERATION (±10V OUTPUT)

The bipolar configuration of Figure 3 provides positive and negative output voltage under control of one's complement digital input coding. Calibration is accomplished by turning all bits OFF (digital zero input code) and adjusting trimmer R1 for -10.000V output. Next turn ON the MSB (digital 1000 0000 input code) and adjust R2 for 0.0000V.

This circuit can easily be converted to ±5V output by connecting Pin-10 to the OP-01 output, making the span resistor 5kΩ.


Figure 1 Unbuffered Unipolar 0 to +10V Output

Figure 2 +10V Unipolar Voltage Output


Figure 3 ±10V Bipolar Voltage Output
PRECISION X-Y POSITIONING SYSTEM

4-20mA TRANSMITTER


DIGITALLY CONTROLLED R.F. OSCILLATOR




PM-565A

COMPLETE HIGH-SPEED 12-BIT MONOLITHIC D/A CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Very Fast-Settling (Sample Tested) 250ns Max
- High-Stability Buried-Zener Reference on Chip
- Linearity Guaranteed Over Temperature . . 1/2 LSB Max
- Monotonicity Guaranteed Over Temperature
- Low Power Consumption 345mW Max
- Operation Guaranteed at $\pm 12V$ Supplies
- Inputs Compatible with 5V and 15V Logic
- AD565A Second-Source Pin Compatibility with Improved Tempco, Reference Load Capability, and Trimming

ORDERING INFORMATION†

LINEARITY OVER TEMPERATURE RANGE	FULL-SCALE TEMP CO, MAX	PACKAGE		OPERATING TEMPERATURE RANGE
		EPOXY DIP 24-PIN	HERMETIC DIP 24-PIN	
$\pm 1/2$ LSB	15 ppm/°C	—	PM565AAV*	MIL
$\pm 3/4$ LSB	30 ppm/°C	—	PM565ABV*	MIL
$\pm 1/2$ LSB	15 ppm/°C	PM565AGP	—	COM
$\pm 3/4$ LSB	30 ppm/°C	PM565AHP	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

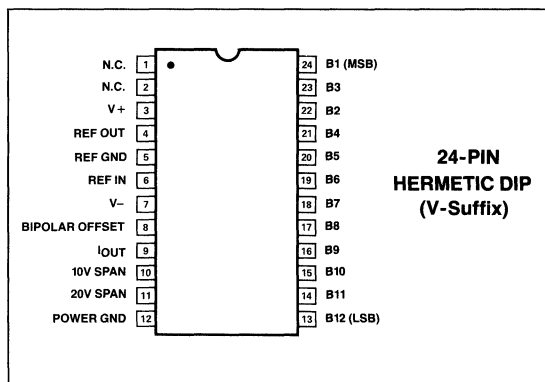
The PM-565A is a high-speed 12-bit bipolar digital-to-analog converter which provides a trimmed reference and application resistors. The output is a 0-2mA current, which can be converted to

0 to 10V, 0 to 5V, -5 to 5V, -10 to 10V output voltages using an external op-amp and the internal resistors. The digital inputs are TTL-compatible and may be driven by 5V or 15V CMOS.

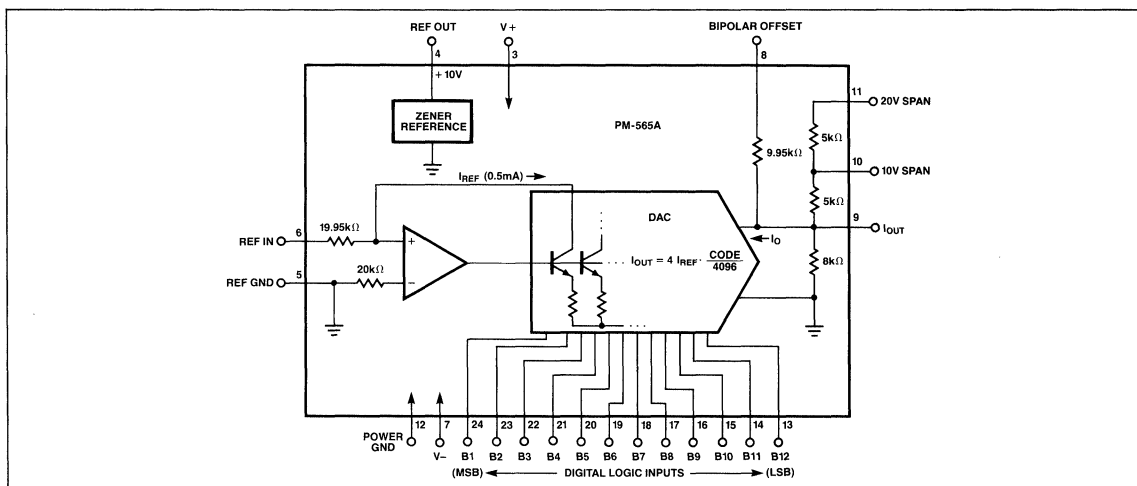
Logic delay to analog output is typically only 40ns, and settling to 0.01% of full-scale is factory tested. Great attention has been given to minimizing glitch energy and amplitude.

The subsurface zener reference is very stable, both over temperature and time. Typical gain tempco is only 10ppm/°C. The zener reference has less wideband noise than a typical bandgap type and is also free from excessive low-frequency noise. The reference is trimmed to 2 LSB Typ.

PIN CONNECTIONS



EQUIVALENT CIRCUIT



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



PM-7226

QUAD 8-BIT CMOS D/A CONVERTER
WITH VOLTAGE OUTPUT

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Four Voltage Output DACs on a Single Chip
- Microprocessor Compatible
- Internal Output Buffer Amplifiers
- Common 8-Bit Data Bus
- Adjustment-Free $\pm 2\text{LSB}$ Total Error
- Guaranteed Monotonicity
- Single or Dual Supply Operation
- Latch-Up Resistant
- Space Saving 20-Pin 0.3 Inch Wide DIP

APPLICATIONS

- Automatic Test Equipment
- Industrial Automation
- Process Controls
- Instrumentation Equipment
- Medical Equipment
- Multi-Channel Microprocessor-Controlled Systems
- X-Y Graphics

ORDERING INFORMATION†

TOTAL UNADJUSTED ERROR	PACKAGE: 20-PIN**		
	COMMERCIAL TEMPERATURE	INDUSTRIAL TEMPERATURE	MILITARY* TEMPERATURE
$\pm 2\text{LSB}$	PM7226GP	PM7226ER	PM7226AR

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

** Package Designation: Suffix R: Hermetic DIP; Suffix P: Plastic Dip.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7226AR	AD7226TD	MIL
PM7226ER	AD7226BQ	IND
PM7226GP	AD7226KN	COM

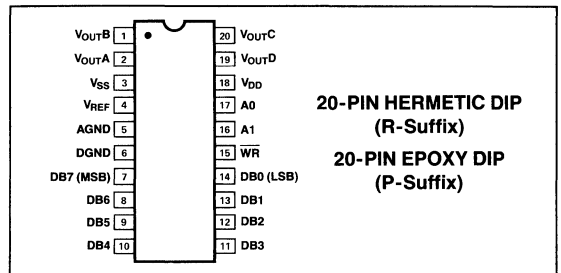
GENERAL DESCRIPTION

The PM-7226 places four 8-bit voltage output CMOS digital-to-analog converters on a single chip. By using a single 8-bit data bus port, the device fits into a space saving 20-pin 300 mil DIP package. The internal output buffer amplifiers can each drive up to 5mA from either single or dual supply rails. Each DAC has individually addressable data latches for easy microprocessor interface.

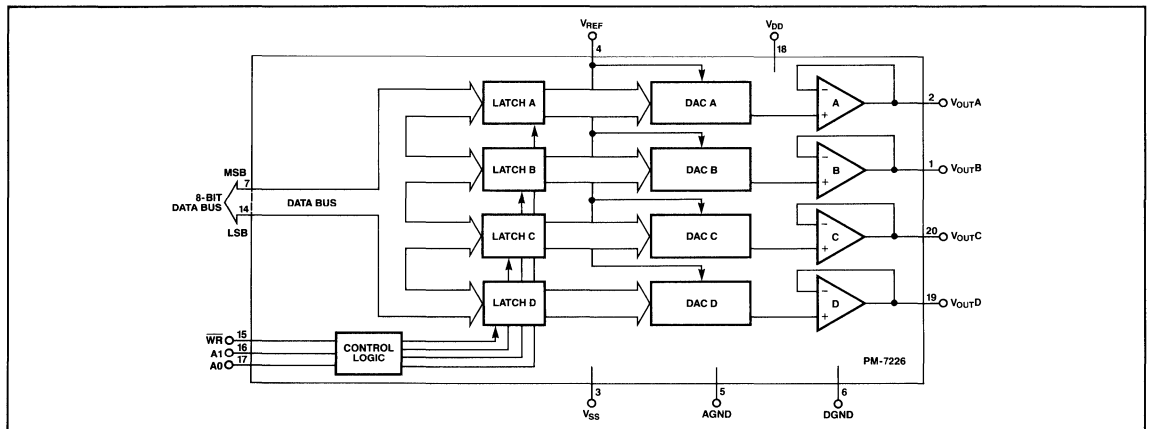
The compact size, low power, and economical cost-per-channel, makes the PM-7226 attractive for applications requiring multiple D/A converters without sacrificing circuit-board space.

The PM-7226 is a direct replacement for AD7226.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



PM-7524

CMOS 8-BIT BUFFERED MULTIPLYING D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- $\pm 1/8$ LSB Endpoint Linearity
- Microprocessor Compatible
- On-Board Data Latches
- Guaranteed Monotonicity Over Full Temperature Range
- Low Power Consumption 5mW @ +5V
- +5V to +15V Operation
- Full Four Quadrant Multiplication
- TTL/CMOS Compatible
- Latch-Up Resistant
- No Schottky Diodes Required

APPLICATIONS

- Microprocessor Controlled Circuits
- Precision AGC Circuits
- Bus Structured Instruments
- Function Generators
- Digitally Controlled Attenuators and Power Supplies

ORDERING INFORMATION†

PACKAGE: 16-PIN**			
NONLINEARITY	MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -25°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
$\pm 1/8$ (LSB)	PM7524AQ	PM7524EQ	PM7524GP
$\pm 1/4$ (LSB)	PM7524BQ	PM7524FQ	PM7524HP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

** Package Designation: Suffix Q: Hermetic DIP, Suffix P: Epoxy DIP.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The PM-7524 is an 8-bit monolithic multiplying digital-to-analog converter with input latches. It is compatible with all popular 8-bit microprocessors including the 6800, 8080, 8085, and Z80. Its load cycle is similar to that of a RAM's write cycle.

PMI's tightly controlled thin-film resistor processing provides 1/8 LSB linearity without laser trimming. The design incorporates a matching MOS transistor in series with the feedback resistor to achieve a gain and linearity error tempco of 2ppm/°C.

The PM-7524 exhibits excellent performance on a single +5V to +15V power supply. It is TTL compatible at +5V and dissipates less than 10 mW; at +15V it is CMOS compatible and dissipates less than 30 mW.

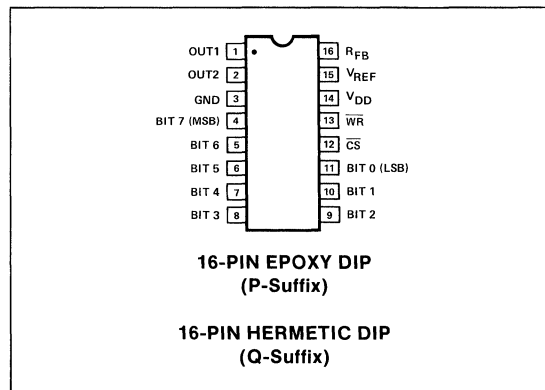
PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

The PM-7524 is manufactured using thin-film resistors on an advanced oxide-isolated silicon-gate CMOS process.

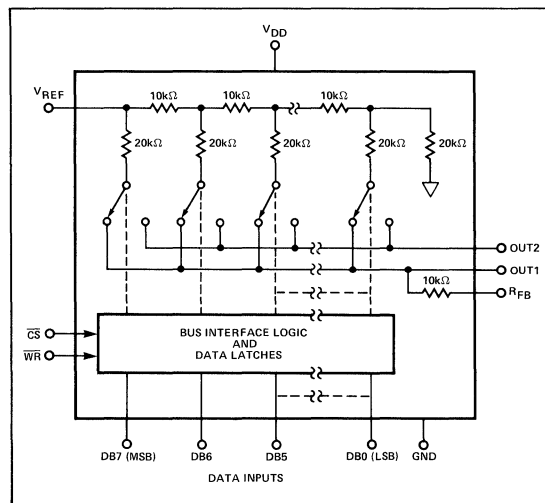
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7524AQ	AD7524UD	MILITARY
PM7524BQ	AD7524TD	
PM7524BQ	AD7524SD	
PM7524EQ	AD7524CD	INDUSTRIAL
PM7524FQ	AD7524BD	
PM7524FQ	AD7524AD	
PM7524GP	AD7524LN	COMMERCIAL
PM7524HP	AD7524KN	
PM7524HP	AD7524JN	

PIN CONNECTIONS



FUNCTIONAL DIAGRAM





ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} (to GND)	-0.3V, +17V
V_{REF} (to GND)	$\pm 25\text{V}$
R_{FB} (to GND)	$\pm 25\text{V}$
Digital Input Voltage To GND	-0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	-0.3V to V_{DD}
Power Dissipation (Package)	
Ceramic (Suffix Q)	
To $+75^\circ\text{C}$	450mW
Derates Above $+75^\circ\text{C}$ By	6mW/ $^\circ\text{C}$
Plastic (Suffix P)	
To $+70^\circ\text{C}$	670mW
Derates Above $+70^\circ\text{C}$ By	8.3mW/ $^\circ\text{C}$
Operating Temperature Range	
Military (AQ, BQ Versions)	-55°C to $+125^\circ\text{C}$
Industrial (EQ, FQ Versions)	-25°C to $+85^\circ\text{C}$
Commercial (GP, HP Versions)	0°C to $+70^\circ\text{C}$

Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener protected, however, permanent damage may occur on unconnected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at $V_{REF} = +10\text{V}$; $V_{OUT1} = V_{OUT2} = 0\text{V}$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for PM-7524AQ/BQ; $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ apply for PM-7524EQ/FQ; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for PM-7524GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
STATIC ACCURACY									
			PM-7524A/E/G			PM-7524B/F/H			
Resolution	N	$V_{DD} = +5$ or $+15\text{V}$ $T_A = \text{Full Temp. Range}$	8	—	—	8	—	—	Bits
Relative Accuracy (Notes 1, 2)	INL	$V_{DD} = +5\text{V}$ $T_A = \text{Full Temp. Range}$	—	—	± 0.2	—	—	± 0.2	%FSR
		$V_{DD} = +15\text{V}$ $T_A = \text{Full Temp. Range}$	—	—	± 0.05	—	—	± 0.1	
Gain Error (Note 3)	G_{FSE}	$V_{DD} = +5\text{V}$ $T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	—	—	± 1.0	—	—	± 1.0	%FSR
		$V_{DD} = +15\text{V}$ $T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	—	—	± 0.5	—	—	± 0.5	
Gain T.C. (Notes 4, 5)	TCG_{FS}	$V_{DD} = +5\text{V}$ $T_A = \text{Full Temp. Range}$	—	± 0.004	—	—	± 0.004	—	%FSR/ $^\circ\text{C}$
		$V_{DD} = +15\text{V}$ $T_A = \text{Full Temp. Range}$	—	± 0.001	—	—	± 0.001	—	
DC Power Supply Rejection $\Delta\text{Gain}/\Delta V_{DD}$ (Notes 3, 6)	PSR	$V_{DD} = +5\text{V}$ $T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	—	0.002	0.08	—	0.002	0.08	%FSR/%
		$V_{DD} = +15\text{V}$ $T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	—	0.001	0.02	—	0.001	0.02	
		$V_{DD} = +15\text{V}$ $T_A = \text{Full Temp. Range}$	—	0.005	0.04	—	0.005	0.04	
Output Leakage Current I_{OUT1}, I_{OUT2}	I_{LKG}	$V_{DD} = +5\text{V}$ $T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$ (Notes 7, 8)	—	—	± 50	—	—	± 50	nA
		$V_{DD} = +15\text{V}$ $T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	—	—	± 400	—	—	± 400	
		$V_{DD} = +15\text{V}$ $T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$ (Notes 7, 8)	—	—	± 200	—	—	± 200	



ELECTRICAL CHARACTERISTICS at $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7524AQ/BQ; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7524EQ/FQ; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7524GP/HP, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE									
Propagation Delay (From Digital Input to 90% of Final Analog Output Current) (Note 4)	t_{PD}	$V_{DD} = +5V$	PM-7524A/B			PM-7524E/F/G/H			ns
		$T_A = +25^\circ C$	—	—	150	—	—	150	
		$T_A = \text{Full Temp. Range}$ (Note 9)	—	—	200	—	—	175	
		$V_{DD} = +15V$	PM-7524A/E/G			PM-7524B/F/H			
Output Current Settling Time (To 1/2 LSB) (Note 4, 15)	t_s	$V_{DD} = +5V$	—	—	300	—	—	300	ns
		$T_A = +25^\circ C$	—	—	350	—	—	350	
		$T_A = \text{Full Temp. Range}$ (Note 9)	—	—	200	—	—	200	
		$V_{DD} = +15V$	—	—	250	—	—	250	
AC Feedthrough I_{OUT1}, I_{OUT2} (Note 4)	FT	$V_{DD} = +5V$ or $+15V$	—	—	0.25	—	—	0.25	%FSR
		$T_A = +25^\circ C$	—	—	0.50	—	—	0.50	
		$T_A = \text{Full Temp. Range}$ (Note 10)	—	—	0.25	—	—	0.25	
		$V_{DD} = +5V$ or $+15V$	—	—	30	—	—	30	
Output Capacitance C_{OUT1} (Pin 1) C_{OUT2} (Pin 2)	C_O	$V_{DD} = +5V$ or $+15V$	—	—	120	—	—	120	pF
		$T_A = \text{Full Temp. Range}$ (Note 4, 12)	—	—	30	—	—	30	
		$V_{DD} = +5V$ or $+15V$	—	—	30	—	—	30	
		$T_A = \text{Full Temp. Range}$ (Note 4, 13)	—	—	120	—	—	120	
DIGITAL INPUTS									
Digital Input High	V_{IH}	$V_{DD} = +5V$	+2.4	—	—	+2.4	—	—	V
		$T_A = \text{Full Temp. Range}$	—	—	—	—	—	—	
Digital Input Low	V_{IL}	$V_{DD} = +5V$	—	—	+0.8	—	—	+0.8	V
		$T_A = \text{Full Temp. Range}$	—	—	+1.5	—	—	+1.5	
Input Current $V_{IN} = 0V$ or V_{DD}	I_{IN}	$V_{DD} = +5V$ or $+15V$	—	—	± 1	—	—	± 1	μA
		$T_A = +25^\circ C$	—	—	± 10	—	—	± 10	
Input Capacitance DB0-DB7 WR, CS (Note 4)	C_{IN}	$V_{DD} = +5V$ or $+15V$	—	—	5	—	—	5	pF
		$T_A = \text{Full Temp. Range}$ $V_{IN} = 0V$	—	—	20	—	—	20	



ELECTRICAL CHARACTERISTICS at $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7524AQ/BQ; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7524EQ/FQ; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7524GP/HP, unless otherwise noted. (Continued)

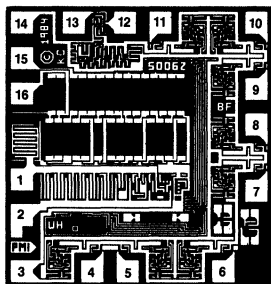
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4)									
Chip Select to Write Setup Time ($t_{WR} = t_{CS}$) (Note 14)	t_{CS}	$V_{DD} = +5V$	PM-7524A/B			PM-7524E/F/G/H			ns
		$T_A = -25^\circ C$	170	—	—	170	—	—	
		$T_A = \text{Full Temp. Range}$	240	—	—	220	—	—	
		$V_{DD} = +15V$	100	—	—	100	—	—	
		$T_A = +25^\circ C$	150	—	—	130	—	—	
		$T_A = \text{Full Temp. Range}$	150	—	—	130	—	—	
Chip Select to Write Hold Time	t_{CH}	$V_{DD} = +5V$ or $+15V$	PM-7524A/E/G			PM-7524B/F/H			ns
		$T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	
Write Pulse Width ($t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$)	t_{WR}	$V_{DD} = +5V$	PM-7524A/B			PM-7524E/F/G/H			ns
		$T_A = +25^\circ C$	170	—	—	170	—	—	
		$T_A = \text{Full Temp. Range}$	240	—	—	220	—	—	
		$V_{DD} = +15V$	100	—	—	100	—	—	
		$T_A = +25^\circ C$	150	—	—	130	—	—	
		$T_A = \text{Full Temp. Range}$	150	—	—	130	—	—	
Data Setup Time	t_{DS}	$V_{DD} = +5V$	PM-7524A/E/G			PM-7524B/F/H			ns
		$T_A = +25^\circ C$	135	—	—	135	—	—	
		$T_A = \text{Full Temp. Range}$	170	—	—	170	—	—	
		$V_{DD} = +15V$	60	—	—	60	—	—	
		$T_A = +25^\circ C$	100	—	—	80	—	—	
		$T_A = \text{Full Temp. Range}$	100	—	—	80	—	—	
Data Hold Time	t_{DH}	$V_{DD} = +5V$ or $+15V$	PM-7524A/E/G			PM-7524B/F/H			ns
		$T_A = \text{Full Temp. Range}$	10	—	—	10	—	—	
POWER SUPPLY									
Supply Current (All Digital Inputs = V_{IL} or V_{IH})	I_{DD}	$V_{DD} = +5V$	PM-7524A/B			PM-7524E/F/G/H			mA
		$T_A = +25^\circ C$	—	—	1	—	—	1	
		$T_A = \text{Full Temp. Range}$	—	—	2	—	—	2	
		$V_{DD} = +15V$	—	—	2	—	—	2	
		$T_A = +25^\circ C$	—	—	2	—	—	2	
		$T_A = \text{Full Temp. Range}$	—	—	2	—	—	2	
Supply Current (All Digital Inputs = $0V$ or V_{DD})	I_{DD}	$V_{DD} = +5V$ or $+15V$	PM-7524A/B			PM-7524E/F/G/H			μA
		$T_A = +25^\circ C$	—	—	100	—	—	100	
		$T_A = \text{Full Temp. Range}$	—	—	500	—	—	500	

NOTES:

- Guaranteed monotonic over full temperature range and at $V_{DD} = +5V$ and $+15V$.
- FSR (Full Scale Range) = $V_{REF} - 1 \text{ LSB}$.
- Using internal feedback resistor.
- Guaranteed by design and not production tested.
- Gain TC measured from $+25^\circ C$ to T_{MIN} or from $+25^\circ C$ to T_{MAX} .
- $\Delta V_{DD} = \pm 10\%$.
- DB0—DB7 = $0V$; $\overline{WR} = \overline{CS} = 0V$; $V_{REF} = \pm 10V$, for I_{OUT1} .
- DB0—DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$; $V_{REF} = \pm 10V$, for I_{OUT2} .
- OUT1 load = 100Ω ; $C_{EXT} = 13pF$; $\overline{WR} = \overline{CS} = 0V$; DB0—DB7 = $0V$ to V_{DD} or V_{DD} to $0V$.
- $V_{REF} = \pm 10V$, $f = 100kHz$; DB0—DB7 = $0V$; $\overline{WR} = \overline{CS} = 0V$.
- Temperature coefficient approximately equals $+300ppm/^\circ C$.
- DB0—DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$.
- DB0—DB7 = $0V$; $\overline{WR} = \overline{CS} = 0V$.
- See Timing Diagram.
- Extrapolated: $t_g (1/2 \text{ LSB}) = t_{pD} + 6.2\tau$, where τ = the measured first time constant of the final RC decay.



DICE CHARACTERISTICS

DIE SIZE 0.067 x 0.070 inch; 4690 sq. mils
(1.7 x 1.78 mm, 3.03 sq. mm)

- | | |
|--------------|----------------------|
| 1. OUT1 | 9. DB2 |
| 2. OUT2 | 10. DB1 |
| 3. GND | 11. DB0 (LSB) |
| 4. DB7 (MSB) | 12. CS |
| 5. DB6 | 13. WR |
| 6. DB5 | 14. V _{DD} |
| 7. DB4 | 15. V _{REF} |
| 8. DB3 | 16. R _{FB} |

For additional DICE information refer to
1986 Data Book, Section 2.WAFER TEST LIMITS at V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V; T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	PM-7524G LIMIT	UNITS
STATIC ACCURACY				
Resolution	N	V _{DD} = +5V or +15V	8	Bits MIN
Relative Accuracy (Notes 1, 2)	INL	V _{DD} = +5V V _{DD} = +15V	±0.02 ±0.05	% of FSR MAX
Gain Error (Note 3)	G _{FSE}	V _{DD} = +5V or +15V	±0.05	% of FSR MAX
DC Power Supply Rejection ΔGain/ΔV _{DD} (Notes 3, 4)	PSR	V _{DD} = +5V V _{DD} = +15V	0.08 0.02	% of FSR/% MAX
Output Leakage Current I _{OUT1} , I _{OUT2}	I _{LKG}	V _{DD} = +5V or +15V (Notes 5, 6)	±50	nA MAX
REFERENCE INPUT				
Input Resistance (Note 7)	R _{IN}	V _{DD} = +5V or +15V	5/20	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input High	V _{IH}	V _{DD} = +5V V _{DD} = +15V	+2.4 +13.5	V MIN
Digital Input Low	V _{IL}	V _{DD} = +5V V _{DD} = +15V	+0.8 +1.5	V MAX
Input Current (V _{IN} = 0V or V _{DD})	I _{IN}	V _{DD} = +5V or +15V	±1	μA MAX
POWER SUPPLY				
Supply Current (V _{IN} = V _{IL} or V _{IH})	I _{DD}	V _{DD} = +5V V _{DD} = +15V	1 2	mA MAX
Supply Current (V _{IN} = 0V or V _{DD})	I _{DD}	V _{DD} = +5V or +15V	100	μA MAX

NOTES:

- Guaranteed monotonic over full temperature range and at V_{DD} = +5V and +15V.
- FSR (Full Scale Range) = V_{REF} - 1 LSB.
- Using internal feedback resistor.

- ΔV_{DD} = ±10%.
- DB0-DB7 = 0V; WR = CS = 0V; V_{REF} = ±10V, for I_{OUT1}.
- DB0-DB7 = V_{DD}; WR = CS = 0V; V_{REF} = ±10V, for I_{OUT2}.
- Temperature coefficient approximately equals +300ppm/°C.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

DEFINITIONS
RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where n is equal to the number of bits. Resolution in no way implies linearity.

RELATIVE ACCURACY

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1 LSB.

PROPAGATION DELAY

The time for the output current to reach 90% of its final value from a given digital input signal.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when using the DAC's internal feedback resistor.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideal output is equal to $V_{REF} - 1 \text{ LSB}$.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches off.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

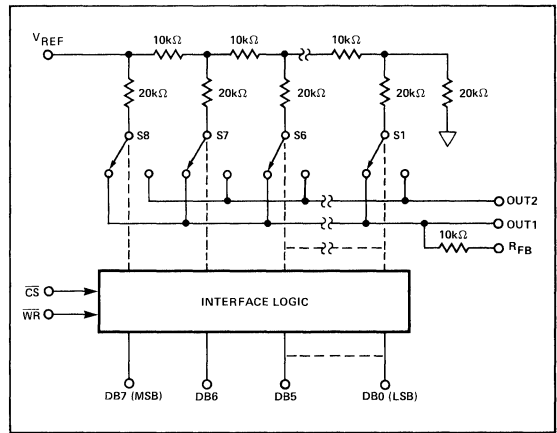
OUTPUT LEAKAGE CURRENT

Current which appears on I_{OUT1} terminal with all digital inputs low or on I_{OUT2} terminal when all inputs are high.

CIRCUIT DESCRIPTION
CIRCUIT INFORMATION

The PM-7524 is an 8-bit multiplying CMOS digital-to-analog converter with on-board data latches. It is fabricated using a highly stable thin-film R-2R resistor ladder network and eight N-channel current switches. A voltage or current reference and an operational amplifier are all that is required in the majority of applications.

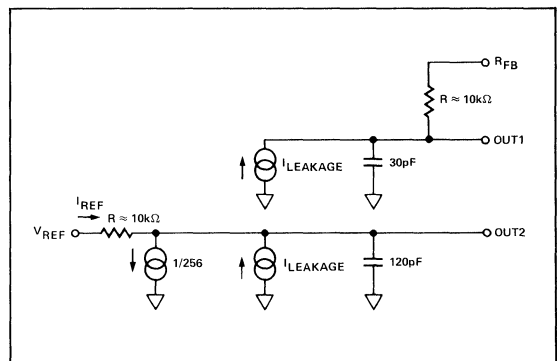
Figure 1 shows a simplified circuit of the PM-7524 converter. The R-2R ladder, current steering switches, and interface

FIGURE 1: PM-7524 Functional Diagram


logic are shown. The switches are binary weighted and switch the ladder current between I_{OUT1} and I_{OUT2} bus lines; this switching allows a constant current to be maintained in each resistor leg regardless of the switch state.

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an equivalent circuit for the PM-7524 with all digital inputs LOW. The I_{OUT1} and I_{OUT2} leakage current source is the combination of surface and junction leakages to the substrate. The 1/256 current source represents the constant 1-bit current drain through the ladder termination resistor. The situation is reversed with all digital inputs HIGH, i.e., the current output is now switched to the I_{OUT1} terminal. The output capacitance is dependent upon the digital input code, and is therefore modulated between the low and high values.

FIGURE 2: PM-7524 Equivalent Circuit (All Digital Inputs LOW)


INTERFACE LOGIC

MODE SELECTION

The mode selection is controlled by the \overline{CS} and \overline{WR} inputs.

WRITE MODE

The PM-7524 is in the WRITE mode when both the \overline{CS} and \overline{WR} are both LOW; the input latches are transparent and the output immediately follows the data input logic. See the MODE SELECTION TABLE.

HOLD MODE

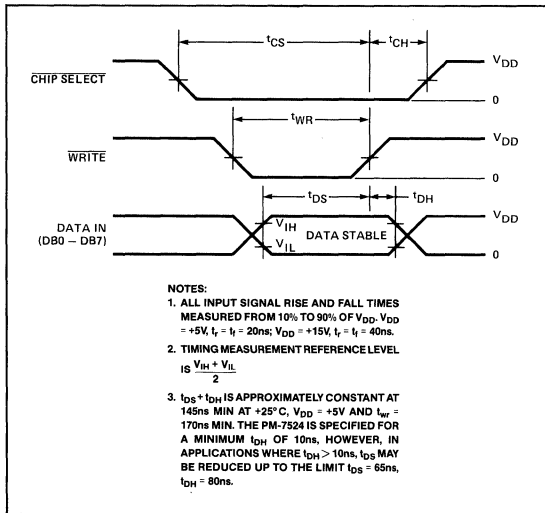
The MODE SELECTION TABLE shows the output results when either \overline{CS} or \overline{WR} is HIGH. The output holds the value corresponding to the last digital inputs prior to \overline{CS} or \overline{WR} assuming the HIGH state.

MODE SELECTION TABLE

\overline{CS}	\overline{WR}	MODE	DAC RESPONSE
L	L	WRITE	DAC responds to data bus (DB0 — DB7) inputs (transparent)
H	X	HOLD	Data bus (DB0 — DB7) is locked out
X	H	HOLD	DAC holds last data present when \overline{WR} or \overline{CS} assumes a HIGH state

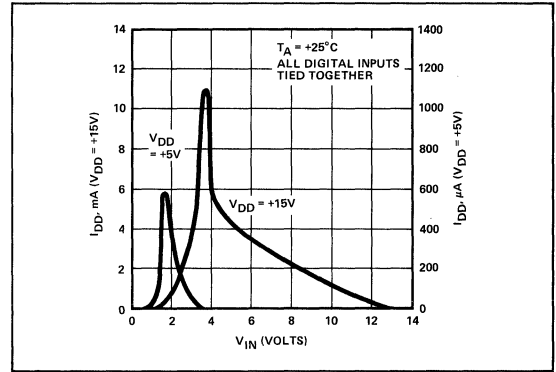
L = Low State, H = High State, X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



Supply current (I_{DD}) versus Logic input voltage (V_{IN}) is shown in Figure 3. This plot shows the supply current for both $V_{DD} = +5V$ and $V_{DD} = +15V$.

FIGURE 3: Supply Current vs Logic Level



APPLICATIONS

FIGURE 4: Unipolar Binary Operation (2-Quadrant Multiplication)

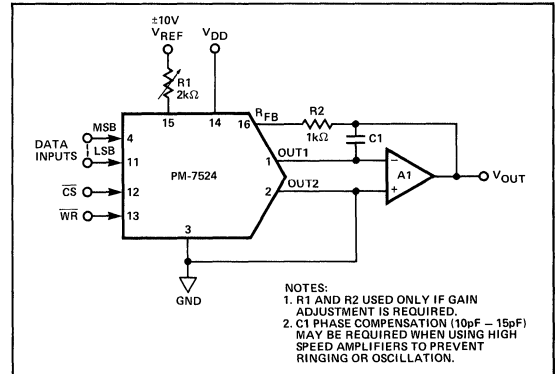


TABLE I: Unipolar Binary Code Table

DIGITAL INPUT		ANALOG OUTPUT
MSB	LSB	
1	1 1 1 1 1 1 1	$-V_{REF} \left(\frac{255}{256} \right)$
1	0 0 0 0 0 0 1	$-V_{REF} \left(\frac{129}{256} \right)$
1	0 0 0 0 0 0 0	$-V_{REF} \left(\frac{128}{256} \right) = -\frac{V_{REF}}{2}$
0	1 1 1 1 1 1 1	$-V_{REF} \left(\frac{127}{256} \right)$
0	0 0 0 0 0 0 1	$-V_{REF} \left(\frac{1}{256} \right)$
0	0 0 0 0 0 0 0	$-V_{REF} \left(\frac{0}{256} \right) = 0$

NOTE:

$$1LSB = (2^{-8}) (V_{REF}) = \frac{1}{256} (V_{REF})$$

FIGURE 5: Bipolar (4-Quadrant) Operation

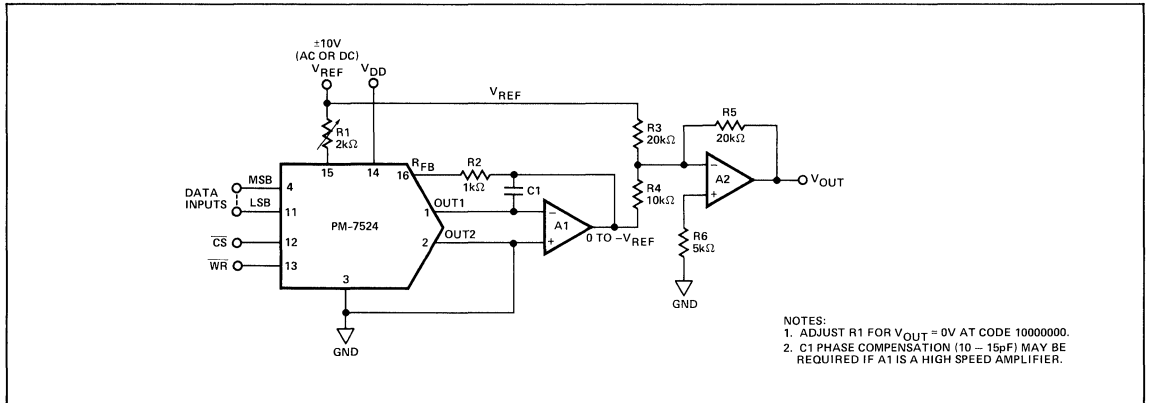


TABLE II: Bipolar (Offset Binary) Code Table

DIGITAL INPUT		ANALOG OUTPUT
MSB	LSB	
1	1 1 1 1 1 1 1	$+V_{REF} \left(\frac{127}{128} \right)$
1	0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{128} \right)$
1	0 0 0 0 0 0 0	0
0	1 1 1 1 1 1 1	$-V_{REF} \left(\frac{1}{128} \right)$
0	0 0 0 0 0 0 1	$-V_{REF} \left(\frac{127}{128} \right)$
0	0 0 0 0 0 0 0	$-V_{REF} \left(\frac{128}{128} \right)$

NOTE:
 $1\text{LSB} = (2^{-7}) (V_{REF}) = \frac{1}{128} (V_{REF})$

FIGURE 7: PM-7524/MC6800 Interface

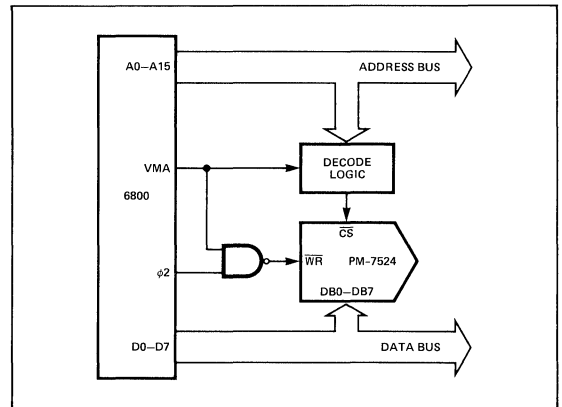


FIGURE 6: PM-7524/8085A Interface

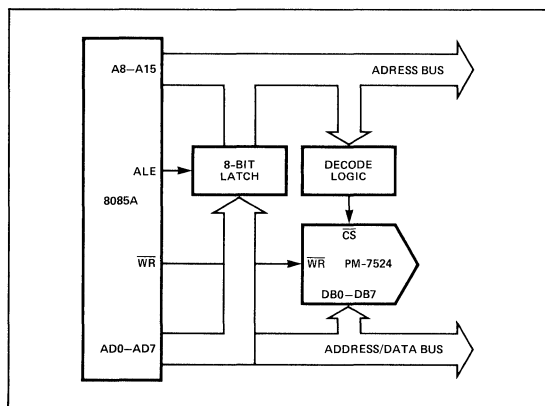




FIGURE 8: Power Generation Connection

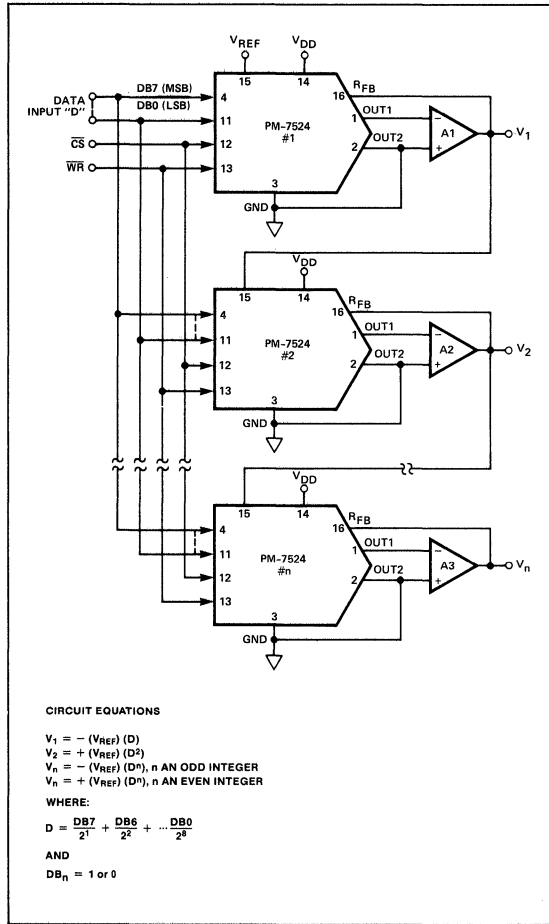
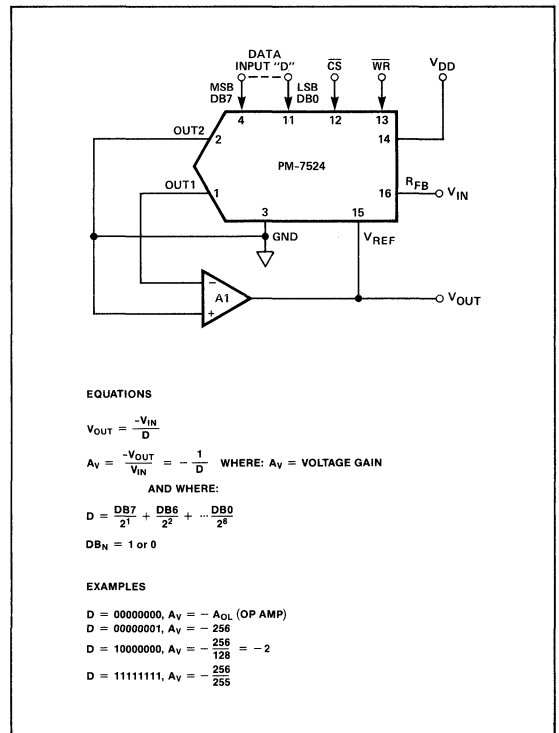


FIGURE 9: Divider
(Digitally Controlled Gain)



Precision Monolithics Inc.

FEATURES

- On-Chip Latches For Both DACs
- +5V To +15V Single Supply Operation
- DACs Matched To 1%
- Four-Quadrant Multiplication
- TTL/CMOS Compatible
- 8-Bit Endpoint Linearity ($\pm 1/2$ LSB)
- Full Temperature Operation
- Low Power Consumption
- Microprocessor Compatible

APPLICATIONS

- Digital Gain/Attenuation Control
- Digital Control Of Filter Parameters
- Digitally-Controlled Audio Circuits
- X-Y Graphics
- Digital/Synchro Conversion
- Robotics
- Ideal For Battery-Operated Equipment

ORDERING INFORMATION†

PACKAGE: 20-PIN**

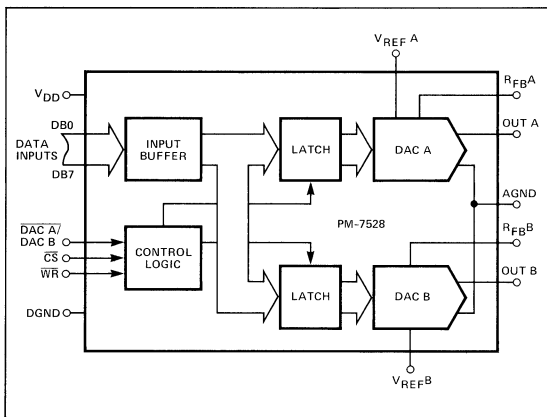
RELATIVE ACCURACY	GAIN ERROR	MILITARY* TEMPERATURE RANGE	INDUSTRIAL TEMPERATURE RANGE	COMMERCIAL TEMPERATURE RANGE
$\pm 1/2$ LSB	± 2 LSB	-55°C TO +125°C	-25°C TO +85°C	0°C TO +70°C
$\pm 1/2$ LSB	± 1 LSB	PM-7528BR	PM-7528FR	PM-7528HP
		PM-7528AR	PM-7528ER	PM-7528GP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

** Package designation: Suffix R: Hermetic Dip, Suffix P: Plastic Dip

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

FUNCTIONAL DIAGRAM



CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7528AR	AD7528UD	MILITARY
PM7528BR	AD7528TD	
PM7528BR	AD7528SD	
PM7528ER	AD7528CQ	INDUSTRIAL
PM7528FR	AD7528BQ	
PM7528FR	AD7528AQ	
PM7528GP	AD7528LN	COMMERCIAL
PM7528HP	AD7528KN	
PM7528HP	AD7528JN	

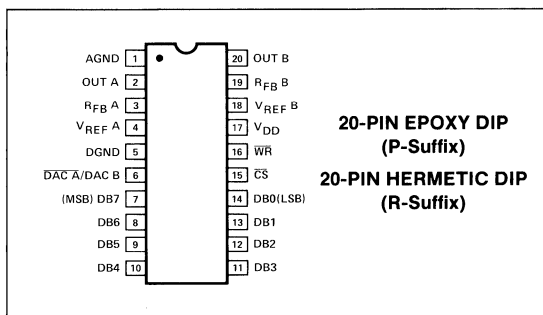
GENERAL DESCRIPTION

The PM-7528 contains two 8-bit multiplying digital-to-analog converters. Excellent DAC-to-DAC matching and tracking results from monolithic construction. The PM-7528 consists of two thin-film R-2R resistor-ladder networks, two data latches, one input buffer, and control logic. Operation from a 5 to 15 volt single power supply dissipates only 20mW of power.

Digital input data is directed into one of the DAC data latches determined by the DAC selection control line DAC A/DAC B. The 8-bit wide input data path provides TTL/CMOS compatibility. The data load cycle is similar to the write cycle of a random access memory. The PM-7528 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80.

The PM-7528 saves PC board space with the narrow 20-pin 0.3" wide DIP. A set of internal tracking span resistors is included, minimizing external parts.

PIN CONNECTIONS



DIGITAL-TO-ANALOG CONVERTERS

**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} to AGND	0V, +17V
V _{DD} to DGND	0V, +17V
AGND to DGND	V _{DD}
DGND to AGND	V _{DD}
Digital Input Voltage to DGND	-0.3V, V _{DD}
V _{PIN 2} , V _{PIN 20} to AGND	-0.3V, V _{DD}
V _{REF A} , V _{REF B} to AGND	±25V
V _{RFB A} , V _{RFB B} to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derate Above +75°C by	6mW/°C
Operating Temperature Range	
AR, BR Versions	-55°C to +125°C
ER, FR Versions	-25°C to +85°C
GP, HP Versions	0°C to +70°C

Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF A} = V_{REF B} = +10V, OUT A = OUT B = 0V; T_A = -55°C to +125°C apply for PM-7528AR/BR; T_A = -25°C to +85°C apply for PM-7528ER/FR; T_A = 0°C to +70°C apply for PM-7528GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7528A/E/G			PM-7528B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY (Note 1)									
Resolution	N		8	—	—	8	—	—	Bits
Relative Accuracy (Note 2)	NL		—	—	±1/2	—	—	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL		—	—	±1	—	—	±1	LSB
Full Scale Gain Error (Note 4)	G _{FSE}	T _A = +25°C T _A = Full Temp. Range	—	—	±1 ±3	—	—	±2 ±4	LSB
Gain Temperature Coefficient (ΔGain/ΔTemperature) (Notes 4, 10)	TCG _{FS}		—	—	±0.007	—	—	±0.007	%/°C
Output Leakage Current Out A (Pin 2)/Out B (Pin 20) (Note 5)	I _{LKG}	T _A = +25°C T _A = Full Temp. Range	—	5	±50 ±400	—	5	±50 ±400	nA
Input Resistance (V _{REF A} , V _{REF B}) (Note 6)	R _{REF}		8	—	15	8	—	15	kΩ
V _{REF A} /V _{REF B} (Input Resistance Match)	ΔV _{REF A, B}		—	0.1	±1	—	0.1	±1	%
DIGITAL INPUTS (Note 9)									
Digital Input High	V _{INH}		2.4	—	—	2.4	—	—	V
Digital Input Low	V _{INL}		—	—	0.8	—	—	0.8	V
Input Current (Note 7)	I _{IN}	T _A = +25°C T _A = Full Temp. Range	—	.001	±1 ±10	—	.001	±1 ±10	μA
Input Capacitance (Note 10)	C _{IN}	DB0-DB7 WR, CS, DAC A/DAC B	—	—	10 15	—	—	10 15	pF



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7528AR/BR; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7528ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7528GP/HP, unless otherwise noted.
(Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7528A/E/G			PM-7528B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS (Notes 10, 11)									
Chip Select to Write Set-Up Time	t_{CS}	$T_A = +25^\circ C$	200	—	—	200	—	—	ns
		$T_A = \text{Full Temp. Range}$	230	—	—	230	—	—	
Chip Select to Write Hold Time	t_{CH}	$T_A = +25^\circ C$	20	—	—	20	—	—	ns
		$T_A = \text{Full Temp. Range}$	30	—	—	30	—	—	
DAC Select to Write Set-Up Time	t_{AS}	$T_A = +25^\circ C$	200	—	—	200	—	—	ns
		$T_A = \text{Full Temp. Range}$	230	—	—	230	—	—	
DAC Select to Write Hold Time	t_{AH}	$T_A = +25^\circ C$	20	—	—	20	—	—	ns
		$T_A = \text{Full Temp. Range}$	30	—	—	30	—	—	
Data Valid to Write Set-Up Time	t_{DS}	$T_A = +25^\circ C$	110	—	—	110	—	—	ns
		$T_A = \text{Full Temp. Range}$	130	—	—	130	—	—	
Data Valid to Write Hold Time	t_{DH}		0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	$T_A = +25^\circ C$	180	—	—	180	—	—	ns
		$T_A = \text{Full Temp. Range}$	200	—	—	200	—	—	
POWER SUPPLY (Note 12)									
Supply Current (Note 21)	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	—	—	1	—	—	1	mA
		All Digital Inputs 0V or V_{DD}	—	—	100	—	—	100	μA
AC PERFORMANCE CHARACTERISTICS (Note 13)									
DC Supply Rejection ($\Delta\text{Gain}/\Delta V_{DD}$) (Note 14)	PSRR	$T_A = +25^\circ C$	—	—	0.02	—	—	0.02	%/%
		$T_A = \text{Full Temp. Range}$	—	—	0.04	—	—	0.04	
Propagation Delay (Notes 15, 16, 17)	t_{PD}	$T_A = +25^\circ C$	—	—	220	—	—	220	ns
		$T_A = \text{Full Temp. Range}$	—	—	270	—	—	270	
Current Settling Time (Notes 16, 17, 22)	t_s	$T_A = +25^\circ C$	—	—	350	—	—	350	ns
		$T_A = \text{Full Temp. Range}$	—	—	400	—	—	400	
Digital Charge Injection (Note 18)	Q	$T_A = +25^\circ C$	—	160	—	—	160	—	nVs
Output Capacitance	$C_{OUT A}$	DAC Latches Loaded with 00000000	—	—	50	—	—	50	pF
	$C_{OUT B}$	DAC Latches Loaded with 00000000	—	—	50	—	—	50	
	$C_{OUT A}$	DAC Latches Loaded with 11111111	—	—	120	—	—	120	
	$C_{OUT B}$	DAC Latches Loaded with 11111111	—	—	120	—	—	120	
AC Feedthrough (Note 19)	FT_A	$V_{REF A}$ to OUT A; $T_A = +25^\circ C$	—	—	-70	—	—	-70	dB
		$T_A = \text{Full Temp. Range}$	—	—	-65	—	—	-65	
	FT_B	$V_{REF B}$ to OUT B; $T_A = +25^\circ C$	—	—	-70	—	—	-70	
		$T_A = \text{Full Temp. Range}$	—	—	-65	—	—	-65	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7528AR/BR; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7528ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7528GP/HP, unless otherwise noted.
(Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7528A/E/G			PM-7528B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC PERFORMANCE CHARACTERISTICS (Note 13)									
Channel-to-Channel Isolation (Note 20)	CCI_{BA}	$V_{REF A}$ to $OUT B$; $V_{REF A} = 20V_{p-p}$ Sinewave @ $f = 100kHz$ $V_{REF B} = 0V$. $T_A = +25^\circ C$	—	-77	—	—	-77	—	dB
	CCI_{AB}	$V_{REF B}$ to $OUT A$; $V_{REF B} = 20V_{p-p}$ Sinewave @ $f = 100kHz$ $V_{REF A} = 0V$. $T_A = +25^\circ C$	—	-77	—	—	-77	—	
Digital Crosstalk	Q	For Code Transition From 00000000 to 11111111. $T_A = +25^\circ C$	—	30	—	—	30	—	nVs
Harmonic Distortion	THD	$V_{IN} = 6V_{rms}$ @ $f = 1kHz$. $T_A = +25^\circ C$	—	-85	—	—	-85	—	dB

ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7528AR/BR; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7528ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7528GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7528A/E/G			PM-7528B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY (Note 1)									
Resolution	N		8	—	—	8	—	—	Bits
Relative Accuracy (Note 2)	NL		—	—	$\pm 1/2$	—	—	$\pm 1/2$	LSB
Differential Nonlinearity (Note 3)	DNL		—	—	± 1	—	—	± 1	LSB
Full Scale Gain Error (Note 4)	G_{FSE}	$T_A = +25^\circ C$	—	—	± 1	—	—	± 2	LSB
		$T_A = \text{Full Temp. Range}$	—	—	± 1	—	—	± 3	
Gain Temperature Coefficient $\Delta\text{Gain}/\Delta\text{Temperature}$ (Notes 4, 10)	TCG_{FS}		—	—	± 0.0035	—	—	± 0.0035	%/ $^\circ C$
Output Leakage Current Out A (Pin 2)/Out B (Pin 20) (Note 5)	I_{LKG}	$T_A = +25^\circ C$	—	5	± 50	—	5	± 50	nA
		$T_A = \text{Full Temp. Range}$	—	—	± 200	—	—	± 200	
Input Resistance ($V_{REF A}$, $V_{REF B}$) (Note 6)	R_{REF}		8	—	15	8	—	15	k Ω
$V_{REF A}/V_{REF B}$ (Input Resistance Match)	$\Delta V_{REF A, B}$		—	0.1	± 1	—	0.1	± 1	%
DIGITAL INPUTS (Note 9)									
Digital Input High	V_{INH}		13.5	—	—	13.5	—	—	V
Digital Input Low	V_{INL}		—	—	1.5	—	—	1.5	V



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7528AR/BR; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7528ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7528GP/HP, unless otherwise noted.
(Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7528A/E/G			PM-7528B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS (Note 9)									
Input Current (Note 7)	I_{IN}	$T_A = +25^\circ C$	—	—	± 1	—	—	± 1	μA
		$T_A = \text{Full Temp. Range}$	—	—	± 10	—	—	± 10	
Input Capacitance (Note 10)	C_{IN}	DB0-DB7	—	—	10	—	—	10	pF
		WR, CS, DAC A/DAC B	—	—	15	—	—	15	
SWITCHING CHARACTERISTICS (Notes 10, 11)									
Chip Select to Write Set-Up Time	t_{CS}	$T_A = +25^\circ C$	60	—	—	60	—	—	ns
		$T_A = \text{Full Temp. Range}$	80	—	—	80	—	—	
Chip Select to Write Hold Time	t_{CH}	$T_A = +25^\circ C$	10	—	—	10	—	—	ns
		$T_A = \text{Full Temp. Range}$	15	—	—	15	—	—	
DAC Select to Write Set-Up Time	t_{AS}	$T_A = +25^\circ C$	60	—	—	60	—	—	ns
		$T_A = \text{Full Temp. Range}$	80	—	—	80	—	—	
DAC Select to Write Hold Time	t_{AH}	$T_A = +25^\circ C$	10	—	—	10	—	—	ns
		$T_A = \text{Full Temp. Range}$	15	—	—	15	—	—	
Data Valid to Write Set-Up Time	t_{DS}	$T_A = +25^\circ C$	50	—	—	50	—	—	ns
		$T_A = \text{Full Temp. Range}$	70	—	—	70	—	—	
Data Valid to Write Hold Time	t_{DH}		10	—	—	10	—	—	ns
Write Pulse Width	t_{WR}	$T_A = +25^\circ C$	60	—	—	60	—	—	ns
		$T_A = \text{Full Temp. Range}$	80	—	—	80	—	—	
POWER SUPPLY (Note 12)									
Supply Current (Note 21)	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	—	—	1	—	—	1	mA
		All Digital Inputs 0V or V_{DD}	—	—	100	—	—	100	μA
AC PERFORMANCE CHARACTERISTICS (Note 13)									
DC Supply Rejection ($\Delta \text{Gain}/\Delta V_{DD}$) (Note 14)	PSRR	$T_A = +25^\circ C$	—	—	0.01	—	—	0.01	%/%
		$T_A = \text{Full Temp. Range}$	—	—	0.02	—	—	0.02	
Propagation Delay (Notes 15, 16, 17)	t_{pD}	$T_A = +25^\circ C$	—	—	80	—	—	80	ns
		$T_A = \text{Full Temp. Range}$	—	—	100	—	—	100	
Current Settling Time (Notes 16, 17, 22)	t_s	$T_A = +25^\circ C$	—	—	180	—	—	180	ns
		$T_A = \text{Full Temp. Range}$	—	—	200	—	—	200	
Digital Charge Injection (Note 18)	Q	$T_A = +25^\circ C$	—	440	—	—	440	—	nVs



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7528AR/BR; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7528ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7528GP/HP, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7528A/E/G			PM-7528B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC PERFORMANCE CHARACTERISTICS (Note 13)									
Output Capacitance	$C_{OUT A}$	DAC Latches Loaded	—	—	50	—	—	50	pF
	$C_{OUT B}$	with 00000000	—	—	50	—	—	50	
	$C_{OUT A}$	DAC Latches Loaded	—	—	120	—	—	120	
	$C_{OUT B}$	with 11111111	—	—	120	—	—	120	
AC Feedthrough (Note 19)	FT_A	$V_{REF A}$ to $OUT A$; $T_A = +25^\circ C$	—	—	-70	—	—	-70	dB
		$T_A =$ Full Temp. Range	—	—	-65	—	—	-65	
	FT_B	$V_{REF B}$ to $OUT B$; $T_A = +25^\circ C$	—	—	-70	—	—	-70	
		$T_A =$ Full Temp. Range	—	—	-65	—	—	-65	
Channel-to-Channel Isolation (Note 20)	CCI_{BA}	$V_{REF A}$ to $OUT B$; $V_{REF A} = 20Vp-p$ Sinewave @ $f = 100kHz$ $V_{REF B} = 0V$. $T_A = +25^\circ C$	—	-77	—	—	-77	—	dB
		$V_{REF B}$ to $OUT A$; $V_{REF B} = 20Vp-p$ Sinewave @ $f = 100kHz$ $V_{REF A} = 0V$. $T_A = +25^\circ C$	—	-77	—	—	-77	—	
	CCI_{AB}	$V_{REF A}$ to $OUT B$; $V_{REF A} = 20Vp-p$ Sinewave @ $f = 100kHz$ $V_{REF B} = 0V$. $T_A = +25^\circ C$	—	-77	—	—	-77	—	
		$V_{REF B}$ to $OUT A$; $V_{REF B} = 20Vp-p$ Sinewave @ $f = 100kHz$ $V_{REF A} = 0V$. $T_A = +25^\circ C$	—	-77	—	—	-77	—	
Digital Crosstalk	Q	For Code Transition From 00000000 to 11111111. $T_A = +25^\circ C$	—	60	—	—	60	—	nVs
Harmonic Distortion	THD	$V_{IN} = 6V_{rms}$ @ $f = 1kHz$. $T_A = +25^\circ C$	—	-85	—	—	-85	—	dB

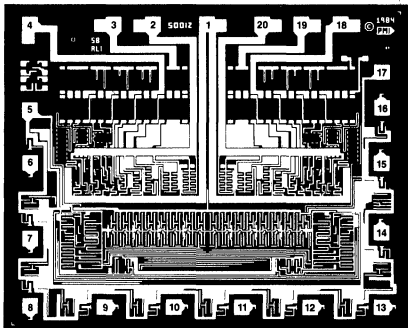
NOTES:

- Specifications apply to both DAC A and DAC B.
- This is an endpoint linearity specification.
- All grades guaranteed to be monotonic over the full operating temperature range.
- Measured using internal $R_{FB A}$ and $R_{FB B}$. Both DAC latches loaded with 11111111. Gain error is adjustable using circuits of Figures 5 and 6.
- DAC loaded with 00000000.
- Input resistance $TC = +300ppm/^\circ C$; typical input resistance = $11k\Omega$.
- $V_{IN} = 0V$ or V_{DD} .
- For all data bits DB0-DB7, \overline{WR} , \overline{CS} , $\overline{DAC A}$ /DAC B.
- Logic inputs are MOS gates. Typical input current ($+25^\circ C$) is less than $1nA$.
- Guaranteed and not tested.

- See timing diagram.
- See Figure 3.
- These characteristics are for design guidance only and are not subject to test.
- $\Delta V_{DD} = \pm 5\%$.
- From digital input to 90% of final analog-output current.
- $V_{REF A} = V_{REF B} = +10V$; $OUT A$, $OUT B$ load = 100Ω , $C_{EXT} = 13pF$.
- \overline{WR} , $\overline{CS} = 0V$, $DB0-DB7 = 0V$ to V_{DD} or V_{DD} to $0V$.
- For code transition 00000000 to 11111111.
- $V_{REF A}$, $V_{REF B} = 20Vp-p$ Sinewave @ $f = 100kHz$.
- Both DAC latches loaded with 11111111.
- $I_{DD} = 500\mu A$ at $T_A =$ Full Temp. Range.
- Extrapolated; $t_s (1/2 LSB) = t_p D + 6.2\tau$, where τ = the measured first time constant of the final RC decay.



DICE CHARACTERISTICS



DIE SIZE 0.135 × 0.110 Inch, 14,850 sq. mils
(3.429 × 2.794 mm, 9.58 sq. mm)

For additional DICE Information refer to
1986 Data Book, Section 2.

1. ANALOG GROUND (AGND)
2. OUTPUT A (OUT A)
3. DAC A FEEDBACK RESISTOR ($R_{FB A}$)
4. DAC A REFERENCE INPUT ($V_{REF A}$)
5. DIGITAL GROUND (DGND)
6. DIGITAL SELECTION ($\overline{DAC A}/DAC B$)
7. DIGITAL INPUT DB7 (MSB)
8. DIGITAL INPUT DB6
9. DIGITAL INPUT DB5
10. DIGITAL INPUT DB4
11. DIGITAL INPUT DB3
12. DIGITAL INPUT DB2
13. DIGITAL INPUT DB1
14. DIGITAL INPUT DB0 (LSB)
15. CHIP SELECT (\overline{CS})
16. WRITE (\overline{WR})
17. POSITIVE POWER SUPPLY (V_{DD})
18. DAC B REFERENCE INPUT ($V_{REF B}$)
19. DAC B FEEDBACK RESISTOR ($R_{FB B}$)
20. OUTPUT B (OUT B)

WAFER TEST LIMITS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7528G	
			LIMIT	UNITS
Relative Accuracy	NL	Endpoint Linearity Error	$\pm 1/2$	LSB MAX
Differential Nonlinearity	DNL		± 1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 11111111	± 2	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 00000000 Pad 2 and 20	± 50	nA MAX
Input Resistance	R_{REF}	Pad 4 and 18	8/15	K Ω MIN/ K Ω MAX
$V_{REF A}/V_{REF B}$ Input Resistance Match	$\Delta V_{REF A, B}$		± 1	% MAX
Digital Input High	V_{IH}	$V_{DD} = 5V$ $V_{DD} = 15V$	2.4 13.5	V_{MIN}
Digital Input Low	V_{IL}	$V_{DD} = 5V$ $V_{DD} = 15V$	0.8 1.5	V_{MAX}
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}	± 1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs $0V$ or V_{DD}	1 0.1	mA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	$V_{DD} = \pm 5\%$	0.02	%/% MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

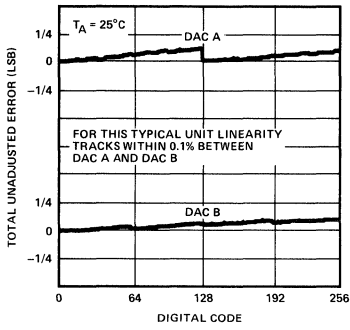
TYPICAL ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$, $T_A = 25^\circ C$, unless otherwise noted. (Note 13)

PARAMETER	SYMBOL	CONDITIONS	PM-7528G	
			TYPICAL	UNITS
Digital Input Capacitance	C_{IN}		6	pF
Output Capacitance	$C_{OUT A}$	DAC Latches Loaded with 00000000	22	pF
	$C_{OUT B}$		22	
Output Capacitance	$C_{OUT A}$	DAC Latches Loaded with 11111111	40	pF
	$C_{OUT B}$		40	
Propagation Delay (Notes 15, 16, 17)	t_{PD}	$V_{DD} = 15V$ $V_{DD} = 5V$	70 150	ns

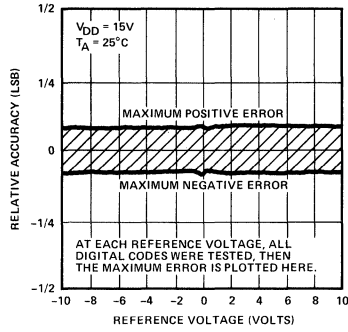


TYPICAL PERFORMANCE CHARACTERISTICS

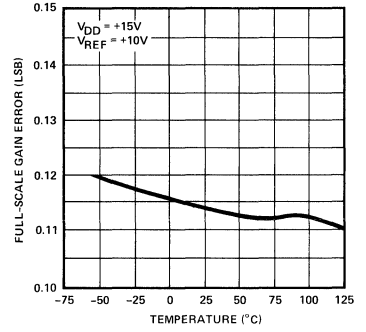
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT



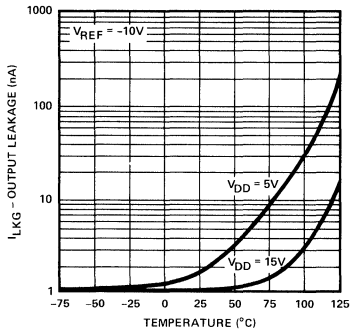
RELATIVE ACCURACY vs REFERENCE VOLTAGE



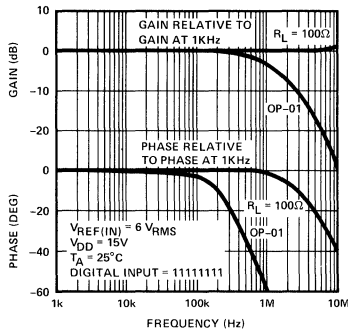
FULL-SCALE GAIN ERROR vs TEMPERATURE



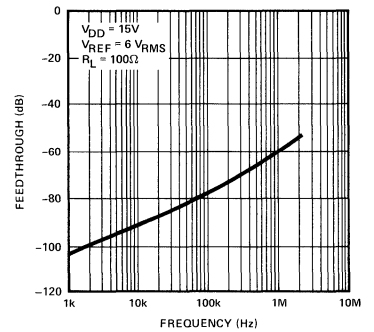
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



GAIN AND PHASE SHIFT vs FREQUENCY WITH RESISTIVE LOAD AND OP-01 AMPLIFIER



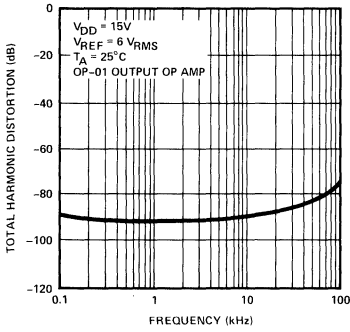
FEEDTHROUGH vs FREQUENCY



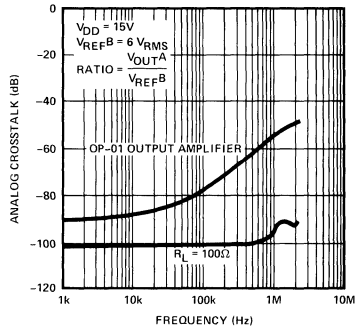


TYPICAL PERFORMANCE CHARACTERISTICS

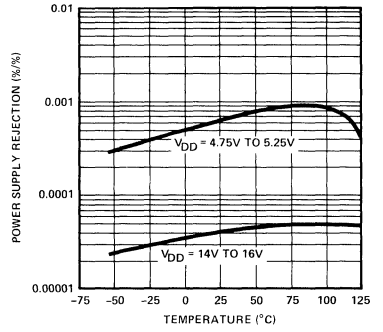
TOTAL HARMONIC DISTORTION vs FREQUENCY



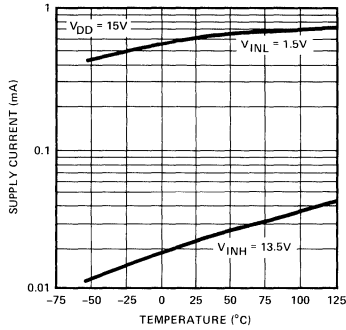
ANALOG CROSSTALK vs FREQUENCY



POWER SUPPLY REJECTION vs TEMPERATURE

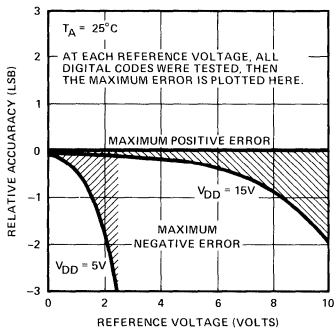


SUPPLY CURRENT vs TEMPERATURE

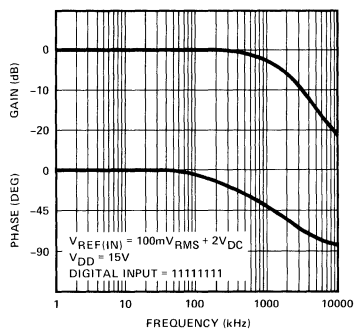


VOLTAGE SWITCHING MODE CHARACTERISTICS

RELATIVE ACCURACY vs REFERENCE VOLTAGE



GAIN AND PHASE vs FREQUENCY





PARAMETER DEFINITIONS

RELATIVE ACCURACY

Relative accuracy, or endpoint nonlinearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale, and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error, or full-scale error, is a measure of the output error between an ideal DAC and the actual device output. The ideal full-scale output is V_{REF} minus 1 LSB. Gain error of both DAC's in the PM-7528 is adjustable to zero with external resistance.

OUTPUT CAPACITANCE

Capacitance from OUT A or OUT B to AGND.

DIGITAL CHARGE INJECTION

The amount of charge injected from the digital inputs to the analog output when the inputs change states. This is normally specified as the area of the glitch in either pAsecs or nVsecs, depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with $V_{REF A}$, $V_{REF B} = AGND$.

PROPAGATION DELAY

This is a measure of the internal delays of the circuit. It is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

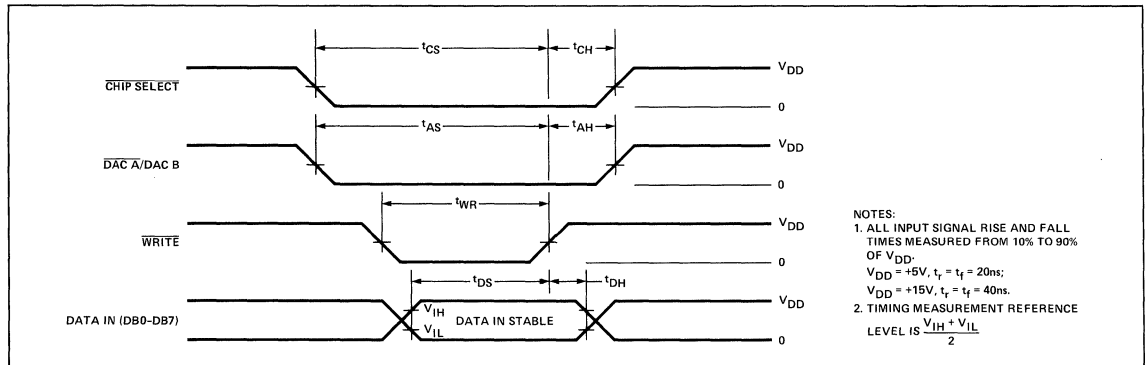
CHANNEL-TO-CHANNEL ISOLATION

The portion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

DIGITAL CROSSTALK

The glitch energy transferred to the output of one converter, due to a change in digital input code to the other converter, specified in nVsec.

WRITE CYCLE TIMING DIAGRAM



NOTES:
 1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD} .
 $V_{DD} = +5V$, $t_r = t_f = 20ns$;
 $V_{DD} = +15V$, $t_r = t_f = 40ns$.
 2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

AC FEEDTHROUGH

AC signal due to capacitive coupling from V_{REF} to output with all switches "off."

INTERFACE LOGIC INFORMATION

DAC SELECTION

Both DAC latches share a common 8-bit input port. The control input DAC A/DAC B selects which DAC can accept data from the input port.

MODE SELECTION

The inputs \overline{CS} and \overline{WR} control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When \overline{CS} and \overline{WR} are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data on the data bit lines DB0-DB7.

HOLD MODE

The selected DAC latch retains the data which was present on the data lines just prior to \overline{CS} or \overline{WR} assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

MODE SELECTION TABLE

DAC A/DAC B	\overline{CS}	\overline{WR}	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

CIRCUIT INFORMATION—D/A SECTION

The PM-7528 contains two identical 8-bit multiplying digital-to-analog converters, DAC A and DAC B. Each DAC includes a stable thin-film R-2R resistor ladder and eight NMOS current steering switches. Figure 1 shows a simplified equivalent circuit

of either DAC. The inverted R-2R ladder takes a voltage or current reference and divides it in a binary manner among the eight current steering switches. The number of switches selected to the output (OUT) add their currents together forming an analog output current representation of the switch selection. The DAC OUT and analog ground (AGND) should be maintained at the same voltage for proper operation.

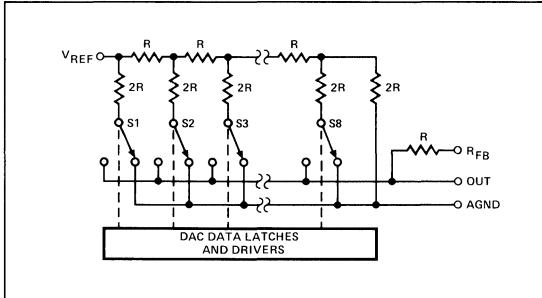


FIGURE 1: Simplified functional circuit for DAC A or DAC B.

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit of DAC A shown in Figure 2 is similar to DAC B. DAC A and DAC B both share the analog ground pin 1 (AGND). With all digital inputs high, the reference current flows to OUT A. A small leakage current ($I_{LEAKAGE}$) flows across internal junctions, doubling every 10°C . The R-2R ladder termination resistor generates a constant $1/256$ current which is

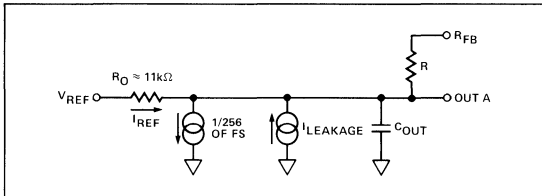


FIGURE 2: PM-7528 DAC A equivalent circuit. All digital inputs high.

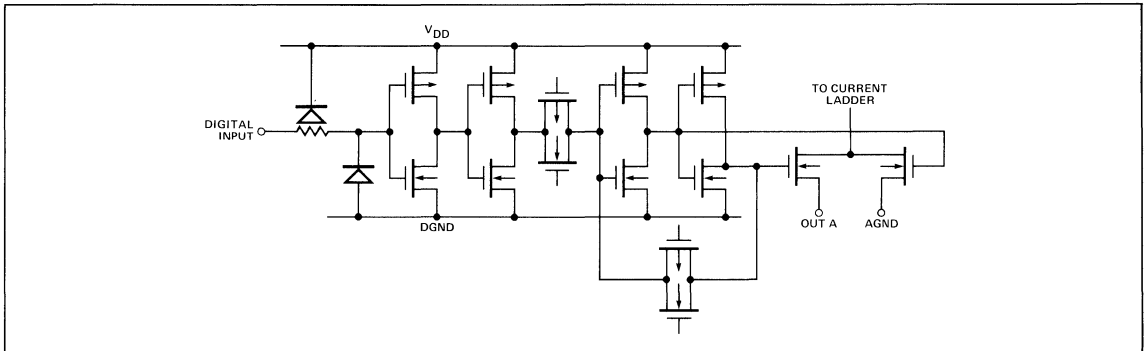


FIGURE 4: Simplified equivalent gate-input protection circuit. One of eight current switches, and its associated internal CMOS-drive-circuitry, is shown.

1 LSB of the reference current (I_{REF}). C_{OUT} is the parallel combination of the NMOS current steering switches. The value of C_{OUT} depends on the number of switches connected to the output. The range of C_{OUT} is 50pF to 120pF maximum. The equivalent output resistance R_O varies with input code from $0.8R$ to $3R$, where R is the nominal ladder resistor of the R-2R ladder.

CIRCUIT INFORMATION—DIGITAL SECTION

The digital inputs provide TTL input compatibility ($V_{INH} = 2.4$, $V_{INL} = 0.8\text{V}$) when the PM-7528 operates with V_{DD} of +5V. The digital inputs effect the amount of quiescent supply current as shown in Figure 3. Peak supply current occurs as the digital input (V_{IN}) passes through the transition voltage. Maintaining the digital input voltages as close as possible to the supplies (V_{DD} and DGND) minimizes supply current consumption. When operating the PM-7528 from CMOS logic the digital inputs are driven very close to the supply rails, minimizing power consumption.

Digital input protection from electrostatic discharge and electrostatic buildup occurs in the input network shown in Figure 4.

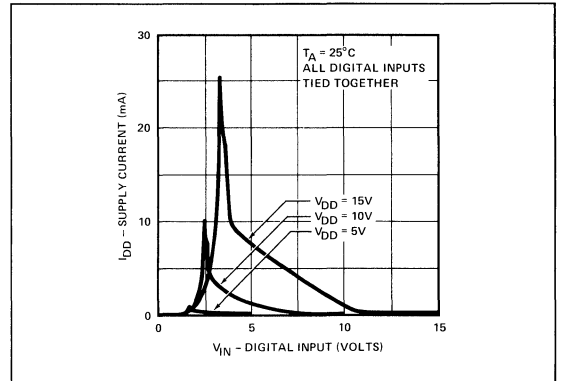
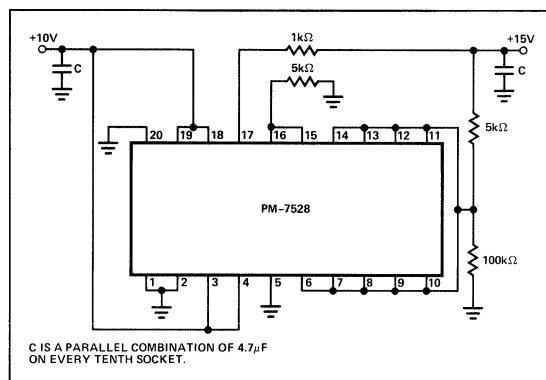


FIGURE 3: Typical plots of supply current, I_{DD} vs logic input voltage (V_{IN}), for $V_{DD} = +5\text{V}$, +10V, and +15V.

BURN-IN CIRCUIT



reference voltage and the digital input code. The reference input voltage can be any value in the range of ±25 volts for both DC or AC signals. The circuit in Figure 5 performs two-quadrant multiplication. Table 1 provides example analog outputs for the given digital input codes.

For bipolar output operation connect the PM-7528 as shown in Figure 6. This circuit configuration provides an offset current, derived from the reference, to enable the output op amp to swing in both polarities. The digital input coding becomes offset binary. Table 2 provides some example analog outputs for various digital inputs (D). The transfer equation for bipolar operation is $V_{OUT} = V_{IN} \times (D/128 - 1)$, where D is the decimal value of the data bit inputs DB0 thru DB7. This circuit provides full four-quadrant multiplication able to accept both polarities on all inputs as well as the circuit output.

APPLICATIONS INFORMATION

The most common application of this DAC is voltage output operation. Unipolar output operation provides a 0 to 10 volt output swing when connected, as shown in Figure 5. The maximum output voltage polarity is the inverse of the input reference voltage, since the op amp inverts the input currents. The transfer equation for unipolar operation is $V_{OUT} = -V_{IN} \times D/256$, where D is the decimal value of the data bit inputs DB0 thru DB7 and V_{IN} is the reference input voltage. The transfer equation highlights another popular application of CMOS DAC's, multiplication. The output voltage is the product of the

APPLICATION HINTS

To ensure system performance consistent with PM-7528 specifications, careful attention must be given to the following points:

1. **GENERAL GROUND MANAGEMENT:** AC or transient voltages between the PM-7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal, is to tie AGND and DGND together at the PM-7528. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that diodes (1N914 or equivalent) be connected in inverse parallel between the PM-7528 AGND and DGND pins.

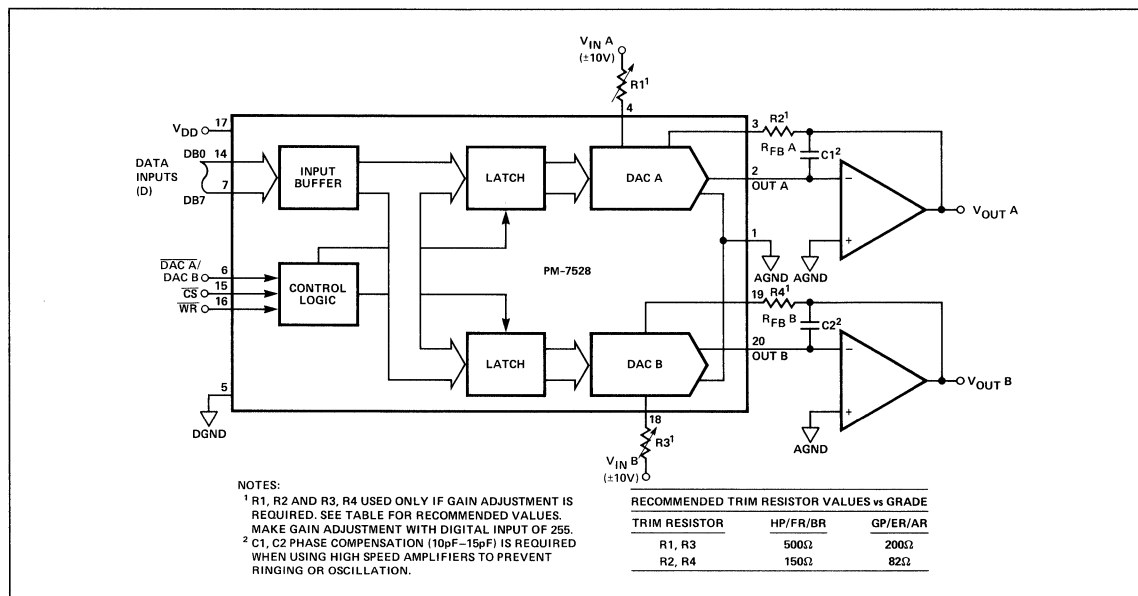


FIGURE 5: Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table 1.

- OUTPUT AMPLIFIER OFFSET:** CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output with a maximum magnitude of $0.67 V_{OS}$ (V_{OS} is amplifier input-offset voltage). This differential nonlinearity term adds to the $R/2R$ differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.
- HIGH-FREQUENCY CONSIDERATIONS:** The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open-loop response; this can cause ringing or oscillation. Stability can be restored by adding a phase-compensation capacitor in parallel with the feedback resistor.
- DYNAMIC PERFORMANCE:** The dynamic performance of the two DACs in the PM-7528 will depend upon the gain and phase characteristics of the output amplifiers, together with the optimum choice of the PC board layout and decoupling components.
- CIRCUIT LAYOUT SUGGESTIONS:** Analog and digital ground traces should be routed between package pins to isolate the digital inputs from the analog circuitry. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, 4-5 to minimize reference feedthrough to the output in multiplying applications. A power supply bypass capacitor (0.1 μ F) is recommended across V_{DD} to DGND.

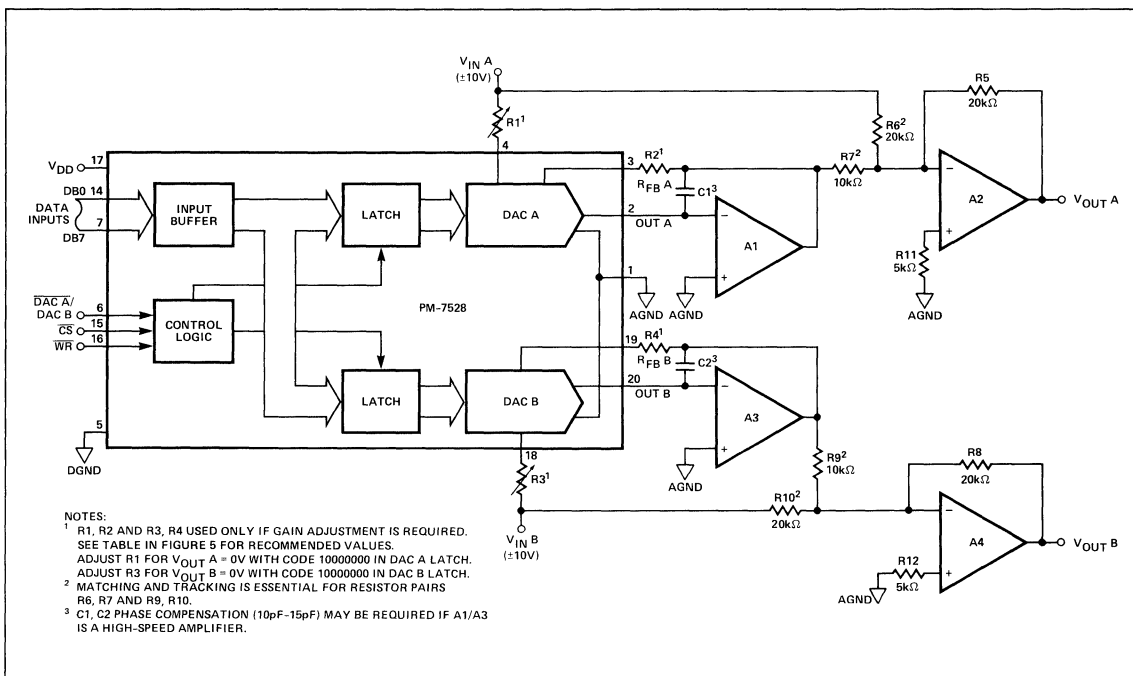


FIGURE 6: Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table 2.

TABLE 1: Unipolar Binary Code Table

DAC LATCH CONTENTS		ANALOG OUTPUT (DAC A or DAC B)
MSB	LSB	
1	11111111	$-V_{IN} \left(\frac{255}{256} \right)$
1	0000001	$-V_{IN} \left(\frac{129}{256} \right)$
1	0000000	$-V_{IN} \left(\frac{128}{256} \right) = -\frac{V_{IN}}{2}$
0	11111111	$-V_{IN} \left(\frac{127}{256} \right)$
0	0000001	$-V_{IN} \left(\frac{1}{256} \right)$
0	0000000	$-V_{IN} \left(\frac{0}{256} \right) = 0$

NOTE: $1 \text{ LSB} = (2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

TABLE 2: Bipolar (Offset Binary) Code Table

DAC LATCH CONTENTS		ANALOG OUTPUT (DAC A or DAC B)
MSB	LSB	
1	11111111	$+V_{IN} \left(\frac{127}{128} \right)$
1	0000001	$+V_{IN} \left(\frac{1}{128} \right)$
1	0000000	0
0	11111111	$-V_{IN} \left(\frac{1}{128} \right)$
0	0000001	$-V_{IN} \left(\frac{127}{128} \right)$
0	0000000	$-V_{IN} \left(\frac{128}{128} \right)$

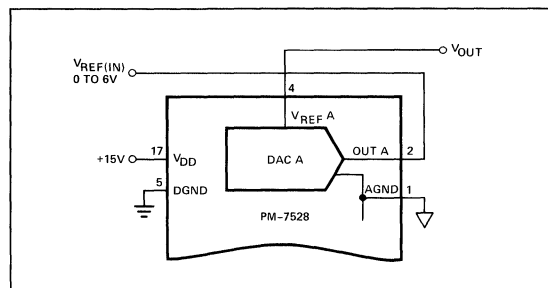
NOTE: $1 \text{ LSB} = (2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

SINGLE SUPPLY OPERATION

With the PM-7528 connected in the voltage switching mode of operation, Figure 7, only one power supply is necessary. There is no voltage inversion between the reference input polarity and the output in the voltage switching mode.

Two characteristic curves in the typical performance characteristics section were generated using this voltage switching mode of operation. The first graph, linearity error versus input reference voltage, shows that to maintain a $\pm\frac{1}{2}$ LSB maximum linearity error, V_{REF} should be less than 1.5 volts for $V_{DD} = 5$ volts or less than 6 volts for $V_{DD} = 15$ volts. The gain-phase response graph shows a dominant pole response for single supply applications where the reference input is an AC signal. In this application the reference input should remain between 1.5 volts and ground when $V_{DD} = 5$ volts. Additionally settling time measures 400 to 500 nano seconds for a digital input change of 255 to 0 when $V_{DD} = 5V$.

The output terminal in the voltage switching mode has a constant output resistance ($\approx 11K\Omega$) independent of the digital input code. The output should be buffered with a voltage follower when driving low impedance loads.


FIGURE 7: PM-7528 in Single Supply, Voltage Switching Mode

PROGRAMMABLE WINDOW COMPARATOR

A programmable window-comparator in Figure 8 will determine if voltage inputs applied to the DAC feedback resistors are within limits programmed into the PM-7528 data latches. The

input signal range depends on the reference and polarity, that is the test input range is 0 to minus V_{REF} . The A and B data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output to logic high.

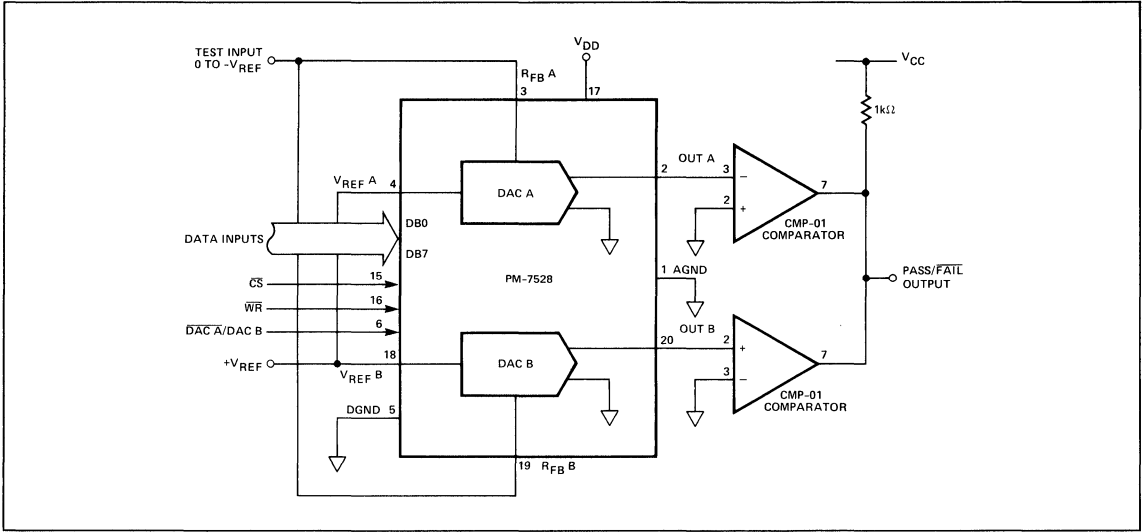


FIGURE 8: Digitally Programmable Window Comparator (Upper and Lower Limit Detector).

MICROPROCESSOR INTERFACE

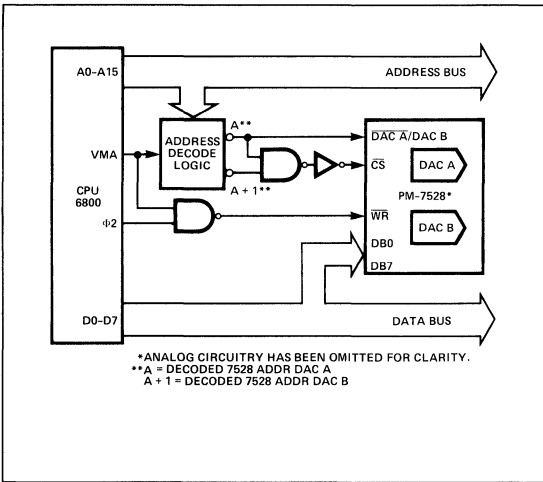


FIGURE 9: PM-7528 Dual DAC to 6800 CPU Interface.

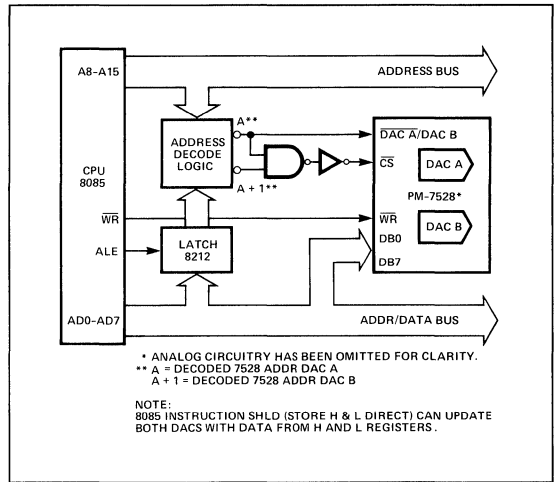


FIGURE 10: PM-7528 Dual DAC to 8085 CPU Interface.

DIGITALLY CONTROLLED SIGNAL ATTENUATOR

Figure 11 shows the PM-7528 configured as a two-channel programmable attenuator. Applications include stereo, audio, and telephone signal-level control applications. In order to

generate logarithmic attenuation, Table 4 was generated based on the equation:

$$\text{Digital Input} = 256 \times \exp\left(\frac{-\text{Attenuation (dB)}}{20}\right)$$

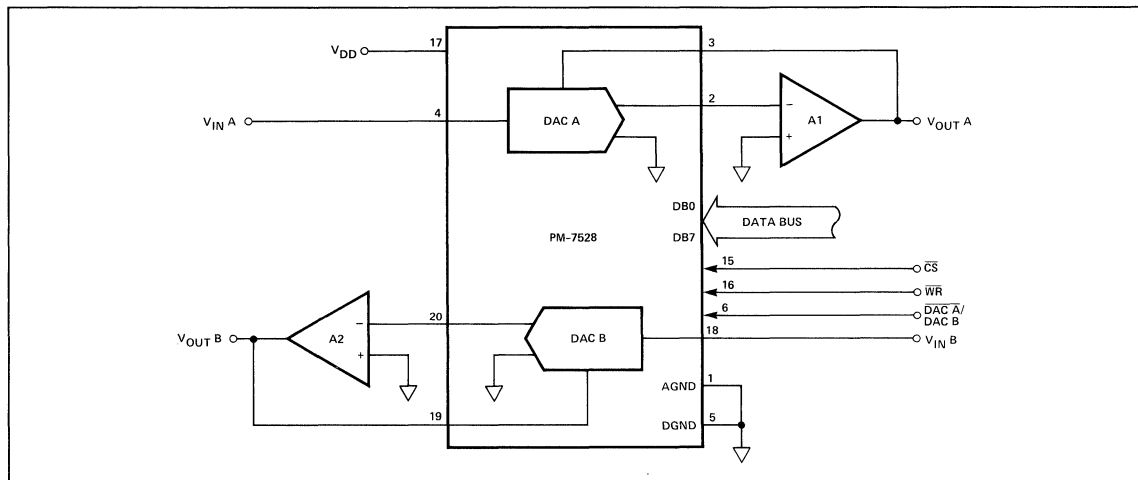


FIGURE 11: Digitally-Controlled Dual Telephone Attenuator.

TABLE 4: Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 11

ATTN. dB	DAC INPUT CODE	CODE IN DECIMAL	ATTN. dB	DAC INPUT CODE	CODE IN DECIMAL
0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 0 0 0 0	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1 1	51
6.5	0 1 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

Precision Monolithics Inc.

FEATURES

- 10-Bit Resolution
- Full Four-Quadrant Multiplication
- Nonlinearity: 1/2 or 1 LSB
- TTL/CMOS Compatible
- Improved Gain Error and Linearity Error from +5V to +15V
- Low Power Consumption
- Low Feedthrough Error
- Low Cost
- AD7520 and AD7533 Replacement
- Full Temperature Operation

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Gain Amplifiers
- Ratiometric A/D Conversion
- Function Generator
- CRT Graphics Generator
- Digitally-Controlled Attenuator
- Digitally-Controlled Power Supplies
- Digital Filters
- Linear Automatic Gain Control

ORDERING INFORMATION†

PACKAGE: 16-PIN**

	MILITARY*	INDUSTRIAL	COMMERCIAL
	TEMPERATURE	TEMPERATURE	TEMPERATURE
	-55°C to +125°C	-25°C to +85°C	0°C to +70°C
NONLINEARITY	±0.1% (±1 LSB)	PM7533BQ	PM7533HP
	±0.05% (±1/2 LSB)	PM7533AQ	PM7533GP

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

**Package Designation: Suffix Q: Hermetic DIP, Suffix P: Epoxy DIP

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7533AQ	AD7533UD	MILITARY
PM7533BQ	AD7533TD	
PM7533BQ	AD7533SD	
PM7533EQ	AD7533CD	INDUSTRIAL
PM7533FQ	AD7533BD	
PM7533FQ	AD7533AD	
PM7533GP	AD7533LN	COMMERCIAL
PM7533HP	AD7533KN	
PM7533HP	AD7533JN	

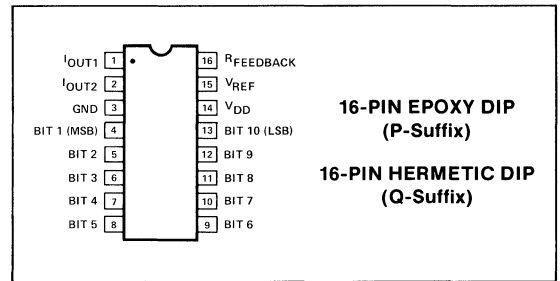
GENERAL DESCRIPTION

The PM-7533 is a 10-bit 4-quadrant multiplying DAC. It is manufactured using thin film on an oxide-isolated, silicon-gate, monolithic CMOS wafer fabrication process. PMI's advanced thin-film resistor processing provides true 10-bit linearity and excellent long-term stability achieved without laser trimming.

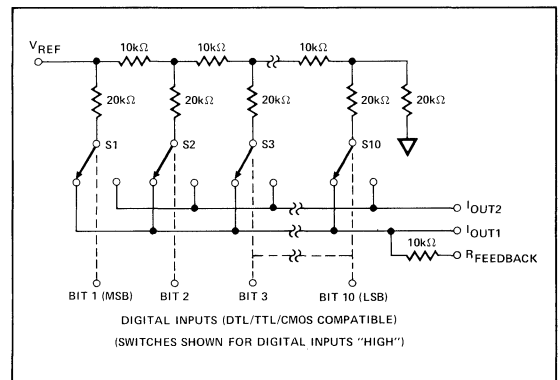
The PM-7533 is pin and function equivalent to the AD7520 and AD7533.

The PMI PM-7533 applications flexibility allows direct interface to TTL or CMOS circuitry and operation from +5V to +15V power supplies. Output scaling is provided by the internal feedback resistor and an external op amp; both positive and negative reference voltages can be accommodated.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} (to GND)	-0.3V, +17V
V_{REF} (to GND)	$\pm 25\text{V}$
R_{FB} (to GND)	$\pm 25\text{V}$
Digital Input Voltage Range	-0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	-0.3V to V_{DD}
Power Dissipation (Package)	
Ceramic (Suffix Q)	
To $+70^\circ\text{C}$	450mW
Derates Above $+75^\circ\text{C}$ By	6mW/ $^\circ\text{C}$
Plastic (Suffix P)	
To $+70^\circ\text{C}$	670mW
Derates Above $+70^\circ\text{C}$ By	8.3mW/ $^\circ\text{C}$
Operating Temperature Range	
Military (AQ, BQ Versions)	-55°C to $+125^\circ\text{C}$
Industrial (EQ, FQ Versions)	-25°C to $+85^\circ\text{C}$
Commercial (GP, HP Versions)	0°C to $+70^\circ\text{C}$

Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$

CAUTION

- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
- The digital control inputs are zener protected, however, permanent damage may occur on unconnected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
- Use proper anti-static handling procedures.
- Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +15\text{V}$, $V_{REF} = +10\text{V}$, $AGND = DGND = 0\text{V}$, $V_{OUT1} = V_{OUT2} = 0\text{V}$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for PM-7533AQ/BQ, $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ apply for PM-7533EQ/FQ, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for PM-7533GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7533A/E/G			PM-7533B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY									
Resolution			10	—	—	10	—	—	Bits
Relative Accuracy (Note 1)			—	—	± 0.05	—	—	± 0.1	% FSR
Gain Error (Notes 2, 3)		$T_A = +25^\circ\text{C}$	—	—	± 1.4	—	—	± 1.4	% FS
		$T_A = \text{Full Temp. Range}$	—	—	± 1.5	—	—	± 1.5	
Power Supply Rejection $\Delta\text{Gain}/\Delta V_{DD}$ (Note 4)	PSRR	$T_A = +25^\circ\text{C}$	—	—	0.005	—	—	0.005	%/%
		$T_A = \text{Full Temp. Range}$	—	—	0.008	—	—	0.008	
Output Leakage Current I_{OUT1} (Pin 1) (Note 6)	I_{LKG1}	$T_A = +25^\circ\text{C}$	—	—	± 50	—	—	± 50	nA
		$T_A = \text{Full Temp. Range}$	—	—	± 200	—	—	± 200	
Output Leakage Current I_{OUT2} (Pin 2) (Note 7)	I_{LKG2}	$T_A = +25^\circ\text{C}$	—	—	± 50	—	—	± 50	nA
		$T_A = \text{Full Temp. Range}$	—	—	± 200	—	—	± 200	
DYNAMIC ACCURACY									
Output Current Settling Time (Notes 5, 8)	t_S	$T_A = +25^\circ\text{C}$ (Note 10)	—	—	600	—	—	600	ns
		$T_A = \text{Full Temp. Range}$	—	—	800	—	—	800	
Feedthrough Error (Notes 5, 10)		$T_A = +25^\circ\text{C}$	—	—	± 0.05	—	—	± 0.05	% FSR
		$T_A = \text{Full Temp. Range}$	—	—	± 0.1	—	—	± 0.1	
REFERENCE INPUT									
Reference Input Resistance (Pin 15) (Note 11)	R_{IN}		5	—	20	5	—	20	k Ω
ANALOG OUTPUTS									
Output Capacitance (Note 5)	C_{OUT1} C_{OUT2}	Digital Inputs = V_{INH}	—	—	220	—	—	220	pF
			—	—	60	—	—	60	
Output Capacitance (Note 5)	C_{OUT1} C_{OUT2}	Digital Inputs = V_{INL}	—	—	120	—	—	120	pF
			—	—	165	—	—	165	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7533AQ/BQ, $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7533EQ/FQ, $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7533GP/HP, unless otherwise noted. (Continued)

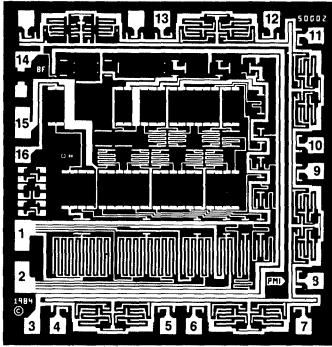
PARAMETER	SYMBOL	CONDITIONS	PM-7533A/E/G			PM-7533B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS									
Digital Input High	V_{INH}		2.4	—	—	2.4	—	—	V
Digital Input Low	V_{INL}		—	—	0.8	—	—	0.8	V
Input Leakage Current	I_{IN}	$V_{IN} = 0V$ and V_{DD}	—	—	± 1	—	—	± 1	μA
Input Capacitance (Note 5)	C_{IN}		—	—	10	—	—	10	pF
POWER REQUIREMENTS									
Power Supply Voltage	V_{DD}		—	—	$+15 \pm 10\%$	—	—	$+15 \pm 10\%$	V
Power Supply Voltage Range	PSR	Accuracy is not guaranteed over this range	+5	—	+16	+5	—	+16	V
Supply Current	I_{DD}	Digital inputs = V_{INL} or V_{INH}	—	—	2	—	—	2	mA

NOTES:

- "FSR" is full-scale range.
- Full-scale (FS) = $-(V_{REF}) \left(\frac{1023}{1024} \right)$; Digital inputs = V_{INH} .
- Maximum gain change from $T_A = +25^\circ C$ to T_{MIN} or T_{MAX} is $\pm 0.1\%$ FSR.
- Digital inputs = V_{INH} , $V_{DD} = +14V$ to $+17V$.
- Guaranteed and not tested.
- Digital inputs = V_{INL} .
- Digital inputs = V_{INH} .
- Settles to 0.05% FSR; $R_{LOAD} = 100\Omega$; digital inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH} .
- AC parameters sample tested to ensure spec compliance.
- Digital input = V_{INL} ; $V_{REF} = 20V_{p-p}$, $f = 100kHz$ Sinewave.
- Absolute temperature coefficient is approximately $+300ppm/^\circ C$.



DICE CHARACTERISTICS



DIE SIZE 0.106 × 0.110 inch, 11,660 sq. mils
(2.692 × 2.794 mm, 7.52 sq. mm)

1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT BIT 1 (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT BIT 2
6. DIGITAL INPUT BIT 3
7. DIGITAL INPUT BIT 4
8. DIGITAL INPUT BIT 5
9. DIGITAL INPUT BIT 6
10. DIGITAL INPUT BIT 7
11. DIGITAL INPUT BIT 8
12. DIGITAL INPUT BIT 9
13. DIGITAL INPUT BIT 10 (LEAST SIGNIFICANT BIT)
14. POSITIVE POWER SUPPLY
15. REFERENCE INPUT VOLTAGE
16. INTERNAL FEEDBACK RESISTOR

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +15V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7533G LIMIT	UNITS
STATIC ACCURACY				
Resolution			10	Bits MIN
Relative Accuracy (Notes 1, 2)			±0.1	% FSR MAX
Gain Error (Notes 2, 3, 4)			±1.4	% FS MAX
Power Supply Rejection $\Delta Gain/\Delta V_{DD}$ (Notes 2, 5, 6)	PSR		0.005	%/ % MAX
Output Leakage Current I_{OUT1} (Notes 2, 7)	I_{LKG1}		±50	nA MAX
Output Leakage Current I_{OUT2} (Notes 2, 8)	I_{LKG2}		±50	nA MAX
REFERENCE INPUT				
Reference Input Resistance (Notes 2, 9)	R_{IN}		5/20	k Ω MIN/MAX



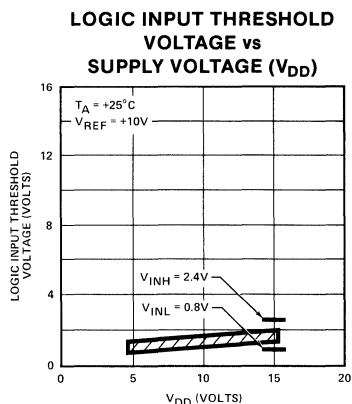
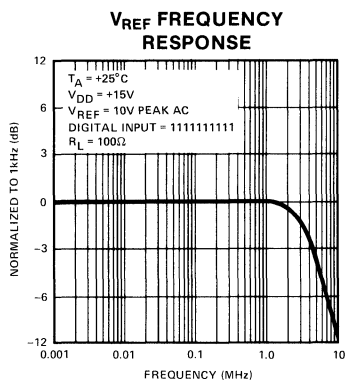
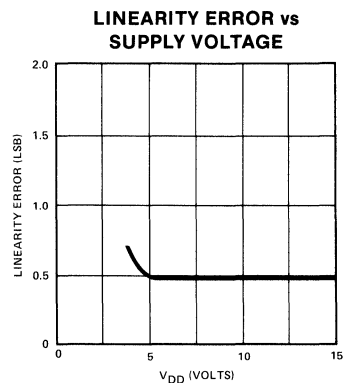
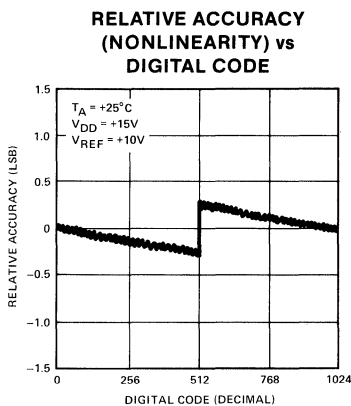
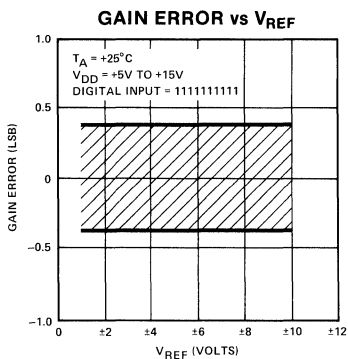
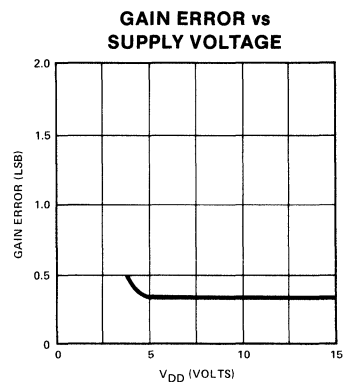
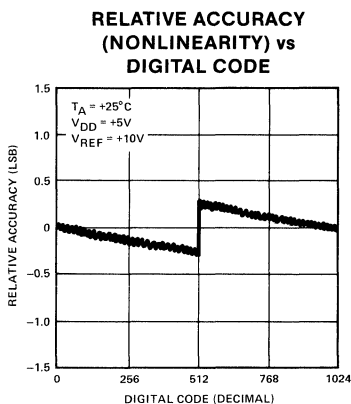
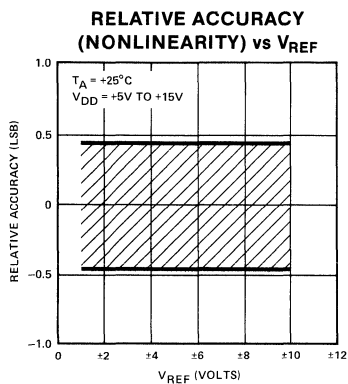
WAFER TEST LIMITS at $V_{DD} = +15V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = +25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7533G LIMIT	UNITS
DIGITAL INPUTS				
Digital Input High (Note 2)	V_{INH}		2.4	V MIN
Digital Input Low (Note 2)	V_{INL}		0.8	V MAX
Input Leakage Current (Note 2)	I_{IN}	$V_{IN} = 0V$ and V_{DD}	± 1	μA MAX
POWER REQUIREMENTS				
Power Supply Voltage	V_{DD}		$+15 \pm 10\%$	V MAX
Supply Current (Note 2)	I_{DD}	Digital Inputs = V_{NL} or V_{INH}	2	mA MAX

NOTES:

- "FSR" is full-scale range.
- DICE final electrical tests are: relative accuracy, gain error, output leakage current, V_{INH} , V_{INL} , PSR, R_{IN} , I_{IN} and I_{DD} at $+25^\circ C$.
- Full-scale (FS) = $-(V_{REF}) \left(\frac{1023}{1024} \right)$; Digital inputs = V_{INH} .
- Maximum gain change from $T_A = +25^\circ C$ to T_{MIN} or T_{MAX} is $\pm 0.1\%$ FSR.
- Digital inputs = V_{INH} , $V_{DD} = +14V$ to $+17V$.
- Guaranteed and not tested.
- Digital inputs = V_{INL} .
- Digital inputs = V_{INH} .
- Absolute temperature coefficient is approximately $+300ppm/^\circ C$.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS


DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where n is equal to the number of bits. Resolution in no way implies linearity.

RELATIVE ACCURACY

Relative accuracy or end-point (nonlinearity) is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1 LSB.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when using the DAC's internal feedback resistor.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches off.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on I_{OUT1} terminal with all digital inputs low or on I_{OUT2} terminal when all inputs are high.

CIRCUIT DESCRIPTION

The PM-7533 is a 10-bit multiplying D/A converter. It consists of a silicon-chrome thin-film R-2R resistor ladder network and ten pairs of NMOS current steering switches, all on a monolithic chip. The NMOS current steering switches are

controlled by CMOS inverters. Most applications require the addition of only an operational amplifier and a current or voltage reference.

An inverted R-2R ladder network in a simplified D/A converter circuit is shown in Figure 1. The current through each ladder leg is switched between I_{OUT1} and I_{OUT2} under the control of the digital inputs. This allows a constant current to be maintained in each ladder leg regardless of the digital-input switch states.

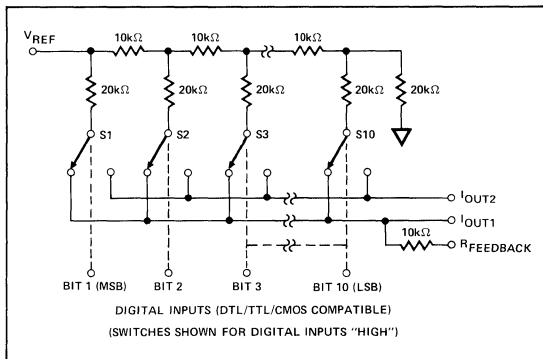


FIGURE 1: SIMPLIFIED DAC CIRCUIT

Figure 2 shows one of ten digital input CMOS inverters driving an NMOS switch. The size of devices 1, 2, and 3 are optimized to make the digital inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives the two inverters (4, 5) and (6, 7), which drives the two NMOS switches (8 and 9). The switch "ON" resistances are binarily-scaled so that the voltage drop across each switch is the same; that is, switch S1 in Figure 1 (8 and 9 of Figure 2) was designed for an "ON" resistance of 20 ohms, switch S2 for 40 ohms, etc. With a 10V reference input, switch S1 current is 0.5mA, switch S2 is 0.25mA, etc. This will maintain a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal so that the D/A converter accuracy is maintained.

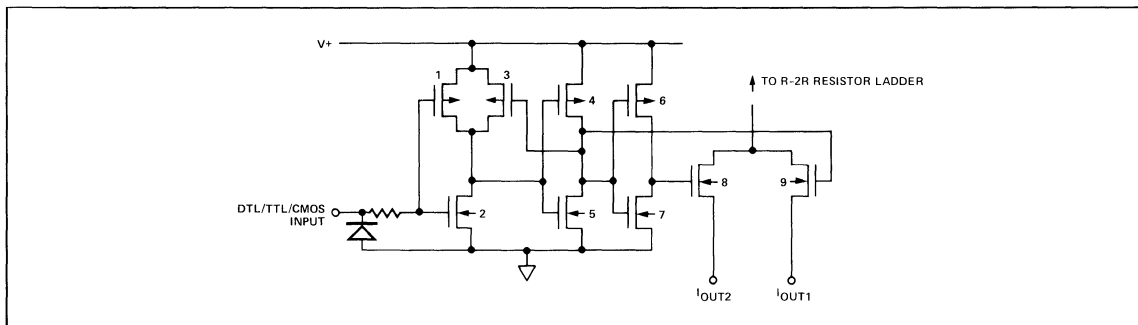


FIGURE 2: CMOS SWITCH

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits of the DAC with all digital inputs high and low respectively. With all digital inputs in the high state as shown in Figure 3, the reference current is switched to the I_{OUT1} terminal, and the I_{OUT2} terminal is open-circuited. Only the output capacitance, surface, leakages, and junction leakages appear at the I_{OUT2} terminal. The $1/1024$ current source is a constant 1-bit current drain through the termination resistor of the R-2R ladder network. The $I_{LEAKAGE}$ current source represents a combination of surface and junction leakages to the substrate. The "ON" capacitance of the output NMOS switch is higher on the I_{OUT1} terminal when all digital inputs are high (MOS transistor gate capacitance increases with applied gate voltage).

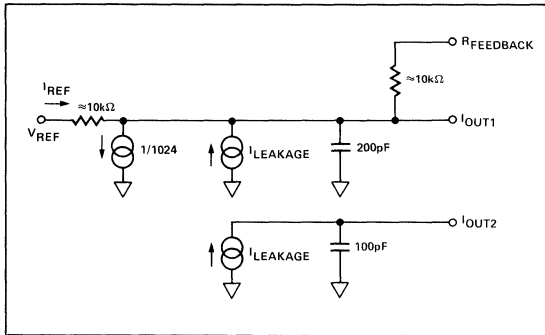


FIGURE 3: EQUIVALENT DAC CIRCUIT
(All digital inputs HIGH).

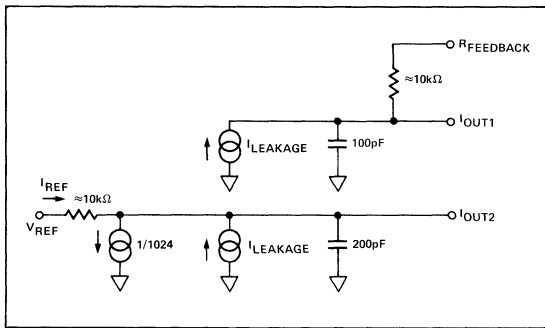


FIGURE 4: EQUIVALENT DAC CIRCUIT
(All digital inputs LOW).

When the conditions are reversed with all digital inputs low as shown in Figure 4, the I_{OUT1} terminal is open-circuited and the current is directed towards the I_{OUT2} terminal.

APPLICATIONS INFORMATION

Figure 5 shows a simple unipolar circuit using the PM-7533. Resistors R1 and R2 are used to trim for full scale. Full-scale output voltage = $-V_{REF} \times (1023/1024)$ with all digital inputs high. Full scale can also be adjusted using V_{REF} thereby eliminating resistors R1 and R2. In many applications, R1 and R2 are not required. Zero-scale output voltage (with all digital inputs low) should be adjusted to less than 10% of 1 LSB using the op amp offset adjust. This will help to keep the nonlinearity errors to a minimum. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high-speed op amps.

The circuit of Figure 5 can be used either as a fixed reference digital-to-analog converter, or can be used with an AC signal at the V_{REF} terminal. Used with a fixed reference voltage, the output voltage range will be from zero to $-V_{REF}$, (the op amp inverts the voltage). The circuit behaves as an attenuator when used with an AC V_{REF} signal. The input voltage range is $\pm 20V$, but this voltage will be limited by the op amp voltage range. The digital-input-code versus analog-output-voltage is shown in Table I. The transfer function is:

$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \dots + \frac{A_{10}}{2^{10}} \right)$$

where $A_1 \dots A_{10}$ assumes a value of 1 for an ON bit and 0 for an OFF bit.

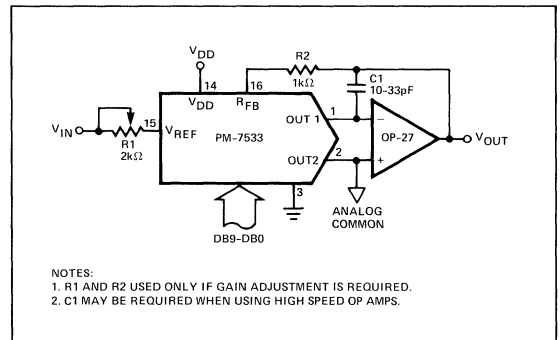


FIGURE 5: UNIPOLAR BINARY OPERATION
(2-QUADRANT MULTIPLICATION)

TABLE I: UNIPOLAR BINARY CODE TABLE

DIGITAL INPUT MSB	LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1	1 1 1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{1023}{1024} \right)$
1	0 0 0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{513}{1024} \right)$
1	0 0 0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{512}{1024} \right) = \frac{V_{REF}}{2}$
0	1 1 1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{511}{1024} \right)$
0	0 0 0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{1}{1024} \right)$
0	0 0 0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{0}{1024} \right) = 0$

NOTES:

1. Nominal full scale for the circuit of Figure 5 is given by

$$FS = -V_{REF} \left(\frac{1023}{1024} \right)$$

2. Nominal LSB magnitude for the circuit of Figure 5 is given by

$$LSB = V_{REF} \left(\frac{1}{1024} \right) \text{ or } V_{REF} (2^{-n})$$

Figure 6 shows a simple bipolar output circuit using the PM-7533 and a PMI OP-215 dual op amp. The circuit uses offset binary coding and a fixed DC voltage for V_{REF} . Digitally-controlled attenuation of an AC signal occurs when the signal is used as the signal source at V_{REF} . Negative output full-scale is adjusted by setting the digital inputs to all zeros and adjusting the value of the V_{REF} voltage or $R5$. The zero-scale output voltage is adjusted while the digital inputs

are set to 1000000000 and adjusting $R1$ for a zero output voltage (less than 10% of 1 LSB). Resistors $R3$, $R4$ and $R5$ must be selected for matching and tracking in order to keep offset and full scale errors to a minimum. Resistors $R1$ and $R2$ temperature coefficients must be taken into account if they are used. $C1$ phase compensation capacitor may not be needed and should be selected empirically. The digital input code versus analog output voltage is shown in Table II.

TABLE II: BIPOLAR (OFFSET BINARY) CODE TABLE

DIGITAL INPUT MSB	LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1	1 1 1 1 1 1 1 1 1 1	$+V_{REF} \left(\frac{511}{512} \right)$
1	0 0 0 0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{512} \right)$
1	0 0 0 0 0 0 0 0 0 0	0
0	1 1 1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{1}{512} \right)$
0	0 0 0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{511}{512} \right)$
0	0 0 0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{512}{512} \right)$

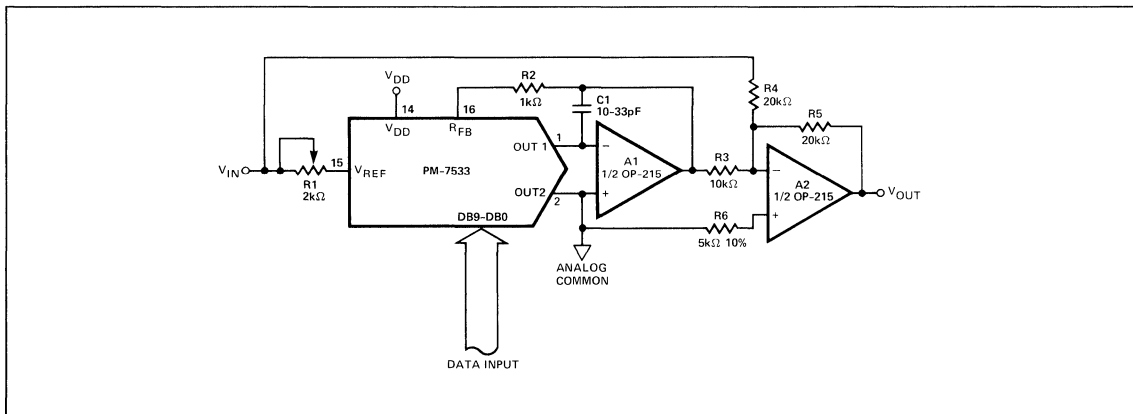
NOTES:

1. Nominal full scale for the circuit of Figure 6 is given by

$$FSR = V_{REF} \left(\frac{512}{512} \right)$$

2. Nominal LSB magnitude for the circuit of Figure 6 is given by

$$LSB = V_{REF} \left(\frac{1}{512} \right)$$


FIGURE 6: BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The PM-7533 may be used in the voltage output operation as shown in Figure 7. This circuit configuration will lend itself to single-supply operation because signal inversion does not occur. The output should be buffered due to its high output resistance (10kΩ) to prevent loading errors. The reference voltage should be kept to +1.5 volts maximum to keep nonlinearity errors to less than 1 LSB as shown in Figure 8.

By connecting the DAC in the feedback of an op amp as shown in Figure 9, the circuit behaves as a programmable gain amplifier (analog/digital divider). The transfer function is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \dots + \frac{A_{10}}{2^{10}}} \right)$$

where $A_1 \dots A_{10}$ assumes a value of 1 or 0.

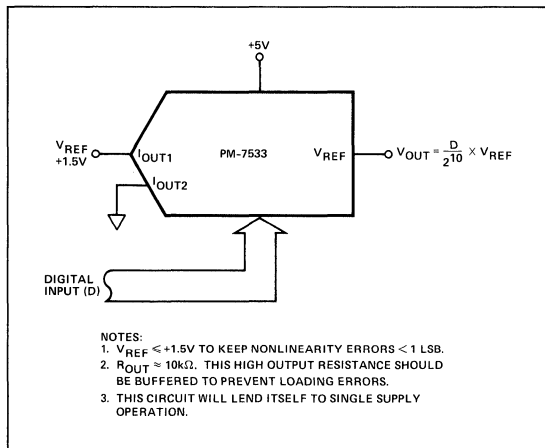


FIGURE 7: VOLTAGE OUTPUT OPERATION

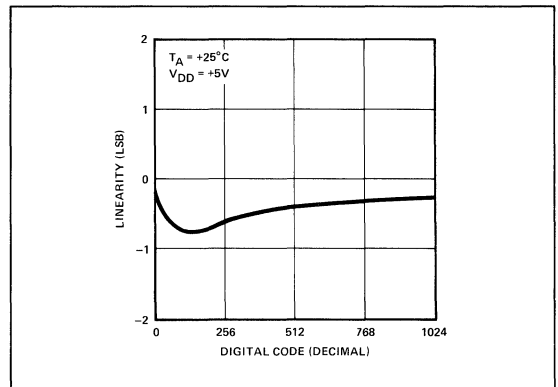


FIGURE 8: VOLTAGE MODE

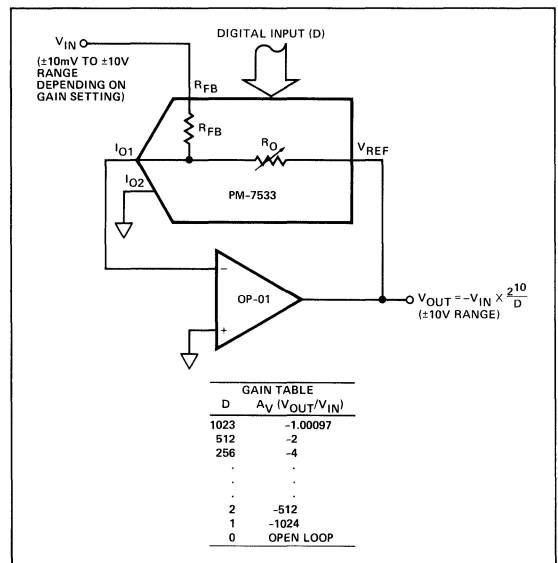


FIGURE 9: PROGRAMMABLE GAIN AMPLIFIER



PM-7541

CMOS 12-BIT MONOLITHIC MULTIPLYING D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- Full Four-Quadrant Multiplication
- 12-Bit Endpoint Linearity ($\pm 1/2$ LSB)
- Pretrimmed Gain
- TTL/CMOS Compatible
- Low Power Consumption
- Low Feedthrough Error
- Direct Replacement for AD7521 and AD7541
- Superior Power Supply Rejection from +5V to +15V
- Low Gain and Linearity Tempcos (TYP 2ppm of FSR/ $^{\circ}$ C)
- Latch-Up Resistant

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Amplifiers
- Ratiometric A/D Conversion
- Function Generator
- CRT Graphics Generator
- Digitally-Controlled Attenuator
- Digitally-Controlled Power Supplies
- Digital Filters

ORDERING INFORMATION†

NONLINEARITY	PACKAGE: 18-PIN**		
	MILITARY* TEMPERATURE -55 $^{\circ}$ C TO +125 $^{\circ}$ C	INDUSTRIAL TEMPERATURE -25 $^{\circ}$ C TO +85 $^{\circ}$ C	COMMERCIAL TEMPERATURE 0 $^{\circ}$ C TO +70 $^{\circ}$ C
1 LSB	PM7541BX	PM7541FX	PM7541HP
1/2 LSB	PM7541AX	PM7541EX	PM7541GP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
(also available in Side Braze—XB)

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

** Package Designation:

Suffix X: Hermetic DIP (XB - Side Braze)
Suffix P: Epoxy DIP

CROSS REFERENCE

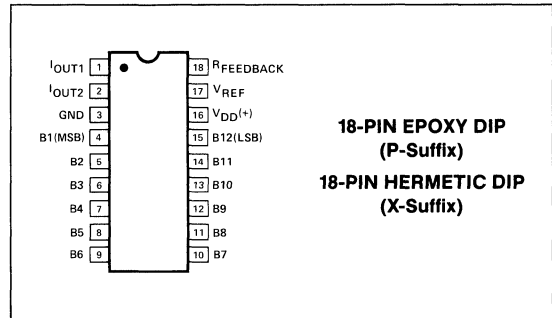
PMI	ADI	TEMPERATURE RANGE
PM7541AX	AD7541TD	MILITARY
PM7541BX	AD7541SD	
PM7541EX	AD7541BD	INDUSTRIAL
PM7541FX	AD7541AD	
PM7541GP	AD7541KN	COMMERCIAL
PM7541HP	AD7541JN	

GENERAL DESCRIPTION

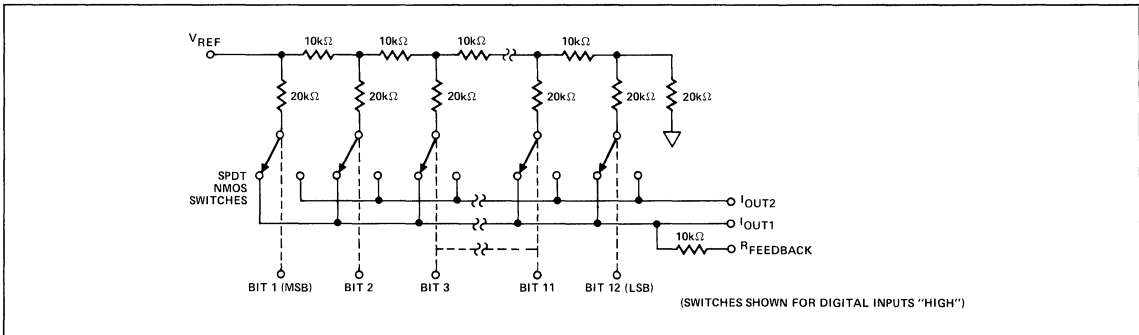
The PMI PM-7541 is a 12-bit, 4-quadrant multiplying digital-to-analog converter. It is manufactured using an advanced oxide-isolated, silicon-gate, monolithic CMOS technology.

Laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity and excellent absolute accuracy. The low power dissipation, together with NMOS temperature-compensating switches, assures the performance over the full temperature range. It is a pin-compatible replacement for Analog Devices AD7521 and AD7541 with equal or better performance.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



DIGITAL-TO-ANALOG CONVERTERS

11

**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} (to GND)	+17V
V _{REF} (to GND)	±25V
Digital Input Voltage Range	V _{DD} to GND
Output Voltage (Pin 1, Pin 2)	-0.3V to V _{DD}
Power Dissipation (Package)	450mW
Derate Above +75°C	6mW/°C
Operating Temperature Range	
AX/BX Versions	-55°C to +125°C
EX/FX Versions	-25°C to +85°C
GP/HP Versions	0°C to +70°C

Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 17) and R_{FB} (Pin 18).
2. The digital control inputs are zener protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT1} = V_{OUT2} = 0V; and T_A = -55°C to +125°C apply for PM-7541AX/BX; T_A = -25°C to +85°C apply for PM-7541EX/FX; and T_A = 0°C to +70°C apply for PM-7541GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7541A/E/G			PM-7541B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Nonlinearity (Notes 1, 2)	INL		—	—	±1/2	—	—	±1	LSB
Gain Error (Notes 3, 4)	G _{ER}	T _A = +25°C T _A = Full Temp. Range	—	—	±12.5 ±16.7	—	—	±12.5 ±16.7	LSB
Power Supply Rejection ΔGain/ΔV _{DD}	PSRR	V _{DD} = +14.5V to +15.5V T _A = +25°C T _A = Full Temp. Range	—	—	±0.01 ±0.02	—	—	±0.01 ±0.02	%/%
Output Leakage Current (I _{OUT1}) (Notes 5, 6)	I _{LKG}	T _A = +25°C T _A = Full Temp. Range	—	—	±50 ±200	—	—	±50 ±200	nA
DYNAMIC PERFORMANCE									
Output Current Settling Time (Note 7)	t _S	To ±1/2 LSB of FSR	—	—	1.0	—	—	1.0	μs
Feedthrough Error (Note 7)		V _{REF} = 20V _{p-p} @ f = 10kHz All digital inputs low	—	—	1.0	—	—	1.0	mV _{p-p}
REFERENCE INPUT									
Input Resistance (Note 8)	R _{REF}		5	—	20	5	—	20	kΩ
DIGITAL INPUTS									
Digital Input High	V _{IH}		2.4	—	—	2.4	—	—	V
Digital Input Low	V _{IL}		—	—	0.8	—	—	0.8	V
Input Leakage Current	I _{IL}	V _{IN} = 0 to 15V	—	—	±1	—	—	±1	μA
Input Capacitance (Note 7)	C _{IN}		—	—	10	—	—	10	pF
Input Coding		(Tables 1, 2)	Binary or Offset			Binary or Offset			



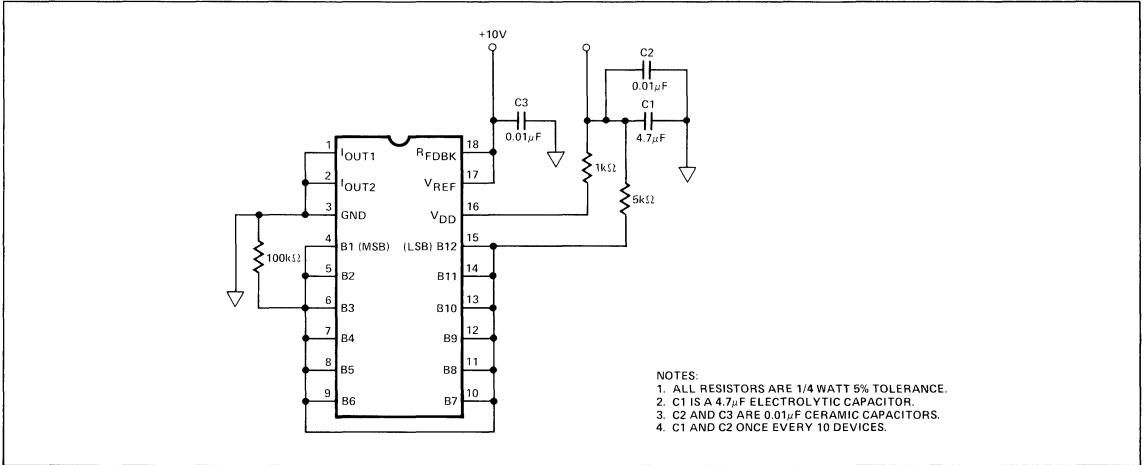
ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$; and $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7541AX/BX; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7541EX/FX; and $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7541GP/HP, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7541A/E/G			PM-7541B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUTS									
Output Capacitance (Note 7)	C_{OUT1}	Digital Inputs = V_{IH}	—	189	220	—	189	220	pF
	C_{OUT2}		—	36	60	—	36	60	
Output Capacitance (Note 7)	C_{OUT1}	Digital Inputs = V_{IL}	—	95	120	—	95	120	pF
	C_{OUT2}		—	134	165	—	134	165	
POWER SUPPLY									
V_{DD} Range	V_{DD}	Accuracy is not guaranteed over this range.	+5	—	+16	+5	—	+16	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	—	—	2	—	—	2	mA

NOTES:

1. A/E/G versions are monotonic to 12-bits.
2. B/F/H versions are monotonic to 11-bits.
3. Using internal feedback resistor.
4. Maximum gain change from $+25^\circ C$ to T_{MAX} or T_{MIN} is ± 4.2 LSB maximum.
5. Digital Inputs = V_{IL} .
6. Specification also applies for I_{OUT2} with all digital inputs = V_{IH} .
7. Guaranteed and not tested.
8. Absolute temperature coefficient is approximately $+300$ ppm/ $^\circ C$.

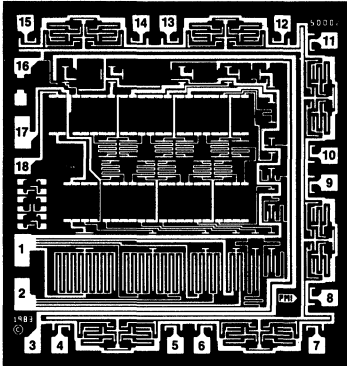
BURN-IN CIRCUIT



- NOTES:
1. ALL RESISTORS ARE 1/4 WATT 5% TOLERANCE.
 2. C1 IS A 4.7μF ELECTROLYTIC CAPACITOR.
 3. C2 AND C3 ARE 0.01μF CERAMIC CAPACITORS.
 4. C1 AND C2 ONCE EVERY 10 DEVICES.



DICE CHARACTERISTICS



DIE SIZE 0.110 × 0.106 inch, 11,660 sq. mils
(2.692 × 2.794 mm, 7.52 sq. mm)

For additional DICE information refer to
1986 Data Book, Section 2.

1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT (BIT 1) (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT (BIT 2)
6. DIGITAL INPUT (BIT 3)
7. DIGITAL INPUT (BIT 4)
8. DIGITAL INPUT (BIT 5)
9. DIGITAL INPUT (BIT 6)
10. DIGITAL INPUT (BIT 7)
11. DIGITAL INPUT (BIT 8)
12. DIGITAL INPUT (BIT 9)
13. DIGITAL INPUT (BIT 10)
14. DIGITAL INPUT (BIT 11)
15. DIGITAL INPUT (BIT 12) (LEAST SIGNIFICANT BIT)
16. POSITIVE POWER SUPPLY
17. REFERENCE INPUT VOLTAGE
18. INTERNAL FEEDBACK RESISTOR

WAFER TEST LIMITS at $V_{DD} = +15V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = +25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	PM-7541G			UNITS
			MIN	TYP	MAX	
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Nonlinearity	INL		—	—	±1	LSB
Gain Error (Note 1)	G_{ER}		—	—	±12.5	LSB
Power Supply Rejection	PSRR	$V_{DD} = +14.5V$ to $+15.5V$	—	—	±0.01	%/%
Output Leakage Current (I_{OUT1}) (Note 2)	I_{LKG}	Digital Inputs = V_{IL}	—	—	±50	nA
REFERENCE INPUT						
Input Resistance	R_{REF}		5	—	20	k Ω
DIGITAL INPUTS						
Digital Input High	V_{IH}		2.4	—	—	V
Digital Input Low	V_{IL}		—	—	0.8	V
Input Leakage Current	I_{IL}	$V_{IN} = 0$ to $15V$	—	—	±1	μA
POWER SUPPLY						
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	—	—	2	mA

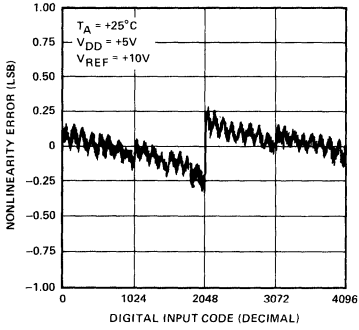
NOTES:

1. Using internal feedback resistor.
 2. Specification also applies for I_{OUT2} but all Digital Inputs = V_{IH} .
- Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

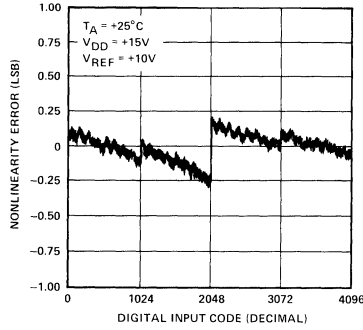


TYPICAL PERFORMANCE CHARACTERISTICS

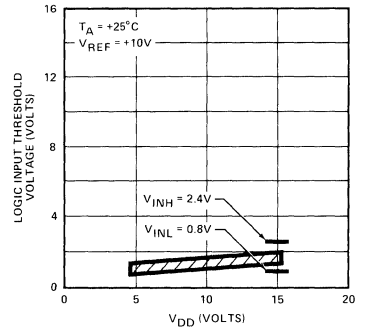
NONLINEARITY ERROR vs DIGITAL CODE



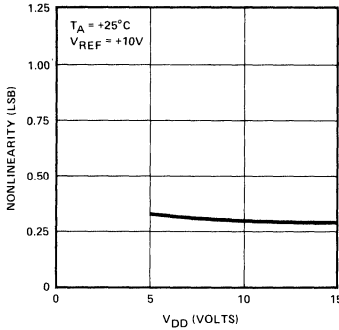
NONLINEARITY ERROR vs DIGITAL CODE



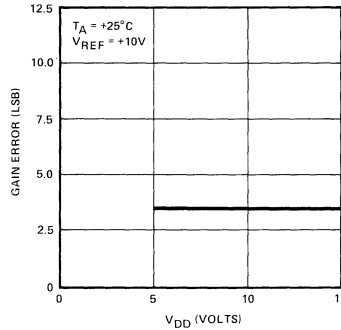
LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE (V_{DD})



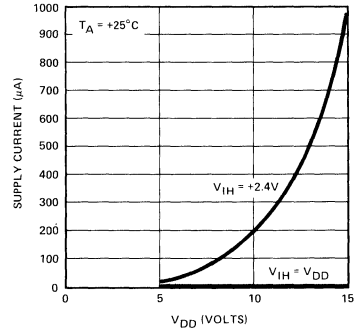
NONLINEARITY vs SUPPLY VOLTAGE



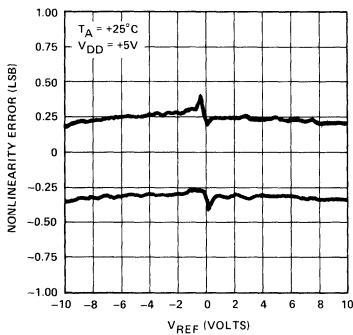
GAIN ERROR vs SUPPLY VOLTAGE



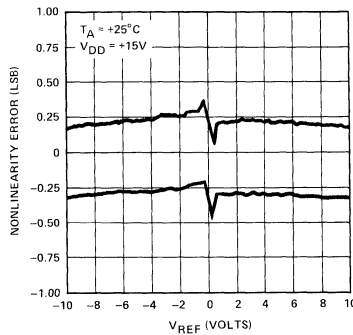
SUPPLY CURRENT vs SUPPLY VOLTAGE

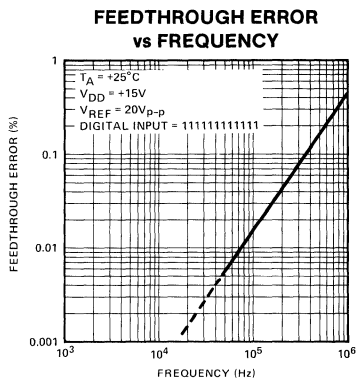
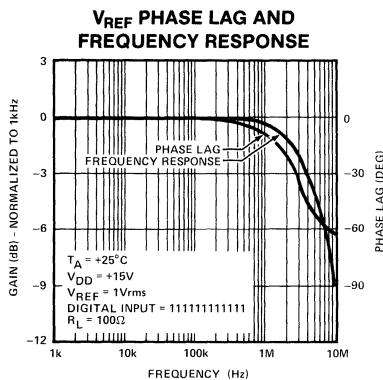


NONLINEARITY ERROR vs REFERENCE VOLTAGE



NONLINEARITY ERROR vs REFERENCE VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS

SPECIFICATION DEFINITIONS
RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus; i.e., zero to full scale.

GAIN

Ratio of the DAC's external-operational-amplifier output voltage to the V_{REF} input voltage.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} or I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on I_{OUT1} terminal with all digital inputs LOW, or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION
GENERAL CIRCUIT INFORMATION

The PM-7541 is a 12-bit multiplying D/A converter consisting of a highly-stable, silicon-chrome thin film R-2R ladder network and twelve pairs of NMOS current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the PM-7541 is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between I_{OUT1} and I_{OUT2} BUS lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

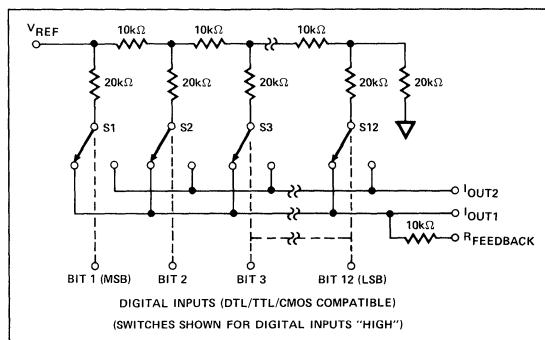
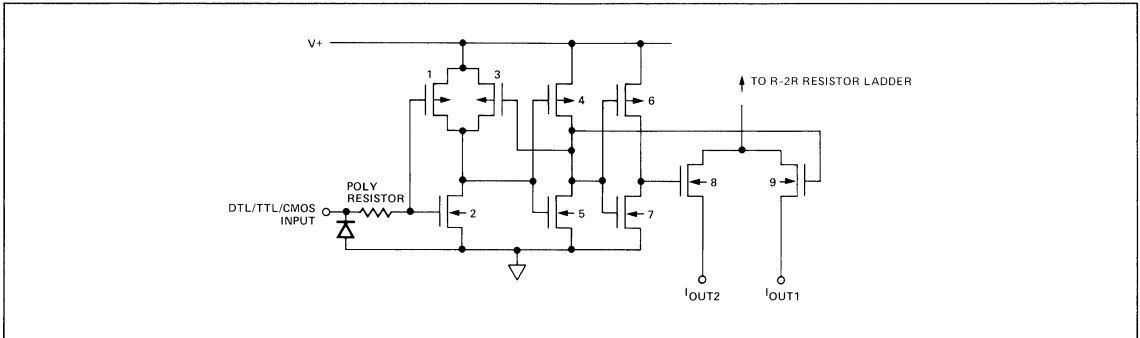
FIGURE 1: SIMPLIFIED DAC CIRCUIT


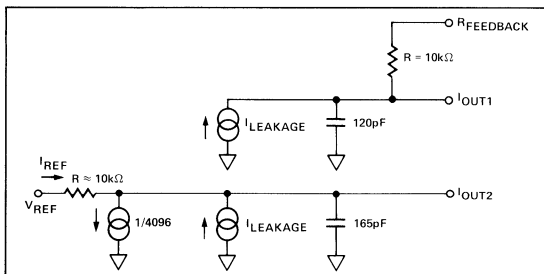
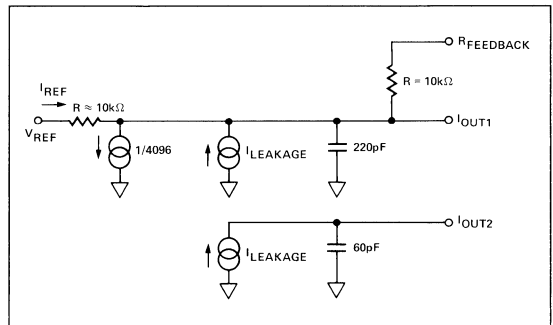
FIGURE 2: CMOS SWITCH


One of the twelve CMOS switches is shown in Figure 2. The digital input stage, devices 1, 2, and 3, drives the two inverters, devices 4, 5, 6, and 7; these inverters in turn drive the two output current steering switches, devices 8 and 9. Devices 1, 2, and 3 are designed such that the digital control inputs are DTL, TTL, and CMOS compatible over the full military temperature range.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., then with a 10 volt reference input, the current through switch 1 is 0.5mA, switch 2 is 0.25mA, etc., a constant 5mV drop will then be maintained across each switch.

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show the equivalent circuits for all digital inputs LOW and HIGH respectively. The reference current is switched to I_{OUT2} when all inputs are LOW and I_{OUT1} when inputs are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant 1-bit current drain through the ladder terminating resistor. The output capacitance is dependent upon the digital input code, and is therefore modulated between the low and high values.

FIGURE 3: PM-7541 EQUIVALENT CIRCUIT (ALL INPUTS LOW)

FIGURE 4: PM-7541 EQUIVALENT CIRCUIT (ALL DIGITAL INPUTS HIGH)


DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, is also modulated by the digital input code. The resistance looking back into the I_{OUT1} terminal, may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). The static accuracy and dynamic performance will be affected by this modulation. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7541. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase Compensation (See Figures 5 and 6).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

APPLICATIONS INFORMATION

APPLICATION TIPS

Linearity depends upon the potential of I_{OUT1} and I_{OUT2} (pins 1 and 2) being exactly equal to GND (pin 3). In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground, see Figures 5 and 6. The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifiers usual bias current compensation resistor in the noninverting input should not be used; the input should be connected directly to ground with a low-resistance wire. This resistor can cause a variable offset voltage contributing an error. All pins going to ground should be taken to a common point to avoid ground loops. The V_{DD} power supply should have a low noise level and not have transients greater than +17V.

Unused digital inputs must always be grounded or taken to V_{DD} ; this will prevent noise from triggering the high impedance digital input resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value ($1M\Omega$) resistor; this will prevent the accumulation of static charge whenever the PC card is disconnected from the system.

OUTPUT AMPLIFIER CONSIDERATIONS

For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been pointed out that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input-terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

FIGURE 5: UNIPOLAR BINARY OPERATION (2-QUADRANT)

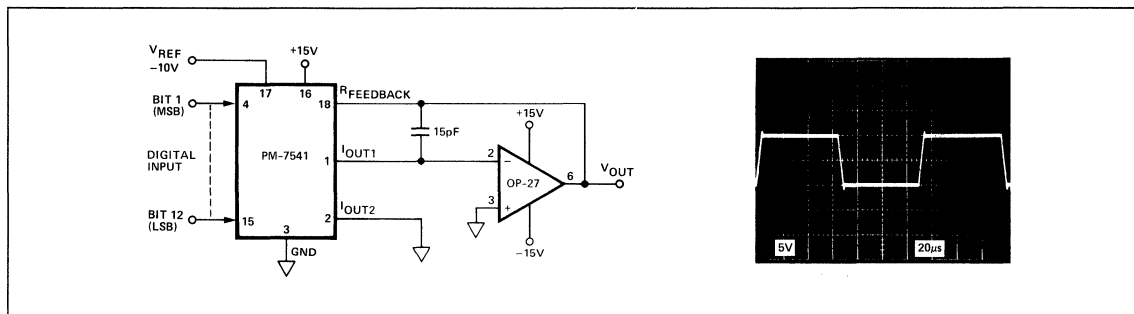
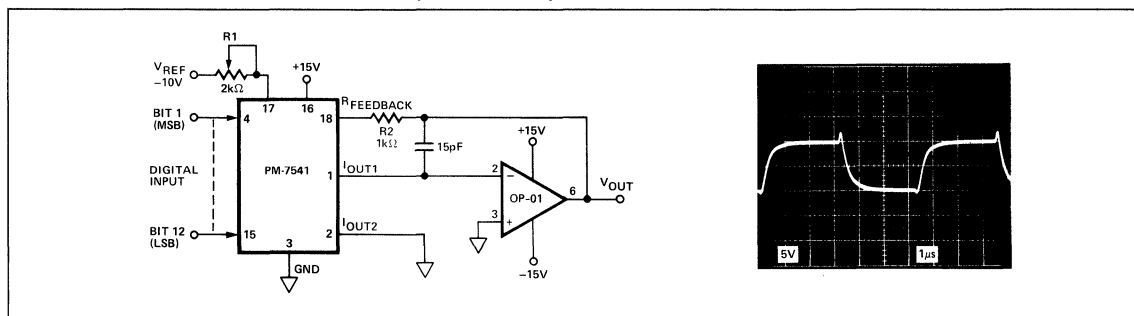


FIGURE 6: UNIPOLAR BINARY OPERATION (2-QUADRANT)





The static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 8 and the equation:

$$\text{Error Voltage} = V_{OS} \left(1 + \frac{R_{FB}}{R_O} \right)$$

where R_O = function of digital code.
 $R_O \cong 10k\Omega$ for more than 4-bits of logic 1.
 $R_O \cong 30k\Omega$ for any single bit logic 1.

Therefore, the offset gain varies as follows:

$$\text{At code } 001111111111: V_{ERROR1} = V_{OS} \left(1 + \frac{10k\Omega}{10k\Omega} \right) = 2 V_{OS}$$

$$\text{At code } 010000000000: V_{ERROR2} = V_{OS} \left(1 + \frac{10k\Omega}{30k\Omega} \right) = \frac{4}{3} V_{OS}$$

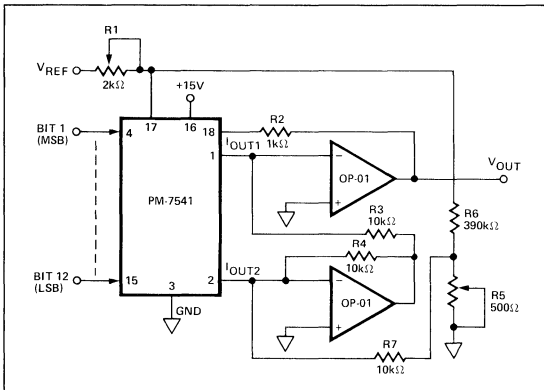
The error difference is $2/3 V_{OS}$.

Since one LSB has a weight (for $V_{REF} = +10V$) of 2.5mV for the PM-7541 DAC, it is clearly important that V_{OS} be nulled, either using the amplifier's nulling pins or an external network.

APPLICATIONS

Figures 5, 6, and 7 show simple unipolar and bipolar circuits with their associated waveforms using the PM-7541 and two PMI types of output amplifiers. A small feedback capacitor should be used across the amplifier to help prevent overshoot and ringing when using high-speed op amps. Resistor R1 is used to trim for full scale, low tempco (approximately 50ppm/°C) resistors or trim pots should be selected when gain adjustments are required.

FIGURE 7: BIPOLAR OPERATION (4-QUADRANT)



UNIPOLAR BINARY OPERATION (2-QUADRANT)

The circuits of Figures 5 and 6 can either be used as a fixed reference D/A converter, or as an attenuator with an AC input voltage. In the fixed reference mode, the DAC provides an analog output voltage in the range of zero to plus or minus V_{REF} , depending on V_{REF} polarity. The reference input voltage can range between $-20V$ to $+20V$; this is due to the ability of V_{REF} being able to exceed V_{DD} , the limiting factor being the op amp voltage range. Table 1 shows the code relationship for the circuit of Figure 6. R1 can be omitted with a resulting maximum gain error of 0.3% of full scale.

Table 1: Code Table for Circuit of Figure 6

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-0.99975 V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0	$-0.50000 V_{REF}$
0 1 1 1 1 1 1 1 1 1 1 1 1 1	$-0.49975 V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

BIPOLAR BINARY OPERATION (FOUR-QUADRANT)

The recommended circuit and code relationship is shown in Figure 7 and Table 2. The digital input is offset binary coded and multiplies V_{REF} per Table 2. Resistors R3 and R4 should be equal within 0.1% at all temperatures, but need not track the resistors within the PM-7541. The network comprised of R5, R6, and R7 sums 1/2 LSB of current into I_{OUT2} to ensure correct coding at zero. R1 can be adjusted to produce the outputs shown in Table 2. However, when the application permits it, R1 and R2 should be omitted. The maximum gain error in this condition is 0.3% of full scale. R5 may be replaced by a 100Ω fixed resistor; the maximum zero error is then 0.015% of full scale. The input offset voltage of both amplifiers should be adjusted to less than 0.1mV and be better than 0.5mV over the temperature range of interest. With V_{REF} set to 10V, R5 is adjusted so that with code 100000000000, $V_{OUT} = 0V \pm 0.2mV$. R1 is adjusted so that code 000000000000 causes V_{OUT} to equal V_{REF} .

Table 2: Code Table for Circuit of Figure 7

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-0.99951 V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 0 0 1	$-0.00049 V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 0 0 0	0
0 1 0 0 0 0 0 0 0 0 0 0 0 0	$+0.50000 V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 0 0 0	$+1.00000 V_{REF}$

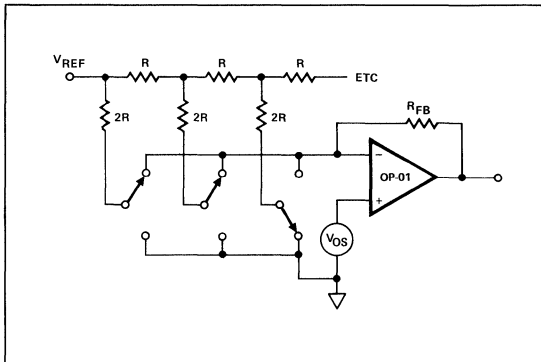
OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately +10V.
2. Set R5 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT2} amplifier offset trimpot for $0V \pm 0.1mV$ at I_{OUT2} amplifier output.
5. Connect a short circuit across R4.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset trimpot for $0V \pm 0.1mV$ at I_{OUT1} amplifier output.
8. Remove short circuit across R4.
9. Connect MSB (Bit-1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R5 for $0V \pm 0.2mV$ at V_{OUT} .

GAIN ADJUSTMENT

1. Connect all digital inputs to V_{DD} .
2. Monitor V_{OUT} for $-V_{REF} \left(1 - \frac{1}{2^{11}}\right)$ volts reading while adjusting R1.

FIGURE 8: SIMPLIFIED CIRCUIT



ANALOG/DIGITAL DIVISION

The transfer function for the PM-7541 connected in the multiplying mode as shown in Figure 6 is:

$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}} \right)$$

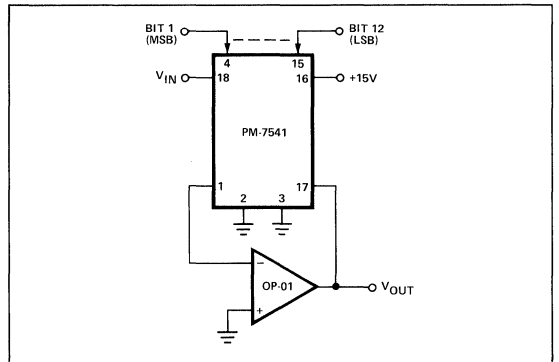
where A_x assume a value of 1 for an "ON" bit and 0 for an "OFF" bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 9, it now is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}}} \right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (± 1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

FIGURE 9: ANALOG/DIGITAL DIVIDER





PM-7542

12-BIT (4-BIT BYTE INPUT)
MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- $\pm 1/2$ LSB Nonlinearity Over Temperature
- Low Gain Tempco 5ppm/ $^{\circ}$ C Max
- Microprocessor Compatible
- Four Quadrant Multiplication
- Low AC Feedthrough
- Low Power Dissipation 40mW
- Low Cost
- Small 16-Pin 0.3" DIP Package
- Latch-Up Resistant

APPLICATIONS

- Industrial Automation
- Process Controls
- Instrumentation Equipment

ORDERING INFORMATION†

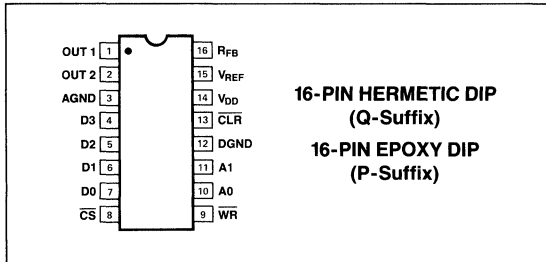
GAIN ERROR	PACKAGE: 16-PIN DIP**		
	MILITARY* TEMPERATURE	INDUSTRIAL TEMPERATURE	COMMERCIAL TEMPERATURE
± 1 LSB	PM7542AQ	PM7542EQ	PM7542GP
± 6 LSB	PM7542BQ	PM7542FQ	PM7542HP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

** Package Designation: Suffix Q: Hermetic DIP; Suffix P: Epoxy DIP.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

PIN CONNECTIONS



GENERAL DESCRIPTION

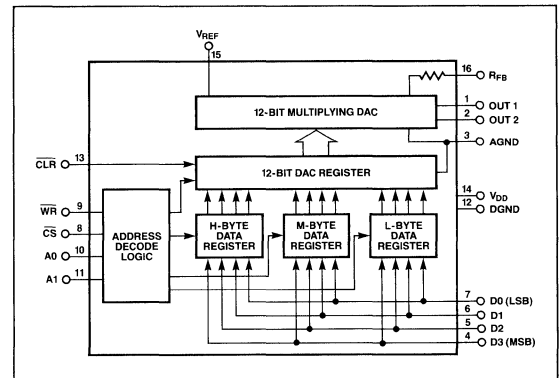
The PM-7542 is a 12-bit monolithic, CMOS digital-to-analog converter. It consists of three 4-bit data registers, a 12-bit DAC register, a 12-bit multiplying DAC, and address decoding.

Data is accepted in three 4-bit bytes that facilitate direct interfacing to 4 or 8-bit microprocessors. Data loading is similar to a static RAM's write cycle. A $\overline{\text{CLR}}$ pin is provided to reset the DAC's internal registers to zeros.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7542AQ	AD7542GTD	MILITARY
PM7542BQ	AD7542TD	
PM7542BQ	AD7542SD	
PM7542EQ	AD7542GBD	INDUSTRIAL
PM7542FQ	AD7542BD	
PM7542FQ	AD7542AD	
PM7542GP	AD7542GKN	COMMERCIAL
PM7542HP	AD7542KN	
PM7542HP	AD7542JN	

FUNCTIONAL DIAGRAM



DIGITAL-TO-ANALOG CONVERTERS

11

This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



PM-7543

12-BIT SERIAL-INPUT
MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- $\pm 1/2$ LSB Nonlinearity Over Temp
- Low Gain Tempco 5ppm/ $^{\circ}$ C Max
- Serial Load on Positive or Negative Strobe
- Asynchronous CLEAR Input for Initialization
- Low AC Feedthrough
- No Schottky Diode Output Protection Required
- Four Quadrant Multiplication
- Low Power Dissipation
- Single Supply Operation
- Low Cost
- Small 16-Pin 0.3" DIP
- Latch-Up Resistant

ORDERING INFORMATION†

PACKAGE: 16-PIN DIP**

RELATIVE ACCURACY	GAIN ERROR	MILITARY*	INDUSTRIAL	COMMERCIAL
		TEMPERATURE -55 $^{\circ}$ C to +125 $^{\circ}$ C	TEMPERATURE -25 $^{\circ}$ C to +85 $^{\circ}$ C	TEMPERATURE 0 $^{\circ}$ C to +70 $^{\circ}$ C
$\pm 1/2$ LSB	± 1 LSB	PM7543AQ	PM7543EQ	PM7543GP
$\pm 1/2$ LSB	± 6 LSB	PM7543BQ	PM7543FQ	PM7543HP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

**Package Designation: Suffix Q: Hermetic DIP; Suffix P: Epoxy DIP.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7543AQ	AD7543GTD	MILITARY
PM7543BQ	AD7543TD	
PM7543BQ	AD7543SD	
PM7543EQ	AD7543GBD	INDUSTRIAL
PM7543FQ	AD7543BD	
PM7543FQ	AD7543AD	
PM7543GP	AD7543GKN	COMMERCIAL
PM7543HP	AD7543KN	
PM7543HP	AD7543JN	

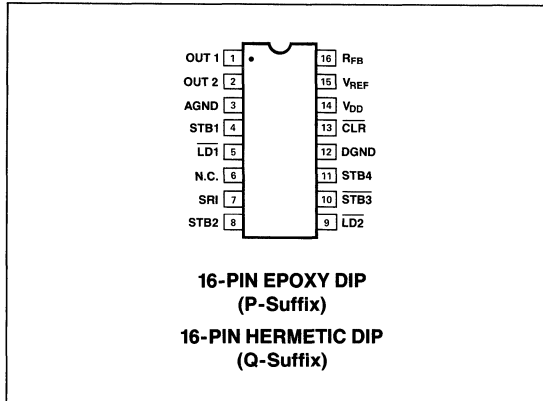
GENERAL DESCRIPTION

The PM-7543 is a monolithic, serial input, 12-bit CMOS digital-to-analog converter. It is intended for applications where serial input data is used. Serial input reduces pin count and is, therefore, well-suited where PC board space is at a premium.

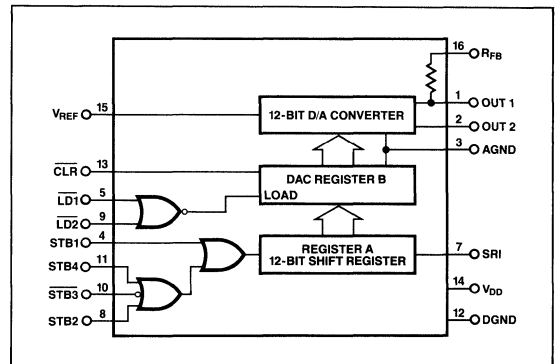
The PM-7543 contains a 12-bit serial-in parallel-out input register, a 12-bit shift register, and a 12-bit DAC. A signal at the strobe pin clocks the serial data input on the leading or trailing edge of the strobe signal; selection is at the user's discretion. Data at the serial-in input register is then loaded onto the shift register with the load input controls. A CLR input pin is provided to asynchronously reset the shift register.

The PM-7543 operates from a single +5V supply and is packaged in a small 16-pin 0.3" wide DIP.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



PM-7545/PM-7645

12-BIT BUFFERED
MULTIPLYING CMOS D/A CONVERTERS

Precision Monolithics Inc.

FEATURES

- Preadjusted Full Scale . . . ± 1 LSB Maximum Gain Error
- Low Gain Temperature Coefficient 2ppm/°C
- Small 20-Pin 0.3" Wide DIP
- PM-7545 TTL Compatible for $V_{DD} = 5V$
- PM-7645 TTL and 5V CMOS Compatible for $V_{DD} = 15V$

ORDERING INFORMATION†

PACKAGE: 20-PIN*			
	MILITARY**	INDUSTRIAL	COMMERCIAL
MAXIMUM GAIN ERROR $T_A = +25^\circ\text{C}$	TEMPERATURE -55°C to +125°C	TEMPERATURE -25°C to +85°C	TEMPERATURE 0°C to +70°C
± 1 LSB	PM7545AR	PM7545ER	PM7545GP
± 3 LSB	PM7545BR	PM7545FR	PM7545HP
± 1 LSB	PM7645AR	PM7645ER	PM7645GP
± 3 LSB	PM7645BR	PM7645FR	PM7645HP

*Package designation:
Suffix R: Hermetic DIP
Suffix P: Plastic DIP

**For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

CROSS REFERENCE

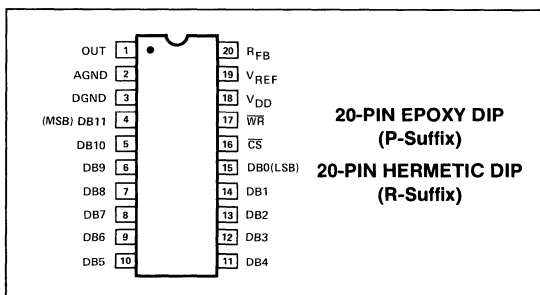
PMI	ADI	TEMPERATURE RANGE
PM7545AR	AD7545GUD	MILITARY
PM7545BR	AD7545UD	
PM7545BR	AD7545TD	
PM7545BR	AD7545SD	
PM7545ER	AD7545GCCQ	INDUSTRIAL
PM7545FR	AD7545CQ	
PM7545FR	AD7545BQ	
PM7545FR	AD7545AQ	
PM7545GP	AD7545GLN	COMMERCIAL
PM7545HP	AD7545LN	
PM7545HP	AD7545KN	
PM7545HP	AD7545JN	

GENERAL DESCRIPTION

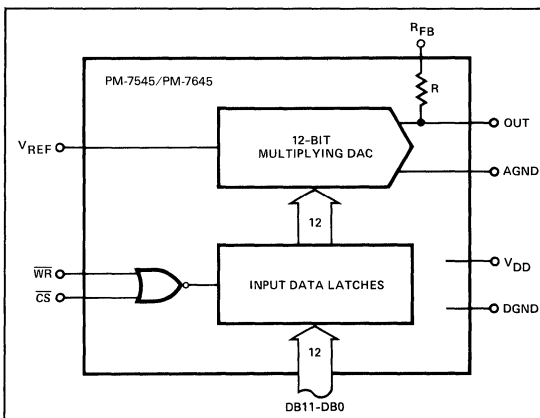
The PM-7545/PM-7645 are 12-bit CMOS multiplying DACs with internal data latches. Digital data is input in a 12-bit wide data format, while \overline{CS} and \overline{WR} control inputs are active low. During this time the latches are transparent allowing digital inputs direct connection to the DAC. When \overline{WR} is returned to logic high, the current data word in the latch is saved.

The PM-7545 operates from 5 to 15 volt power supplies, offering TTL logic compatibility at V_{DD} of 5V and CMOS logic compatibility at V_{DD} of 15V. The PM-7645 is specified for operation at V_{DD} of 15V, offering TTL logic input compatibility.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



DIGITAL-TO-ANALOG CONVERTERS

**ABSOLUTE MAXIMUM RATINGS**(T_A = 25°C unless otherwise noted.)

V _{DD} to DGND	-0.3V, +17V
Digital Input Voltage to DGND	-0.3V, V _{DD}
AGND to DGND	-0.3V, V _{DD}
V _{REFB} , V _{REF} to DGND	±25V
V _{PIN1} to DGND	-0.3V, V _{DD}
Power Dissipation (Any Package) to +75°C	450mW
Derates Above +75°C by	6mW/°C
Operating Temperature Range	
Military (AR, BR) Grades	-55°C to +125°C
Industrial (ER, FR) Grades	-25°C to +85°C
Commercial (GP, HP) Grades	0°C to +70°C
Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper anti-static handling procedures.
4. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = -55°C to +125°C apply for PM-7545AR/BR, T_A = -25°C to +85°C apply for PM-7545ER/FR, T_A = 0°C to +70°C apply for PM-7545GP/HP, unless otherwise noted. For 15V operation, see pages 4 and 5.

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G			PM-7545B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Relative Accuracy	INL	T _A = Full Temp. Range	—	—	±1/2	—	—	±1/2	LSB
Differential Nonlinearity	DNL	T _A = Full Temp. Range (Note 1)	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G _{FSE}	T _A = +25°C	—	—	±1	—	—	±3	LSB
		T _A = Full Temp. Range	—	—	±2	—	—	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG _{FS}	(Note 4)	—	±2	±5	—	±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV _{DD}	PSS	T _A = +25°C	—	—	0.002	—	—	0.002	%/%
		T _A = Full Temp. Range (ΔV _{DD} = ±5%)	—	—	0.004	—	—	0.004	
Output Leakage Current at OUT	I _{LKG}	T _A = +25°C, WR = CS = 0V, All Digital Inputs = 0V	—	—	10	—	—	10	nA
		T _A = Full Temp. Range	—	—	200	—	—	200	
		A/B Versions	—	—	50	—	—	50	
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 5, 6, 7)	t _{PD}	T _A = +25°C	—	—	300	—	—	300	ns
		(OUT Load = 100Ω, C _{EXT} = 13pF)	—	—	—	—	—	—	
Current Settling Time	t _s	T _A = Full Temp. Range (To 1/2 LSB) (Note 4) I _{OUT} Load = 100Ω	—	—	1	—	—	1	μs
Digital Charge Injection	Q	T _A = +25°C	—	—	300	—	—	300	nVs
		T _A = Full Temp. Range V _{REF} = AGND (Note 4)	—	—	400	—	—	400	
AC Feedthrough at I _{OUT}	FT	T _A = Full Temp. Range V _{REF} = ±10V, f = 10kHz All Digital Inputs = 0V	—	5	—	—	5	—	mV _{p-p}



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF} = +10V$, $V_{OUT} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7545AR/BR, $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7545ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7545GP/HP, unless otherwise noted. For 15V operation, see pages 4 and 5. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G			PM-7545B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R_{REF}	$T_A =$ Full Temp. Range Input Resistance	7	11	15	7	11	15	$k\Omega$
ANALOG OUTPUTS									
Output Capacitance (Note 4)	C_{OUT}	$T_A =$ Full Temp. Range DB0-DB11 = 0V, WR = CS = 0V	—	—	70	—	—	70	pF
C_{OUT}		DB0-DB11 = V_{DD} , WR = CS = 0V	—	—	150	—	—	150	
DIGITAL INPUTS									
Input High Voltage	V_{INH}	$T_A =$ Full Temp. Range	2.4	—	—	2.4	—	—	V
Input Low Voltage	V_{INL}		—	—	0.8	—	—	0.8	
Input Current	I_{IN}	$T_A = +25^\circ C$ $T_A =$ Full Temp. Range	—	—	1 10	—	—	1 10	μA
Input Capacitance DB0-DB11, WR, CS	C_{IN}	$T_A =$ Full Temp. Range $V_{IN} = 0$ (Note 4)	—	—	8	—	—	8	pF
SWITCHING CHARACTERISTICS (Notes 4, 8, 9) See Timing Diagram									
Chip Select to Write Setup Time	t_{CS}	$T_A = +25^\circ C$ $T_A =$ Full Temp. Range	280 380	200 270	—	280 380	200 270	—	ns
Chip Select to Write Hold Time	t_{CH}	$T_A =$ Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	$T_A = +25^\circ C$ $T_A =$ Full Temp. Range	250 380	175 270	—	250 380	175 270	—	ns
Data Setup Time	t_{DS}	$T_A = +25^\circ C$ $T_A =$ Full Temp. Range	140 210	100 150	—	140 210	100 150	—	ns
Data Hold Time	t_{DH}	$T_A =$ Full Temp. Range	10	—	—	10	—	—	ns
POWER SUPPLY									
Supply Current	I_{DD}	$T_A =$ Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	$T_A = +25^\circ C$ $T_A =$ Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	2 5	100 100	—	2 5	100 100	μA

NOTES:

- 12-bit monotonic over full temperature range.
- Includes the effects of 5ppm max. gain T.C.
- Using internal R_{FB} . DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- GUARANTEED and NOT TESTED.
- From digital input change to 90% of final analog output.
- All digital inputs = 0V to V_{DD} ; or V_{DD} to 0V.
- Logic inputs are MOS gates, typical input current (at $+25^\circ C$) is less than 1nA.
- Sample tested at $+25^\circ C$ to ensure compliance.
- Chip select CS must be coincident or present before and/or after write WR; that is, $t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$.



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $V_{OUT} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7545/PM-7645AR/BR, $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7545/PM-7645ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7545/PM-7645GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G PM-7645A/E/G			PM-7545B/F/H PM-7645B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Relative Accuracy	INL	$T_A = \text{Full Temp. Range}$	—	—	$\pm 1/2$	—	—	$\pm 1/2$	LSB
Differential Nonlinearity	DNL	$T_A = \text{Full Temp. Range}$ (Note 1)	—	—	± 1	—	—	± 1	LSB
Gain Error (Notes 2, 3)	G_{FSE}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	± 1 ± 2	—	—	± 3 ± 4	LSB
Gain Temperature Coefficient $\Delta\text{Gain}/\Delta\text{Temperature}$	TCG_{FS}	(Note 4)	—	± 2	± 5	—	± 2	± 5	ppm/ $^\circ C$
DC Supply Rejection $\Delta\text{Gain}/\Delta V_{DD}$	PSS	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$ ($\Delta V_{DD} = \pm 5\%$)	—	—	0.002 0.004	—	—	0.002 0.004	%/%
Output Leakage Current at OUT	I_{LKG}	$T_A = +25^\circ C$, $WR = CS = 0V$, All Digital Inputs = 0V $T_A = \text{Full Temp. Range}$ A/B Versions E/F/G/H Versions	—	—	10 200 50	—	—	10 200 50	nA
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 5, 6, 7)	t_{pD}	$T_A = +25^\circ C$ (OUT Load = 100 Ω , $C_{EXT} = 13pF$)	—	—	300	—	—	300	ns
Current Setting Time	t_s	$T_A = \text{Full Temp. Range}$ (To 1/2 LSB) (Note 4) I_{OUT} Load = 100 Ω	—	—	1	—	—	1	μs
Digital Charge Injection	Q	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$ $V_{REF} = AGND$ (Note 4)	—	—	300 400	—	—	300 400	nVs
AC Feedthrough at I_{OUT}	FT	$T_A = \text{Full Temp. Range}$ $V_{REF} = \pm 10V$, $f = 10kHz$ All Digital Inputs = 0V	—	5	—	—	5	—	mV _{p-p}
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R_{REF}	$T_A = \text{Full Temp. Range}$ Input Resistance	7	11	15	7	11	15	k Ω
ANALOG OUTPUTS									
Output Capacitance (Note 4) C_{OUT}	C_{OUT}	$T_A = \text{Full Temp. Range}$ DB0-DB11 = 0V, $WR = CS = 0V$ DB0-DB11 = V_{DD} , $WR = CS = 0V$	—	—	70 150	—	—	70 150	pF
DIGITAL INPUTS									
Input High Voltage	V_{INH}	$T_A = \text{Full Temp. Range}$, PM-7545	13.5	—	—	13.5	—	—	V
Input Low Voltage	V_{INL}		—	—	1.5	—	—	1.5	
Input High Voltage	V_{INH}	$T_A = \text{Full Temp. Range}$, PM-7645	2.4	—	—	2.4	—	—	V
Input Low Voltage	V_{INL}		—	—	0.8	—	—	0.8	
Input Current	I_{IN}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	1 10	—	—	1 10	μA
Input Capacitance DB0-DB11, WR , CS	C_{IN}	$T_A = \text{Full Temp. Range}$ $V_{IN} = 0$ (Note 4)	—	—	8	—	—	8	pF



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $V_{OUT} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7545/PM-7645AR/BR, $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7545/PM-7645ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7545/PM-7645GP/HP, unless otherwise noted. (Continued)

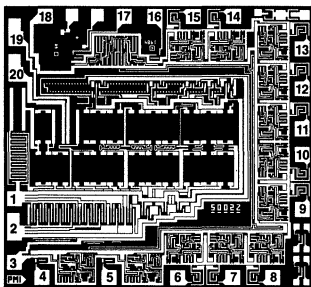
PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G PM-7645A/E/G			PM-7545B/F/H PM-7645B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY									
Supply Current	I_{DD}	$T_A =$ Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	$T_A = +25^\circ C$ $T_A =$ Full Temp. Range (All Digital Inputs $0V$ or V_{DD})	—	2	100	—	2	100	μA
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)									
		See Timing Diagram	PM-7545 A/E/G			PM-7545 B/F/H			
Chip Select to Write Setup Time	t_{CS}	$T_A = +25^\circ C$	180	120	—	180	120	—	ns
		$T_A =$ Full Temp. Range	200	150	—	200	150	—	
Chip Select to Write Hold Time	t_{CH}	$T_A =$ Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	$T_A = +25^\circ C$	160	100	—	160	100	—	ns
		$T_A =$ Full Temp. Range	240	170	—	240	170	—	
Data Setup Time	t_{DS}	$T_A = +25^\circ C$	90	60	—	90	60	—	ns
		$T_A =$ Full Temp. Range	120	80	—	120	80	—	
Data Hold Time	t_{DH}	$T_A =$ Full Temp. Range	10	—	—	10	—	—	ns
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)									
		See Timing Diagram	PM-7645 A/E/G			PM-7645 B/F/H			
Chip Select to Write Setup Time	t_{CS}	$T_A = +25^\circ C$	150	—	—	150	—	—	ns
		$T_A =$ Full Temp. Range	210	—	—	210	—	—	
Chip Select to Write Hold Time	t_{CH}	$T_A =$ Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	$T_A = +25^\circ C$	150	—	—	150	—	—	ns
		$T_A =$ Full Temp. Range	210	—	—	210	—	—	
Data Setup Time	t_{DS}	$T_A = +25^\circ C$	225	—	—	225	—	—	ns
		$T_A =$ Full Temp. Range	300	—	—	300	—	—	
Data Hold Time	t_{DH}	$T_A =$ Full Temp. Range	10	—	—	10	—	—	ns

NOTES:

- 12-bit monotonic over full temperature range.
- Includes the effects of 5ppm max. gain T.C.
- Using internal R_{FB} . DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- GUARANTEED and NOT TESTED.
- From digital input change to 90% of final analog output.
- All digital inputs = $0V$ to V_{DD} ; or V_{DD} to $0V$.
- Logic inputs are MOS gates, typical input current (at $+25^\circ C$) is less than $1nA$.
- Sample tested at $+25^\circ C$ to ensure compliance.
- Chip select CS must be coincident or present before and/or after write \overline{WR} ; that is, $t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$.



DICE CHARACTERISTICS



DIE SIZE 0.093 × 0.101 inch, 9.393 sq. mils
(2.36 × 2.57mm, 6.07 sq. mm)

- | | |
|---------------|----------------------|
| 1. OUT | 11. DB4 |
| 2. AGND | 12. DB3 |
| 3. DGND | 13. DB2 |
| 4. DB11 (MSB) | 14. DB1 |
| 5. DB10 | 15. DB0 (LSB) |
| 6. DB9 | 16. CS |
| 7. DB8 | 17. WR |
| 8. DB7 | 18. V _{DD} |
| 9. DB6 | 19. V _{REF} |
| 10. DB5 | 20. R _{FB} |

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at V_{DD} = +5 or +15V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V.

PARAMETER	SYMBOL	CONDITIONS	PM-7545G/PM-7645G LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G _{FSE}	DAC Latches Loaded with 1111 1111 1111	±5	LSB MAX
Output Leakage	I _{LKG}	DAC Latches Loaded with 0000 0000 0000 Pad 1	±10	nA MAX
Input Resistance	R _{REF}	Pad 19	7/15	kΩ MIN/kΩ MAX
Digital Input High	V _{INH}	V _{DD} = 5V V _{DD} = 15V PM-7545 only	2.4 13.5	V MIN
Digital Input Low	V _{INL}	V _{DD} = 5V V _{DD} = 15V PM-7545 only	0.8 1.5	V MAX
Digital Input High	V _{INH}	V _{DD} = 15V PM-7645 only	2.4	V MIN
Digital Input Low	V _{INL}	V _{DD} = 15V PM-7645 only	0.8	V MAX
Input Current	I _{IN}	V _{IN} = 0V or V _{DD}	±1	μA MAX
Supply Current	I _{DD}	All Digital Inputs V _{INL} or V _{INH} All Digital Inputs 0V or V _{DD}	2 0.1	mA MAX
DC Supply Rejection (ΔGain/ΔV _{DD})	PSS	ΔV _{DD} = ±5%	0.02	%/% MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



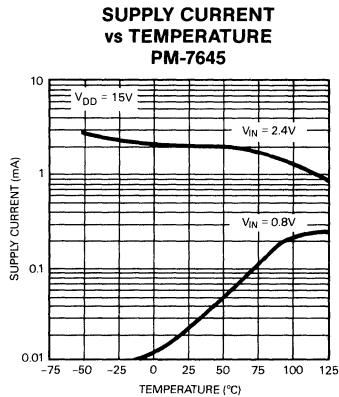
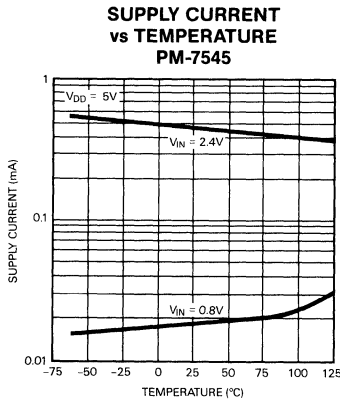
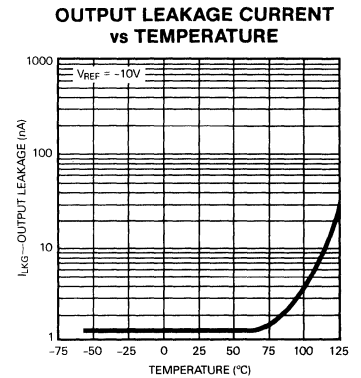
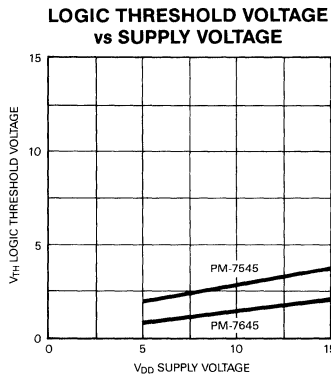
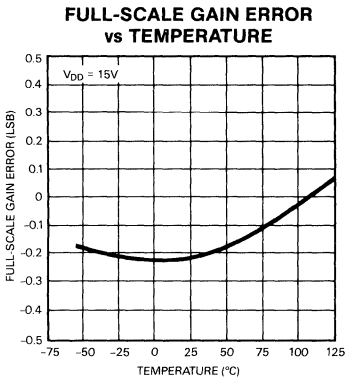
TYPICAL ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $AGND = DGND = 0V$, $V_{REF} = +10V$, $OUT = 0V$; $T_A = 25^\circ C$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	PM-7545G/PM-7645G	
			TYPICAL	UNITS
Digital Input Capacitance	C_{IN}		7	pF
Output Capacitance	C_{OUT}	DAC Latches Loaded with 0000 0000 0000	50	pF
		DAC Latches Loaded with 1111 1111 1111	110	
Propagation Delay (Notes 2, 3, 4)	t_{PD}	$V_{DD} = 15V$	140	ns
		$V_{DD} = 5V$ PM-7545 only	230	

NOTES:

1. These characteristics are for design guidance only and are not subject to test.
2. From digital input change to 90% of final analog output.
3. OUT load = 100Ω , $C_{EXT} = 13pF$.
4. $CS = WR = 0$, $DB0$ to $DB11 = 0V$ to V_{DD} or V_{DD} to $0V$.

TYPICAL PERFORMANCE CHARACTERISTICS



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

DIFFERENTIAL NONLINEARITY

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of ± 1 LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will increase for an increase in digital code applied).

GAIN ERROR

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is V_{REF} minus 1 LSB. The gain error is adjustable to zero using external resistance.

OUTPUT CAPACITANCE

The capacitance from OUT to AGND.

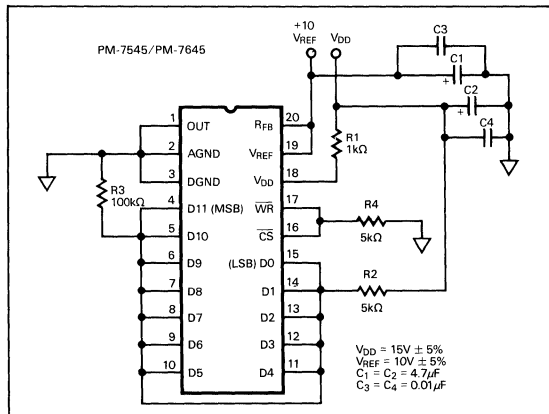
PROPAGATION DELAY

This is measured from the digital input change to the analog output current reaching 90% of its final value.

DIGITAL CHARGE INJECTION

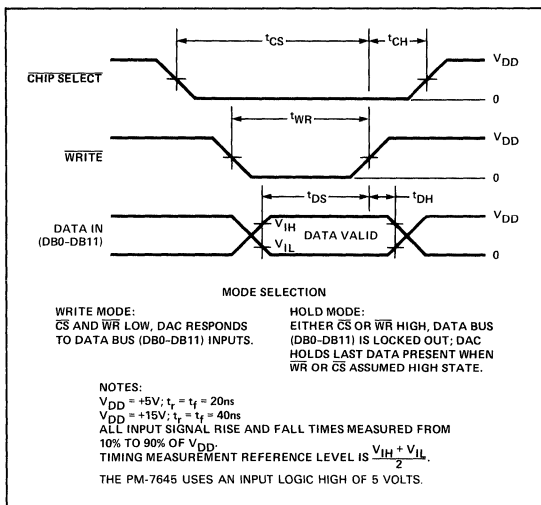
This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with $V_{REF} = AGND$.

BURN-IN CIRCUIT



LOGIC INFORMATION

WRITE CYCLE TIMING DIAGRAM



D/A CONVERTER SECTION

FIGURE 1: Simplified D/A Circuit of PM-7545

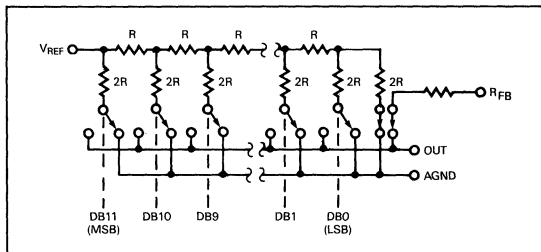


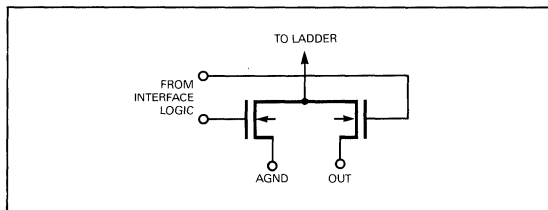
Figure 1 shows a simplified circuit of the D/A Converter section and Figure 2 gives an approximate equivalent switch circuit. R is typically $11k\Omega$.

The binary-weighted currents are switched between OUT and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT terminal, C_{OUT} , is code dependent and varies from $70pF$ (all switches to AGND) to $150pF$ (all switches to OUT). One of the current switches is shown in Figure 2.

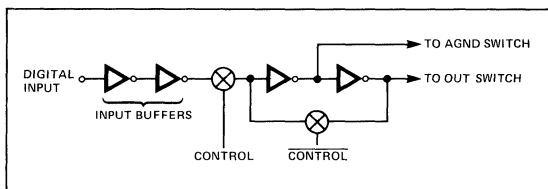
The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the $R/2R$ ladder characteristics resistance and is equal to value "R"). Since the input resistance at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} is recommended to define scale factor.)

The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however when the circuit is not powered up the switch assumes an open state.

FIGURE 2: N-Channel Current Steering Switch


DIGITAL SECTION

Figure 3 shows the digital structure for one bit. The digital signals CONTROL and CONTROL are generated from CS and WR.

FIGURE 3: Digital Input Structure


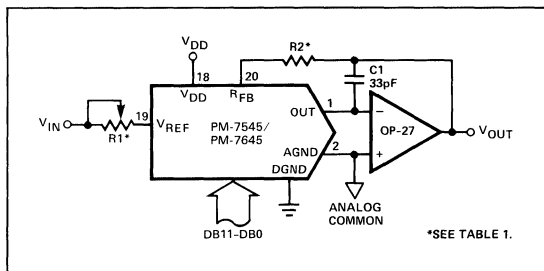
The input buffers are simple CMOS inverters designed such that when the PM-7545 is operated with $V_{DD} = 5V$, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0 volts to 6.0 volts, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible. The PM-7545 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With $V_{DD} = +15V$, the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V. The PM-7645 operates with $V_{DD} = 15V$ only; the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the PM-7545/PM-7645. Resistor R1 is used to trim for full scale. The following versions (PM-7545AR, PM-7545ER, PM-7545GP) have a guaranteed maximum gain error of ± 1 LSB at $+25^\circ C$ and $V_{DD} = +5V$, and in many applications the gain trim resistors are

not required. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (the inversion is introduced by the op amp); or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD} . Table 2 shows the code relationship for the circuit of Figure 4.

FIGURE 4: Unipolar Binary Operation

TABLE I: Recommended Trim Resistor Value vs. Grades

TRIM RESISTOR	CR	HP/FR/BR	GP/ER/AR
R1	200Ω	100Ω	20Ω
R2	68Ω	33Ω	6.8Ω

TABLE II: Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT
1111	1111	1111	$-V_{IN} \cdot \left\{ \frac{4095}{4096} \right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{ \frac{2048}{4096} \right\} = -1/2V_{IN}$
0000	0000	0001	$-V_{IN} \cdot \left\{ \frac{1}{4096} \right\}$
0000	0000	0000	0 Volts

Figure 5 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter U_1 on the MSB line, converts 2's-complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software.

R3, R4 and R5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

TABLE III: 2's Complement Code Table for Circuit of Figure 5

DATA INPUT			ANALOG OUTPUT
0111	1111	1111	$+V_{IN} \cdot \left\{ \frac{2047}{2048} \right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{ \frac{2048}{2048} \right\}$

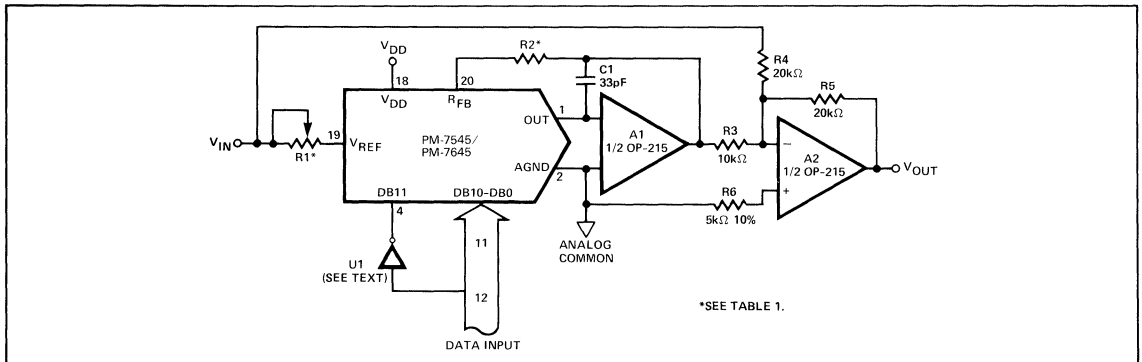
APPLICATION HINTS

Output Offset: CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is $0.67 V_{OS}$ where V_{OS} is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than 10% of 1 LSB over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the PM-7545/PM-7645. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

Digital Glitches: When \overline{WR} and \overline{CS} are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which \overline{WR} is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse \overline{WR} , so that it only occurs when data is valid, will eliminate the problem.

FIGURE 5: Bipolar Operation (2's Complement Code)

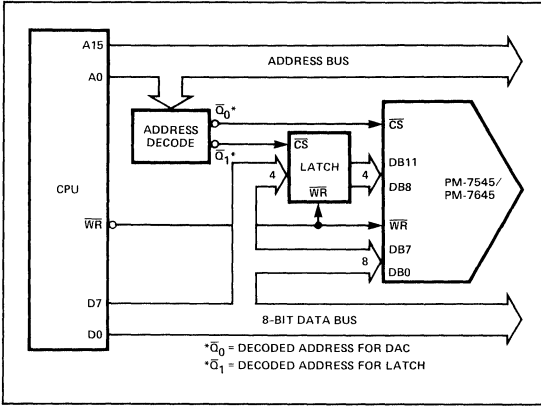


INTERFACING THE PM-7545/PM-7645 TO MICROPROCESSORS

The PM-7545 can be directly interfaced to either an 8 or 16-bit microprocessor via its 12-bit wide data latch using the CS and \overline{WR} control signals.

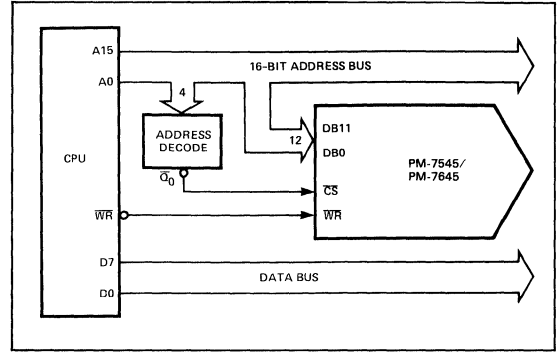
An 8-bit processor interface configuration is shown in Figure 6. It uses two memory addresses, one for the lower 8-bits and one for the upper 4-bits of data into the DAC via the latch.

FIGURE 6: 8-Bit Processor to PM-7545/7645 Interface



Connection to an 8-bit processor with a full 16-bit wide address bus (such as the 6800, 8080, Z80) is shown in Figure 7. The 12 lower address lines are fed directly to the PM-7545; this allows the PM-7545 to use 4k bytes for its address location. The address field of the instruction is organized so that the lower 12-bits contain the DAC data. Data is written into the DAC using a single write instruction.

FIGURE 7: Connecting the PM-7545/7645 to an 8-Bit Microprocessor via the Address Bus





PM-7548

12-BIT (8-BIT BYTE INPUT)
MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- 12-Bit Resolution with an 8-Bit Data Bus
- Direct Interface to Most 8-Bit Microprocessors
- Selectable Input Data Format (Left or Right-Justified)
- TTL/CMOS Compatible
- Gain Drift 5ppm/°C Max
- Guaranteed Monotonic Over Full Temperature Range
- Single Supply Operation
- Four Quadrant Multiplication
- Latch-Up Resistant
- Small 20-Pin 0.3" DIP Package

APPLICATIONS

- 8-Bit Microprocessor-Controlled Systems
- Industrial Automation
- Process Controls
- Servo Control Systems
- Programmable Filters and Amplifiers

ORDERING INFORMATION†

PACKAGE: 20-PIN DIP**				
RELATIVE ACCURACY	GAIN ERROR	MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -25°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±3 LSB	PM7548AR	PM7548ER	PM7548GP
±1 LSB	±6 LSB	PM7548BR	PM7548FR	PM7548HP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

**Package Designation: Suffix R: Hermetic DIP; Suffix P: Epoxy DIP.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

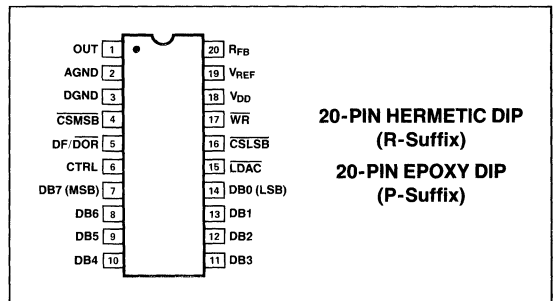
The PM-7548 is a 12-bit monolithic, CMOS digital-to-analog converter with an 8-bit data input bus. Simple interfacing to 8-bit microprocessors results when using a two-step data-load operation from the 8-bit data bus. The PM-7548 allows either left or right-justified data. This simplifies data-formatting when used with various types of microprocessors.

In multiple DAC applications, it sometimes becomes necessary to simultaneously update the outputs. The PM-7548 is ideally suited for this application, providing a separate LDAC control pin that immediately updates an analog output from the input registers.

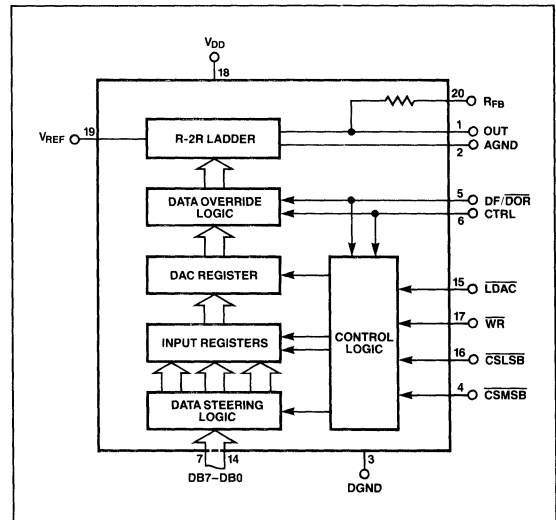
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7548AR	AD7548TD	MILITARY
PM7548BR	AD7548SD	
PM7548ER	AD7548BQ	INDUSTRIAL
PM7548FR	AD7548AQ	
PM7548GP	AD7548KN	COMMERCIAL
PM7548HP	AD7548JN	

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



JM38510/11301/11302

JAN 8-BIT MULTIPLYING
D/A CONVERTERS

Precision Monolithics Inc.

GENERAL DESCRIPTION

This data sheet covers the electrical requirements of the monolithic 8-bit digital-to-analog converters found in MIL-M-38510/113. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/113 for Class B processed devices.

Device Types shall be as follows:

- 01 D/A Converter, 8 bit, 0.19% linearity
- 02 D/A Converter, 8 bit, 0.10% linearity

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The Generic-Industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510/113 devices.

Military Device Type	Generic-Industry Type
01	DAC-08
02	DAC-08A

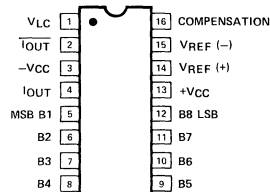
CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline D-2 (16-Lead 1/4" x 7/8", dual-in-line). Package type designator "E".

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{J-C}	Maximum θ_{J-A}
Dual-in-line	E	400mW at $T_A = 125^\circ\text{C}$	35°C/W	120°C/W

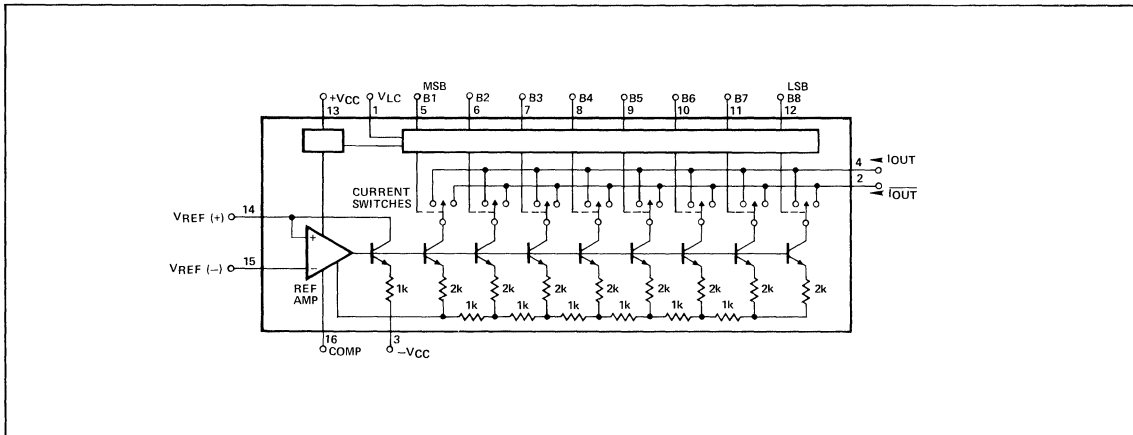
PIN CONNECTIONS & ORDERING INFORMATION



Jan Device Type	PMI Device Type	Linearity
JM38510/11301BEC	DAC08Q1/38510	0.19%
JM38510/11302BEC	DAC08AQ1/38510	0.10%
JM38510/11301BEB	DAC08Q2/38510	0.19%
JM38510/11302BEB	DAC08AQ2/38510	0.10%

NOTES: Lead finish as follows
 BEC: Gold Plate, side braze package
 BEB: Tin Plate, CERDIP Package

SIMPLIFIED SCHEMATIC



DIGITAL-TO-ANALOG CONVERTERS

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage [+V _{CC} - (-V _{CC})]	36Vdc
Voltage, Digital Input to Negative Supply [V _{logic} - (-V _{CC})]	0 to 36Vdc
Voltage, Logic Control (V _{LC})	-V _{CC} to +V _{CC}
Reference Voltage Input [(V ₁₄ , V ₁₅)]	-V _{CC} to +V _{CC}
Reference Input Current (I ₁₄)	5mA
Reference Input Differential Voltage [(V ₁₄ - V ₁₅)]	±18Vdc
Lead Temperature (Soldering, 60 sec)	300° C

Junction Temperature	175° C
Storage Temperature	-65° C to +150° C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	±5Vdc to ±15Vdc*
Ambient Temperature Range	-55° C to +125° C

***NOTE:**

A slight degradation in linearity can occur when the supply voltage is near the ±5V end of the recommended operating range.

ELECTRICAL CHARACTERISTICS at ±V_{CC} = ±15Vdc; Source resistance = 50 ohms; I_{REF} = 2.0mA; Figure 1; Ambient temperature range = -55° C to +125° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Monotonicity	Δ(i)	Measure I _O , (I _{ON} - I _{ON-1}) ≥ 0 at each major carry point	0	16	0	16	μA
	Δ(ī)	Measure I _O , (I _{ON} - I _{ON-1}) ≥ 0 at each major carry point	0	16	0	16	
Output Symmetry	ΔI _{FS}	I _{FS} - I _{FS}	-8	8	-4	4	μA
Full-Scale Current Temperature Coefficient	$\frac{T_C(I_{FS})}{T_C(I_{FS})}$	All input bits high, Measure I _O All input bits low, Measure I _O	-50	50	-50	50	ppm/° C
Full-Scale Current	I _{FS}	All input bits high, Measure I _O	1.94	2.04	1.984	2	mA
	I _{FS}	All input bits low, Measure I _O					
Zero-Scale Current	I _{ZS}	All input bits low, Measure I _O	-2	2	-1	1	μA
	I _{ZS}	All input bits high, Measure I _O					
Positive Bit Errors	ΣNL+	Measure I _O (Σ Positive bit errors)/I _{FS}	0	0.19	0	0.10	%
	ΣNL+	Measure I _O (Σ Positive bit errors)/I _{FS}					
Negative Bit Errors	ΣNL-	Measure I _O (Σ Negative bit errors)/I _{FS}	-0.19	0	-0.10	0	%
	ΣNL-	Measure I _O (Σ Negative bit errors)/I _{FS}					
Positive and Negative Bit Error Difference	ΔΣNL	Measure I _O ΣNL+ - ΣNL-	-0.05	0.05	-0.03	0.03	%
	ΔΣNL	Measure I _O ΣNL+ - ΣNL-					
Positive Relative Accuracy	NL+	Measure I _O ΣNL+ + ΔΣNL	0	0.19	0	0.10	%
	NL+	Measure I _O ΣNL+ + ΔΣNL					
Negative Relative Accuracy	NL-	Measure I _O ΣNL- + ΔΣNL	0	0.19	0	0.10	%
	NL-	Measure I _O ΣNL- + ΔΣNL					

Bit Error

Bit error is the deviation of the analog output from its ideal value (after zero-scale and full-scale errors have been calibrated out) when turning on an individual bit. This is measured for all n bits.

$$\text{Bit error (analog value)} = V_n - (\text{FSR}/2^n)$$

Where V_n = analog output with bit n on only.

FSR = full-scale range

n = number of bits

Summation Nonlinearity (ΣNL)

Summation nonlinearity is the sum of all positive bit errors or all negative bit errors, whichever is larger. By summing up all the bit errors in one direction, you obtain the worst possible nonlinearity (i.e. if bit 2 is 1 LSB high and bit 4 is 1/2 LSB high, then bits 2 and 4 together will be 1 1/2 LSBs high. This is essentially the same as integral nonlinearity since the bit errors are superimposed on each other to give the worst case nonlinearity.



ELECTRICAL CHARACTERISTICS at $\pm V_{CC} = \pm 15V_{dc}$; Source resistance = 50 ohms; $I_{REF} = 2.0mA$; Figure 1; Ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Output Current Range	$I_{FS} R_1$	All input bits high, Measure I_O , $-V_{CC} = -10V$, $V_{REF} = 15V$	2.1	—	2.1	—	mA
	$\overline{I_{FS} R_1}$	All input bits low, Measure $\overline{I_O}$, $-V_{CC} = -10V$, $V_{REF} = 15V$					
	$I_{FS} R_2$	All input bits high, Measure I_O , $-V_{CC} = -12V$, $V_{REF} = 25V$	4.2	—	4.2	—	
	$\overline{I_{FS} R_2}$	All input bits low, Measure $\overline{I_O}$, $-V_{CC} = -12V$, $V_{REF} = 25V$					
Reference Bias Current	I_{REF}	All input bits low	-3	0	-3	0	μA
High Level Input Current	I_{IH}	All input bits $V_{IN} = 18V$, each input measured separately	-0.05	10	-0.05	10	μA
Low Level Input Current	I_{IL}	All input bits $V_{IN} = 10V$, each input measured separately	-10	—	-10	—	μA
Full-Scale Current At +18V Compliance	$I_{FS} +$	All input bits high, Measure I_O , $V_{IO} = 18V$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS} +}$	All input bits low, Measure $\overline{I_O}$, $V_{IO} = 18V$					
Full-Scale Current At -10V Compliance	$I_{FS} -$	All input bits high, Measure I_O , $V_{IO} = -10V$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS} -}$	All input bits low, Measure $\overline{I_O}$, $V_{IO} = -10V$					
Change In Full Scale Current Due to Voltage Compliance	ΔI_{FSC}	All input bits high, Measure I_O , $25^{\circ}C \leq T_A \leq 125^{\circ}C$	-4	4	-4	4	μA
		$T_A = -55^{\circ}C$	-8	8	-8	8	
	$\overline{\Delta I_{FSC}}$	All Input bits low, Measure $\overline{I_O}$, $V_{IO} = 18V$ to $-10V$	-4	4	-4	4	
		$25^{\circ}C \leq T_A \leq 125^{\circ}C$	-8	8	-8	8	
Power Supply Sensitivity From + V_{CC}	$P_{SS} I_{FS} +1$	All input bits high, Measure I_O , $+V_{CC} = 4.5V$ to $+5.5V$, $-V_{CC} = -18V$	-4	4	-4	4	μA
	$\overline{P_{SS} I_{FS} +1}$	All input bits low, Measure $\overline{I_O}$, $+V_{CC} = 4.5V$ to $+5.5V$, $-V_{CC} = -18V$					
	$P_{SS} I_{FS} +2$	All input bits high, Measure I_O , $+V_{CC} = 12V$ to $18V$, $-V_{CC} = -18V$	-8	8	-8	8	
	$\overline{P_{SS} I_{FS} +2}$	All input bits low, Measure $\overline{I_O}$, $+V_{CC} = 12V$ to $18V$, $-V_{CC} = -18V$					
Power Supply Sensitivity From - V_{CC}	$P_{SS} I_{FS} -1$	All input bits high, Measure I_O , $+V_{CC} = 18V$, $-V_{CC} = -12V$ to $-18V$	-8	8	-8	8	μA
	$\overline{P_{SS} I_{FS} -1}$	All input bits low, Measure $\overline{I_O}$, $+V_{CC} = 18V$, $-V_{CC} = -12V$ to $-18V$					
	$P_{SS} I_{FS} -2$	All input bits high, Measure I_O , $+V_{CC} = 18V$, $-V_{CC} = -4.5V$ to $-5.5V$, $I_{REF} = 1mA$	-2	2	-2	2	
	$\overline{P_{SS} I_{FS} -2}$	All input bits low, Measure $\overline{I_O}$, $+V_{CC} = 18V$, $-V_{CC} = -4.5V$ to $-5.5V$, $I_{REF} = 1mA$					

ELECTRICAL CHARACTERISTICS at $\pm V_{CC} = \pm 15Vdc$; Source resistance = 50 ohms; $I_{REF} = 2.0mA$; Figure 1; Ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Supply Current From $+V_{CC}$	I_{CC+}	All input bits high	0.4	3.8	0.4	3.8	mA
Supply Current From $-V_{CC}$	I_{CC-}	All input bits high	-7.8	-0.8	-7.8	-0.8	mA
Propagation Delay Time, High-to-Low Level	t_{PHL}	Figure 2, Measure V_O	6	60	6	60	ns
Propagation Delay Time, Low-to-High Level	t_{PLH}	Figure 2, Measure V_O	6	60	6	60	ns
Reference Amplifier Input Slew Rate	dI_O/dt $T_A = 25^{\circ}C$	Figure 3, Measure V_O	1.5	—	1.5	—	mA/ μs
Settling Time, High-to-Low Level	t_{SHL} $T_A = 25^{\circ}C$	Figure 2, Output within 1/2 LSB of final value of I_O	10	135	10	135	ns
Settling Time, Low-to-High Level	t_{SLH} $T_A = 25^{\circ}C$	Figure 2, Output within 1/2 LSB of final value of I_O	10	135	10	135	ns

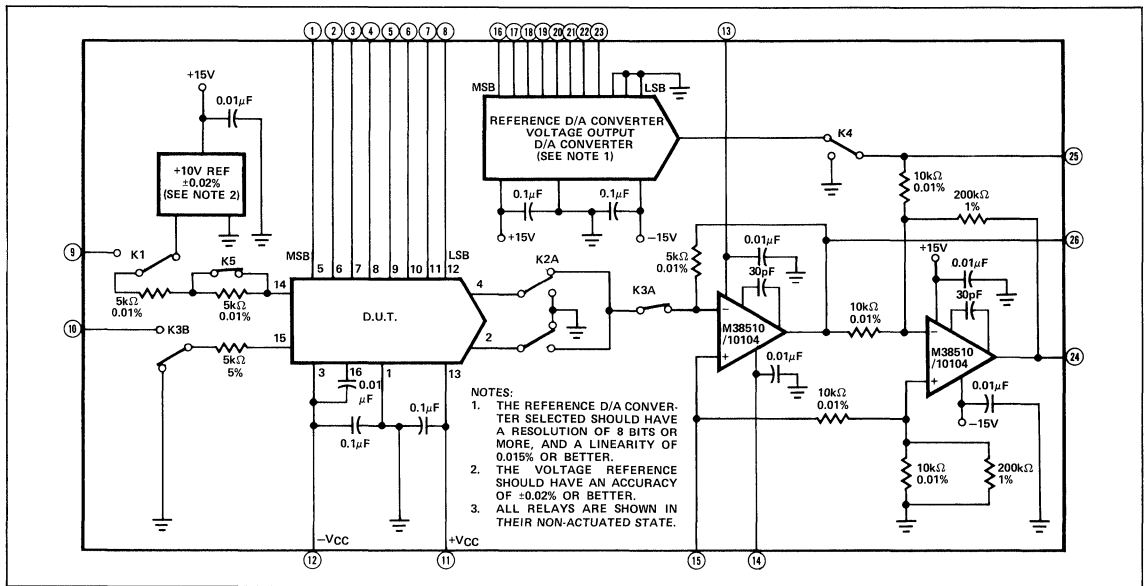


Figure 1. Test Circuit For Static Tests

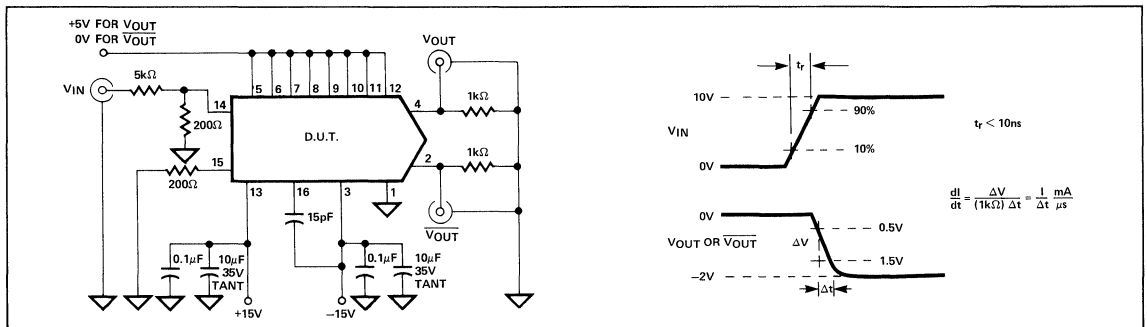


Figure 3. Test Circuit For Slew Rate, Device Types 01, 02

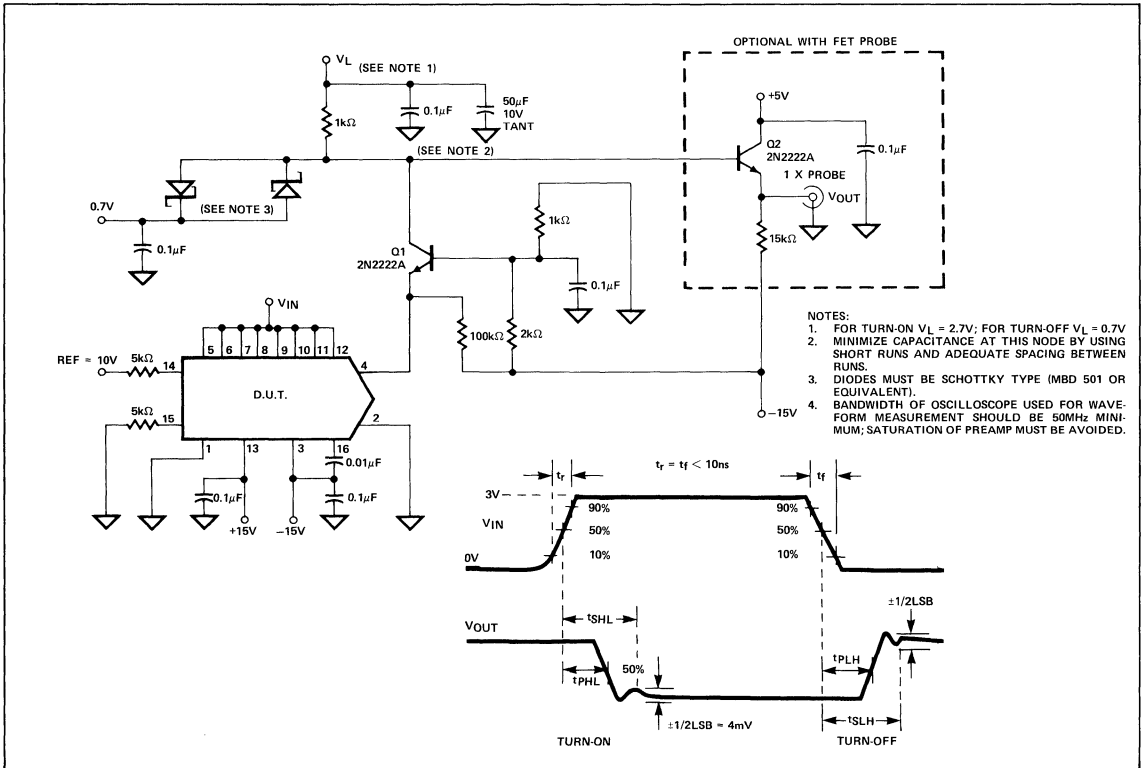


Figure 2. Test Circuit For Propagation Delay and Settling Time, Device Types 01 and 02

BURN-IN

Devices supplied by PMI have been subjected to burn-in per method 1015 of MIL-STD-883 using test condition C or test condition F with the circuit shown in Figure 4.

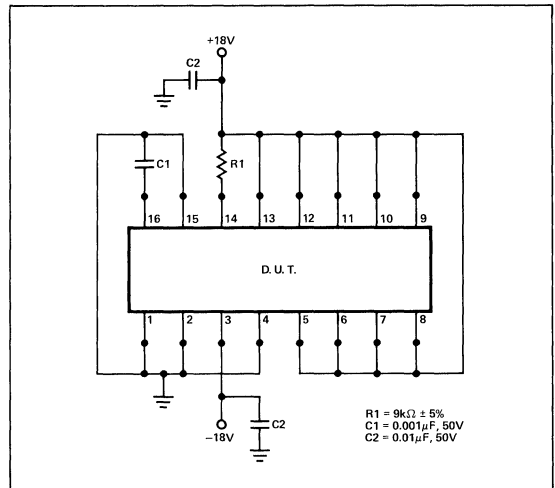


Figure 4. Test Circuit, Burn-In and Operating Life Test

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



A/D CONVERTERS

Precision Monolithics Inc.

12-3 Introduction

12-3 Definitions

12-7 **ADC-910**

High-Speed "Microprocessor
Compatible" A/D Converter

12-19 **ADC-8208**

Microprocessor-Compatible 8-Bit
CMOS A/D Converter

INTRODUCTION

Analog-to-digital converters (ADC) translate analog input voltages into an equivalent digital value. PMI's ADCs use the general purpose successive approximation conversion (SAC) technique. The basic SAC architecture consists of a DAC, comparator, input scaling resistors, and a successive approximation register. A clock and a voltage reference make a complete ADC system.

PMI uses both bipolar and CMOS technologies to optimize ADC designs. The bipolar technology lends itself to high speed ADC conversion and provides the complete ADC function including an internal reference. The CMOS technology offers ADC designs with very low power consumption and good interface versatility at lower prices. PMI's improved bipolar and oxide-isolated CMOS processes offer the best conversion speeds in the SAC architecture.

A SAC ADC has inherent ratioing capability between the input voltage and the input reference level. The digital output is proportional to V_{IN}/V_{REF} . Important criteria for selection of A/D converters include accuracy, conversion speed and resolution. Other requirements include temperature stability, output coding, output data format, reference stability, clock and power needs.

At the digital output many interface data formats are available to match the wide variety of application needs. The ADC-910 provides a very complete microprocessor-controlled interface which contains data registers, control registers and hand-shaking lines. This architecture provides a complete microprocessor compatible system that allows total software control of all ADC functions. For stand-alone applications the ADC-8208 offers direct data output, start conversion and very low power dissipation.

DEFINITIONS— ANALOG-TO-DIGITAL CONVERTERS

Accuracy—ADC total accuracy consists of the sum of integral nonlinearity (INL) error, zero error, gain error and reference error specifications. The INL is the most critical specification since no additional user calibration can be easily performed. Additional specifications affecting ADC device accuracy includes zero drift, gain drift, power

supply sensitivity, and noise. Proper circuit layout and grounding are also important factors in achieving rated performance.

Aperture—The period of time during which an analog input to an ADC should not change more than 1/2 LSB. Determines maximum sampling frequency of the ADC.

ADC—An acronym for **Analog-to-Digital Conversion**, sometimes written as A/D.

Binary Coding—The digital output of an ADC is considered binary-coded when outputs start at all zeros for a zero-scale analog input counting up to all-ones' output code for a full-scale analog input signal.

Bipolar Mode—An ADC configured to convert both positive and negative input voltages.

Bipolar Offset—The analog displacement of one half of full scale range when the ADC operates in the bipolar mode. The offset is generally derived from the converter reference circuit.

Bus—A parallel path of binary information signals—usually 4, 8, or 16 bits wide.

Byte—A binary digital word often 8 bits long.

Chip Select (CS)—A logic input signal activating data or control information transfer between the ADC and the digital circuitry. This signal is usually active low designated by a bar over the top of (CS). CS is used in conjunction with additional qualifying logic signals to determine the exact activities to take place.

Clock (CK)—The operation of the successive approximation conversion process requires a clock. The clock sets the basic conversion rate. Some ADCs have an internal clock, using an external capacitor to set the frequency. Most ADCs have an external clock input.

Code Width—The amount of input voltage change which occurs between output code transitions expressed in LSBs of full scale. The ideal code width is one LSB.

Code Width Uncertainty—The dynamic variation or jitter in the code width due to noise.

Coding—The format of the ADC digital output data. Common formats include binary, offset binary, complementary binary, two's complement, low byte and high byte.

Command Register—An internal register of the ADC that can be programmed by the user to select various modes of operation. For example, unipolar or bipolar conversion selection, range selection, data output format, etc.

Control Lines—Digital input/output pins that activate/monitor and control ADC operation. For example, chip select, write, low byte, high byte, start convert, end of conversion, conversion complete, busy, read, etc.

Conversion Complete (CC)—This digital output signal indicates the end of conversion. When this signal is in the opposite state the ADC is considered to be in the “busy” state.

Conversion Time (t_c)—The amount of time elapsed from the start-conversion control signal until the conversion complete signal occurs.

Differential Nonlinearity (DNL)—The worst-case deviation of distance between transition voltages from the ideal 1 LSB code width. The parameter uses units of LSBs. DNL is one of an ADC’s errors which cannot be removed by user adjustments.

Drift—See Gain Drift, Zero Drift, and Offset Drift specifications.

End Of Conversion (EOC)—This digital output signal flags the conversion complete and data ready condition of an ADC.

Full Scale (FS)—Maximum input voltage of an ADC. A full-scale input voltage to a natural binary-coded ADC outputs the all-ones code.

Full-Scale Error—This parameter applied to ADCs is the same as the gain error specification. See Gain Error.

Full-Scale Range (FSR)—The difference between maximum and minimum analog values for an ADC input.

Gain Drift—The change in the full-scale transition voltage measured over the operating temperature range. This parameter has units of % of full scale, ppm of full scale, or LSB. It may also be expressed as % of FS/°C, ppm of FS/°C, etc.

Gain Error—The difference between the actual full-scale transition voltage and the ideal full-scale transition voltage. The units of this parameter are in LSBs or percent of full scale.

Half-Step Offset—The half-step offset is necessary in ADCs to center the analog input voltages half way between the output code transition points. The SAC converter architecture inherently has a 1 LSB transition voltage for the first code change if a half-step offset is not inserted.

High Byte (HB)—In ADCs with resolutions greater than 8 bits, some products are offered in a high byte, low byte format to simplify interface to 8-bit microprocessor systems. The high byte contains the most significant bit and some or all of the upper 8 bits of the ADC output. Generally bits are loaded in a right or left justified format. Individual product data sheets should be consulted.

Input Impedance (R_{IN})—Analog input resistance of the ADC. In SAC converters input impedance is primarily resistive, but should be buffered by an amplifier with a low output impedance at the clock frequency of the SAC ADC to maintain a stiff input voltage to the ADC.

Input Range—The analog voltage input range which results in a zero code to full-scale code digital output in a natural binary-coded ADC. This parameter is identical to full-scale range. Common preset ranges include 0 to 10V, -10 to +10V, -5 to +5V, etc.

Integral Nonlinearity (INL)—This error specification is a measure of the straightness of the ADC transfer function. It is measured as the worst-case deviation in LSBs from a straight line drawn through the center of the first and last code widths. INL is one of the key error specifications of an ADC which cannot be calibrated by the user.

Left Justified Data—In the byte-oriented data-output format, data bit sets shorter than 8 bits are placed starting in the left side of the data output transfer register. This could apply to the upper or lower byte. For example, a 12-bit ADC will have 4 extra bits which could be left justified.

Least Significant Bit (LSB)—The binary digit with the smallest numerical weighting, normally one LSB equals full-scale range divided by (2^n), where n is the number of bits of the ADC. This parameter may be expressed in millivolts.

Low Byte (LB)—In ADCs with resolutions greater than 8 bits, some products are offered in a high



A/D CONVERTERS

Precision Monolithics Inc.

byte, low byte format to simplify interface to 8-bit microprocessor systems. The low byte contains the least significant bit and some or all of the low 8 bits of the ADC output. Generally bits are loaded in a right or left justified format. Individual product data sheets should be consulted.

Major Transition—The digital output code change between one-and-all-zeros code and zero-and-all-ones code. For example an 8-bit ADC major transition occurs between the codes 1000 0000 and 0111 1111 (half-scale).

Missing Code—As an analog input voltage is swept from zero input to full scale, the output digital codes should change by 1 LSB as each transition voltage is reached. If an output code is skipped, we have a missing code.

Most Significant Bit (MSB)—The binary digit of the resulting ADC conversion with the largest numerical weighting. Normally the MSB has a weighting of one-half full-scale range.

Offset Binary Code—A digital binary code used to represent plus or minus input polarity analog voltages. Negative full-scale voltage is assigned all-zeros code. Zero input voltage has the MSB high (logic one) and the remaining bits at zero. Positive full-scale voltage is assigned all-ones code.

Offset Drift—The change with temperature of analog zero for an ADC operating in the bipolar mode. It is generally expressed in ppm of FSR/ $^{\circ}$ C or LSBs.

Offset Error—The error at analog zero for an ADC operating in the bipolar mode. It has units of % of FSR or LSBs.

Overrange—When analog input voltages exceed the input range, an overrange condition is in effect. Normally the digital output code stays at all ones for positive overrange and all zeros for negative overrange with standard binary coding.

Power Supply Sensitivity (PSS)—The change in the full-scale transition voltage due to a change in power supply voltage. The units are in LSB, % of FS per % of supply voltage, or ppm of FS per % of supply voltage.

Quantization Error—An ADC of n bits can only identify 2^n output codes; however, there exists an infinite number of analog input values adjacent to

the LSB of the ADC which are assigned the same output code. The $\pm 1/2$ LSB limit to resolution is known as the fundamental quantization error of an ADC.

R-2R Ladder—A resistor network providing the basic binary-current-division used in SAC ADCs.

Reference (V_{REF})—Reference voltages determine ADC system's absolute conversion accuracy at full scale. At other voltages the INL and reference determine absolute accuracy. References may be internally or externally supplied.

Relative Accuracy—Relative accuracy error, expressed in LSBs or % of full scale, is the deviation of the analog value at any code from its theoretical value after gain and offset is calibrated. PMI's usage of this specification is identical to the integral nonlinearity specification.

Resolution—The resolution of an ADC is the number of states (2^n) that the analog input voltage is divided (or resolved) into, where n is equal to the number of bits.

Right Justified Data—In the byte-oriented data-output format, data bit sets shorter than 8 bits are placed starting in the right side of the data output transfer register. This could apply to the upper or lower byte. For example, a 12-bit ADC will have 4 extra bits which could be right justified.

Sampling Frequency—The rate at which the ADC can continuously convert analog inputs into digital outputs. In SAC ADCs clock frequency and data transfer overhead determines the sampling frequency.

Short Cycling—Termination of the conversion sequence of an ADC to less than the total number of clock periods required for a full resolution conversion.

Span—Sometimes used to describe the full-scale analog input voltage. Some ADCs have resistor-selectable analog input ranges.

Status Register—A register indicating current status of the analog-to-digital conversion with a busy signal or a conversion complete signal.

Successive Approximation Conversion (SAC)—Successive approximation converters compare an analog input against an accurately-known binary



A/D CONVERTERS

Precision Monolithics Inc.

fraction of a reference input. Starting with half the reference value (the MSB) the converter determines whether the input is greater than or less than this value. Next the converter divides the remaining value in half again determining whether the input value is in the upper or lower quarter. This process is continued until all bits have been tried. The digital result of each trial is a numerical representation of the analog input.

Successive Approximation Register (SAR)—A digital circuit that controls the operation of a successive approximation ADC and accumulates the output digital word in its register.

Three-State Output Buffer—A digital output circuit that can be programmed to output a logic low, logic high or a high output impedance state. These devices are generally connected to digital buses.

Transition Noise—Width of the transition voltage region.

Transition Voltage—The transition voltage is the center of a finite band of analog input voltages where the digital output code of the ADC toggles between two adjacent codes.

Unipolar Mode—Operation of an ADC with zero to full-scale voltage inputs of one polarity only.

Word—A set of binary digits that represent the fundamental register size of the digital circuits being used. For example, Z80, 8085, and 6800 microprocessor systems use 8-bit words, while 68000 and 80186 microprocessor systems have 16-bit words.

Zero Drift—The change with temperature of analog zero for an ADC operating in the unipolar mode. It is generally expressed in ppm of FS/ $^{\circ}$ C, or LSBs.

Zero Error—The error at analog zero for an ADC operating in the unipolar mode. This is a user adjustable parameter.



ADC-910

HIGH-SPEED "MICROPROCESSOR COMPATIBLE"
A/D CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Includes Clock, Reference, 3-State Buffered Outputs
- Fast Conversion Time 6 μ s
- Four Input Ranges .. +/-2.5V, +/-5.0V, +5.0V and +10.0V
- 1/2 LSB INL
- No Missing Codes Over Temperature
- Low ESD Sensitivity Due to Rugged Bipolar Processing
- Software Programmable Unipolar/Bipolar
- Easily Interfaced to 8 and 16-Bit μ P Bus

read/write inputs and 3 Chip Select inputs to control the 10 data lines is included. Interrupt enable, start conversion and bipolar/unipolar mode selection are controlled by the data bus. The use of high-speed Linear Differential Logic results in fast (6 μ s) conversion time and low power dissipation.

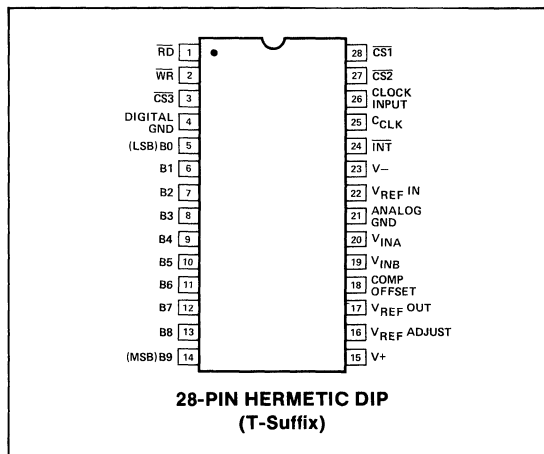
ORDERING INFORMATION†

PMI MODEL NO.	TEMP RANGE
ADC910AT*	-55°C/+125°C
ADC910ET	-25°C/+85°C
ADC910GT	0°C/+70°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

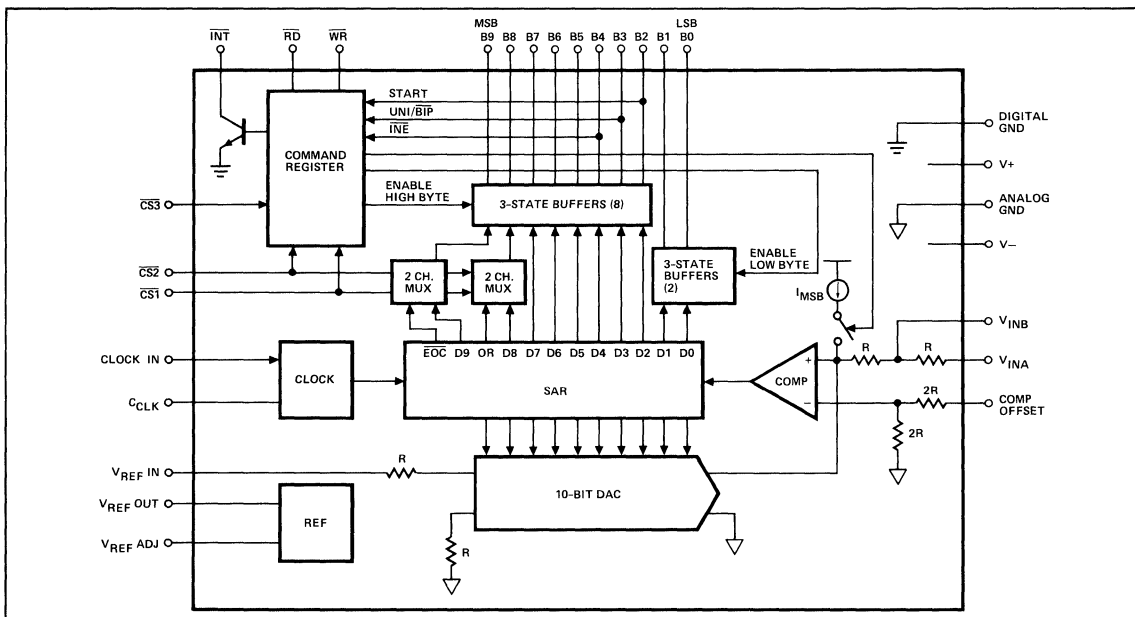
PIN CONNECTIONS



GENERAL DESCRIPTION

The ADC-910 is a 10-bit A/D converter designed specifically for interfacing with microprocessors. 3-state data outputs allow direct connection to an 8-bit data bus in an MSB byte of 8 bits and an LSB byte of 2 bits. A command register with

SIMPLIFIED SCHEMATIC



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature Range	
ADC-910AT/BT	-55°C to +125°C
ADC-910ET/FT	-25°C to +85°C
ADC-910GT/HT	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation at $T_A = 125^\circ\text{C}$	1000mW
Lead Temperature (Soldering, 60 sec)	300°C
Supply Voltage (V_+)	6V

Supply Voltage (V_-)	6V
V_+ to V_-	12V
Logic Inputs	+6V, -0.3V
Logic Outputs (in 3-state)	+6V, -0.3V
V_{INA}	15V
V_{INB}	7.5V
Reference Inputs	3.0V
Digital Ground to Analog Ground Voltage	0.5V

ELECTRICAL CHARACTERISTICS at $V_+ = 5V$, $V_- = -5V$, $V_{REF} = 2.5V$, $f_{CLK} = 0.5\text{MHz}$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for ADC-910AT/BT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910AT			ADC-910BT			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Integral Nonlinearity (Note 3)	INL	$T_A = 25^\circ\text{C}$	—	—	1/2	—	—	1	LSB
		$T_A = \text{Full Temp. Range}$	—	—	3/4	—	—	1	
Gain Drift (Note 1)	TCG_{FS}	External Reference	—	—	25	—	—	30	ppm FS/ $^\circ\text{C}$
		Internal Reference	—	—	40	—	—	50	
Reference Line Regulation		$4.75V < V_+ < 5.25V$	—	—	500	—	—	600	$\mu\text{V}/V$
Positive Supply Current	I_+		—	30	40	—	30	40	mA
Negative Supply Current	I_-		—	50	60	—	50	60	mA

ELECTRICAL CHARACTERISTICS at $V_+ = 5V$, $V_- = -5V$, $V_{REF} = 2.5V$, $f_{CLK} = 0.5\text{MHz}$; $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ apply for ADC-910ET/FT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910ET			ADC-910FT			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Integral Nonlinearity (Note 3)	INL	$T_A = 25^\circ\text{C}$	—	—	1/2	—	—	1	LSB
		$T_A = \text{Full Temp. Range}$	—	—	1/2	—	—	1	
Gain Drift (Note 1)	TCG_{FS}	External Reference	—	—	20	—	—	25	ppm FS/ $^\circ\text{C}$
		Internal Reference	—	—	35	—	—	45	
Reference Line Regulation		$4.75V < V_+ < 5.25V$	—	—	500	—	—	600	$\mu\text{V}/V$
Positive Supply Current	I_+		—	30	40	—	30	40	mA
Negative Supply Current	I_-		—	50	60	—	50	60	mA

ELECTRICAL CHARACTERISTICS at $V_+ = 5V$, $V_- = -5V$, $V_{REF} = 2.5V$, $f_{CLK} = 0.5\text{MHz}$; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for ADC-910GT/HT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910GT			ADC-910HT			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Integral Nonlinearity (Note 3)	INL	$T_A = 25^\circ\text{C}$	—	—	1/2	—	—	1	LSB
		$T_A = \text{Full Temp. Range}$	—	—	3/4	—	—	1	
Gain Drift (Note 1)	TCG_{FS}	External Reference	—	10	—	—	10	—	ppm FS/ $^\circ\text{C}$
		Internal Reference	—	25	—	—	25	—	
Reference Line Regulation		$4.75V < V_+ < 5.25V$	—	300	—	—	300	—	$\mu\text{V}/V$
Positive Supply Current	I_+		—	30	—	—	30	—	mA
Negative Supply Current	I_-		—	50	—	—	50	—	mA

**ELECTRICAL CHARACTERISTICS** at $V_+ = 5V$, $V_- = -5V$, $V_{REF} = 2.5V$, $f_{CLK} = 0.5MHz$; $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910AT/ET/GT			ADC-910BT/FT/HT			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution	N	$T_A = \text{Full Temp. Range}$	10	—	—	10	—	—	Bits
Resolution for which No Missing Codes Guaranteed		$T_A = \text{Full Temp. Range (Notes 2, 3)}$	10	—	—	10	—	—	Bits
Gain Error	G_{FSE}	$V_{REF} = 2.500V$ (Notes 2, 3)	—	—	4	—	—	6	LSB
Unipolar Mode Offset Error	V_{ZSE}	$T_A = \text{Full Temp. Range}$	—	—	1/2	—	—	1	LSB
Bipolar Mode Offset Error	V_{OSE}		—	—	1	—	—	1.5	LSB
Bipolar Mode Zero- Scale Offset Drift	TCV_{ZS}	$T_A = \text{Full Temp. Range (Note 1)}$	—	—	1	—	—	1.5	LSB
Analog Input Impedance	$R_{IN A}$	Pin 20	3.5	5	7	3.5	5	7	k Ω
Analog Input Impedance	$R_{IN B}$	Pin 19	1.75	2.5	3.5	1.75	2.5	3.5	k Ω
Reference Input Resistance	R_{REF}	Pin 22	1.75	2.5	3.5	1.75	2.5	3.5	k Ω
Reference Voltage Output	V_{REFOUT}	Pin 17, Untrimmed	2.45	2.50	2.55	2.45	2.50	2.55	V
Reference Voltage Trim Range		$R_T = 10k\Omega$	± 50	—	—	± 50	—	—	mV
Reference Output Load Regulation		$1mA < I < 5mA$, $T_A = \text{Full Temp. Range}$	—	—	1.5	—	—	1.5	mV/mA
Positive Power Supply Sensitivity	$+P_{SS}$	4.5V to 5.5V, V_{REF} External	—	—	1/2	—	—	1/2	LSB
Negative Power Supply Sensitivity	$-P_{SS}$	-4.5V to -5.5V, V_{REF} External	—	—	1/2	—	—	1/2	LSB
Conversion Time	T_C	$f_{CLK} = 1MHz$ (Note 5)	—	—	6	—	6	—	μs
Conversion Time	T_C	$f_{CLK} = 0.5MHz$ (Note 6)	—	—	12	—	12	—	μs
Digital Input High	V_{INH}	$T_A = \text{Full Temp. Range}$	2.0	—	—	2.0	—	—	V
Digital Input Low	V_{INL}	$T_A = \text{Full Temp. Range}$	—	—	0.8	—	—	0.8	V
Digital Input Current	I_{INH}	$T_A = \text{Full Temp. Range}$	—	0.4	1	—	0.4	1	μA
Digital Input Current	I_{INL}	$T_A = \text{Full Temp. Range}$	—	10	20	—	10	20	μA
Digital Output High	V_{OH}	$I_{OH} = -400\mu A$, $T_A = \text{Full Temp. Range}$	2.4	3.7	—	2.4	3.7	—	V
Digital Output Low	V_{OL}	$I_{OL} = 1.6mA$, $T_A = \text{Full Temp. Range}$	—	0.1	0.4	—	0.1	0.4	V
Digital Output Current	I_{OH}	$V_{OH} = 2.4V$	-400	—	—	-400	—	—	μA
Digital Output Current	I_{OL}	$V_{OL} = 0.4V$	—	—	1.6	—	—	1.6	mA
Three-State Output Leakage	I_{OZ}	$T_A = \text{Full Temp. Range}$	—	5	10	—	5	10	μA

NOTES:

1. Change in $25^\circ C$ value from $25^\circ C$ to T_{Min} or T_{Max} .
2. Tested in the 5V unipolar mode at $6\mu s$ conversion time.
3. Tested in the $\pm 5V$ bipolar mode at $12\mu s$ conversion time.
4. Measured individually on V_+ and V_- supplies.
5. Applies to 5V input unipolar operation; see Figure 1 for connections.
6. Applies to 10V input unipolar operation, and $\pm 5V/\pm 10V$ input bipolar operation; see Figure 1 for connections.

APPLICATIONS INFORMATION

CIRCUIT OPERATION (refer to the simplified schematic)

The ADC-910 uses a successive approximation type A/D conversion routine. When a start command is received by the command register, the SAR, DAC and comparator begin a bit-by-bit trial against the analog input voltage. When all ten bits have been tried, the ten data outputs of the SAR will contain a 10-bit digital representation of the analog input voltage.

When the conversion is complete, a read command and a chip selection will output the data through the 3-state output buffers. Selecting $\overline{CS1}$ will output the eight MSBs (the high byte) and selecting $\overline{CS2}$ will output the two LSBs (the low byte). Selecting both $\overline{CS1}$ and the $\overline{CS2}$ will cause all ten data bits to be output through the 3-state output buffers.

When the conversion is complete, the SAR sends an end of conversion (EOC) signal to the command register, which turns on the interrupt output open-collector NPN transistor (\overline{INT}), providing the interrupt disable bit (\overline{INE}) is set to "0". The EOC signal is also multiplexed into the input of the 3-state buffer for bit 9 (B9). Also, at this time, the overrange signal appears at the SAR output and is multiplexed into the input of the 3-state buffer for bit 8 (B8). These two bits of information comprise the status register, which is multiplexed to the data bus with a read command and a selection of $\overline{CS3}$.

Unipolar/bipolar mode selection and the enabling/disabling of the interrupt output is done when the start of conversion

command is entered. In the unipolar mode, the I_{MSB} current source is turned off. For bipolar mode operation, the I_{MSB} current source is applied to the summing mode of the comparator. This provides the proper offset of I_{MSB} to do a bipolar conversion.

BASIC CONNECTIONS (refer to Fig. 1)

Power Supply Connections: The ADC-910 is operated on ± 5 volt power supplies. +5 volts is applied to pin 15 and -5 volts is applied to pin 23. These lines should be bypassed near the device with a $0.1\mu F$ capacitor in parallel with a large value capacitor such as $10\mu F$.

Analog and Digital Ground: Separate analog and digital grounds are provided to maintain optimum noise rejection. Care should be maintained to insure that digital switching noise is not introduced into the analog ground line. This can be accomplished by making the final ground point as close (physically and electrically) as possible to the analog ground pin of the ADC-910.

Analog Inputs: There are two analog voltage inputs to the ADC-910. V_{INA} (pin 20) accepts input signals between 0 volts and +10 volts in the unipolar mode and between -5 volts and +5 volts in the bipolar mode. V_{INB} (pin 19) accepts input signal levels between 0 volts and +5 volts in the unipolar mode and between -2.5 volts and +2.5 volts in the bipolar mode. The input resistance is nominally $5k\Omega$ for V_{INA} and $2.5k\Omega$ for V_{INB} . The comparator offset pin (pin 18) is left open when using V_{INA} , and is tied to analog ground when using V_{INB} .

FIGURE 1: BASIC CONNECTIONS

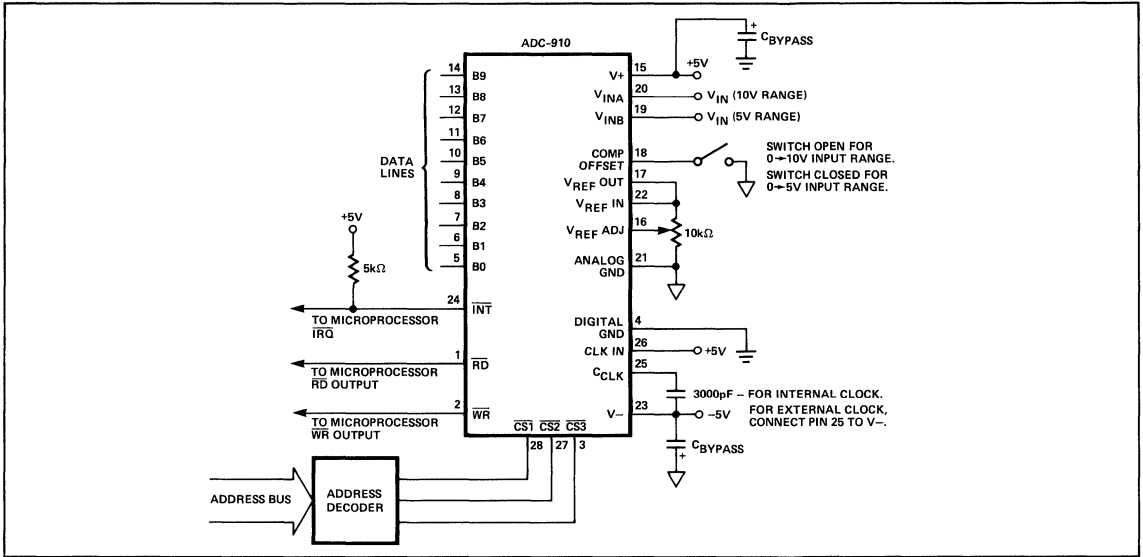


FIGURE 2: START CONVERSION AND OPERATING MODE SELECTION (WRITE MODE WR = "LOW", CS3 = "LOW")

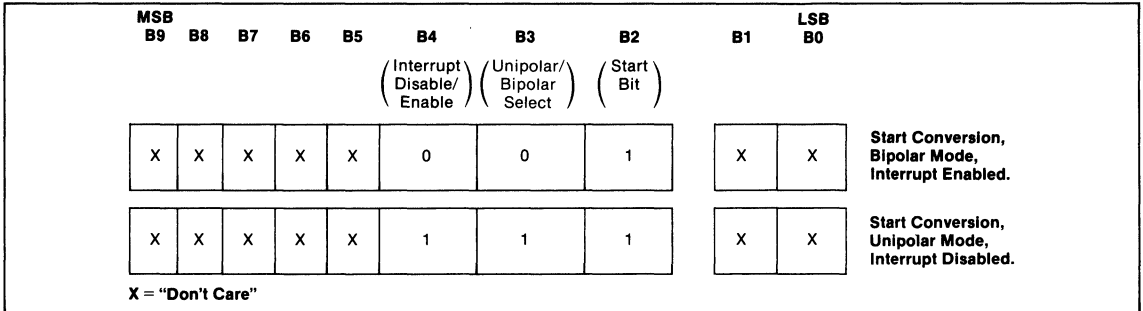


FIGURE 3: READING DATA AND STATUS (READ MODE RD = "LOW")

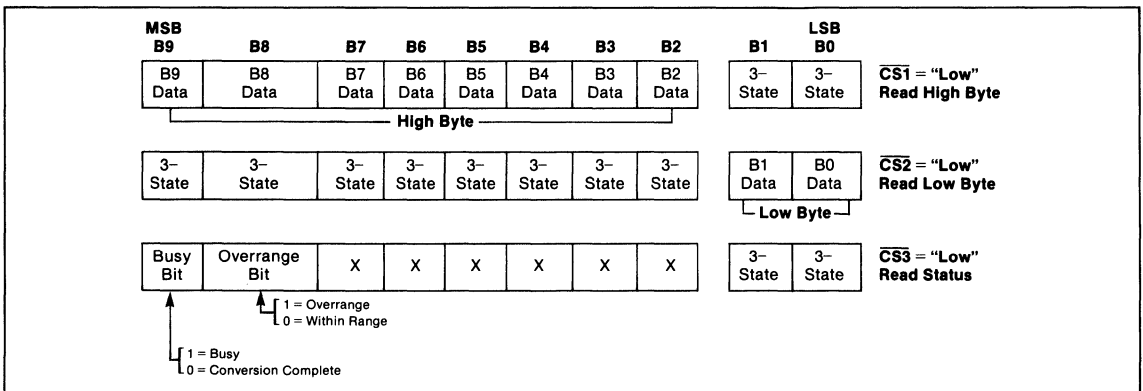
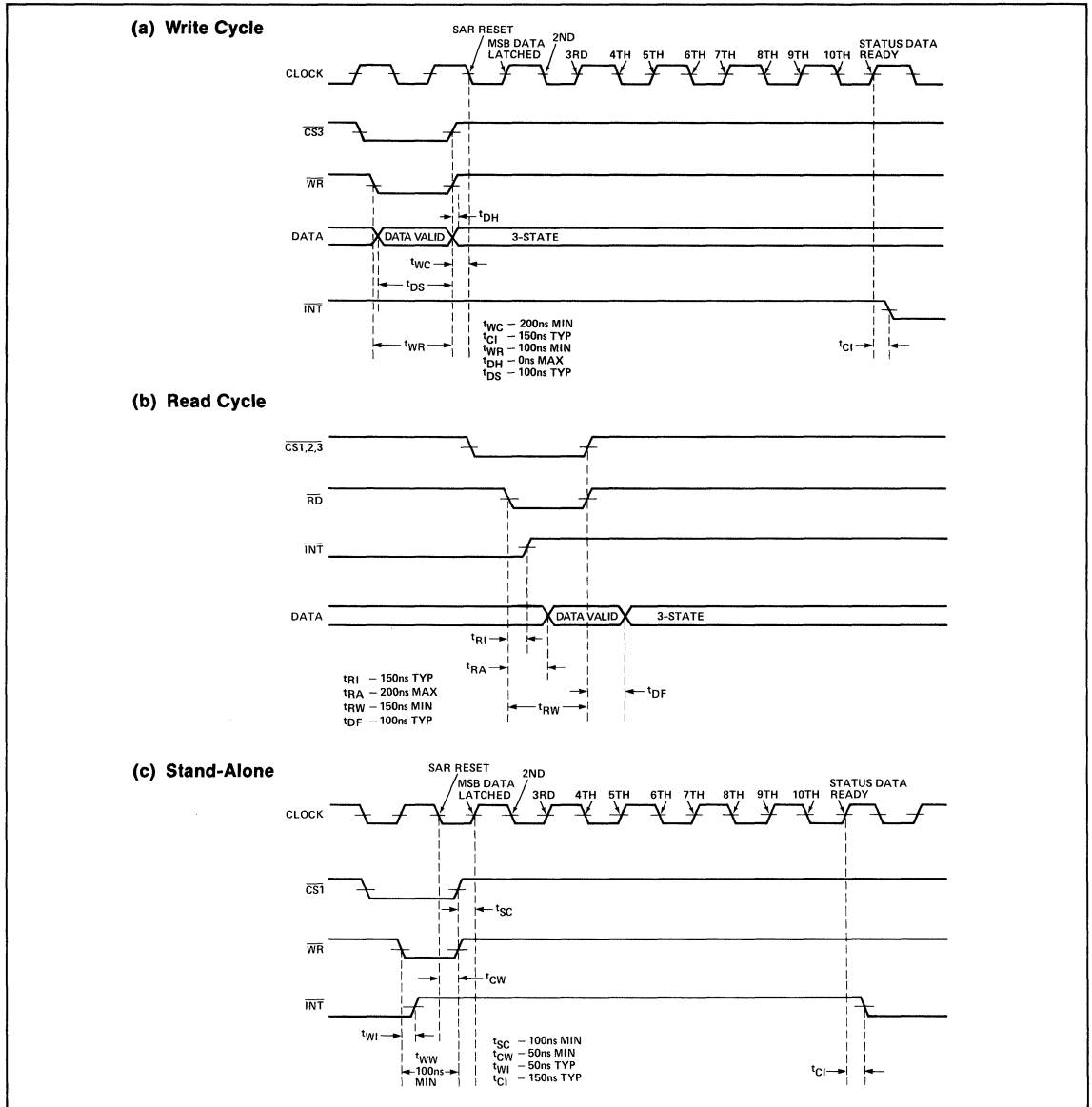


FIGURE 4: ADC-910 TIMING DIAGRAMS


Voltage Reference: The voltage reference for the ADC-910 is nominally +2.5 volts. To use this internal reference, the reference output pin (pin 17) should be tied to the reference input pin (pin 22). Adjustment of the reference voltage may be done by applying a 10k Ω trimpot between the reference output and analog ground with the center tap wiper tied to the

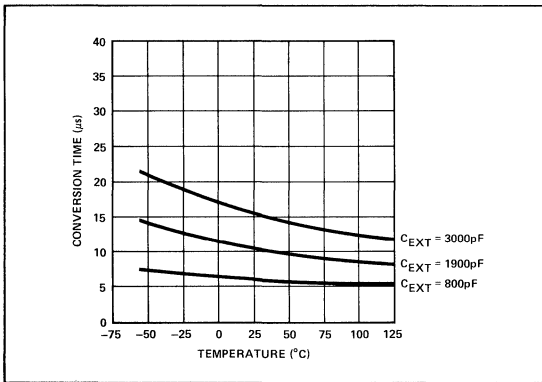
reference adjust pin (pin 16).

To use an external reference with the ADC-910, simply apply it to the V_{REF} input pin (pin 22). This voltage should be bypassed to analog ground with a 0.1 μ F capacitor.

Clock: For internal clock operation, the external capacitor (C_{CLK}) sets the conversion rate. The conversion rate graph provides the relationship of C_{CLK} and temperature to conversion rate. The C_{CLK} capacitor is connected between C_{CLK} (pin 25) and the $V-$ supply (pin 23), see Figure 1. The clock input (pin 26) is connected to the $V+$ supply (pin 15). Internal clock operation exhibits a conversion time variation from device to device for a given C_{CLK} , due to capacitor and internal resistor tolerances of the basic R-C oscillator. For operation at the upper frequencies of 0.5 and 1MHz, an external clock input is recommended.

For external clock operation, no clock capacitor is required. The C_{CLK} pin (pin 25) should be tied to the -5 volt supply and the external clock is applied to the clock input (pin 26). 1.0MHz clock maximum may be used. This will result in a $6\mu s$ conversion time. Slower clock rates will result in slower conversion speeds.

$$\text{Conversion time} \approx 6 \times \frac{1}{f_{CLK}}$$



CHIP SELECT, READ AND WRITE INPUTS (refer to Fig. 2)

Start Commands: To start a conversion the \overline{WR} input (pin 2) must be held "low" while $\overline{CS3}$ (pin 3) is held "low" and a logic "high" is applied to bit 2 (pin 7). Another way to start a conversion is to hold $\overline{CS1}$ (pin 28) and \overline{WR} (pin 2) "low" for a complete clock cycle.

Operating mode selection is done when the start command is applied. As with the start command, \overline{WR} and $\overline{CS3}$ are held "low". A logic "high" applied to bit 4 (pin 9) disables the interrupt and a logic "low" enables the interrupt. A logic "high" applied to bit 3 (pin 8) selects unipolar mode and a logic "low" selects bipolar-mode operation.

READING DATA AND CONVERSION STATUS

(refer to Fig. 3)

Data can be read in two ways: a single 10-bit word or in a 8-bit "high byte" with a 2-bit "low byte". When interfacing to a

16-bit bus, single 10-bit word reading is possible. When using an 8-bit data bus, the "high byte" and "low byte" can be multiplexed onto a single 8-bit bus as indicated in Fig. 5.

To read all 10 bits at once, the \overline{RD} (pin 1), $\overline{CS1}$ (pin 28) and $\overline{CS2}$ (pin 27) are all held "low". This turns on 3-state output buffers and all data bits can be read.

To read the 8-bit "high byte", the \overline{RD} (pin 1) and $\overline{CS1}$ (pin 28) lines are held "low".

To read the 2-bit "low byte", the \overline{RD} and $\overline{CS2}$ lines are held "low".

Included on the ADC-910 is a 2-bit status register which is multiplexed onto the data bus on lines B9 and B8.

To read the status register, \overline{RD} (pin 1) and $\overline{CS3}$ are held "low". End of conversion (EOC) is indicated by a "low" bit 9 (pin 14) and overrange (OR) is indicated by a "high" in bit 8 (pin 13).

CALIBRATION (10 Volt unipolar mode only)

To adjust out gain error, a trimpot may be inserted in series with the analog input voltage input. Assuming a 2.500 volt reference is applied at the reference input, gain error trimming is accomplished by adjusting the input trimmer so that the final digital output code transition occurs for an input voltage of $V_A = 9.985$ volts (this is the transition from 111111110 to 111111111). When using the internal reference or an adjustable external reference, gain error trimming may be accomplished by adjusting the reference voltage until the final digital output code transition occurs at $V_A = 9.985$ volts.

DRIVING THE ANALOG INPUT

To insure 10-bit accuracy the input to the ADC-910 must be driven by a source which has an output impedance of less than 0.5 ohms at 1MHz.

INTERFACING THE ADC-910 TO THE 6502µP

(refer to Fig. 5)

An example of direct connection to an 8-bit data bus is shown in Fig. 5. Notice that the two least significant bits are connected to data bits B3 and B4. This allows a 10-bit data transfer over an 8-bit bus. In this example, a Synertek Systems SYM-1 Educational Computer Board supports the 6502µP. The flow charts and op codes for a variety of conversion exercises are shown below.

INTERFACING THE ADC-910 TO THE MC68000

(refer to Fig. 6)

An example of a direct connection to a 16-bit data bus is shown in Fig. 6. The 10-bit output of the ADC-910 is connected directly to the 10 least significant bits of the MC68000 data bus. In this example a Motorola MC68000 Computer Board supports the 68000µP. A flow chart and assembly language program is shown below for a simplified 10-bit wide conversion.

FIGURE 5: ADC-910 INTERFACE TO 6502 μ P ON SYM-1 BOARD

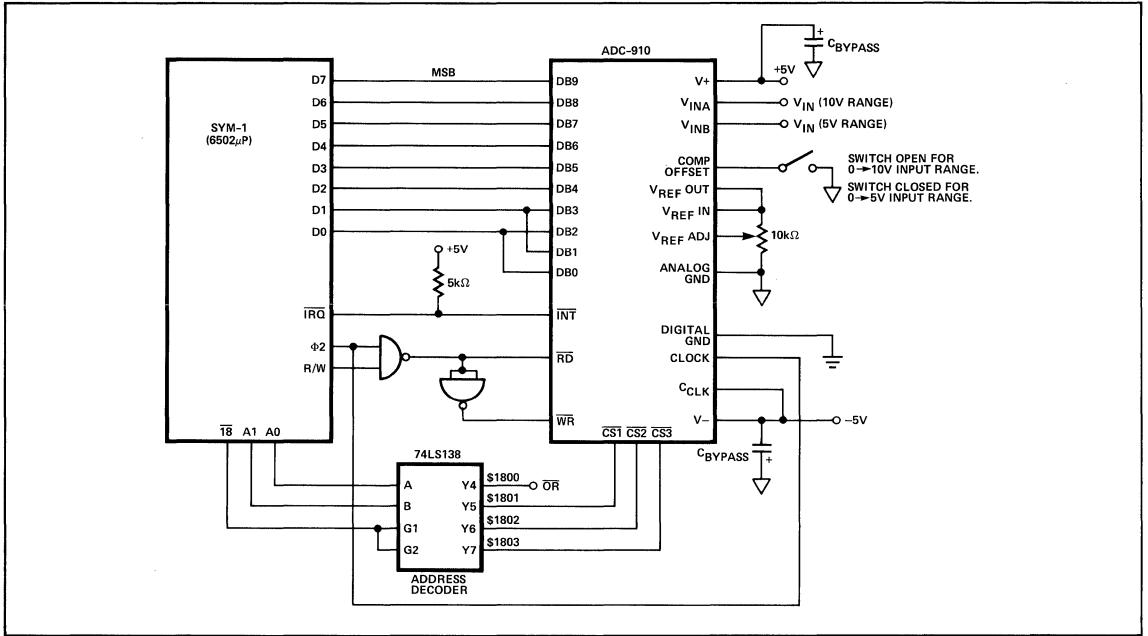
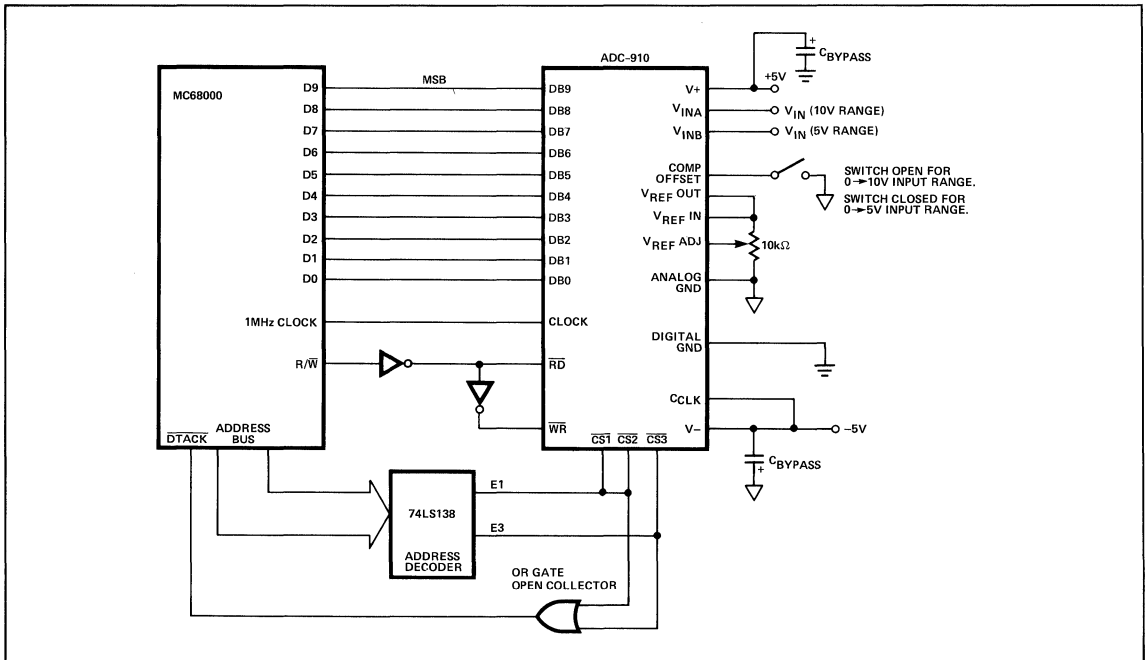
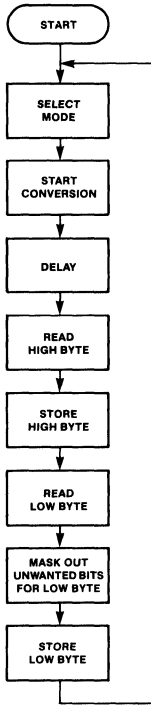
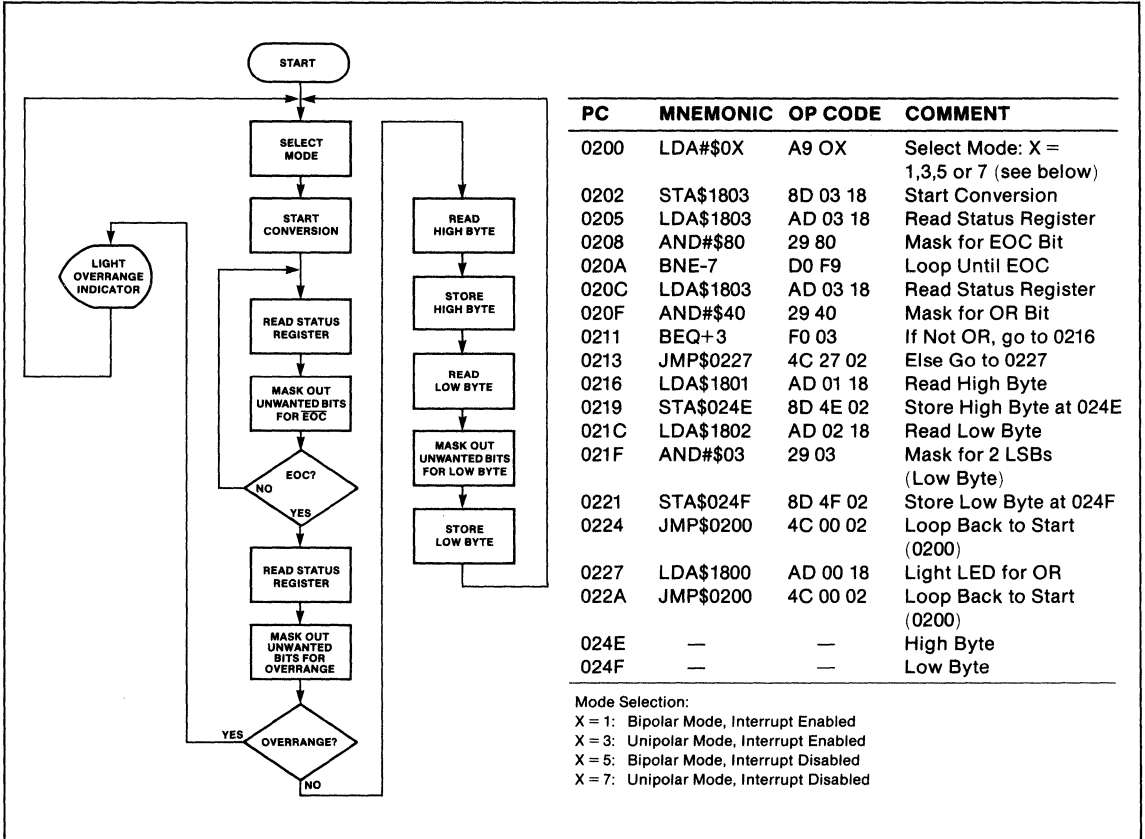


FIGURE 6: ADC-910 INTERFACE TO MC68000 COMPUTER BOARD



**ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 6502 μ P (SYM-1)
 Unipolar Mode, Interrupt Disabled**


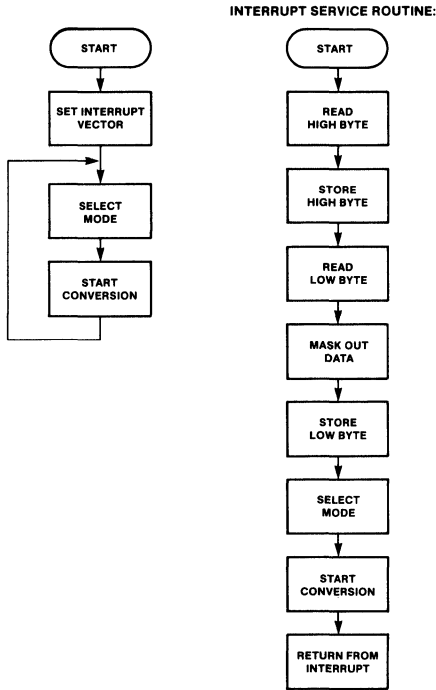
PC	MNEMONIC	OP CODE	COMMENT
0302	LDA#\$07	A9 07	Select Mode
0304	STA\$1803	8D 03 18	Start Conversion
0307	NOP	EA	Wait 2 μ s
0308	NOP	EA	Wait 2 μ s
0309	LDA\$1801	AD 01 18	Read High Byte
030C	STA\$03A0	8D A0 03	Store High Byte
030F	LDA\$1802	AD 02 18	Read Low Byte
0312	AND#\$03	29 03	Mask Bits B7--B2
0314	STA\$03A1	8D A1 03	Store Low Byte
0317	JMP\$0302	4C 02 03	Go to 0302

ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 6502 μ P (SYM-1)
Polled Mode, Overrange Test


PC	MNEMONIC	OP CODE	COMMENT
0200	LDA#\$0X	A9 0X	Select Mode: X = 1,3,5 or 7 (see below)
0202	STA\$1803	8D 03 18	Start Conversion
0205	LDA\$1803	AD 03 18	Read Status Register
0208	AND#\$80	29 80	Mask for EOC Bit
020A	BNE-7	D0 F9	Loop Until EOC
020C	LDA\$1803	AD 03 18	Read Status Register
020F	AND#\$40	29 40	Mask for OR Bit
0211	BEQ+3	F0 03	If Not OR, go to 0216
0213	JMP\$0227	4C 27 02	Else Go to 0227
0216	LDA\$1801	AD 01 18	Read High Byte
0219	STA\$024E	8D 4E 02	Store High Byte at 024E
021C	LDA\$1802	AD 02 18	Read Low Byte
021F	AND#\$03	29 03	Mask for 2 LSBs (Low Byte)
0221	STA\$024F	8D 4F 02	Store Low Byte at 024F
0224	JMP\$0200	4C 00 02	Loop Back to Start (0200)
0227	LDA\$1800	AD 00 18	Light LED for OR
022A	JMP\$0200	4C 00 02	Loop Back to Start (0200)
024E	—	—	High Byte
024F	—	—	Low Byte

Mode Selection:
 X = 1: Bipolar Mode, Interrupt Enabled
 X = 3: Unipolar Mode, Interrupt Enabled
 X = 5: Bipolar Mode, Interrupt Disabled
 X = 7: Unipolar Mode, Interrupt Disabled

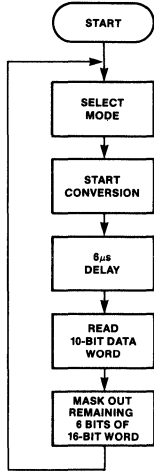
ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 6502 μ P (SYM-1)
Interrupt-Driven Conversion



PC	MNEMONIC	OP CODE	COMMENT
0200	LDA#\$02	A9 02	Set Interrupt Vector
0202	STA\$A679	8D 79 A6	
0205	LDA#\$10	A9 12	
0207	STA\$A678	8D 78 A6	
020A	LDA#\$03	A9 03	Select Mode (Unipolar, Interrupt Enabled)
020C	STA\$1803	8D 03 18	Start Conversion
020F	JMP\$20A	4C 0A 02	Jump to 20A (Loop Until Interrupt)
Interrupt Service Routine			
0212	LDA\$1801	AD 01 18	Read High Byte
0215	STA\$024E	8D 4E 02	Store High Byte at 024E
0218	LDA\$1802	AD 02 18	Read Low Byte
021B	AND#\$03	29 03	Mask Out Bits 9--4
021D	STA\$024F	8D 4F 02	Store Low Byte at 024F
0220	LDA#\$03	A9 03	Select Mode
0222	STA\$1803	8D 03 18	Start Conversion
0225	RTI	40	Return from Interrupt



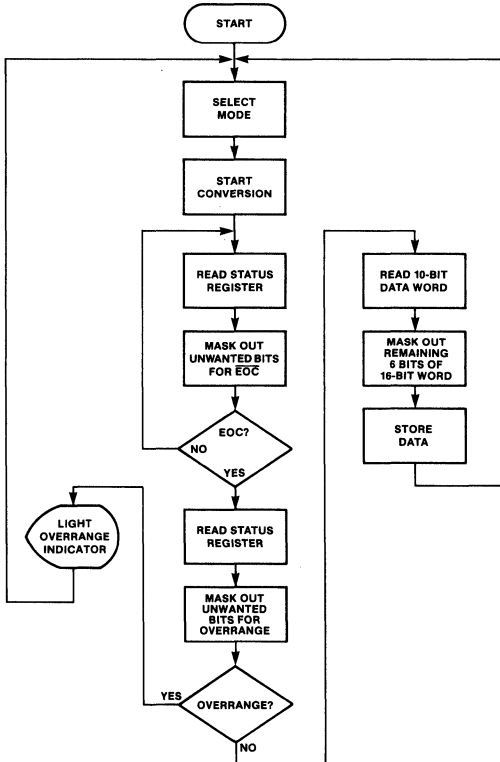
**ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 16-BIT μ P
MC68000 Computer Board Start Sequence**



PC	MNEMONIC	COMMENT
1000	MOVEQ #12, D0	Select Mode*
1002	MOVE D0, \$50000	Start Conversion
1008	NOP	
100A	NOP	Delay
100C	NOP	
100E	MOVE \$20000, D1	Read Data
1014	ANDI #1023, D1	Mask out B15→B10 leaving B9→B0
1008	JMP \$1000	Jump to 1000

* Loading a decimal 12 into D0 will apply the following binary word to the command register at the start of the conversion:
 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
 0 0 0 0 0 0 1 1 0 0
 This results in unipolar mode selection with the interrupt disabled.

**ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 16-BIT μ P
MC68000 Computer Board Polling Status Register**



PC	MNEMONIC	COMMENT
1000	MOVEQ #X,D0	Select Mode*
1002	MOVE D0, \$50000	Start Conversion
1008	MOVE \$50000,D1	Read Status Register into D1
100E	AND #512,D1	Mask for EOC Bit (1000000000 = 512 Decimal)
1012	BNE.L \$1008	Loop Until EOC
1016	MOVE \$50000,D2	Read Status Register
101C	AND #256,D2	Mask for OR Bit (0100000000 = 256 Decimal)
1020	BEQ.L \$102E	Branch to \$102E Unless OR
1024	MOVE D3,\$40000	Light OR Indicator
102A	JMP \$1000	Start Over
102E	MOVE \$20000,D4	Read and Store 10-Bit Data
1032	AND #1023,D4	Mask Unwanted 6 LSBs
1036	JMP \$1000	Start Over

*For Bipolar Mode with Interrupt Enabled: X = 4 Decimal
 For Unipolar Mode with Interrupt Enabled: X = 12 Decimal
 For Bipolar Mode, Interrupt Disabled: X = 20 Decimal
 For Unipolar Mode, Interrupt Disabled: X = 28 Decimal



ADC-8208

MICROPROCESSOR-COMPATIBLE
8-BIT CMOS A/D CONVERTER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- **Fast Conversion Time** 5 μ s
- **8-Bit Accuracy** $\pm 1/2$ LSB Max INL
- **Memory-Mapped Interface**
- **Low Power Dissipation** 30mW
- **Operates from Single +5V**
- **Fits AD7574 Sockets, with Improved Conversion Time**
- **Space Saving 0.3 Inch Wide 18-Pin DIP**

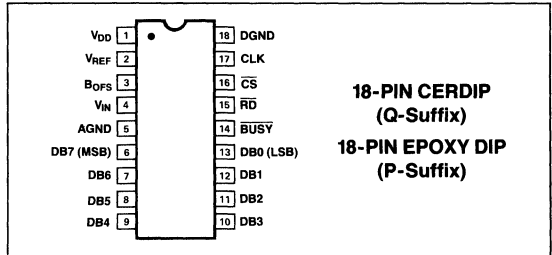
The ADC-8208 provides an improved second-source to the AD7574, providing a three-times faster conversion time.

This low power device is ideal for process control, instrumentation, navigation, and general data-acquisition systems.

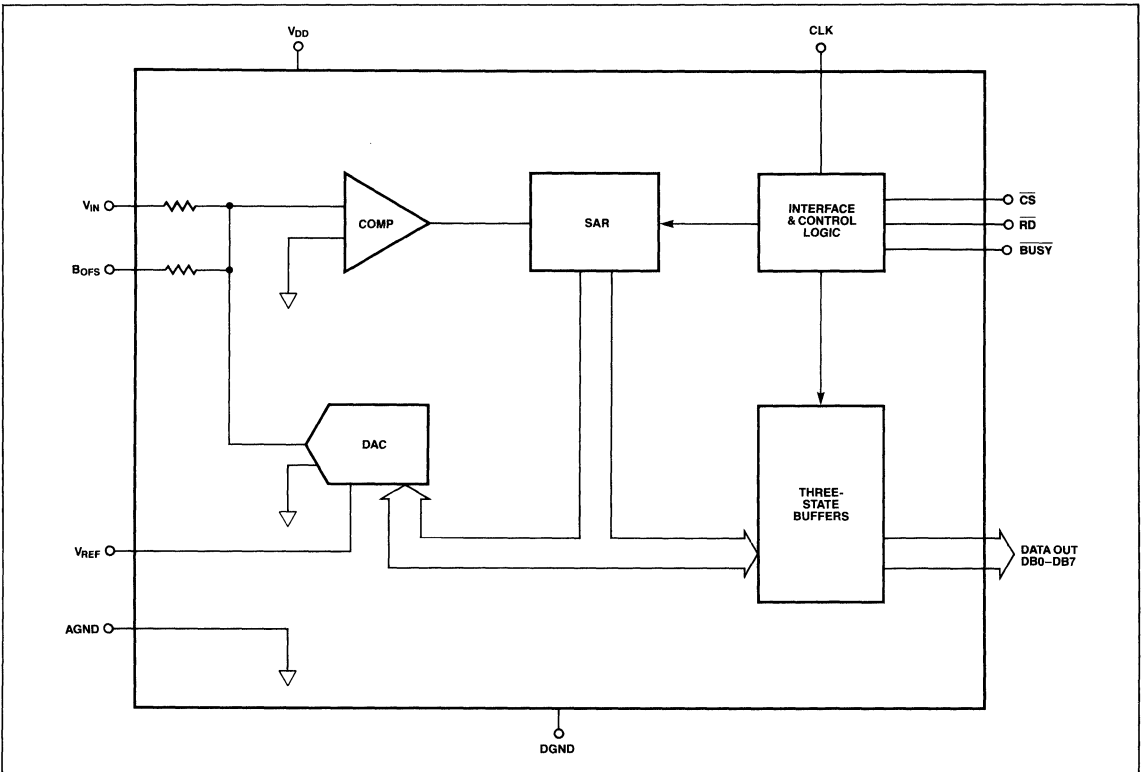
GENERAL DESCRIPTION

The ADC-8208 is an 8-bit microprocessor compatible A/D converter which uses the successive-approximation conversion technique to provide a 5 μ s maximum conversion time. Control logic and three-state data output buffers constitute the memory-mapped microprocessor interface. The \overline{CS} and \overline{RD} control lines reset the converter, start conversion, and read output data. The \overline{BUSY} output indicates conversion in progress.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



ANALOG SWITCHES MULTIPLEXERS

Precision Monolithics Inc.

- | | | | |
|-------|--------------------------------|-------|---|
| 13-3 | Introduction | 13-48 | MUX-08/MUX-24 |
| 13-3 | Definitions | | 8-Channel/Dual 4-Channel JFET
Analog Multiplexers |
| 13-7 | SW-01/SW-02 | 13-59 | MUX-16/MUX-28 |
| | Quad SPST JFET Analog Switches | | 16-Channel/Dual 8-Channel JFET
Analog Multiplexers |
| 13-14 | SW-05 | 13-69 | MUX-88 |
| | Dual SPST JFET Analog Switch | | 8-Channel Analog Multiplexer For
PCM CODECs |
| 13-22 | SW-06 | 13-74 | DMX-88 |
| | Quad SPST JFET Analog Switch | | 8-Channel Analog De-Multiplexer |
| 13-33 | SW-201/SW-202 | | |
| | Quad SPST JFET Analog Switches | | |
| 13-40 | SW-7510/SW-7511 | | |
| | Quad SPST JFET Analog Switches | | |

ANALOG SWITCHES MULTIPLEXERS

INTRODUCTION

Analog multiplexers and switches find applications in data acquisition, metrology, telemetry, process control and telephony systems. Multiplexers are multiple analog switches which share a common output. An on-chip address decoder selects the appropriate input by means of a binary code. All channels may be deactivated by an enable/disable control pin.

In the past multiplexers/switches have been manufactured with hybrid, monolithic CMOS or dielectrically isolated CMOS technologies. The merging of ion implant techniques with the standard bipolar process creates a fourth technological alternative — the bipolar-JFET process. High-quality ion implanted p-channel FET's can now be compatibly processed with bipolar devices.

The cost of hybrid devices limits their use to applications which require the extremely low "R_{ON}" resistance made possible by discrete FET's. MOS technologies are inherently plagued by SCR "latch up" problems and analog signal overvoltage destruction. The use of buried layers and expensive dielectric isolation processing can eliminate the SCR failure mode, but the overvoltage blowout problems can be solved only by adding large series input resistance with each switch. This increases system errors since the equivalent "R_{ON}" may typically be over 1000 ohms.

JFET switches have no SCR "latch up" tendency and can withstand analog input overvoltages while maintaining low "R_{ON}" resistance. In addition, the special handling required with CMOS devices is not necessary with JFET switches.

In selecting analog multiplexers, attention must be paid to several key specs. Break-before-make switching insures no two-channel inputs are simultaneously connected. This prevents input sensor damage and misoperation. Acquiring analog input signals within a specified time and error band are primary concerns affected by "R_{ON}" resistance and "C_{OUT}" capacitance specifications. A low "R_{ON}" insures minimum signal attenuation and maximum accuracy. The "C_{OUT}" capacitance forms on R-C time constant

with "R_{ON}" placing fundamental limits on signal acquisition time. Low "R_{ON}" and "C_{OUT}" insures minimum elapsed time between the channel select command and the acquisition of data to within a specified error band. High cross talk and off isolation specifications prevent unselected input signals from affecting the signal path.

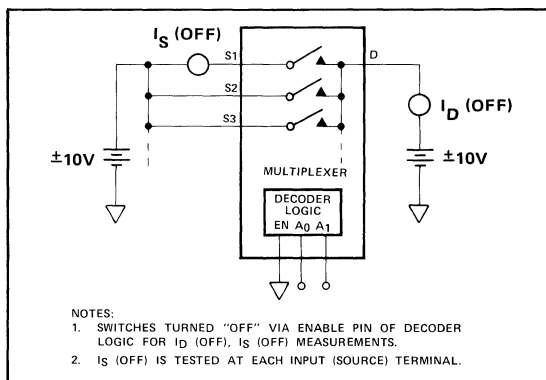
PMI offers a wide selection of single-ended and differential multiplexers and switches. Sixteen and eight-channel multiplexers as well as differential eight and four-channel devices are available. Dual and Quad SPST switches in normally closed and open configurations are also available. All devices are pin-for-pin replacements for many industry standard CMOS devices.

DEFINITIONS

Analog Current Range (I_A, I_S) — The minimum range of currents the switch is capable of conducting in the ON state without degrading ON resistance. It is measured as the value of conduction current that does not cause more than a doubling of the R_{ON} value for the product grade.

Analog Input Leakage Current (I_{S(OFF)}) — The algebraic sum of diode current losses from an OFF-channel source input to the power supplies, ground and through the channel. Specified

I_{D(OFF)}, I_{S(OFF)} Test Condition Definitions





ANALOG SWITCHES MULTIPLEXERS

as an absolute value, as the direction of current flow is not predictable.

Analog Output Leakage Current ($I_{D(OFF)}$) — The algebraic sum of diode current losses from an OFF-channel "D" output to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

Analog Output-To-Input Capacitance ($C_{DS(OFF)}$) — The equivalent capacitance which shunts an open switch effectively between "S" and "D" output.

Analog Input Capacitance ($C_{S(ON)}$) — The capacitance between an analog "S" input and ground with the channel ON.

Analog Input Capacitance ($C_{S(OFF)}$) — The capacitance between an analog "S" input and ground with the channel OFF.

Analog Output Capacitance ($C_{D(OFF)}$) — The capacitance between the analog (DRAIN) output and ground with the channel OFF. High-frequency transmission and output settling time characteristics are highly influenced by this parameter in conjunction with R_{ON} .

Analog Output Capacitance ($C_{D(ON)}$) — The capacitance between the analog "D" output and ground with the channel ON.

Analog Voltage Range (V_A) — The range of analog-voltage amplitudes, with-respect-to ground, over which the analog switch operates (ON/OFF) within the R_{ON} and leakage specifications — $I_{S(OFF)}$, $I_{D(OFF)}$ and $I_{D(ON)} + I_{S(ON)}$.

Break-Before-Make Delay (t_{OPEN}) — The elapsed time between the turn-off of one analog input and the subsequent turn-on of another input as determined by the appropriate instantaneous change in the digital input code for both inputs measured between the outputs' 50% transition points.

Channel Capacitance ($C_{SS(OFF)}$, $C_{DD(OFF)}$) — The capacitance between the D(S) terminals of any two channels.

Charge Transfer (Q) — Charge transfer appears as a voltage step (pedestal) on the output capacitor after switch turn OFF. The undesirable charge AC couples directly from the logic-control driver to the switch contact.

Crosstalk (CT) — The proportionate amount of cross-coupling from an analog input channel to another output channel, expressed in dB.

Digital Input Capacitance (C_{DIG}) — The capacitance between a digital input and ground.

Insertion Loss — Insertion loss measures the amount of signal power absorbed by the switch ON resistance at a given measurement frequency. Insertion loss is defined in decibels as a ratio of the output-voltage amplitude (V_D) versus the input-voltage amplitude (V_S) with a specified load impedance.

$$\text{Insertion Loss (dB)} = 20 \log \frac{|V_D|}{|V_S|}$$

At low frequencies this equation simplifies to:

$$\text{Insertion Loss (dB)} = 20 \log \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Logic "0" Input Current (I_{INL}) — The current flowing into a digital input when a specified low-level voltage is applied to that input.

Logic "0" Input Voltage Level (V_{INL}) — The maximum (or most-positive) digital low-level input voltage for which proper operation of the device is guaranteed.

Logic "1" Input Voltage Level (V_{INH}) — The minimum (or least-positive) digital high-level input voltage for which proper operation of the device is guaranteed.

Negative Voltage Supply (V^-) — The most negative voltage supply with respect to ground.

Positive Voltage Supply (V^+) — The most positive voltage supply with respect to ground.

OFF Isolation (ISO_(OFF)) — The proportionate amount of a high-frequency analog input signal which is coupled through the channel of an OFF device. This feedthrough is transmitted through C_{DS(OFF)} to a load comprised of C_{D(OFF)} in parallel with an external load. Isolation generally decreases by 6dB/octave with increasing frequency.

ON Resistance (R_{ON}) — The series ON - channel resistance measured between "S" input and "D" output terminals under specified conditions.

ON Resistance Match (R_{ON} Match) — The channel-to-channel matching of ON resistance when channels are operated under identical conditions.

$$R_{ON \text{ Match}} = \frac{R_i - R_{AVG}}{R_{AVG}} \times 100\%$$

where

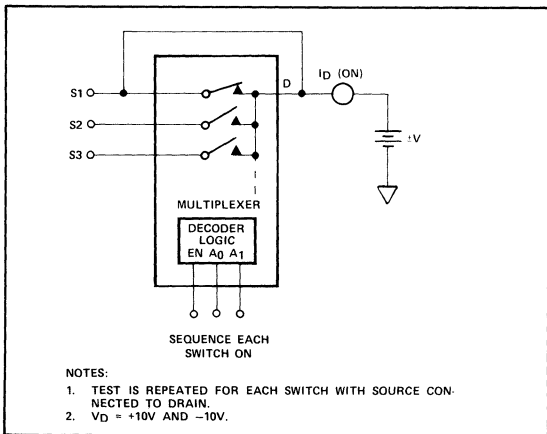
N = # of channels in package (i.e., for MUX-08

N = 8, for MUX-16 N = 16, etc.)

R_i = Each channel's ON resistance

$$R_{AVG} = \frac{1}{N} \sum_{i=1}^N R_i$$

I_{D(ON)} Test Condition Definitions



ON Resistance Variation (ΔR_{ON}) — The variation of ON resistance produced by the specified analog input voltage change with a constant load current.

$$\Delta R_{ON} (\%) =$$

$$\frac{R_{ON @ V_A = -10V} - R_{ON @ V_A = +10V}}{R_{ON @ V_A = 0V}} \times 100\%$$

ON Channel Analog Leakage Current (I_{D(ON)} + I_{S(ON)}) Current loss (or gain) through an ON-channel resistance creating a voltage offset across the device. As the direction of current flow is not predictable, only the magnitude is specified at various temperature ranges.

Output Enable Delay Time OFF (t_{OFF(EN)}) — Multiplexers — The time required to disconnect the analog output from the analog input determined by the digital address input code. It is measured from the 50% point of ENABLE input logic change to the time the output reaches 10% of the initial value.

Output Enable Delay Time ON (t_{ON(EN)}) — Multiplexers — The time required to connect the analog output to the analog input determined by the digital address input code. It is measured from the 50% point of the ENABLE input logic change to the time the output is within 90% of final value.

Output ON Switching Time (t_{ON}) — The time required to connect the analog output to the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 90% of the final value.

Output OFF Switching Time (t_{OFF}) — The time required to disconnect the analog output from the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

Output Settling Time (t_s) — The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. It is measured from the 50% point of the logic input change to the time the output reaches final value within specified error band.



ANALOG SWITCHES MULTIPLEXERS

Precision Monolithics Inc.

Power Supply Rejection (PSRR) — The ratio of the change in switch contact voltage (V_D) to the change in voltage supply ($V+$ or $V-$) that causes it.

$$+PSRR \text{ (dB)} = 20 \log \left(\frac{\Delta V_D}{\Delta V+} \right)$$

$$-PSRR \text{ (dB)} = 20 \log \left(\frac{\Delta V_D}{\Delta V-} \right)$$

Switching Time (t_{TRAN}) — Multiplexers — The time required to switch and slew from one analog input channel to another analog input with a full-scale differential between inputs with a high impedance output load. The time is measured from the 50% point of the logic input change to the time the output reaches 80% of the final value.

Total Harmonic Distortion (THD) — The ratio of the signal power at the fundamental frequency to the signal power of all harmonics observed at the switch output (V_D) with a pure sinusoid applied to the switch input (V_S).



SW-01/SW-02

QUAD SPST JFET ANALOG SWITCHES (TEMPERATURE COMPENSATED R_{ON})

Precision Monolithics Inc.

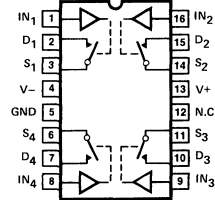
FEATURES

- Low R_{ON} vs Temperature 0.03%/°C
- Low Absolute R_{ON} 85Ω
- Low R_{ON} Variation vs Analog Signal 7%
- High Speed 300ns
- Low Leakage Current 0.2nA
- Overvoltage and Supply Loss Protected
- SW-01 is Improved Pin Compatible Device for DG201, ADG201, LF11201
- SW-02 is Improved Pin Compatible Device for DG202, LF11202, IH202

vs. analog input signals. The junction FET construction also reduces static discharge destruction prevalent in CMOS devices.

Low R_{ON} sensitivity to temperature and voltage is complemented by guaranteed high-speed operation and low-leakage currents. Logic inputs may operate directly from either CMOS or TTL logic levels and are supply voltage independent. The SW-01/02 are protected during supply voltage power loss and against input signal overvoltages.

PIN CONNECTIONS



16-PIN DUAL-IN-LINE PACKAGE
(Q-Package)

CONTROL LOGIC

LOGIC IN_y	SWITCH STATE	
	SW-01	SW-02
0	ON	OFF
1	OFF	ON

NOTE: $IN_y =$ INPUT 1-4

ORDERING INFORMATION†

16-PIN HERMETIC DUAL-IN-LINE PACKAGE

FUNCTION	MILITARY*	INDUSTRIAL
N.C.	SW01BQ	SW01FQ
N.O.	SW02BQ	SW02FQ

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

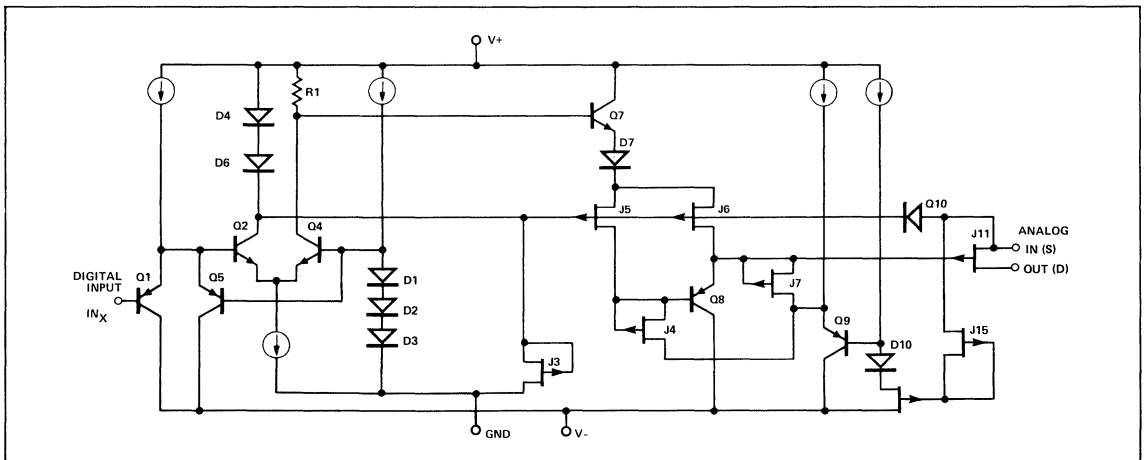
† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The SW-01/02 are four-channel single-pole, single-throw analog switches which offer operating characteristics unavailable in other JFET or CMOS devices. A unique circuit design provides a nearly constant R_{ON} over the full operating temperature span. R_{ON} drift typically runs under 300ppm/°C.

The SW-01/02 are pin compatible with the DG201/202. An Ion Implanted FET switch inherently exhibits low R_{ON} variations

SIMPLIFIED SCHEMATIC DIAGRAM (TYPICAL SWITCH)



ANALOG SWITCHES/MULTIPLEXERS

13

**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, unless otherwise noted).

Operating Temperature Range	SW-01/02BQ -55°C to $+125^\circ\text{C}$
	SW-01/02FQ -25°C to $+85^\circ\text{C}$
DICE Junction Temperature (T_J) -65°C to $+150^\circ\text{C}$
Storage Temperature Range -65°C to $+150^\circ\text{C}$
Power Dissipation (Q-Package) 900mW
Lead Temperature (Soldering, 60 sec) 300°C
Maximum Junction Temperature 150°C
V+ Supply to V- Supply 36V
V+ Supply to Ground 36V

Logic Input Voltage (V- or -4V) to V+ Supply
Logic Input Voltage	Continuous V- Supply -25V to V+ Supply +25V
	For $V+ = V- = 0$ $\pm 15\text{V}$
Maximum Current Through Any Pin 30mA
Peak Current,	(Pulsed at 1ms, 10% Duty Cycle) 70mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, and $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01/02B			SW-01/02F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$-10\text{V} \leq V_A \leq 10\text{V}$, $I_D \leq 1\text{mA}$	—	85	100	—	85	120	Ω
R_{ON} Match		(Note 1)	—	4	10	—	4	10	%
Analog Voltage Range	V_A	Full Temperature Range (Note 8)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V
ΔR_{ON} vs V_A	ΔR_{ON}	$V_A \leq 10\text{V}$, $I_D \leq 1\text{mA}$	—	7	10	—	7	10	%
Analog Current Range	I_A	$V_A \leq 10\text{V}$	—	5	—	—	5	—	mA
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$	—	0.2	1	—	0.2	2	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$	—	0.2	1	—	0.2	2	nA
Leakage Current in "ON" Condition	$I_{D(ON)}^+$ $I_{S(ON)}$	$V_S = \pm 10\text{V}$, (Note 2)	—	—	1	—	—	2	nA
"OFF" Isolation	ISO_{OFF}	Test Figure 2	—	58	—	—	58	—	dB
Crosstalk	C_T	Test Figure 3	—	70	—	—	70	—	dB
Turn-On-Time	T_{ON}	Test Figure, (Note 3)	—	300	400	—	300	400	ns
Turn-Off-Time	T_{OFF}	Test Figure 1, (Note 3)	—	200	300	—	200	300	ns
Break-Before-Make Time	$T_{ON} - T_{OFF}$	Test Figure 1, (Note 7)	—	100	—	—	100	—	ns
Source Capacitance	$C_{S(OFF)}$	$V_A \leq 10\text{V}$	—	7	—	—	7	—	pF
Drain Capacitance	$C_{D(OFF)}$	$V_A \leq 10\text{V}$	—	5.5	—	—	5.5	—	pF
Logic "1" Input Voltage	V_{INH}	Full Temperature Range (Note 8)	2	—	—	2	—	—	V
Logic "0" Input Voltage	V_{INL}	Full Temperature Range (Note 8)	—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$2 \leq V_{IN} \leq 15\text{V}$	—	1	3	—	1	3	μA
Logic "0" Input Current	I_{INL}	$0 \leq V_{IN} \leq 0.8\text{V}$	—	1	3	—	1	3	μA
Positive Supply Current	I+	(Note 5)	—	6.3	8.0	—	6.3	9.0	mA
Negative Supply Current	I-	(Note 5)	—	3.2	4.5	—	3.2	5.5	mA
Ground Current	I_G	(Note 5)	—	3.0	4.0	—	3.0	4.5	mA

NOTES:

1. $V_A = 0\text{V}$, $I_D = 100\mu\text{A}$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. The conditions listed specify the worst case leakage current. The leakage currents apply equally to source or drain.
3. Sample tested.
4. Parameter tested at $T_A = 125^\circ\text{C}$ for military temperature range device.
5. Power supply and ground currents specified for switch "ON" or "OFF". The "OFF" state consumes highest power.
6. $TC_R = \frac{R_{ON@T_H} - R_{ON@25^\circ\text{C}}}{R_{ON@25^\circ\text{C}} \times (T_H - 25^\circ\text{C})} \times 100$; where $T_H = 125^\circ\text{C}$ for B grade
 $T_H = 85^\circ\text{C}$ for F grade
7. Switching is guaranteed to be break-before-make.
8. Guaranteed by leakage currents and R_{ON} tests. For normal operation analog signal voltages should be restricted to less than $(V+) - 4\text{V}$.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $-55^\circ C \leq T_A \leq +125^\circ C$ for SW-01/02B and $-25^\circ C \leq T_A \leq 85^\circ C$ for SW-01/02F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01/02B			SW-01/02F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V, I_D \leq 1mA$	—	—	120	—	—	140	Ω
R_{ON} Match		(Note 1)	—	10	15	—	10	15	%
R_{ON} Temperature Coefficient — Average	TC_R	$V_A = 0V, I_D = 100\mu A$, (Note 6)	—	0.03	0.20	—	0.03	0.15	%/ $^\circ C$
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$, (Note 4)	—	—	10	—	—	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$, (Note 4)	—	—	10	—	—	10	nA
Leakage Current in "ON" Condition	$I_{D(ON)}^+$ $I_{S(ON)}$	$V_S = \pm 10V$, (Notes 2, 4)	—	—	10	—	—	10	nA
Turn-On-Time	T_{ON}	Test Figure 1, (Note 3)	—	500	600	—	500	600	ns
Turn-Off-Time	T_{OFF}	Test Figure 1, (Note 3)	—	400	500	—	400	500	ns
Break-Before-Make Time	$T_{ON} - T_{OFF}$	Test Figure 1, (Notes 3, 7)	—	100	—	—	100	—	ns
Logic "1" Input Current	I_{INH}	$2 \leq V_{IN} \leq 15V$	—	1	5	—	1	5	μA
Logic "0" Input Current	I_{INL}	$0 \leq V_{IN} \leq 0.8V$	—	—	5	—	—	5	μA
Positive Supply Current	I^+	(Note 5)	—	—	11	—	—	12	mA
Negative Supply Current	I^-	(Note 5)	—	—	6	—	—	7	mA
Ground Current	I_G	(Note 5)	—	—	5	—	—	6	mA

NOTES:

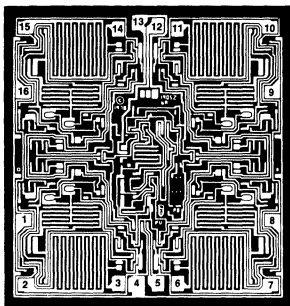
1. $V_A = 0V, I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

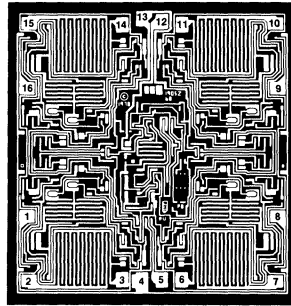
2. The conditions listed specify the worst case leakage current. The leakage currents apply equally to source or drain.
 3. Guaranteed by design.
 4. Parameter tested at $T_A = 125^\circ C$ for military temperature range device.
 5. Power supply and ground currents specified for switch "ON" or "OFF". The "OFF" state consumes highest power.
 6. $TC_R = \frac{R_{ON@T_H} - R_{ON@25^\circ C}}{R_{ON@25^\circ C} \times (T_H - 25^\circ C)} \times 100$; where $T_H = 125^\circ C$ for B grade
 $T_H = 85^\circ C$ for F grade
 7. Switching is guaranteed to be break-before-make.



DICE CHARACTERISTICS



SW-01



SW-02

DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils
(2.540 × 2.438 mm, 6.193 sq. mm)

- | | |
|-----------------------------|------------------------------|
| 1. SWITCH (1) ADDRESS (IN1) | 9. SWITCH (3) ADDRESS (IN3) |
| 2. SWITCH (1) DRAIN (D1) | 10. SWITCH (3) DRAIN (D3) |
| 3. SWITCH (1) SOURCE (S1) | 11. SWITCH (3) SOURCE (S3) |
| 4. NEGATIVE SUPPLY | 12. NO CONNECTION |
| 5. GROUND | 13. POSITIVE SUPPLY |
| 6. SWITCH (4) SOURCE (S4) | 14. SWITCH (2) SOURCE (S2) |
| 7. SWITCH (4) DRAIN (D4) | 15. SWITCH (2) DRAIN (D2) |
| 8. SWITCH (4) ADDRESS (IN4) | 16. SWITCH (2) ADDRESS (IN2) |

DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils
(2.540 × 2.438 mm, 6.193 sq. mm)

- | | |
|-----------------------------|------------------------------|
| 1. SWITCH (1) ADDRESS (IN1) | 9. SWITCH (3) ADDRESS (IN3) |
| 2. SWITCH (1) DRAIN (D1) | 10. SWITCH (3) DRAIN (D3) |
| 3. SWITCH (1) SOURCE (S1) | 11. SWITCH (3) SOURCE (S3) |
| 4. NEGATIVE SUPPLY | 12. NO CONNECTION |
| 5. GROUND | 13. POSITIVE SUPPLY |
| 6. SWITCH (4) SOURCE (S4) | 14. SWITCH (2) SOURCE (S2) |
| 7. SWITCH (4) DRAIN (D4) | 15. SWITCH (2) DRAIN (D2) |
| 8. SWITCH (4) ADDRESS (IN4) | 16. SWITCH (2) ADDRESS (IN2) |

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01/02N LIMIT	SW-01/02G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_D \leq 1mA$	100	120	Ω MAX
R_{ON} Match		$V_A = 0V$, $I_D \leq 100\mu A$	10	10	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$V_A \leq 10V$, $I_D \leq 1mA$	10	10	% MAX
Positive Supply Current	I_+	(Note 1)	8	9	mA MAX
Negative Supply Current	I_-	(Note 1)	4.5	5.5	mA MAX
Ground Current	I_G		4.0	4.5	mA MAX
Analog Voltage Range	V_A	(Note 2)	± 10	± 10	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 2)	2	2	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 2)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0 \leq V_{IN} \leq 0.8V$	3	3	μA MAX
Logic "1" Input Current	I_{INH}	$2 \leq V_{IN} \leq 15V$	3	3	μA MAX

NOTE:

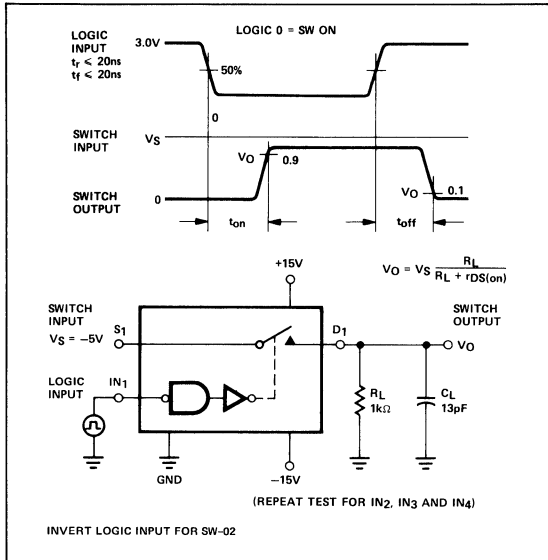
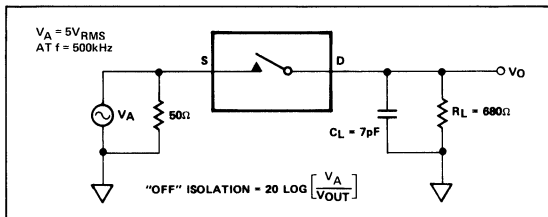
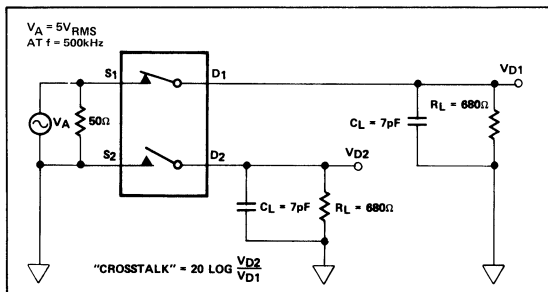
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01/02N TYPICAL	SW-01/02G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-55^\circ C \leq T_A \leq 125^\circ C$	90	90	Ω
R_{ON} Temperature Coefficient	TC_R	$V_A = 0$, $I_D = 100\mu A$	0.03	0.03	%/ $^\circ C$
Turn-On-Time	T_{ON}	$R_L = 1k$, $C_L = 13pF$	300	300	ns
Turn-Off-Time	T_{OFF}	$R_L = 1k$, $C_L = 13pF$	200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.2	0.2	nA
"OFF" Isolation	ISO_{OFF}	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

NOTES:

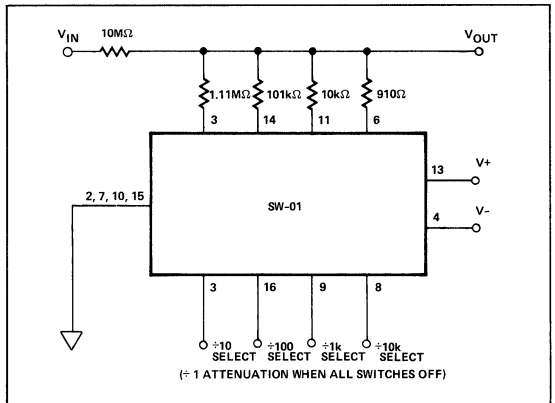
- Power supply and ground current specified for switch "ON" or "OFF".
- Guaranteed by R_{ON} and leakage current measurements.

TEST CIRCUITS

TEST FIGURE 1

TEST FIGURE 2

TEST FIGURE 3
APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P , and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

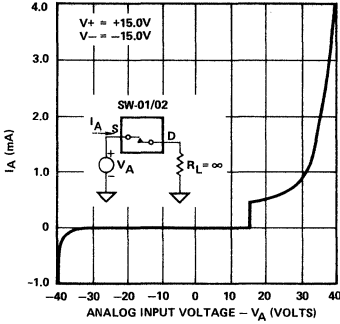
Proper switching requires the "Source" terminal to be connected to the input driving signal.

PROGRAMMABLE ATTENUATOR (1 to 0.0001)


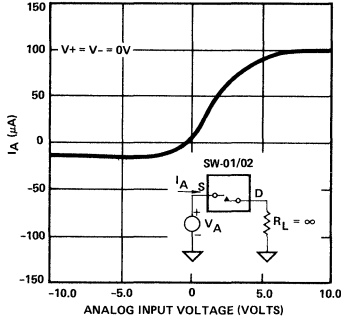


TYPICAL PERFORMANCE CHARACTERISTICS (SW-01/02)

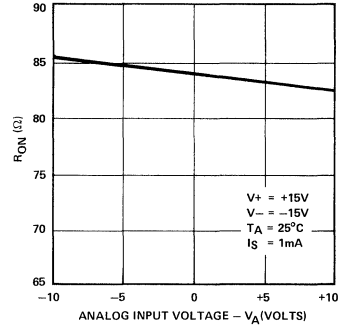
OVERVOLTAGE CHARACTERISTIC



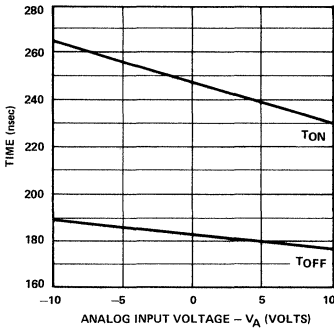
POWER SUPPLY LOSS CHARACTERISTIC



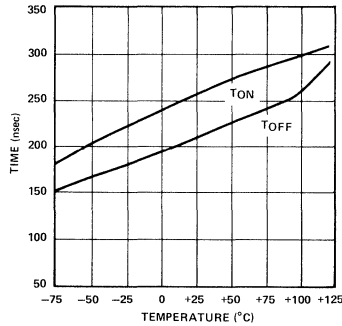
"ON" RESISTANCE vs ANALOG VOLTAGE (V_A)



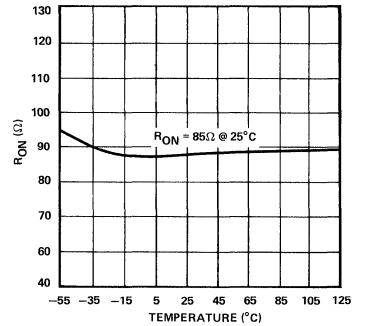
SWITCHING TIME vs ANALOG VOLTAGE



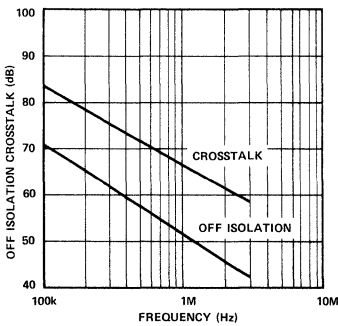
SWITCHING TIMES vs TEMPERATURE



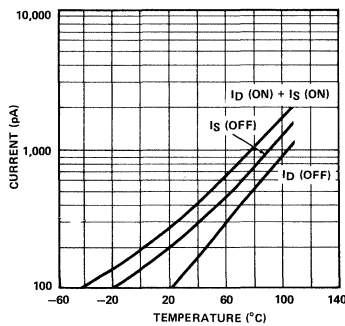
R_{ON} vs TEMPERATURE



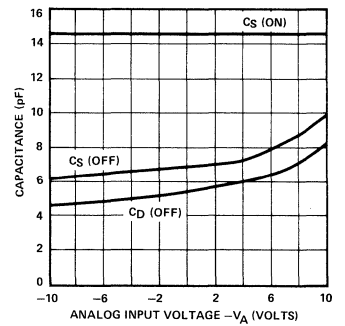
CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



LEAKAGE CURRENT vs TEMPERATURE



SWITCH CAPACITANCE vs ANALOG VOLTAGE





The SW-01/02 designs have been optimized for low "ON" resistance variation with temperature, signal voltage, and supply voltage changes. Fast switching response and low leakage currents at high temperature are also key performance improvements over older circuit designs.

The static-electricity-resistant JFET switches and additional overvoltage-protection circuitry make the precision switches extremely durable in most application environments.

The SW-01/02 are well suited to applications requiring analog currents <5mA with driving source impedances <100Ω. Applications using op amps, buffers or voltage sources as input drive sources are typical of those fulfilling these conditions. Within the given range of source impedance

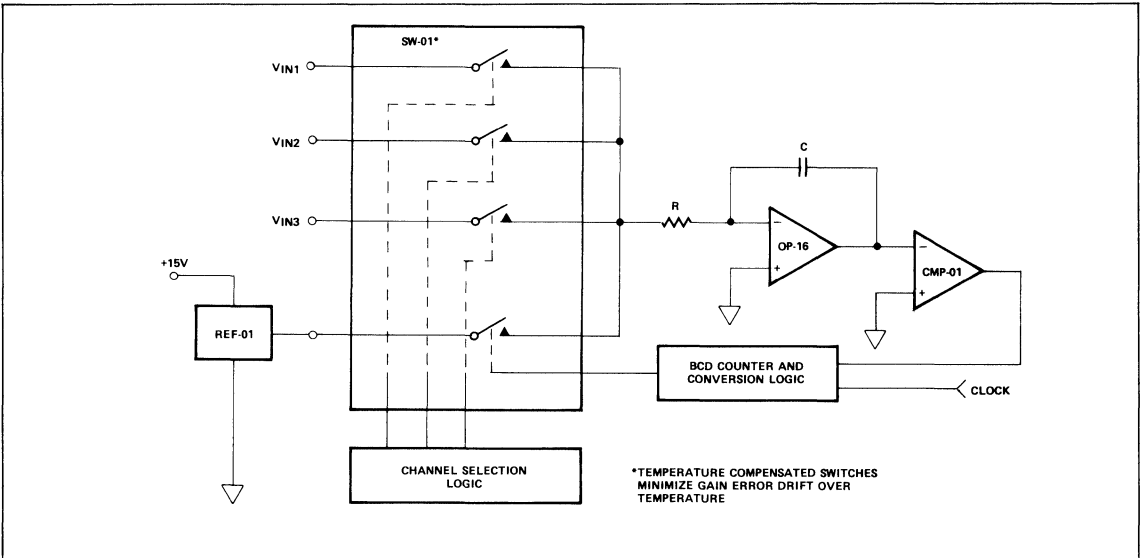
and analog current near ideal signal transfer accuracy is obtainable.

Applications needing very high analog current capability (>5mA) or where the switch is driven from high source impedances (>100Ω) should use the SW-201 (Pin Compatible to SW-01) or the SW-202 (Pin Compatible to SW-02) high-current quad switches.

Although the SW-201/202 do not offer the same "ON" resistance temperature coefficient, many other premium characteristics are similar. In addition, the SW-201/202 offer exceptionally low signal distortion over a wide signal voltage and frequency range.

TYPICAL APPLICATIONS

DUAL SLOPE A/D CONVERSION





SW-05

DUAL SPST JFET ANALOG SWITCH

Precision Monolithics Inc.

FEATURES

- Low "ON" Resistance 25°C 70Ω Max
125°C 100Ω Max
- Accurate Switching ($I_{D(ON)} \times R_{ON}$ @ 125°C)
ERROR Worst Case 10μV
- Low R_{ON} Variation With Analog Input Voltage 5%
- Improved Switching Speed $T_{ON} = 450ns$ Max
 $T_{OFF} = 400ns$ Max
- Resistant to Static Discharge Damage
- Higher Resistance to Radiation Than Analog Switches
Designed With MOS Devices.
- Latch Proof
- Digital Inputs TTL and CMOS Compatible
- Dual or Single Power Supply Operation
- Pin Compatible With DG200, IH200, HI200, ADG200

GENERAL DESCRIPTION

The monolithic SW-05 provides two independently selectable single-pole-single-throw (SPST) analog switches. The units are

ORDERING INFORMATION†

PLASTIC	HERMETIC PACKAGE		OPERATING TEMPERATURE RANGE
14-PIN DIP	TO-100 10-PIN	14-PIN DIP	
—	SW05BK*	SW05BY*	MIL
—	SW05FK	SW05FY	IND
SW05GP	—	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

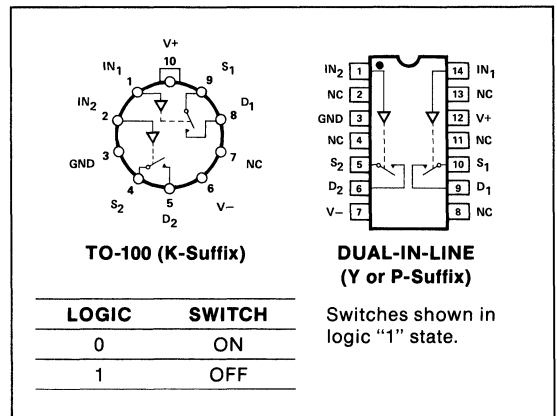
† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

fabricated with Precision Monolithics' ion-implant JFET-bipolar technology. The JFET switch structure parametrically improves R_{ON} variation with input voltages, total harmonic distortion, lowers noise, and reduces susceptibility to power supply feed-through when compared to the CMOS switch technology.

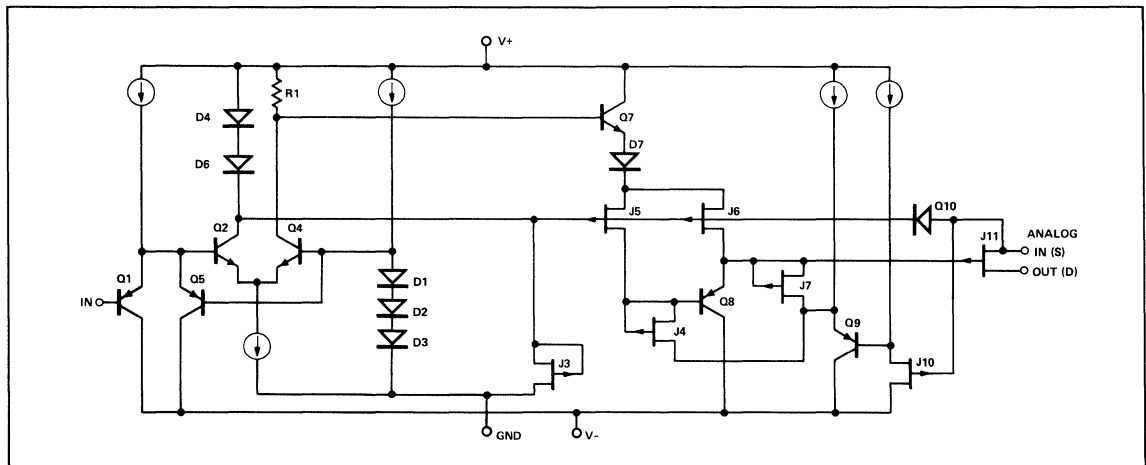
The JFET-bipolar process inherently reduces susceptibility to electrostatic voltage destruction commonly experienced in the CMOS process technology. Additionally, the elimination of MOS devices results in a circuit less susceptible to radiation.

An internal logic reference voltage maintains logic compatibility with full noise immunity over full temperature range and all variations of power supply voltage.

PIN CONNECTIONS



SCHEMATIC DIAGRAM (Typical Switch)



Manufactured under one or more of the following patents: 4,228,367.

**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Operating Temperature Range	Lead Temperature (Soldering, 60 sec)	300°C
SW05BY, SW05BK	Maximum Junction Temperature	150°C
SW05FY, SW05FK	V+ Supply to V- Supply	36V
SW05GP	V+ Supply to Ground	36V
Storage Temperature Range	Logic Input Voltage	(-4V or V-) to V+ Supply
Power Dissipation	Analog Input Voltage Range	
K, Y Packages	Continuous	V- Supply to V+ Supply +20V
P Package	Maximum Current Through any Pin	30mA
Derate K, Y Package by 12mW/°C Above 75°C	Switch Current 1ms, 10% Duty Cycle Max.	100mA
Derate P Package by 10mW/°C Above 25°C		

ELECTRICAL CHARACTERISTICS at $V+ = 15\text{V}$, $V- = -15\text{V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-05B			SW-05F			SW-05G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S = 0\text{V}$, $I_S = 1\text{mA}$ $V_S = \pm 10\text{V}$, $I_S = 1\text{mA}$	—	45	70	—	45	80	—	45	80	Ω
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0\text{V}$, $I_S = 100\mu\text{A}$ (Note 1)	—	5	10	—	—	10	—	—	15	%
Analog Voltage Range	V_A	$I_S = 1\text{mA}$ (Note 4)	10	11	—	10	11	—	10	11	—	V
Analog Current Range	I_A	$V_S = \pm 10\text{V}$	10	15	—	8	12	—	6	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	$-10\text{V} \leq V_S \leq 10\text{V}$, $I_S = 1\text{mA}$	—	5	10	—	—	10	—	—	15	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$, $V_{IN} = 2\text{V}$	—	—	2	—	—	3	—	—	5	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$, $V_{IN} = 2\text{V}$	—	—	2	—	—	3	—	—	5	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10\text{V}$, $V_{IN} = 0.8\text{V}$	—	—	2	—	—	3	—	—	5	nA
Logical "1" Input Voltage	V_{INH}	Full Temp. Range (Note 4)	2	—	—	2	—	—	2	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temp. Range (Note 4)	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	$V_{IN} = 2$ to 15V (Note 3)	—	—	5	—	—	5	—	—	10	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8\text{V}$	—	1.5	5	—	1.5	5	—	1.5	10	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Note 2)	—	325	450	—	325	450	—	325	450	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Note 2)	—	310	400	—	310	400	—	310	400	ns
Source Capacitance	$C_{S(OFF)}$	$V_S = 0\text{V}$, $V_{IN} = 2\text{V}$	—	8	—	—	8	—	—	8	—	pF
Drain Capacitance	$C_{D(OFF)}$	$V_D = 0\text{V}$, $V_{IN} = 2\text{V}$	—	5	—	—	5	—	—	5	—	pF
Channel "ON" Capacitance	$C_{D(ON)} + C_{S(ON)}$	$V_S = V_D = 0\text{V}$	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	$V_S = 5V_{RMS}$, $R_L = 680\Omega$, $C_L = 7\text{pF}$, $f = 500\text{kHz}$	—	62	—	—	62	—	—	62	—	dB
Crosstalk	C_T	$V_S = 5V_{RMS}$, $R_L = 680\Omega$, $C_L = 7\text{pF}$, $f = 500\text{kHz}$	—	76	—	—	76	—	—	76	—	dB
Positive Supply Current	$I+$	$V_{IN} = 0.8$ or 2V	—	2.6	6	—	3	6	—	4	8	mA
Negative Supply Current	$I-$	$V_{IN} = 0.8$ or 2V	—	1.5	3	—	2	3	—	3	4	mA

NOTES:

1. $V_S = 0\text{V}$, $I_D = 100\mu\text{A}$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2}}{2}$$

- Sample tested.
- Current tested at $V_{IN} = 2.0\text{V}$. This is worst case condition.
- Guaranteed by R_{ON} and leakage tests.

ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for SW-05BY and SW-05BK; $-25^\circ C \leq T_A \leq +85^\circ C$ for SW-05FY and SW-05FK; $0^\circ C \leq T_A \leq 70^\circ C$ for SW-05GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-05B			SW-05F			SW-05G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Temperature Range	T_A	Operating	-55	—	125	-25	—	85	0	—	70	$^\circ C$
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 1mA$	—	—	100	—	—	100	—	—	100	Ω
		$V_S = \pm 10V$, $I_S = 1mA$	—	—	100	—	—	100	—	—	100	
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 100\mu A$ (Note 1)	—	10	15	—	—	15	—	—	20	%
Analog Voltage Range	V_A	$I_S = 1mA$	10	—	—	10	—	—	10	—	—	V
		$I_S = 1mA$ (Note 5)	-10	—	—	-10	—	—	-10	—	—	
Analog Current Range	I_A	$V_S = \pm 10V$	10	—	—	8	—	—	6	—	—	mA
ΔR_{ON} with Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq +10V$, $I_S = 1mA$	—	—	10	—	—	10	—	—	15	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, $V_{IN} = 2V$, $T_A = \text{Max}$. Operating Temp. (Note 4)	—	—	50	—	—	50	—	—	50	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, $V_{IN} = 2V$, $T_A = \text{Max}$. Operating Temp. (Note 4)	—	—	50	—	—	50	—	—	50	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10V$, $V_{IN} = 0.8V$, $T_A = \text{Max}$. Operating Temp. (Note 4)	—	—	100	—	—	100	—	—	100	nA
Logical "1" Input Current	I_{INH}	$V_{IN} = 2V$ to $15V$ (Note 3)	—	—	10	—	—	10	—	—	15	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8V$	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Note 2)	—	—	600	—	—	600	—	—	600	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Note 2)	—	—	500	—	—	500	—	—	500	ns
Positive Supply Current	I_+	$V_{IN} = 0$ or $2V$	—	—	8	—	—	8	—	—	10	mA
Negative Supply Current	I_-	$V_{IN} = 0$ or $2V$	—	—	4.5	—	—	4.5	—	—	5	mA

NOTES:

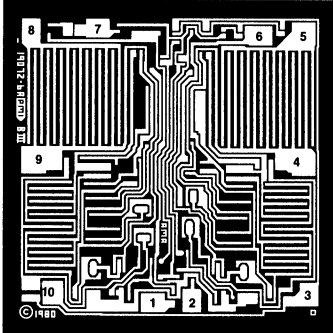
- $V_S = 0V$, $I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2}}{2}$$

- Parameter guaranteed by design.
- Current tested at $V_{IN} = 2V$. This is worst case condition.
- Parameter tested only at $T_A = 125^\circ C$ for military grade device.
- Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltages should be restricted to $(V_+) - 4V$.



DICE CHARACTERISTICS



DIE SIZE 0.067 × 0.067 inch, 4489 sq mils
(1.702 × 1.702 mm, 2.896 sq. mm)

- | | |
|--------|-------------------|
| 1. IN1 | 6. V- (SUBSTRATE) |
| 2. IN2 | 7. NC |
| 3. GND | 8. D1 |
| 4. S2 | 9. S1 |
| 5. D2 | 10. V+ |

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-05N LIMIT	SW-05G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	70	80	Ω MAX
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_S \leq 100\mu A$	10	10	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	10	10	% MAX
Positive Supply	I+	(Note 1)	6	6	mA MAX
Negative Supply Current	I-	(Note 1)	3	3	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$	± 10	± 10	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 3)	2	2	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 3)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \leq V_{IN} \leq 0.8V$	5	5	μA MAX
Logic "1" Input Current	I_{INH}	$2V \leq V_{IN} \leq 15V$ (Note 2)	5	5	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	8	mA MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-05N TYPICAL	SW-05G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	45	45	Ω
Turn-On-Time	t_{ON}		325	325	ns
Turn-Off-Time	t_{OFF}		310	310	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
Leakage Current in "ON" Condition	$I_{S(ON)}$ + $I_{D(ON)}$	$V_S = V_D = \pm 10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	62	62	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	76	76	dB

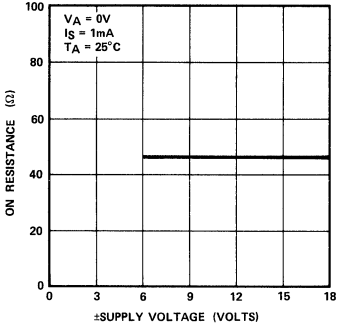
NOTES:

- Power supply and ground current specified for switch "ON" or "OFF".
- Current tested at $V_{IN} = 2V$. This is worst case condition.
- Guaranteed by R_{ON} and leakage tests.

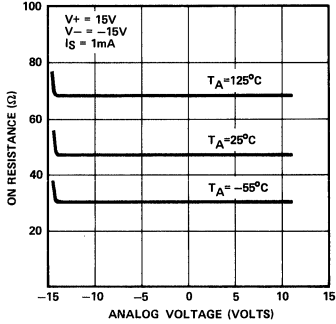


TYPICAL PERFORMANCE CHARACTERISTICS

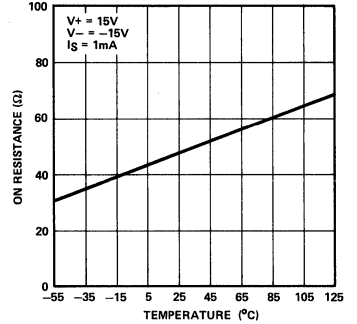
"ON" RESISTANCE vs POWER SUPPLY VOLTAGE



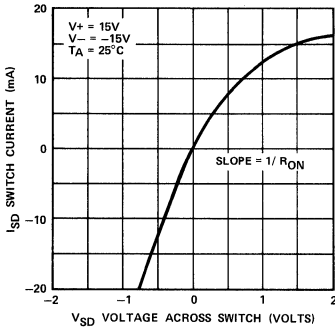
"ON" RESISTANCE vs ANALOG VOLTAGE (V_A)



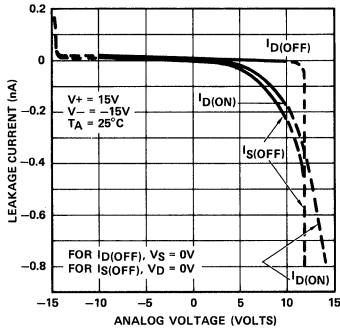
"ON" RESISTANCE vs TEMPERATURE



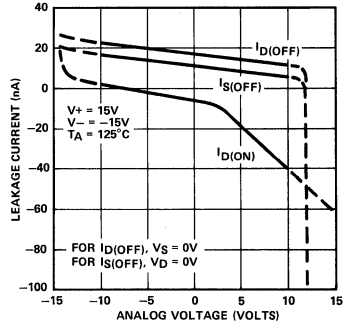
SWITCH CURRENT vs VOLTAGE



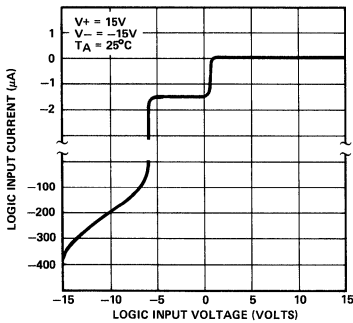
LEAKAGE CURRENT vs ANALOG VOLTAGE



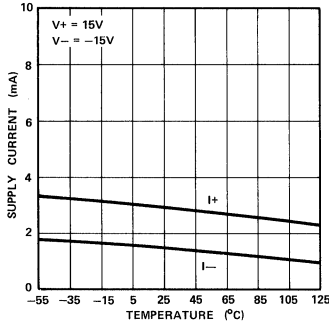
LEAKAGE CURRENT AT 125°C vs ANALOG VOLTAGE



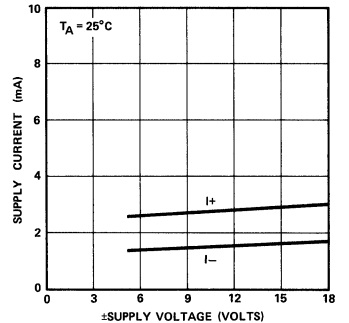
LOGIC INPUT CURRENT vs VOLTAGE



SUPPLY CURRENT vs TEMPERATURE

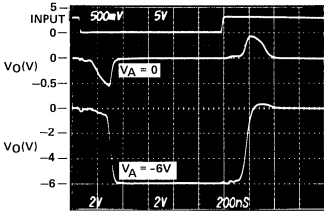


SUPPLY CURRENT vs SUPPLY VOLTAGE



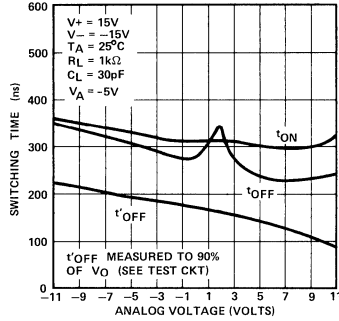
TYPICAL PERFORMANCE CHARACTERISTICS

SWITCHING RESPONSE

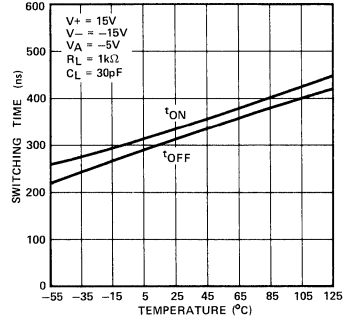


(SEE SWITCHING TIME TEST CIRCUIT)

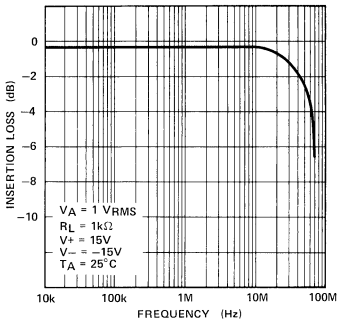
SWITCHING TIME vs ANALOG VOLTAGE



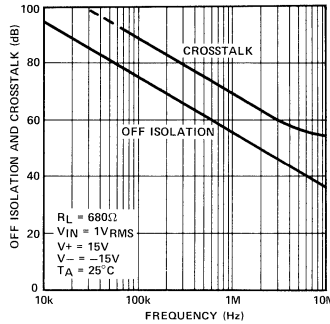
SWITCHING TIME vs TEMPERATURE



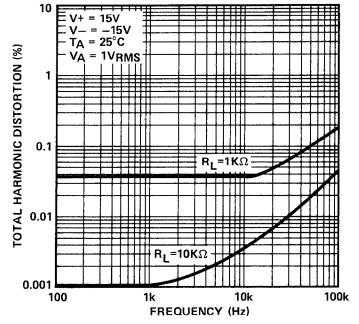
INSERTION LOSS vs FREQUENCY



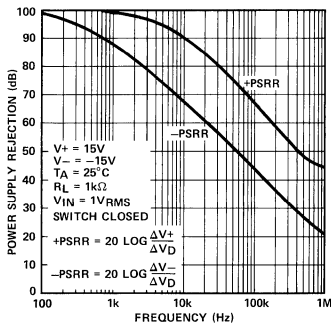
OFF ISOLATION AND CROSSTALK vs FREQUENCY



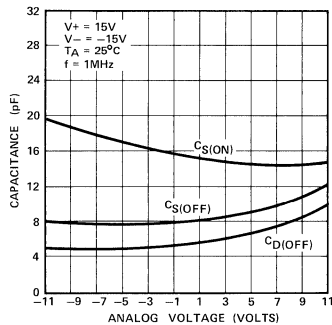
DISTORTION vs FREQUENCY



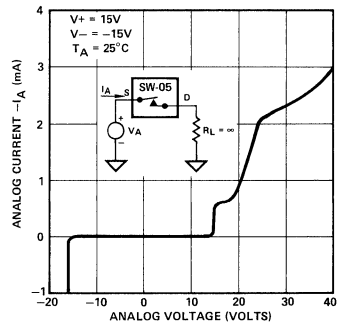
POWER SUPPLY REJECTION vs FREQUENCY

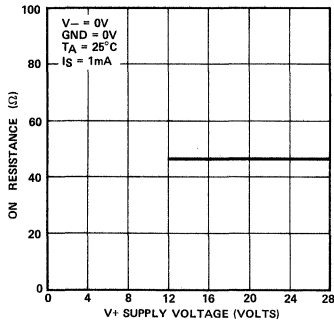
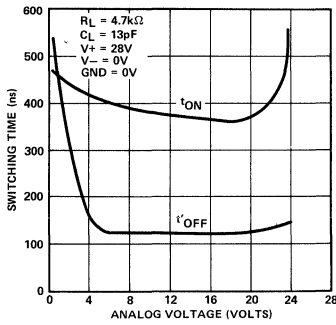
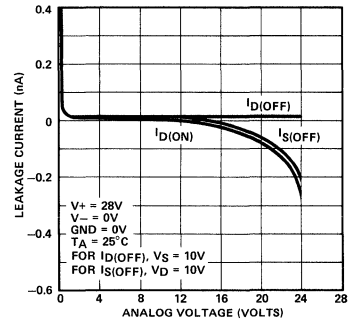
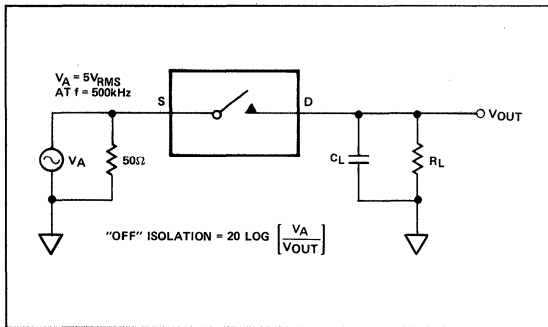
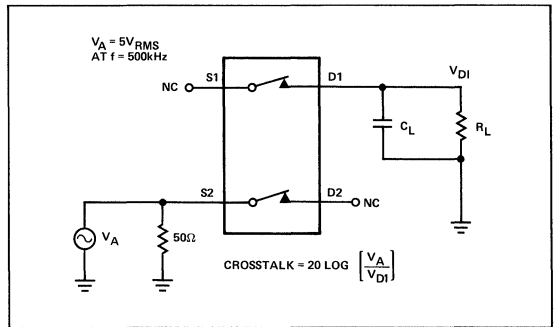
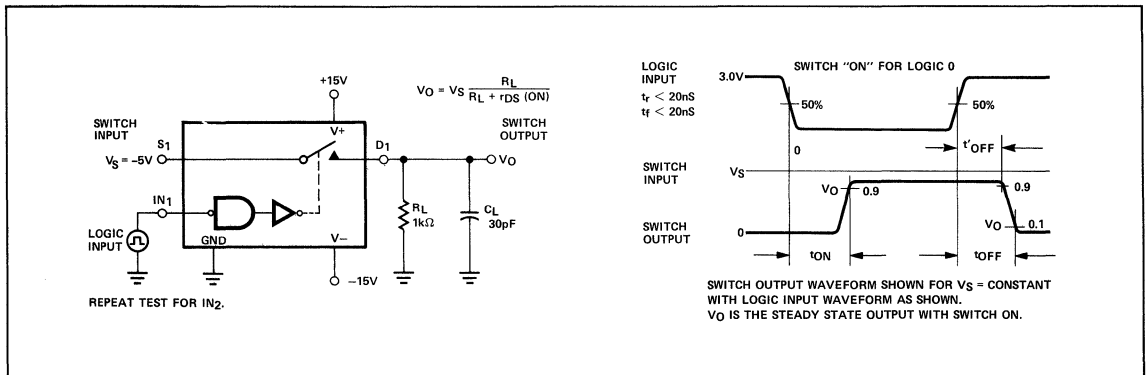


CAPACITANCE vs ANALOG VOLTAGE



OVERVOLTAGE CHARACTERISTIC



TYPICAL PERFORMANCE CHARACTERISTICS (Single Supply Operation)
"ON" RESISTANCE vs SUPPLY VOLTAGE

SWITCHING TIME vs ANALOG VOLTAGE

LEAKAGE CURRENT vs ANALOG VOLTAGE

TEST CIRCUITS
OFF ISOLATION TEST CIRCUIT

CROSSTALK TEST CIRCUIT

SWITCHING TIME TEST CIRCUIT


APPLICATIONS INFORMATION

The SW-05 provides a rugged JFET alternative to the industry standard CMOS generic DG200 device. The basic differences in process (CMOS vs Bipolar-JFET) effecting switch characteristics result from the parallel connected enhancement mode FETs used in CMOS versus the single depletion mode JFET used by the Bipolar-JFET process. The junction technology is far less susceptible to electrostatic damage (ESD), and offers a higher resistance to radiation exposure. No extensive threshold shifts take place as commonly found in CMOS.

The basic JFET switch design inherently results in a more linear "ON" resistance over the designed analog signal range of -15 to +11 volts. The "ON" resistance is independent of analog voltage and supply voltage, but does have a positive temperature coefficient of 0.4%/°C. Leakage currents stay in the low picoamps at room temperature providing very high "OFF" resistance characteristics.

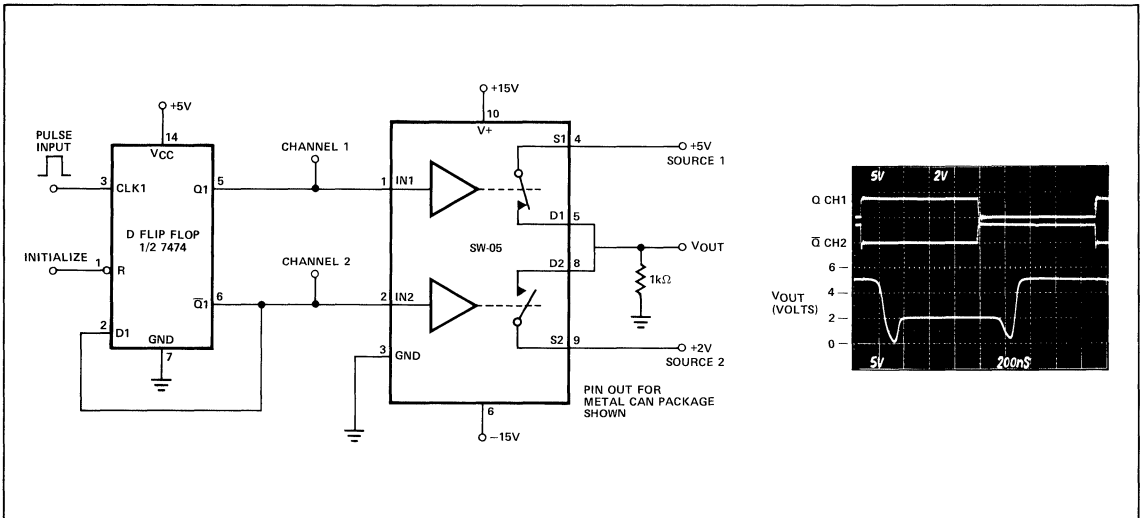
The logic control inputs are TTL input compatible with full 400mV noise immunity over the full operating temperature range. The PNP input structure requires very little logic drive current resulting in minimum output loading to both TTL and

CMOS logic. Since the SW-05 incorporates a standard two forward diode drop logic voltage reference, pin 7 in the metal can and pin 12 in the DIP package were left unconnected. This allows direct plug-in compatibility with DG200's requiring external logic threshold adjustment to their V_{REF} pin when operating from supplies other than ± 15 volts. No logic threshold adjustment is necessary with the SW-05 operating, for example, at ± 12 volts.

The addition of a 7474 latch in front of the SW-05 (Figure 1) results in a pulse input latching SPDT analog switch. A positive edge of an input pulse to the TTL D type flip flop causes the Q and \bar{Q} outputs to change state. Taking advantage of the complementary outputs turns the SW-05 into a break-before-make SPDT analog switch. The short dead time between switch closures prevents damaging current flowing between the two low impedance sources. The photograph illustrates the dead time when V_{OUT} is pulled to ground by the 1k ohm termination resistor.

The initialize input, connected to the D flip flop reset (clear) input, resets Q_1 sending an active low to the IN_1 terminal of the SW-05 closing switch 1.

FIGURE 1: Pulse Input Latching SPDT Analog Switch

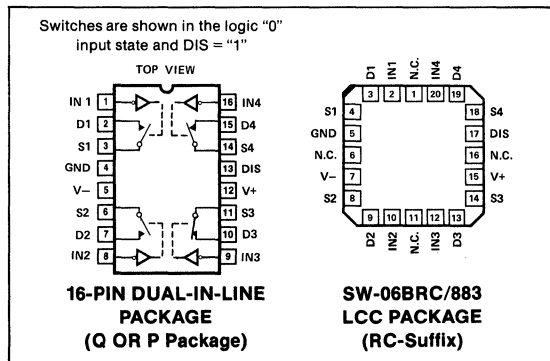


Precision Monolithics Inc.

FEATURES

- Two Normally Open and Two Normally Closed SPST Switches with Disable
- Switches can be Easily Configured as a Dual SPDT or a DPDT
- Highly Resistant to Static Discharge Destruction
- Higher Resistance to Radiation Than Analog Switches Designed with MOS Devices
- Guaranteed R_{ON} Matching 10% Max
- Guaranteed Switching Speeds $T_{ON} = 500ns$ Max
 $T_{OFF} = 400ns$ Max
- Guaranteed Break-Before-Make Switching
- Low "ON" Resistance 80Ω Max
- Low R_{ON} Variation from Analog Input Voltage 5%
- Low Total Harmonic Distortion 0.01%
- Low Leakage Currents at High Temperature:
 $T_A = 125^\circ C$ 100nA Max
 $T_A = 85^\circ C$ 30nA Max
- Digital Inputs TTL/CMOS Compatible and Independent of $V+$
- Improved Specifications and Pin Compatible to LF-11333/13333
- Dual or Single Power Supply Operation

PIN CONNECTIONS



ORDERING INFORMATION†

PACKAGE IS	ORDER PART NUMBER	LCC	OPERATING TEMPERATURE RANGE
HERMETIC	SW06BQ*	SW06BRC/883	MIL
	SW06FQ		IND
EPOXY	SW06GQ		COM
	SW06GP		COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

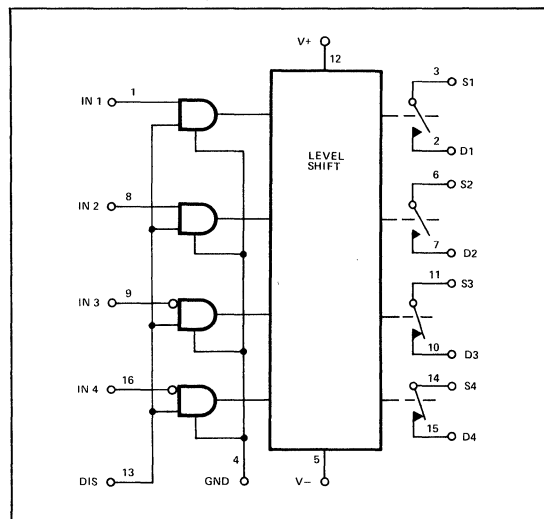
GENERAL DESCRIPTION

The SW-06 is a four channel single-pole, single-throw analog switch that employs both bipolar and ion-implanted FET devices. The SW-06 FET switches use bipolar digital logic inputs which are more resistant to static electricity than CMOS devices. Ruggedness and reliability are inherent in the SW-06 design and construction technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With $V+ = 36V$, $V- = 0V$, the analog signal range will extend from ground to +32V.

PNP logic inputs are TTL and CMOS compatible to allow the SW-06 to upgrade existing designs. The logic "0" and logic "1" input currents are at micro-ampere levels reducing loading on CMOS and TTL logic.

FUNCTIONAL DIAGRAM



TRUTH TABLE

DISABLE INPUT	LOGIC INPUT	SWITCH STATE	
		CHANNELS 1 & 2	CHANNELS 3 & 4
0	X	OFF	OFF
1 or NC	0	OFF	ON
1 or NC	1	ON	OFF

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Operating Temperature Range		
SW-06BQ, BRC	-55°C to +125°C
SW-06FQ	-25°C to +85°C
SW-06GP	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation (Note 2)		
Q Package	900mW
P Package	500mW
Lead Temperature (Soldering 60 sec)	300°C
Maximum Junction Temperature	150°C

V+ Supply to V- Supply	36V
V+ Supply to Ground	36V
Logic Input Voltage	(-4V or V-) to V+ Supply
Analogue Input Voltage Range		
Continuous	V- Supply to V+ Supply +20V
Maximum Current Through Any Pin Including Switch	30mA

NOTES:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Q Package derated 12mW/°C above 75°C, P Package derated 10mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V- = -15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06B			SW-06F			SW-06G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R _{ON}	V _S = 0V, I _S = 1mA V _S = ±10V, I _S = 1mA	—	60	80	—	60	100	—	100	150	Ω
R _{ON} Match Between Switches	R _{ON} Match	V _S = 0V, I _S = 100μA (Note 1)	—	5	10	—	5	20	—	—	20	%
Analogue Voltage Range	V _A	I _S = 1mA (Note 8) I _S = 1mA	+10	+11	—	+10	+11	—	+10	+11	—	V
Analogue Current Range	I _A	V _S = ±10V	10	15	—	7	12	—	5	10	—	mA
ΔR _{ON} vs Applied Voltage	ΔR _{ON}	-10V ≤ V _S ≤ 10V, I _S = 1.0mA	—	5	15	—	10	20	—	10	20	%
Source Current in "OFF" Condition	I _{S(OFF)}	V _S = 10V, V _D = -10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Drain Current in "OFF" Condition	I _{D(OFF)}	V _S = 10V, V _D = -10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Source Current in "ON" Condition	I _{S(ON)+} I _{D(ON)}	V _S = V _D = ±10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Logical "1" Input Voltage	V _{INH}	Full Temperature Range (Notes 6, 8)	2.0	—	—	2.0	—	—	2.0	—	—	V
Logical "0" Input Voltage	V _{INL}	Full Temperature Range (Notes 6, 8)	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I _{INH}	V _{IN} = 2.0V to 15.0V (Note 4)	—	—	5	—	—	5	—	—	10	μA
Logical "0" Input	I _{INL}	V _{IN} = 0.8V	—	1.5	5.0	—	1.5	5.0	—	1.5	10.0	μA
Turn-On-Time	t _{ON}	See Switching Time Test Circuit (Notes 6, 9)	—	340	500	—	340	600	—	340	700	ns
Turn-Off-Time	t _{OFF}	See Switching Time Test Circuit (Notes 6, 9)	—	200	400	—	200	400	—	200	500	ns
Break-Before-Make Time	t _{ON} -t _{OFF}	(Note 9)	50	140	—	50	140	—	50	140	—	ns
Source Capacitance	C _{S(OFF)}	V _S = 0V (Note 5)	—	7.0	—	—	7.0	—	—	7.0	—	pF
Drain Capacitance	C _{D(OFF)}	V _S = 0V (Note 5)	—	5.5	—	—	5.5	—	—	5.5	—	pF
Channel "ON" Capacitance	C _{D(ON)+} C _{S(ON)}	V _S = V _D = 0V (Note 5)	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	I _{SO(OFF)}	V _S = 5V _{RMS} , R _L = 680Ω, C _L = 7pF, f = 500kHz (Note 5)	—	58	—	—	58	—	—	58	—	dB
Crosstalk	C _T	V _S = 5V _{RMS} , R _L = 680Ω, C _L = 7pF, f = 500kHz (Note 5)	—	70	—	—	70	—	—	70	—	dB
Positive Supply Current	I+	All Channels "OFF", DIS = "1" (Note 5)	—	5.0	6.0	—	5.0	9.0	—	6.0	9.0	mA
Negative Supply Current	I-	All Channels "OFF", DIS = "0" (Note 5)	—	3.0	5.0	—	4.0	7.0	—	4.0	7.0	mA
Ground Current	I _G	All Channels "ON" or "OFF" (Note 5)	—	3.0	4.0	—	3.0	4.0	—	3.0	5.0	mA



ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for SW-06BQ, $-25^\circ C \leq T_A \leq +85^\circ C$ for SW-06FQ and $0^\circ C \leq T_A \leq 70^\circ C$ for SW-06GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06B			SW-06F			SW-06G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Temperature Range	T_A	Operating	-55	—	125	-25	—	85	0	—	70	$^\circ C$
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 1.0mA$	—	75	110	—	75	125	—	75	175	Ω
		$V_S = \pm 10V$, $I_S = 1.0mA$	—	80	110	—	80	125	—	80	175	
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 100\mu A$ (Note 1)	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	$I_S = 1.0mA$ (Note 8)	+10	+11	—	+10	+11	—	+10	+11	—	V
		$I_S = 1.0mA$	-10	-15	—	-10	-15	—	-10	-15	—	
Analog Current Range	I_A	$V_S = \pm 10.0V$	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq +10V$, $I_S = 1.0mA$	—	10	—	—	12	—	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, $T_A = \text{Max. Operating Temp.}$ (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, $T_A = \text{Max. Operating Temp.}$ (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)+}$	$V_S = V_D = \pm 10V$, $T_A = \text{Max. Operating Temp.}$ (Notes 5, 7)	—	—	100	—	—	30	—	—	60	nA
	$I_{D(ON)}$											
Logical "1" Input Current	I_{INH}	$V_{IN} = 2.0V$ to $15.0V$ (Note 4)	—	—	10	—	—	10	—	—	15	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8V$	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Notes 2, 6)	—	440	900	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Notes 2, 6)	—	300	500	—	330	500	—	—	500	ns
Break-Before-Make Time	$t_{ON}-t_{OFF}$	(Note 3)	—	70	—	—	70	—	—	50	—	ns
Positive Supply Current	I_+	All Channels "OFF" (Note 5)	—	—	9.0	—	—	13.5	—	—	13.5	mA
Negative Supply Current	I_-	All Channels "OFF" (Note 5)	—	—	7.5	—	—	10.5	—	—	10.5	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	—	—	6.0	—	—	7.5	—	—	7.5	mA

NOTES:

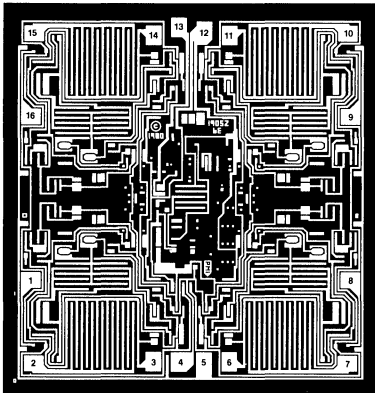
1. $V_S = 0V$, $I_S = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

- Guaranteed by design.
- Switch is guaranteed to provide break-before-make operation.
- Current tested at $V_{IN} = 2.0V$. This is worst case condition.
- Switch being tested ON or OFF as indicated, $V_{INH} = 2.0V$ or $V_{INL} = 0.8V$, per logic truth table.
- Also applies to disable pin.
- Parameter tested only at $T_A = +125^\circ C$ for military grade device.
- Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltages should be restricted to less than $(V_+) - 4V$.
- Sample tested.



DICE CHARACTERISTICS



DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils
(2.540 × 2.438 mm, 6.193 sq. mm)

1. IN (1)
2. D (1)
3. S (1)
4. GND
5. V- (SUBSTRATE)
6. S (2)
7. D (2)
8. IN (2)
9. IN (3)
10. D (3)
11. S (3)
12. V+
13. DISABLE
14. S (4)
15. D (4)
16. IN (4)

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 15V$, $V_- = -15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06N LIMIT	SW-06G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	80	100	Ω MAX
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_S \leq 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	10	20	% MAX
Positive Supply Current	I+	(Note 1)	6.0	9.0	mA MAX
Negative Supply Current	I-	(Note 1)	5.0	7.0	mA MAX
Ground Current	I_G	(Note 1)	4.0	4.0	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$	± 10.0	± 10.0	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 3)	2.0	2.0	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 3)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \leq V_{IN} \leq 0.8V$	5.0	5.0	μA MAX
Logic "1" Input Current	I_{INH}	$2.0V \leq V_{IN} \leq 15V$ (Note 2)	5	5	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06N TYPICAL	SW-06G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

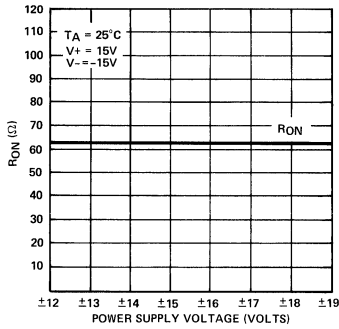
NOTES:

1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at $V_{IN} = 2.0V$. This is worst case condition.
3. Guaranteed by R_{ON} and leakage tests.

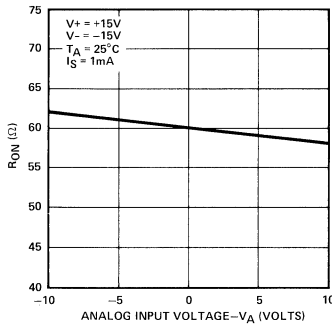


TYPICAL PERFORMANCE CHARACTERISTICS

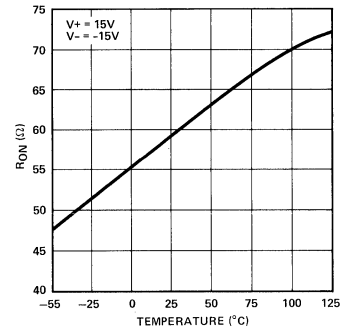
"ON" RESISTANCE vs POWER SUPPLY VOLTAGE



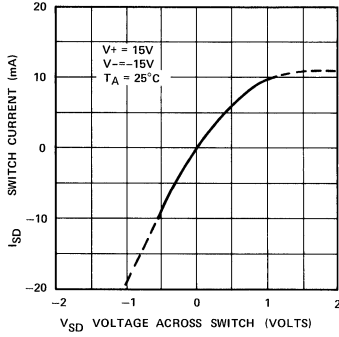
"ON" RESISTANCE vs ANALOG VOLTAGE



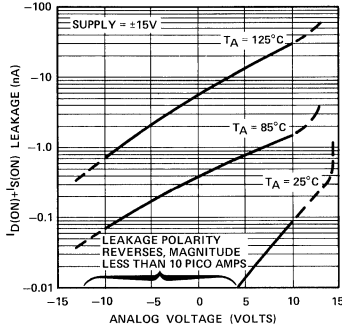
R_ON vs TEMPERATURE



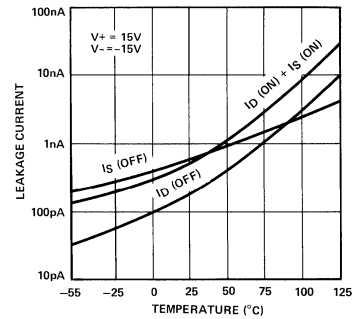
SWITCH CURRENT vs VOLTAGE



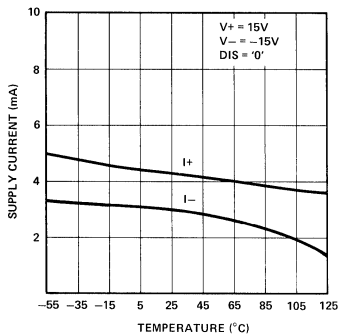
LEAKAGE CURRENT vs ANALOG VOLTAGE



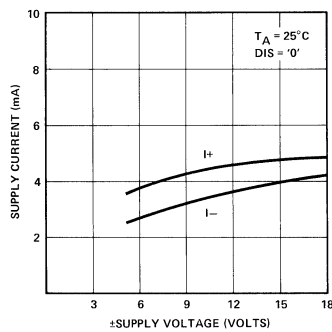
LEAKAGE CURRENT vs TEMPERATURE



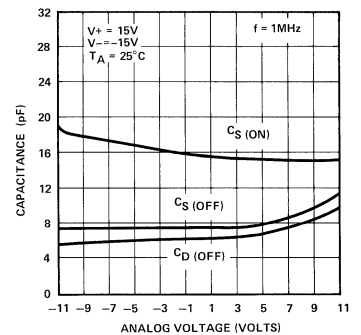
SUPPLY CURRENT vs TEMPERATURE



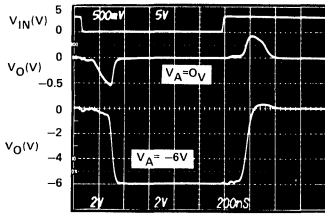
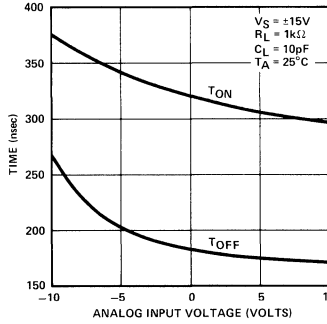
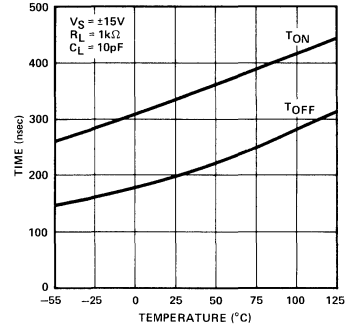
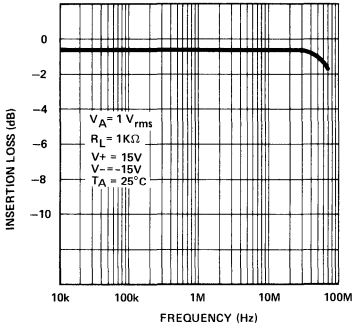
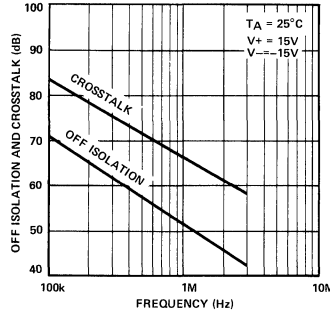
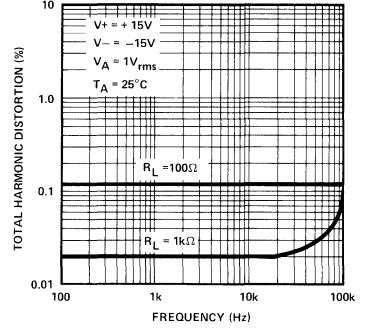
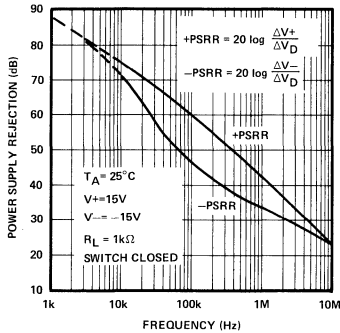
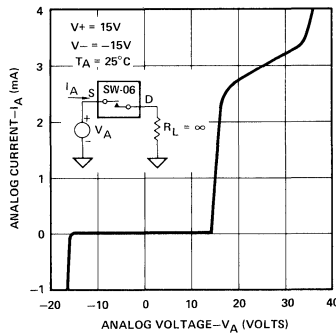
SUPPLY CURRENT vs SUPPLY VOLTAGE



SWITCH CAPACITANCE vs ANALOG VOLTAGE

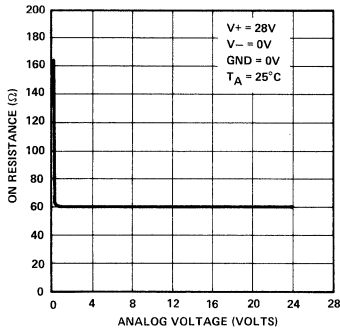


TYPICAL PERFORMANCE CHARACTERISTICS

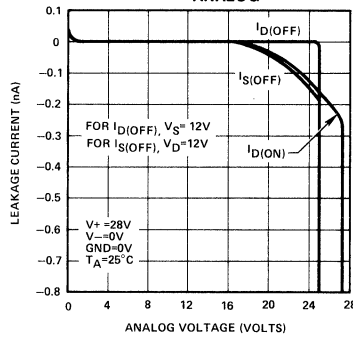
 **T_{ON}/T_{OFF}
SWITCHING RESPONSE**

**SWITCHING TIME
vs ANALOG VOLTAGE**

**SWITCHING TIME
vs TEMPERATURE**

**INSERTION LOSS
vs FREQUENCY**

**CROSSTALK AND "OFF"
ISOLATION vs FREQUENCY**

**TOTAL HARMONIC
DISTORTION**

**POWER SUPPLY REJECTION
vs FREQUENCY**

**OVERVOLTAGE
CHARACTERISTICS**


TYPICAL PERFORMANCE CHARACTERISTICS (OPERATING SINGLE SUPPLY)

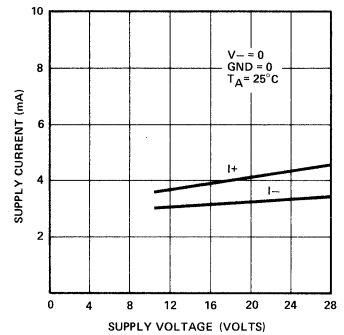
"ON" RESISTANCE vs ANALOG VOLTAGE



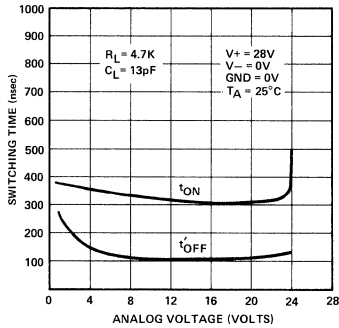
LEAKAGE CURRENT vs V_{ANALOG}



SUPPLY CURRENT vs SUPPLY VOLTAGE

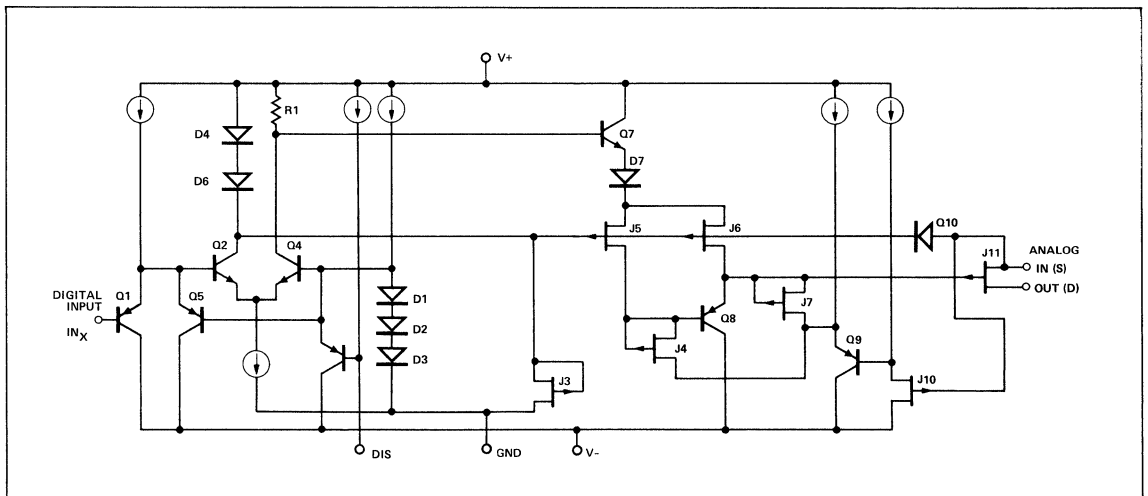


SWITCHING TIME vs SUPPLY VOLTAGE



NOTE: These single-supply-operation characteristic curves are valid when the negative power supply V_{-} is tied to the logic ground reference pin "GND". TTL input compatibility is still maintained when "GND" is the same potential as the TTL ground. t_{OFF} is measured from 50% of logic input waveform to 0.9 V_O . The analog voltage range extends from 0 to $V_{+} - 4V$, the switch will no longer respond to logic control when V_A is within 4 volts of V_{+} .

SIMPLIFIED SCHEMATIC DIAGRAM (TYPICAL SWITCH)



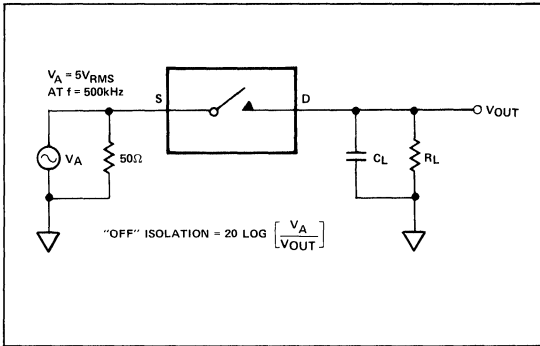
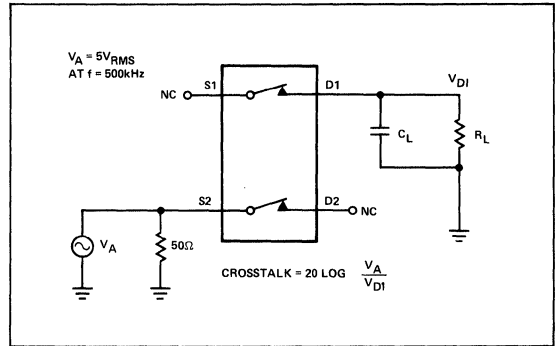
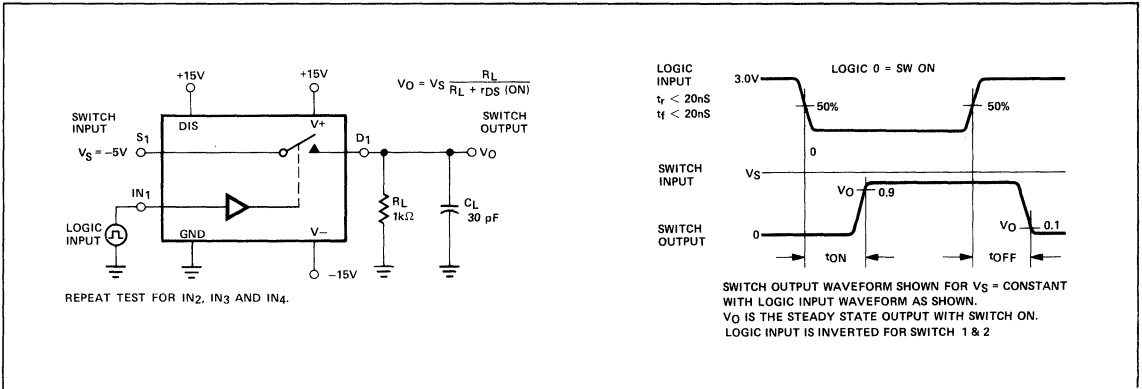
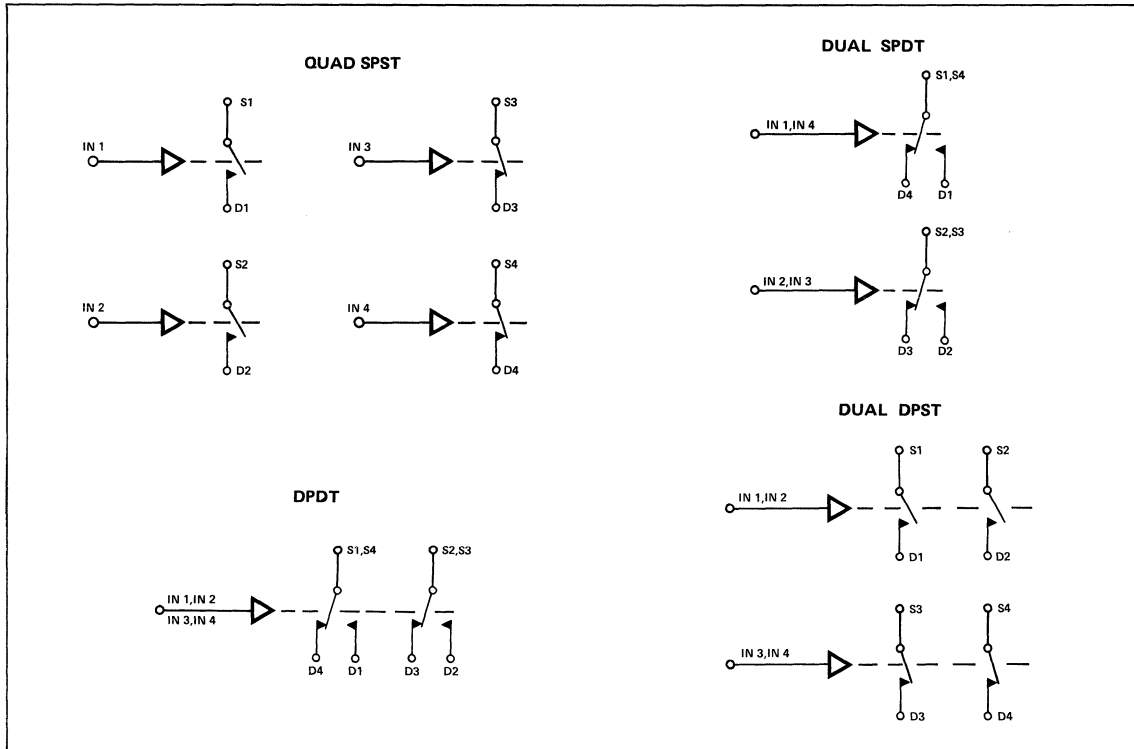
OFF ISOLATION TEST CIRCUIT

CROSSTALK TEST CIRCUIT

SWITCHING TIME TEST CIRCUIT


Figure 1: Functional Applications of SW-06


APPLICATIONS INFORMATION

This single analog switch product configures, by appropriate pin connections, into four switch applications. As shown in Figure 1, the SW-06 connects as a QUAD SPST, a DUAL SPDT, a DUAL DPST, or a DPDT analog switch. This versatility increases further when taking advantage of the disable input (DIS) which turns all switches OFF when taken active low.

Ion-implantation of the JFET analog switch achieves low ON resistance and tight channel to channel matching. Combining the low ON resistance and low leakage currents results in a worst case voltage error figure $V_{\text{ERROR}} @ 125^{\circ}\text{C} = I_{\text{D(ON)}} \times R_{\text{SD(ON)}} = 100\text{nA} \times 100\Omega = 11$ microvolts. This amount of error is negligible considering dissimilar-metal thermally-induced offsets will be in the 5 to 15 microvolt range.

LOGIC INPUTS

The logic inputs (IN_x) and disable input (DIS) are referenced to a TTL logic threshold value of two forward diode drops (1.4V at 25°C) above the GND terminal. These inputs use PNP transistors which draw maximum current at a logic "0" level and drops to a leakage current of a reverse biased diode as the logic input voltage raises above 1.4 volts. Any logic input voltage greater than 2.0 volts becomes logic "1", less than 0.8 volts becomes logic "0" resulting in full TTL noise immunity not available from similar CMOS input analog

switches. The PNP transistor inputs require such low input current that the SW-06 approaches fan-ins of CMOS input devices. These bipolar logic inputs exceed any CMOS input circuit in resistance to static voltage and radiation susceptibility. No damage will occur to the SW-06 if logic high voltages are present when the SW-06 power supplies are OFF. When the $V+$ and $V-$ supplies are OFF, the logic inputs present a reverse bias diode loading to active logic inputs. Input logic thresholds are independent of $V+$ and $V-$ supplies making single $V+$ supply operation possible by simply connecting GND and $V-$ together to the logic ground supply.

ANALOG VOLTAGE AND CURRENT

ANALOG VOLTAGE

These switches have constant ON resistance for analog voltages from the negative power supply ($V-$) to within 4 volts of the positive power supply. This characteristic shown in the plots results in good total harmonic distortion, especially when compared to CMOS analog switches that have a 20 to 30 percent variation in ON resistance versus analog voltage. Positive analog input voltages should be restricted to 4 volts less than $V+$ assuring the switch remains open circuit in the OFF state. No increase in switch ON resistance occurs when operating at supply voltages less than ± 15 volts (see plot). Small signals have a 3dB down frequency of 70MHz (see insertion loss versus frequency plot).

ANALOG CURRENT

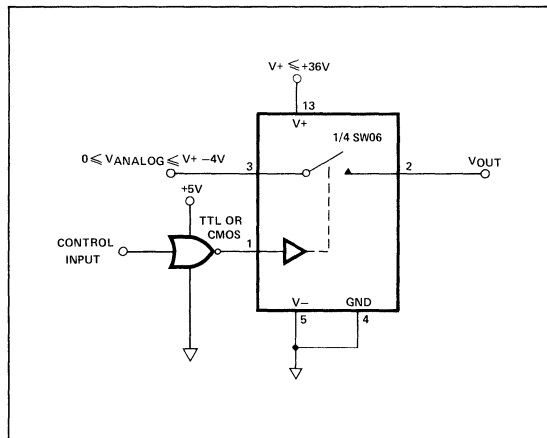
The analog switches in the ON state are JFETs biased in their triode region and act as switches for analog current up to the I_A specification (see plot of I_{DS} vs V_{DS}). Some applications require pulsed currents exceeding the I_A spec. For example, an integrator reset switch discharging a shunt capacitor will produce a peak current of $I_{A(PEAK)} = V_{CAP}/R_{DS(ON)}$. In this application, it is best to connect the source to the most positive end of the capacitor, thereby achieving the lowest switch resistance and fastest reset times. The switch can easily handle any amount of capacitor discharge current subject only to the maximum heat dissipation of the package and the maximum operating junction temperature from which repetition rates can be established.

SWITCHING

Switching time t_{ON} and t_{OFF} characteristics are plotted versus V_{ANALOG} and temperature. In all cases, t_{OFF} is designed faster than t_{ON} to insure a break-before-make interval for SPDT and DPDT applications. The disable input (DIS) has the same switching times (t_{ON} and t_{OFF}) as the logic inputs (IN_X).

TYPICAL APPLICATIONS

OPERATION FROM SINGLE POSITIVE POWER SUPPLY



Switching transients occurring at the source and drain contacts results from AC coupling of the switching FET's gate-to-source and gate-to-drain coupling capacitance. The switch turn ON will cause a negative going spike to occur and the turn OFF will cause a positive spike to occur. These spikes can be reduced by additional capacitance loading, lower values of R_L , or switching an additional switch (with its extra contact floating) to the opposite state connected to the spike sensitive node.

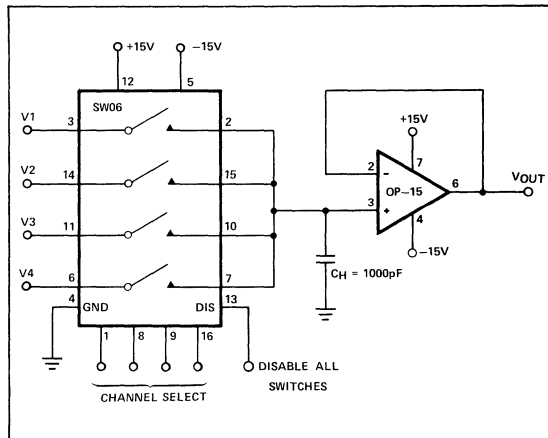
DISABLE NODE

This TTL compatible node is similar to the logic inputs IN_X but has an internal $2\mu A$ current source pull-up. If disable is left unconnected, it will assume the logic "1" state, then the state of the switches is controlled only by the logic inputs IN_X .

POWER SUPPLIES

This product operates with power supply voltages ranging from ± 12 to ± 18 volts; however, the specifications only guarantee device parameters with ± 15 volt $\pm 5\%$ power supplies. The power supply sensitive parameters have plots to indicate effects of supply voltages other than ± 15 volts.

4-CHANNEL SAMPLE HOLD AMPLIFIER



**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Operating Temperature Range	
SW-201BQ, SW-202BQ	-55°C to +125°C
SW-201FQ, SW-202FQ	-25°C to +85°C
SW-201GP, SW-202GP	0°C to +70°C
DICE Junction Temperature (T _j)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
P-Suffix	-65°C to +125°C
Power Dissipation (Note 2)	900mW
Lead Temperature (Soldering, 60 sec)	300°C
Maximum Junction Temperature	150°C
V+ Supply to V- Supply	36V

V+ Supply to Ground	36V
Logic Input Voltage	(-4V or V-) to V+ Supply
Analog Input Voltage Range	
Continuous	V- Supply to V+ Supply +20V
1% Duty Cycle and Driving	
all 4 Inputs with	
500μsec pulse	V- Supply -15V to V+ Supply +20V
Maximum Current Through Any Pin	30mA

NOTES:

- Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
- Derated 12mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS at V_± = ±15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201B SW-202B			SW-201F SW-202F			SW-201G SW-202G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R _{ON}	V _A = 0V, I _S = 1mA V _A = ±10V, I _S = 1mA	—	60	80	—	60	100	—	100	150	Ω
R _{ON} Match Between Switches	R _{ON} Match	V _A = 0V, I _D = 100μA; (Note 1)	—	5	15	—	5	20	—	—	20	%
Analog Voltage Range	V _A	I _S = 1.0mA (Note 6) I _S = 1.0mA	+10	+11	—	+10	+11	—	+10	+11	—	V
Analog Current Range	I _A	V _S = ±10V	10	15	—	7	12	—	5	10	—	mA
ΔR _{ON} vs Applied Voltage	ΔR _{ON}	V _S ≤ 10V, I _S = 1mA	—	5	15	—	10	20	—	10	20	%
Source Current in "OFF" Condition	I _S (OFF)	V _S = 10V, V _D = -10V, (Note 5)	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Drain Current in "OFF" Condition	I _D (OFF)	V _S = 10V, V _D = -10V, (Note 5)	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Leakage Current in "ON" Condition	I _S (ON) + I _D (ON)	V _S = V _D = ±10V, (Note 5)	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Logical "1" Input Current	I _{INH}	V _{IN} = 2V to 15V, (Note 4)	—	—	5	—	—	5	—	—	10	μA
Logical "0" Input Current	I _{INL}	V _{IN} = 0.8	—	1.5	5.0	—	1.5	5.0	—	1.5	10.0	μA
Turn-On-Time	t _{ON}	See Switching Time Test Circuit, (Note 7)	—	340	500	—	340	600	—	340	700	ns
Turn-Off-Time	t _{OFF}	See Switching Time Test Circuit, (Note 7)	—	200	400	—	200	400	—	200	500	ns
Break-Before-Make Time	t _{ON} -t _{OFF}	(Note 7)	50	140	—	50	140	—	50	140	—	ns
Source Capacitance	C _S (OFF)	V _A = 0V, (Note 5)	—	7	—	—	7	—	—	7	—	pF
Drain Capacitance	C _D (OFF)	V _A = 0V, (Note 5)	—	5.5	—	—	5.5	—	—	5.5	—	pF
Channel "ON" Capacitance	C _D (ON) + C _S (ON)	V _S = V _D = 0V, (Note 5)	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	I _{SO} (OFF)	V _S = 5V _{RMS} , R _L = 680Ω, C _L = 7pF, f = 500kHz, (Note 5)	—	58	—	—	58	—	—	58	—	dB
Crosstalk	C _T	V _S = 5V _{RMS} , R _L = 680Ω, C _L = 7pF, f = 500kHz, (Note 5)	—	70	—	—	70	—	—	70	—	dB
Positive Supply Current	I+	All Channels "ON", (Note 5)	—	4	9	—	4	10.5	—	4	12	mA
Negative Supply Current	I-	All Channels "ON", (Note 5)	—	1	5	—	1	6	—	1	6.5	mA
Positive Supply Current	I+	All Channels "OFF", (Note 5)	—	5	9	—	5	10.5	—	6	12	mA
Negative Supply Current	I-	All Channels "OFF", (Note 5)	—	4	6	—	4	7	—	4	8	mA
Ground Current	I _G	All Channels "ON" or "OFF"	—	3	4	—	3	4	—	3	6	mA



ELECTRICAL CHARACTERISTICS at $V_{\pm} = \pm 15V$; $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for SW-201BQ/202BQ; $-25^{\circ}C \leq T_A \leq +85^{\circ}C$ for SW-201FQ/202FQ; $0^{\circ}C \leq T_A \leq 70^{\circ}C$ for SW-201GP/202GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201B SW-202B			SW-201F SW-202F			SW-201G SW-202G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Temperature Range	T_A	Operating	-55	—	125	-25	—	85	0	—	70	$^{\circ}C$
"ON" Resistance	R_{ON}	$V_A = 0V, I_D = 1mA$ $V_A = \pm 10V, I_D = 1mA$	—	75	110	—	75	125	—	—	175	Ω
R_{ON} Match Between Switches	$R_{ON\ Match}$	$V_A = 0V, I_D = 100\mu A$; (Note 1)	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	$I_S = 1.0mA$ $I_S = 1.0mA$ (Note 6)	+10	+11	—	+10	+11	—	+10	+11	—	V
Analog Current Range	I_A	$V_S = \pm 10.0V$	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$V_S \leq +10V$ $I_S = 1mA$	—	10	—	—	12	—	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$; (Note 5) $T_A = \text{Max. Operating Temp.}$	—	—	60	—	—	30	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$; (Note 5) $T_A = \text{Max. Operating Temp.}$	—	—	60	—	—	30	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10V$, (Note 5) $T_A = \text{Max. Operating Temp.}$	—	—	100	—	—	30	—	—	60	nA
Logical "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	2	—	—	2	—	—	V
Logic "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	$V_{IN} = 2V$ to $15V$, (Note 4)	—	—	10	—	—	10	—	—	15	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8$	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Test Circuit, (Note 2)	—	440	900	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Test Circuit, (Note 2)	—	300	500	—	330	500	—	—	500	ns
Break-Before-Make Time	$t_{ON-t_{OFF}}$	(Note 3)	—	70	—	—	70	—	—	50	—	ns
Positive Supply Current	I_+	All Channels "ON", (Note 5)	—	—	13.5	—	—	14.0	—	—	15.8	mA
Negative Supply Current	I_-	All Channels "ON", (Note 5)	—	—	8.5	—	—	11.0	—	—	14.5	mA
Positive Supply Current	I_+	All Channels "OFF", (Note 5)	—	—	13.5	—	—	14.0	—	—	18	mA
Negative Supply Current	I_-	All Channels "OFF", (Note 5)	—	—	8.5	—	—	11.0	—	—	14.5	mA
Ground Current	I_G	All Channels "ON" or "OFF"	—	—	6.0	—	—	7.8	—	—	10.0	mA

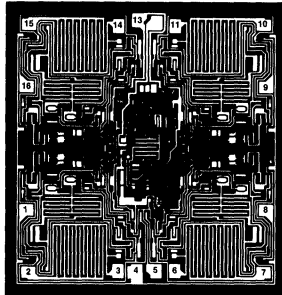
NOTES:

- $V_A = 0V, I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$
- Guaranteed by design.
- Switch is guaranteed to provide break-before-make operation.
- Current tested at $V_{IN} = 2V$. This is worst case condition.
- Switch being tested ON or OFF as indicated, $V_{INH} = 2V$ or $V_{INL} = 0.8V$, per logic truth table.
- Guaranteed by R_{ON} and leakage tests. For normal operation analog signal voltages should be restricted to less than $(V_+) - 4V$.
- Sample tested.



DICE CHARACTERISTICS



DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils
(2.540 × 2.438 mm, 6.193 sq. mm)

- | | |
|-------------------|---------|
| 1. IN1 | 9. IN3 |
| 2. D1 | 10. D3 |
| 3. S1 | 11. S3 |
| 4. V- (SUBSTRATE) | 12. V+ |
| 5. GND | 14. S4 |
| 6. S2 | 15. D4 |
| 7. D2 | 16. IN4 |
| 8. IN2 | |

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 15V$, $V_- = -15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N LIMIT	SW-201G SW-202G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	80	100	Ω MAX
R_{ON} Mismatch	R_{ON} Match	$V_A = 0V$, $I_S \leq 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$V_S \leq 10V$, $I_S = 1mA$	15	20	% MAX
Positive Supply	I+	(Note 1)	9	10.5	mA MAX
Negative Supply Current	I-	(Note 1)	6	7	mA MAX
Ground Current	I_G		4	4	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$ (Note 3)	± 10	± 10	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 3)	2	2	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 3)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \leq V_{IN} \leq 0.8V$	5	5	μA MAX
Logic "1" Input Current	I_{INH}	$2V \leq V_{IN} \leq 15V$, (Note 2)	5	5	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

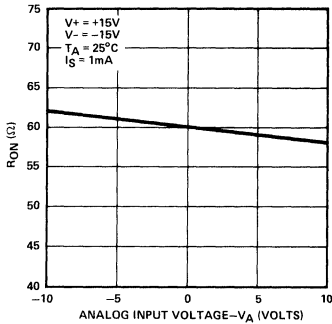
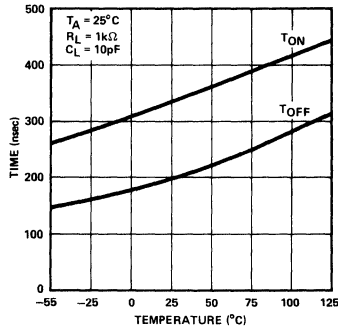
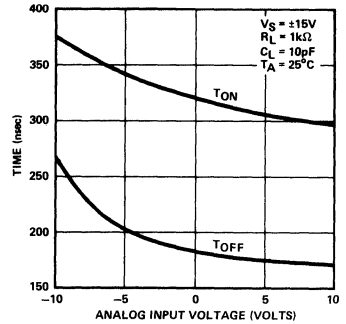
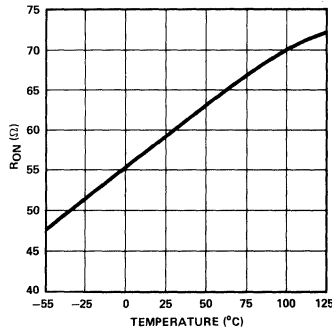
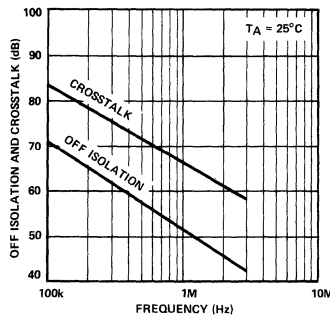
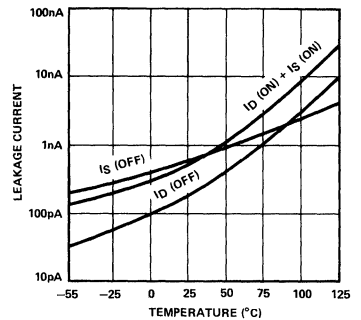
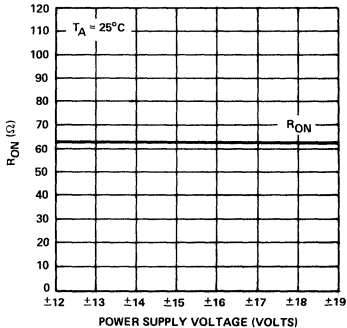
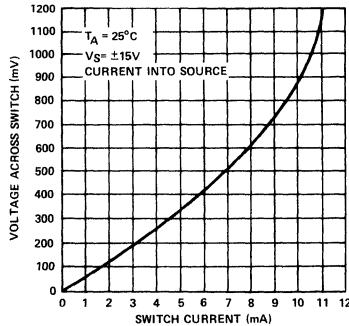
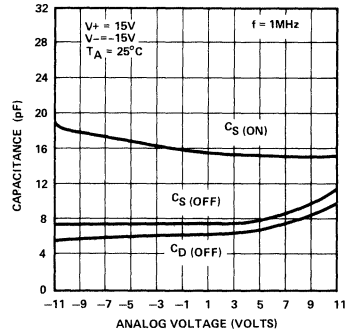
TYPICAL ELECTRICAL CHARACTERISTICS $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N TYPICAL	SW-201G SW-202G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

NOTES:

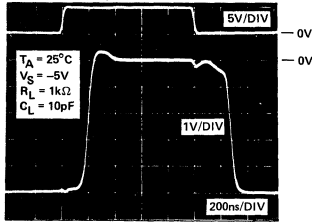
- Power supply and ground current specified for switch "ON" or "OFF".
- Current tested at $V_{IN} = 2V$. This is worst case condition.
- Guaranteed by R_{ON} and leakage tests.

TYPICAL PERFORMANCE CHARACTERISTICS

"ON" RESISTANCE vs ANALOG VOLTAGE (V_A)

SWITCHING TIME vs TEMPERATURE

SWITCHING TIME vs ANALOG VOLTAGE

 R_{ON} vs TEMPERATURE

CROSTALK AND "OFF" ISOLATION vs FREQUENCY

LEAKAGE CURRENT vs TEMPERATURE

"ON" RESISTANCE vs POWER SUPPLY VOLTAGE

SWITCH CURRENT vs VOLTAGE

SWITCH CAPACITANCE vs ANALOG VOLTAGE


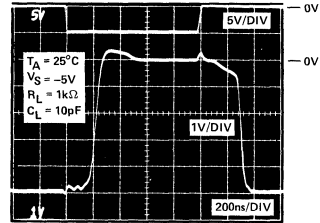
TYPICAL PERFORMANCE CHARACTERISTICS

SW-201 t_{ON}/t_{OFF} SWITCHING RESPONSE



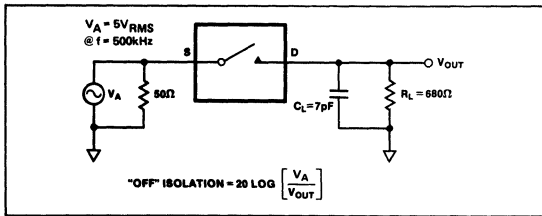
TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

SW-202 t_{ON}/t_{OFF} SWITCHING RESPONSE

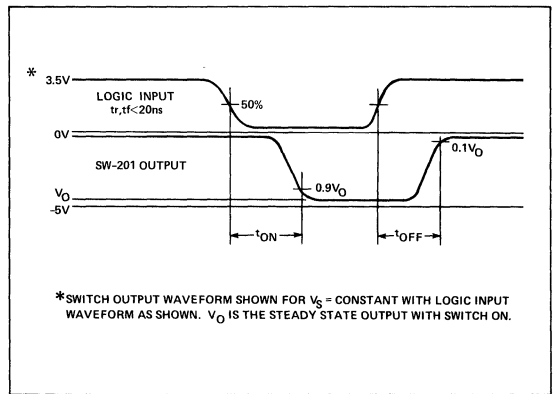


TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

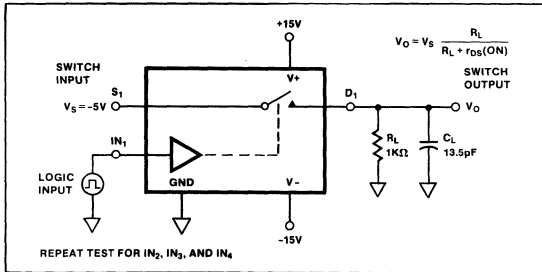
OFF ISOLATION TEST CIRCUIT



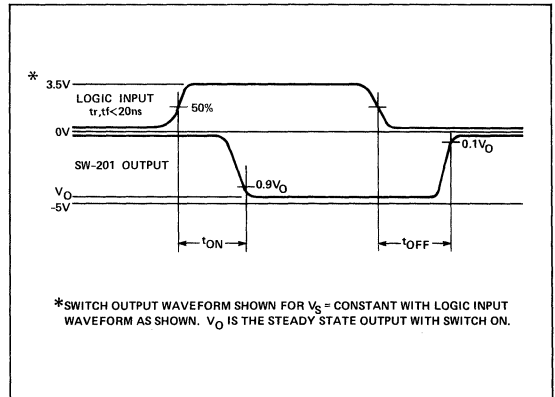
SW-201 WAVEFORMS



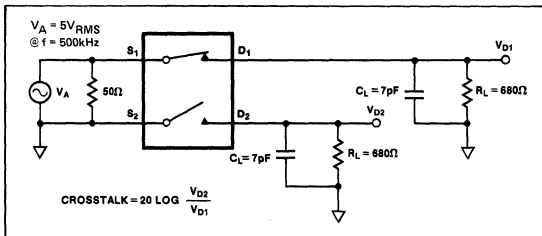
SWITCHING TIME TEST CIRCUIT



SW-202 WAVEFORMS



CROSSTALK TEST CIRCUIT

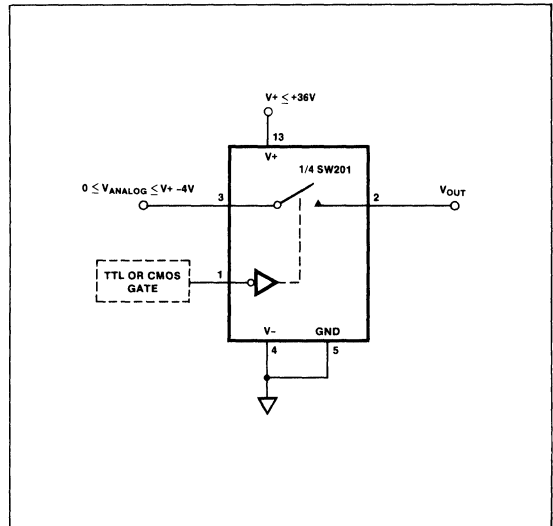


APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode as the input voltage is raised above $\approx 1.4V$.

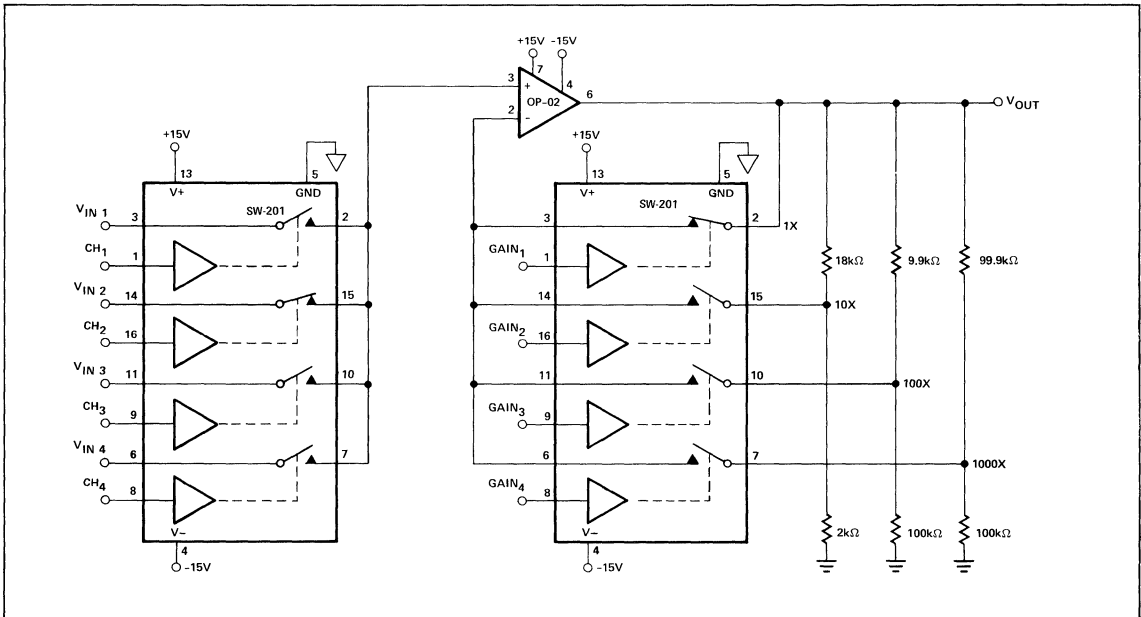
The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to $11V$ (or $4V$ less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p , and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

OPERATION FROM SINGLE POSITIVE POWER SUPPLY



TYPICAL APPLICATIONS

PROGRAMMABLE GAIN NONINVERTING AMPLIFIER WITH SELECTABLE INPUTS



ANALOG SWITCHES/MULTIPLEXERS



SW-7510/SW-7511

QUAD SPST JFET
ANALOG SWITCHES

Precision Monolithics Inc.

FEATURES

- Pin Compatible with AD7510 DI, AD7511 DI
- JFET Switches Rather than CMOS
- Highly Resistant to Static Discharge Damage
- Radiation Resistant
- No SCR Latch-up Problems
- Low "ON" Resistance — 75Ω Max
- Superior "OFF" Isolation and Crosstalk
- Digital Inputs Compatible with TTL and CMOS
- No Pull-Up Resistors Required to Insure Break-Before-Make Action with TTL Inputs

ORDERING INFORMATION†

TYPICAL 25°C RESISTANCE	PACKAGE HERMETIC DIP	TEMPERATURE RANGE
60Ω	SW7510AQ* SW7510EQ	MIL IND
80Ω	SW7510BQ* SW7510FQ	MIL IND
60Ω	SW7511AQ* SW7511EQ	MIL IND
80Ω	SW7511BQ* SW7511FQ	MIL IND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The SW-7510/7511 are monolithic linear devices, each containing four independently selectable SPST analog switches. The SW-7510 operates normally-open with logic-low inputs. The SW-7511 operates normally-closed with logic-low inputs. All logic inputs are fully TTL input compatible.

Performance advantages include exceptionally high "OFF" isolation, low leakage current and low crosstalk. Data conversion, position controllers, choppers, demodulators and programmable-gain amplifiers are popular SW-7510/7511 circuit applications.

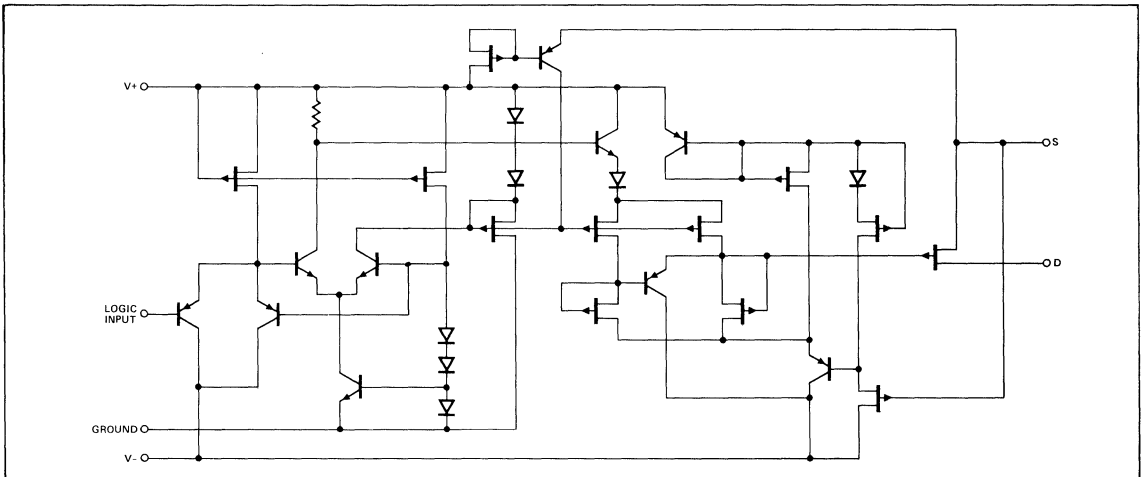
The PMI Bipolar-JFET process reduces susceptibility to electrostatic destruction and offers a high resistance to radiation exposure. Plus, total freedom from the intrinsic SCR latch-up problems encountered in equivalently manufactured CMOS products.

PIN CONNECTIONS

16-PIN HERMETIC DUAL-IN-LINE (Q-Suffix)

CONTROL LOGIC:
SW-7510: Switch "ON" for Address "HIGH"
SW-7511: Switch "ON" for Address "LOW"

SCHEMATIC DIAGRAM (Typical SW-7510 Switch)



**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, unless otherwise noted).

Operating Temperature Range, SW-7510/7511AQ, BQ	-55°C to $+125^\circ\text{C}$
SW-7510/7511EQ, FQ	-25°C to $+85^\circ\text{C}$
DICE Junction Temperature (T_j)	-65°C to $+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Power Dissipation	500mW
Derate above 100°C	10mW/ $^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C
Maximum Junction Temperature	150°C
V+ Supply to V- Supply	36V

V+ Supply to Ground	36V
Logic Input Voltage	(-2V or V-) to V+ Supply
Analog Input Voltage	
Continuous	V- Supply to V+ Supply +20V
1% Duty Cycle and Driving	
all 4 Inputs with	
500 μs pulse	V- Supply -15V to V+ Supply +20V
Maximum Current Through Any Pin	25mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510A/E SW-7511A/E			SW-7510B/F SW-7511B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_D = 0\text{V}$, $I_{DS} = 1\text{mA}$	—	60	75	—	80	100	Ω
ΔR_{ON} vs. V_D (V_S)	ΔR_{ON}	$V_D \leq 10\text{V}$, $I_D = 1\text{mA}$	—	15	—	—	15	—	%
R_{ON} Match of Switches	R_{ON} Match	$V_D = 0\text{V}$, $I_{DS} = 1\text{mA}$	—	1.5	10	—	1.5	10	%
Analog Voltage Range	V_A	$I_S = 1\text{mA}$ (Note 5)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V
"OFF" Leakage Current	$I_{S(OFF)}$, $I_{D(OFF)}$	$V_S = +10\text{V}$, $V_D = -10\text{V}$, (Note 1)	—	—	1.0	—	—	3.0	nA
"ON" Leakage Current	$I_{S(ON)}$, $I_{D(ON)}$	$V_S = V_D = +10\text{V}$, (Note 1)	—	—	1.0	—	—	3.0	nA
Logic "1" Voltage	V_{INH}	(Note 5)	2.0	—	—	2.0	—	—	V
Logic "0" Voltage	V_{INL}	(Note 5)	—	—	0.8	—	—	0.8	V
Logic "0" Current	I_{INL}	$V_{IN} = +0.4\text{V}$	—	1.5	3.5	—	1.5	3.5	μA
Logic Input Capacitance	C_{DIG}	$V_{IN} = +0.4\text{V}$	—	1.5	—	—	1.5	—	pF
"ON" Switching Time	t_{ON}	$V_S = -5\text{V}$, $R_L = 1\text{k}\Omega$, $C_L = 7\text{pF}$, (Note 4)	—	350	450	—	450	550	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5\text{V}$, $R_L = 1\text{k}\Omega$, $C_L = 7\text{pF}$, (Note 4)	—	260	300	—	350	450	ns
"OFF" Isolation	ISO_{OFF}	(Note 2)	—	66	—	—	66	—	dB
Crosstalk	C_T	(Note 3)	—	70	—	—	70	—	dB
Analog "OFF" Capacitance	$C_{S(OFF)}$, $C_{D(OFF)}$	$V_S = V $, $V_D = 0$	—	6.5	—	—	6.5	—	pF
Analog "ON" Capacitance	$C_{S(ON)}$, $C_{D(ON)}$	$V_S = 0\text{V}$, $V_D = 0$	—	14	—	—	14	—	pF
Feedthrough Capacitance	$C_{DS(OFF)}$	$V_S = 0\text{V}$	—	0.8	—	—	0.8	—	pF
Channel Capacitance	$C_{SS(OFF)}$, $C_{DD(OFF)}$	$V_S = 0\text{V}$ $V_S = 0\text{V}$	—	0.4	—	—	0.4	—	pF
Positive Supply Current	I^+	Logic Inputs at "0" or "1"	—	5.0	9.0	—	3.0	9.0	mA
Negative Supply Current	I^-	Logic Inputs at "0" or "1"	—	2.8	5.0	—	1.7	5.0	mA

NOTES:

- The conditions listed specify the worst case leakage currents. The leakage currents apply equally to source (S) or drain (D).
- OFF isolation is measured by driving the source of any OFF switch and observing the voltage which appears on the drain. The conditions are: $R_L = 680\Omega$, $C_L = 7\text{pF}$, $V_S = 5V_{RMS}$, $f = 100\text{kHz}$.
- Crosstalk is measured by driving source of any OFF switch and observing voltage which appears on any other "ON" output drain. The conditions are: $R_L = 680\Omega$, $C_L = 7\text{pF}$, $V_S = 5V_{RMS}$, $f = 100\text{kHz}$.
- Sample tested.
- Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltages should be restricted to less than $(V^+) - 4\text{V}$.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for SW-7510AQ, BQ and SW-7511AQ, BQ; and $-25^\circ C \leq T_A \leq +85^\circ C$ for SW-7510EQ, FQ and SW-7511EQ, FQ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510A/E SW-7511A/E			SW-7510B/F SW-7511B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_D = 0V, I_{DS} = 1mA$	—	—	100	—	—	150	Ω
ΔR_{ON} vs. Temperature	ΔR_{ON} Drift	$V_D = 0V, I_{DS} = 1mA$	—	0.4	—	—	0.5	—	%/ $^\circ C$
Analog Voltage Range	V_A	$I_S = 1mA$ (Note 4)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V
"OFF" Leakage Current	$I_{S(OFF)}, I_{D(OFF)}$	$V_S = +10V, V_D = -10V$, (Notes 1, 3)	—	—	90	—	—	100	nA
"ON" Leakage Current	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = +10V$, (Notes 1, 3)	—	—	90	—	—	100	nA
Logic "1" Voltage	V_{INH}	(Note 4)	2.0	—	—	2.0	—	—	V
Logic "0" Voltage	V_{INL}	(Note 4)	—	—	0.8	—	—	0.8	V
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	—	—	5.0	—	—	7.0	μA
"ON" Switching Time	t_{ON}	$V_S = -5V, R_L = 1k\Omega, C_L = 7pF$ (Note 2)	—	—	600	—	—	1000	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V, R_L = 1k\Omega, C_L = 7pF$ (Note 2)	—	—	500	—	—	750	ns
Positive Supply Current	I_+	Logic Inputs at "0" or "1"	—	—	13	—	—	13	mA
Negative Supply Current	I_-	Logic Inputs at "0" or "1"	—	—	7.5	—	—	7.5	mA

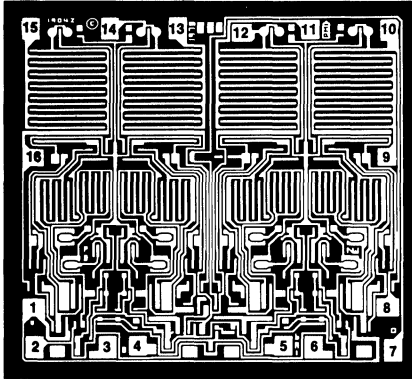
NOTES:

1. The conditions listed specify the worst case leakage currents. The leakage currents apply equally to source (S) or drain(D).
2. Guaranteed by design.
3. Tested at $125^\circ C$ only for "A" and "B" grades.
4. Guaranteed by R_{ON} and leakage tests.

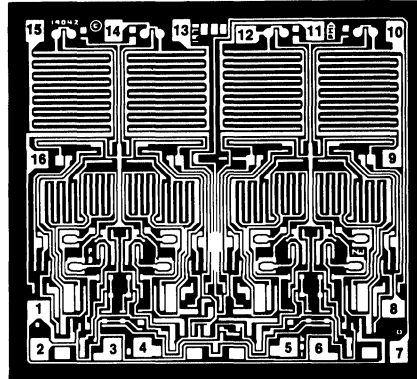


DICE CHARACTERISTICS

SW-7510 (SWITCH ON FOR ADDRESS HIGH)



SW-7511 (SWITCH ON FOR ADDRESS LOW)



DIE SIZE 0.091 × 0.083 inch, 7553 sq. mils
(2.311 × 2.108 mm, 1.918 sq. mm)

- | | | | |
|--------------------------------|-----------------|--------------------------------|-----------------|
| 1. NEGATIVE SUPPLY (SUBSTRATE) | 9. DRAIN (D4) | 1. NEGATIVE SUPPLY (SUBSTRATE) | 9. DRAIN (D4) |
| 2. GROUND | 10. SOURCE (S4) | 2. GROUND | 10. SOURCE (S4) |
| 3. ADDRESS (A1) | 11. DRAIN (D3) | 3. ADDRESS (A1) | 11. DRAIN (D3) |
| 4. ADDRESS (A2) | 12. SOURCE (S3) | 4. ADDRESS (A2) | 12. SOURCE (S3) |
| 5. ADDRESS (A3) | 13. DRAIN (D2) | 5. ADDRESS (A3) | 13. DRAIN (D2) |
| 6. ADDRESS (A4) | 14. SOURCE (S2) | 6. ADDRESS (A4) | 14. SOURCE (S2) |
| 7. DISABLE (NO CONNECT) | 15. DRAIN (D1) | 7. DISABLE (NO CONNECT) | 15. DRAIN (D1) |
| 8. POSITIVE SUPPLY | 16. SOURCE (S1) | 8. POSITIVE SUPPLY | 16. SOURCE (S1) |

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = +15V$, $V_- = -15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510N/ SW-7511N LIMIT	SW-7510G/ SW-7511G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	75	100	Ω MAX
Logic "1" Voltage	V_{INH}	(Note 1)	2.0	2.0	V MIN
Logic "0" Voltage	V_{INL}	(Note 1)	0.8	0.8	V MAX
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	3.5	3.5	μA MAX
Positive Supply Current	I+	Logic Inputs at "0"	9	9	mA MAX
Negative Supply Current	I-	Logic Inputs at "0"	5	5	mA MAX

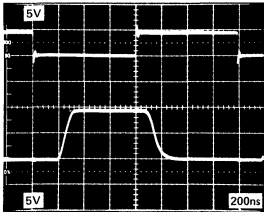
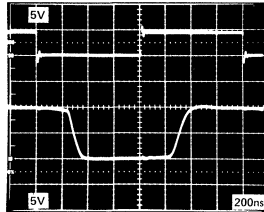
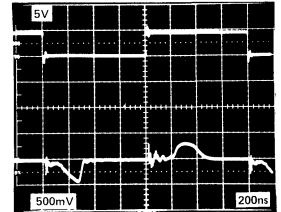
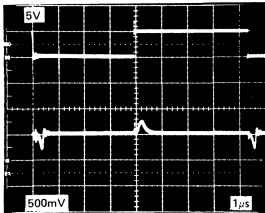
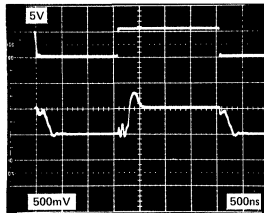
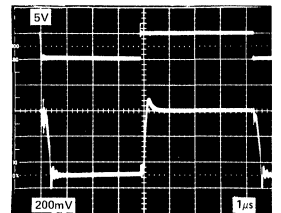
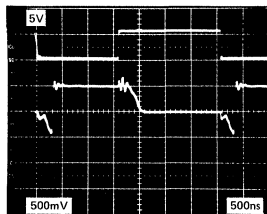
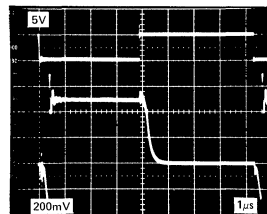
NOTES:

1. Guaranteed by R_{ON} and leakage tests.
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = +15V$, $V_- = -15V$ and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510N/ SW-7511N TYPICAL	SW-7510G/ SW-7511G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	60	80	Ω
R_{ON} vs. Temperature	R_{ON} Drift	$V_D = 0V$, $I_{DS} = 1mA$	0.4	0.5	%/ $^\circ C$
"ON" Switching Time	t_{ON}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$	350	450	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$	260	350	ns

TYPICAL PERFORMANCE CHARACTERISTICS (Apply to all models, unless otherwise noted)

LARGE-SIGNAL SWITCHING

 $V_A = +10V, R_L = 1k\Omega, C_L = 13pF$
LARGE-SIGNAL SWITCHING

 $V_A = -10V, R_L = 1k\Omega, C_L = 100pF$
SMALL-SIGNAL SWITCHING

 $V_A = 0V, R_L = 1k\Omega, C_L = 13pF$
SMALL-SIGNAL SWITCHING WITH FILTERING

 $V_A = 0V, R_L = 1k\Omega, C_L = 100pF$
SMALL-SIGNAL SWITCHING

 $V_A = -500mV, R_L = 1k\Omega, C_L = 13pF$
SMALL-SIGNAL SWITCHING WITH FILTERING

 $V_A = -500mV, R_L = 1k\Omega, C_L = 100pF$
SMALL-SIGNAL SWITCHING

 $V_A = 500mV, R_L = 1k\Omega, C_L = 13pF$
SMALL-SIGNAL SWITCHING WITH FILTERING

 $V_A = 500mV, R_L = 1k\Omega, C_L = 100pF$
NOTE:

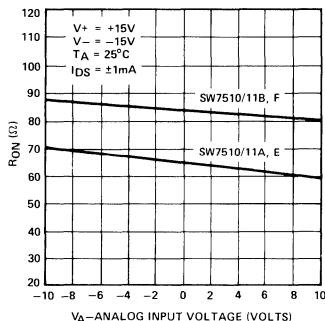
 Upper Photo Traces: Logic Control Signal A_X (5V/DIV)

 Lower Photo Traces: Switch Outputs V_D

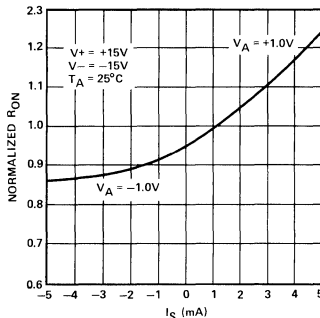


TYPICAL PERFORMANCE CHARACTERISTICS (Apply to all models, unless otherwise noted)

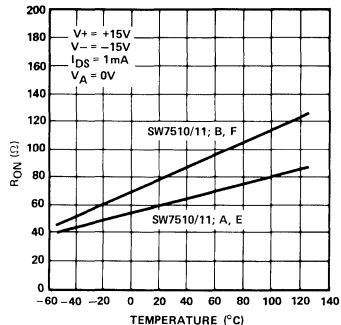
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



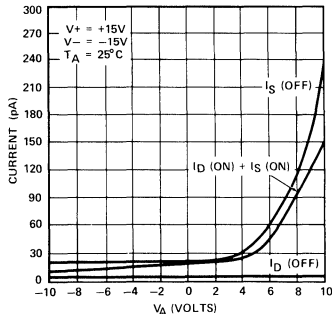
NORMALIZED R_{ON} vs SWITCH CURRENT (I_S)



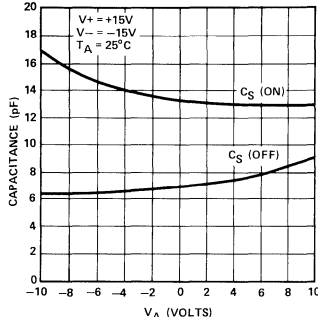
R_{ON} vs TEMPERATURE



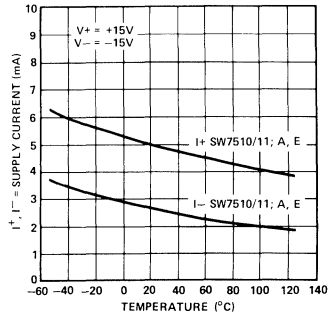
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



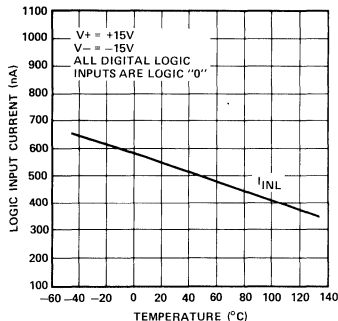
SWITCH CAPACITANCES vs ANALOG VOLTAGE (V_A)



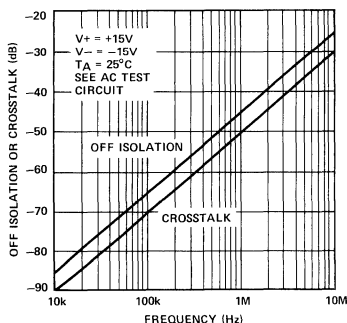
SUPPLY CURRENTS vs TEMPERATURE



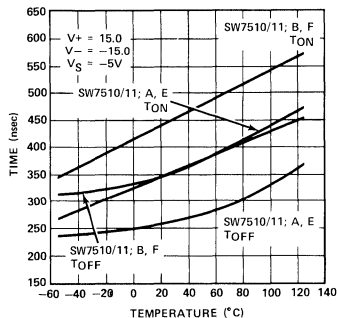
DIGITAL INPUT CURRENT I_{INL} vs TEMPERATURE



CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



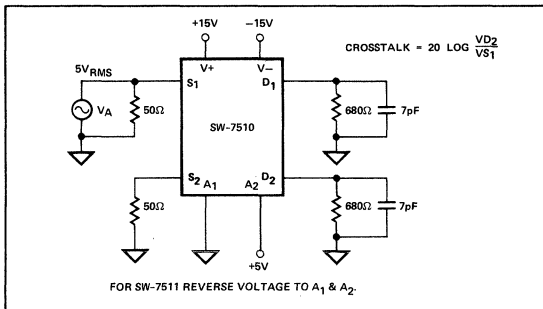
SWITCHING TIMES vs TEMPERATURE



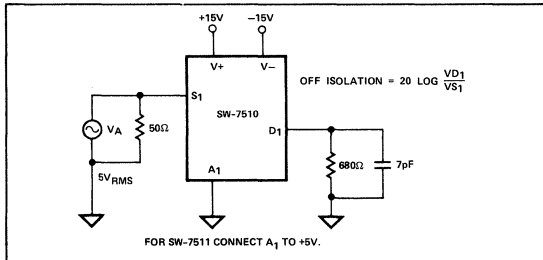


AC TEST CIRCUITS

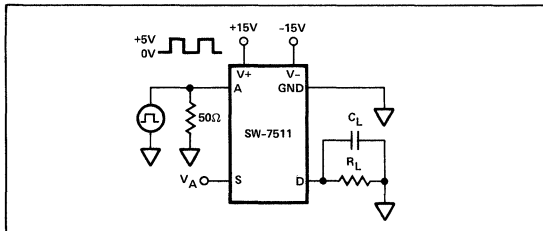
CROSSTALK MEASUREMENT CIRCUIT



ISOLATION MEASUREMENT CIRCUIT



SWITCHING TIME TEST CIRCUIT



APPLICATIONS INFORMATION

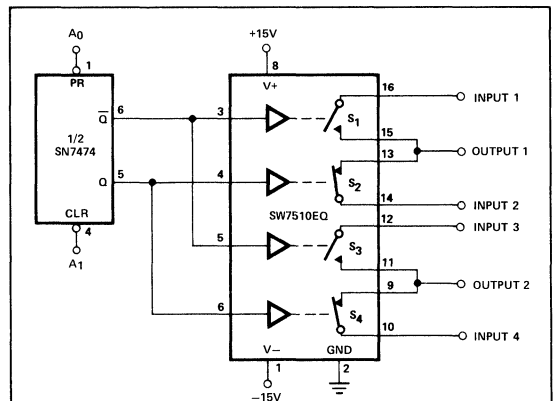
This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with

$V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P , and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

Proper switching requires the "Source" terminal be connected to the input driving signal.

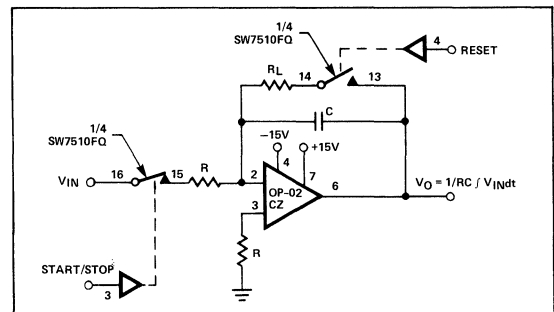
LATCHING DPDT SWITCH



Truth Table

Command		State of Switches After Command	
A ₀	A ₁	S2 and S3	S1 and S3
1	1	same	same
0	1	on	off
1	0	off	on
0	0	INDETERMINATE	

INTEGRATOR WITH ANALOG RESET AND START/STOP CAPABILITY

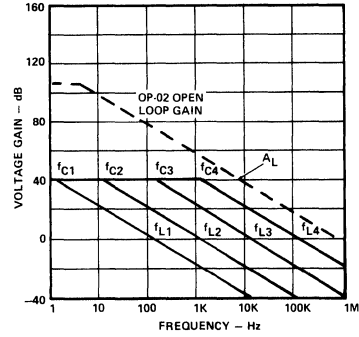
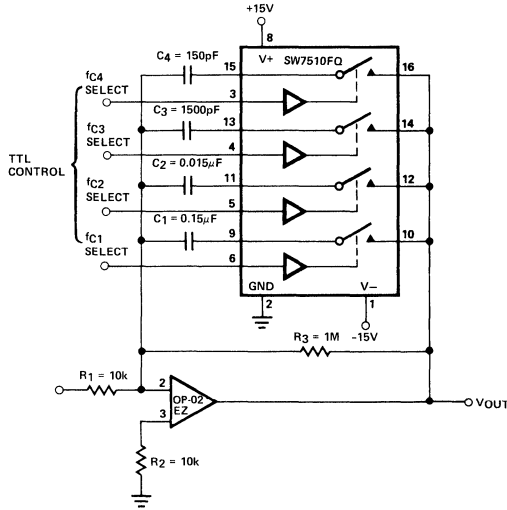


NOTE: Applications show SW-7510. For SW-7511 applications the logic is inverted.



TYPICAL APPLICATIONS

ACTIVE LOW-PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY



A_L (VOLTAGE GAIN BELOW BREAK FREQUENCY) =

$$\frac{R_3}{R_1} = 100 \text{ (40dB)}$$

$$f_C \text{ (BREAK FREQUENCY)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (UNITY GAIN FREQUENCY)} = \frac{1}{2\pi R_1 C_X}$$

NOTE: Applications show SW-7510. For SW-7511 applications the logic is inverted.



MUX-08/MUX-24

8-CHANNEL/DUAL 4-CHANNEL JFET ANALOG MULTIPLEXERS
(OVERVOLTAGE AND POWER SUPPLY LOSS PROTECTED)

Precision Monolithics Inc.

FEATURES

- JFET Switches Rather Than CMOS
- Low "ON" Resistance 220Ω Typ
- Highly Resistant to Static Discharge Damage
- No SCR Latch-Up Problems
- Digital Inputs Compatible With TTL and CMOS
- 125° C Temperature Tested Dice Available
- MUX-08 Pin Compatible With DG508, HI-508A, IH5108, IH6108, LF11508/12508/13508, AD7506
- MUX-24 Pin Compatible With DG509, HI-509A, IH5208, IH6208, LF11509/12509/13509, AD7507

ORDERING INFORMATION†

25° C ON RESISTANCE	PACKAGE			TEMPERATURE RANGE
	HERMETIC DIP	PLASTIC DIP	LCC	
220Ω	MUX08AQ*	—	—	MIL
	MUX08EQ	—	—	IND
	—	MUX08EP	—	COM
300Ω	MUX08BQ*	—	MUX08BRC/883	MIL
	MUX08FQ	—	—	IND
	—	MUX08FP	—	COM
220Ω	MUX24AQ*	—	—	MIL
	MUX24EQ	—	—	IND
	—	MUX24EP	—	COM
300Ω	MUX24BQ*	—	—	MIL
	MUX24FQ	—	—	IND
	—	MUX24FP	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address.

The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four-position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs.

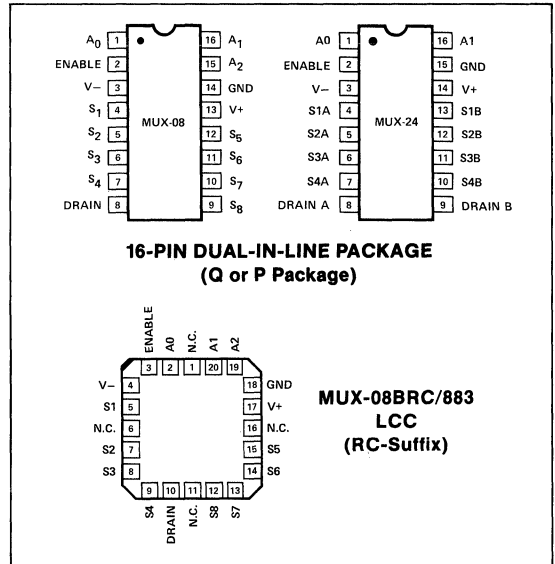
All switches in the MUX-08/MUX-24 are turned OFF by applying logic "0" to the ENABLE pin, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance, low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite

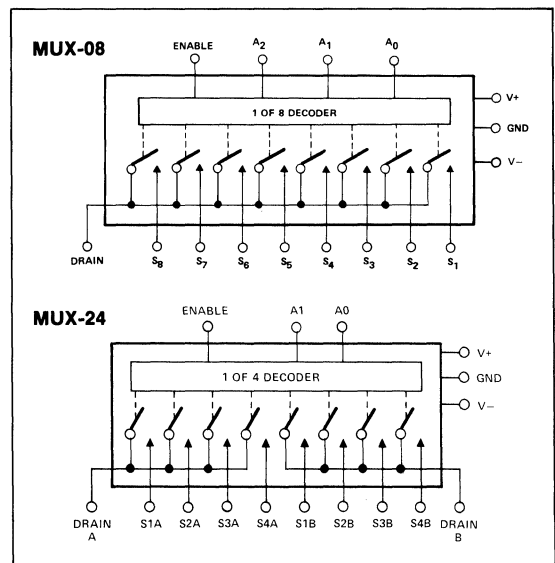
break-before-make action without the need for external pull-up resistors over the full operating temperature range.

For single sixteen-channel and dual eight-channel models, refer to the MUX-16/MUX-28 data sheet.

PIN CONNECTIONS



FUNCTIONAL DIAGRAMS





ABSOLUTE MAXIMUM RATINGS (Note)

Operating Temperature Range
 MUX-08/24-AQ, BQ, BRC -55°C to +125°C
 MUX-08/24-EQ, FQ -25°C to +85°C
 MUX-08/24-EP, FP 0°C to +70°C
 DICE Junction Temperature (T_J) -65°C to +150°C
 Storage Temperature Range -65°C to +150°C
 P-Suffix -65°C to +125°C
 Power Dissipation 500mW
 Derate above 100°C 10mW/°C

Lead Temperature (Soldering, 60 sec) 300°C
 Maximum Junction Temperature 150°C
 V+ Supply to V- Supply 36V
 Logic Input Voltage (-4V or V-) to V+ Supply
 Analog Input Voltage ... V- Supply -20V to V+ Supply +20V
 Maximum Current Through Any Pin 25mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V- = -15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08A/E MUX-24A/E			MUX-08B/F MUX-24B/F			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
"ON" Resistance	R _{ON}	V _S ≤ 10V, I _S ≤ 200μA	—	220	300	—	300	400	Ω	
ΔR _{ON} With Applied Voltage	ΔR _{ON}	-10V ≤ V _S ≤ 10V, I _S = 200μA	—	1	5	—	3	7	%	
R _{ON} Match Between Switches	R _{ON} Match	V _S = 0V, I _S = 200μA	—	7	15	—	9	20	%	
Analog Voltage Range	V _A	(Note 6)	+10	+10.4	—	+10	+10.4	—	V	
			-10	-15	—	-10	-15	—		
Source Current (Switch "OFF")	I _{S(OFF)}	V _S = 10V, V _D = -10V (Note 1)	—	0.01	1.0	—	0.01	2.0	nA	
Drain Current (Switch "OFF")	I _{D(OFF)}	V _S = 10V, V _D = -10V (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Leakage Current (Switch "ON")	I _{D(ON)} + I _{S(ON)}	V _D = 10V (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Digital Input Current	I _{IN}	V _{IN} = 0.4V to 15V	—	1	10	—	1	10	μA	
Digital "0" Enable Current	I _{INL(EN)}	V _{EN} = 0.4V	—	4	10	—	4	10	μA	
Digital Input Capacitance	C _{DIG}		—	3	—	—	3	—	pF	
Switching Time	t _{TRAN}	(Notes 2, 5) Figure 1 (Test Circuit)	—	1.8	2.1	—	1.8	2.1	μs	
Output Settling Time	t _S	10V Step to 0.10% 10V Step to 0.05% 10V Step to 0.02%	—	1.3	—	—	1.7	—	μs	
			—	1.5	—	—	1.9	—		
			—	2.3	—	—	2.5	—		
Break-Before-Make Delay	t _{OPEN}	Figure 3 (Test Circuit)	—	0.8	—	—	1.0	—	μs	
Enable Delay "ON"	t _{ON(EN)}	(Note 5) Figure 2 (Test Circuit)	—	1	2	—	1	2	μs	
Enable Delay "OFF"	t _{OFF(EN)}	(Note 5) Figure 2 (Test Circuit)	MUX-08 MUX-24	— —	0.1 0.2	0.4 0.5	— —	0.2 0.3	0.4 0.6	μs
"OFF" Isolation	ISO _{OFF}	(Note 4) Figure 5 (Test Circuit)	MUX-08 MUX-24	— —	60 66	— —	— —	60 66	— —	dB
Crosstalk	CT	(Note 3) Figure 4 (Test Circuit)	MUX-08 MUX-24	— —	70 76	— —	— —	70 76	— —	dB
Source Capacitance	C _{S(OFF)}	Switch "OFF", V _S = 0V, V _D = 0V	MUX-08 MUX-24	— —	2.5 2	— —	— —	2.5 2	— —	pF
Drain Capacitance	C _{D(OFF)}	Switch "OFF", V _S = 0V, V _D = 0V	MUX-08 MUX-24	— —	7 4	— —	— —	7 4	— —	pF
Input to Output Capacitance	C _{DS(OFF)}	(Note 4)	MUX-08 MUX-24	— —	0.3 0.15	— —	— —	0.3 0.15	— —	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I ₊	V ₊ = 15V V ₊ = 5V	—	10 8	12 —	—	6 5	12 —	— —	mA
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I ₋	V ₊ = -15V V ₊ = -5V	—	3.0 2.5	3.8 —	—	2.0 1.8	3.8 —	— —	mA

NOTES: See next page.



ELECTRICAL CHARACTERISTICS at $V+ = 15V$, $V- = -15V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08A/ MUX-24A			MUX-08B/ MUX-24B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S \leq 10V, I_S \leq 200\mu A$	—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V, I_S = 200\mu A$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V, I_S = 200\mu A$	—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	—	—	25	—	—	50	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24	—	100 50	—	—	500 500	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+ I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24	—	100 50	—	—	500 500	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	—	2	—	—	2	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.7	—	—	0.7	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA
Negative Supply Current	I-	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA

ELECTRICAL CHARACTERISTICS at $V+ = 15V$, $V- = -15V$ and $-25^{\circ}C \leq T_A \leq +85^{\circ}C$ for MUX-08EQ, FQ and MUX-24EQ, FQ; $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for MUX-08EP, FP and MUX-24EP, FP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08E/ MUX-24E			MUX-08F/ MUX-24F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S \leq 10V, I_S \leq 200\mu A$	—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V, I_S = 200\mu A$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V, I_S = 200\mu A$	—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24	—	100 50	—	—	100 50	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+ I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24	—	100 50	—	—	100 50	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	—	2	—	—	2	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.8	—	—	0.8	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA
Negative Supply Current	I-	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA

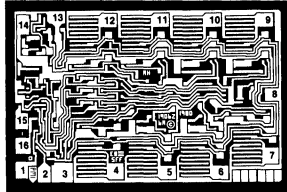
NOTES:

- Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
- $R_L = 10M\Omega$, $C_L = 10pF$.
- Crosstalk is measured by driving channel 8 with channel 4 "ON".
 $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, $f = 500kHz$.

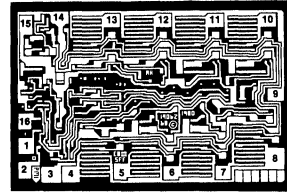
- "OFF" isolation is measured by driving channel 8 with ALL channels "OFF".
 $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, $f = 500kHz$. C_{DS} is computed from the OFF isolation measurement.
- Sample tested.
- Guaranteed by leakage current and R_{ON} tests.
- Leakage tests are performed only on military temperature grades at 125°C.



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



MUX-08



MUX-24

**DIE SIZE 0.090 × 0.061 inch, 5490 sq. mils
(2.286 × 1.549 mm, 3542 sq. mm)**

- 1. A0
- 2. ENABLE
- 3. V- (SUBSTRATE)
- 4. S1
- 5. S2
- 6. S3
- 7. S4
- 8. DRAIN
- 9. S8
- 10. S7
- 11. S6
- 12. S5
- 13. V+
- 14. GND
- 15. A2
- 16. A1

- 1. A0
- 2. ENABLE
- 3. V- (SUBSTRATE)
- 4. S1 A
- 5. S2 A
- 6. S3 A
- 7. S4 A
- 8. DRAIN A
- 9. DRAIN B
- 10. S4 B
- 11. S3 B
- 12. S2 B
- 13. S1 B
- 14. V+
- 15. GND
- 16. A1

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at V+ = 15V, V- = -15V, TA = 25°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT LIMIT	MUX-08/ MUX-24N LIMIT	MUX-08/ MUX-24G LIMIT	UNITS
"ON" Resistance	R _{ON}	V _S = 0V, I _S = 200µA T _A = 125° C	300 400	300 —	400 —	Ω MAX
Digital "1" Input Voltage	V _{INH}	(Note 2)	2	2	2	V MIN
Digital "0" Input Voltage	V _{INL}	(Note 2)	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I _{INL}	V _{IN} = 0.4V T _A = 125° C	10 20	10 —	10 —	µA MAX
Digital "0" Enable Current	I _{INL(EN)}	V _{IN} = 0.4V T _A = 125° C	10 20	10 —	10 —	µA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I ⁺	T _A = 125° C	12 15	12 —	12 —	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I ⁻	T _A = 125° C	3.8 5	3.8 —	3.8 —	mA MAX
Analog Input Range	V _A	(Note 2)	±10	±10	±10	V MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 15V, V- = -15V and T_A = 25° C for MUX-08/24N & G, T_A = 125° C for MUX-08/24NT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT TYPICAL	MUX-08/ MUX-24N TYPICAL	MUX-08/ MUX-24G TYPICAL	UNITS
Switching Time	t _{TRAN}	(Note 1)	1.7	1.3	2.1	µs
Output Settling Time	t _S	10V Step to 0.1% (Note 1)	2.1	1.5	1.9	µs
Break-Before-Make Delay	t _{OPEN}	(Note 1)	0.8	0.8	1.0	µs
Crosstalk	CT	(Note 1)	70	70	70	dB
ΔR _{ON} With Applied Voltage	ΔR _{ON}	-10V ≤ V _S ≤ 10V, I _S = 200µA	2	2	6	%
Leakage Current (Switch "ON")	I _{DI(ON)}	V _D = 10V (Note 1)	20	0.5	0.5	nA
Analog Input Range	V _A		+10.4/-15	+10.4/-15	+10.4/-15	V

NOTES:

- 1. The data shown is extrapolated from measurements made on the packaged devices.
- 2. Guaranteed by leakage current and R_{ON} tests.

ANALOG SWITCHES/MULTIPLEXERS



**MUX-08
LOGIC STATE**

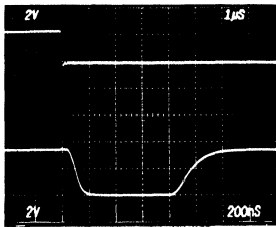
A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

**MUX-24
LOGIC STATE**

A ₁	A ₀	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

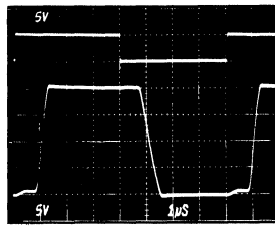
TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

**MUX-08
BREAK-BEFORE-MAKE
SWITCHING**



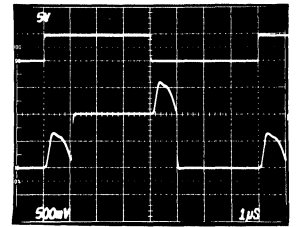
R_L = 1kΩ, C_L = 10pF, V₁, 8 = 10V
VOLTAGE = 2V/DIV
TIME = 200ns/DIV

**MUX-08
LARGE-SIGNAL SWITCHING**



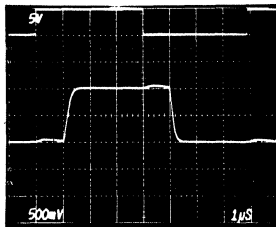
R_L = 1MΩ, C_L = 10pF, V₁ = -10V, V₈ = +10V
VOLTAGE = 5V/DIV
TIME = 1µs/DIV

**MUX-08
SMALL-SIGNAL SWITCHING**



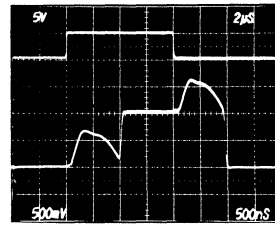
R_L = 1MΩ, C_L = 10pF, V₁ = -500mV, V₈ = +500mV
VOLTAGE = 500mV/DIV
TIME = 1µs/DIV

**MUX-08
SMALL-SIGNAL SWITCHING
WITH FILTERING**



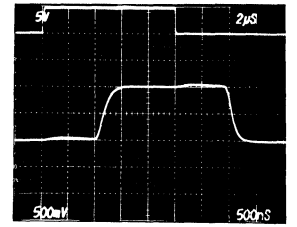
R_L = 1MΩ, C_L = 500pF, V₁ = 500mV, V₈ = +500mV
VOLTAGE = 500mV/DIV
TIME = 1µs/DIV

**MUX-08
SMALL-SIGNAL SWITCHING
WITH 2µs SAMPLE TIME**



R_L = 1MΩ, C_L = 10pF, V₁ = -500mV, V₈ = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

**MUX-08
SMALL-SIGNAL SWITCHING
WITH FILTERING AND
2.5µs SAMPLE TIME**



R_L = 1MΩ, C_L = 500pF, V₁ = -500mV, V₈ = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

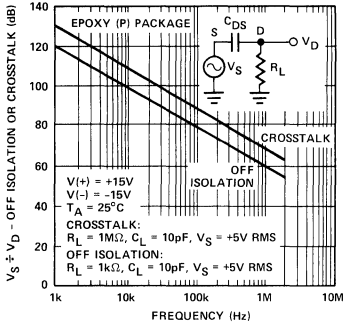
NOTE:

Top waveforms: Digital Input 5V/DIV
Bottom waveforms: Multiplexer Output

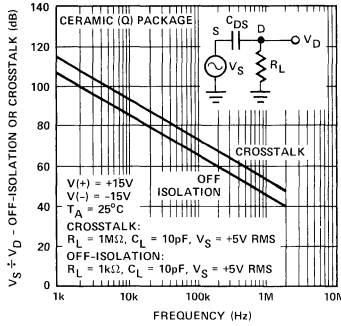


TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

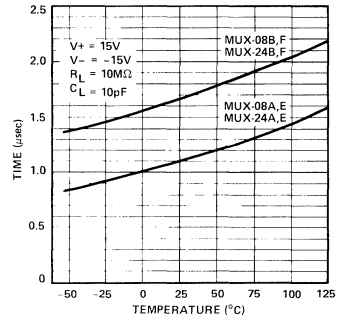
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



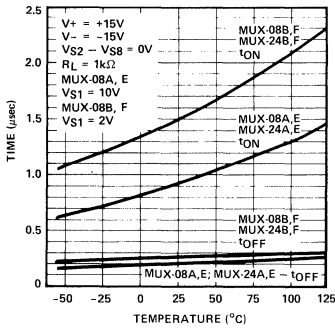
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



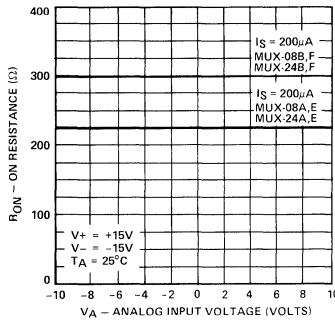
TRANSITION TIMES vs TEMPERATURE



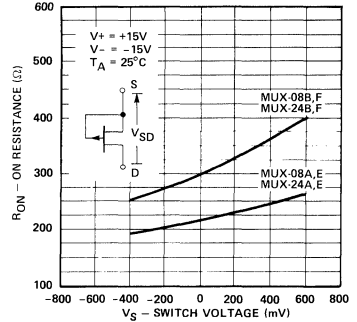
ENABLE DELAY TIMES vs TEMPERATURE



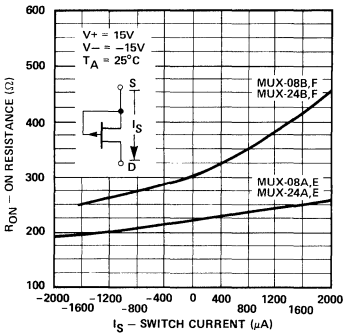
“ON” RESISTANCE (RON) vs ANALOG VOLTAGE (VA)



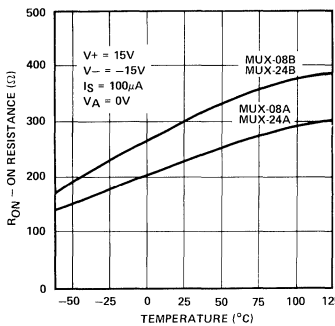
RON vs SWITCH VOLTAGE (VSD)



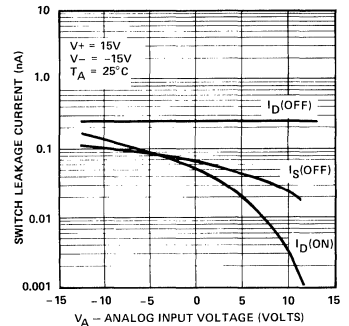
RON vs SWITCH CURRENT (IS)



RON vs TEMPERATURE



SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE

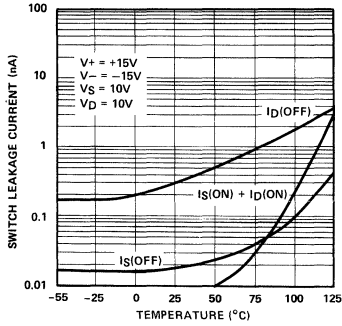


ANALOG SWITCHES/MULTIPLEXERS

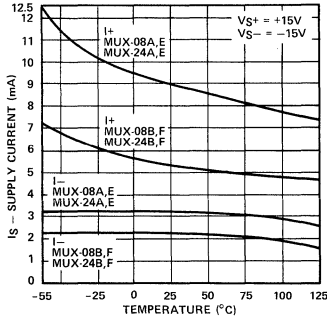


TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

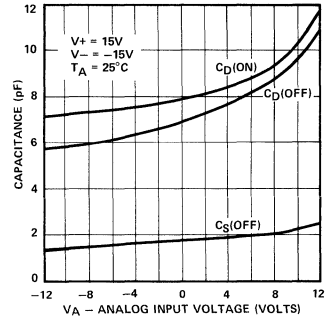
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



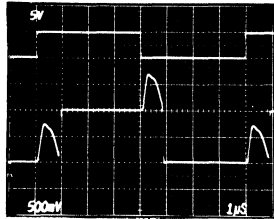
SUPPLY CURRENTS vs TEMPERATURE



MUX-08 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE

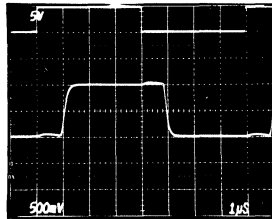


MUX-24 SMALL-SIGNAL SWITCHING



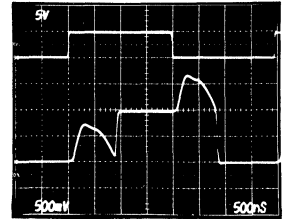
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING



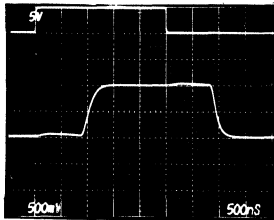
$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME



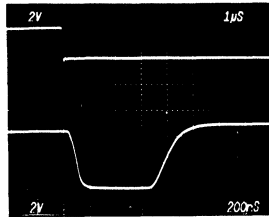
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5µs SAMPLE TIME



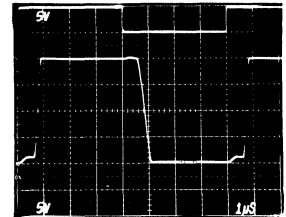
$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 BREAK-BEFORE-MAKE SWITCHING



$R_L = 1k\Omega$, $C_L = 10pF$, $V_1 = 4 = 10V$
 VOLTAGE = 2V/DIV, TIME = 200ns/DIV

MUX-24 LARGE-SIGNAL SWITCHING



$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -10V$, $V_4 = +10V$
 VOLTAGE = 5V/DIV, TIME = 1µs/DIV

NOTE:
 Top waveforms: Digital Input 5V/DIV
 Bottom waveforms: Multiplexer Output

A.C. TEST CIRCUITS

OFF-ISOLATION MEASUREMENT CIRCUIT

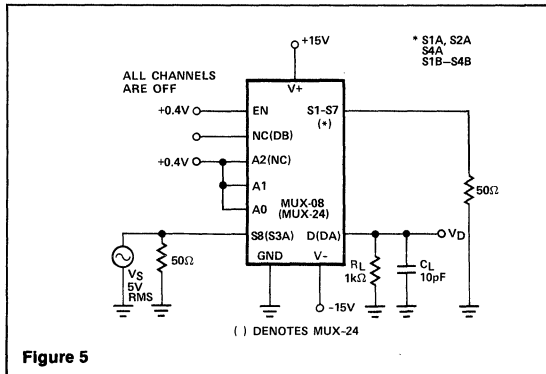
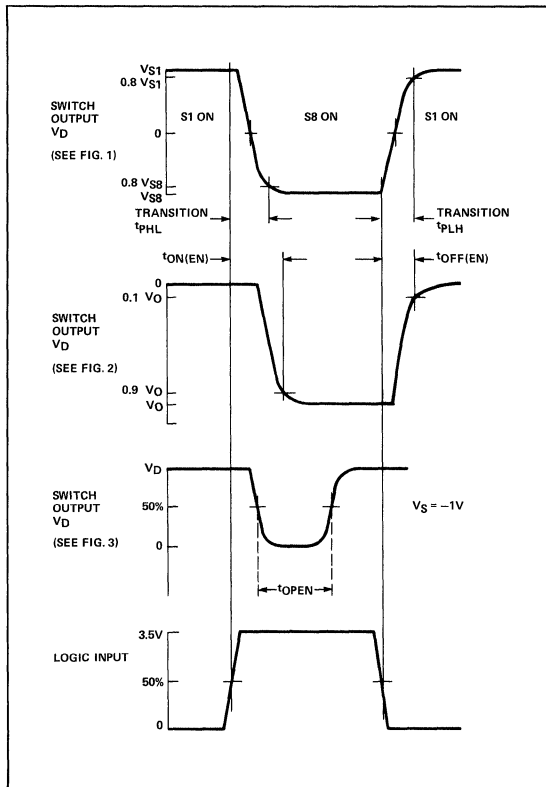


Figure 5

SWITCHING TIME WAVEFORMS



APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing, **special handling as required with CMOS devices, is not necessary to prevent damage to this multiplexer.** Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an "OFF" switch remains greater than its V_p , and prevents that channel from being falsely turned "ON". When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an "ON" switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a $0.01\mu F$ capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_8 = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was $0.3V/\mu s$ which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was $0.7V/\mu s$ which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned "ON" it has a drop of $-20V$ across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS} .

CROSSTALK AND OFF-ISOLATION

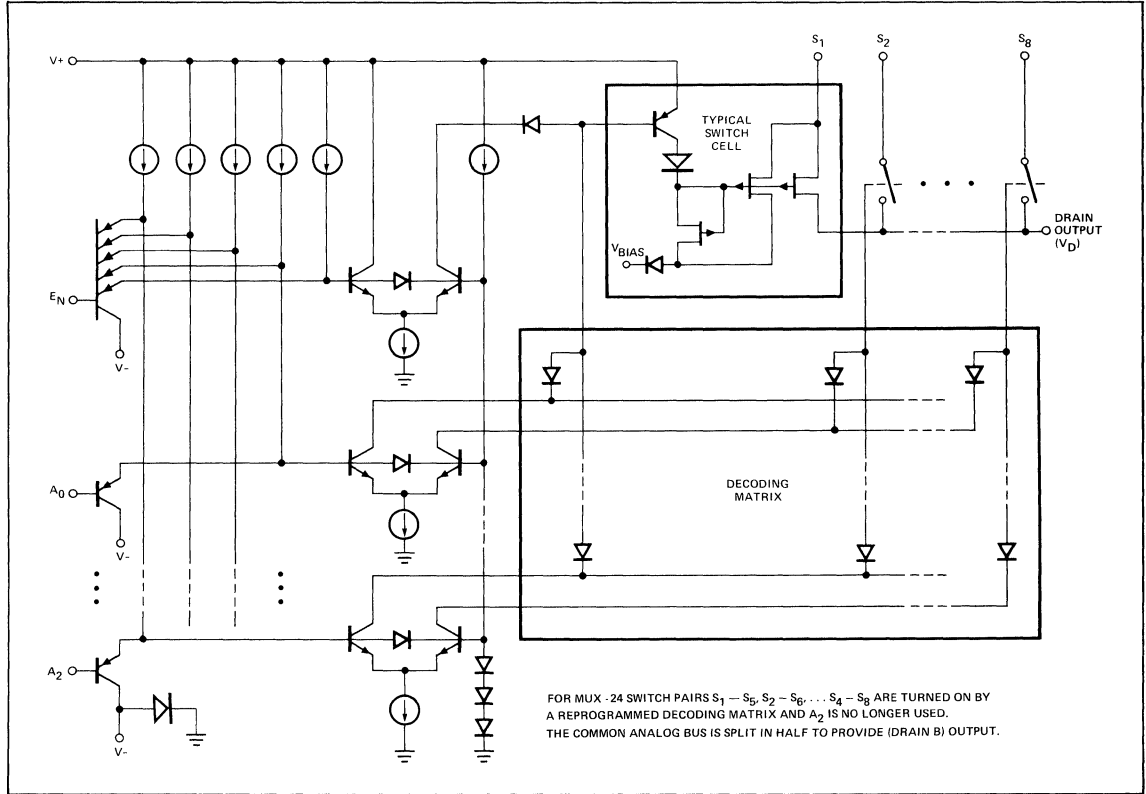
Crosstalk and off-isolation performance is influenced by the type of package selected. Epoxy (P) packaged devices typically exhibit a 12dB improvement in off-isolation ($f = 500kHz$) performance when compared to ceramic (Q) packaged devices. Epoxy packaged devices typically exhibit a 15dB improvement in crosstalk ($f = 500kHz$) performance when compared to ceramic (Q) packaged devices.

SINGLE SUPPLY OPERATION OF JFET MULTIPLEXERS

PMI's JFET multiplexers will operate from a single positive supply voltage with the negative supply pin at ground potential. The analog signal range will include ground.

For complete single supply operation information, refer to application note, AN-32.

SIMPLIFIED MUX-08 SCHEMATIC



The simplified MUX-08/MUX-24 schematic shows that logic trip points are determined by two forward diode drops. An internal clamping diode between V- and ground prevents excessive current flow between V+ and ground in the event that V- becomes open circuit. The decoding matrix is accomplished by a programmed diode array. The switch cell consists of P channel JFET's with appropriate blocking diodes which ruggedizes the circuit's overvoltage and supply loss characteristics.

DIFFERENTIAL MULTIPLEXERS

One characteristic unique to differential multiplexers (MUX-24) is the ability to reject common-mode signals from becoming differential error signals. Common-mode rejection is a parameter which defines the amount of rejection in terms of dB. The MUX-24 exhibits a 106dB at 60Hz and 101dB at 400Hz of CMRR using the test circuit of Figure 6.

CMRR TEST CIRCUIT

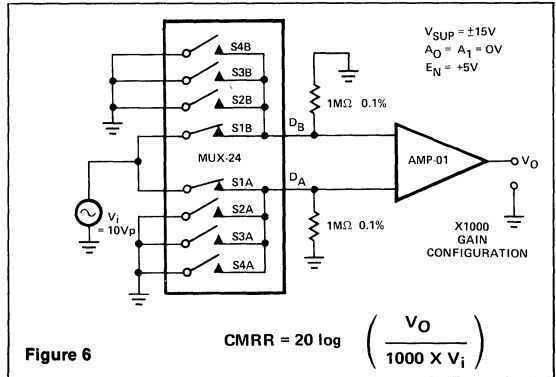
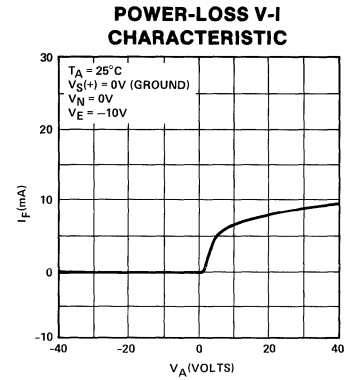
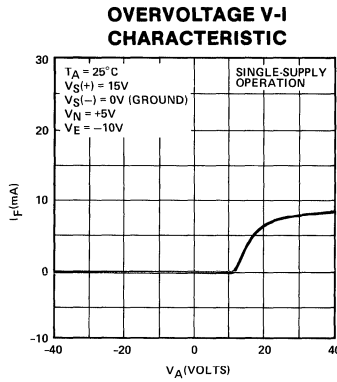
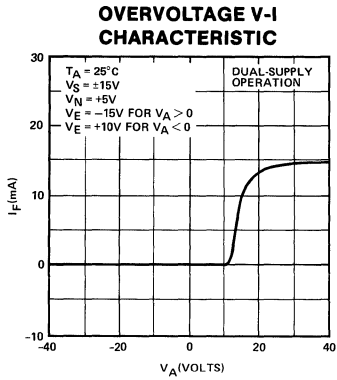
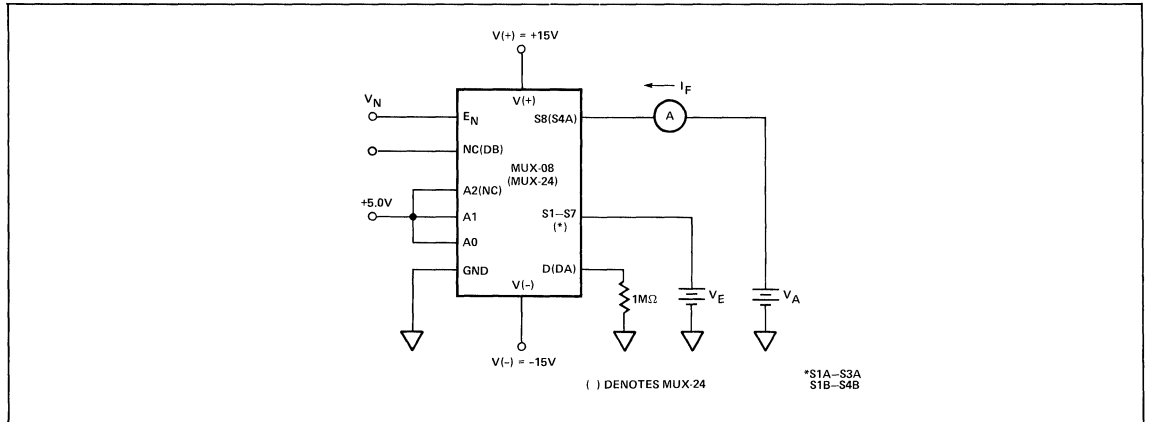


Figure 6

TYPICAL PERFORMANCE CHARACTERISTICS

OVERVOLTAGE/POWER-LOSS MEASUREMENT TEST CIRCUIT




MUX-16/MUX-28

16-CHANNEL/DUAL 8-CHANNEL JFET ANALOG MULTIPLEXERS (OVERVOLTAGE PROTECTED)

Precision Monolithics Inc.

FEATURES

- JFET Switches Rather Than CMOS
- Highly Resistant To Static Discharge Damage
- No SCR Latch-up Problems
- Low "ON" Resistance — 290Ω Typical
- Low Leakage Current
- Digital Inputs Compatible With TTL and CMOS
- Break-Before-Make Action
- 125° C Temperature-Tested Dice Available
- Overvoltage Protected
- Supply Loss Protection
- MUX-16 Pin Compatible With DG506, HI-506A, AD7506
- MUX-28 Pin Compatible With DG507, HI-507A, AD7507

GENERAL DESCRIPTION

The MUX-16 is a monolithic 16-channel analog multiplexer which connects a single output to 1 of the 16 analog inputs depending upon the state of a 4-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package selection function.

The MUX-28 is a monolithic 8-channel differential analog multiplexer configured in a double pole, 8-position (plus OFF) electronic switch array. A 3-bit binary input address connects a pair of independent analog inputs from each 8-channel input section to the corresponding pair of independent analog outputs. Disconnection of both inputs is provided by a logical "0" at the ENABLE input, thereby offering a package select function.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static discharge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors. For single 8-channel and dual 4-channel models, refer to the MUX-08/MUX-24 data sheet.

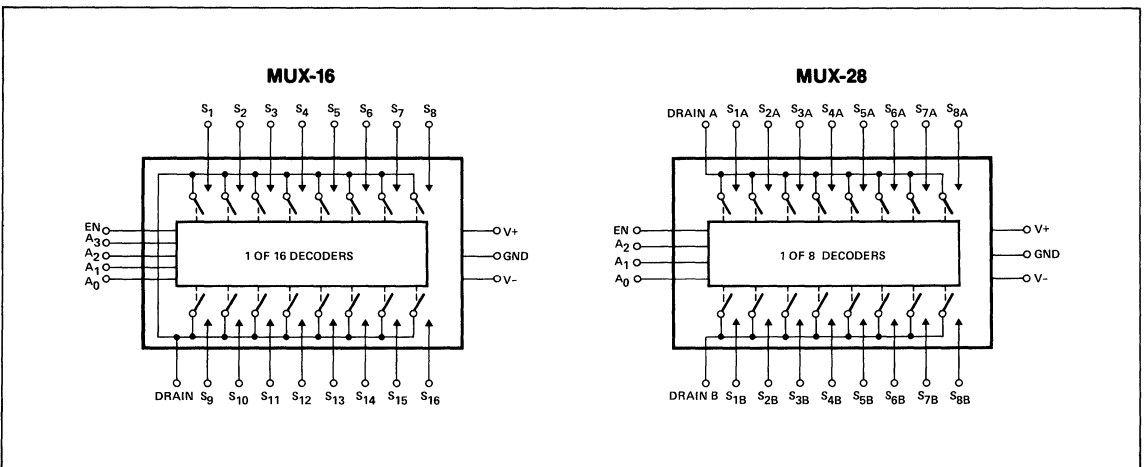
ORDERING INFORMATION†

25° C RESISTANCE	PACKAGE		TEMPERATURE RANGE
	HERMETIC DIP	LCC	
290Ω*	MUX16AT		MIL
290Ω	MUX16ET		IND
400Ω*	MUX16BT	MUX16BTC/883	MIL
400Ω	MUX16FT		IND
290Ω*	MUX28AT		MIL
290Ω	MUX28ET		IND
400Ω*	MUX28BT		MIL
400Ω	MUX28FT		IND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

FUNCTIONAL DIAGRAMS



ANALOG SWITCHES/MULTIPLEXERS

13



ABSOLUTE MAXIMUM RATINGS(Ratings apply to both DICE and packaged parts, unless otherwise noted.)

Operating Temperature Range, MUX-16/28-AT, BT, BTC	-55°C to +125°C	Lead Temperature (Soldering, 60 sec)	300°C
MUX-16/28-ET, FT	-25°C to +85°C	Maximum Junction Temperature	150°C
Dice Junction Temperature (T _J)	-65°C to +150°C	V+ Supply to V- Supply	36V
Storage Temperature Range	-65°C to +150°C	Logic Input Voltage	(V- or -4V) to V+ Supply
Power Dissipation	1000mW	Analog Input Voltage	V- Supply -20V to V+ Supply +20V
		Maximum Current Through Any Pin	25mA

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16A/E MUX-28A/E			MUX-16B/F MUX-28B/F			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
"ON" Resistance	R _{ON}	V _S ≤ 10V, I _S ≤ 200μA	—	290	380	—	400	580	Ω	
ΔR _{ON} With Applied Voltage	ΔR _{ON}	-10V ≤ V _S ≤ 10V, I _S = 200μA	—	1.5	5	—	1.5	5	%	
R _{ON} Match Between Switches	R _{ON} Match	V _S = 0V, I _S = 200μA	—	7	15	—	9	20	%	
Analog Voltage Range	V _A	(Note 6)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V	
Source Current (Switch "OFF")	I _S (OFF)	V _S = 10V, V _D = -10V (Note 1)	—	0.01	1	—	0.01	2	nA	
Drain Current (Switch "OFF")	I _D (OFF)	V _S = 10V, V _D = -10V (Note 1)	MUX-16	—	0.2	1	—	0.2	2	nA
			MUX-28	—	0.1	1	—	0.1	2	
Leakage Current (Switch "ON")	I _D (ON) +I _S (ON)	V _D = 10V (Note 1)	MUX-16	—	0.2	1	—	0.2	2	nA
			MUX-28	—	0.1	1	—	0.1	2	
Digital Input Current	I _{IN}	V _{IN} = 0.4V to 15V	—	1	10	—	1	10	μA	
Digital "0" Enable Current	I _{INL} (EN)	V _{EN} = 0.4V	—	4	10	—	4	10	μA	
Digital Input Capacitance	C _{DIG}		—	3	—	—	3	—	pF	
Switching Time	t _{TRAN}	(Notes 2, 5) Figure 1 (Test Circuits)	—	1.7	2.0	—	2.2	2.5	μs	
Output Settling Time	t _S	10V Step to 0.10%	—	1.5	—	—	1.9	—	μs	
		10V Step to 0.05%	—	1.7	—	—	2.1	—		
		10V Step to 0.02%	—	2.5	—	—	2.7	—		
Break-Before-Make Delay	t _{OPEN}	Figure 3	—	0.7	—	—	1	—	μs	
Enable Delay "ON"	t _{ON (EN)}	(Note 5) Figure 2 (Test Circuits)	—	1	2	—	1.2	2.5	μs	
Enable Delay "OFF"	t _{OFF (EN)}	(Note 5) Figure 2 (Test Circuits)	MUX-16	—	0.25	0.5	—	0.25	0.5	μs
			MUX-28	—	0.25	0.5	—	0.25	0.6	
"OFF" Isolation	ISO _{OFF}	(Note 4) Figure 4 (Test Circuits)	—	66	—	—	66	—	dB	
Crosstalk	CT	(Note 3) Figure 5 (Test Circuits)	—	75	—	—	75	—	dB	
Source Capacitance	C _{S (OFF)}	Switch "OFF", V _S = 0V, V _D = 0V	—	2.5	—	—	2.5	—	pF	
Drain Capacitance	C _{D (OFF)}	Switch "OFF", V _S = 0V, V _D = 0V	MUX-16	—	13	—	—	13	—	pF
			MUX-28	—	8	—	—	8	—	
Input to Output Capacitance	C _{DS (OFF)}	(Note 4)	—	0.15	—	—	0.15	—	pF	
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V	MUX-16	—	15	19	—	9	19	mA
			MUX-28	—	15	19	—	8	19	
		V+ = 5V	MUX-16	—	12	—	—	8	—	
			MUX-28	—	12	—	—	7	—	
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I-	V- = -15V	MUX-16	—	5	7	—	3.5	7	mA
			MUX-28	—	5	7	—	3	7	
		V- = -5V	MUX-16	—	4	—	—	3	—	
			MUX-28	—	4	—	—	2.5	—	

NOTES:

- Conditions applied to leakage tests insure worst case leakages.
- R_L = 10MΩ, C_L = 10pF.
- Crosstalk is measured by driving channel 8 (8B*) with channel 7 (7B*) ON.
R_L = 1MΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz.
- "OFF" isolation is measured by driving channel 8 (8B) with ALL channels OFF. R_L = 1kΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz. C_{DS} is computed from the OFF isolation measurement.
- Sample tested.
- Guaranteed by leakage current and R_{ON} tests.

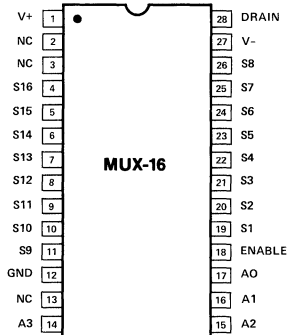


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for MUX-16AT/BT and MUX-28AT/BT; and $-25^\circ C \leq T_A \leq +85^\circ C$ for MUX-16ET/FT and MUX-28ET/FT, unless otherwise noted.

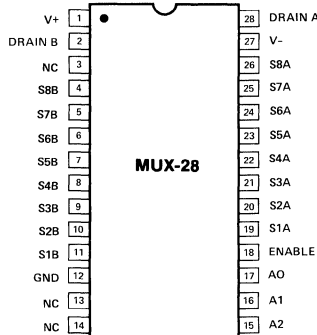
PARAMETER	SYMBOL	CONDITIONS	MUX-16A/E MUX-28A/E			MUX-16B/F MUX-28B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S \leq 10, I_S \leq 200\mu A$	—	—	500	—	—	800	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V, I_S = 200\mu A$	—	2	—	—	5.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V, I_S = 200\mu A$	—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$ (Note 1)	—	—	25	—	—	50	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$ (Note 1)	—	—	75	—	—	250	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+ I_{S(ON)}$	$V_D = 10V$ (Note 1)	—	—	75	—	—	250	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.7	—	—	0.7	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to $15V$	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA
Positive Supply Current	I_+	All Digital Inputs Logic "0" or "1"	—	—	24	—	—	24	mA
Negative Supply Current	I_-	All Digital Inputs Logic "0" or "1"	—	—	8.2	—	—	8.2	mA

PIN CONNECTIONS & TRUTH TABLES

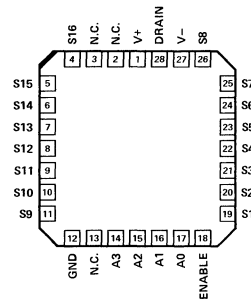
28-PIN HERMETIC DUAL-IN-LINE (T-Suffix)



MUX-16



MUX-28



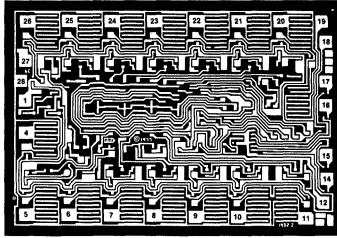
**MUX-16BTC/883
LCC
(TC-Suffix)**

MUX-16					MUX-28						
A ₃	A ₂	A ₁	A ₀	EN	"ON" CHANNEL	A ₃	A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	X	L	NONE	H	L	L	L	H	9
L	L	L	L	H	1	H	L	L	H	H	10
L	L	L	H	H	2	H	L	H	L	H	11
L	L	H	L	H	3	H	L	H	H	H	12
L	L	H	H	H	4	H	H	L	L	H	13
L	H	L	L	H	5	H	H	L	H	H	14
L	H	L	H	H	6	H	H	H	L	H	15
L	H	H	L	H	7	H	H	H	H	H	16
L	H	H	H	H	8						

MUX-28				
A ₂	A ₁	A ₀	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

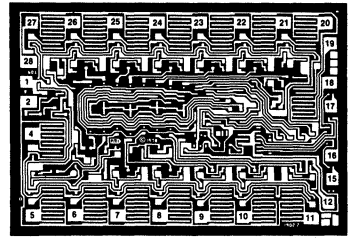


DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



MUX-16

MUX-28



DIE SIZE 0.109 × 0.075 inch, 8175 sq. mils
(2.769 × 1.905 mm, 5274 sq. mm)

For additional DICE information refer to
1986 Data Book, Section 2.

- 1. POSITIVE SUPPLY
- 4. SOURCE 16 (S16)
- 5. SOURCE 15 (S15)
- 6. SOURCE 14 (S14)
- 7. SOURCE 13 (S13)
- 8. SOURCE 12 (S12)
- 9. SOURCE 11 (S11)
- 10. SOURCE 10 (S10)
- 11. SOURCE 9 (S9)
- 12. GROUND
- 14. ADDRESS BIT 3 (A3)
- 15. ADDRESS BIT 2 (A2)
- 16. ADDRESS BIT 1 (A1)
- 17. ADDRESS BIT 0 (A0)
- 18. ENABLE
- 19. SOURCE 1 (S1)
- 20. SOURCE 2 (S2)
- 21. SOURCE 3 (S3)
- 22. SOURCE 4 (S4)
- 23. SOURCE 5 (S5)
- 24. SOURCE 6 (S6)
- 25. SOURCE 7 (S7)
- 26. SOURCE 8 (S8)
- 27. NEGATIVE SUPPLY (SUBSTRATE)
- 28. DRAIN

- 1. POSITIVE SUPPLY
- 2. DRAIN B
- 4. SOURCE 8 (S8B)
- 5. SOURCE 7 (S7B)
- 6. SOURCE 6 (S6B)
- 7. SOURCE 5 (S5B)
- 8. SOURCE 4 (S4B)
- 9. SOURCE 3 (S3B)
- 10. SOURCE 2 (S2B)
- 11. SOURCE 1 (S1B)
- 12. GROUND
- 15. ADDRESS BIT 2 (A2)
- 16. ADDRESS BIT 1 (A1)
- 17. ADDRESS BIT 0 (A0)
- 18. ENABLE
- 19. SOURCE 1 (S1A)
- 20. SOURCE 2 (S2A)
- 21. SOURCE 3 (S3A)
- 22. SOURCE 4 (S4A)
- 23. SOURCE 5 (S5A)
- 24. SOURCE 6 (S6A)
- 25. SOURCE 7 (S7A)
- 26. SOURCE 8 (S8A)
- 27. NEGATIVE SUPPLY (SUBSTRATE)
- 28. DRAIN A

WAFER TEST LIMITS at $V_+ = 15V$, $V_- = -15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT LIMIT	MUX-16/ MUX-28N LIMIT	MUX-16/ MUX-28GT LIMIT	MUX-16/ MUX-28G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 200\mu A$	380 540	380 —	580 800	580 —	Ω MAX
Digital "1" Input Voltage	V_{INH}		2	2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}		0.8	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.4V$	20	10	20	10	μA MAX
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	20	10	20	10	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I+		24	19	24	19	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I-		8.2	7	8.2	7	mA MAX
Analog Input Range	V_A	(Note 3)	± 10	± 10	± 10	± 10	V MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS for $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$, unless otherwise noted.

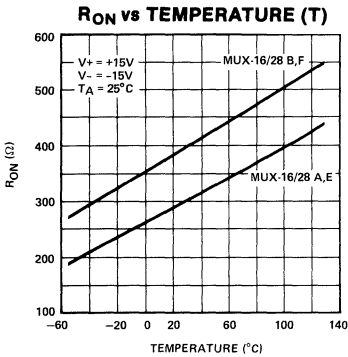
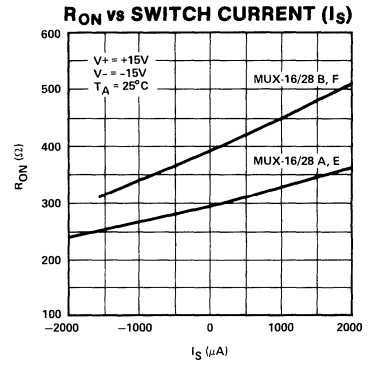
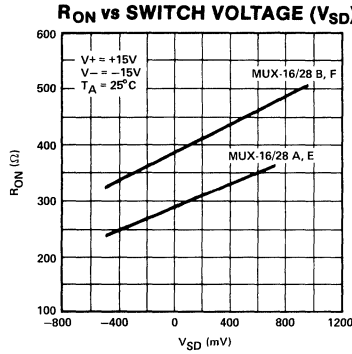
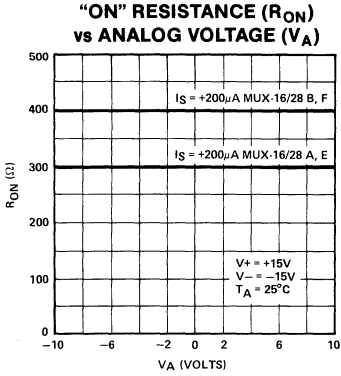
PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT TYPICAL	MUX-16/ MUX-28N TYPICAL	MUX-16/ MUX-28GT TYPICAL	MUX-16/ MUX-28G TYPICAL	UNITS
Switching Time	t_{TRAN}	(Note 2) Figure 1	2	1	2.6	1.5	μs
Output Settling Time	t_S	10V Step to 0.1% (Note 2)	2.5	1.5	2.9	1.9	μs
Break-Before-Make Delay	t_{OPEN}	(Note 2) Figure 3 (Test Circuits)	0.8	0.8	1	1	μs
Crosstalk	CT	(Note 2) Figure 5 (Test Circuits)	70	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$	1.5	1.5	1.5	1.5	%
Leakage Current (Switch "ON")	$I_D(ON)$	$V_D = 10V$ (Note 2)	20	0.2	20	0.2	nA
Analog Input Range	V_A	(Note 3)	+11 -15	+11 -15	+11 -15	+11 -15	V

NOTES:

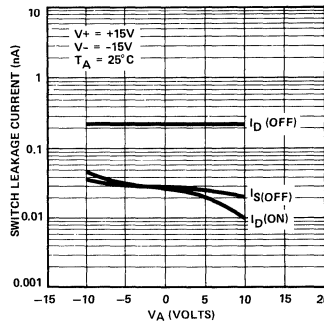
1. For MUX-16/28NT and MUX-16/28GT electrical characteristics apply at 25° C and 125° C, unless otherwise noted.
2. The data shown is extrapolated from measurements made on the packaged devices.
3. Guaranteed by R_{ON} and leakage current tests.



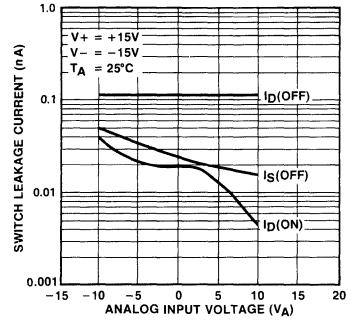
TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)



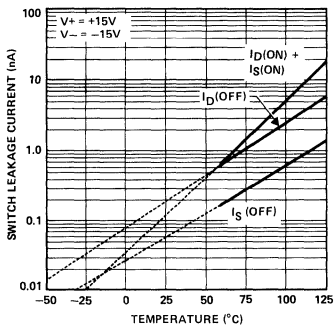
MUX-16 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)



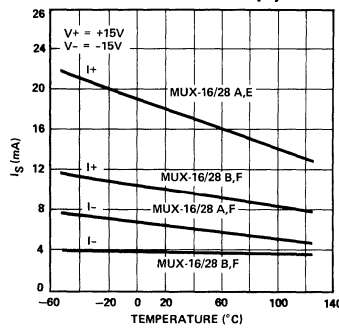
MUX-28 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)



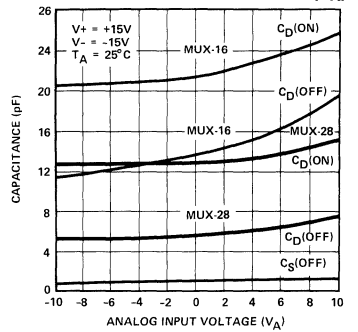
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SUPPLY CURRENTS vs TEMPERATURE (T)



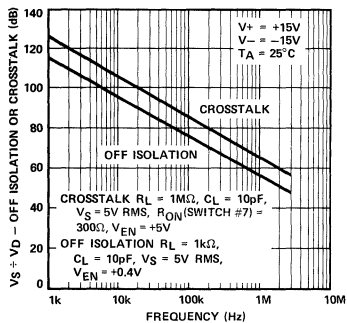
SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE (V_A)



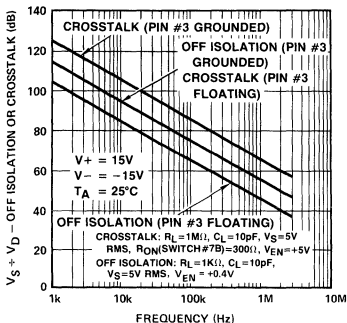
ANALOG SWITCHES/MULTIPLEXERS

TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

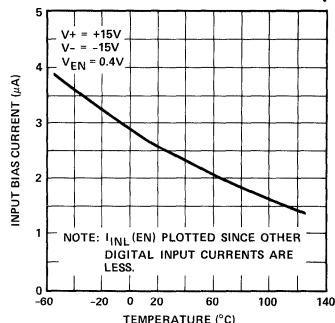
MUX-16
OFF PERFORMANCE OF
CHANNEL 8



MUX-28
OFF PERFORMANCE OF
CHANNEL 8

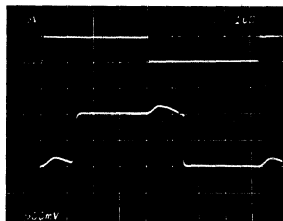


DIGITAL INPUT BIAS
CURRENTS vs TEMPERATURE (T)



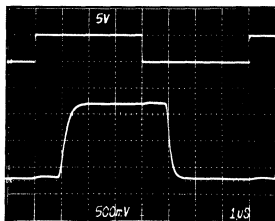
MUX-16 DYNAMIC CHARACTERISTIC CURVES

SMALL-SIGNAL SWITCHING



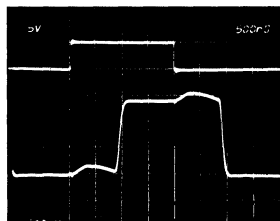
RL = 1MΩ, CL = 10pF, V1 = -500mV, V16 = +500mV

SMALL-SIGNAL SWITCHING WITH FILTERING



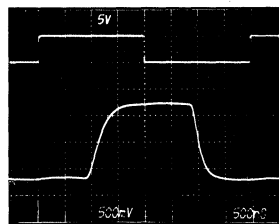
RL = 1MΩ, CL = 500pF, V1 = -500mV, V16 = +500mV

SMALL-SIGNAL SWITCHING WITH 2μs SAMPLE TIME



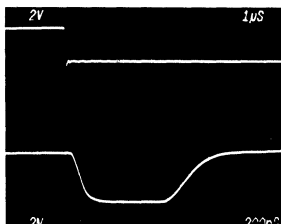
RL = 1MΩ, CL = 10pF, V1 = -700mV, V16 = +700mV

SMALL-SIGNAL SWITCHING WITH FILTERING AND 2μs SAMPLE TIME



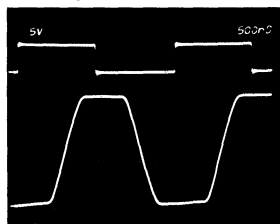
RL = 1MΩ, CL = 500pF, V1 = -700mV, V16 = +700mV

BREAK-BEFORE-MAKE SWITCHING



RL = 1kΩ, CL = 10pF, V1 = V16 = +10V

LARGE-SIGNAL SWITCHING



RL = 1MΩ, CL = 10pF, V1 = -10V, V16 = +10V

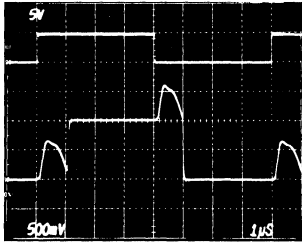
NOTE:

Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplexer Output (VD)



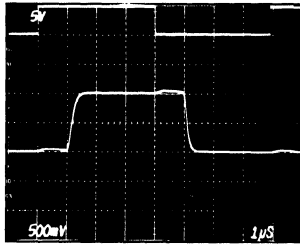
MUX-28 DYNAMIC CHARACTERISTIC CURVES

SMALL-SIGNAL SWITCHING



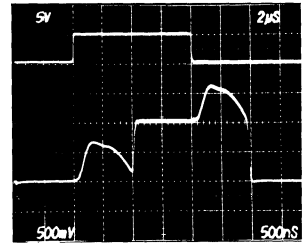
$R_L = 1M\Omega, C_L = 10pF, V_1 = -500mV, V_g = +500mV$

SMALL-SIGNAL SWITCHING WITH FILTERING



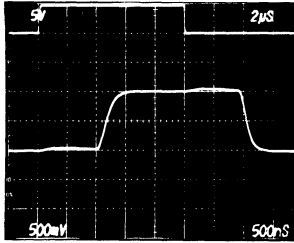
$R_L = 1M\Omega, C_L = 500pF, V_1 = -500mV, V_g = +500mV$

SMALL-SIGNAL SWITCHING WITH 2 μs SAMPLE TIME



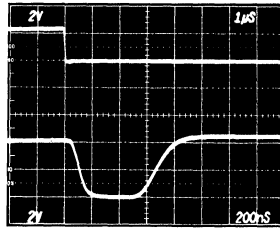
$R_L = 1M\Omega, C_L = 10pF, V_1 = -700mV, V_g = +700mV$

SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5 μs SAMPLE TIME



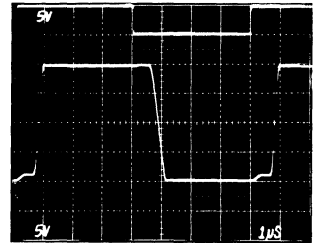
$R_L = 1M\Omega, C_L = 500pF, V_1 = -700mV, V_g = +700mV$

BREAK-BEFORE-MAKE SWITCHING



$R_L = 1K\Omega, C_L = 10pF, V_1 = V_g = +10V$

LARGE-SIGNAL SWITCHING



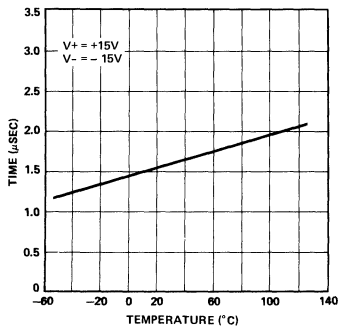
$R_L = 1M\Omega, C_L = 10pF, V_1 = -10V, V_g = +10V$

NOTE:

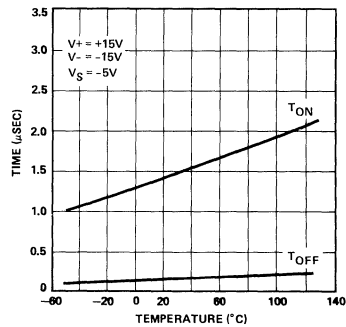
Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplexer Output (V_D)

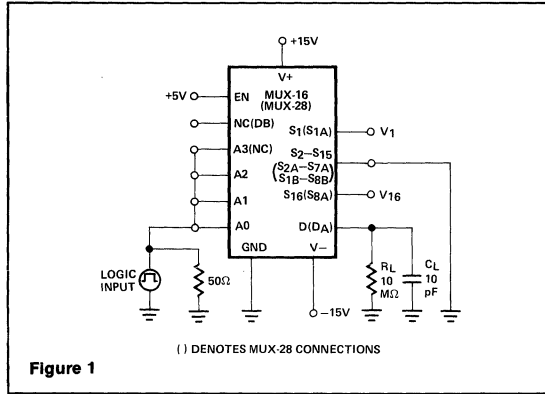
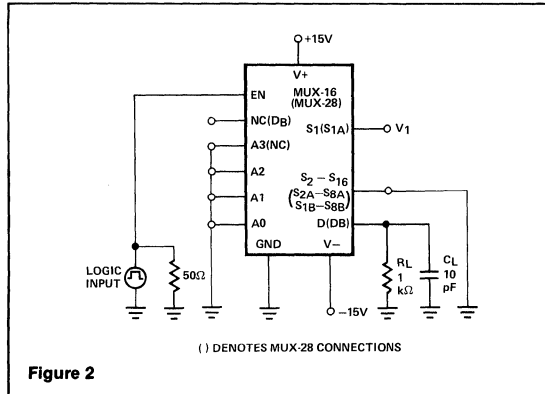
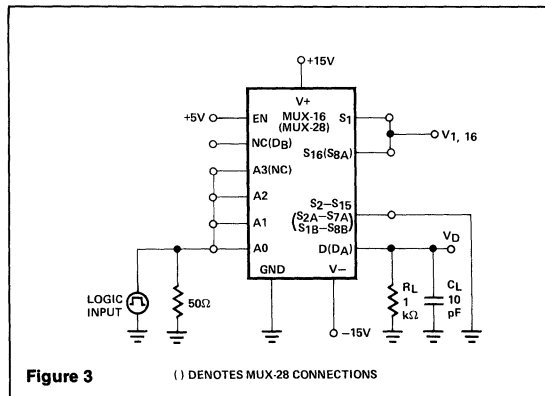
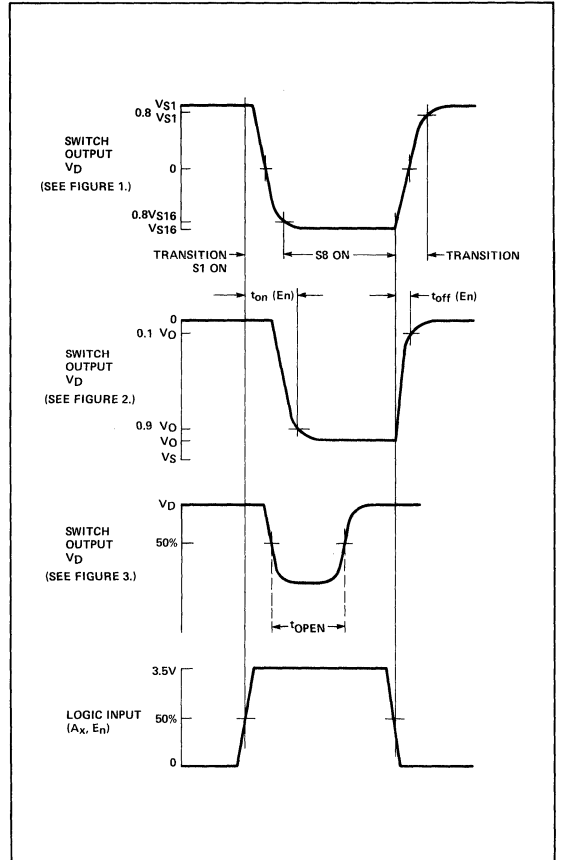
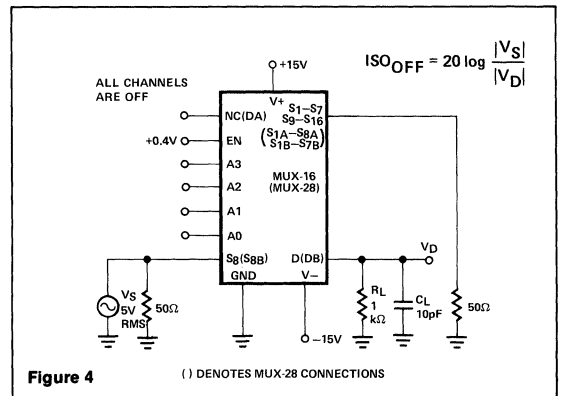
TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

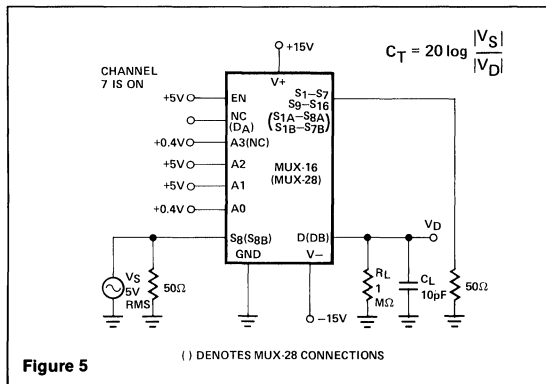
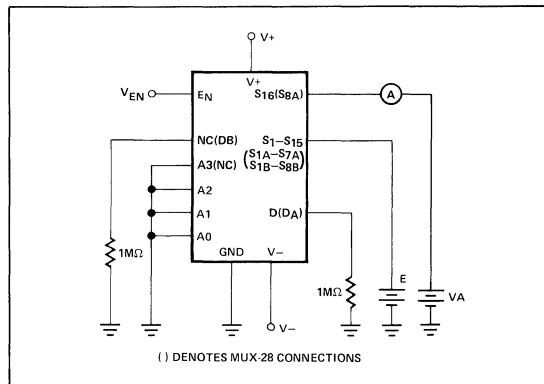
TRANSITION TIME vs TEMPERATURE



ENABLE DELAY TIME vs TEMPERATURE



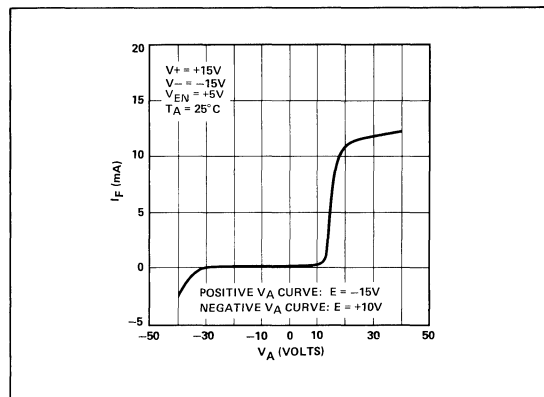
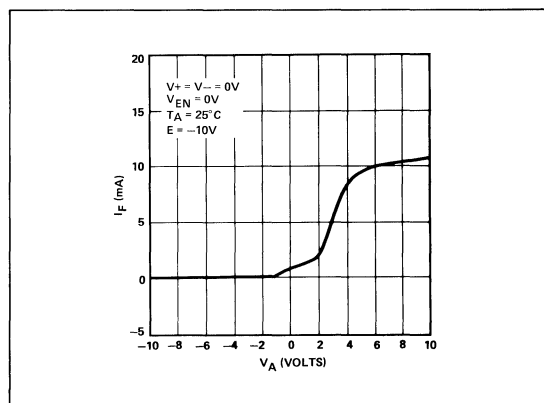
A.C. TEST CIRCUITS
TRANSITION TIME TEST CIRCUIT

Figure 1
ENABLE DELAY TIME TEST CIRCUIT

Figure 2
BREAK-BEFORE-MAKE TEST CIRCUIT

Figure 3
SWITCHING TIME WAVEFORMS

OFF ISOLATION TEST CIRCUIT

Figure 4

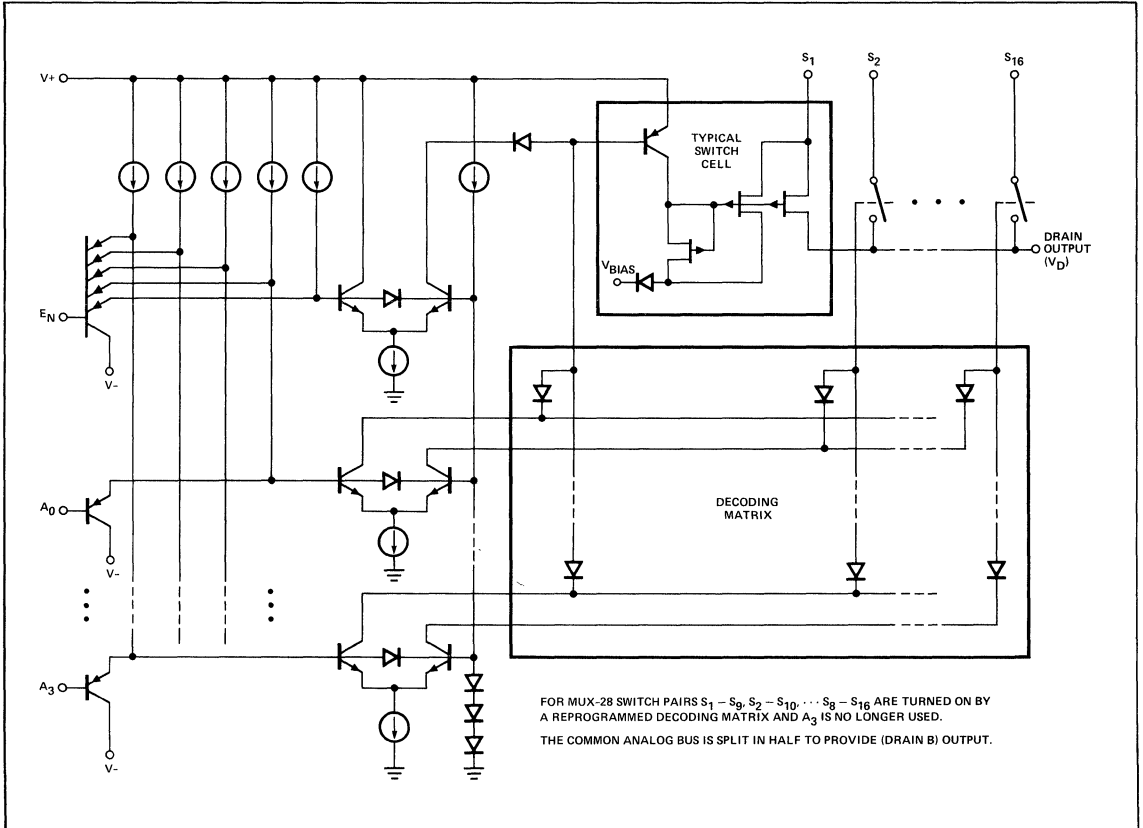
CROSSTALK MEASUREMENT CIRCUIT

Figure 5
OVERVOLTAGE MEASUREMENT TEST CIRCUIT

APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make (B.B.M.) action. The turn-off time is much faster than the turn-on time to guarantee B.B.M. over the full operating temperature and input voltage range. Fabricated with JFET processing rather than CMOS, special handling is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. The overvoltage and supply-loss V-I characteristics shown indicate typical performance when the multiplexer is subjected to abnormal signals. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF FET switch remains greater than its V_p , preventing that channel from being falsely turned ON.

When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a $0.01\mu F$ capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_{16} = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was $0.3V/\mu Sec$ which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was $0.7V/\mu sec$ which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch one (1) is first turned ON it has a drop of $-20V$ across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS} .

OVERVOLTAGE V-I CHARACTERISTIC

SUPPLY-LOSS V-I CHARACTERISTIC


SIMPLIFIED SCHEMATIC (MUX-16)




MUX-88

8-CHANNEL ANALOG MULTIPLEXER FOR PCM CODECS (OVERVOLTAGE PROTECTED)

Precision Monolithics Inc.

FEATURES

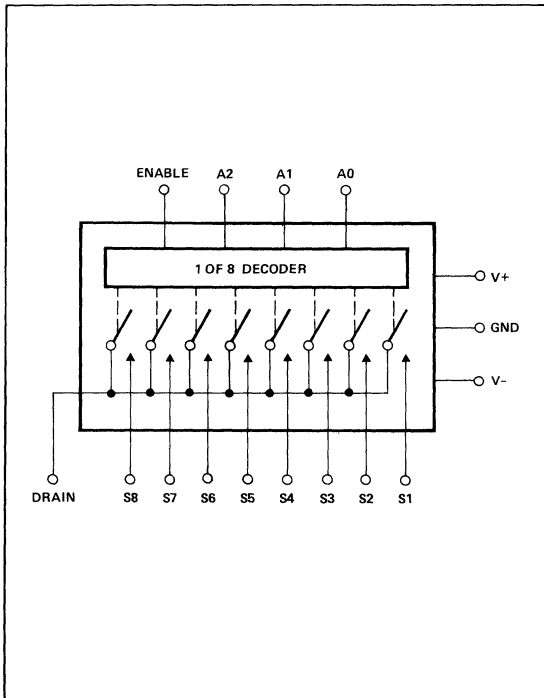
- Compatible with Standards for Noise and Crosstalk in Telephony Systems
- Pin Compatible with DG508, HI-508A, LF11508
- JFET Switches Rather Than CMOS
- Low "ON" Resistance — 220Ω Typical
- Low Output Leakage Current — 100nA Max
- Digital Inputs Compatible with TTL and CMOS
- Input Overvoltage and Supply Loss Protected

ORDERING INFORMATION†

R _{ON}	MODEL	TEMP RANGE
400Ω	MUX-88EQ	IND
520Ω	MUX-88FQ	IND

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

FUNCTIONAL DIAGRAM



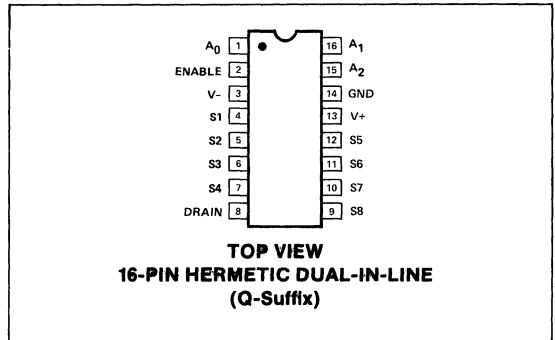
GENERAL DESCRIPTION

The MUX-88 is a monolithic eight-channel analog multiplexer ideally suited to shared-channel PCM CODEC systems. One-of-eight channels is selected upon the decoding of a 3 bit binary address. An enable input (E_N) disables all switches when logic low providing package select. All logic control inputs have true TTL input compatibility eliminating the need for pull-up resistors necessary for some CMOS equivalent products.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, this device offers low "ON" resistance, low leakage, fast settling time and excellent crosstalk isolation (98dB @ 20kHz). These characteristics make this device suitable for meeting system level communication requirements in shared-channel PCM CODECs.

Additional ruggedization results from built-in overvoltage, supply loss, and latch-up free circuit characteristics.

PIN CONNECTIONS



TRUTH TABLE

A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

ANALOG SWITCHES/MULTIPLEXERS

13

**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Operating Temperature Range,

MUX-88EQ, FQ -25°C to $+85^\circ\text{C}$ Storage Temperature Range -65°C to $+150^\circ\text{C}$

Power Dissipation 500mW

Derate above 100°C $10\text{mW}/^\circ\text{C}$ Lead Temperature (Soldering, 60 sec) 300°C

V+ Supply to V- Supply 36V

V+ Supply to Ground 18V

Logic Input Voltage (Note 5) (V- or -4V) to V+

Analog Input Voltage . . . V- Supply -20V to V+ Supply +20V

Maximum Current Through Any Pin 25mA

ELECTRICAL CHARACTERISTICS for $V+ = -15\text{V}$ and $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, unless otherwise noted.

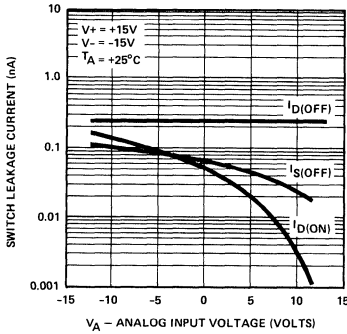
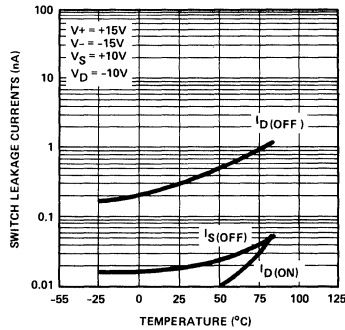
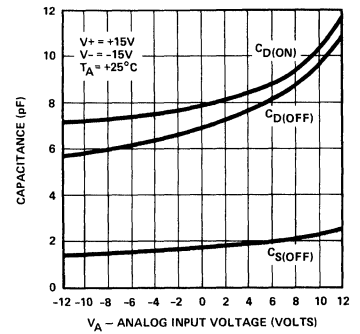
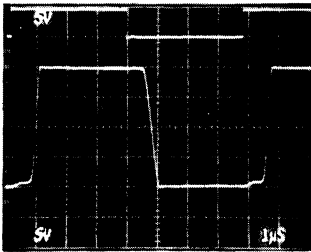
PARAMETER	SYMBOL	CONDITIONS	MUX-88E			MUX-88F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S = 0\text{V}$, $I_S = 200\mu\text{A}$	—	—	400	—	—	520	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10\text{V} \leq V_S \leq 10\text{V}$, $I_S = 200\mu\text{A}$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	$R_{ON\text{ Match}}$	$V_S = 0\text{V}$, $I_S = 200\mu\text{A}$	—	25	—	—	30	—	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$, (Note 1)	—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$, (Note 1)	—	—	100	—	—	100	nA
Leakage Current (Switch "ON")	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10\text{V}$, (Note 1)	—	—	100	—	—	100	nA
Digital "1" Input Voltage	V_{INH}	(Note 5)	—	2	—	—	2	—	V
Digital "0" Input Voltage	V_{INL}	(Note 5)	—	—	0.8	—	—	0.8	V
Digital Input Current	I_{IN}	$V_{IN} = 0.7\text{V}$ to $+5\text{V}$	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.7\text{V}$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0"	—	—	15	—	—	15	mA
Negative Supply Current	I-	All Digital Inputs Logic "0"	—	—	5	—	—	5	mA
Switching Time	t_{TRAN}	Figure 1, (Note 2)	—	1.8	2.1	—	2.2	2.5	μs
Output Settling Time	t_S	10V Step 0.10%	—	1.3	—	—	1.7	—	μs
		10V Step 0.05%	—	1.5	—	—	1.9	—	μs
		10V Step 0.02%	—	2.3	—	—	2.5	—	μs
Break-Before-Make Delay	t_{OPEN}		—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON(EN)}$		—	1.0	—	—	1.2	—	μs
Enable Delay "OFF"	$t_{OFF(EN)}$		—	0.2	—	—	0.2	—	μs
"OFF" Isolation	ISO_{OFF}	(Note 4)	—	88	—	—	88	—	dB
Crosstalk	CT	(Note 3)	—	98	—	—	98	—	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", $V_S = 0\text{V}$, $V_D = 0\text{V}$	—	2.5	—	—	2.5	—	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", $V_S = 0\text{V}$, $V_D = 0\text{V}$	—	7	—	—	7	—	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	—	0.3	—	—	0.3	—	pF

NOTES:

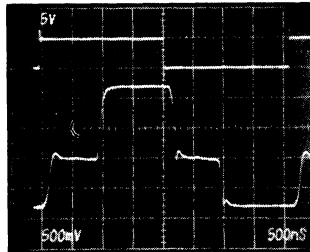
- Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
- Sample tested. The measurement conditions of Figure 1 insure worst case transition time.
- Crosstalk is measured by driving channel 8 with channel 4 ON.
 $R_L = 1\text{M}\Omega$, $C_L = 10\text{pF}$, $V_S = 5\text{V RMS}$, $f = 20\text{kHz}$. (See Figure 2)
- OFF isolation is measured by driving channel 8 with ALL channels OFF.
 $R_L = 1\text{k}\Omega$, $C_L = 10\text{pF}$, $V_S = 5\text{V RMS}$, $f = 20\text{kHz}$. C_{DS} is computed from the OFF isolation measurement.
- Guaranteed by R_{ON} and leakage current testing. For normal operation maximum analog signal voltages should be restricted to less than (V+) -4V.

DICE

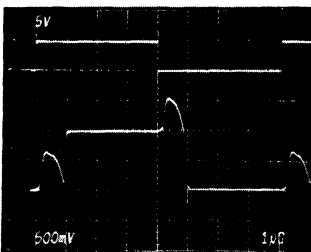
For applicable DICE information see MUX-08/MUX-24 data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE

SWITCH LEAKAGE CURRENTS vs TEMPERATURE

SWITCH CAPACITANCE vs ANALOG INPUT VOLTAGE

LARGE-SIGNAL SWITCHING


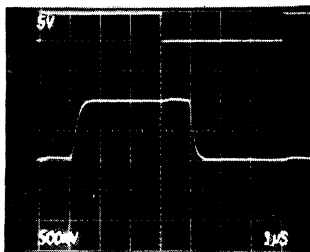
* $R_L = 10M\Omega$, $C_L = 10pF$, $V_1 = -10V$, $V_8 = +10V$
 Voltage = 5V/Div, Time = 1µs/Div, See Transition Time Circuit of Figure 1.

BREAK-BEFORE-MAKE SWITCHING


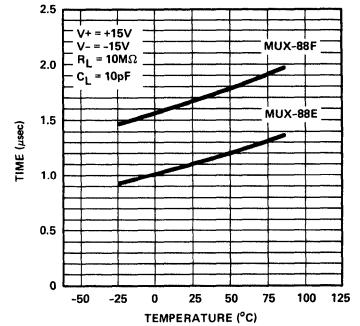
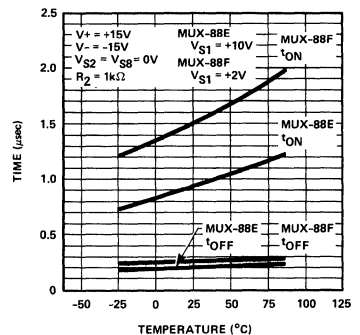
*Voltage = 500mV/Div, Time = 500ns/Div, See Break-Before-Make Circuit of Figure 3.

SMALL-SIGNAL SWITCHING


* $R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$, $V_{S8} = +500mV$
 Voltage = 500mV/Div, Time = 1µs/Div, See Transition Circuit of Figure 1.

SMALL-SIGNAL SWITCHING WITH FILTERING


* $R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$, $V_{S8} = 500mV$
 Voltage = 500mV/Div, Time = 1µs/Div, See Transition Time Circuit of Figure 1.

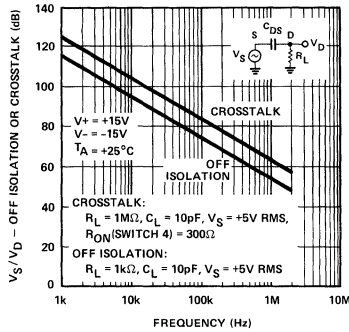
TRANSITION TIMES vs TEMPERATURE

ENABLE DELAY TIME vs TEMPERATURE

NOTE:

*Top Waveforms: Digital Input 5V/Div
 Bottom Waveforms: Multiplex Output

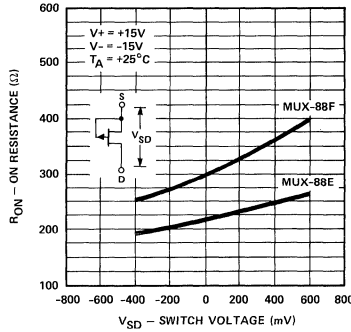


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

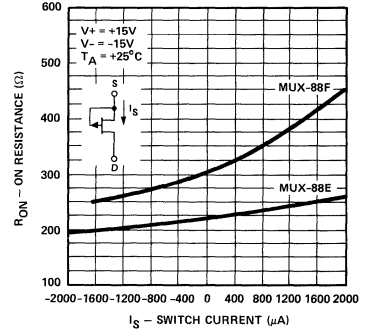
OFF PERFORMANCE OF CHANNEL 8



RON vs SWITCH VOLTAGE (VSD)

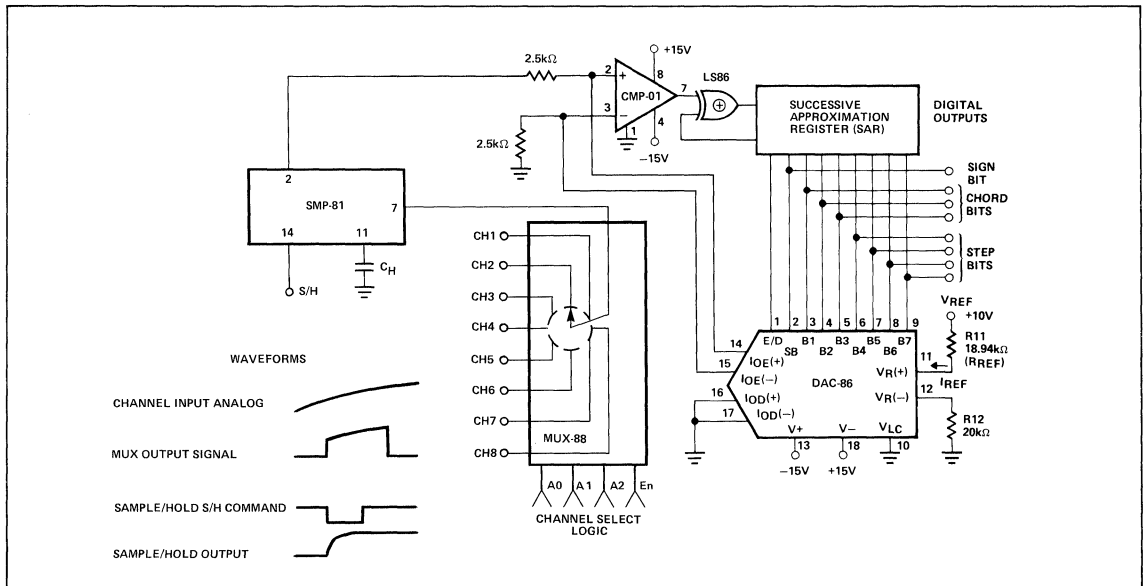


RON vs SWITCH CURRENT (IS)



TYPICAL APPLICATION

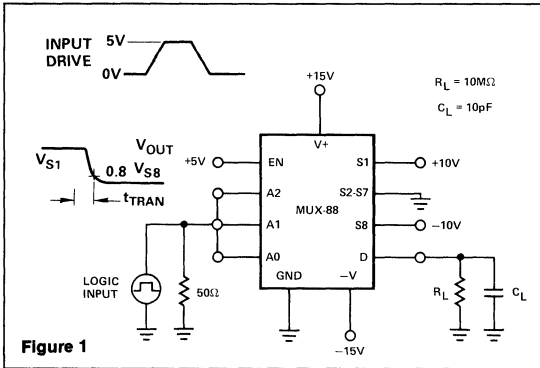
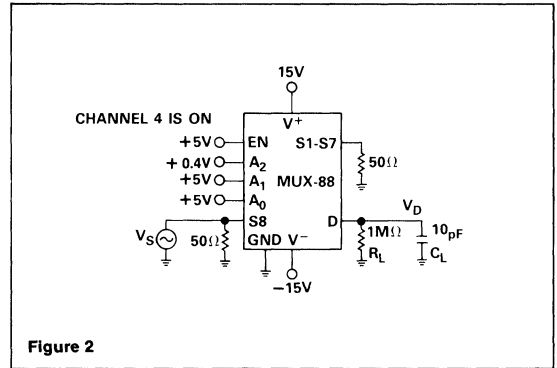
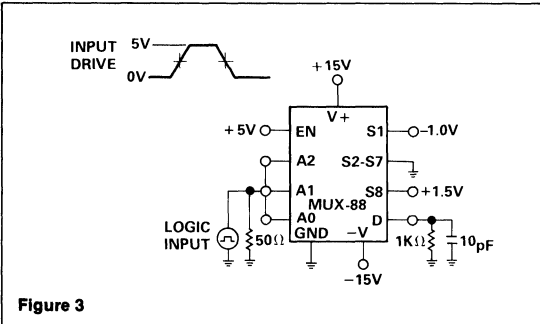
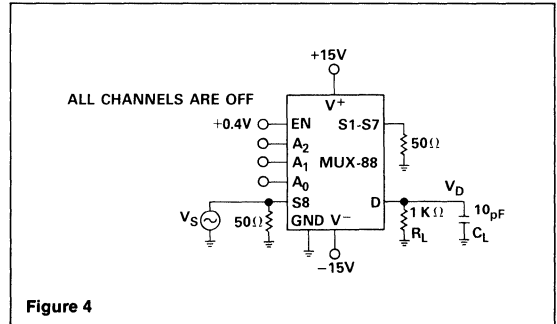
EIGHT-CHANNEL SHARED CODEC PCM ENCODER



CROSSTALK IN PCM SYSTEMS

In PAM or PCM systems crosstalk specifications for components, such as multiplexers, are related to overall system crosstalk specifications in a complex manner. Component specification must, of necessity, refer to the operation of the multiplexer in a non-sampling mode of operation. When rapid sequential sampling takes place, such as would be the case with a typical shared-channel CODEC, crosstalk will be caused by the off isolation properties of the

multiplexer as well as by storage elements on chip and PC card stray capacitance. For example, the capacitance has the effect of conferring the channels and increasing crosstalk. Thus, system crosstalk in a shared-channel PCM CODEC is influenced by multiplexed characteristics as well as PC card layout and the timing relationship between the multiplexer and the sample-hold circuit.

A.C. TEST CIRCUITS
TRANSITION TIME

Figure 1
CROSSTALK MEASUREMENT CIRCUIT

Figure 2
BREAK-BEFORE-MAKE DELAY

Figure 3
OFF ISOLATION MEASUREMENT CIRCUIT

Figure 4
APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal

operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p , and prevents that channel from being falsely turned ON.

When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output load capacitor has increased to $0.01\mu F$ in the Transition Time circuit, Figure 1. With $V_{S1} = -10V$ and $V_{S8} = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was $0.3V/\mu sec$ which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was $0.7V/\mu sec$ which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned ON it has a drop of $-20V$ across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS} .



DMX-88

8-CHANNEL ANALOG DE-MULTIPLEXER (LOW CHARGE TRANSFER)

Precision Monolithics Inc.

FEATURES

- Low Charge Transfer — 18pC Typ
- Compatible with Standards for Noise and Crosstalk in Telephony Systems
- Pin Compatible with DG508, HI-508A, LF12508/13508
- JFET Switches Rather Than CMOS
- Low "ON" Resistance — 220Ω Typ
- Low Output Leakage Current — 100nA Max
- Digital Inputs Compatible with TTL and CMOS
- No Pull-up Resistors Required to Ensure Break-Before-Make Action with TTL Inputs

ORDERING INFORMATION†

R _{ON}	MODEL	TEMP RANGE
400Ω	DMX88EQ	IND
520Ω	DMX88FQ	IND

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

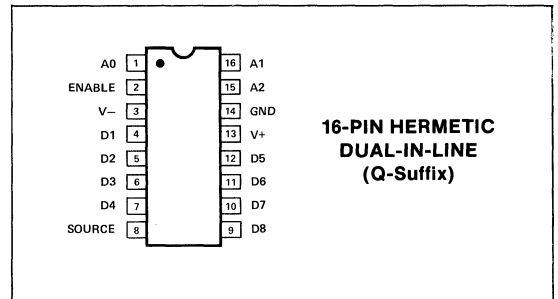
GENERAL DESCRIPTION

The DMX-88 is an 8-channel analog multiplexer optimized for minimum charge transfer, approximately 4 times lower than MUX-88 or MUX-08. This is important when a Multiplexer is terminated in capacitive loads, as in shared-channel PCM decoder systems. Typical crosstalk at 20kHz is 98dB. Monolithic construction makes possible this kind of performance while keeping the price reasonable. The DMX-88 makes use of digital logic to select one-of-eight output

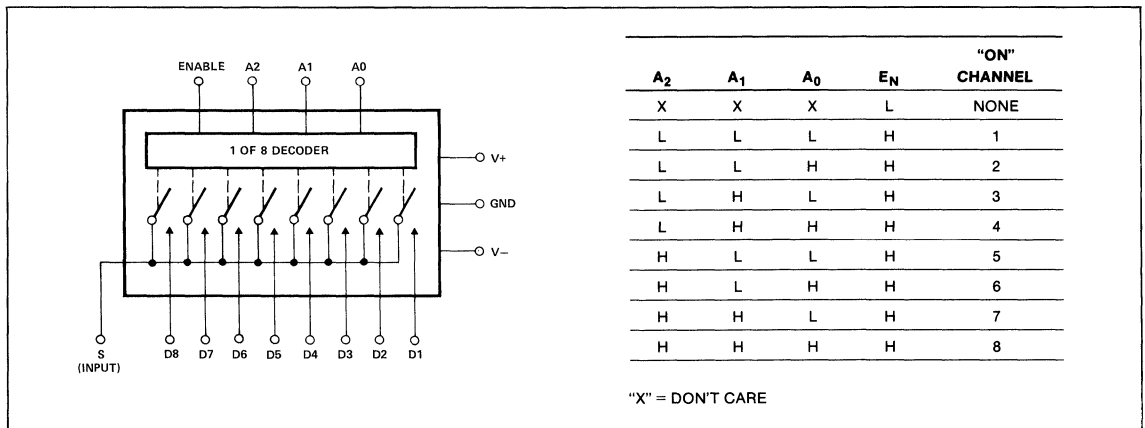
channels. In addition, there is an ENABLE input which permits turning OFF all channels. Using this function permits selection of any given circuit in a system employing multiple devices.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, this device offers low, constant "ON" resistance. In addition the multiplexer has fast settling times and low leakage currents necessary to satisfy the requirements of an 8-channel PCM DECODER. This demultiplexer does not suffer from latch-up and is highly resistant to static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM & TRUTH TABLE



**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, unless otherwise noted.)

Operating Temperature Range,

DMX-88EQ, FQ -25°C to $+85^\circ\text{C}$ Storage Temperature Range -65°C to $+150^\circ\text{C}$

Power Dissipation 500mW

Derate About 100°C 10mW/ $^\circ\text{C}$ Lead Temperature (Soldering, 60 sec) 300°C

V+ Supply to V- Supply 36V

V+ Supply to Ground 18V

Logic Input Voltage (-4V or V-) to V+ Supply

Analog Input Voltage V- Supply -20V to V+ Supply

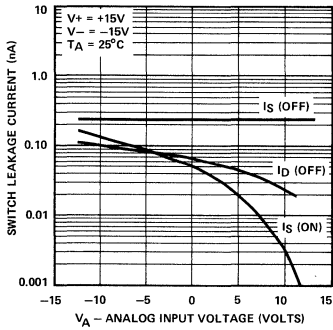
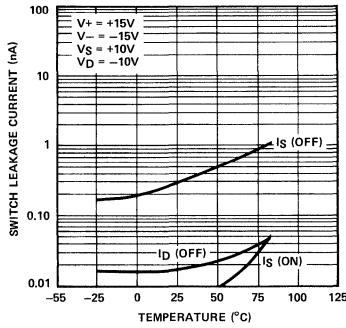
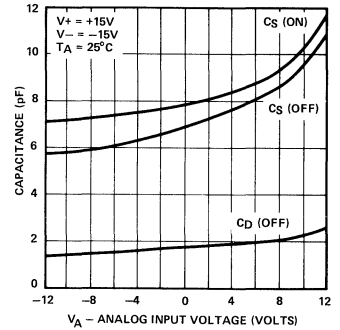
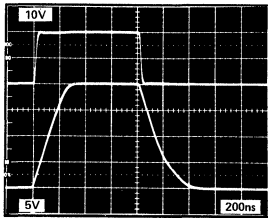
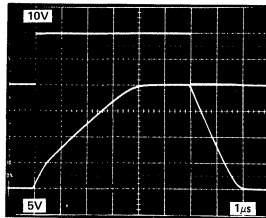
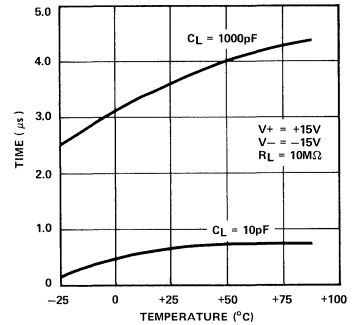
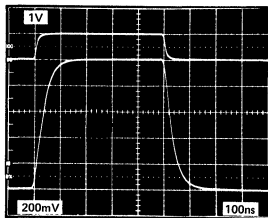
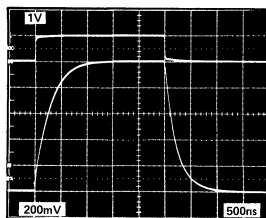
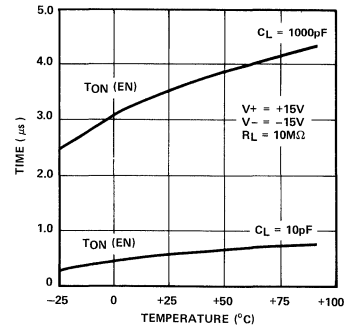
Maximum Current Through Any Pin 25mA

ELECTRICAL CHARACTERISTICS for $V+ = 15\text{V}$, $V- = -15\text{V}$ and $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DMX-88E			DMX-88F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ON Resistance	R_{ON}	$V_S = 0\text{V}$, $I_S = 200\mu\text{A}$	—	—	400	—	—	520	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10\text{V} \leq V_S \leq 10\text{V}$, $I_S = 200\mu\text{A}$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0\text{V}$, $I_S = 200\mu\text{A}$	—	25	—	—	30	—	Ω
Analog Voltage Range	V_A	(Note 5)	10	10.4	—	+10	10.4	—	V
Drain Current (Switch OFF)	$I_{D(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$ (Note 1)	—	—	10	—	—	10	nA
Source Current (Switch OFF)	$I_{S(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$ (Note 1)	—	—	100	—	—	100	nA
Charge Transfer	Q_t	$R_S = 0$, $C_L = 200\text{pF}$ $V_{IN} = 0$ (Note 4)	—	18	25	—	18	25	pC
Leakage Current (Switch ON)	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10\text{V}$ (Note 1)	—	—	100	—	—	100	nA
Digital "1" Input Voltage	V_{INH}	(Note 5)	2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 5)	—	—	0.8	—	—	0.8	V
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.7\text{V}$	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.7\text{V}$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0"	—	—	15	—	—	15	mA
Negative Supply Current	I-	All Digital Inputs Logic "0"	—	—	5	—	—	5	mA
Switching Time	t_{TRAN}	Figure 3 $C_L = 10\text{pF}$	—	0.8	—	—	1.5	—	μs
Output Settling Time	t_S	10V Step 0.10%	—	1.3	—	—	1.7	—	μs
		10V Step 0.05%	—	1.5	—	—	1.9	—	μs
		10V Step 0.02%	—	2.3	—	—	2.5	—	μs
Break-Before-Make Delay	t_{OPEN}		—	0.8	—	—	1	—	μs
Enable Delay ON	$t_{ON(EN)}$	$C_L = 10\text{pF}$ (Figure 1)	—	1	—	—	1.2	—	μs
Enable Delay OFF	$t_{OFF(EN)}$	$C_L = 10\text{pF}$ (Figure 1)	—	0.2	—	—	0.2	—	μs
OFF Isolation	$ISO_{(OFF)}$	(Note 3)	—	88	—	—	88	—	dB
Crosstalk	CT	(Note 2)	—	98	—	—	98	—	dB
Drain Capacitance	$C_{D(OFF)}$	Switch OFF, $V_S = 0\text{V}$, $V_D = 0\text{V}$	—	2.5	—	—	2.5	—	pF
Source Capacitance	$C_{S(OFF)}$	Switch OFF, $V_S = 0\text{V}$, $V_D = 0\text{V}$	—	7	—	—	7	—	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 3)	—	0.3	—	—	0.3	—	pF

NOTES:

- Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an OFF channel to turn ON.
- Crosstalk is measured by driving channel 8 with channel 4 ON.
 $R_L = 1\text{M}\Omega$, $C_L = 10\text{pF}$, $V_S = 5\text{V RMS}$, $f = 20\text{kHz}$. (see figure 2)
- OFF isolation is measured by monitoring channel 8 with ALL channels OFF. $R_L = 1\text{k}\Omega$, $C_L = 10\text{pF}$, $V_S = 5\text{V RMS}$, $f = 20\text{kHz}$. C_{DS} is computed from the OFF isolation measurement. (see figure 4)
- Guaranteed by design.
- Guaranteed by leakage current and R_{ON} tests.

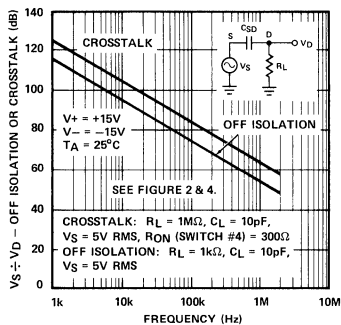
TYPICAL PERFORMANCE CHARACTERISTICS
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE

SWITCH LEAKAGE CURRENTS vs TEMPERATURE

SWITCH CAPACITANCE vs ANALOG INPUT VOLTAGE

LARGE-SIGNAL TRANSIENT RESPONSE (THROUGH A CLOSED SWITCH)

 $R_L = 1M\Omega, C_L = 100pF, V_{IN} = \pm 10V$
LARGE-SIGNAL TRANSIENT RESPONSE (THROUGH A CLOSED SWITCH)

 $R_L = 1M\Omega, C_L = 1000pF, V_{IN} = \pm 10V$
SWITCHING TIME vs TEMPERATURE

SMALL-SIGNAL TRANSIENT RESPONSE (THROUGH A CLOSED SWITCH)

 $R_L = 1M\Omega, C_L = 100pF, V_{IN} = \pm 0.5V$
SMALL-SIGNAL TRANSIENT RESPONSE (THROUGH A CLOSED SWITCH)

 $R_L = 1M\Omega, C_L = 1000pF, V_{IN} = \pm 0.5V$
ENABLE DELAY TIME vs TEMPERATURE

NOTE:

Upper Waveform Photos: Input Voltage on SOURCE

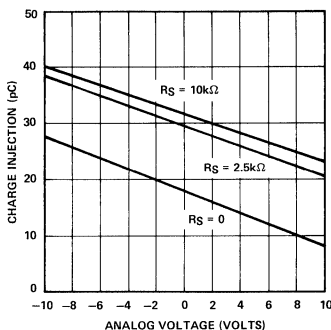
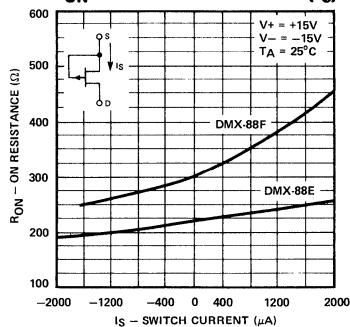
Lower Waveform Photos: Output Voltage on DRAIN

TYPICAL PERFORMANCE CHARACTERISTICS

CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



CHARGE INJECTION vs ANALOG VOLTAGE


 R_{ON} vs SWITCH CURRENT (I_S)


A.C. TEST CIRCUITS

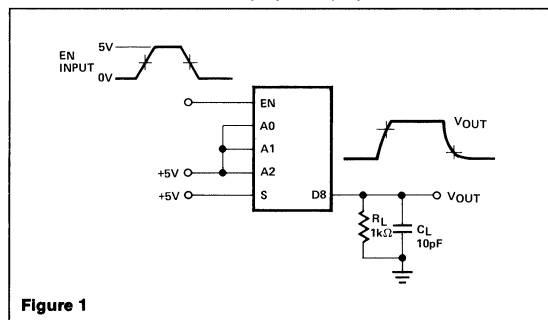
 ENABLE DELAY TIME $t_{ON(EN)}$, $t_{OFF(EN)}$


Figure 1

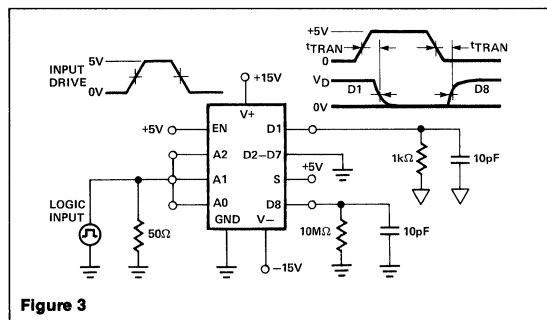
 SWITCHING TIME t_{TRAN}


Figure 3

CROSSTALK MEASUREMENT CIRCUIT

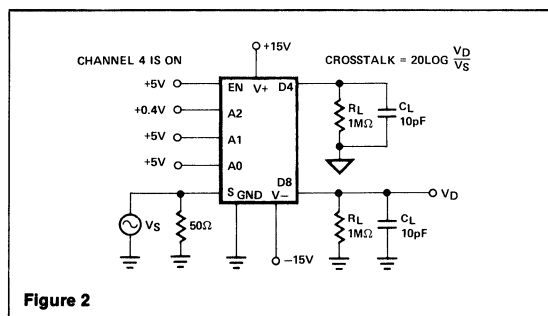


Figure 2

OFF ISOLATION MEASUREMENT CIRCUIT

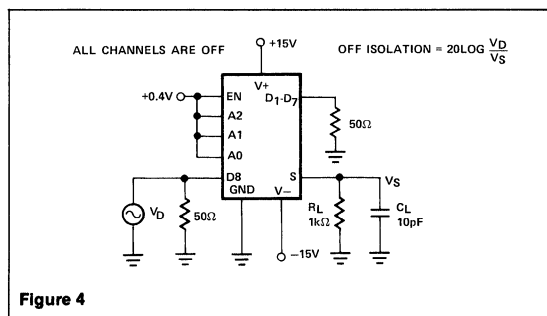
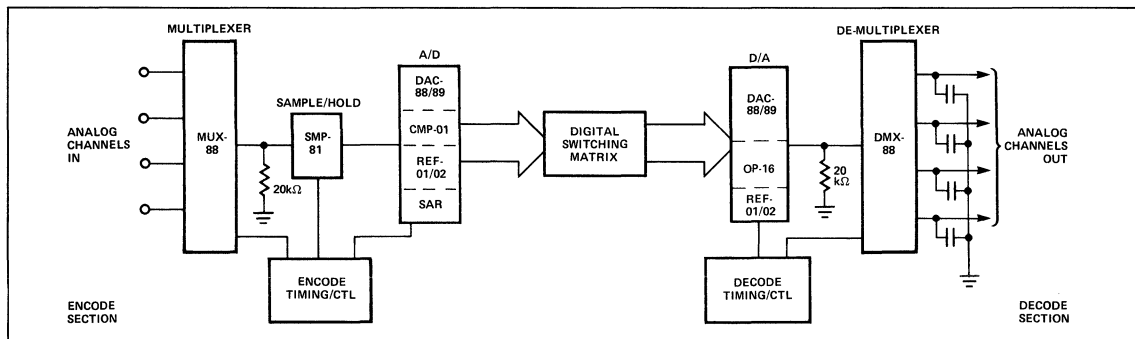


Figure 4

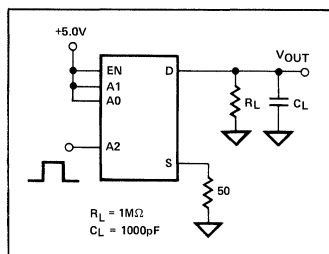
TYPICAL APPLICATION

FOUR-CHANNEL SHARED CHANNEL PCM CODEC

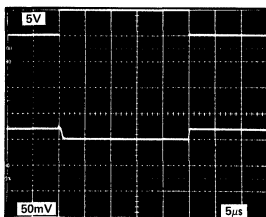


CHARGE TRANSFER

TEST CIRCUIT

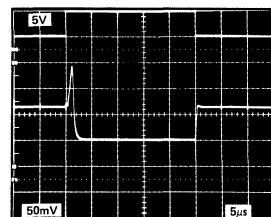


TYPICAL CHARGE TRANSFER OF DMX-88



TOP TRACE : ADDRESS INPUT
BOTTOM TRACE : DRAIN OUTPUT

TYPICAL CHARGE TRANSFER OF CONVENTIONAL JFET SWITCH



TOP TRACE : ADDRESS INPUT
BOTTOM TRACE : DRAIN OUTPUT

APPLICATIONS INFORMATION

These de-multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS devices. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The ON resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p , and prevents that channel from being falsely turned ON.

When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch.

CROSSTALK IN PCM SYSTEMS

In PAM or PCM systems crosstalk specifications for components, such as multiplexers or de-multiplexers, are related to overall system crosstalk specifications in a complex manner. Component specification must, of necessity, refer to the operation of the multiplexer in a non-sampling mode of operation. When rapid sequential sampling takes place, such as would be the case with a typical shared-channel CODEC, crosstalk will be caused by the off isolation properties of the multiplexer as well as by storage elements on chip and PC card stray capacitance. For example, the capacitance has the effect of conferring the channels and increasing crosstalk. Thus, system crosstalk in a shared-channel PCM CODEC is influenced by multiplexer characteristics as well as PC card layout and the timing relationship between the multiplexer and the sample-hold circuit.

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



SAMPLE-AND-HOLD AMPLIFIERS

Precision Monolithics Inc.

14-3 Introduction

14-3 Definitions

14-6 **SMP-10/SMP-11**

Low-Droop-Rate/Accurate Sample-and-Hold Amplifiers

14-15 **SMP-81**

Telecommunications Sample-and-Hold Amplifier



SAMPLE-AND-HOLD AMPLIFIERS

Precision Monolithics Inc.

INTRODUCTION

Sample-and-hold amplifiers “sample” an analog input signal and then “hold” the instantaneous input value upon the command of a logic control signal. Basically the sample-and-hold is an “analog memory” where a capacitor serves as the storage element. Applications in which a time varying input cannot be tolerated require sample-and-hold circuits. A fast successive-approximation analog-to-digital converter is one application. Data acquisition, data distribution, analog delay and telephony require sample-and-hold circuits to “freeze” the analog signal for further signal processing.

PMI sample-and-hold amplifiers are functionally identical to track-and-hold circuits. They continuously track input signals during the sample mode. PMI circuits should not be confused with AC controlled sample-and-holds. When an AC controlled sample-and-hold is commanded to sample, it will take a fast sample and immediately return to the hold mode. It can not continuously track an input signal.

A sample-and-hold circuit consists of an amplifier, switch, and capacitor. Many specifications are similar to those of switches and operational amplifiers — bias currents, voltage gain, and charge injection are examples. These and other specifications pertaining uniquely to sample-and-hold circuits are defined below.

The SMP-10 and SMP-11 are precision sample-and-hold amplifiers with high accuracy, low droop rate, and fast signal acquisition time. These circuits contain a high impedance input buffer, a diode bridge switch, a transconductance or “Super-Charger” circuit to enhance slewing and a high speed output amplifier. The “Super-Charger” is capable of supplementing the capacitor charging current whenever the difference between input and output levels exceeds a given threshold. Settling to final value is under control of currents from the diode bridge, thus minimizing overshoot and instability. The inherent low offset voltage errors and low charge injection allows the residual zero-scale errors to be actively trimmed using PMI’s zener-zapping technology without degrading

temperature performance. “Super Beta” transistors provides the high input-impedance amplifier needed for low droop rate and minimal signal loading.

The SMP-10 and SMP-11 have different droop rate and settling hold mode times specifications.

The SMP-81 is characterized for the sampling requirements found in telecommunications applications.

In addition to precision sample-and-hold amplifiers, two products with related capabilities are available. The GAP-01 general purpose analog processor provides the user with two independently switched transconductance amplifiers, a unity gain buffer and an uncommitted voltage comparator. The GAP-01 is a non-dedicated functional block which has a wide variety of applications. The second device is the PKD-01 monolithic peak detector. This device performs the peak detector function with accuracies approaching those obtainable with high cost hybrid modules at a cost approaching the low cost, low performance discrete designs. Data sheets for the GAP-01 and PKD-01 are located in the SPECIAL FUNCTIONS SECTION of this catalog.

DEFINITIONS

Acquisition Time (t_{aq})— The minimum time for the output voltage to begin tracking the input voltage, to within a specified error band, after the inception of the sample command. By convention, acquisition time is defined for sampling of a DC level. For instance a circuit which is “holding” a 10V output signal, and operating with zero input volts, is switched to the sample mode. The acquisition time is then the time required for the output to decrease to within a $\pm 10\text{mV}$ (0.01%FS) band about ground potential (see timing diagram).

Aperture Jitter (Δt_a) — The maximum amount of deviation in aperture time from sample to sample. Errors resulting from aperture jitter increase

SAMPLE-AND-HOLD AMPLIFIERS

in proportion to the slew rate of the sampled analog input signal. Also called aperture uncertainty time.

Aperture Time (t_{ap}) — The time between the inception of the hold command and the time the circuit output ceases tracking the input signal (see timing diagram).

Change In Hold Step (ΔV_{HS}) — Actual hold step less the hold step measured after sampling $V = 0$. A change in hold step has two components: the first is a function of input voltage, the second is a function of the rise time of the S/H voltage. Note that rise time of S/H voltage $dV_{(S/H)}/dt$ also effects ZERO-SCALE ERROR.

Charge Transfer (Q_t) — The amount of charge transferred to the holding capacitor due to the action of the switch. Charge is transferred to C_H when the circuit is switched to the hold mode. Charge transfer causes a change in output voltage V_{ZS} as defined by the equation:

$$V_{ZS}(V) = \frac{Q_t(pC)}{C_H(pF)}$$

Note that for $Q_t = 5pC$ and $C_H = 5000pF$ offset error = 1mV. The SMP-10/11/81 has been factory nulled for $C_H = 5000pF$. For other values of C_H the zero-scale shift can be calculated from the equation:

$$\Delta V_{ZS}(V) = \frac{Q_t}{C_H} - 1mV$$

Droop Rate (dV_{CH}/dt) — Droop rate dV_{CH}/dt is the rate of change of output voltage while the circuit is in the hold mode. dV_{CH}/dt is a direct function of droop current I_{DR} :

$$\frac{dV_{CH}}{dt} = \frac{I_{DR}}{C_H}$$

where dV_{CH}/dt is expressed in $\mu V/ms$, I_{DR} in nanoamperes and C_H in microfarads (see timing diagram).

Feedthrough Attenuation Ratio (F_A) — Feedthrough attenuation is a measurement of the off-isolation of the analog switch (specified in dB). The parameter is a direct function of feedthrough capacitance.

Full Power Bandwidth (F_p) — The maximum frequency at which rated output voltage E_p can

be supplied without significant distortion. Full power bandwidth F_p is related to slew rate SR by the following equation:

$$F_p = \frac{SR}{2\pi E_p}$$

Using this equation F_p of 160kHz can be computed. This is applicable only for pulsed conditions. Power dissipation limits F_p to 100kHz for C.W. operation.

Gain Error — Voltage difference between input and output voltage measured over a specified voltage range, assuming the ideal gain is unity.

Hold Capacitor Charging Current (I_{CH}) — The current I_{CH} which charges, or discharges, the hold capacitor C_H while the circuit is in the sample mode.

Hold Mode Settling Time (t_{HM}) — The time for all output transients to settle within a specified error band. Measured from the inception of the hold command (see timing diagram).

Hold Step (V_{HS}) — Magnitude of step caused in the output voltage by switching the circuit from sample mode to hold mode. Hold step is sometimes called pedestal error, or sample to hold offset (see timing diagram).

Input Bias Current (I_B) — Input terminal current with input voltage held at zero volts.

Input Resistance (R_{IN}) — AC impedance measured as a ratio of input voltage V_{IN} to input current I_{IN} .

Leakage (Droop) Current (I_{DR}) — The current which flows out of holding capacitor C_H while the circuit is operating in the hold mode. In general droop current I_{DR} is defined positive when its direction is into the C_H pin. This parameter is sometimes called drift current.

Linearity Error — The maximum deviation from an ideal straight line drawn between the output voltage when $V_{IN} = 0$ and the output voltage when $V_{IN} =$ maximum analog voltage, expressed as a percentage of the maximum analog voltage.

Output Resistance (R_o) — An AC change in output voltage as a result of an AC change in load current.

Power Supply Rejection Ratio (PSRR) — The change in output voltage for a change in power supply voltage when the circuit is in the sample mode. The best power supply rejection ratio PSRR is obtained with the power supply voltage changing at a very low rate (DC). For essentially DC conditions PSRR for the hold mode of operation is essentially the same as the PSRR for the sample mode. PSRR is degraded as the frequency of the disturbance increases.

Sample Hold Current Ratio (I_{CH}/I_{DR}) — The ratio of the peak charging current available to the droop current.

Signal Transfer Nonlinearity — The total input to output, hold mode error caused by gain nonlinearity, feedthrough, thermal transient, charge transfer and droop rate. These error terms cannot be corrected by offset and gain adjustments.

Slew Rate (SR) — The maximum possible rate of change of the output voltage when supplying the rated output. For a sample-and-hold circuit, slew rate must be defined with a specified value of holding capacitor C_H . Slew rate can either be measured by operating the circuit in the sample mode and applying a step function to the input,

or by applying an input voltage which differs from the output voltage, with the circuit in the hold mode, then switching to the sample mode and observing the rate of change of the output voltage.

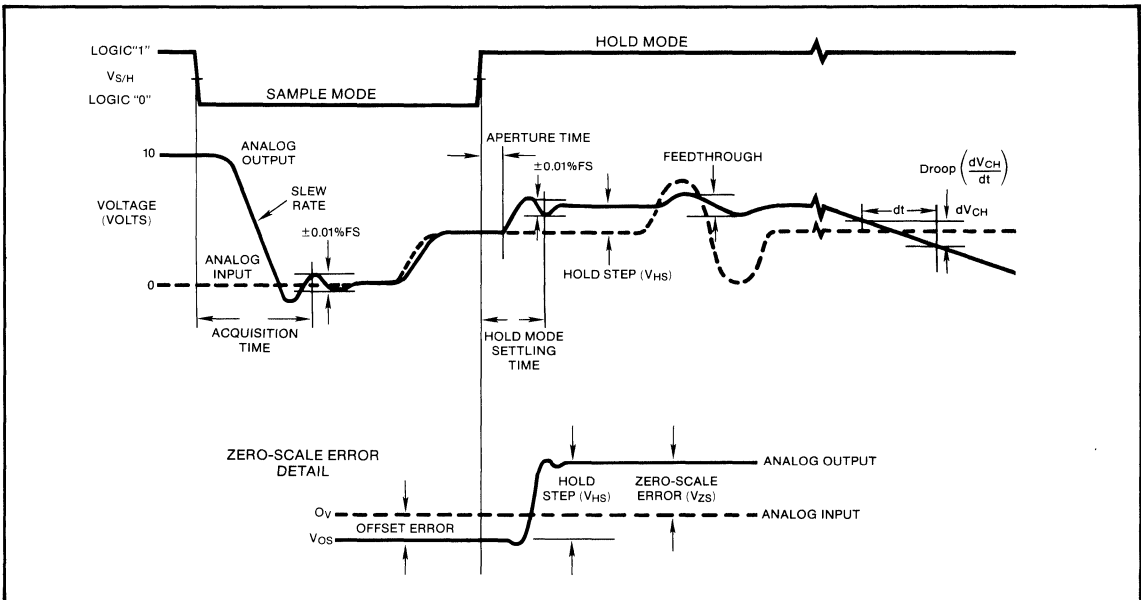
Total Error — The algebraic sum of the following factors:

- i. ZERO-SCALE ERROR
- ii. Gain Error
- iii. Hold Step Change versus $\frac{dV(S/H)}{dt}$
- iv. Hold Step Change versus V_{IN}

Voltage Gain (A_V) — The ratio of the output voltage to the input voltage with the circuit operating in the sample mode.

Zero-Scale Error (V_{ZS}) — The magnitude of the output voltage when the circuit is switched from sample to hold mode while holding the input at zero volts. ZERO-SCALE ERROR V_{ZS} is the algebraic sum of the offset voltage and the charge transfer hold step voltage (see timing diagram). V_{ZS} can be adjusted to zero (see ZERO-SCALE ERROR null adjustment).

TIMING DIAGRAM





SMP-10/SMP-11

LOW-DROOP-RATE/ACCURATE
SAMPLE-AND-HOLD AMPLIFIERS

Precision Monolithics Inc.

FEATURES

SMP-10

- Low Droop Rate 5.0 $\mu\text{V/ms}$
- Low Signal Transfer Nonlinearity 0.005%
- High Sample/Hold Current Ratio 2×10^9

SMP-11

- Low Droop Rate over Temperature 120 $\mu\text{V/ms}$
- High Sample/Hold Current Ratio 1.7×10^8

BOTH SMP-10 AND SMP-11

- Fast Acquisition Time, 10V Step to 0.1% 3.5 μs
- High Slew Rate 10V/ μs
- Low Aperture Time 50ns
- Trimmed for Minimum Zero-Scale Error 0.45mV
- Feedthrough Attenuation Ratio 96dB
- Low Power Dissipation 160mW
- DTL, TTL & CMOS Compatible Logic Input
- HA-2420, HA-2425, SHM-IC-1, and AD583 Socket Compatible

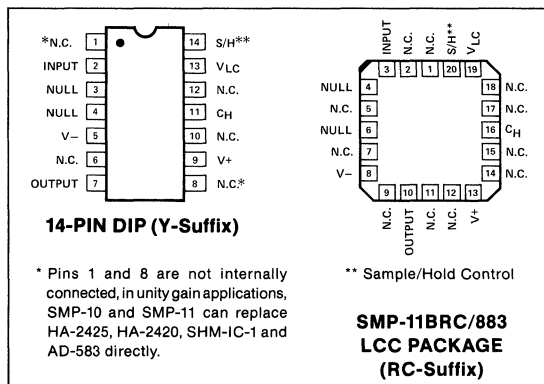
ORDERING INFORMATION†

$T_A = +25^\circ\text{C}$				
V_{ZS} (mV)	DROOP RATE IN $\mu\text{V/ms}$	PACKAGE		OPERATING TEMPERATURE RANGE
		14-PIN DIP HERMETIC	LCC	
1.5	20	SMP10AY*		MIL
3.0	50	SMP10BY*		MIL
1.5	20	SMP10EY		COM
3.0	50	SMP10FY		COM
1.5	200	SMP11AY*		MIL
3.0	500	SMP11BY*	SMP11BRC/883	MIL
1.5	200	SMP11EY		COM
3.0	500	SMP11FY		COM
7.0	900	SMP11GY		COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

PIN CONNECTIONS



GENERAL DESCRIPTION

The SMP-10/11 are precision sample-and-hold amplifiers that provide the high accuracy, the low droop rate and the fast acquisition time required in data acquisition and signal processing systems. Both devices are essentially noninverting unity gain circuits consisting of two very high input impedance buffer amplifiers connected together by a diode bridge switch.

HIGH ACCURACY AND LOW DROOP RATE

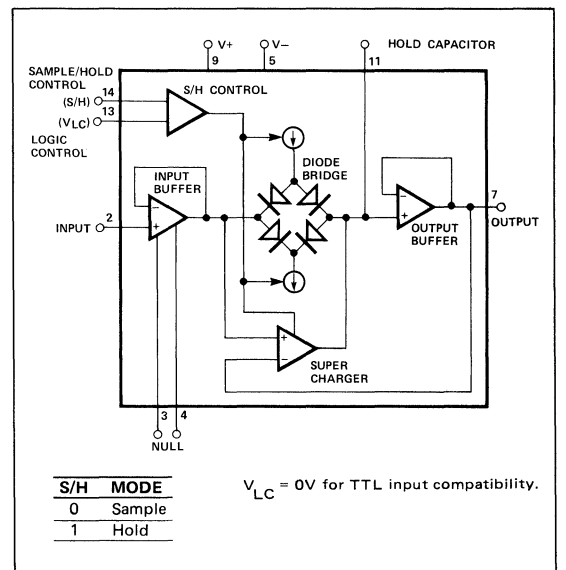
The high input impedance and the low droop rates of the SMP-10 and the SMP-11 are achieved by using bipolar Darlingon circuits and an ion implant process that creates "super beta" transistors.

The output buffer's input stage converts to a super beta Darlington configuration during the hold mode, which results in a very low droop rate with no penalty in acquisition time. The use of bipolar transistors achieves a low change in droop rate over the operating temperature range.

FAST ACQUISITION

A unique super charger provides up to 50mA of charging current to the hold capacitor, which results in smooth, fast charging with minimum noise. As the hold capacitor voltage nears its final value, the low current diode bridge controls the final settling time. This unique combination of linear functions in a monolithic circuit enables the system designer to achieve superior performance.

FUNCTIONAL DIAGRAM



Manufactured under the following patents: 4,109,215 and 4,142,117.

**ABSOLUTE MAXIMUM RATINGS** (Note)

Supply Voltage (V+ minus V-)	36V
Power Dissipation	500mW
Derate Above 100° C	10mW/° C
Input Voltage	Equal to Supply Voltage
Logic and Logic Reference Voltage	Equal to Supply Voltage
Output Short-Circuit Duration	Indefinite
Hold Capacitor Short-Circuit Duration	60 sec
Storage Temperature Range	-65° C to +150° C

Lead Temperature (Soldering, 60 sec)	300° C
Operating Temperature Range	
SMP-10AY, BY	-55° C to +125° C
SMP-10EY, FY	0° C to +70° C
SMP-11AY, BY, BRC	-55° C to +125° C
SMP-11EY, FY, GY	0° C to +70° C
DICE Junction Temperature (T _J)	-65° C to +150° C

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, C_H = 0.005μF, V_{LC} connected to ground, T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10A/E SMP-11A/E			SMP-10B/F SMP-11B/F			SMP-11G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero-Scale Error (Hold Mode)	V _{ZS}	V _{IN} = 0 V _{S/H} = 3.5V, (Note 3)	—	0.45	1.5	—	0.60	3.0	—	1.5	7.0	mV
Input Bias Current	I _B	V _{IN} = 0	—	35	65	—	55	90	—	90	160	nA
Leakage (Droop) Current	I _{DR}	Device Warmed Up (See Note 2)	—	—	0.10	—	—	0.25	—	—	—	nA
Droop Rate	dV _{CH} /dt	Device Warmed Up (See Note 2)	—	5	20	—	5	50	—	—	—	μV/ms
Input Resistance	R _{IN}	See Note 1	2.0	3.0	—	1.4	2.5	—	—	2.0	—	GΩ
Voltage Gain	A _V	Sample Mode V _{IN} = ±10V, R _L = 5kΩ or V _{IN} = ±5V, R _L = 2.5kΩ	0.99963	0.99983	—	0.99953	0.99978	—	0.99940	0.99975	—	V/V
Acquisition Time	t _{aq}	10V step to within 10mV of final value (0.1%)	—	3.5	—	—	3.5	—	—	3.5	—	μs
		10V step to within 1.0mV of final value (0.01%)	—	5.0	—	—	5.0	—	—	5.0	—	μs
Aperture Time	t _{ap}		—	50	—	—	50	—	—	50	—	ns
Hold Mode Settling Time	t _{Hm}	Settling to 1mV of final value.	—	7	—	—	7	—	—	—	—	μs
Charge Transfer	Q _t	V _{IN} = 0 V _{S/H} = 3.5V	—	5	—	—	5	—	—	5	—	pC
Slew Rate	SR	V _{IN} = ±10V R _L = 2.5kΩ	—	10	—	—	10	—	—	10	—	V/μs
Hold Capacitor Charging Current	I _{CH}	V _{IN} - V _{OUT} ≥ ±3V	30	50	—	20	50	—	—	50	—	mA
Sample/Hold Current Ratio	I _{CH} /I _{DR}	SMP-10 SMP-11	3×10 ⁸	2×10 ⁹	—	8×10 ⁷	8×10 ⁸	—	—	—	—	mA/mA
Feedthrough Attenuation Ratio	F _A	Input = 20V _{p-p} 1kHz R _L = 5kΩ, (Note 1)	86	96	—	80	90	—	—	90	—	dB
Full Power Bandwidth	F _P	±10V _{p-p} (Dissipation Limited)	—	100	—	—	100	—	—	100	—	kHz
Input Voltage Range and/or Output Voltage Swing		R _L = 2.5kΩ	±11	±11.5	—	±10.5	±11.5	—	±10.5	±11.5	—	V
Output Resistance	R _O		—	0.15	—	—	0.15	—	—	0.15	—	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode V _S = ±9V to ±18V	82	92	—	77	92	—	72	92	—	dB
Power Consumption (DC)	P _D	Sample Mode V _{IN} = 0	—	160	180	—	170	210	—	180	240	mW

- NOTES:**
- Guaranteed by design.
 - These measurements are made with the devices warmed-up. It can be seen that there is a selection trade off between droop rate and hold mode settling time.
 - Measured 500μs after hold command.



ELECTRICAL CHARACTERISTICS — SMP-10 ONLY at $V_S = \pm 15V$, $C_H = 0.005\mu F$, $V_{LC} = 0V$, $T_A = 25^\circ C$, device fully warmed-up, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10A/E			SMP-10B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Hold Step	V_{HS}	$V_{IN} = 0$	-1.0	+1.5	+4.0	-3.0	+1.5	+6.0	mV
Linearity Error	NL	$V_{IN} = \pm 10V$, $R_L = 5k\Omega$	—	0.005	—	—	0.007	—	% of 10V
Output Noise	$E_{N(RMS)}$	Wideband Noise 100Hz to 100kHz Sample Mode	—	40	—	—	50	—	μV_{RMS}

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10E SMP-11E			SMP-10F SMP-11F			SMP-11G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 3)	—	0.75	2.0	—	1.0	4.0	—	2.7	10	mV
Input Bias Current	I_B	$V_{IN} = 0V$	—	50	90	—	80	140	—	120	250	nA
Leakage (Droop) Current	I_{DR}	Device Warmed Up SMP-10	—	0.05	0.25	—	0.080	0.65	—	—	—	nA
		(See Note 2) SMP-11	—	0.5	1.8	—	0.6	2.8	—	0.7	5	nA
Droop Rate	dV_{CH}/dt	Device Warmed Up SMP-10	—	10	50	—	16	130	—	—	—	$\mu V/ms$
		(See Note 2) SMP-11	—	100	360	—	120	560	—	140	1000	$\mu V/ms$
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99955	0.99976	—	0.99950	0.99972	—	0.99930	0.99970	—	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	80	90	—	75	80	—	70	90	—	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$	—	-1	-2	—	-1	-3	—	-1	-4	μA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$	—	-5	-15	—	-5	-15	—	-5	-15	μA
		Hold Mode $V_{S/H} = 5.0V$	—	0.2	—	—	0.2	—	—	0.2	—	nA
Differential Logic Threshold	V_{TH}		0.8	1.3	2.0	0.8	1.3	2.0	0.8	1.3	2.0	V

NOTES:

1. Guaranteed by design.
2. These measurements are made with the devices warmed-up. It can be seen that there is a selection trade off between droop rate and hold mode settling time.
3. Measured 500 μs after hold command.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10A SMP-11A			SMP-10B SMP-11B			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 3)	—	1.25	3.0	—	1.60	5.5	mV	
Input Bias Current	I_B	$V_{IN} = 0V$	—	90	180	—	160	280	nA	
Leakage (Droop) Current	I_{DR}	$T_A = -55^\circ C$ $T_A = +125^\circ C$ $T_A = \text{Full Range}$ (See Note 2)	SMP-10	—	0.050	0.50	—	0.080	1.22	nA
		SMP-11		—	6	7.5	—	8	10	
Droop Rate	dV_{CH}/dt	$T_A = -55^\circ C$ $T_A = +125^\circ C$ $T_A = \text{Full Range}$ (See Note 2)	SMP-10	—	10	100	—	16	250	$\mu V/ms$
		SMP-11		—	1200	1500	—	1600	2000	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$		0.99950	0.99972	—	0.99940	0.99968	—	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$		78	88	—	72	90	—	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$		—	-1	-3	—	-1	-5	μA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$		—	-5	-15	—	-5	-15	μA
		Hold Mode $V_{S/H} = 5.0V$		—	0.2	—	—	0.2	—	nA
Differential Logic Threshold	V_{TH}			0.6	1.3	2.0	0.6	1.3	2.0	V

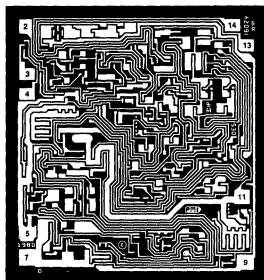
NOTES:

- Guaranteed by design.
- These measurements are made with the devices warmed-up. It can be seen that there is a selection trade off between droop rate and hold mode settling time.
- Measured 500 μs after hold command.



DICE CHARACTERISTICS

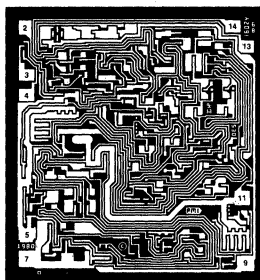
SMP-10



2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND

DIE SIZE 0.081 × 0.086 inch, 6966 sq. mils
(2.057 × 2.184 mm, 4.772 sq. mm)

SMP-11



2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND

For additional DICE information refer to 1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10N SMP-11N LIMIT	SMP-10G SMP-11G LIMIT	UNITS
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$ Hold Mode, (Note 3)	1.5	3.0	mV MAX
Input Bias Current	I_B	$V_{IN} = 0V$	60	90	nA MAX
Leakage (Droop) Current	I_{DR}	Device Warmed-Up	SMP-10 0.10 SMP-11 1	0.25 2.5	nA MAX
Droop Rate	dV_{CH}/dt	Device Warmed-Up	SMP-10 20 SMP-11 200	50 500	$\mu V/ms$ MAX
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$ or $V_{IN} = \pm 5V$	0.99963	0.99953	V/V MIN
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3V$	30	20	mA MIN
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	± 11	± 10.5	V MIN
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	82	77	dB MIN
Power Consumption	P_D	Sample Mode $V_{IN} = 0$	180	210	mW MAX
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$	-2	-3	μA MAX
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$ Hold Mode $V_{S/H} = 5V$	-15 0	-15 0	μA MAX nA MAX
Differential Logic Threshold	V_{TH}	$V_{LC} = 0$	2.0 0.8	2.0 0.8	V MAX V MIN

NOTE:

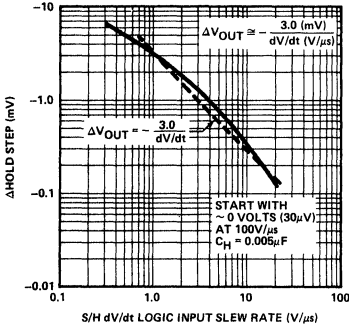
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25^\circ C$, unless otherwise noted.

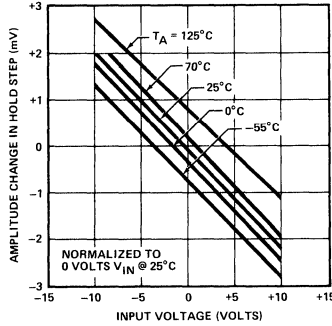
PARAMETER	SYMBOL	CONDITIONS	SMP-10N SMP-11N TYPICAL	SMP-10G SMP-11G TYPICAL	UNITS
Acquisition Time	t_{aq}	10V step to 0.1% of final value	3.5	3.5	μs
Aperture Time	t_{ap}		50	50	ns
Charge Transfer	Q_t	$V_{IN} = 0$, $V_{S/H} = 3.5V$	5	5	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$	10	10	$V/\mu s$

TYPICAL PERFORMANCE CHARACTERISTICS

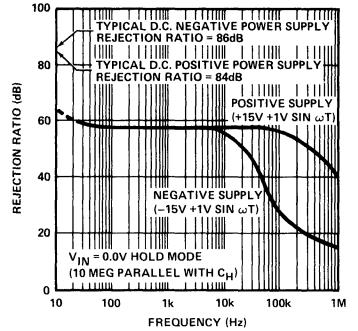
CHANGE IN HOLD STEP
vs $S/H \frac{dV}{dt}$



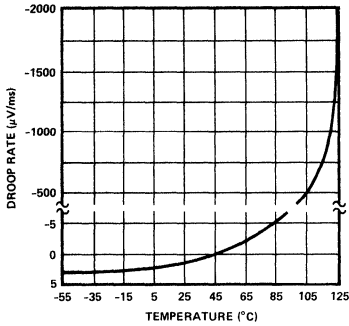
AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE



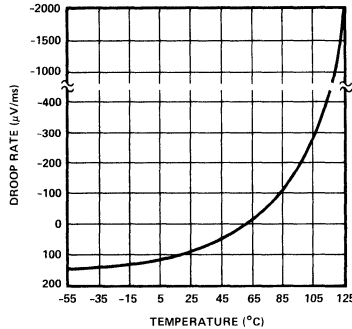
HOLD MODE POWER SUPPLY REJECTION



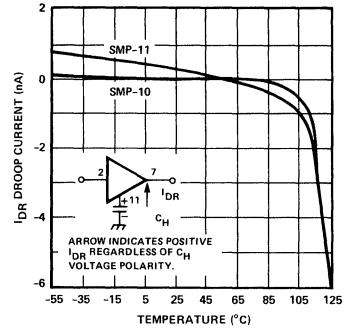
SMP-10 DROOP RATE vs TEMPERATURE



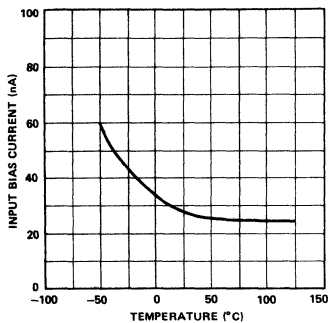
SMP-11 DROOP RATE vs TEMPERATURE



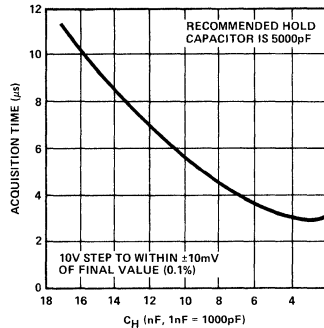
DROOP CURRENT vs TEMPERATURE



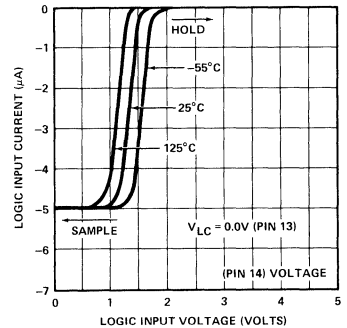
INPUT BIAS CURRENT vs TEMPERATURE



ACQUISITION TIME vs HOLD CAPACITOR

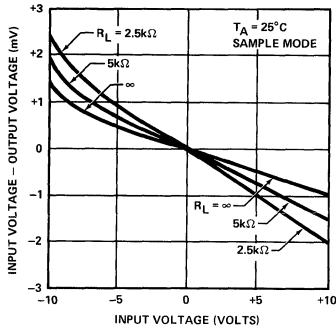


LOGIC INPUT CURRENT

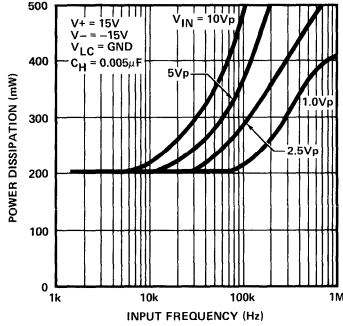


TYPICAL PERFORMANCE CHARACTERISTICS

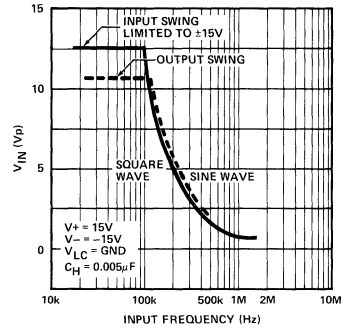
GAIN ERROR



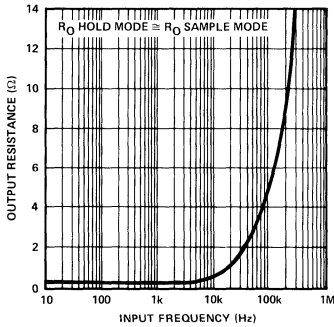
POWER DISSIPATION vs INPUT FREQUENCY = $V_p \sin \omega t$



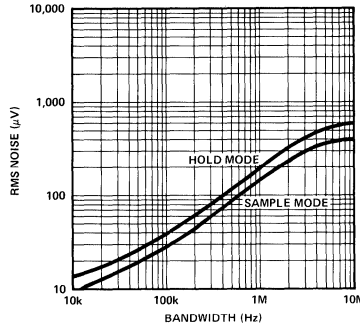
MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY



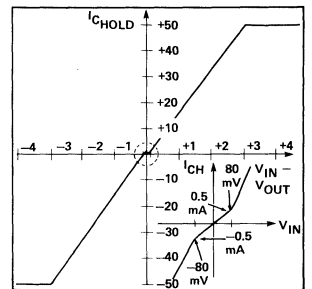
OUTPUT RESISTANCE vs FREQUENCY



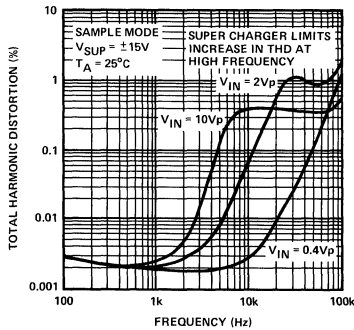
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



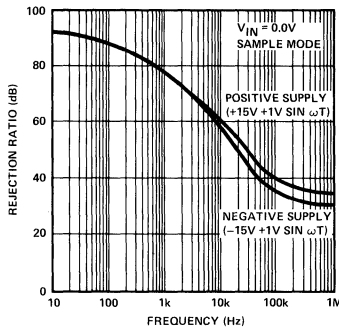
HOLD CAPACITOR CHARGING CURRENT vs INPUT OUTPUT VOLTAGE



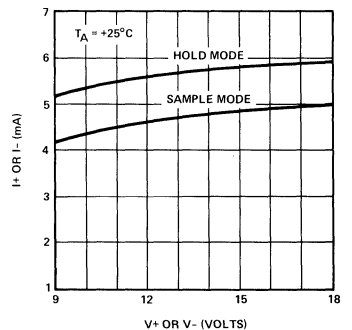
TOTAL HARMONIC DISTORTION vs FREQUENCY

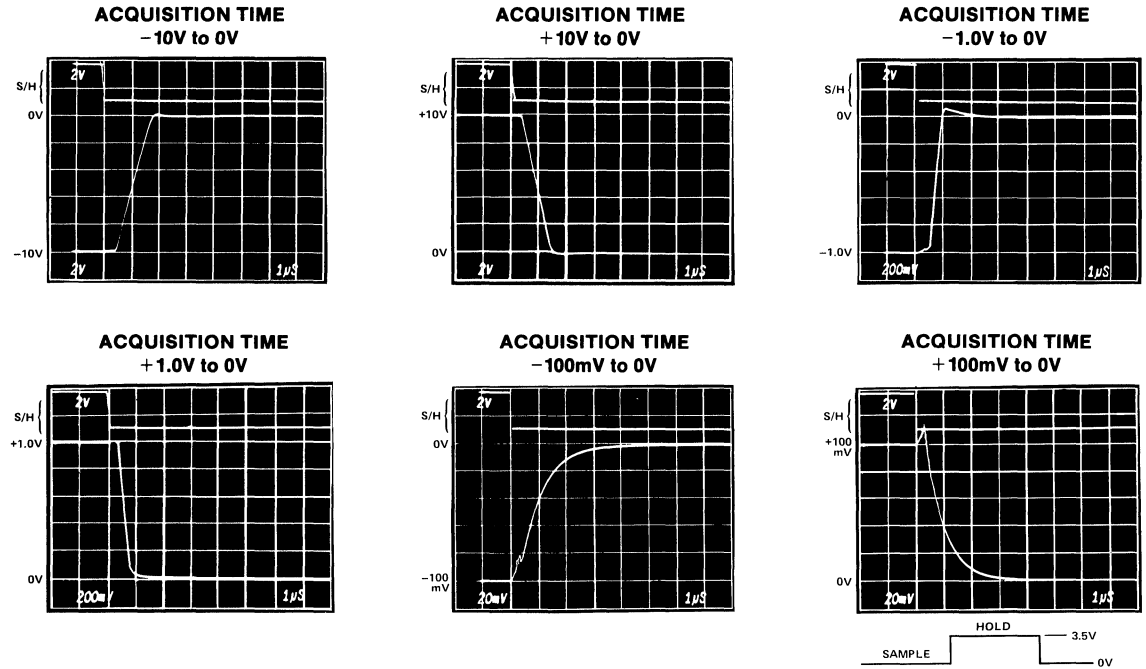


SAMPLE MODE POWER SUPPLY REJECTION



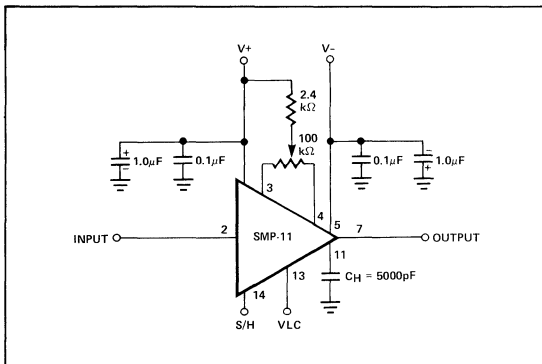
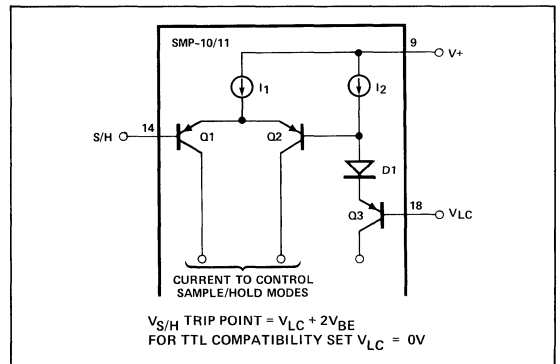
POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE



SMP-10/SMP-11 ACQUISITION TIMES

APPLICATIONS INFORMATION

During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero.

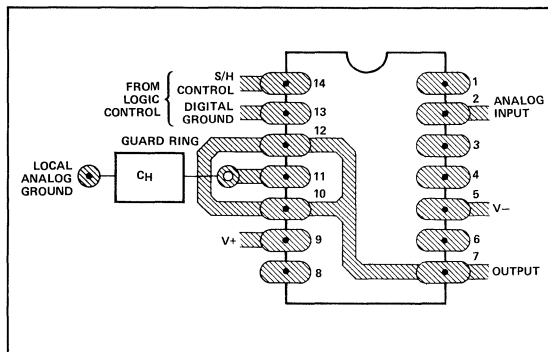
As shown in the Figure, the sample/hold mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high-speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (Pin 13). For CMOS, HTL and HNIL interface, the appropriate

ZERO-SCALE NULL ADJUSTMENT

LOGIC CONTROL


threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC} .

For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample-and-hold control voltage (S/H) must always be at least 2.8V above the negative supply.



GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path.

HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample-and-hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The devices have been internally trimmed for $C_H = 5000\text{pF}$. Other values of C_H will cause a zero-scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS}(\text{mV}) = \frac{5 (\text{pC}) \times 10^3}{C_H (\text{pF})} - 1$$

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.



SMP-81

TELECOMMUNICATIONS
SAMPLE-AND-HOLD AMPLIFIER

Precision Monolithics Inc.

FEATURES

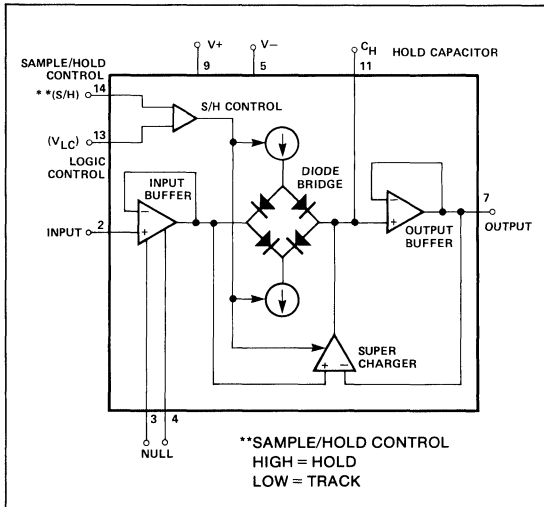
- Meets System Performance Requirements in Multi-Channel CODECs
- Trimmed for Minimum Zero-Scale Error 0.6mV
- Low Droop Rate Over Temperature 0.1 μ V/ μ s
- Low Aperture Time 50ns
- Fast Acquisition Time 10V Step to 0.1% 3.5 μ s
- High Slew Rate 10V/ μ s
- High Sample-Current to Hold-Current Ratio .. 1.7 \times 10⁸
- DTL, TTL & CMOS Compatible Logic Input
- HA-2425, DATEL SHM-IC-1, and AD-583 Socket Compatible*
- Low Power Dissipation
- Low Cost
- Feedthrough Attenuation Ratio 96dB

ORDERING INFORMATION†

V _{ZS} (mV)	HERMETIC 14-PIN DIP	OPERATING TEMPERATURE RANGE
1.6	SMP-81EY	IND
3.5	SMP-81FY	IND

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The SMP-81 precision sample-and-hold amplifier provides the high accuracy, low droop rate and fast acquisition ideally required for PCM encoders. The SMP-81 is a non-inverting unity gain circuit consisting of two buffer amplifiers of very high input impedance connected by a diode bridge switch.

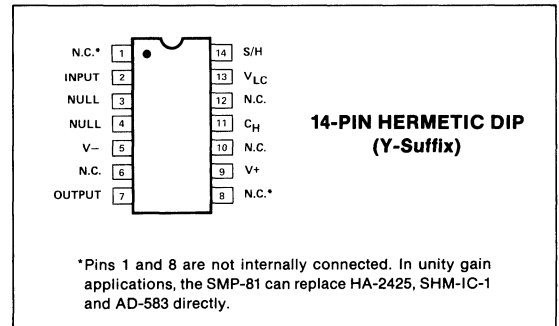
HIGH ACCURACY AND LOW DROOP RATE

The high input impedance and low droop rate of the SMP-81 are achieved by PMI's ion implant super beta process. The high input impedance permits high source impedance applications without degrading accuracy, and low droop rate. Other features of the SMP-81 include high accuracy, 0.6mV of combined offset voltage and step transfer error, and very low feedthrough. A diode bridge switch design allows minimum charge transfer step. On-chip zener-zap trimming eliminates nulling for most applications.

FAST ACQUISITION

A unique super charger or transconductance amplifier provides up to 50mA charging current to the hold capacitor. As a result, smooth charging of the hold capacitor is achieved with minimum noise. The super charger, in conjunction with the high slewing rate input and output buffer amplifiers, permits fast acquisition operation. The adjustable logic input threshold makes the SMP-81 compatible to all logic families.

PIN CONNECTIONS



SAMPLE-AND-HOLD AMPLIFIERS

14

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage ($V+$ minus $V-$)	36V	Output Short-Circuit Duration	Indefinite
Power Dissipation	500mW	Hold Capacitor Short-Circuit Duration	60sec
Derate Above 100° C	10mW/° C	Operating Temperature Range	-25° C to +85° C
Input Voltage	Equal to Supply Voltage	Storage Temperature Range	-65° C to +150° C
Logic and Logic Control Voltage	Equal to Supply Voltage	Lead Temperature (Soldering, 60 sec)	300° C

ELECTRICAL CHARACTERISTICS at $V_S \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-81E			SMP-81F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Zero-Scale Error (Hold Mode)	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$ (500 μ sec after Hold Command)	—	0.6	1.6	—	0.9	3.5	mV
Input Bias Current	I_B	$V_{IN} = 0$	—	105	225	—	120	450	nA
Leakage (Droop) Current	I_{DR}	Device Warmed-up	—	0.5	10	—	0.5	20	nA
Droop Rate	dV_{C_H}/dt		—	0.1	2.0	—	0.1	4.0	mV/msec
Input Resistance	R_{IN}	(See Note)	0.6	2.0	—	0.3	1.4	—	G Ω
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99960	0.99980	—	0.99955	0.99978	—	V/V
Acquisition Time	t_{aq}	10V step to within 10mV of final value (0.1%)	—	3.5	—	—	3.5	—	μ s
Aperture Time	t_{ap}		—	50	—	—	50	—	nsec
Charge Transfer	Q_t	$V_{IN} = 0$, $V_{S/H} = 3.5V$	—	5	—	—	5	—	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$	—	10	—	—	10	—	V/ μ s
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3$ volts	30	50	—	20	50	—	mA
Feedthrough Attenuation Ratio	F_A	Input -20V _{p-p} 1kHz, $R_L = 5K\Omega$ (See Note)	86	96	—	80	90	—	dB
Full Power Bandwidth	F_P	$\pm 10V_{p-p}$ (Dissipation Limited)	—	100	—	—	100	—	kHz
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	± 10	± 11.5	—	± 10	± 11.5	—	V
Output Resistance	R_O		—	0.15	—	—	0.15	—	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	80	90	—	75	90	—	dB
Power Consumption (DC)	P_D	Sample Mode $V_{IN} = 0$	—	160	180	—	170	210	mW
Logic Control Input Current	I_{LC}		-6	-3	—	-9	-3	—	μ A
Logic Input Current	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$ Hold Mode $V_{S/H} = 5.0V$	—	-15	-45	—	-15	-45	μ A
			—	0.6	—	—	0.6	—	nA
Differential Logic Threshold	V_{TH}		0.8	1.3	2.0	0.8	1.3	2.0	V
Hold Mode Settling Time	t_{HM}	5V step to within 1mV of final value	—	1.5	—	—	1.5	—	μ s

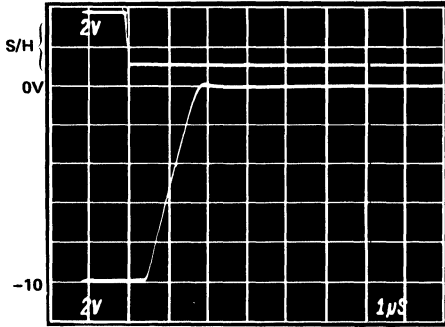
NOTE: Guaranteed by design.

DICE

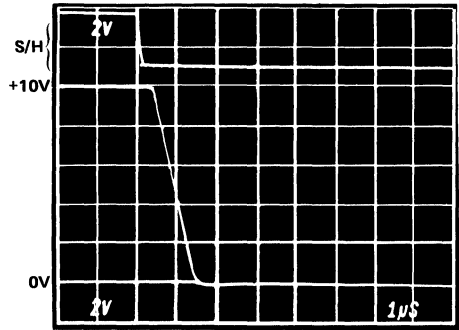
For applicable DICE information, see SMP-11 Data Sheet.

TYPICAL PERFORMANCE CHARACTERISTICS
SMP-81 ACQUISITION TIMES

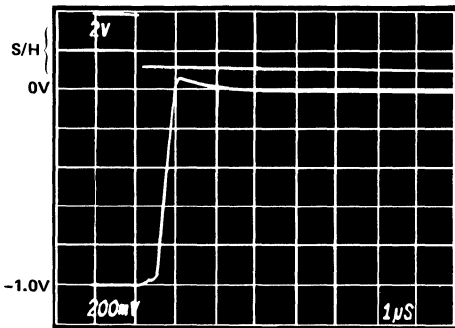
ACQUISITION TIME
 - 10V TO 0V



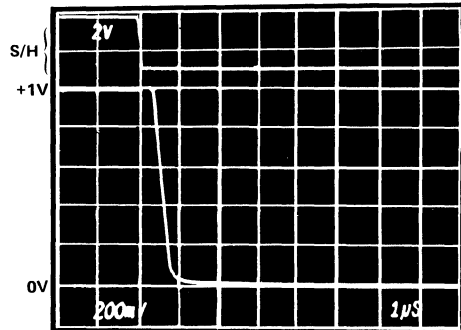
ACQUISITION TIME
 + 10V TO 0V



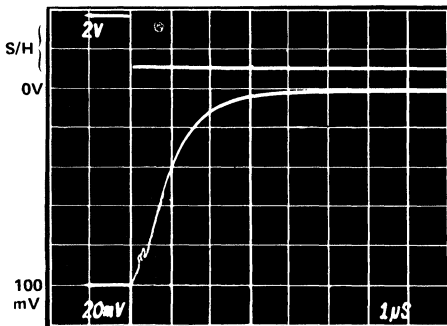
ACQUISITION TIME
 - 1.0V TO 0V



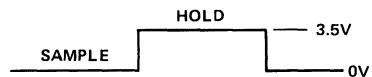
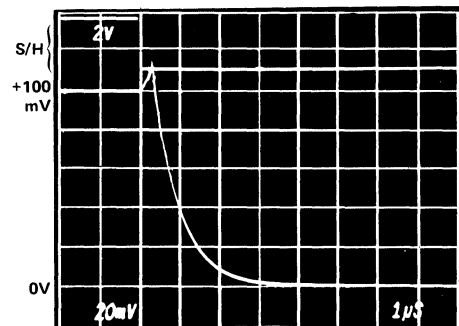
ACQUISITION TIME
 + 1.0V TO 0V



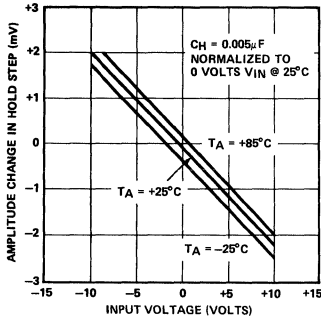
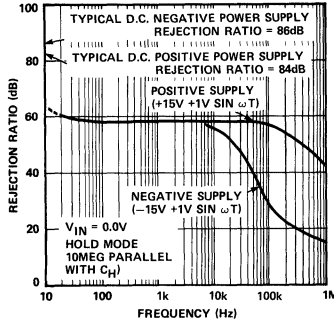
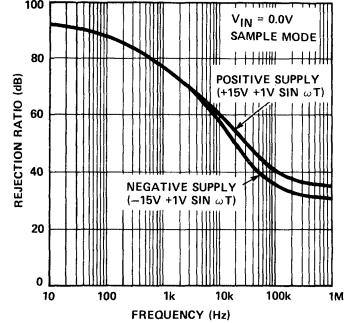
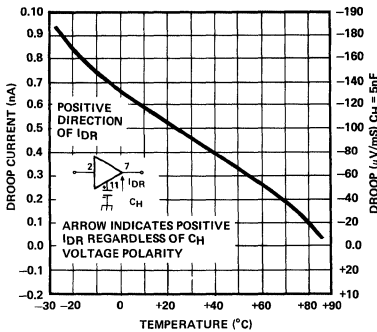
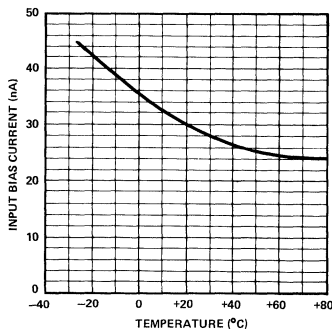
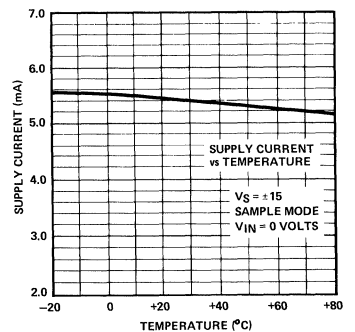
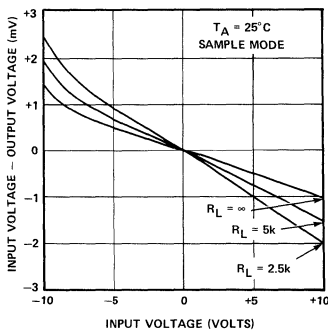
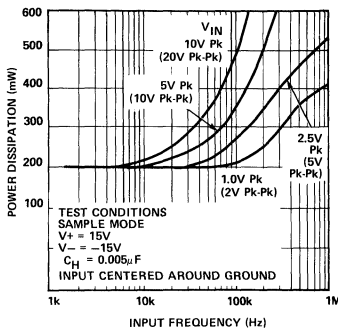
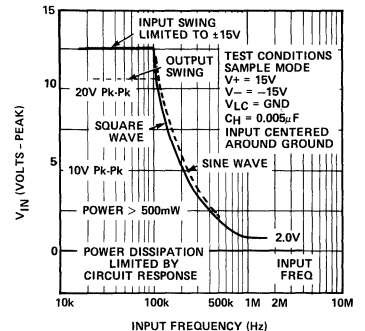
ACQUISITION TIME
 - 100mV TO 0V

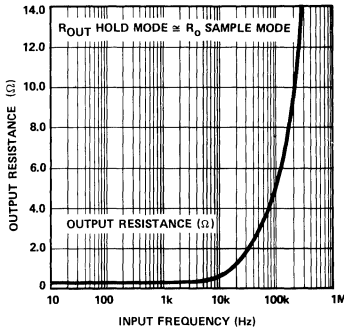
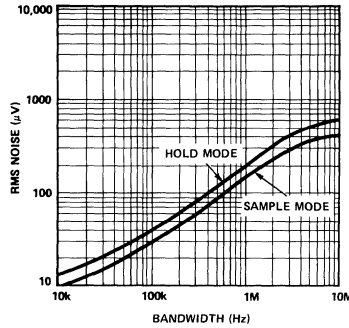
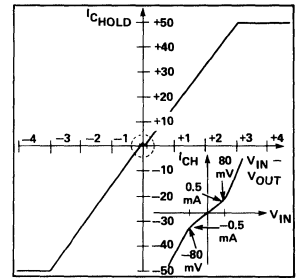
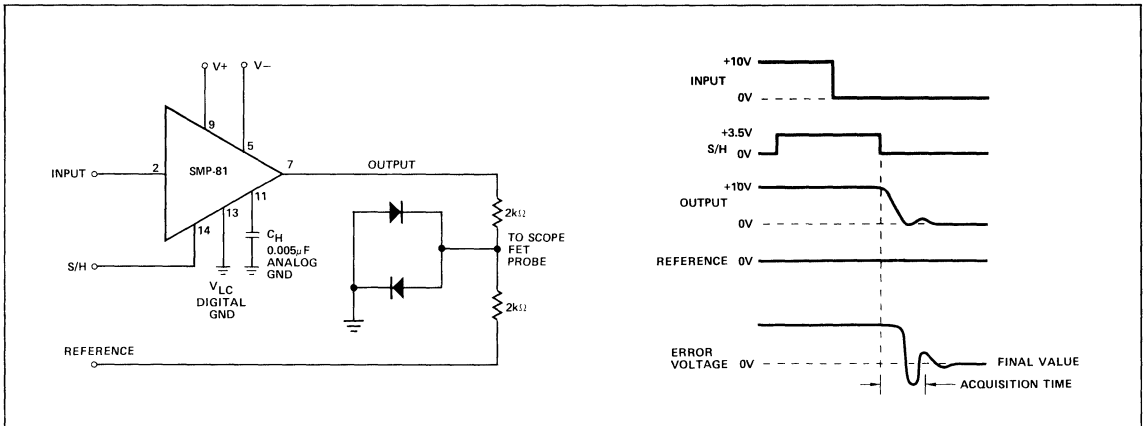


ACQUISITION TIME
 + 100mV TO 0V



TYPICAL PERFORMANCE CHARACTERISTICS

AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE

HOLD-MODE POWER SUPPLY REJECTION

SAMPLE-MODE POWER SUPPLY REJECTION

LEAKAGE (DROOP) CURRENT vs TEMPERATURE

INPUT BIAS CURRENT vs TEMPERATURE

SAMPLE-MODE SUPPLY CURRENT vs TEMPERATURE

GAIN ERROR

POWER DISSIPATION vs FREQUENCY INPUT = $V_p \sin \omega t$

MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS
OUTPUT RESISTANCE vs FREQUENCY

OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

HOLD CAPACITOR CHARGING CURRENT vs INPUT OUTPUT VOLTAGE

ACQUISITION TIME TEST CIRCUIT

APPLICATIONS INFORMATION
HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample-and-hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The SMP-81 is internally trimmed for $C_H = 5000\text{pF}$. Other values of C_H will cause a zero-scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS} (\text{mV}) = \frac{5 (\text{pC}) \times 10^3}{C_H (\text{pF})} - 1$$

A C_H of 5000pF has been empirically determined to be an optimum value for 8-channel shared CODEC operation.

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.

SMP-81 LOGIC CONTROL

The sample/hold mode control of the SMP-81 incorporates a unique logic input circuit, which enables direct interface to all popular logic families and provides maximum noise immunity. As shown in Figure 1, the mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (pin 13). For CMOS, HTL and HN1L interface, the appropriate threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC} .

SAMPLE/HOLD MODE INTERFACE CIRCUITRY

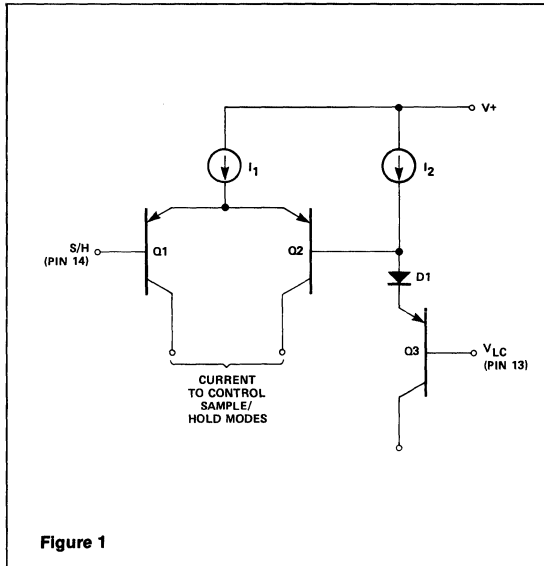


Figure 1

For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample-and-hold control voltage (S/H) must always be at least 2.8V above the negative supply.

ZERO-SCALE ERROR NULL ADJUSTMENT

During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero. Figure 2 shows the recommended 10kΩ trim pot connected to $V+$ if user needs better V_{ZS} than 1.6mV.

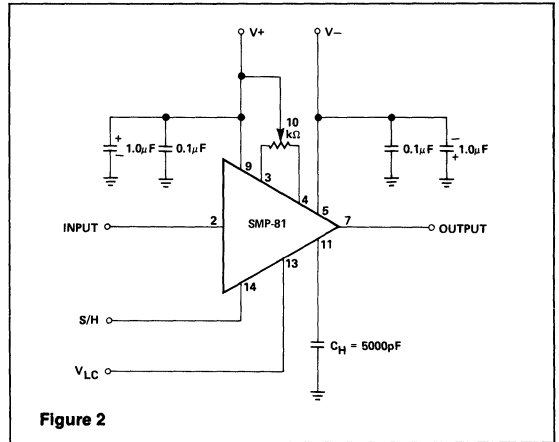


Figure 2

GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path. A guard trace surrounding the hold capacitor node pin 11, minimizes PC board leakage problems, see Figure 3.

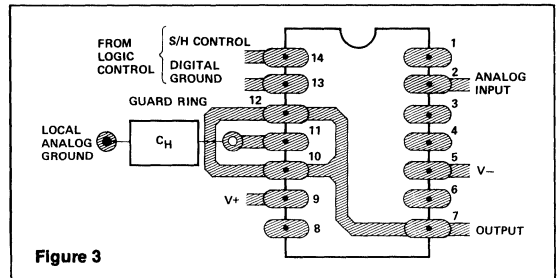


Figure 3



TYPICAL APPLICATION

EIGHT-CHANNEL SHARED CODEC PCM ENCODER

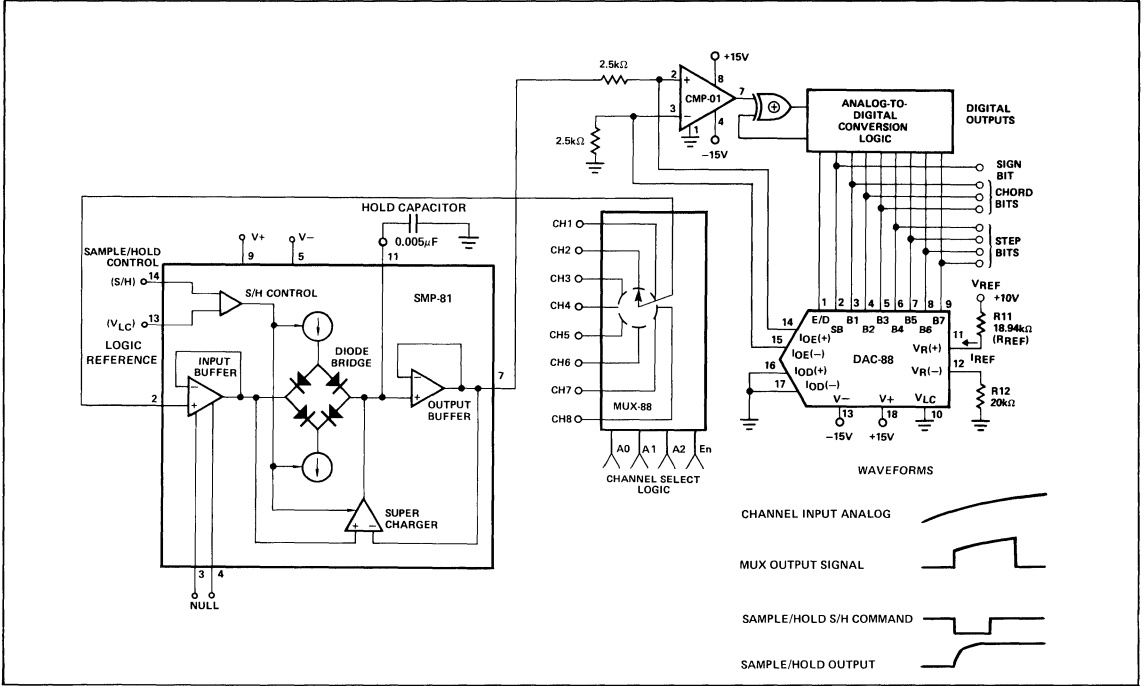


Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



SPECIAL FUNCTIONS

Precision Monolithics Inc.

15-3 Introduction

15-3 Definitions

15-4 **GAP-01**

General-Purpose Analog Signal
Processing Subsystem

15-19 **PKD-01**

Monolithic Peak Detector



SPECIAL FUNCTIONS

Precision Monolithics Inc.

INTRODUCTION

This section includes analog subsystems made up of standard integrated circuit building blocks such as op amps, comparators, analog switches, sample/hold, and buffers.

The GAP-01 is a general-purpose analog signal processing subsystem. This precision circuit contains circuit building blocks used to construct synchronous demodulators, absolute value amplifiers, window comparators, a two-channel S/H amplifier or a two-channel multiplexer with gain.

The PKD-01 functions as an analog peak detector. Peak detection, peak hold and reset are all digitally-controllable. Circuit gain is set by external resistor ratios. The PKD-01 configures into both positive or negative peak detector circuits.

DEFINITIONS

Refer to the sample-and-hold amplifier section of this catalog for the GAP-01 and PKD-01 circuit definitions.



Precision Monolithics Inc.

FEATURES

- Low Offset Voltage 3mV
- Low Zero-Scale Error 4mV
- Low Droop Rate 0.1mV/ms
- Wide Bandwidth 400kHz
- Digitally Selected Signal Path
- Uncommitted Comparator On Chip
- Wide Application Versatility
 - Synchronous Demodulator
 - Absolute Value Amplifier
 - Two-Channel S/H Amplifier
 - Two-Channel Multiplexer With Gain

ORDERING INFORMATION†

V_{OS} (mV)	V_{ZS} (mV)	MILITARY	HERMETIC INDUSTRIAL	PLASTIC COMMERCIAL
3	4	GAP01AX*	GAP01EX	GAP01EP
6	7	GAP01BX*	GAP01FX	GAP01FP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

Designed as a general-purpose analog processing subsystem, the GAP-01 combines many commonly used system building blocks within a single integrated circuit.

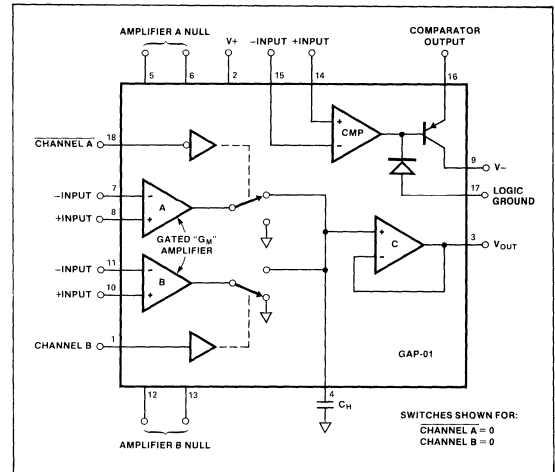
The basic circuit versatility stems from the GAP-01's architecture. The circuit features two differential input transconductance amplifiers, two low-glitch current mode switches, an output voltage buffer amplifier, and a precision comparator.

Both transconductance amplifier outputs are switched by current-mode switches into the voltage follower output buffer, thus providing two digitally selectable signal paths through the device. Gain through the two channels may be different in both sign and magnitude depending upon feedback selection. An external capacitor provides loop compensation and doubles as a hold or "memory" capacitor when the GAP-01 functions as a dual-channel sample/hold amplifier. Offset voltage and charge transfer errors are trimmed by using the "Zener-Zap" trim technique. The output buffer features a FET input stage to reduce droop rate error in S/H applications. A bias current cancellation circuit minimizes droop error at high ambient temperature.

The inclusion of a precision comparator on chip increases the GAP-01's versatility and cost effectiveness in data conversion applications. The output high voltage level is set by external resistors. This scheme maximizes noise immunity and permits interface to all standard logic families.

Several applications exploit the ability to select the signal path through the GAP-01. As a two-channel multiplexer or analog switch, the GAP-01 high input impedance offers advantages when switching high impedance signals. Gain through the "MUX" is also possible. The GAP-01 operates as a sample/hold amplifier in the hold mode when both transconductance amplifiers are unselected. With the on-board comparator, a two-channel successive approximation analog-to-digital conversion (ADC) system may be constructed. Combining a sign-magnitude, digital-to-analog (DAC) converter with the GAP-01 results in a four-quadrant multiplying DAC. The GAP-01 contains all the functional devices needed to perform synchronous demodulation or implement the absolute value function.

FUNCTIONAL DIAGRAM



CONTROL LOGIC

Ch A	Ch B	OUTPUT to C
0	0	Channel A
0	1	Sum
1	0	Hold Last Input
1	1	Channel B



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±18V
Power Dissipation	500mW
Input Voltage	Equal to Supply Voltage
Logic and Logic Ground Voltage	Equal to Supply Voltage
Output Short-Circuit Duration	Indefinite
Amplifier A or B Differential Input Voltage	±24V
Comparator Differential Input Voltage	±24V
Comparator Output Voltage ...	Equal to Positive Supply Voltage
Hold Capacitor Short-Circuit Duration	Indefinite
Storage Temperature	-65° C to +150° C
Lead Temperature (Soldering, 60 sec)	300° C

Operating Temperature Range

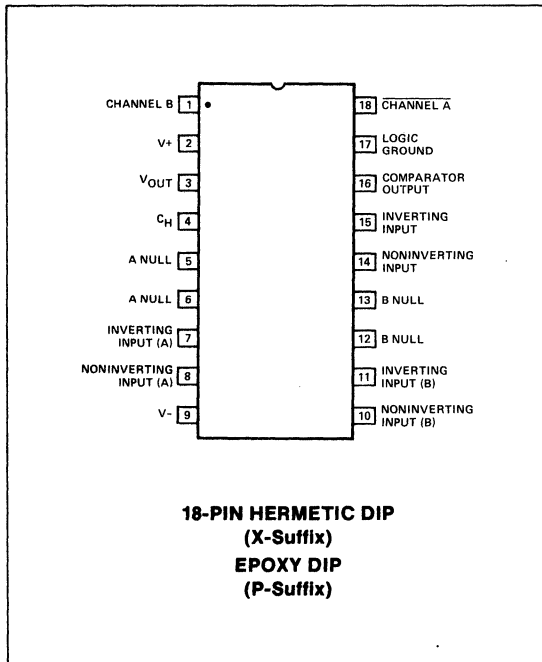
GAP01AX, BX	-55° C to +125° C
GAP01EX, FX	-25° C to +85° C
GAP01EP, FP	0° C to +70° C
DICE Junction Temperature (T _j)	-65° C to +150° C

(NOTE 1)	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
18-Pin DIP (X)	100° C	10mW/° C
18-Pin DIP (P)	50° C	10mW/° C

NOTES:

1. Maximum package power dissipation vs. ambient temperature.
2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

PIN CONNECTIONS



DICE CHARACTERISTICS

DIE SIZE 0.090 × 0.100 inch, 9,000 sq. mils
(2.286 × 2.54; 5.8 sq.mm)

1. CHANNEL (B)	10. NONINVERTING INPUT (B)
2. V+	11. INVERTING INPUT (B)
3. V _{OUT}	12. (B) NULL
4. C _H	13. (B) NULL
5. (A) NULL	14. COMPARATOR NONINVERTING INPUT
6. (A) NULL	15. COMPARATOR INVERTING INPUT
7. INVERTING INPUT (A)	16. COMPARATOR OUTPUT
8. NONINVERTING INPUT (A)	17. LOGIC GND
9. V-	18. CHANNEL (A)

For additional DICE information refer to
1986 Data Book, Section 2.

SPECIAL FUNCTIONS

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	GAP01A/E			GAP01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	2	4	—	3	7	mV
Input Offset Voltage	V_{OS}		—	2	3	—	3	6	mV
Input Bias Current	I_B		—	80	150	—	80	250	nA
Input Offset Current	I_{OS}		—	20	40	—	50	100	nA
Voltage Gain	A_V		18	25	—	10	25	—	V/mV
Open-Loop Bandwidth	BW	$A_V = 1$	—	0.4	—	—	0.4	—	MHz
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	86	96	—	76	96	—	dB
Input Voltage Range	V_{CM}	(Note 2)	± 11.5	± 12	—	± 11.5	± 12	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/ μs
Feedthrough Error		$\Delta V_{IN} = 20V$, CHA = 1, CHB = 0 (Note 2)	66	80	—	66	80	—	dB
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$ (Note 2)	—	41	70	—	41	70	μs
Acquisition Time to 0.01% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$ (Note 2)	—	45	—	—	45	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	0.5	1.5	—	1	3	mV
Input Bias Current	I_B		—	700	1000	—	700	1000	nA
Input Offset Current	I_{OS}		—	75	300	—	75	300	nA
Voltage Gain	A_V	2k Ω Pull-up Resistor to 5V (Note 2)	5	7.5	—	3.5	7	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	76	90	—	76	90	—	dB
Input Voltage Range	V_{CM}	(Note 2)	± 11.5	± 12.5	—	± 11.5	± 12.5	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	μA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	7	12	45	7	12	45	mA
Response Time	t_s	5mV Overdrive, (Note 3) 2k Ω Pull-up Resistor to 5V	—	150	—	—	150	—	ns
DIGITAL INPUTS—CHA, CHB (Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	2	10	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_j = +25^\circ C$ (Note 1)	—	0.02	0.07	—	—	0.1	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11.5	± 12.5	—	± 11	± 12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Switch Switching Time	t_s		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/ μs
Power Supply Current	I_{SY}	No Load	—	5	7	—	6	9	mA

NOTES:

1. Due to limited production test times the droop current corresponds to junction temperature (T_j).

2. Guaranteed by design.

3. Channel A = "1", Channel B = "0".



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55^\circ C \leq T_A \leq 125^\circ C$ for GAP01AX & BX; $-25^\circ C \leq T_A \leq 85^\circ C$ for GAP01EX & FX, and $0^\circ C \leq T_A \leq 70^\circ C$ for GAP01EP & FP.

PARAMETER	SYMBOL	CONDITIONS	GAP01A/E			GAP01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	4	7	—	6	12	mV
Input Offset Voltage	V_{OS}		—	3	6	—	5	10	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-3	-6	—	-5	-6	$\mu V/^\circ C$
Input Bias Current	I_B		—	160	250	—	160	500	nA
Input Offset Current	I_{OS}		—	30	100	—	30	150	nA
Voltage Gain	A_V		7.5	9	—	5	9	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	80	90	—	70	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	± 11	± 12	—	± 10.5	± 12	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/ μs
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$	—	60	—	—	60	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	2	2.5	—	2	5	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-4	-6	—	-4	-6	$\mu V/^\circ C$
Input Bias Current	I_B		—	1000	2000	—	1100	2000	nA
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2k Ω Pull-up Resistor to 5V, (Note 1)	4	6.5	—	2.5	6.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 1)	± 11	—	—	± 11	—	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 5V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	25	160	μA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	6	10	45	6	10	45	mA
Response Time	t_s	5mV Overdrive, (Note 3) 2k Ω Pull-up Resistor to 5V	—	200	—	—	200	—	ns
DIGITAL INPUTS-CHA, CHB (Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_J = \text{Max. Operating Temp.}$, (Note 2)	—	1	10	—	1	10	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11	± 12	—	± 10.5	± 12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2	—	—	2	—	V/ μs
Power Supply Current	I_{SY}	No Load	—	5.5	8	—	6.5	10	mA

NOTES: See next page.



WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	GAP-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V_{ZS}		7	mV MAX
Input Offset Voltage	V_{OS}		6	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		100	nA MAX
Voltage Gain	A_V		10	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, $CHA = 1$, $CHB = 0$ (Note 1)	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2k Ω Pull-up Resistor to 5V (Note 1)	3.5	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 5V	0.4 -0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	μA MAX
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7	mA MAX mA MIN
DIGITAL INPUTS-\overline{CHA}, CHB (Note 3)				
Logic "1" Input Voltage	V_H		2	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1	μA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	μA MAX
MISCELLANEOUS				
Drop Rate	V_{DR}	$T_j = 25^\circ C$ $T_A = 25^\circ C$ (See Note 2)	0.1 0.20	mV/ms MAX mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11	V MIN
Short-Circuit Current: Amplifier C	I_{SC}		40 7	mA MAX mA MIN
Power Supply Current	I_{SY}	No Load	9	mA MAX

NOTES:

1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than

1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures.

3. Channel \overline{A} = "1", Channel B = "0".

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

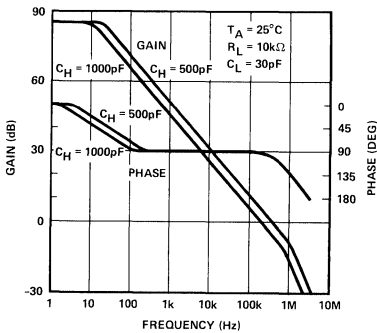


TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$.

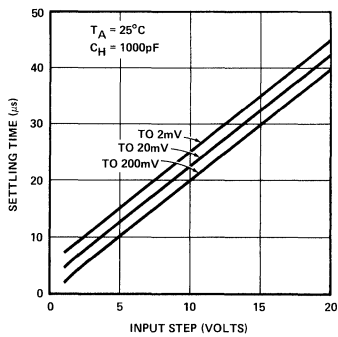
PARAMETER	SYMBOL	CONDITIONS	GAP-01N TYPICAL	UNITS
"g_m" AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/ μ s
Acquisition Time to 0.1% Accuracy	t_{aq}	20V step, $A_{VCL} = 1$	41	μ s
Acquisition Time to 0.01% Accuracy	t_{aq}	20V step, $A_{VCL} = 1$	45	μ s
COMPARATOR				
Response Time	t_s	5mV Overdrive 2k Ω Pull-up Resistor to +5V	150	ns
MISCELLANEOUS				
Switch Aperture Time	t_{ap}		75	ns
Switching Time	t_s		50	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k\Omega$	2.5	V/ μ s

TYPICAL PERFORMANCE CHARACTERISTICS

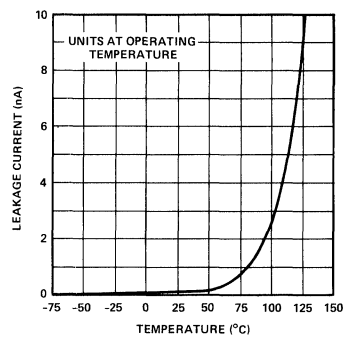
SMALL-SIGNAL OPEN-LOOP GAIN/PHASE vs FREQUENCY



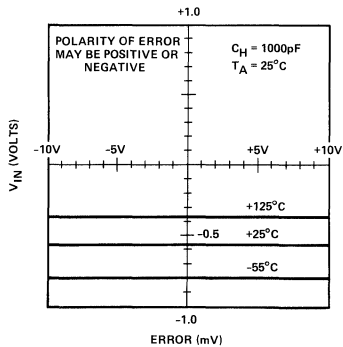
ACQUISITION TIME vs INPUT VOLTAGE STEP SIZE



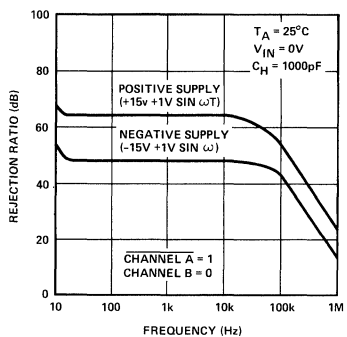
DROOP CURRENT vs TEMPERATURE



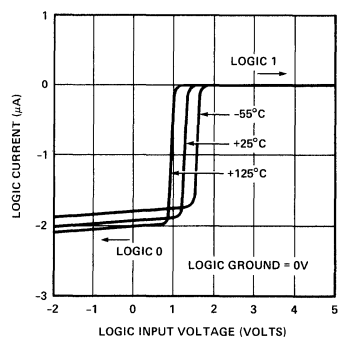
AMPLIFIER CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE



HOLD-MODE POWER SUPPLY REJECTION vs FREQUENCY

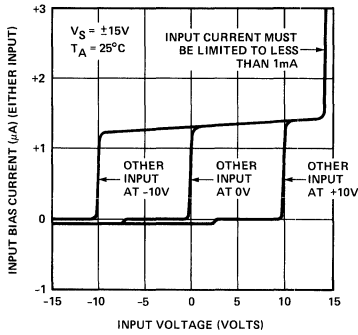
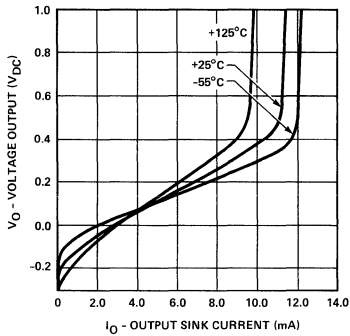
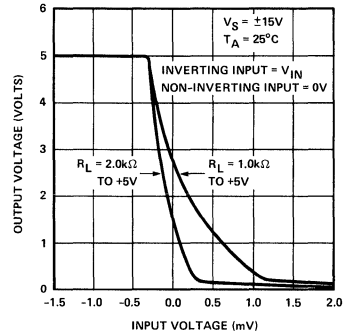
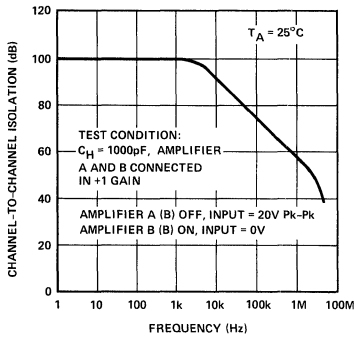
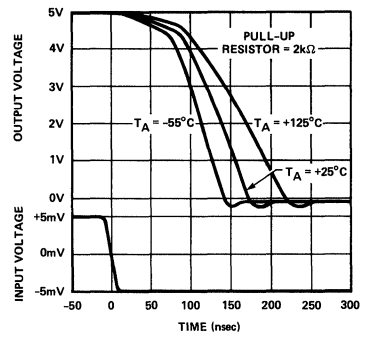
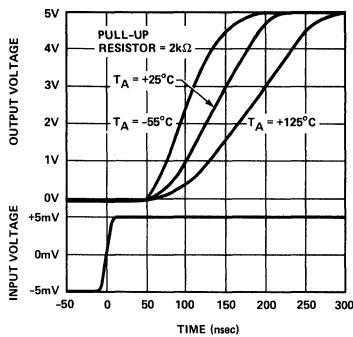
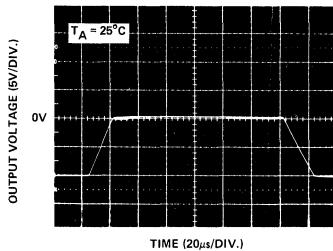
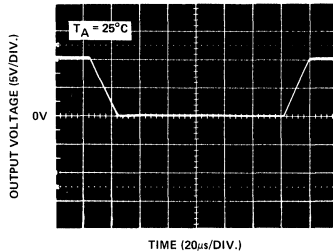
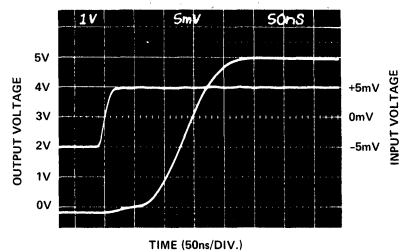


LOGIC INPUT CURRENT vs LOGIC INPUT VOLTAGE

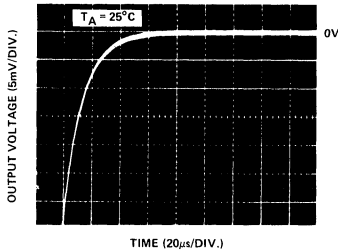
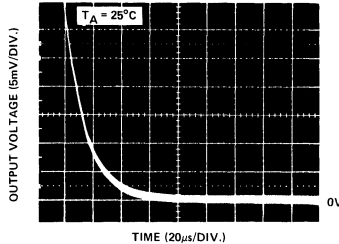
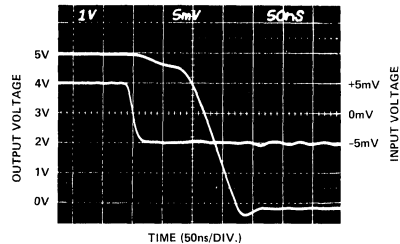
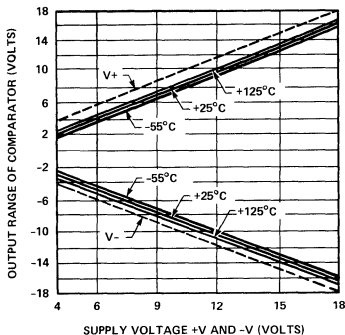
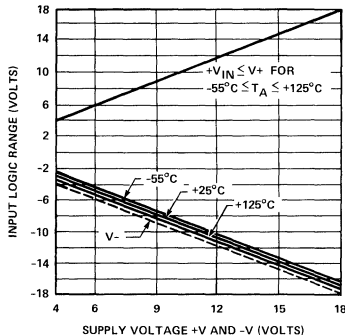
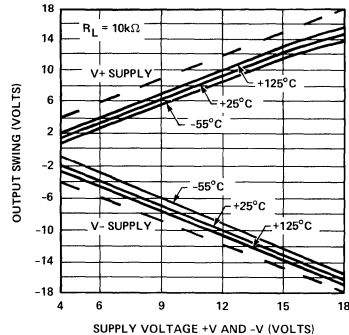
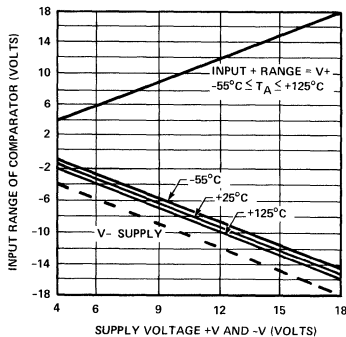
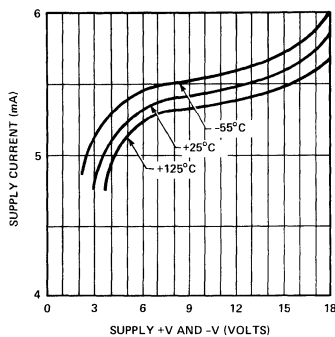


SPECIAL FUNCTIONS

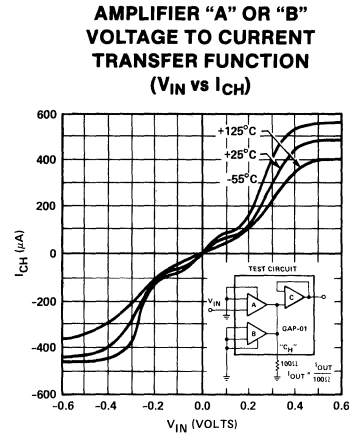
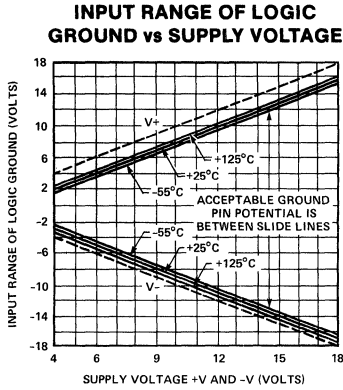
15

TYPICAL PERFORMANCE CHARACTERISTICS
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE

COMPARATOR TRANSFER CHARACTERISTIC

CHANNEL TO CHANNEL ISOLATION vs FREQUENCY

COMPARATOR RESPONSE TIME vs TEMPERATURE

LARGE-SIGNAL INVERTING RESPONSE

LARGE-SIGNAL NONINVERTING RESPONSE

COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, T_A = 25°C)


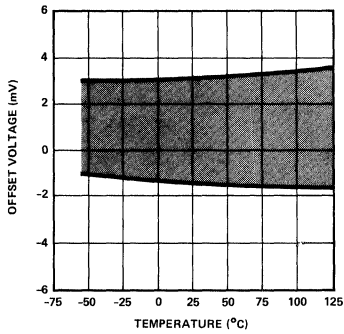
TYPICAL PERFORMANCE CHARACTERISTICS

**COMPARATOR
SETTLING TIME FOR
-10V TO 0V STEP INPUT**

**COMPARATOR
SETTLING TIME FOR
+10V TO 0V STEP INPUT**

**COMPARATOR OUTPUT
RESPONSE TIME (2kΩ
PULL-UP RESISTOR, TA = 25°C)**

**OUTPUT SWING OF
COMPARATOR vs
SUPPLY VOLTAGE**

**INPUT LOGIC RANGE vs
SUPPLY VOLTAGE**

**BUFFER OUTPUT VOLTAGE
SWING vs SUPPLY VOLTAGE
(DUAL SUPPLY OPERATION)**

**A AND B INPUT RANGE vs
SUPPLY VOLTAGE**

**SUPPLY CURRENT vs
SUPPLY VOLTAGE**


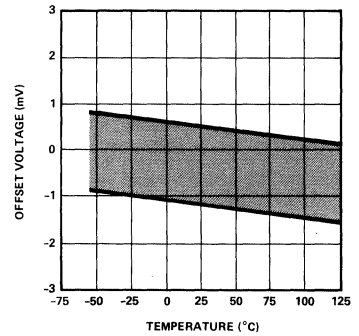
TYPICAL PERFORMANCE CHARACTERISTICS



A AND B AMPLIFIERS OFFSET VOLTAGE vs TEMPERATURE

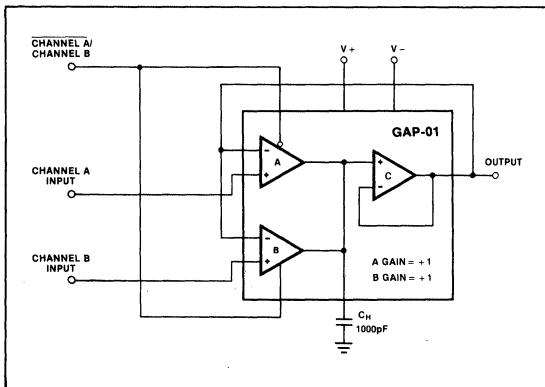


COMPARATOR OFFSET VOLTAGE vs TEMPERATURE

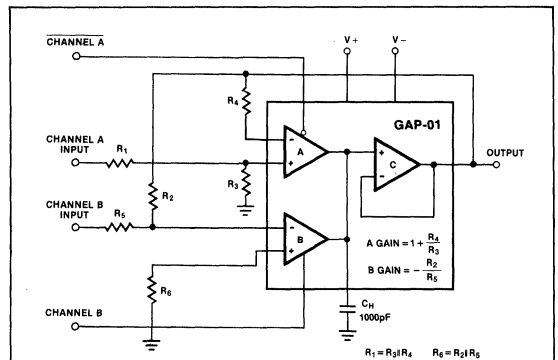


APPLICATION CIRCUITS

GAP-01 IN UNITY GAIN (+1) CONFIGURATION



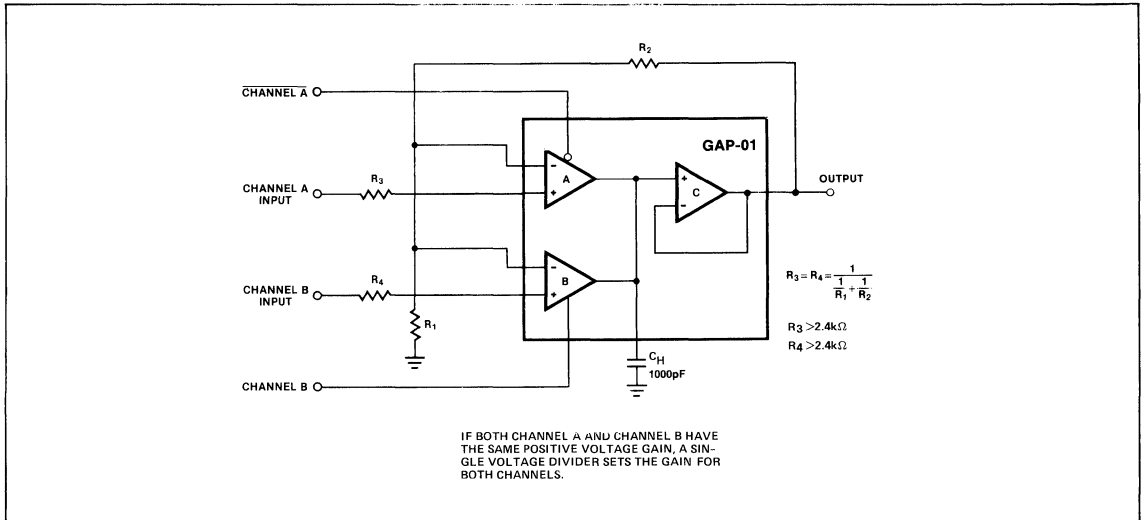
GAP-01 WITH POSITIVE AND NEGATIVE GAINS



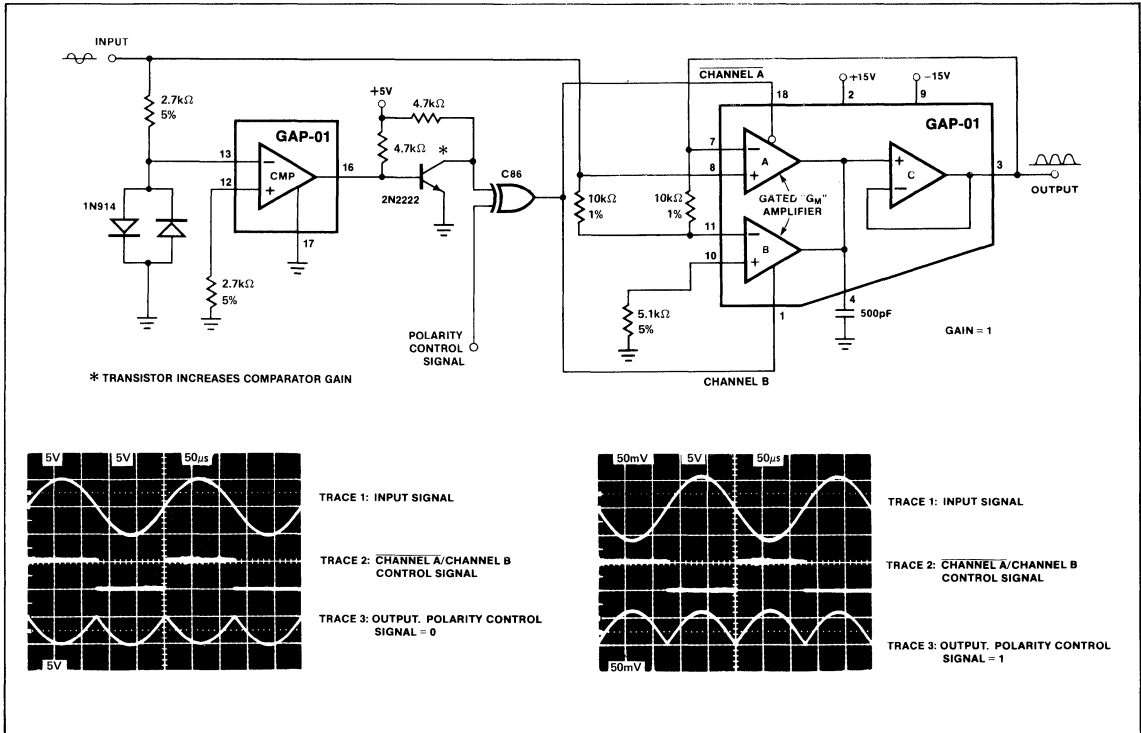


APPLICATION CIRCUITS

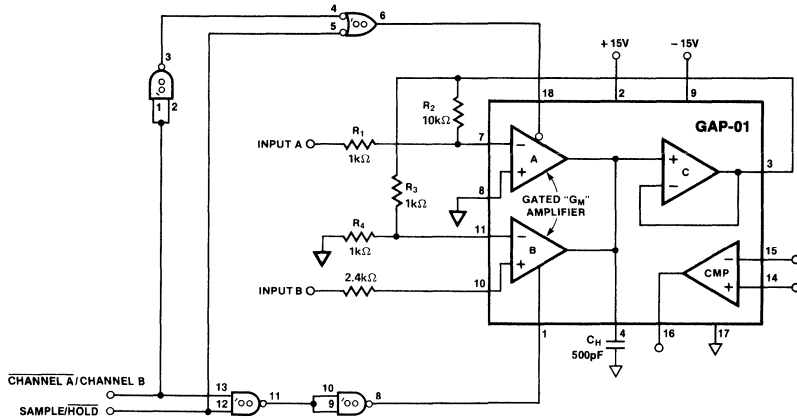
ALTERNATE GAIN CONFIGURATION



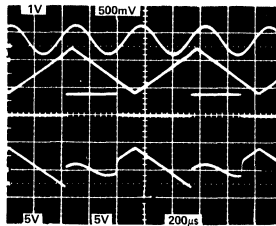
ABSOLUTE VALUE CIRCUIT WITH POLARITY PROGRAMMABLE OUTPUT



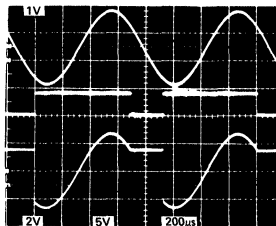
TWO-CHANNEL SAMPLE/HOLD AMPLIFIER



CHANNEL A GAIN = $-\frac{R_2}{R_1} = -10$
 CHANNEL B GAIN = $1 + \frac{R_2}{R_1} = 2$



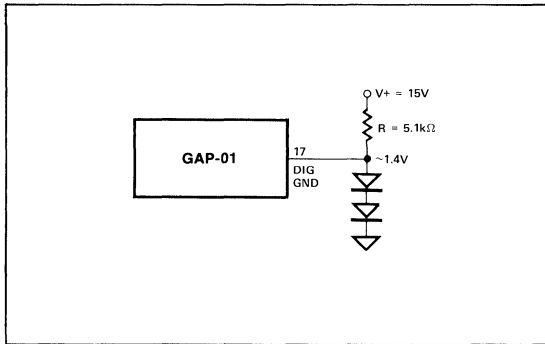
TRACE 1: INPUT SIGNAL B (1V/DIV.)
 TRACE 2: INPUT SIGNAL A (0.5V/DIV.)
 TRACE 3: CHANNEL A/CHANNEL B CONTROL SIGNAL (5V/DIV.)
 TRACE 4: OUTPUT WITH SAMPLE/HOLD = "1" (5V/DIV.)



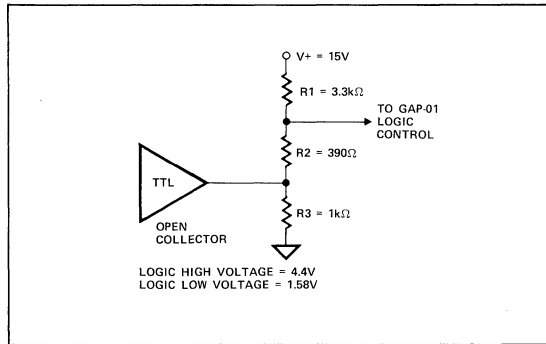
TRACE 1: INPUT SIGNAL B (1V/DIV.)
 TRACE 2: SAMPLE/HOLD (5V/DIV.) CONTROL SIGNAL
 TRACE 3: OUTPUT SIGNAL (2V/DIV.) CHANNEL A/CHANNEL B = "1"

APPLICATION CIRCUITS

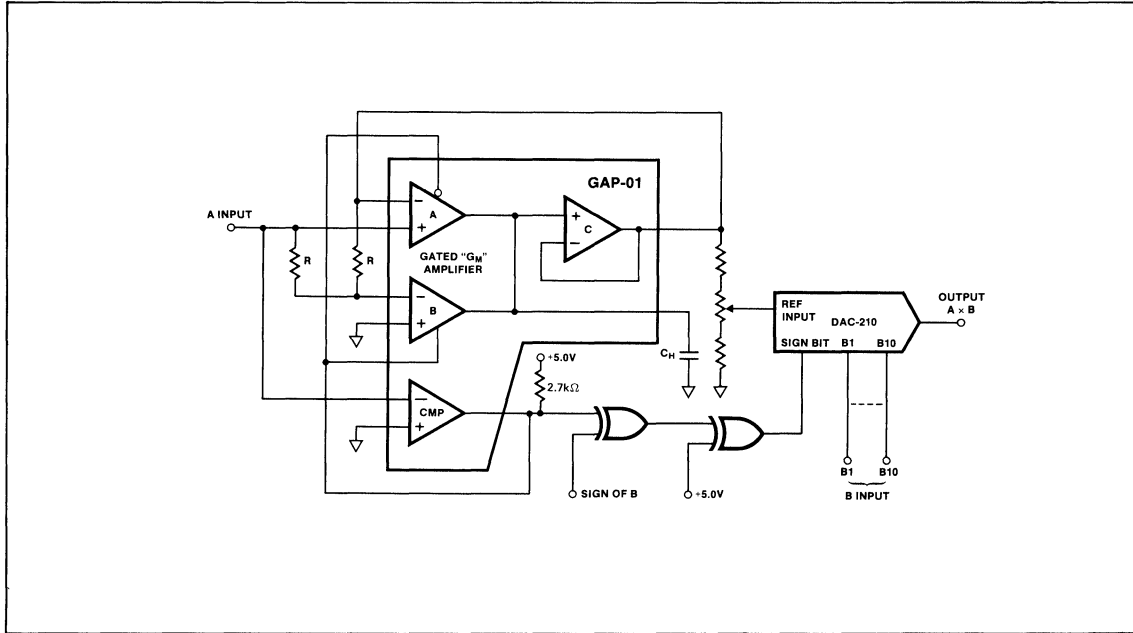
DIGITAL GROUND CONNECTION FOR SINGLE SUPPLY OPERATION



LOGIC LEVEL TRANSLATION FOR GAP-01 SINGLE SUPPLY OPERATION

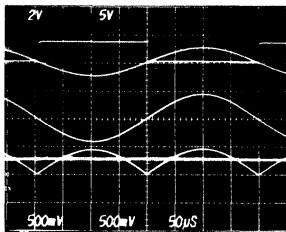
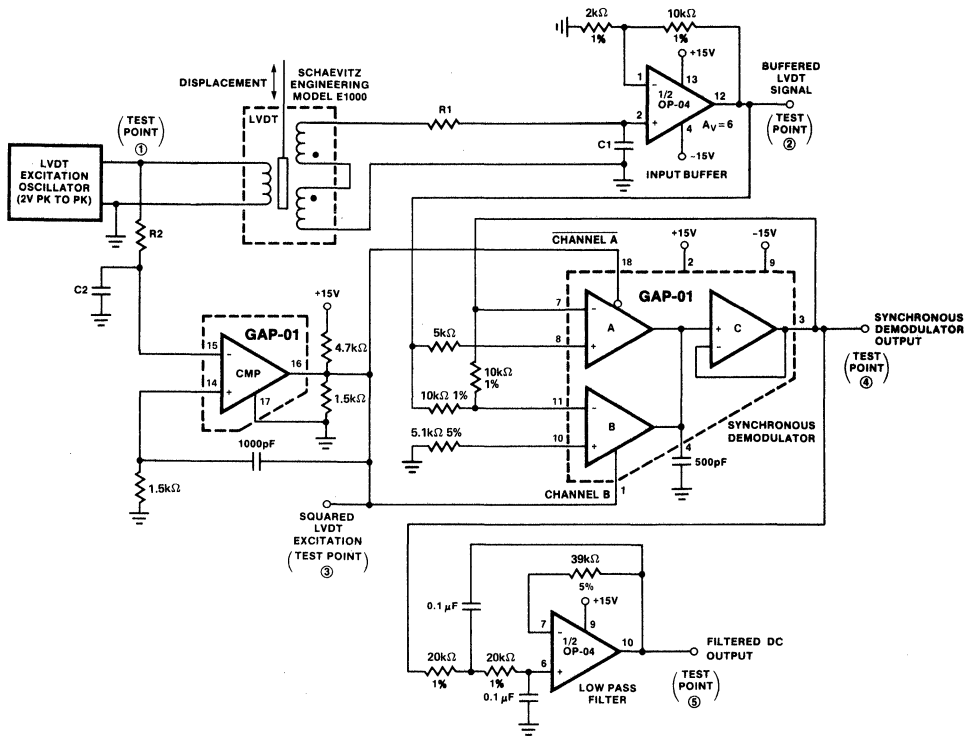


FOUR QUADRANT MULTIPLYING DAC



APPLICATION CIRCUITS

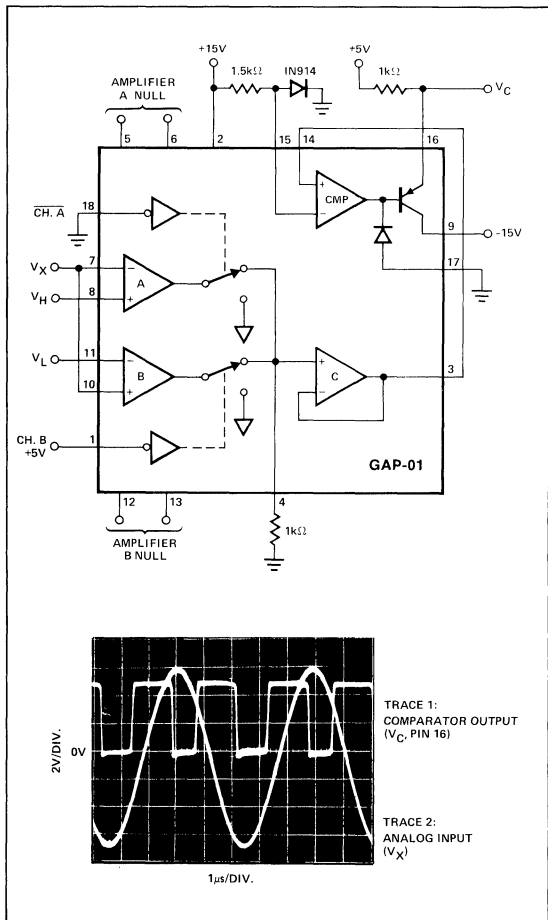
SYNCHRONOUS DEMODULATION OF LVDT SIGNAL



- 0V TRACE 1A: LVDT SINEWAVE EXCITATION (TEST POINT 1) -2V/DIV.
- TRACE 1B: GAP-01 COMPARATOR OUTPUT (TEST POINT 3) -5V/DIV.
- 0V TRACE 2: BUFFERED LVDT OUTPUT AT GAP-01 INPUT (TEST POINT 2) 0.5V/DIV.
- 0V TRACE 3A: LVDT SIGNAL AFTER GAP-01 SYNCHRONOUS DEMODULATION (TEST POINT 4) -0.5V/DIV.
- TRACE 3B: DC OUTPUT LEVEL INDICATING LVDT CORE POSITION (TEST POINT 5) 0.5V/DIV.

APPLICATION CIRCUITS

WINDOW COMPARATOR



APPLICATION INFORMATION

CAPACITOR RECOMMENDATIONS

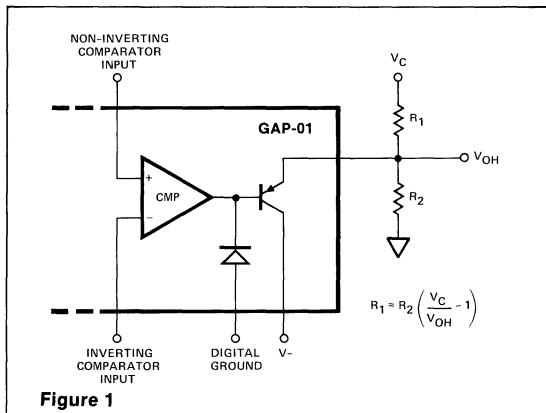
The external capacitor (C_H) serves as the compensation capacitor and hold capacitor in sample/hold applications. Stable operation requires a minimum value of 500pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase and bandwidth decrease.

The capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1 .



V _C	V _{OH}	R ₁	R ₂
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{\text{sink}}}$$

$$R_2 \approx R_1 \left(\frac{1}{\frac{V_C}{V_{OH}} - 1} \right)$$

Table I

The maximum comparator high output voltage (V_{OH}) should be constrained to: $V_{OH}(\text{max}) < V+ - 2V$

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the

common system ground. This avoids digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point. To minimize gain errors and maintain the GAP-01's inherently low droop rate, guarding Pin 4 as shown in Figure 2 is recommended.

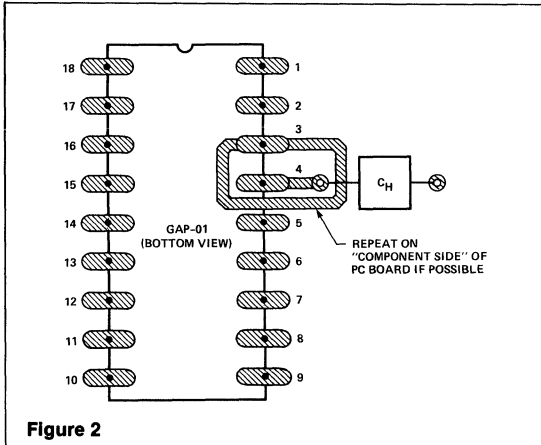


Figure 2

LOGIC CONTROL

The transconductance amplifier outputs are switched by the digital logic signals applied at Channel A and Channel B pins. Two signal paths through the GAP-01 are possible.

The logic threshold voltage is 1.4 volts when digital ground is at zero volts. Other threshold voltages (V_{TH}) may be selected by applying the formula:

$$V_{TH} \approx 1.4V + \text{Digital Ground Potential.}$$

Figure 3 shows the simplified logic control circuit. For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The logic signals must always be at least 2.8V above the negative supply.

Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

$$V_{OL} \approx 0.2V + \text{Digital Ground Potential.}$$

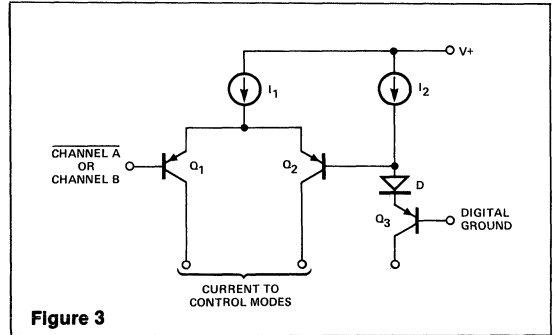


Figure 3

ZERO-SCALE ERROR ADJUSTMENT

For sample/hold applications the zero-scale error (V_{OS} plus charge injection error) can be adjusted to zero. With the input to each channel equal to zero, the GAP-01 is switched between the sample mode (either channel A or channel B active) and the hold mode (channel A = 1, channel B = 0). The output is adjusted to read zero when the unit is in the hold mode.

The V_{ZS} trim circuit is identical to the V_{OS} trim circuit.

OFFSET VOLTAGE ERROR ADJUSTMENT Offset voltage through either channel A or channel B may be nulled with an external 100k Ω potentiometer as shown below.

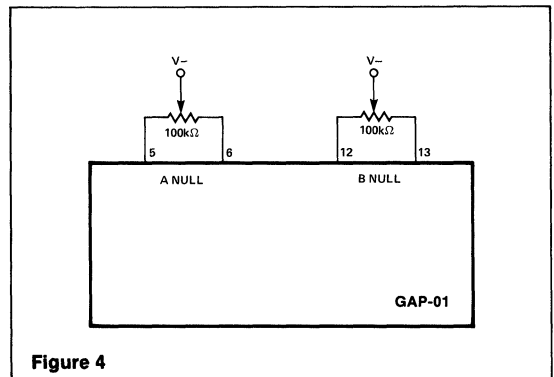


Figure 4

Precision Monolithics Inc.

FEATURES

- **Monolithic Design for Reliability and Low Cost**
- **High Slew Rate** 0.5V/ μ s
- **Low Droop Rate**
 $T_A = 25^\circ\text{C}$ 0.1mV/ms
 $T_A = 125^\circ\text{C}$ 10mV/ms
- **Low Zero-Scale Error** 4mV
- **Digitally Selected Hold and Reset Modes**
- **Reset to Positive or Negative Voltage Levels**
- **Logic Signals TTL and CMOS Compatible**
- **Uncommitted Comparator on Chip**

ORDERING INFORMATION†

25°C V_{ZS} (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	14-PIN DUAL-IN-LINE PACKAGE HERMETIC*	PLASTIC	
4	PKD01AY*	—	MIL
7	PKD01BY*	—	MIL
4	PKD01EY	—	IND
7	PKD01FY	—	IND
4	—	PKD01EP	COM
7	—	PKD01FP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The PKD-01 tracks an analog input signal until a maximum amplitude is reached. The maximum value is then retained as a peak voltage on a hold capacitor. Being a monolithic circuit, the PKD-01 offers significant performance and package density advantages over hybrid modules and discrete designs without sacrificing system versatility. The matching characteristics attained in a monolithic circuit provide inherent advantages when charge injection and droop rate error reduction are primary goals.

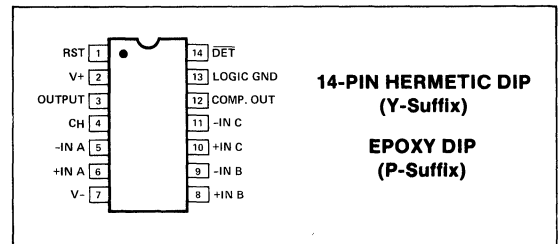
Innovative design techniques maximize the advantages of monolithic technology. Transconductance (g_m) amplifiers were chosen over conventional voltage amplifier circuit building blocks. The " g_m " amplifiers simplify internal frequency compensation, minimize acquisition time and maximize circuit accuracy. Their outputs are easily switched by low glitch current steering circuits. The steered outputs are clamped to reduce charge injection errors upon entering the hold mode or exiting the reset mode. The inherently low zero-scale error is reduced further by active "Zener-Zap" trimming to optimize overall accuracy.

The output buffer amplifier features an FET input stage to reduce droop rate error during lengthy peak hold periods. A bias current cancellation circuit minimizes droop error at high ambient temperatures.

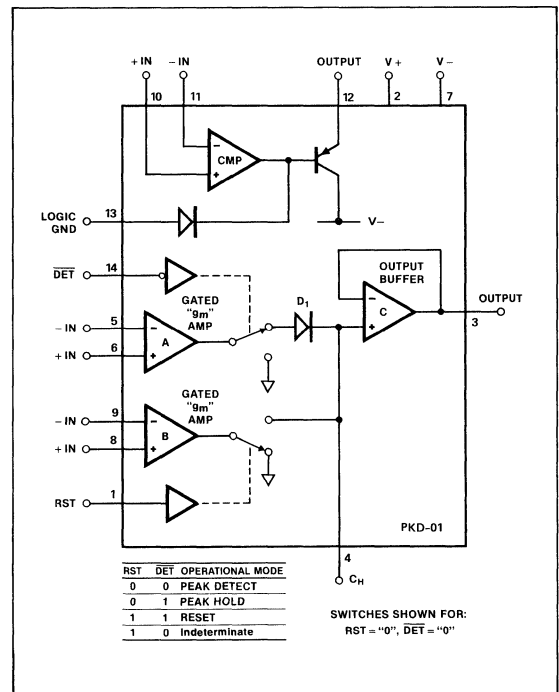
Through the $\overline{\text{DET}}$ control pin, new peaks may either be detected or ignored. Detected peaks are presented as positive output levels. Positive or negative peaks may be detected without additional active circuits since amplifier A can operate as an inverting or noninverting gain stage.

An uncommitted comparator provides many application options. Status indication and logic shaping/shifting are typical examples.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



SPECIAL FUNCTIONS

15



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage $\pm 18V$
 Power Dissipation 500mW
 Input Voltage Equal to Supply Voltage
 Logic and Logic Ground
 Voltage Equal to Supply Voltage
 Output Short-Circuit Duration Indefinite
 Amplifier A or B Differential Input Voltage $\pm 24V$
 Comparator Differential Input Voltage $\pm 24V$
 Comparator Output Voltage
 Equal to Positive Supply Voltage
 Hold Capacitor Short-Circuit Duration Indefinite
 Lead Temperature (Soldering, 60 sec) 300°C
 Storage Temperature Range
 PKD01AY, PKD01BY -65°C to +150°C
 PKD01EY, PKD01FY -65°C to +150°C
 PKD01EP, PKD01FP -65°C to +125°C

Operating Temperature Range

PKD01AY, PKD01BY -55°C to +125°C
 PKD01EY, PKD01FY -25°C to +85°C
 PKD01EP, PKD01FP 0°C to +70°C
 Dice Junction Temperature -65°C to +150°C

PACKAGE (Note 1)	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin DIP (Y)	80°C	10mW/°C
14-Pin DIP (P)	50°C	6mW/°C

NOTES:

1. Maximum package power dissipation vs. ambient temperature.
2. Absolute ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E			PKD01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	2	4	—	3	7	mV
Input Offset Voltage	V_{OS}		—	2	3	—	3	6	mV
Input Bias Current	I_B		—	80	150	—	80	250	nA
Input Offset Current	I_{OS}		—	20	40	—	20	75	nA
Voltage Gain	A_V		18	25	—	10	25	—	V/mV
Open-Loop Bandwidth	BW	$A_V = 1$	—	0.4	—	—	0.4	—	MHz
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	86	96	—	76	96	—	dB
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	± 12	—	± 11.5	± 12	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/ μs
Feedthrough Error		$\Delta V_{IN} = 20V, \overline{DET} = 1, RST = 0$, (Note 1)	66	80	—	66	80	—	dB
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$, (Note 1)	—	41	70	—	41	70	μs
Acquisition Time to 0.01% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$, (Note 1)	—	45	—	—	45	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	0.5	1.5	—	1	3	mV
Input Bias Current	I_B		—	700	1000	—	700	1000	nA
Input Offset Current	I_{OS}		—	75	300	—	75	300	nA
Voltage Gain	A_V	2k Ω Pull-up Resistor to 5V, (Note 1)	5	7.5	—	3.5	7.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	76	90	—	76	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	± 12.5	—	± 11.5	± 12.5	—	V

NOTES:

1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The

warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.

3. $\overline{DET} = 1, RST = 0$.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E			PKD01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 5V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	μA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	7	12	45	7	12	45	mA
Response Time	t_s	5mV Overdrive, (Note 3) 2k Ω Pull-up Resistor to 5V	—	150	—	—	150	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	1.6	10	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_j = 25^\circ C$, $T_A = 25^\circ C$ (See Note 2)	—	0.01	0.07	—	0.01	0.1	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$\overline{DET} = 1$ $R_L = 2.5k$	± 11.5	± 12.5	—	± 11	± 12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Switch Switching Time	t_s		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/ μs
Power Supply Current	I_{SY}	No Load	—	5	7	—	6	9	mA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55^\circ C \leq T_A \leq 125^\circ C$ for PKD01AY, PKD01BY, $-25^\circ C \leq T_A \leq 85^\circ C$ for PKD01EY, PKD01FY and $0^\circ C \leq T_A \leq 70^\circ C$ for PKD01EP, PKD01FP.

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E			PKD01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	4	7	—	6	12	mV
Input Offset Voltage	V_{OS}		—	3	6	—	5	10	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-9	-24	—	-9	-24	$\mu V/^\circ C$
Input Bias Current	I_B		—	160	250	—	160	500	nA
Input Offset Current	I_{OS}		—	30	100	—	30	150	nA
Voltage Gain	A_V		7.5	9	—	5	9	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	80	90	—	70	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	± 11	± 12	—	± 10.5	± 12	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/ μs
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$, (Note 1)	—	60	—	—	60	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	2	2.5	—	2	5	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-4	-6	—	-4	-6	$\mu V/^\circ C$
Input Bias Current	I_B		—	1000	2000	—	1100	2000	nA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55^\circ C \leq T_A \leq 125^\circ C$ for PKD01AY, PKD01BY, $-25^\circ C \leq T_A \leq 85^\circ C$ for PKD01EY, PKD01FY and $0^\circ C \leq T_A \leq 70^\circ C$ for PKD01EP, PKD01FP. (Continued)

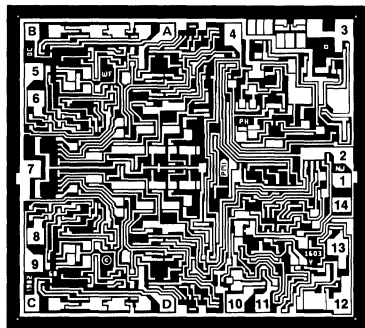
PARAMETER	SYMBOL	CONDITIONS	PKD01A/E			PKD01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2k Ω Pull-up Resistor to 5V, (Note 1)	4	6.5	—	2.5	6.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 1)	± 11	—	—	± 11	—	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 5V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	100	180	μA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	6	10	45	6	10	45	mA
Response Time	t_S	5mV Overdrive, 2k Ω Pull-up Resistor to 5V	—	200	—	—	200	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	T_j = Max. Operating Temp T_A = Max. Operating Temp. DET = 1, (Note 2)	—	1.2	10	—	3	15	mV/ms
			—	2.4	20	—	6	20	
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11	± 12	—	± 10.5	± 12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2	—	—	2	—	V/ μs
Power Supply Current	I_{SY}	No Load	—	5.5	8	—	6.5	10	mA

NOTES:

- Guaranteed by design.
- Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
- DET = 1, RST = 0.



DICE CHARACTERISTICS



- | | |
|------------------------------------|-----------------------------------|
| 1. RST (RESET CONTROL) | 9. INVERTING INPUT (B) |
| 2. V+ | 10. COMPARATOR NONINVERTING INPUT |
| 3. OUTPUT | 11. COMPARATOR INVERTING INPUT |
| 4. C _H (HOLD CAPACITOR) | 12. COMPARATOR OUTPUT |
| 5. INVERTING INPUT (A) | 13. LOGIC GROUND |
| 6. NONINVERTING INPUT (A) | 14. DET (PEAK DETECT CONTROL) |
| 7. V- | A, B (A) NULL |
| 8. NONINVERTING INPUT (B) | C, D (B) NULL |

DIE SIZE 0.090 × 0.100 inch, 9000 sq. mils
(2.286 × 2.54mm, 5.8 sq mm)

For additional DICE information refer to
1986 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V_{ZS}		7	mV MAX
Input Offset Voltage	V_{OS}		6	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		75	nA MAX
Voltage Gain	A_V		10	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, $\overline{DET} = 1$, RST = 0, (Note 1)	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2k Ω Pull-up Resistor to 5V, (Note 1)	3.5	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 5V	0.4 -0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	μA MAX
Output Short- Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7	mA MAX mA MIN

NOTES:

- Guaranteed by design.
- Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The

warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.

- $\overline{DET} = 1$, RST = 0.

**WAFER TEST LIMITS** at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
DIGITAL INPUTS-RST, DET (See Note 3)				
Logic "1" Input Voltage	V_H		2	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1	μA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	μA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$T_j = 25^\circ C$, $T_A = 25^\circ C$ (See Note 2)	0.1	mV/ms MAX
			0.20	mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11	V MIN
Short-Circuit Current: Amplifier C	I_{SC}		40	mA MAX
			7	mA MIN
Power Supply Current	I_{SY}	No Load	9	mA MAX

NOTES:

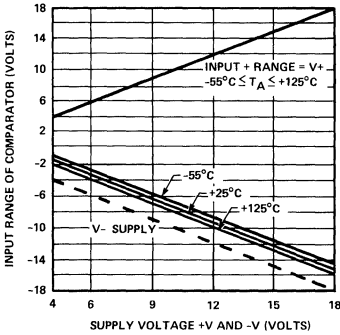
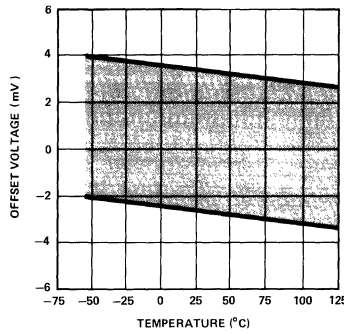
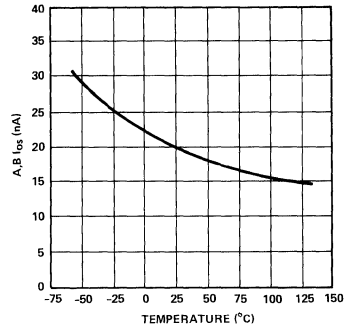
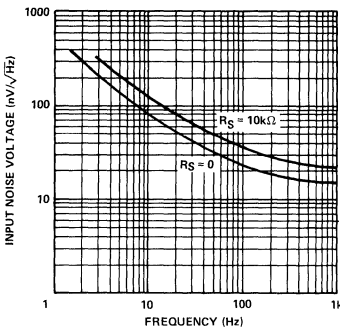
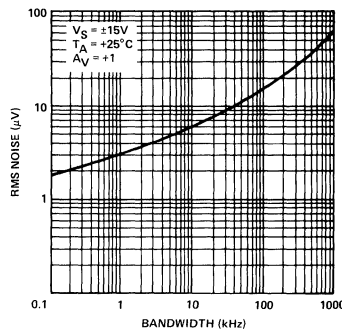
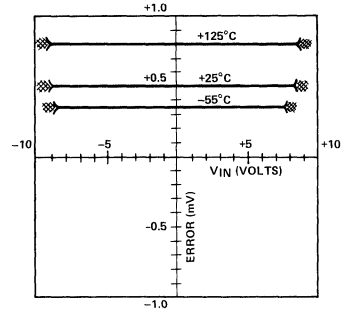
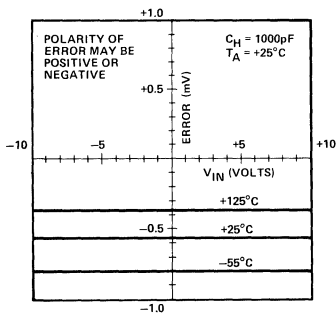
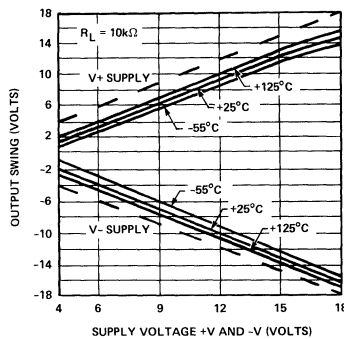
- Guaranteed by design.
- Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures. Ambient (T_A) temperature specifications are not subject to production testing.
- $\overline{DET} = 1$, $RST = 0$.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

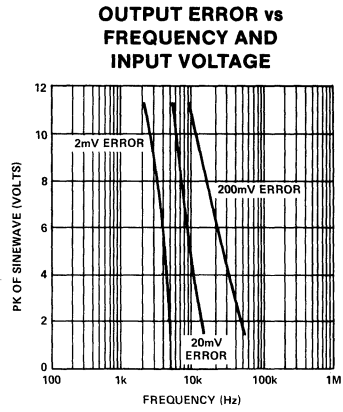
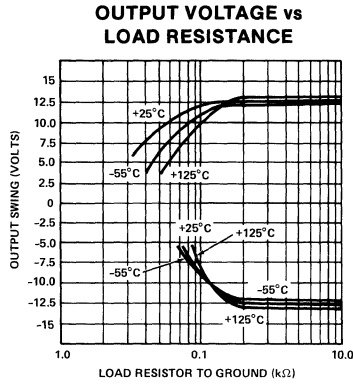
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PKD-01N TYPICAL	UNITS
"g_m" AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/ μs
Acquisition Time	t_a	0.1% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	41	μs
Acquisition Time	t_a	0.01% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	45	μs
COMPARATOR				
Response Time		5mV Overdrive, 2k Ω Pull-up Resistor to +5V	150	ns
MISCELLANEOUS				
Switch Aperature Time	t_{ap}		75	ns
Switching Time	t_s		50	ns
Buffer Slew Rate	SR	$R_L = 2.5k\Omega$	2.5	V/ μs

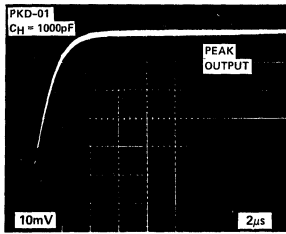
TYPICAL PERFORMANCE CHARACTERISTICS

A AND B INPUT RANGE vs SUPPLY VOLTAGE

A AND B AMPLIFIERS OFFSET VOLTAGE vs TEMPERATURE

A, B I_{OS} vs TEMPERATURE

INPUT SPOT NOISE vs FREQUENCY

WIDEBAND NOISE vs BANDWIDTH

AMPLIFIER B CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE

AMPLIFIER A CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE

OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (DUAL SUPPLY OPERATION)


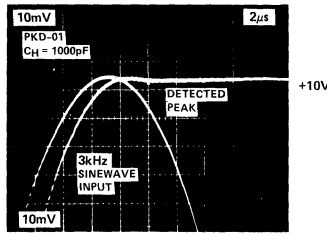
TYPICAL PERFORMANCE CHARACTERISTICS



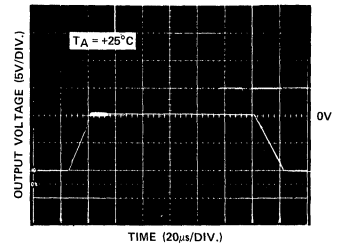
PKD-01 SETTling RESPONSE



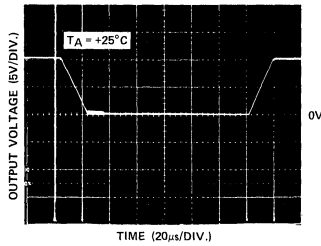
PKD-01 SETTling RESPONSE



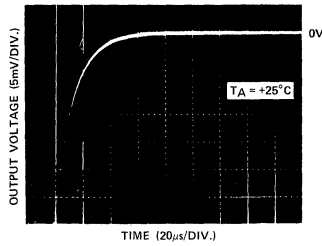
LARGE-SIGNAL INVERTING RESPONSE



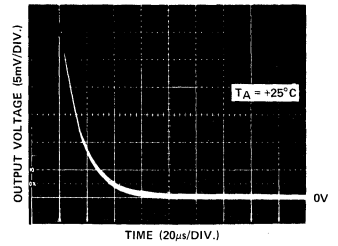
LARGE-SIGNAL NONINVERTING RESPONSE



SETTLING TIME FOR -10V TO 0V STEP INPUT

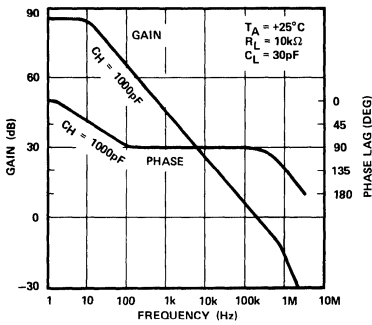


SETTLING TIME FOR +10V TO 0V STEP INPUT

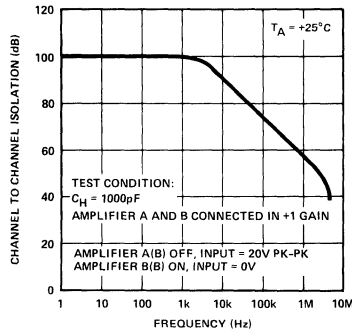


TYPICAL PERFORMANCE CHARACTERISTICS

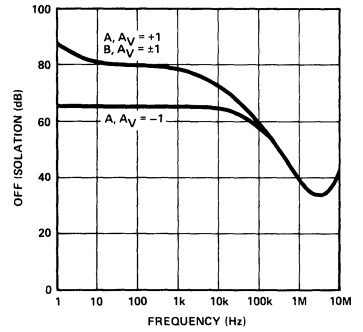
SMALL-SIGNAL OPEN LOOP GAIN/PHASE vs FREQUENCY



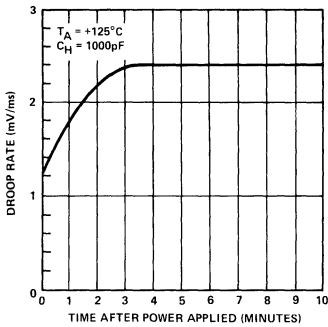
CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



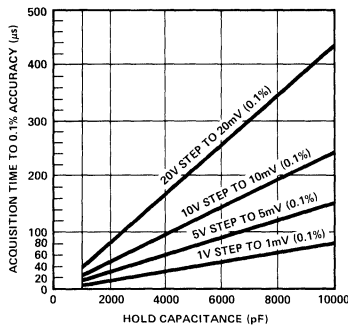
OFF ISOLATION vs FREQUENCY



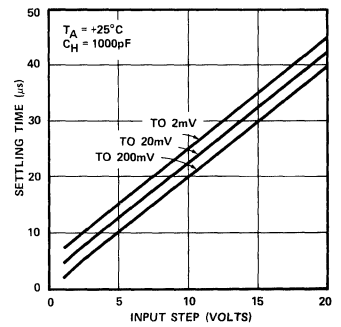
DROOP RATE vs TIME AFTER POWER ON



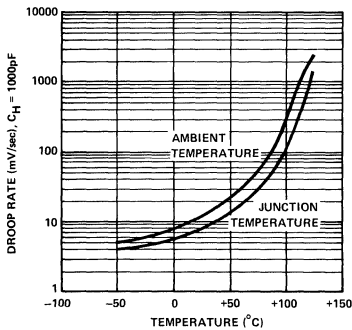
ACQUISITION TIME vs EXTERNAL HOLD CAPACITOR AND ACQUISITION STEP



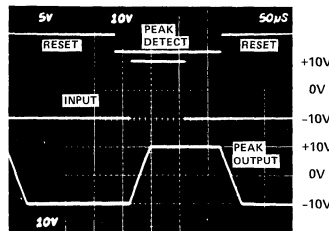
ACQUISITION TIME vs INPUT VOLTAGE STEP SIZE



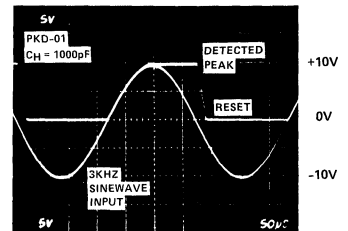
DROOP RATE vs TEMPERATURE

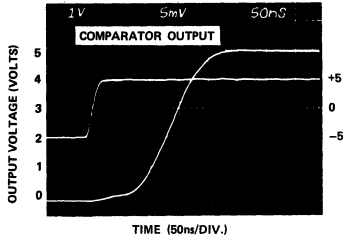
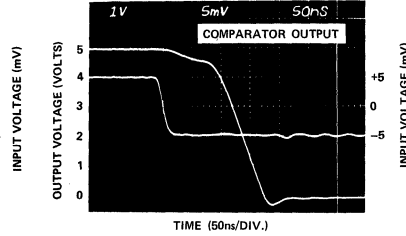
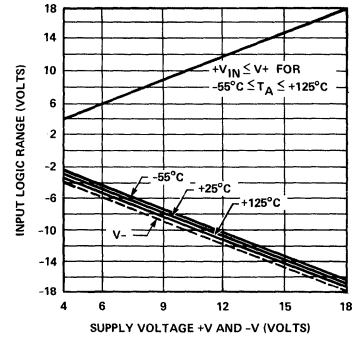
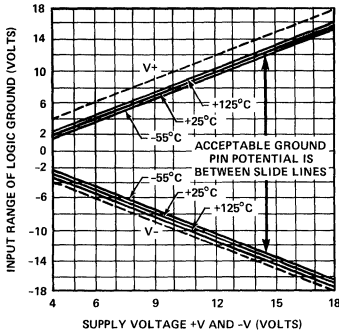
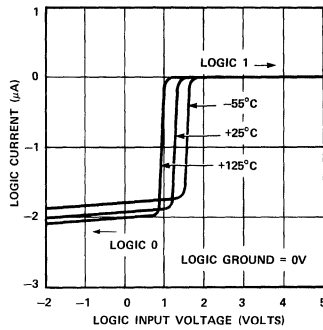
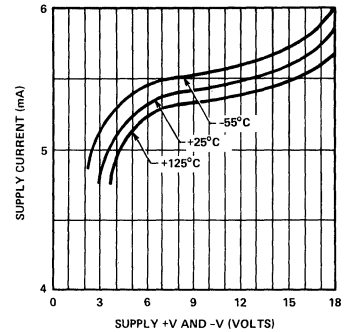
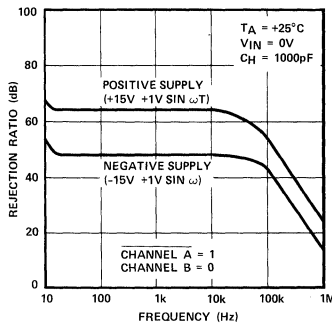


ACQUISITION OF STEP INPUT



ACQUISITION OF SINEWAVE PEAK

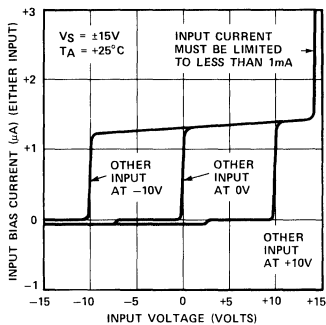


TYPICAL PERFORMANCE CHARACTERISTICS
**COMPARATOR OUTPUT
RESPONSE TIME
(2kΩ PULL-UP RESISTOR, T_A = +25°C)**

**COMPARATOR OUTPUT
RESPONSE TIME
(2kΩ PULL-UP RESISTOR, T_A = +25°C)**

**INPUT LOGIC RANGE vs
SUPPLY VOLTAGE**

**INPUT RANGE OF LOGIC
GROUND vs SUPPLY VOLTAGE**

**LOGIC INPUT CURRENT vs
LOGIC INPUT VOLTAGE**

**SUPPLY CURRENT vs
SUPPLY VOLTAGE**

**HOLD MODE POWER SUPPLY
REJECTION vs FREQUENCY**


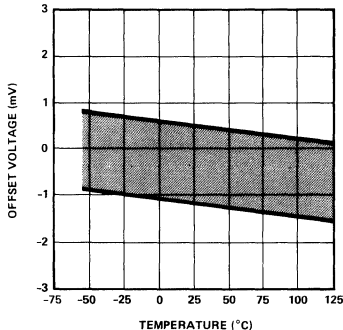


TYPICAL PERFORMANCE CHARACTERISTICS

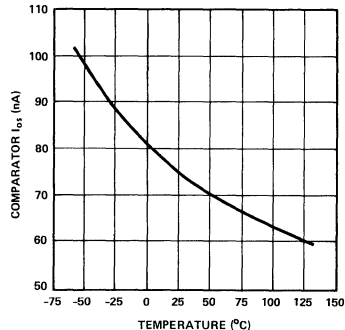
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



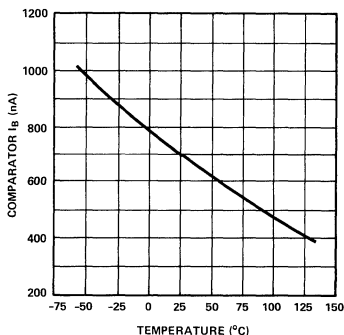
COMPARATOR OFFSET VOLTAGE vs TEMPERATURE



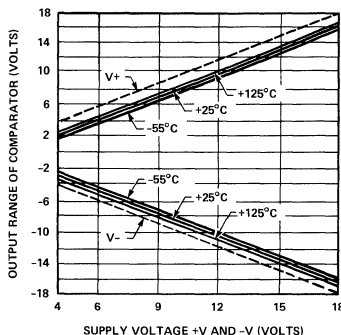
COMPARATOR IOS vs TEMPERATURE



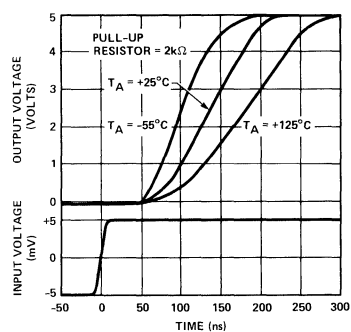
COMPARATOR IB vs TEMPERATURE



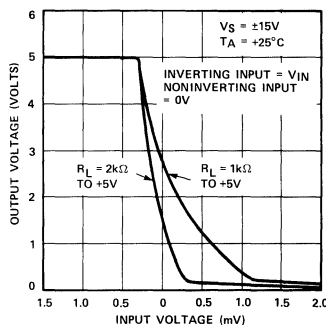
OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE



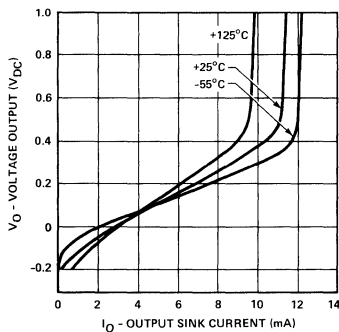
COMPARATOR RESPONSE TIME vs TEMPERATURE



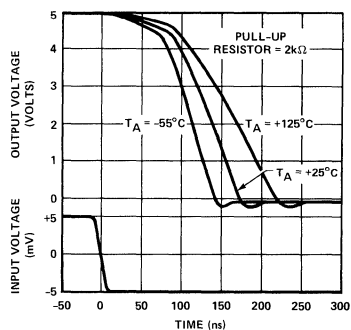
COMPARATOR TRANSFER CHARACTERISTIC



COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



COMPARATOR RESPONSE TIME vs TEMPERATURE



SPECIAL FUNCTIONS

15

THEORY OF OPERATION

The typical peak detector uses voltage amplifiers and a diode or an emitter follower to charge the hold capacitor, C_H , unidirectionally (Figure 1). The output impedance of A plus D_1 's dynamic impedance, r_d , make up the resistance which determines the feedback loop pole. The dynamic impedance is $r_d = \frac{kT}{qI_d}$. I_d is the capacitor charging current.

The pole moves toward the origin of the S plane as I_d goes to zero. The pole movement in itself will not significantly lengthen the acquisition time since the pole is enclosed in the system feedback loop.

When the moving pole is considered with the typical frequency compensation of voltage amplifiers there is however, a loop stability problem. The necessary compensation can increase the required acquisition time. PMI's approach replaces the input voltage amplifier with a transconductance amplifier; Figure 2.

The PKD-01 transfer function can be reduced to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + \frac{sC_H}{g_m} + \frac{1}{g_m R_{OUT}}} \approx \frac{1}{1 + \frac{sC_H}{g_m}}$$

Where: $g_m \approx 1\mu A/mV$, $R_{OUT} \approx 20M\Omega$.

The diode in series with A's output (Figure 2) has no effect because it is a resistance in series with a current source. In addition to simplifying the system compensation, the input transconductance amplifier output current is switched by current steering. The steered output is clamped to reduce and match any charge injection.

Fig. 3 shows a simplified schematic of the reset "g_m" amplifier, B. In the track mode, Q_1 & Q_4 are ON and Q_2 & Q_3 are OFF. A current of 2I passes through D_1 , I is summed at "B" and passes through Q_1 , and is summed with $g_m V_{IN}$. The current sink can absorb only 3I, thus, the current passing through D_2 can only be: $2K - g_m V_{IN}$. The net current into the hold capacitor node then, is $g_m V_{IN} (C_H = 2I - (2I - g_m V_{IN}))$. The hold mode, Q_2 & Q_3 are ON while Q_1 & Q_4 are OFF. The net current into the top of D_1 is -I until D_3 turns ON. With Q_1 OFF, the bottom of D_2 is pulled up with a current I until D_4 turns ON, thus D_1 & D_2 are reverse biased by $\approx 0.6V$ and charge injection is independent of input level.

The monolithic layout results in points A and B having equal nodal capacitance. In addition, matched diodes D_1 and D_2 have equal diffusion capacitance. When the transconductance amplifier outputs are switched open, points A and B are ramped equally but in opposite phase. Diode clamps D_3 and D_4 cause the swings to have equal amplitudes. The net charge injection (voltage change) at node C is therefore zero.

The peak transconductance amplifier, A, is shown in Figure 4. Unidirectional hold capacitor charging requires diode D_1 to be connected in series with the output. Upon entering the peak hold mode D_1 is reverse biased. The voltage clamp limits charge injection to approximately 1pC and the hold step to 0.6mV.

Minimizing acquisition time dictated a small C_H capacitance. A 1000pF value was selected. Droop rate was also minimized

by providing the output buffer with an FET input stage. A current cancellation circuit further reduces droop current and minimizes the gate current's tendency to double for every 10°C temperature change.

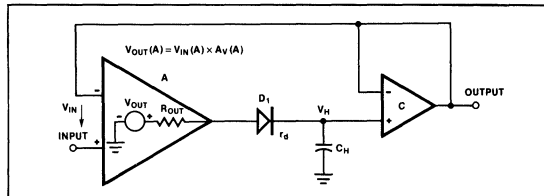


Figure 1. Conventional Voltage Amplifier Peak Detector

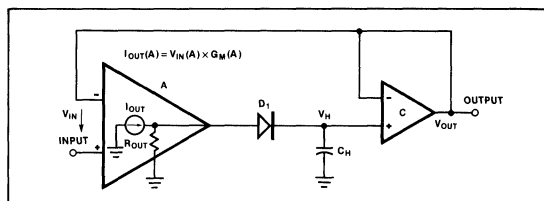


Figure 2. Transconductance Amplifier Peak Detector

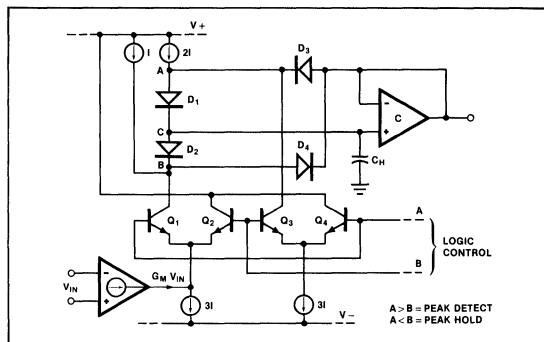


Figure 3. Transconductance Amplifier with Low Glitch Current Switch

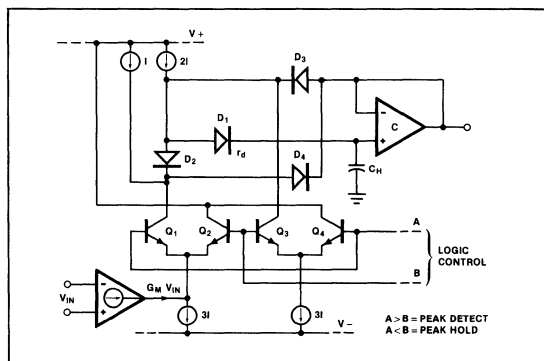


Figure 4. Peak Detecting Transconductance Amplifier with Switched Output

APPLICATIONS INFORMATION
OPTIONAL OFFSET VOLTAGE ADJUSTMENT

Offset voltage is the primary zero scale error component since a variable voltage clamp limits voltage excursions at D_1 's anode and reduces charge injection. The PKD-01 circuit gain and operational mode (positive or negative peak detection) determine the applicable null circuit. Figures A through D are suggested circuits. Each circuit corrects amplifier C offset voltage error also.

A. NULLING GATED OUTPUT g_m AMPLIFIER A. Diode D_1 must be conducting to close the feedback circuit during

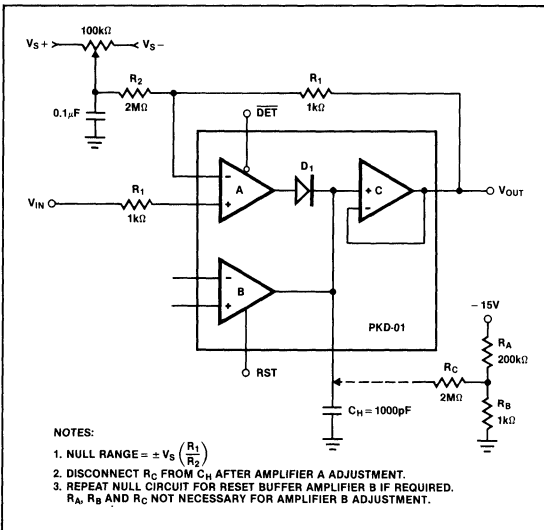


Figure A. V_{OS} Null Circuit for Unity Gain Positive Peak Detector

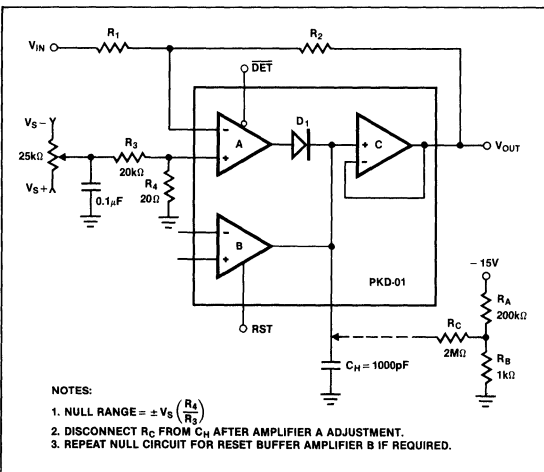


Figure C. V_{OS} Null Circuit for Negative Peak Detector

amplifier A V_{OS} adjustment. Resistor network $R_A - R_C$ cause D_1 to conduct slightly. With $DET = 0$ and $V_{IN} = 0V$ monitor the PKD-01 output. Adjust the null potentiometer until $V_{OUT} = 0V$. After adjustment, disconnect R_C from C_H .

B. NULLING GATED g_m AMPLIFIER B. Set amplifier B signal input to $V_{IN} = 0V$ and monitor the PKD-01 output. Set $DET = 1$, $RST = 1$ and adjust the null potentiometer for $V_{OUT} = 0V$. The circuit gain — inverting or noninverting — will determine which null circuit illustrated in Figures A through D is applicable.

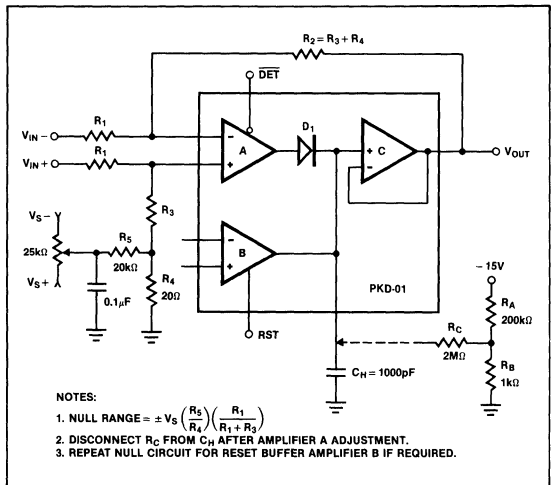


Figure B. V_{OS} Null Circuit for Differential Peak Detector

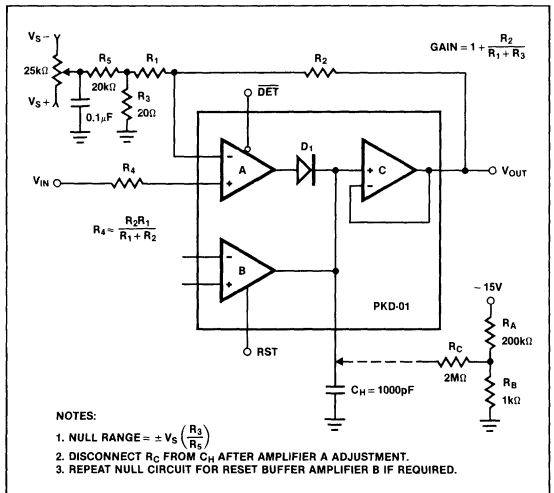


Figure D. V_{OS} Null Circuit for Positive Peak Detector With Gain

PEAK HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) serves as the peak memory element and compensating capacitor. Stable operation requires a minimum value of 1000pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase.

Zero scale error is internally trimmed for $C_H = 1000\text{pF}$. Other C_H values will cause a zero scale shift which can be approximated with the following equation.

$$\Delta V_{ZS}(\text{mV}) = \frac{1 \times 10^3(\text{pC})}{C_H(\text{nF})} - 0.6\text{mV}$$

The peak hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. This avoids digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point. To minimize gain errors and maintain the PKD-01's inherently low droop rate, guarding Pin 4 as shown in Figure 2 is recommended.

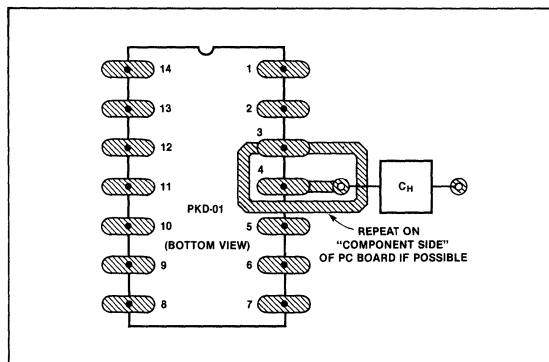


Figure 2. C_H terminal (Pin 4) guarding. See text.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

The maximum comparator high output voltage (V_{OH}) should be limited to:

$$V_{OH}(\text{maximum}) < V^+ - 2.0V$$

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1 .

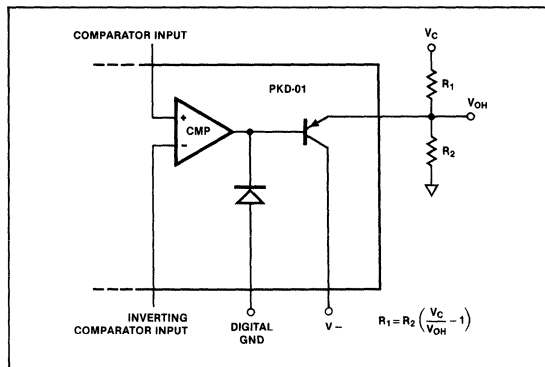


Figure 1

Table I.

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{SINK}}$$

$$R_2 \approx \left(\frac{1}{\frac{V_C}{V_{OH}} - 1} \right)$$

PEAK DETECTOR LOGIC CONTROL (RST, \overline{DET})

The transconductance amplifier outputs are controlled by the digital logic signals RST and \overline{DET} . The PKD-01 operational mode is selected by steering the current (I_1) through Q_1 and Q_2 , thus providing high-speed switching and a predictable logic threshold. The logic threshold voltage is 1.4 volts when digital ground is at zero volts.

Other threshold voltages (V_{TH}) may be selected by applying the formula:

$$V_{TH} \approx 1.4V + \text{Digital Ground Potential.}$$

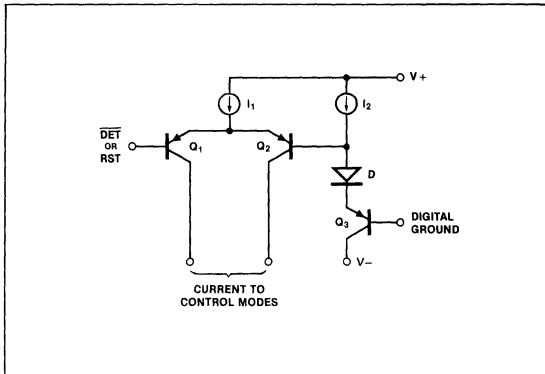
For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The RST or \overline{DET} signal must always be at least 2.8V above the negative supply.

Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

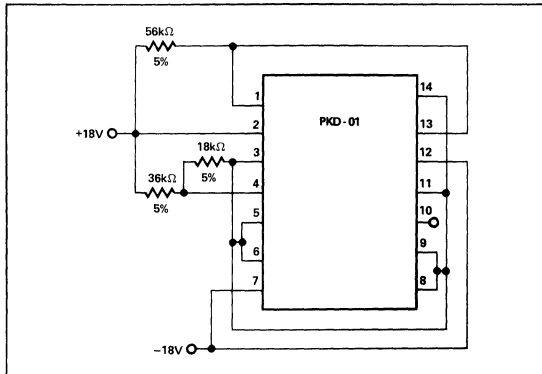
$$V_{OL} \approx 0.2V + \text{Digital Ground Potential.}$$



PKD-01 LOGIC CONTROL

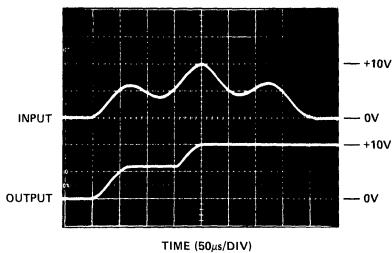


BURN-IN CIRCUIT

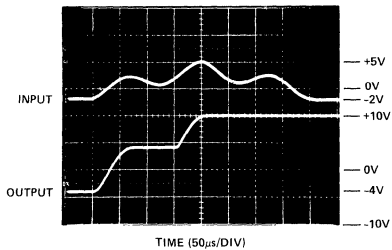


TYPICAL CIRCUIT CONFIGURATIONS

UNITY GAIN POSITIVE PEAK DETECTOR



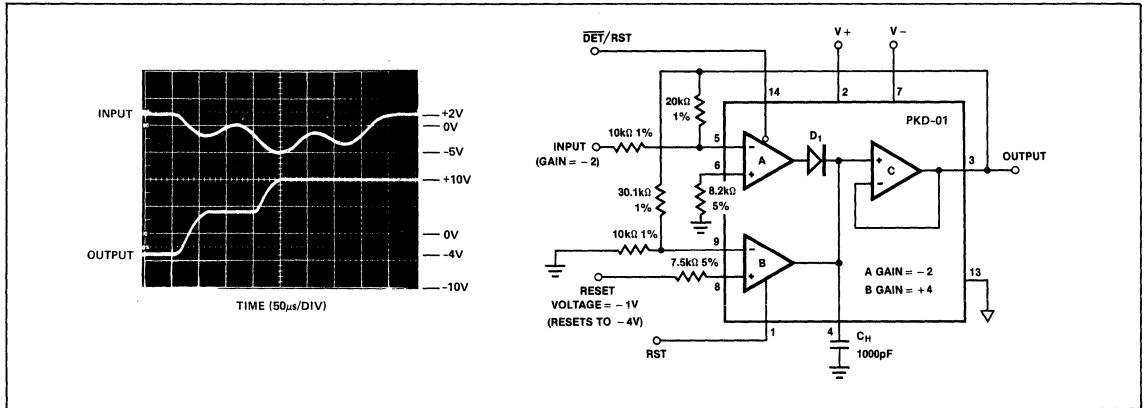
POSITIVE PEAK DETECTOR WITH GAIN



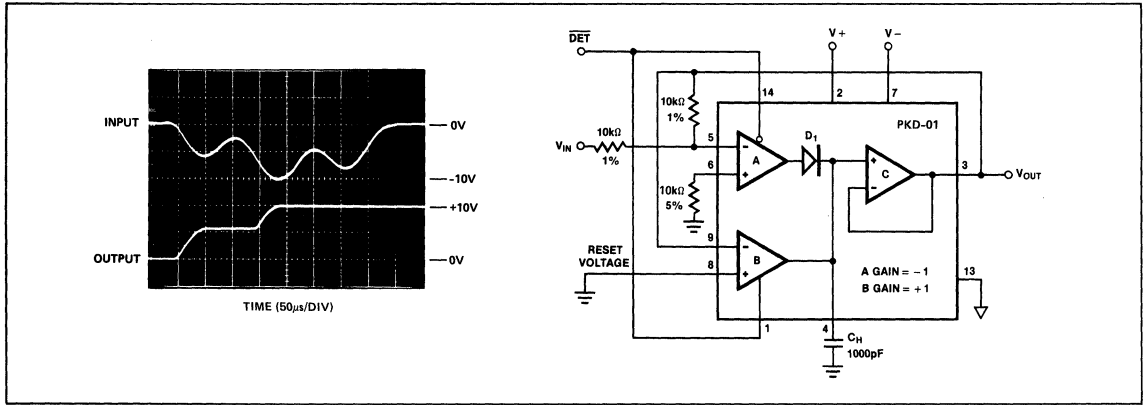
SPECIAL FUNCTIONS

15

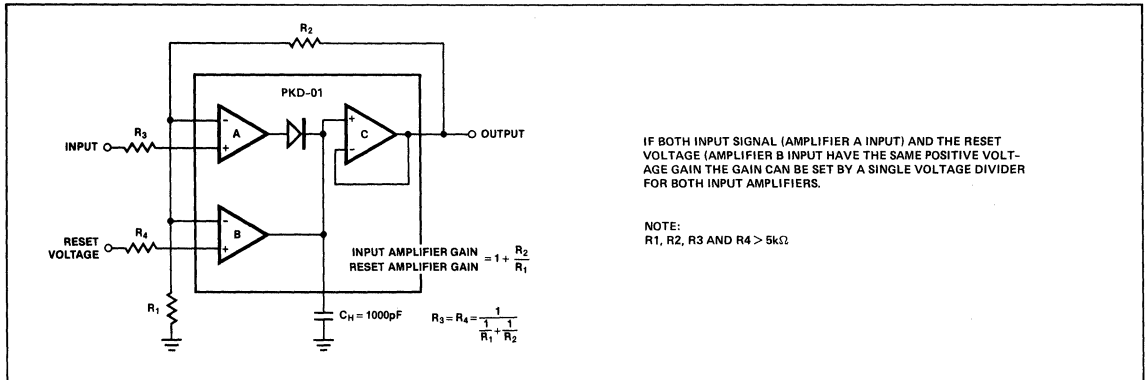
NEGATIVE PEAK DETECTOR WITH GAIN



UNITY GAIN NEGATIVE PEAK DETECTOR

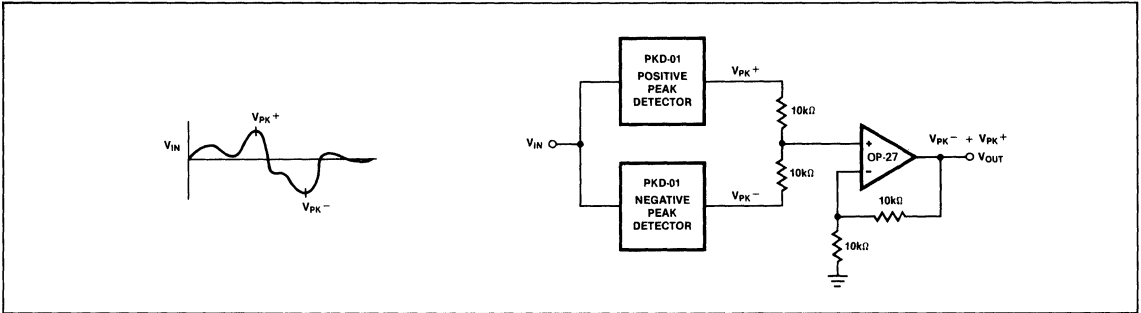


ALTERNATE GAIN CONFIGURATION

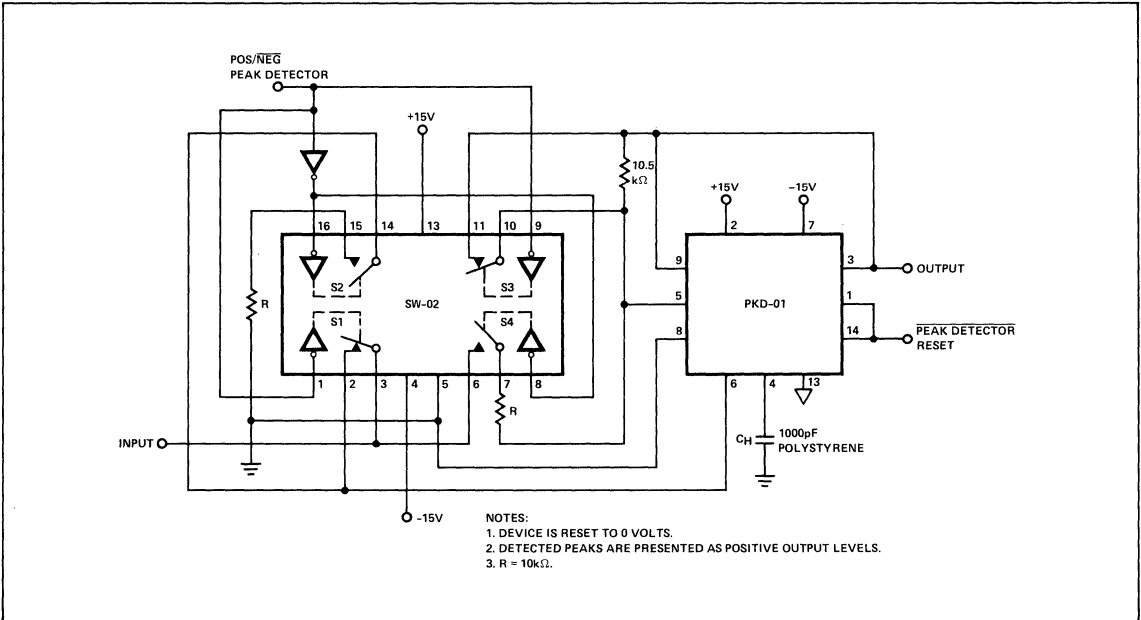




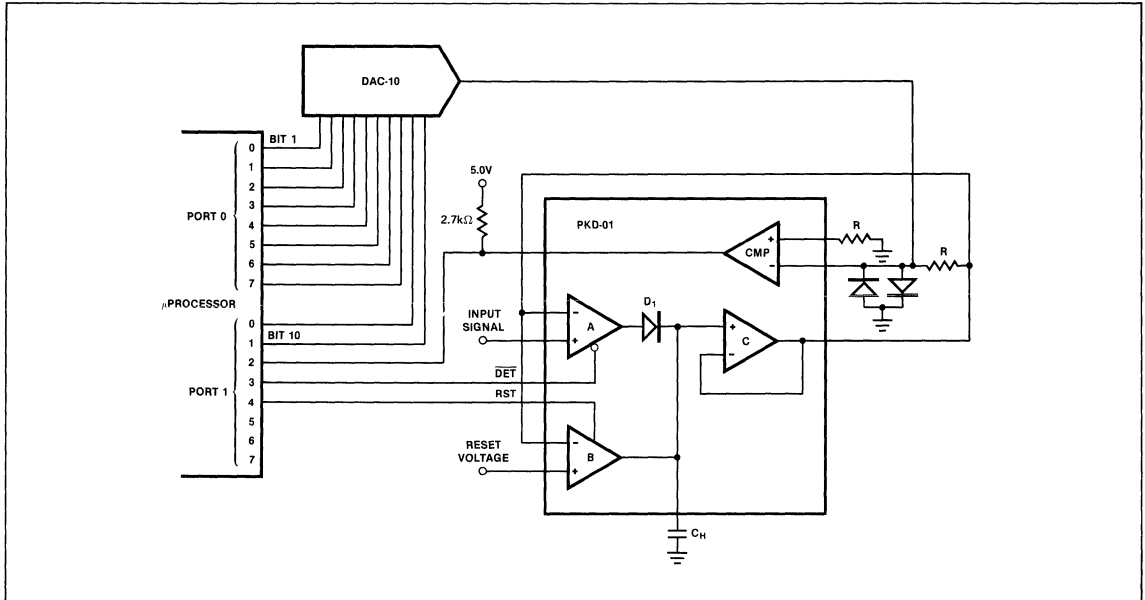
PEAK-TO-PEAK DETECTOR



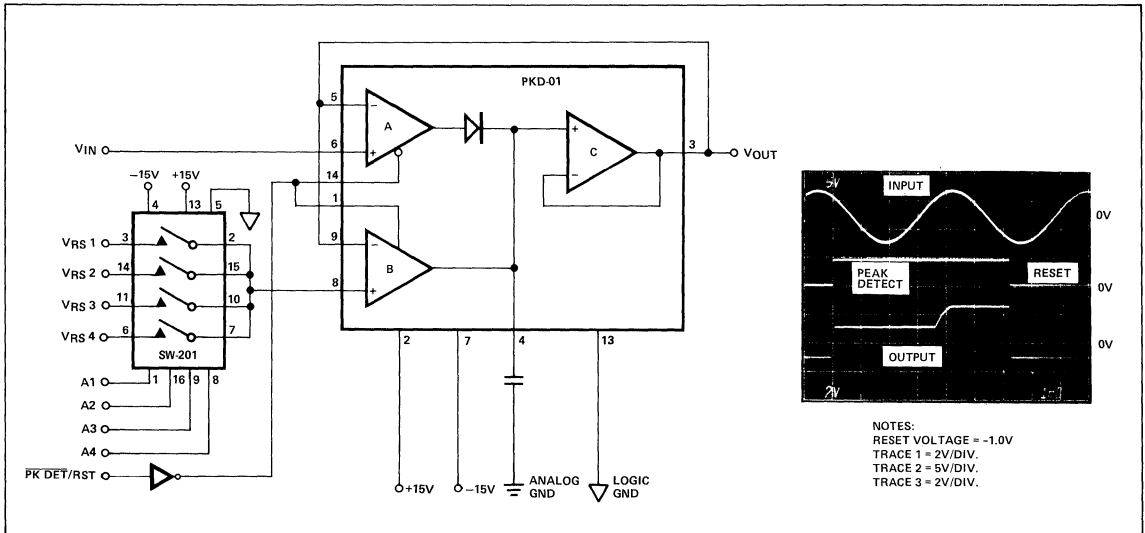
LOGIC SELECTABLE POSITIVE OR NEGATIVE PEAK DETECTOR



PEAK READING A/D CONVERTER

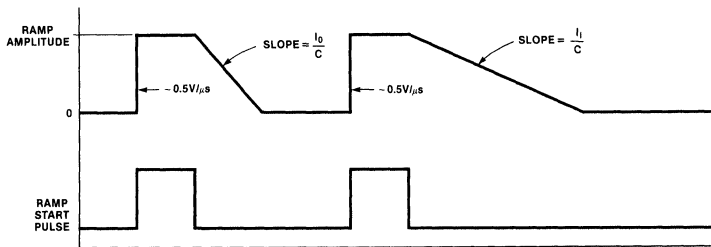
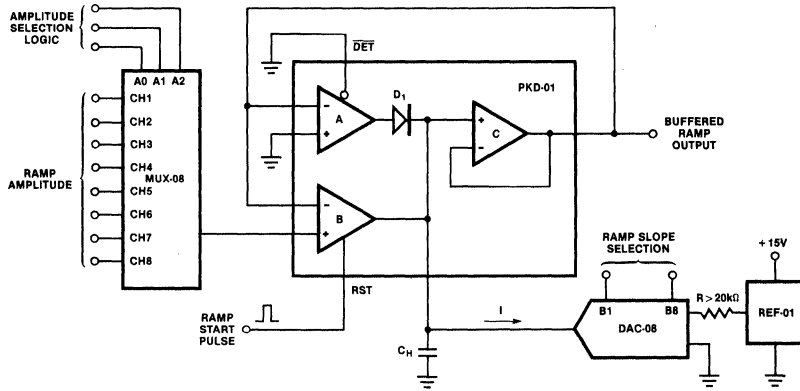


POSITIVE PEAK DETECTOR WITH SELECTABLE RESET VOLTAGE





PROGRAMMABLE LOW FREQUENCY RAMP GENERATOR



- NOTES:
 1. NEGATIVE SLOPE OF RAMP IS SET BY DAC-08 OUTPUT CURRENT.
 2. DAC-08 IS DIGITALLY CONTROLLED CURRENT GENERATOR.
 THE MAXIMUM FULL SCALE CURRENT MUST BE LESS THAN 0.5mA.

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



COMMUNICATIONS PRODUCTS

Precision Monolithics Inc.

16-3 Introduction

16-4 **RPT-82/RPT-83**

PCM Repeaters



COMMUNICATIONS PRODUCTS

Precision Monolithics Inc.

INTRODUCTION

PCM repeater circuits are used to regenerate alternate-mark-inversion pulses in PCM carrier systems operating at the 1.444-2.048 Mega-bits-per-second data rate. Information in a PCM system is transmitted over cable pairs by the presence or absence of pulses within specific time slots. A repeater-circuit amplifies degraded PCM pulses, sets an output flip-flop, and drives an output transformer that connects to the PCM cable pair. In addition, repeater amplifiers can be used for clock-recovery circuits in high-data-rate pulse transmission systems.

The PMI repeater amplifiers, RPT-82 and RPT-83, are monolithic integrated circuits that perform all of the necessary active functions for a PCM repeater. RPT-82 and RPT-83 are very similar; the primary functional difference is the incorporation of an automatic-clock-shutdown circuit in the RPT-83. When the signal into the RPT-83 becomes too low, the clock amplifier is automatically shut down to prevent the transmission of erroneous data. Both repeaters are fully described and specified in this section of the catalog.



RPT-82/RPT-83

PCM
REPEATERS

Precision Monolithics Inc.

FEATURES

- Automatic ALBO Function
- Clock-Shutdown Circuit (RPT-83)
- Low-Power Operation (100mW)
- Pin Compatible with XR-C277

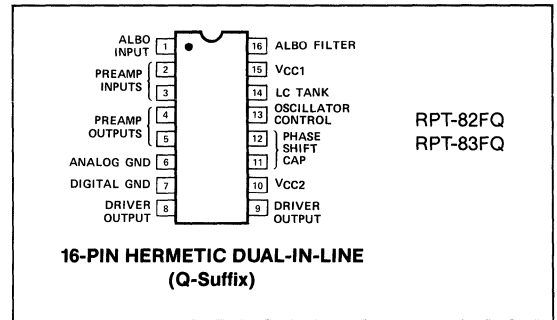
GENERAL DESCRIPTION

The RPT-82/83 are integrated circuits that perform the active functions required for regenerative PCM repeaters. They can operate from less than 100kHz to greater than 3MHz. In PCM systems, information is transmitted by the presence or absence of bipolar pulses in specified time slots. The RPT-82/83 repeaters automatically adjust gain to optimize signal levels, determine if a pulse is present or not, and retransmit the reconstructed pulses.

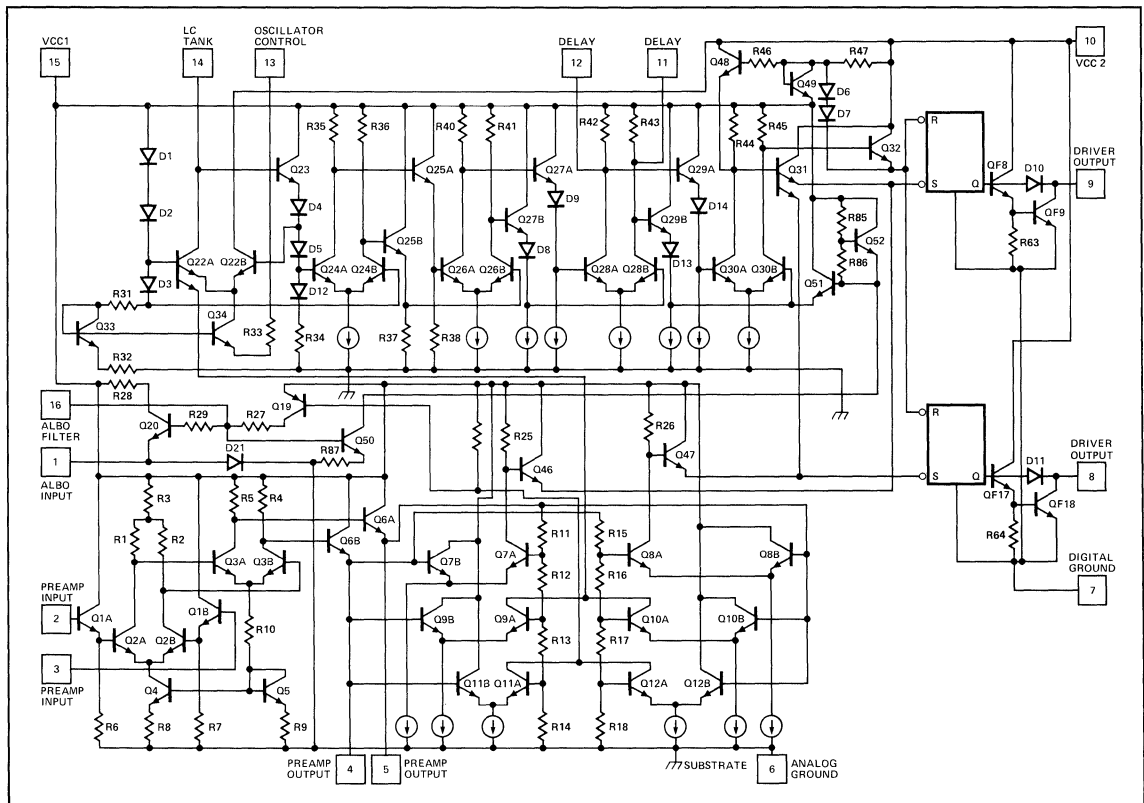
The difference between the RPT-82 and the RPT-83 is that the RPT-83 contains a **clock-shutdown circuit**. This shutdown circuit senses the incoming signal level and disables the clock

drive if the incoming signal is below the level where accurate reconstruction is possible. This prevents noise or cross-talk from appearing as a valid signal that would be retransmitted.

PIN CONNECTIONS & ORDERING INFORMATION



RPT-83 SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS**

Pin 10 to Pin 7 or 6	16.0V, -0.2V
Pin 15 to Pin 7 or 6	8.0V, -0.2V
Maximum Voltage at Pins 8 or 9	30V, -0.2V
Maximum Voltage at Pins 2, 3, 4, 5, 11, 12, 14	V_{CC2}
Maximum Sinking Current at Pin 8 or 9	300mA

Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	500mW
Lead Soldering Temperature	300°C

ELECTRICAL CHARACTERISTICS at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted. $V_{pin\ 6} = V_{pin\ 7} = V_{pin\ 13} = GND$.

PARAMETER	SYMBOL	CONDITIONS	RPT-82/RPT-83			UNITS
			MIN	TYP	MAX	
SUPPLY						
Supply Current	I_{CC1}	$T_A = 25^\circ C$ (Note 1)	5.0	8.5	9.5	mA
Supply Current	I_{CC2}	$T_A = 25^\circ C$ (Note 1)	1.0	2.5	3.5	mA
Total Supply Current	$I_{CC1} + I_{CC2}$	$T_A = 25^\circ C$ (Note 1)	6	11	13	mA
PREAMPLIFIER						
Preamplifier Open-Loop Gain	$\frac{\Delta V_{pin\ 5}}{\Delta V_{pin\ 2}}$	Measure $\Delta V_{pin\ 2}$ necessary to change pins from 1.9V to 3.2V	44	48	51	dB
Preamplifier Bandwidth	B_W	3dB Points (Note 2)	3	5	—	MHz
Preamplifier Input Impedance	Z_{IN}	Shunted by 2pF	—	600	—	k Ω
Preamplifier Input Offset Voltage	V_{OS}	$V_{pin\ 2} - V_{pin\ 3}$. (Note 1)	—	1	15	mV
Preamplifier Output Impedance	Z_{OUT}	(Note 2)	—	80	150	Ω
Preamplifier Output High	V_{OHA}	$V_{pin\ 4}$ with $V_{pin\ 2} = 2.5V$, $V_{pin\ 3} = 2.7V$, $T_A = 25^\circ C$.	3.35	3.45	3.75	V
Preamplifier Output Low	V_{OHL}	$V_{pin\ 4}$ with $V_{pin\ 2} = 2.5V$, $V_{pin\ 3} = 2.3V$, $T_A = 25^\circ C$.	1.0	1.4	1.45	V
Preamplifier Input Bias Current	I_B	$I_{pin\ 2}$ or $I_{pin\ 3}$ (Note 1)	—	1	4	μA
Preamplifier Input Offset Current	I_{OS}	$I_{pin\ 2} - I_{pin\ 3}$ (Note 1)	—	0.05	2	μA
OUTPUT DRIVE						
Output Voltage Swing	V_{OP}	$V_{pin\ 8\ High} - V_{pin\ 8\ Low}$, $V_{pin\ 9\ High} - V_{pin\ 9\ Low}$	—	6	—	V
Output Voltage, Low	V_{OL}	$T_A = 25^\circ C$, $I_{LOAD} = 15mA$	0.5	0.8	1.1	V
Differential Output Voltage, Low	V_{OLD}	$T_A = 25^\circ C$, $I_{LOAD} = 15mA$	—	0.02	0.15	V
Output Leakage Current	I_{OH}	$V_{pin\ 14} = 4.9V$, $V_{pin\ 8} = V_{pin\ 9} = 20V$, (Note 1) $T_A = 25^\circ C$	—	0.05	50	μA
Output Pulse Rise-Time	T_{OS}	(Note 2)	—	30	50	ns
Output Pulse Fall-Time	T_{of}	(Note 2)	—	10	60	ns
Output Pulse Width	P_w	At $f = 1.544\ MHz$	—	324	—	ns
Pulse-Width Differential	P_{wD}	(Note 2)	—	3	12	ns
Bipolar Violations at Maximum Density	$BV_1\ MAX$		—	0	—	—
Bipolar Violations with Quasi-Random Input Pattern	$BV_R\ MAX$		—	0	—	—
CLOCK CIRCUIT						
Tank Emitter-Follower Base Current	I_{TB}	$I_{pin\ 14}$, $V_{pin\ 14} = 4.9V$ (Note 1)	—	4	15	μA
Tank Input Impedance	Z_{INT}	Measured from pin 14 to pin 15	—	300	—	k Ω
Oscillator Bias Current	I_{OSC}	$V_{pin\ 14} = 3.9V$ ($I_{OSC} - I_{TB}$) (Note 1)	10	30	50	μA
Oscillator Injection Current	I_{INJ}	Set $V_{pin\ 4} - V_{pin\ 5} = \pm 1.4V$, $V_{pin\ 14} = 3.9V$ ($I_{INJ} - I_{OSC}$)	60	160	190	μA
Delay Circuit Resistor	R_d	Measured from pin 11 or pin 12 to pin 15, $T_A = 25^\circ C$	3.2	4.0	4.8	k Ω

NOTES:

- $V_{pin\ 2} = 2.5V$; adjust $V_{pin\ 3}$ until $V_{pin\ 4} = V_{pin\ 5}$.
- Sample tested.



ELECTRICAL CHARACTERISTICS at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$, unless otherwise noted.
 $V_{pin\ 6} = V_{pin\ 7} = V_{pin\ 13} = GND$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	RPT-82/RPT-83			UNITS
			MIN	TYP	MAX	
MISCELLANEOUS						
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 4 and 5, required to activate the Peak Detector. $T_A = 25^{\circ}C$	1.35	1.5	1.65	V
Clock Threshold	V_{TC}	Differential voltage, measured between pins 4 and 5, required to activate the Clock Detector. $T_A = 25^{\circ}C$	0.85	1.0	1.2	V
Data Threshold	V_{TL}	Differential voltage, measured between pins 4 and 5, required to activate the Data Detector. $T_A = 25^{\circ}C$	0.65	0.75	0.85	V
Clock Threshold as % of ALBO Voltage	V_{TC}	$T_A = 25^{\circ}C$	67	73	78	%
Data Threshold as % of ALBO Voltage	V_{TL}	$T_A = 25^{\circ}C$	46	54	58	%
ALBO ON Voltage	V_{O16}	Measured at pin 16, [$V_{p4} - V_{p5}$] = ALBO Threshold	1.0	1.7	2.5	V
ALBO OFF Voltage	V_{F16}	Measured at pin 16 and pin 1 $T_A = 25^{\circ}C$ (Note 1)	—	—	75	mV
Minimum ALBO Diode Resistance	R_D MIN		—	8	—	Ω
Maximum ALBO Diode Resistance	R_D MAX		—	30	—	k Ω
ALBO Gain Range	A_m	(Note 3)	36	48	—	dB

NOTES:

1. $V_{pin\ 2} = 2.5V$; adjust $V_{pin\ 3}$ until $V_{pin\ 4} = V_{pin\ 5}$.

2. Sample tested.

3. Guaranteed by design.

FUNCTIONAL DESCRIPTION

Bipolar-pulse transmission, the transmission of alternately positive and negative pulses, is used on repeater lines to remove the DC component present in unipolar PCM pulse trains. This also places the principal energy components in the 0-1.544MHz band, as opposed to the 0-3.088MHz band for

unipolar pulse trains. The absence of a DC component in bipolar pulse trains permits the repeater to be transformer-coupled to the repeater line and helps prevent time-shifting of the regenerator firing levels with variations in input pulse density (see Figure 1).

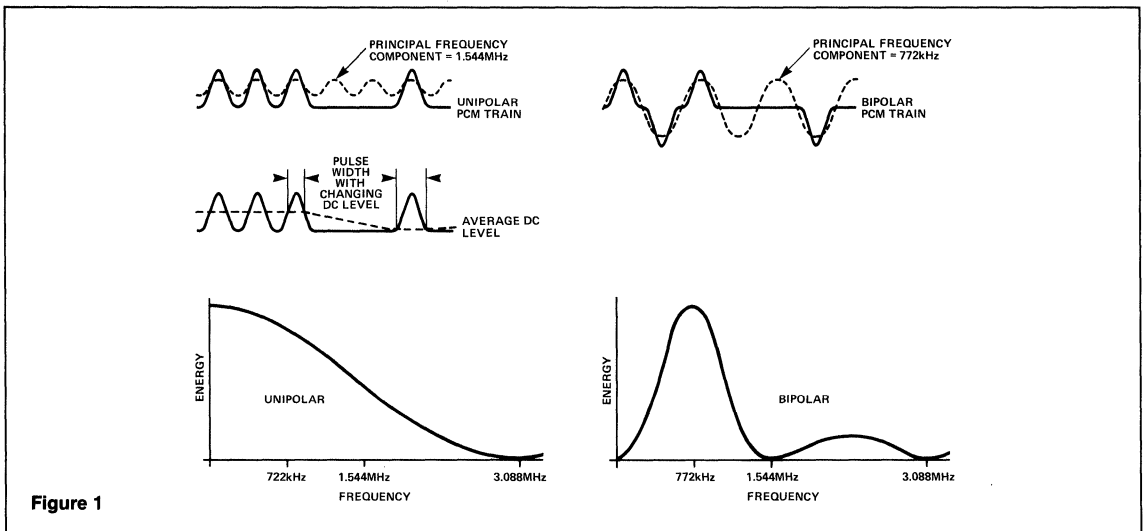
ENERGY SPECTRA OF BIPOLAR AND UNIPOLAR PULSE TRAINS

Figure 1

FUNCTIONAL BLOCK DIAGRAM

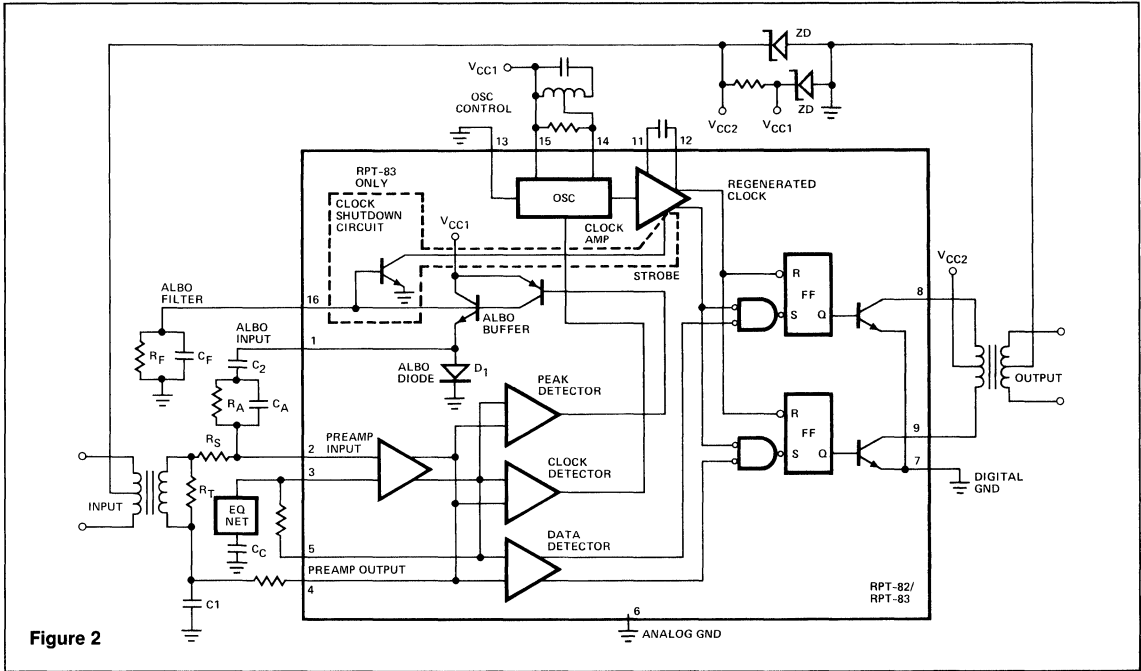


Figure 2

The bipolar-PCM pulse train is transformer-coupled into the preamplifier as shown in the functional block diagram (Figure 2). The secondary of the input transformer is loaded with the proper terminating resistor, R_T , to match the line impedance. One side of the transformer secondary is AC-coupled to ground by capacitor C_1 ; the other side of the secondary winding is in series with resistance R_S . Resistor R_S and the RC network $R_A C_A$ are AC-coupled to the ALBO input by capacitor C_2 . The impedance of the ALBO (Automatic Line Build-Out) input to ground is governed by the amount of current through the ALBO diode. R_S , in series with $R_A C_A$, provides signal attenuation proportional to the current flowing through the ALBO diode. When minimum current flows through the ALBO diode, C_2 is effectively isolated from ground and the input signal attenuation is minimal. The ALBO diode range of 8Ω to $30k\Omega$ provides compensation for line losses of approximately 5dB to 41dB.

The preamplifier stage amplifies the input signal and applies it to the three comparators labeled **data detector**, **clock detector**, and **peak detector**, respectively. Each comparator provides an output whenever the signal exceeds the trip point on both positive and negative pulses. Each comparator trips at a different threshold. The data detector is set to trip at the 54% point; the clock detector trips at the 73% point; and the peak detector trips at peak amplitude. Thresholds and waveforms are shown in Figure 3.

Current pulses from the peak detector are integrated by the capacitor in the ALBO filter. This causes a relatively constant

current to flow through the emitter follower and D_1 . In the RPT-83, a low voltage at the ALBO filter enables the clock-shutdown circuit when there is no input signal. The clock-shutdown circuit turns off the clock amplifier so that neither the regenerated clock, nor the strobe outputs, are sent to the flip-flops. This prevents the RPT-83 from sending noise or crosstalk out as valid-appearing data pulses when the incoming data level is too low.

The clock detector output locks the oscillator to the input frequency. The following amplifier stages shape the oscillator

THRESHOLDS AND WAVEFORMS

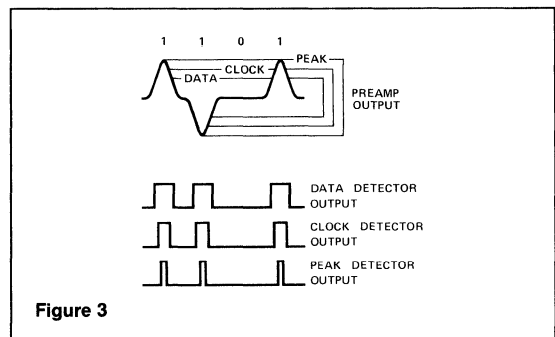


Figure 3

output and shift it in time. The phase-shift capacitor is selected to provide additional phase-shift so that the strobe pulses will occur at the center of the incoming pulses. This provides optimum timing for determining if a "1" or a "0" is present. A 0-to-30pF capacitor (10pF is typical at 1.544MHz) will optimize the performance of the complete repeater.

The delayed regenerated clock and the data-detector outputs drive the input flip-flops and output transistors. The output transistors are coupled to the transmission line through an output transformer.

DETAILED DESCRIPTION

PREAMPLIFIER

The preamplifier performs two basic functions. The first is to raise the level of the incoming signal to the correct level to trip the comparators. The second is to provide frequency/gain compensation to enhance the signal-to-noise ratio of the incoming signal. The preamp is designed to be operated in a near open-loop condition. A limited amount of feedback is used to control the frequency response. The gain-phase relationship of the preamp (see Figures 4 and 5) implies that the feedback network must have 40dB attenuation or more at 20MHz and above to ensure stability.

ALBO

To enable the preamp to operate open-loop with a wide range of signal levels, the ALBO diode is connected between the preamp input and ground. Since the ALBO-diode conductance is directly proportional to the ALBO-diode current, and the ALBO diode is driven by the peak detector, any signal in excess of that required to trip the peak detector will be shunted to ground through the ALBO diode. This automatic-gain-control function maintains the signal at the optimum level to operate the clock and data detectors.

The combination of R_S and R_A , in parallel with both C_A and the series impedance of the ALBO diode, perform the following two functions: 1) the automatic-gain-control function previously described, and 2) the frequency/phase compensation for transmission-line losses.

FREQUENCY/PHASE COMPENSATION

Frequency/phase compensation is desirable for three reasons:

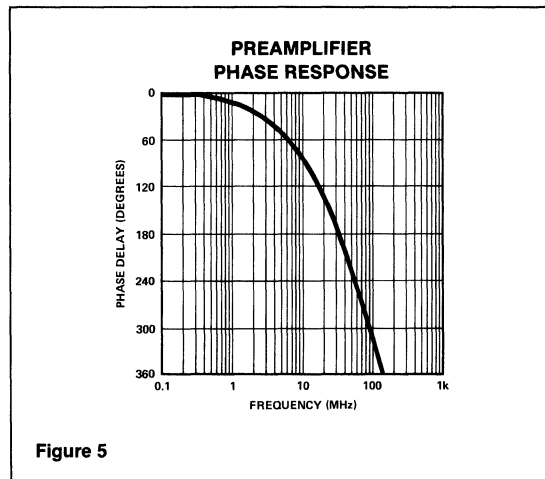
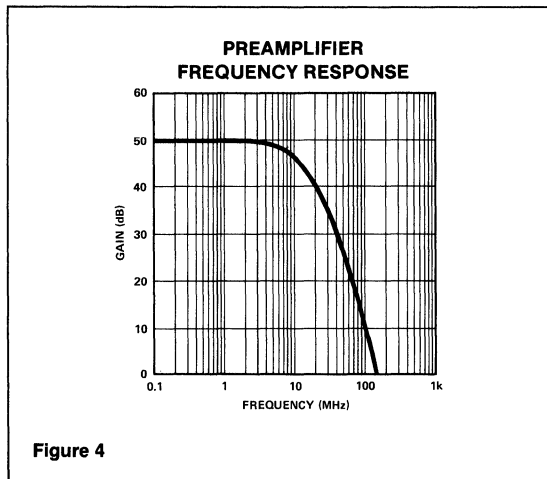
1. If the bandwidth is wider than necessary, noise and cross-talk outside of the signal-frequency band will appear at the threshold detectors. Out-of-band signals increase the probability that an incorrect logic decision will be made. These incorrect logic decisions will increase the bit error rate.
2. Nonlinear phase-shifts in the transmission line may cause the signal to be distorted to the extent that bit errors occur. Phase compensation in the repeater can partly correct for this problem.
3. Large phase-shifts in the preamplifier at high frequencies can cause instability if not compensated for by the feedback network. (See Figures 4 and 5).

CLOCK DETECTOR

The clock detector drives the clock-tank circuit with a pulse each time that the incoming signal is greater than 73% of the average peak signal.

PEAK DETECTOR

The peak detector drives the ALBO buffer and ALBO diode at the peak of the amplified "1" bits. Whenever the preamp AC-signal-output exceeds about 1.5V peak-to-peak, the ALBO buffer becomes forward biased and drives current into both the ALBO diode and the ALBO filter. This closed-loop AGC action maintains the preamp input signal at about 5mVp-p.



RPT-82/83 IN TYPICAL 1.544MHz T1 REPEATER SYSTEM

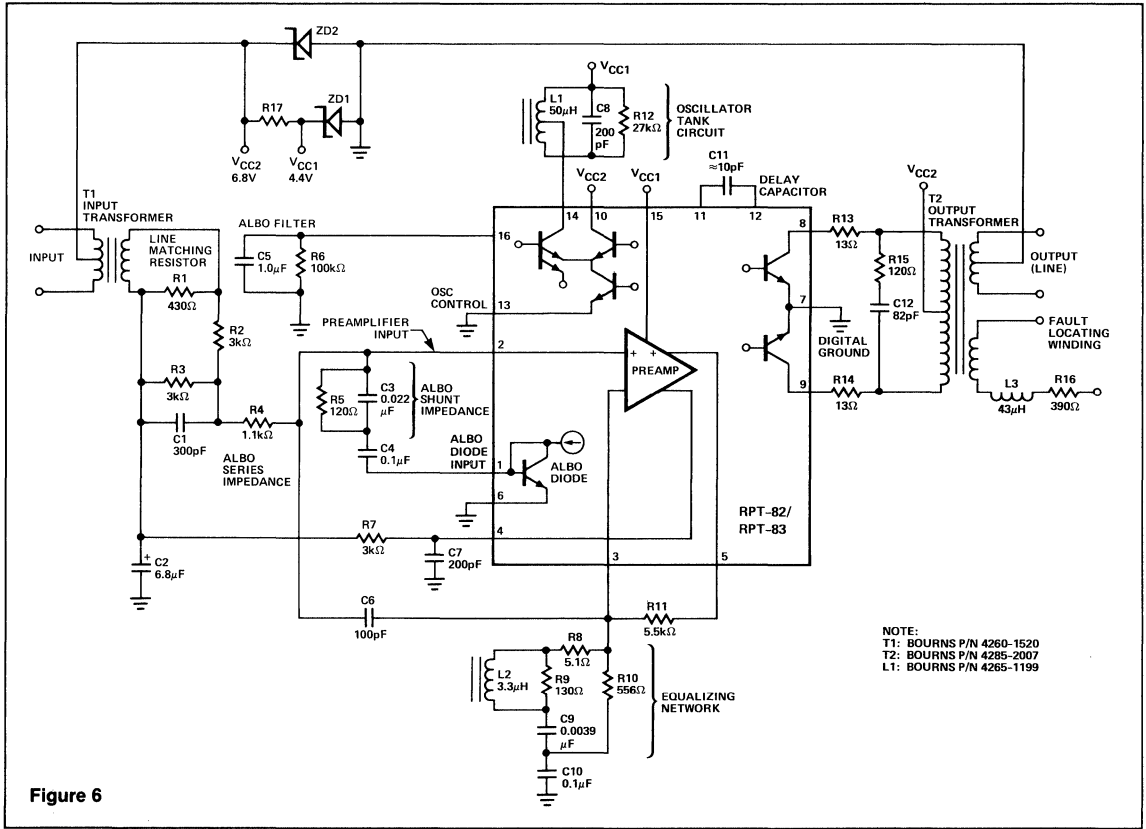


Figure 6

APPLICATION

In a typical T1, 1.544MHz repeater system (see Figure 6), the repeater is placed in series with a twisted-pair transmission line at distances of up to approximately 6000 feet. The power is supplied by a constant current of 60mA that is sent common-mode down the transmission line. This constant current is separated from the signal by input transformer T1 and output transformer T2, and is converted to voltages V_{CC1} and V_{CC2} by zener diodes Z_{D1} and Z_{D2} . The signal is coupled into the input network by T1. One end of T1 is held at AC ground by C2; and the other end is terminated by the line-matching resistor R1. The line-matching resistor is followed with a resistive attenuator consisting of R2 and R3, and the ALBO series impedance R4. The two resistors, R2 and R3, isolate the changing ALBO-diode impedance from the transmission line such that the transmission line is always correctly terminated. Resistor R4, in series with the shunt ALBO-diode impedance, determines the amount of attenuation provided at any given ALBO-diode current. Capacitor C1 provides a shunt path to ground for signals that are above the signal frequency.

When the ALBO-diode impedance is high, the ALBO series and shunt impedances have very little effect, so the unattenuated signal is applied to the preamp input with only C1 affecting the frequency response. When the ALBO-diode input impedance is reduced by higher signal levels, more of the input signal is shunted to ground through the ALBO shunt impedance.

The ALBO shunt impedance, C3 and R5, changes the input attenuation vs. frequency such that the system has more high frequency response at low signal levels, and less high frequency response at high signal levels. This change in bandwidth with signal level is intended to partially compensate for the increased high-frequency losses that occur in long transmission lines.

The bias feedback components between pin 4 and pin 2, consisting of C7, R7, and C2, operate as a DC self-biasing network. This C-R-C network prevents AC feedback and allows the preamp to establish a balanced input-and-output DC bias of 2.5 to 2.6 volts. Resistor R11 provides the DC path for biasing between pins 5 and 3.

Resistor R11 and capacitor C6 provide an AC feedback path. Resistors R10 and R11 act as an AC voltage divider that is shunted by the variable impedance of the resonant circuit comprised of L2 and C9. This frequency-selective feedback path, between pin 5 and pin 3, increases preamp gain at approximately 900kHz which further improves the system signal-to-noise ratio. The beneficial effect of the frequency-selective network is shown in Figure 7. The lower trace is a typical input signal (all 1's in this example) and the upper trace is the pre-amp output.

Figures 8 and 9 show the appearance of different preamp inputs measured at pin 5. Figure 8 is typical of an all 1's signal pattern with very little cross-talk or noise. Figure 9 shows a normal pattern of random 1's and 0's.

Due to the automatic-gain-control action of the ALBO circuitry, the peak amplitude is held constant for line losses of approximately 5dB to greater than 36dB. These signals are superimposed on a DC level of approximately 2.5V.

The preamp output drives the clock detector (reference Figures 2 and 6) which drives the clock-tank circuitry (L1, C8, and R12). The signal at pin 14, a sine wave of 0.2 to 1.0Vp-p (depending upon the percentage of 1-bits), drives the clock amplifier. The phase-shift capacitor, C11, provides the additional phase shift so that this integrated and phase-shifted signal (Figure 10) will strobe the output flip-flops at the optimum time to determine if a 1-bit is present. If a 1-bit is present, outputs from the data detector and the strobe cause the flip-flops to drive alternate output transistors. This signal is coupled through the output transformer into the next section of transmission line (see Figure 11, all 1's; and Figure 12, a random 1-0 pattern).

Figure 13 is a scope photograph of the signals as observed at several locations in the system. All traces are DC coupled and referenced to zero volts at the bottom graticule line. All signals, except the output, are displayed at 1-volt-per-division. The output is shown at 2-volts-per-division. The signal is all 1's. The phase relationships are typical for this type of repeater.

The signals shown are:

1. The preamp output at pin 5.
2. The clock-tank at pin 14.
3. The phase-shifted clock at pin 11.
4. The output signal at pin 8.

R13, 14, 15, and C12 control ringing and overshoot in the output waveform.

The fault-locating winding with L3 and R16 is used in long-line systems to determine which repeater, in a large series of repeaters, has become defective.

The RPT-82 and RPT-83 can be used in a variety of systems over a wide range of frequencies. The low-frequency response is limited by the difficulty in maintaining useable Q in the clock-tank circuit and by transformer-coupling losses. At high frequencies, the major limitation is the output-pulse rise-and-fall time.

The preamp is a high-gain, wide-bandwidth linear amplifier. Analog circuits do not have the noise rejection that is common with most digital circuits. To obtain best performance, certain precautions should be observed.

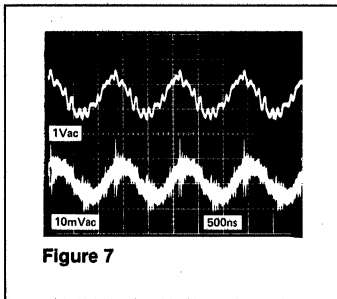


Figure 7

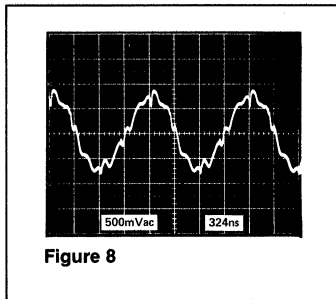


Figure 8

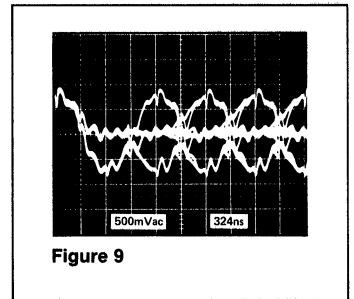


Figure 9

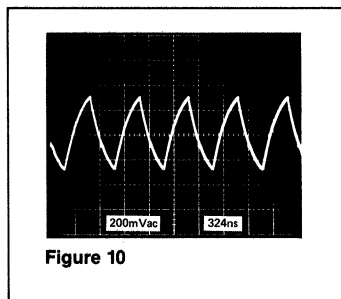


Figure 10

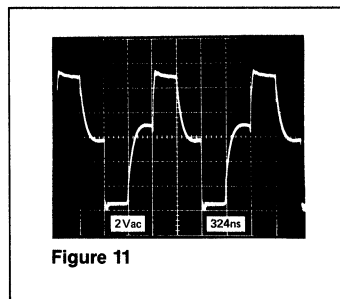


Figure 11

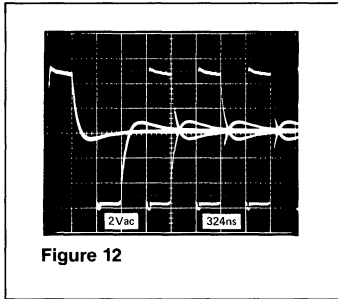


Figure 12

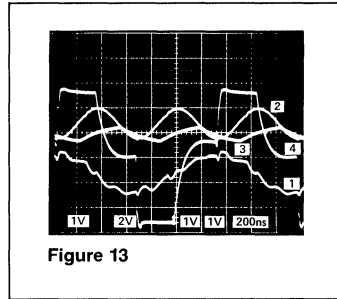


Figure 13

Circuit layout techniques used for R.F. amplifiers should be followed. Use of double-sided boards with all unused circuit-board area made into a ground plane is highly recommended. Keep input and output leads as far apart as possible, and signal runs as short as possible. Locate the attenuator network and the ALBO series impedance R4 as close to pin 2 as possible.

Power supply voltages V_{CC1} and V_{CC2} should be bypassed near pins 10 and 15. A bypass capacitor between the V_{CC2} connection on T_2 and pin 7 is also recommended.

REPEATER DEFINITIONS

ALBO DIODE RESISTANCE

The small-signal resistance of the ALBO diode measured between pins 1 and 6. The ALBO diode is a diode-connected transistor whose current-resistance relationship is $R_D = 26/I_D$ where R_D is the ALBO-diode resistance in ohms and I_D is the ALBO-diode current in mA.

ALBO THRESHOLD

The differential voltage measured between pins 4 and 5 that is required to activate the internal peak detector.

AMI

Alternate Mark Inversion. A form of digital signal transmission where each successive 1-bit is of opposite polarity.

AUTOMATIC LINE BUILD-OUT

An automatic-gain-control circuit which operates by simulating a line "build-out" or extension.

BIPOLAR VIOLATION

The transmission of two consecutive pulses of the same polarity.

CLOCK THRESHOLD

The differential voltage measured between pins 4 and 5 that is required to activate the clock detector.

DATA THRESHOLD

The differential voltage measured between pins 4 and 5 that is required to activate the data detector.

DIFFERENTIAL OUTPUT VOLTAGE

The difference in voltage between the two outputs with a binary "1" output of either polarity.

EQUALIZING NETWORK

A network which compensates for the amplitude and phase response of the cable over the operating bandwidth.

LINE BUILD-OUT

The attenuation added to the output of a short line to increase the total attenuation.

MAXIMUM DENSITY

An input signal pattern consisting of all 1's.

MINIMUM DENSITY

A repeating signal pattern consisting of two 1's followed by fourteen zeros.

OUTPUT-PULSE RISE (FALL) TIME

Rise (Fall) time of regenerated pulse. Measured from the 10% to 90% points.

OUTPUT-PULSE-WIDTH DIFFERENTIAL

In a T1 carrier system, a typical pulse width is 324nsec. The pulse-width differential is the difference in pulse width of two successive outputs.

PREAMPLIFIER BANDWIDTH

3dB bandwidth of the preamplifier circuit.

QRSS

QRSS is Quasi-Random Signal Source; a signal consisting of random 1's and 0's.

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



PACKAGE INFORMATION

Precision Monolithics Inc.

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Metal Cans			
H	6-Lead TO-78 Metal Can	—	17-3
J	8-Lead TO-99 Metal Can	A1	17-3
K	10-Lead TO-100 Metal Can	A2	17-3

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Ceramic DIPs			
Z	8-Lead Ceramic DIP	D4-1	17-4
Y	14-Lead Ceramic DIP	D1-1	17-4
Q	16-Lead Ceramic DIP	D2-1	17-5
X	18-Lead Ceramic DIP	D6-1	17-5
R	20-Lead Ceramic DIP	D8-1	17-6
V	24-Lead Ceramic DIP	D3-1	17-7
T	28-Lead Ceramic DIP	—	17-8

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Side-Brazed DIPs			
YB*	14-Lead Side-Brazed DIP	D1-3	17-9
QB*	16-Lead Side-Brazed DIP	D2-3	17-9
XB*	18-Lead Side-Brazed DIP	D6-3	17-10
RB*	20-Lead Side-Brazed DIP	D8-3	17-10
VB*	24-Lead Side-Brazed DIP	D3-3	17-11
TB*	28-Lead Side-Brazed DIP	—	17-12

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Epoxy DIPs			
P	8-Lead Epoxy DIP	—	17-13
P	14-Lead Epoxy DIP	—	17-13
P	16-Lead Epoxy DIP	—	17-14
P	18-Lead Epoxy DIP	—	17-14
P	20-Lead Epoxy DIP	—	17-15
P	24-Lead Epoxy DIP	—	17-16

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Cerpacks			
L	10-Lead Cerpack	—	17-17
M	14-Lead Cerpack	—	17-17
F	16-Lead Cerpack	—	17-18
N	24-Lead Cerpack	—	17-18

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Flatpacks			
L*	10-Lead Flatpack	F4-1	17-19
LB*	10-Lead Flatpack, Bottom-Brazed	F4-2	17-19
M*	14-Lead Flatpack	F1-1	17-19
MB*	14-Lead Flatpack, Bottom-Brazed	F1-2	17-19
F*	16-Lead Flatpack	F5-1	17-20
FB*	16-Lead Flatpack, Bottom-Brazed	F5-2	17-20
N*	24-Lead Flatpack	F8-1	17-20
NB*	24-Lead Flatpack, Bottom-Brazed	F8-2	17-20

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Leadless Chip Carriers			
RC*	20-Position Chip Carrier	C-2	17-21
TC*	28-Position Chip Carrier	C-4	17-22

*Special Order Only.

Dimensioning Symbols

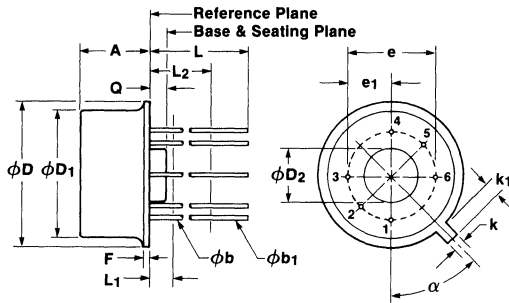
The symbols to be used for dimensioning case outlines will be as listed below. To designate the dimension as a diameter, the lower-case Greek letter ϕ (phi) will be added in front of the dimension symbol.

- A — Body dimensions.
- ϕb — Terminal lead diameters.
- b — Terminal lead widths.
- c — Terminal lead thicknesses.
- ϕD — Body diameters.
- D — Body lengths.
- E — Body widths.
- e — Terminal lead spacings.
- F — Flange dimensions.
- k — Index dimensions, length.
- L — Terminal lead lengths.
- Q — Standoff height. The height from the seating plane or a reference plane parallel to the seating plane.
- R — Radius dimensions.
- S — Distance between terminal leads and the body end.
- α — Angular dimensions.

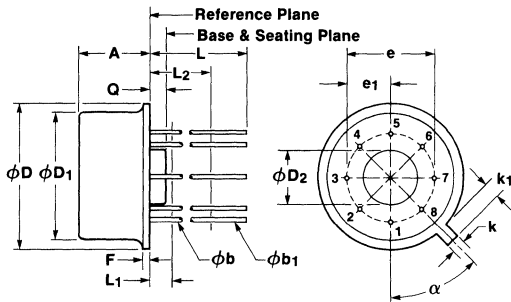
Standard lead finish is matte tin/lead. Other lead finishes per MIL-M-38510 are available on special orders. Standard 883 product meets lead finish requirements per MIL-M-38510.

PACKAGE DIMENSIONS — METAL CANS

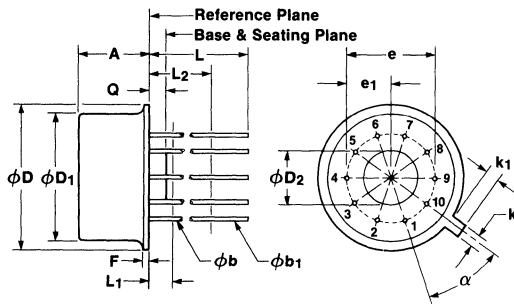
6-Lead TO-78 Metal Can (H-Suffix)



8-Lead TO-99 Metal Can (J-Suffix)



10-Lead TO-100 Metal Can (K-Suffix)



6 & 8-Lead Can Dimensions

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	—
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.335	0.370	8.51	9.40	—
ϕD_1	0.305	0.335	7.75	8.51	—
ϕD_2	0.110	0.160	2.79	4.06	—
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F	—	0.040	—	1.02	—
k	0.027	0.034	0.69	0.86	—
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1	—	0.050	—	1.27	1
L_2	0.250	—	6.35	—	1
Q	0.010	0.045	0.25	1.14	—
α	45° BSC		45° BSC		3

10-Lead Can Dimensions

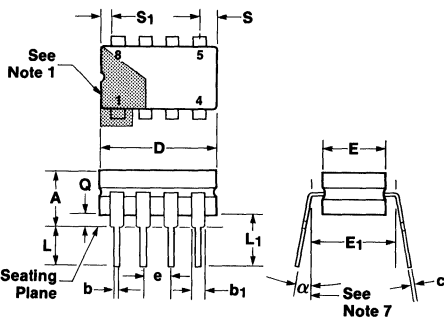
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	—
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.335	0.370	8.51	9.40	—
ϕD_1	0.305	0.335	7.75	8.51	—
ϕD_2	0.110	0.160	2.79	4.06	—
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F	—	0.040	—	1.02	—
k	0.027	0.034	0.69	0.86	—
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1	—	0.050	—	1.27	1
L_2	0.250	—	6.35	—	1
Q	0.010	0.045	0.25	1.14	—
α	36° BSC		36° BSC		3

NOTES:

- (All leads) ϕb applies between L_1 and L_2 . ϕb_1 applies between L_2 and 0.500 (12.70 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500 (12.70 mm) from the reference plane.
- Measured from the maximum diameter of the product.
- Leads having a maximum diameter 0.019 (0.48 mm) measured in gaging plane 0.054 (1.37 mm) + 0.001 (0.03 mm) - 0.000 (0.00 mm) below the base plane of the product is within 0.007 (0.18 mm) of their true position relative to a maximum width tab.

PACKAGE DIMENSIONS — CERAMIC DIPS

8-Lead Ceramic Dip

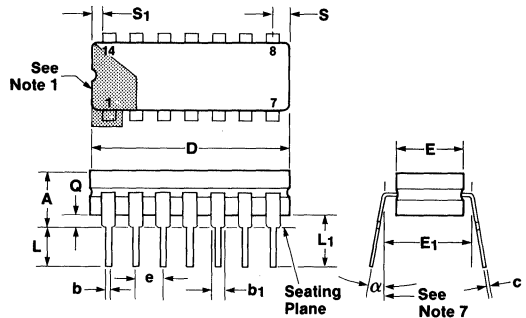


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.405	—	10.29	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.055	—	1.35	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.

14-Lead Ceramic Dip

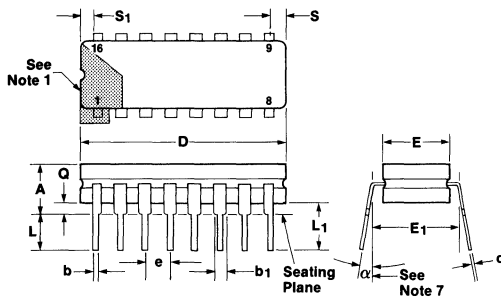


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.785	—	19.94	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — CERAMIC DIPS

16-Lead Ceramic Dip (Q-Suffix)

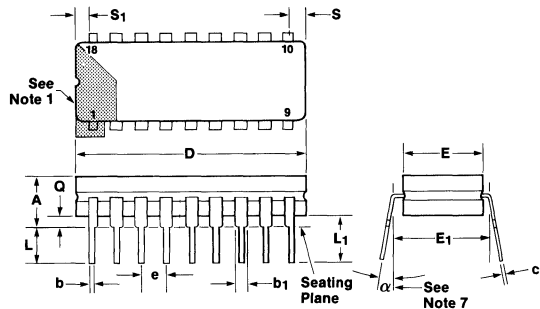


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.

18-Lead Ceramic Dip (X-Suffix)



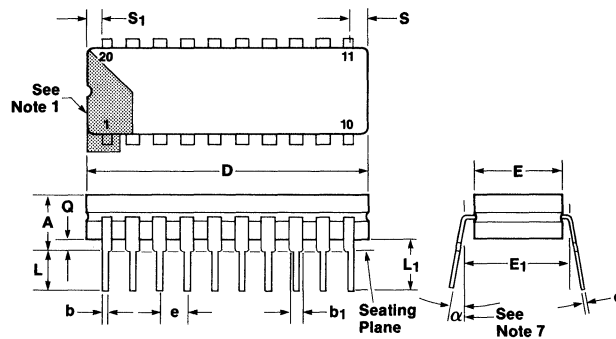
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

Precision Monolithics Inc.

PACKAGE DIMENSIONS — CERAMIC DIPS

20-Lead Ceramic Dip (R-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

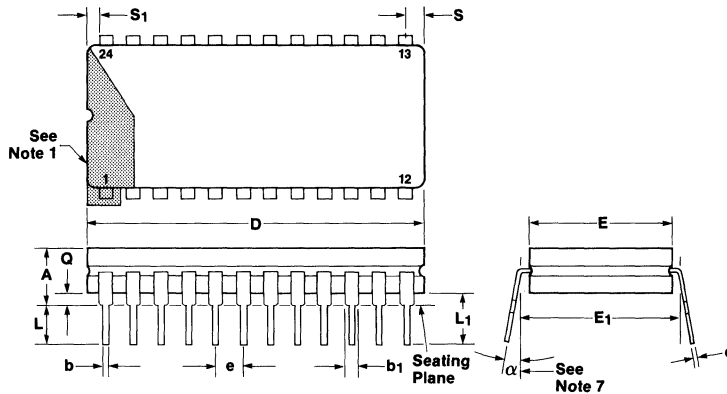


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — CERAMIC DIPS

24-Lead Ceramic Dip
(V-Suffix)



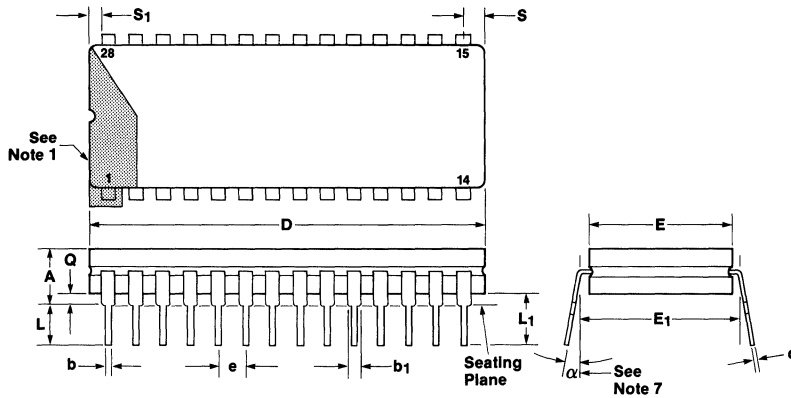
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E ₁	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — CERAMIC DIPS

28-Lead Ceramic Dip (T-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

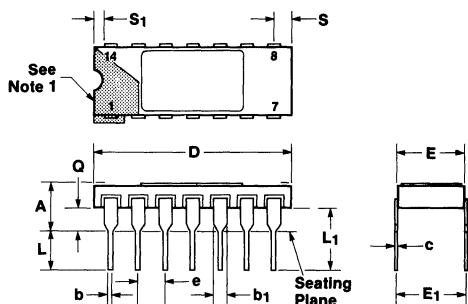
NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

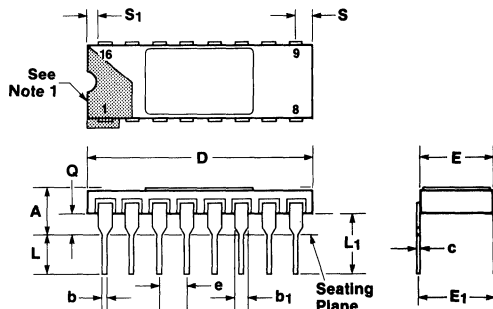
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PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

14-Lead Side-Brazed Dip (YB-Suffix)



16-Lead Side-Brazed Dip (QB-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.785	—	19.94	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

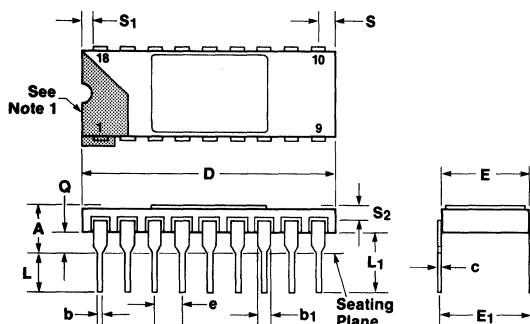
1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

18-Lead Side-Brazed Dip (XB-Suffix)

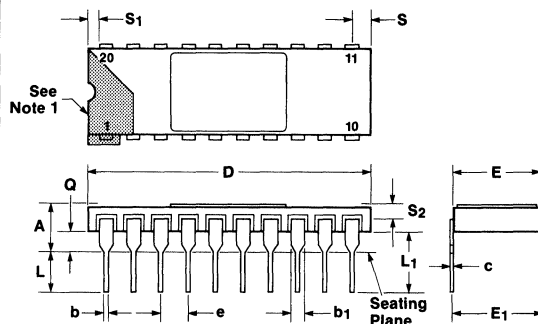


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

- Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
- The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
- Dimension Q shall be measured from the seating plane to the base plane.

20-Lead Side-Brazed Dip (RB-Suffix)

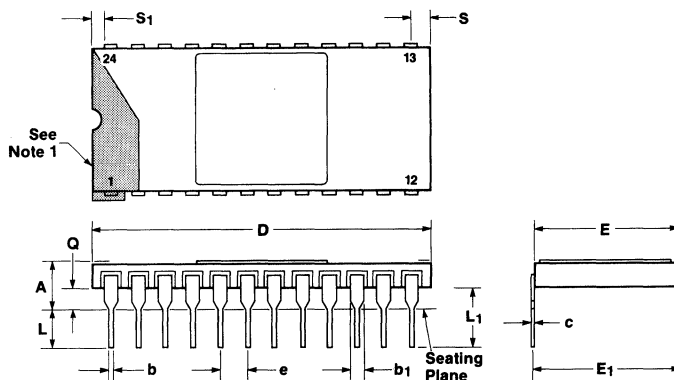


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic lead spacing is 0.100 (2.54 mm) between centerlines.
- Applies to all four corners.
- Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

24-Lead Side-Brazed Dip (VB-Suffix)



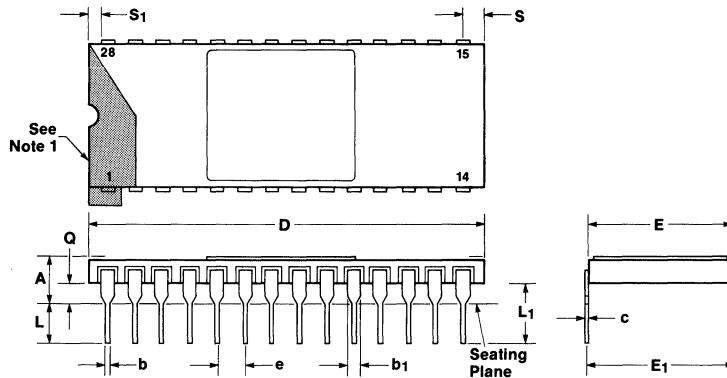
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E ₁	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

28-Lead Side-Brazed Dip (TB-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E ₁	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

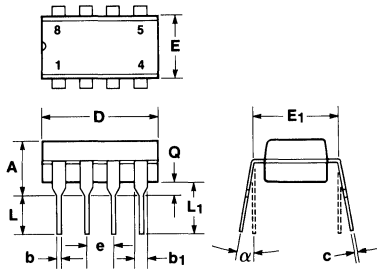
NOTES:

1. Index area; a notch is or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

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PACKAGE DIMENSIONS — EPOXY DIPS

8-Lead Epoxy Dip (P-Suffix)

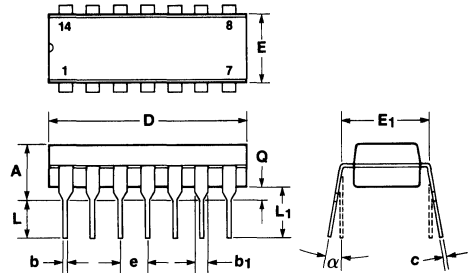


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.148	0.152	3.76	3.86	—
b	0.016	0.020	0.406	0.508	—
b ₁	0.058	0.062	1.47	1.58	—
c	0.008	0.012	0.203	0.304	—
D	0.370	0.382	9.47	9.70	—
E	0.246	0.254	6.25	6.45	—
E ₁	0.298	0.302	7.57	7.67	2
e	0.100 BSC		2.54 BSC		—
L	0.128	0.132	3.25	3.35	—
L ₁	0.148	0.152	3.76	3.86	—
Q	0.020 TYP		0.508 TYP		—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.

14-Lead Epoxy Dip (P-Suffix)



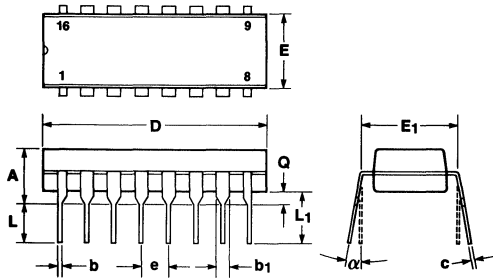
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	0.748	0.754	18.99	19.1	—
E	0.220	0.310	5.59	7.87	—
E ₁	0.290	0.320	7.37	8.13	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.

PACKAGE DIMENSIONS — EPOXY DIPS

16-Lead Epoxy Dip (P-Suffix)

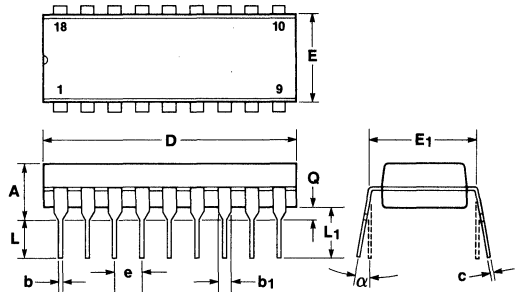


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	0.748	0.754	18.99	19.1	—
E	0.220	0.310	5.59	7.87	—
E ₁	0.290	0.320	7.37	8.13	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.05	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

- Minor changes in dimensions may occur without advance notice.
- Dimension "E₁" to center of leads when formed parallel.

18-Lead Epoxy Dip (P-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	0.898	0.904	22.81	22.91	—
E	0.220	0.310	5.59	7.87	—
E ₁	0.290	0.320	7.37	8.13	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

- Minor changes in dimensions may occur without advance notice.
- Dimension "E₁" to center of leads when formed parallel.

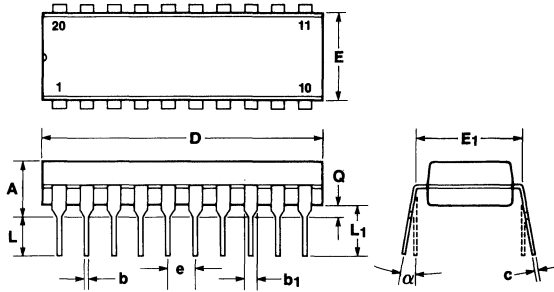


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — EPOXY DIPS

20-Lead Epoxy Dip
(P-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.255	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	1.029	1.035	26.14	26.24	—
E	0.220	0.310	5.59	7.87	—
E ₁	0.290	0.320	7.37	8.13	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

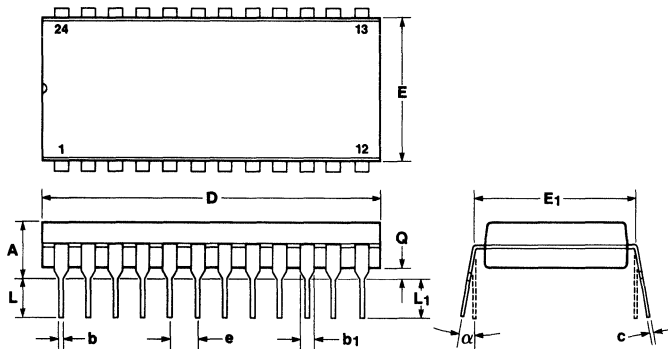
NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.

PACKAGE INFORMATION

PACKAGE DIMENSIONS — EPOXY DIPS

24-Lead Epoxy Dip (P-Suffix)



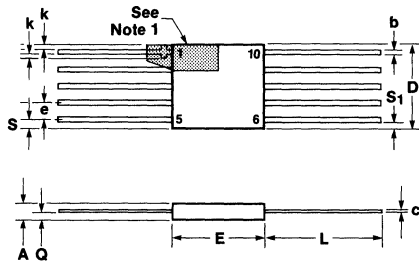
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.20	0.38	—
D	1.248	1.254	31.7	31.8	—
E	0.538	0.542	13.67	13.77	—
E ₁	0.598	0.602	15.19	15.29	2
e	0.100 BSC		2.54 BSC		—
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.

PACKAGE DIMENSIONS — CERPACKS

10-Lead Cerpack (L-Suffix)

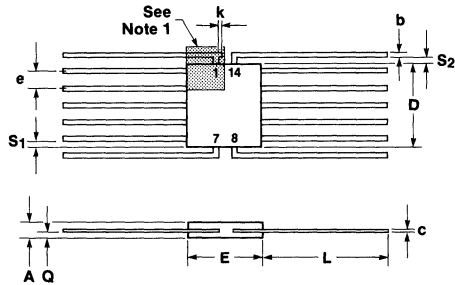


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.290	—	7.37	3
E	0.240	0.260	6.10	6.60	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S	—	0.045	—	1.14	5
S ₁	0.005	—	0.13	—	5, 6

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050 (1.27 mm) between centerlines.
5. Applies to all four corners.

14-Lead Cerpack (M-Suffix)

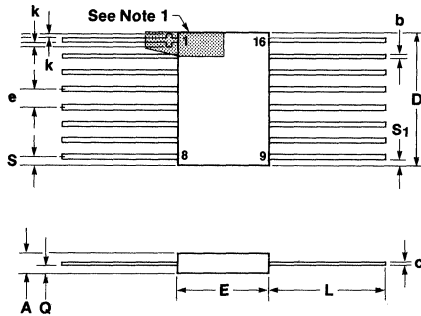


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.280	—	7.11	3
E	0.240	0.260	6.10	6.60	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S ₁	0.005	—	0.13	—	5, 6
S ₂	0.004	—	0.10	—	—

6. Dimension S₁ (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

PACKAGE DIMENSIONS — CERPACKS

16-Lead Cerpack (F-Suffix)

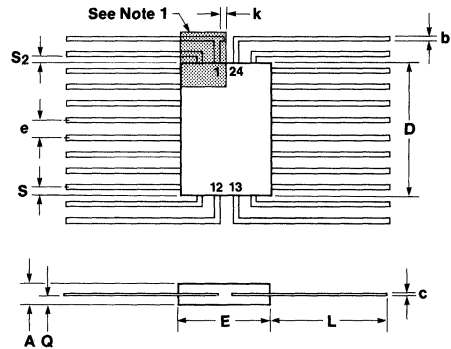


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.085	1.14	2.16	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.440	—	11.18	3
E	0.245	0.285	6.22	7.24	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.23	1.02	2
S	—	0.045	—	1.14	5
S ₁	0.005	—	0.13	—	5, 6

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050 (1.27 mm) between centerlines.
5. Applies to all four corners.

24-Lead Cerpack (N-Suffix)



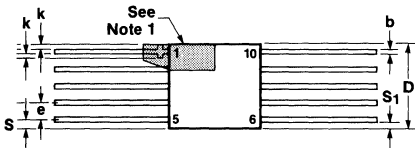
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.090	1.14	2.29	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.430	—	10.92	3
E	0.245	0.285	6.22	7.24	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S	0.005	—	0.13	—	5, 6
S ₂	0.004	—	0.10	—	—

6. Dimension S₁ (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

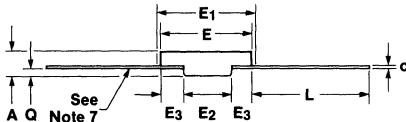
Precision Monolithics Inc.

PACKAGE DIMENSIONS — FLATPACKS

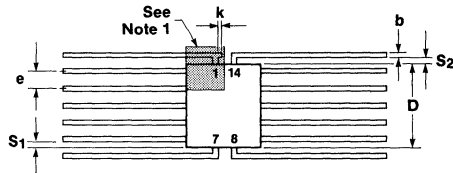
10-Lead Flatpack (L-Suffix)



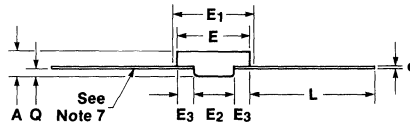
Bottom-Brazed (LB-Suffix)



14-Lead Flatpack (M-Suffix)



Bottom-Brazed (MB-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.290	—	7.37	3
E	0.240	0.260	6.10	6.60	—
E ₁	—	0.260	—	7.11	3
E ₂	0.125	—	3.18	—	—
E ₃	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S	—	0.045	—	1.14	5
S ₁	0.005	—	0.13	—	5, 6

NOTES:

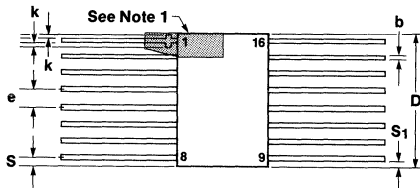
1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050 (1.27 mm) between centerlines.
5. Applies to all four corners.

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.280	—	7.11	3
E	0.240	0.260	6.10	6.60	—
E ₁	—	0.260	—	7.11	3
E ₂	0.125	—	3.18	—	—
E ₃	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S ₁	0.005	—	0.13	—	5, 6
S ₂	0.004	—	0.10	—	—

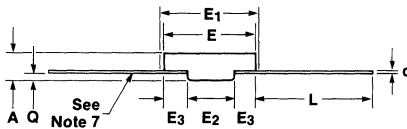
6. Dimension S₁ (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

PACKAGE DIMENSIONS — FLATPACKS

16-Lead Flatpack (F-Suffix)



Bottom-Brazed (FB-Suffix)

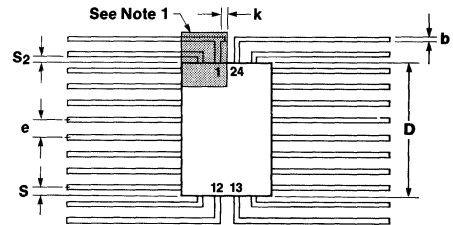


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.085	1.14	2.16	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.440	—	11.18	3
E	0.245	0.285	6.22	7.24	—
E ₁	—	0.305	—	7.75	3
E ₂	0.130	—	3.30	—	—
E ₃	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.23	1.02	2
S	—	0.045	—	1.14	5
S ₁	0.005	—	0.13	—	5, 6

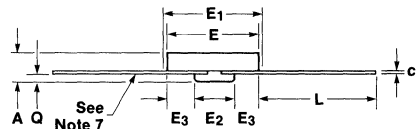
NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050 (1.27 mm) between centerlines.
5. Applies to all four corners.

24-Lead Flatpack (N-Suffix)



Bottom-Brazed (NB-Suffix)

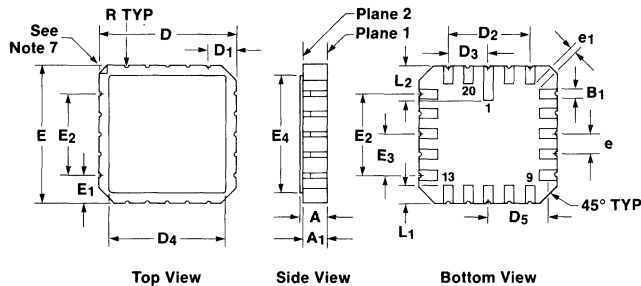


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.090	1.14	2.29	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.430	—	10.92	3
E	0.245	0.285	6.22	7.24	—
E ₁	—	0.305	—	7.75	3
E ₂	0.125	—	3.18	—	—
E ₃	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S	0.005	—	0.13	—	5, 6
S ₂	0.004	—	0.10	—	—

6. Dimension S₁ (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

PACKAGE DIMENSIONS — LEADLESS CHIP CARRIERS

20-Position Chip Carrier (RC-Suffix)



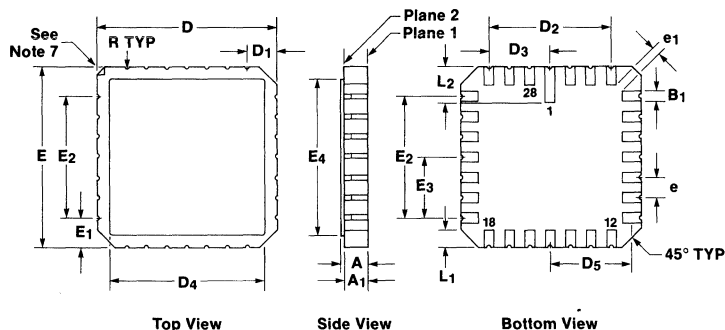
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	5
A ₁	0.054	0.088	1.37	2.24	—
B ₁	0.022	0.028	0.56	0.71	2
D	0.342	0.358	8.69	9.09	—
D ₁	0.075 REF		1.91 REF		—
D ₂	0.200 REF		5.08 REF		—
D ₃	0.100 REF		2.54 REF		—
D ₄	—	0.358	—	9.09	3
D ₅	0.150 BSC		3.81 BSC		—
E	0.342	0.358	8.69	9.09	—
E ₁	0.075 REF		1.91 REF		—
E ₂	0.200 REF		5.08 REF		—
E ₃	0.100 REF		1.91 REF		—
E ₄	—	0.358	—	9.09	3
e	0.050 BSC		1.27 BSC		—
e ₁	0.015	—	0.38	—	1
L ₁	0.045	0.055	1.14	1.40	—
L ₂	0.077	0.093	1.96	2.36	4
R	0.007	0.011	0.18	0.28	—

NOTES:

1. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on plane 1. Metallization is optional on plane 2. However, if plane 2 is metallized it must be electrically connected.
3. A minimum clearance of 0.020" (0.508 mm) is maintained between overall dimensions D₄ × E₄ and all other features, including metallization, chamfers and edges.
4. Non-electrical features for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metallization may increase only toward package periphery.
7. When space is available, the index corner may be metallized on either or both planes 1 and 2. The package edge at the index corner shall not be metallized.

PACKAGE DIMENSIONS — LEADLESS CHIP CARRIERS

28-Position Chip Carrier (TC-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	5
A ₁	0.054	0.088	1.37	2.24	—
B ₁	0.022	0.028	0.56	0.71	2
D	0.442	0.458	11.23	11.63	—
D ₁	0.075	REF	1.91	REF	—
D ₂	0.300	REF	7.62	REF	—
D ₃	0.150	REF	3.81	REF	—
D ₄	—	0.458	—	11.63	3
D ₅	0.200	BSC	5.08	BSC	—
E	0.442	0.458	11.23	11.63	—
E ₁	0.075	REF	1.91	REF	—
E ₂	0.300	REF	7.62	REF	—
E ₃	0.150	REF	3.81	REF	—
E ₄	—	0.458	—	11.63	3
e	0.050	—	1.27	—	—
e ₁	0.015	—	0.38	—	1
L ₁	0.045	0.055	1.14	1.40	—
L ₂	0.077	0.093	1.96	2.36	4
R	0.007	0.011	0.18	0.28	—

NOTES:

1. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on plane 1. Metallization is optional on plane 2. However, if plane 2 is metallized it must be electrically connected.
3. A minimum clearance of 0.020" (0.508 mm) is maintained between overall dimensions D₄ × E₄ and all other features, including metallization, chamfers and edges.
4. Non-electrical features for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metallization may increase only toward package periphery.
7. When space is available, the index corner may be metallized on either or both planes 1 and 2. The package edge at the index corner shall not be metallized.

Table of Contents	1
Ordering Information	2
Product Assurance Program	3
Industry Cross Reference	4
Operational Amplifiers	5
Instrumentation Amplifiers	6
Voltage Followers/Buffers	7
Voltage Comparators	8
Matched Transistors	9
Voltage References	10
Digital-to-Analog Converters	11
Analog-to-Digital Converters	12
Analog Switches/Multiplexers	13
Sample-and-Hold Amplifiers	14
Special Functions	15
Communications Products	16
Package Information	17
Sales Offices, Representatives and Distributors	18



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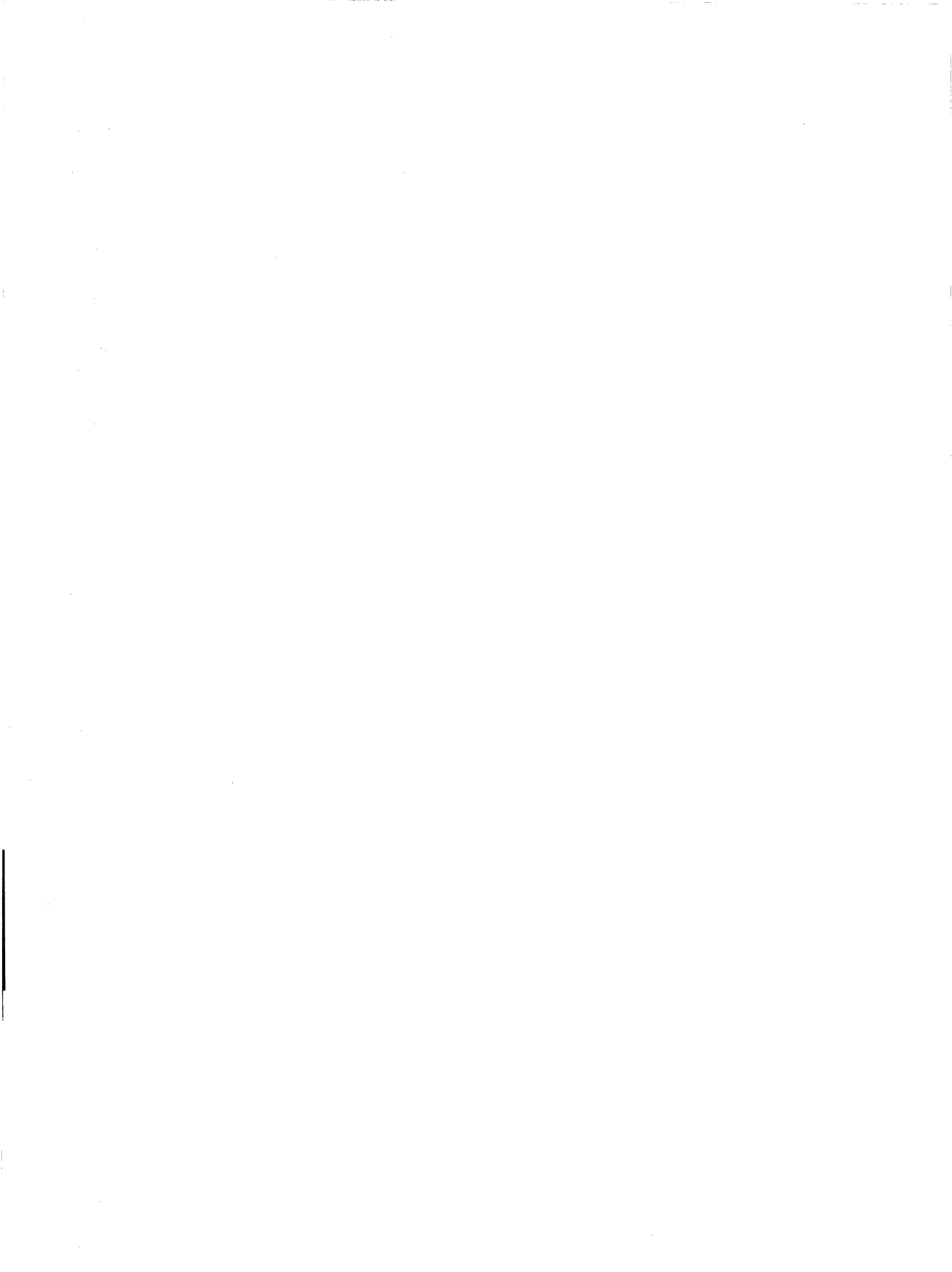
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