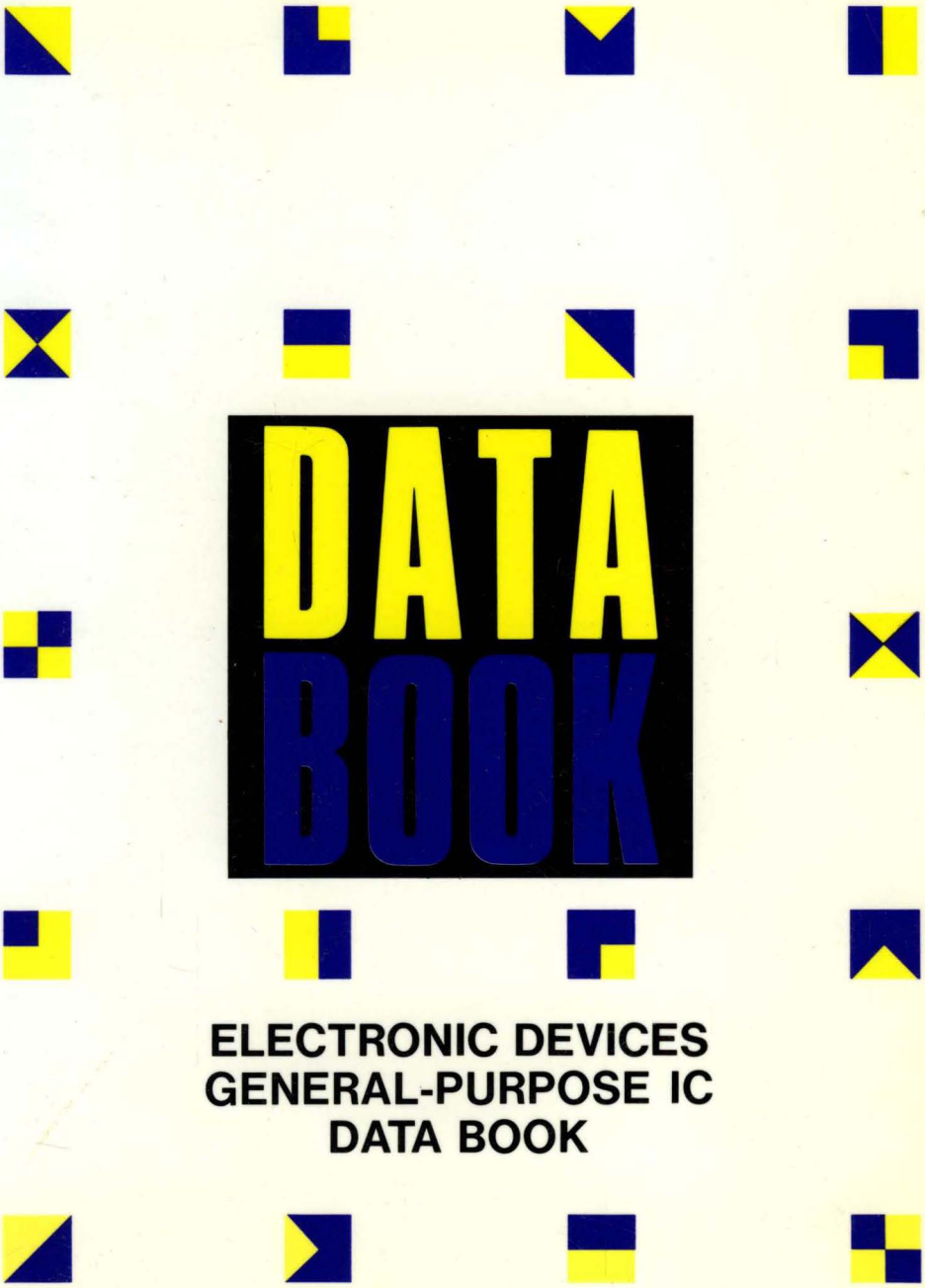
RICOH



ELECTRONIC DEVICES
GENERAL-PURPOSE IC
DATA BOOK

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DATA BOOK

RICOH

RICOH COMPANY, LTD.
ELECTRONIC DEVICES DIVISION

NOTICE

* Specifications described herein are subject to change without notice.
* The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass-produced.
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Printed in Japan

Table of Contents

7. LINEAR IC

8. APPLICATION MANUAL

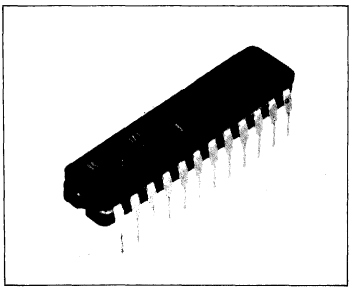
1.GENERAL INFORMATION

EPL

Features

This is the ASIC which allows the user to program optional logic circuits with many standard PAL programmers. This is optimum replacement for small-scale logic and CPU peripheral devices. EPL's provide a quick evaluation and correction of logic circuits.

- Upward compatible to AMD PAL.
- CMOS EPROM process
  - Low current consumption and high programmability.
  - Erasable by ultraviolet light (ceramic window package).
- Maximum access time 25/35ns
- 20pin, 24pin types
- Up to 900 gate equivalents
- Security fuse
- Output polarities are programmable.



Lineup

	Model name	Configuration	Power supply	Electrical characteristics				Package	Compatible products
				Max. Icc		Max. access time	Max. operating freq.		
				Operation	Standby				
GI	EPL10P8 B	10 input 8 output AND-OR/XOR Array	5V±5%	50mA*	40mA*	35ns	20MHz	20DIP (plastic, ceramic with window)	PAL10L8, 10H8
	EPL12P6 B	12 input 6 output AND-OR/XOR Array							PAL12L6, 12H6
	EPL14P4 B	14 input 4 output AND-OR/XOR Array							PAL14L4, 14H4
	EPL16P2 B	16 input 2 output AND-OR/XOR Array							PAL16L2, 16H2
GII	EPL16P8 B	10 input 6 input/output AND-OR/XOR Array		70mA	60mA				PAL16L8
	EPL16RP8 B	8 input 8 feedback 8 output 8 register AND-OR/XOR Array							PAL16R8
	EPL16RP6 B	8 input 6 feedback 2 input/ output 6 output 6 register AND-OR/XOR Array							PAL16R6
	EPL16RP4 B	8 input 4 feedback 4 input/ output 4 output 4 register AND-OR/XOR Array							PAL16R4
	EPL241ED/ EP/EJ	6 input 16 input/output 16 feedback 16 macrocell clock select asychronous reset with 16 register		140mA**	120mA**	25ns	30MHz	24DIP 28PLCC	22V10 & others
	EPL204ED/ EP	10 input 8 input/output 8 feedback 8 macrocell clock select asynchronous reset with 8 register		70mA	60mA	25ns	30MHz	20DIP	16V8, 18P8 and other 20pin PAL
	EPL242***	16 input 8 input/output 8 macrocell asynchronous reset with 8 register		80mA	70mA	25ns	30MHz	24DIP (Plastic) 24CERDIP 28PLCC	20V8
	EPL20F***	Same as GII type (except for XOR)		70mA	60mA	15ns	40MHz	20DIP 20CERDIP 20PLCC	Same as GII

GI : Group I GII : Group II

* Since Group I has twice as many product terms as PAL products, typical currents will be reduced to a half of the above specification values by power-down circuits in RICOH's EPL.

** It will proportional to the product term usage. (40 mA at 35% utilization)

***Under development

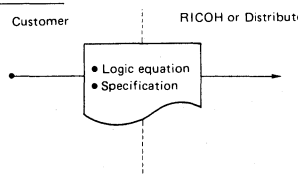
Support Tool

Software
- ◉EPLASM (RICOH)
- ◉ABEL (Data I/O)

Hardware
- ◉Universal Programmer UNISITE40, 29B (Data I/O)
- ◉Model 60A (Data I/O)
- ◉Model PW98-20 (RICOH)
- ◉EPROGRAMER241 (RICOH)
- Pecker 30 (AVAL)
- PROMAC Model 11 (Japan Macnics)

Hardware
- SW16 (Ricoh) (RICOH)
- IBM-PC AT (IBM)
- PC9801 (NEC)

Interface



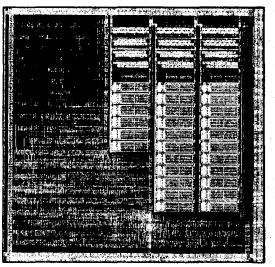
- If the customer has the programer, it can be programed by the customer.

◉mark: Products handled by RICOH's sales

GATE ARRAY

Features

- A variety of line-up
  High speed (0.38ns) High density (200k Gate), Low power operation (3V), Small gates with a number of I/Os.
- Design support system is available for a Work Station (SPARC).



Memory Build-in type

5GU Series (CMOS Gate Array, 0.8μ Design rule)

5GU Series	Gates	No. of I/O*	Gate Delay Time	Supply Voltage	I/O Level	Output Drive Current	Type
5GU020	21.976	136	(5V operation)				
5GU030	33.000	164	0.38ns/gate			(5V operation)	
5GU040	43.092	188	(3V operation)	5V±10%	CMOS/TTL	4/8/12mA	Sea
5GU050	54.016	208	0.63ns/gate		Compatible		of
5GU075	82.056	256	Load	3V±10%		(3V operation)	Gate
5GU100	109.080	292	FAN OUT=2			2/4/6 mA	
5GU200	194.400	384	wire length=2mm				

5GL Series (CMOS Gate Array, 1.2μ Design rule, Small gates with a number of I/Os)

5GL Series	Gates	No. of I/O*	Gate Delay Time	Supply Voltage	I/O level	Package (Number of Pins)	
						QFP	SQFP
5GL005	500	64	(5V operation)			64	64
5GL009	900	84	0.8ns/gate			64, 80	64, 80
5GL015	1500	104	(3V operation)	5V±10%	CMOS/TTL	64, 80, 100	64, 80, 100
5GL026	2600	132	1.6ns/gate		Compatible	64, 80, 100	64, 80, 100, 128
5GL035	3500	148	Load	3V±10%		80, 100, 128, 144	80, 100, 128
5GL045	4500	164	FAN OUT=2			100, 128, 144	100
5GL100	10000	236	wire length=2mm			128, 144, 160	208

* 8 pins in I/O pads are dedicated to Vcc and GND. 64, 80 and 128 pin type of SQFP are under development.

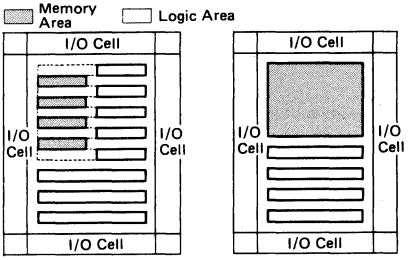
5GV Series (CMOS Gate Array, 1.2μ Design rule)

5GV Series	Gates	No. of I/O*	Gate Delay Time	Supply Voltage	I/O level	Package (Number of pins)				
						DIP	SDIP	FLAT	SQFP	PLCC
5GV041	4100	106	(5V operation) 0.8ns/gate	5V±10%		24, 28, 40	42, 64	60, 64, 80, 100	64, 80, 100	44, 68, 84
5GV053	5300	118	(3V operation) 1.6ns/gate			24, 28, 40	42, 64	60, 64, 80, 100, 128	64, 80, 100, 128	44, 68, 84
5GV073	7300	136			CMOS/TTL	24, 28, 40	42, 64	60, 64, 80, 100, 128, 144	64, 80, 100	44, 68, 84
5GV094	9400	154	Load		Compatible	24, 28, 40	42, 64	64, 80, 100, 128, 144	64, 80, 100, 128	44, 68, 84
5GV124	12400	178	FAN OUT=2	3V±10%		–	42, 64	64, 80, 100, 128, 144, 160	64, 80, 100, 128	44, 68, 84
5GV161	16100	204	wire length=2mm			–	42, 64	80, 100, 128, 144, 160	80, 100, 128	44, 68, 84

* 8 pins in I/O pads are dedicated to Vcc and GND. 64, 80 and 128 pin type of SQFP are under development.

Features of 5GF Series

5GF Series Gate Arrays allow memory (ROM, RAM) in conjunction with Logic requirements.
RICOH's unique system of constituting the memory using wired area, as shown on the right diagram. Since it does not require the master for memory, the cost for development can be kept down in case of memory integrated.



5GF Series　　Example of other systems

5GF Series (CMOS Gate Array, 1.5μ Design rule)

5GF Series	Gates	Max. loading memory capacity RAM (ROM) (bit)	No. of I/O	Gate Delay Time	Supply Voltage	I/O level	Package (Number of pins)			
							DIP	Shrink DIP	FLAT	PLCC
5GF21	2100	2 K (4 K)	84	1.0ns/gate Load 2 input NAND FAN OUT = 3 3mm	5V±10%	CMOS/TTL Compatible	40	64	44, 60, 64, 80, 100	68
5GF26	2600	2 K (4 K)	94				40	64	44, 60, 64, 80, 100	68
5GF32	3200	2 K (4 K)	102				40	64	44, 60, 64, 80, 100	68
5GF45	4500	4 K (8 K)	120				40	64	60, 64, 80, 100	68
5GF58	5800	8 K (16 K)	138				40	64	64, 80, 100	68
5GF82	8200	16 K (32 K)	168				40	64	80, 100	68

Note: Available number of gates for logic are reduced due to memory capacity.

5GH Series (CMOS Gate Array, 2.0μ Design rule)

5GH Series	Dates	No. of I/O	Gate Delay Time	Supply Voltage	I/O level	Package (Number of pins)			
						DIP	Shrink DIP	FLAT	PLCC
5GH05	560	40	1.5ns/gate Load 2 input NAND FAN OUT = 3	5V±10%	CMOS/TTL Compatible	14, 16, 18, 20, 22, 24, 28, 40	–	–	–
5GH10	1000	60				24, 28, 40, 48	28	60, 44	44*, 52, 68
5GH16	1600	72				24, 28, 40, 48*	28, 42, 64	60, 80, 44	44*, 68
5GH23	2300	88				28, 40, 48*	64	60, 80, 100	68, 84*
5GH29	2900	98				28, 40, 48*	64	60, 100	68*, 84*
5GH38	3800	108				40, 48*	64	60, 80, 100	68*, 84*

(*) : Under Development

STANDARD CELL

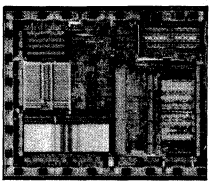
Features

- Abundant Cell Library
  (CPU : 8/16 bit, CPU peripheral Cell, Compiled Cell, Analog Cell (A/D, D/A)).
- High-Speed (0.26ns).
- Low voltage operation (5V/3V).
- Design support system is available for a Workstation (SPAPC).

Development Example

ASIC Micro Computor

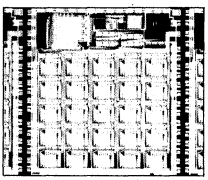
RICOH prepairs 3 CPUs; & Ru 8 (8bit), 65C02 (8bit) and 65C816 (16bit). These CPUs are High-speed (pipe-line archtecture, powerful addressing mode) and small size.



Example (Using 65C02)

Compiled Cell

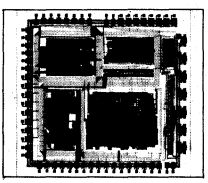
RICOH prepairs large scale cells. (Compiled cell).



Example
(Image Processing IC)

Digital/Analog Cell

Digital circuit and Analog Circuit can be integrated on a chip.

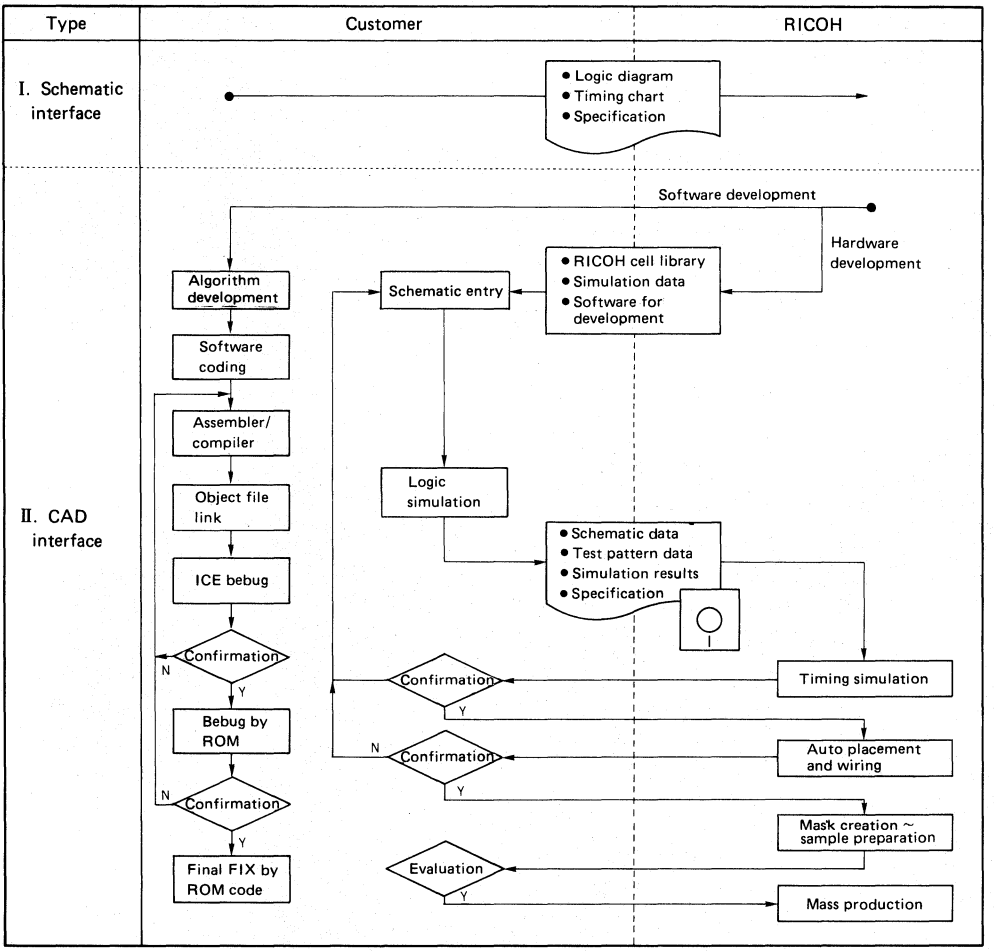


Example (Controller IC)

< Cell Library >

Cell Name	Cells
Basic Cell	Macro Cell Macrofunction Cell (411 Cells)
CPU Cell	8bit : Ru8, R65C02 16bit : R65C816 (3 Cells)
CPU Peripheral Cell	ACi (Asynchronous communication interface) INTC (Interrupt controller) TCC (Timer/Counter) PIO&HS (Parallel input/output) RTC 8 (Real Time Clock) (5 Cells)
Compiled Cell	MUL (Multiplier) ALU (Arithmetic Logic Unit) ADS (Adder/Subtructor) BRS (Barrel Shifter) RGF (Register file) DMX (Multiplexer) SEQ (Microprogram sequencer) PIP (Pipeline register) MRO (Mask ROM Asynchronous) SRA (SRAM Asynchronous) HSR (SRAM Synchronous) (11 Cells)
Analog Cell	AD8SRA (8 bit Successive Approximation A/D Convertor) AD8TRW/AD8TRWL (8 bit Series – Parallel A/D Convertor) DA8RRV/DA8RRI (8 bit R-2R D/A Convertor) DA8VA (8 bit Current Adder D/A Convertor) (4 Cells)

Interface



Note) The CAD interface system provides software development for any practical circuit.

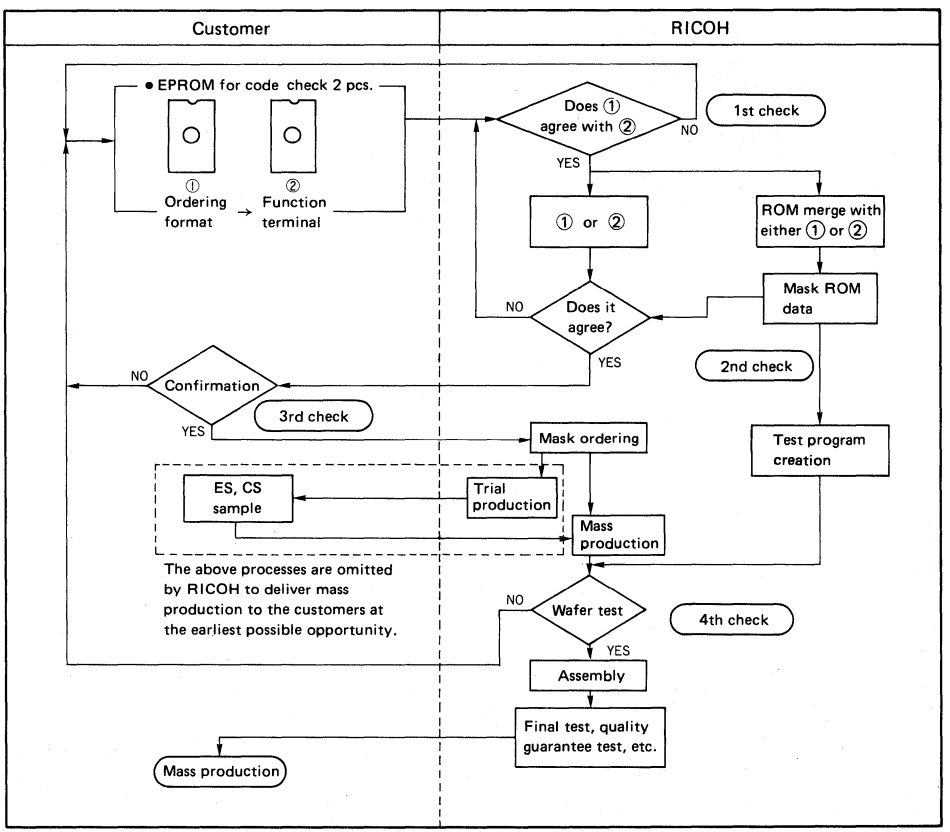
MASK ROM

Lineup

Model name	Process	Memory capacity	Memory configuration	Access time (nsec)	Power supply voltage	Max. power consumption (mW)		No. of pins	Pin compatibility
						Operation	Standby		
PR2D32/33	NMOS	32K	4096x8	250	5V±10%	440	–	24	TI/INTEL
RP2364E		64K	8192x8	200		550	110	28	INTEL
RP23128E		128K	16384x8	200		550	110	28	INTEL
RP23256D/E		256K	32768x8	250/200		550	110	28	INTEL
RP231027D/E		1M	131072x8	250/200		550	165	28	
RP231028E *		1M	131072x8	200		275	110	28	
RP234096 *		4M	524288x8	200		440	–	32	

* Under development

Interface



RICOH STANDARD

EPROM

Model name	Type	Memory capacity	Configu-ration	Access time (μs)	Power supply voltage	Max. power consumption (mW)		No. of pin	Pin compatible
						Operation	Standby		
RP/RF5H01	CMOS	64 bits	64x1	1	5V±5%	55	0.55	8	–

MPU

Model name	Circuit function	Power consumption (MAX.)		Operation frequency	Cycle time	Package
		Operation	Standby			
RP65C02G/G-06	8bit CMOS MPU	5mA/MHz	28μA	4/6MHz (MAX.)	250/166ns (MIN.)	40pin DIP

DSP

Model name	Circuit function	Power supply voltage	Supply current (TYP.)	Execution speed	Clock (MAX.)	Package
RP5C72	Digital Signal Processor (fixed point operation)	5V ± 5%	60mA	100ns/ Instruction	40MHz	28pin DIP

REAL-TIME CLOCK

Model name	Circuit function	Power supply voltage	Max. current consumption		Backup power voltage	Package
			Operation	During backup		
RP/RF/RJ5C15	REAL TIME CLOCK	5V±10%	250μA	15μA	2.0V	18DIP/18SOP/28PLCC
RP5C01	REAL TIME CLOCK with RAM		250μA	15μA	2.2V	18-DIP
RP/RF5C62	REAL TIME CLOCK	5V±10%	50μA	3μA	2.0V	18DIP/18SOP

CRT CONTROLLER

Model name	Circuit function	Power supply voltage	Power supply current	Package
RF5C16A/RP5C16	CRT DISPLAY CONTROLLER (All in One Type) 640x200 or 80x25 (character x line)	5V±10%	50mA	64-FLAT 64-DIP
RF5C56	CRT DISPLAY CONTROLLER (All in One Type with Look up Table and analog RGB) 512x192 dots or 32x24 characters display	5V±10%	60mA	64-DIP

Note) EPL is a registered trademark of RICOH. LOGICIAN is a registered trademark of Daisy Systems Co. IDEA1000 is a registered trademark of Mentor Graphics Co. IBM-PC is a registered trademark of IBM Co. DASH is a registered trademark of FutureNet Co. CADAT is a registered trademark of HHB Systems Co. PAL is a registered trademark of Advanced Micro Devices, INC.

QUAD. UART

Model name	Circuit function	Power supply voltage	Max. power current	Package
RF5C59	Asynchronous receiver transmitter with 4 channel ports.	5V	20mA	60-FLAT

PARALLEL I/O

Model name	Circuit function	Power supply voltage	Supply current (MAX.)	Package
RF5C60	6 I/O Port (8 bit I/O x 5, 5 bit I/O x 1)	5V ± 10%	30mA	60pin FLAT

PCM SOUND GENERATOR

Model name	Circuit function	Power supply voltage	Supply current (MAX.)	Clock (MAX.)	Package
RF5C68A	8 ch. stereo output	5V ± 10%	30mA	10MHz	80pin FLAT

PWM GENERATOR

Model name	Circuit function	Power supply voltage	Supply current (MAX.)	PWM resolution	Clock (MAX.)	Package
RF5C86	8 ch. PWM output	5V ± 10%	30mA	16 bit	16MHz	28pin SOP

2 DIMENSION FILTER

Model name	Circuit function	Power supply voltage	Clock (MAX.)	Processing speed (MAX.)	Package
RF5C67	5 x 5 image element filtering process	5V ± 10%	20MHz	25ns/element	100pin FLAT

VOLTAGE DETECTOR

Model Name	Function	Voltage Detect Accuracy	Operation Voltage	Current Consumption	Package
RX5VL	Voltage Detection. Possible to set detect voltage at 0.1V step.	±2.5%	1.5 ~ 10V	1μA	(SOT-89) TO-92, SOT-23-5
RN5VT*	Voltage Detection. Low voltage operation.	±2.5%	0.7 ~ 10V	1μA	Mini mold 5 pin (SOT-23-5)

* Under Development

VOLTAGE REGULATOR

Model Name	Function	Output Voltage Accuracy	Operation Voltage	Current Consumption	Package
RX5RL	Power Supply. Possible to set output voltage at 0.1V step.	±2.5%	1.5 ~ 10V	1μA	(SOT-89) TO-92, SOT-23-5
RX5RE	Power Supply. Large current output	±2.5%	1.5 ~ 10V	1μA	Mini Power mold TO-92

DC/DC CONVERTOR

Model Name	Function	Starting Voltage	Output Voltage	Current Consumption	Package
RH5RC	Step-up voltage switching regulator, low voltage operation	0.9 ~ 1.0V	3V, 3.5V, 5V	3.5μA	Mini power mold
RF5RD	Step-up/down voltage series regulator.	1.2V	3V. 5V	6μA	8-SOP
RS5RM*	Series Regulator, Voltage Detect, Enable, PWM type Step-up/down.	1.2V	–	10μA	8-SOP
RS5RJ*	Series Regulator, Voltage Detect, Enable, VFM type, Step-up/down.	1.2V	–	10μA	8-SOP

* Under Development

SWITCHING REGULATOR

Model Name	Function	Starting Voltage	Output Voltage	Current Consumption	Package
RH5RH	PWM type Step-up Voltage Switching Regulator	0.9	–	5μA	Mini power mold (SOT-89)
RH5RI*	VFM type Step-up Voltage Switching Regulator	–	–	–	–

* Under Development

MULTI POWER SUPPLY

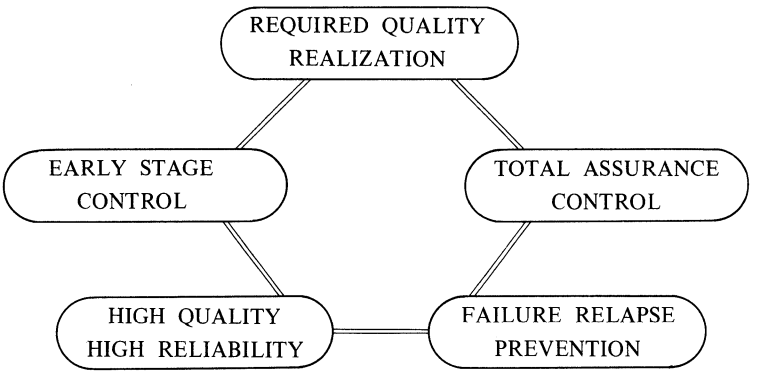
Model Name	Function	Voltage Accuracy	Operation Voltage	Package
RF5C133	Multi Power Supply for Audio (DC/DC + Power Supply)	±2.5%	5V(TYP.)	SSOP24
RS5VE*	Multi Power Supply for Communication (Regulation + Detector)	±2.5%	1.5 ~ 10V	SSOP16

* Under Development

2. QUALITY ASSURANCE SYSTEM

THE POLICY OF QUALITY ASSURANCE

RICOH, Electronic Devices Division, keeps in mind to develop devices and assure the quality putting ourselves in customers' place. RICOH pursuits following 5 points night and day to offer the best quality timely with the optimum cost to the customers.



1. Accomplish the quality aim satisfying the use condition and requirements of customers.

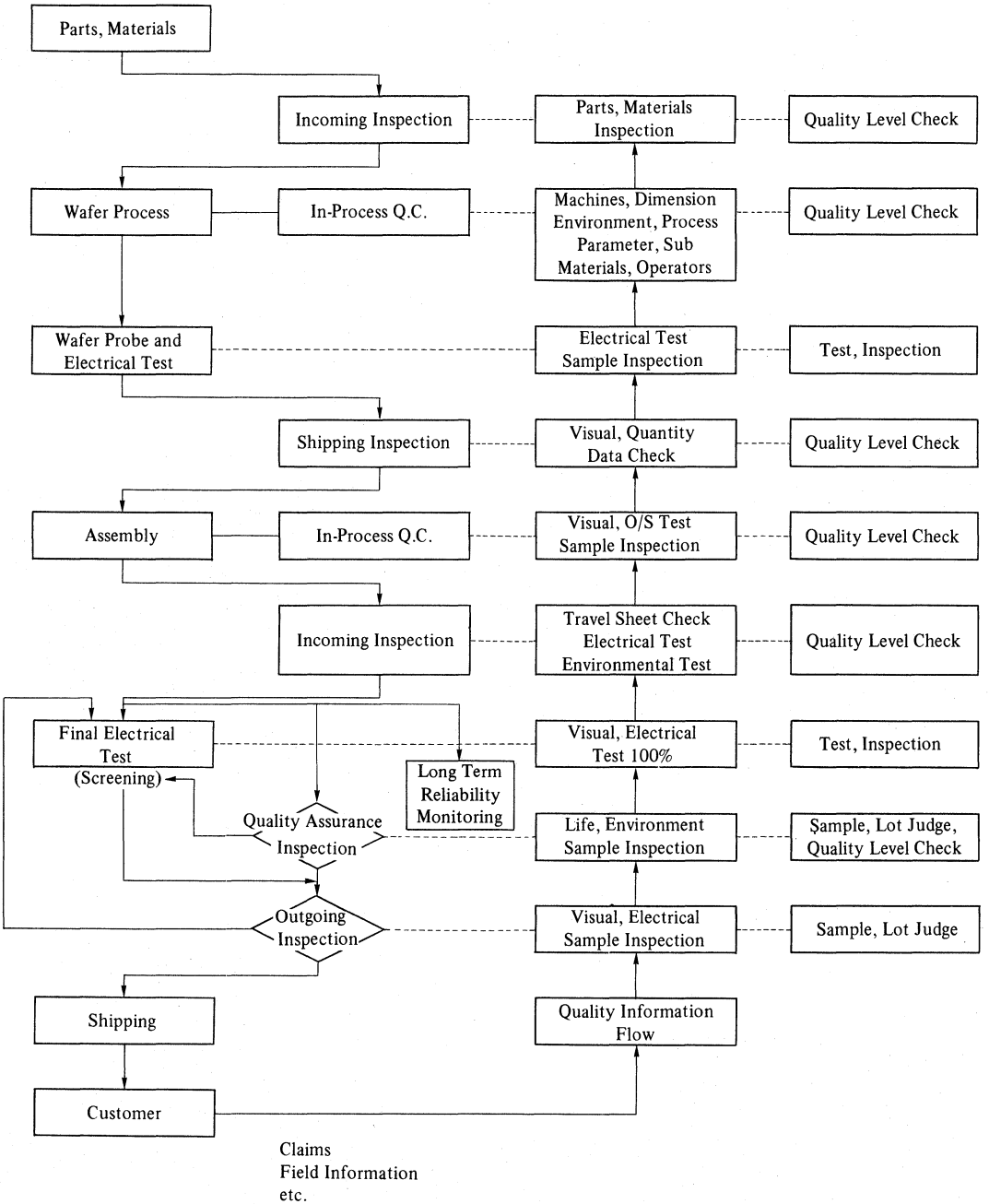
2. Control the first stage thoroughly to make in the quality on development and manufacturing steps.

3. Recognize the importance of quality through quality improvements and quality educations, and then aim at the high quality and high reliability.

4. Inquire into the cause of failure in cooperation with other sections and take measures immediately and completely not to meet the recurrence.

5. Complete the synthetic assurance and control system which satisfy quality, cost, and delivery.

QUALITY CONTROL FLOW CHART IN MANUFACTURE



QUALITY ASSURANCE SYSTEM

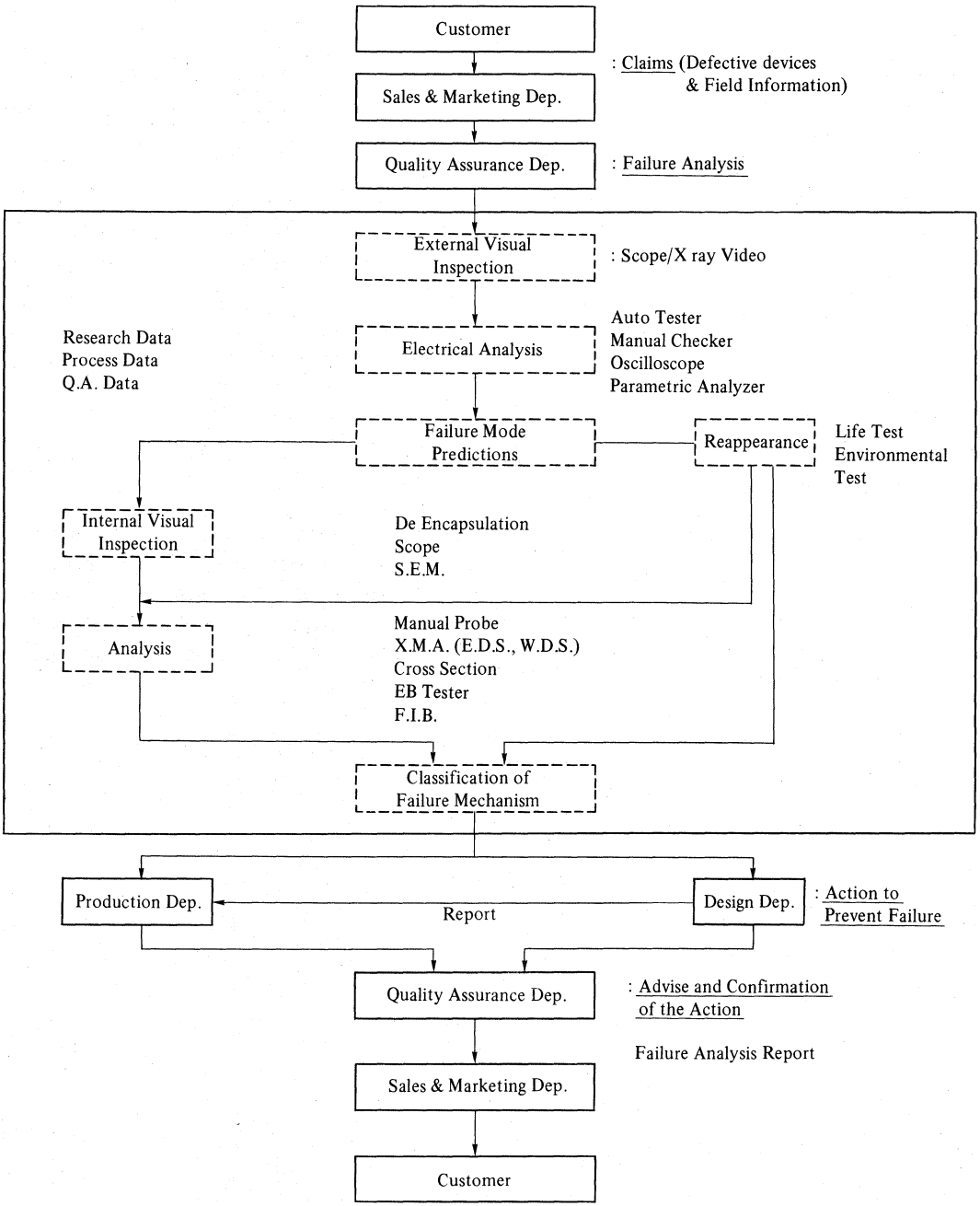
An effective quality assurance system cannot be undertaken on an individual basis. Only a cooperative effort among all divisions can consistently achieve a solid guarantee of top quality. Put into practical use, a system of this type must be functional, it must be based on the idea of standardization, and it must quickly accommodate the data and feedback that continually pass between departments.

We have developed a Quality Assurance System that incorporates these concepts. Our Quality Assurance Department is set up to ensure fast, accurate relay of information between divisions and prompt execution of quality assurance tasks at each step in the manufacturing process – from product development to mass production.

At the product development stage, the tasks required in all succeeding stages are defined and responsibility for their execution is assigned. The Quality Assurance Department then undertakes inspections from a comprehensive point of view, through its inquiry groups. Our quality and reliability criteria are geared to meet reliability and qualification testing standards such as MIL, EIAJ, and JIS to ensure that our product designs, processes, and conformity to standards are approved.

At the mass-production stage, the Manufacturing Department undertakes strict control of processes, product quality within processes, equipment, and the environment, in order to build in quality at each step. The Quality Assurance Department safeguards overall quality by inspecting incoming materials, controlling product amendments, maintaining accuracy in measurement devices, inspecting wafers and making final checks, monitoring quality, and undertaking quality assurance checks which ensure that no defective products reach the market.

FAILURE ANALYSIS FLOW CHART



LOT ASSURANCE INSPECTION

(+ASSEMBLY INCOMING INSPECTION)

Sampling: Every Wafer Lot

No.	TEST ITEMS	TEST METHODS			LTPD (%)	Maximum Accept No.
1	ELECTRICAL (Open, Short check)	Auto Tester QAT Specification			5	0
2	HIGH TEMPERATURE OPERATING LIFE	Ta = T jmax 125°C 20 Hrs. Dynamic Operation			10	0
3	THERMAL SHOCK (liquid)	Ta = T stgmin ~ T stgmax (5′ –10″ –5′) 10 Cycles			20	0
	MIX PCT	TYPE A DIP package	TYPE B QFP, SOP package	TYPE C PLCC package		
	SOLDERING HEAT	260°C Lead only 10 sec.	260°C Full dip 5 sec. or IR Reflow 2 times or VPS 215°C 60 sec.	IR Reflow 2 times or VPS 215°C 60 sec.		
	THERMAL SHOCK	T stgmin ~ T stgmax 10 Cycles	T stgmin ~ T stgmax 10 Cycles	T stgmin ~ T stgmax 10 Cycles	20	0
	PRESSURE COOKER	121°C 2 atms 20 Hrs.	121°C 2 atms 20 Hrs.	121°C 2 atms 20 Hrs.		

OUTGOING INSPECTION

Sampling Method: MIL-STD 105D

No.	DIVISION	TEST ITEMS	CRITERIA	LEVEL
1	ELECTRICAL	Function DC AC	QAT Specification	AQL 0.25% *1)
2	APPEARANCE	Heavy Defect Light Defect	Visual Inspection Criteria	0.65% 1.0%

*1) Catastrophic Failures (short, open, or functially inoperative) AQL 0.065%

RELIABILITY TEST REQUIREMENTS

TABLE I RELIABILITY/ENVIRONMENTAL

No.	TEST ITEMS	TEST CONDITION	PACKAGE TYPE		QUALIFY TEST TIME
			PLASTIC	CERAMIC	
1	High Temp. Operating Life	125°C (150°C) Vcc Max	M	M	1000 Hrs.
2	High Temp. Reverse Bias	125°C (150°C) Max	O	O	1000 Hrs.
3	High Temp. Storage	125°C (150°C)	M	M	1000 Hrs.
4	Low Temp. Storage	−55°C (−65°C)	O	O	1000 Hrs.
5	85/85 Temp. Humidity Bias	85°C/85% RH Vcc Max	M	M	1000 Hrs.
6	Low Temp. Operating Life	−20°C (−40°C)	O	O	1000 Hrs.
7	Pressure Cooker	121°C/15PSIG/100% RH	M	*	200 Hrs.
8	Thermal Shock	−55~125°C(−65~150°C)	M	M	200 Cycles
9	Temp. Cycle	−55~125°C(−65~150°C)	M	M	1000 Cycles
10	ESD Sensitivity	1000V(MIL)/200V(EIAJ)	M	M	−
11	Latch Up (CMOS Device Only)	−	M	M	−
12	Mechanical Shock	1500g/Z1, Y1, X1	*	M	−
13	Vibration	20 ~ 2 kHz	*	M	4 Cycles

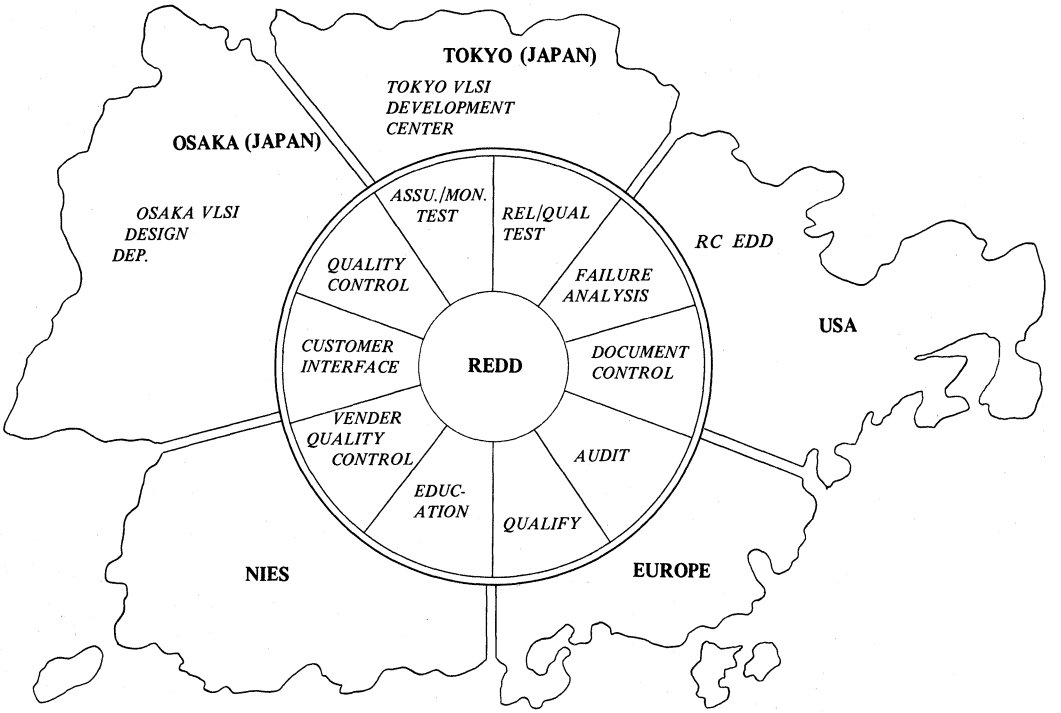
( ): Option

TABLE II MECHANICAL

No.	TEST ITEMS	TEST CONDITION	PACKAGE TYPE		QUALIFY TEST TIME
			PLASTIC	CERAMIC	
14	Physical Dimensions	−	M	M	−
15	Marking Permanency	COND.B or D	M	M	−
16	Visual and Mechanical	−	M	M	−
17	Solderability	245°C 5sec	M	M	−
18	Lead Integrity (Fatigue, Forming, Pull)	−	O	O	−
19	Hermeticity (Fine, Gross)	F/L: 5 x 10^{-8} ATMcc/sec G/L: 2 Hrs. at 60 PSIG	*	M	−

M: Mandatory O: Optional *: Not Applicable

QUALITY & RELIABILITY ASSURANCE FUNCTION



REDD: RICOH ELECTRONIC DEVICE DIV.
RC : RICOH CORPORATION.

3. ASSP

No. 84-01 4-1-1984

REAL TIME CLOCK

RP5C01

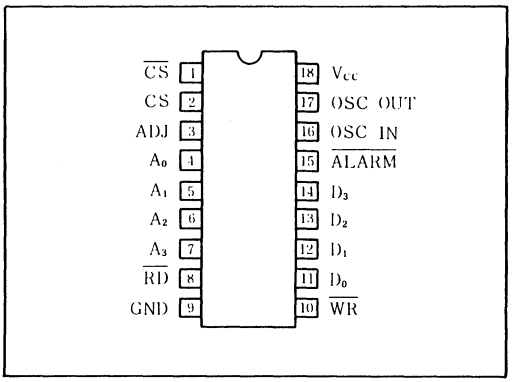
■ GENERAL DESCRIPTION

The RP5C01 bus compatible real-time clock is designed for use with most of the popular microprocessors such as the 8085A, Z-80 and others. Time setting and readout can be readily done in the same manner as writing/readout in and from memory. This RTC device features : counters for complete time-of-day clock alarm, a hundred year calendar, also a 26 × 4-bit RAM providing battery backed up functions and applications as an involatile RAM.

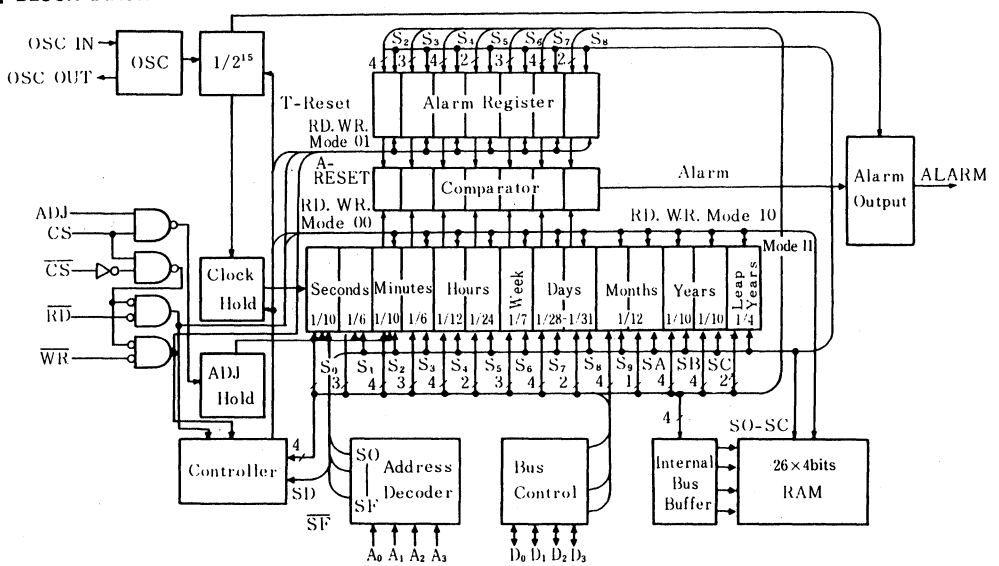
■ FEATURES

- Direct connection with CPU-Bus
- 4-bit bi-directional bus ; D_0-D_3
- 4-bit address input ; A_0-A_3
- Counters for Time (hour, minute, second) and Calendar (leap year, year, month, date, day of the week) are built in.
- 24 Hours, or 12 Hours am/pm display
- All the clock data is BCD encoded
- ADJ terminal for ±30 seconds adjustment
- Provision for battery-backup
- Self-contained 26 × 4-bit RAM
- Provision for Alarm signal, or 16Hz or 1Hz Timing pulse output.

■ PIN CONFIGURATION (Top view)



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Conditions	Limits	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.3~7	V
V_I	Input Voltage		−0.3~7	V
V_O	Output Voltage		−0.3~7	V
P_d	Power Dissipation	Ta=25℃	700	mW
T_{opr}	Operating Ambient Temperature		0~70	℃
T_{stg}	Storage Temperature		−40~125	℃

■ RECOMMENDED OPERATING CONDITIONS (Unless Noted : Ta=0~70℃)

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{DH}	Data Hold Voltage	2.2		5.5	V
f_{XT}	Crystal Oscillation Frequency		32.768		kHz

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Unless Noted : Ta=0~70℃, V_{CC}=5V±10%)

Symbol	Parameters	Measuring Conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=2mA			0.4	V
I_I	Input Current	V_I=0~5.5V			±10	μA
I_{LO}	Output Leakage Current				±10	μA
I_{CC1}	Standby Supply Current	f_{XT}=32.768kHz V_{CC}=2.2V			15	μA
I_{CC2}	Operating Supply Current	f_{XT}=32.768kHz V_{CC}=5.0V (N2)			250	μA

(NOTE 1) : Current flow is 'positive' when flowing toward the IC.
(NOTE 2) : When connected to a CPU R/W cycle-time is 10μs.

● AC ELECTRICAL CHARACTERISTICS (Unless Noted : Ta=0~70℃, V_{CC}=5V±5%)

Symbol	Parameters	Measuring Conditions	Limits			Unit
			Min	Typ	Max	
t_{AC}	Address−$\overline{RD}$/$\overline{WR}$ Delay Time		170			ns
t_{CC}	$\overline{RD}$/$\overline{WR}$ Pulse Width		400		10000	ns
t_{CA}	Address Valid Time After $\overline{RD}$/$\overline{WR}$ Pulse Rise		10			ns
t_{RD}	Data Delay Time After $\overline{RD}$ Fall				340	ns
t_{RDH}	Data Hold Time After $\overline{RD}$ Rise		0			ns
t_{WDL}	Data Delay Time After $\overline{WR}$ Fall				40	ns
t_{WD}	Data Hold Time After $\overline{WR}$ Rise		20			ns

SPECIFICATIONS Under $V_{CC}=5V\pm10\%$ are as follows.

● **AC ELECTRICAL CHARACTERISTICS** (Unless Noted : Ta=0~70℃, $V_{CC}=5V\pm10\%$)

Symbol	Parameters	Measuring Conditions	Limits			Unit
			Min	Typ	Max	
t_{AC}	Adress−$\overline{RD}/\overline{WR}$ Delay Time		170			ns
t_{CC}	$\overline{RD}/\overline{WR}$ Pulse Width		450		10000	ns
t_{CA}	Effective Address Time After $\overline{RD}/\overline{WR}$ Pulse Rise		10			ns
t_{RD}	Data Delay Time After$\overline{RD}$ Fall				400	ns
t_{RDH}	Data Hold Time After $\overline{RD}$ Rise		0			ns
t_{WDL}	Data Delay Time After $\overline{WR}$ Fall				40	ns
t_{WD}	Data Hold Time After $\overline{WR}$ Rise		20			ns

■ PIN DESCRIPTION

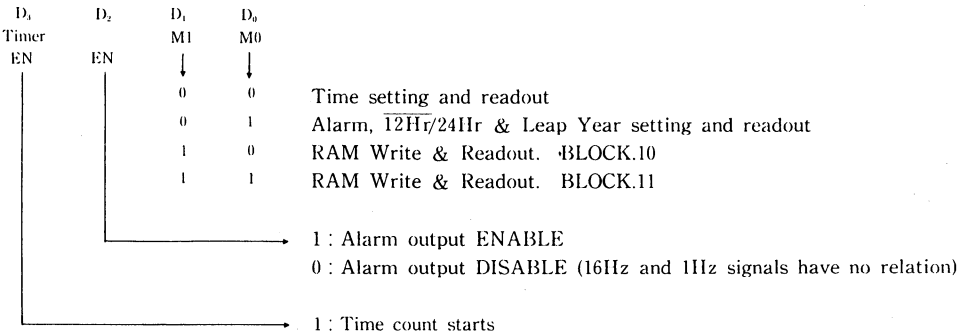
Symbol	Pin No.	Function
$\overline{CS}$, CS	1, 2	Terminals for external interfacing. Valid when CS=H, $\overline{CS}$=L. CS is connected to the power-down detector of peripheral circiut power supply, and $\overline{CS}$ is connected to the microcomputer.
ADJ	3	This pin provides easy zero setting for the "seconds" independently of the CPU. When ADJ=H in the range of from 0 to 29 secs, the "seconds" are preset at zero and not released in the range of 30 to 59 secs by countup until the full minute expires.
A_0~A_3	4, 5, 6, 7	ADDRESS pin. Connected to ADDRESS bus of CPU.
$\overline{RD}$	8	I/O control input. L when CPU←RP5C01.
GND	9	0 V
$\overline{WR}$	10	I/O control input. L when CPU→RP5C01.
D_0~D_3	11, 12, 13, 14	Bi-directional data bus. Connected to the data bus of CPU.
$\overline{ALARM}$	15	Alarm signal and pulse (16Hz CK or 1HzCK) are put out. Open drain output.
OSC_{IN}, OSC_{OUT}	16, 17	Crystal resonator connecting terminal. 32.768kHz.
V_{CC}	18	+5V power supply.

■ ADDRESS MODES

MODE	MODE 00					MODE 01					10	11
$A_3 \sim A_0$	Contents	D_3	D_2	D_1	D_0	Contents	D_3	D_2	D_1	D_0	Contents	Contents
0	1 Sec Counter						×	×	×	×		
1	10 Sec Counter	×					×	×	×	×		
2	1 Min Counter					Alarm 1 Min Register					block 10	block 11
3	10 Min Counter	×				Alarm 10 Min Register	×					
4	1 Hr Counter					Alarm 1 Hr Register						
5	10 Hr Counter	×	×			Alarm 10 Hr Register	×	×			4bit	4bit
6	Day Counter	×				Alarm Day Register	×				×	×
7	1 Day Counter					Alarm 1 Day Register					13	13
8	10 Day Counter	×	×			Alarm 10 Day Register	×	×				
9	1 Mo Counter						×	×	×	×	RAM	RAM
A	10 Mo Counter	×	×	×		$\overline{12\text{ Hr}}$/24 Hr Selector	×	×	×			
B	1 Yr Counter					Leap Year Counter	×	×				
C	10 Yr Counter						×	×	×	×		
D	MODE Register	Timer EN	Alarm EN	MODE Register M1	M0		Timer EN	Alarm EN	MODE Register M1	M0	As at left	As at left
E	TEST Register	Test 3	Test 2	Test 1	Test 0		Test 3	Test 2	Test 1	Test 0	As at left	As at left
F	RESET Controller and Others	1Hz ON	16Hz ON	Timer RESET	Alarm RESET		1Hz ON	16Hz ON	Timer RESET	Alarm RESET		

× indicates : don't care for WR, always zero for RD.

● MODE REGISTER (A_3, A_2, A_1, A_0) = (1, 1, 0, 1) = D



● LEAP YEAR Counter

Leap year when $D_1 = D_2 = 0$. It counts up simultaneously with Year Counter.

● 12h/24h Selector

24-hour counter when $D_0 = 1$

12-hour counter when $D_0 = 0$

PM when $D_1 = 1$, and AM when $D_1 = 0$ respectively of 10h counter

● RESET Controller 16Hz · 1HzCK Register

(A_3, A_2, A_1, A_0)=(1, 1, 1, 1)=F

$D_0 = 1$: Resetting of all alarm registers

$D_1 = 1$: Resetting of frequency divisions before Second

$D_2 = 0$: 16Hz CK pulse ON

$D_3 = 0$: 1Hz CK pulse ON

● ADDRESS 0~D

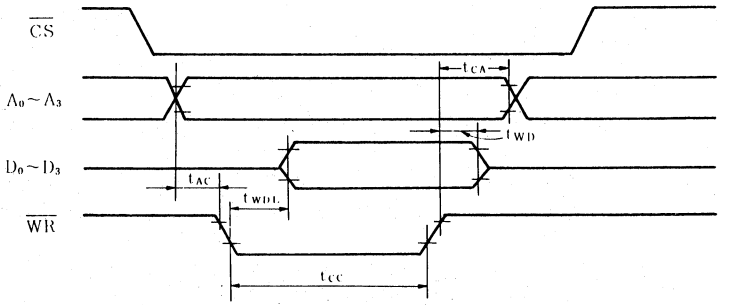
Both READ and WRITE are possible.

● ADRESS E~F

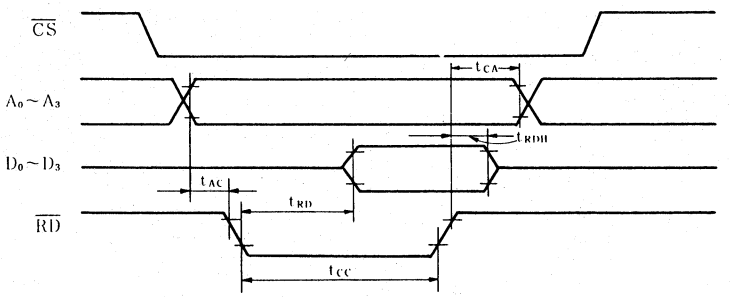
WRITE only is possible.

■ TIMING DIAGRAM

● WRITE CYCLE (CS="H")



READ CYCLE (CS="H")



■ APPLICATION NOTES

1. Oscillating Circuit

1-1 When using a crystal oscillating element.

The oscillator circuit is shown in Figure 1.

Externally connected parts consist of : a resistor, capacitors and a trimmer capacitor. To adjust the frequency, use the trimmer capacitor (The 16Hz or 1Hz signal output at the $\overline{\text{ALARM}}$ pin should be used), for calibration.

When calibrating with the 16Hz signal :

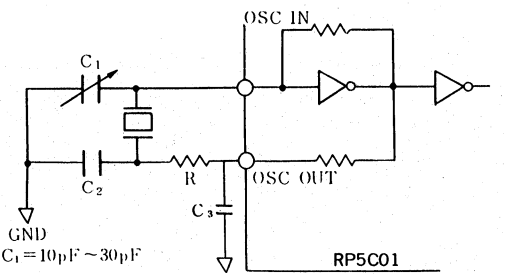
The Address is $(A_3, A_2, A_1, A_0)=(1, 1, 1, 1)$.

The Data is $(1, 0, 0, \times)$.

When calibrating with the 1 Hz signal:

The Address is $(A_3, A_2, A_1, A_0)=(1, 1, 1, 1)$

The Data is $(0, 1, 0, \times)$.



(The crystal employed is Nippon Dempa Kogyo MX38Tor equivalent)

Fig. 1

1-2 When using an external Clock

The external clock should be connected through the circuits shown in Fig.2(a), and (b). The OSCOUT pin should be left with no connection.

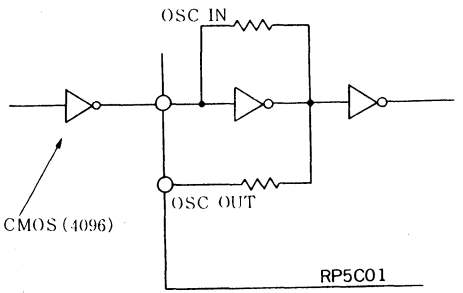


Fig.2 (a) CMOS INVERTER CONNECTION

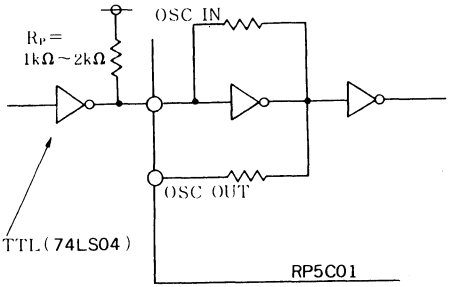


Fig.2 (b) TTL INVERTER CONNECTION

2. Input/Output, and Chip selection Pins.

2-1 Input/Output Pins

In order to stabilize the potential at the Input/Output Pins during 'battery backup' operation, and a pull -down resistor (100~300kΩ), and a pull up resistor (4.7~47kΩ)

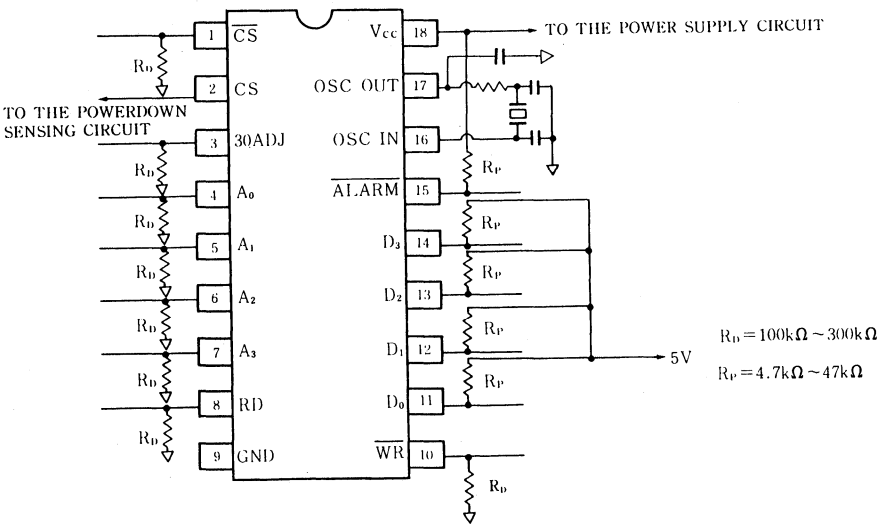


Fig. 3

2-2 Chip selection Pins

There are two chip selection Pins. The CS pin should be connected to the powerdown sensing circuit, and the $\overline{CS}$ pin to the CPU. CS is active "H", whereas $\overline{CS}$ is active "L".

3. Interfacing with typical CPU

3-1 Applicable CPU

CPU	External Circuit
Z-80A	Nil
8085A	74LS74 (NOTE 1)
6800	74LS00, 74LS04

(NOTE 1) Not needed when the X'tal used is below 5MHz

3-2 Standard Interfacing examples.

Examples of Interfacing the RTC with typical CPU (Z80,8085,6800) are presented hereunder.

(1) Z80

The Data Bus, Address Bus, and $\overline{RD}$, $\overline{WR}$ pins are connected to the corresponding pins of the Z-80 (the same symbols are used). The $\overline{CS}$ pin of the RP5C01 should connect with the IORQ pin, or one Bit of the Address Bus (e.g.A_0).

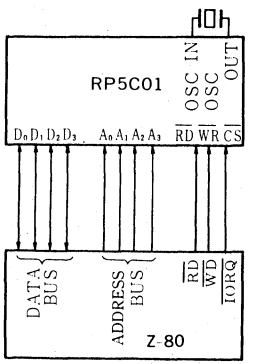
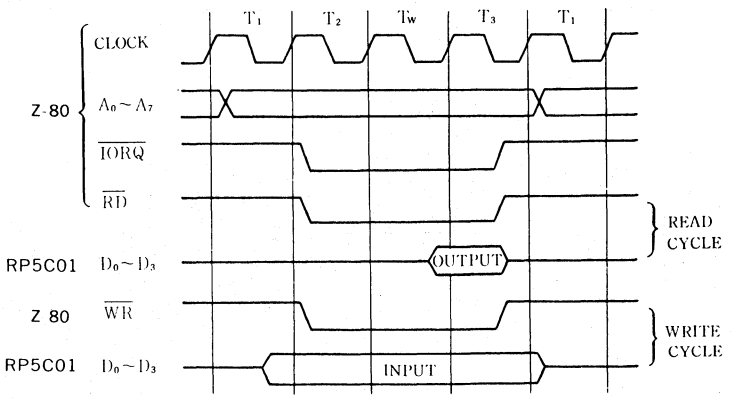


Fig. 4 CONNECTION DIAGRAM WITH Z-80

TIMING CHART



(2) 8085

The Data Bus, Address Bus, and $\overline{RD}$, $\overline{WR}$ pins of the RTC correspond with those of the 8085 (the same symbols are used). The $\overline{CS}$ pin of the RP5C01 should connect with one Bit of the 8085 Address Bus (e.g.pin A_0).

When the crystal oscillator used has a frequency of 6MHz, a 74LS74 (externally connected circuit shown in the dotted line) should be added to provide 1 Wait.

Connection Diagram

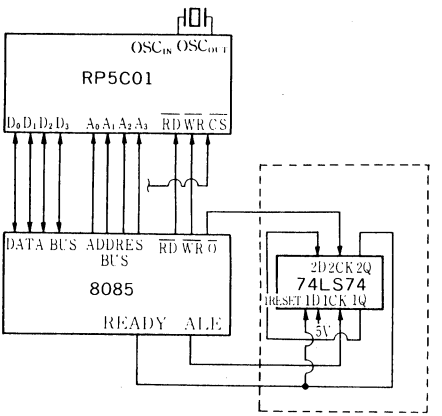
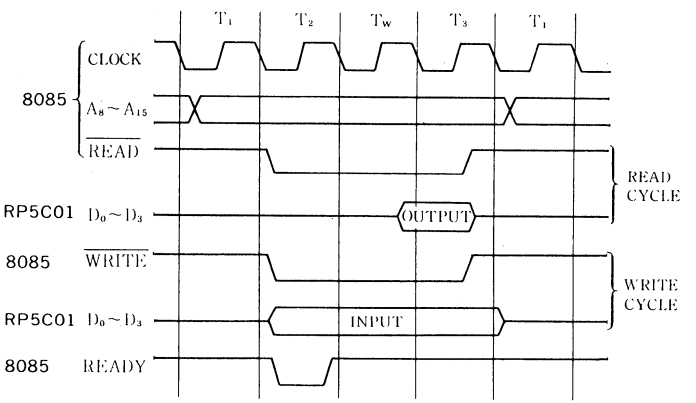


Fig. 5 CONNECTION EXAMPLE WITH 8085

Timing Chart



(3) 6800

The pin connections for the RTC are compatible with the Data Bus, Address Bus of the 6800. (The symbols are the same).

The $\overline{RD}$, $\overline{WR}$, pins of the RP5C01 should be connected to the ϕ_1, and R/W pins of the 6800, but with the addition of the following : two 74LS04 inverters, two input NANDs and two 74LSOO.

Besides, the $\overline{CS}$ pin of the RTC should be connected to one Bit of the 6800 Address Bus (e.g.A_0).

Connection Diagram

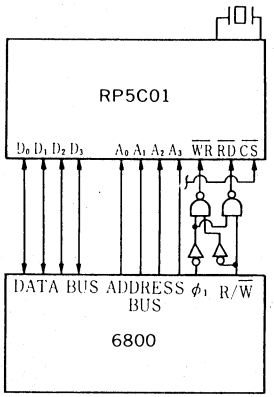
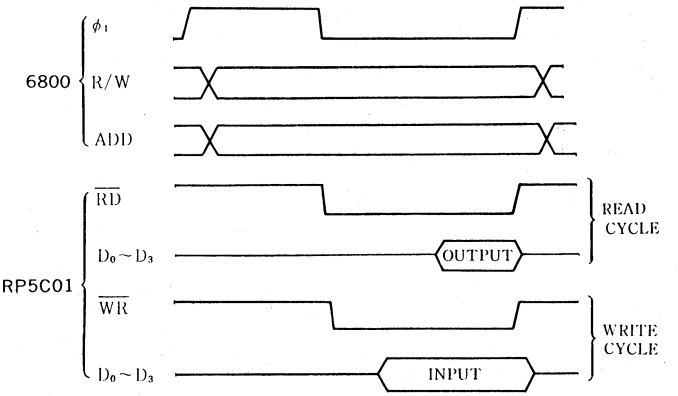


Fig. 6

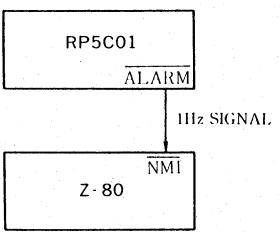
Timing Chart



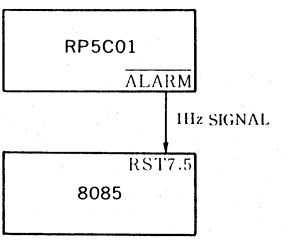
3-3 Interrupt into the CPU

The Data of RP5C01 is read-out by using Interrupt to the CPU at the rate of once every second.

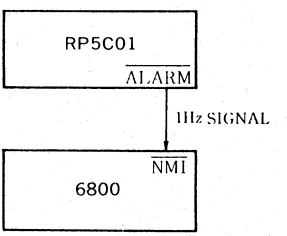
(1) Z80



(2) 8085



(3) 6800



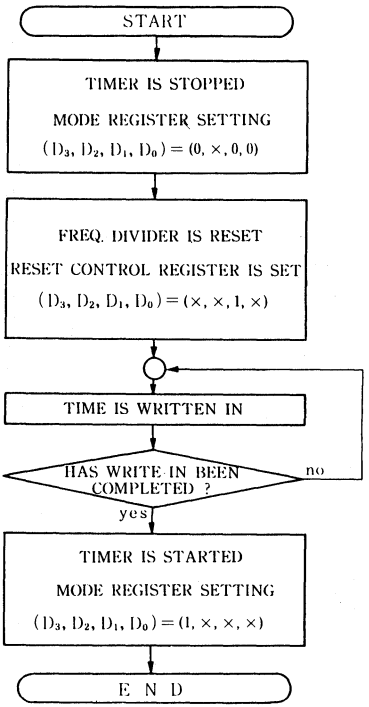
4. Example of a program for setting Time/Alarm

4-1 Flowchart for the time setting operation

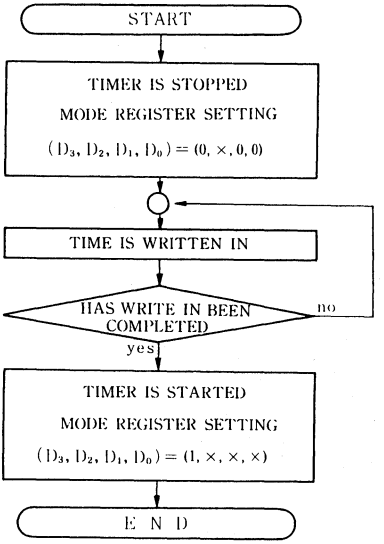
By setting Data (D_3, D_2, D_1, D_0) in the test register (Address (A_3, A_2, A_1, A_0)=(1, 1, 1, 0)), operation of the clock is maintained.

For Time setting, the Timer is stopped, and readout and write-in should be executed within one second.

(1) Timer Setting Program

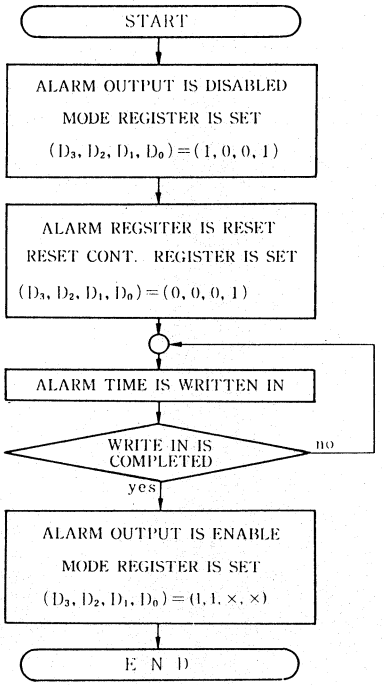


(2) Time Readout Program

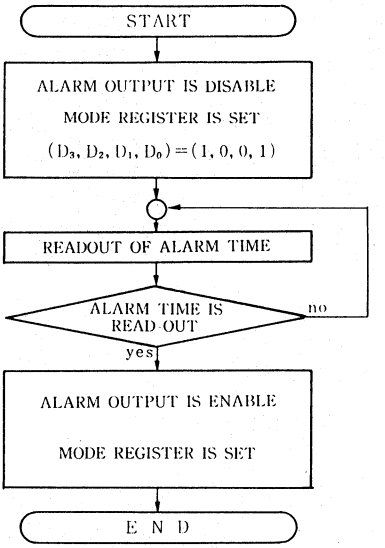


4-2 Alarm Setting Flowchart

(1) Alarm Time Write-in Program



(2) Read-out of Alarm Time

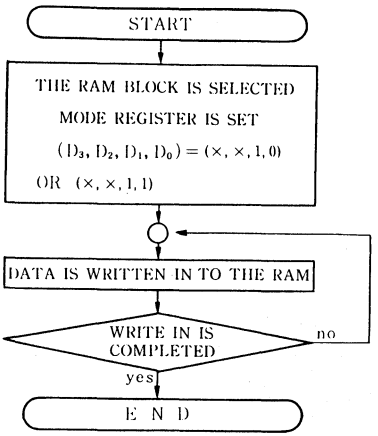


5. Read/Write With RAM Program

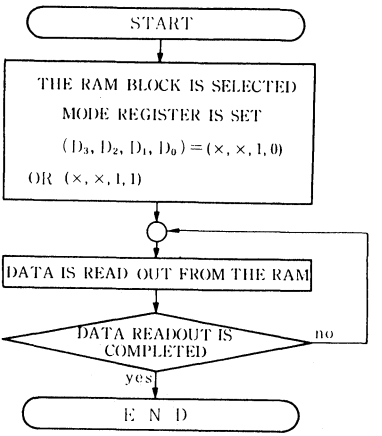
The 26 × 4 Bit User RAM, has provisions for Battery Backup, and can be used as a non-volatile RAM.

The RAM consists of two Blocks (1 Block : 13×4 Bits). A Mode Register enables Selecting the needed Block.

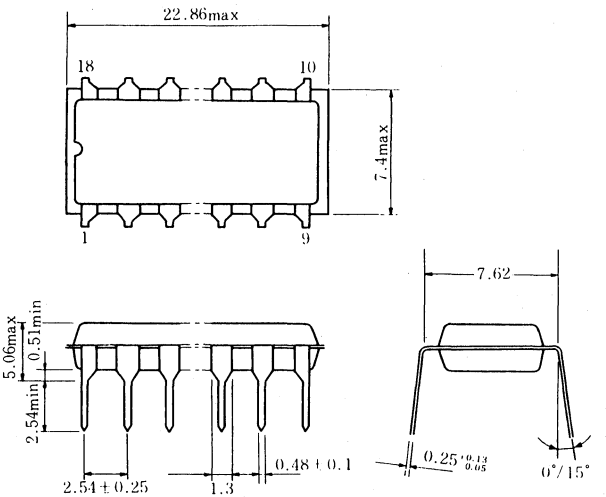
(1) Write-in



(2) Read-out



■ 18 PIN PLASTIC PACKAGE (UNIT : mm)



RICOH

REAL TIME CLOCK

RP/RF/RJ5C15

■ GENERAL DESCRIPTION

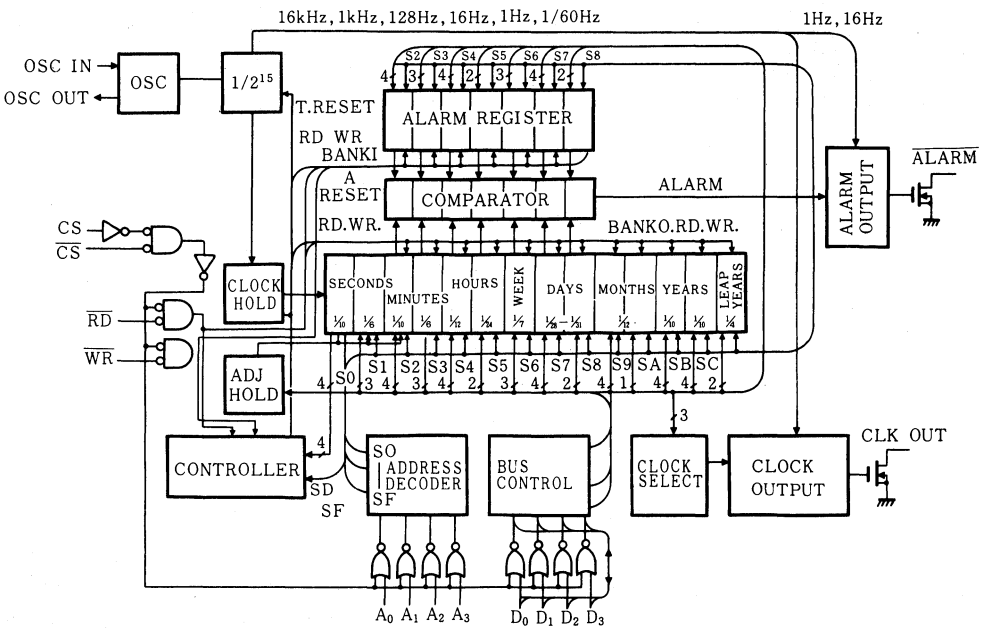
The 5C15 is a real-time clock for microcomputer that can be connected directly with the data bus of 16-bit CPUs such as 8086, Z8000 and 68000 as well as 8-bit CPUs such as 8085, Z-80, 6809 and 6502, and is able to set up and read a time in the same process with READ/WRITE of the memory.

It is provided with alarm function in addition to basic functions of time and calendar, and the battery backup is possible.

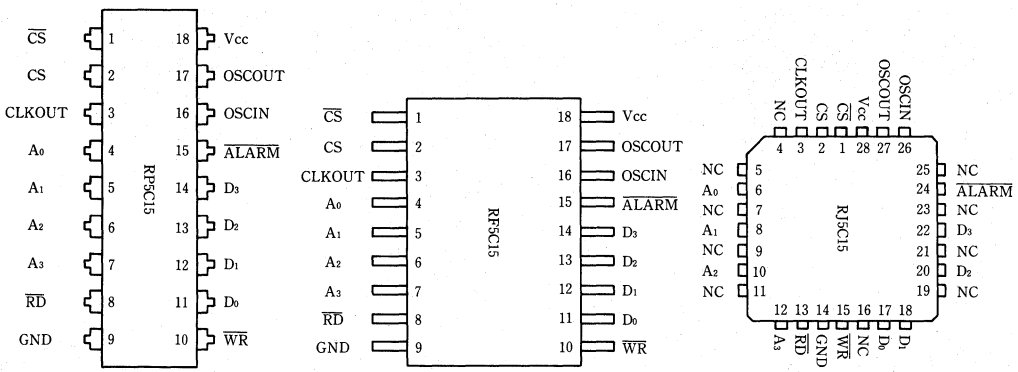
■ FEATURES

- Direct connection with CPU, and high speed access time.
- 4-bit bi-directional data bus $D_0 \sim D_3$
- 4-bit address input $A_0 \sim A_3$
- Counters for Time (hour, minute, second) and Calendar (leap year, year, month, date, day of the week) are built in.
- All the clock data are expressed with BCD code.
- ± 30 second adjustment function is built in.
- Battery backup is possible. (min. 2.0V)
- 16kHz, 1kHz, 128Hz, 16Hz, 1Hz, 1/60Hz are selectable as the reference clock.
- Alarm signal or timing pulse (16Hz or 1Hz) can be put out.

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



RP5C15 RF5C15 RJ5C15

■ PIN DESCRIPTION

Symbol	Function
$\overline{CS}$, CS	Terminals for external interfacing. Valid when CS=H, $\overline{CS}$=L. CS is connected to the power-down detector of peripheral power supply circiut and $\overline{CS}$ is connected to the microcomputer.
CLK OUT	Reference clock output terminal. Open drain output. 8 kinds of mode are selectable as seen in the table, according to content of the clock select register.
$A_0 \sim A_3$	ADDRESS pin. Connected to ADDRESS bus of CPU.
$\overline{RD}$	I/O control input. L when CPU←RP5C15.
GND	0 V
$\overline{WR}$	I/O control input. L when CPU→RP5C15.
$D_0 \sim D_3$	Bi-directional data bus. Connected to the data bus of CPU.
$\overline{ALARM}$	Alarm signal and pulse (16Hz CK or 1HzCK) are put out. Open drain output.
OSC IN, OSC OUT	Crystal resonator connecting terminal. 32.768kHz.
V_{CC}	+5V power supply.

■ ABSOLUTE MAXIMUM RATING

Symbol	Parameters	Conditions	Limits	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.3~7	V
V_I	Input Voltage		−0.3~7	V
V_O	Output Voltage		−0.3~7	V
P_d	Maximum Power Dissipation	Ta=25℃	400	mW
T_{opr}	Operating Ambient Temperature		−20~70	℃
T_{stg}	Storage Temperature		−40~125	℃

■ RECOMMENDED OPERATING CONDITIONS (Unless Noted : Ta=−20~70℃)

Symbol	Parameters	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{DH}	Data Hold Voltage	2.0		5.5	V
f_{XT}	Crystal Oscillation Frequency		32.768		kHz

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Unless Noted : Ta=−20~70℃, V_{CC}=5V±10%)

Symbol	Parameters	Measuring Conditions	Specified Value			Unit
			Min	Typ	Max	
V_{IH}	Input High Voltage		2.0		V_{CC}+0.3	V
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=2mA			0.4	V
I_{LI}	Input Leakage Current	V_I=0~5.5V			±10	μA
I_{OZ}	Output-off Leakage Current	V_{OZ}=0~5.5V			±10	μA
I_{CC1}	Standby Supply Current	f_{XT}=32.768kHz, V_{CC}=2.0V			15	μA
I_{CC2}	Operating Supply Current	f_{XT}=32.768kHz, V_{CC}=5.5 (NOTE1)			250	μA
V_{ILCS}	CS Pin Input "L" Voltage at Backup	V_{CC}=2.0V	−0.2		0.2	V
V_{IHCS}	$\overline{CS}$ Pin Input "H" Voltage at Backup	V_{CC}=2.0V	1.8		2.0	V

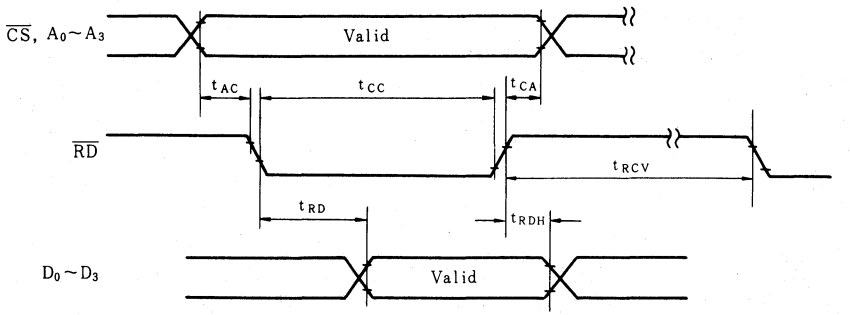
(NOTE 1) $\overline{RD}$, $\overline{WR}$ Signal Frequency : 100kHz, Input Terminal fixed V_{CC}, or GND level, Output Terminal Open

● AC ELECTRICAL CHARACTERISTICS (Unless Noted : Ta=−20~70℃, V_{CC}=5V±10%)

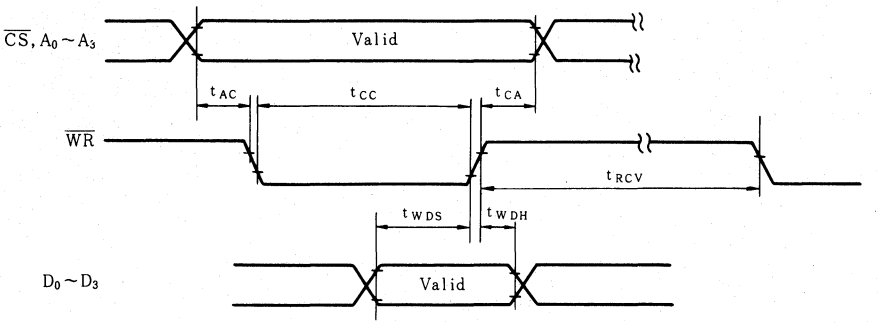
Symbol	Parameters	Measuring Conditions	Specified Value			Unit
			Min	Typ	Max	
t_{AC}	Address −$\overline{RD}$/$\overline{WR}$ Delay Time		50			ns
t_{CC}	$\overline{RD}$/$\overline{WR}$ Pulse Width		120		13,000	ns
t_{CA}	Address Valid Time After $\overline{RD}$/$\overline{WR}$ Rise		10			ns
t_{RD}	Data Delay Time After $\overline{RD}$ Fall	1TTL+100pF Load			120	ns
t_{RDH}	Data Hold Time After $\overline{RD}$ Rise		10			ns
t_{WDS}	Data Setup Time at Write in		100			ns
t_{WDH}	Data Hold Time at Write in		20			ns
t_{TED}	Timer Enable~Timer Disable		100			μs
t_{ADJ}	Adjust Completed Time				100	μs
t_{AINH}	Alarm Write Inhibit Time after Alarm set		100			μs
t_{RCV}	$\overline{RD}$/$\overline{WR}$ Recovery Time		1			μs

■ TIMING DIAGRAM

● READ CYCLE



● WRITE CYCLE



■ ADDRESS ASSIGNMENT

MODE		BANK 0				BANK 1				
A_3~A_0		D_3	D_2	D_1	D_0	Contents	D_3	D_2	D_1	D_0
0	1 Sec. Counter					CLK OUT Select Register	×			
1	10 Sec. Counter	×				adjust	×	×	×	
2	1 Min. Counter					Alarm 1 Min. Register				
3	10 Mins. Counter	×				Alarm 10 Mins Register	×			
4	1 Hr. Counter					Alarm 1 Hr. Register				
5	10 Hrs. Counter	×	×			Alarm 10 Hrs. Register	×	×		
6	Week Counter	×				Alarm Week Register	×			
7	1 Day Counter					Alarm 1 Day Register				
8	10 Days Counter	×	×			Alarm 10 Days Register	×	×		
9	1 Month Counter						×	×	×	×
A	10 Months Counter	×	×	×		12/24 Hour Selecter	×	×	×	
B	1 Year Counter					Leap Year Counter	×	×		
C	10 Years Counter						×	×	×	×
D	MODE Register	Timer EN	Alarm EN	×	BANK 1/0		Timer EN	Alarm EN	×	BANK 1/0
E	TEST Register	Test 3	Test 2	Test 1	Test 0		Test 3	Test 2	Test 1	Test 0
F	RESET Register	$\overline{1Hz}$ ON	$\overline{16Hz}$ ON	Timer RESET	Alarm RESET		$\overline{1Hz}$ ON	$\overline{16Hz}$ ON	Timer RESET	Alarm RESET

× : Don't care for WR, always 0 for RD.

■ CLOCK OUTPUT SELECT REGISTER

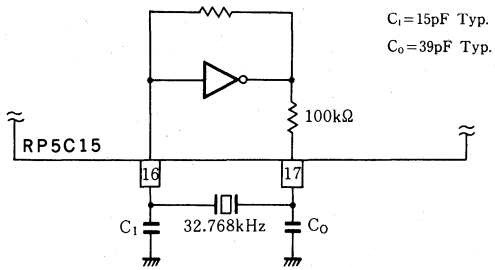
D_3	D_2	D_1	D_0	CLK OUT	Remark
×	0	0	0	"Z"	High Impedance
×	0	0	1	16.384kHz	duty 50%
×	0	1	0	1.024kHz	duty 50%
×	0	1	1	128 Hz	duty 50%
×	1	0	0	16 Hz	duty 50%
×	1	0	1	1 Hz	∫ Second Counter Count up, duty 50%
×	1	1	0	1/60 Hz	∫ Minute Counter Count up, duty 50%
×	1	1	1	"L"	

■ ADJUST FUNCTION

BANK 1 Address (A_3, A_2, A_1, A_0)=(0, 0, 0, 1) Data (D_3, D_2, D_1, D_0)=(×, ×, ×, 1)	If adjusted during the Second counter being 0~29, the Second comes to be 0, and if adjusted during 30~59, the minute is counted up, and the Second comes to be 0.

■ OSCILLATION CIRCUIT

As the output stabilizer resistor (≈100kΩ) is built in, it is not necessary to fix it externally.



● MODE REGISTER $(A_3, A_2, A_1, A_0) = (1, 1, 0, 1) = D$

D_3	D_2	D_1	D_0	
Timer EN	Alarm EN			
		×	0	BANK 0 : Setup and Read of time
		×	1	BANK 1 : Setup and Read of Alarm, $\overline{12h}$/24h and Leap year, Selection of CLK OUT Operation of Adjust.
	1			1 : Alarm output ENABLE
	0			0 : Alarm output DISABLE (16Hz and 1Hz signals are independent)
1				1 : Time count starts
0				0 : Time count after Second stops

● LEAP YEAR COUNTER

Leap year when $D_1 = D_2 = 0$. It counts up simultaneously with Year Counter.

● $\overline{12h}$/24h SELECTOR

24-hour counter when $D_0 = 1$

12-hour counter when $D_0 = 0$

PM when $D_1 = 1$, and AM when $D_1 = 0$ respectively of 10h counter

● RESET CONTROLLER 16 Hz · 1HzCK REGISTER

$(A_3, A_2, A_1, A_0) = (1, 1, 1, 1) = F$

$D_0 = 1$: Resetting of all alarm registers

$D_1 = 1$: Resetting of frequency divisions before Second

$D_2 = 0$: 16Hz CK pulse ON

$D_3 = 0$: 1Hz CK pulse ON

● ADDRESS 0~D

Both READ and WRITE are possible.

● ADDRESS E~F

WRITE only is possible.

● TEST REGISTER $(A_3, A_2, A_1, A_0) = (1, 1, 1, 0,) = E$

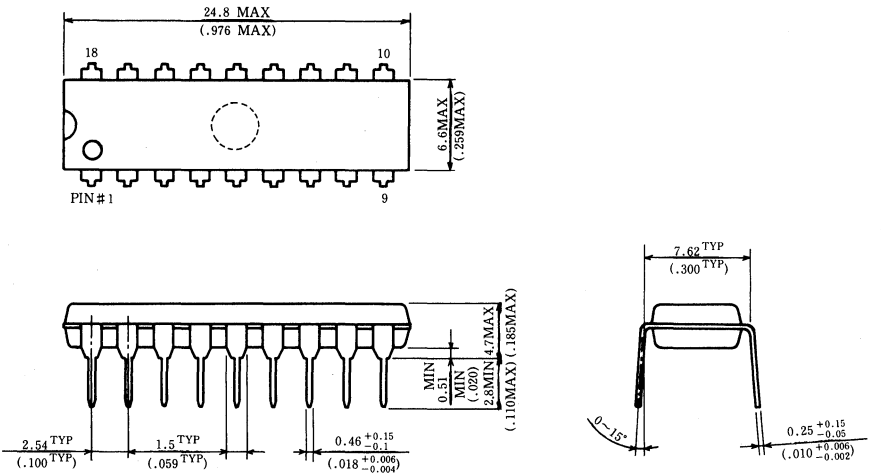
Register to be used for our inspection.

Normal count is operated by setting up data $(D_3, D_2, D_1, D_0) = (0, 0, 0, 0)$.

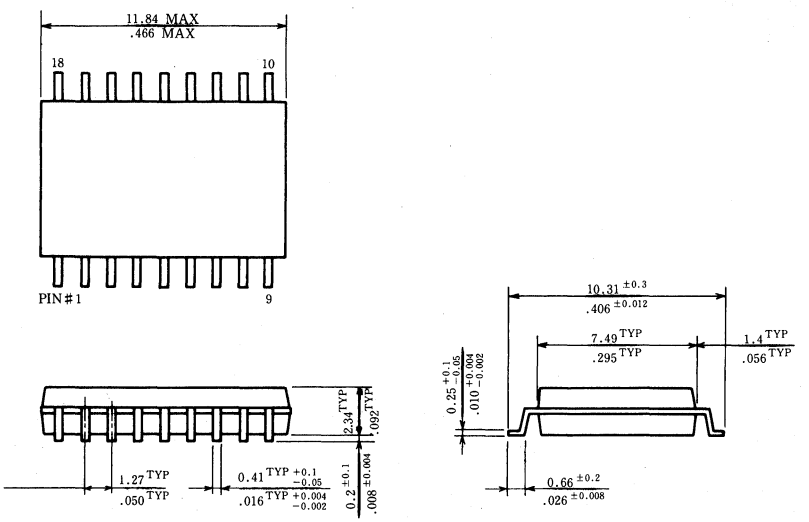
*Please refer to "Application Manual" that we offer.

■ PACKAGE DIMENSION (Unit: mm/inch)

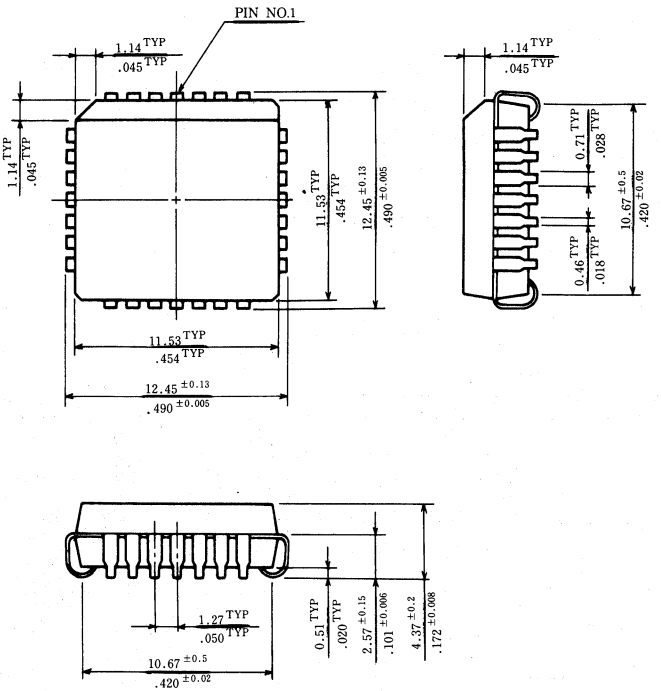
●RP5C15(18pin DIP)



●RF5C15(18pin FLAT)



● RJ5C15(24pin PLCC)



REAL TIME CLOCK

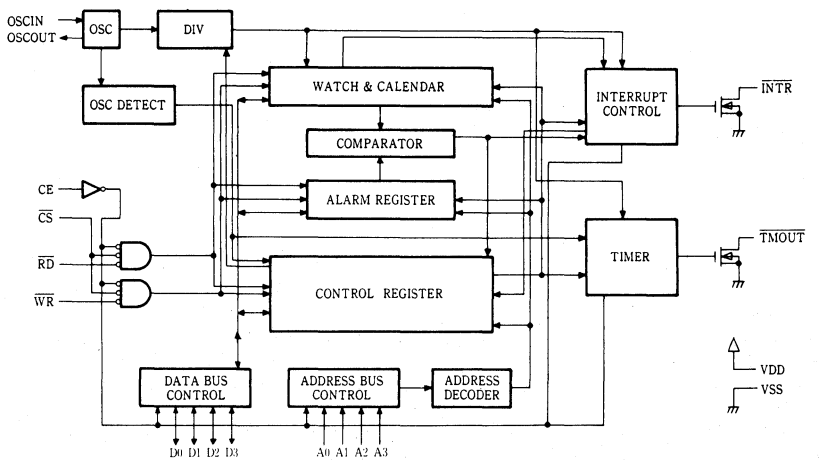
RP/RF5C62

RP5C62 and RF5C62 are CMOS real time clock LSIs for microcomputers. RP5C62 and RF5C62 have clock, calendar, and alarm functions. They can be directly connected to the data buses of 8 bit or 16 bit CPUs such as 8086, Z80, 6809, 6502 and 68000. With a built-in timer counter, they can be used as watch-dog-timer or interrupt timer.

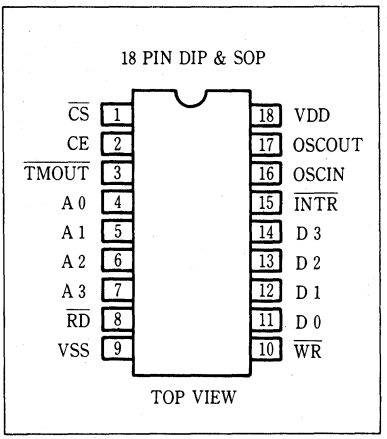
■ FEATURES

- Directly connected to CPU, enabling fast access.
- 4 bit bidirectional data bus, and 4 bit address bus.
- The oscillator is driven by a constant voltage, so the oscillation frequency is stable (within ±1 ppm) even when the power supply voltage fluctuates.
- Built-in timer counter using internal clock.
- Generates cyclic CPU interrupts, and generates alarm-match interrupts.
- Interrupt flag and interrupt inhibit.
- Clock (hour, minute, second), calendar (leap year, year, month, day, day of the week), alarm (hour, minute).
- 12- or 24-hour mode is selectable.
- Recognizes leap years automatically.
- All clock and alarm data expressed in BCD codes.
- ±30 seconds adjustment function.
- Determines whether clock data is valid or invalid.
- Consumes very low power due to CMOS technology, so it can be backed up by batteries.
- 5V single power supply.
- Package: 18-pin DIP for RP5C62, 18-pin SOP for RF5C62.

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Symbol	Name	Function
$\overline{CS}$ CE	Chip select Chip enable input	$\overline{CS}$ and CE are used when interfacing external devices. They may be accessed when $\overline{CS}$ is low and CE is high. CE is connected to a power down detector on the system power supply side, and $\overline{CS}$ is connected to the microcomputer address bus.
$\overline{TMOUT}$	Timer output	Timer output may be used as an interrupt free-run timer or watchdog timer. When CE is low (running on battery backup), operation stops (there is no output). It is N-ch open drain output.
A0 ~ A3	Address input	Address input is connected to the CPU address bus. It is gated internally with CE.
$\overline{RD}$	Read control input	When RD is set low, the contents of the counters or registers specified by A0~A3 are output to D0~D3. It is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
$\overline{WR}$	Write control input	When WR is low or rises from low to high, the contents of D0~D3 are written to registers or counters specified by A0~A3. $\overline{WR}$ is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
D0~D3	Bi-directional data bus	D0~D3 are connected to the CPU data bus. The input section is gated internally with CE. It is CMOS input/output.
$\overline{INTR}$	Interrupt output	$\overline{INTR}$ outputs timing CLOCK interrupts or alarm match interrupts to CPU. It also operates when CE is low (at battery backup). It is N-ch open drain output.
OSCIN OSCOUT	Oscillator circuit input/output	Crystal oscillator of 32.768 KHz must be connected between OSCIN and OSCOUT. Capacitance is connected externally between VDD and OSCIN and VDD and OSCOUT, forming the oscillator circuit.
VDD VSS	Power supply	VDD connects to +5V and VSS to ground.

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
VDD	Supply Voltage	VSS=0	−0.3 ~ +7.0	V
VI	Input Voltage		−0.3 ~ VDD+0.3	V
VO	Output Voltage		−0.3 ~ VDD+0.3	V
PD	Maximum Power Consumption	TA = 25°C	300	mW
TA	Operating Temperature		−20 ~ +70	°C
TSTG	Storage Temperature		−40 ~ +125	°C

■ RECOMMENDED OPERATING CONDITION

(VSS = 0V, TA = −20 ~ +70°C)

Symbol	Parameter	Condition	MIN.	Typ.	MAX.	Unit
VDD	Supply Voltage			5.0	6.0	V
VCLK	Supply Voltage of Clock		2.0		6.0	V
fXT	Crystal Oscillation Frequency			32.768		kHz

■ DC CHARACTERISTICS

Symbol	Parameter	Pin Name	Condition		MIN.	Typ.	MAX.	Unit
VIH1	"H" input voltage	A0~A3, D0~D3			2.2		VDD+0.3	V
VIL1	"L" input voltage	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$			−0.3		0.8	V
VIH2	"H" input voltage	CE			0.8*VDD		VDD+0.3	V
VIL2	"L" input voltage				−0.3		0.2*VDD	V
VOH1	"H" output voltage	D0~D3	IOH1 = −400μA		2.4			V
VOL1	"L" output voltage		IOL1 = 2mA				0.4	V
VOL2	"L" output voltage	$\overline{INTR}$, $\overline{TMOUT}$	IOL2 = 2mA				0.4	V
IILK	Input leak current	A0~A3, CE, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$	VILK = VDD or VSS		−1		1	μA
IOZ1	Output off leak current	D0~D3	VOZ1 = VDD or VSS		−5		5	μA
IOZ2		$\overline{INTR}$, $\overline{TMOUT}$	VOZ2 = VDD		−2		2	μA
IDD1	Consumption current for back-up	VDD	VDD=2.5V	Input: VDD or VSS			3	μA
IDD2	Consumption current for stand-by	VDD	VDD=5.5V	Output: OPEN			8	μA
∂f	Oscillation frequency drift for voltage drift	OSCIN OSCOUT	VDD=2.5~5.5V		−1		1	PPM

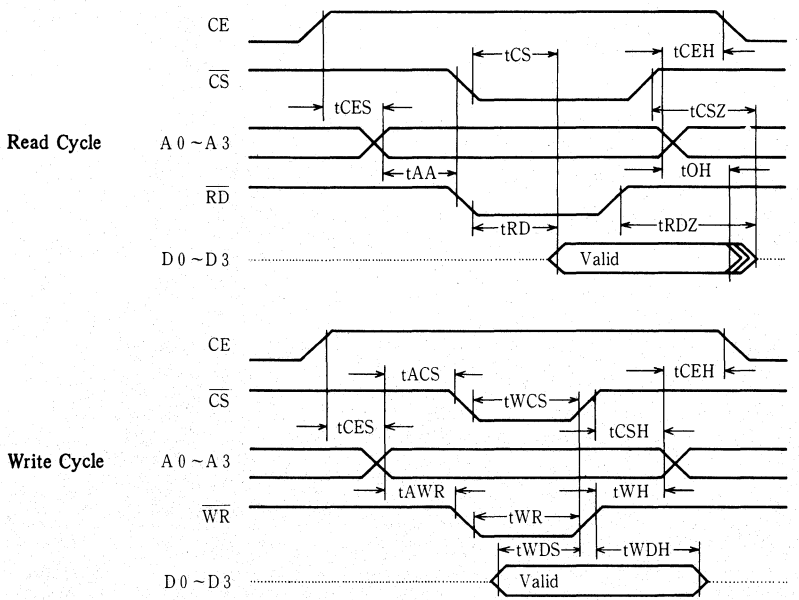
(Unless Noted, VSS=0V, VDD=5V±10%, TA=−20 ~ +70°C, X'tal=32.768KHz(CI≦35KΩ), CG=CD=33pF)

■ AC CHARACTERISTICS

(VSS=0V, TA=−20~70°C, Note1; VDD=5V±10%, Note2; VDD=3V±10%, Note3; VDD=5V±20%)

Symbol	Parameter	Description	Note1	Note2	Note3	Unit
tCES	CE setup time	Time for which CE must be kept "H" before the address is determined.	MIN 500	MIN 1000	MIN 500	nS
tCEH	CE hold time	Time for which CE must be kept "H" until the address finishes changing.	MIN 500	MIN 1000	MIN 500	nS
tAA	Address setup time (RD)	Time for which the address must be determined before $\overline{CS}$=$\overline{RD}$="L".	MIN 20	MIN 20	MIN 20	nS
tCS	$\overline{CS}$ setup time (RD)	Time between the trailing edge of $\overline{CS}$ and data output, after the address is determined and $\overline{RD}$="L" (CL=100 pF).	MAX 120	MAX 295	MAX 150	nS
tRD	$\overline{RD}$ setup time (RD)	Time between the trailing edge of $\overline{RD}$ and data output, after the address is determined and $\overline{CS}$="L" (CL=100 pF)	MAX 120	MAX 295	MAX 150	nS
tOH	Data hold time (RD)	Time for which data does not change though the address changes, when $\overline{CS}$=$\overline{RD}$="L"	MIN 10	MIN 10	MIN 10	nS
tCSZ	$\overline{CS}$ output delay time (RD)	Time between the rising edge of $\overline{CS}$ and the data bus line becoming high impedance.	MAX 70	MAX 95	MAX 75	nS
tRDZ	$\overline{RD}$ output delay time (RD)	Time between the rising edge of $\overline{RD}$ and the data bus line becoming high impedance.	MAX 70	MAX 95	MAX 75	nS
tACS	$\overline{CS}$ setup time (WR)	Time for which the address must be determined before the trailing edge of $\overline{CS}$ while $\overline{WR}$ is "L".	MIN 20	MIN 20	MIN 20	nS
tAWR	$\overline{WR}$ setup time (WR)	Time for which the address must be determined before the trailing edge of $\overline{WR}$ while $\overline{CS}$ is "L".	MIN 20	MIN 20	MIN 20	nS
tWCS	$\overline{CS}$ pulse width (WR)	Pulse width when writing by $\overline{CS}$ while $\overline{WR}$ is "L".	MIN 120	MIN 195	MIN 150	nS
tWR	$\overline{WR}$ pulse width (WR)	Pulse width when writing by $\overline{WR}$ while $\overline{CS}$ is "L".	MIN 120	MIN 195	MIN 150	nS
tWDS	Data setup time (WR)	Time for which the data must be determined before the rising edge of $\overline{CS}$ or $\overline{RD}$.	MIN 60	MIN 95	MIN 75	nS
tCSH	Address $\overline{CS}$ hold time (WR)	Time for which the address needs to be held after the rising edge of $\overline{CS}$.	MIN 10	MIN 10	MIN 10	nS
tWH	Address $\overline{WR}$ hold time (WR)	Time for which the address needs to be held after the rising edge of $\overline{WR}$.	MIN 10	MIN 10	MIN 10	nS
tWDH	Data hold time (WR)	Time for which the data needs to be held after the rising edge of $\overline{CS}$ or $\overline{WR}$.	MIN 10	MIN 10	MIN 10	nS

■ TIMING DIAGRAM

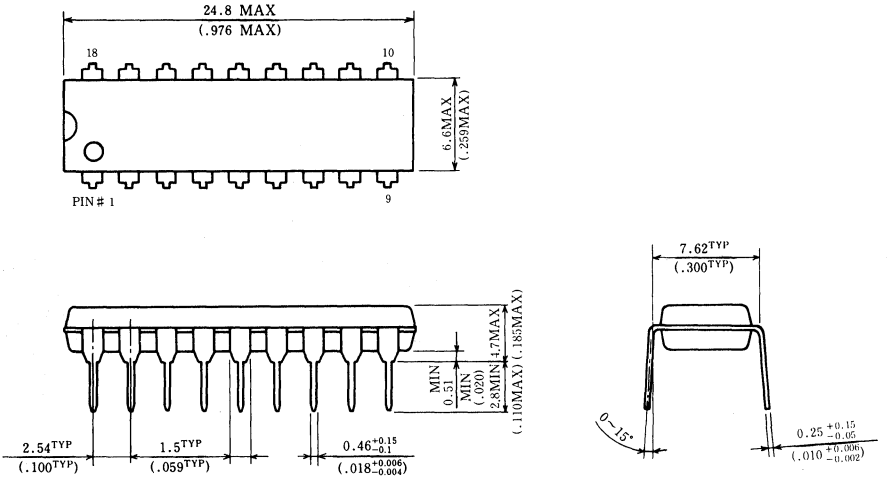


Input/Output Condition

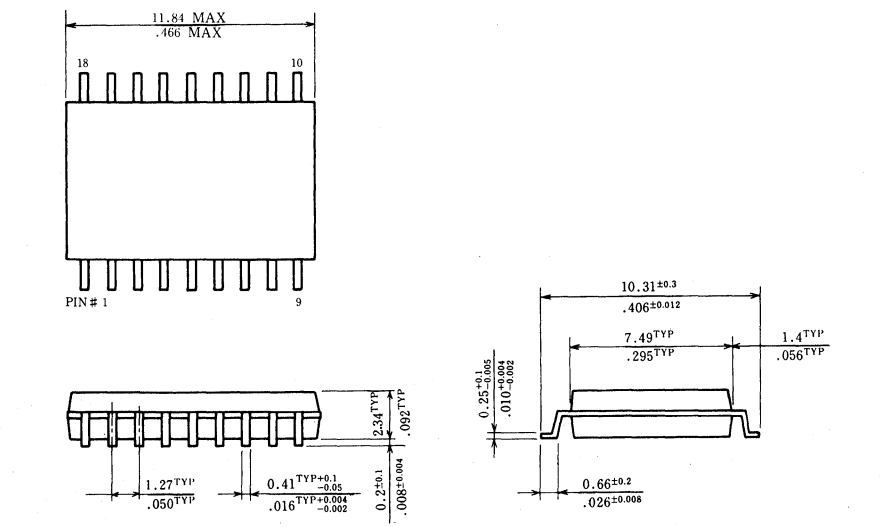
(VDD= 5V±10%)	(VDD= 3V±10%)	(VDD= 5V±20%)
VIH = 2.2V	VIH = 0.8×VDD	VIH = 2.4V
VIL = 0.8V	VIL = 0.2×VDD	VIL = 0.4V
VOH ≧ 2.2V	VOH = 0.8×VDD	VOH ≧ 2.4V
VOL ≦ 0.8V	VOL = 0.2×VDD	VOL ≦ 0.4V

■ PACKAGE DIMENSION (Unit: mm/inch)

- RP5C62 (18pin DIP)



- RF5C62 (18pin SOP)



RF5C16A/RP5C16 CRT CONTROLLER

■ General description

RP5C16/RF5C16A are LSI developed under CMOS process technology for application to CRT controller. They allow to display the various patterns on the CRT by control commands and image data fed from 8 bit CPU including 8085, Z80, etc. With use of this 5C16, CRT controller system can be configurated by merely connecting DRAM.

Note)

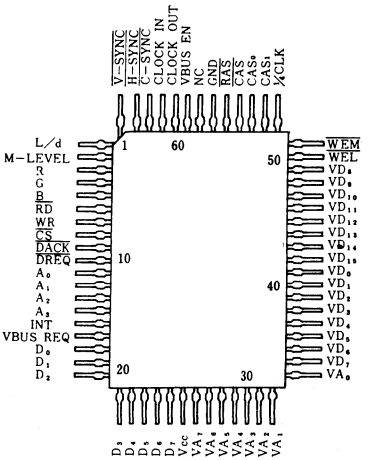
RF5C16A is the 64 pin FLAT packaged product.
RP5C16 is the 64 pin DIL packaged product.

■ Features

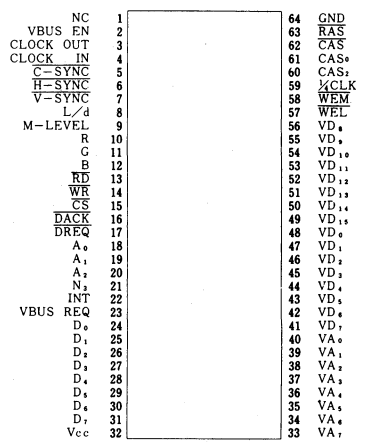
- 4 modes
  - ·Color picture with 80 X 25 characters
  - ·Color picture with 640 X 200 dots
  - ·2 color pictures with 40 X 25 characters and 40 X 25 characters
  - ·2 color pictures with 320 X 200 dots and 40 X 25 characters
- Display of maximum 15 colors with RGB output (2 values or 3 values)
- Virtual screen
- Smooth scroll to horizontal and vertical directions are practicable.
- Abundant attribute function (transverse invert, longitudinal invert, vertical invert and black white invert)
- Cursor built-in (for mouse)
- Master/Slave mode (Superimpose practicable)
- Redefinable character set
- Buffer register and address counter built-in for updating of V-RAM (Video RAM)
- Low power consumption for the sake of CMOS process
- 60 Hz non-interlace display

■ Pin configuration

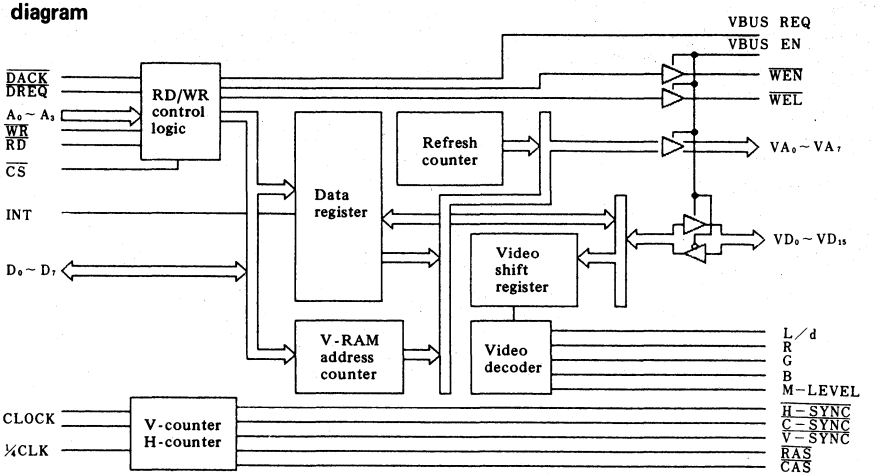
RF5C16A



RP5C16



■ Block diagram



■ Pin description

(1) CPU interface

Symbol	Name	Input/output	Logic	Function
$\overline{CS}$	Chip Select	IN	Active L	Make it possible to Read and Write of control register, address register and buffer register
$\overline{RD}$	Read Strobe	IN	L	
$\overline{WR}$	Write Strobe	IN	L	
A_0~A_3	Address 0 ~ Address 3	IN	(positive)	Selective line of control register
D_0~D_7	Data 0 ~ Data 7	IN/OUT	(positive)	Data bus Data 0 = LSB Data 7 = MSB
INT	Interrupt	OUT	Active H	
$\overline{DREQ}$	DMA Request	OUT	L	
$\overline{DACK}$	DMA Acknowledge	IN	L	

(2) V-RAM interface

Symbol	Name	Input/output	Logic	Function
$\overline{RAS}$	ROW Address Strobe	OUT	Active L	Set Row Address, Provide Timing
$\overline{CAS}$	Column Address Strobe	OUT	L	Set Column Address, Provide Timing
$\overline{CAS_0}$	Column Address Strobe 0	OUT	L	$\overline{CAS}$ which turns to active only when address is 0~3 FFFH.
$\overline{CAS_1}$	Column Address Strobe 1	OUT	L	$\overline{CAS}$ which turns to active only when active is 4000H~7 FFFH.
VBUS EN	VIDEO BUS ENABLE	IN	H	When L, it turns $\overline{CAS}$, $\overline{CAS_0}$, $\overline{CAS_1}$, $\overline{RAS}$, $\overline{WEL}$, $\overline{WEM}$, $VA_{0\sim7}$ and $VD_{0\sim15}$ to Hi-Z.
VBUS REQ	VIDEO BUS REQUEST	OUT	H	5C16 accesses VBUS, it turns to active before 4 clock.
$\overline{WEM}$	Write Enable MSB	OUT	L	Write is early write operation
$\overline{WEL}$	Write Enable LSB	OUT	L	Write is early write operation
VA_0~VA_7	Video Memory Address 0~7	OUT	(positive)	
VD_0~VD_{15}	Video Memory Data 0~15	IN/OUT	(positive)	Data 0 = LSB Data 15 = MSB

(3) Clock and Video output

Symbol	Name	Input/output	Logic	Function
CLOCK IN CLOCK OUT	Clock In Clock Out			14.31818 MHz which connects quartz crystal.
M-LEVEL	Middle Level	IN		When RGB3 value output, it provides CRTC with intermediate level
Vcc, GND	Vcc, GND	–	–	
R, G, B L/d	Red, Green, Blue Light and dark	OUT	(positive)	Video output (2 values or 3 values)
$\overline{\text{C-SYNC}}$	Composite Synchronous	OUT/IN	(negative)	Output (open drain output) when master mode and input H-SYNC when slave mode
$\overline{\text{V-SYNC}}$	Vertical Synchronous	OUT/IN	(negative)	Output (open drain output) when master mode and input V-SYNC when slave mode
$\overline{\text{H-SYNC}}$	Horizontal Synchronous	OUT/IN	(negative)	Output (open drain output) when master mode and input H-SYNC when slave mode
¼ CLK	¼ CLOCK	OUT		Clock ¼ frequency division output

■ Absolute maximum rating

Symbol	Parameter	Condition	Value	Unit
Vcc	Supply voltage		−0.3 ~ +7.0	V
VI	Input voltage		−0.3 ~ +7.0	V
VO	Output voltage		−0.3 ~ +7.0	V
Pd	Maximum power consumption	Ta = 25°C	300	mW
Ta	Operating ambient temperature		−10 ~ 70	°C
Tstg	Storage temperature		−40 ~ 125	°C

■ Recommended operating condition

Symbol	Parameter	Condition	Value	Unit
Vcc	Supply voltage		4.5 ~ 5.5	V
Vss	Supply voltage		0	V
VIH	"H" input voltage		2.0 ~ Vcc + 0.3	V
VIL	"L" input voltage		−0.3 ~ 0.8	V
Ta	Ambient temperature		−10 ~ 70	°C

■ DC electrical characteristics (Vcc = 5.0V ± 10%, Ta = −10 ~ 70°C)

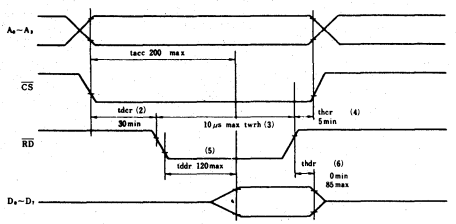
Symbol	Parameter	Condition	Value			Unit
			Min.	Typ.	Max.	
VIH	"H" input voltage		2.0		Vcc + 0.3	V
VIL	"L" input voltage		−0.3		0.8	V
VOH	"H" output voltage	IOH = −400 μA	2.4			V
VOL	"L" output voltage	IOL = 3.2 mA			0.4	V
ILI	Input leakage current	0 ≦ VI ≦ Vcc			10	μA
ILO	3-state floating current	0.4 ≦ VI ≦ 2.4			10	μA
Icc	Supply current				50	mA
VINφ	Clock input "H" input voltage		0.7 x Vcc			V
VILφ	Clock input "L" input voltage				0.3 x Vcc	V

■ AC characteristics (Vcc = 5.0V ± 10%, Ta = −10~70°C) and Timing diagram (Unit : ns)

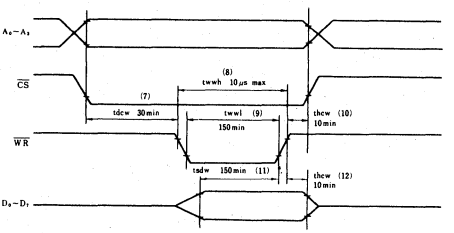
(1) CPU-5C16 READ/WRITE

No.	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
1	tacc	Access time from $\overline{CS}$, A_0~A_3 and $\overline{DACK}$			200	ns
2	tdcr	$\overline{RD}$ delay time from $\overline{CS}$, A_0~A_3 and $\overline{DACK}$	30			ns
3	twrh	$\overline{RD}$ pulse width (H-threshold)			10	ns
4	thcr	$\overline{CS}$, A_0~A_3 and $\overline{DACK}$ hold time during read	5			ns
5	tddr	Data delay time from $\overline{RD}$			120	ns
6	thdr	Data hold time during read	0		85	ns
7	tdcw	$\overline{WR}$ delay time from $\overline{CS}$, A_0~A_3 and $\overline{DACK}$	30			ns
8	twwh	$\overline{WR}$ pulse width (H-threshold)			10	ns
9	twwl	$\overline{WR}$ pulse width (L-threshold)	150			ns
10	thcw	$\overline{CS}$, A_0~A_3 and $\overline{DACK}$ hold time from $\overline{WR}$	10			ns
11	tsdw	Data setup time	150			ns
12	thdw	Data hold time during write	10			ns
13	tddgl	$\overline{DREQ}$ ↓ delay time from CLK OUT			90	ns
14	tddgh	$\overline{DREQ}$ ↑ delay time from CLK OUT			60	ns
15	tdinl 1	INT ↓ delay time from $\overline{RD}$ or $\overline{WR}$ (End of INT by Buffer Ready)			410	ns
16	tdinl 2	INT ↓ delay time from CLK OUT			120	ns
17	tdinh	INT ↑ delay time from CLK OUT			90	ns

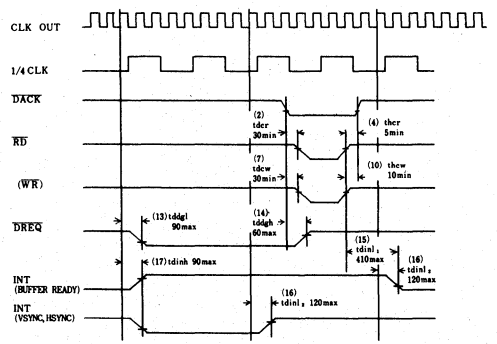
(1−1) CPU READ 5C16



(1−2) CPU WRITE IN 5C16



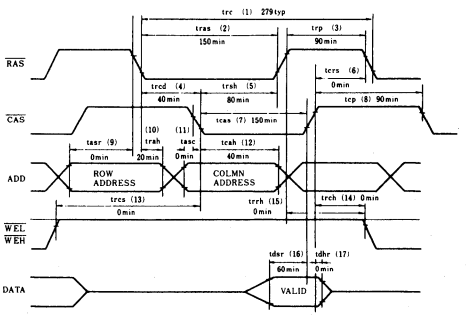
(1−3) INT, $\overline{DREQ}$, $\overline{DACK}$



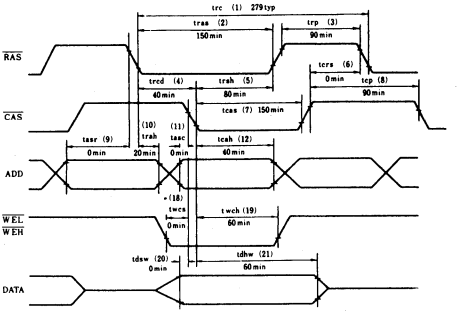
(2) 5C16-V-RAM READ/WRITE

No.	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
1	trc	Read cycle time	270	279		ns
2	tras	$\overline{RAS}$ pulse width	150			ns
3	trp	$\overline{RAS}$ pre-charge time	90			ns
4	trcd	$\overline{RAS}$-$\overline{CAS}$ delay time	40			ns
5	trsh	$\overline{RAS}$ hold time	80			ns
6	tcrs	$\overline{CAS}$-$\overline{RAS}$ setup time	0			ns
7	tcas	$\overline{CAS}$ pulse width	150			ns
8	tcp	$\overline{CAS}$ pre-charge time	60			ns
9	tasr	Line address setup time	0			ns
10	trah	Line address hold time	20			ns
11	tasc	Column address setup time	0			ns
12	tcah	Column address hold time ($\overline{CAS}$ reference)	40			ns
13	trcs	Read command setup time	0			ns
14	trch	Read command hold time ($\overline{CAS}$ reference)	0			ns
15	trrh	Read command hold time ($\overline{RAS}$ reference)	0			ns
16	tdsr	Data input setup time ($\overline{CAS}$ reference)	60			ns
17	tdhr	Data input hold time ($\overline{CAS}$ reference)	0			ns
18	twcs	Write command setup time	0			ns
19	twch	Write command hold time ($\overline{CAS}$ reference)	60			ns
20	tdsw	Data input setup time ($\overline{CAS}$ reference)	0			ns
21	tdhw	Data input hold time ($\overline{CAS}$ reference)	60			ns
22	tdvr	VBUS REQ delay time from CLK OUT			90	ns
23	thve	Hold time of VBUS EN against CLK OUT	40			ns
24	tsve	Setup time of VBUS against CLK OUT	0			ns
25	tdral	$\overline{RAS}$ ↓ delay time from CLK OUT			100	ns
26	tdraf	Delay time for $\overline{RAS}$ from CLK OUT to turn to floating	0		60	ns
27	tdwev	Delay time for $\overline{WEL}$ or $\overline{WEM}$ from CLK OUT to turn to valid			70	ns
28	tdwef	Delay time for $\overline{WEL}$ or $\overline{WEM}$ from CLK OUT to turn to floating	0		60	ns
29	tdcav	Delay time for $\overline{CAS}$, $\overline{CAS_0}$ and $\overline{CAS_1}$ from CLK OUT to turn from floating to valid			70	ns
30	tdcaf	Delay time for $\overline{CAS}$, $\overline{CAS_0}$ and $\overline{CAS_1}$ from CLK OUT to turn to floating	30		130	ns
31	tdvav	Delay time for $VA_{0\sim7}$ and $VD_{0\sim15}$ from CLK OUT to turn from floating to valid			70	ns
32	tdvaf	Delay time for $VA_{0\sim7}$ and $VD_{0\sim15}$ from CLK OUT to turn to floating	0		60	ns

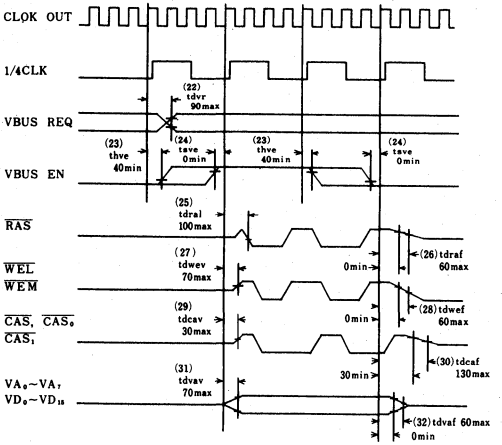
(2–1) 5C16 READ V-RAM



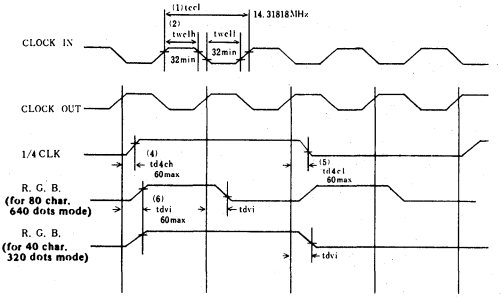
(2–2) 5C16 WRITE V-RAM



(2–3) VBUS REQ, VBUS EN



(3–1) CLK IK, CLK OUT



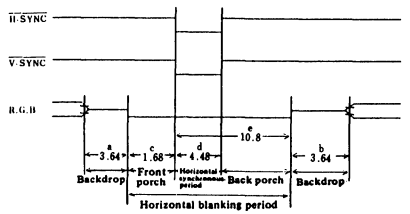
(3) CLK IN, CLK OUT

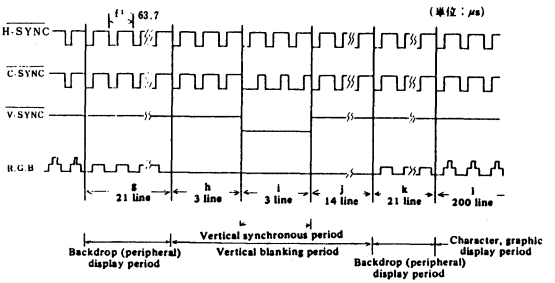
No.	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
1	tccl	Clock frequency	−300	14.318 18	+300	MHz ppm.
2	twch	Clock pulse width (H period)	32			ns
3	twcl	Clock pulse width (L period)	32			ns
4	td4ch	¼ CLK ↑ delay time from CLK OUT			60	ns
5	td4cl	¼ CLK ↓ delay time from CLK OUT			60	ns
6	tdvi	RGB delay time from CLK OUT			60	ns

(4) SYNC wave, R.G.B. output

No.	Symbol	Parameter	Value	Unit
7	a	Backdrop (peripheral) display period front porch side	3.64±0.50	μs
8	b	Backdrop (peripheral) display period back porch side	3.64±0.50	μs
9	c	Front porch	1.68±0.30	μs
10	d	Horizontal synchronous period	4.48±0.30	μs
11	e	Horizontal synchronous period + back porch	10.80±0.30	μs
12	f	Horizontal synchronous signal cycle	63.70±0.50	μs
13	g	Display period of backdrop (peripheral)	21	line
14	h	Blanking period before vertical synchronous period	3	line
15	i	Vertical synchronous period	3	line
16	j	Blanking period after vertical synchronous period	14	line
17	k	Display period of backdrop (peripheral)	21	line
18	l	Display period of character and graphic	200	line

(4–1) SYNC wave, R.G.B. output (Unit : μs)





■ Connectible CPU

8085 6MHz 8085AH-2 8085A-2
Z-80 6MHz Z-80B
6502 3MHz 65C02B
16bitCPU

■ Usable memory

64 X 1bit, 16k X 4bit or 64k X 4bit
·Use Tacc (access time) of below 120 ns.
·Memory at maximum 128K byte is usable.

■ Table of control register

〈WR〉

Register No.	Data b7 b6 b5 b4 b3 b2 b1 b0	CONTENTS
0	TR-L	Transfer Register – L
1	TR-M	Transfer Register – M
2	Add-L	Transfer Address – L
3	Add-M	Transfer Address – M
4	MV MH MB DMA 1/2 byWR byRD ML/L	Transfer mode interrupt mask
5	MODE FG-on BG-on R-on M/S AH	Display mode
6	CsHL	Cursor coordinate HL
7	CsV	Cursor coordinate V
8	BCG-M X CsHm	Chara. Gen. Base Address M cursor coordinate CsHm
9	BFG-M × ×	Fore Ground Base Address M
A	BBG-L	Back Ground Base Address L
B	BBG-M	Back Ground Base Address M
C	CFG3 CFG2	FG 3rd color FG 2 color
D	CBG3 CBG2	BG 3rd color BG 2 color
E	CBD-p CBD-c	BD color (peripheral) BD color (center)
F	SL SV × SH	Dot Scroll V direction H direction

〈RD〉

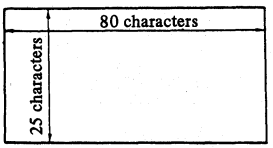
0	TR-L	Transfer Register – L
1	TR-M	Transfer Register – M
2	Add-L	Transfer Address – L
3	Add-M	Transfer Address – M
4	MV MH MB X FV FH FB X	Interrupt flag

■ Description of function

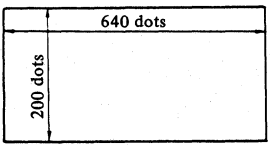
(1) Display mode

- Following 4 display modes are available.

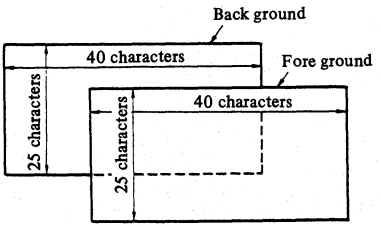
A. 80 character X 25 line character display mode (only back ground)



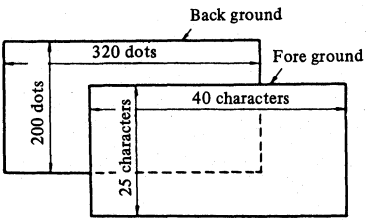
B. 640 X 200 dot graphic dispaly mode (only back ground)



C. 40 characters – 40 character display mode

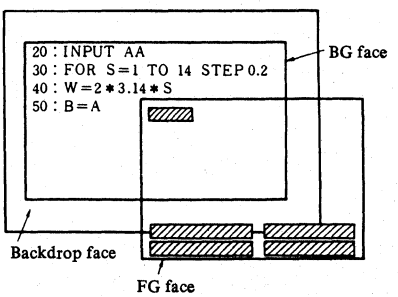


D. 40 character – 320 dot display



(2) Picture simultaneous display (display mode 3 and 4)

- 2 pictures of fore ground face and back ground face are simultaneously displayed.
- When overlapping of FG face pattern with BG face pattern, FG face is displayed.
- In case where there is neither pattern present on FG face nor on BG face, backdrop color (CBD-C) is displayed.
- As far as the distance ranging from the outside of display window to the edge of cathode ray tube, the color of backdrop face (CBD-P) is displayed. (Backdrop color is specified by register E)



(3) 15 color display

15 colors can be displayed.

Color code				Color	Color code				Color
L/d	B	G	R		L/d	B	G	R	
0	0	0	0	Black	1	0	0	0	Black
0	0	0	1	Red	1	0	0	1	Pink
0	0	1	0	Green	1	0	1	0	Light Green
0	0	1	1	Yellow	1	0	1	1	Light Yellow
0	1	0	0	Blue	1	1	0	0	Light Blue
0	1	0	1	Magenta	1	1	0	1	Light Magenta
0	1	1	0	Cyan	1	1	1	0	Light Cyan
0	1	1	1	Gray	1	1	1	1	White

(4) R, G, B output

- Following outputs are held as image signal. R, G, B, L/d, $\overline{\text{C-SYNC}}$, $\overline{\text{V-SYNC}}$ and $\overline{\text{H-SYNC}}$
- RGB terminal takes the following output levels at 3 value output.

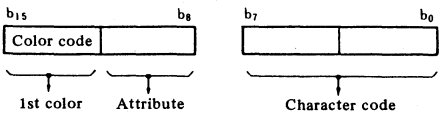
	Min.	Max.
High	4.4	Vcc
Middle	M-LEVEL−0.6	M-LEVEL+0.4
Low	−	0.4

Vcc = 5V, M-LEVEL = 2.5V, Io = ±1mA

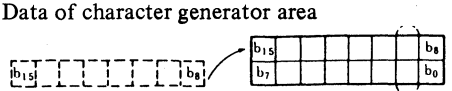
- $\overline{\text{V-SYNC}}$, $\overline{\text{C-SYNC}}$ and $\overline{\text{H-SYNC}}$ terminals turn to output terminal (open drain) under master mode and to input terminal under slave mode.
  (Refer "Terminal function (3) Clock and Video output")

(5) Character display

- The size of character at character display is 8 X 8 dots.
- Fonts are kept in memory area of 2K words from character generator base address (BCG-M). (Max. 256 kinds)
- Data of code area



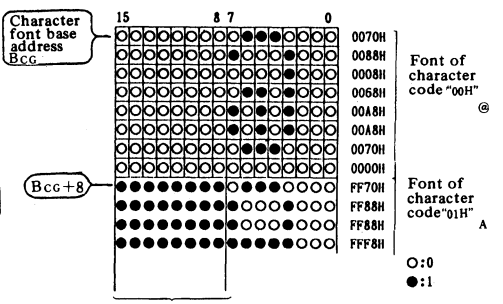
- Data of character generator area



Character generator value	Display color
00	Clear
01	1st color
10	2nd color
11	3rd color

2nd and 3rd colors are specified by control register (C, D).

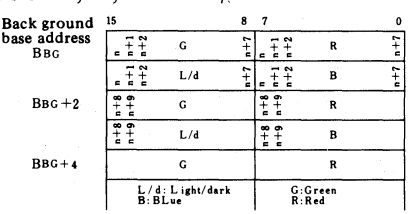
- Configuration of character font

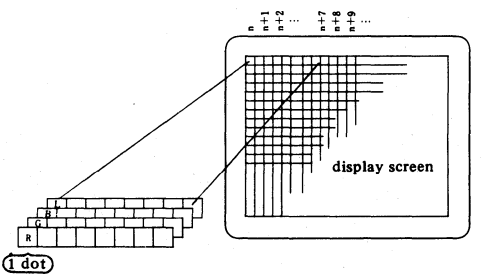


- When displaying MSByte in single color such as alphanumeric character, etc., all "0" or all "1" is used.
- When drawing the picture such as game, etc, 4 colors can be displayed at each dot with 2 bit of combination such as bit 15 with bit 7, bit 14 with bit 6 and so on.

(6) Graphic display

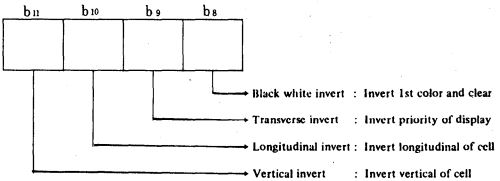
- 1 dot is consisted of 4 bits, and 8 dots are allocated as 1 block.
- Display color is decided by 4 face synthesis of R, G, B and L/d.

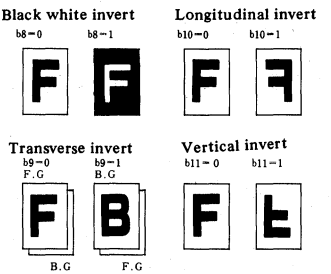




(7) Attribure (character display)

- 4 kinds of attribute can be decided with bit 8 ~ bit 11 of code area data.

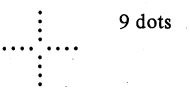




(8) Cursor

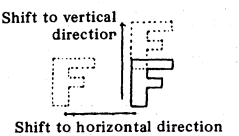
- Cross hair cursor is displayed. The coordinate of cursor in the horizontal direction is specified with 10 bits of cursor register CsHm and CsHL while in the vertical direction with 8 bits of CsV. 2 bits of cursor register CsHm will not become effective unless CsHL is written.

Shape of cursor



(9) Dot scroll (only back ground)

- It allows scroll of 0~7 dots in the horizontal and vertical directions. The number of shift to the horizontal and vertical directions is specified by respective dot scroll register SH and SV.



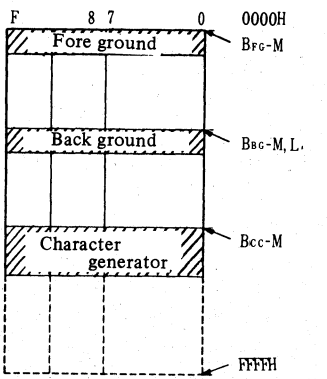
(10) Control of video memory area

- Base address

BG base address (BBG-M, BBG-L) is consisted of 16 bits and allows to specify by 1 character unit. Therefore, the change of BG base address allows scroll in the column or line direction. BBG-M becomes effective when BBG-L is written. Those subsequent to this address area fall in code data of back ground. In case of graphic, too, data are stored here.

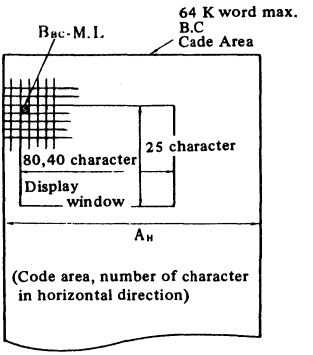
FG base address (BFG-M) allows paging of each 1,024 characters with 6 bit. Subsequent to this address, code data of fore ground are stored in 1,000 words (40 character X 25 line).

Character generator base address (BCG-M) is able to specify the start address of character font for each 2,048 words with 5 bit. Character font is consisted of 1 cell 8 words and is able to select 256 patterns. (Refer diagram) It will not be used for only graphic display.



- Width of code area (No. of character AH)

  FG is fixed with 40 characters. BG can be selected from 40 characters (320 dots), 64 characters (512 dots), 80 characters (640 dots) and 128 characters (1,024 dots). With this, the width of virtual screen is set.



(11) Updating function of frame buffer

- Since it has the transfer register and address counter, it allows read/write of frame buffer data, making use of retrace line section in horizontal/vertical direction without relying on externally mounted circuit.
- Write mode/read mode/read modify write mode (see diagram below)
- Word transfer/Byte transfer (see diagram below)

	Write mode		Read mode		Read modify write	
	Word transfer	Byte transfer	Word transfer	Byte transfer	Word transfer	Byte transfer
Read TR-M	–	–	–	Add+1-RT	–	–
Read TR-L	–	–	Add+1-RT	Add+1-RT	–	–
Write TR-M	–	WT-Add+1	–	WT	–	WT-Add+1 -RT
Write TR-L	WT-Add+1	WT-Add+1	WT	WT	WT-Add+1 -RT	WT-Add+1 -RT
Read Add-M	–	–	–	–	–	–
Read Add-L	–	–	–	–	–	–
Write Add-M	–	–	–	–	–	–
Write Add-L	–	–	RT	RT	RT	RT

TR : Transfer register
Add: Address counter
RT : Read transfer (frame buffer read)
WT : (frame buffer write)

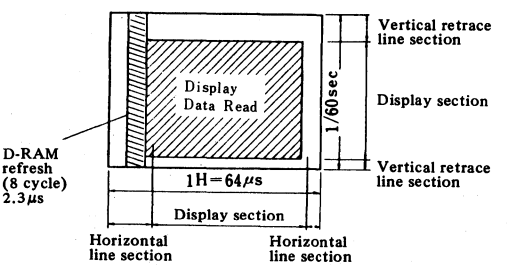
The relationship " – " between read/write operation of transfer register and read/write toward frame buffer represents the sequence of process. For example, when CPU side read TR-L register under (read mode), first of all, number of address counter is set as +1, then, perform read of frame buffer. " – " represents that no steps are being taken for frame buffer.

- The mode of increment +1/+2+2 of address counter is used in graphic display, for example, only the face of BLUE is rewritten in sequence.
- DMA transfer

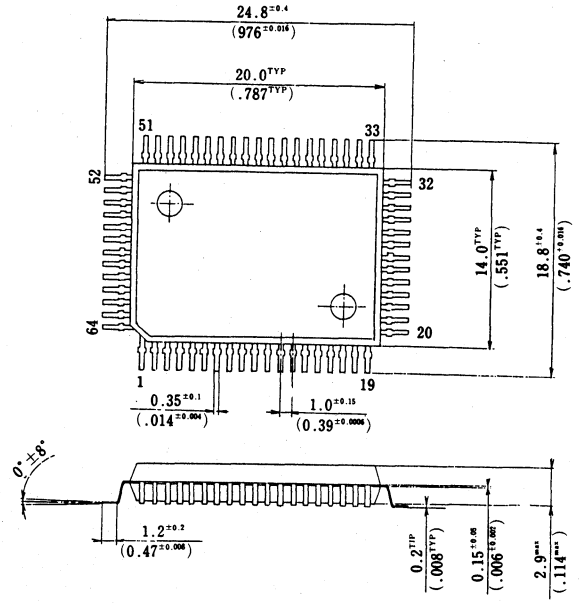
  In case of DMA transfer, it is necessary to set whether to read or write to LSB of transfer register, or to read or write to MSB. In case of word transfer, TR-L and TR-M vary at every 1 byte. In case of byte transfer, it is always written in the register that has been set.

(12) D-RAM refresh

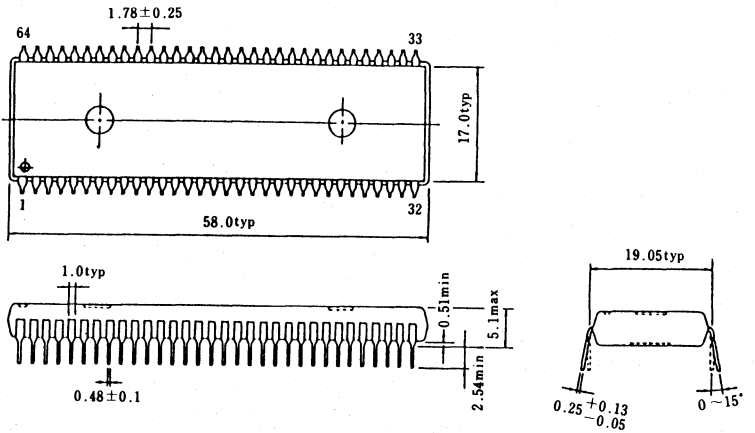
- 8 addresses per 1 H (64 μs) are refreshed within retrace line section.



■ 64pin flat package dimension (Unit : mm)



■ 64pin DIL package dimension (Unit : mm)



QUAD.UART
RF5C59

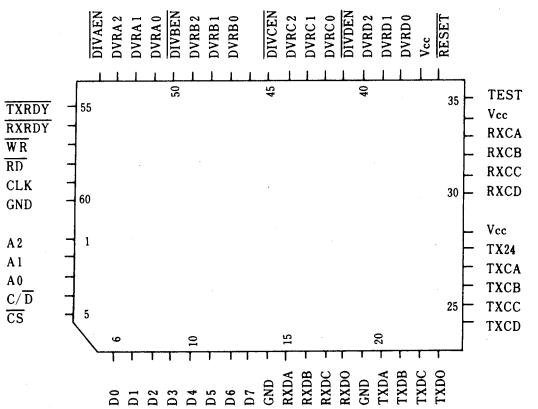
■ GENERAL DESCRIPTION

RF5C59 is the CMOS LSI with 4 channels of serial port built-in for application to asynchronous communication. The operations including transfer rate, transmit/receive of communication and etc. can be specified by program independently for each channel and it allows the use as peripheral circuit of CPU.

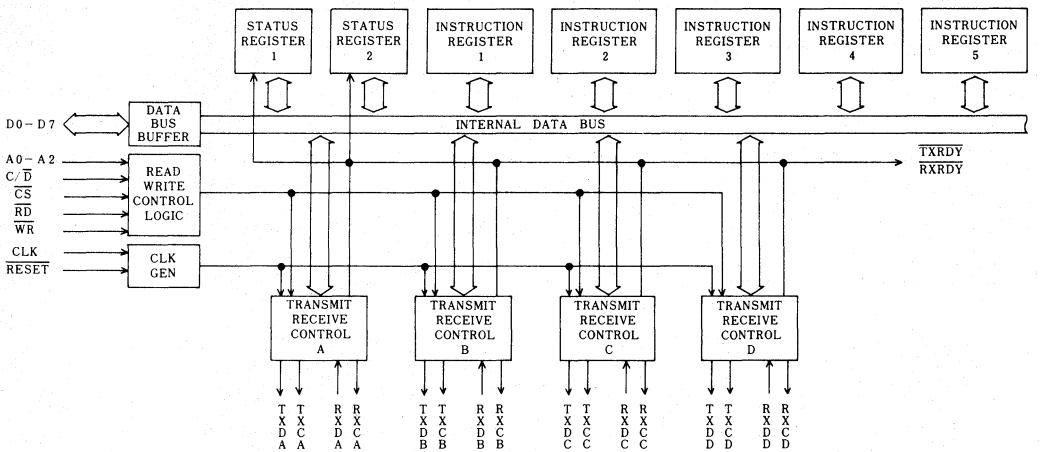
■ FEATURES

- Double-buffer mode transmitter/receiver
- Dual transmit/receive of communication is practicable for all 4 channels.
- Setting of transfer rate at each channel for both hardware and software is practicable.
  When input clock is 14.7456 MHz, the following rates are applicable.
  614.4 KHz, 307.2 KHz, 153.6 KHz, 76.8 KHz, 38.4 KHz, 19.2 KHz, 9.6 KHz and 4.8 KHz.
- Freedom of combination of logical address with physical address for 4 channels.
- Data length 8 bit, stop bit 1 bit fixed.
- Overrun and framing error are detectable.
- Error start bit is detectable.
- Direct connection to 8 bit bidirectional data bus and data bus is practicable.
- 4 bit address input.
- Hardware interrupt signal of $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ that can be masked.
- Connection to high speed CPU is practicable.
- 5V single voltage supply.
- 60 pin flat package.

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ DESCRIPTION OF FUNCTION

RF5C59, which is the UART for data communication, is used as peripheral circuit of CPU, and operation under serial data transfer mode can be specified with program.

RF5C59 has the transmit/receive ports with 4 channels, which receive parallel data from CPU, convert them into serial data and feed them out from TXD * terminal. In addition, RF5C59 receives data fed to RDX * terminal and feed them to CPU.

All 4 channels are controllable independently. Reading of status register 1 will not only make it possible to find the condition of transmit/receive operation but also allow to notify CPU of hardware interrupt signal from $\overline{\text{TXRDY}}$ terminal and $\overline{\text{RXRDY}}$ terminal.

The combination of logical port with physical port can be freely set with instruction register 3. In other words, logical ports in plural number can be assigned to one physical port. The transfer rate is 1/(24 * n) of input clock. (n : 1, 2, 4, 8, 16, 32, 64, 128)

■ PIN DESCRIPTION

PIN No.	Symbol	I/O	Function
6,7,8,9 10, 11 12, 13	D0 ~ D7	I	Bidirectional 3 state data bus used for transfer of command, data and status between RF5C59 and CPU. TTL compatible input.
36	$\overline{RESET}$	I	Reset input. Active LOW. During reset, • All internal registers turn to reset or default value. • Transmit outputs TXDA and TXDD turn to mark (HIGH) condition. • All transmit/receive ports are enabled. • $\overline{TXRDY}$ and $\overline{RXRDY}$ lines turn to active. (CMOS compatible Schumit input)
5	$\overline{CS}$	I	Chip select input. Active LOW. When $\overline{CS}$ is at LOW level, it allows data transfer with CPU. TTL compatible.
57	$\overline{WR}$	I	$\overline{WR}$ input. When $\overline{WR}$ is LOW and $\overline{CS}$ is LOW, the data on D0~D7 are written in this LSI. TTL compatible.
58	$\overline{RD}$	I	$\overline{RD}$ input. When $\overline{RD}$ is LOW and $\overline{CS}$ is LOW, the content of internal register of specified address is read on D0~D7. TTL compatible.
4	C/$\overline{D}$	I	C/$\overline{D}$ represents the input which informs whether the data on the bus is control information or status information. TTL compatible.
1,2,3	A2, A1 A0	I	Address input. TTL compatible.
56	$\overline{RXRDY}$	O	Interrupt signal to CPU which informs the receipt of data. If the data exist in any one of the receive ports being unmasked by RIM* flag of instruction register 1, it turns to LOW. When the data are read from all unmasked receive ports and each receive buffer has the space, it turns to HIGH. When RIM* flags are all turned to 1, it also turns to HIGH. Meanwhile, aparting from this signal, CPU is also able to confirm the existence of receive data by reading $\overline{RXRDY}$ bit of status register.
59	CLK	I	System clock input. CMOS compatible.
20 21 22 23	TXDA TXDB TXDC TXDD	O O O O	Transmit receive section of channel A~D serial data output. Following the start bit, it is output from LSB and after MSB, 1 bit of stop bits is added. During disable of port or during idle, it holds the "MARK" condition. With 'Mark' at HIGH level and 'Space' at LOW level, it performs Enable/Disable of coordinate ports with bit 7 and bit 3 of instruction register 4 and 5.
15 16 17 18	RXDA RXDB RXDC RXDD	I I I I	Receive section of channel A~D serial data input. Receive from LSB. 'Mark' is HIGH and 'Space' is LOW. It performs Enable/Disable of coordinate ports with bit 7 and bit 3 of instruction register 4 and 5.
29 34, 37	Vcc Vcc		+5V power supply. Make sure 29 Pin is connected with power supply.
14 19, 60	GND GND		
55	$\overline{TXRDY}$	O	Interrupt signal to CPU which informs that the data are transmissible. If any one of the transmit ports unmasked by TIM* flag of instruction register 1 is in transmissible condition, LOW output. (NOR output of TXRDY flag of each port) When TXRDY flags of all ports are masked, it turns to HIGH. Meanwhile, aparting from this signal, CPU is also able to confirm the condition of transmit register buffer by reading TXRDY* flag of status register 1.
28	TX 24	O	1/24 frequency division output of CLK input.
54 53 52 51 50 49 48 47 45 44 43 42 41 40 39 38	$\overline{DIVAEN}$ DVRA2 DVRA1 $\overline{DVRA0}$ $\overline{DIVBEN}$ DVRB2 DVRB1 $\overline{DVRB0}$ $\overline{DIVCEN}$ DVRC2 DVRC1 $\overline{DVRC0}$ $\overline{DIVDEN}$ DVRD2 DVRD1 DVRD0	I I I I I I I I I I I I I I I I	Preset input by hardware of transfer rate. When $\overline{DIV*EN}$ is LOW, transfer rate of coordinate port is decided by input condition of DVR*2, DVR*1 and DVR*0. When $\overline{DIV*EN}$ is HIGH, transfer rate is decided by the data written in instruction register 4 and 5. All pull-up Schumit input. When CLK input is 14.7454 MHz, the transmit rates are:

DVR*2	DVR*1	DVR*0	Frequency division ratio (vs. CLK/24)	Transmit rate
L	L	L	1	614.4 KHz
L	L	H	1/2	307.2
L	H	L	1/4	153.6
L	H	H	1/8	76.8
H	L	L	1/16	38.4
H	L	H	1/32	19.2
H	H	L	1/64	9.6
H	H	H	1/128	4.8

27 26 25 24	TXCA TXCB TXCC TXCD	O O O O	Transfer clock output during transmit of each port. Transmit data are output in synchronizing with the rise of this clock.
33 32 31 30	RXCA RXCB RXCC RXCD	O O O O	Transfer clock output during receive of each port. Frame synchronization is taken in synchronizing with the rise of start bit.
35	TEST	I	It turns to test mode at HIGH active. 1/24 frequency division circuit of CLK is bypassed under the test mode. Normally, it is kept LOW.

■ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Test condition	Value	Unit
V_{CC}	Supply voltage	GND = 0 V	−0.3 ~ 7	V
V_I	Input voltage		−0.3 ~ Vcc +0.3	V
V_O	Output voltage		−0.3 ~ Vcc +0.3	V
Pd	Power consumption		200	mW
Topg	Operating ambient temperature		0 ~ 70	℃
Tstg	Storage ambient temperature		−40 ~ 125	℃

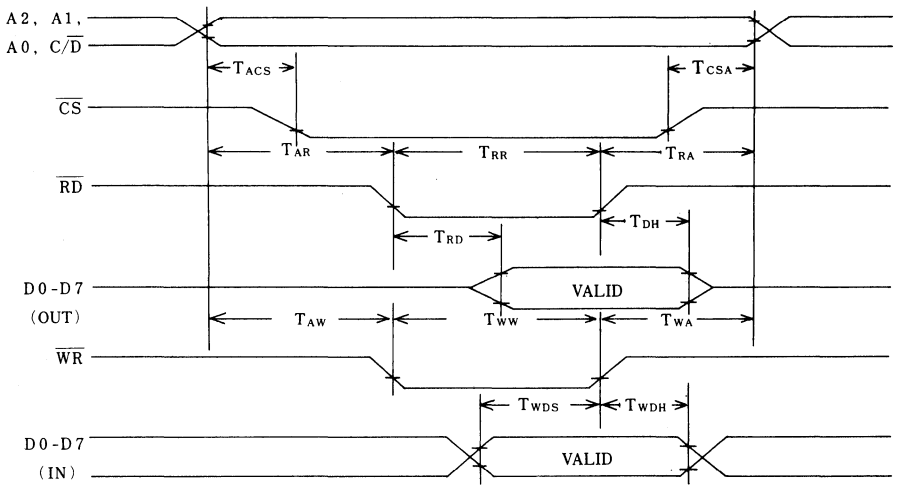
■ DC CHARACTERISTICS (Ta = 0 ~ 70℃, Vcc = 5 V ± 10%)

Symbol	Parameter	Test condition	Value			Unit
			MIN.	TYP.	MAX.	
V_{IH}	"H" input voltage (TTL)		2.2		Vcc +0.3	V
V_{IL}	"L" input voltage (TTL)		−0.3		0.8	V
V_{IH2}	"H" input voltage (CMOS)		Vcc × 0.7		Vcc +0.3	V
V_{IL2}	"L" input voltage (CMOS)		−0.3		Vcc × 0.3	V
V_{OH}	"H" output voltage	I_{OH} = −4mA	2.4			V
V_{OL}	"L" output voltage	I_{OL} = 4mA			0.4	V
I_{LI}	Input leakage current	0 ≦ VI ≦ Vcc			±10	μA
I_{LO}	Output leakage current	0 ≦ VO ≦ Vcc			±10	μA
V_T	Input rise threshold voltage				3.8	V
V_T	Input fall threshold voltage		1.3			V
I_{CC}	Supply current				20	mA

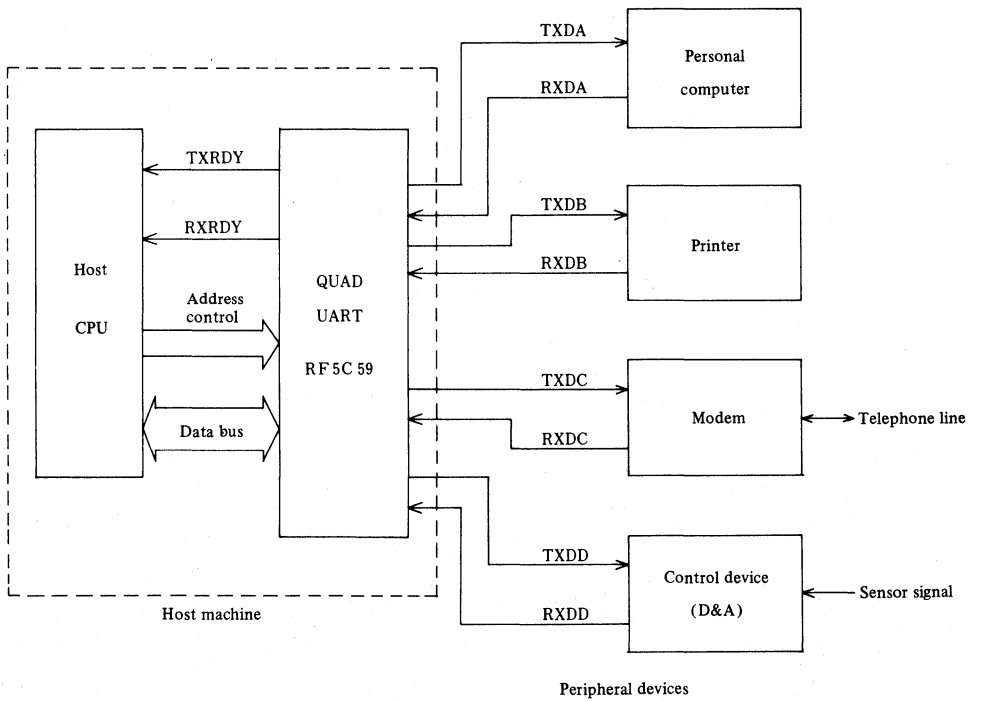
■ AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Value			Unit
			MIN.	TYP.	MAX.	
T_{WW}	$\overline{WR}$ pulse width		200			ns
T_{WDS}	$\overline{WR}$ data setup time		60			ns
T_{WDH}	$\overline{WR}$ data hold time		45			ns
T_{AW}	$\overline{WR}$ before rise ~ address setup time		50			ns
T_{WA}	$\overline{WR}$ after rise ~ address hold time		80			ns
T_{ACS}	$\overline{CS}$ after fall ~ address setup time		0			ns
T_{CSA}	$\overline{CS}$ before rise ~ address hold time		0			ns
T_{RR}	$\overline{RD}$ pulse width		200			ns
T_{RD}	$\overline{RD}$ data delay time	CL = 100pF			105	ns
T_{DH}	$\overline{RD}$ data hold time		10			ns
T_{AR}	$\overline{RD}$ before rise ~ address setup time		50			ns
T_{RA}	$\overline{RD}$ after rise ~ address hold time		80			ns

■ TIME CHART



■ EXAMPLE OF APPLICATION



■ REGISTER MAP

register	b7	b6	b5	b4	b3	b2	b1	b0
instr. 1	RIMA	RIMB	RIMC	RIMD	TIMA	TIMB	TIMC	TIMD
	L. P. A	L. P. B	L. P. C	L. P. D	L. P. A	L. P. B	L. P. C	L. P. D
	0 : non mask 1 : mask							
instr. 2	INIRER				ERSTA	ERSTB	ERSTC	ERSTD
	0 : NOP 1 : Initial Reset				0 : NOP 1 : Error Flag Reset			
instr. 3	LPAb1	LPAb0	LPBb1	LPBb0	LPCb1	LPCb0	LPDb1	LPDb0
	11 : physical port A 10 : physical port B 01 : physical port C 00 : physical port D							
instr. 4	ENLPA	ADIV2	ADIV1	ADIV0	ENLPB	BDIV2	BDIV1	BDIV0
	L. P. A	physical port A			L. P. B	physical port B		
	0 : DIS 1 : ENA	note 1			0 : DIS 1 : ENA	note 1		
instr. 5	ENLPC	CDIV2	CDIV1	CDIV0	ENLPD	DDIV2	DDIV1	DDIV0
	0 : DIS 1 : ENA	note 1			0 : DIS 1 : ENA	note 1		
stat. 1	RXRDYA	RXRDYB	RXRDYC	RXRDYD	TXRDYA	TXRDYB	TXRDYC	TXRDXD
	L. P. A	L. P. B	L. P. C	L. P. D	L. P. A	L. P. B	L. P. C	L. P. D
	0 : no receive data 1 : receive data in buffer				0 : transmit busy 1 : transmit ready			
stat. 2	FREA	FREB	FREC	FRED	OVEA	OVEB	OVED	OVEE
	L. P. A	L. P. B	L. P. C	L. P. D	L. P. A	L. P. B	L. P. C	L. P. D
	0 : no error 1 : framing error				0 : no error 1 : over run error			

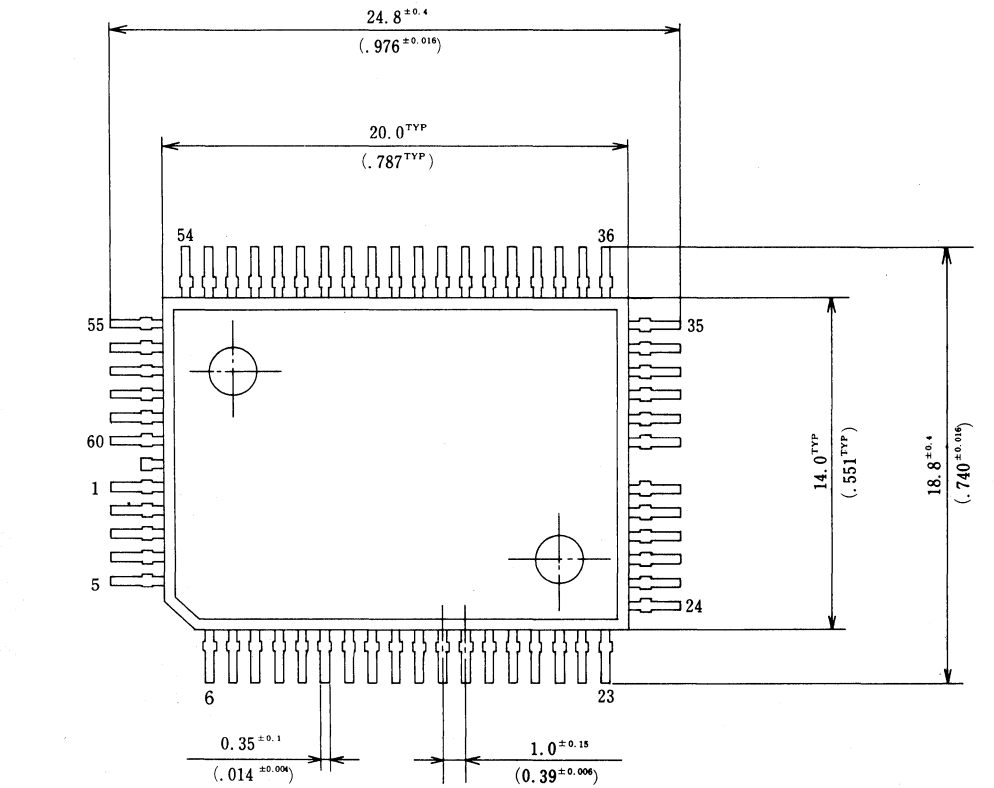
L. P. * : Logical Port *

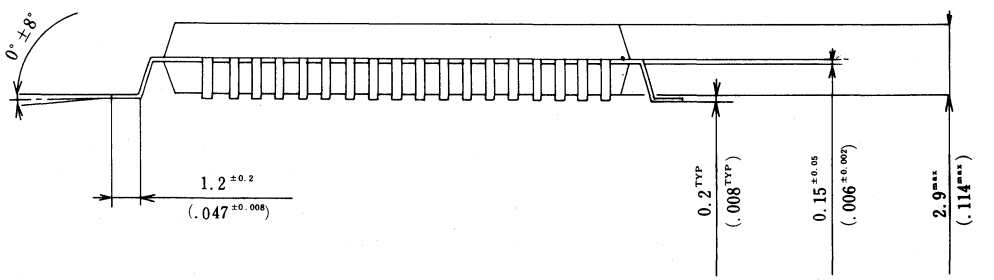
note 1 : 000 : 1/1, 001 : 1/2, 010 : 1/4, 011 : 1/8, 100 : 1/16, 101 : 1/32, 110 : 1/64, 111 : 1/128

■ ADDRESS ASSIGNMENT OF REGISTER

C/D	A 2	A 1	A 0	write register	read register
L	L	L	L	TXDA (Logical port)	RXDA (Logical port)
L	L	L	H	TXDB (Logical port)	RXDB (Logical port)
L	L	H	L	TXDC (Logical port)	RXDC (Logical port)
L	L	H	H	TXDD (Logical port)	RXDD (Logical port)
H	L	L	L	instruction register 1	instruction register 1
H	L	L	H	instruction register 2	instruction register 2
H	L	H	L	instruction register 3	instruction register 3
H	L	H	H	instruction register 4	instruction register 4
H	H	L	L	instruction register 5	instruction register 5
H	H	L	H		status register 1
H	H	H	L		status register 2

■ PACKAGE DIMENSIONS (60 pin FLAT)





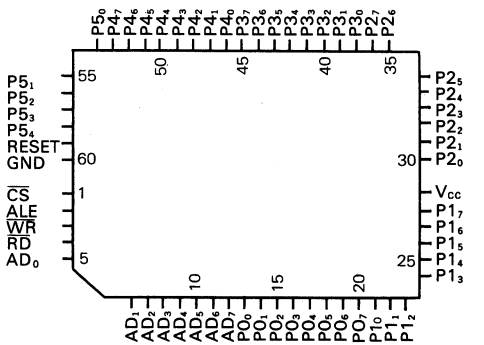
RF5C60

RF5C60 Parallel Input Output (PIO) LSI is designed to solve a wide range of peripheral control problems in the implementation of microcomputer systems. This device has five Input/Output ports of 8 bits and one Input/Output ports of 5 bits.

■ Features

- Six I/O ports (five parallel 8 bit ports and one parallel 5 bit port)
- Bidirectional I/O ports
- TTL I/O Level
- Low power CMOS silicon gate technology
- 5V single power supply
- 60 pin plastic Flat package

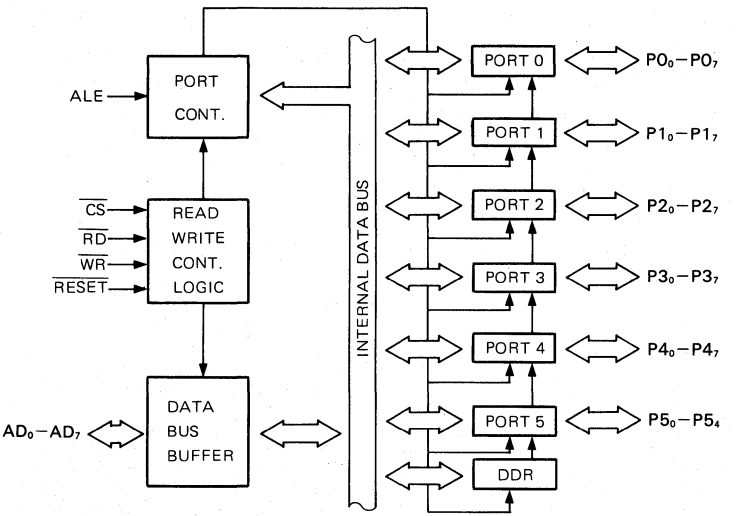
■ Pin Configuration



■ Pin Description

$\overline{CS}$	Chip Select	$AD_0 \sim AD_7$	Address/Data Bus
$\overline{RD}$	Read	$PO_0 \sim PO_7$	Port 0
$\overline{WR}$	Write	$P1_0 \sim P1_7$	Port 1
ALE	Address latch Enable	$P2_0 \sim P2_7$	Port 2
$\overline{RESET}$	Reset	$P3_0 \sim P3_7$	Port 3
Vcc	Power Supply	$P4_0 \sim P4_7$	Port 4
GND	Ground	$P5_0 \sim P5_4$	

■ Block Diagram



*** Addressing**

AD_2	AD_1	AD_0	select	AD_2	AD_1	AD_0	select
L	L	L	PORT 0	H	L	L	PORT 4
L	L	H	PORT 1	H	L	H	PORT 5
L	H	L	PORT 2	H	H	L	–
L	H	H	PORT 3	H	H	H	DDR

■ Absolute Maximum Ratings

Symbol	Parameter	Condition	Value	Unit
Vcc	Supply Voltage	GND = 0V	-0.3 ~ 7	V
VI	Input Voltage		-0.3 ~ Vcc + 0.3	V
Vo	Output Voltage		-0.3 ~ Vcc + 0.3	V
Pd	Power Consumption		200	mW
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-40 ~ 125	°C

■ DC Electrical Characteristics (Ta=0~70°C, Vcc=5V±10%)

Symbol	Parameter	Condition	MIN.	TYP.	MAX.	Unit	Note
V_{IH}	"H" Input Voltage		2.2		Vcc+0.3	V	Note 1
V_{IL}	"L" Input Voltage		-0.3		0.8	V	
VT^+	Input Rise Threshold Voltage		1.3	1.9	2.4	V	Note 2
VT^-	Input Fall Threshold Voltage		0.7	1.2	1.7	V	
TV^+-VT^-	Hysteresis Voltage		0.4	0.5		V	
V_{OH}	"H" Output Voltage	I_{OH}=-4mA	2.4			V	
V_{OL}	"L" Output Voltage	I_{OL}=4mA			0.4	V	
I_I	Input Leakage Current	$0 \leqq V_1 \leqq Vcc$	-10		10	μA	
I_{OZ}	Output Leakage Current (off)	$0V \leqq V_0 \leqq Vcc$	-10		10	μA	
I_{CC0}	Power Supply Current (operating)				30	mA	
I_{CC1}	Power Supply Current(standby)				200	μA	

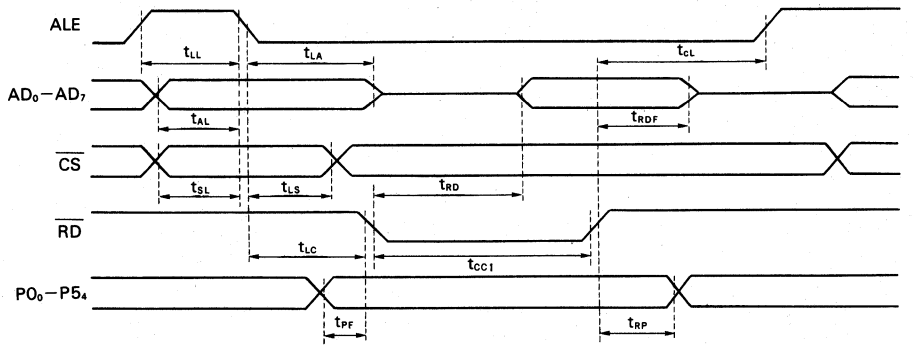
Note 1 : The values are for $\overline{CS}$, ALE, $\overline{RD}$, $\overline{WR}$ and AD_0~AD_7. Note 2 : The values are for $\overline{RESET}$ and $P0_0$~$P5_4$.

■ AC Electrical Characteristics (Ta=0~70°C, Vcc=5V±10%)

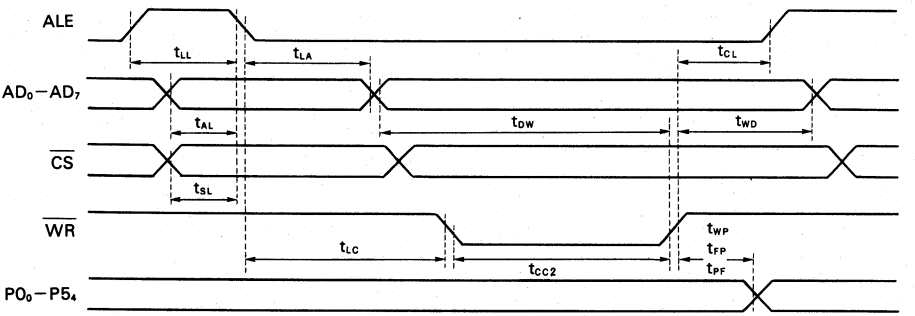
Symbol	Parameter	Condition	MIN.	TYP.	MAX.	Unit
t_{LL}	ALE Pulse Width		80			ns
t_{AL}	Address Setup Time (to ALE↓)		40			ns
t_{LA}	Address Hold Time (to ALE↓)		40			ns
t_{SL}	$\overline{CS}$ Setup Time (to ALE↓)		30			ns
t_{LS}	$\overline{CS}$ Hold Time (to ALE↓)		40			ns
t_{LC}	ALE↓$\overline{RD}$/$\overline{WR}$ Delay Time		30			ns
t_{CC1}	$\overline{RD}$ Pulse Width		160			ns
t_{CC2}	$\overline{WR}$ Pulse Width		120			ns
t_{CL}	$\overline{RD}$/$\overline{WR}$ ↑~ALE↑ Delay Time		25			ns
t_{RD}	$\overline{RD}$ ↓~Data Output Delay Time	CL=0~150pF	30		120	ns
t_{RDF}	$\overline{RD}$ ↑~Data Float Delay Time				80	ns
t_{PR}	Poat Input Setup Time		50			ns
t_{RP}	Port Input Hold Time		50			ns
t_{DW}	Data Input Setup Time		100			ns
t_{WD}	Data Input Hold Time		30			ns
t_{WP}	$\overline{WR}$ ↑ Port Output Delay Time	CL=150pF			300	ns
t_{FP}	$\overline{WR}$ ↑ Poat Output Mode Delay Time				400	ns
t_{PF}	$\overline{WR}$ ↑ Poat Input Mode Delay Time				400	ns

■ Timing Chart

READ CYCLE



WRITE CYCLE



PCM Sound Generator IC

RF5C68A

■ GENERAL DESCRIPTION

RF5C68A is a sound generator IC that uses pulse code modulation (PCM). It has a digital control oscillator (DCO) and digital control amplifier (DCA) built in. You can structure a PCM sound generator system by connecting external waveform data memories (pseudo SRAM, SRAM, or mask ROM) and D/A converters, controlling them with a microcomputer.

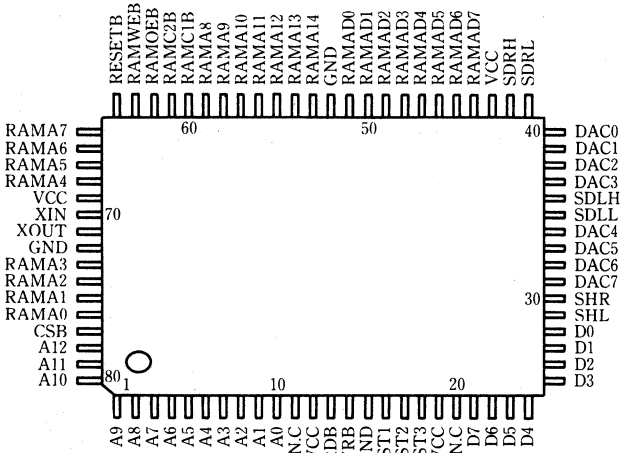
■ FEATURES

- PCM sound generation method
- Number of channels 8
- Source clock frequency . . . . . 10 MHz max.
- Sampling frequency . . . . . 19.8 kHz (source clock = 7.6 MHz)
- Waveform data width . . . . . 8 bits
- Number of waveform words . . . . . Any
- Waveform memory space . . . . . 64 K-bytes max.
- Envelope data width . . . . . 8 bits
- Left(L) and Right(R) stereo output at arbitrary orientation level
- Pitch fine adjustment
- Interface with 8-bit CPUs
- Interface with waveform memories
  Can be directly coupled with two 256K (32K × 8) pseudo SRAMs.
  Can be directly coupled with two 256K (32K × 8) mask ROMs.
  Can be directly coupled with two 256K (32K × 8) SRAMs.
- Interface with D/A converters
  Can be directly coupled with 10-bit serial D/A converters.
  Can be directly coupled with 8-bit parallel D/A converters.
- Silicon gate CMOS process
- 5V single power supply
- Package . . . . . 80-pin flat package.

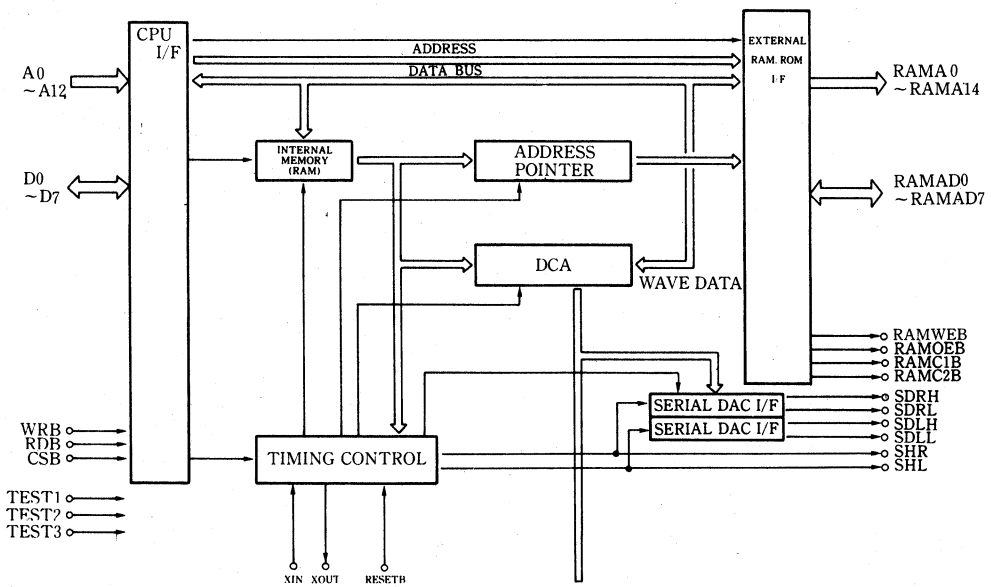
■ APPLICATIONS

Sound generator for personal computers, electronic instruments, TV games, and toys.

■ PIN CONFIGURATION (Top View)



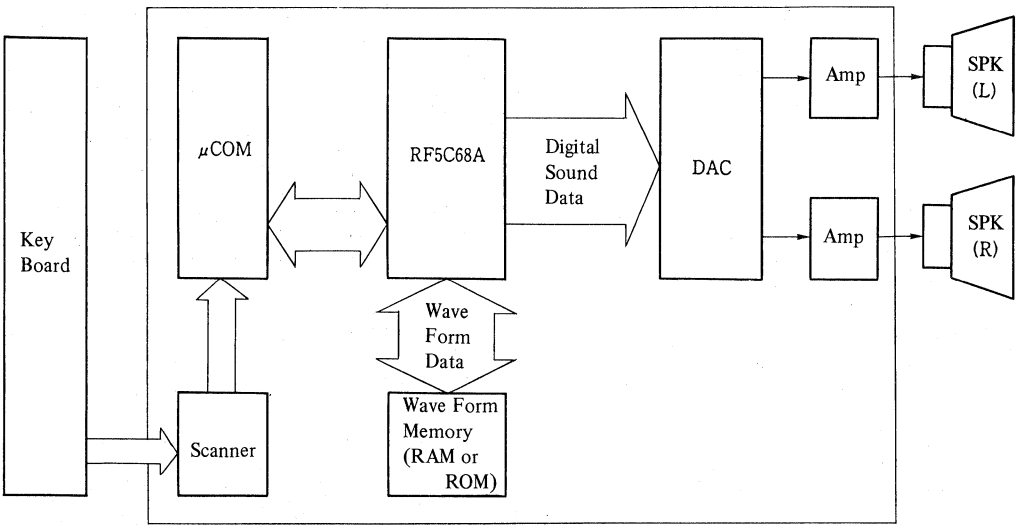
■ BLOCK DIAGRAM



■ PIN DESCRIPTION

PIN NAME	FUNCTION	I/O	DESCRIPTION
A0 ~ A12	Address input	I	Address signals input from a microcomputer .
D0 ~ D17	Data input output	I/O	Data bus signals between RF5C68A and a microcomputer
CSB	Chip select input	I	Chip select signals input from a microcomputer
RDB	Read enable input	I	Read signals input from a microcomputer
WRB	Write enable input	I	Write signals input from a microcomputer
RAMAD0 ~ RAMAD7	RAM address input output	I/O	When pseudo SRAMs are connected, these are multiplex signals of lower addresses/data between RF5C68A and SRAMs. When MROMs are connected, these are data input signals from MROMs. When SRAMs are connected, these are data bus signals between RF5C68A and SRAMs.
RAMA8 ~ RAMA14	RAM address output	O	Higher address signals of SRAM and MROM
RAMA0 ~ RAMA7	RAM address output	O	Lower address signals of SRAM and MROM
RAMC2B	Memory select output	O	SRAM and MROM select signals of higher 32 K-bytes
RAMC1B	Memory select output	O	SRAM and MROM select signals of lower 32 K-bytes
RAMWEB	RAM write enable output	O	Write signals of pseudo SRAM and SRAM
RAMOEB	Memory output enable output	O	Read signals of pseudo SRAM, SRAM, and MROM
SDLH	Higher "L" data output	O	Higher "L" data signals output to serial DACs
SDLL	Lower "L" data output	O	Lower "L" data signals output to serial DACs
SDRH	Higher "R" data output	O	Higher "R" data signals output to serial DACs
SDRL	Lower "R" data output	O	Lower "R" data signals output to serial DACs
DAC0 ~ DAC7	Multiplex signal output	O	"R" data/"L" data multiplex signals output to parallel DACs
SHL	"L" data sample/hold signals output	O	"L" data sample/hold signals of DAC0 to DAC7
SHR	"R" data sample/hold signals output	O	"R" data sample/hold signals of DAC0 to DAC7
RESETB	Reset signals input	I	Reset signals
XIN	Crystal signals input	I	External terminal of crystal oscillator Clock can be directly input to XIN.
XOUT	Crystal signals output	O	
TEST 1 TEST 2 TEST 3	Test input pin	I	These are test inputs usually set to logic "L". When MROM or SRAM is used for memory, TEST2 is set to logic "H".
VCC	Power supply	–	Power supply terminal
GND	Ground	–	Grounding terminal

■ APPLICATION EXAMPLE



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
Vcc	Supply voltage	GND = 0V	−0.3 ~ 7	V
VTE	Input and Output Voltage	GND = 0V	−0.3 ~ Vcc + 0.3	V
Pd	Maximum Power consumption		200	mW
Topr	Operating Ambient Temperature		0 ~ 70	°C
Tstg	Storage Temperature		−40 ~ 125	°C

■ RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Specified Value			Unit
		Min	Typ.	Max.	
Vcc	Supply Voltage	4.5		5.5	V
VIH	Input High Voltage	2.2		Vcc + 0.3	V
VIL	Input Low Voltage	−0.3		0.8	V
Ta	Ambient Temperature	0		70	°C

■ DC CHARACTERISTICS

(Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min.	Typ.	Max.	
V_{IH1}	Input High Voltage (TTL Compatible)		2.0		Vcc + 0.3	V
V_{IL1}	Input Low Voltage (TTL Compatible)		−0.3		0.8	V
V_{IH2}	Input High Voltage (XIN pin)		3.5		Vcc + 0.3	V
V_{IL2}	Input Low Voltage (XIN pin)		−0.3		1.5	V
I_{LI}	Input Leakage Current	$0v \leqq V_{IN} \leqq Vcc$	−10		10	μA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA			0.4	V
I_{OZ}	Output Leakage Current for OFF State	$0v \leqq V_{OUT} \leqq Vcc$	−10		10	μA
I_{CCO}	Standby Supply Current	V_{IN} = 0V, Vcc			300	μA
I_{CC1}	Operating Supply Current	f_{OPR} = 10 MHz			30	mA

■ AC CHARACTERISTICS

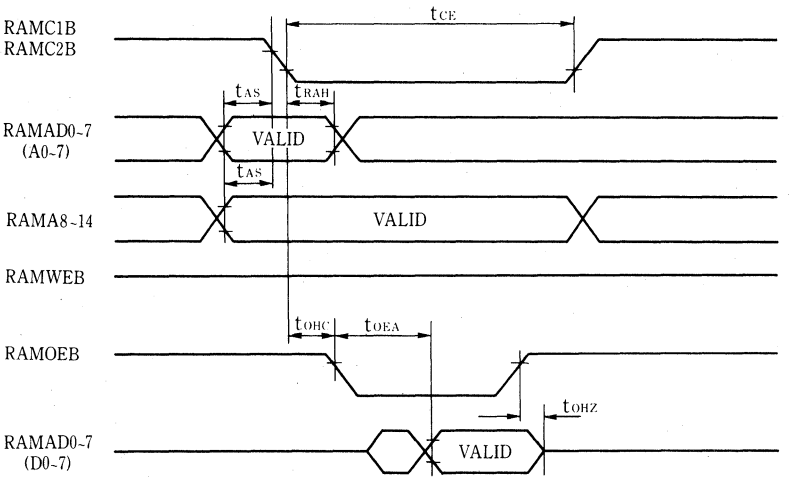
(Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min.	Typ.	Max.	
f_{OPR}	Input Clock Frequency				10	MHz
T_{CE}	RAMCE 1, 2 Pulse Width		200			ns
T_{AS}	Address to RAMCE 1, 2		0			ns
T_{RAH}	RAMCE 1, 2 to Row Address		30			ns
T_{OHC}	RAMCE 1, 2 to RAMOEB		0			ns
T_{OEA}	RAMOEB to Read Data Valid				50	ns
T_{OHZ}	RAMOEB to Read Data Float		20			ns
T_{CW}	RAMCE 1, 2 to RAMWEB High		200			ns
T_{WP}	RAMWEB Pulse Width		35			ns
T_{DW}	Write-Data Valid to RAMWEB High		30			ns
T_{DH}	Write-Data Hold after RAMWEB High		0			ns
T_{RDA}	Read-Data Valid to RDB High				100	ns
T_{RDH}	Read-Data Hold after RDB High		10			ns
T_{WRH}	Write-Data Valid to WRB High		30			ns
T_{WRH}	Write-Data Hold after WRD High		30			ns

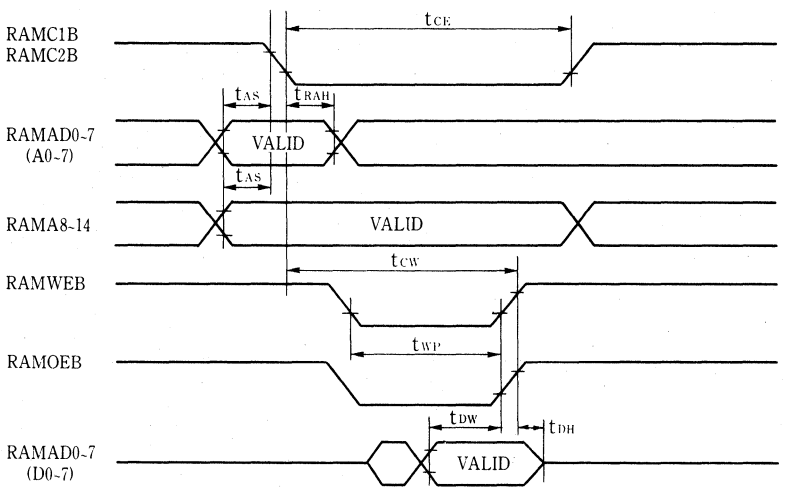
■ TIMING CHART

1. Psendo SRAM Interface

* Read Cycle

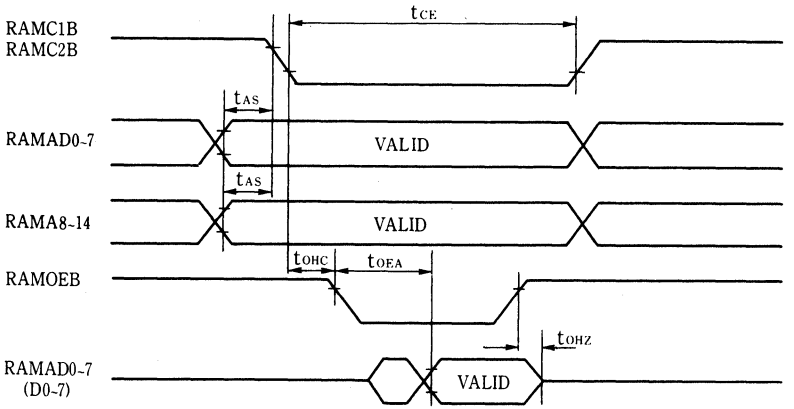


* Write Cycle



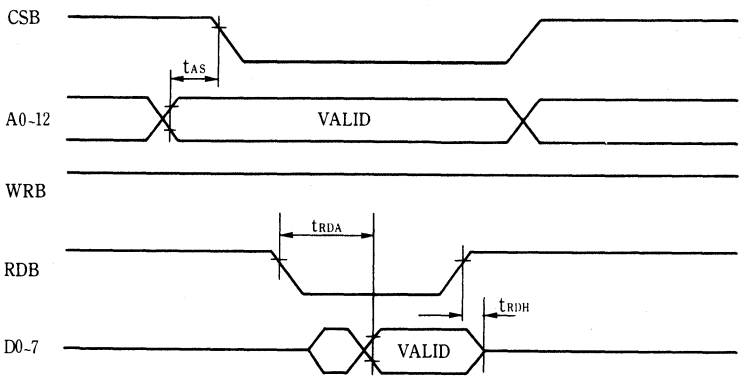
2. Mask ROM Interface

* Read Cycle

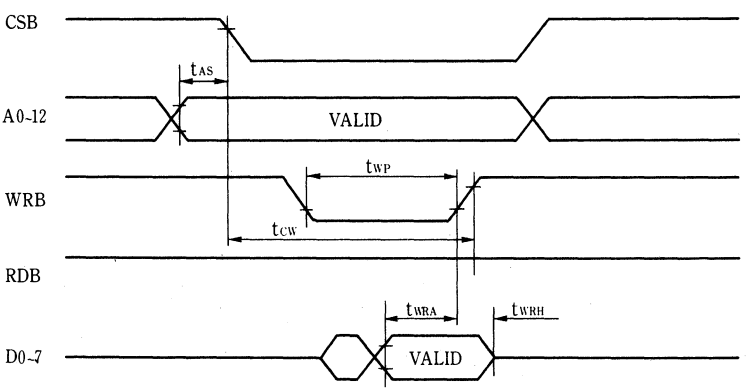


3. CPU Interface

* Read Cycle



* Write Cycle



■ FUNCTIONS

1. PCM Sound Generation

Waveform data (WAVE DATA) is specified by the internal address pointer of RF5C68A, and is read from external waveform memories. RF5C68A multiplies it with envelope data (ENV DATA) or stereo pan pot data (PAN DATA) that are stored in the internal memory (RAM). The operation above is performed for each of the eight channels. RF5C68A outputs the total of the results as single-sample PCM sound data (digital data).

RF5C68A performs the operation even to the channel that is not sounding. Therefore, one sampling requires a fixed time (one cycle of source clock × 384).

However, the operation result of the channel that is not sounding does not affect the output PCM sound data.

The digital control amplifier (DCA) block, which executes the above processing, is described below.

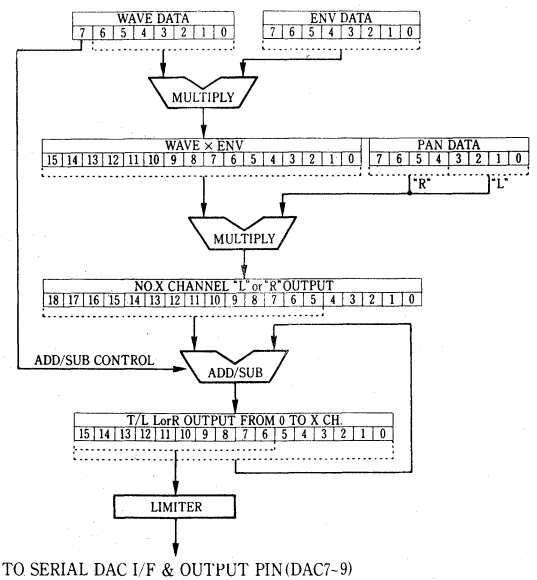
[DCA block]

The digital control amplifier block generates musical tones using the data read from internal and external memories.

The figure below shows how each type of data is processed.

The above processing is performed sequentially for each of the channels 1 to 8. Every time the R and L outputs of the eight channels are totaled, sample/hold signals for R and L are generated.

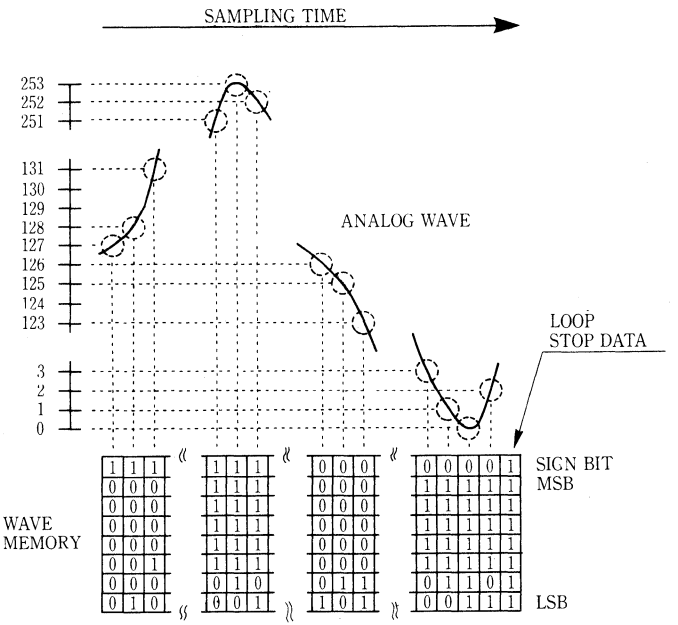
If there is a plus side overflow while totaling the values of the eight channels, the limiter circuit sets FFFFH as the result. If there is a minus side overflow, the limiter sets 0000H as the result.



[Example of waveform data format]

The figure below shows an example format of waveform data to be stored in an external waveform memory. In this example, digital sampling is performed assuming that the values of the analog waveform are 127 at the center, 253 at maximum, and 0 at minimum.

The 'FFH' waveform data is handled as loop stop data (therefore, 'FFH' cannot be used as waveform data). If 'FFH' data is read from the waveform memory, the waveform memory read address is reset to the LSH and LSL data (see 2. Wave Form Memory Read), and waveform data is read again.



2. Wave Form Memory Read

RF5C68A has an address pointer that specifies addresses of a 64K-byte waveform memory independently for eight channels, according to start address data (ST data), loop start address data (LSH data, LSL data), and address count data (FDH data, FDL data) that are stored in the internal memory, and loop stop data that is stored in the waveform memory.

The address pointer fixes the waveform memory read address of a channel that is not sounding to the ST data of that channel. Therefore, in the first sampling cycle after the channel has started sounding, music tones are always read from the waveform memory specified by the ST data.

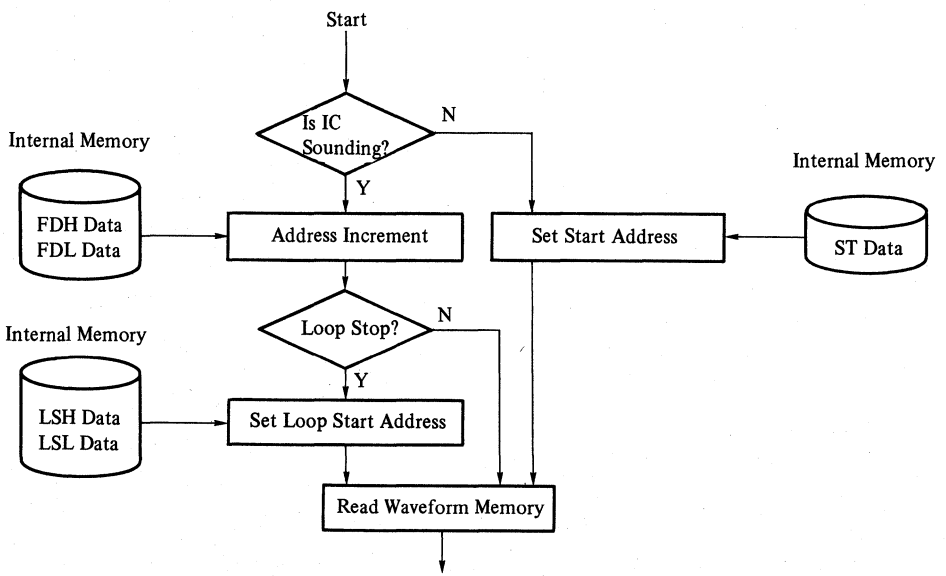
Waveform memories are read after the waveform memory address which has been sampled previously by the sounding channel is incremented according to FDH and FDL data of that channel.

The waveform memory is read after its address which has been smapled previously by the sounding channel is incremented according to FDH and FDL data of that channel. Therefore, the music tone data stored in the waveform memory can be set to any frequency.

If the loop stop data (FFH) stored in the waveform memory is read, waveform memory read address is set to the LSH and LSL data, and the waveform memory is read again. Therefore, any part of music tone data stored in the waveform memory can sound repeatedly.

[Address pointer function]

The address pointer controls addresses of 11 digits below the decimal point, for fine-adjusting the integer address to specify addresses of the 64K-byte waveform memory and the music tone frequency. The flow-chart below shows the processing executed independently for each of the eight channels.



[Example of music tone data frequency setting]

Examples of FDH and FDL setting are shown below.

[Number of timbre data words: 256 words
Source clock frequency: 10 MHz]

Timbre name	FD set value		Frequency responding to the FD set value (Hz)	Voice	FD set value		Frequency responding to the FD set value (Hz)
	FDH	FDL			FDH	FDL	
C_1	02	92	32.68	C_4	14	93	261.61
C_1	02	B9	34.62	C_4	15	D4	277.56
D_1	02	E3	36.71	D_4	17	18	293.65
D_1	03	0E	38.84	D_4	18	77	311.09
E_1	03	3D	41.18	E_4	19	EC	329.61
F_1	03	6E	43.61	F_4	1B	76	349.18
F_1	03	A3	46.24	F_4	1D	18	369.95
G_1	03	DA	48.98	G_4	1E	D4	392.00
G_1	04	15	51.91	G_4	20	A9	415.30
A_1	04	53	54.99	A_4	22	9A	439.98
A_1	04	95	58.26	A_4	24	A9	466.16
B_1	04	DA	61.69	B_4	26	D7	493.87
C_2	05	24	65.37	C_5	29	26	523.23
C_2	05	72	69.24	C_5	2B	98	554.32
D_2	05	C5	73.36	D_5	2E	30	587.30
D_2	06	1D	77.73	D_5	30	EF	622.22
E_2	06	7A	82.35	E_5	33	D8	659.23
F_2	06	DD	87.27	F_5	36	ED	698.42
F_2	07	46	92.49	F_5	3A	31	739.94
G_2	07	B5	98.00	G_5	3D	A7	783.95
G_2	08	2A	103.81	G_5	41	52	830.59
A_2	08	A6	109.97	A_5	45	34	879.96
A_2	09	2A	116.53	A_5	49	52	932.32
B_2	09	B5	123.43	B_5	4D	AE	987.75
C_3	0A	49	130.78	C_6	52	4C	1046.5
C_3	0A	E6	138.58	C_6	57	31	1108.7
D_3	0B	8C	146.83	D_6	5C	61	1174.7
D_3	0C	3B	155.52	D_6	61	DF	1244.5
E_3	0C	F6	164.81	E_6	67	B0	1318.5
F_3	0D	BB	174.59	F_6	6D	D3	1396.5
F_3	0E	8C	184.97	F_6	74	64	1480.0
G_3	0F	6A	196.00	G_6	7B	50	1568.0
G_3	10	54	207.62	G_6	82	A4	1661.2
A_3	11	4D	219.99	A_6	8A	69	1760.0
A_3	12	54	233.05	A_6	92	A5	1864.7
B_3	13	6B	246.91	B_6	9B	60	1975.7
				C_7	A4	99	2093.0

3. Internal Data Setting

(1) Address map

There is an 8K byte address space inside that can be accessed from a microcomputer. The table below shows the address map.

[Address]	[Content]
1FFFH 1000H	Waveform data Waveform data memory is accessed via this IC. 4K byte can be directly accessed. Using the bank function in the control Reg enables access to up to 64K byte.
0FFFH 0009H	Not used
0008H	Channel ON/OFF Reg
0007H	Control Reg
0006H	*ST data memory
0005H	*LSH data memory
0004H	*LSL data memory
0003H	*FDH data memory
0002H	*FDL data memory
0001H	*PAN data memory
0000H	*ENV data memory

* : Items marked with * must be set independently for each channel by the bank function in the control Reg.

(2) Control Reg

This register sets modes of this IC, waveform memory bank addresses, and internal memory bank channels.

This is a write-only register.

7	6	5	4	3	2	1	0	Bit
ON OFF	MOD	–	–	*WB3	WB2	WB1	WB0	Address
				–	CB2	CB1	CB0	0007H

*WB: Wave bank

Bit 7: ON/OFF

This IC starts sounding when this bit is set and stops sounding when this bit is reset. External waveform memories of a microcomputer can be read only when the IC is not sounding. When the IC is sounding, writing to the external waveform memories is restricted as described later.

Bit 6: MOD

This bit controls to which register the content of bits 3 to 0 is written.

The microcomputer writes the content of bits 2 to 0 to CBs 2 to 0 when this bit is "H", and writes the content of bits 3 to 0 to WBs 3 to 0 when this bit is "L"

When MOD = 'H'

Bits 2 to 0: CBs* 2 to 0

These bits control selection of channels when the microcomputer accesses internal memories (ENV, PAN, FDL, FDH, LSL, LSH, and ST).

*CB: Channel Bank

CB 2	CB 1	CB 0	Channel NO.
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

When MOD = 'L'

Bits 3 to 0: WBs 3 to 0

These bits control higher addresses when the micro computer accesses external waveform memories.

The table below shows the relation between set values of WBs 3 to 0 and the addresses for accessing external waveform memories.

WB 3	WB 2	WB 1	WB 0	External waveform memory address	
				Memory No.	Address
0	0	0	0	1	0000H~0FFFH
0	0	0	1	1	1000H~1FFFH
0	0	1	0	1	2000H~2FFFH
0	0	1	1	1	3000H~3FFFH
0	1	0	0	1	4000H~4FFFH
0	1	0	1	1	5000H~5FFFH
0	1	1	0	1	6000H~6FFFH
0	1	1	1	1	7000H~7FFFH
1	0	0	0	2	0000H~0FFFH
1	0	0	1	2	1000H~1FFFH
1	0	1	0	2	2000H~2FFFH
1	0	1	1	2	3000H~3FFFH
1	1	0	0	2	4000H~4FFFH
1	1	0	1	2	5000H~5FFFH
1	1	1	0	2	6000H~6FFFH
1	1	1	1	2	7000H~7FFFH

Note: Memory No. 1 is selected by RAMC1B.
Memory No. 2 is selected by RAMC2B.

(3) Internal memory

This internal memory stores data for sounding, which will be described later, for each of the eight channels.

a. ST data ..... (Address = 0006H)
For the address of the waveform memory read of a channel that starts sounding, the higher eight bits are the ST data that responds to the channel. 'OOH' is set to the lower address.

b. LSH data ..... (Address = 0005H)
When the stop data is read from the waveform memory while the IC is sounding, its lower address is converted into LSH data, and the waveform memory is read again.

c. LSL data ..... (Address = 0004H)
When the stop data is read from the waveform memory while the IC is sounding, its lower address is converted into LSL data, and the waveform memory is read again.

d. FDH data ..... (Address = 0003H)
This data controls the address counter that indicates the address to be read from the waveform memory while the IC is sounding.

Setting arbitrary bits of FDH enables address increment of one sampling time as shown in the table below.

FDH bit	Address increment
7	2^4
6	2^3
5	2^2
4	2^1
3	2^0
2	2^{-1}
1	2^{-2}
0	2^{-3}

Example: When only bits 4 and 3 of FDH are set, the address is incremented by $2^1 + 2^0 = 3$ counts in one sampling.

e. FDL data ..... (Address = 0002H)
This data controls the address counter that indicates the address to be read from the waveform memory while the IC is sounding.

Setting arbitrary bits of FDL enables address increment of one sampling time as shown on the next page.

FDL bit	Address increment
7	2^{-4}
6	2^{-5}
5	2^{-6}
4	2^{-7}
3	2^{-8}
2	2^{-9}
1	2^{-10}
0	2^{-11}

Example: When only bits 4 and 3 of FDL are set, the address is incremented by $2^{-7} + 2^{-8}$ counts in one sampling.

f. PAN data ..... (Address = 0001H)

This data controls the separation of output generated from the sounding channel into 'L' and 'R' stereo outputs.

The higher four bits of PAN data are the coefficient of the 'R' output, and the lower four bits are that of the 'L' output.

7	6	5	4	3	2	1	0	Bit
MSB			LSB	MSB			LSB	Address
Coefficient of the 'R' output				Coefficient of the 'L' output				0001H

g. ENV data ..... (Address = 0001H)

To vary the amplitude of the waveform data read from the waveform memory by the sounding channel, this data multiplies it with the ENV data.

Bit 7 is MSB, and bit 0 is LSB.

(4) Channel ON/OFF Reg

This register controls start/stop of sounding for each channel.
However, the control by the control register is given priority, and this register is valid when the control register sets the sounding state.

Bit 0 responds to channel 1, and bit 7 responds to channel 8.

4. Interface with Peripheral Devices

(1) Microcomputer interface

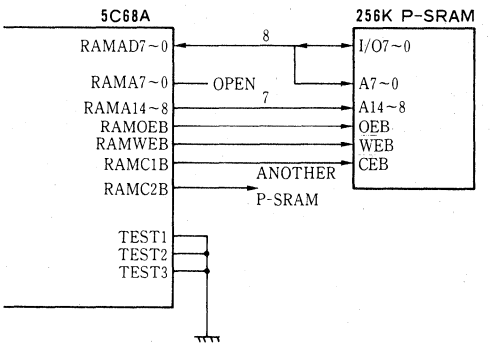
This IC can be used as a peripheral device of an 8-bit CPU.

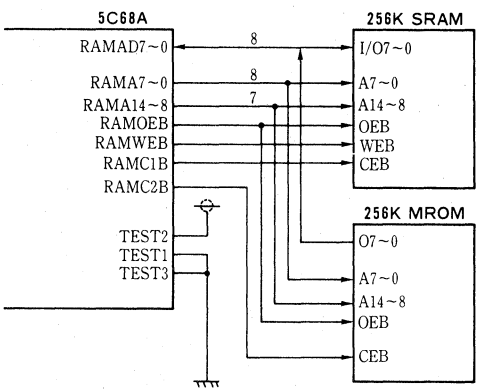
The control Reg's setting of sounding/not sounding states changes the conditions of the access from the microcomputer to this IC. See the table below.

Condition	External waveform memory		Internal memory	
	Read	Write	Read	Write
Sounding	Impossible	Access by cycles more than the 16 cycles of the source clock.	Impossible	Possible
Stopping	Possible	Possible	Impossible	Possible

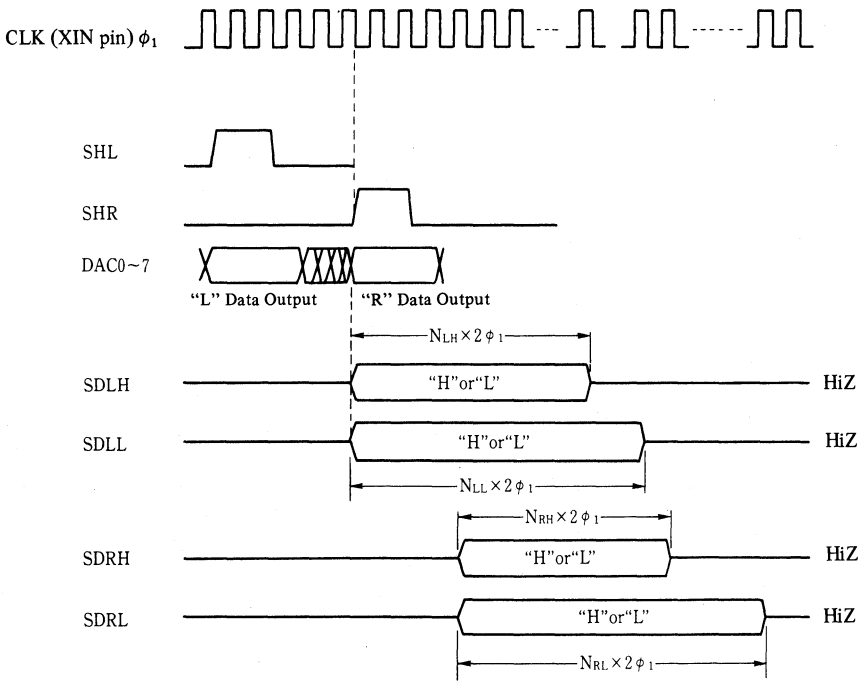
(2) Waveform memory interface

This IC externally connects pseudo SRAMs, SRAMs, or MROMs as waveform memories. Examples are shown in the figure below.





(3) RF5C68A outputs PCM sounds in digital values, and must have an external D/A converter connected. The output timing chart is shown below.

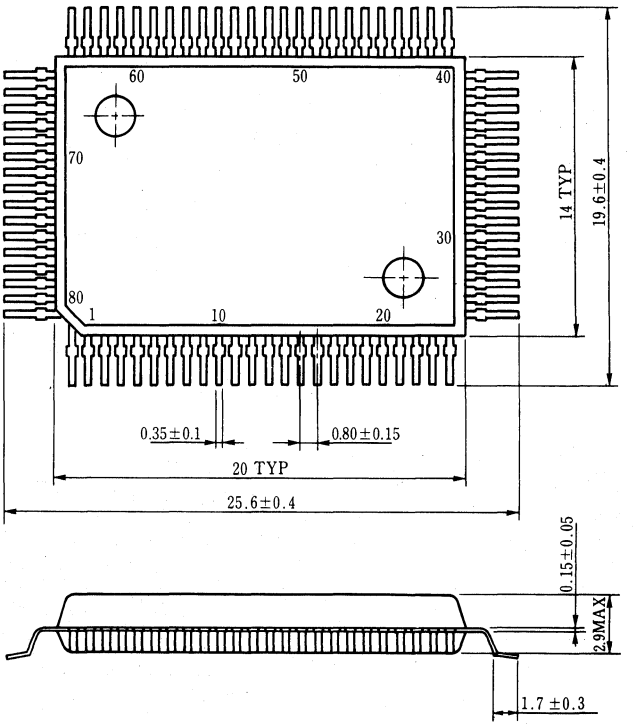


However, NLH, NLL, NRH, and NRL are the number of bits of the absolute value of the difference of the previous sound data. If it is larger than the previous data, the output value is "H", and if it is smaller, the output value is "L"

[Example]

	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	← Previous sound data (10 bits)
−	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	
	c_9	c_8	c_7	c_6	c_5	c_4	c_3	c_2	c_1	c_0	← Absolute value of the sound data difference
	NLH or NRH					NLL or NRL					

■ PACKAGE DIMENSION



Unit: mm

PWM GENERATOR

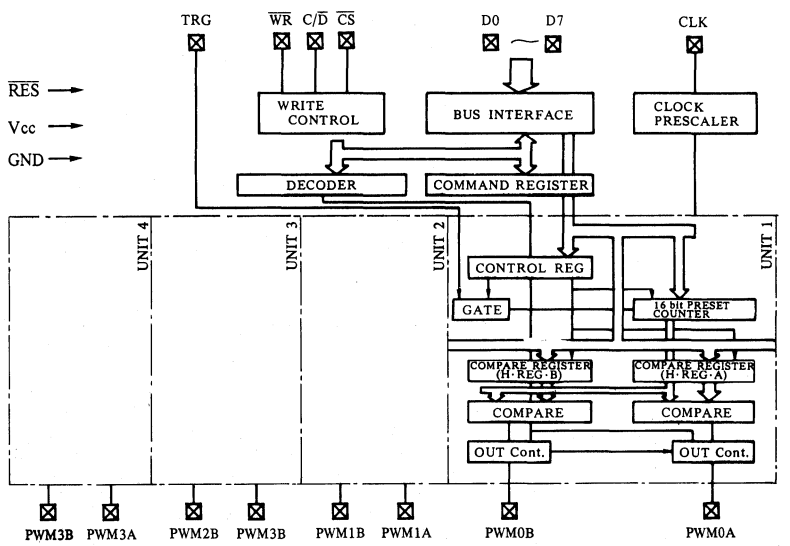
RF5C86

Ricoh's RF5C86 is an integrated circuit (IC) for generating pulse width modulation (PWM) signals. It has eight output channels. The pulse cycle, pulse high width, and output mode can be set. The RF5C86 is ideal for servo control of motor lamps and actuators. If the multiplier (MPL) mode is set, it operates as an analog multiplier, so it can be used as four electronic volumes.

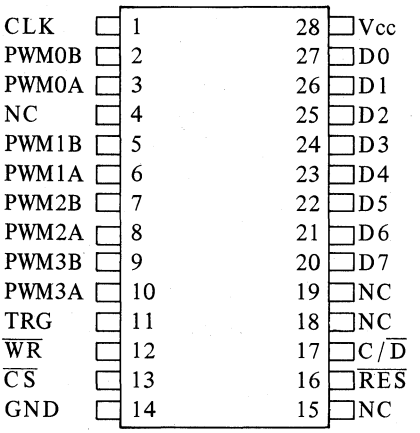
■ FEATURES

- Three types of mode for various purposes (modes may also be mixed)
  PWM mode: The period value can be set for every two channels. It can be used as a PWM generator for up to eight channels.
  The pulse high width can be set for all eight channels.
  One-shot mode: Outputs a one-shot pulse using an external TRG signal.
  MPL mode: Can be used as an analog multiplier and as up to four electronic volumes.
- Built-in prescaler: One of $f_{CLK}/2$, $f_{CLK}/8$, $f_{CLK}/32$, or $f_{CLK}/128$ can be chosen for each channel (f_{CLK} = 16 MHz maximum).
- The external trigger can be selected (common in all channels).
- The output polarity can be selected (PWM mode only).
- The register values can be changed after completion of the current cycle.
- Direct link to CPU bus
- 5 V single power supply
- CMOS process
- 28-pin SOP package

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin No.	Name	I / O	Function
1	CLK	I	Clock input
2	PWM0B	I / O	PWM mode: PWM signal output, MPL mode: Vref input
3	PWM0A	O	PWM signal output
4	NC		No connection
5	PWM1B	I / O	PWM mode: PWM signal output, MPL mode: Vref input
6	PWM1A	O	PWM signal output
7	PWM2B	I / O	PWM mode: PWM signal output, MPL mode: Vref input
8	PWM2A	O	PWM signal output
9	PWM3B	I / O	PWM mode: PWM signal output, MPL mode: Vref input
10	PWM3A	O	PWM signal output
11	TRG	I	External trigger input, active high edge
12	$\overline{WR}$	I	Write signal input
13	$\overline{CS}$	I	Chip select signal input
14	GND		Ground
15	NC		No connection
16	$\overline{RES}$	I	Internal register or counter reset signal input
17	C / $\overline{D}$	I	Selection of command input/data input
18	NC		No connection
19	NC		No connection
20 ~ 27	D0 ~ D7	I	Data input
28	Vcc		Power supply

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
Vcc	Supply Voltage		-0.5~+7.0	V
V_I	Input Voltage		-0.5~Vcc+0.3	V
Vo	Output Voltage		-0.5~Vcc+0.3	V
Topr	Operating Ambient Temperature		0~70	°C
Tstg	Storage Temperature		-40~125	°C

■ DC CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V±10%)

Symbol	Parameter	Condition	Specified Value			Unit
			MIN	TYP	MAX	
V_{IH}	Input High Voltage		2.2		Vcc+0.3	V
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
I_{LI}	Input Leakage Current	V_I = 0, Vcc CLK, $\overline{CS}$, $\overline{WR}$, C/$\overline{D}$, GATE Data bus	-10		10	μA
$I_{LI(1)}$		$\overline{RESET}$ V_I = 0	-300		10	μA
Icc1	Supply Current	16 MHz Operations			30	mA
Icc2		Input : 0 or Vcc Output : OPEN			10	μA
R_{ON}	Input Resistance	Analog Switch			100	Ω
V_{AI}	Input Analog Voltage		2.0		Vcc+0.3	V
V_{AO}	Output Analog Voltage		V_{AI-}		V_{AO+}	V

Note : Input Pull-Up Pin

■ TERMINAL CAPACITANCE (Ta = 25°C, Vcc = 0V)

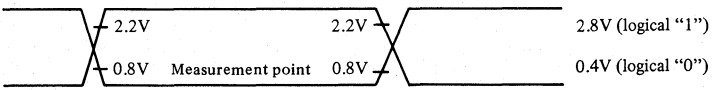
Symbol	Parameter	Condition	Specified Value			Unit
			MIN	TYP	MAX	
C_I	Input Capacitance	f_{CLK} = 1 MHz			10	pF
C_O	Output Capacitance	0 V except at pins to be measured			20	pF

■ AC CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V±10%)

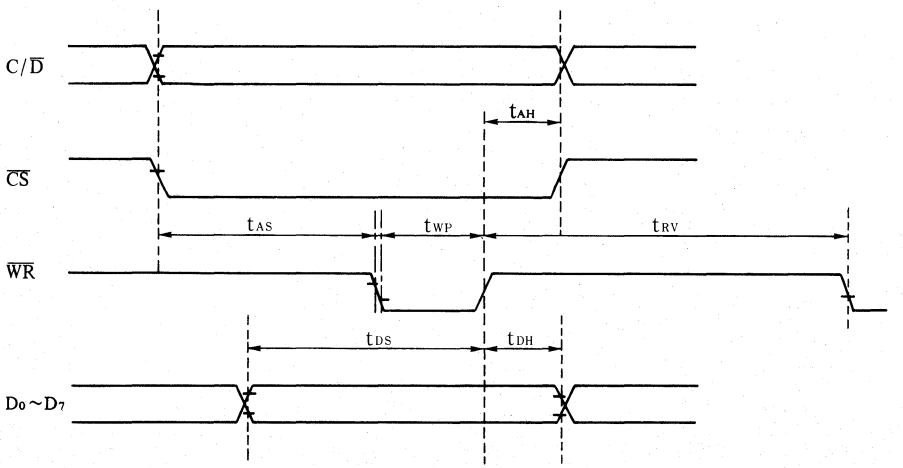
① Bus timing

Symbol	Item	Condition	Specified Value			Unit
			MIN	TYP	MAX	
t_{WP}	WR pulse width		80			ns
t_{AS}	C/$\overline{D}$ and $\overline{CS}$ setup time		30			ns
t_{AH}	C/$\overline{D}$ and $\overline{CS}$ hold time		10			ns
t_{DS}	Data setup time		60			ns
t_{DH}	Data hold time		20			ns
t_{RV}	Write recovery time		$\frac{1}{f} \times 2$			S

AC test input waveform



TIMING CHART

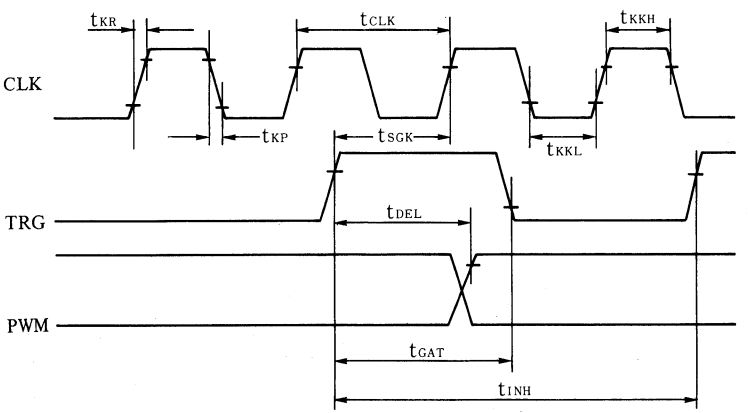


② Clock and trigger timing

Symbol	Item	Specified Value			Unit
		MIN	TYP	MAX	
t_{CLK}	Clock cycle	62.5		DC	ns
t_{KKH}	Clock pulse width H	30			ns
t_{KKL}	Clock pulse width L	30			ns
t_{KR}, t_{KP}	Close rise and fall time			15	ns
t_{SGK}	Trigger setup time	30			ns
t_{GAT}	Trigger effective time	30			ns
t_{DEL}	Output delay time after trigger input			1	sel
t_{INH}	Retrigger input inhibition time	2			sel

Note : sel means one cycle of clock selected in each mode

Clock and trigger timing chart

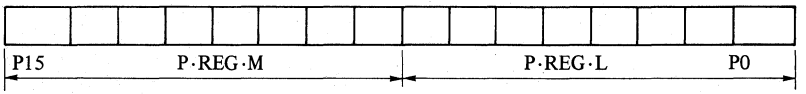


■ FUNCTIONS

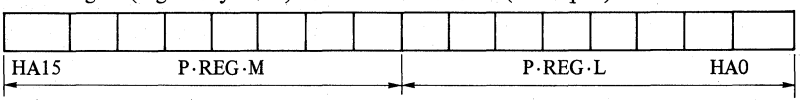
(1) Register ($C/\overline{D} = 0$)

This IC includes four P·REG, H·REG·A, H·REG·B 16-bit registers, and four C·REG 8-bit registers. Write is enabled after a desired register is set by a command.

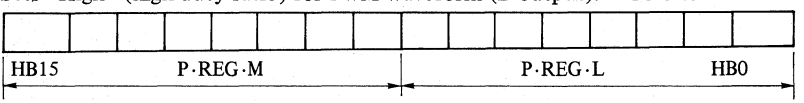
- P·REG ..... Sets the PWM waveform cycle (same at A and B output). 16 bits × 4



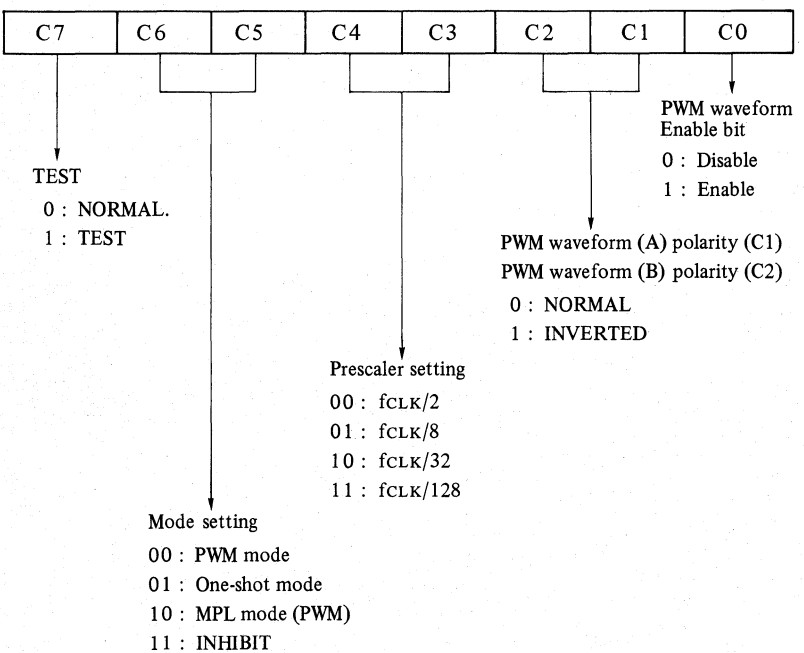
- H·REG·A ..... Sets "High" (high duty ratio) for PWM waveform (A output). 16 bits × 4



- H·REG·B ..... Sets "High" (high duty ratio) for PWM waveform (B output). 16 bits × 4



- C·REG ..... Sets the mode for each channel. 8 bits × 4



Explanation of C register bits

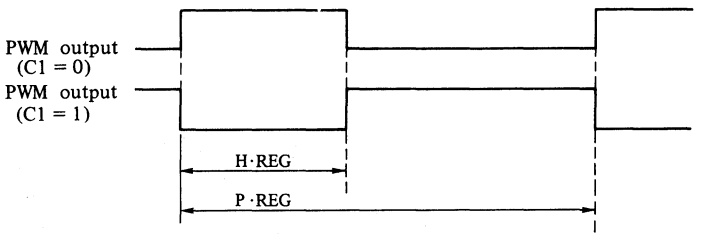
- Bit 0 (C0) : Enable bit for each channel function (counter)

  When this bit is set to 1, the internal counter is enabled and the waveform selected from the control register is output. When this bit is set to 0, the PWM counter is disabled and the PWM output is set to low. The registers are not affected. This bit is set to 0 by external reset.

- Bit 1 (C1) : PWM waveform (A) polarity

  When this bit is set to 1, the polarity of the PWM waveform (A) is inverted. The H·REG value specifies "Low".

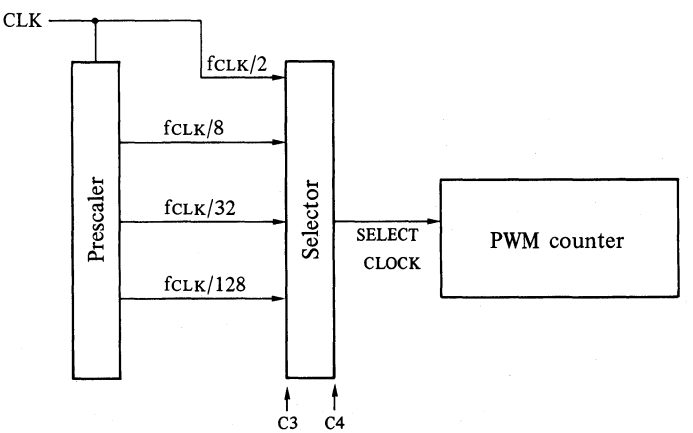
  When bit 0 (C0) is set to 0 while Bit 1 (C1) is 1, the PWM output pin is set to High. This bit is 0 at reset.



- Bit 2 (C2) : PWM waveform (B) polarity

  When this bit is set to 1, the polarity of the PWM waveform (B) is inverted.
  The function is the same as that of Bit 1.

- Bits 3 and 4 (C3 and C4) : Prescaler setting



Bits 3 and 4 set the PWM counter clock input. $f_{CLK}/2$ is set at reset.

bit 4	bit 3	PWM counter clock
0	0	$f_{CLK}/2$
0	1	$f_{CLK}/8$
1	0	$f_{CLK}/32$
1	1	$f_{CLK}/128$

- Bits 5 and 6 (C5 and C6) : Mode setting

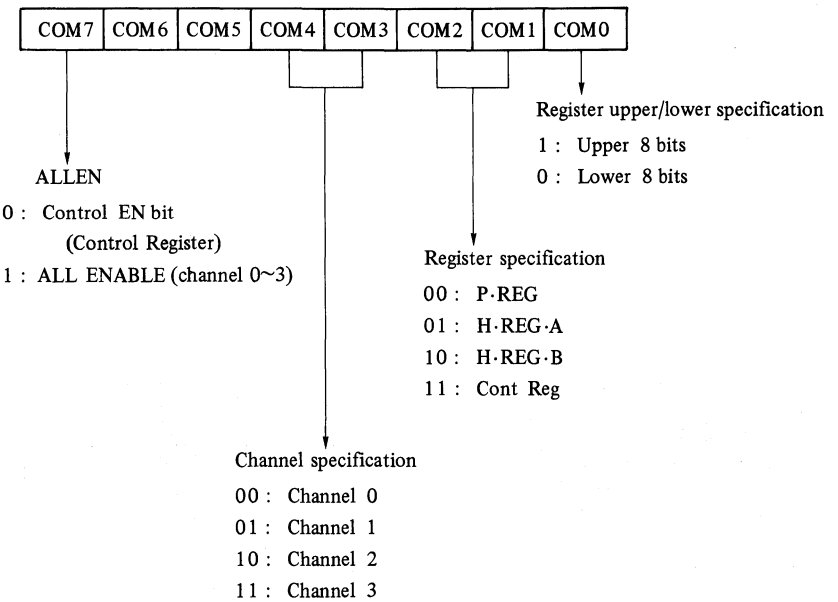
  Bits 5 and 6 select the mode for each channel. The PWM mode is selected at reset.

bit 6	bit 5	Mode
0	0	PWM mode
0	1	One-shot mode
1	0	MPL mode (PWM)
1	1	INHIBIT

See (3) for explanation of the modes.

(2) Command ($C/\overline{D} = 1$)

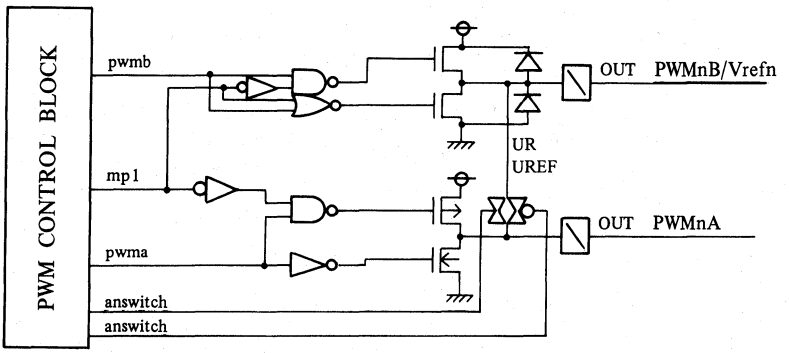
This 6-bit register specifies which register within RF5C86 is to be selected. Write is enabled by setting the $C/\overline{D}$ pin to High.



Notes:

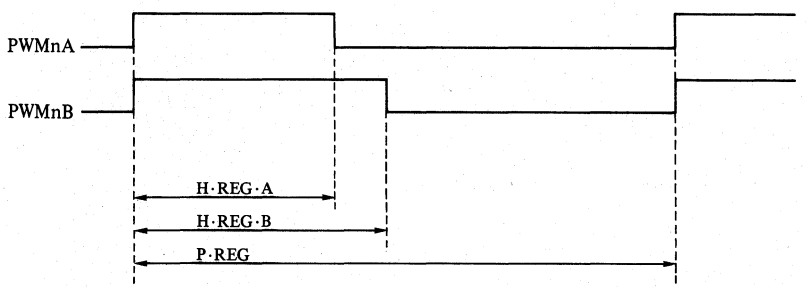
- When COM7 (ALLEN bit) is set to 1, the PWM output is enabled regardless of the PWM waveform Enable bit. In other words, when the ALLEN bit is 1, the status of the Enable bit of the data register does not affect the PWM output.
- When data is written to H·REG·A, H·REG·B, or P·REG, write to the upper 8 bits first, then to the lower 8 bits.
- Inhibit the condition of P·REG=H·REG·A or P·REG=H·REG·B.

(3) Explanation of modes



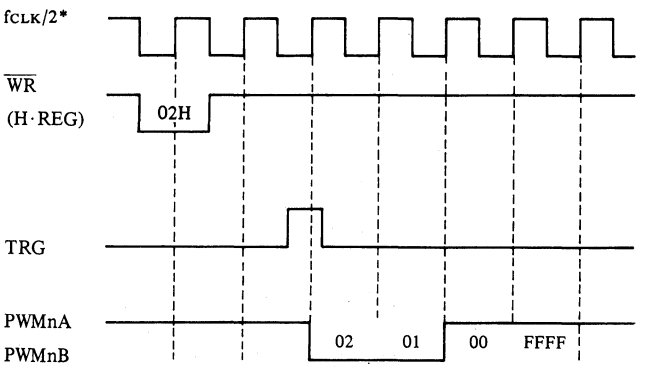
① PWM mode

In the PWM mode, the A output buffer and the B output buffer are both active, and the analog switch is off. Two PWM waveforms with different duty ratios are output from the two output terminals. To reset the cycle pulse width, reloading from the registers (double registers) to the PWM counter and compare latch is performed after the completion of the PWM cycle, so this reloading is effective from the next cycle of the PWM output waveform.



② One-shot mode

A low-level, one-shot pulse with the specified length is output.
Retrigger is enabled by TRG input.
The operation in the previous block diagram is equal to that in the PWM mode.



The one-shot pulse length is set at H·REG·A and B, so it is possible to output a one-shot waveform to A output and B output independently. The clock input selection from the PWM counter is the same.

In this mode, the H·REG value is latched from the register to the compare latch by a TRG signal.

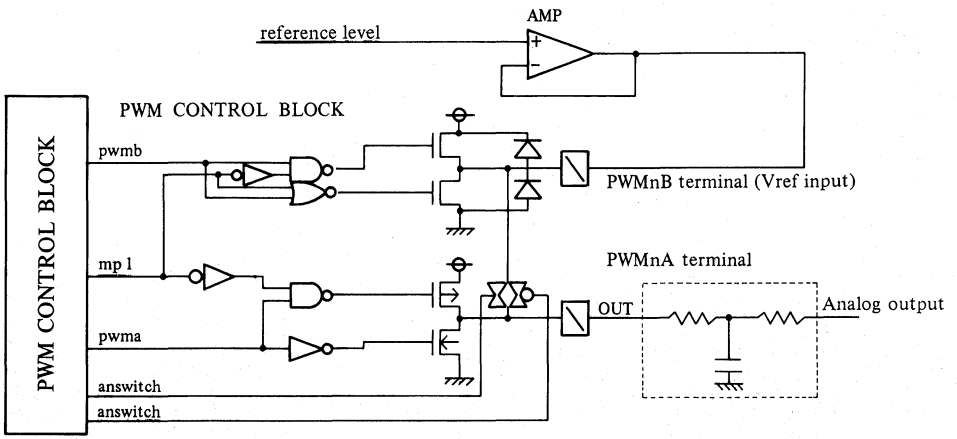
Note: Can be selected from fCLK/2, fCLK/8, fCLK/32 or fCLK/128.

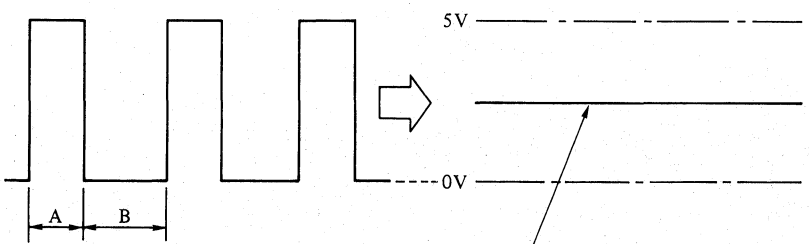
③ MPL mode

In the MPL mode, the B output buffer is in tri-state, the A output buffer is in OPEN drain, and the analog switch is on. Analog input to the PWMnB terminal enables an analog multiplier.

An example of the configuration of a simple-type electronic volume is given below.

An operation amplifier is provided externally and Vref is input to the PWMnB terminal through the amplifier. A low pass filter is connected to the PWMnA terminal. Then the analog output can be obtained by the formula given below.





PWMnA output

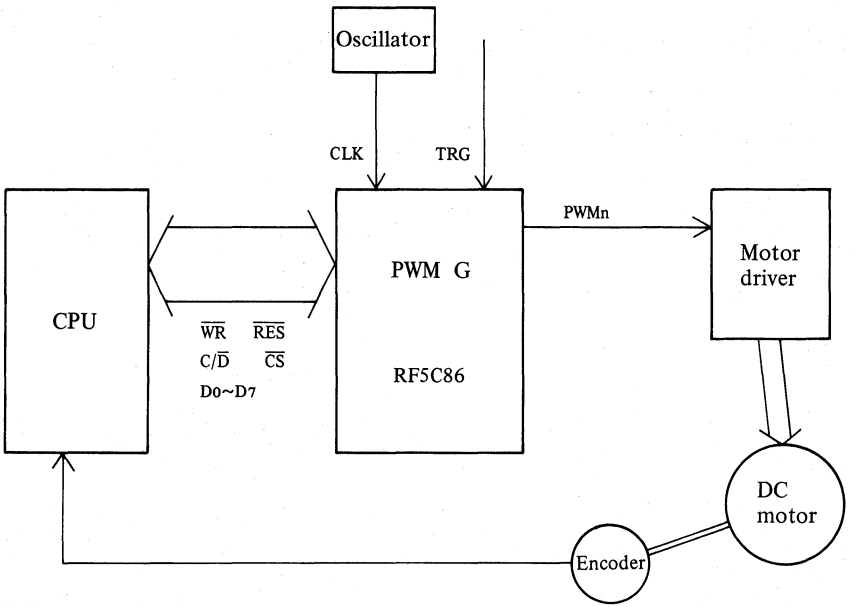
Analog output = Vref × $\frac{A}{A+B}$

(4) Control signals

An $\overline{RES}$, $\overline{CS}$, $\overline{WR}$, or C/$\overline{D}$ control signal is input to this IC for various control operations. The truth values are given below.

$\overline{RES}$	$\overline{CS}$	$\overline{WR}$	C/$\overline{D}$	Contents
1	0	0	1	Command write
1	0	0	0	Data write
1	1	X	X	Device non-selection
0	X	X	X	Reset (The PWM output is set to Low at reset.)

■ CONNECTION EXAMPLE



■ APPLICATION EXAMPLES

☆ DC motor control

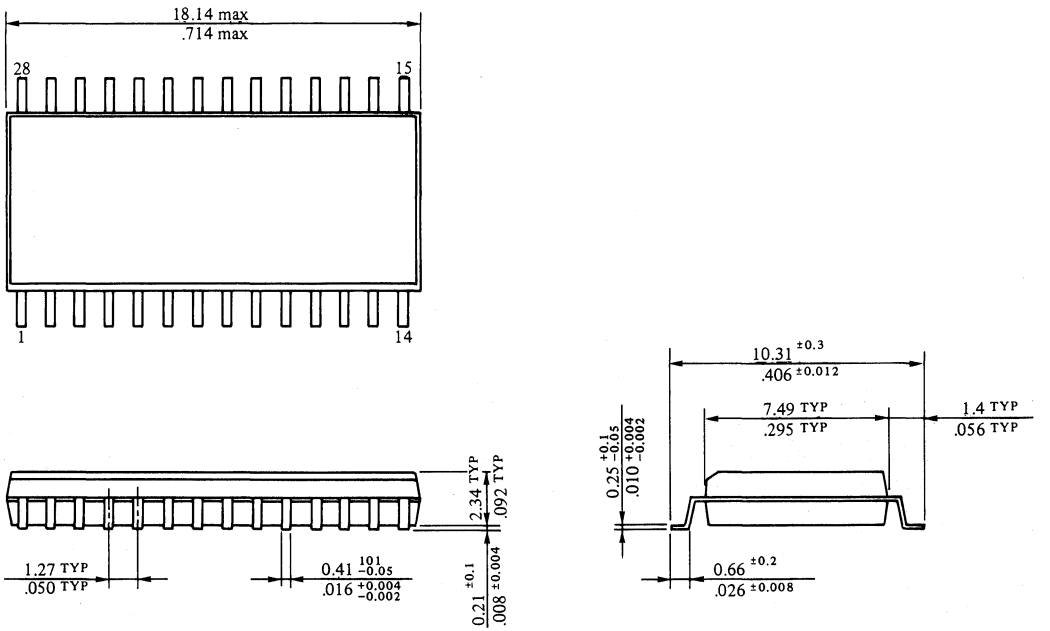
(wire dot printer, laser printer, LED printer, copier, printer)

☆ Electronic volume

(TV set, stereo set)

■ PACKAGE DIMENSION (mm/inch)

28 pin SOP



2-Dimension Filter

RF5C67

The RF5C67 is a Filter IC that performs 5x5 elements two-dimension filtering. There are two methods of data input available: serial mode, that enters one data item for each line in the main scanning direction; and odd-even mode, that enters two data items (odd and even) for each line. (Two RF5C67 are needed for the odd-even mode.)

Operation speed is 20 MHz, enabling fast image processing: 50 ns/element in serial mode and 25 ns/element in odd-even mode.

Input element data is a 6-bit absolute value, and the filter coefficient is signed 7-bit absolute two's compliment.

As shown in Fig-1, the filter coefficient must be symmetric to the central scanning line that includes the processing element or must have the opposite sign.

W_{11}	W_{12}	W_{13}	$\pm W_{12}$	$\pm W_{11}$
W_{21}	W_{22}	W_{23}	$\pm W_{22}$	$\pm W_{21}$
W_{31}	W_{32}	W_{33}	$\pm W_{32}$	$\pm W_{31}$
W_{41}	W_{42}	W_{43}	$\pm W_{42}$	$\pm W_{41}$
W_{51}	W_{52}	W_{53}	$\pm W_{52}$	$\pm W_{51}$

Filter Coefficient of the RF5C67

Writing various filter coefficients to the RF5C67 from the host CPU enables space filtering of various characteristics.

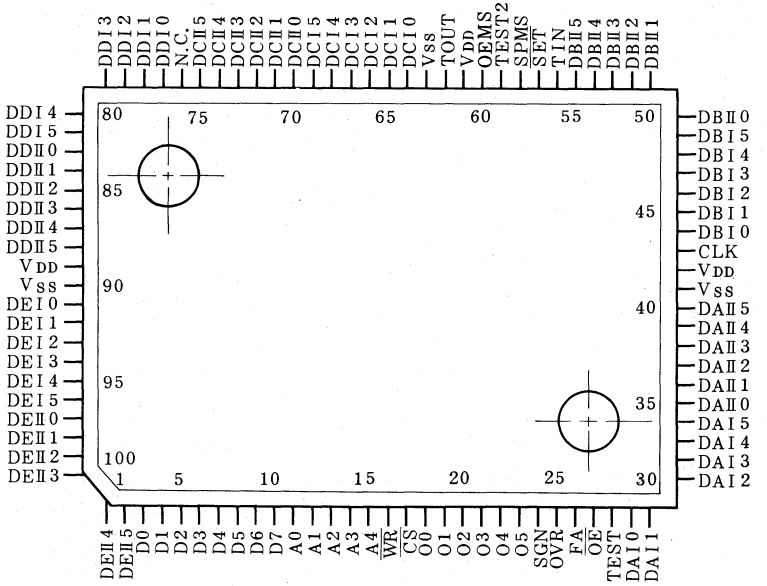
■ Features

- 5 x 5 elements two-dimension filter
- Operation speed 40 MHz max. (two ICs) ..... odd/even mode
  20 MHz max. (one IC) ..... serial mode
- Filter coefficient: 7 bits (signed binary)
- Image data: 6 bits (absolute values)
- Overflow/underflow terminal
- Image element output enable terminals
- 8-bit and 16-bit CPU interface (coefficient setting)
- Silicon gate CMOS process
- 5V single power supply
- 100-pin flat package

■ Applications

Digital copiers, CT scanners, radars, and other devices

■ Pin Configuration

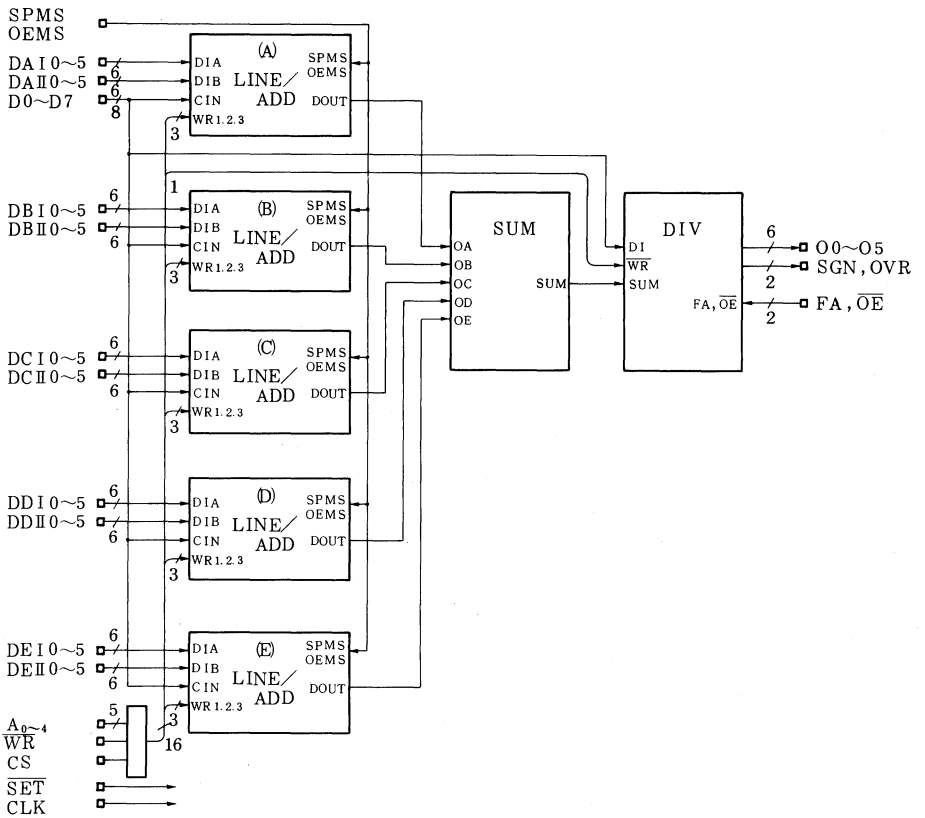


■ Pin Description

Pin name	I/O	Description
VDD	—	Power supply
VSS	—	Power supply
CLK	I	Element clock. Element data is input, processed and output in synchronization with the rising edge of this clock.
DAI0 ~ 5	I	Element data input of the first line
DBI0 ~ 5	I	Element data input of the second line
DCI0 ~ 5	I	Element data input of the third line
DDI0 ~ 5	I	Element data input of the fourth line
DEI0 ~ 5	I	Element data input of the fifth line
DAII0 ~ 5	I	Element data input of the first line
DBII0 ~ 5	I	Element data input of the second line
DCII0 ~ 5	I	Element data input of the third line
DDII0 ~ 5	I	Element data input of the fourth line
DEII0 ~ 5	I	Element data input of the fifth line
00 ~ 5	O	Element output data
D0 ~ 7	I	Data input to internal coefficient register
$\overline{WR}$	I	Write pulse input to internal coefficient register
A0 ~ 4	I	Select signal input of internal coefficient register
FA	I	Format adjustment input "H": Negative values become absolute. "L": Negative values are rounded to 0.
$\overline{CS}$	I	Chip select input in host interfacing
OE	I	Element output enable "H": D000 to 5 and D0E0 to 5, SGN, and OVR become high impedance.
SGN	O	Outputs the sign before format adjustment. "H": Negative value "L": Positive value
OVR	O	"H": Overflow or underflow in format adjustment
SPMS	I	Select signal of serial and odd-even mode SPMS = "H": serial mode SPMS = "L": odd-even mode

OEMS	I	In odd-even mode Selects odd or even output. In odd output (OEMS = "L") Odd data is input to DAI to DEI and even data is input to DAII to DEII. In even output (OEMS = "H") Even data is input to DAI to DEI and odd data is input to DAII to DEII.
$\overline{SET}$	I	Reset signal of multiplication coefficient Setting this signal L makes $W_{33} = 1$, $W_{11} = W_{12} = W_{13} = \cdots\cdots = W_{55} = 0$ Division coefficient 1 is set, and data before processing can be output.
TIN	I	Test terminal
TOUT	O	Test terminal
TEST1	I	Test terminal
TEST2	I	Test terminal

■ Block Diagram



■ Description of Block

- LINE ADD
  Multiplies and adds five data items (A to E) in the main scanning direction and the preset filter coefficient for each line.

- SUM
  Adds the results of LINE ADD operation of all main scanning lines. Operation results are expressed by 13-bit integer two's compliment.

- DIV/FA
  Divides the final results of the addition, and rounds down the results.

■ Absolute Maximum Ratings

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply Voltage	GND = 0V	−0.3 ~ 7	V
VTE	Terminal Voltage	GND = 0V	−0.3 ~ VCC +0.3	V
Pd	Power Consumption		700	mW
Topr	Operating Ambient Temperature		0 ~ 70	°C
Tstg	Storage Temperature		−40 ~ 125	°C

■ DC Electrical Characteristics

(Ta = 0 ~ 70°C, VCC = 5V ± 10%)

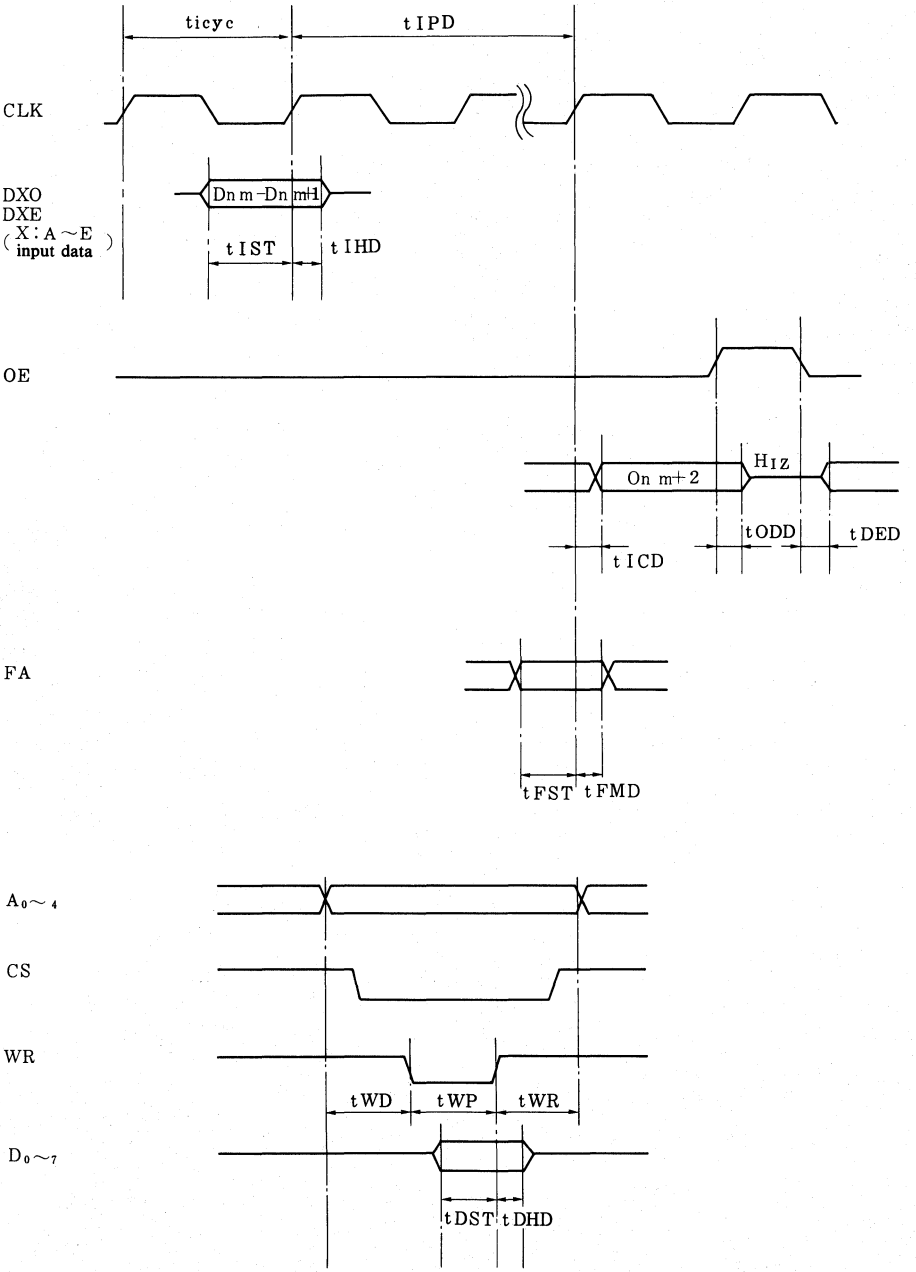
Symbol	Parameter	Condition	MIN.	TYP.	MAX.	Unit	Note
VIH	"H" Input Voltage		2.2		VCC +0.3	V	
VIL	"L" Input Voltage		−0.3		0.8	V	
ILI	Input Leakage Current	0 ≦ VI ≦ VCC			±10	μA	
VOH	"H" Output Voltage	IOH = −4.0 mA	2.4			V	
VOL	"L" Output Voltage	IOL = 4.0 mA			0.4	V	
ICC	Supply Voltage Current (Operating)				100	mA	Note1

Note 1: When the carriers of all multipliers are propagated from the lowest bit to the highest bit.

■ AC Electrical Characteristics

Symbol	Item	MIN.	MAX.	Unit
ticyc	Clock cycle	50	—	ns
tist	Element input set-up time	30	—	ns
tiHD	Element input hold time	5	—	ns
tiPD	Element output pipeline delay time (odd-even) (serial)	650 700		ns
tiCD	Delay time from element output and SGN and OVR clocks		30	ns
tFST	Format adjustment set-up time	40		ns
tODD	Disable time of element output from OE and SGN and OVR outputs		30	ns
tDED	Enable time of element output from OE and SGN and OVR outputs		30	ns
tDST	Coefficient data input set-up time	30		ns
tDHD	Coefficient data input hold time	10		ns
tWP	Write pulse width	40		ns
tWD	Set-up time for —A signal (to RW)	30		ns
tWR	Hold time for —A signal (to RW)	30		ns
tFMD	Format adjustment hold time	40		ns

■ Timing Chart



■ Operation

1. Flat surface filtering

	1	2	3	4	5	6		n − 1	n
1	D_{11}	D_{11}	D_{13}	D_{14}	D_{15}	D_{16}		$D_1(n-_1)$	D_1n
2	D_{21}	D_{22}						$D_2(n-_1)$	D_2n
3	D_{31}	D_{32}	D_{33}					$D_3(n-_1)$	D_3n
4	D_{41}	D_{42}							
5	D_{51}	D_{52}							

Fig-1 Flat Surface Element Data

W_{11}	W_{12}	W_{13}	W_{14}	W_{15}
W_{21}	W_{22}	W_{23}	W_{24}	W_{25}
W_{31}	W_{32}	W_{33}	W_{34}	W_{35}
W_{41}	W_{42}	W_{43}	W_{44}	W_{45}
W_{51}	W_{52}	W_{53}	W_{54}	W_{55}

Fig-2 Filter Coefficient

When performing flat surface filtering on element data as shown in Fig-1 with filter coefficients as shown in Fig-2, the operation results of element data D_{33} is as follows:

$$F(D_{33}) = \sum_{i=1}^{5} \left(\sum_{j=1}^{5} W_{ij} D_{ij} \right)$$

The RF5C67 IC performs the above flat surface filtering on consecutive input elements. The coefficients are as follows:

$$W_{i5} = \pm W_{i1}$$
$$W_{i4} = \pm W_{i2} \qquad (i = 1 \sim 5)$$

2. Data input

The RF5C67 IC has two modes of element data input:

1) serial mode and
2) odd-even mode.

1) Serial mode

When flat-surface element data in Fig-1 is input as in Fig-3:

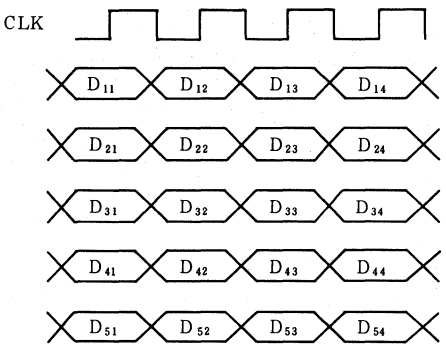


Fig-3 Data Input in Serial mode

The RF5C67 outputs results of processing accordingly, as shown in Fig-4.
Data in the first line is input simultaneously to DAI and DAII.
Data in the second to fifth lines are also input to I and II.

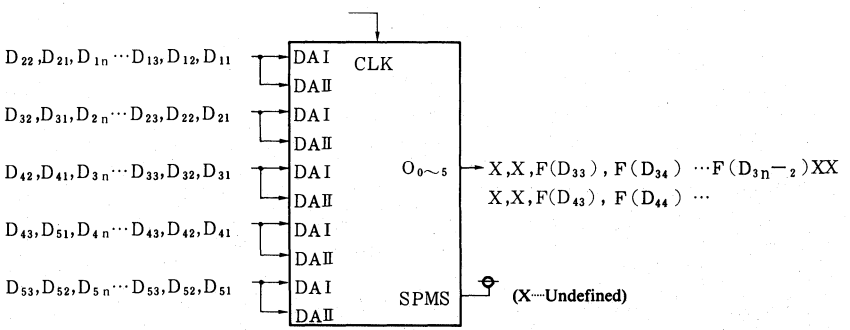


Fig-4 Flow of Data Processing in Serial Mode

2) Odd-even mode
When the flat-surface element data in Fig-1 is input as in Fig-5:

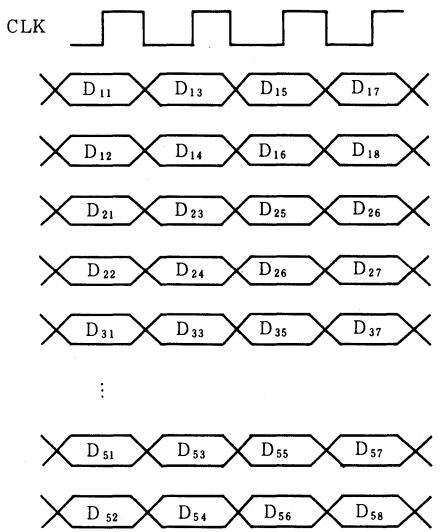


Fig-5 Data Input in Odd-even mode

Two RF5C67 are required for flat-surface filtering, as shown in Fig-6. The odd data in the first line is input to DAI of the RF5C67 in odd mode and to DAII of the other RF5C67 in even mode. Even data is input to both DAII and DAI. Data in the second to fifth lines is also treated in the same way.

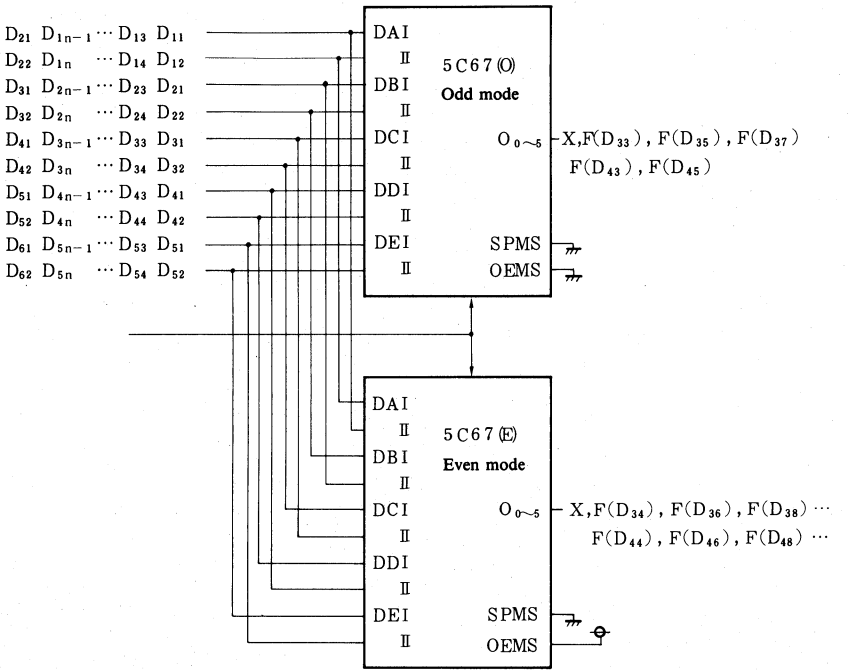


Fig-6 Flow of Data Processing in Odd-even mode

The processing results of elements D_{i2m-1}, D_{i2m} (m is integer) are output simultaneously from the RF5C67 (O) and the RF5C67 (E).

1) and 2) modes are switched at the SPMS (serial/parallel mode select) and the OEMS (odd-even mode select) terminals. (See Table-1.)

SPMS	OEMS	Mode of RF5C67
L	L	Odd-even mode, odd data output
L	H	Odd-even mode, even data output
H	X	Serial mode

Table-1 Mode Switching of RF5C67

3. LINE ADD

This section explains the flow of signals in the LINE ADD block shown in Block Diagram.

1) Serial mode

Fig-7 shows the flow of signals in LINE ADD when using the RF5C67 in serial mode.

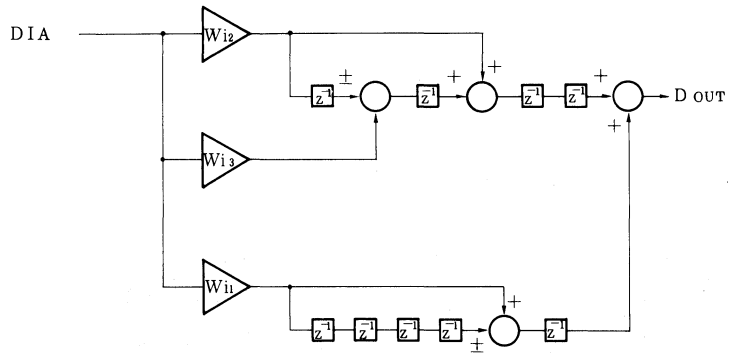


Fig-7 Flow of Signals in Serial mode

As shown in the figure, data items are input from DIA in the order: D_{i1}, D_{i2}, D_{i3}, . . . , and are multiplied by W_{i1}, W_{i2}, and W_{i3}. The results of multiplication is delayed by an appropriate clock in the delay unit, then added or subtracted.

$$F(Din) = W_{i1} \cdot D_{in+2} + W_{i2} \cdot D_{in+1} + W_{i3} \cdot D_{in} \pm W_{i2} \cdot D_{in-1} \pm W_{i1} \cdot D_{in-2}$$

D_{out} outputs the following as a result:

Determine the sign (+ or −) by writing it from the CPU to a register simultaneously with the coefficient of multiplier, as described later.

2) Odd-even mode

Fig-8 shows the folow of signals in LINE ADD in odd-even mode.

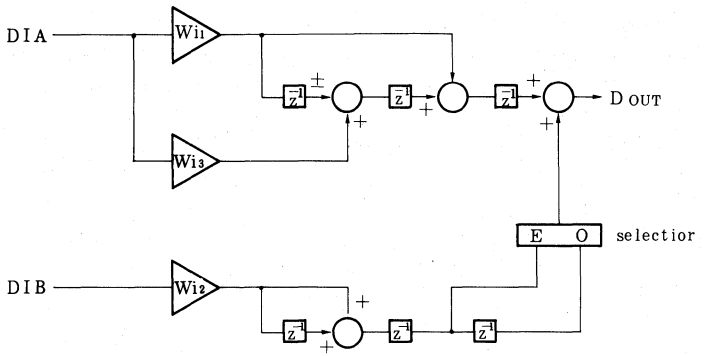


Fig-8 Flow of Signals in Odd-even Mode

The flows of signals are a little different in odd mode (odd data output) and even mode (even data output). Table-2 shows the relationship of data I/O in each mode.

	Odd mode	Even mode
DIA	D_{i1}, D_{i3}, D_{i5}, ···, D_{i2n-1},	D_{i2}, D_{i4}, D_{i6}, ···, D_{i2n}, ···
DIB	D_{i2}, D_{i4}, D_{i6}, ···, D_{i2n}, ···	D_{i1}, D_{i3}, D_{i5}, ···, D_{i2n-1}, ···
DOUT	F (D_{i3}), F (D_{i5}), F (D_{2n-1})	F (D_4), F (D_6), ··· F (D_{i2n}) ···

Table-2

At the selector, O is selected in odd mode and E is selected in even mode.
In odd mode, the processing result of odd data is output as follows:

$$F(D_{i2n-1}) = W_{i1} \cdot D_{i2n+1} + W_{i2} \cdot D_{i2n} + W_{i3} \cdot D_{i2n-1} \pm W_{i2} \cdot D_{i2n-2} \pm W_{i1} \cdot D_{i2n-3}$$

At the same time, in even mode, the processing result of even data is output as follows:

$$F(D_{i2n}) = W_{i1} \cdot D_{i2n+2} + W_{i2} \cdot D_{i1n+1} + W_{i3} \cdot D_{i3n} \pm W_{i2} \cdot D_{i2n-1} \pm W_{i1} \cdot D_{i2n-2}$$

As seen in the comparison of Fig-7 and Fig-8, the multipliers, which multiply the filter coefficients W_{i1} and W_{i2}, are different in 1) serial mode and 2) odd-even mode.

As described later, when setting filter coefficients from the CPU, W_{i1} and W_{i2} must be written to different addresses in different modes.

4. DEV/FA

a) Division circuit

The RF5C67 performs division using a shifter and addition/subtraction unit. Fig-9 shows the circuit diagram of the part of DIV/FA that performs division.

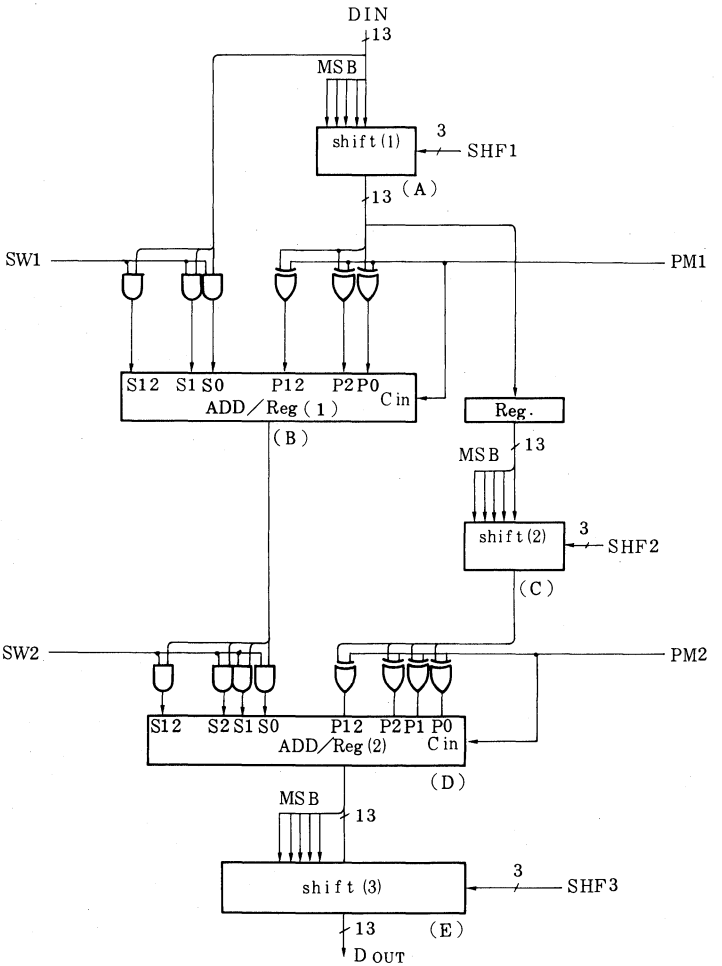


Fig-9 Division Circuit

shift (1), shift (2) : Arbitrary 0- to 4-bit shift to right
shift (3) : Arbitrary 0- to 5-bit shift to right
ADD/Reg : 13-bit adder + register
SW1, SW2 : Selects whether to enter data or 0 in one input of the adder.
PM1, PM2 : Selects whether to add or subtract the other input of the adder.
SHF1, SHF2, SHF3: Determines the shift length of shifts (1), (2), and (3).

b) Principle of division

Input (DIN) : X
Length of shift (1) : p
Length of shift (2) : q
Length of shift (3) : r

When SW1 = SW = 1 and PM1 = PM2 = 0, the values output to (A), (B), (C), (D), and (E) in Fig-1 are as follows:

$$(A) = 2^{-p} \cdot X$$
$$(B) = X + 2^{-p} \cdot X$$
$$(C) = 2^{-(p+q)} \cdot X$$
$$(D) = X + 2^{-p} \cdot X + 2^{-(p+q)} \cdot X$$
$$(E) = 2^{-r} \cdot X + 2^{-(p+r)} \cdot X + 2^{-(p+q+r)} \cdot X$$

For example, to calculate 1/25X,

$$1/25 = 0.04$$
$$\fallingdotseq 1 \times 2^{-5} + 1 \times 2^{-7} + 1 \times 2^{-10} \ (=0.040039)$$

Therefore, the following values calculate 1/25X:

r = 5, p = 2, q = 3

$$1/15 = 0.06666$$
$$\fallingdotseq 1 \times 2^{-4} + 1 \times 2^{-8} \ (=0.06640)$$

Therefore, the following values calculate 1/15X:
0-bit shift of shift (1) (p = 0), SW1 = 0
4-bit shift of shift (2) (q = 4), SW1 = 1
4-bit shift of shift (3) (r = 4)

Then obtain 1/9:

$$1/9 = 0.1111_{2}$$
$$\fallingdotseq 1 \times 2^{-4} + 1 \times 2^{-5} + 1 \times 2^{-6} + 1 \times 2^{-9} \ (=0.11132)$$

3-bit shift of shift (1) (p = 3)
PM1 = 1 (subtraction)
SW1 = 1
Then,

$$(C) = X - 2^{-3} \cdot X = 2^{-1} \cdot X + 2^{-2} \cdot X + 2^{-3} \cdot X$$

3-bit shift of shift (2) (q = 3)
PM2 = 0 (addition)
SW1 = 1
3-bit shift of shift (3) (r = 3)
Then,

$$(E) = 2^{-3}(2^{-1} \cdot X + 2^{-2} \cdot X + 2^{-3} \cdot X + 2^{-6} \cdot X)$$
$$= 2^{-4} \cdot X + 2^{-5} \cdot X + 2^{-6} \cdot X + 2^{-9} \cdot X$$
$$\fallingdotseq 1/9 \cdot X$$

For 1/2n, n is changed by operation of SHF1, SHF2, and SHF3, within $0 \leqq n \leqq 11$ (see Table-3).

	p(SHF1)	PM1	SW1	q(SHF2)	PM2	SW2	r(SHF3)	Approximation
1/25·X	2	0	1	3	0	1	5	$(2^{-5}+2^{-7}+2^{-10})\cdot X$
1/15·X	0	0	0	4	0	1	4	$(2^{-4}+2^{-8})\cdot X$
1/9 ·X	3	1	1	3	0	1	3	$(2^{-4}+2^{-5}+2^{-6}+2^{-9})\cdot X$
X	0	0	0	0	0	0	0	X
1/2 ·X	0	0	0	0	0	0	1	$2^{-1}\cdot X$

Table-3 Division Coefficient and Its Input Setting

c) Operation deviation

In performing divisions using the circuit in Fig-9, errors occur due to following two reasons:

1. Errors due to expressing divisions in the approximation.
2. Errors due to truncating the lower bits of data in shifts (1), (2), and (3).

Table-4, -5, and -6 show the errors in executing divisions of 1/25, 1/15, and 1/9.

Division	Quotient	Maximum error
⋮	⋮	⋮
① 51/25 ~ 75/25	2	1
② 76/25 ~ 99/25	3	0
⋮	⋮	⋮

The following is an explanation of Table-4, -5, and -6 with the above example:

① The result of divisions from 51/25 to 75/25 is always 2. At that time, 75/25 = 3 actually, so the maximum error in this operation is 1.

② The result of divisions from 76/25 to 99/25 is always 3. At that time, 99/25 = 3.96 actually, so the maximum error in this operation is 0 considering the divisions that cuts off the values after the decimal point.

Division	Quotient	Maximum error
0/25 ~ 25/25	0	1
26/25 ~ 50/25	1	1
51/25 ~ 75/25	2	1
76/25 ~ 99/25	3	1
100/25 ~ 125/25	4	0
126/25 ~ 150/25	5	1
151/25 ~ 175/25	6	1
176/25 ~ 199/25	7	1
200/25 ~ 224/25	8	0
225/25 ~ 250/25	9	0
251/25 ~ 275/25	10	1
276/25 ~ 299/25	11	1
300/25 ~ 324/25	12	0
325/25 ~ 350/25	13	0
351/25 ~ 375/25	14	1
376/25 ~ 399/25	15	1
400/25 ~ 424/25	16	0
425/25 ~ 499/25	17	0
450/25 ~ 475/25	18	0
476/25 ~ 499/25	19	1
500/25 ~ 524/25	20	0
525/25 ~ 549/25	21	0
550/25 ~ 575/25	22	0
576/25 ~ 599/25	23	1
600/25 ~ 624/25	24	0
625/25 ~ 649/25	25	0
650/25 ~ 674/25	26	0
675/25 ~ 699/25	27	0
700/25 ~ 724/25	28	0
725/25 ~ 749/25	29	0
750/25 ~ 774/25	30	0
775/25 ~ 799/25	31	0
800/25 ~ 824/25	32	0
825/25 ~ 849/25	33	0
850/25 ~ 874/25	34	0
875/25 ~ 899/25	35	0
900/25 ~ 924/25	36	0
925/25 ~ 949/25	37	0
950/25 ~ 974/25	38	0
975/25 ~ 999/25	39	0
1000/25 ~ 1023/25	40	0
1024/25 ~ 1049/25	41	−1
1050/25 ~ 1074/25	42	0
1075/25 ~ 1099/25	43	0
1100/25 ~ 1123/25	44	0
1124/25 ~ 1149/25	45	−1
1150/25 ~ 1174/25	46	0
1175/25 ~ 1199/25	47	0
1200/25 ~ 1223/25	48	0
1224/25 ~ 1248/25	49	−1
1249/25 ~ 1274/25	50	−1
1275/25 ~ 1299/25	51	0
1300/25 ~ 1323/25	52	0
1324/25 ~ 1348/25	53	−1
1349/25 ~ 1374/25	54	−1
1375/25 ~ 1399/25	55	0
1400/25 ~ 1423/25	56	0
1424/25 ~ 1448/25	57	−1
1449/25 ~ 1473/25	58	−1
1474/25 ~ 1499/25	59	−1
1500/25 ~ 1523/25	60	0
1524/25 ~ 1548/25	61	−1
1549/25 ~ 1573/25	62	−1
1574/25 ~ 1599/25	63	−1

Table-4 Errors in 1/25 Operation

Division			Quotient	Maximum error
0/15	~	15/15	0	1
16/15	~	30/15	1	1
31/15	~	45/15	2	1
46/15	~	60/15	3	1
61/15	~	75/15	4	1
76/15	~	90/15	5	1
91/15	~	105/15	6	1
106/15	~	120/15	7	1
121/15	~	135/15	8	1
136/15	~	150/15	9	1
151/15	~	165/15	10	1
166/15	~	180/15	11	1
181/15	~	195/15	12	1
196/15	~	210/15	13	1
211/15	~	225/15	14	1
226/15	~	240/15	15	1
241/15	~	255/15	16	1
256/15	~	271/15	17	1
272/15	~	286/15	18	1
287/15	~	301/15	19	1
302/15	~	316/15	20	1
317/15	~	331/15	21	1
332/15	~	346/15	22	1
347/15	~	361/15	23	1
362/15	~	376/15	24	1
377/15	~	391/15	25	1
392/15	~	406/15	26	1
407/15	~	421/15	27	1
422/15	~	436/15	28	1
437/15	~	451/15	29	1
452/15	~	466/15	30	1
467/15	~	481/15	31	1
482/15	~	496/15	32	1
497/15	~	511/15	33	1
512/15	~	527/15	34	1
528/15	~	542/15	35	1
543/15	~	557/15	36	1
558/15	~	572/15	37	1
573/15	~	587/15	38	1
588/15	~	602/15	39	1
603/15	~	617/15	40	1
618/15	~	632/15	41	1
633/15	~	647/15	42	1
648/15	~	662/15	43	1
663/15	~	677/15	44	1
678/15	~	692/15	45	1
693/15	~	707/15	46	1
708/15	~	722/15	47	1
723/15	~	737/15	48	1
738/15	~	752/15	49	1
753/15	~	767/15	50	1
768/15	~	783/15	51	1
784/15	~	798/15	52	1
799/15	~	813/15	53	1
814/15	~	828/15	54	1
829/15	~	843/15	55	1
844/15	~	858/15	56	1
859/15	~	873/15	57	1
874/15	~	888/15	58	1
889/15	~	903/15	59	1
904/15	~	918/15	60	1
919/15	~	933/15	61	1
934/15	~	948/15	62	1
949/15	~	963/15	63	1

Table-5 Errors in 1/15 Operation

Division	Quotient	Maximum error
0 /9 ~ 8/9	0	0
9 /9 ~ 17/9	1	0
18 /9 ~ 26/9	2	0
27 /9 ~ 35/9	3	0
36 /9 ~ 44/9	4	0
45 /9 ~ 53/9	5	0
54 /9 ~ 62/9	6	0
63 /9 ~ 70/9	7	0
71 /9 ~ 80/9	8	− 1
81 /9 ~ 89/9	9	0
90 /9 ~ 98/9	10	0
99 /9 ~ 107/9	11	0
108 /9 ~ 116/9	12	0
117 /9 ~ 125/9	13	0
126 /9 ~ 133/9	14	0
134 /9 ~ 142/9	15	− 1
143 /9 ~ 152/9	16	− 1
153 /9 ~ 161/9	17	0
162 /9 ~ 170/9	18	0
171 /9 ~ 179/9	19	0
180 /9 ~ 188/9	20	0
189 /9 ~ 196/9	21	0
197 /9 ~ 205/9	22	− 1
206 /9 ~ 214/9	23	− 1
215 /9 ~ 224/9	24	− 1
225 /9 ~ 233/9	25	0
234 /9 ~ 242/9	26	0
243 /9 ~ 251/9	27	0
252 /9 ~ 259/9	28	0
260 /9 ~ 268/9	29	− 1
269 /9 ~ 277/9	30	− 1
278 /9 ~ 286/9	31	− 1
287 /9 ~ 296/9	32	− 1
297 /9 ~ 305/9	33	0
306 /9 ~ 314/9	34	0
315 /9 ~ 322/9	35	0
323 /9 ~ 331/9	36	− 1
332 /9 ~ 340/9	37	− 1
341 /9 ~ 349/9	38	− 1
350 /9 ~ 358/9	39	− 1
359 /9 ~ 368/9	40	− 1
369 /9 ~ 377/9	41	0
378 /9 ~ 385/9	42	0
386 /9 ~ 394/9	43	− 1
395 /9 ~ 403/9	44	− 1
404 /9 ~ 412/9	45	− 1
413 /9 ~ 421/9	46	− 1
422 /9 ~ 430/9	47	− 1
431 /9 ~ 440/9	48	− 1
441 /9 ~ 448/9	49	0
449 /9 ~ 457/9	50	− 1
458 /9 ~ 466/9	51	− 1
467 /9 ~ 475/9	52	− 1
476 /9 ~ 484/9	53	− 1
485 /9 ~ 493/9	54	− 1
494 /9 ~ 502/9	55	− 1
503 /9 ~ 511/9	56	− 1
512 /9 ~ 520/9	57	− 1
521 /9 ~ 529/9	58	− 1
530 /9 ~ 538/9	59	− 1
539 /9 ~ 547/9	60	− 1
548 /9 ~ 556/9	61	− 1
557 /9 ~ 565/9	62	− 1
566 /9 ~ 574/9	63	− 1

Table-6 Errors in 1/9 Division

d) FA (Format Adjust)

The result output of shifter (3) is finally made into a 6-bit absolute integral value. Two ways are available for handling negative values:

When FA = 1
The negative value is converted into a positive value with the same absolute value. Then, values not smaller than 64 are rounded down to 63.

When FA = 0
Negative values are rounded to 0. Values not smaller than 64 are rounded down to 63.

5. Coefficient Input

a) Coefficient address

When performing space filtering with the RF5C67 IC, the filter coefficient and division coefficient must be prespecified. Select a corresponding register at A0 to A4 terminals, and write 8-bit data with $\overline{CS}$ and $\overline{WR}$ signals. Table-7 shows A0 to A4 signals and registers to be selected. As described earlier, the addresses to select filter coefficients W_{i1} and W_{i2} are different in serial mode and in odd-even mode.

A					Odd-even mode	Serial mode
4	3	2	1	0		
0	0	0	0	0	W_{11}	W_{12}
0	0	0	0	1	W_{12}	W_{11}
0	0	0	1	0	W_{13}	W_{13}
0	0	0	1	1	W_{21}	W_{22}
0	0	1	0	0	W_{22}	W_{21}
0	0	1	0	1	W_{23}	W_{23}
0	0	1	1	0	W_{31}	W_{32}
0	0	1	1	1	W_{32}	W_{31}
0	1	0	0	0	W_{33}	W_{33}
0	1	0	0	1	W_{41}	W_{42}
0	1	0	1	0	W_{42}	W_{41}
0	1	0	1	1	W_{43}	W_{43}
0	1	1	0	0	W_{51}	W_{52}
0	1	1	0	1	W_{52}	W_{51}
0	1	1	1	0	W_{53}	W_{53}

Filter coefficient

A					
4	3	2	1	0	
1	0	0	0	0	LATCH1
1	0	0	0	1	LATCH2
1	0	0	1	0	LATCH3

Division coefficient

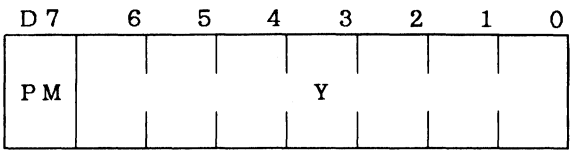
Table-7 A0 to A4 Signals and Selected Coefficient

b) Coefficient format

The coefficient to be specified consists of eight bits. The filter and division coefficients are different.

1) Filter coefficient

A filter coefficient consists of the following eight bits:



Y: 7-bit integral two's compliment of W_{i1}, W_{i2}, and W_{i3}
Expression
D6 indicates the sign bit.
D0 indicates LSB.

PM: Indicates whether the sign of W_{i5} and W_{i4} is reversed for W_{i1} and W_{i2}.
When PM = 0, $W_{i5} = W_{i1}$ and $W_{i4} = W_{i2}$
When PM = 1, $W_{i5} = -W_{i1}$ and $W_{i4} = -W_{i2}$
With W_{i3}, PM is ignored.

2) Division coefficient

Setting division coefficients

Select a coefficient register (LATCH 1, 2, and 3) by A0 to A4, and write a specific value to each.

The formats of LATCH 1, 2, and 3 are as follows:

LATCH 1

D7	6	5	4	3	2	1	0
X	PM1	SW1	p (SHF1)				

LATCH 2

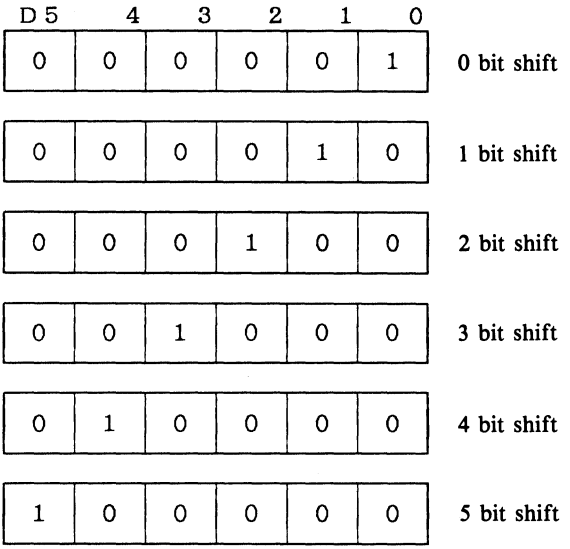
X	PM2	SW2	q (SHF2)				

LATCH 3

X	X	r (SHF3)					

As shown in Section 4 b), PM1, SW1, p, PM2, SW2, q, and r indicate sign control, 0 selection, and shift length.

The relationship between the shift length of the shifters and the register coefficient is as follows:



The division coefficient is as shown in Table-3.

Table-8 shows the data input to LATCH1 (address 10), LATCH2 (11), and LATCH3 (12) to calculate 1/25, 1/15, 1/9, 1/3, and 1/8.

Division coefficient	Address	Input data								
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
1/25	10	X	0	1	0	0	1	0	0	24
	11	X	0	1	0	1	0	0	0	28
	12	X	X	1	0	0	0	0	0	20
1/15	10	X	0	0	0	0	0	0	0	00
	11	X	0	1	1	0	0	0	0	30
	12	X	X	0	1	0	0	0	0	10
1/9	10	X	1	1	0	1	0	0	0	68
	11	X	0	1	0	1	0	0	0	28
	12	X	X	0	0	1	0	0	0	08
1/3	10	X	0	1	0	0	1	0	0	24
	11	X	0	1	0	0	1	0	0	24
	12	X	X	0	0	0	1	0	0	04
1/8	10	X	0	0	0	0	0	0	1	01
	11	X	0	0	0	0	0	0	1	01
	12	X	X	0	0	1	0	0	0	08

X: Don't Care

Table-8 Division coefficient and input data

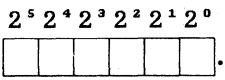
6. Set Function

The RF5C67 has $\overline{SET}$ terminal. Setting this terminal to 0 sets $W_{33} = 1$, $W_{11} = W_{12} = \cdots\cdots W_{54} = W_{55} = 0$ to filter coefficients and sets 1 to division coefficient. Then, unprocessed data is output.

7. Value Format

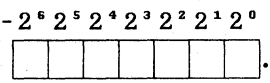
The following defines the format of external signals and internal operation values:

1) Input signal DA0 to DE0, DAE to DEE (0 to 63)



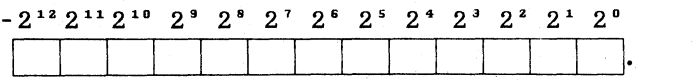
6 bit integer unsigned magnitude

2) Filter coefficient W_{11} to W_{33} (-64 to 63)



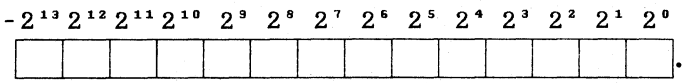
7 bit integer two's compliment

3) Intermediate operation (sum of products) (-4096 to 4095)



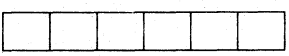
13bit integer two's compliment

4) Division output (shifter 2 output) (-8192 to 8191)



14bit integer two's compliment

5) Format adjustment circuit output (0 to 63)



6 bit integer unsigned magnitude

8. Overflow in convolution

The sum-of-product operation of intermediate 25 elements are performed in 13-bit two's compliment. Therefore, the intermediate result must be within -4096 to 4095. Otherwise the results will be incorrect because of overflow or underflow.

RF5C136

Transversal Filter for Video Signal

The RF5C136 Video Signal transversal Filter performs a ghost canceller of TV pictures by use of GCR signal on the TV signal.
The LSI has 8-bit signal Inputs and 8-bit coefficient Inputs and includes 32 multipliers and 32 adders. The 5C136 is fabricated in low-power COMS technology and is available in a 80 pin QFP.

■ Features

(Function)

- Asymmetric 32 taps transversal filter (Cascade connection available)

(Data length)

- Input data : 8 bit (Possible to switch absolute value with no-sign and 2's complement.)
- Input coefficient : 8 bit (2's complement)
- SUM I/O : 16 bit (2's complement, SUM output reset)
- Multiplier : 8 x 8 ⇒ 16 bit
- Adder : 16+19⇒ 19 bit · SUM output 16 bit

(Operating frequency)

- Max. 16 MHz (Clock rate)

(Rewriting coefficient)

- Specifing the address of the coefficient register
- 8 bit parallel
- Coefficient reset

(Overflow detection)

- Overflow detect pin
- Possible to detect the overflow in the cascade connection by the use of daisy chain.

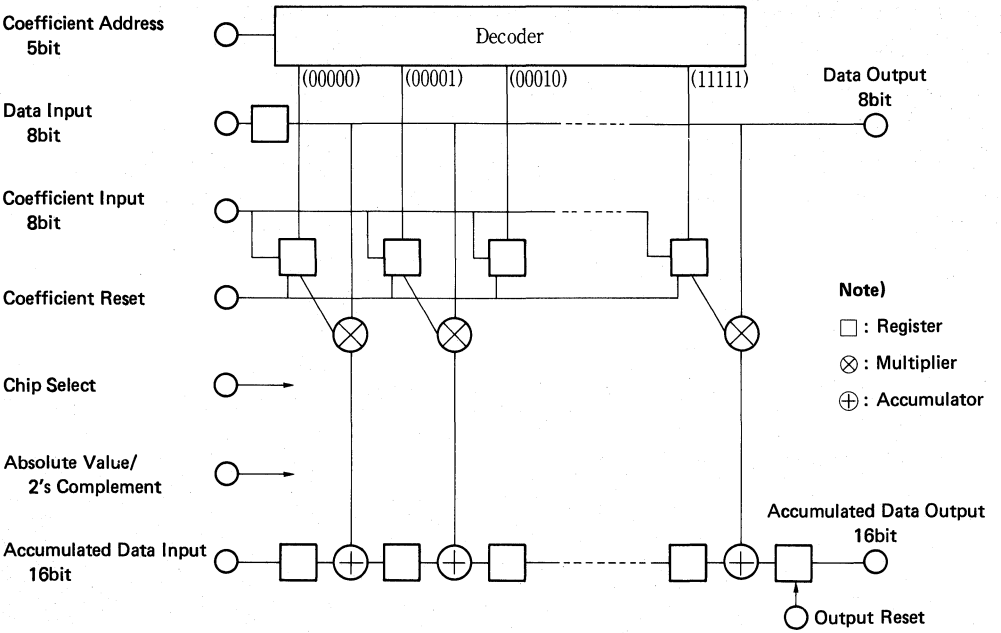
(Package)

- 80 PIN QFP

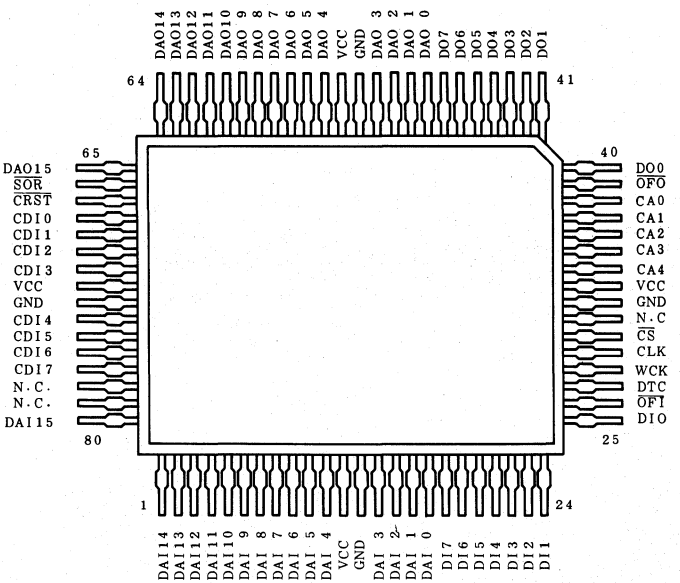
■ Application

- Ghost canceller
- Digital Video
- etc.

■ Block Diagram



■ Pin Configuration



■ Pin Description

Pin Name	I/O	Description
Vcc		Power Supply
GND		GND
DI_7~DI_0	I	Data Input DI_7 (MSB) ~ DI_0 (LSB) Data are input on the rising edge of CLK.
DO_7~DO_0	O	Data Output DO_7 (MSB) ~ DO_0 (LSB)
DAI_{15}~DAI_0	I	SUM Data Input DAI_{15} (MSB) ~ DAI_0 (LSB) Data are input on the rising edge of CLK.
DAO_{15}~DAO_0	O	SUM Data Output DAO_{15} (MSB) ~ DAO_0 (LSB)
GDI_7~CDI_0	I	Coefficient Data Input Data are input on the rising edge of WCK.
CA_4~CA_0	I	Coefficient Address Input CA_4 CA_3 CA_2 CA_1 CA_0 — Number of Coefficient Register 0 0 0 0 0 — 0 0 0 0 0 1 — 1 0 0 0 1 0 — 2 . . . . . — . . . . . . — . . . . . . — . 1 1 1 1 1 — 31
$\overline{CS}$	I	Chip Select (LOW Active) When $\overline{CS}$ is Low, the coefficient can be input.
DTC	I	Data Input Switch High Absolute value format LOW 2's complement
$\overline{OFI}$	I	Overflow Input $\overline{OFI}$ is used for cascade connection for overflow signal. When Low, overflow is detected.
$\overline{OFO}$	O	Overflow Output $\overline{OFO}$ becomes Low for overflow on the rising edge of CLK.
CLK	I	Clock Input
WCK	I	Clock Input for coefficient input
$\overline{SOR}$	I	SUM Data output reset (LOW Active) When $\overline{SOR}$ is Low, all SUM out data become Low on the rising edge of CLK.
$\overline{CRST}$	I	Coefficient Reset Input (LOW Active) When $\overline{CRST}$ is Low, all coefficient registers become Low on the rising edge of CLK.

■ Absolute Maximum Ratings

Symbol	Parameter	Condition	Rating	Unit	Note
Vcc	Supply Voltage	GND=0V	-0.3~7	V	
VTE	Voltage Range on Any Pin	GND=0V	-0.3~Vcc+0.3	V	
Pd	Power Consumption Power Reduction Rate	Ta≦25°C Ta>25°C	1200 11	mW mW/°C	Mounted on a Board
Topr	Operating Temperature		0~70	°C	
Tstg	Storage Temperature		-40~125	°C	

■ Recommended Operating Condition

Symbol	Parameter	Condition	Value	Unit	Note
Vcc	Supply Voltage		4.5~5.5	V	
Ta	Operating Temperature		0~70	°C	

■ DC Electrical Characteristics

(Ta=0~70°C Vcc=5V±10%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Note
V_{IH}	"H" Input Voltage		2.0		Vcc+0.3	V	
V_{IL}	"L" Input Voltage		-0.3		0.8	V	
I_{LI}	Input Leakage Current	V_{IN}=0~Vcc	-10		10	μA	
V_{OH}	"H" Output Voltage	I_{OH}=-4mA	2.4			V	
V_{OL}	"L" Output Voltage	I_{OL}=4mA			0.4	V	
I_{CC1}	Supply Current (stand by)	V_{IN}=Vcc			300	μA	
I_{CC2}	Supply Current (operating)	14.3MHz			125	mA	

■ AC Electrical Characteristics

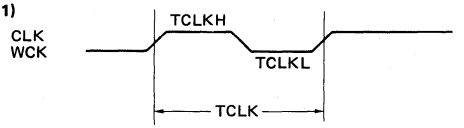
(Ta = 25°C Vcc = 5.0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Note
TCLK	Clock Cycle		62			nsec	CLK WCK [Note 1]
TCLK L	"L" Level Clock Pulse Width		20			nsec	CLK WCK [Note 1]
TCLK H	"H" Level Clock Pulse Width		20			nsec	CLK WCK [Note 1]
IMLS	Picture Input Setup Time	refer to CLK	25			nsec	[Note 2]
IMIH	Picture Input Hold Time	refer to CLK	5			nsec	[Note 2]
RDIS	Accumulated Data Input Setup Time	refer to CLK	25			nsec	[Note 2]
RDIH	Accumulated Data Input Hold Time	refer to CLK	5			nsec	[Note 2]
CDS	Coefficient Data Setup Time	refer to WCK	25			nsec	[Note 3]
CDH	Coefficient Data Hold Time	refer to WCK	5			nsec	[Note 3]
CSS	Chip Select Setup Time	refer to WCK	25			nsec	[Note 3]
CSH	Chip Select Hold Time	refer to WCK	5			nsec	[Note 3]
CAS	Coefficient Address Setup Time	refer to WCK	30			nsec	[Note 3]
CAH	Coefficient Address Hold Time	refer to WCK	5			nsec	[Note 3]
ODD	Output Data Delay Time	from CLK			35	nsec	[Note 4]
SORS	SOR Setup Time	refer to CLK	25			nsec	[Note 2]
SORH	SOR Hold Time	refer to CLK	5			nsec	[Note 2]
CRTS	Coefficient Reset Setup Time	refer to WCK	25			nsec	[Note 3]
CRTH	Coefficient Reset Hold Time	refer to WCK	5			nsec	[Note 3]

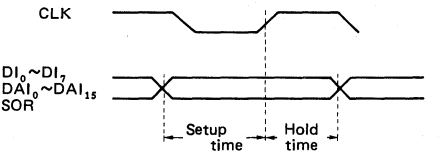
Note) Output load=35pF

(Timing Chart)

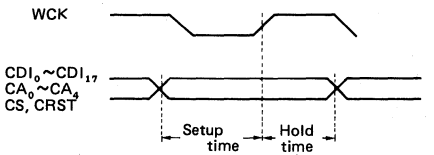
Note 1)



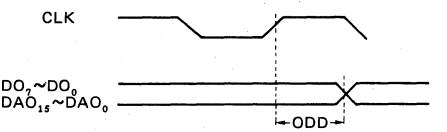
Note 2)



Note 3)



Note 4)



■ Description

(1) Data Input Format

DTC	Input Format
High	Absolute value
Low	2's complement

(Absolute value format)

▽ decimal point

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
-1 2	-2 2	-3 2	-4 2	-5 2	-6 2	-7 2	-8 2

(2's complement)

▽ decimal point

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0 -2	-1 2	-2 2	-3 2	-4 2	-5 2	-6 2	-7 2

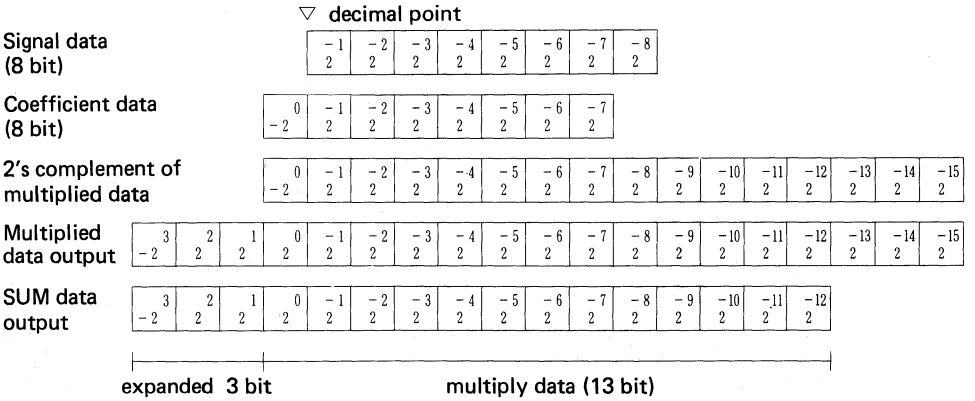
(2) Coefficient data format (2's complement)

▽ decimal point

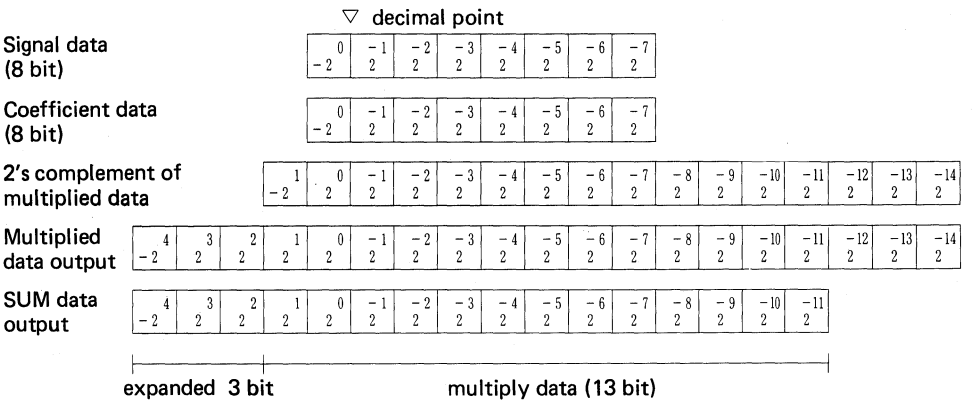
CD_7	CD_6	CD_5	CD_4	CD_3	CD_2	CD_1	CD_0
0 -2	-1 2	-2 2	-3 2	-4 2	-5 2	-6 2	-7 2

(3) Input/Output data on multiplier

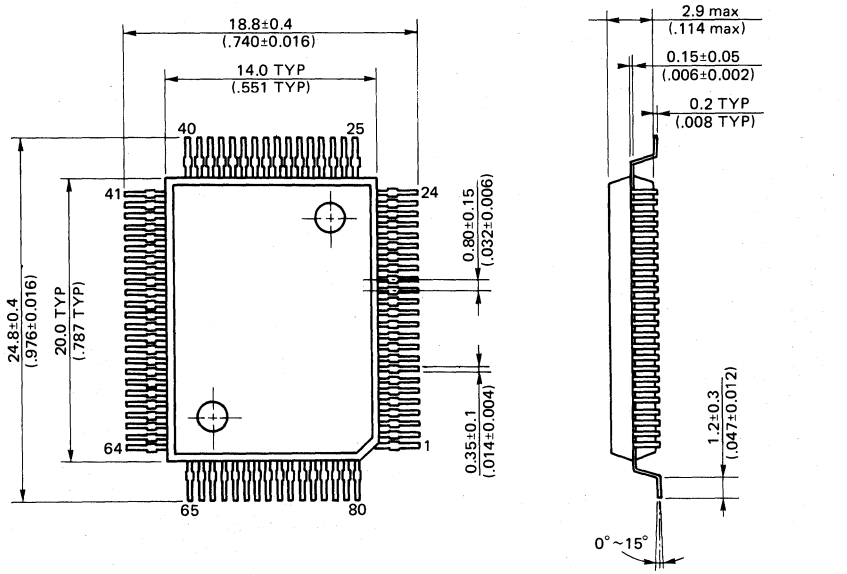
(Absolute value format)



(2's complement)



■ Package Demension



Unit : mm (inch)

4. MPU

CMOS 8bit MPU

RP65C02 G/G-06

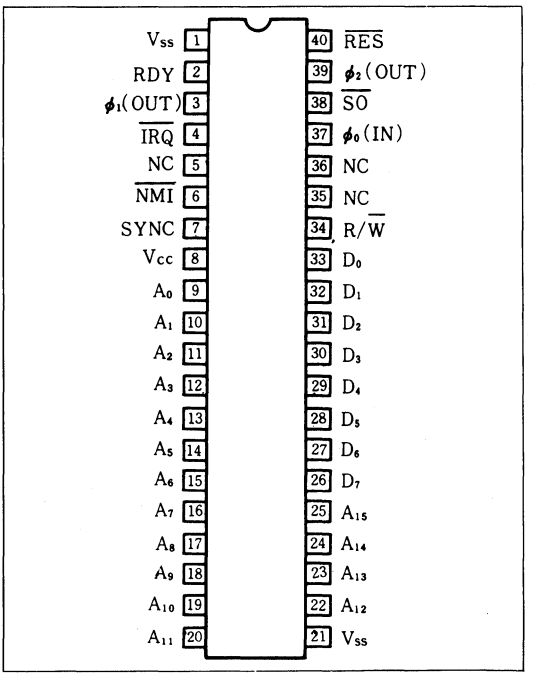
■ GENERAL DESCRIPTION

The RP65C02 is 8-bit CMOS MPU. It has the instruction set and pins which are fully compatible with the NMOS 6502 MPU, and in addition with 59 new instructions. It is provided with the features of the CMOS such as the power-down standby mode, etc.

■ FEATURES

- 68-type 210 instructions
- Powerful 13-type addressing modes
- Programmable stack pointer
- Maskable interrupt and non-maskable interrupt
- 6-type internal registers
- Enable to connect the external memory with up to 64Kbytes
- 8-bit bi-directional data bus, parallel processing
- Clock RP65C02G ..... 4 MHz
  RP65C02G-06 ..... 6 MHz
- Computable decimal and binary
- Bus compatible with M6800
- Pin compatible with ROCKWELL R65C02
- Single power supply 5V operation
- Low power dissipation

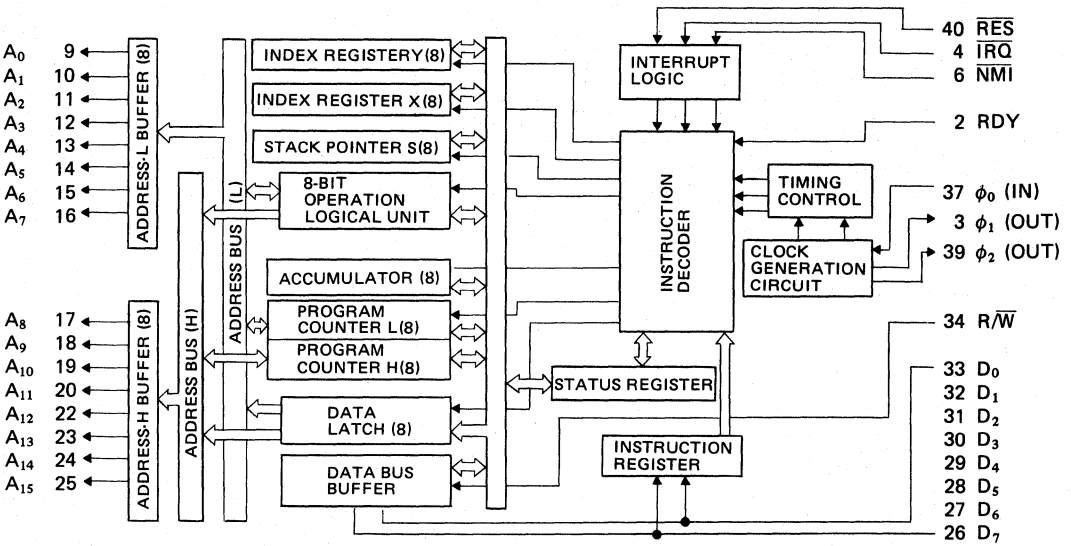
■ PIN CONFIGURATION (TOP VIEW)



■ PIN DESCRIPTION

PIN NAME	FUNCTION	PIN NAME	FUNCTION
Vss	Internal Logic Ground	Vcc	+5V Power Supply
RDY	Ready	$A_0 \sim A_{15}$	Address Bus
ϕ_1 (OUT)	Clock 1 Out	$\overline{RES}$	Reset
$\overline{IRQ}$	Interrupt Request	ϕ_2 (OUT)	Clock 2 Out
NC	No Connection	$\overline{SO}$	Set Overflow
$\overline{NMI}$	Non-Maskable Interrupt	ϕ_0 (IN)	Clock 0 In
SYNC	Synchronize	R/$\overline{W}$	Read/Write
		$D_0 \sim D_7$	Data Bus

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Limits	Unit
V_{CC}	Supply Voltage	−0.3 ~ +7.0	V
V_I	Input Voltage	−0.3 ~ +7.0	V
P_d	Power Dissipation	500	mW
T_{opr}	Operating Ambient Temperature	0 ~ +70	°C
T_{stg}	Storage Temperature	−40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

• DC ELECTRICAL CHARACTERISTICS (Vcc = 5.0 ± 5%, Ta = 0 ~ +70°C)

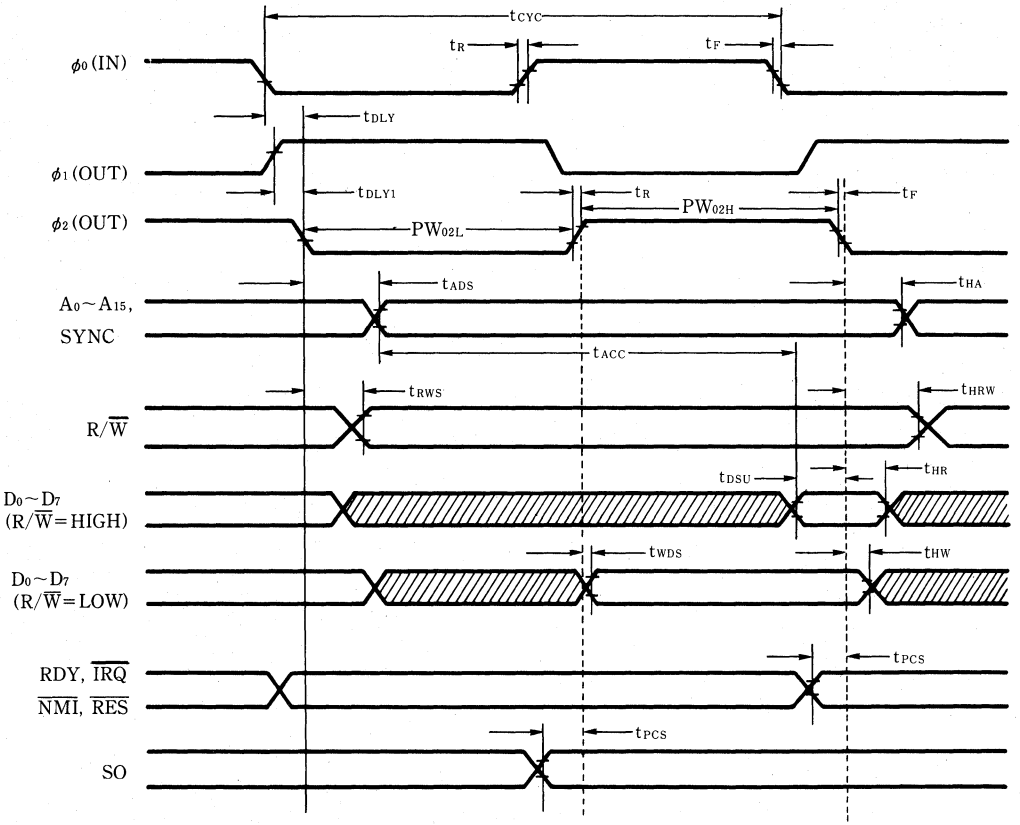
Symbol	Parameters	Measuring Conditions	Specified Value			Unit
			Min	Typ	Max	
V_{IH}	Input High Voltage ϕ_0 (IN), $\overline{NMI}$ $\overline{RES}$, RDY, $\overline{IRQ}$, $\overline{SO}$, $D_0 \sim D_7$		0.7·Vcc 2.0		Vcc+0.3 Vcc+0.3	V V
V_{IL}	Input Low Voltage ϕ_0 (IN), $\overline{NMI}$ $\overline{RES}$, RDY, $\overline{IRQ}$, $\overline{SO}$, $D_0 \sim D_7$		−0.3 −0.3		0.2 0.8	V V
I_{LI}	Input Leak Current $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, $\overline{SO}$ (Internal Pull-Up) ϕ_0 (IN)	Vcc = 5.25V V_{IN} = 0 ~ 5.25V	−100 −10		10 10	μA μA
I_{LO}	Output Floating Leakage Current $D_0 \sim D_7$	V_{IN} = 0 ~ 5.25V	−10		10	μA
V_{OH}	Output High Voltage ϕ_1 (OUT), ϕ_2 (OUT), SYNC, $D_0 \sim D_7$, $A_0 \sim A_{15}$, R/$\overline{W}$	I_{LOAD} = −100μA Vcc = 4.75V	2.4			V
V_{OL}	Output Low Voltage ϕ_1 (OUT), ϕ_2 (OUT), SYNC, $D_0 \sim D_7$, $A_0 \sim A_{15}$, R/$\overline{W}$	I_{LOAD} = 1.6 mA Vcc = 4.75V			0.4	V
I_{OC}	Power Disspation (No-Load) Stand-By Active Low-Power	ϕ_0 * = Vcc or 0, V_{IN} = Vcc RDY = 0			28 5 2	μA mA/MHz mA/MHz
C	Input Capacitance Logic, ϕ_0 (IN) ϕ_1 (OUT), ϕ_2 (OUT), SYNC, $D_0 \sim D_7$, $A_0 \sim A_{15}$, R/$\overline{W}$	V_{IN} = 0, f = 1 MHz			10 20	pF pF

• AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, Ta = 0 ~ 70°C)

Symbol	Parameters	65C02G (4 MHz)		65C02G-06 (6 MHz)		Unit
		Min	Max	Min	Max	
t_{CYC}	Cycle Time	250	DC	166	DC	ns
PW_{02L}	ϕ_2 (OUT) "Low" Clock Pulse Width	100	DC	75	DC	ns
PW_{02H}	ϕ_2 (OUT)"High" Clock Pulse Width	110	DC	80	DC	ns
t_R, t_F	Clock Rising Time, Clock Falling Time		10		10	ns
t_{ADS}	Address Delay Time		80		70	ns
t_{HA}	Address Hold Time	15		15		ns
t_{RWS}	R/$\overline{W}$ Delay Time		80		80	ns
t_{HRW}	R/$\overline{W}$ Hold Time	20		15		ns
t_{DSU}	Read Data Set-Up Time	30		20		ns
t_{HR}	Read Data Hold Time	10		10		ns
t_{WDS}	Write Data Delay Time		60		50	ns
t_{HW}	Write Data Hold Time	30		20		ns
t_{ACC}	Read Access Time	140		76		ns
t_{PCS}	Processor Control Set-Up Time (RDY, $\overline{SO}$, $\overline{IRQ}$, $\overline{NMI}$, $\overline{RES}$)	60		40		ns
t_{DLY}	Delay Time ϕ_0 (IN) to ϕ_2 (OUT)		50		40	ns
$t_{DLY\,1}$	Delay Time ϕ_1 (OUT) to ϕ_2 (OUT)	-20	20	-20	20	ns

(Output Load Includes Scope and Jig Capacitance is 130pF)

■ TIMING CHART



■ PIN DESCRIPTION

• Clock Input (ϕ_0 (IN))

It is the input terminal to generate the system clock in the inside and input the reference clock from the outside. The operating frequency is between 4 and 8 MHz. And when ϕ_0(IN) stops at highlevel or lowlevel, the CPU becomes the stand-by mode.

• Clock Output (ϕ_1 (OUT), ϕ_2 (OUT))

The two signal ϕ_1 (OUT) or ϕ_2 (OUT) for the system-clock output. These are provided with each device for control bus synchronous signal. Phase relation ϕ_1 (OUT), ϕ_2 (OUT) are as shown in Fig. 1

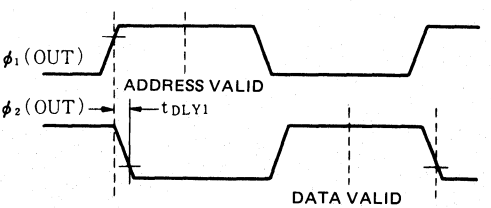


Fig. 1 Phase Relation by System-Clock ϕ_1 (OUT), ϕ_2 (OUT)

- **Address Bus ($A_0 \sim A_{15}$)**

$A_0 \sim A_{15}$ constitute a 16-bit address bus. The address that is indicated with these bits are hexadecimal $0000 ~ FFFF. (decimal 0 ~ 65535)

- **Data Bus ($D_0 \sim D_7$)**

$D_0 \sim D_7$ constitute the 8-bit bidirectional data bus, input or output.

- **Bus Direction Indicative Signal (R/W)**

It is the signal to decide the direction of data bus.
In reading (input data from other device to the CPU) "1" is output, and in writing (output data from the CPU to other) "0" is output. Read or write timing are as shown in Fig. 2, Fig. 3.

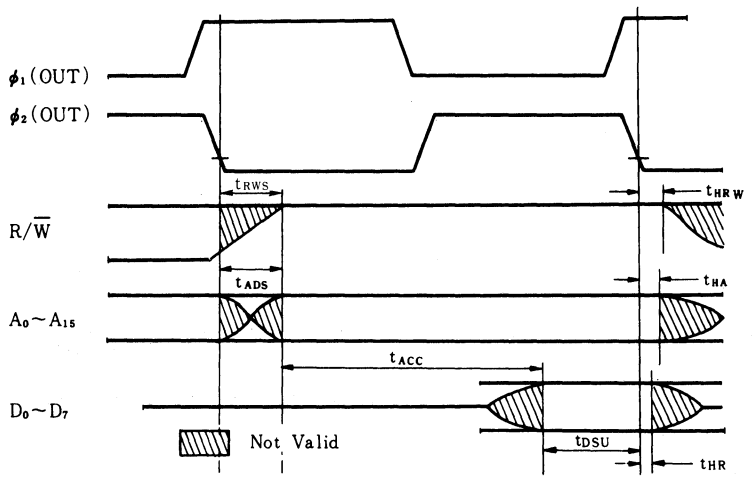


Fig. 2 Read Mode Timing

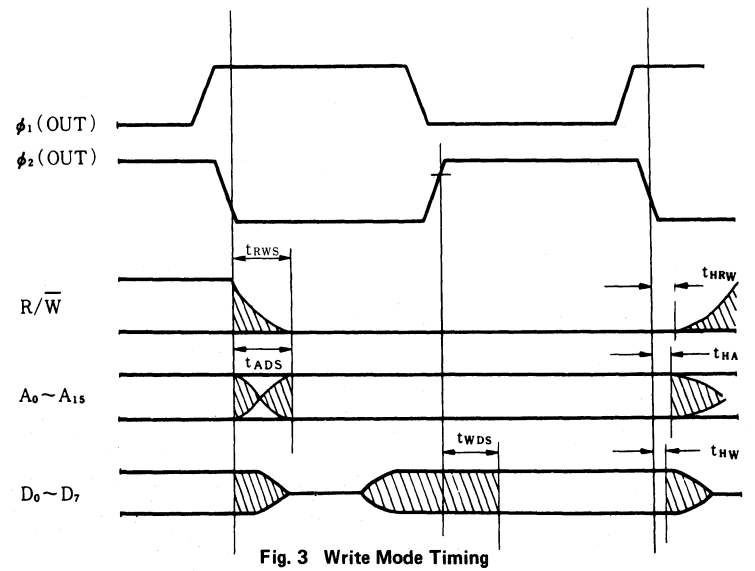


Fig. 3 Write Mode Timing

- Ready Signal (RDY)

This RDY input allows to single-step operation or stop on all cycles. When the falling edge of ϕ_2 (OUT) is detected, the CPU stop. When the CPU stop, the address line fetch the current address and when the operation is WRITE mode, the data bus fetch the current data. When the RDY input is low, the CPU becomes low-power mode.

- System Reset ($\overline{RES}$)

The input is used to reset the CPU in a power down state and to start. During that the input is Low level, READ/WRITE to the CPU is not all accepted. When the rising time signal of the pin is detected, the CPU becomes the reset mode at once.

After initial setting time of the 5 clock time, the interrupt mask flag is set, the CPU reads the vector address from each location (FFFC)(FFFD), and sets the program-counter.

The input consists of the Schmitt trigger circuit as which power on reset is acted by only CR.

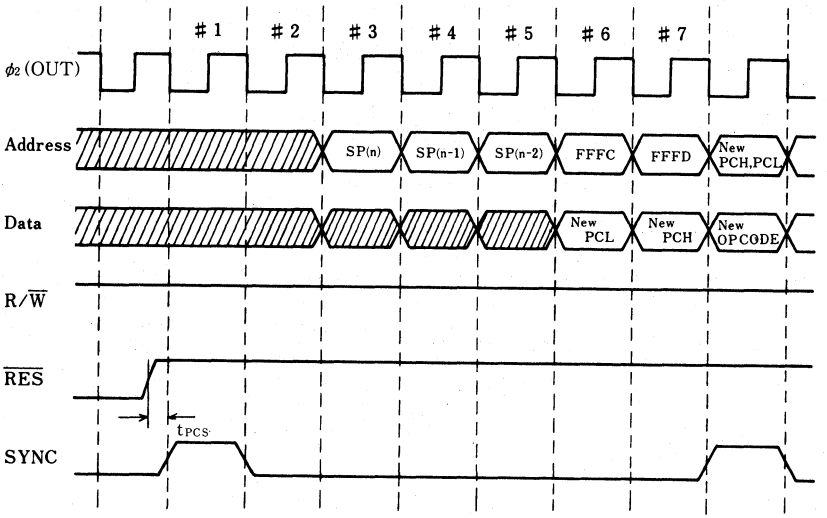


Fig. 4 Reset Mode Timing

- Interrupt Request Signal ($\overline{IRQ}$, $\overline{NMI}$)

$\overline{IRQ}$ (Interrupt Request)

If the TTL compatible input is the low level, the CPU starts the interrupt operation. When the instruction in execution is finished, the CPU allows the interrupt request, but at the same time, the interrupt mask bit in the status code register is checked, and if not set, the CPU begins the execution of the interrupt sequence. The program-counter and status register are loaded with stack, the interrupt mask flag is set so as not to accept any other interrupts. At the end of this cycle, the content of location FFFF load into high order 8-bit of program-counter, and the content of location FFFE load into low order 8-bit of program-counter. The program control is changed a memory vector which is stored these location.

To accept an interrupt, RDY signal should be high level. These are just same with all interruptions. When it is used to the wired OR with this pin, it must use a pullup resistor.

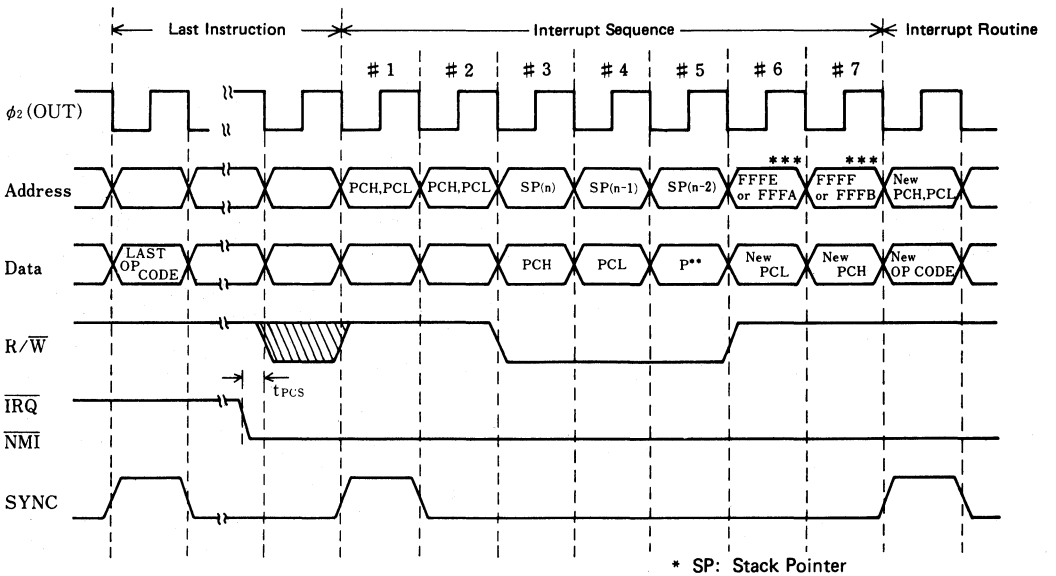
$\overline{NMI}$ (Nonmaskable Interrupt)

When the falling signal is input in pin, the CPU detects this edge, and starts the nonmaskable interrupt operation.

NMI is unconditional interrupt request. When the instruction in execution becomes end, the similar operation to IRQ is executed regardless of the state of interrupt mask flag.

In the vector address which is loaded to program-counter, high order 8-bit are contents of location FFFB, and low order 8-bit are contents of location FFFA. The program-counter changes to these addresses. When it uses the wired OR with this pin, it must use the pullup resistor.

$\overline{IRQ}$ and $\overline{NMI}$ are interrupt inputs of hardware which is sampled in the inside of the CPU during ϕ_2 time. After a instruction in execution comes at the end, it executes next interrupt routine from the first ϕ_1 time.



* SP: Stack Pointer
** P: Processor Status Register
*** Vector Address of $\overline{IRQ}$ FFFE/FFFF
Vector Address of $\overline{NMI}$ FFFA/FFFB

Fig. 5 Interrupt Operation Timing

Vector Address		Signal Names
MSB	LSB	
FFFF	FFFE	$\overline{IRQ}$
FFFD	FFFC	$\overline{RES}$
FFFB	FFFA	$\overline{NMI}$

- Overflow Flag Set Signal ($\overline{SO}$)

The overflow flag bit (V) in the status code register is set by the falling edge input to this pin. As this signal is sampled by the rising edge of ϕ_2 (OUT), the input must be synchronized outside.

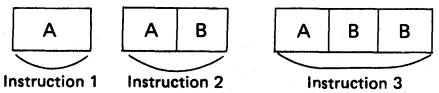
- Instruction Fetch Cycle Synchronous Signal (SYNC)

This output signal indicates the cycle that the CPU fetch the instruction code. It becomes "High Level" at the instruction is load and during the cycle time that SYNC is high level. During cycle time that SYNC is high level, if RDY input is set at the low level, the CPU halts with the state until RDY becomes high level.

The single step execution is enabled by control of RDY.

■ ADDRESSING MODE

The Fig. 6 shows a sample of pattern which machine language is stored in the memory. Generally the instruction consists of OP-code and operand (modifies the OP-code). The operand gives the information of address. Instruction 1 consists of the OP-code, and instruction 2 consists of the 1-byte OP-code and operand. Instruction 3 consists 1-byte OP-code, 2-byte operand. The CPU is informed the length of each instruction by the OP-code and is fetch the operand of the number of the required bytes by this information. The OP-code have the information which shows the kind of the operand. The kind of this operand is equivalent to the addressing mode.

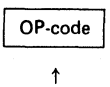


A : OP-code
B : Operand

Fig. 6 A Sample of Pattern which Machine Language is Stored in Memory

• Accumulator Addressing

This type includes the addressing in the single byte and is equivalent to the execution in the accumulator.

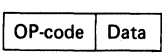


The execution on the accumulator.

Fig. 7 Accumlator

• Immediate Addressing

This type is 2-byte instructions having the OP-code and operand. The operand has not information of addressing, but describes the data itself.

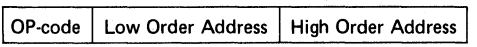


Address is not needed.

Fig. 8 Immediate

• Absolute Addressing

This type is 3-byte instruction (OP-code is 1-byte and operand is 2-byte). The 2-byte address indicates the low order, the third byte address the high order, all of 64 Kbytes is accessed.

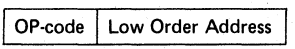


Describes directly the execution address.

Fig. 9 Absolute

• Zero Page Addressing

This type is 2-byte instruction of OP-code and operand. The high order address is automatically set "00". With addressing a low order address, it is able to code and the short of the execution. It is able to use efficiently the memory space and execute time by using the addressing suitably.

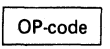


Execution high order address becomes "00".

Fig. 10 Zero Page

• Implied Addressing

The instruction code is 1-byte order. Almost all of the instruction control registers which is the internal memory equipment of the CPU, and needs no addressing.



Without address.

Fig. 11 Implied

• Indexed Zero Page Addressing

This is 2-byte instruction of OP-code and operand. It is called as "ZERO PAGE X" or "ZERO PAGE Y ' because the execution address is addressed with the indexed register (X or Y).

This is one of the zero page addressing. The high order addressing is set automatically "00", and low address is added with the content of the 2-byte. As the carry after the calculation is not added, the execute address does not exceed zero page.

OP-code	LOW Order Address

Execution High Order Address: 00
Execution Low Order Address:

Low Order Address	+	Index register (X or Y)

Neglect the carry.

Fig. 12 Z Page X; Z Page Y

- Indexed Absolute Addressing

This is 3-byte instruction of 1-byte OP-code, 2-byte operand. The execute addressing is addressed with the index (X or Y). It is called as "absolute X" or "absolute Y".
This is one of the absolute addressing. Execute address is added with the content of index register. The count of index and content of count are stored in the index register. And it is able to address the base address by the OP-code. It is able to modify the plural areas by using some base address and index, and the code and execution time can be shortened.

OP-code	Low Order Address	High Order Address

Execution address:

High Order Address	Low Order Address	+

Index Register (X or Y)

Fig. 13 ABS, X; ABS, Y

- Relative Addressing

This is 2-byte instruction of OP-code and operand. It is used only for the jump OP-code, and appoints the jump address, 2-byte oder of OP-code is called as "offset" and is added with the content of offset to the low oder 8-bit of program-counter set to the location of next instruction.
It has the range of −128 to +127-byte. The range of the branch is −128 to 127-byte from the head address of next instruction.

OP-code	Offset

Offset value is −128(80H) ~ +127(7FH)

Fig. 14 Relative

- Indexed Indirect Addressing

This is 2-byte instruction of OP-code and operand. As execute address is indirectly addressed, it is called as "Indirect X"
The execute address is added with 2-byte of instruction and content of X-register, and the carry is neglected. When the content of calculation is the address of Zero page the content stored in the address becomes the low order 8-bit of effective address, and the content of next address becomes the high order. The address of stored memory (high and low order) that appoints the effective address must be in the zero-page.
The content is stored in the address is low order 8-bit of effective address.

OP-code	Low Order Address

Execution Address Low Order:

00	Low Order Address + X register	content of address

Execution Address High Order:

00	Low Order Address + X register + 1	content of the address

Fig. 15 (IND, X)

- Indirect Indexed Addressing

This is 2-byte instruction of OP-code and operand. It is called as "Indirect, Y" as it appoints indirectly effective address. The 2-byte of OP-code shows the address of Zero page. The content of Y register is added with the content of memory, and the result becomes the low 8-bit of effective address. Carry is added to the content of next memory in the zero-page and it becomes the high order 8-bit of effective address.

OP-code	Low Order Address

Execution Address Low Order:

00	Low Order Address

Content of Address + Y register

Execution Address High Order:

00	Low Order Address + 1

Content of Address + Carry

Fig. 16 (IND), Y

- Indirect Addressing

This instruction is 2-byte of OP-code and operand. Execution address is address of Zero page.
Contents of this address becomes low order 8-bit of execution address, and contents of the next address becomes high order 8-bit of execution address. This is the same operation as in the ease of X being zero in "indirect, X".

OP-code	Low Order Address

Execution Address Low Order:

00	Low Order Address

content of address

Execution Address High Address:

00	Low Order Address + 1

content of address

Fig. 17 Indirect

- Indexed Absolute Indirect Addressing

This is 3-byte instruction (OP-code is 1-byte, operand is 2-byte). The result which adds the content of 2-byte or 3-byte to content of X register becomes the memory address that stores information of execution low order address 8-bit. The content of next address becomes high order 8-bit of the execution address.

OP-code	Low Order Address	High Order Address

Execution Address Low Order:

High Order Address	Low Order Address

+

X Register

Content of Address

Execution Address High Order:

High Order Address	Low Order Address

+

X Register

Next Memory data

Fig. 18 JMP (IND), X

- Absolute Indirect Addressing

The 2-byte of the instruction contains the low order 8-bit of a memory location. The high order 8-bit of that memory location are contained in the 3-byte of the instruction.
The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of effective address which is loaded into the 16-bit of the program counter.

OP-code	Low Order Address	High Order Address

Execution Address Low Order:

High Order Address	Low Order Address

Content of Address

Execution Address High Order:

High Order Address	Low Order Address

Next memory data

Fig. 19 JMP (IND)

- Bit Addressing

In the instruction set (BBR, BBS, RMB, SMB), OP-code corresponds to bit OP-code.
[BBR, BBS] This is 3-byte instruction (OP–code is 1-byte, operand is 2-byte). Execution address is zero page. Low order address is 2-byte of instruction.
3-byte of instruction is offset content which points the address of branching.

OP-code	Low Order Address	Offset

Execution Address:

00	Low Order Address

Fig. 20 BBR, BBS

[RMB, SMB] This is 2-byte instruction of OP-code, operand. Execution address is zero page, low order address is 2-byte of instruction.

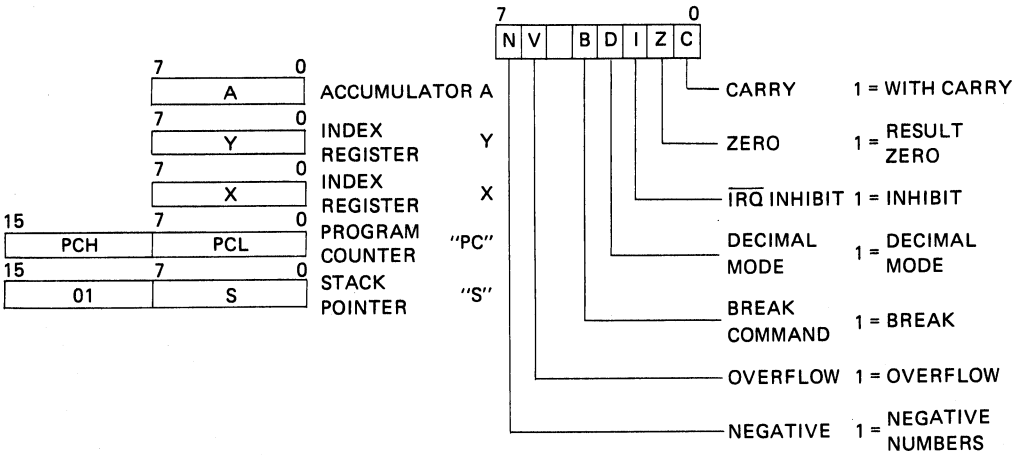
OP-code	Low Order Address

Execution Address:

00	Low Order Address

Fig. 21 RMB, SMB

■ INTERNAL REGISTER



■ INSTRUCTION SET (Alphabetical order)

(2)	A D C	Add memory and accumulator with carry
(2)	A N D	Logical AND memory and accumulator
	A S L	One bit left shift (memory or accumulator)
(1)	B B R	Branch if bit reset
(1)	B B S	Branch if bit is set
	B C C	Branch if carry is cleared
	B S C	Branch if carry is set
	B E Q	Branch if result is zero
(2)	B I T	Test memory bit with accumulator
	B M I	Branch if result is negative
	B N E	Branch if result is not zero
	B P L	Branch if result is positive
(1)	B R A	Unconditional branch
	B R K	Forced break
	B V C	Branch if overflow is cleared
	B V S	Branch if overflow is set
	C L C	Clear carry flag
	C L D	Clear decimal mode
	C L I	Clear disable interrupt
	C L V	Clear overflow flag
(2)	C M P	Compare memory with accumulator
	C P X	Compare memory with index register X
	C P Y	Compare memory with index register Y
(2)	D E C	Decrement memory
	D E X	Decrement index register X
	D E Y	Decrement index register Y
(2)	E O R	Exclusive OR memory or accumulator
(2)	I N C	Increment memory
	I N X	Increment index register X
	I N Y	Increment index register Y
(2)	J M P	Jump to new location
	J S R	Jump to new location, hold return address
(2)	L D A	Load memory into accumulator
	L D X	Load memory into index register X
	L D Y	Load memory into index register Y
	L S R	One bit right shift (memory or accumulator)
	N O P	No operation
(2)	O R A	Logical OR memory and accumulator
	P H A	Push accumulator on stack
	P H P	Push processer status on stack
(1)	P H X	Push X register on stack
(1)	P H Y	Push Y register on stack

	P L A	Pull accumulator from stack
	P L P	Pull processer status from stack
(1)	P L X	Pull X register from stack
(1)	P L Y	Pull Y register from stack
(1)	R M B	Reset memory bit
	R O L	Rotate left circular of one bit (memory or accumulator)
	R O R	Rotate right circular of one bit (memory or accumulator)
	R T I	Return from interrupt
	R T S	Return from subroutine
(2)	S B C	Subtract memory ar.d borrow from accumulator
	S E C	Set carry flag
	S E D	Set decimal
	S E I	Set disable interrupt ststus
(1)	S M B	Set memory bit
(2)	S T A	Store accumulator to memory
	S T X	Store index register X to memory
	S T Y	Store index register Y to memory
(1)	S T Z	Zero store
	T A X	Transfer accumulator to index register X
	T A Y	Transfer accumulator to index register Y
(1)	T R B	Test or reset bit
	T S B	Test or set bit
	T S X	Transfer stack pointer to accumulator
	T X A	Transfer index register to accumulator
	T X S	Transfer index register to stack pointer
	T Y A	Transfer index register to accumulator

Note (1): the instructions are newly designed in 65C02
(2): the instructions are added addressing in 65C02

■ INSTRUCTION SET (Matrix Map)

BRK Impied 1 7	— Operation Code — Addressing Mode — Bytes: Cycles

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK IMP 1 7	ORA (IND,X) 2 6			TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP IMP 1 3	ORA IMM 2 2	ASL ACC 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBS0 ZP 3 5**	0
1	BPL REL 2 2**	ORA (IND),Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP,X 2 4	ASL ZP,X 2 6	RMB1 ZP 2 5	CLC IMP 1 2	ORA ABS,Y 3 4*	INC ACC 1 2		TRB ABS 3 6	ORA ABS,X 3 4*	SAL ABS,X 3 6*	BBR1 ZP 3 5**	1
2	JSR ABS 3 6	AND (IND,X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP IMP 1 4	AND IMM 2 2	ROL ACC 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI REL 2 2**	AND (IND),Y 2 5*	AND (IND) 2 5		BIT ZP,X 2 4	AND ZP,X 2 4	ROL ZP,X 2 6	RMB3 ZP 2 5	SEC IMP 1 2	AND ABS,Y 3 4*	DEC ACC 1 2		BIT ABS,X 3 4*	AND ABS,X 3 4*	ROL ABS,X 3 6*	BBR3 ZP 3 5**	3
4	RTI IMP 1 6	EOR (IND,X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA IMP 1 3	EOR IMM 2 2	LSR ACC 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC REL 2 2**	EOR (IND),Y 2 5*	EOR (IND) 2 5			EOR ZP,X 2 4	LSR ZP,X 2 6	RMB5 ZP 2 5	CLI IMP 1 2	EOR ABS,Y 3 4*	PHY IMP 1 3			EOR ABS,X 3 4*	LSR ABS,X 3 6*	BBR5 ZP 3 5**	5
6	RTS IMP 1 6	ADC (IND,X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA IMP 1 4	ADC IMM 2 2†	ROR ACC 1 2		JMP IND 3 6	ADC ABS 3 4†	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS REL 2 2**	ADC (IND),Y 2 5*†	ADC (IND) 2 5†		STZ ZP,X 2 4	ADC ZP,X 2 4†	ROR ZP,X 2 6	RMB7 ZP 2 5	SEI IMP 1 2	ADC ABS,Y 3 4*†	PLY IMP 1 4		JMP (IND),X 3 6	ADC ABS,X 3 4*†	ROR ABS,X 3 6*	BBR7 ZP 3 5**	7
8	BRA REL 2 3	STA (IND,X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY IMP 1 2	BIT IMM 2 2	TXA IMP 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBR0 ZP 3 5**	8
9	BCC REL 2 2**	STA (IND),Y 2 6	STA (IND) 2 5		STY ZP,X 2 4	STA ZP,X 2 4	STX ZP,Y 2 4	SMB1 ZP 2 5	TYA IMP 1 2	STA ABS,Y 3 5	TXS IMP 1 2		STZ ABS 3 4	STA ABS,X 3 5	STZ ABS,X 3 5	BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND,X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY IMP 1 2	LDA IMM 2 2	TAX IMP 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS REL 2 2**	LDA (IND),Y 2 5*	LDA (IND) 2 5		LDY ZP,X 2 4	LDA ZP,X 2 4	LDX ZP,Y 2 4	SMB3 ZP 2 5	CLV IMP 1 2	LDA ABS,Y 3 4*	TSX IMP 1 2		LDY ABS,X 3 4*	LDA ABS,X 3 4*	LDX ABS,Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND,X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY IMP 1 2	CMP IMM 2 2	DEX IMP 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE REL 2 2**	CMP (IND),Y 2 5*	CMP (IND) 2 5			CMP ZP,X 2 4	DEC ZP,X 2 6	SMB5 ZP 2 5	CLD IMP 1 2	CMP ABS,Y 3 4*	PHX IMP 1 3			CMP ABS,X 3 4*	DEC ABS,X 3 6*	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND,X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INX IMP 1 2	SBC IMM 2 2†	NOP IMP 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ REL 2 2**	SBC (IND),Y 2 5*†	SBC (IND) 2 5†			SBC ZP,X 2 4†	INC ZP,X 2 6	SMB7 ZP 2 5	SED IMP 1 2	SBC ABS,Y 3 4*†	PLX IMP 1 4			SBC ABS,X 3 4*†	INC ABS,X 3 6*	BBS7 ZP 3 5**	F

† Cycles Add 1 when decimal mode

* Cycles Add 1 when page crossing occurs

** Cycles Add 1 when branch in same page
Add 2 when branch in different page

Newly Designed Instruction

■ INSTRUCTION SET

ADDRESSING

MNEMOMC	OPERATION	IMMEDIATE			ABSOLUTE			ZEROPAGE			ACCUM			IMPLIED			(IND. X)			(IND). Y		
		op	n	0	op	n	0	op	n	0	op	n	0	op	n	0	op	n	0	op	n	0
ADC	A+M+C→A (1)(5)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2
AND	A∧M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2
ASL	C←[7 0]←0 (1)				0E	6	3	06	5	2	0A	2	1									
BBR(#0-7)	Branch on Mb=0							–	5	3												
BBS(#0-7)	Branch on Mb=1							–	5	3												
BCC	Branch on C=0 (2)																					
BCS	Branch on C=1 (2)																					
BEQ	Branch on Z=1 (2)																					
BIT	A∧M (6)	89	2	2	2C	4	3	24	3	2												
BMI	Branch on N=1 (2)																					
BNE	Branch on Z=0 (2)																					
BPL	Branch on N=0 (2)																					
BRA	Branch Allways (2)																					
BRK	Break													00	7	1						
BVC	Branch on V=0 (2)																					
BVS	Branch on V=1 (2)																					
CLC	0→C													18	2	1						
CLD	0→D													D8	2	1						
CLI	0→I													58	2	1						
CLV	0→V													B8	2	1						
CMP	A−M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2
CPX	X−M	E0	2	2	EC	4	3	E4	3	2												
CPY	Y−M	C0	2	2	CC	4	3	C4	3	2												
DEC	M−1→M (1)				CE	6	3	C6	5	2	3A	2	1									
DEX	X−1→X													CA	2	1						
DEY	Y−1→Y													88	2	1						
EOR	V∨M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2
INC	M+1→M (1)				EE	6	3	E6	5	2	1A	2	1									
INX	X+1→X													E8	2	1						
INY	Y+1→Y													C8	2	1						
JMP	Jumo to New Loc				4C	3	3										7C	6	3			
JSR	Jump Sub				20	6	3															
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2												
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2												
LSR	0→[7 0]→C (1)				4E	6	3	46	5	2	4A	2	1									
NOP	No Operation													EA	2	1						
ORA	A∨M→A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2
PHA	A→Ms S−1→S													48	3	1						
PHP	P→Ms S−1→S													08	3	1						
PHX	X→Ms S−1→S													DA	3	1						
PHY	Y→Ms S−1→S													5A	3	1						
PLA	S+1→S Ms→A													68	4	1						
PLP	S+1→S Ms→P													28	4	1						
PLX	S+1→S Ms→X													FA	4	1						
PLY	S+1→S Ms→Y													7A	4	1						
RMB(#0-7)	0→Mb (4)							–	5	2												
ROL	[7 0]←[C] (1)				2E	6	3	26	5	2	2A	2	1									
ROR	[C]→[7 0] (1)				6E	6	3	66	5	2	6A	2	1									
RTI	Rtrn Int													40	6	1						
RTS	Rtrn Sub													60	6	1						
SBC	A−M−C→A (1)(5)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2
SEC	1→C													38	2	1						
SED	1→D													F8	2	1						
SEI	1→I													78	2	1						
SMB(#0-7)	1→Mg (4)							–	5	2												
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2
STX	X→M				8E	4	3	86	3	2												
STY	Y→M				8C	4	3	84	3	2												
STZ	0→M				9C	4	3	64	3	2												
TAX	A→X													AA	2	1						
TAY	A→Y													A8	2	1						
TRB	A∧M→M				1C	6	3	14	5	2												
TSB	A∨M→M				0C	6	3	04	5	2												
TSX	S→X													BA	2	1						
TXA	X→A													8A	2	1						
TXS	X→S													9A	2	1						
TYA	Y→A													98	2	1						

(Symbol Description)
X: Index X
Y: Index Y
A: Accumulator
M: Designated Memory with Effective Address
Ms: Designated Memory with Stack pointer
Mb: Zero page Memory Bit
M_7: Memory Bit 7
M_6: Memory Bit 6
+: Add
−: Subtract
∧: Logical AND
∨: Logical OR
∀: Exclusive OR
n: Machine Cycles
#: Bytes

MODE

ZPAGE, X			ZPAGE, Y			ABS, X			ABS, Y			RELATIVE			INDIRECT			BIT ADDRESSING(OP BY BIT 0)								PROCESSOR STATUS CODES						
op	n	0	op	n	0	op	n	0	op	n	0	op	n	0	op	n	0	0	1	2	3	4	5	6	7	7	6	5	4	3	2	1	0
																										N	V	·	B	D	I	Z	C
75	4	2				7D	4	3	79	4	3				72	5	2									N	V	·	·	·	·	Z	C
35	4	2				3D	4	3	39	4	3				32	5	2									N	·	·	·	·	·	Z	·
16	6	2				1E	6	3																		N	·	·	·	·	·	Z	C
																		0F	1F	2F	3F	4F	5F	6F	7F	·	·	·	·	·	·	·	·
																		8F	9F	AF	BF	CF	DF	EF	FF	·	·	·	·	·	·	·	·
												90	2	2												·	·	·	·	·	·	·	·
												B0	2	2												·	·	·	·	·	·	·	·
												F0	2	2												·	·	·	·	·	·	·	·
34	4	2				3C	4	3																		M_7	M_6	·	·	·	·	Z	·
												30	2	2												·	·	·	·	·	·	·	·
												D0	2	2												·	·	·	·	·	·	·	·
												10	2	2												·	·	·	·	·	·	·	·
												80	3	2												·	·	·	·	·	·	·	·
																										·	·	·	·	1	·	1	·	·
												50	2	2												·	·	·	·	·	·	·	·
												70	2	2												·	·	·	·	·	·	·	·
																										·	·	·	·	·	·	·	0
																										·	·	·	·	0	·	·	·
																										·	·	·	·	·	0	·	·
																										·	0	·	·	·	·	·	·
D5	4	2				DD	4	3	D9	4	3				D2	5	2									N	·	·	·	·	·	Z	C
																										N	·	·	·	·	·	Z	C
																										N	·	·	·	·	·	Z	C
D6	6	2				DE	6	3																		N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
55	4	2				5D	4	3	59	4	3				52	5	2									N	·	·	·	·	·	Z	·
F6	6	2				FE	6	3																		N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
															6C	5	3									·	·	·	·	·	·	·	·
B5	4	2				BD	4	3	B9	4	3				B2	5	2									N	·	·	·	·	·	Z	·
			B6	4	2				BE	4	3															N	·	·	·	·	·	Z	·
B4	4	2				BC	4	3																		N	·	·	·	·	·	Z	·
56	6	2				5E	6	3																		0	·	·	·	·	·	Z	C
																										·	·	·	·	·	·	·	·
15	4	2				1D	4	3	19	4	3				12	5	2									N	·	·	·	·	·	Z	·
																										·	·	·	·	·	·	·	·
																										·	·	·	·	·	·	·	·
																										·	·	·	·	·	·	·	·
																										·	·	·	·	·	·	·	·
																										N	·	·	·	·	·	Z	·
																													(Restored)				
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																		07	17	27	37	47	57	67	77	·	·	·	·	·	·	·	·
36	6	2				3E	6	3																		N	·	·	·	·	·	Z	C
76	6	2				7E	6	3																		N	·	·	·	·	·	Z	C
																													(Restored)				
																										·	·	·	·	·	·	·	·
F5	4	2				FD	4	3	F9	4	3				F2	5	2									N	V	·	·	·	·	Z	(3)
																										·	·	·	·	1	·	·	1
																										·	·	·	·	·	1	·	·
																		87	97	A7	B7	C7	D7	E7	F7	·	·	·	·	·	·	·	·
95	4	2				9D	3	3	99	5	3				92	5	2									·	·	·	·	·	·	·	·
			96	4	2																					·	·	·	·	·	·	·	·
94	4	2																								·	·	·	·	·	·	·	·
74	4	2				9E	3	3																		·	·	·	·	·	·	·	·
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										·	·	·	·	·	·	Z	·
																										·	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										·	·	·	·	·	·	·	·
																										N	·	·	·	·	·	Z	·

NOTE (1) Add 1 to "N" when machine cycles or zero page crossing.
(2) Add 1 to "N" when branch in same page. Add 2 to "N" when branch in different page.
(3) Not carry = borrow
(4) Effect when zero page address.
(5) Add 1 when decimal mode.
(6) When the BIT (IMM mode), not related to M_7 or M_6 bit (N, V flag) of register P.

■ Instruction Description (Alphabetical Order)

Description of symbol using in list

A	Accumulator	−	Subtract
X, Y	Index Register	∀	Exclusive OR
M	Memory	→	Transfer
P	Processor Status Register	←	Transfer
S	Stack Pointer	V	Logical OR
Ms	Stack Memory	PCH	Program Counter High
Mb	Memory Bit	PCL	Program Counter Low
+	Add		
	Logical AND		

ADC Add with carry of memory and accumulator.
Operation: A+M+C → A
"P" Register: N, V, Z, C

AND Logical AND of memory and accumulator. The result is stored in accumulator.
Operation: A M → A
"P" Register: N, Z

ASL One bit left shift. LSB is placed "0". Contents of MSB is placed C.
Operation: C ← [7|6|5|4|3|2|1|0] ← "0"
"P" Register: N, Z, C

BBR If specific bit of zero page is a reset state, branch relatively.

OP-Code	Low Order Address	Offset

3-byte instruction
If the specific bit (a bit is decided on the instruction code) of effective address [00 | Low Order Address] is a reset state, relative branch by the Offset value on the basis of lead address of next instruction.
Operation: branch when $M_b = 0$
"P" Register: Not affected

BBS If specific bit of zero page is a set state, branch relatively.

OP-code	Low Order Address	Offset

3-byte instruction
If the specific bit (a bit is decided on the instruction code) of effective address [00 | Low Order Address] is a set state, relative branch by the [Offset] value to base with lead address of next instruction.
Operation: branch when $M_b = 1$
"P" Register: Not affected

BCC Branch if the carry is reset.
Operation: branch when C = 0
"P" Register: Not affected

BCS Branch if the carry is set.
Operation: branch when C = 1
"P" Register: Not affected

BEQ Branch if the zero flag is set.
Operation: branch when Z = 1
"P" Register: Not affected

BIT Test the memory bit by the accumulator.
Operation: A M, M_7 → N, M_6 → V
The bit 6 and bit 7 of the memory are transferred to "P" Register.
If the result of A M is zero, Z = 1
"P" Register: N, V, Z
$(M_7)(M_6)$

BMI Branch if result is negative.
Operation: branch when N = 1
"P" Register: Not affected

BNE Branch if result is not zero.
Operation: branch when Z = 0
"P" Register: Not affected

BPL Branch if result is positive.
Branch if result is positive.
Operation: branch when N ≠ 0
"P" Register: Not affected

BRA Unconditional branch.
"P" Register: Not affected

BRK Forced break

Operation: Execute the interrupt. In this instruction, a lead address (2-byte) of next instruction is stored in the stack. At the same time, it is stored into contents of "P" Register. Program-counter (FFFE) → PCL, (FFFF) → PCH, and Execution of program is same vector address with IRQ. The difference from the IRQ interrupt is that in the BKK operation, the B flag of "P" register is set "1" and can't mask by the I flag.

"P" Register: $\frac{B}{1}$

BVC Branch if the overflow flag is reset.

Operation: branch when V = 0

"P" Register: Not affected

BVS Branch if the overflow flag is set.

Operation: branch when V = 1

"P" Register: Not affected

CLC Clear the carry flag (C).

Operation: 0 → C

"P" Register: $\frac{C}{0}$

CLD Clear the decimal mode.

Operation: 0 → C

"P" Register: $\frac{D}{0}$

CLI Clear the interrupt disenable flag (I).

Operation: 0 → I

"P" Register: $\frac{V}{0}$

CLV Clear overflow flag.

Operation: 0 → V

"P" Register: $\frac{V}{0}$

CMP Compare memory with accumulator.

Operation: A-M

The result is not stored. If it is negative, N flag is set 1. If it is positive, C flag is set 1. And if it is zero, Z and C flags are respectively 1.

"P" Register: N, Z, C

CPX Compare memory with the index registerX.

Operation: Y-M

Flag condition of "P" Register is the same as CMP.

"P" Register: N, Z, C

CPY Compare memory with the index register Y.

Operation: Y-M

Flag condition of "P" Register is the same as CMP.

"P" Register: N, Z, C

DEC Decrement the contents of memory.

Operation: M−1 → M

"P" Register: N, Z

DEX Decrement the contents of index register X.

Operation: X−1 → X

"P" Register: N, Z

DEY Decrement the contents of index register Y.

Operation: Y−1 → Y

"P" Register: N, Z

EOR Execute the exclusive OR of memory and accumulator

Operation: A M → A

"P" Register: N, Z

INC Increment the contents of memory.

Operation: M+1 → M

"P" Register: N, Z

INY Increment the contents of index register Y.

Operation: Y+1 → Y

"P" Register: N, Z

JMP Execution of program jumps to designation address.

Operation:

OP-Code	Operand	Operand

The designation address by operands with 2-bytes is placed in PCL and PCH.

"P" Register: Not affected

JSR The execution of program jumps to designation address.

Operation: When jump to designation address, return address (lead address of next instruction) is stored into stack. The return is executed by RTS.

OP-Code	Operand	Operand

The disignation address by operands with 2-bytes is stored into the PCL and PCH.

Lead address of next instruction (2-byte)

→ Ms, S−1 → S

→ Ms, S−1 → S "P" Register: Not affected

LDA Load the contents of memory to the accumulator.
Operation: M → A "P" Register: N, Z

LDX Load the contents of memory to index register X.
Operation: M → X
"P" Register: N, Z

LDY Load the contents of memory to index register Y.
Operation: M → Y
"P" Register: N, Z

LSR One bit right shift. MSB (7 bit) is placed to 0, LSB (0 bit) is loaded the C.
Operation: 0 → [7|6|5|4|3|2|1|0] → C
"P" Register: N 0, Z, C

NOP No-operation
Operation: No operation
"P" Register: Not affected

ORA Logical OR of memory and accumulator. The result is stored into the accumulator.
Operation: A M → A
"P" Register: N, Z

PHA Store the contents of the accumulator into the memory stack.
Operation: A → Ms, S−1 → S
"P" Register: Not affected

PHP Store the contents of the register P into the stack.
Operation: P → Ms, S−1 → S
"P" Register: Not affected

PHX Store the contents of the index register X into the stack.
Operation: X → Ms, S−1 → S
"P" Register: Not affected

PHY Store the contents of the index register Y into the stack.
Operation: Y → Ms, S−1 → S
"P" Register: Not affected

PLA Pull accumulator from stack.
Operaton: Ms → A, S + 1 → S
"P" Register: N, Z

PLP Pull processer status from stack.
Operation: Ms → P, S + 1 → S
"P" Register: Restore

PLX Pull X register from stack.
Operation: Ms → X, S + 1 → S
"P" Register: N, Z

PLY Pull Y register from stack.
Operation: Ms → Y, S + 1 → S
"P" Register: N, Z

RMB Reset the specific bit in the zero page address.
[OP-Code | Low Order Bit] 2-byte instruction
The specific bit (a bit is decided by the instruction code) of execution address [00 | Low Order Address] is reset.
Operation: 0 → M_b
"P" Register: Not affected

ROL Rotate left circular of one bit. The contents of the MSB are moved into the C, the contents of the C are moved into the LSB.
Operation: [7|6|5|4|3|2|1|0] → C
"P" Register: N, Z, C

ROR Rotate right circular of one bit. The contents of the C are moved into the MSB, the contents of the LSB are moved into the C.
Operation: [7|6|5|4|3|2|1|0] → C
"P" Register: N, Z, C

RTI Return from interrupt. The return address in stack is loaded into the program counter, and it becomes the lead address of a next instruction of the interrupt.
Operation: Ms → P, S + 1 → S
Ms → PCL, S + 1 → S
Ms → PCH, S + 1 → S
"P" Register: Restore

RTS Return from subroutine.
The return address in stack is loaded into the program counter. It becomes the lead address of a next instruction of the JSR.
Operation: Ms → PCL, S + 1 → S
Ms → PCH, S + 1 → S
"P" Register: Not affected

SBC Subtract memory and borrow from accumulator, and the result is stored into the accumulator.
Operation: $A - M - C \rightarrow A$
C = borrow
"P" Register: N, V, Z, C

SEC Set carry flag.
Operation: $1 \rightarrow C$
"P" Register: $\overset{C}{1}$

SED Set decimal flag.
Operation: $1 \rightarrow D$
"P" Register: $\overset{D}{1}$

SEI Set disable interrupt status.
Operation: $1 \rightarrow I$
"P" Register: $\overset{I}{1}$

SMB Set the specific bit of zero page address.

OP-Code	Low Order Bit

2-byte instruction
It sets the specific bit (a bit is decided on the instruction code) of effective address

00	Low Order Address

Operation: $1 \rightarrow M_b$
"P" Register: Not affected

STA Store the contents of the accumulator into the memory.
Operation: $A \rightarrow M$
"P" Register: Not affected

STX Store the contents of the index register X into the memory.
Operation: $X \rightarrow M$
"P" Register: Not affected

STY Store the contents of the index register Y into the memory.
Operation: $Y \rightarrow M$
"P" Register: Not affected

STZ Clear the contents of memory.
Operation: $0 \rightarrow M$
"P" Register: Not Affected

TAX Transfer the contents of the accumulator to the index register X.
Operation: $A \rightarrow M$
"P" Register: N, Z

TAY Transfer the contents of the accumulator to the index register Y.
Operation: $A \rightarrow Y$
"P" Register: N, Z

TRB Reset the contents of memory by accumulator, and test at the same time.
Operation: $\overline{A} \wedge M \rightarrow M$
If the result is zero, Z flag = 1
"P" Register: Z

TSB Set the contents of memory by accumulator, and test at the same time.
Operation: $A \vee M \rightarrow M$
If the result is zero, Z flag = 1
"P" Register: Z

TSX Transfer stack pointer to the index register X.
Operation: $S \rightarrow X$
"P" Register: N, Z

TXA Transfer the contents of the index register X to the accumulator.
Operation: $X \rightarrow A$
"P" Register: N, Z

TXS Transfer the contents of the index register X to stack pointer.
Operation: $X \rightarrow S$
"P" Register: Not affected

TYA Transfer the contents of the index register Y to the accumulator.
Operation: $Y \rightarrow A$
"P" Register: N, Z

■ DETAILED INSTRUCTION OPERATION

ADDRESS MODE	CYCLE	ADDRESS BUS	DATA BUS	R/$\overline{W}$
1 Immediate IMM	1	PC	OP CODE	1
LDA(A9), AND(29), ORA(09), EOR(49), CMP(C9),	2	PC+1	ID	1
BIT(89), ADC(69), SBC(E9), LDX(A2), LDY(A0),	(1)2a	PC+2	IO	1
CPX(E0), CPY(C0)				
2a Absolute ABS	1	PC	OP CODE	1
	2	PC+1	AAL	1
LDA(AD), STA(8D), ADC(6D), SBC(ED), AND(2D),	3	PC+2	AAH	1
ORA(0D), EOR(4D), CMP(CD), BIT(2C), LDX(AE),	4	AA	DATA	1/0
LDY(AC), STX(8E), STY(8C), CPX(EC), CPY(CC),	(1)4a	PC+3	IO	1
STZ(9C)				
2b Absolute (R-M-W) ABS	1	PC	OP CODE	1
TRB(1C), TSB(0C), LSR(4E), ASL(0E), ROL(2E),	2	PC+1	AAL	1
ROR(6E), INC(EE), DEC(CE)	3	PC+2	AAH	1
	4	AA	DATA	1
	5	AA	IO	1
	6	AA	DATA	0
2c Absolute (JUMP) ABS	1	PC	OP CODE	1
JMP(4C)	2	PC+1	PCL	1
	3	PC+2	PCH	1
	1	NEW PC	OP CODE	1
2d Absolute (Jump to subroutine) ABS	1	PC	OP CODE	1
JSR(20)	2	PC+1	NEW PCL	1
	3	01,S	IO	1
	4	01,S	PCH	0
	5	01,S−1	PCL+2	0
	6	PC+2	NEW PCH	1
	1	NEW PC	OP CODE	1
3a Zero Page ZP	1	PC	OP CODE	1
LDA(A5), STA(85), ADC(65), SBC(E5), AND(25),	2	PC+1	BAL	1
ORA(05), EOR(45), CMP(C5), BIT(24), LDX(A6),	3	00,BAL	DATA	1/0
LDY(A4), STX(86), STY(84), CPX(E4), CPY(C4),	(1)3a	PC+2	IO	1
STZ(64)				
3b Zero Page (R-M-W) ZP	1	PC	OP CODE	1
TRB(14), TSB(04), LSR(46), ASL(06), ROL(26),	2	PC+1	BAL	1
ROR(66), INC(E6), DEC(C6)	3	00,BAL	DATA	1
	4	00,BAL	IO	1
	5	00,BAL	DATA	0

ADDRESS MODE	CYCLE	ADDRESS BUS	DATA BUS	R/$\overline{W}$
4 Accumulator ACC	1	PC	OP CODE	1
LSR(4A), ASL(0A), ROL(2A), ROR(6A), INC(1A), DEC(3A)	2	PC+1	IO	1
5a Implied IMP	1	PC	OP CODE	1
SEC(38), CLC(18), SEI(78), CLI(58), SED(F8), CLD(D8), CLV(B8), NOP(EA), INX(E8), INY(C8), DEX(CA), DEY(88), TAX(AA), TXA(8A), TAY(A8), TYA(98), TSX(BA), TXS(9A)	2	PC+1	IO	1
5b Implied (Stack Push) IMP	1	PC	OP CODE	1
PHA(48), PHP(08), PHX(DA), PHY(5A)	2	PC+1	IO	1
	3	01,S	REG	0
5c Implied (Stack Pull) IMP	1	PC	OP CODE	1
PLA(68), PLP(28), PLX(FA), PLY(7A)	2	PC+1	IO	1
	3	01,S	IO	1
	4	01,S+1	REG	1
5d Implied (Return from subroutine) IMP	1	PC	OP CODE	1
RTS(60)	2	PC+1	IO	1
	3	01,S	IO	1
	4	01,S+1	NEW PCL	1
	5	01,S+2	NEW PCH	1
	6	NEW PC	IO	1
	1	PC+1	OP CODE	1
5e Implied (Return from interrupt) IMP	1	PC	OP CODE	1
RTI(40)	2	PC+1	IO	1
	3	01,S	IO	1
	4	01,S+1	P	1
	5	01,S+2	NEW PCL	1
	6	01,S+3	NEW PCH	1
	1	NEW PC	OP CODE	1
5f Implied (Interrupt) IMP	1	PC	OP CODE	1
BRK(00), $\overline{RES}$, $\overline{IRQ}$, $\overline{NMI}$	2	PC**	IO	1
	3	01,S	PCH	1/0*
	4	01,S−1	PCL***	1/0*
	5	01,S−2	P	1/0*
	6	VA	AAVL	1
* RESET: "1"	7	VA+1	AAVH	1
** BRK: PC + 1	1	AAV	OP CODE	1
*** BRK: PCL + 2				

ADDRESS MODE	CYCLE	ADDRESS BUS	DATA BUS	R/W
6 Indexed Indirect (IND, X)	1	PC	OP CODE	1
LDA(A1), STA(81), ADC(61), SBC(E1), AND(21),	2	PC+1	BAL	1
ORA(01), EOR(41), CMP(C1)	3	PC+1	IO	1
	4	00,BAL+X	AAL	1
	5	00,BAL+X+1	AAH	1
	6	AA	DATA	1/0
	(1)6a	PC+2	IO	1
7 Indirect Index (IND), Y	1	PC	OP CODE	1
LDA(B1), STA(91), ADC(71), SBC(F1), AND(31),	2	PC+1	IAL	1
ORA(11), EOR(51), CMP(D1)	3	00,IAL	AAL	1
	4	00,IAL+1	AAH	1
	(4)(2)4a	00,IAL+1	IO	1
	5	AA+Y	DATA	1/0
	(1)5a	PC+2	IO	1
8a Zero Page Index X ZP, X	1	PC	OP CODE	1
LDA(B5), STA(95), ADC(75), SBC(F5), AND(35),	2	PC+1	BAL	1
ORA(15), EOR(55), CMP(D5), BIT(34), LDY(B4),	3	PC+1	IO	1
STY(94), STZ(74)	4	00,BAL+X	DATA	1/0
	(1)4a	PC+2	IO	1
8b Zero Page Index X (R-M-W) ZP, X	1	PC	OP CODE	1
LSR(56), ASL(16), ROL(36), ROR(76), INC(F6),	2	PC+1	BAL	1
DEC(D6)	3	PC+1	IO	1
	4	00,BAL+X	DATA	1
	5	00,BAL+X	IO	1
	6	00,BAL+X	DATA	0
9 Zero Page Index Y ZP, Y	1	PC	OP CODE	1
LDX(B6), STX(96)	2	PC+1	BAL	1
	3	PC+1	IO	1
	4	00,BAL+Y	DATA	1/0
10a Absolute Index X ABS, X	1	PC	OP CODE	1
LDA(BD), STA(9D), ADC(7D), SBC(FD), AND(3D),	2	PC+1	AAL	1
ORA(1D), EOR(5D), CMP(DD), BIT(3C), LDY(BC),	3	PC+2	AAH	1
STZ(9E)	(4)(2)3a	PC+2	IO	1
	4	AA+X	DATA	1/0
	(1)4a	PC+3	IO	1

ADDRESS MODE	CYCLE	ADDRESS BUS	DATA BUS	R/$\overline{W}$
10b Absolute Index X (R-M-W) ABS, X	1	PC	OP CODE	1
LSR(5E), ASL(1E), ROL(3E), ROR(7E), INC(FE),	2	PC+1	AAL	1
DEC(DE)	3	PC+2	AAH	1
	(2)3a	PC+2	IO	1
	4	AA+X	DATA	1
	5	AA+X	IO	1
	5	AA+X	DATA	0
11 Absolute Index Y ABS, Y	1	PC	OP CODE	1
LDA(B9), STA(99), ADC(79), SBC(F9), AND(39),	2	PC+1	AAL	1
ORA(19), EOR(59), CMP(D9), LDX(BE)	3	PC+2	AAH	1
	(4)(2)3a	PC+2	IO	1
	4	AA+Y	DATA	1/0
	(1)4a	PC+3	IO	1
12 Relative REL	1	PC	OP CODE	1
BMI(30), BPL(10), BCC(90), BCS(B0), BEQ(F0),	2	PC+1	off	1
BNE(D0), BVS(70), BVC(50), BRA(80)	(3)2a	PC+2	IO	1
	(2)2b	PC+2	IO	1
	(5)1	PC+2+(off)	OP CODE	1
13 Indirect IND	1	PC	OP CODE	1
LDA(B2), STA(92), ADC(72), SBC(F2), AND(32),	2	PC+1	IAL	1
ORA(12), EOR(52), CMP(D2)	3	00,IAL	AAL	1
	4	00,IAL+1	AAH	1
	5	AA	DATA	1/0
	(1)5a	PC+2	IO	1
14 Absolute Indirect (IND)	1	PC	OP CODE	1
JMP(6C)	2	PC+1	AAL	1
	3	PC+2	AAH	1
	4	PC+2	IO	1
	5	AA	PCL	1
	6	AA+1	PCH	1
	1	NEW PC	OP CODE	1
15 Absolute Indexed Indirect (IND), X	1	PC	OP CODE	1
JMP(7C)	2	PC+1	AAL	1
	3	PC+2	AAH	1
	4	PC+2	IO	1
	5	AA+X	PCL	1
	6	AA+X+1	PCH	1
	1	NEW PC	OP CODE	1

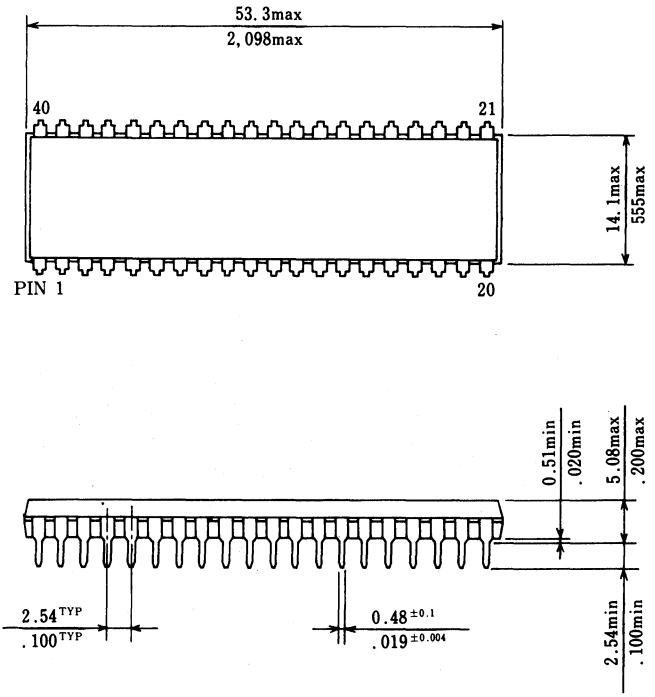
ADDRESS MODE	CYCLE	ADDRESS BUS	DATA BUS	R/$\overline{W}$
16a Bit Addressing (R-M-W)	1	PC	OP CODE	1
RMB(07~77), SMB(87~F7)	2	PC+1	BAL	1
	3	00,BAL	DATA	1
	4	00,BAL	IO	1
	5	00,BAL	DATA	0
16b Bit Addressing (Branch)	1	PC	OP CODE	1
BBR(0F~7F), BBS(8F~FF)	2	PC+1	BAL	1
	3	00,BAL	DATA	1
	4	00,BAL	IO	1
	5	PC+2	off	1
	5a	PC+3	IO	1
	5b	PC+3	IO	1
	1	PC+3+off	OP CODE	1

ABBREVIATIONS

AA	Absolute Address	–L	Lower 8 bit Address
IO	Internal Operation	ID	Immediate Data
REG	Data of Each Register (ACC, X, Y, P)	DATA	Memory Data
PC	Program Counter	BAL	Base Address (Low)
S	Stack Address	off	Off-Set Data
VA	Vector Address	IA	Indirect Address
AAV	Absolute Address Vector	X, Y	Index Register
P	Processor Status Register	R-M-W	Read-Modify-Write
–H	Higher 8 bit Address		

NOTE: (1) Add 1 cycle if decimal mode of ADC, SBC
(2) Add 1 cycle if page boundary is crossed
(3) Add 1 cycle if branch is taken
(4) Add 1 cycle for write
(5) PC+2 if branch is not taken

■ 40-PIN DUAL-IN-LINE PACKAGE (UNIT: $\frac{\text{mm}}{\text{inch}}$)



5. DSP

RICOH

Digital Signal Processor

RP5C72

The RP5C72 is a high-performance general-purpose digital signal processor (DSP). Its 32-bit internal operation includes a 512-word data RAM (1 word = 16 bits), 4k-word ROM (1 word = 16 bits) that can be assigned to both program and data areas, and a 32-bit multiplier (16 × 16 bits, fixed point operation). It processes at 100 ns per instruction.

The index function of the memory has two sets of hardware (index units) that contain ALUs dedicated to addressing, enabling operations required for various digital signal processing.

By changing software in the built-in program memory, the RP5C72 can be adapted to various applications.

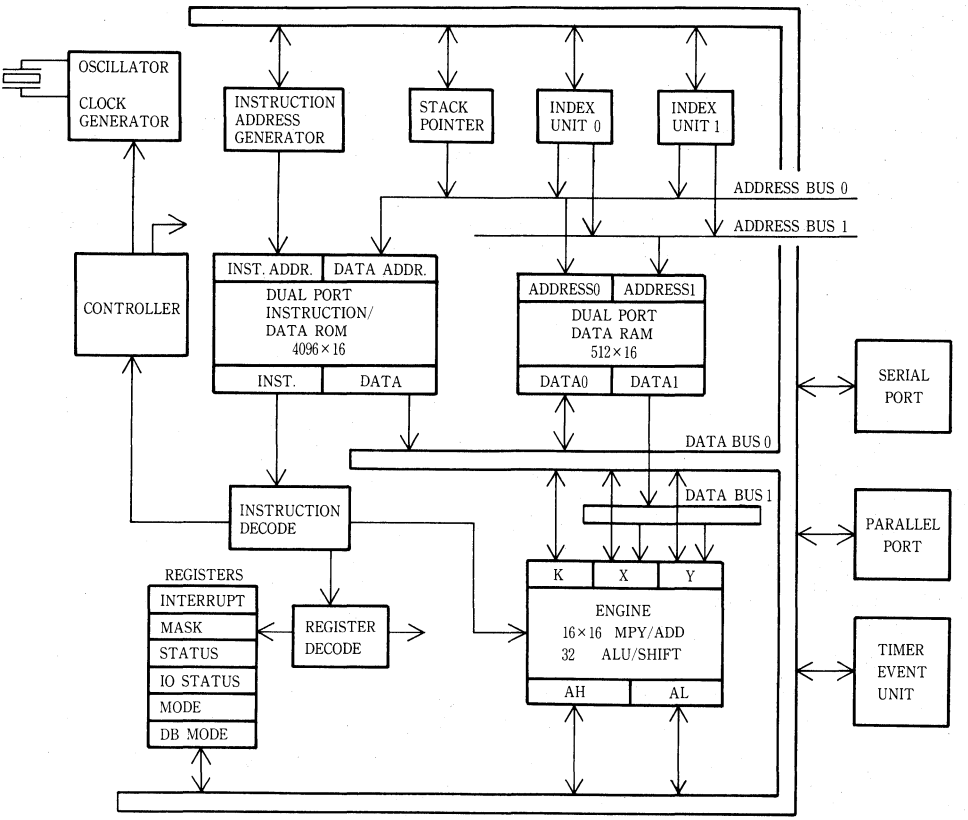
■ FEATURES

- Fast processing: 100 ns/instruction (for fck = 40 MHz)
- 16 × 16 bits → 32-bit MPY/ACC built-in
- 32-bit width ALU built-in (Fixed decimal point operation)
- 4-stage pipeline architecture
- 512 words × 16 bits RAM built-in (for data only)
- 4 k words × 16 bits ROM built-in (mask programmable) (for data and program)
- Repeat instruction function, HOLD function
- External interrupt/internal condition acknowledge EVENT port (2 pins) I/O port (2 pins)
- Two EVENT registers and one TIMER register built-in (16-bit width)
- Serial I/O port (3-line × 1)
- Parallel I/O port (8-bit × 1)
- 2-layer metal CMOS process
- 28-pin DIL plastic package
- Power consumption: 630 mW (max.)

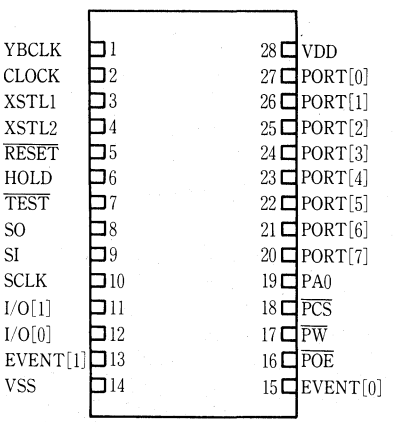
■ APPLICATION

Fast MODEM	Echo canceller
Filter bank	Motor control
Digital filters	Voice composition/recognition
ADPCM	FFT

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin Name	Pin No.	I/O	Description
VDD	28	I	+5 V power supply
VSS	14	I	GND
XSTL 1	3	I	System clock input (external clock input) Connecting a crystal oscillator between XSTL1 and XSTL2 structures an oscillation circuit. (An oscillation circuit is built-in.)
XSTL 2	4	O	
CLOCK	2	O	Internal clock output. Clock signal which is half frequency of XSTL1 is out from the CLOCK pin.
YBCLK	1	O	Internal instruction bus clock output. ¼ of the XSTL1 input frequency. When HOLD is High, the output is fixed to the Low level.
$\overline{\text{RESET}}$	5	I (Schmit Input)	Reset input. Initializes the chip. Sets bus mode, clears the MASK, INTR, STAT, IOSTAT, MODE, and DEBMODE registers, and initializes the serial/parallel port. Starts a program from the address of the values stored in memory address' h0000.
HOLD	6	I	Hold internal clock except for serial port, parallel port and timer event unit.
EVENT [0] EVENT [1]	15 13	I/O	EVENT/Compare I/O pin. This pin can be programmed to input or output. Performs sampling timing, real-time timer event, and timer value read.
I/O [1] I/O [0]	11 12	I/O	Programmable I/O port pin. Input : Senses external signals and generates interrupts to DSP. Output: For transfers of data written to internal MODE register bits 2 and 3 to the outside.
SI	9	I	Serial port data input pin. The input data synchronized with the SCLK Low timing is an input enable signal (SIEN). The input data synchronized with the SCLK High timing is SI data.
SO	8	O	Serial port data output pin. The output data synchronized with the SCLK Low timing is an output enable signal (SOEN). The output signal synchronized with the SCLK High timing is SO data.

Pin Name	Pin No.	I/O	Description
SCLK	10	O	Serial clock output. Synchronized with the DSP internal clock, 1/16 of the original oscillation frequency (XSTL1) is output. Example) When fck = 40 MHz, SCLK = 2.5 MHz (400 ns cycle)
PORT 0 ~ PORT 7	27~20	I/O	8-bit parallel port data pin.
$\overline{PW}$	17	I	Parallel port write strobe. When PW = "L" and PCS = "L", the PORT is input state.
$\overline{POE}$	16	I	Parallel port output enable. When POE = "L" and PCS = "L", the PORT is output state.
$\overline{PCS}$	18	I	Parallel port chip select.
PA 0	19	I	Parallel port address select. When PA0 = "L", selects the lower eight bits of the parallel port register (16-bit width) When PA0 = "H", selects the upper eight bits of the parallel port register (16-bit width)

Parallel port control pin assignment

$\overline{PCS}$	$\overline{POE}$	$\overline{PW}$	PA 0	PORT[7] ~ PORT[0]	Selected register
0	0	1	0	Lower 8 bit read	Lower eight bits of parallel port output
0	0	1	1	Upper 8 bit read	Upper eight bits of parallel port output
0	1	0	0	Lower 8 bit write	Lower eight bits of parallel port input
0	1	0	1	Upper 8 bit write	Upper eight bits of parallel port input
0	0	0	x	Prohibition	
0	1	1	x	Hi − Z	No Transfer
1	x	x	x	Hi − Z	No Transfer

x : Don't Care.

$\overline{TEST}$	7	I (Schmit Input)	Test mode input. Using this terminal and the $\overline{RESET}$ pin starts the test mode. Set to VDD level normally.

Note: Hi−Z: high impedance state

■ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Condition	Ratings	Unit
Vcc	Supply Voltage	Vss = 0V	-0.3 ~ +7.0	V
V_I	Input Voltage		-0.3 ~ Vcc +0.3	V
Vo	Output Voltage		-0.3 ~ Vcc +0.3	V
PD	Power Consumption	Ta = 25°C	1.0	W
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-40 ~ +125	°C

■ RECOMMENDED CONDITIONS (Ta = 0 ~ +70°C, Vss = 0V)

Symbol	Parameter		Min.	Typ.	Max.	Unit
Vcc	Supply Voltage		4.75	5.0	5.25	V
V_{IH}	"H" Input Voltage	TTL Level	2.0		Vcc +0.3	V
		CMOS Level	3.5		Vcc +0.3	V
		Schmitt Input Level	2.4		Vcc +0.3	V
V_{IL}	"L" Input Voltage	TTL Level	-0.3		0.8	V
		CMOS Level	-0.3		1.5	V
		Schmitt Input Level	-0.3		0.6	V

■ DC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 5 V ±5%)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current		V_{IN} = 0V ~ Vcc	-10		10	μA
ILO	Output Off Leakage Current		Vo = 0V ~ Vcc	-10		10	μA
V_{IH}	"H" Input Voltage	TTL Level		2.0		Vcc + 0.3	V
		Schmitt Input Level ($\overline{RESET}$, $\overline{TEST}$)		2.4			V
		Clock Input Level (XSTL 1)		4.0			V
V_{IL}	"L" Input Voltage	TTL Level		-0.3		0.8	V
		Schmitt Input Level ($\overline{RESET}$, $\overline{TEST}$)		-0.3		0.6	V
		Clock Input Level (XSTL 1)		-0.3		1.0	V
V_{OH}	"H" Output Voltage		Vcc = Min I_{OH} = -0.4 mA	2.4			V
V_{OL}	"L" Output Voltage		Vcc = Min I_{OL} = 2 mA			0.5	V
Icc	Operating Current		Vcc = Max note) V_{IN} = Vss or Vcc fck = 40 MHz			120	mA

Note 1) Output pins are measured with output unloaded
Input pins are fixed in GND or Vcc.

■ Capacitance (Ta = 25°C, f = 1 MHz)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	V_{IN} = 0V note 2)			5	pF
Co	Output Capacitance	V_{OUT} = 0V note 2)			7	pF

Note 2) This parameter is periodically sampled and not 100% tested.

■ ELECTRICAL CHARACTERISTICS

1. Clock characteristics

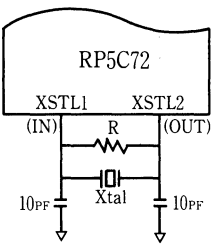
RP5C72 can use both internal oscillation circuit (Crystal oscillation) and external oscillator clock input.

1—(1) Internal clock circuit

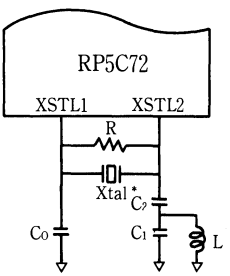
The internal clock circuit starts oscillation when inserting a crystal oscillator between XSTL 1 and XSTL 2 pins.

〈Recommended oscillation circuit〉

$f_{CK} \leqq 20MHz$



$20MHz < f_{CK} \leqq 40MHz$



Internal Clock Option

Condition

$(2\pi)^2 \left(\frac{2f_{CK}}{3}\right)^2 C_1 L \fallingdotseq 1$

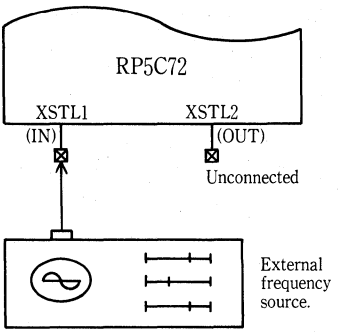
*) 3rd overtone crystal

1—(2) Load Condition ($Ta = 0°C \sim 70°C$, $Vcc = 5V \pm 5\%$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fck	Crystal Frequency		1		40	MHz
C_0	Load Capacitance of XSTL 1			15		pF
C_1	Load Capacitance of XSTL 2			15		pF
C_2	Load Capacitance of XSTL 2			0.01		μF
L	Load Inductance of XSTL 2			2.2		μH
R	Feed Back Register			1		MΩ

1–(3) External Clock

As shown in the figure on the right, an external clock device can input clock directly to the XSTL 1 pin. At that time, open the XSTL2 pin.

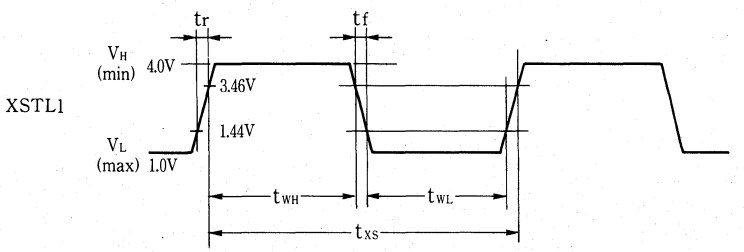


1–(4) External Clock Input Timing ($Ta = 0°C \sim 70°C$, $Vcc = 5V \pm 5\%$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{XS}	External Clock Input Cycle Time		25		1000	ns

Note) Duty ratio of the external clock : $40\% \leq (t_r + t_{WH})/t_{XS} \leq 60\%$

〈Timing Chart〉

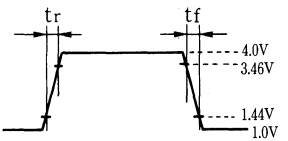


1–(5) Clock Output Switching Characteristics ($Ta = 0°C \sim 70°C$, $Vcc = 5V \pm 5\%$)

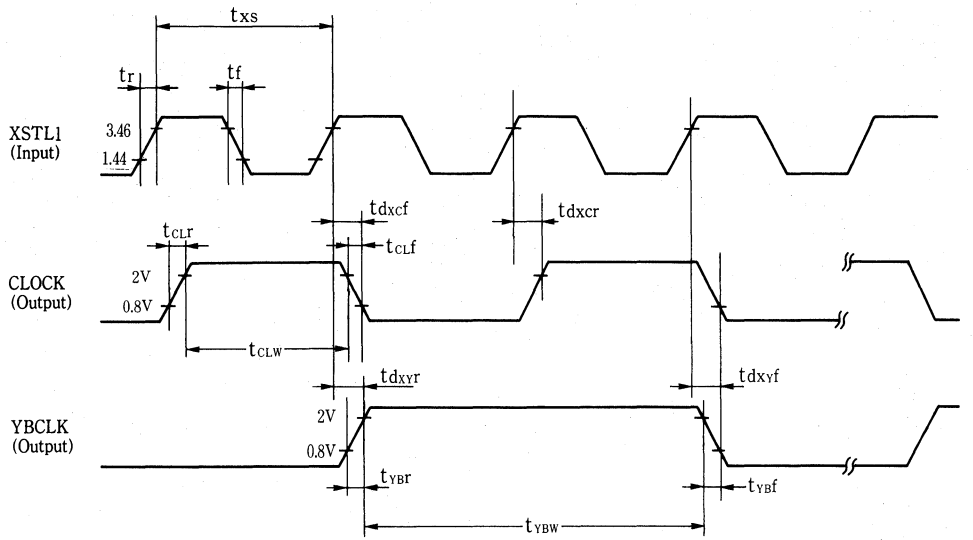
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{CLr}	CLOCK Output Rise Time	$C_L = 100pF$			8	ns
t_{CLf}	CLOCK Output Rise Time	$C_L = 100pF$			8	ns
t_{CLW}	CLOCK Output High Pulse Width		$t_{xs}-8$	t_{xs}	$t_{xs}+8$	ns
t_{YBr}	YBCLK Output Rise Time	$C_L = 100pF$			8	ns
t_{YBf}	YBCLK Output Fall Time	$C_L = 100pF$			8	ns
t_{YBW}	YBCLK Output High Pulse Width		$2t_{xs}-8$	$2t_{xs}$	$2t_{xs}+8$	ns
t_{dxcr}	XSTL 1 → CLOCK ⌋ Delay Time	$C_L = 100pF$			25	ns
t_{dxcf}	XSTL 1 → CLOCK ⌊ Delay Time	$C_L = 100pF$			25	ns
t_{dxyr}	XSTL 1 → YBCLK ⌋ Delay Time	$C_L = 100pF$			35	ns
t_{dxyf}	XSTL 1 → YBCLK ⌊ Delay Time	$C_L = 100pF$			35	ns

Rise/fall time of clock input signal
The following times are recommended:

Rise time (t_r) : 5 ns max.
Fall time (t_f) : 5 ns max.



〈Timing Chart〉



Note) Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V unless otherwise noted.

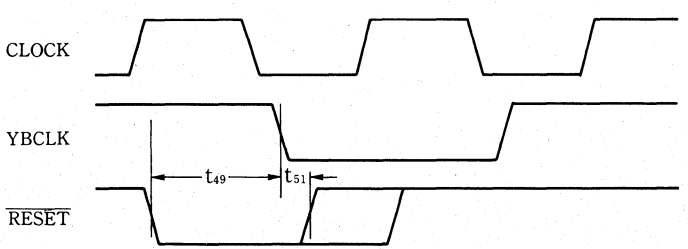
2. Control Pin

2–(1) Soft Reset (Ta = 0°C ~ 70°C, Vcc = 5V±5%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{49}	YBCLK → $\overline{\text{RESET}}$ Setup Time		40		$4t_{xs}-10$	ns
t_{51}	$\overline{\text{RESET}}$ Active Hold Time		10		$4t_{xs}-50$	ns

Note) Soft reset is not performed in the timing that YBCLK stretches internally.

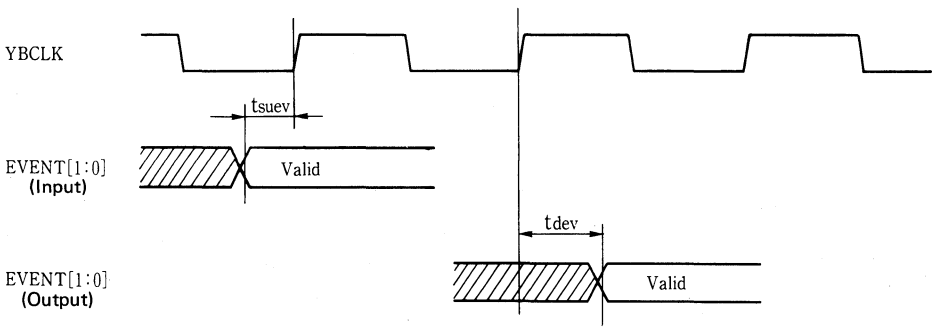
〈Timing Chart〉



2–(2) EVENT Pin (Ta = 0°C ~ 70°C, Vcc = 5V±5%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{suev}	Setup Time of EVENT Input before YBCLK ↓		30		$4t_{xs}-10$	ns
t_{dev}	EVENT Output Delay Time		0		35	ns

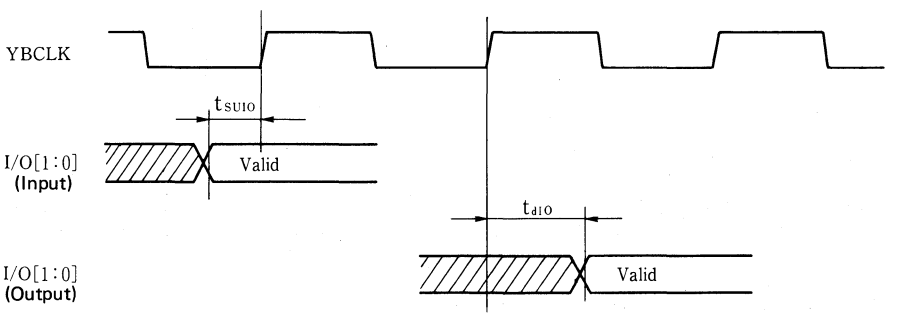
〈Timing Chart〉



2–(3) I/O Pin (Ta = 0°C ~ 70°C, Vcc = 5V±5%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{suIO}	Setup Time of I/O Input before YBCLK ↓		30		$4t_{xs}-10$	ns
t_{dIO}	I/O Output Delay Time		0		35	ns

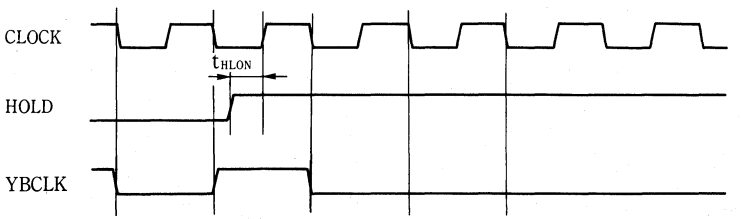
〈Timing Chart〉



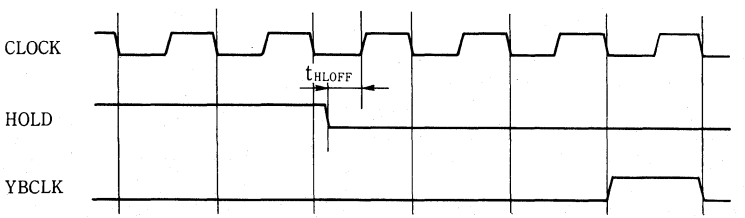
2–(3) HOLD Pin ($Ta = 0°C \sim 70°C$, $Vcc = 5V \pm 5\%$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{HLON}	Setup Time HOLD ↓ before CLOCK ↓		20		$2t_{xs} - 10$	ns
t_{HLOFF}	Setup Time HOLD ↑ before CLOCK ↓		20		$2t_{xs} - 10$	ns

〈Timing Chart HOLD enable〉



〈Timing Chart HOLD disable〉



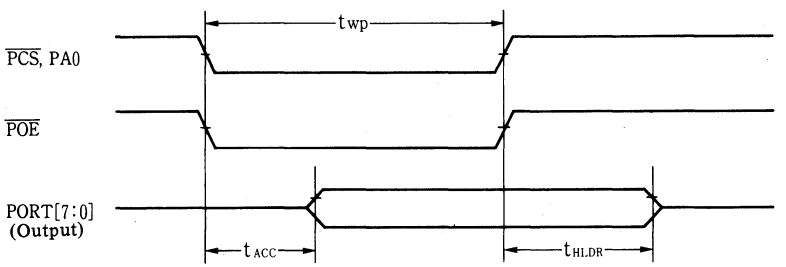
3. I/O Port

3–(1) Parallel Port (Ta = 0°C ~ 70°C, Vcc = 5V±5%)

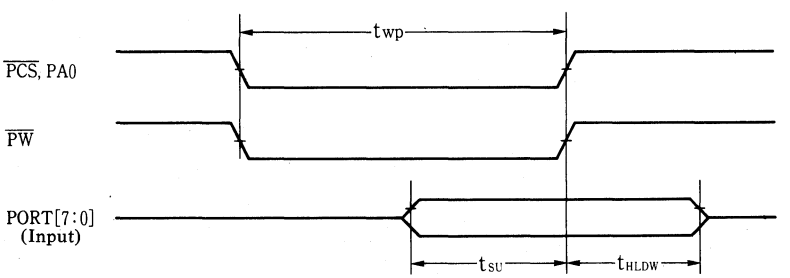
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{ACC}	Parallel Port Output Access Time		0		75	ns
t_{HLDR}	Parallel Port Output Read Hold Time		5			ns
t_{SU}	Parallel Port Input Setup Time		25			ns
t_{HLDW}	Parallel Port Input Write Hold Time		10			ns
t_{WP}	$\overline{PCS}$, PAO, $\overline{POE}$, $\overline{PW}$ Pulse Width		$4t_{XS}+50$			ns

〈Timing Chart〉

Parallel Port Output Timing (External Read)

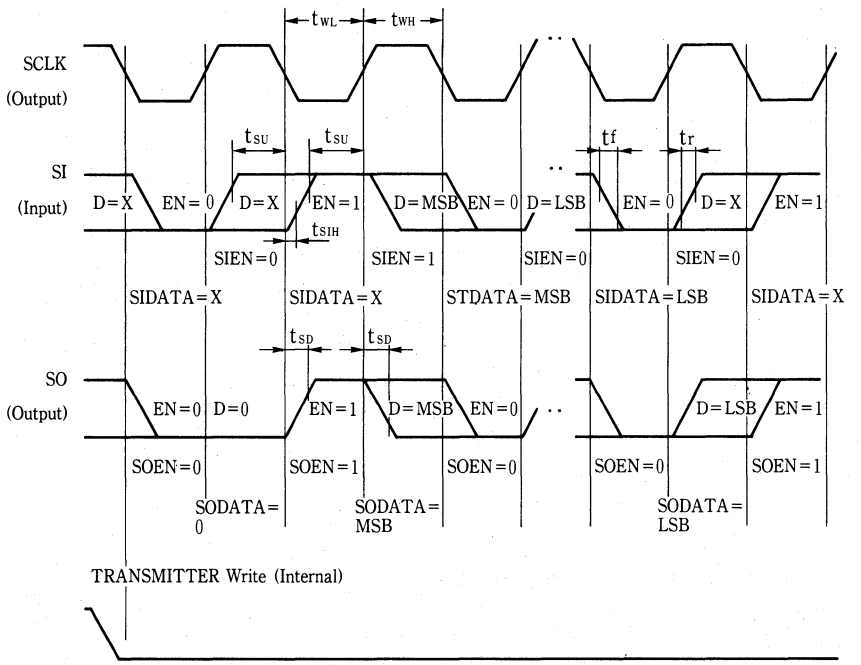


Parallel Port Input Timing (External Write)



3–(2) Serial Poat (Ta = 0°C ~ 70°C, Vcc = 5V±5%)

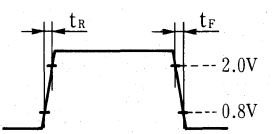
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$tw_{L(H)}$	SCLK 'LOW' ('High') Pulse Width		200	$8t_{XS}$		ns
t_{SU}	SI Input Setup Time		50			ns
t_{SIH}	SI Input Hold Time		0			ns
t_{SD}	SO Output Delay Time		0		25	ns



Rise/fall time of serial input signal (SI)
The following times are recommended:

Rise time (t_r) : 5 ns (Max.)

Fall time (t_p) : 5 ns (Max.)



3–(3)

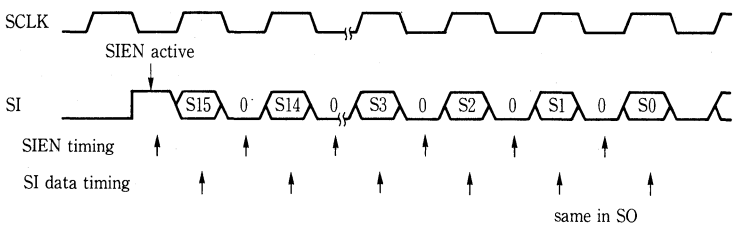
—— Notes for Serial Port Timing ——

(1) D = X and SIDATA = X in the timing chart mean the data is "don't care".

(2) SIEN and SI are time-divided and input to the same input pin (SI).
SIEN is synchronized with the rising edge of SCLK and input.
SI data is synchronized with the falling edge of SCLK and input.

(3) SOEN and SO is time-divided and output from the same output pin (SO).
SOEN is synchronized with the falling edge of SCLK and output.
SO data is synchronized with the rising edge of SCLK and output.

(4) To transfer data, make the enable signal active first (1), then fetch 16-bit data as shown in the figure below:



(5) SCLK is 1/16 of the XSTL1 frequency (original oscillation frequency).

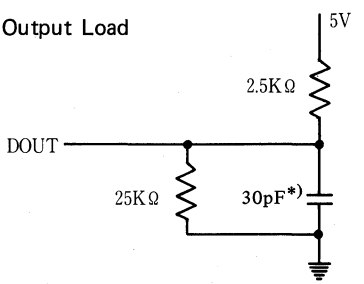
(6) The SCLK clock is always output from an external pin.

(7) SO does not become Hi–Z state.

4. AC Test Condition

Input Pulse Levels	GND to 3.0V
Input Rise and Fall times	10ns
Input Timing Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure

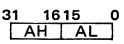
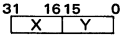
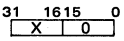
Output Load



*) Includes scope and jig.

■ INSTRUCTIONS

● Description of Symbols

Symbol	Meaning	Symbol	Meaning
A	Accumulator (32-bit width) 	SX(XX)	Sign-extends MSB.
AH	Upper 16-bits of accumulator	1 (a)	Increase in the instruction cycle (case a).
AL	Lower 16-bits of accumulator		The case that the instruction cycle is increased by one in the edual (external dual) mode.
X, Y, K	Input registers for ENGINE (MPY, ALU etc.)		
X @ Y	Configures a 32-bit width making the upper 16-bits the X register and lower 16-bits the Y register. 	1 (b)	Increase in the instruction cycle (case b). The case that the instruction cycle is increased by one when transferring data to the register in the INDEX UNIT (r, i, p, t) and the stack pointer.
X @ 0	Makes the upper 16-bits the X register and makes the lower 16-bits all zeros, and configures a 32-bit width. 		
SP	Stack pointer (16-bit width)	1 (c)	Increase in the instruction cycle (case c). The case that the instruction cycle is increased by one when no jump and call occur by the control instruction (JMPRNZ CALLRNZ) of one instruction cycle.
PC	Program counter (16-bit width)		
(aa)	Absolute address		
(ra)	Relative address		
freg	Fast register (for types, see the internal register list (P25).)		
hxxxx	Hexadecimal data display	XX,?	Don't care

● Description of Operand Symbols

The operands are in the same form as the symbols for assembler description.

Symbol	Field size	Meaning
⟨eidx⟩	11 bits	eidx mode bit (*1)
⟨dir. ix⟩	8 bits	Direct indexing mode bit (*1)
⟨const n⟩	n bit	n-bit-constant
⟨freg⟩	4 bits	Fast register address
⟨reg⟩	5 bits	Address of all registers (fast and slow registers)
⟨src⟩	5 bits	Source register code of data transfer instruction (XFR)
⟨dst⟩	5 bits	Destination register code of data transfer instruction (XFR)
⟨cond⟩	5 bits	Condition code (*2)
⟨dest⟩	n bit	Jump destination value of jump and call instructions (n bits)
⟨imm n⟩	n bit	Immediate data value

*1: See the INDEXING DEFINITION TABLE. (P24)

*2: For details, see the CONDITION TABLE. (P26)

• Description of Instructions (Alphabetic order)

(Instruction group A : Arithmetic/logical operation instructions　　Instruction group C : Control flow instructions
Instruction group B : Load/store instructions　　Instruction group D : Illegal op-codes)

No.	Mnemonic	Operation	Explanation of instruction	Number of words/cycles Bits with changing flag	Instruction group
1.	**ADD**		Addition of accumulator and X and Y registers	1/1+1(a)	A group
		Operation :	(A) + (X @ Y) → A, (PC) + 1 → PC	FLAG : V, C, N, Z, B	
2.	**ADDXY**		Addition of X and Y registers	1/1+1(a)	A group
		Operation :	(X @ 0) + (Y @ 0) → A, (PC) + 1 → PC	FLAG : V, C, N, Z, B	
3.	**AND**		Logical product of accumulator and X and Y registers	1/1+1(a)	A group
		Operation :	(A) AND (X @ Y) → A, (PC) + 1 → PC	FLAG : N, Z, B	
4.	**ANDXY**		Logical product of X and Y registers	1/1+1(a)	A group
		Operation :	(X @ 0) AND (Y @ 0) → A, (PC) + 1 → PC	FLAG : N, Z, B	
5.	**CALLA**		Conditional absolute address subroutine call	2/2	C group
		Operation :	When the condition is true : (PC) + 1 → (SP)	FLAG : No change	
			(SP) + 1 → SP		
			(aa) → SP		
			else : (PC) + 1 → PC		
6.	**CALLS**		System routine call ('h0010 address)	1/2+1(a)	C group
		Operation :	(PC) + 1 → (SP)		
			(SP) + 1 → SP		
			'h0010 → PC	FLAG : No change	
7.	**CALLRNZ**		Conditional (≠0) relative address (−1024 to +1023) subroutine call	1/1+1(c)	C group
		Operation :	When the condition is true : (PC) + SX(ra) → PC		
			else : (PC) + 1 → PC		
			−1024 ≦ ra ≦ + 1023	FLAG : No change	
			('hFC00) ('h03FF)		
8.	**CALLRT**		Unconditional relative address (−1024 to +1023) subroutine call	1/1	C group
		Operation :	(PC) + 1 → (SP)		
			(SP) + 1 → SP		
			(PC) + SX(ra) → PC	FLAG : No change	
9.	**ENOP**		No operation	1/1	A group
		Operation :	(PC) + 1 → PC		
			Nothing is done otherwise.	FLAG : No change	
10.	**IDS**		Interrupt inhibit instruction	1/1	C group
		Operation :	Interrupt inhibit (normally used after the IEN instruction)		
			(PC) + 1 → PC	FLAG : No change	
11.	**IEN**		Interrupt enable instruction	1/1	C group
		Operation :	Enables interrupt.	FLAG : No change	
12.	**ILLOP0**		Illegal op-code 0	1/1	D group
		Operation :	Sets bit 15 of the IOSTAT register (instruction for debugging)		
			(PC) + 1 → PC	FLAG : No change	

13. ILLOP1 — Illegal op-code 1 — 1/1 — D group

Operation : Sets bit 15 (ILLOP) of the IOSTAT register.
(PC) + 1 → PC — FLAG : No change

14. ILLOP2 — Illegal op-code 2 — 1/1 — D group

Operation : Sets bit 15 (ILLOP) of the IOSTAT register.
(PC) + 1 → PC — FLAG : No change

15. ILLOP3 — Illegal op-code 3 — 1/1 — D group

Operation : Sets bit 15 (ILLOP) of the IOSTAT register.
(PC) + 1 → PC — FLAG : No change

16. ILLOP4 — Illegal op-code 4 — 1/1 — D group

Operation : Sets bit 15 (ILLOP) of the IOSTAT register.
(PC) + 1 → PC — FLAG : No change

17. ILLOP5 — Illegal op-code 5 — 1/1 — D group

Operation : Sets bit 15 (ILLOP) of the IOSTAT register.
(PC) + 1 → PC — FLAG : No change

18. ILLOP6 — Illegal op-code — 1/1 — D group

Operation : Sets bit 15 (ILLOP) of the IOSTAT register.
(PC) + 1 → PC — FLAG : No change

19. ILLOP7 — Illegal op-code — 1/1 — D group

Operation : Sets bit 15 (ILLOP) of the IOSTAT register.
(PC) + 1 → PC — FLAG : No change

20. JMPA — Conditional absolute address jump instruction — 2/2 — C group

Operation : Condition (see the condition table.) — FLAG : No change
When true : (aa) → PC
else : (PC) + 2 → PC

21. JMPR — Conditional relative address (–64 to +63) jump instruction — 1/1+1(c) — C group

Operation : Condition (see the condition table.) — FLAG : No change
When true: (PC) + SX(ra) → PC
else : (PC) + 1 → PC

22. LDB — One-byte data load instruction (fast register only) — 1/1+1(b) — B group

Operation : Sign-extends 8-bit data, and loads it to the fast register as 16-bit data (see the register classification table).
(PC) + 1 → PC
SX (8-bit data) → freg — FLAG : No change

23. LDIX — Index load instruction (fast register only) — 1/1+1(b) — B group

Operation : (1) ((r0) + SX(ra)) → freg, (PC) + 1 → PC
(2) ((r1) + SX(ra)) → freg, (PC) + 1 → PC — FLAG : No change

24. LDW — 1-word (16-bit) data load instruction (all registers) — 2/2+1(b) — B group

Operation : (PC) + 2 → PC

16-bit data → reg (fast/slow register) — FLAG : No change

25. LPC — Conditional loop instruction — 1/1+n+1 — C group

Operation : While the condition is true, repeats execution of the next instruction.

(PC) + 1 → PC After that, if the condition is : — FLAG : No change

True : (PC) → PC

else : (PC) + 1 → PC

(For conditions, see the condition table.)

26. LPI — Immediate loop instruction — 1/1+n+1 — C group

Operation : Repeats the execution of the next instruction as many times as indicated by the lower 7-bits of the instruction.

(PC) + 1 → PC After that, if $n > 0$, (PC) → PC, n-1 → n

if $n = 0$, (PC) + 1 → PC

n : lower 7-bits of the instruction code

$(0 \leqq n \leqq 127)$ — FLAG : No change

27. MAC — Adds the accumulator and the result of multiplication of the X and Y registers. — 1/1+1(a) — A group

Operation : (A) + (X) × (Y) → A, (PC) + 1 → PC — FLAG : V, C, N, Z

28. MACAX — Adds the X@0 register (32-bit) and the result of multiplication of the upper 16-bits of the accumulator and the Y register. — 1/1+1(a) — A group

Operation : (X @ 0) + (AH) × (Y) → A, (PC) + 1 → PC — FLAG : V, C, N, Z

29. MACK — Adds the X@0 register and the result of multiplication of the K and Y registers, and outputs to the accumulator. — 1/1+1(a) — A group

Operation : (X @ 0) + (K) × (Y) → A, (PC) + 1 → PC — FLAG : V, C, N, Z

30. MSB — Subtracts the result of multiplication of the X and Y registers from the accumulator. — 1/1+1(a) — A group

Operation : (A) − (X) × (Y) → A, (PC) + 1 → PC — FLAG : V, C, N, Z,

31. MUL — Outputs the result of the multiplication of the X and Y registers to the accumulator. — 1/1+1(a) — A group

Operation : (X) × (Y) → A, (PC) + 1 → PC — FLAG : V, N, Z

32. OR — Logical add of the accumulator and the X@Y register. — 1/1+1(a) — A group

Operation : (A) OR (X @ Y) → A, (PC) + 1 → PC — FLAG : N, Z, B

33. ORXY — Logical add of the X@0 register and the Y@0 register. — 1/1+1(a) — A group

Operation : (X @ 0) OR (Y @ 0) → A, (PC) + 1 → PC — FLAG : N, Z, B

34. POP — Draws data from the stack to the register. — 1/1+(b) — B group

Operation : (SP) + 1 → SP, (SP) → reg (All registers)

(PC) + 1 → PC — FLAG : No change

35. PSH — Stores the register value in the stack. — 1/1+1(b) — B group

Operation : (reg) → (SP), (SP) − 1 → SP

(PC) + 1 → PC — FLAG : No change

36. RTI — Return from the interrupt routine. — 1/3 — C group

Operation : (SP) + 1 → SP

(SP) → PC — FLAG : No change

Return from the interrupt routine by storing the value again from the stack pointer to the program counter.

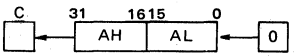
37. RTS — Return from subroutine — 1/3 — C group

Operation : (SP) + 1 → SP
(SP) → PC — FLAG : No change

Return from the subroutine by storing the value again from the stack pointer to the program counter.

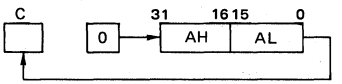
38. SHL — Accumulator value logical shift instruction (1-bit to the left) — 1/1+1(a) — A group

Operation : (A) shift left 1-bit → A, (PC) + 1 → PC — FLAG : C, N, Z, B



39. SHR — Accumulator value logical shift instruction (1-bit to the right) — 1/1+1(a) — A group

Operation : (A) shift right 1-bit → A, (PC) + 1 → PC — FLAG : C, N, Z, B



40. STIX — Index store from the fast register to the memory — 1/1 — B group

Operation : (freg) → (r0) + sx(ra)
(freg) → (r1) + sx(ra) — FLAG : No change

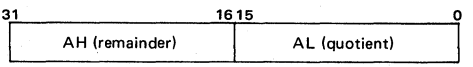
41. SUB — Subtracts the X@Y register value from the accumulator. — 1/1+1(a) — A group

Operation : (A) − (X@Y) → A, (PC) + 1 → PC — FLAG : V, C, N, Z, B

42. SUBC — Conditional subtract instruction — 1/1 — A group

Operation : If (A) − (X@Y) < 0, (A) X 2 → A, LSB = 0
If (A) − (X@Y) ≧ 0, [(A) − (X@Y)] X 2 → A
LSB = 1 — FLAG : V, C, N, Z

(Division) Using the loop instruction and SUBC in combination, the division results (quotient and remainder) can be obtained by the accumulator.



result of division

43. SUBI — Subtracts the accumulator value from the X@Y register. — 1/1+1(a) — A group

Operation : (X @ Y) − (A) → A, (PC) + 1 → PC — FLAG : V, C, N, Z, B

44. SUBXY — Subtracts the Y@0 register value from the X@0 register. — 1/1+1(a) — A group

Operation : (X @ 0) − (Y @ 0) → A, (PC) + 1 → PC — FLAG : V, C, N, Z, B

45. SUBYX — Subtracts the X@0 register value from the Y@0 register. — 1/1+1(a) — A group

Operation : (Y @ X) − (X @ 0) → A, (PC) + 1 → PC — FLAG : V, C, N, Z, B

46. XFR — Data transfer instruction between any registers — 1/1+1(b) — B group

Operation : (reg) → reg, (PC) + 1 → PC — FLAG: No change

reg is all registers (16-bit width).

47. XOR — Exclusive logical add of the accumulator and the X@Y register — 1/1+1(a) — A group

Operation : (A) XOR(X @ Y) → A, (PC) + 1 → PC — FLAG : N, Z, B

48. XORXY — Exclusive logical add of the X@0 register and the Y@0 register — 1/1+1(a) — A group

Operation : (X @ 0) XOR (Y @ 0) → A, (PC) + 1 → PC — FLAG : N, Z, B

■ INSTRUCTION SET SUMMARY

〔A〕 Arithmetic/Logic Instruction					Instruction Bit Pattern
MNEMONIC	WORDS	CYCLES	DESCRIPTION	OPERANDS	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ENOP	1	1+1(a)	Indexing only	⟨eidx⟩	0 0 0 0 0 ←——— eidx ———→
ADD	1	1+1(a)	A ← (A) + (X @ Y)	⟨eidx⟩	0 0 0 0 1 ←——— eidx ———→
ADDXY	1	1+1(a)	A ← (X @ 0) + (Y @ 0)	⟨eidx⟩	0 0 0 1 0 ←——— eidx ———→
SUB	1	1+1(a)	A ← (A) - (X @ Y)	⟨eidx⟩	0 0 0 1 1 ←——— eidx ———→
SUBXY	1	1+1(a)	A ← (X @ 0) - (Y @ 0)	⟨eidx⟩	0 0 1 0 0 ←——— eidx ———→
SUBI	1	1+1(a)	A ← (X @ Y) - (A)	⟨eidx⟩	0 0 1 0 1 ←——— eidx ———→
SUBYX	1	1+1(a)	A ← (Y @ 0) - (X @ 0)	⟨eidx⟩	0 0 1 1 0 ←——— eidx ———→
SUBC	1	1	If (A)-(X@Y)⟨0 then (A)*2-⟩ A.LSB=0 (A)-(X@Y)≧0 then (A-X@Y)*2→A, LSB=1 The Result AH = the remainder AL = the quotient	—— —— —— ——	1 1 0 1 0 1 0 1 1 1 0 0 0 0 1 0
MUL	1	1+1(a)	A ← (X) * (Y)	⟨eidx⟩	0 0 1 1 1 ←——— eidx ———→
MAC	1	1+1(a)	A ← (A) + (X) * (Y)	⟨eidx⟩	0 1 0 0 0 ←——— eidx ———→
MACAX	1	1+1(a)	A ← (X @ 0) + (AH) * (Y)	⟨eidx⟩	0 1 0 0 1 ←——— eidx ———→
MACK	1	1+1(a)	A ← (X @ 0) + (K * Y)	⟨eidx⟩	0 1 0 1 0 ←——— eidx ———→
MSB	1	1+1(a)	A ← (A) - (X) * (Y)	⟨eidx⟩	0 1 0 1 1 ←——— eidx ———→
AND	1	1+1(a)	A ← (A) AND (X @ Y)	⟨eidx⟩	0 1 1 0 0 ←——— eidx ———→
ANDXY	1	1+1(a)	A ← (X @ 0) AND (Y @ 0)	⟨eidx⟩	0 1 1 0 1 ←——— eidx ———→
OR	1	1+1(a)	A ← (A) OR (X @ Y)	⟨eidx⟩	0 1 1 1 0 ←——— eidx ———→
ORXY	1	1+1(a)	A ← (X @ 0) OR (Y @ 0)	⟨eidx⟩	0 1 1 1 1 ←——— eidx ———→
XOR	1	1+1(a)	A ← (A) XOR (X @ Y)	⟨eidx⟩	1 0 0 0 0 ←——— eidx ———→
XORXY	1	1+1(a)	A ← (X @ 0) XOR (Y @ 0)	⟨eidx⟩	1 0 0 0 1 ←——— eidx ———→
SHR	1	1+1(a)	A ← (A) SHR 1 (right)	⟨eidx⟩	1 0 0 1 0 ←——— eidx ———→
SHL	1	1+1(a)	A ← (A) SHL 1 (left)	⟨eidx⟩	1 0 0 1 1 ←——— eidx ———→

〔B〕 Load/Store Instruction					Instruction Bit Pattern
MNEMONIC	WORDS	CYCLES	DESCRIPTION	OPERANDS	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
LDW	2	2+1(b)	Load 16_bit immediate value into register.	⟨const 16⟩ ⟨reg⟩	1 1 0 1 0 1 0 1 0 1 0 ←—reg—→ ←——————imm 16——————→
LDB	1	1+1(b)	Load 8_bit immediate value into fast register with sign extend.	⟨const 8⟩ ⟨freg⟩	1 1 0 0 ←—freg—→ ←—— imm 8 ——→
LDIX	1	1+1(b)	Indexed load to fast register. (freg)	⟨dir. ix⟩ ⟨freg⟩	1 0 1 0 ←—freg—→ ←——idx——→
STIX	1	1	Indexed store to fast register. (freg)	⟨freg⟩ ⟨dir. ix⟩	1 0 1 1 ←—freg—→ ←——idx——→
XFR	1	1+1(b)	Register transfer, any registers. src -⟩ dst (src and dst are reg)	⟨src⟩ ⟨dst⟩	1 1 0 1 0 0 ←—src—→ ←—dst—→
PSH	1	1+1(b)	Push reg. onto stack.	⟨reg⟩	1 1 0 1 0 1 0 1 0 0 1 ←—reg—→
POP	1	1+1(b)	Pop reg. from stack	⟨reg⟩	1 1 0 1 0 1 0 1 0 0 0 ←—reg—→

[C] Control Flow Instruction					Instruction Bit Pattern
MNEMONIC	WORDS	CYCLES	DESCRIPTION	OPERANDS	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
LPC	1	1+n+1	Loop conditional	⟨cond⟩	1 1 0 1 0 1 0 0 0 ? ? ⟵cond⟶
LPI	1	1+n+1	Loop immediate	⟨const 7⟩	1 1 0 1 0 1 0 0 1 ⟵imm 7⟶
JMPA	2	2	Conditional absolute jump	⟨cond⟩ ⟨dest⟩	1 1 0 1 0 1 0 1 1 0 0 ⟵cond⟶ ⟵imm 16⟶
CALLA	2	2	Conditional absolute call	⟨cond⟩ ⟨dest⟩	1 1 0 1 0 1 0 1 1 0 1 ⟵cond⟶ ⟵imm 16⟶
CALLS	1	2	Call location 16	⟨eidx⟩	1 1 0 1 1 ⟵eidx⟶
JNPR	1	1+1(c)	Conditional jump relative +63/-64	⟨cond⟩ ⟨dest⟩	1 1 1 0 ⟵cond⟶ ⟵imm 7⟶
CALLRNZ	1	1+1(c)	Not zero call relative +1023/-1024	⟨dest⟩	1 1 1 1 0 ⟵imm 11⟶
CALLRT	1	1	Unconditional call relative +1023/-1024	⟨dest⟩	1 1 1 1 1 ⟵imm 11⟶
RTS	1	3	Return from subroutine by restoring PC from the SP.	——	1 1 0 1 0 1 0 1 1 1 1 0 0 0 0 1 1
RTI	1	3	Return from interrupt service	——	1 1 0 1 0 1 0 1 1 1 1 0 0 0 1 1 1
IEN	1	1	Enable interrupts	——	1 1 0 1 0 1 0 1 1 1 1 0 0 0 0 0 0
IDS	1	1	Disable interrupts (used after IEN)	——	1 1 0 1 0 1 0 1 1 1 1 0 0 0 0 0 1

[D] Illegal Opcode Instruction					Instruction Bit Pattern
MNEMONIC	WORDS	CYCLES	DESCRIPTION	OPERANDS	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ILLOP0	1	1	Illegal opcode 0	⟨const 5⟩	1 1 0 1 0 1 0 1 0 1 1 ⟵imm 5⟶
ILLOP1	1	1	Illegal opcode 1	⟨const 5⟩	1 1 0 1 0 1 0 1 1 1 1 ⟵imm 5⟶
ILLOP2	1	1	Illegal opcode 2	⟨const 4⟩	1 1 0 1 0 1 0 1 1 1 0 1 ⟵imm 4⟶
ILLOP3	1	1	Illegal opcode 3	⟨const 3⟩	1 1 0 1 0 1 0 1 1 1 0 0 ⟵imm 3⟶
ILLOP4	1	1	Illegal opcode 4	——	1 1 0 1 0 1 0 1 1 1 0 0 0 1 0 0
ILLOP5	1	1	Illegal opcode 5	——	1 1 0 1 0 1 0 1 1 1 0 0 0 1 0 1
ILLOP6	1	1	Illegal opcode 6	——	1 1 0 1 0 1 0 1 1 1 0 0 0 1 1 0
ILLOP7	1	1	Illegal opcode 7	⟨const 9⟩	1 1 0 1 0 1 1 ⟵imm 9⟶

■ INSTRUCTION CYCLE

	[A] Arithmetic/ Logic	[B] Load/Store	[C] Control Flow	[D] Illegal Opcode
1 W 1 C [Single word Single cycle]	ENOP ADD ADDXY SUB SUBXY SUBI SUBYX SUBC MUL MAC MACAX MACK MSB AND ANDXY OR ORXY XOR XORXY SHR SHL	LDB LDIX STIX XFR PSH POP	JMPR (taken) CALLRT CALLRNZ (taken)	ILLOP0 ILLOP1 ILLOP2 ILLOP3 ILLOP4 ILLOP5 ILLOP6 ILLOP7
1 W 2 C [Single word 2 cycles]	ENOP AND ADDXY SUB SUBXY SUBI SUBYX MUL MAC MACAX MACK MSB AND ANDXY OR ORXY XOR XORXY SHR SHL [external dual (EXDUAL) mode]	LDB n IU LDIX (rx, n) IU POP IU POP SP XFR reg IU XFR reg SP [IU: p0, p1, i0 i1, t0, t1 r0, r1]	JMPR (not taken) CALLRNZ (not taken) CALLS	
1 W 3 C [Single word 3 cycles]			RTS RTI	
2 W 2 C [2 words 2 cycles]		LDW n reg (except IU/SP)	JMPA CALLA	
2 W 3 C [2 words 3 cycles]		LDW n IU LDW n SP		
MISC.			LPC --- 1+n+1 LPI --- 1+n+1	

■ INDEXING DEFINITION

MODE	Assembler Syntax	Bit Pattern 10 9 8 7 6 5 4 3 2 1 0	Descriptions
⟨EIDX⟩	⟨eidx⟩	e e e e e e e e e e e	
edual	⟨y index⟩ ⟨x index⟩	0 y y y y y x x x x x	Two fields of five bits.
eimm	⟨const 8⟩ x	1 0 0 i i i i i i i i	X ← sx(imm8)
	⟨const 8⟩ y	1 0 1 i i i i i i i i	Y ← sx(imm8)
edx	(r0, ⟨const 7⟩) x	1 1 0 0 i i i i i i i	X ← (r0 + sx(idx7))
	(r1, ⟨const 7⟩) y	1 1 0 1 i i i i i i i	Y ← (r1 + sx(idx7))
	ah (r0, ⟨const 7⟩)	1 1 1 0 i i i i i i i	(r0 + sx(idx7)) ← AH
	ah (r1, ⟨const 7⟩)	1 1 1 1 i i i i i i i	(r1 + sx(idx7)) ← AH
⟨DIRECT INDEXING⟩	⟨direct ix⟩	u u u u u u u u u	
idx	(r0, ⟨const 7⟩)	0 i i i i i i i i	freg ← (r0 + sx(idx7)) : LDIX
		0 i i i i i i i i	(r0 + sx(idx7)) ← freg : STIX
	(r1, ⟨const 7⟩)	1 i i i i i i i i	freg ← (r1 + sx(idx7))
		1 i i i i i i i i	(r1 + sx(idx7)) ← freg

= N.B. = sx -⟩ Sign extend

■ EDUAL (engine dual) INDEXING DESCRIPTION

Mnemonic ⟨y index⟩	Mnemonic ⟨x index⟩	Pattern yyyyy xxxxx	Description Description for ⟨x index⟩
nop1	nop0	00000	no operation for IU0
0y	0x	00010	x ← 0
-1y	-1x	00110	x ← -1
!p1+	!p0+	00001	p0 ← p0 + 1
!p1-	!p0-	00111	p0 ← p0 - 1
!p1+i	!p0+i	00011	p0 ← p0 + i0
!p1+r	!p0+r	00100	p0 ← p0 + r0
!p1c	!p0c	00101	if p0 = t0 then p0 ← r0, else p0 ← p0+1
ah(p1)	ah(p0)	01000	(p0) ← ah
ah(r1)	ah(r0)	01001	(r0) ← ah
ah(t1)	ah(t0)	01010	(t0) ← ah
ah(p1+i)	ah(p0+i)	01011	(p0 + i0) ← ah
ah(p1+r)	ah(p0+r)	01100	(p0 + r0) ← ah
ah(!p1c)	ah(!p0c)	01101	if p0 = t0 then p0 ← r0, else p0 ← p0 +1, (p0) ← ah
ah(!p1+i)	ah(!p0+i)	01110	p0 ← p0 + i0 , (p0) ← ah
ah(!p1+r)	ah(!p0+r)	01111	p0 ← p0 + r0 , (p0) ← ah
(p1)y	(p0)x	10000	x ← (p0)
(t1)y	(t0)x	10101	x ← (t0)
(r1)y	(r0)x	11000	x ← (r0)
(p1+)y	(p0+)x	10001	x ← (p0 + 1)
(p1++)y	(p0++)x	10010	x ← (p0 + 2)
(p1-)y	(p0-)x	10111	x ← (p0 - 1)
(p1--)y	(p0--)x	10110	x ← (p0 - 2)
(p1+i)y	(p0+i)x	10011	x ← (p0 + i0)
(p1+r)y	(p0+r)x	10100	x ← (p0 + r0)
(!p1+)y	(!p0+)x	11001	p0 ← p0 + 1 , x ← (p0)
(!p1++)y	(!p0++)x	11010	p0 ← p0 + 2 , x ← (p0)
(!p1-)y	(!p0-)x	11111	p0 ← p0 - 1 , x ← (p0)
(!p1--)y	(!p0--)x	11110	p0 ← p0 - 2 , x ← (p0)
(!p1+i)y	(!p0+i)x	11011	p0 ← p0 + i0 , x ← (p0)
(!p1+r)y	(!p0+r)x	11100	p0 ← p0 + r0 , x ← (p0)
(!p1c)y	(!p0c)x	11101	if p0 = t0 then p0 = r0, else p0 ← p0+1 : x ← (p0)

⟨Y index⟩ is same in operation as ⟨X index⟩.

■ INTERNAL REGISTER SUMMARY (27)

FAST REGISTERS

Reg #	Mnemonic	Description
00	P0	pointer ┐
01	I 0	index ├ Index Unit 0
02	T0	test ├
03	R0	reload ┘
04	P1	pointer ┐
05	I 1	index ├ Index Unit 1
06	T1	test ├
07	R1	reload ┘
08	AL	Least significant accumulator word
09	AH	Most significant accumulator word
0A	AZ	LOAD: load AH, zero AL STORE: store AH
0B	X	┐
0C	Y	├ Engine registers
0D	K	┘
0E	PARPORT	Parallel Port data register
0F	SERPORT	Serial Port data register

SLOW REGISTERS

Reg #	Mnemonic	Description
10	MASK	Interrupt mask
11	INTR	Interrupt
12	STAT	Execution status
13	IOSTAT	Serial, Parallel & debug status
14	MODE	Mode select
15		Reserved
16	DEBMODE	Debug and test mode
17	SP	Stack pointer
18	E0	Event/Compare 0
19	E1	Event/Compare 1
1A		Reserved
1B		Reserved
1C	TIMER	Timer
1D		Reserved
1E	PROGMAT	Program address compare
1F		Reserved

■ FLAG CONDITION

FLAG CONDITION

Mnemonic	V	C	N	Z	B
ENOP	-	-	-	-	-
ADD	m	m	m	m	m
ADDXY	m	m	m	m	m
SUB	m	m	m	m	m
SUBXY	m	m	m	m	m
SUBI	m	m	m	m	m
SUBYX	m	m	m	m	m
MUL	m	-	m	m	-
MAC	m	m	m	m	-
MACAX	m	m	m	m	-
MACK	m	m	m	m	-
MSB	m	m	m	m	-
SUBC	m	m	m	m	-
AND	-	-	m	m	m
ANDXY	-	-	m	m	m
OR	-	-	m	m	m
ORXY	-	-	m	m	m
XOR	-	-	m	m	m
XORXY	-	-	m	m	m
SHL	-	m	m	m	m
SHR	-	m	m	m	m

Note) The meaning of the symbol are following this ...

V : Over flow flag

C : Carry flag

N : Negative sign flag

Z : Zero flag

B : Bitwise XOR set flag

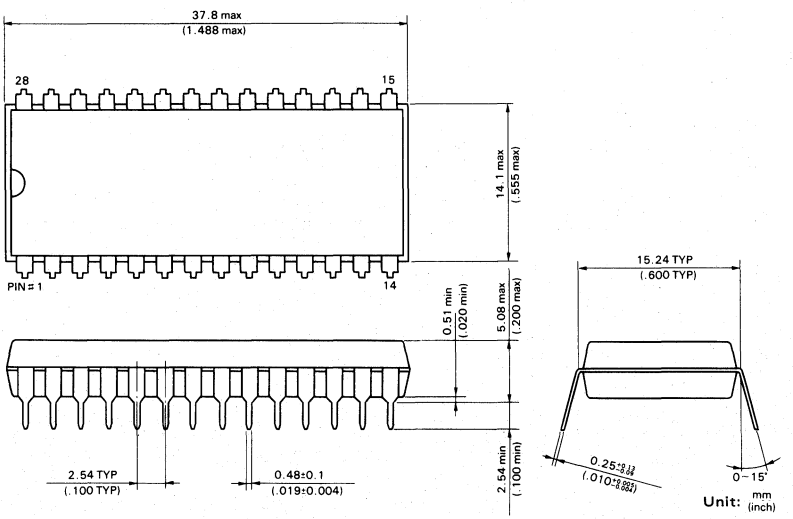
m : Flag bit change

■ CONDITIONED INSTRUCTION TABLE

Alias	Pattern	Logic	Description
⟨cond⟩	ccccc		
)s	00000	$N \& V \& \overline{Z} \mid \overline{N} \& \overline{V} \& \overline{Z}$	Signed strictly greater than
⟨=s	00001	$\overline{(N \& V \& \overline{Z} \mid \overline{N} \& \overline{V} \& \overline{Z})}$	Signed less than or equal
)=s	00010	$N \& V \mid \overline{N} \& \overline{V}$	Signed greater than or equal
⟨s	00011	$\overline{(N \& V \mid \overline{N} \& \overline{V})}$	Signed strictly less than
m	00100	N	Sign bit set (minus)
p	00101	$\overline{N}$	Sign bit reset (plus)
)u	00110	$\overline{C} \& \overline{Z}$	Unsigned strictly greater than
⟨=u	00111	$\overline{(C \& \overline{Z})}$	Unsigned less than or equal
)=u	01000	$\overline{C}$	Unsigned greater than or equal
⟨u	01001	C	Unsigned strictly less than
v	01010	V	Overflow
!v	01011	$\overline{V}$	Not overflow
!iu0	01100	$\overline{IU}0$	P0 not equal to T0
!iu1	01101	$\overline{IU}1$	P1 not equal to T1
=	01110	Z	Equal
!=	01111	$\overline{Z}$	Not equal
t	10000	1	Always
!t	10001	0	Never
ah7	10010	AH[7]	AH register bit 7 (AH[7]) set
ah6	10011	AH[6]	AH register bit 6 (AH[6]) set
ah5	10100	AH[5]	AH register bit 5 (AH[5]) set
ah4	10101	AH[4]	AH register bit 4 (AH[4]) set
ah3	10110	AH[3]	AH register bit 3 (AH[3]) set
ah2	10111	AH[2]	AH register bit 2 (AH[2]) set
ah1	11000	AH[1]	AH register bit 1 (AH[1]) set
ah0	11001	AH[0]	AH register bit 0 (AH[0]) set
e0	11010	EVENT[0]	Sense of EVENT[0] pin
e1	11011	EVENT[1]	Sense of EVENT[1] pin
io0	11100	I/O[0]	Sense of I/O[0] pin
io1	11101	I/O[1]	Sense of I/O[1] pin
b	11110	B	Bitwise XOR of AH
!b	11111	$\overline{B}$	Bitwise XNOR of AH

■ PACKAGE DIMENSION

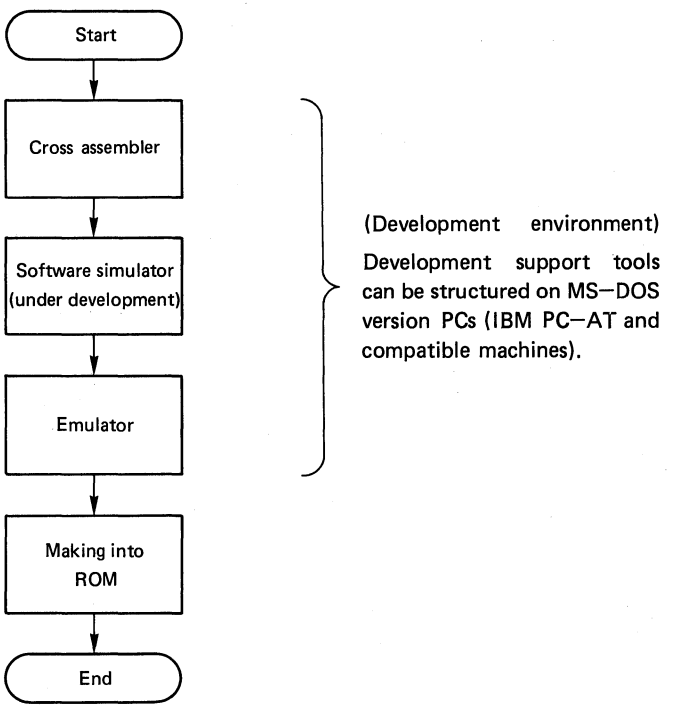
28 pin DIP



■ DEVELOPMENT TOOL

A cross assembler and an emulator are available to efficiently develop application algorithms and software and to debug target systems.

(RP5C72 program development procedure)



● Cross assembler

The cross assembler (XAS71) converts a source code generated by the RP5C72 assembly language into an executable object code.

The source file is generated by an ordinary ASCII file, using an ordinary editor to indicate the instruction in mnemonic. (Use .X71 for the extension of source file)

The object file of the output file is output in Motorola-S format, and can be executed by the emulator or the processor.

The cross assembler (XAS71) can operate on VAX and SUN3 UNIXs and on MS-DOS OSs.

● Emulator

The emulator of the RP5C72 is a support tool for program debugging using actual DSP chips and target systems. It has various functions required for a basic real-time in-circuit emulator.

The main functions are as follows:

- Built-in 12-bit A/D converter for input signals
- Two built-in 16-bit D/A converters for output signals
- Processes the same signals as those given to the RP5C72, with the 28-pin socket.
- Break pointer setting
- Reverse assembler
- Line assembler
- Operation commands for various memories (block transfer and replacement of files and data)
- Develops programs of up to 8 K words.
- Single step function
- A 40–MHz crystal oscillator is built-in. It is also possible to input clocks from an external oscillator.

MS–DOS version PCs (IBM PC–AT and compatible machines) are used as host computers.

6. MEMORY

RICOH

RP/RS53256E

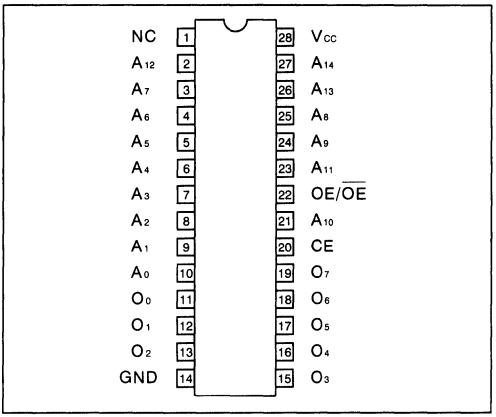
CMOS 256kbit MASK ROM

(32,768 word × 8 bit)

RP/RS53256E is a CMOS Read Only Memory organized as 32768 words × 8 bits and operates from a single 5V supply. The supply current is reduced from 50 mA (Max.) to 100 μA (Max.) by the power down function.

Accoding to your order, the logic of OE signal can be selected as either ACTIVE HIGH or ACTIVE LOW.

■ PIN CONFIGURATION (TOP VIEW)



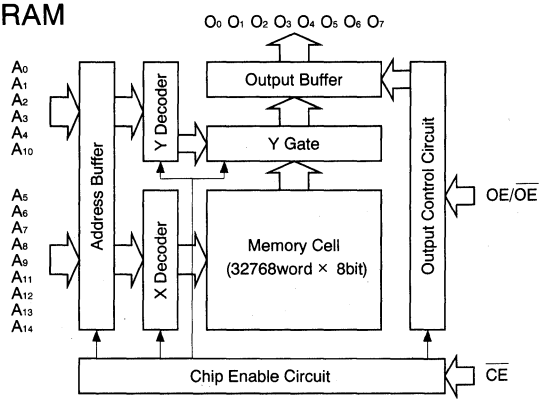
■ FEATURES

1. Organization: 32768 words × 8 bits
2. Access Time: 200 ns
3. TTL Compatible Input/Output
4. Single 5V Power Supply
5. Package RP53256E · · · 28pin DIP
   RS53256E · · · 28pin SOP

■ PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_{14}$	Address Input
$O_0 \sim O_7$	Data Output
OE/$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
V_{CC}	Power Supply (+5V)
GND	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	− 0.3 ~ 7	V
V_I	Input Voltage		− 0.3 ~ V_{CC} + 0.3	V
V_O	Output Voltage		− 0.3 ~ V_{CC} + 0.3	V
Pd	Power Consumption	Ta = 25℃	350	mW
Topr	Operating Temperature		0 ~ 70	℃
Tstg	Storage Temperature		− 40 ~ 125	℃

■ RECOMMENDED OPERATING CONDITION (Ta=0~70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃、Vcc=5V ±10%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current (Operation)	t_{RC} = 200 ns			50	mA
I_{SB1}	Supply Current (Stand by)	$\overline{CE}$ = V_{IH}			2	mA
I_{SB2}		$\overline{CE}$ = V_{CC} − 0.2V			100	μA
V_{OH}	" H " Output Voltage	I_{OH} = − 0.4 mA	2.4			V
V_{OL}	" L " Output Voltage	I_{OL} = 1.6 mA			0.4	V
V_{IH}	" H " Input Voltage		2.2		V_{CC}	V
V_{IL}	" L " Input Voltage		− 0.3		0.8	V
I_{LI}	Input Lenkage Current	V_I = 0V ~ V_{CC}	− 10		10	μA
I_{LO}	Output Leakage Current	V_O = 0V ~ V_{CC} Chip Deselected	− 10		10	μA

The supply current is measured at output open state.

●AC ELECTRICAL CHARACTERISTICS (T_a=0～70℃、V_{CC}=5V ±10%)

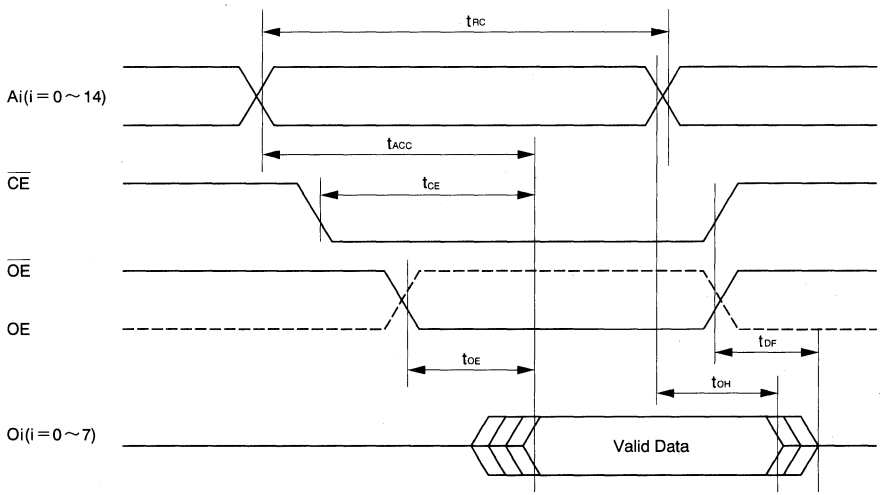
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	200			ns
t_{ACC}	Address Access Time			200	ns
t_{CE}	Chip Enable Access Time			200	ns
t_{OE}	Output Enable Access Time			80	ns
t_{DF}	Output Floating Delay Time	0		80	ns
t_{OH}	Output Hold Time	0			ns

Input Voltage : V_{IL} = 0.6V、 V_{IH} = 2.4V 、 tr、tf = 10 ns

Output Load : 1 TTL + 100 pF

Measuring Voltage : V_{IL} = 0.8V、 V_{IH} = 2.2V 、 V_{OL} = 0.8V 、 V_{OH} = 2.2V

●TIMING CHART

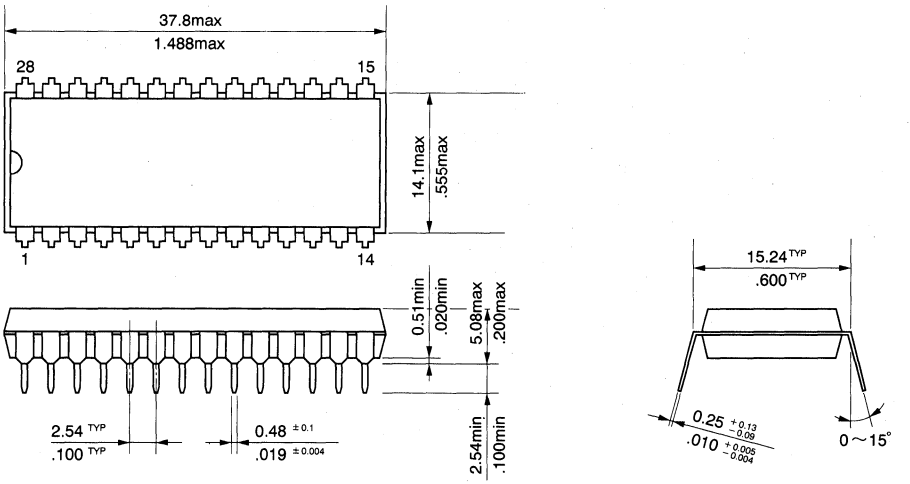


●CAPACITANCE

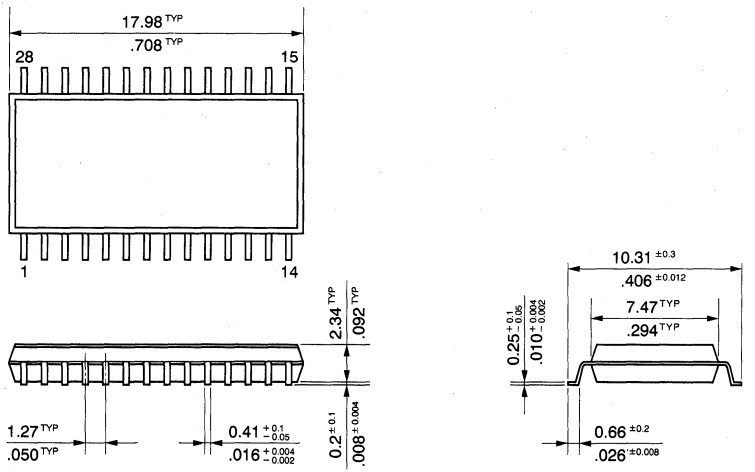
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ci	Input Capacitance	f = 1MHz			10	pF
Co	Output Capacitance				12	pF

■ PACKAGE DIMENSION (Unit : mm/inch)

●28PIN DIP (RP53256E)



●28PIN SOP (RS53256E)



RP/RS531010E

CMOS 1Mbit MASK ROM

(131,072 word × 8 bit)

RP/RS531010E is a 1 Mbit programmable mask ROM using CMOS process technology.

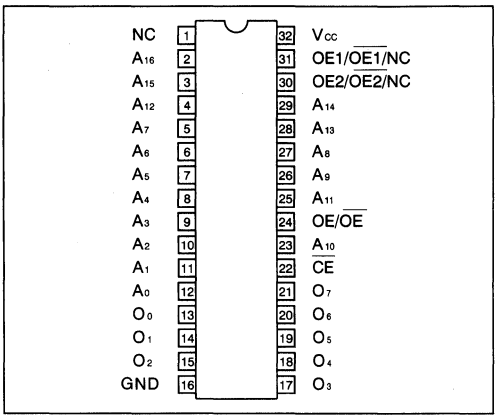
It has also been provided with a power down function which reduces supply current from 30mA (Max.) to 100μA (Max.) by setting the $\overline{CE}$ input to the "H" level.

In addition, the logic level of the output enable can be selected from among three types of logic levels, ACTIVE HIGH, ACTIVE LOW and ISOLATED.

■ FEATURES

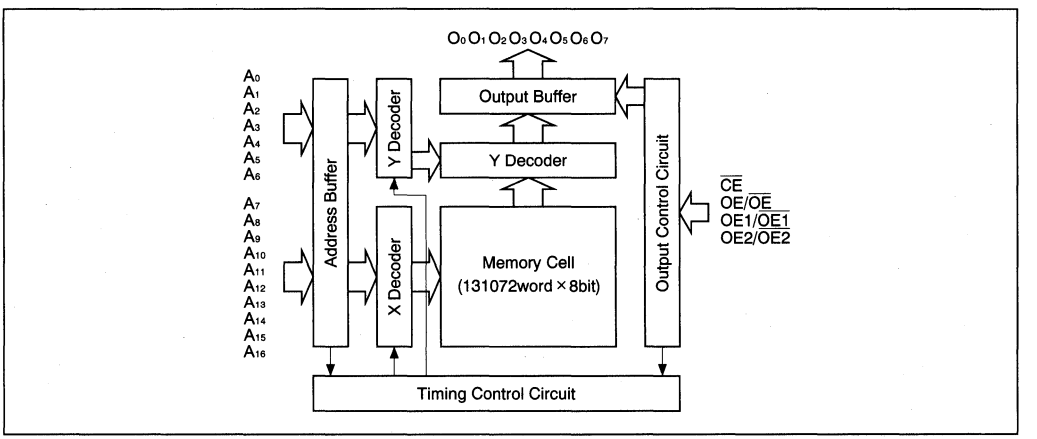
1. Organization : 131072 words x 8 bits
2. Access Time : 200 ns
3. TTL Compatible Input/Output
4. Single 5V Power Supply
5. Power Consumption :
   operation 165 mW (Max.)
   standby 0. 55 mW (Max.)
6. 3 - state Output
7. Package : RP531010E · · · 32 pin DIP
   RS531010E · · · 32 pin SOP

■ PIN CONFIGURATION (TOP VIEW)



■ PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_{16}$	Address Input
$O_0 \sim O_7$	Data Output
OE/$\overline{OE}$	Output Enable Input
OE1/$\overline{OE1}$	Output Enable Input
OE2/$\overline{OE2}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
V_{CC}	Power Supply (+ 5V)
GND	Ground
NC	No connection



■ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	− 0.3 ~ 7	V
V_I	Input Voltage		− 0.3 ~ V_{CC} + 0.5	V
V_O	Output Voltage		− 0.3 ~ V_{CC} + 0.3	V
Pd	Power Consumption	Ta = 25 ℃	210	mW
Topr	Operating Temperature		0 ~ 70	℃
Tstg	Storage Temperature		− 40 ~ 125	℃

■ RECOMMENDED OPERATING CONDITION (Ta=0~70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	" H " Input Voltage	2.2		V_{CC}	V
V_{IL}	" L " Input Voltage	0		0.8	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

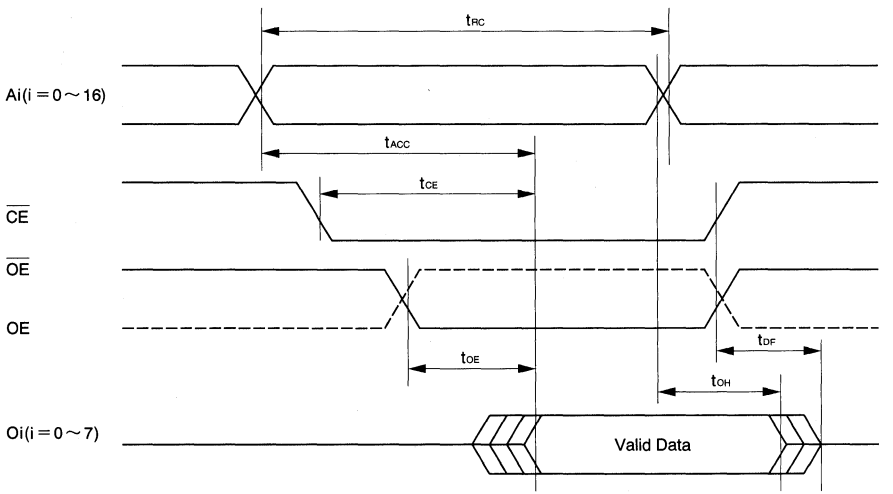
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{SB1}	Supply Current (Standby)	Io = 0 mA, $\overline{CE}$ = 2.2V Total input = 2.2Vor 0.8V			3	mA
I_{SB2}	Supply Current (Standby)	Io=0 mA, $\overline{CE}$ = Vcc−0.2V Total input = Vcc − 0.2V or GND+0.2V			0.1	mA
I_{CC1}	Supply Current (Operation)	Io = 0 mA, t_{RC} = 200 ns			30	mA
I_{CC2}	Supply Current (Operation)	t_{RC} = 1 μs (CL = 100PF) $\overline{CE}$, $\overline{OE}$ = GND + 0.2V V_{IL} = GND + 0.2V V_{IH} = Vcc − 0.2V			10	mA
V_{OH1}	" H " Output Voltage	I_{OH} = − 0.4 mA	2.4			V
V_{OH2}	" H " Output Voltage	I_{OH} = − 0.1 mA	Vcc × 0.8			V
V_{OL}	" L " Output Voltage	I_{OL} = 3.2 mA			0.4	V
V_{IH}	" H " Input Voltage		2.2		Vcc	V
V_{IL}	" L " Input Voltage		− 0.3		0.8	V
I_{LI}	Input Leakage Current	V_I = 0V ~ Vcc	− 10		10	μA
I_{LO}	Output Leakage Current	Vo = 0V ~ Vcc Chip Deselected	− 10		10	μA

● AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	200			ns
t_{ACC}	Address Access Time			200	ns
t_{CE}	Chip Enable Access Time			200	ns
t_{OE}	Output Enable Access Time			80	ns
t_{DF}	Output Floating Delay Time	0		80	ns
t_{OH}	Output Hold Time	0			ns

Input Voltage : V_{IL} = 0.6V, V_{IH} = 2.4V, tr, tf = 10 ns
Output Load : 1 TTL + 100 pF
Measuring Voltage : V_{IL} = 0.8V, V_{IH} = 2.2V, V_{OL} = 0.8V, V_{OH} = 2.2V

● TIMING CHART



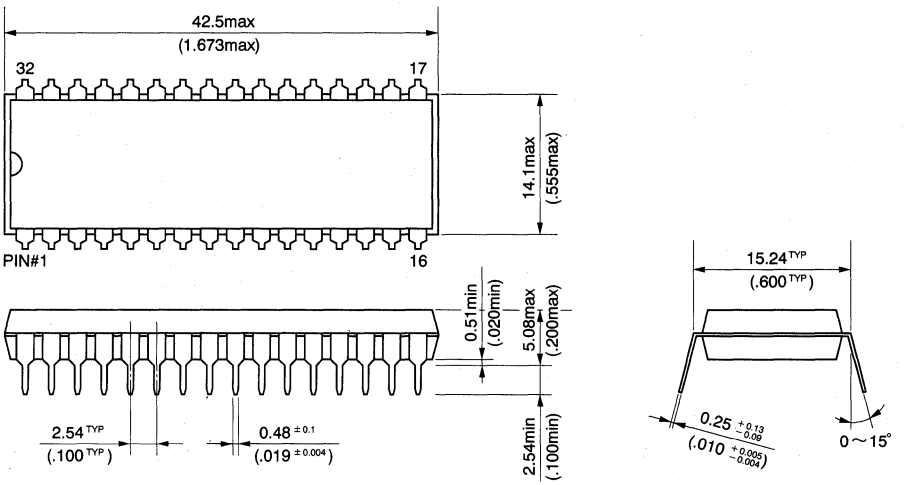
NOTE
(Valid data after power on)
After power on, with $\overline{CE}$ set to GND level, valid data output will be sent after t_{ACC}, from a change in at least one address input.
If other than the above parameters, the valid data output will be sent after t_{CE} due to the $\overline{CE}$ rise pulse.

● CAPACITANCE

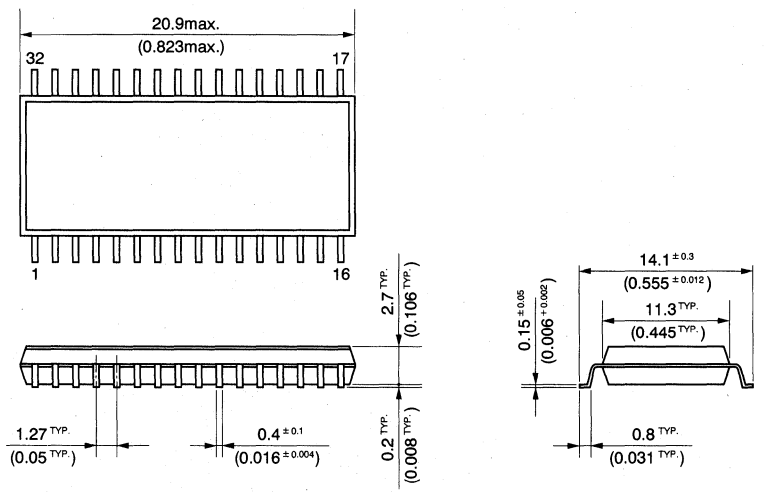
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ci	Input Capacitance	f = 1MHz			10	pF
Co	Output Capacitance				15	pF

■ PACKAGE DIMENSION (Unit:mm/inch)

● 32PIN DIP (RP531010E)



● 32PIN SOP (RS531010E)



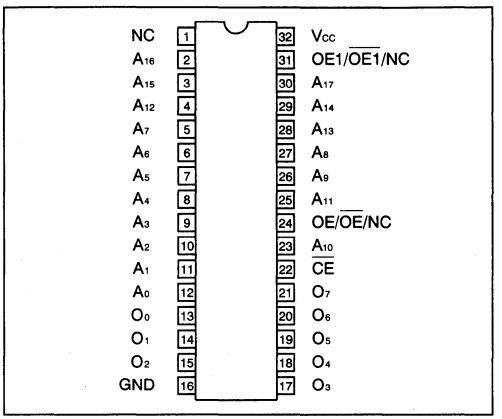
RP/RS532010E

CMOS 2Mbit MASK ROM

(262,144 word × 8 bit)

RP/RS532010E is a 2 Mbit programmable mask ROM using CMOS process technology.
It has also been provided with a power down function which reduces supply current from 50 mA (Max.) to 100 μA (Max.) by setting the $\overline{CE}$ input to the " H " level.
In addition, the logic level of the number 31 pin output enable can be selected from among three types of logic levels, ACTIVE HIGH, ACTIVE LOW and ISOLATED. Further the logic level of the number 24 pin output enable can be specified from among two types either ACTIVE HIGH or ACTIVE LOW.

■ PIN CONFIGURATION (TOP VIEW)

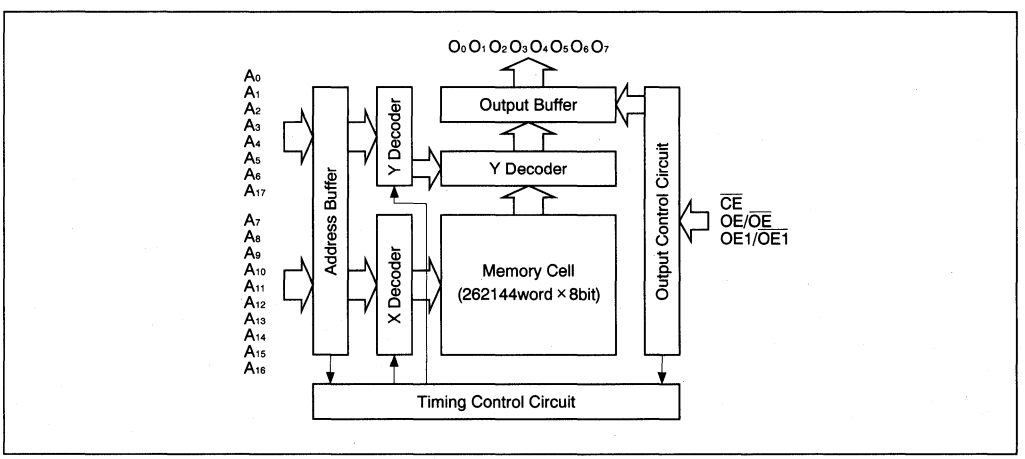


■ FEATURES

1. Organization : 262144 words x 8 bits
2. Access Time : 200 ns
3. TTL Compatible Input/Output
4. Single 5V Power Supply
5. Power Consumption :
   operation 275 mW (Max.)
   standby 0. 55 mW (Max.)
6. 3 - state Output
7. Package : RP532010E · · · 32 pin DIP
   RS532010E · · · 32 pin SOP

■ PIN DESCRIPTION (TOP VIEW)

Pin Name	Function
A0～A17	Address Input
O0～O7	Data Output
OE/$\overline{OE}$	Output Enable Input
OE1/$\overline{OE1}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
VCC	Power Supply (+5V)
GND	Ground
NC	No connection



■ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	− 0.3 ~ 7	V
V_I	Input Voltage		− 0.3 ~ V_{CC} + 0.5	V
V_O	Output Voltage		− 0.3 ~ V_{CC} + 0.3	V
Pd	Power Consumption	Ta = 25 ℃	350	mW
Topr	Operating Temperature		0 ~ 70	℃
Tstg	Storage Temperature		− 40 ~ 125	℃

■ RECOMMENDED OPERATING CONDITION (Ta=0~70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	" H " Input Voltage	2.2		V_{CC}	V
V_{IL}	" L " Input Voltage	0		0.8	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{SB1}	Supply Current (Standby)	Io = 0 mA, $\overline{CE}$ = 2.2V Total input = 2.2V or 0.8V			3	mA
I_{SB2}	Supply Current (Standby)	Io = 0 mA, $\overline{CE}$ = V_{CC} − 0.2V Total input = V_{CC} − 0.2V or GND + 0.2V			0.1	mA
I_{CC1}	Supply Current (Operation)	Io = 0 mA, t_{RC} = 200 ns			50	mA
I_{CC2}	Supply Current (Operation)	t_{RC} = 1 µs (CL = 100PF) $\overline{CE}$, $\overline{OE}$ = GND + 0.2V V_{IL} = GND + 0.2V V_{IH} = V_{CC} − 0.2V			10	mA
V_{OH1}	" H " Output Voltage	I_{OH} = − 0.4 mA	2.4			V
V_{OH2}	" H " Output Voltage	I_{OH} = − 0.1 mA	V_{CC} × 0.8			V
V_{OL}	" L " Output Voltage	I_{OL} = 3.2 mA			0.4	V
V_{IH}	" H " Input Voltage		2.2		V_{CC} + 0.3	V
V_{IL}	" L " Input Voltage		− 0.3		0.8	V
I_{LI}	Input Leakage Current	V_I = 0V ~ V_{CC}	− 10		10	µA
I_{LO}	Output Leakage Current	V_O = 0V ~ V_{CC} Chip Deselected	− 10		10	µA

● AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

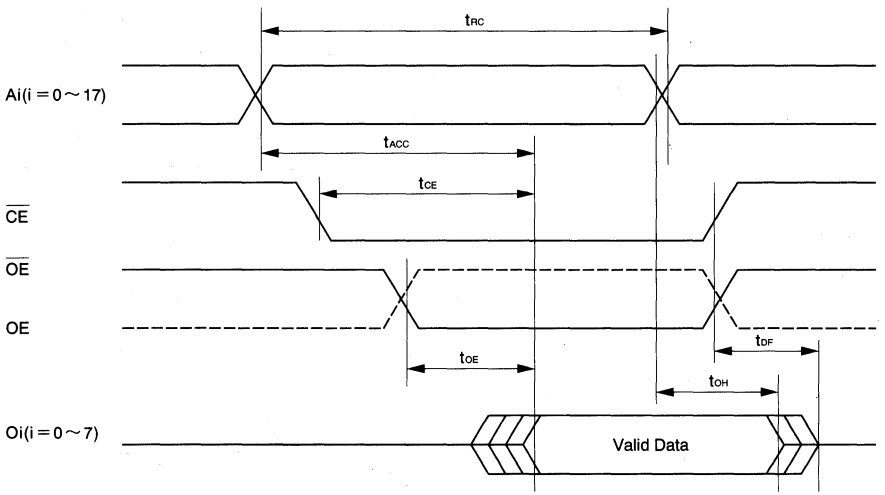
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	200			ns
t_{ACC}	Address Access Time			200	ns
t_{CE}	Chip Enable Access Time			200	ns
t_{OE}	Output Enable Access Time			80	ns
t_{DF}	Output Floating Delay Time	0		80	ns
t_{OH}	Output Hold Time	0			ns

Input Voltage : V_{IL} = 0.6V, V_{IH} = 2.4V, tr, tf = 10 ns

Output Load : 1 TTL + 100 pF

Measuring Voltage : V_{IL} = 0.8V, V_{IH} = 2.2V, V_{OL} = 0.8V, V_{OH} = 2.2V

● TIMING CHART



NOTE

(Valid data after power on)

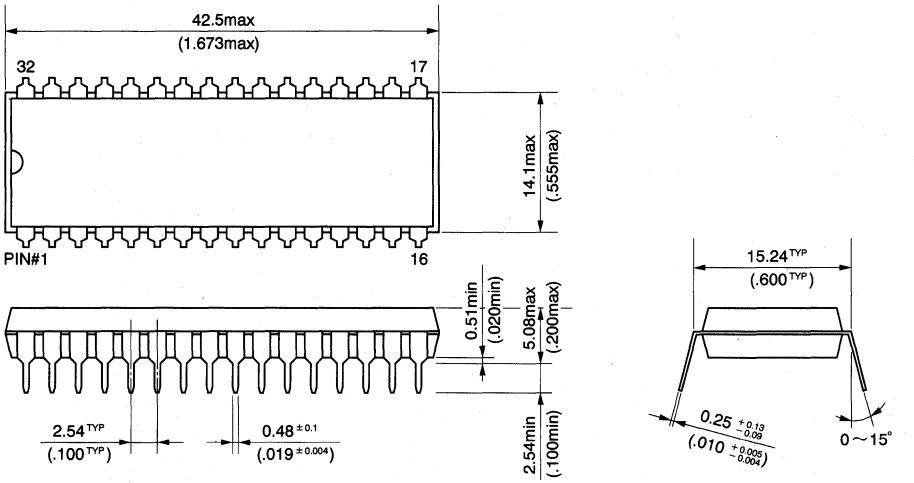
After power on, with $\overline{CE}$ set to GND level, valid data output will be sent after t_{ACC}, from a change in at least one address input. If other than the above parameters, the valid data will be sent after t_{CE} due to the $\overline{CE}$ rise pulse.

● CAPACITANCE

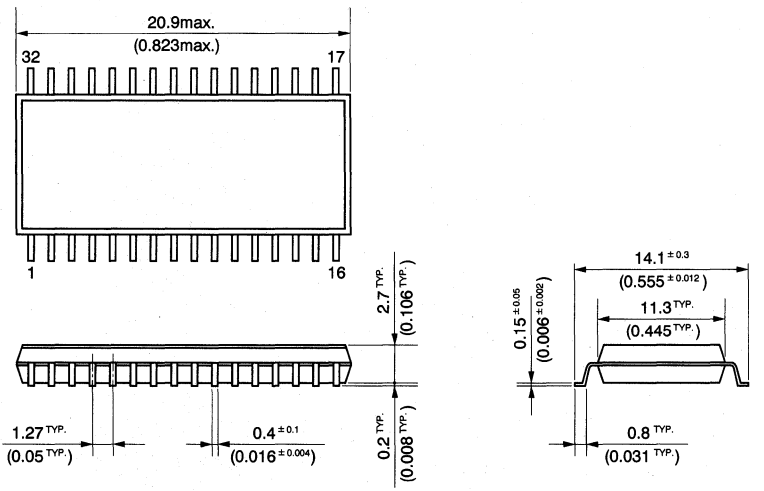
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ci	Input Capacitance	f = 1MHz			10	pF
Co	Output Capacitance				15	pF

■ PACKAGE DIMENSION (Unit:mm/inch)

● 32PIN DIP (RP531010E)



● 32PIN SOP (RS531010E)



RP/RF534040E

CMOS 4Mbit MASK ROM

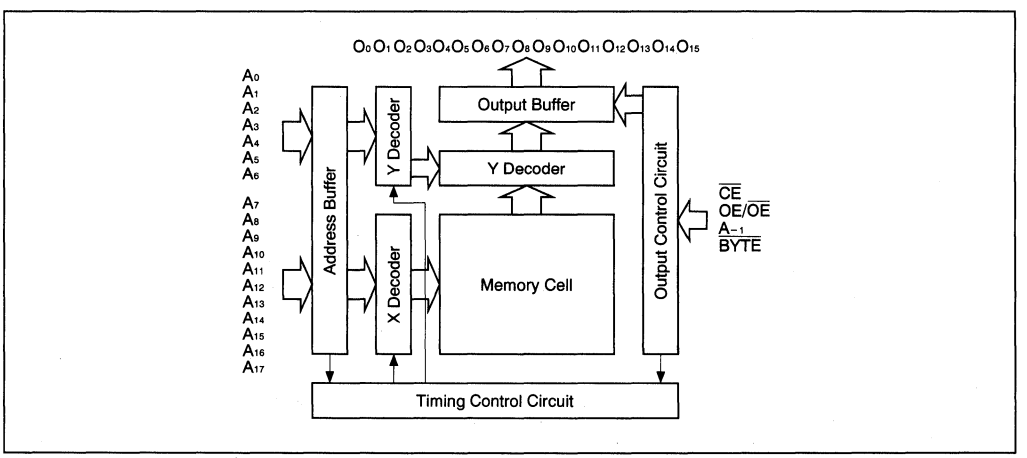
(524,288 word × 8 bit / 262,144 word × 16 bit)

RP/RF534040E is a 4 Mbit programmable mask ROM using CMOS process technology.
It has also been provided with a power down function which reduces supply current from 50mA (Max.) to 100 μA (Max.) by setting the $\overline{CE}$ input to the " H " level.
In addition, the logic level of the output enable can be selected from among three types of logic levels, ACTIVE HIGH, ACTIVE LOW and ISOLATED.

■ FEATURES

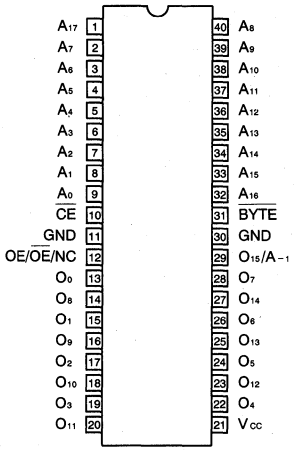
1. Organization : 524288 words x 8 bits
   262144 words x 16 bits
2. Access Time : 200 ns
3. TTL Compatible Input/Output
4. Single 5V Power Supply
5. Power Consumption : operation 275 mW (Max.)
   standby 0. 55 mW (Max.)
6. 3 - state Output
7. Package : RP534040E · · · 40 pin DIP
   RF534040E · · · 64 pin QFP

■ BLOCK DIAGRAM

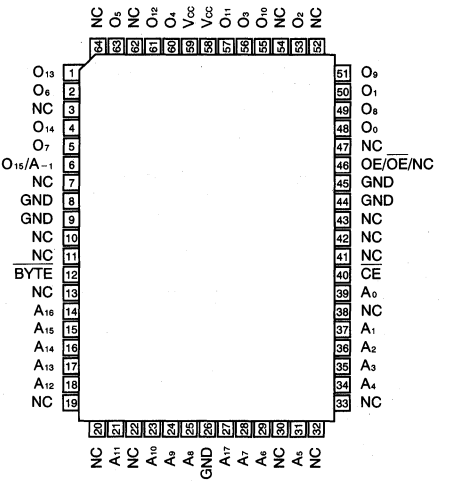


■ PIN DESCRIPTION

● RP534040E (40PIN DIP)



● RF534040E (64PIN QFP)



■ PIN DESCRIPTION

Pin Name	Function
A_{-1}～A_{17}	Address Input
O_0～O_{15}	Data Output
OE/$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
$\overline{BYTE}$	BYTE output/WORD MODE swiching
Vcc	Power Supply (+5V)
GND	Ground
NC	No connection

■ OUTPUT MODE SWITCHING

Output mode switching is done by $\overline{BYTE}$ input. $\overline{BYTE}$ input at high level sets to WORD MODE (16 bit output). $\overline{BYTE}$ input at low level sets to BYTE MODE (8 bit output). During BYTE MODE the O_{15} output pin switches to A_{-1} input pin.

$\overline{CE}$	$\overline{OE}$ (OE)	$\overline{BYTE}$	A_{-1} (O_{15})	O_0～7	O_8～15	MODE	LSB	MSB
H	X	X	X	Hi－Z	Hi－Z	Standby	–	–
L	H (L)	X	X	Hi－Z	Hi－Z	Output Hi－Z	–	–
L	L (H)	H	Inhibit	O_0～7	O_8～15	WORD	A_0	A_{17}
L	L (H)	L	L	O_0～7	Hi－Z	BYTE	A_{-1}	A_{17}
L	L (H)	L	H	O_8～15	Hi－Z			

(Note) X : Don't Care
Hi －Z : High Impedance

■ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	− 0.3 ~ 7	V
V_I	Input Voltage		− 0.3 ~ V_{CC} + 0.5	V
V_O	Output Voltage		− 0.3 ~ V_{CC} + 0.3	V
Pd	Power Consumption	Ta = 25 ℃	350	mW
Topr	Operating Temperature		0 ~ 70	℃
Tstg	Storage Temperature		− 40 ~ 125	℃

■ RECOMMENDED OPERATING CONDITION (Ta=0~70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	" H " Input Voltage	2.2		V_{CC}	V
V_{IL}	" L " Input Voltage	0		0.8	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{SB1}	Supply Current (Standby)	*1			0.1	mA
I_{SB2}	Supply Current (Standby)	*2			2	mA
I_{CC}	Supply Current (Operation)	I_O = 0 mA, t_{RC} = 200 ns			50	mA
V_{OH}	" H " Output Voltage	I_{OH} = − 0.4 mA	2.4			V
V_{OL}	" L " Output Voltage	I_{OL} = 2.5 mA			0.4	V
V_{IH}	" H " Input Voltage		2.2		V_{CC}+0.3	V
V_{IL}	" L " Input Voltage		− 0.3		0.8	V
I_{LI}	Input Leakage Current	V_I = 0V ~ V_{CC}	− 10		10	μA
I_{LO}	Output Leakage Current	V_O = 0V ~ V_{CC} Chip Deselected	− 10		10	μA

*1 : CE = Vcc − 0.2V, Total input = 0.2V or Vcc − 0.2V, Io = 0 mA

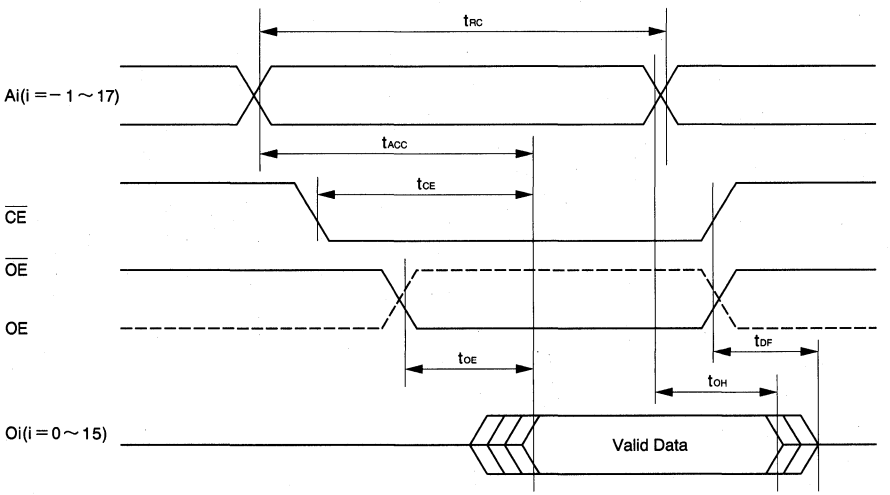
*2 : $\overline{CE}$ = 2.2V, Total input = 0.8V or 2.2V, Io = 0 mA

● AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	200			ns
t_{ACC}	Address Access Time			200	ns
t_{CE}	Chip Enable Access Time			200	ns
t_{OE}	Output Enable Access Time			80	ns
t_{DF}	Output Floating Delay Time	0		80	ns
t_{OH}	Output Hold Time	0			ns

Input Voltage : V_{IL} = 0.6V, V_{IH} = 2.4V, tr, tf = 10 ns
Output Load : 1 TTL + 100 pF
Measuring Voltage : V_{IL} = 0.8V, V_{IH} = 2.2V, V_{OL} = 0.8V, V_{OH} = 2.2V

● TIMING CHART



NOTE

(Valid data after power on)

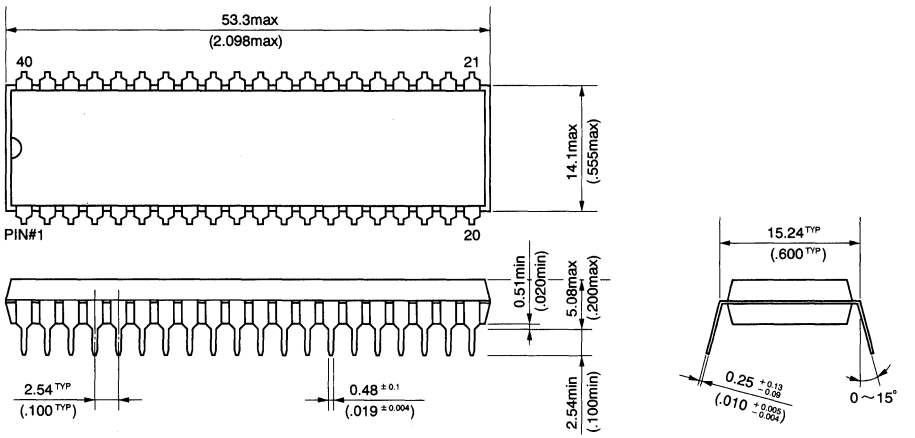
After power on, with $\overline{CE}$ set to GND level, valid data output will be sent after t_{ACC}, from a change in at least one address input. If other than the above parameters, the valid data output will be sent after t_{CE} due to the $\overline{CE}$ rise pulse.

● CAPACITANCE

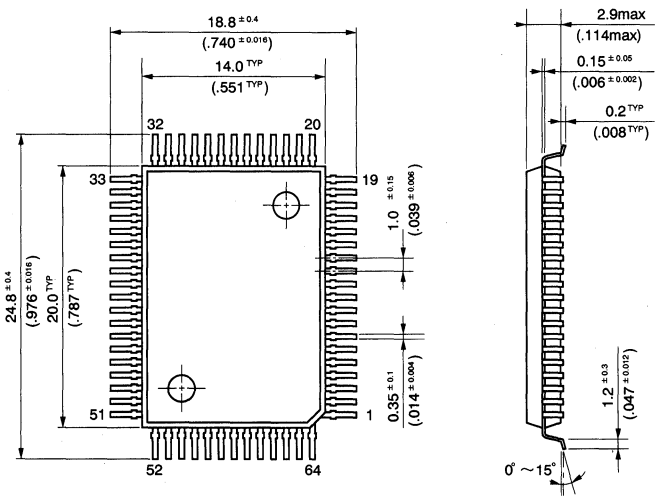
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ci	Input Capacitance	f = 1MHz			10	pF
Co	Output Capacitance				15	pF

■ PACKAGE DIMENSION (Unit : mm/inch)

● 40PIN DIP (RP534040E)



● 64PIN QFP (RF534040E)



RICOH

RP2364E

NMOS 64 Kbit MASK ROM
(8,192 word × 8 bit)

■ GENERAL DESCRIPTION

The RP2364E is static NMOS Read Only Memory organized as 8,192 words by 8-bits and operate from a single +5V supply.

The RP2364E features automatic power-down mode. When Chip Enable ($\overline{CE}$) goes HIGH level, the supply current is reduced from 100mA (max.) to 20mA (max.).

The device has Chip Enable ($\overline{CE}$) input and output Enable (OE/$\overline{OE}$) inputs allowing up to 32 wired ORs to be tied without external decoding.

According to your order, logic of the following pins may be selected ACTIVE LOW or ACTIVE HIGH or NC.

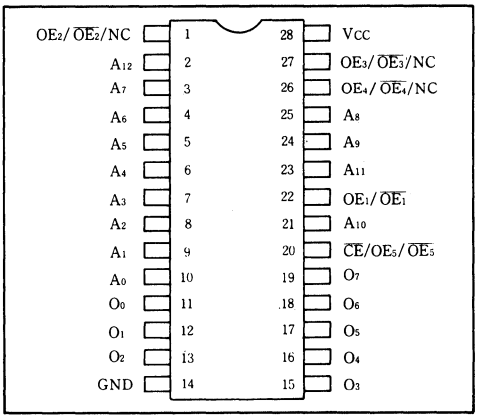
Pins 1, 22, 26 and 27.

and Pin 20 may be selected as $\overline{CE}$ or $\overline{OE}$.

■ FEATURES

- 8,192 words×8 bits organization
- Low power dissipation: Active 550mW max.
  Standby 110mW max.
- Fast access time: 200ns max.
- Single +5V(±10%) power supply
- Completely TTL compatible: All outputs and inputs

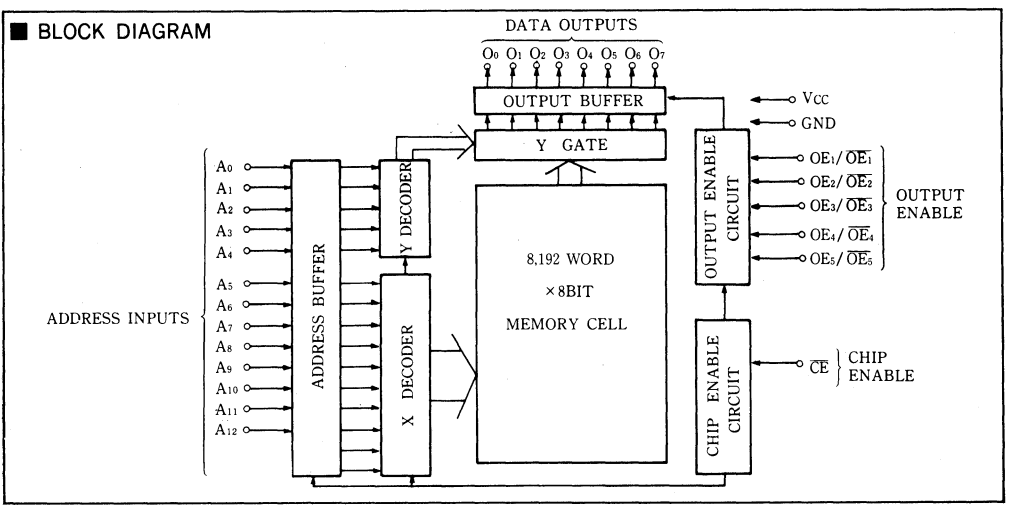
■ PIN CONFIGURATION (Top view)



■ PIN DESCRIPTION

PIN NAME	FUNCTION
A0 ~ A12	Address Input
O0 ~ O7	Data Output
$\overline{OE}_1$ ~ $\overline{OE}_5$	Output Enable
$\overline{CE}$	Chip Enable
NC	No Connection
Vcc	Power Supply
GND	GND

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.5～7	V
V_I	Input Voltage		−0.5～7	V
V_O	Output Voltage		−0.5～7	V
Pd	Maximum Power Dissipation	Ta=25℃	700	mW
Topr	Operating Ambient Temperature		0～70	℃
Tstg	Storage Temperature		−40～125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃)

Symbol	Parameter	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.5		0.8	V

■ ELECTRICAL CHARACTERISTICS

●DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{CC}$			20	mA
I_{CC2}	Supply Current (Active)	I_O=0mA			100	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=3.2mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
I_{LI}	Input Leakage Current	V_I=0V～V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current	V_O=0V～V_{CC} Chip Deselected	−10		10	μA

●AC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Valve			Unit
			Min	Typ	Max	
t_{RC}	Read Cycle Time	Output Load= 1TTL+100pF	200			ns
t_{ACC}	Address Access Time				200	ns
t_{CE}	Chip Enable Access Time				200	ns
t_{OE}	Output Enable Access Time				80	ns
t_{DF}	Output Hold Time after Output Enable Change				80	ns
t_{OH}	Output Hold Time after Address Change		0			ns
t_{CH}	Output Hold Time after Chip Enable Change				80	ns

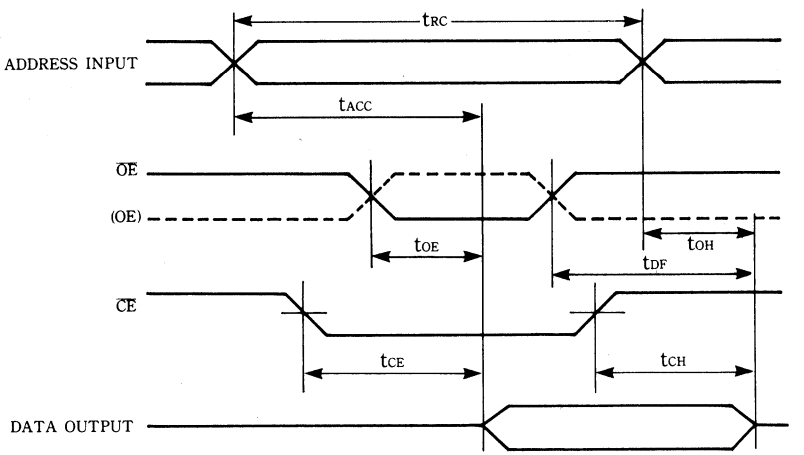
Notes : 1. Input Pulse Levels : V_{IL}=0.6V, V_{IH}=2.2V

2. Output Timing Reference Level : V_{OL}=0.8V, V_{OH}=2.0V

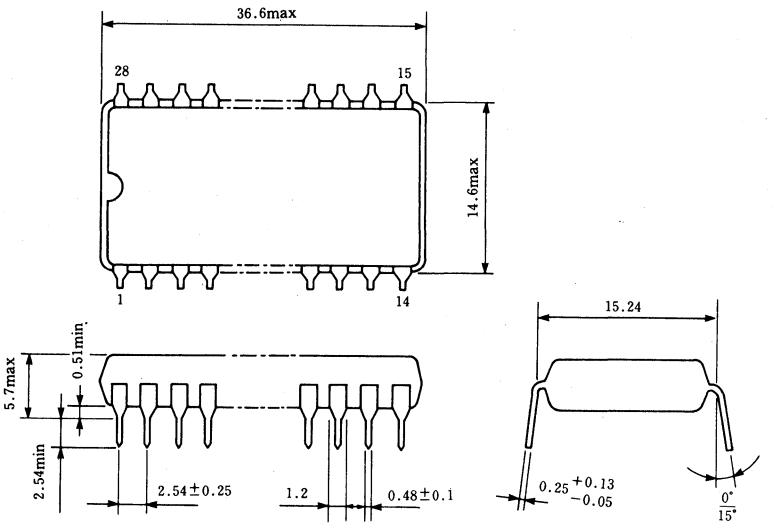
● TERMINAL CAPACITANCE

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
Ci	Input Capacitance	f=1MHz			8	pF
Co	Output Capacitance				12	pF

■ TIMING CHART



■ 28 PIN PLASTIC PACKAGE (Unit: mm)



NMOS 128kbit MASK ROM
(16,384word×8bit)

RP23128E

■ GENERAL DESCRIPTION

The RP23128E is static NMOS Read Only Memory organized as 16,384 words by 8-bits and operate from a single + 5V supply.

The RP23128E features automatic power-down mode. When Chip Enable ($\overline{CE}$) goes HIGH level, the supply current is reduced from 100mA (max.) to 20mA (max.).

These devices have Chip Enable ($\overline{CE}$) input and output Enable (OE/$\overline{OE}$) inputs allowing up to 16 wired ORs to be tied without external decoding.

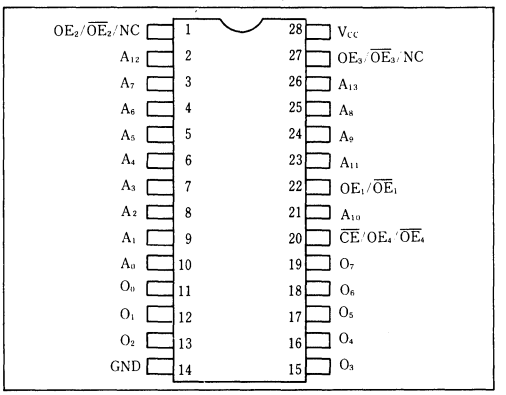
According to your order, logic of the following pins may be selected.

Pin 22 (active low/active high)
Pin 1, 27 (active low/active high/No Connection)
Pin 20 (Chip Enable/active low/active high)

■ FEATURES

- 16,384 words × 8 bits organization
- Low power dissipation: Active 550mW max.
  Standby 110mW max.
- Fast access time: 200ns max.
- Single + 5V (±10%) power supply
- Completely TTL compatible: All outputs and inputs

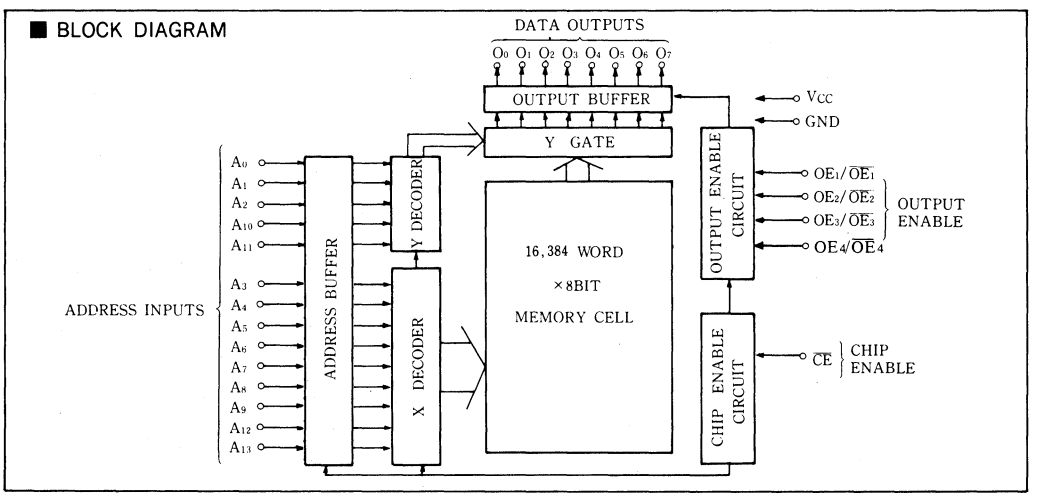
■ PIN CONFIGURATION (Top view)



■ PIN DESCRIPTION

PIN NAME	FUNCTION
$A_0 \sim A_{13}$	Address Input
$O_0 \sim O_7$	Data Output
$\overline{OE}_1 \sim \overline{OE}_4$	Output Enable
$\overline{CE}$	Chip Enable
NC	No Connection
Vcc	Power Supply
GND	GND

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.3～7	V
V_I	Input Voltage		−0.3～Vcc+0.3	V
V_O	Output Voltage		−0.3～Vcc+0.3	V
Pd	Maximum Power Dissipation	Ta=25℃	700	mW
Topr	Operating Ambient Temperature		0～70	℃
Tstg	Storage Temperature		−40～125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃)

Symbol	Parameter	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{CC}$			20	mA
I_{CC2}	Supply Current (Active)	I_O=0mA			100	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=2.0mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		−0.3		0.8	V
I_{LI}	Input Leakage Current	V_I=0V～V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current	V_O=0V～V_{CC} Chip Deselected	−10		10	μA

● AC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

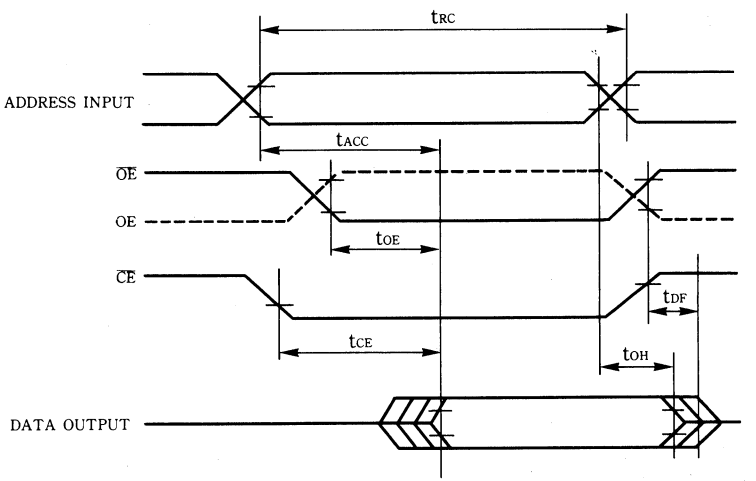
Symbol	Parameter	Specified Valve			Unit
		Min	Typ	Max	
t_{RC}	Read Cycle Time	200			ns
t_{ACC}	Address Access Time			200	ns
t_{CE}	Chip Enable Access Time			200	ns
t_{OE}	Output Enable Access Time			80	ns
t_{DF}	Output Floating Delay Time			80	ns
t_{OH}	Output Hold Time	0			ns

Note) Test Condition
Input Pulse Voltage: V_{IL}=0.6V, V_{IH}=2.4V
Input Pulse Rise/Fall Time: 10ns
Timing Measuring Voltage:
Input V_{IL}=0.8V, V_{IH}=2.2V
Output V_{OL}=0.8V, V_{OH}=2.0V
Output Load: 1TTL + 100pF
(including jig capacitance)

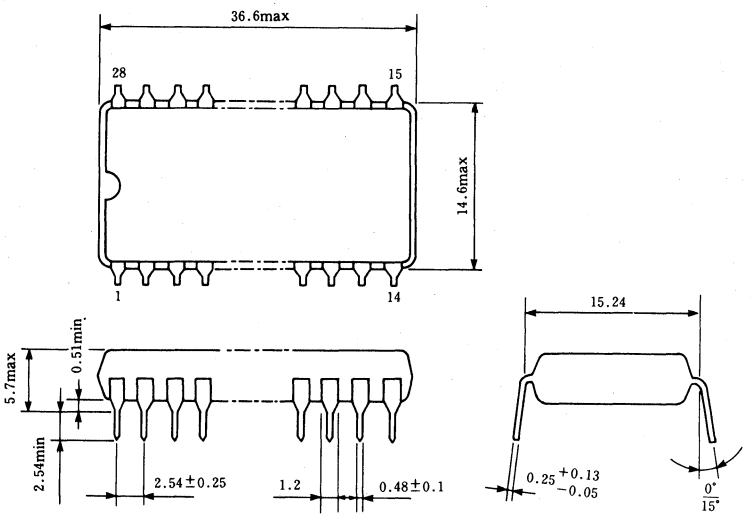
● TERMINAL CAPACITANCE

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
C_i	Input Capacitance	f = 1MHz			8	pF
C_O	Output Capacitance				12	pF

■ TIMING CHART



■ 28 PIN PLASTIC PACKAGE (Unit: mm)



NMOS 256 Kbit MASK ROM
(32,768 word × 8 bit)

RP23256D/E, RP23257D/E

■ GENERAL DESCRIPTION

The RP23256D/E and RP23257D/E are static NMOS Read Only Memories organized as 32,768 words by 8-bits and operate from a single +5V supply.

The RP23256D/E and RP23257D/E features automatic power-down mode. When Chip Enable ($\overline{CE}$) goes HIGH level, the supply current is reduced from 100mA (max.) to 20mA (max.).

These devices have Chip Enable ($\overline{CE}$) input and two output Enable (OE/$\overline{OE}$) inputs allowing up to eight wired ORs to be tied without external decoding.

According to your order, logic of the following pins may be selected ACTIVE LOW or ACTIVE HIGH.

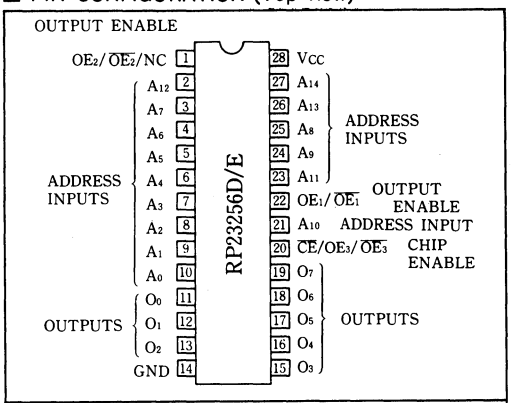
Pins 1, and 22 for RP23256D/E
Pins 1, and 26 for RP23257D/E

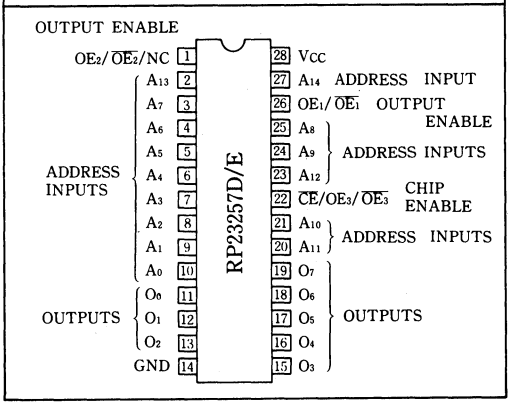
and OE_2 may be changed to NC (No Connection), $\overline{CE}$ may be selected to OE_3.

■ FEATURES

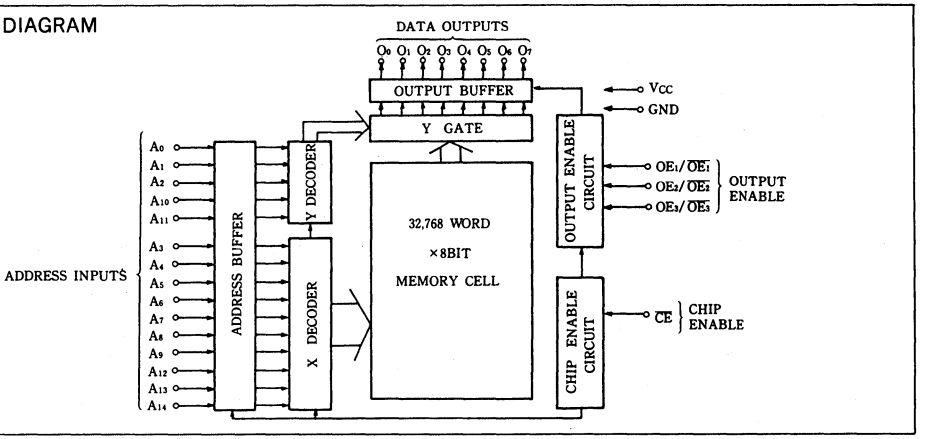
- 32,768 words×8 bits organization
- Low power dissipation: Active 550mW max.
  Standby 110mW max.
- Fast access time: RP23256D/257D 250ns max.
  RP23256E/257E 200ns max.
- Single +5V(±10%) power supply
- Completely TTL compatible: All outputs and inputs
- 3-state outputs for wired-OR expansion
- Pin compatible with: Intel 27256 EPROM (RP23256D/E)
  TI 2564 EPROM (RP23257D/E)

■ PIN CONFIGURATION (Top view)





■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.5～7	V
V_I	Input Voltage		−0.5～7	V
V_O	Output Voltage		−0.5～7	V
Pd	Maximum Power Dissipation	Ta=25℃	700	mW
Topr	Operating Ambient Temperature		0～70	℃
Tstg	Storage Temperature		−40～125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃)

Symbol	Parameter	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.5		0.8	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{CC}$			20	mA
I_{CC2}	Supply Current (Active)	I_O=0mA			100	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=3.2mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
I_{LI}	Input Leakage Current	V_I=0V～V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current	V_O=0V～V_{CC} Chip Deselected	−10		10	μA

● AC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

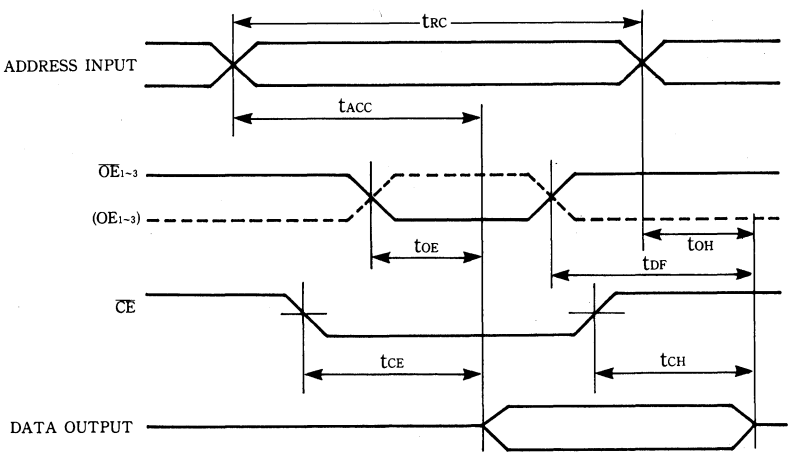
Symbol	Parameter	Test Condition	RP23256D/257D			RP23256E/257E			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	Output Load= 1TTL+100pF	250			200			ns
t_{ACC}	Address Access Time				250			200	ns
t_{CE}	Chip Enable Access Time				250			200	ns
t_{OE}	Output Enable Access Time				100			80	ns
t_{DF}	Output Hold Time after Output Enable Change				100			80	ns
t_{OH}	Output Hold Time after Address Change		0			0			ns
t_{CH}	Output Hold Time after Chip Enable Change				100			80	ns

Notes : 1. Input Pulse Levels : V_{IL}=0.6V, V_{IH}=2.2V
2. Output Timing Reference Level : V_{OL}=0.8V, V_{OH}=2.0V

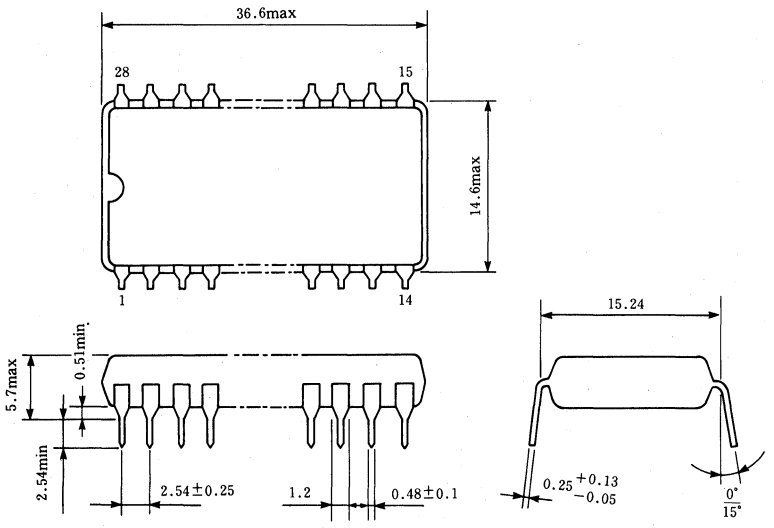
● TERMINAL CAPACITANCE

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
Ci	Input Capacitance	f=1MHz			8	pF
Co	Output Capacitance				12	pF

■ TIMING CHART



■ 28 PIN PLASTIC PACKAGE (Unit: mm)



RP231027D/E

NMOS 1Mbit MASK ROM
(131,072 word × 8 bit)

■ GENERAL DESCRIPTION

The RP231027D/E is a static NMOS read only Memory organized as 131,072 words by 8 bits and operates from a single+5V supply.

The RP231027D/E features automatic power-down mode. When Chip Enable ($\overline{CE}$) goes HIGH level, the supply current is reduced from 100mA (max.) to 30mA (max.).

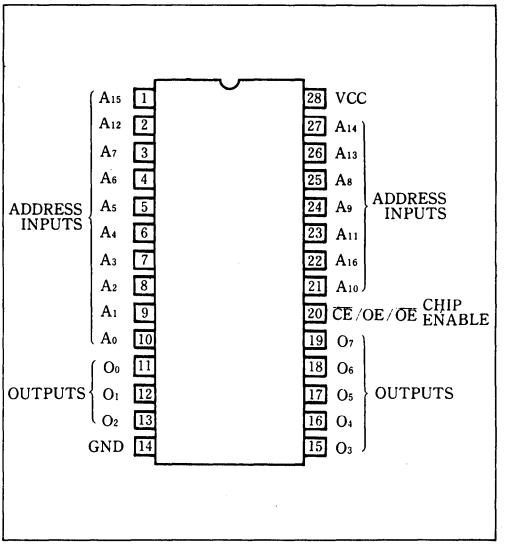
Pin 20 can be used as OE.

According to your order, Logic of the OE pin may be selected ACTIVE LOW or ACTIVE HIGH.

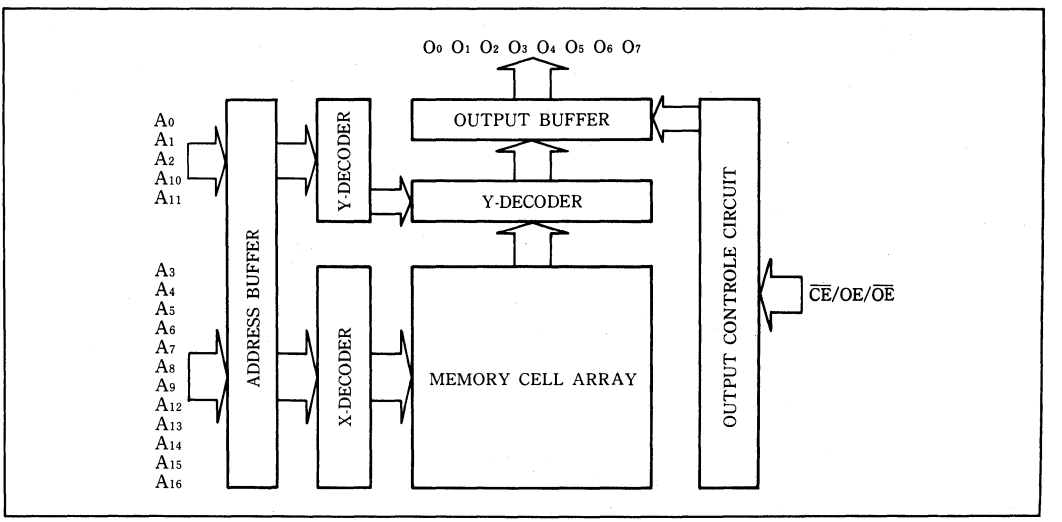
■ FEATURES

- 131,072 words×8 bits organization
- Low power dissipation Active 550mW max.
  Standby 165mW max.
- Fast access time RP231027D 250ns max.
  RP231027E 200ns max.
- Single +5V (±10%) power supply
- Completely TTL compatible: All outputs and inputs
- 3-state outputs for wired-OR expansion
- Pin compatible with Intel 27512

■ PIN CONFIGURATION (Top view)



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.3~7	V
V_I	Input Voltage		−0.3~Vcc+0.3	V
V_O	Output Voltage		−0.3~Vcc+0.3	V
Pd	Maximum Power Dissipation	Ta=25℃	700	mW
Topr	Operating Ambient Temperature		0~70	℃
Tstg	Storage Temperature		−40~125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=0~70℃)

Symbol	Parameter	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{CC}$			30	mA
I_{CC2}	Supply Current (Active)	I_O=0mA			100	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4		V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL}=2.0mA			0.4	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage		−0.3		0.8	V
I_{LI}	Input Leakage Current	$V_I=0V\sim V_{CC}$	−10		10	μA
I_{LO}	Output Leakage Current	$V_O=V_{CC}$, Chip Deselected	−10		10	μA

● AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, V_{CC}=5V±10%)

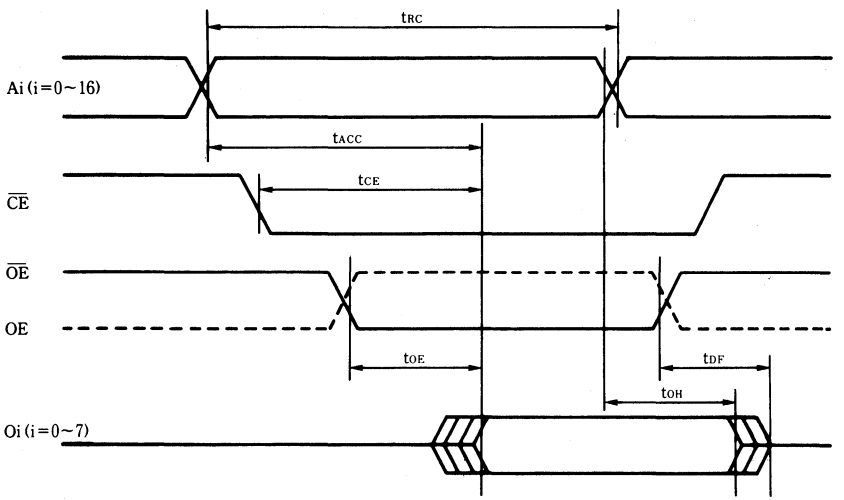
Symbol	Parameter	RP231027D			RP231027E			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	250			200			ns
t_{ACC}	Address Access Time			250			200	ns
t_{CE}	Chip Enable Access Time			250			200	ns
t_{OE}	Output Enable Access Time			100			80	ns
t_{DF}	Output Floating Delay Time	0		100	0		80	ns
t_{OH}	Output Hold Time	0			0			ns

Note) Test Condition
Input Pulse Voltage: V_{IL}=0.6V, V_{IH}=2.4V
Input Pulse Rise/Fall Time: 10ns
Timing Measuring Voltage: Input V_{IL}=0.8V, V_{IH}=2.2V
Output V_{OL}=0.8V, V_{OH}=2.0V
Output Load: 1TTL + 100pF (including jig capacitance)

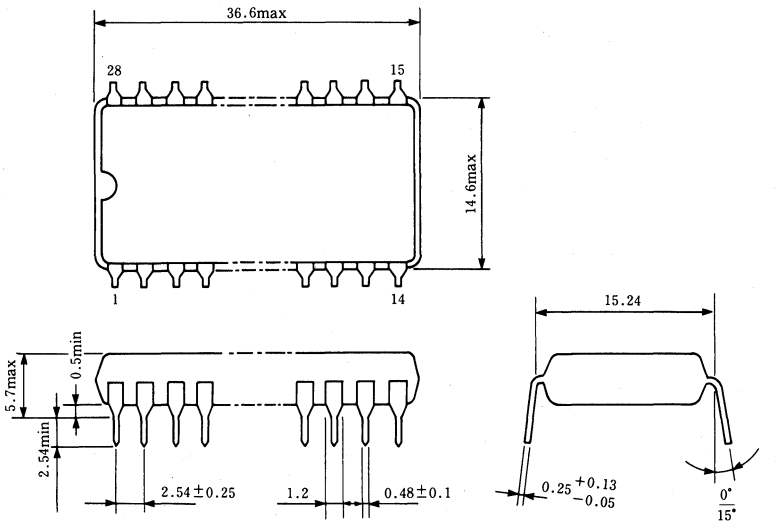
● TERMINAL CAPACITANCE

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
Ci	Input Capacitance	f=1MHz			8	pF
Co	Output Capacitance				12	pF

■ TIMING CHART



■ 28 PIN PLASTIC PACKAGE (Unit:mm)



RICOH

RP234096

NMOS 4Mbit MASK ROM

(524,288word×8bit)

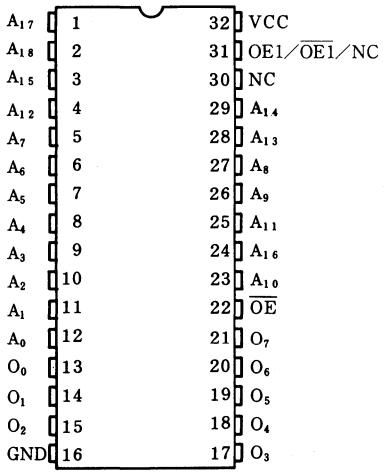
The RP234096 is static NMOS Read Only Memory organized as 524288 words × 8bits and operates from a single +5V Supply. And the consumption current is 50mA (MAX). Tow Output Enable signals allows up to 4 wired ORs.

The Output Enable of the pin31 can be selected as Active High, Active Low or NC (No Connection).

■ FEATURES

1. Organization: 524288words×8bits
2. Access Time: 200ns (MAX.)
3. Input/Output Level: TTL
4. Single 5V power supply
5. Package: 32pin plastic DIP

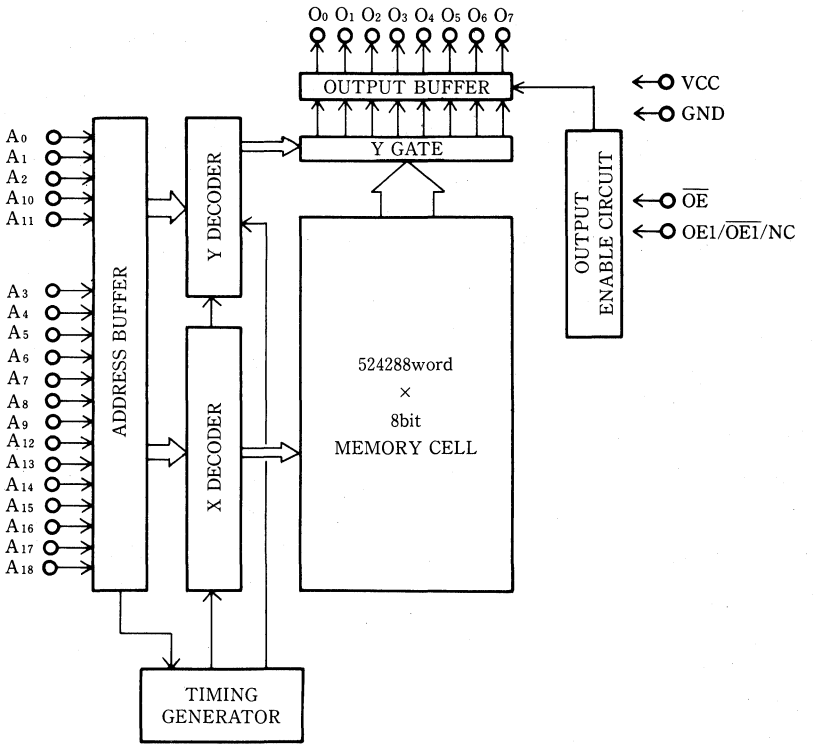
■ PIN CONFIGURATION (Top view)



■ PIN DESCRIPTION

Pin Name	Description
$A_0 \sim A_{18}$	Address Input
$O_0 \sim O_7$	Data Output
$\overline{OE}$	Output Enable Input
OE1/$\overline{OE1}$	Output Enable Input
NC	No Connection
Vcc	Power Supply (+5V)
GND	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Condition	Limit	Unit
Vcc	Supply Voltage	With respect to GND	-0.3 ~ 7	V
VI	Input Voltage		-0.3 ~ Vcc+0.3	V
Vo	Output Voltage		-0.3 ~ Vcc+0.3	V
Pd	Power Consumption	Ta = 25°C	350	mW
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-40 ~ 125	°C

■ RECOMMENDED OPERATING CONDITION (Ta = 0 ~ 70°C)

Symbol	Parameter	MIN.	TYP.	MAX.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
VIH	"H" Input Voltage	2.0		Vcc+0.3	V
VIL	"L" Input Voltage	-0.3		0.8	V

■ ELECTRICAL CHARACTERISTICS

• **DC Electrical Characteristics** (Ta = 0 ~ 70°C, Vcc = 5V±10%)

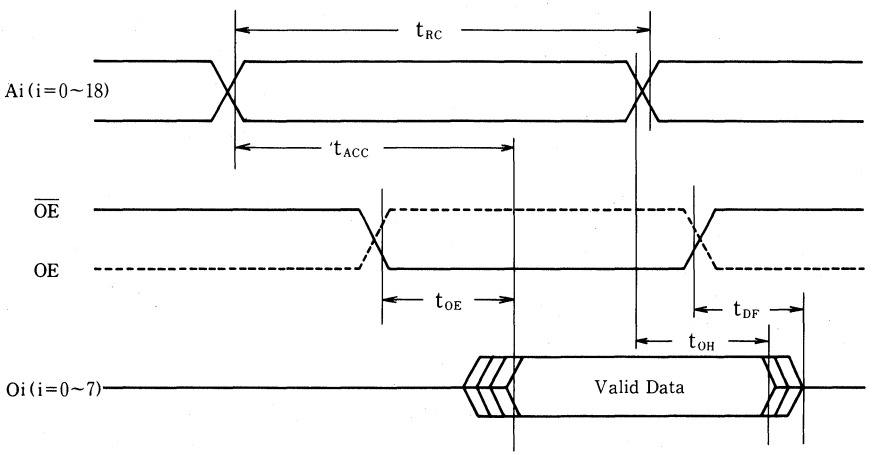
Symbol	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Icc	Supply Current (operation)	Io = 0 mA			50	mA
VOH	"H" Output Voltage	IOH = -400 μA	2.4			V
VOL	"L" Output Voltage	IOL = 3.2 mA			0.4	V
VIH	"H" Input Voltage		2.0		Vcc+0.3	V
VIL	"L" Input Voltage		-0.3		0.8	V
ILI	Input Leakage Current	VI = 0V ~ Vcc	-10		10	μA
ILO	Output Leakage Current	Vo = 0V ~ Vcc Output Deselected	-10		10	μA

● **AC Electrical Characteristics** (Ta = 0~70°C, Vcc = 5V±10%)

Symbol	Parameter	MIN.	TYP.	MAX.	Unit
t_{RC}	Read Cycle Time	200			ns
t_{ACC}	Address Access Time			200	ns
t_{OE}	Output Enable Access Time			80	ns
t_{DF}	Output Floating Delay Time	0		80	ns
t_{OH}	Output Hold Time	0			ns

Note) Test Condition
Input Pulse Voltage: V_{IL} = 0.6V, V_{IH} = 2.4V
Input Pulse Rise/Fall Time: 10 ns
Timing Measuring Voltage: Input V_{IL} = 0.8V, V_{IH} = 2.2V
Output V_{OL} = 0.8V, V_{OH} = 2.2V
Output Load: I_{TTL} + 100pF (Including Jig capacitance)

● **Timing Chart**



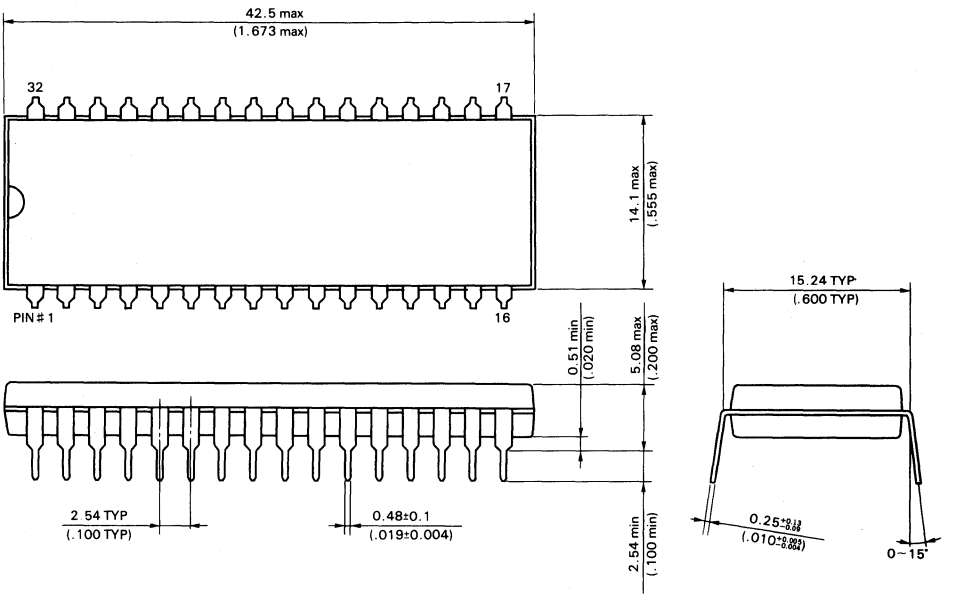
* Valid data at power-on
Valid data is output after t_{ACC} from the change of at least one of the Address Input signals at the power-on.

● **Capacitance**

Symbol	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Ci	Input Capacitance	f = 1MHz			8	pF
Co	Output Capacitance	f = 1MHz			12	pF

■ PACKAGE DIMENSION (unit: $\frac{mm}{(inch)}$)

32 pin DIP



RF/RP5H01

CMOS 64 bit PROM

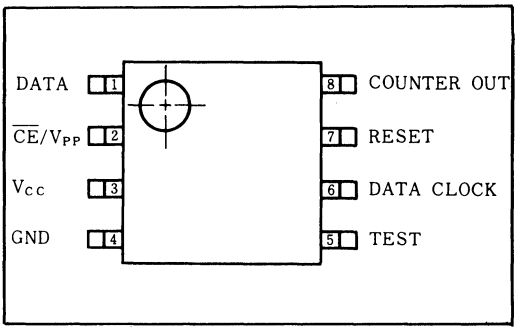
■ GENERAL DESCRIPTION

RF5H01/RP5H01 is a PROM with 64 × 1bit organization (+ dummy 8 bits), employing 2-layer silicon gate CMOS processing technology.

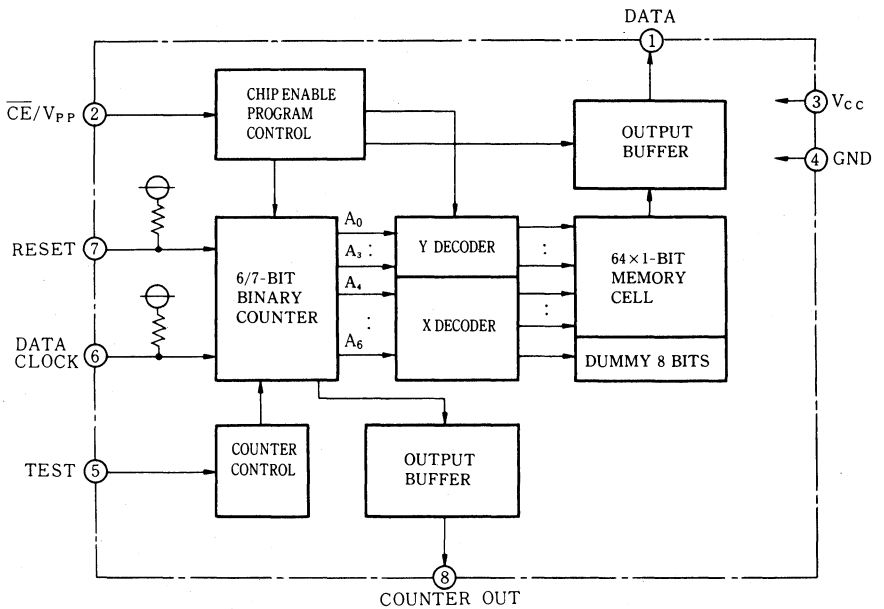
■ FEATURES

- 64× 1bit organization (+ dummy 8 bits)
- Low power dissipation
  - Active 55mW (max)
  - Standby 550μW (max)
- Access time 1μs (max)
- Single power supply 5V±10%
- Serial outputs
- Inputs and outputs TTL level
- 3-state (Tri-state) outputs

■ PIN CONFIGURATION (Top view)



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Conditions	Limits	Unit
V_{CC}	V_{CC} Supply Voltage	With respect to GND	−0.3~7	V
V_{PP}	V_{PP} Supply Voltage		−0.3~22	V
V_I	Input Voltage		−0.3~7	V
V_O	Output Voltage		−0.3~7	V
P_d	Maximum Power Dissipation	Ta=25℃	0.3	W
T_{opr}	Operating Temperature Range		−20~70	℃
T_{stg}	Storage Temperature		−40~125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=−20~70℃)

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	−0.1		0.8	V

■ ELECTRICAL CHARACTERISTICS

● READ OPERATION D.C. CHARACTERISTICS (Ta=−20~70℃, V_{CC}=5V±10%)

Symbol	Parameters		Test Conditions	Limits			Unit
				Min	Typ	Max	
I_{CC1}	Standby V_{CC} Supply Current		$\overline{CE}/V_{PP}=V_{CC}\pm0.3V$ DATA CLOCK,RESET=V_{CC} or Open TEST=GND or $V_{CC}\pm0.3V$			100	μA
I_{CC2}	Operating V_{CC} Supply Current		I_{OUT}=0mA			10	mA
V_{OH}	Output High Voltage		$I_{OH}=-400\mu A$	2.4			V
V_{OL}	Output Low Voltage		I_{OL}=2.1mA			0.45	V
V_{IH}	Input High Voltage	Except TEST		2.0		V_{CC}+0.3	V
		TEST		4.0		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	Except TEST		−0.1		0.8	V
		TEST		−0.1		1.0	V
I_{LI}	Input Leakage Current	RESET,DATA CLOCK	V_I=0V,V_{CC}=5.5V	−180		−20	μA
		TEST,$\overline{CE}/V_{PP}$	V_I=0V~V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current		V_O=0V~V_{CC}	−10		10	μA

● READ OPERATION, A.C. CHARACTERISTICS (Ta=−20~70℃, V_{CC}=5V±10%)

Symbol	Parameters	Test Conditions		Limits			Unit
				Min	Typ	Max	
t_{ACC}	Clock to Output Delay	$\overline{CE}/V_{PP}=V_{IL}$	Load= 1TTL+100pF			1	μs
t_{CE}	$\overline{CE}$ to Output Delay					1	μs
t_{DF}	$\overline{CE}$ High to Output Float			0		200	ns
t_{RW}	Reset pulse width			2			μs
t_{CW}	Clock pulse width			2			μs

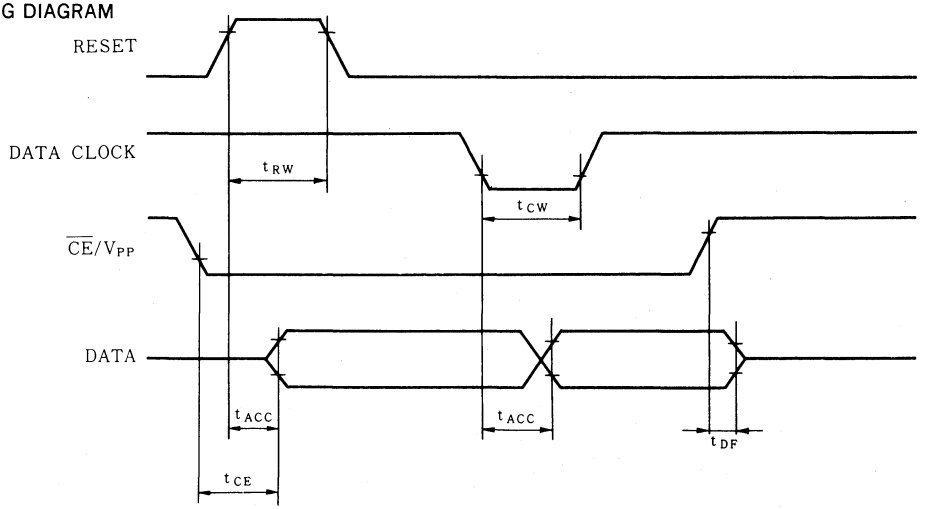
● D.C. PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%)

Symbol	Parameters		Test Conditions	Limits			Unit
				Min	Typ	Max	
I_{PP}	V_{PP} Supply Current		$\overline{CE}/V_{PP}=V_{IHP}$			5	mA
I_{CC}	V_{CC} Supply Current					0.5	mA
V_{IH}	Input High Voltage	Except TEST		2.0		V_{CC}+0.3	V
		TEST		4.0		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	Except TEST		−0.1		0.8	V
		TEST		−0.1		1.0	V
V_{IHP}	Program pulse Input High Voltage			20.5	21.0	21.5	V
V_{ILP}	Program pulse Input Low Voltage			2.0	V_{CC}	6.0	V
I_{LI}	Input leakage Current	RESET,DATA CLOCK	V_I=0V, V_{CC}=5.25V	−170		−20	μA
		TEST	V_I=0V~V_{CC}	−10		10	μA

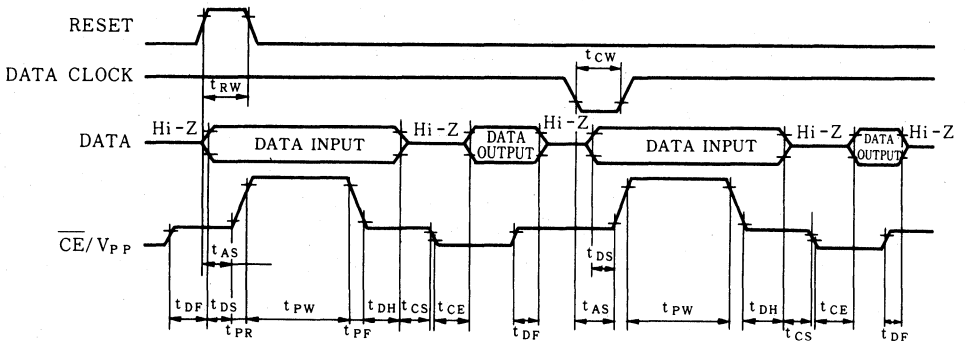
● PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%)

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
t_{AS}	Address Set-up Time	2			μs
t_{CS}	$\overline{CE}$ Set-up Time	2			μs
t_{DS}	Data Set-up Time	2			μs
t_{DH}	Data Hold Time	2			μs
t_{DF}	$\overline{CE}$ to Output Float	0		200	ns
t_{CE}	$\overline{CE}$ to Output Delay			1	μs
t_{PW}	Program pulse width	45	50	55	ms
t_{PR}	V_{PP} Pulse rise time	0.5		100	μs
t_{PF}	V_{PP} Pulse fall time	0.5		100	μs
t_{RW}	Reset pulse width	2			μs
t_{CW}	Clock pulse width	2			μs

■ TIMING DIAGRAM



● PROGRAM MODE



■ OPERATING MODES

Mode \ Pins	Data 1	Counter output 8	$\overline{CE}/V_{PP}$ 2	V_{CC} 3	GND 4
Read	Data Output	Clock (A5) Output	V_{IL}	V_{CC}	GND
Standby	High impedance	High impedance	V_{IH}	V_{CC}	GND
Program	Data Input	High impedance	V_{IHP}	V_{CC}	GND

	Counter operation mode
TEST (5) = GND	6 bits
TEST (5) = V_{CC}	7 bits

■ EXPLANATION ON OPERATION

● READ MODE

RF5H01/RP5H01 is a serial address type PROM with 6-bit/7-bit counter. The first bit can be read out by adding reset pulse after $\overline{CE}/V_{PP} = V_{IL}$. The 2nd bit~the 64th bit can be sequencially read out by adding data clock pulse. The output data is valid after a delay of t_{ACC} from reset rise up or data clock fall down, in the state of $\overline{CE}/V_{PP} = V_{IL}$.

In the state of TEST=GND, the counter operates as a 6-bit counter. It returns to the reset condition (address 000000), if it is added with 64-time data clock pulses after the reset pulse is applied.

The counter output pin is for operation test of the built-in counter. It puts out the highest output (A5) of the 6-bit counter.

● STANDBY MODE

RF5H01/RP5H01 is provided with power down function that is controlled by $\overline{CE}$ input. If TTL high level is given to the chip enable input ($\overline{CE}$), the device comes to be the Standby Mode, and the output is in the state of high impedance.

● PROGRAM MODE

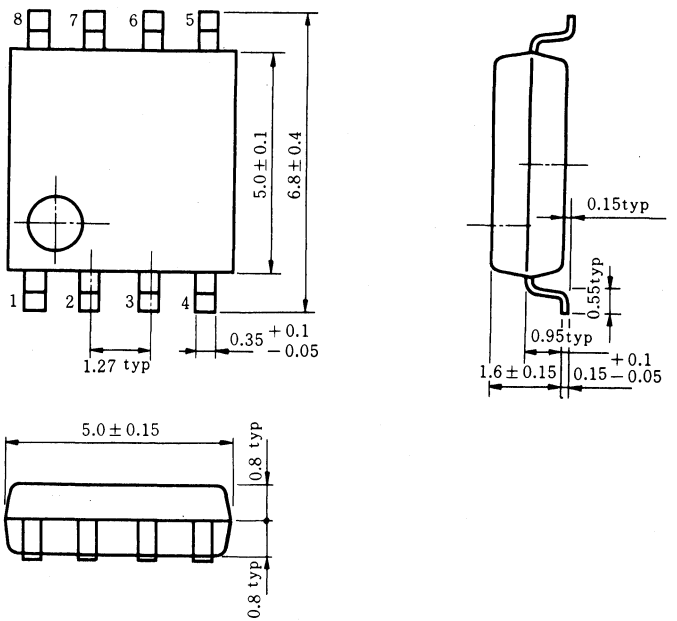
Initially, all bits of RF5H01/RP5H01 are in the "1" state. Data is introduced by selectively programming "0"into the desired bit locations.

The program is operated by setting up $\overline{CE}/V_{PP} = V_{IH}$, and adding the reset pulse, and then applying the 50mS 21V program pulse. The data are verified by making $\overline{CE}/V_{PP} = V_{IL}$. The 2nd bit~the 64th bit are programmed by progressing the addresses in sequence by means of adding the data clock pulse.

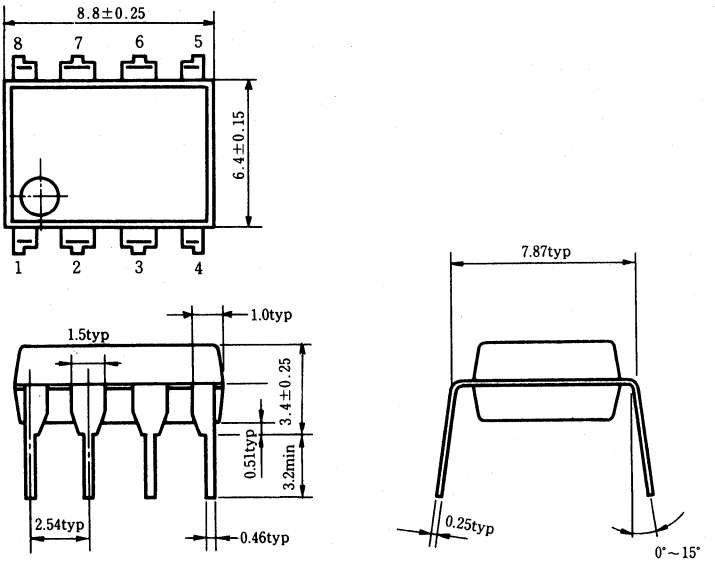
● DUMMY BITS

RF5H01/RP5H01 is a one-time PROM. For this reason, it is provided with a dummy bit of 8 bits for test programming. The dummy bit is located after the practical use 64th bit. The address is 8 bits of 1000000~1000111. The built-in counter operates as a 7-bit counter when "Test" (5 pins) is set at V_{CC} level, enabling to select the dummy bit. In the case of the "Test" being GND level, the counter operates as the 6-bit counter, being unable to select the dummy bit. In the 7-bit counter, when the clock pulse is added in sequence, the address progresses from 0000000 to 1111111, and then returns to 0000000.

■ 8-PIN PLASTIC FLAT PACKAGE (EXTERNAL VIEW) (UNIT : mm)



■ 8-PIN PLASTIC DIL PACKAGE (EXTERNAL VIEW) (UNIT : mm)



7. LINEAR IC

VOLTAGE DETECTORS
RX5VA Series

■ OUTLINE

RX5VA series, developed with C-MOS processing technology, are accurate, low-power-consumption voltage detectors. The detectors include comparators, output drivers and hysteresis circuit.
The value of detect voltage is set internally, and is accurately controlled by Laser Trimming.
There are three types of output : N-ch open-drain, P-ch open-drain, and C-MOS. There are two convenient packages : mini-power-mold and TO-92. The RX5VA series can be used as a reference voltage supply for ICs in many applications.

■ FEATURES

- Extremely low power consumption ..... TYP. 1.0μA (VDD = 3.0V)
- Wide voltage range ..... 1.5V to 10.0V
- Variety of detect voltage ..... 0.1V step
- High accuracy ..... ±2.5%
- Good temperature characteristic for detect voltage ..... TYP. ±100 PPM/°C
- Output Options ..... N-ch open drain,
  P-ch open drain,
  CMOS
- Compact Package ..... TO-92, min-power-mold

■ APPLICATIONS

- Resets circuit of P-ch, N-ch, and C-MOS microcomputers
- Battery checker
- Logic circuit reset
- Level discriminator
- Waveform shaping circuit
- Switching circuit for battery backup
- Power failure detector

Notice
The RX5VA Series will be discontinued, and therefore please order the RX5VL Series for the shipment after December 1992.

■ SELECTION GUIDE

You can define several options, including output driver type, package and packing method with the RX5VA series.

The devices are defined by the following characters.

R X 5 V A X X X X ← Type number

↑ ↑ ↑ ↑

a b c d

Character	Meaning
a	Defines the packaging type E : TO-92 H : Mini-power-mold
b	Defines the voltage value that is to be monitored (−VDET) The monitor range is 2.00V to 6.00V in 0.1V units, with an accuracy of ±2.5%.
c	Defines the output type A : N-ch open drain B : P-ch open drain C : C-MOS
d	Defines the packing method A-T1 : Taping-T1 type (See Fig. 1) A-T2 : Taping-T2 type (See Fig. 1) A-RF : Taping-RF type (See Fig. 1) A-RR : Taping-RR type (See Fig. 1) B : Gluing (Gluing is for mini power mold package as a sample) C : Electric conductive bagging (for TO-92)

Table 1

Example

Type number	Voltage Detect (−VDET)			Output Driver			Package	Packing method
	MIN.(V)	TYP.(V)	MAX.(V)	N-ch Open-Drain	P-ch Open-Drain	C-MOS		
RX5VA20AX	1.950	2.000	2.050	○			E:TO-92 H:Minipower mold (SOT-89)	A:Taping B:Gluing C:Electric Conductive bagging
RX5VA20BX					○			
RX5VA20CX						○		
RX5VA21AX	2.048	2.100	2.152	○				
RX5VA21BX					○			
RX5VA21CX						○		
RX5VA27AX	2.633	2.700	2.767	○				
RX5VA27BX					○			
RX5VA27CX						○		
RX5VA45AX	4.388	4.500	4.612	○				
RX5VA45BX					○			
RX5VA45CX						○		
RX5VA47AX	4.583	4.700	4.817	○				
RX5VA47BX					○			
RX5VA47CX						○		
RX5VA55AX	5.363	5.500	5.637	○				
RX5VA55BX					○			
RX5VA55CX						○		

Table 2

* Consult the guide to determine specifications other than those shown in Table 2. Use the type number.

■ TAPING METHODS

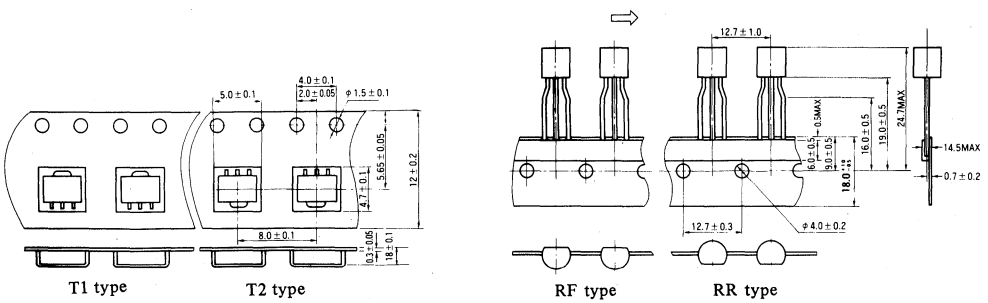


Figure 1

■ SYSTEM BLOCK DIAGRAMS

Figure 2 is block diagrams of RX5VA series and shows the system with three terminals. The system has three types of output drive : N-ch open-drain, P-ch open-drain, and C-MOS.

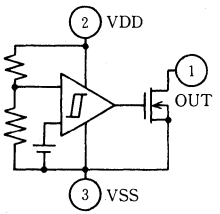
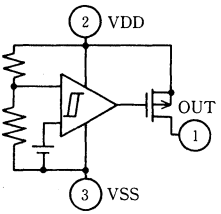
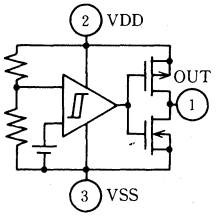
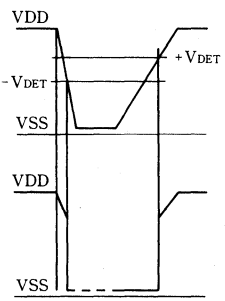
	N-ch open-drain (RX5VAXXAX)	P-ch open-drain (RX5VAXXBX)	C-MOS (RX5VAXXCX)
Block Diagrams			
Time Chart			
Package	3-terminals mini-power-mold TO-92		

Figure 2

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYNBOL	RATINGS	UNIT
Supply Voltage	VDD	12	V
Output Voltage	VOUT	VSS−0.3～VDD+0.3	
Output Current	IOUT	70	mA
Power Dissipation	Pd	300	mW
Operating Temperature Range	Topr	−30～+80	℃
Storage Temperature Range	Tstg	−40～+125	
Soldering Temperature	Tsolder	260℃ (10Sec)	

■ ELECTRICAL CHARACTERISTICS

Topr : 25℃

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Detect Voltage	−VDET		(−VDET) ×0.975		(−VDET) ×1.025	V
Hysteresis	VHYS			(−VDET) ×0.05		V
Supply Current	Iss	VDD= 2.0V		0.9	2.7	μA
		3.0V		1.0	3.0	
		4.5V		1.15	3.45	
		6.0V		1.3	3.9	
		10.0V		1.7	5.1	
Operating Voltage	VDD		1.5		10.0	V
Output Current	IOUT	Nch VDS=0.5V VDD:1.0V		0.5		mA
		2.4V		3.6		
		3.6V		6.5		
		4.6V		8.6		
		6.0V		11.6		
		10.0V		19.6		
		Pch VDS=2.1V VDD:4.5V	0.04			
Temperature Coefficient	△(−VDET) /△Ta	−30℃≦Ta≦80℃		±100		PPM/℃

■ PACKAGE INFORMATION

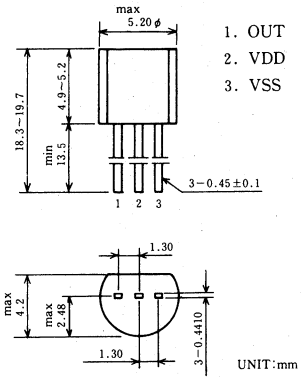


Figure 3. TO-9 (3-terminal)

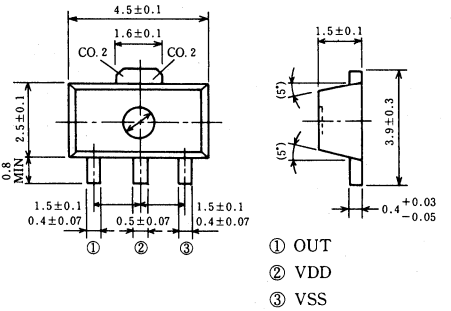


Figure 4. Mini-power-mold (3-terminal)

RICOH

Product News

PRELIMINARY

ES-113-9107

VOLTAGE DETECTOR RN5VL Series

RN5VL series, developed with CMOS process technology, are accurate, low-power-consumption, voltage detectors. The devices include reference voltage supply, comparators, resistor network, hysteresis circuit and output driver transistors. The detect voltage value is fixed internally.
There are 2 types of output(Nch open-drain, CMOS).
The very small package is available (SOT-23) and useful to be mounted in high density.

■ FEATURES

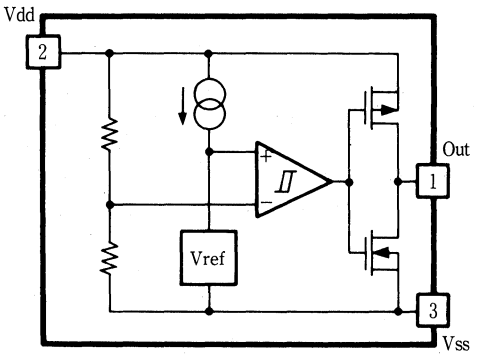
- Extremely low power consumption ..... TYP.1.0μA (Vdd = 3.0V)
- Wide operation voltage range ..... 1.5V ~ 10.0V
- Variety of detect voltage ..... 0.1V step
- High accuracy voltage detection ..... ±2.5%
- Small temperature coefficient of detect voltage ... TYP.±100PPM/°C
- Output options ..... Nch Open drain, CMOS
- Compact package ..... SOT-23-5 (mini mold 5 pin)

■ APPLICATIONS

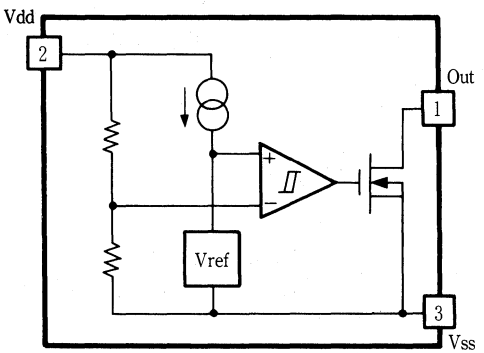
- Reset circuit of micro-computer and logic circuit
- Battery checker
- Level discriminator
- Waveform shaping circuit
- Switching circuit for battery back-up
- Power failure detector

■ BLOCK DIAGRAM

- CMOS type



- Nch Open-drain



■ SELECTION GUIDE

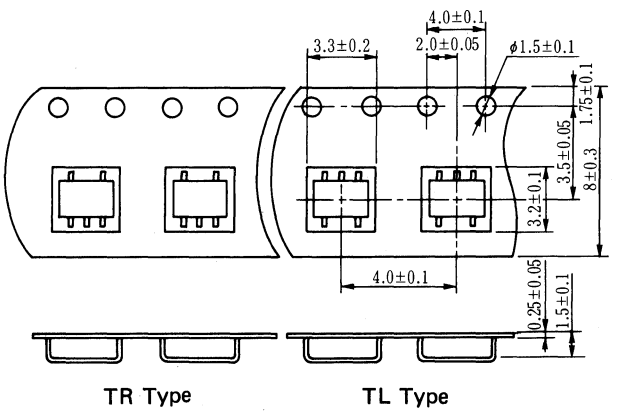
You can define the detect voltage, output driver, taping of the RN5VL series.
The devices are defined by the following characteristics.

R N 5 V L X X X X ←Type number

↑ ↑ ↑
a b c

No.	Meaning
a	Defines detect voltage value (-Vdet) The detect voltage is 2.0V to 6.0V in units of 0.1V with an accuracy of ±2.5%
b	Defines output type. A : Nch open-drain C : C-MOS
c	Defines taping type: (TR, TL) (See below)

Note) Taping (3000 pcs/one reel)



TR Type TL Type

■ ABSOLUTE MAXIMUM RATINGS

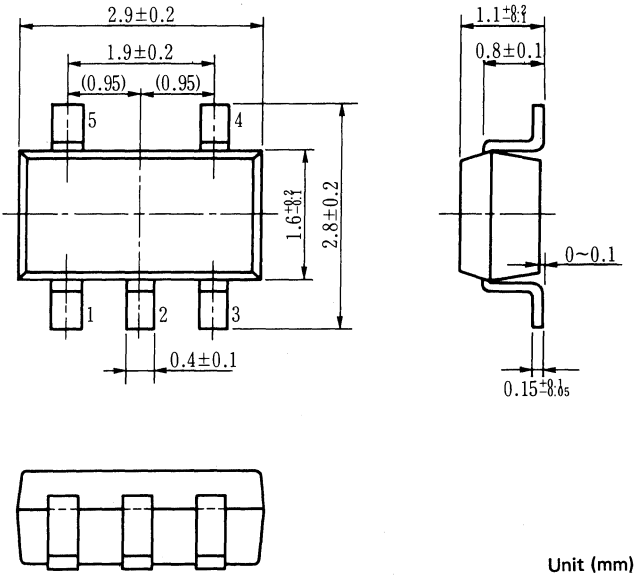
Parameter	Symbol	Rating	Unit
Supply Voltage	Vdd	12	V
Output Voltage (CMOS)	Vout	Vss-0.3 ~ Vdd+0.3	V
Output Voltage (Nch)		12	V
Output Current	Iout	70	mA
Power Dissipation	Pd	150	mW
Operating Temperature	Topr	-30 ~ +80	°C
Storage Temperature	Tstg	-40 ~ +125	°C
Soldering Temperature	Tsolder	260°C 10 sec.	

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect Voltage	-Vdet		(-Vdet) x 0.975		(-Vdet) x 1.025	V
Hysteresis	Vhys			(-Vdet) x 0.05		V
Consumption Current	Iss	Vdd=2.0V 3.0V 4.5V 6.0V 10V		0.9 1.0 1.15 1.3 1.7	2.7 3.0 3.45 3.9 5.1	μA
Operating Voltage	Vdd		1.5		10	V
Output Current (Driver Output)	Iout	Nch Vds=0.5V, Vdd=1.0V 2.4V 3.6V 4.6V 6.0V		0.5 3.6 6.5 8.6 11.6		mA
		Pch Vds=2.1V, Vdd=4.5V	0.04			
Temperature Coefficient	△(-Vdet) /△Ta	-30°C≦Ta≦80°C		±100		PPM /°C

■ PACKAGE DIMENSION (SOT23-5)



Unit (mm)

RICOH

PRELIMINARY

Product News

VOLTAGE DETECTOR
RN5VT Series(Low voltage)

The RN5VT Series ICs are high-precision voltage detectors, developed by CMOS process technology, featuring extremely low current consumption. The RN5VT Series ICs are used for system resetting. The internal circuit consists of a reference voltage source, comparator, voltage detection resistance network, hysteresis circuit, and output drive transistor. The detection voltage is fixed accurately inside the IC and requires no adjustment.

Two types of output are available: Nch open drain and CMOS.

For the electrical characteristics, the RN5VT achieved a lower operation voltage than the previous RH5VA Series. The RN5VT Series ICs operate with a single battery (minimum operating voltage is 0.7V).

Packaged in an ultra-compact 5-pin mini mold (SOT-23), the RN5VT Series ICs allow high-density mounting.

■ FEATURES

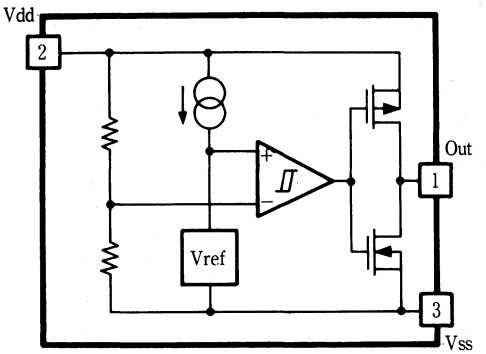
- Extremely low power consumption ..... TYP. 0.5 μA (Vdd = 1.5V)
- Wide operation voltage range ..... 0.7V ~ 10.0V
- Variety of detect voltage ..... 0.1V step from 0.9V to 3.0V
- High accuracy voltage detection ..... ±2.5%
- Small temperature coefficient of detect voltage .. TYP. ±100 PPM/°C
- Output option ..... Nch Open drain, CMOS
- Extremely compact package ..... SOT-23-5 (Mini mold 5 pin)

■ APPLICATIONS

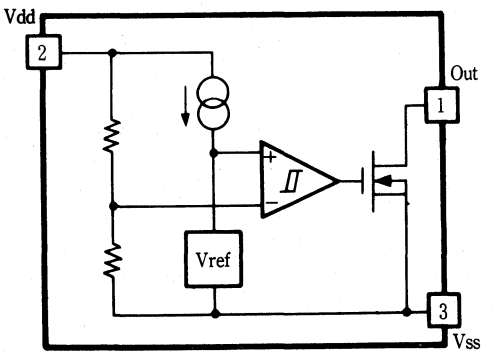
- Reset circuit of micro-computer and logic circuit
- Battery checker
- Level discriminator
- Waveform shaping circuit
- Switching circuit for battery back-up
- Power failure detector

■ BLOCK DIAGRAM

- **CMOS Output type**



- **Nch Open drain output type**



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	Vdd	12	V
Output Voltage (CMOS)	Vout	Vss−0.3 ~ Vdd+0.3	V
Output Voltage (Nch)	Vout	12	V
Output Current	Iout	70	mA
Power Dissipation	Pd	150	mW
Operating Temperature	Topr	−30 ~ +80	°C
Storage Temperature	Tstg	−40 ~ +125	°C
Soldering Temperature	Tsolder	260°C, 10 sec.	

■ ELECTRICAL CHARACTERISTICS

(Ta = 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Detect Voltage	−Vdet		(−Vdet) x 0.975		(−Vdet) x 1.025	V
Hysteresis	Vhys			(−Vdet) x 0.025		V
Consumption Current	Iss	Vdd = 2.0V 3.0V 4.5V 6.0V		0.3 0.5 1.0 1.5	1.0 1.5 3.0 5.0	μA
Operating Voltage	Vdd		0.7		10	V
Output Current (Driver Output)	Iout	Nch Vds = 0.5V, Vdd = 0.8V 1.5V		0.1 0.5		mA
		Pch Vds = 2.1V, Vdd = 4.5V	0.04			
Temperature Coefficient	Δ(−Vdet) /ΔTa	−30°C ≦ Ta ≦ 80°C		±100		PPM/°C

■ SELECTION GUIDE

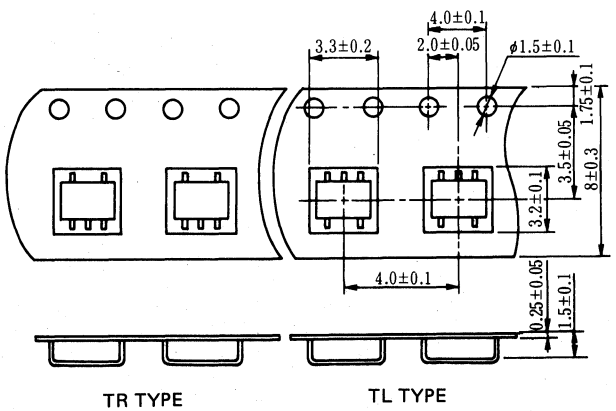
You can define the output voltage and package of the RN5VT Series. The devices are defined by the following characters.

RN5VTXXXX ← Type number

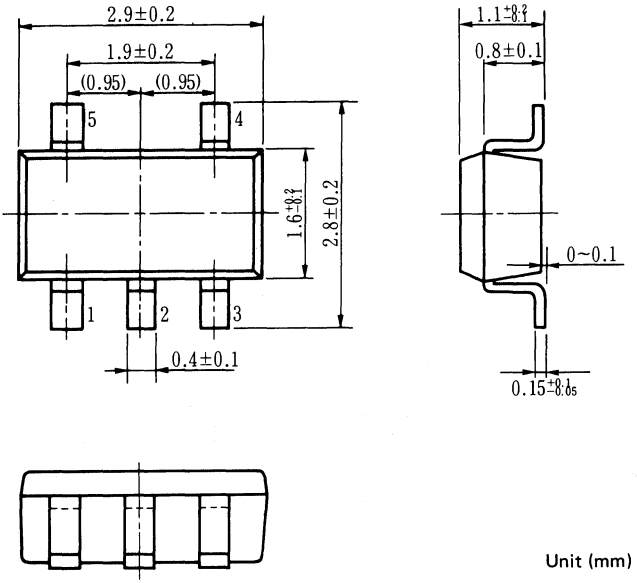
↑ ↑↑
a b c

No.	Meaning
a	Defines detect voltage value (−Vdet) The detect voltage range is from 0.9V to 3.0V in unit of 0.1V with an accuracy of ±2.5%.
b	Defines output type A: Nch open drain C: C-MOS
c	Defines taping type (TR, TL) (See below)

Note) Taping (3,000 pcs/one reel)



■ PACKAGE DIMENSION (SOT23-5)



Unit (mm)

VOLTAGE REGULATORS
RX5RA Series

■ OUTLINE

The RX5RA series, developed with C-MOS processing technology, are highly accurate, low-power-consumption, fixed three terminal voltage regulators. They include reference voltage supply, error amplifier, control transistor, and resistor network to control the output voltage. The output voltage is fixed in the IC.

The RX5RA series are both available in two different types of package : mini-power-mold and TO-92.

■ FEATURES

- Extremely low power consumption ..... TYP. 1.0μA Vout = 3.0V
- Small input-output voltage difference ..... TYP. 60mV Iout = 1.0mA
- Low temperature coefficient for output voltage ..... TYP. ±100PPM/°C
- Stable input rate ..... TYP. 0.1%/V
- Accurate output voltage ..... ±2.5%
- Variety of output voltage levels ..... 0.1V step
- Compact package ..... TO-92, mini power mold

■ APPLICATIONS

- Constant-voltage power supply for battery-powered devices
- Constant-voltage power supply for camera, communication, and video equipment
- Stable standard voltage supply

■ BLOCK DIAGRAMS

Type RX5RAXXXX
(positive-voltage regulator)

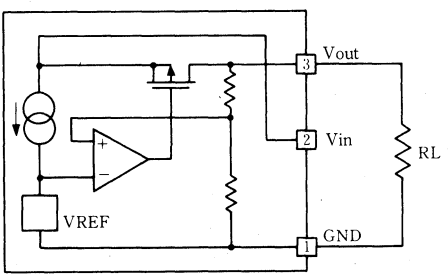


Figure 1

Notice
The RX5RA Series will be discontinued, and therefore please order the RX5RL Series for the shipment after December 1992.

■ SELECTION GUIDE

You can define the output voltage and package of the RX5RA series.
The devices are defined by the following characters.

RX5RAXXXX ← Type number

↑ ↑ ↑↑

a b c d

No.	Meaning
a	Defines the packaging type E : TO-92 H : Mini power mold (SOT-89)
b	Defines output voltage (Vout) The range for Vout is 2.0V to 6.0V in units of 0.1V, with an accuracy of ±2.5%.
c	Defines the output current type A : Standard type
d	Defines the packaging method for shipment A-T1 : Taping-T1 type (See Fig. 2) A-T2 : Taping-T2 type (See Fig. 2) A-RF : Taping-RF type (See Fig. 2) A-RR : Taping-RR type (See Fig. 2) B : Gluing (Gluing is for mini power mold package as a sample) C : Electric conductive bagging (for TO-92)

Table 1

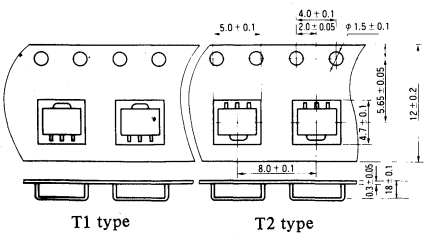
Example : positive-voltage regulator

Type numbers	output voltage(Vout)			Package	Packing method
	MIN.(V)	TYP.(V)	MAX.(V)		
RX5RA21AX	2.048	2.100	2.152	E:TO-92 H:Mini power mold	A:Taping B:Gluing C:Electric conductive bagging
RX5RA30AX	2.925	3.000	3.075		
RX5RA33AX	3.218	3.300	3.382		
RX5RA37AX	3.608	3.700	3.792		
RX5RA40AX	3.900	4.000	4.100		
RX5RA50AX	4.875	5.000	5.125		
RX5RA60AX	5.850	6.000	6.150		

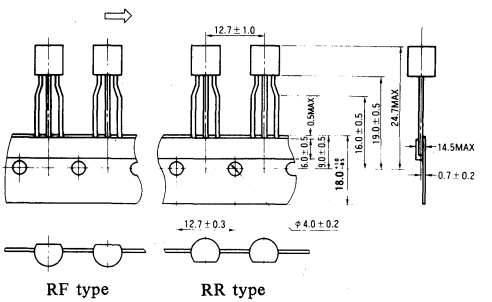
Table 2

* Following the selection guide, determine specification other than those shown in Table 2. Use the type number.

■ TAPING METHODS



mini-power-mold



TO-92

Figure 2

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage	Vin	+12	V
Output Current	Iout	150	mA
Output Voltage	Vout	Vin+0.3～−0.3	V
Power Dissipation	Pd	300	mW
Operating Temperature Range	Topr	−30～+80	℃
Storage Temperature Range	Tstg	−40～+125	
Soldering Temperature	Tsolder	260℃ 10Sec	

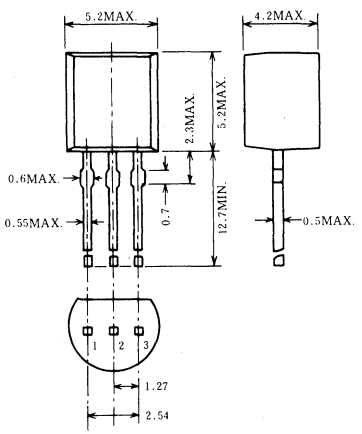
■ ELECTRICAL CHARACTERISTICS

Topr : 25℃

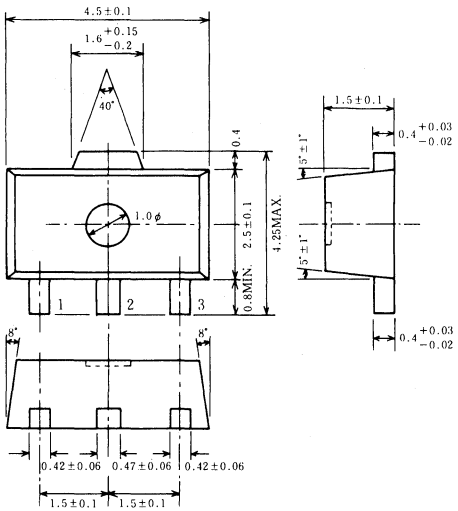
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vout	Iout=10mA	(Vout) ×0.975		(Vout) ×1.025	V
Output Current	Iout	Vin−Vout =2.0V Vout =3.0V Vout =5.0V		40 60		mA
Load Regulation	△Vout	Vin−Vout =2.0V Vout =3.0V 1mA≦Iout≦20mA Vout =5.0V 1mA≦Iout≦40mA		60 40		mV
Input-Output Voltage Difference	Vdif	Iout=1mA Vout =3.0V =5.0V		60 30		mV

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	Iss	Vin−Vout =2.0V Vout =3.0V =5.0V		1.1 1.3	3.3 3.9	μA
Line Regulation	$\frac{\triangle Vout}{Vout \cdot \triangle Vin}$	Iout=1mA Vout +0.5V≦ Vin ≦10V		0.1		%/V
Input Voltage	Vin				10	V
Temperature Coefficient	△Vout/△Topr	Iout=10mA −30℃ ≦Topr≦80℃		±100		PPM/℃

■ PACKAGE INFORMATION



TO-92



mini-power-mold

1	GND
2	Vin
3	Vout

RICOH

Product News

PRELIMINARY

ES-114-9107

VOLTAGE REGULATOR RN5RL Series

The RN5RL series, developed with CMOS process technology, are highly accurate, low-power-consumption, voltage regulators which include reference voltage supply, error amplifier, control transistor, and resistor network to control the output voltage. The output voltage is fixed in the RN5RL device.
The very small package is available (SOT-23) and useful to be mounted in high density.

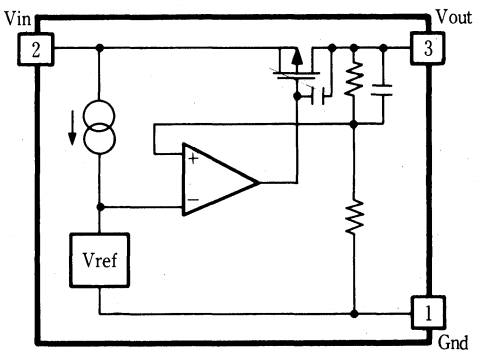
■ FEATURES

- Extremely low power consumption TYP.1.1μA (RN5RL30AX)
- Small input/output voltage difference ..... TYP.30mV Iout = 1mA (RN5RL50AX)
- Variety of output voltage levels ..... 0.1V step
- Stable input rate TYP.0.1%/V
- Small temperature coefficient for output voltage .. TYP.±100PPM/°C
- Accurate output voltage ..... ±2.5%
- Compact package ..... SOT-23-5 (mini mold 5 pin)

■ APPLICATIONS

- Constant-Voltage power supply for battery-powered devices
- Constant-voltage power supply for camera, communication, and video equipment.
- Stable standard voltage supply.

■ BLOCK DIAGRAM



■ SELECTION GUIDE

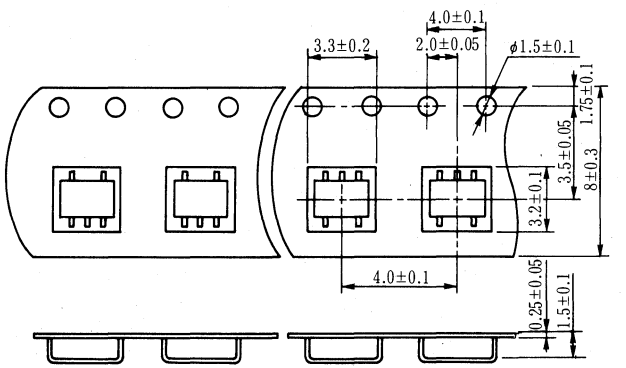
You can define the output voltage, version and taping of the RN5RL series.
The devices are defined by the following characters.

R N 5 R L X X X X ←Type number

↑ ↑ ↑
a b c

No.	Meaning
a	Defines output voltage (Vout) The range for the Vout is 2.0V to 6.0V in units of 0.1V, with an accuracy of ±2.5%.
b	Defines version beginning with A.
c	Defines taping type: (TR, TL) (See below)

Note) Taping (3000 pcs/one reel)



TR type TL type

■ ABSOLUTE MAXIMUM RATINGS

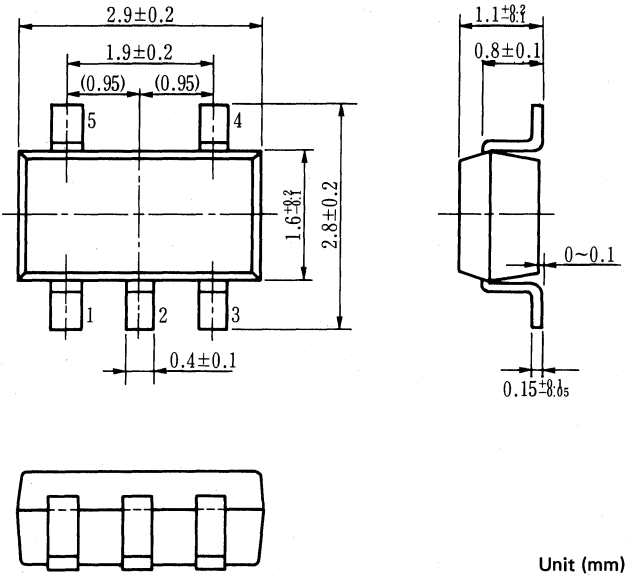
Parameter	Symbol	Rating	Unit
Input Voltage	Vin	12	V
Output Voltage	Vout	-0.3 ~ Vin+0.3	V
Output Current	Iont	150	mA
Power Dissipation	Pd	150	mW
Operating Temperature	Topr	-30 ~ +80	°C
Storage Temperature	Tstg	-40 ~ +125	°C
Soldering Temperature	Tsolder	260°C 10 sec.	

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Iout=10mA	Vout x0.975		Vout x1.025	V
Output Current	Iout	(Vin-Vout)=2.0V (Vout)=3.0V (Vout)=5.0V		40 60		mA
Load Regulation	△Vout	(Vin-Vout)=2.0V (Vout)=3.0V 1mA≦Iout≦20mA (Vout)=5.0V 1mA≦Iout≦40mA		60 40		mV
Input Output Voltage Difference	Vdif	Iout=1mA (Vout)=3.0V =5.0V		60 30		mV
Consumption Current	Iss	(Vin-Vout)=2.0V (Vout)=3.0V =5.0V		1.1 1.3	3.3 3.9	μA
Line Regulation	△Vout/△Vin x Vout	Iout=1mA (Vout)+0.5V≦(Vin)≦10V		0.1		%/V
Input Voltage	Vin				10	V
Temperature Coefficient	△Vout/△Topr	Iout=10mA -30°C≦Topr≦80°C		±100		PPM/°C

■ PACKAGE DIMENSION (SOT23-5)



Unit (mm)

VOLTAGE REGULATORS
RX5RE Series

The RX5RE series, developed with CMOS processing technology, are highly accurate, low power consumption, large output current 3-terminal voltage Regulators. They include reference voltage supply, error amplifier, control transistor, and resistor network to control the output voltage. Because of small input-output voltage difference, effective constant-voltage power supply can be designed. The RX5RE series have a current control circuit to protect themself from the destruction due to over current. The output voltage is fixed in the device. The RX5RE series are both available in two different types of package: mini-power-mold and TO-92.

■ FEATURES

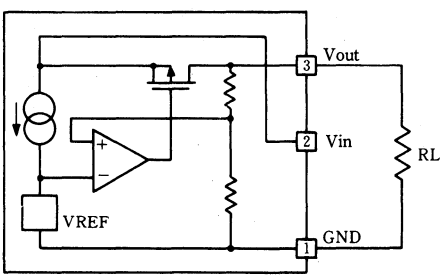
- Extremely low power consumption ..... TYP. 1.1μA (RX5RE30X, Vin = 5.0V)
- Small input-output voltage difference ..... TYP. 0.5V Iout = 60mA (RX5RE50X)
- Large output current ..... TYP. 120mA (RX5RE50X)
- Low temperature coefficient for output voltage ... TYP. ±100PPM/°C
- Wide operating voltage range ..... MAX. 10.0V
- Stable input rate ..... TYP. 0.1%/V
- Accurate output voltage ..... ±2.5%
- Variety of output voltage levels ..... 0.1V step (Note)
- Compact package ..... TO-92, mini power mold

(Note: RX5RE30X and RX5RE50X are standard. Custom type is also available.)

■ APPLICATIONS

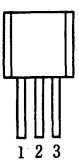
- Constant-voltage power supply for battery-powered devices
- Constant-voltage power supply for camera, communication, and video equipment
- Stable standard voltage supply

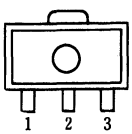
■ BLOCK DIAGRAM



■ PIN CONFIGURATION

TO-92





1 GND
2 Vin
3 Vout

■ SELECTION GUIDE

You can define the output voltage and package of the RX5RA series.
The devices are defined by the following characters.

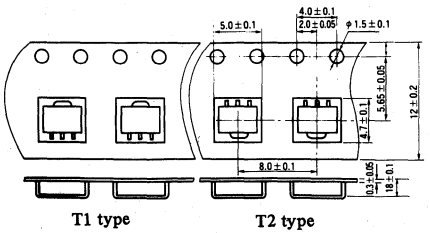
R X 5 R E X X X ← Type number

↑ ↑ ↑

a b c

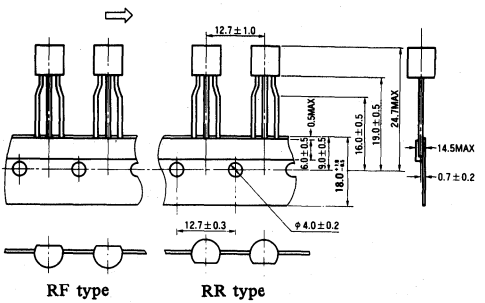
No.	Meaning
a	Defines the packaging type E : TO-92 H : Mini power mold (SOT-89)
b	Defines output voltage (Vout) The range for Vout is 2.0V to 6.0V in units of 0.1V, with an accuracy of ±2.5%.
c	Defines the packaging method for shipment A-T1 : Taping-T1 type A-T2 : Taping-T2 type A-RF : Taping-RF type A-RR : Taping-RR type B : Gluing (Gluing is for mini power mold package as a sample) C : Electric conductive bagging (for TO-92)

■ TAPING METHODS



T1 type T2 type

mini-power-mold



RF type RR type

TO-92

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage	Vin	+12	V
Output Current	Iout	150	mA
Output Voltage	Vout	Vin+0.3～−0.3	V
Power Dissipation	Pd	300	mW
Operating Temperature Range	Topr	−30～+80	℃
Storage Temperature Range	Tstg	−40～+125	
Soldering Temperature	Tsolder	260℃ 10Sec	

■ RX5RE50X (Vout = 5.0V)

Topr : 25°C

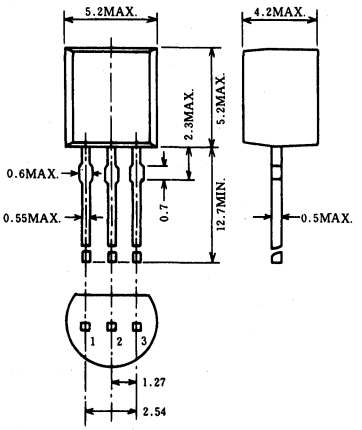
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vout	Iout = 10mA	4.875	5.000	5.125	V
Output Current	Iout	Vin = 7.0V	80	120		mA
Load Regulation	ΔVout	Vin = 7.0V, 1mA ≦ Iout ≦ 80mA		40	80	mV
Input-Output Voltage Difference	Vdif	Iout = 60mA		0.5	0.7	V
Consumption Current	Iss	Vin = 7.0V		1.3	3.9	μA
Line Regulation	$\frac{\Delta Vout}{\Delta Vin \cdot Vout}$	Iout = 10mA | Vout | + 1.0V ≦ | Vin | ≦ 10V		0.1		%/V
Input Voltage	Vin				10	V
Limit Current	Ilim			240		mA
Temperature Coefficient	$\frac{\Delta Vout}{\Delta Topr}$	Iout = 10mA −30°C ≦ Topr ≦ 80°C		±100		$\frac{PPM}{°C}$

■ RX5RE30X (Vout = 3.0V)

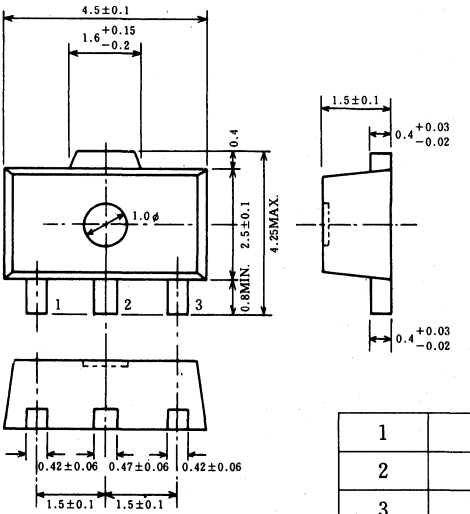
Topr : 25°C

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vout	Iout = 10mA	2.925	3.000	3.075	V
Output Current	Iout	Vin = 5.0V	50	80		mA
Load Regulation	ΔVout	Vin = 5.0V, 1mA ≦ Iout ≦ 60mA		40	80	mV
Input-Output Voltage Difference	Vdif	Iout = 40mA		0.5	0.7	V
Consumption Current	Iss	Vin = 5.0V		1.1	3.3	μA
Line Regulation	$\frac{\Delta Vout}{\Delta Vin \cdot Vout}$	Iout = 10mA | Vout | + 1.0V ≦ | Vin | ≦ 10V		0.1		%/V
Input Voltage	Vin				10	V
Limit Current	Ilim			240		mA
Temperature Coefficient	$\frac{\Delta Vout}{\Delta Topr}$	Iout = 10mA −30°C ≦ Topr ≦ 80°C		±100		$\frac{PPM}{°C}$

■ PACKAGE INFORMATION



TO-92



mini-power-mold

1	GND
2	Vin
3	Vout

RH5RC301/302/501/502

STEP-UP DC/DC CONVERTER

RH5RC301/302/501/502 are compact step-up DC/DC converter ICs, developed with the CMOS process technology. They consist of reference voltage source, error amplifier, control transistor, oscillation circuit, and output voltage setting resistor. As external parts, a coil, a diode, and a capacitor are available for obtaining a constant output voltage (3V, 5V) higher than the input voltage.

The package is a compact three-terminal mini power mold type.

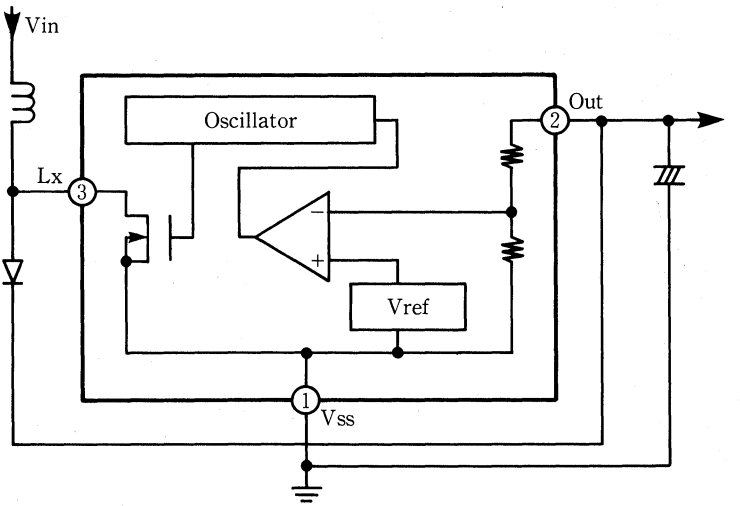
■ Features

- RH5RC301 ..... 3V output, normal type
  RH5RC302 ..... 3V output, low input voltage type
  RH5RC501 ..... 5V output, normal type
  RH5RC502 ..... 5V output, low input voltage type
- Small invalid current ..... 2.5μA (Typ., no step-up, RH5RC301/302)
- Low voltage operation ..... Input voltage Vin ≧ 0.9V (RH5RC302/502)
- High efficiency ..... 80% (Typ.)
- High output voltage accuracy ..... ±5%
- Small temperature drift of output voltage ..... ±50ppm (Typ.)
- Compact package ..... Mini power mold (SOT-89)

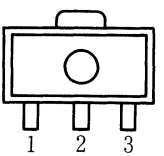
■ Application

Constant voltage source for battery-operated devices.
Constant voltage source for cameras, communications equipment, and videos.
Local regulator for different operating voltages.

■ Block Diagram



■ Pin Configuration



■ Pin Description

Pin No.	Name	Function
1	Vss	Ground
2	Out	Voltage Output
3	Lx	Switching pin

■ Absolute Maximum Ratings

(Vss=0V)

Parameter	Symbol	Limit	Unit
Input Voltage	Vin	7	V
Output Voltage	Vout	7	V
Output Current of Lx pin	ILx	120	mA
Power Dissipation	Pd	300	mW
Operating Temperature	Topr	-20 ~ +70	°C
Storage Temperature	Tstg	-40 ~ +125	°C

■ Electrical Characteristics

1. RH5RC301

(Ta = 25°C, Vss = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				6	V	
Starting Voltage	Vst	No Load			1.0	V	1
Holding Voltage	Vhld	No Load			0.6	V	1
Current Consumption	Iin	Vin = 5V		2.5	6	μA	
		Vin = 1.5V		7.5	20	μA	1
Output Voltage	Vout		2.85		3.15	V	1
Output Current of Lx pin	ILx	VOL = 0.4V	40			mA	
Leakage Current of Lx pin	ILxL				2	μA	
Oscillating Frequency	fosc		60		90	KHz	
Duty Ratio of Oscillation	Df			50		%	

2. RH5RC302

(Ta = 25°C, Vss = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				2	V	
Starting Voltage	Vst	No Load			0.9	V	1
Holding Voltage	Vhld	No Load			0.5	V	1
Current Consumption	Iin	Vin = 5V		2.5	6	μA	
		Vin = 1.5V		7.5	20	μA	1
Output Voltage	Vout		2.85		3.15	V	1
Output Current of Lx pin	ILx	VOL = 0.4V	40			mA	
Leakage Current of Lx pin	ILxL				2	μA	
Oscillating Frequency	fosc		60		100	KHz	
Duty Ratio of Oscillation	Df			25		%	2

3. RH5RC501

(Ta=25°C, Vss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				6	V	
Starting Voltage	Vst	No Load			1.0	V	1
Holding Voltage	Vhld	No Load			0.6	V	1
Current Consumption	Iin	Vin = 7V		3.5	9	μA	
		Vin = 2.4V		12	32	μA	1
Output Voltage	Vout		4.75		5.25	V	1
Output Current of Lx pin	ILx	VOL = 0.4V	60			mA	
Leakage Current of Lx pin	ILxL				9	μA	
Oscillating Frequency	fosc		100		140	KHz	
Duty Ratio of Oscillation	Df			50		%	

4. RH5RC502

(Ta=25°C, Vss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				2	V	
Starting Voltage	Vst	No Load			0.9	V	1
Holding Voltage	Vhld	No Load			0.5	V	1
Current Consumption	Iin	Vin = 7V		3.5	9	μA	
		Vin = 2.4V		12	32	μA	1
Output Voltage	Vout		4.75		5.25	V	1
Output Current of Lx pin	ILx	VOL = 0.4V	60			mA	
Leakage Current of Lx pin	ILxL				2	μA	
Oscillating Frequency	fosc		110		150	KHz	
Duty Ratio of Oscillation	Df			25		%	2

Note: 1. The above table assumes that L=270μH (Sumida Denki CM-5), D=MA721 (Matsushita Electronics), and C=33μF (Tantaru), or equivalent products are used for external parts.

2. Duty Ratio of oscillation Df is expressed as follows: :

$$Df = \frac{t_H}{t_H + t_L} \times 100(\%)$$

■ Design of DC/DC Converter

To design a DC/DC converter using this IC, the step-up capability varies with the external attachments (such as coils) and input voltage. The output voltage Iout is expressed as follows:

$$Iout = K \frac{Vin^2}{8 \cdot L \cdot fosc \cdot (Vout - Vin)} \qquad (RH5RC301/501)$$

$$Iout = K \frac{9 \cdot Vin^2}{32 \cdot L \cdot fosc \cdot (Vout - Vin)} \qquad (RH5RC302/502)$$

(for K = 0.5 to 0.8)

The following external attachments are recommended for optimum performance:

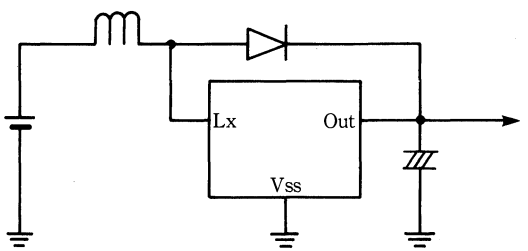
(1) Coil
- CMD-6L (Sumida Electric Company Ltd.) or equivalent product
- CM-5 (Sumida Electric Company Ltd.) or equivalent product

(2) Diode
- Schottoky type Diode

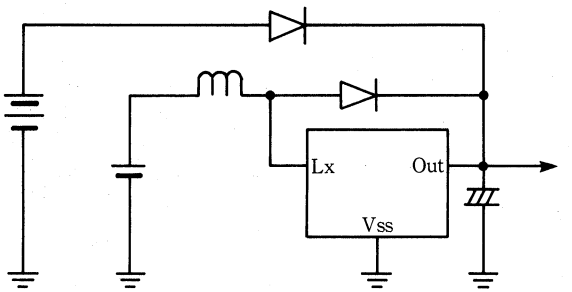
(3) Capacitor
- 22 to 47μ

■ Application Circuit

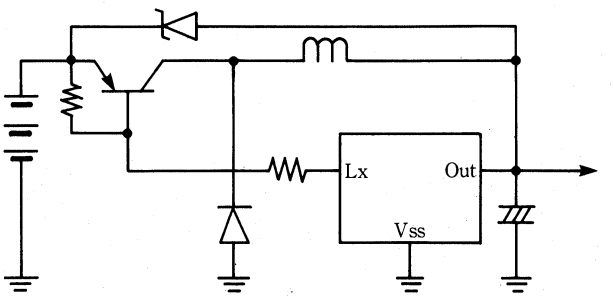
1. Step-up DC/DC Converter



2. Power Supply Switching Circuit



3. Step-down DC/DC Converter



■ Packaging Information

1. There are two packaging methods: taping and conductive bag.

   The packaging method is specified with the device model number as follows:

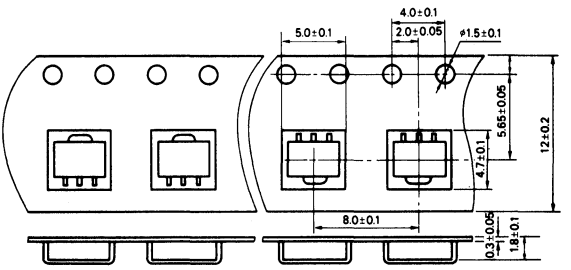
   RH5RC301A-T1: Taping

   RH5RC301A-T2: Taping

   RH5RC301C ___: Conductive bag (for sample only)

   Indication of the packaging method

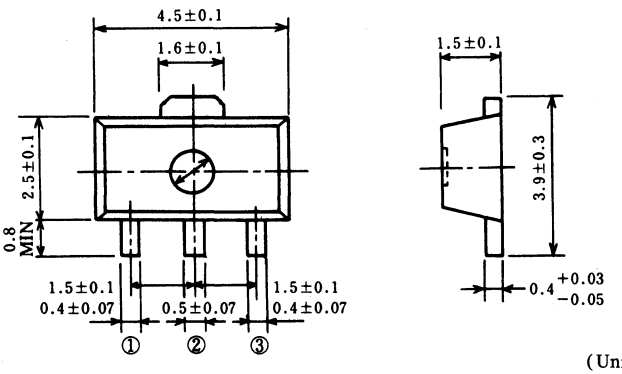
2. Taping method



T1 type T2 type

(Unit: mm)

■ Package Dimension



(Unit: mm)

RICOH

PRELIMINARY

EK-032-8906

RF5RD301/501

STEP-UP/STEP-DOWN DC/DC CONVERTER

RF5RD301/501 are compact DC/DC converter ICs developed with the CMOS process technology. When the input voltage is sufficiently high, they work as series regulators. When the input voltage falls down, they work as step-up switching regulators.

They consist of a step-up switching regulator circuit and series regulator circuit. The switching regulator circuit consists of the reference voltage source, error amplifier, control transistor, oscillation circuit, and output voltage setting resistor. The series regulator circuit consists of the reference voltage source (shared with the switching regulator circuit), error amplifier, output transistor, and output voltage setting resistor.

As external parts, a coil, a diode, and a capacitor are available for making the output voltage constant even when the input voltage changes across the output voltage.

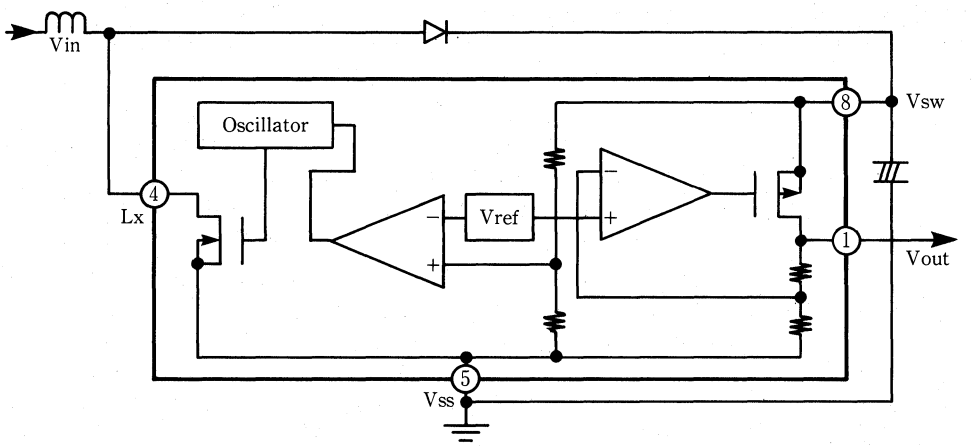
■ Features

- RF5RD301 ..... Output voltage 3V (Typ.)
  RF5RD501 ..... Output voltage 5V (Typ.)
- Low invalid current ..... 4.0μA (Typ., no step up, RF5RD301)
- Small invalid current ..... Input voltage Vin ≧ 1.2V (no load)
- High efficiency ..... 70% (Typ., step up)
- High output voltage accuracy ..... ±5%
- Small temperature drift of output voltage ..... ±100ppm (Typ.)
- Small package ..... 8-pin SOP

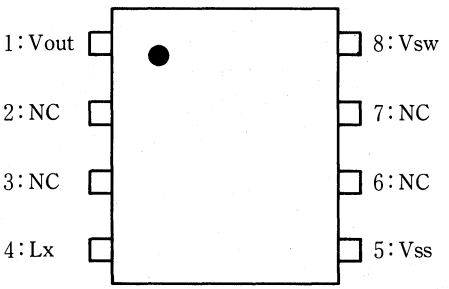
■ Application

- Constant voltage source for battery-operated devices.
- Constant voltage source for cameras, communication equipment, and videos.
- Local regulator for different operating voltages.

■ Block Diagram



■ Pin Configuration



■ Pin Description

Pin No.	Name	Function
1	Vout	Output Voltage
2, 3	NC	No Connection
4	Lx	Switching pin
5	Vss	Ground
6, 7	NC	No Connection
8	Vsw	Step-up Output

■ Absolute Maximum Ratings

(Vss=0V)

Parameter	Symbol	Limit	Unit
Input Voltage	Vin	12	V
Output Voltage	Vout	12	V
Output Current of Lx pin	ILx	100	mA
Power Dissipation	Pd	300	mW
Operating Temperature	Topr	-20 ~ +70	°C
Storage Temperature	Tstg	-40 ~ +125	°C

■Electrical Characteristics

● RF5RD301 (3V Output)

(Ta = 25°C Vss = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage	Vin				8	V
Starting Voltage	Vst	No Load	1.2			V
Holding Voltage	Vhld	No Load	0.8			V
Current Consumption	Iin	No Load, Vin = 5V		4	9	μA
		No Load, Vin = 2.4V		7	20	μA
Output Voltage	Vout		2.85		3.15	V
Output Current	Iout	Vin = 5V		40		mA
		Vin = 2.4V		15		mA
Output Current of Lx pin	ILx	Vol = 0.4V	40			mA
Leakage Current of Lx pin	ILXL				1	μA
Oscillating Frequency	fosc		60		90	KHz

● RF5RD501 (5V Output)

(Ta = 25°C Vss = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage	Vin				8	V
Starting Voltage	Vst	No Load	1.2			V
Holding Voltage	Vhld	No Load	0.8			V
Current Consumption	Iin	No Load, Vin = 7V		6	11	μA
		No Load, Vin = 3.6V		15	40	μA
Output Voltage	Vout		4.75		5.25	V
Output Current	Iout	Vin = 7V		40		mA
		Vin = 3.6V		20		mA
Output Current of Lx pin	ILx	Vol = 0.4V	60			mA
Leakage Current of Lx pin	ILxl				1	μA
Oscillating Frequency	fosc		100		140	KHz

Note: The above table assumes that L = 120μH (CMD6L), MA721 diode or equivalent, and C = 22μF are used for external parts.

■ Design of DC/DC Converter

To design a DC/DC converter using this IC, the output voltage Iout depends on the output current capability of the series regulator when stepping down, and on the step-up capability of the switching regulator when stepping up. Therefore, Iout is expressed as follows:

(Step-down)

$$Iout = Kp\,(Vin - Vf - Vout)$$

(Vf = forward direction voltage of diode, Kp = conductance coefficient of transistor)

(Step-up)

$$Iout = KL \frac{Vin}{8 \cdot L \cdot fosc \cdot (Vout - Vin)}$$

(for, KL = 0.5 to 0.8)

The following external attachments are recommended for optimum performance:

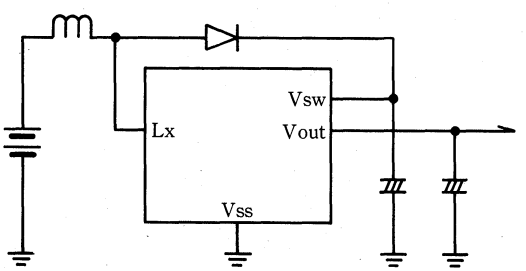
(1) Coil
- CMD-6L (Sumida Electric Company Ltd.) or equivalent
- CM-5 (Sumida Electric Company Ltd.) or equivalent

(2) Diode
- Shottkey diode

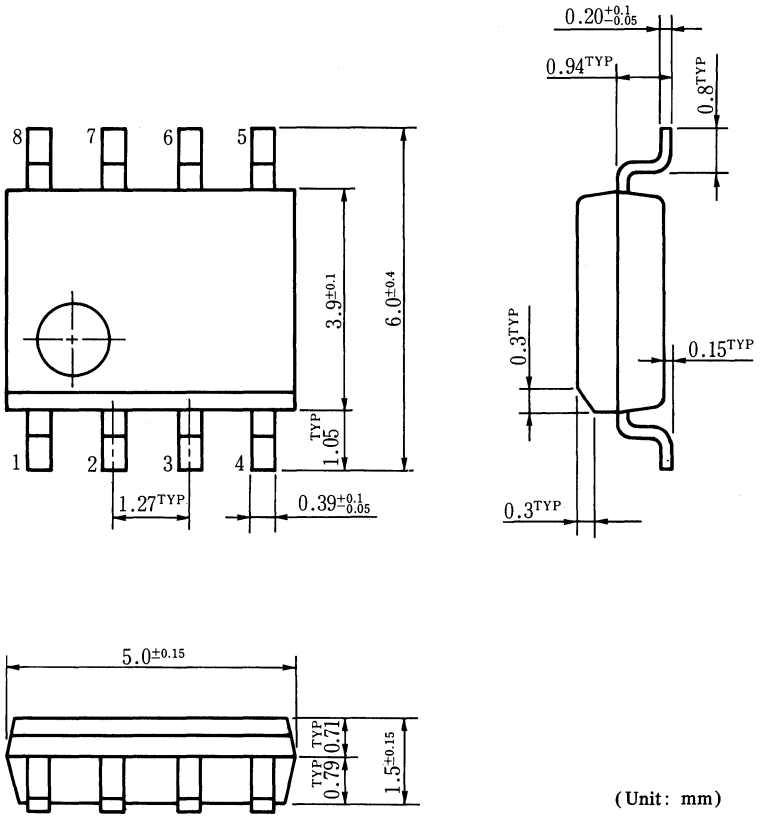
(3) Capacitor
- 22 to 47μF or more

■ Application Circuit

Step-up/Step-down DC/DC Converter



■ Package Dimension



(Unit: mm)

RICOH

Product News

PRELIMINARY

ES-116-9202

STEP-UP/STEP-DOWN PWM DC/DC CONVERTER with VOLTAGE DETECTOR RS5RM Series

■ OUTLINE

RS5R Series are compact DC/DC converter ICs with a voltage detector and are developed with CMOS process technology. The devices consist of a PWM type DC/DC converter, a series regulator and a voltage detector. As external components, a coil, a diode, and a capacitor are available for making the output constant. When the input voltage is sufficiently high, they work as series regulators. When the input voltage falls down, they work as step-up DC/DC converters. The RS5RM series include a voltage detector and the output voltage can be detected. The chip enable can switch off the DC/DC converter and the voltage detector, and can save consumption current at standby state. The RS5R is fit for battery-operated equipment.

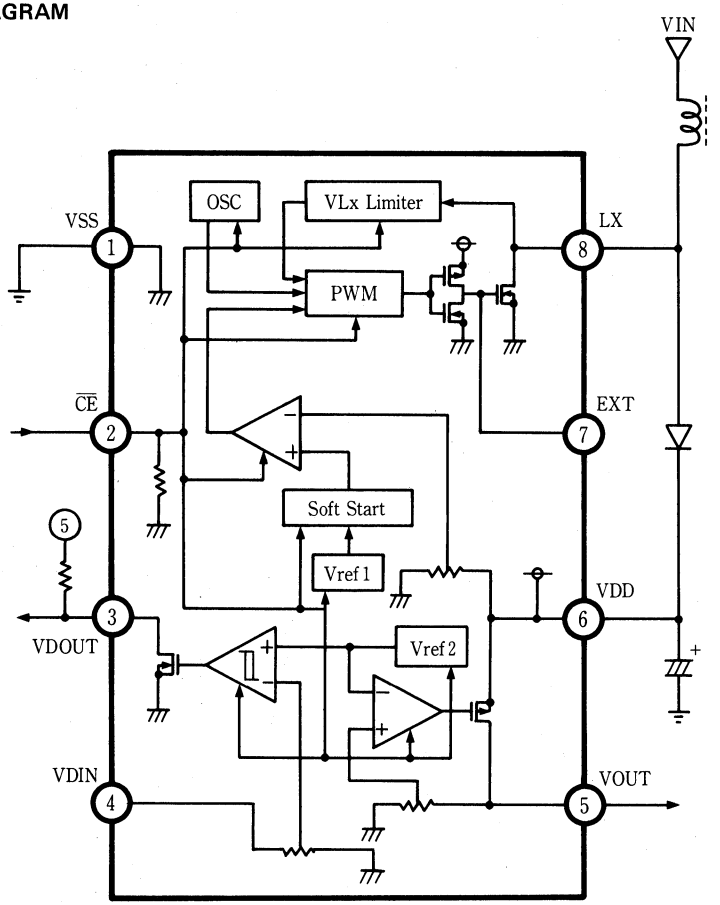
■ FEATURES

- Small invalid current ..... TYP50μA (RS5RM3624; Vin = 3.0V, no Load)
- Standby mode ..... Istb = MAX1.0μA
- Low voltage operation ..... operating voltage Vin = 0.9 ~ 10V
- High accuracy of output voltage ..... fixed output voltage, accuracy ± 2.5%
- Variety of output voltage level
- Output voltage is in the neighborhood of battery voltage due to the step-up/step-down function (Ex. getting 3V output using 3V-battery)
- Soft start and driver proof circuit
- Phase conpensation circuit
- Large current can be get by connecting a driving transistor externally.
- Small package ..... 8 pin SOP

■ APPLICATION

- Camera, Video camera, Hand-held audio system.
- Book type personal computer, Word processor, small size office automation equipment.
- Pocket bell, Code-less telephone, Hand-held telephone.

■ BLOCK DIAGRAM



■ DESCRIPTION

Pin No.	Symbol	Description
1	VSS	Ground
2	$\overline{CE}$	Chip Enable. Set the pin to VDD then the device become standby state.
3	VDOUT	Output for voltage detector (NMOS open drain output)
4	VDIN	Input for voltage detector
5	VOUT	Output for voltage regulator
6	VDD	Output for step-up voltage. Power supply for the device.
7	EXT	Driving output for external transistor
8	LX	Output for switching

■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, Vss = OV)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDD	−0.3 ~ 12	V
Output Voltage LX Pin	VLX	−0.3 ~ 12	V
EXT Pin	VEXT	−0.3 ~ VDD + 0.3	V
VOUT Pin	VOUT	−0.3 ~ VDD + 0.3	V
VDOUT Pin	VDOUT	−0.3 ~ 12	V
Input Voltage	$V\overline{CE}$	−0.3 ~ VDD + 0.3	V
Output Current LX Pin	ILX	250	mA
Power Consumption	Pd	300	mW
Operating Temperature	Topr	−30 ~ +80	°C
Storage Temperature	Tstg	−40 ~ + 125	°C
Soldering Condition	Tsolder	260°C 10sec	

■ ELECTRICAL CHARACTERISTICS

- RS5RM3624 (3.6V Output)

  Vin = 4.0V, Ta = 25°C

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Voltage	Vin	No Load	0.9		10	V
Holding Voltage	Vinhd	No Load Vin = H → L			0.8	V
Output Voltage	Vout	Vin = 4.0V, Iout = 5mA	3.51	3.60	3.69	V
Input Voltage Stability	ΔVout/Vin	Iout = 1mA, Vin = 0.9V ~ 8V		10	100	mV
Load Stability	ΔVout/Iout	Vin = 1.8V, Iout = 1 ~ 30mA		10	100	mV
Step-up Output Voltage	Vdd	Vin = 1.8V, Iout = 5mA	3.99	4.10	4.21	V
Max. Oscillating Frequency	fosc			50		kHz
Duty Ratio	DfMAX			80		%
Lx Switch on Voltage	VOL1	ILX = 50mA			0.5	V
Lx Switch Leakage Current	Ileak				2.0	μA
Detect Voltage	Vdet		2.3	2.4	2.5	V
Detect Voltage Hysteresis	Vhys			120	240	mV
VD Output on Voltage	VdOL	IOL = 5mA			0.5	V
$\overline{CE}$ "H" Input Voltage	VCEH		0.8 VDD		VDD	V
$\overline{CE}$ "L" Input Voltage	VCEL				0.2 VDD	V
$\overline{CE}$ "H" Input Current	ICEH	$\overline{CE}$ = 3.5V	0	0.5	1.0	μA
$\overline{CE}$ "L" Input Current	ICEL	$\overline{CE}$ = 0V	−0.5		0.5	μA
Consumption Current	Iin	Vin=3V (Step-up), No Load		50	100	μA
		Vin=8V (Step-down), No Load			10	μA
Standby Current	Istb	Vin = 3V, No Load			1	μA

■ SELECTION GUIDE

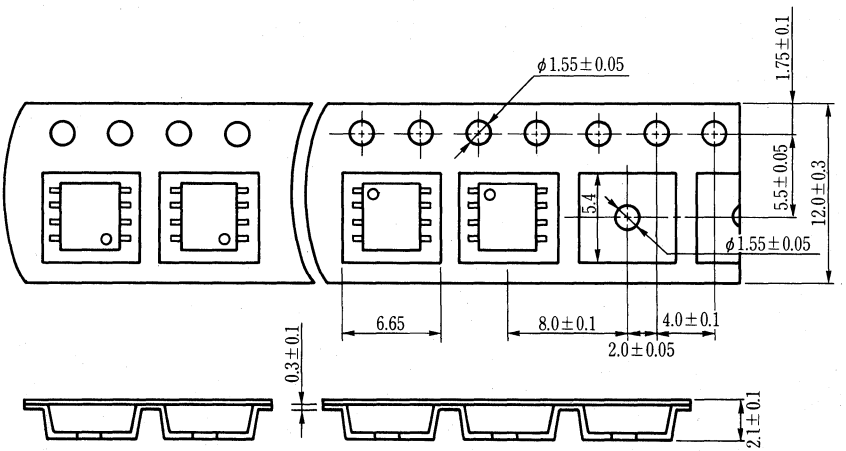
You can define the output voltage, the detect voltage and the taping direction of RS5RM series. The devices are defined by the following characters.

RS5RMXXXXX−X ← Type number

↑ ↑ ↑ ↑
a b c d

Number	Meaning
a	Defines output voltage (Vout). ● The range for Vout is 2.0V to 6.0V in units of 0.1V, with an accuracy of ±2.5%.
b	Defines detect voltage (−Vdet). ● The range for −Vdet is 2.0V to 6.0V in the units of 0.1V, with an accuracy of ±2.5%.
c	Defines version.
d	Defines taping direction with T1 and T2. (See below)

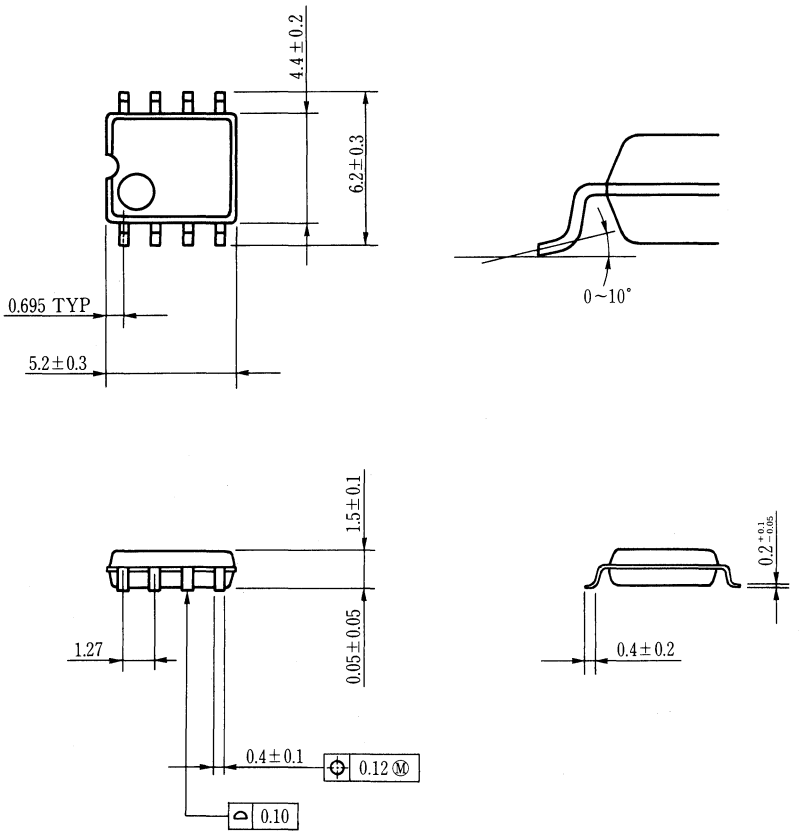
Note) Taping Information (1000 pieces/reel)



T1 Type T2 Type

(Unit: mm)

■ PACKAGE DIMENSION (Unit: mm)



RICOH

Product News

PRELIMINARY

ES-115-9202

STEP-UP/STEP-DOWN VFM DC/DC CONVERTER with VOLTAGE DETECTOR RS5RJ Series

■ OUTLINE

RS5RJ Series are compact DC/DC converter ICs with a voltage detector and are developed with CMOS process technology. The devices consist of a VFM type DC/DC converter, a series regulator and a voltage detector. As external components, a coil, a diode, and a capacitor are available for making the output constant. When the input voltage is sufficiently high, they work as series regulators. When the input voltage falls down, they work as step-up DC/DC converters. The RS5RJ series include a voltage detector and the output voltage can be detected. The chip enable can switch off the DC/DC converter and the voltage detector, and can save consumption current at standby state. The RS5RJ is fit for battery-operated equipment.

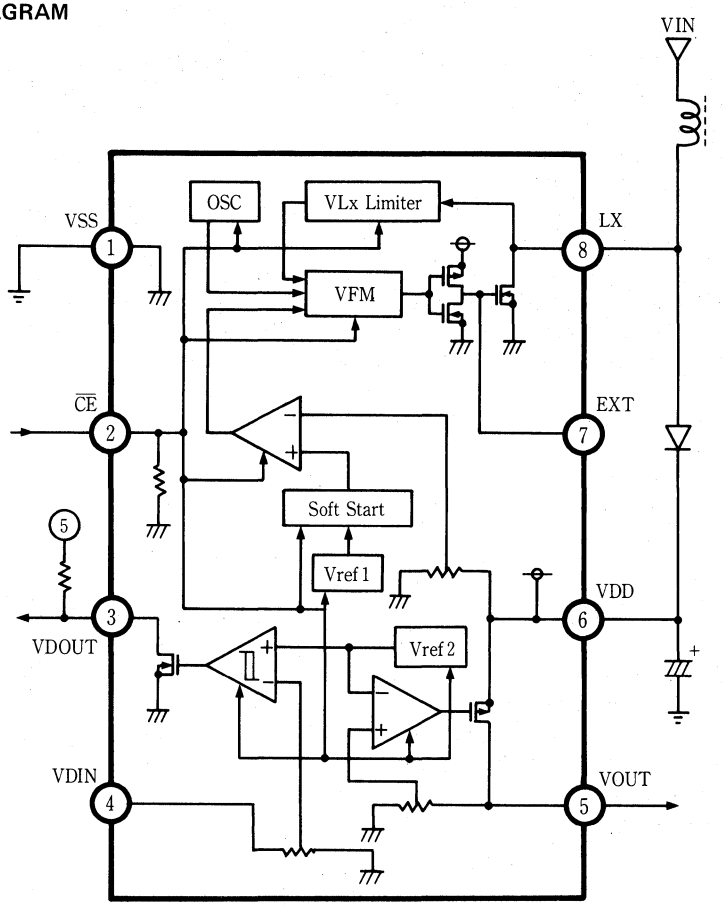
■ FEATURES

- Small invalid current ..... TYP15μA (RS5RJ3624; Vin = 3.0V, no Load)
- Standby mode ..... Istb = MAX1.0μA
- Low voltage operation ..... operating voltage Vin = 0.9 ~ 10V
- High accuracy of output voltage ..... fixed output voltage, accuracy ± 2.5%
- Variety of output voltage level
- Output voltage is in the neighborhood of battery voltage due to the step-up/step-down function (Ex. getting 3V output using 3V-battery)
- Soft start and driver proof circuit
- Phase conpensation circuit
- Large current can be get by connecting a driving transistor externally.
- Small package ..... 8 pin SOP

■ APPLICATION

- Camera, Video camera, Hand-held audio system.
- Book type personal computer, Word processor, small size office automation equipment.
- Pocket bell, Code-less telephone, Hand-held telephone.

■ BLOCK DIAGRAM



■ DESCRIPTION

Pin No.	Symbol	Description
1	VSS	Ground
2	$\overline{CE}$	Chip Enable. Set the pin to VDD then the device become standby state.
3	VDOUT	Output for voltage detector (NMOS open drain output)
4	VDIN	Input for voltage detector
5	VOUT	Output for voltage regulator
6	VDD	Output for step-up voltage. Power supply for the device.
7	EXT	Driving output for external transistor
8	LX	Output for switching

■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, Vss = OV)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDD	−0.3 ~ 12	V
Output Voltage LX Pin	VLX	−0.3 ~ 12	V
EXT Pin	VEXT	−0.3 ~ VDD + 0.3	V
VOUT Pin	VOUT	−0.3 ~ VDD + 0.3	V
VDOUT Pin	VDOUT	−0.3 ~ 12	V
Input Voltage	$V\overline{CE}$	−0.3 ~ VDD + 0.3	V
Output Current LX Pin	ILX	250	mA
Power Consumption	Pd	300	mW
Operating Temperature	Topr	−30 ~ +80	°C
Storage Temperature	Tstg	−40 ~ +125	°C
Soldering Condition	Tsolder	260°C 10sec	

■ ELECTRICAL CHARACTERISTICS

- RS5RJ3624 (3.6V Output)

  Vin = 4.0V, Ta = 25°C

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Voltage	Vin	No Load	0.9		10	V
Holding Voltage	Vinhd	No Load Vin = H → L			0.8	V
Output Voltage	Vout	Vin = 4.0V, Iout = 5mA	3.51	3.60	3.69	V
Input Voltage Stability	ΔVout/Vin	Iout = 1mA, Vin = 0.9V ~ 8V		10	100	mV
Load Stability	ΔVout/Iout	Vin = 1.8V, Iout = 1 ~ 30mA		10	100	mV
Step-up Output Voltage	Vdd	Vin = 1.8V, Iout = 5mA	3.99	4.10	4.21	V
Max. Oscillating Frequency	fosc			100		kHz
Duty Ratio	DfMAX			80		%
Lx Switch on Voltage	VOL1	ILX = 50mA			0.5	V
Lx Switch Leakage Current	Ileak				2.0	μA
Detect Voltage	Vdet		2.3	2.4	2.5	V
Detect Voltage Hysteresis	Vhys			120	240	mV
VD Output on Voltage	VdOL	IOL = 5mA			0.5	V
$\overline{CE}$ "H" Input Voltage	VCEH		0.8 VDD		VDD	V
$\overline{CE}$ "L" Input Voltage	VCEL				0.2 VDD	V
$\overline{CE}$ "H" Input Current	ICEH	$\overline{CE}$ = 3.5V	0	0.5	1.0	μA
$\overline{CE}$ "L" Input Current	ICEL	$\overline{CE}$ = 0V	−0.5		0.5	μA
Consumption Current	Iin	Vin=3V (Step-up), No Load		15	30	μA
		Vin=8V (Step-down), No Load			10	μA
Standby Current	Istb	Vin = 3V, No Load			1	μA

■ SELECTION GUIDE

You can define the output voltage, the detect voltage and the taping direction of RS5RJ series. The devices are defined by the following characters.

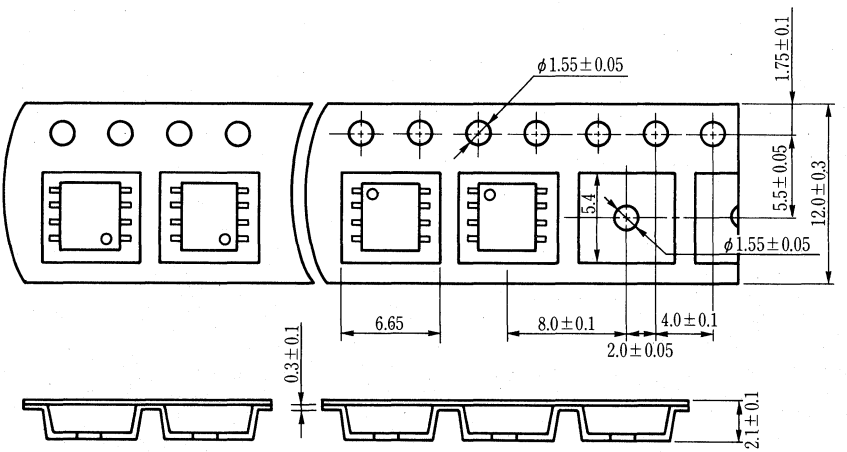
RS5RJXXXXX−X ← Type number

↑ ↑ ↑ ↑

a b c d

Number	Meaning
a	Defines output voltage (Vout). ● The range for Vout is 2.0V to 6.0V in units of 0.1V, with an accuracy of ±2.5%.
b	Defines detect voltage (−Vdet). ● The range for −Vdet is 2.0V to 6.0V in the units of 0.1V, with an accuracy of ±2.5%.
c	Defines version.
d	Defines taping direction with T1 and T2. (See below)

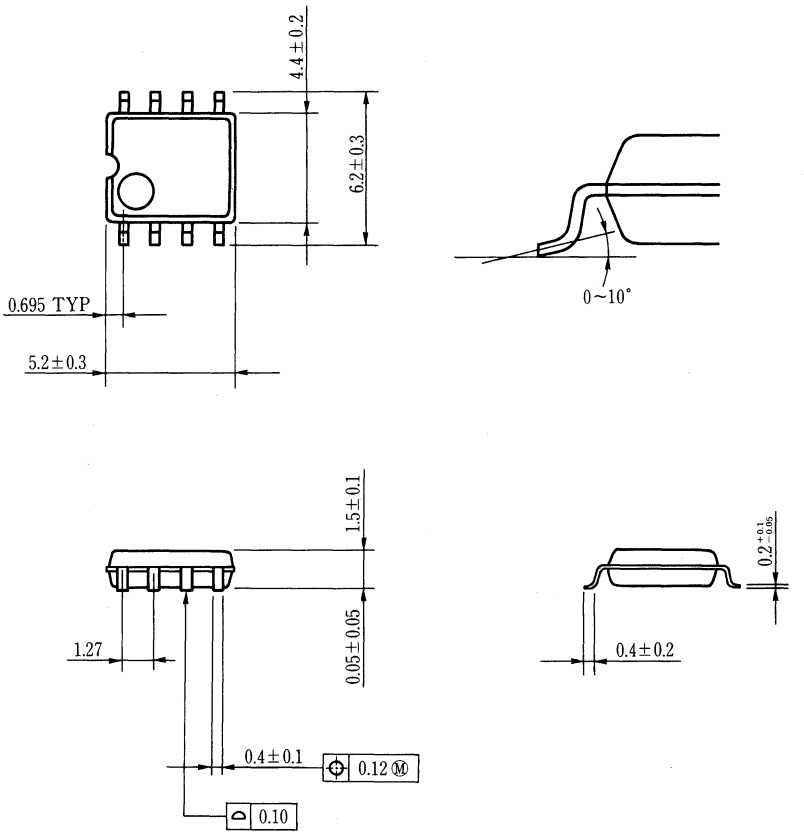
Note) Taping Information (1000 pieces/reel)



T1 Type T2 Type

(Unit: mm)

■ PACKAGE DIMENSION (Unit: mm)



RICOH

PRELIMINARY

ES-112-9205

Product News

PWM STEP-UP SWITCHING REGULATOR RH5RH XX1A/XX2B Series

RH5RHxx1A/xx2B Series ICs are PWM control step-up switching regulators developed with CMOS technology.

The xx1A Series ICs consist of an oscillator circuit, PWM control circuit, control transistor (Lx switch), reference voltage source, error amplifier circuit, phase correction circuit, voltage detection resistor, slow start circuit, and Lx switch protection circuit.

Unlike other PWM switching regulator ICs, the xx1A Series ICs do not require complex external circuits. Only three components – coil, diode, and capacitor – are required for the low-ripple, high-efficiency step-up switching regulator ICs.

The xx2B ICs internally use the same chip as the xx1A Series, but have an external transistor drive pin (EXT) instead of an Lx pin. Attaching an external power transistor with a small ON resistance allows large current to flow in the coil, thus achieving a large output current. The xx2B Series ICs are suitable for applications that require large output current between 10 mA and 100 mA.

The new PWM control circuit suppresses the self-power consumption of these ICs to Typ. 30 μA (5V models), which compares to VFM (chopper) control type switching regulators that consumes relatively low power.

When the input voltage is higher than the specified output voltage plus the voltage drop in the diode coil, the oscillator circuit stops to reduce its own power consumption to Typ. 2 μA.

These ICs are suitable for users who need low ripples but cannot use conventional PWM switching regulators because of high power consumption.

The high performance and low power consumption of these ICs makes them suitable for battery-operated devices.

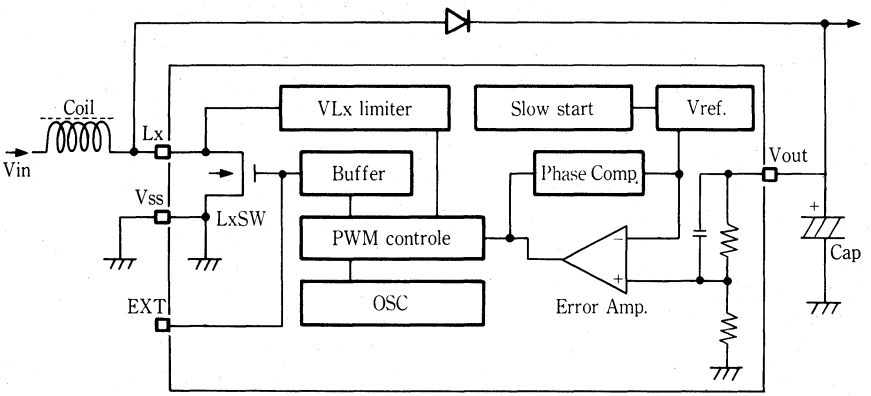
FEATURES

- Only 3 peripheral parts ..... Coil, diode, capacitor
- Low consumption current ..... 30 μA (Typ. 501A)
- Small ripple, Low noise
- Low voltage operation (Output current 1 mA) ... 0.9V (Max.)
- High output voltage accuracy ..... ±2.5% (Max.)
- High efficiency ..... 85% (Typ.)
- Small temperature drift of output voltage ..... ±50 ppm (Typ.)
- Slow · start ..... 500 μs (Min.)
- Compact package ..... Mini power mold (SOT-89 3 pin)

APPLICATIONS

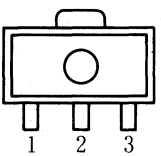
- Constant voltage supply for battery-operated devices
- Constant voltage supply for cameras, camcorders, electronic, and portable communication devices
- Constant voltage source for devices that require low noise and low power consumption such as portable audio equipment
- Constant voltage source for devices that require a higher voltage than battery voltages

■ BLOCK DIAGRAM



The gain of the Error Amp. is 80 dB. The internal Phase Comp. circuit yields a frequency characteristics where the 1st pole is at 0.05 Hz and zero point is at 500 Hz. And the dividing resistor and capacitor connected to Vout pin yields a zero point at fz = 1.5 kHz.

■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin No.		Name	Description
xx1	xx2		
1	1	Vss	Ground
2	2	Vout	Voltage Output
3	–	Lx	Switching pin (Open Drain)
–	3	EXT	Transistor drive pin (CMOS output)

■ RH5RH Series

RH5RHxxxx
- version
- type
- output voltage

Example: RH5RH501A . . . Output Voltage 5.0V (Transistor mounted)
RH5RH352B . . . Output Voltage 3.5V (Transistor connected externally)

■ ABSOLUTE MAXIMUM RATINGS

(Vss = 0V)

Parameter	Symbol	Rating	Unit
Vout Voltage	Vout	12	V
Lx Voltage	VLx	12	V
EXT pin Voltage	VEXT	−0.3 ~ Vout + 0.3	V
Lx Output Current	ILx	250	mA
EXT pin Current	IEXT	±50	mA
Power Dissipation	Pd	500	mW
Operating Temperature	Topr	−30 ~ +80	°C
Storage Temperature	Tstg	−40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

RH5RH501A (Vout = 5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				8	V	
Starting Voltage	Vst	Iout = 1 mA, Vin : 0 → 3V		0.8	0.9	V	
Holding Voltage	Vhld	Iout = 1 mA, Vin : 3 → 0V	0.7			V	
Current Consumption 1	Idd1	at Vout pin		30	45	μA	
Current Consumption 2	Idd2	at Vout pin, Vin = 5.5V		2	5	μA	
Output Voltage	Vout		4.875	5.000	5.125	V	
Lx Switching Current	ILx	VLx = 0.4V	80			mA	
Lx Leakage Current	ILxL	VLx = 6V, Vin = 5.5V			0.5	μA	
Oscillating Frequency	fosc		40	50	60	kHz	
Max. Duty Ratio	Maxdty	on (VLx "L")	70	80	90	%	
Efficiency	Effi		70	85		%	
Slow start Time	tst	Time for Vout = 0 → 5V	0.5	2.0		ms	1
VLx Limit Voltage	VLxlmt	Lx Switch on	0.65	0.8	1.0	V	2

Condition : Vin = 3V, Vss = 0V, Iout = 10 mA, Ta = 25°C (See Fig. 1)

RH5RH502B (Vout = 5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				8	V	
Starting Voltage	Vst	EXT no Load, Vout : 0 → 3V		0.7	0.8	V	
Current Consumption 1	Idd1	EXT no Load, Vout = 4.8V		60	90	μA	
Current Consumption 2	Idd2	EXT no Load, Vout = 5.5V		2	5	μA	
Output Voltage	Vout		4.875	5.000	5.125	V	
EXT "H" Output Current	IEXTH	VEXT = Vout −0.4V	−2			mA	
EXT "L" Output Current	IEXTL	VEXT = 0.4V	2			mA	
Oscillating Frequency	fosc		80	100	120	kHz	
Max. Duty Ratio	Maxdty	VEXT "H"	70	80	90	%	
Slow start Time	tst	Vout = 0 → 5V	0.5	2.0		ms	Note 1

Condition : Vin = 3V, Vss = 0V, Iout = 10 mA, Ta = 25°C (See Fig. 2)

RH5RH301A

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				8	V	
Starting Voltage	Vst	Iout = 1 mA, Vin : 0 → 2V		0.8	0.9	V	
Holding Voltage	Vhld	Iout = 1 mA, Vin : 2 → 0V	0.7			V	
Current Consumption 1	Idd1	at Vout pin		15	25	μA	
Current Consumption 2	Idd2	at Vout pin, Vin = 3.5V		2	5	μA	
Output Voltage	Vout		2.925	3.000	3.075	V	
Lx Switching Current	ILx	VLx = 0.4V	60			mA	
Lx Leakage Current	ILxL	VLx = 6V, Vin = 3.5V			0.5	μA	
Oscillating Frequency	fosc		40	50	60	kHz	
Max. Duty Ratio	Maxdty	on (VLx "L")	70	80	90	%	
Efficiency	Effi		70	85		%	
Slow start Time	tst	Time for Vout = 0 → 5V	0.5	2.0		ms	Note 1
VLx Limit Voltage	VLxlmt	Lx Switch	0.65	0.8	1.0	V	Note 2

Condition : Vin = 2V, Vss = 0V, Iout = 10 mA, Ta = 25°C (See Fig. 1)

RH5RH302B (Vout = 5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				8	V	
Starting Voltage	Vst	EXT no Load, Vout : 0 → 2V		0.7	0.8	V	
Current Consumption 1	Idd1	EXT no Load, Vout = 2.9V		30	50	μA	
Current Consumption 2	Idd2	EXT no Load, Vout = 3.5V		2	5	μA	
Output Voltage	Vout		2.925	3.0	3.075	V	
EXT "H" Output Current	IEXTH	VEXT = Vout −0.4V	−1.5			mA	
EXT "H" Output Current	IEXTL	VEXT = 0.4V	1.5			mA	
Oscillating Frequency	fosc		80	100	120	kHz	
Max. Duty Ratio	Maxdty	VEXT "H"	70	80	90	%	
Slow start Time	tst	Vout = 0 → 3V	0.5	2.0		ms	Note 1

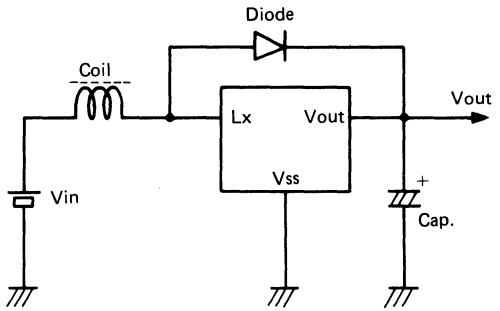
Condition : Vin = 2V, Vss = 0V, Iout = 10 mA, Ta = 25°C (See Fig. 2)

Note 1: The slow start circuit follows the sequence below:
Vin application → Vref is kept at 0V for about 200 μs → During this period, error amplifier output is brought to "H" → Vref rises and then the error amplifier output gradually lowers to the appropriate value due to the internal phase compensator circuit. Accordingly, the output gradually lowers.

Note 2: ILx gradually rises after the Lx switch is turned on, and VLx rises accordingly. If the voltage reaches VLxlmt, the Lx switch protection circuit turns off the Lx switch.

■ CIRCUIT EXAMPLE

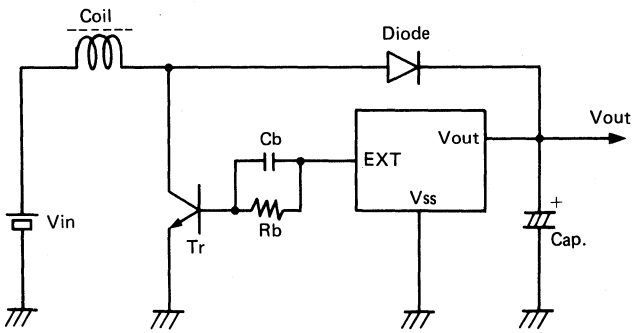
1. RH5RHxx1A



Parts Coil : 120 μH (Sumida Electric Company Ltd. CM-5)
Diode : MA721 (Matsushita Electronics Corp. type Schottkey)
Capacitor : 22 μF (Tantalum type)

Fig. 1

2. RH5RHxx2B



Parts Coil : 28 μH (Troidal Core type)
Diode : HRP22 (Hitachi, Schottkey type)
Capacitor : 100 μF (Tantalum type)
Transistor : 2SD1628G
Base resistor : 300Ω
Base capacitor : 0.01 μF

Fig. 2

■ OUTPUT CURRENT AND PERIPHERAL COMPONENT

This section describes the relationship between the output current and peripheral components for the circuit in Figure 1.

According to the on time of the Lx transistor, a PWM switching regulator operates in two modes: intermittent mode and continuous mode.

Assuming coil inductance as L, the maximum output current in intermittent mode is:

$$Iout = fosc \cdot Vin^2 \cdot ton^2 / [2 \cdot L \cdot (Vout - Vin)] \quad \text{(Equation 1)}$$

Here, if:

$$tonc = (1 - Vin/Vout)/fosc$$

$$tonc < tonmax = maxdty/(fosc \cdot 100) \quad \text{(Equation 2)}$$

Then:

$$ton = tonc$$

If Equation 2 does not apply:

$$ton = tonmax$$

Here, the peak current in the Lx switch coil diode is:

$$ILmax = Vin \cdot ton/L \quad \text{(Equation 3)}$$

Thus, I/O conditions and peripheral components must be selected in consideration to ILxmax.

If Equation 2 applies, Iout may be greater than that calculated by Equation 1. At that time, the switching regulator operates in continuous mode, which can generate up to the current calculated by the Equation below:

$$Iout = fosc \cdot Vin^2 \cdot ton^2 / [2 \cdot L \cdot (Vout - Vin)] + Vin \cdot Iconst/Vout \quad \text{(Equation 4)}$$

Here, Iconst is a current that continuously flows in the coil. At that time, ILxmax becomes very great:

$$ILxmax = Iconst + Vin \cdot ton/L \quad \text{(Equation 5)}$$

Therefore, be careful with ILxmax.

The above description applies only to ideal cases; it does not include the losses in external components and the Lx switch. In reality, the efficiency is 50% to 80% of the values obtained by the above calculation. In particular, if ILx is large or Vin is low, note that the loss of Vin is as same as VLx. For Vout, always consider Vf (about 0.3V) in the diode.

For applications where ILx or VLx is critical, use RH5RHxx2B and attach an external transistor with a low ON resistance.

■ NOTICE

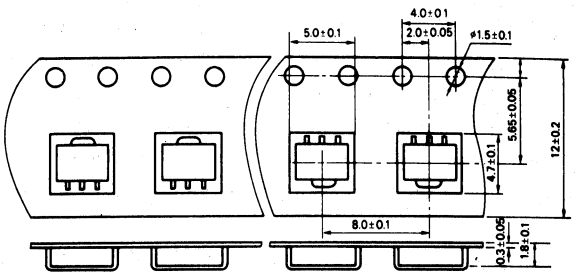
To use these ICs, note the following points:

- Place external components as close to the IC to reduce wiring. In particular, wire the capacitor connected to the Vout pin using the shortest route possible.
- Ensure sufficient grounding. The Vss pin receives large current due to switching. High impedance in the Vss routing causes the internal potential of the IC to fluctuate with the switching current, resulting in unstable operation.
- Use capacitors with good high frequency response, such as tantalum capacitors or electrolytic aluminum + ceramic capacitors. The capacity must be 10 μF or more. It is recommended that the withstand voltage of the capacitors be at least three times the specified output voltage, because the coil may cause a high spike-like voltage when the Lx transistor is turned off.
- Select coils that have a small DC resistance and are not magnetic-saturated easily. If the coil inductance is too small, ILx may exceed the absolute maximum rating under maximum load. Select the proper inductance value.
- Use Schottky diodes with a fast switching speed. Be careful of the current capacity. (See Page8)

■ PACKAGING INFORMATION

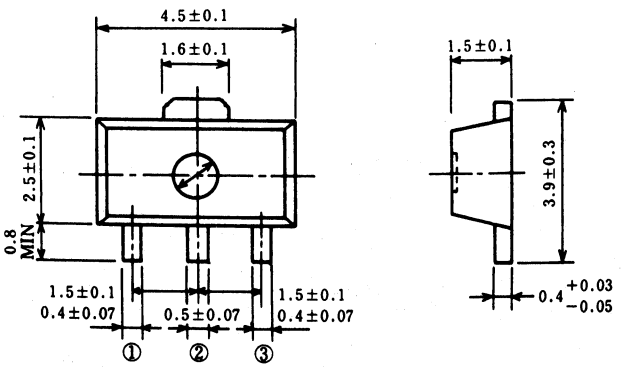
1. The packaging method is specified with the device model number as follows.
   RH5RH301A-T1 : Taping
   RH5RH301A-T2 : Taping

2. Taping method



T1 type T2 type

■ PACKAGE DIMENSION



RICOH

Preliminary

ES-118-9207

Product News

VFM STEP - UP SWITCHING REGULATOR

RH5RI × × 1B / × × 2B series

The RH5RI × × 1 and × × 2 are VFM (chopper) control type - low current consumption, step-up switching regulator ICs using low power linear CMOS technology.

The × × 1 type internally comprises an oscillator, VFM control circuit, control transistor (Lx switch), standard voltage supply, differential amplifier circuit, voltage sensing resistor and an Lx switch protective circuit using a mere three externally connected components a coil, diode and capacitor. The connection of a complex external components arrangement necessary until now in conventional devices has been eliminated in this high efficiency rising voltage switching regulator.

The × × 2 type utilizes the same chip as the × × 1 type. A transistor drive terminal (EXT) has been connected externally in place of the Lx terminal. The connection of a small external power transistor having only a small resistance while switched on, allows a large current flow and therefore, a large current can be taken from the output. This device is ideal for the user needing current output from less than one hundred all the way up to several hundred milliamps.

This device is ideal for use with battery operated devices and combines high efficiency operation with ultra-low current consumption.

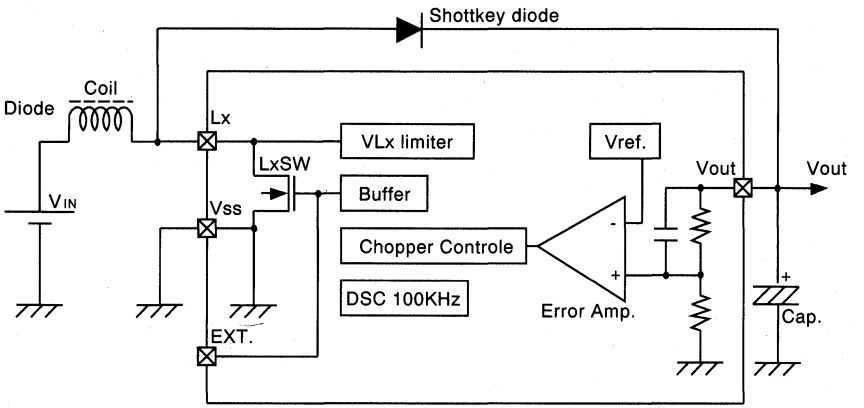
■ FEATURES

Only 3 peripheral parts	Coil, diode, capacitor
Low consomption current	4 μA (3 V, 1.5 V Input, No Load, Typ.)
High output voltage accuracy	± 2.5% (Max.)
Low valtage operation (Output current 1 mA)	0.9 V (Max.)
High efficiency	80 % (Typ.)
Small temperature drift of output voltage	± 50 ppm (Typ.)
Compact package	SOT - 89 3pin

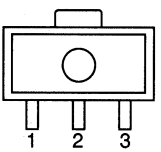
■ APPLICATIONS

Constant voltage supply for battery - operated devices.
Constant voltage supply for cameras, camcorders, electronic, and portable communication devices.
Constant voltage source for devices that require a higher voltage than battery voltages.

■ BLOCK DIAGRAM

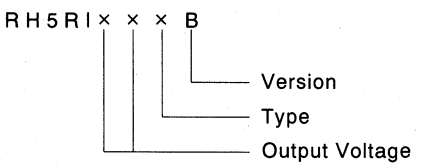


■ PIN CONFIGURATION



Pin No.		Name	Description
× × 1	× × 2		
1	1	V_{SS}	Ground
2	2	V_{OUT}	Voltage Output
3	–	L_X	Switching Pin (Open Drain)
–	3	EXT	Transistor Drive Pin (CMOS Output)

■ RH5RI Series



Example : RH5RI501B ····· Output Voltage, Lx Tr Build - in
: RH5RI352B ····· Output Voltage, Transistor Tr Connected externally

■ ABSOLUTE MAXIMUM RATINGS

(Vss = OV)

Parameter	Symbol	Rating	Unit
Vout Voltage	Vout	12	V
Lx Voltage	VLx	12	V
Ext Voltage	VEXT	−0.3～Vout+0.3	V
Lx Output Current	ILx	250	mA
EXT Current	IEXT	±50	mA
Power Dissipation	Pd	500	mW
Operating Temperature	Topr	−30～+80	℃
Storage Temperature	Tstg	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

RH5RI501B

(Vout = 5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note.
Output Voltage	Vout		4.875	5.000	5.125	V	
Max. Input Voltage	Vin				8	V	
Starting Voltage	Vst	Iout=1mA, Vin : 0→3V		0.8	0.9	V	
Holding Voltage	Vhld	Iout=1mA, Vin : 3→0V	0.7			V	
Input Current 1	Iin 1	at Vin Pin, No Load		6	12	μA	
Input Current 2	Iin 2	at Vin Pin, Vin=5.5V		2	5	μA	
Lx Switch Current	ILx	VLx=0.4V	80			mA	
Lx Leakage Current	ILxL	VLx=6V, Vin=5.5V			0.5	μA	
Max. Oscillating Freguency	fosc		80	100	120	kHz	
Duty Ratio	maxdty	on (VLx"L")	65	75	85	%	
Efficiency	Effi		70	80		%	
VLx Limit Voltage	VLxlmt	Lx Switch ON	0.65	0.8	1.0	V	Note

Condition : Vin=3 V, Vss=0 V, Iout=10 mA, Ta=25℃ (See Fig. 1)

RH5RI502B

(Vout = 5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note.
Output Voltage	Vout		4.875	5.000	5.125	V	
Max Input Voltage	Vin				8	V	
Starting Voltage	Vst	EXT No Load, Vout : 0→3V		0.7	0.8	V	
Current Consumption 1	Idd 1	EXT No Load, Vout=4.8V		60	90	μA	
Current Consumption 2	Idd 2	EXT No Load, Vout=5.5V		2	5	μA	
EXT"H" Output Current	IEXTH	VEXT=Vout−0.4V	−2			mA	
EXT"L" Output Current	IEXTL	VEXT=0.4V	2			mA	
Max Oscillating Frequency	fosc		80	100	120	kHz	
Duty Ratio	maxdty	VEXT"H"	65	75	85	%	

Condition : Vin=3 V, Vss=0 V, Iout=10 mA, Ta=25℃ (See Fig. 2)

RH5RI301B

(Vout = 3V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note.
Output Voltage	Vout		2.925	3.000	3.075	V	
Max. Input Voltage	Vin				8	V	
Starting Voltage	Vst	Iout=1mA, Vin : 0→2V		0.8	0.9	V	
Holding Voltage	Vhld	Iout=1mA, Vin : 2→0V	0.7			V	
Input Current 1	Iin 1	at Vin Pin, No Load		4	8	μA	
Input Current 2	Iin 2	at Vin Pin, Vin=3.5V		2	5	μA	
Lx Switching Current	ILx	VLx=0.4V	60			mA	
Lx Leakage Current	ILxL	VLx=6V, Vin=3.5V			0.5	μA	
Max Oscillating Freguency	fosc		80	100	120	kHz	
Duty Ratio	maxdty	on (VLx"L")	65	75	85	%	
Efficiency	Effi		70	80		%	
VLx Limit Voltage	VLxlmt	Lx Switch ON	0.65	0.8	1.0	V	Note

Condition : Vin=2 V, VSS=0 V, Iout=10 mA, Ta=25℃ (See Fig. 1)

RH5RI302B

(Vout = 3V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note.
Output Voltage	Vout		2.925	3.000	3.075	V	
Max Input Voltage	Vin				8	V	
Starting Voltage	Vst	EXT No Load, Vout : 0→2V		0.7	0.8	V	
Current Consumptin 1	Idd 1	EXT No Load, Vout=2.9V		30	50	μA	
Current Consumptin 2	Idd 2	EXT No Load, Vou=3.5V		2	5	μA	
EXT"H" Output Current	IEXTH	VEXT=Vout−0.4V	−1.5			mA	
EXT"H" Output Current	IEXTL	VEXT=0.4V	1.5			mA	
Max Oscillating Frequency	fosc		80	100	120	kHz	
Duty Ratio	maxdty	VEXT"H"	65	75	85	%	

Condition : Vin=2 V, Vss=0 V, Iout=10 mA, Ta=25℃ (See Fig. 2)

Note : The ILx increases steadily after the Lx switch is set to ON due to use of an external coil. The accompanying VLx also increases. When the VLx reaches the VLxlmt, the Lx switch is set to OFF by the protective circuit.

■ CIRCUIT EXAMPLE

RH5RI × ×1B

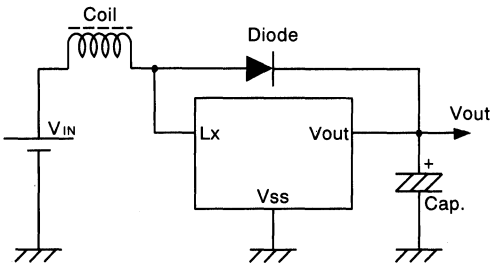


Fig.1

Parts : Coil ····· 82 μ H (Sumida Electric Company, CM - 5)
: Diode ····· MA721 (Matsushita Electronics Corp. Schottkey type)
: Capacitor ····· 22 μ F (Tantalum type)

RH5RI × ×2B

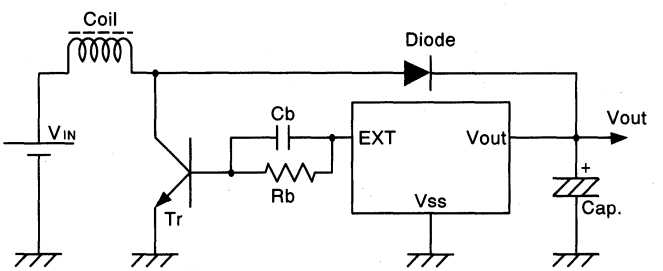


Fig.2

Parts : Coil ····· 28 μ H (Troidal Core Type)
: Diode ····· HRP22 (Hitachi Schottkey Type)
: Capacitor ····· 100 μ F (Tantalum Type)
: Transistor ····· 2SD1628G
: Base Resistor ····· 300Ω
: Base Capacitor ····· 0.01 μ F

■ OUTPUT CURRENT and PERIPHERAL COMPONENT

The following describes the interaction between the output current and peripheral components in the circuit of Figure 1.
With a coil inductance set at L, the maximum current during intermittent mode (VFM normal operating mode) is

$$Iout = Vin^2 \cdot maxdy^2 / \{ 20000 \cdot fosc \cdot L \cdot (Vout - Vin) \}$$

At this time the peak current flowing through the Lx switch coil diode is

$$ILxmax = Vin \cdot maxdty / (100 \cdot fosc \cdot L)$$

The ILxmax is an important I / O power factor that must be considered when choosing the peripheral components.

The above are calculations under ideal conditions and do not include losses in the external components and the Lx switch which may, in fact, amount to between 50 and 80 percent. Caution is particularly needed at times such as when the ILx is large and Vin is low as Vin loss will occur due to VLx. It is also necessary to take into account the amount of diode Vf (about 0.3 V) for calculating the actual Vout.

When ILx and VIx become a problem, use the RH5RI × ×2B and utilize a peripheral transistor with low resistance while switched on.

■ NOTICE

Observe the following precautions when using this IC.

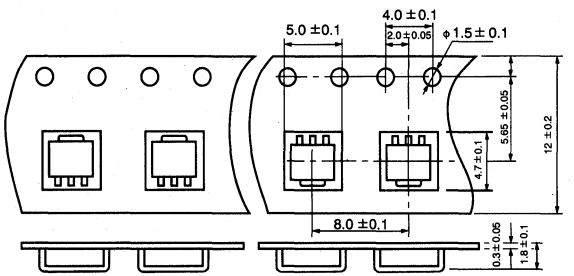
- Locating external components as closes as possible to the IC and keep the wiring short. In particular, capacitor wiring connected to the Vout terminal should be kept to a minimum length.
- Make sure ground wiring is of sufficient strength as a large current will flow at the Vss terminal due to transistor switching. When Vss wiring impedance is high and the IC's internal electrical potential deviates due to current switching, device operation can become unstable.
- Make sure the capacitor has a capacitance of at least 10 μF and has good high frequency characteristics such as obtained with a tantalum capacitor or aluminum electrolytic and ceramic capacitor. When choosing the capacitor , it is recommended that it be able to withstand a voltage at least three times higher than the normal capacitor voltage output since a high voltage spike may be generated from the coil when the Lx transistor is off.
- Care is also required when selecting the coil. Select a coil with low resistance to direct current, adequate current carrying capacity and resistance to magnetic saturation. The ILx may exceed its absolute maximum rated value during a maximum load when the coil inductance value it too low. Therefore, please select a suitable inductance value (reter to page 8).
- When choosing a diode, select a high speed switching Schottky type.
  Ensure it has adequate current carrying capacity (refer to page 8).

☆ The performance of the power supply circuit using this IC is greatly influenced by the peripheral circuit. Ensure that the component parts for the peripheral circuit have the correct circuit values needed before use.
It is essential that allowance is made in the circuit design so that the rated velues (voltage, current and power) are not exceeded in each part of the circuit board and IC.

■ PACKAGING INFORMATION

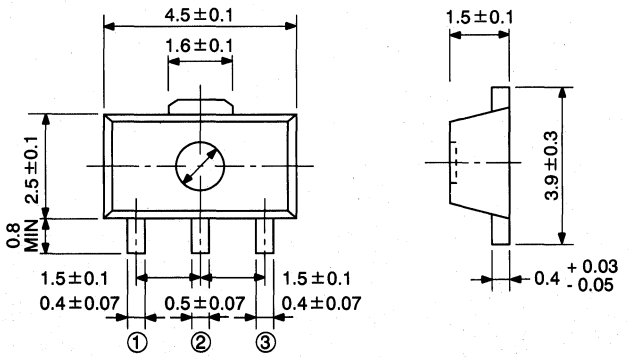
1. The packaging method is specified with device model number as follows.
   RH5RI 301 B - T1 : Taping
   RH5RI 301 B - T2 : Taping

2. Taping method



T1 Type T2 Type

■ PACKAGE DIMENSION



RF5C133

DC/DC MULTI•POWER SUPPLY

RF5C133 is a power circuit controller IC containing three CMOS process DC/DC converter control circuit systems (two ON-time control PWM systems and one OFF-time control VFM system).
With additional components, can RF5C133 configure three SWR systems to generate the CPU power supply voltage, charging voltage, or circuit power supply voltage from AC adapters, dry batteries, or rechargeable batteries. Furthermore, RF5C133 has the following six functions:

1. With the built-in power supply voltage detector, RF5C133 outputs low voltage alarms for dry or rechargeable batteries and for the CPU power supply. (Alarms for batteries are output in frequencies. A V/F converter converts the voltages into frequencies.)
2. RF5C133 controls the charging of rechargeable batteries by AC adapter output. The batteries are charged by a constant current initially, then by a constant voltage after the upper limit voltage is reached. The values for the constant current and voltage are specified externally. While the batteries are being charged, RF5C133 outputs charge indication signals. Upon detection of a low charge current, RF5C133 stops the signals.
3. To protect the charge system, RF5C133 detects and latches output overcurrents and set heating (an external diode must be added externally) and sends alarms. The alarms are released at the rising edge of charge control input signals.
4. The power saving function turns off the circuit power supply voltage generator.
5. RF5C133 can be soft-started to prevent rush current occurring when the output in the circuit or charge system rises.
6. RF5C133 can operate based solely on the internal clock. After self-activation, external sync clocks can be input.

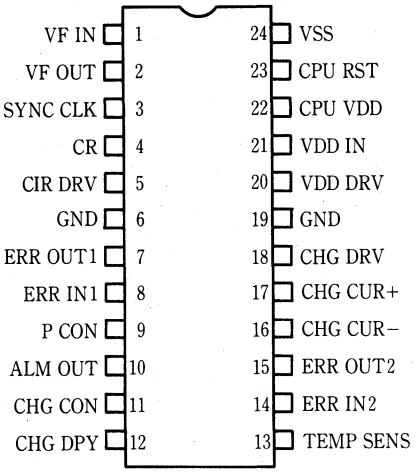
■ FEATURES

- Step-up, step-down, and inversion DC/DC converters can be easily designed by combining RF5C133 with coils, capacitors, and diodes.
- Low current consumption ..... 25 μA (Typ., stand-by)
- High efficiency ..... 70% to 80% (Typ., depends on circuit configuration)
- Accurate output voltage ..... ±5%
- Small temperature drift of output voltage . ±100 ppm/°C
- Package ..... 24-pin shrink SOP

■ APPLICATIONS

Voltage control for portable CD players, electronic book players, video equipment, notebook personal computers, and other battery-operated equipment.

■ PIN CONFIGURATION



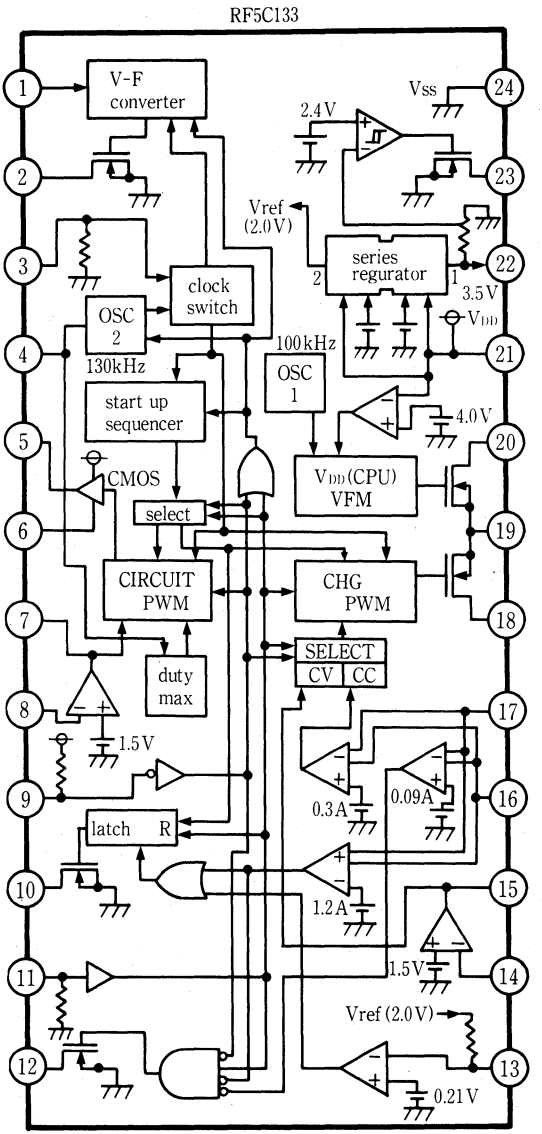
■ PIN DESCRIPTION

To use pins marked *, pull up the signals to the "H" level.

Pin No.	Pin Name	Signal Name	I/O	Description
1	VF IN	VF Converter	Input	Connect to the positive pole of a dry or rechargeable battery. During operation of the circuit or charge system, the potential of the dry or rechargeable battery is detected at this pin.
2	VF OUT *	VF Converter	Nch Open Drain Output	The potential (1.8 to 3.3 V) detected at VF IN is converted into a frequency (1/(4096 × 32) to 1/(4096 × 2) of the external or internal clock OSC2) and output through this pin.
3	SYNC CLK	Synchronized Clock	Input	To synchronize the operation of circuit or charge SWR with an external clock, sync clock signals are input through this pin (176 kHz). The external and built-in clocks are switched automatically. A pull-down resistor is built in.
4	CR	CR	Input	Use an external CR to specify the oscillating frequency for the circuit or charge systems or to specify the maximum duty of the circuit system.
5	CIR DRV	Circuit SWR Drive	CMOS Output	Through this pin, the driver transistor for the circuit SWR is driven by ON-time control PWM.
6	GND		GND	This is the power grounding pin to feed the source current to CIR DRV.
7	ERR OUT1	Error Amp. Output 1	Output	The error output of the circuit power supply voltage is amplified and output through this pin. To adjust the feedback constant, use the C and R externally attached between ERR IN1 and this pin.
8	ERR IN1	Error Amp. Input 2	Input	The error voltage of the circuit power supply voltage is detected at this pin. To specify the circuit power supply voltage, use an external resistor.

Pin No.	Pin Name	Signal Name	I/O	Description
9	P CON	Power Save Switch	Input	When P CON = "H", the circuit power supply voltage generator circuit stops. A pull-up resistor is built in.
10	ALM OUT *	Alarm	Nch Open Drain Output	When a 1 overcurrent or 2 TEMP SENSE input abnormality (of the AC adapter output) is detected and latched, an alarm is output through this pin.
11	CHG CON	Charge Control	Input	When CHG CON = "H", charging is possible. The ALM OUT output is reset at the rising edge of CHG CON = "L" → "H". A pull-down resistor is built in.
12	CHG DPY *	Charge Display	Nch Open Drain Output	When a normal charge current is detected while CHG CON = "H", signals are output through this pin.
13	TEMP SENS	Temperature Sence	Input	This pin is used to feed a forward current to an external diode. According to the temperature characteristics of the VF of the diode, abnormal heat is detected. A regulated current source from internal Vref (2 V) is built in.
14	ERR IN2	Error Amp. Input 2	Input	The error voltage of the charge power supply voltage is detected. To specify the voltage and temperature characteristics of the charging source, add an external resistor and diode.
15	ERR OUT2	Error Amp. Output 2	Output	The error voltage of the charge power supply voltage is amplified and output through this pin. To adjust the feedback constant, use the C and R externally attached between ERR IN and this pin.
16	CHG CUR–	Charge Current (–)	Input	The current of the charge system is detected at this pin. Attach an external resistor (0.5Ω) between CHG CUR+ and this pin to detect the current.
17	CHG CUR+	Charge Current (+)	Input	The current of the charge system is detected at this pin. Attach an external resistor (0.5Ω) between CHG CUR– and this pin to detect the current.
18	CHG DRV	Charge SWR Drive	Nch Open Drain Output	Through this pin, the driver transistor for the charge SWR is driven by ON-time control PWM.
19	GND		GND	This is the power grounding pin to feed the source current to the charge system and CPU power supply drive.
20	VDD DRV	VDD SWR Drive	Nch Open Drain Output	Through this pin, the SWR for the self-bias and CPU power supply system is driven by OFF-time control VFM.
21	VDD (IC)	VDD (IC)	Input	The voltage obtained by SWR through VDD DRV (Typ. 4.0 V) is input to this pin. This voltage is used as the potential of the IC board (IC power supply potential).
22	CPU VDD	CPU Power Supply	Output	A constant voltage (Typ. 3.5 V), obtained by stepping down the VDD (IC) voltage with a series regulator, is output through this pin.
23	CPU RST *	CPU Reset	Nch Open Drain Output	The CPU VDD output voltage is detected at this pin. When the voltage becomes lower than the specified value (Typ. 2.4 V), signals are output through this pin.
24	VSS	VSS (IC)	GND	This is the internal logic grounding of the IC. Connect to the grounding.

■ BLOCK DIAGRAM



■ DESCRIPTION

1. Internal Oscillator

OSC1 (OSC1 and OSC2 are asynchronous.)

OSC1 is an oscillator circuit using a ring oscillator. (Typ. 100 kHz, ON-time duty is Typ. 65%.)

- OSC1 generates clock signals for VDD (CPU) VFM operation. The VDD (CPU) PWM operation generates the power supply voltage (VDD) for RF5C133 between the external diode and capacitor.
- OSC1 is activated by applying the minimum operating voltage or a higher voltage to the VDD (IC) pin ㉑

OSC2

OSC2 is an oscillator circuit by means of external C and R. (Typ. 130 kHz)

- OSC2 generates clock signals for the PWM operation of the circuit and charge systems.
- Connect C and R between CPU VDD ㉒ and VSS ㉔. C = 470 pF (±5%) and R = 18 kΩ (±0.5%).
- OSC2 is activated when P CON ⑨ is set to "L" or CHG CON ⑪ is set to "H".

2. Clock Switch

This circuit switches internal and external clocks. (OSC2 → SYNC CLK)

- To synchronize the PWM operation of the circuit and charge systems with an external clock, input external clock signals to SYNC CLK pin ③. (Typ. 176 kHz)
- Upon detection of the rising edge of external clock signals ("L" → "H"), the clock for the IC is switched from the internal clock (Typ. 130 kHz) to an external clock (Typ. 176 kHz).

3. Start-up Sequencer

The start-up sequencer prevents the rush current from entering the coil when the circuit or charge SWR is activated.

- The circuit SWR is soft-started when P CON ⑨ goes "L".
- The charge SWR is soft-started when CHG CON ⑪ goes "H".
- When P CON ⑨ = "L" and CHG CON ⑪ = "H" compete, priority is given to the first to be input.
- If the interval between the two inputs is within 252.1 msec, the two outputs change simultaneously. See the table below.
- If the interval between the two inputs is over 252.1 msec, output for the later input starts after a delay of 0 to 252.1 msec.
- The table below shows the change of driver output duty at OSC2 = 130 kHz.

Time after Priority Signal Input (OSC2 CLK)	Driver Output Duty Ratio
0 ~ 252.1 msec (4096 × 8 CLKS)	OFF
252.1 ~ 283.6 msec (4096 × 9 CLKS)	1/8
283.6 ~ 315.1 msec (4096 × 10 CLKS)	2/8
315.1 ~ 346.6 msec (4096 × 11 CLKS)	3/8
:	:
(MAX. 504.1 msec, 4096 × 16 CLKS)	Normal PWM Wave Form

4. Circuit PWM

The circuit PWM circuit controls the circuit SWR ON-time.

- To determine the circuit constant, externally attach resistors R1, R2, R3, R4, and R5 and capacitor C1.
- The PWM circuit detects the error between the circuit voltage *R1/(R1 + R2) and the reference voltage in the IC (Typ. 1.5 V), and amplifies the error voltage by multiplying by R5/R3. Then, based on the voltage integrated by the time constant of C1 x R4, PWM control is performed.
- The above voltage is compared with the CLOCK SWITCH output voltage. The CIR DRV output is set to ON while the above voltage is higher than the clock switch output voltage. The ON-timing for the output is synchronized with the clock switch output.
- The maximum duty (at maximum load) is determined by external C7 and R12.
  When C7 = 470 pF and R12 = 18 kΩ
  Maximum duty = 84% (at 176 kHz external clock)
  Maximum duty = 62% (at 130 kHz internal clock)
- The audio PWM circuit is activated when P CON ⑨ is set to "L".
- The C-MOS output is used as the driver of the audio PWM circuit.
- The mask option can be used to invert the output signals. This does not affect the drive performance.
- To soft-start the audio PWM circuit, use the start-up sequencer.
- During stand-by, the CIR DRV output ⑤ impedance becomes high.

5. V–F Converter

The V–F converter converts the voltage applied to the VF IN 1 pin into a frequency during operation of the circuit or charge SWR.

- The V–F converter becomes operable when the P CON ⑨ = "L" or CHG CON ⑪ = "H".
- The output "H" width is fixed to 4096 times the external or internal clock (OSC2) cycle.
- When P CON ⑨ = "H" and CHG CON ⑪ = "L" simultaneously, the VF OUT ② output impedance becomes high.

VF IN 1 Input Voltage	VF OUT 2 Output Frequency	2 Output Duty
3.3 ~ V	"H" ; Nch Output OFF	1
3.2 ~ 3.3 V	Clock frequency x 1/(4096 x 2)	1/2
3.1 ~ 3.2 V	Clock frequency x 1/(4096 x 3)	1/3
3.0 ~ 3.1 V	Clock frequency x 1/(4096 x 4)	1/4
2.9 ~ 3.0 V	Clock frequency x 1/(4096 x 5)	1/5
2.8 ~ 2.9 V	Clock frequency x 1/(4096 x 6)	1/6
2.7 ~ 2.8 V	Clock frequency x 1/(4096 x 7)	1/7
2.6 ~ 2.7 V	Clock frequency x 1/(4096 x 8)	1/8
2.5 ~ 2.6 V	Clock frequency x 1/(4096 x 9)	1/9
2.4 ~ 2.5 V	Clock frequency x 1/(4096 x 10)	1/10
2.3 ~ 2.4 V	Clock frequency x 1/(4096 x 11)	1/11
2.2 ~ 2.3 V	Clock frequency x 1/(4096 x 12)	1/12
2.1 ~ 2.2 V	Clock frequency x 1/(4096 x 13)	1/13
2.0 ~ 2.1 V	Clock frequency x 1/(4096 x 14)	1/14
2.9 ~ 2.0 V	Clock frequency x 1/(4096 x 15)	1/15
1.8 ~ 1.9 V	Clock frequency x 1/(4096 x 16)	1/16
1. ~ 1.8 V	"L" ; Nch Output ON	0

6. Temperature Sensor

The temperature sensor detects heating of the set using the Vf temperature characteristics of the external diode.

- A regulated current source from Vref in the IC (2 V) is built in (Typ. 100 μA).
- Approximate VF temperature characteristics of the external diode (sample DAN202U, If = 100 μA, measured values)

Ambient Temperature	VF
25°C	495 mV
50°C	432 mV
75°C	368 mV
100°C	302 mV
125°C	247 mV
150°C	171 mV

- With the target detection voltage value of 210 mA, high temperatures between 100 and 170°C (range of dispersion) are detected.
- When Vf becomes lower than the detection voltage, the ALM OUT pin output ⑩ is latched to "L".
- The temperature sensor is activated when the CHG CON is set to "H". Detection is enabled after completion of soft-start.

7. Charge Current Sensor

The charge current sensor detects abnormal charge currents flowing from the charging source to the rechargeable battery.

- Attach external resistor R8 (0.5Ω) between input pins ⑯ and ⑰.
- Completion of charging is detected when the voltage drop at R8 becomes 0.045 V or less (90 mA). Upon detection of 0.045 V or a lower voltage, the CHG DPY output ⑫ goes OFF.
- Output from CHG DPY ⑫ is possible even when PCON ⑨ is set to "L".
- Overcurrent during charging is detected when the voltage drop at R8 becomes 0.6 V or more (1.2 A). Upon detection of 0.6 V or a higher voltage, the ALM OUT output ⑩ is latched to "L".
- During soft-start, overcurrent is not detected.
- For the sensor to operate, the voltage at input pins ⑯ and ⑰ must be 0.5 V to VDD + 0.3 V.
- If pins ⑯ and ⑰ may have a higher potential than pin ㉑, an external resistor of 1 to 10 kΩ must be attached to input pins ⑯ and ⑰ to limit the board current flowing into the IC.

8. Charge PWM

The charge PWM circuit controls the charge SWR ON-time.

- To determine the circuit constant, externally attach resistors R6, R7, R8, R9, R10, and R11, capacitor C6, and diodes D2 and D3. The diode is used for adjusting the temperature characteristics of the charge power supply voltage.

- The PWM circuit detects the error between (charge power supply voltage – Vf·D2 – Vf·D3)×R6/(R6+R7) and the reference voltage in the IC (Typ. 1.5 V), and amplifies the error voltage by multiplaying by R11/R9. Then, based on the voltage integrated by the time constant of C6 × R10, PWM control is performed.
- The above voltage is compared with the CLOCK SWITCH output voltage. The CHG DRV output is set to ON while the above voltage is higher than the CLOCK SWITCH output voltage. The ON-timing for the output is synchronized with the clock switch output.
- The maximum duty (at maximum load) is 100%.
- The charge PWM circuit is activated when CHG CON ⑪ is set to "H". To soft-start the audio PWM circuit, use the start-up sequencer.
- When P CON ⑨ = "H" and CHG CON ⑪ = "H" simultaneously, RF5C133 enters charge mode and starts constant current charging (300 mA). During charging, the charge power supply voltage is varied to maintain the voltage drop at R8 at 0.15 V. When the charge power supply voltage exceeds the specified voltage, RF5C133 is automatically switched to constant voltage mode.
- When P CON ⑨ = "L" and CHG CON ⑪ = "H" simultaneously, RF5C133 enters constant voltage operation mode and feeds current to the circuit directly from the charge power supply. When the rechargeable battery and the AC adapter is used at the same time, current is fed to the circuit while the battery is charged.
- When CHG CON ⑪ = "L", the charge PWM circuit is disabled.

9. VDD (for CPU) PWM

The VDD PWM circuit controls the VDD DWR OFF-time.

- The VDD PWM circuit is activated by applying the minimum operating voltage or a higher voltage to the VDD IN ㉑ pin.
- After activation, the VDD PWM circuit fetches a self-rectified voltage at the VDD IN ㉑ pin and uses it as the power supply voltage.
- If the VDD voltage becomes lower than the detection voltage (fixed to Typ. 4.0 V by a built-in resistor), the VDD DRV ⑳ output goes ON.
- The output ON timing is synchronized with the OSC1 output.

10. Series Regulator (for CPU)

The series regulator steps down the VDD IN voltage and outputs a constant potential.

- The series regulator steps down the VDD IN ㉑ voltage and outputs a constant voltage through CPU VDD ㉒
- The output voltage is fixed by a built-in resistor. (Typ. 3.5 V)

11. Voltage Detector (for CPU)

The voltage detector detects drops in the CPU power supply voltage.

- When the CPU power supply voltage drops to the detection voltage or lower, the CPU RST output goes ON.
- The detection voltage is fixed by a built-in resistor. (Typ. 2.4 V)

■ ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDD	−0.3 ~ 6	V
Output Voltage 1. CMOS Output 2. Nch Open Drain Output	 VOUT1 VOUT2	 VSS−0.3 ~ VDD+0.3 VSS−0.3 ~ 12	 V V
Input Voltage CMOS Input	 VIN	 VSS−0.3 ~ VDD+0.3	 V
Coil Drive Output Current 1. Circuit (Circuit PWM Output) 2. Charge (CHG. PWM Output) 3. CPU (VDD. PWM Output)	 IOUT1 IOUT2 IOUT3	 MAX. 200 MAX. 200 MAX. 100	 mA mA mA
Power Consumption	Pd	MAX. 500	mW
Operating Ambient Temperature	Topr	−30 ~ 80	°C
Storage Temperature	Tstg	−40 ~ 125	°C
Soldering Temperature	Tsolder	260°C 10 sec	

■ RECOMMENDED OPERATING CONDITION of RF5C133 and EXTERNAL CIRCUIT

	Parameter		MIN.	TYP.	MAX.	Unit
Input Power	A/C Adapter Output Voltage			5		V
	Dry Battery Output Voltage			3		V
	Storage Battery Output Voltage			4		V
Output Power	0. Internal Power Supply Voltage (Self-Generated)			4		V
	1. Circuit 1	Power Supply Voltage		5.8		V
	(External Tr. necessary)	Power Supply Current		70		mA
	Circuit 2	Power Supply Voltage		3.5		V
	(External Tr. necessary)	Load Current		100		mA
	2. Charge	Power Supply Voltage		5		V
	(External Tr. necessary)	Load Current		300		mA
	3. CPU	Power Supply Voltage		3.5		V
		Load Current		10		mA

■ ELECTRICAL CHARACTERISTICS

V_{DD} = 4.0V, 0°C ≦ Ta ≦ 70°C, the TYP values are measured at 25°C.

1. INTERNAL OSCILLATOR (Associated Pin No. ⑲ ⑳ ㉑ ㉔, ④⑤⑥⑨㉑ ㉔)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
OSC1 Oscillation Start Voltage	V_{OSC1st}	V_{DD} Rise		0.65	1.8	V
OSC1 Oscillation Frequency	f_{OSC1}	Ta = 25°C	90	100	110	kHz
OSC1 Oscillation Duty	D_{OSC1}		60	65	70	%
OSC2 Oscillation Start Voltage	V_{OSC2nd}	V_{DD} Rise		1.35	1.8	V
OSC2 Oscillation Frequency	f_{OSC2}	C7 = 470pF, R12 = 18 kΩ	100	130	160	kHz

2. CLOCK SWITCH (Associated Pin No. ④⑤⑥⑨㉑ ㉔)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Esternal Clock Frequency	f_{CLK}		160	176	193	kHz

3. START UP SEQUENCER (Associated Pin No. ④⑤⑥⑨㉑ ㉔)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
SOFT START Valid Range	(Start)	t_{ST}	OSC2 = 130 kHz	242	252	262	ms
	(End)	t_{END}	OSC2 = 130 kHz	484	504	524	ms

4. CIRCUIT PWM (Associated Pin No. ④⑤⑥⑦⑧⑨㉑ ㉔)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Error Amp. Input Voltage Range	V_{INTER1}		0		V_{DD}	V
Error Amp. Input Reference Voltage	V_{REFER1}		1.4	1.5	1.6	V
Error Amp. Output Voltage	V_{OUTER1}		0		V_{DD}	V
PWM Driver Supply Voltage Range	V_{DRV1}		GND		V_{DD}	V
PWM Driver Nch ON Voltage	V_{OL1}	Iol = 50 mA		0.22	0.5	V
PWM Driver Pch ON Voltage	V_{OH1}	Ioh = −5 mA	V_{DD}-0.5	V_{DD}-0.25	V_{DD}	V

5. V–F CONVERTER (Associated Pin No. ①②③⑨㉑ ㉔)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Voltage Range	V_{INVF}		0		V_{DD}	V
Detect Voltage Set Range	V_{DVF}		1.8		3.3	V
Detect Voltage Set Step	V_{UNITVF}		0.09	0.1	0.11	V
Output Frequency Range	f_{VF}	CLK = OSC2/4096 (kHz)	CLK/16		CLK/2	kHz
Output ON Voltage	V_{DLVF}	Iol = 5 mA		0.3	0.5	V

6. TEMPERATURE SENSOR (Associated Pin No. ⑩ ⑪ ⑬ ㉑ ㉔)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input-Const. Current	ITMP	TEMP SENS ⑬ = 0V	50	100	200	μA
Input-"L" Detect Voltage	VDTMP		0.155	0.21	0.265	V
Detect Voltage Hysteresis Width	ΔVDTMP		10.5	21	42	mV

7. CHARGE CURRENT SENSOR (Associated Pin No. ⑨⑩ ⑪ ⑫ ⑬ ⑯ ⑰ ㉑ ㉔)

The current values are transformed into the voltage fall through the external resistance and shown as below.

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Charge Detect Current	VDCMIN		0.027	0.045	0.063	V
Charge Detect Current Hysteresis Width	ΔVDCMIN		3	6	12	mV
Over Current Detect	VDCMAX		0.5	0.6	0.7	V
Over Current Detect Hysteresis Width	ΔVDCMAX		30	60	120	mV
Input Voltage Range	VINCUR		0.5		VDD+0.3	V

8. CHARGE PWM (Associated Pin No. ⑪ ⑭ ⑮ ⑯ ⑰ ⑱ ⑲ ㉑ ㉔)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Error Amp. Input Voltage Range	VINER2		0		VDD	V
Error Amp. Input Reference Voltage	VREFER2		1.4	1.5	1.6	V
Reference Voltage for Const. Current	VREFCC	R8 = 0.5Ω	0.12	0.15	0.18	V
Error Amp. Output Voltage Range	VOUTER2		0		VDD	V
PWM Output Supply Voltage Range	VDRV2		0		10	V
PWM Output ON Voltage	VDL2	Iol = 50 mA		0.22	0.5	V
PWM Output Leakage Current	IOH2			0.01	10	μA

9. VDD (for CPU) PWM (Associated Pin No. ⑲ ⑳ ㉑ ㉔)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PWM Output Supply Voltage Range	VDRV3				10	V
Output Voltage	VOUTVDD		3.9	4.0	4.1	V
PWM Driver ON Voltage	VOL3	Iol = 50 mA		0.22	0.5	V
PWM Driver Leakage Current	VOH3			0.01	10	μA

10. SERIES REGURATOR (for CPU) (Associated Pin No. ㉑ ㉒ ㉔)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Voltage (㉒ Pin)	VCPUVDD		3.4	3.5	3.6	V
Input/Output Voltage Difference	VDIF	IRL = −10 mA		0.5		V
Load Stability	ΔVCPU	−30 mA ≦ IRL ≦ 0 mA		35	100	mV

11. VOLTAGE DETECTOR (for CPU) (Associated Pin No. ㉑ ㉒ ㉓ ㉔)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Voltage Range	VINRST		0		VDD	V
Input "L" Detect Voltage	VDRST		2.3	2.4	2.5	V
Detect Voltage Hysteresis Width	ΔVDRST		60	120	240	mV

12. INPUT SIGNAL

Pin including Input Pull-Up Resistance (Associated Pin No. ⑨ : 250 kΩ poly-Si resistance)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
"H" Input Voltage	VIM1		0.8VDD		VDD	V
"L" Input Voltage	VIL1		0		0.2VDD	V
"H" Input Current	IIH1	VDD = 4.0V, Vih = 4.0V		0.01	1	μA
"L" Input Current	IIL1	VDD = 4.0V, Vil = 0V	8	16	32	μA

Pin including Pull-Down Resistance (Associated Pin No. ③⑪: 250 kΩ poly-Si resistance)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
"H" Input Voltage	VIH2		0.8VDD		VDD	V
"L" Input Voltage	VIL2		0		0.2VDD	V
"H" Input Current	IIH2	VDD = 4.0V, Vih = 4.0V	8	16	32	μA
"L" Input Current	IIL2	VDD = 4.0V, Vil = 0V		0.01	1	μA

13. OUTPUT SIGNAL

Nch Open-Drain Output (to CPU) (Associated Pin No. ②⑩ ⑫ ㉓)

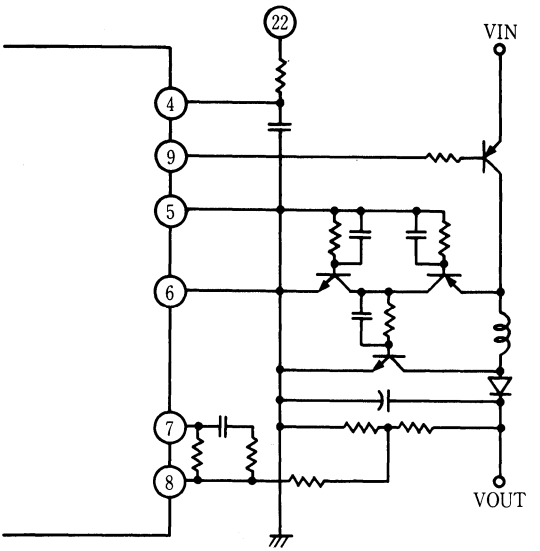
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output ON Voltage	VOL4	Iol = 5 mA		0.3	0.5	V
Output Supply Voltage	VDRV4	(MAX = VDD for ㉓ pin)	0		10	V
Output Leakage Current	IOH4			0.01	5	μA

14. IC TOTAL (Associated Pin No. ⑨⑪ ㉑ ㉔)

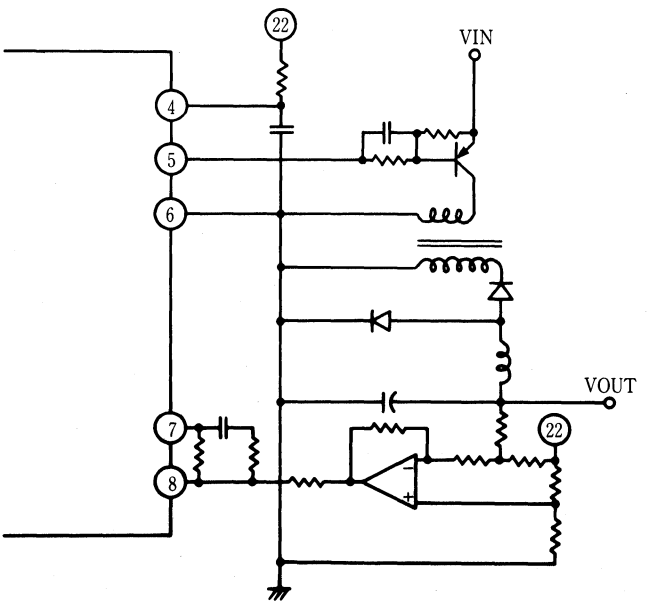
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Min. Operating Voltage	VINMIN			1.2	1.8	V
Max. Operating Voltage	VINMAX		6			V
Current Consumption * Ta = 50°C	IS	Vin = 2.0V, L = 120μH, C = 22μF PCON = H, CHGCON = L, No Load		25	* 60	μA
** Except for Output Driver SINK Current	IDD	Vin = 2.0V, L = 120μH, C = 22μF PCON = L, CHGCON = H, No Load		** 400	** 1000	μA

■ EXTERNAL CIRCUIT

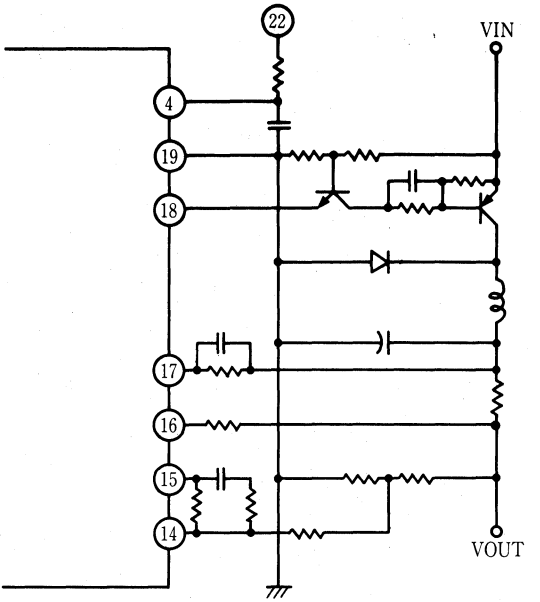
1. CIRCUIT STEP-UP DC/DC CONVERTER



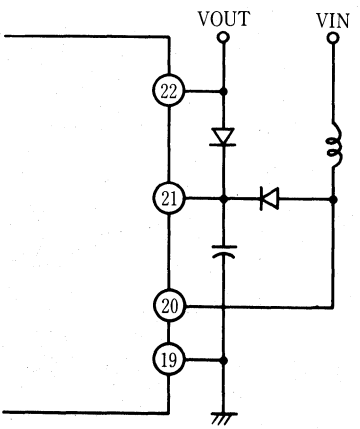
2. CIRCUIT POLARITY INVERSE DC/DC CONVERTER



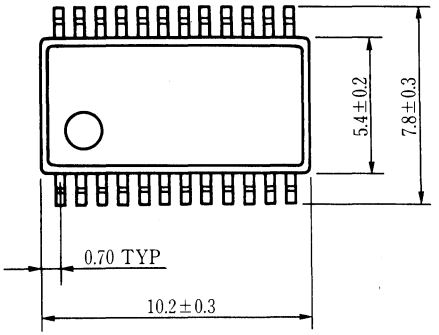
3. CHARGE-UP STEP-DOWN DC/DC CONVERTER

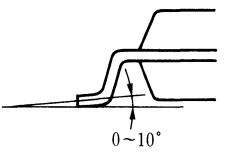


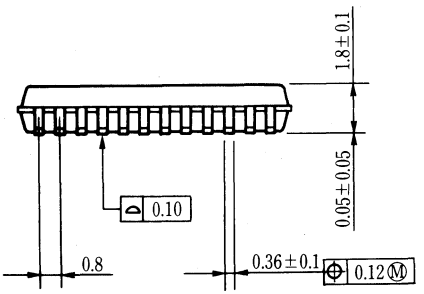
4. CPU STEP-UP/STEP-DOWN DC/DC CONVERTER

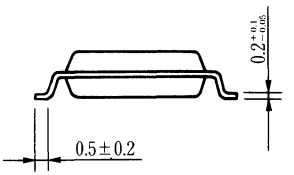


■ **PACKAGE DIMENSION** (Unit : mm)









Preliminary

RICOH

EK-074-9206

Multi - Power - Supply System
RS5VE0XX Series

The RS5VE0XX series are high precision, low current consumption multipower supply ICs. This chip series internally comprises 4 voltage regulators, 2 voltage (monitoring) detectors and a control switch manufactured with CMOS process technology. The device design allows the user to select the ideal power supply to match his system with a mask option providing features such as user setting of pin terminals and ON/OFF control of each circuit.

RICOH's unique trimming technology allows the output voltage and detection voltage to be set internally in the IC. The device package is the SOP 16 pin (0.8mm pitch) type.

■ FEATURES

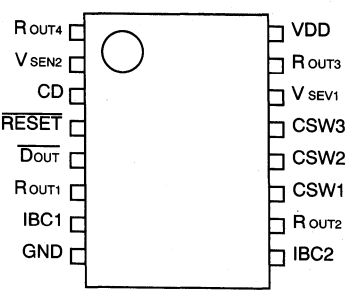
- Low power consumption
- Wide operating voltage range ..... 1.5 V~10.0 V
- High accuracy of Output voltage and Detect voltage ..... ±2.5%
- Voltage selection of output and Detect ..... 0.1 V step
- Low temperature coefficient of output and Detect ..... TYP.± 100 ppm / ℃
- Small input - output voltage difference ..... 50 mV for Iout=80 mA
- Small packege ..... SOP 16 (0.8 mm pitch)
- Possible direct connection to CPU due to the built - in level shift circuit

■ APPLICATIONS

- Constant - voltage power supply for handy communication equipment
- Constant - voltage power supply for battery - powered equipment

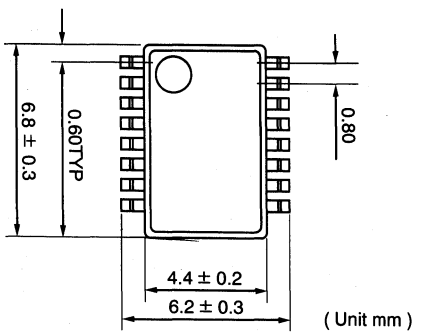
■ PIN CONFIGURATION

(RS5VE 001)



■ PACKAGE DIMENSION

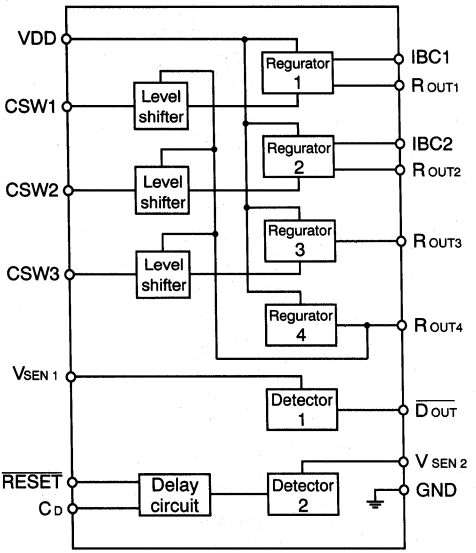
SOP 16 pin 0.8 mm pitch



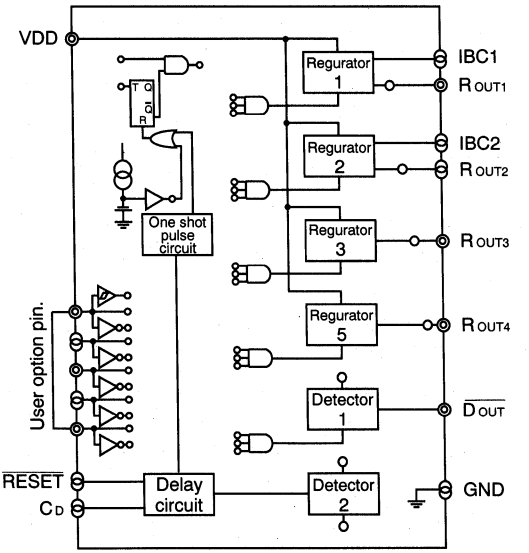
(Unit mm)

■ SYSTEM BLOK DIAGRAM

● RS5VE001X



● RS5VE0XXX (Mask option)



■ SELECTION GUIDE

In the RS5VE0XX series the user can specify standard type and a mask option type. Voltage settings for 6 circuits can each be separately selected. Use the rules in the selection guide below to match your appli-cation.

RS5VE0XXXX → Type number
a b c d

No.	Meaning
a	The RX5VE series (multipower supply) IC production serial number.
b	Mask option part production serial number · 01 is for standard parts · The mask option part number runs in sequence starting from 02.
c	Voltage setting serial number · The letters run in sequence from A to Z in order of production.
d	Used for taping selection · Runs in the E1 and E2 directions.(Refer to the taping Information).

■ PIN DESCRIPTION

1. RS5VE001X

Terminal No.	Terminal Code	Terminal Description
1	R_{OUT4}	Voltage regulator 4 output terminal.
2	V_{SEN2}	Voltage detector 2 output detecting terminal.
3	C_D	Voltage detector 2 terminal for connection to external capacitor for delay s ettings.
4	RESET	Voltage detector 2 output terminal.Nch open drain output. Detector "L" is output.
5	D_{OUT}	Voltage detector 1 output terminal.Nch open drain output. At detection "L" is output.
6	R_{OUT1}	Voltage regulator 1 output terminal.This terminal connects to the PNP transis- tor collector and also comprises an output voltage detection terminal.
7	IBC1	This terminal connects to the base of the PNP transistor externally connected to voltage regulator 1 for regulation of base current.
8	GND	Ground terminal.
9	IBC2	This terminal connects to the base of the PNP transistor externally connected to voltage regulator 2 for regulation of base current.
10	R_{OUT2}	Voltage regulator 2 output terminal.This terminal connects to the PNP tran- sistor collector and also comprises an output voltage detection terminal.
11	CSW1	Control switch input terminal for ON / OFF of voltage regulator 1. Active "H" input. Level shift achieved by means of R_{OUT4} output voltage.
12	CSW2	Control switch input terminal for ON / OFF of voltage regulator 2. Active "H" input. Level shift by means of R_{OUT4} output voltage.
13	CSW3	Control switch input terminal for ON / OFF of voltage regulator 3. Active "H" input. Level shift by means of R_{OUT4} output voltage.
14	V_{SEN1}	Voltage detector 1 Voltage detection input terminal.
15	R_{OUT3}	Voltage regulator 3 output terminal.
16	V_{DD}	V_{DD} terminal.

2. RS5VE0XXX (Mask Option)

Terminal No.	Terminal Code	Terminal Description
2	User designated symbol	The user can specify the 5 terminal numbers 2, 11, 12, 13, 14 as input termi- nals. See the mask option guide for a terminal description. Descriptions of other than these 5 terminals are the same as RS5VE001X (standard type).
11		
12		
13		
14		

■ MASK OPTION GUIDE

In the RS5VE0XX Series the user can specify the following items.

Item	Description
Viltage detector terminals 1 or 2	● The voltage detector 1 or 2 terminals can be connected to the voltage regulator output ROUT1,ROUT2,ROUT3, ROUT4 and VDD.
ON / OFF control for each circuit	● ON / OFF control of voltage regulators 1 through 4 and voltage detector 1 is done by using 3 AND input. ● Direct ON / OFF control of voltage detector 2.
ON / OFF control with toggle input (1 input only)	● ON / OFF control with AND toggle input and level input of main power supply. ● When the edge trigger flip flop (triggers on rising edge) triggers on power supply rise and voltage detector 2 activates, the circuit resets to initial value. ● Reset can be triggered at detection with a one - shot pulse or during the detection period.
User designated terminals	● Five input terminals can be designated as user terminals. ● ON / OFF control input terminals for each circuit. ● Voltage detector input I/O terminals 1 and 2. ● Designation of active "H" and active "L". ● Terminal No.11, can be used as a toggle input for the Schumitt trigger.
Output of voltage detectors 1 and 2	● The voltage detector 1 and 2 output, RESET or DOUT can be designated "L" or "H" during detection. ● The voltage detector 1 and 2 output, RESET or DOUT can be designated "L" or "H" during OFF by ON / OFF control. ● ON / OFF control of voltage regulators 1 through 4 with the output of voltage detectors 1 and 2.

● Functoins of user designated input terminals

User designated input terminals have the functions descrided in the table below.

User terminal	Pin No.	Input terminal functions
User terminal 1	2	Control switch for each circuit, voltage detecion terminals 1 or 2.
User terminal 2	11	Control switch for each circuit, Schmitt trigger input
User terminal 3	12	Only as control switch for each circuit
User terminal 4	13	Only as control switch for each circuit
User terminal 5	14	Control switch for each circuit, voltage detecion terminals 1 or 2.

■ CIRCUIT DESCRIPTION

1. Voltage Regulators 1 and 2
   - These are series regulators with an external PNP transistor for extracting a large output current from a small I/O difference voltage.
   - The output voltage can be set in 0.1V steps from 3 to 6 volts by means of trimming.
   - ON/OFF switching with the control terminal.
   - Use a low saturation type transistor with an hfe of 100 or more. Provide a minimum 10 μ F capacitor at the output.

2. Voltage Regulators 3 and 4
   - These are CMOS type series regulators of the same configuration as the RICOH three terminal RX5RA, RX5RE voltage regulator series.
   - The output voltage can be set in 0.1V steps from 2 to 6 volts by means of trimming.
   - ON/OFF switching with the control terminal

3. Voltage Detector 1
   - This has the same configuration as the RICOH RX5VA 3 terminal voltage detector.
   - The output sets to "L" when a VDD voltage drop is detected.Output is taken from an Nch open drain device.
   - The following settings can be made with the mask option.
     1. Selection for ON/OFF control
     2. Selection of an "L" or "H" level output can be made during detection.
     3. Selection of an "L" of "H" level output can be made during OFF .
     4. The voltage detection terminal can be bonnected to the voltage regulator outputs R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4} and V_{DD}.

4. Voltage Detector 2
   - The output sets to "L" when a V_{SEN} voltage drop is detected.Output is taken from an Nch open drain device.
   - Reset delay settings can be made. Delay time settings can be made with an external CD (capacitor).
   - The following settings can be made with the mask option.
     1. Selection for ON/OFF control
     2. Selection of an "L" or "H" level output can be made during detection.
     3. Selection of an "L" or "H" level output can be made during OFF.
     4. The voltage detection terminal can be connected to the voltage regulator outputs R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4} and V_{DD}.

- Delay time settings are determined by the following formula.

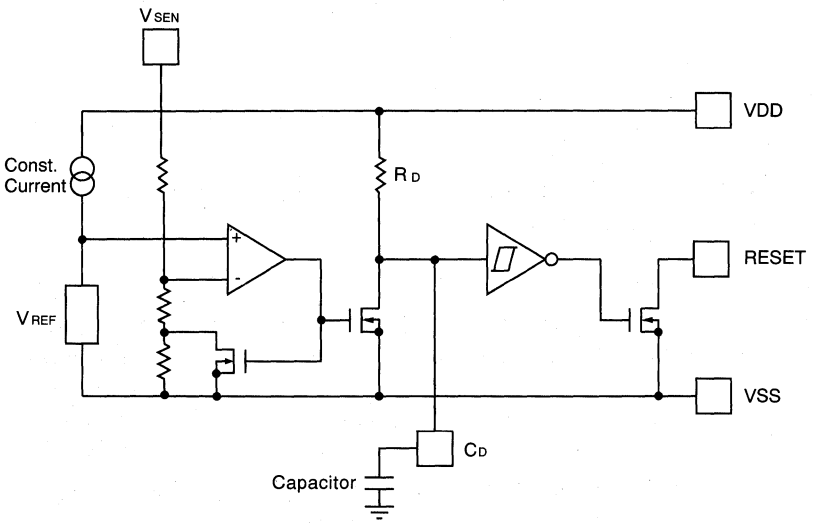
$$T_D = 0.69 \times R_D \times C_D$$

Rd is an internal resistor set at 1 MΩ which gives the following formula.

$$T_D = 0.69 \times 10^6 \times C_D$$

A block diagram of the RS5VE00XX delay generator circuit is shown on the next page.

- Delay generator circuit block diagram.



5. Main Power Supply Regulation (Mask Option)
   - Use of an internal edge trigger flip flop (triggers on rising edge) allows control of the main power supply POWER ON/OFF with AND (gate) toggle input and level input.
   - When voltage detector 2 senses a voltage drop, the flip flop is reset by means of the one-shot pulse generator circuit.(Reset can also be done during the voltage detection period).

■ ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Input Voltage	Vin	+ 12	V
Output Current	Iout	150	mA
Output Voltage	Vout	−0.3 ~ Vin + 0.3	V
Power Dissipation	Pd	500	mW
Operating Temperature	Topr	− 30 ~ + 80	℃
Storage Temperature	Tstg	− 40 ~ +125	℃
Soldering Temperature	Tsolder	260℃ 10sec,	

■ ELECTRONIC CHARACTERISTICS

● CHIP CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage range	VDD		1.5		10.0	V
Output Voltage select range1	$R_{OUT1,2}$	0.1 Vstep	3.0		6.0	V
Output Voltage select range2	$R_{OUT3,4}$	0.1 Vstep	2.0		6.0	V
Detect Voltage select range	VDET	0.1 Vstep	2.0		6.0	V

● Voltage Regurator 1, 2

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Output Voltage	$R_{OUT1,2}$		(R_{OUT}) × 0.975		(R_{OUT}) × 1.025	V
Suppry Current for No Load	$Istb_{1,2}$	Iout = 0mA			100	μA
Invalid Current	$Iopr_{1,2}$	Iout =80mA			1	mA
Input Output Voltage Difference	$Vdif_{1,2}$	Rout 1,2= 5.0V, Iout = 80mA		0.05	0.3	V
Load Reguration	△Vout	Rout 1,2 = 5.0V 1mA ≦ Iout ≦ 80mA			50	mV
Line Reguration	$\frac{\triangle Vout}{\triangle Vin - Vout}$	Rout 1,2+ 0.3V≦V_{DD} ≦10V		0.05	0.3	% / V
Ripple rate		f =120Hz, Ripple 0.5Vrms	40	60		dB
Limit Current	Ilim	$I_{B1,2}$ (PNP transistor Base Current)	1		5	mA
Temperature Coefficient	△Vout / △ Topr			±100		ppm / ℃

Note1 : Common condition V_{DD}=6.0 V, Iout=50 mA, Co=10μF, Ta=25℃

Note2 : External transistor hfe≧100

● Voltage Regurator 3

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Output Voltage	$Rout_3$		(Rout) × 0.975		(Rout) × 1.025	V
Supply Current	Iss3			5.0	10.0	μA
Input Output Voltage Difference	Vdif3	Rout 3 = 5.0 V, Iout = 50mA			0.3	V
Load Reguration	△Vout	Rout 3 = 5.0 V 1mA ≦ Iout ≦ 50 mA			50	mV
Line Reguration	$\frac{\triangle Vout}{\triangle Vin - Vout}$	Rout 3 + 0.5 V ≦ V_{DD} ≦ 10 V		0.05	0.3	% / V
Limit Current	Ilim3		100		300	mA
Temperature Coefficient	△out / △Topr			±100		ppm / ℃

Note : Common condition V_{DD} = 6.0 V, Iout = 30 mA, Ta = 25℃

● Voltage Regurator 4

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Output Voltage	$Rout_4$		(Rout) × 0.975		(Rout) × 1.025	V
Supply Current	Iss4			1.3	3.9	μA
Input Output Voltage Difference	Vdif4	Rout 4 = 5.0 V, Iout = 50 mA			0.3	V
Load Reguration	△Vout	Rout4 = 5.0V 1mA ≦ Iout ≦ 50mA			50	mV
Line Reguration	$\frac{\triangle Vout}{\triangle Vin - Vout}$	Rout3 + 0.5V ≦ V_{DD} ≦ 10V		0.05	0.3	% / V
Limit Current	Ilim4		100		300	mA
Temperature Coefficient	△out / △Topr			±100		ppm / ℃

Note : Common condition V_{DD} = 6.0 V, Iout = 10 mA, Ta = 25℃

● Voltage Detector 1, 2

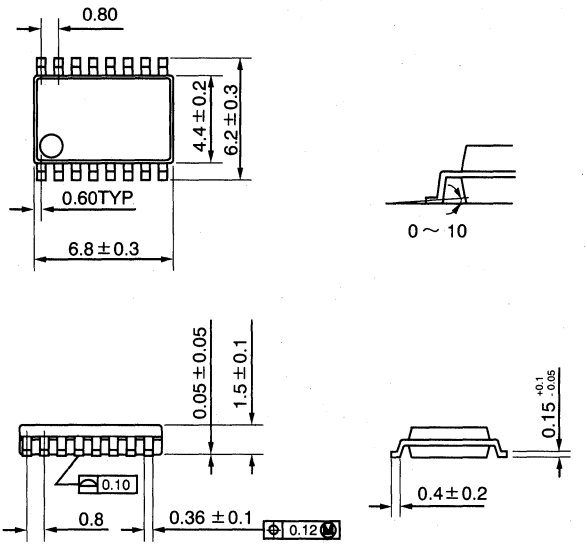
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Detect Voltage	$-V_{DET1.2}$		$(-V_{DET})$ × 0.975		$(-V_{DET})$ × 1.025	V
Hysteresis	V_{HYS}			$(-V_{DET})$ × 0.05		V
Supply Current	Iss5	Voltage Detector 1		1.3	3.9	μA
	Iss6	Voltage Detector 2		1.5	4.5	μA
Output Current	I_{OUT}	V_{DS} = 0.5V, V_{DD} = 1.0V		0.5		mA
		V_{DS} = 0.5V, V_{DD} = 2.4V		3.6		
		V_{DS} = 0.5V, V_{DD} = 3.6V		6.5		
		V_{DS} = 0.5V, V_{DD} = 4.6V		8.6		
		V_{DS} = 0.5V, V_{DD} = 6.0V		11.6		
Delay Circuit Resistance	Rd	Voltage Detector 2	0.5	1.0	2.0	MΩ
Detect Pin Current	I_{SEN}			0.5	2	μA
Temperature Coefficient	$\triangle V_{out}/\triangle T_{opr}$	Iout = 10 mA		±100		ppm / ℃

Note : Common condition V_{DD}=6.0 V, Ta=25℃

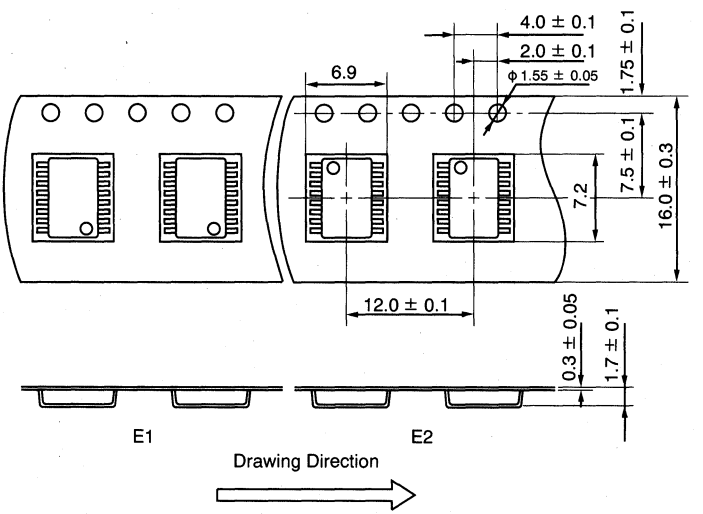
● Input

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Leackage Current	ILI		− 1		1	μA
Control switch "L" level Input Current	V_{IL}	CSW 1 ~ 4	See Reference			V
Control switch "H" level Input Voltage	V_{IH}	CSW 1 ~ 4				
Schumitt trigger "L" level Input Voltage	V_{SIL}	Option				
Schumitt trigger "H" level Input Voltage	V_{SIH}	Option				
Schumitt trigger Hysteresis Voitage	V_{HYS}	Option				

■ PACKAGE DIMENSION (Unit : mm)



■ TAPING INFORMATION (Unit : mm)



8. APPLICATION MANUAL

Real Time Clock RP5C01/5C15

Application Manual

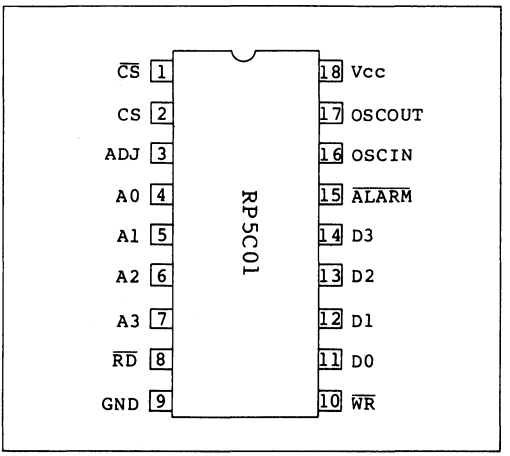
RP5C01/RP5C15 Application Manual

Contents

(1) Specifications of RP5C01

Outline:

The RP5C01 is a real-time clock that can be connected directly to the bus of microprocessors using the 8085A, Z80, 6809, 6502 or other CPU. Time can then be written to or read from the clock in the same way as writing to or reading from RAM. As well as calendar and time counters and alarm function, the RP5C01 has a 26 x 4-bit RAM, allowing battery backup. It can therefore be used as a non-volatile RAM.

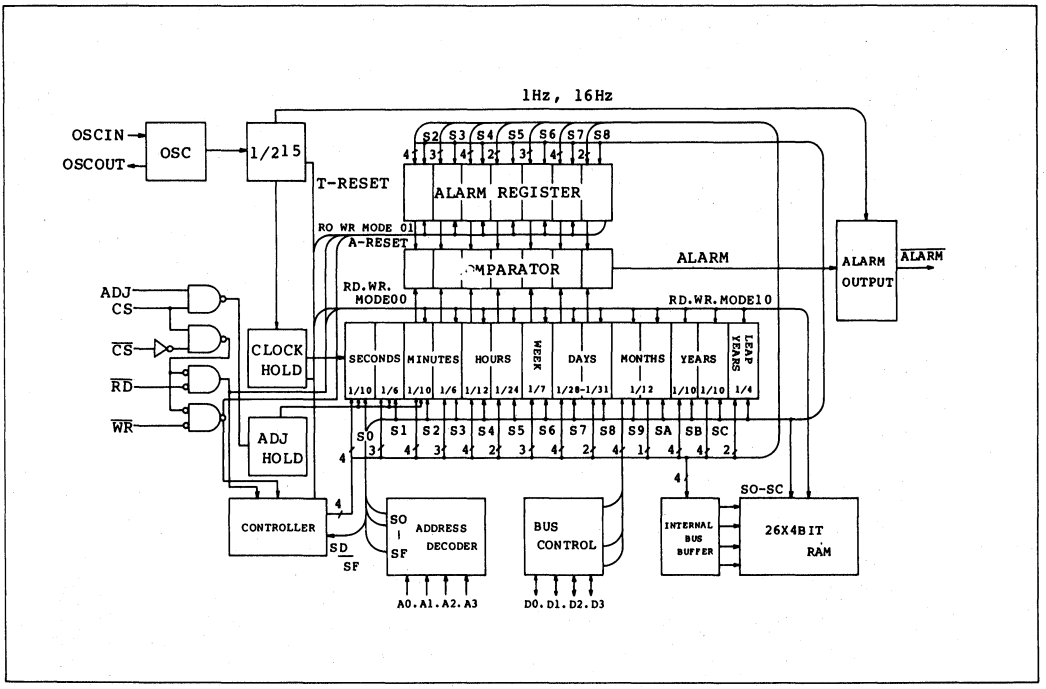


Features:

* Direct connection to CPU
* 4-bit bidirectional bus D0-D3
* 4-bit address inputs A0-A3
* Internal counters for time (hours, min., sec.) and date (100 years, leap years, months, days, and days-of-the-week)
* Choice of 24-hour or 12-hour (AM/PM) system
* All clock data expressed in BCD code
* $\pm$30 sec. adjustment function
* Provision for battery backup
* Internal 26 x 4-bit RAM
* Alarm signal, 16 Hz clock signal or 1 Hz clock signal output

Terminal connection diagram

Block diagram



Absolute max. ratings

Symbol	Item	Conditions	Values	Units
Vcc	Supply voltage		-0.3 ~ +7	V
V_I	Input voltage	Voltage at any pin with respect to GND	-0.3~Vcc+0.3	V
V_O	Output voltage		-0.3~Vcc+0.3	V
Pd	Max. power consumption	Ta=25°C	700	mW
Topg	Under bias		0 ~ 70	°C
Tstg	Storage temperature		-40 ~ 125	°C

Recommended operating conditions (Ta=0 - 70°C unless otherwise specified)

Symbol	Item	Values			Units
		Min	TYP	Max.	
Vcc	Supply voltage	4.75	5	5.25	V
V_{DH}	Data preservation voltage	2.2		5.25	V
f_{XT}	Oscillation frequency of crystal oscillator		32.768		kHz

DC electrical characteristics

Ta=0 - 70°C, Vcc=5V ±10% unless otherwise specified.

Symbol	Item	Measurement conditions	Values			
			Min.	TYP	Max.	Units
V_{IH}	"H" input voltage		2.0		Vcc	V
V_{IL}	"L" input voltage		-0.3		0.8	V
V_{OH}	"H" output voltage	I_{OH}=-400μA	2.4			V
V_{OL}	"L" output voltage	I_{OL}=2mA			0.4	V
I_I	Input current	V_I=0 ~ 5.5V			±10	μA
I_{OZ}	Output leakage current				±10	μA
I_{CC1}	Vcc power supply current	f_{XT}=32.768kHz Vcc=2.2V			15	μA
I_{CC2}	Vcc power supply current	f_{XT}=32.786kHz Vcc=5.0V (Note 2)			250	μA

Note 1: current towards IC is considered positive (no sign)

Note 2: When connected to CPU (read/write cycle 10μs)

AC electrical characteristics

(Ta=0 ~ 70°C, Vcc=5V ±5% unless otherwise specified)

Symbol		Measurement conditions	Values			Units
			Min.	TYP	Max.	
t_{AC}	Address $\overline{RD}/\overline{WR}$ delay time		170			ns
t_{CC}	$\overline{RD}/\overline{WR}$ pulse width		400		10000	ns
tCA	Address valid time after $\overline{RD}/\overline{WR}$ leading edge		10			ns
t_{RD}	Data delay time after $\overline{RD}$ trailing edge				400	ns
t_{RDH}	Data hold time after $\overline{RD}$ leading edge		0			ns
t_{WDL}	Data delay time after $\overline{WR}$ trailing edge				40	ns
tWD	Data hold time after $\overline{WR}$ leading edge		20			ns

AC electrical characteristics are as follows when Vcc=5V ±10%.

Symbol		Measurement conditions	Values			Units
			Min.	TYP	Max.	
t_{AC}	Address $\overline{RD}/\overline{WR}$ delay time		170			ns
t_{CC}	$\overline{RD}/\overline{WR}$ pulse width		450		10000	ns
tCA	Address valid time after $\overline{RD}/\overline{WR}$ leading edge		10			ns
t_{RD}	Data delay time after $\overline{RD}$ trailing edge				400	ns
t_{RDH}	Data hold time after $\overline{RD}$ leading edge		0			ns
t_{WDL}	Data delay time after $\overline{WR}$ trailing edge				40	ns
tWD	Data hold time after $\overline{WR}$ leading edge		20			ns

*Refer to the timing chart of page 51 to check the symbols.

Function of pins

Name of pin	No. of pin	Function
$\overline{CS}$. CS	1,2	External interface terminals, valid when CS = H and $\overline{CS}$ = L. CS is connected to the power-down detector of the peripheral circuitry and $\overline{CS}$ to a CPU address decoder.
ADJ	3	For easy adjustment of the second counter without connection to a CPU. If ADJ is set to high when the second counter registers 0 ~ 29, the seconds are set to 0, and if ADJ is set to high when the second counter registers 30 ~ 59, the seconds are set to 0 and the minutes are incremented. This terminal is designed not for edge detection but for level detection. A minimum of 100 μsec. is required for high-level adjustments.
A_0 ~ A_3	4,5,6,7	Address terminals. Connected to address bus of CPU.
$\overline{RD}$	8	I/O control terminal. Low when RP5C01 is read by CPU.
GND	9	0V
$\overline{WR}$	10	I/O control terminal. Low when RP5C01 is written by CPU.
D_0 ~ D_3	11,12,13,14	Bidirectional data bus. Connected to data bus of CPU.
$\overline{ALARM}$	15	For output of alarm signal or 16Hz/1Hz clock signals. Open-drain output.
OSCIN, OSCOUT	16 17	For connection to 32.768kHz crystal oscillator circuit.
Vcc	18	+5V power supply terminal

Address allocation of MODE 00 (Note 1)

MODE	MODE 00				
A_3 ~ A_1	Contents	D_3	D_2	D_1	D_0
0	1-sec counter				
1	10-sec counter	x			
2	1-min counter				
3	10-min counter	x			
4	1-hour counter				
5	10-hour counter(Note 2)	x	x		
6	Day-of-the-week counter	x			
7	1-day counter				
8	10-day counter	x	x		
9	1-month counter				
A	10-month counter	x	x	x	
B	1-year counter				
C	10-year counter				
D	MODE Register	Timer EN	Alarm EN	MODE selector	
				M1	M0
E	Test Register	Test 3	Test 2	Test 1	Test 0
F	RESET Controller	$\overline{1Hz}$ ON	$\overline{16Hz}$ ON	Timer RESET	Alarm RESET

X indicates that the counter may take any value during write operations, but always be 0 when read out.

(Note 1) MODE 00 is set by writing data (X,X,0,0) to address D.
(Note 2) Bit 1 of the 10-hour counter should be as follows when the 12-hour system is selected:
D1 = 1 (PM)
D1 = 0 (AM)

Address allocation of MODE 01 (Note 1)

MODE		MODE 01			
A3~A1	Contents	D_3	D_2	D_1	D_0
0		x	x	x	x
1		x	x	x	x
2	Alarm 1-min register				
3	Alarm 10-min register	x			
4	Alarm 1-hour register				
5	Alarm 10-hour register	x	x		
6	Alarm day-of-the-week register	x			
7	Alarm 1-day register				
8	Alarm 10-day register	x	x		
9		x	x	x	x
A	$\overline{12\text{-hour}}$/24-hour selector	x	x	x	
B	Leap-year counter	x	x		
C		x	x	x	x
D	Mode Register	Timer EN	Alarm EN	MODE selector M1	MODE selector M0
E	Test Register	Test 3	Test 2	Test 1	Test 0
F	Reset Controller	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET

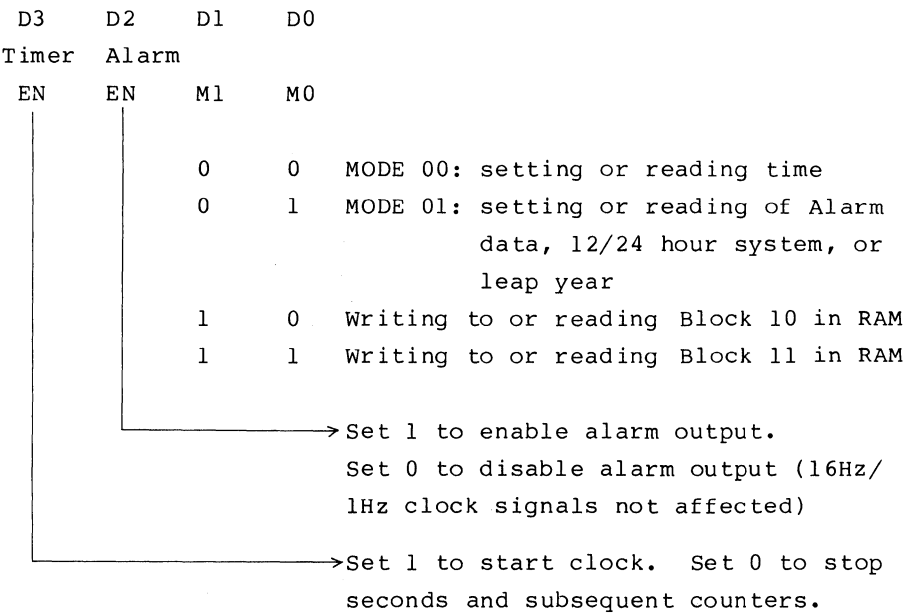
(Note 1) MODE 01 is set by writing data (X,X,0,1) to address D.

Address allocation of MODE 10 and 11 (Note 1)

MODE	MODE 10 (RAM)				MODE 11 (RAM)			
A3~A1	Contents				Contents			
0								
1								
2	block 10				block 11			
3								
4								
5	4 bit				4 bit			
6	x				x			
7	13				13			
8								
9	RAM				RAM			
A								
B								
C								
D	Timer EN	Alarm EN	MODE selector		Timer EN	Alarm EN	MODE selector	
			M1	M0			M1	M0
E	Test 3	Test 2	Test 1	Test 0	Test 3	Test 2	Test 1	Test 0
F	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET

(Note 1) MODE 10 is set to by writing data (X,X,1,0) to address D.
MODE 11 is set by writing data (X,X,1,1) to address D. (MODE 10 and 11 are in RAM areas)

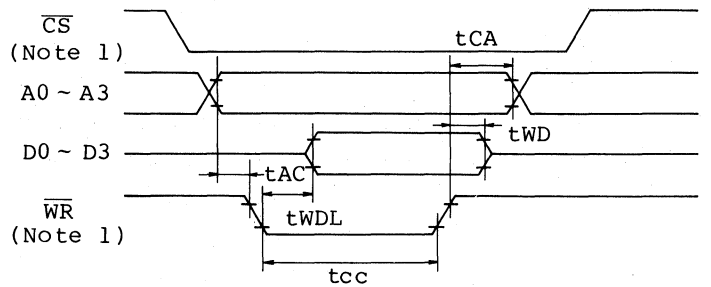
* Mode register (A3,A2,A1,A0) = (1,1,0,1) = D



* The leap-year counter registers a leap year when D1 = D0 = 0. It simultaneously counts with the year counter.
* The $\overline{12\text{-hour}}$/24-hour selector sets the 12-hour system when D0 = 0 and the 24-hour system when D0=1. PM or AM is selected when D1 in the 10-hour counter is 1 or 0, respectively (see page 47).
* Reset controller 16Hz/1Hz clock register.
  (A3,A2,A1,A0) = (1,1,1,1) = F
  D0 = 1: resets all alarm registers and internal Alarm F/Fs.
  D1 = 1: resets the 15-stage dividers before the seconds register.
  D2 = 0: switches on the 16Hz clock pulse generated from the $\overline{\text{ALARM}}$ terminal.
  D3 = 0: switches on the 1Hz clock pulse generated from the $\overline{\text{ALARM}}$ terminal.
* Addresses 0 ~ D: able to read and write.
* Addresses E ~ F: only able to write and 0H always appears when read out.

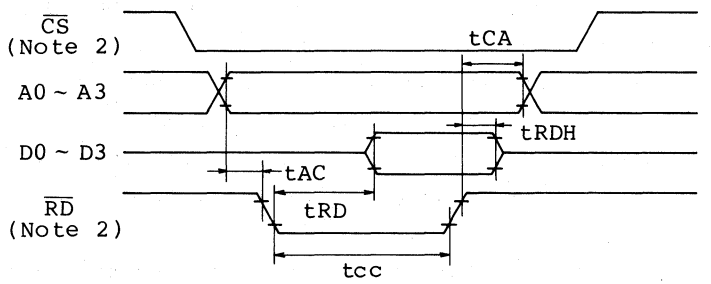
Timing chart

WRITE CYCLE (CS = "H")



(Note 1) The RP5C01 accepts a $\overline{WR}$ signal when both $\overline{CS}$ = low and CS = high. The timing of $\overline{CS}$ is not specified, but because of the construction of the RP5C01, the $\overline{WR}$ signal in the above diagram should be taken as the CS·$\overline{CS}$·$\overline{WR}$ signal. (For details, see the block diagram of the RP5C01 or Section 4 of these Application Notes.)

READ CYCLE (CS = "H")



(Note 2) The RP5C01 accepts an $\overline{RD}$ signal when both $\overline{CS}$ = low and CS = high, in the same way as for a $\overline{WR}$ signal. The $\overline{RD}$ signal in the above diagram should therefore be taken as the CS·$\overline{CS}$·$\overline{RD}$ signal in the same way as the $\overline{WR}$ signal. (For details, see the block diagram of the RP5C01 or Section 4 of these Application Notes.)

Application Notes

(1) Oscillator circuit

(1-1) When constructing the oscillator circuit using a crystal oscillator.

The oscillator circuit should be constructed as shown in Fig. 1. External components needed are a resistor, a condenser, and a trimmer condenser for fine adjustment of the frequency. The oscillation frequency should be adjusted by altering the value of the trimmer condenser using the standard 16Hz or 1Hz clock signal output from the $\overline{\text{ALARM}}$ terminal.

When adjusting with the 16Hz signal:

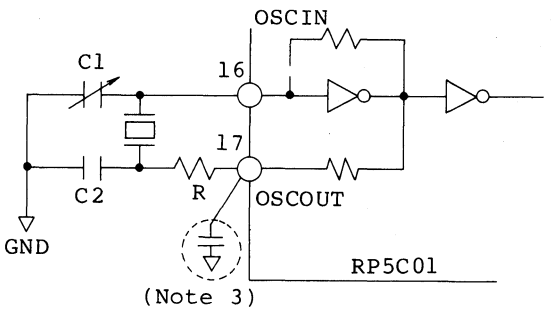
Address: (A3,A2,A1,A0) = (1,1,1,1)

Data: (1,0,0,0)

When adjusting with the 1Hz signal:

Address: (A3,A2,A1,A0) = (1,1,1,1)

Data: (0,1,0,0)



C1 = 10PF ~ 30PFr
C2 = 30PFr (Note 3)
R = 100kΩ
Crystal oscillator: Nihon Denpa Kogyo MX38T

Fig. 1

(Note 3) Different values of C1, C2, and R may be used, and the crystal oscillator is not definitely specified. The values of C1, C2, and R noted above are the best values for the MX38T oscillator used in the measurements carried out by Ricoh. A bypass condenser set between pin 17 and GND is sometimes effective for external noise. Its value should be less than 60 PFr according to the measurements. For details, see Section 1 of these Application Notes.

(1-2) When using an external clock

When an external clock is used, the arrangement shown in Figs. 2-(a) and 2-(b) below should be adopted. The OSCIN terminal is not TTL-compatible but CMOS-compatible.

1) With CMOS inverter

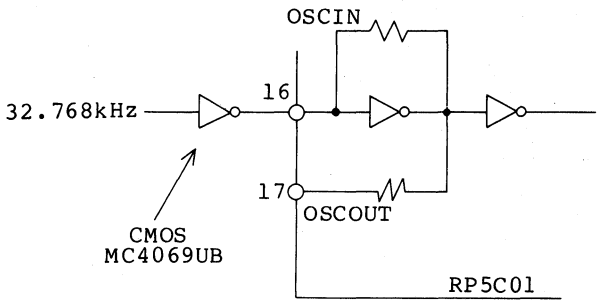


Fig. 2-(a)

2) With TTL inverter

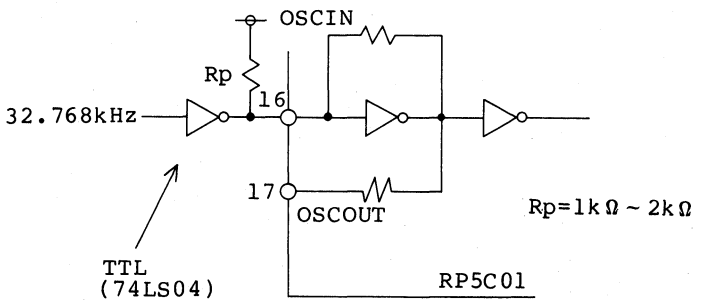


Fig. 2-(b)

(2) Input/output terminals and chip selection terminals

(2-1) Input/output terminals

Pull-up (4.7-47kΩ) or pull-down (100-300kΩ) resistors should be installed to fix the potentials of the I/O terminals during battery backup. (See Note 4 on page 16.)

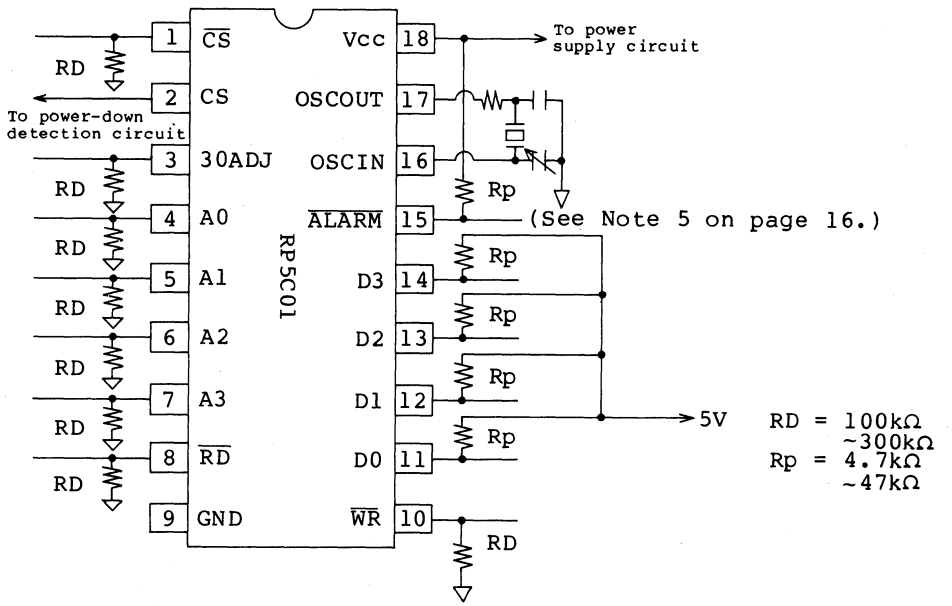


Fig. 3

(2-2) Chip select terminals

Two chip select terminals are provided. The CS terminal should be connected to the power-down detection circuit and the $\overline{CS}$ terminal to the CPU. CS is active when high and $\overline{CS}$ is active when low.

(Note 4)

The values of the pull-up and pull-down resistors need not necessarily be those given above (4.7 ~ 47kΩ and 100 ~ 300kΩ, respectively), but they should be chosen so that the RP5C01's DC characteristics VIH, VIL, VOH and VOL are satisfied. These resistors are used to maintain the level of the I/O terminals (D0 ~ D3) and the input terminals at any time (e.g., during battery backup), and they have the effect of reducing the current consumption during battery backup. It is immaterial whether pull-up or pull-down resistors are selected for any of the I/O or input terminals. However, it is recommended that pull-up resistors be used for $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$, since if pull-down resistors are used for these terminals, they will become active when the CPU is on hold (e.g., at DMA cycle, control lines of $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ start to float instantaneously) and this may lead to problems. The arrangement of resistors shown in Fig. 3 is an example only, and may be altered. For details, see Section 3 of these Application Notes.

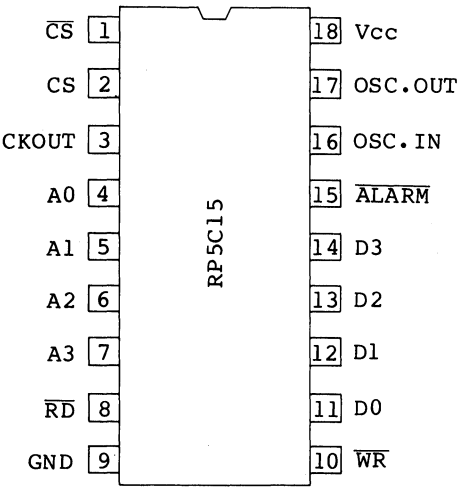
(Note 5)

If terminal 15 (the $\overline{ALARM}$ terminal) is to be used during battery backup, it should be pulled up by the same battery power source as the RP5C01. If it is not to be used during battery backup, it should be pulled up by the system power source, which cannot supply voltage during power down.

(2) Specifications of RP5C15

Outline:

The RP5C15 is a real-time clock that can be connected directly to the bus of microprocessors using not only the 8-bit CPU such as 8085, Z80, 6809, 6502 but also the 16-bit CPU such as 8086, Z8000, 68000 or others. Time can then be written to or read from the clock in the same way as writing to or reading from RAM. As well as calendar and time counters and alarm function allowing battery backup.

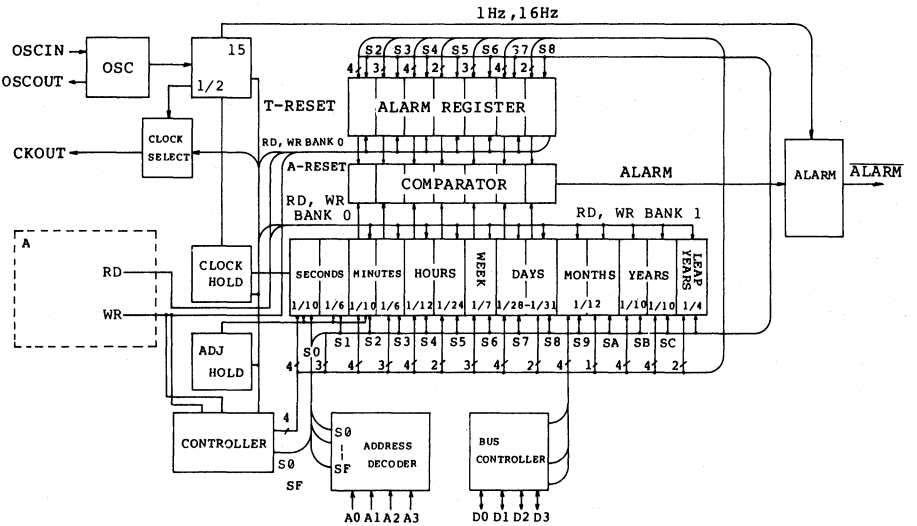


Pin configuration

Featrues:

* Direct connection to CPU and Hi-speed access
* 4-bit bidirectional bus D0~D3
* 4-bit address inputs A0~A3
* Internal counters for time (hours, min., sec.) and date (100 years, leap years, months, days, and days-of-the-week)
* All clock data expressed in BCD code
* ±30 sec. adjustment function
* Provision for battery backup
* Choice of standard clock from 16 kHz, 1.024 kHz, 128 kHz, 16 Hz, 1 Hz, 1/60 Hz
* Alarm signal, 16 Hz clock signal or 1 Hz clock signal output

Block diagram



Absolute maximum ratings (See Note 1)

Symbol	Item	Measurement conditions	Values	Units
VCC	Supply voltage	GND = 0	-0.3 ~ +7	V
VI	Input voltage	GND = 0	-0.3 ~ VCC+0.3	V
VC	Output voltage	GND = 0	-0.3 ~ VCC+0.3	V
PD	Maximum power dissipation	Ta = 25°C	600	mW
TOPG	Ambient temp. during operation		-20 ~ 70	°C
TSTG	Ambient temp. during storage		-40 ~ 125	°C

(Note 1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended operating conditions

Ta = -20°C to 70°C unless otherwise specified.

Symbol	Item	Values			Units
		Min.	Typ.	Max.	
VCC	Supply voltage	4.5	5.0	5.5	V
VDH	Data backup voltage	2.0		5.5	V
fxt	Oscillation frequency of crystal oscillator		32.768		kHz

DC characteristics during normal operation

Ta = -20°C to 70°C, Vcc = 5V ±10% unless otherwise specified.

Symbol	Item	Measurement conditions	Values			Units	Remarks
			Min.	Typ.	Max.		
VIH	"H" input voltage		2.0		Vcc+0.3	V	
VIL	"L" input voltage		-0.3		0.8	V	
VOH	"H" output voltage	IOH=-400μA	2.4			V	Except for pin 3,15
VOL	"L" output voltage	IOL=2mA			0.4	V	
IILK	Input leakage current	VIN=0 ~ VCC	-10		10	μA	
IFLK	Floating leakage current	VFV=0 ~ VCC	-10		10	μA	
IDDI	Current consumed during operation	(Note 2)			300	μA	

(Note 2) Vcc = 5V; R/W signal f =100kHz; Input terminals, Vcc or GND; Output terminals on no-load; Crystal oscillator (32.768kHz); Measurement temp. (25°C).

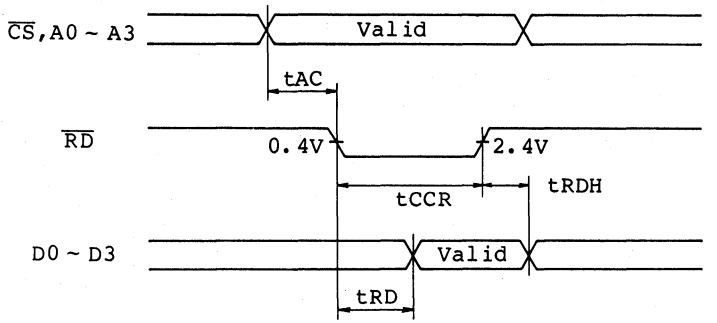
AC electrical characteristics

Ta=-20°C to 70°C, Vcc=5V±10% unless otherwise specified.

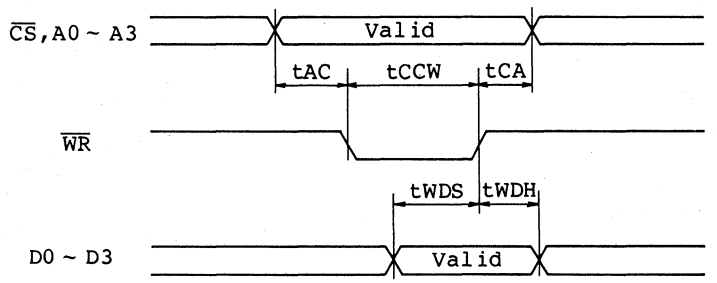
Symbol	Item	Measurement conditions	Values			Units	Remarks
			Min.	Typ.	Max.		
tAC	Address valid -- $\overline{RD}/\overline{WR}$ trailing edge		50			ns	$\overline{CS}$=low and address valid
tccR	$\overline{RD}$ pulse width		120		13000	ns	
tccW	$\overline{WR}$ pulse width		120		13000	ns	
tRD	$\overline{RD}$ trailing edge --data valid	(Note 1)			120	ns	
tcA	$\overline{RD}/\overline{WR}$ leading edge --address hold		10			ns	
tWDS	Write data setup time		100			ns	
tWDH	Write data hold time		20			ns	
tRDH	$\overline{RD}$ leading edge --data valid		10			ns	
tEN-DIS	Timer Enable-- Timer Disable		100			μs	
tADJ	Adjustment completion time				100	μs	
tAINH	Alarm data write inhibit time after alarm reset		100			μs	
tRCV	$\overline{RD}/\overline{WR}$ recovery time		1			μs	

Timing chart

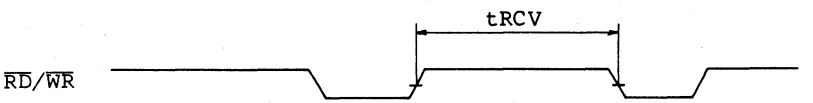
READ cycle (CS = "H")



WRITE cycle (CS = "H")



Others



Function of pins

Name of pin	No. of pin	Function
$\overline{CS}$ CS	1 2	External interface terminals. Valid when both CS = H and $\overline{CS}$ = L. CS is connected to the power-down detector of the peripheral circuitry, and $\overline{CS}$ to the address decoder of the CPU.
CKOUT	3	Output terminal for standard clock signal. Can take 8 different states depending on contents of CKOUT selection register. N-ch open drain output.
A0 ~ A3	4,5,6,7	Address input. Connected to address bus of CPU.
$\overline{RD}$	8	I/O control input. Set to low when data of RP5C15 is read. Low active input.
GND	9	OV
$\overline{WR}$	10	I/O control input. Set to low when data of RP5C15 is written. Low active input.
D0 ~ D3	11,12,13,14	Bidirectional bus. Connected directly to CPU data bus.
$\overline{ALARM}$	15	Output terminal for alarm signal and 1Hz/16Hz clock signals. N-ch open-drain output.
OSC IN	16	Connected to 32.768kHz crystal oscillator circuit.
OSC OUT	17	Connected to 32.768kHz crystal oscillator circuit.
VCC	18	+5V power supply

Address allocation

* "x" means "Don't care" when written, and always "0" when read out.
* Address 0～D: able to read to and write from, except for ADJUST register which can only be written to.
  Address E～F: "write" only (always "0" when read out)

Bank 0						Bank 1				
A3~A0	Contents	D3	D2	D1	D0	Contents	D3	D2	D1	D0
0	1-sec. counter					CKOUT selection register	X	CK2	CK1	CK0
1	10-sec. counter	X				Adjust register	X	X	X	Adjust
2	1-min. counter					Alarm 1-min. register				
3	10-min. counter	X				Alarm 10-min. register	X			
4	1-hour counter					Alarm 1-hour register				
5	10-hour counter	X	X			Alarm 10-hour register	X	X		
6	Day-of-the-week counter	X				Alarm day-of-the-week register	X			
7	1-day counter					Alarm 1-day register				
8	10-day counter	X	X			Alarm 10-day register	X	X		
9	1-month counter						X	X	X	X
A	10-month counter	X	X	X		$\overline{12}$/24 hour selector	X	X	X	
B	1-year counter					Leap-year counter	X	X		
C	10-year counter						X	X	X	X
D	Mode register	Timer EN	Alarm EN	X	Bank 1/0	Mode register	Timer EN	Alarm EN	X	Bank 1/0
E	Test register	Test 3	Test 2	Test 1	Test 0	Test register	Test 3	Test 2	Test 1	Test 0
F	Reset controller	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET	Reset controller	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET

CKOUT selection register

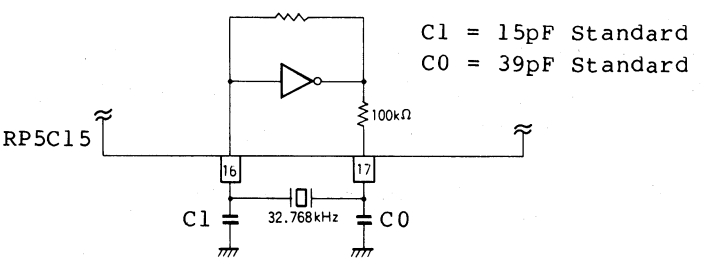
D3	D2	D1	D0	CKOUT	Remarks
X	0	0	0	"Z"	High-impedance
X	0	0	1	16.384kHz	Duty 50%
X	0	1	0	1.024kHz	Duty 50%
X	0	1	1	128Hz	Duty 50%
X	1	0	0	16Hz	Duty 50%
X	1	0	1	1Hz	↓Seconds counter increment. Duty 50%
X	1	1	0	1/60Hz	↓Minutes counter increment. Duty 50%
X	1	1	1	"L"	Low Level

Adjustment function

BANK 1 ADDRESS (A3,A2,A1,A0)=(0,0,0,1) DATA (D3,D2,D1,D0)=(X,X,X,1)	Second counter backs to 0 when it's adjusted 0 ~ 29 sec. If it's adjusted on 30 ~ 59 sec., the second counter goes up to 0 sec. and the minute counter shows the next minute.

Oscillator circuit

Not required because an output ballast registor (Approx. 100kΩ) is used.



*Bank register (A3,A2,A1,A0) = (1,1,0,1) = D

D3	D2	D1	D0	BANK0:setting or rate time
Timer	Alarm	X	0	BANK1:setting or rate of Alarm
EN	EN	X	1	data, $\overline{12}$/24 hour system, leap year, choice of CLKOUT, and adjustment

Set 1 to enable alarm output
Set 0 to disable alarm output
(16Hz/1Hz clock signals not affected)

Set 1 to start clock. Set 0 to stop seconds and subsequent counters.

*The leap-year counter registers a leap year when D1 = D0 = 0. It simultaneously counts with the year counter.

*The $\overline{12\text{-hour}}$/24-hour selector sets the 12-hour system when D0 = 0 and the 24-hour system when D0 = 1. PM or AM is selected when D1 in the 10-hour counter is 1 or 0, respectively.

*Reset controller 16Hz/1Hz clock register.

(A3,A2,A1,A0) = (1,1,1,1) = F

D0 = 1:resets all alarm register and internal Alarm F/Fs.
D1 = 1:dividers before seconds counter reset.
D2 = 0:switches on the 16Hz clock pulse generated from the ALARM terminal.
D3 = 0:switches on the 1Hz clock pulse generated from the ALARM terminal.

*Addresses 0 ~ D:able to read and write.

*Addresses E ~ F:only able to write and 0H always appears when read out.

*TEST register (A3,A2,A1,A0) = (1,1,1,0) = E:use for inspections at Ricoh Co., Ltd. Normal watch function is achieved by setting of the data (D3,D2,D1,D0) = (0,0,0,0).

For details, refer to the Application Manual.

(3) Construction of oscillator circuit

The following external parts are required for constructing the oscillator circuit:

(1) One 32.768 kHz crystal oscillator
(2) Two condensers (including one trimmer condenser)
(3) One resistor of approx. 100 kΩ, for RP5C01 only

The oscillator is easily affected by external noise, leading to error in the clock. Care should therefore be exercised when constructing it on the PCB, and the following general points should be observed when constructing the oscillator circuit on the PCB:

(a) The crystal oscillator and the load capacitor CL should be mounted as close as possible to the OSC terminals.
(b) Signal lines and power supply lines should be placed as far as possible from the oscillator circuit, since they can interfere with its proper operation.
(c) The resistance of the PCB between OSCIN and OSCOUT and the resistance between the pins should be made as high as possible.

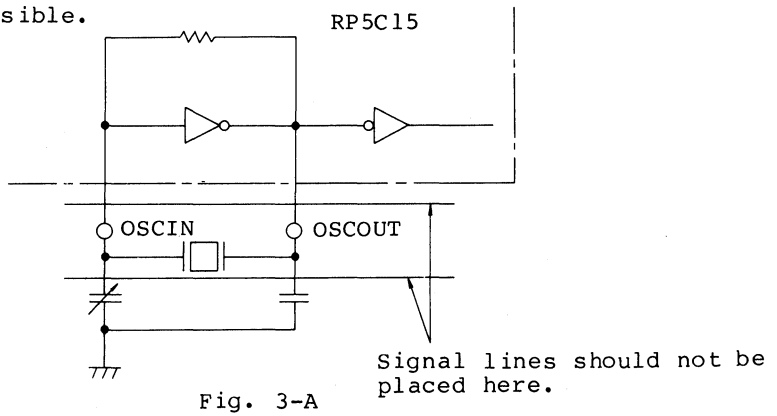


Fig. 3-A

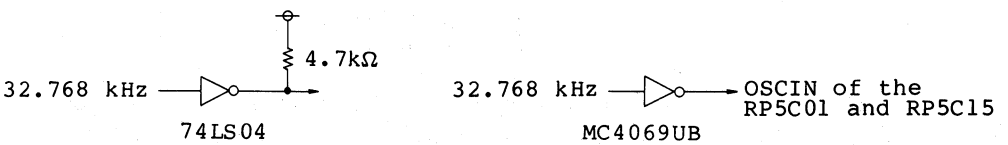
No particular specifications are set for the crystal oscillator. The accuracy of the clock generally depends on the following parameters:

(1) The accuracy of the crystal oscillator
(2) The capacity of the condensers
(3) The ambient temperature
(4) The supply voltage
(5) The gain of the built-in amplifier in the RP5C01 and RP5C15

Data on the oscillator circuit obtained by Ricoh, Ltd. are given for reference in Fig. 4-1 and subsequent diagrams on page 30. However, because of the effect of external stray capacity and other factors, the same results will not necessarily be obtained even if exactly the same measurement circuit is used, and the results therefore cannot be guaranteed. The oscillation accuracy, backup current and oscillation stability should therefore be checked under different supply voltages and ambient temperature conditions with the device mounted on the particular PCB with which it is to be used.

The accuracy of the oscillation frequency should be measured by causing a standard clock signal to be output from terminal 3 (CKOUT) or terminal 15 ($\overline{\text{ALARM}}$) in the case of the RP5C15, or, in the case of the RP5C01, from terminal 15 only. The RP5C15 is programmed to output a 16 kHz clock signal from terminal 3, making it particularly easy to check the accuracy of the oscillation frequency by connecting the CKOUT terminal to a frequency counter.

The measuring probes of a frequency counter or oscilloscope should not be connected directly to the OSCIN or OSCOUT terminal, since the capacity of the probes will alter the oscillation conditions and make correct measurement impossible. When either the RP5C01 or RP5C15 is oscillated externally, a 32.768 kHz clock signal should be input via the OSCIN terminal. However, since the input level of this terminal is not the TTL level for either the RP5C01 or RP5C15, a TTL output cannot be connected directly to it (See Fig. 3-B).



Connection of TTL and CMOS outputs to OSCIN terminal of the RP5C01 and RP5C15

Fig. 3-B

(4) Power dissipation

Except for OSCIN and CS, all the inputs of the RP5C01 and RP5C15 are designed to be TTL-compatible, but the operating current differs depending on whether the input voltage VIN gives VIH = 2.0V (the minimum) or Vcc. To make the power dissipation as low as possible, the input voltage should be set as close as possible to the supply voltage Vcc or GND. Also, most of the power dissipated during backup is consumed by the oscillator circuit. The power dissipation depends closely on the backup voltage, and the results of measurement carried out by Ricoh on this are shown in Tables 4-1 and 4-2 below.

Supply voltage	2.2V	2.5V	3.0V	3.7V	5.0V	Unit
Standby current	7.9	13.2	26.5	56.7	153.8	μA

No. of samples: 10 (average) at 25°C
Input terminal: Vcc or GND. Output terminals on no-load.

Table 4-1 Power dissipation of RP5C01

Supply voltage	2.0V	2.5V	3.0V	3.5V	5.0V	Unit
Standby current	3.0	4.9	8.8	15.3	57.2	μA

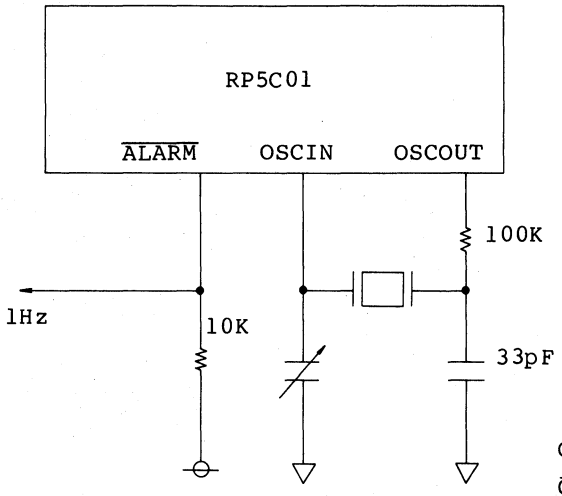
No. of samples: 10 (average) at 25°C
Input terminals: Vcc or GND. Output terminals on no-load.

Table 4-2 Power dissipation of RP5C15

Characteristics of oscillator circuit for RP5C01

Measurement conditions

Crystal oscillator used: Kinsekisha Lab. Type-P3



CS = H

$\overline{CS}$ = L

ADDRESS = F (1,1,1,1)

DATA = B (1,0,1,1)

Measuring 1Hz from $\overline{ALARM}$ terminal
(For temperature characteristics,
RP5C01 alone in a stable-temperature
chamber and other components in ambient
temperature during measurement)

Fig. 4-1

Dependence of oscillation frequency on power supply voltage at room temperature (25°C) (0 PPM is set at 5 volts.)

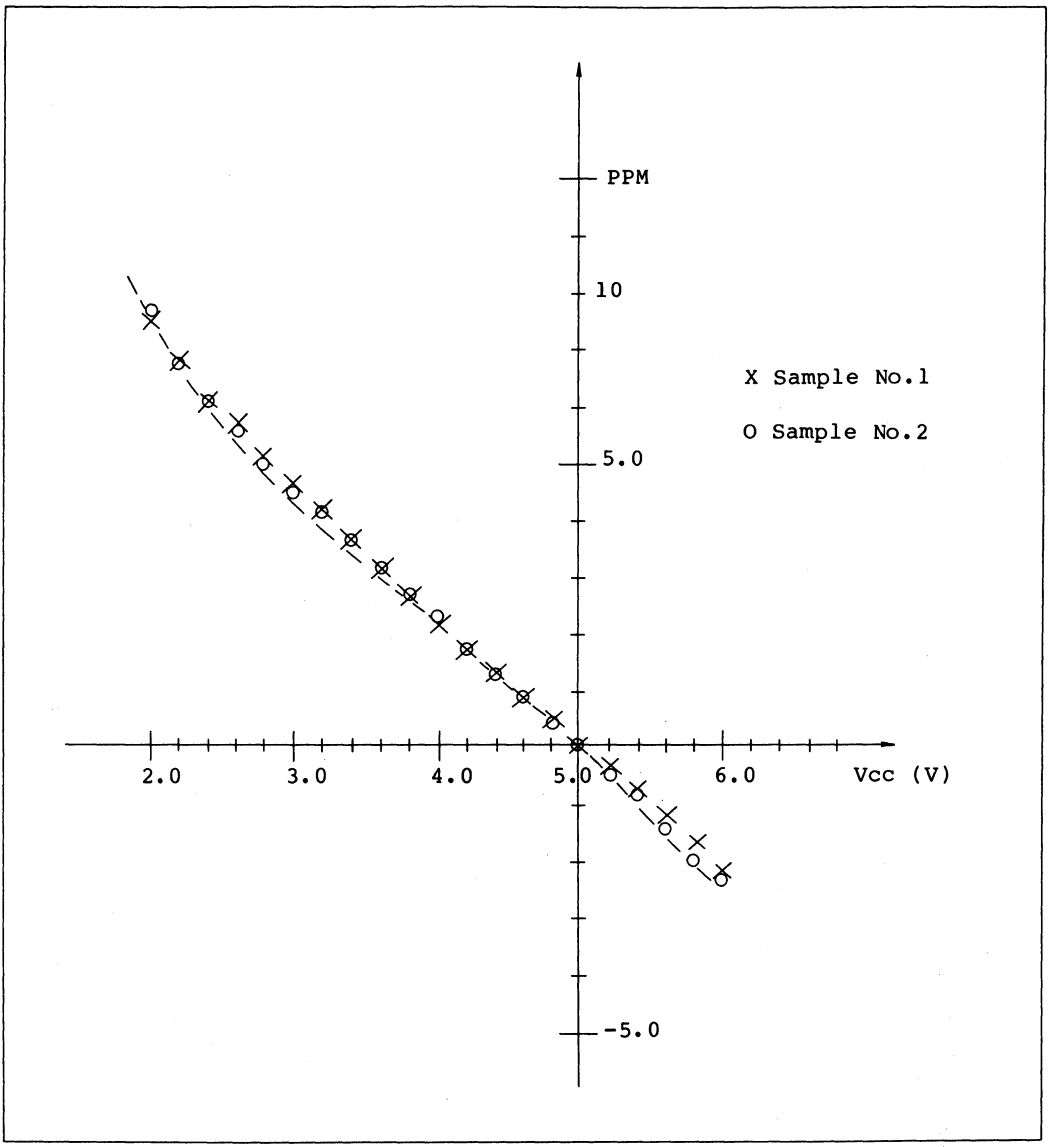


Fig. 4-2

Dependance of oscillation frequency on temperature (Vcc = 5V)
(0 PPM is set at 25°C.)

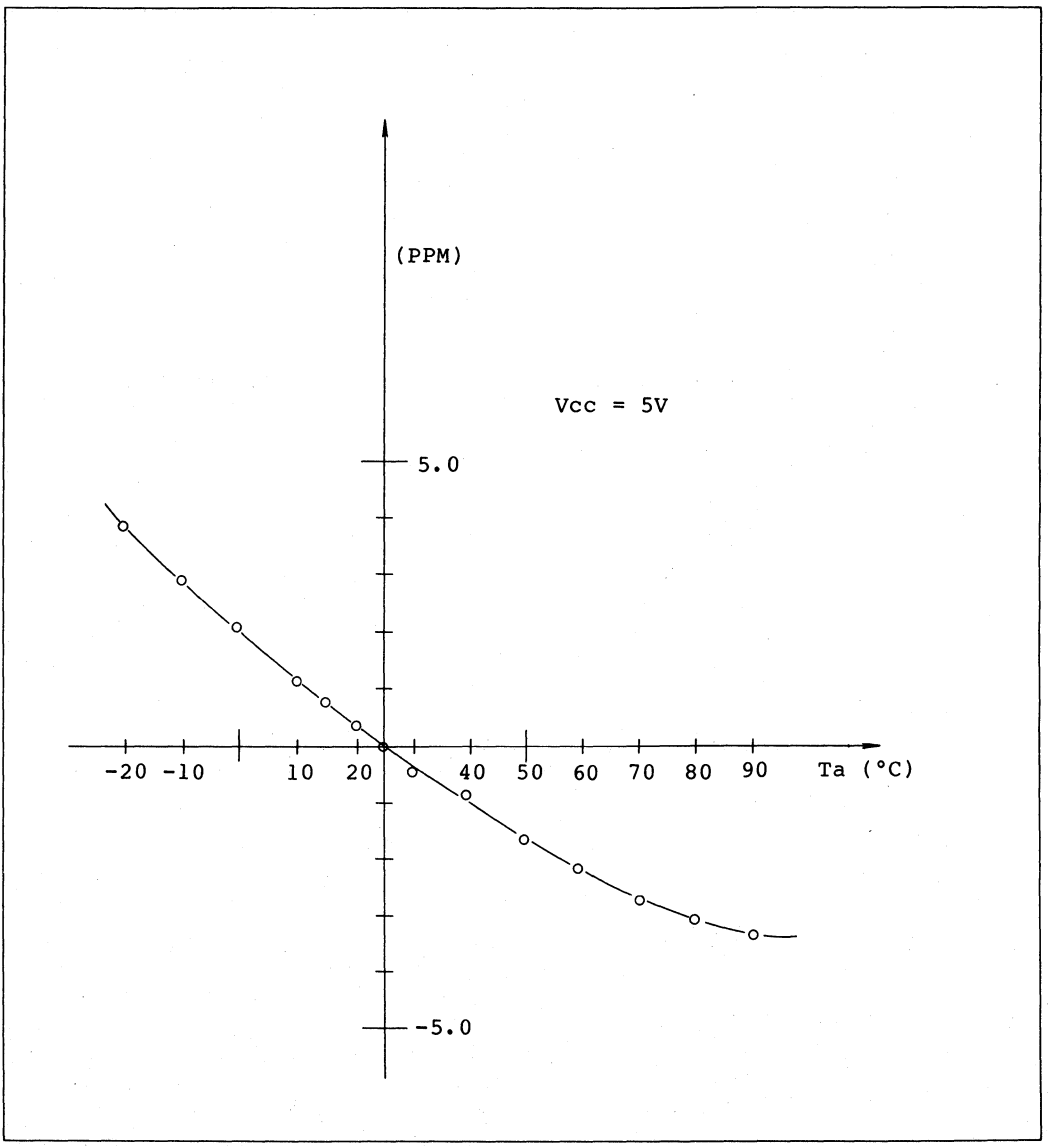


Fig. 4-3

Dependence of oscillation frequency on temperature (Vcc = 3V)
(0 PPM is set at 25°C.)

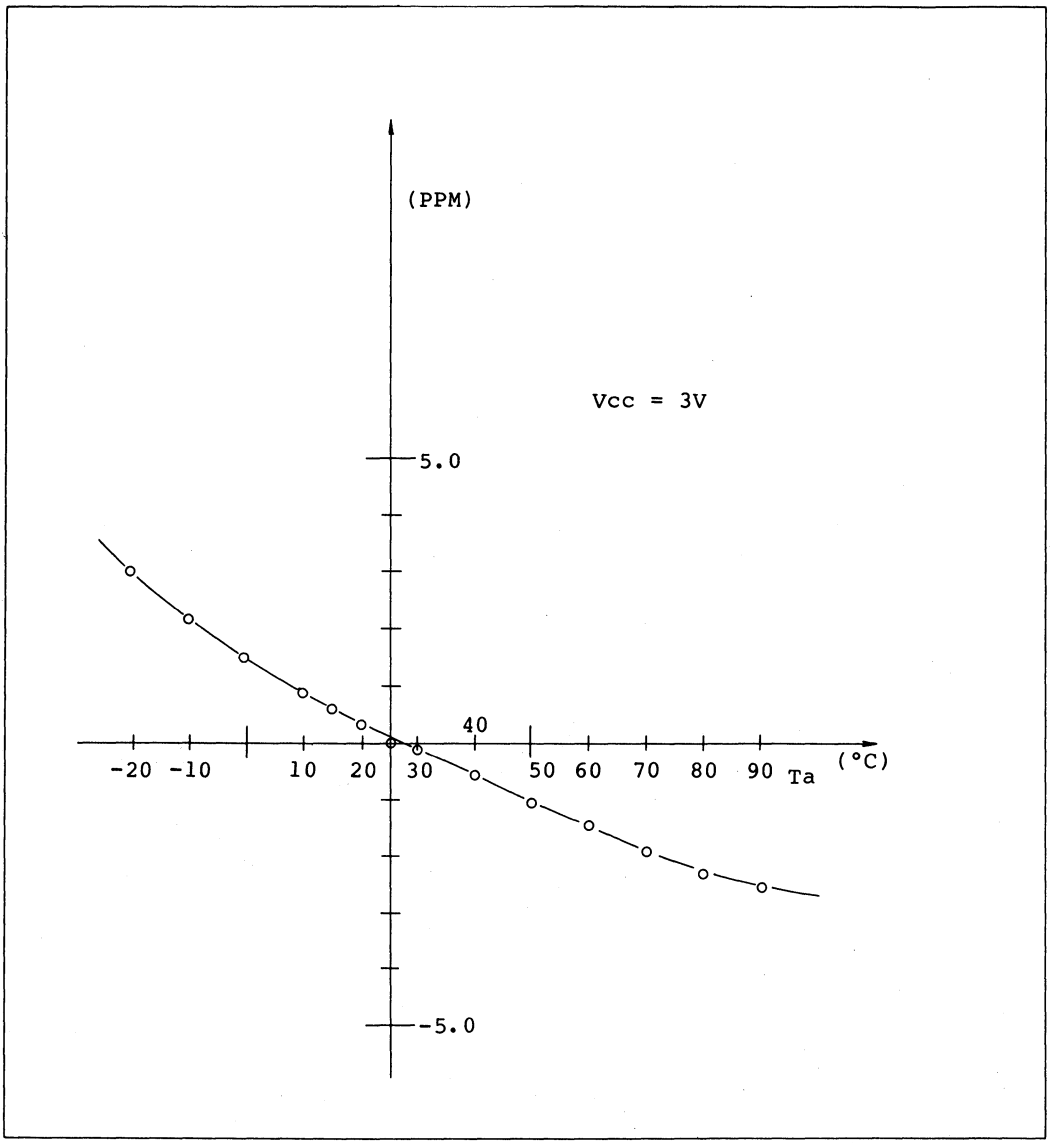


Fig. 4-4

Dependence of oscillation frequency on temperature (Vcc = 2.2V)
(0 PPM is set at 25°C.)

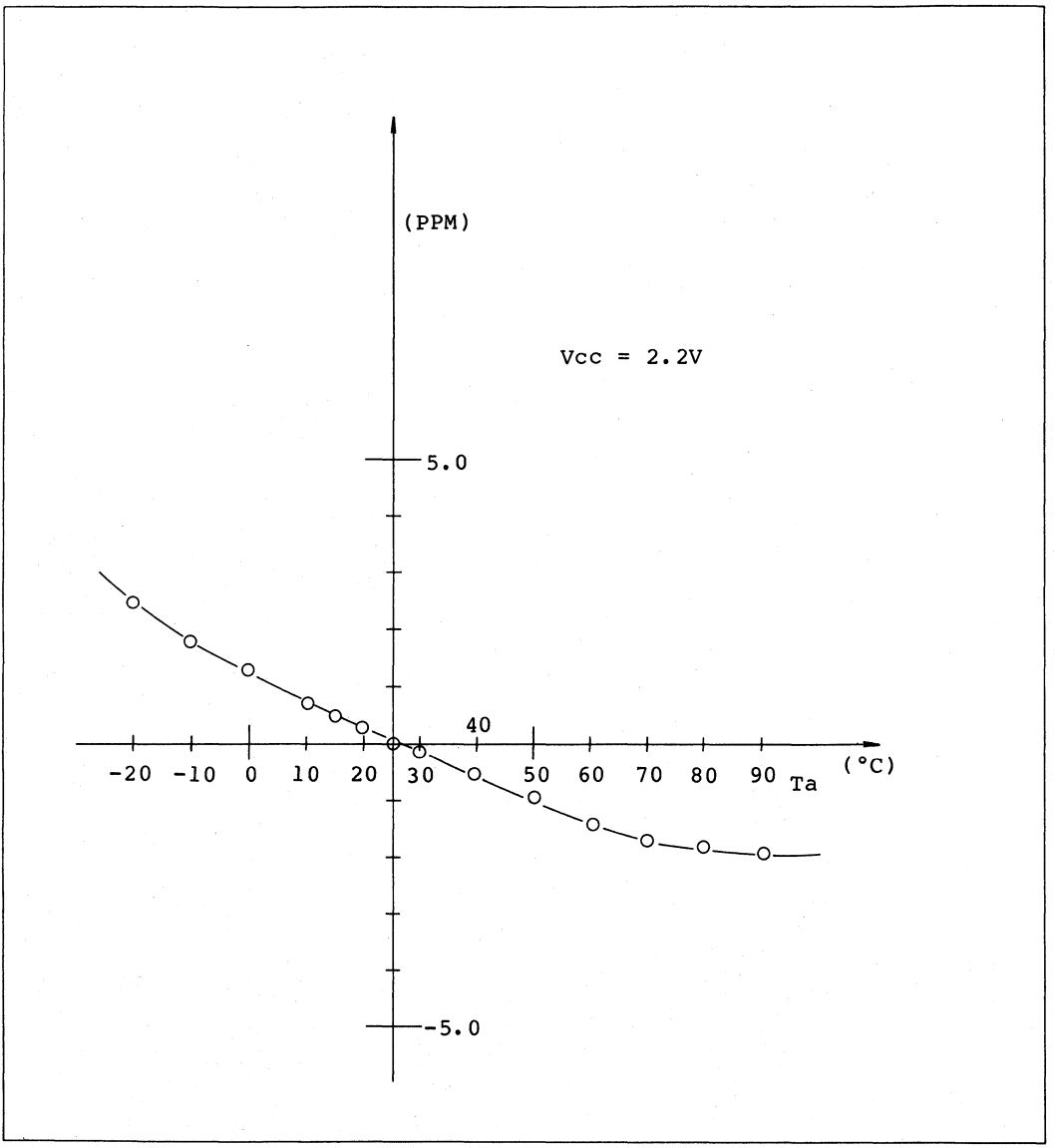
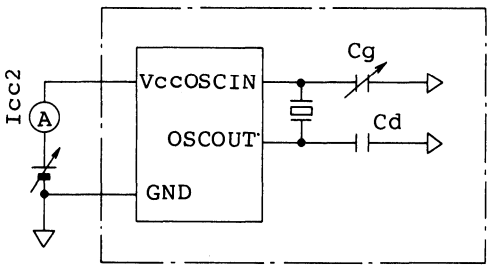


Fig. 4-5

Characteristics of oscillator circuit for RP5C15

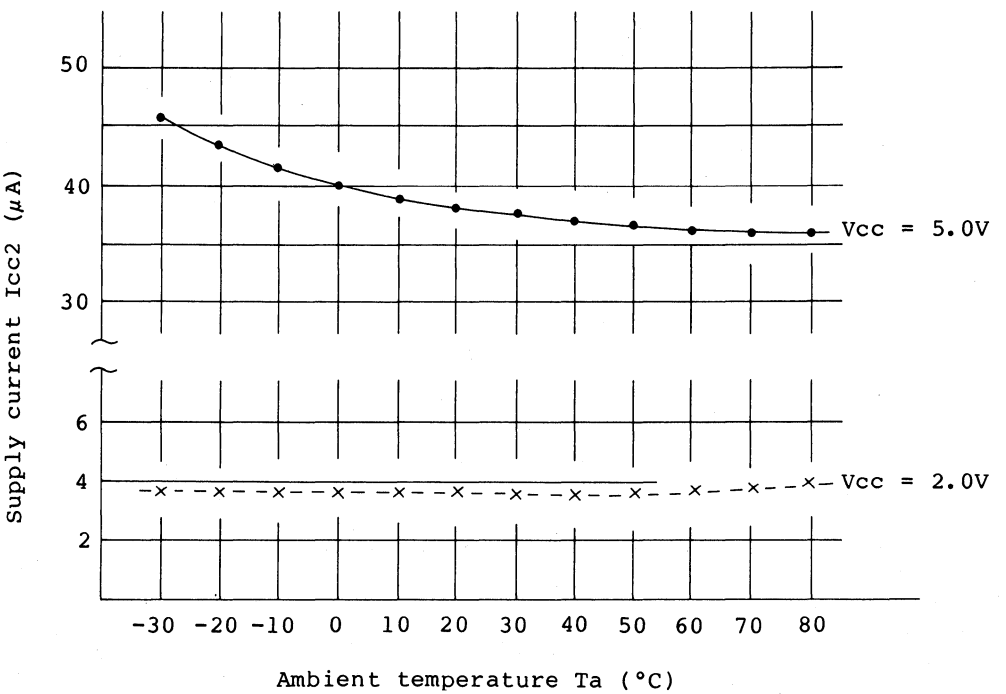
(1) Dependence of standby supply current of RP5C15 (ICC2) on ambient temperature:

Measurement conditions



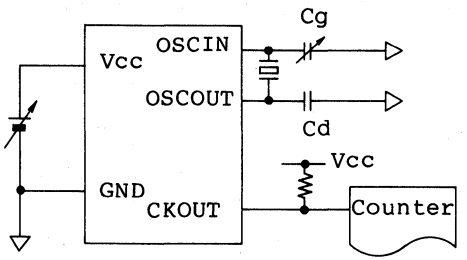
Constant-temp. chamber

CS = H
$\overline{CS}$ = L
A0~A3 = H
$\overline{RD}$,$\overline{WR}$ = H
D0~D3 = GND
CKOUT = OPEN
Cd = 39PF
Cg = 3~11PF trimmer condenser



(2) Dependence of oscillation frequency of RP5C15 on supply voltage at 25°C

Measurement conditions



CS = H

$\overline{CS}$ = GND

A0~A3 = Vcc

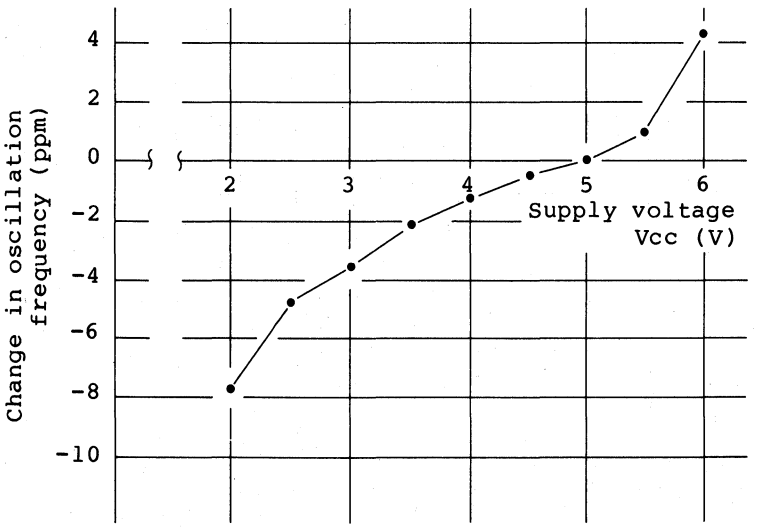
$\overline{RD}$,$\overline{WR}$ = Vcc

D0~D3 = GND

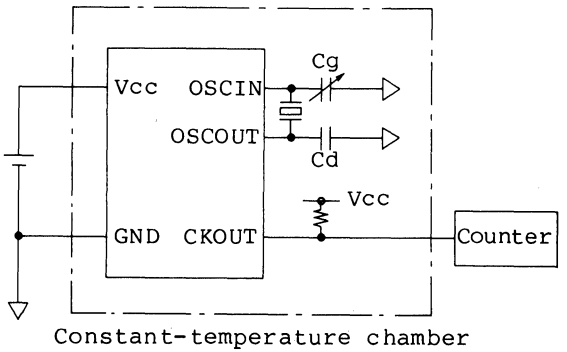
Cd = 39PF

Cg = 3~11PF trimmer condenser

Output 16 kHz via CKOUT and measure with frequency counter.

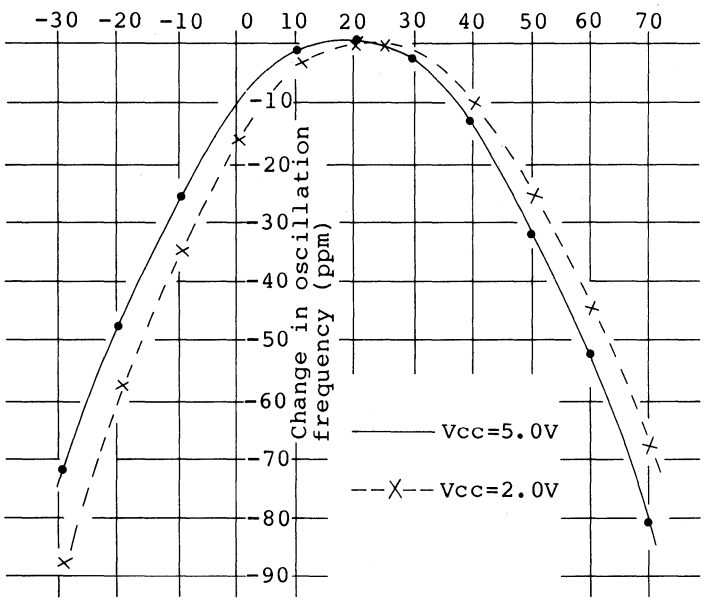


(3) Dependence of oscillation frequency of RP5C15 on ambient temperature



CS = H
$\overline{CS}$ = L
A0-A3 = H
$\overline{RD}$,$\overline{WR}$ = H
D0-D3 = L
Cd = 39PF
Cg = 3-11PF trimmer condenser

Output 16 kHz via CKOUT terminal and measure with frequency counter.



Note: The variation in oscillation frequency can be reduced slightly by the use of a temperature-stabilized condenser for Cd. However, the frequency variation obtained here results almost entirely from the characteristics of the crystal oscillator used.

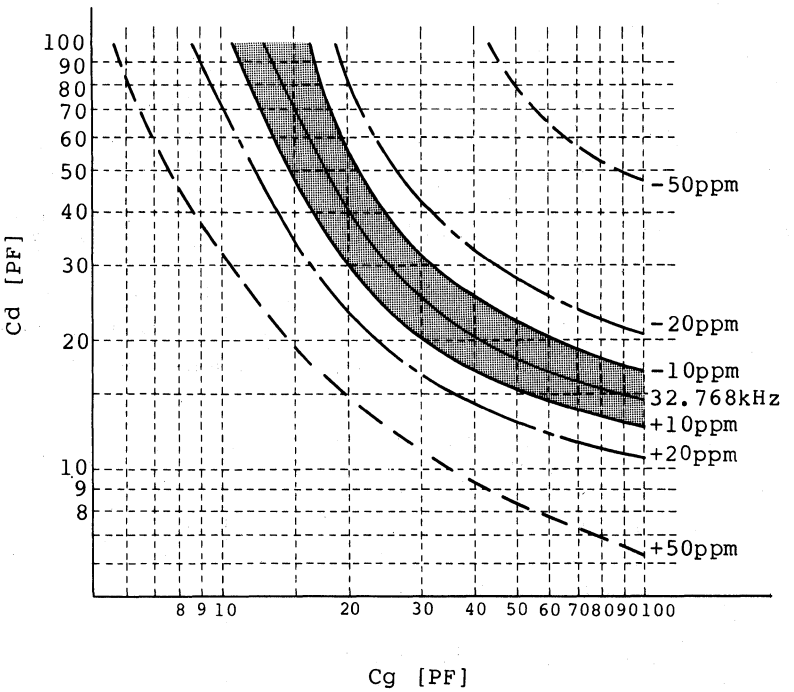

100
90
80
70
60
50
40
30
20
10
9
8
Cd [PF]
8 9 10
20
30
40
50 60 70 80 90 100
Cg [PF]
-50ppm
-20ppm
-10ppm
32.768kHz
+10ppm
+20ppm
+50ppm

Fig. 4-9

(5) Connection to CPU

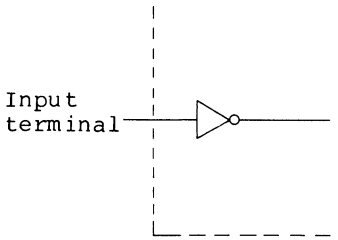


Fig. 5-1

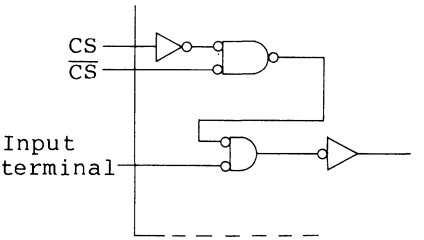
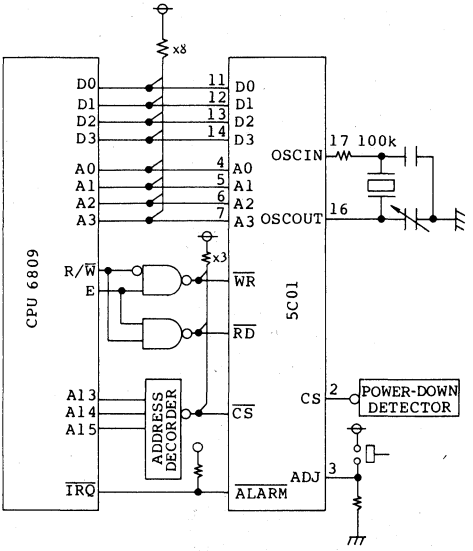
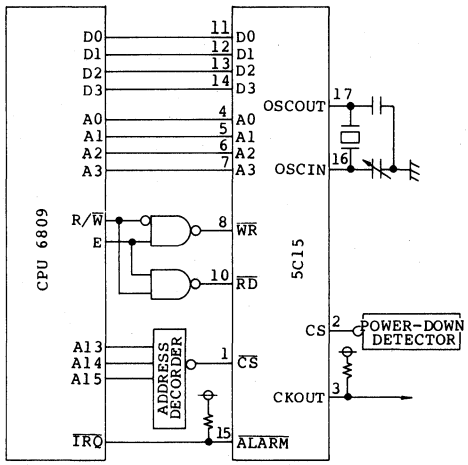


Fig. 5-2

Because of the structure of the input terminals of the RP5C01 ($\overline{WR}$,$\overline{RD}$, A0-A3, D0-D3,ADJUST, and CS) as shown in Fig. 5-1, a through current flows at the input buffer transistor when an input is allowed to float, making it necessary to connect a pull-up or pull-down resistor externally. The RP5C15, however, has the structure shown in Fig. 5-2, and there is no danger of through current flow even if terminals other than CS and OSCIN are allowed to float. The pull-up or pull-down resistors needed with the RP5C01 are therefore unnecessary with the RP5C15. The resistors used with the RP5C01 are for the purpose of keeping the input terminal levels equal to Vcc or GND, and it is immaterial whether pull-up or pull-down resistors are used. This applies to all inputs. However, it is recommended that pull-up resistors be used with $\overline{WR}$, $\overline{RD}$, and $\overline{CS}$ so that these terminals become non-active, for example, when the CPU is in the "hold" state and the control signals of the CPU start to float instantaneously. This instantaneous $\overline{WR}$ = $\overline{CS}$ = low state may affect memory or cause peripherals to write invalid data.



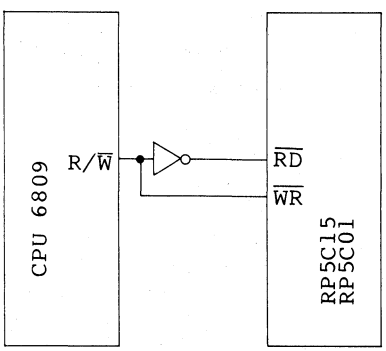
Connection example for RP5C01



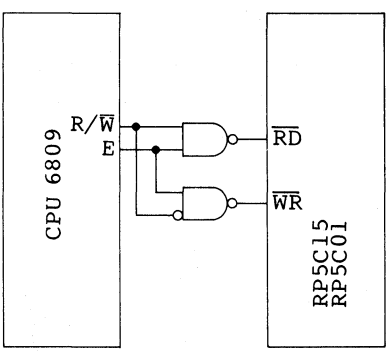
Connection example for RP5C15

Fig. 5-3

A further specification to which attention must be paid when connecting the RP5C01 and RP5C15 to a CPU is the AC characteristics tAC. An example is shown in Fig. 5-4, where connection to a 6809 CPU in the way shown will result in tAC failing to reach the required value. The correct method of connection is shown in Fig. 5-5. When the RP5C01 is used, care must also be taken that tWDL is satisfied. If a CPU is to be used which does not give the correct value of tWDL (e.g., 8-bit 1-chip microcomputers, such as MC6801, HD6301, μPD78C05, etc.) care should be taken.



Inappropriate
Fig. 5-4



Appropriate
Fig. 5-5

It should also be noted that the definition of the AC characteristic tAC (see pages 12 and 21)differs for the RP5C01 and RP5C15 as follows:

(1) In the case of the RP5C01, tAC is the time taken from address valid to logical AND (CS·$\overline{CS}$·$\overline{RD}$) or (CS·$\overline{CS}$·$\overline{WR}$) (See page 12).

(2) In the case of the RP5C15, tAC is the time taken from logical AND (CS·$\overline{CS}$·address valid) to logical AND (CS·$\overline{CS}$·$\overline{RD}$) or (CS·$\overline{CS}$·$\overline{WR}$) (See page 21).

The following explanation shows how (1) and (2) above apply to connection to a 6809 or Z80:

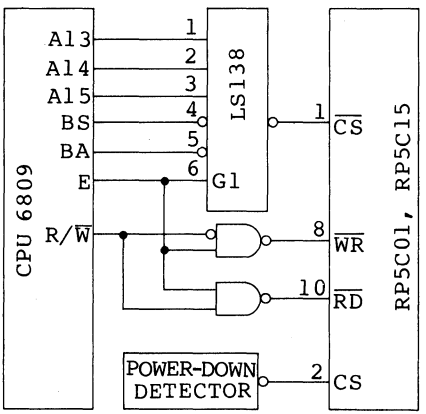


Fig. 5-6 Connection to 6809

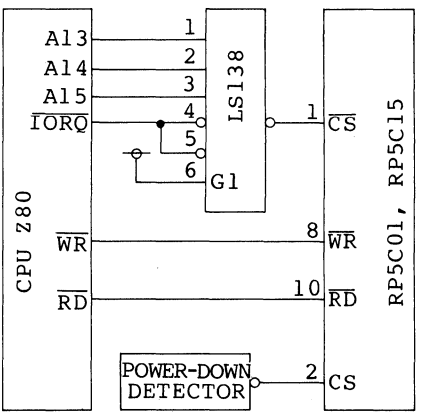


Fig. 5-7 Connection to Z80

Fig. 5-6 shows the RP5C01 connected to a 6809 CPU. The following explanation applies when CS is high, i.e., when the supply voltage is normal. If a 6809 CPU is connected as shown in Fig. 5-6, the timing chart will be as shown in Fig. 5-8 below, if decoder and gate propagation delays between the CPU, the RP5C01 and the RP5C15 are ignored.

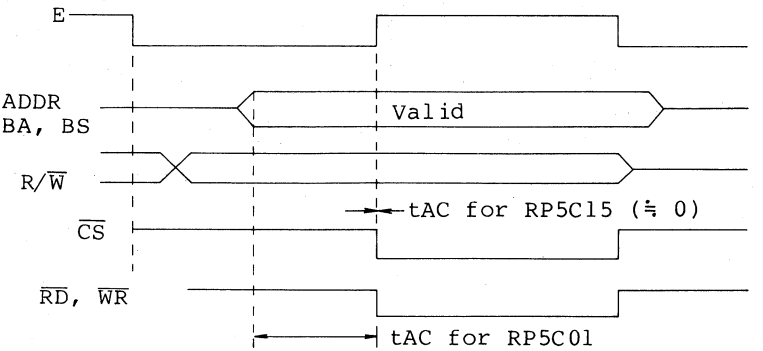


Fig. 5-8 (Timing chart for arrangement shown in Fig. 5-6)

The following points arising from the timing shown in Fig. 5-8 should be noted about the connection to the 6809 CPU shown in Fig. 5-6 :

(a) There is no problem when using the RP5C01.

(b) With the RP5C15, tAC ≒ 0, and the arrangement shown in Fig. 5-6 cannot be used.

The same considerations apply when a Z80 is connected as shown in Fig. 5-7. The timing chart for this arrangement is shown in Fig. 5-9, which shows that $\overline{CS}$ does not become active until $\overline{IORQ}$ becomes active. Thus in the case of the RP5C15, tAC ≒ 0 and the AC characteristics are not satisfied.

Thus the connection to a Z80 shown in Fig. 5-7 can be used with the RP5C01, but not with the RP5C15.

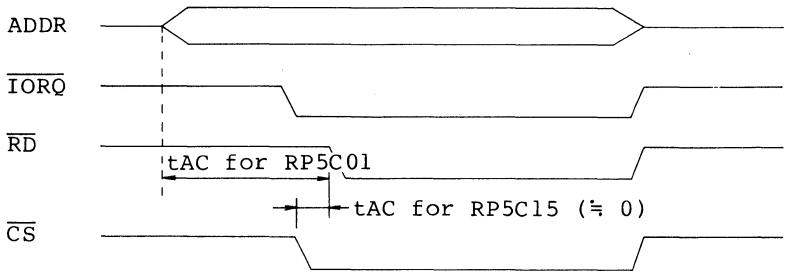


Fig. 5-9 (Timing chart for arrangement shown in Fig. 5-7)

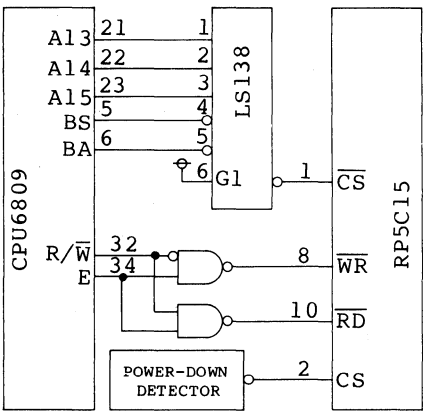


Fig. 5-10
Connection of RP5C15 to 6809

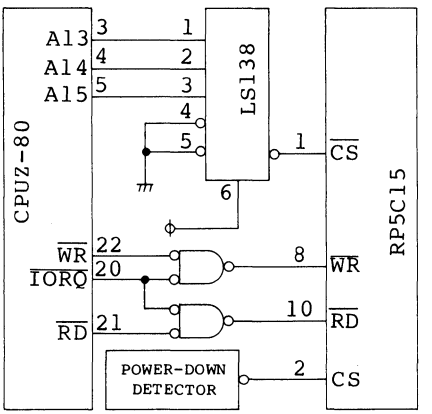


Fig. 5-11
Connection of RP5C15 to Z80

The necessary arrangements for achieving the required value of tAC when the RP5C15 is connected to a 6809 or Z80 CPU are shown in Fig. 5-10 and Fig. 5-11. If these arrangements are used, the timing will be as shown in Fig. 5-12 and tAC will reach the required value even when the RP5C15 is used.

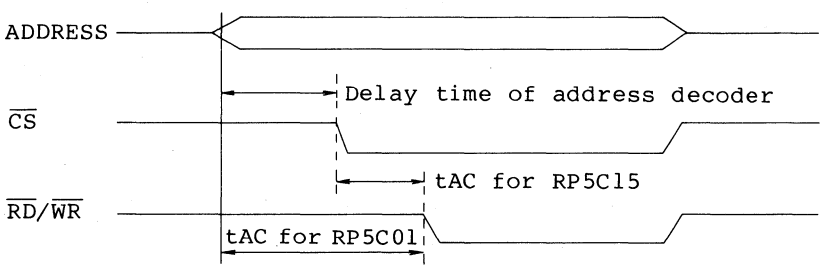


Fig. 5-12

To achieve the required value of tAC with the RP5C15 in this way, it is necessary to make $\overline{CS}$ active as quickly as possible. To do this, it is recommended that a high-speed decoder such as a 74ALS138, 74ALS139 or other ALS series decoder be used with a high-speed CPU such as an 8086, Z8000 or 68000. For the same reasons as above, the following points should be noted when connecting the RP5C01 or RP5C15 to a 4-bit CPU as shown in Figs. 5-13 and 5-14.

(1) With the RP5C01, $\overline{CS}$ and $\overline{RD}$ ($\overline{CS}$ and $\overline{WR}$ during write operations) can be simultaneously set to low after validating the address.

(2) With the RP5C15, $\overline{CS}$ and $\overline{RD}$ or $\overline{CS}$ and $\overline{WR}$ cannot be set simultaneously set to low. $\overline{CS}$ should be set to low at least one command before $\overline{RD}$ or $\overline{WR}$ is set to low.

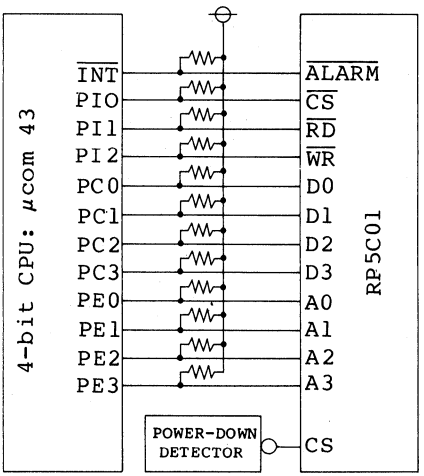


Fig. 5-13 Connection of RP5C01 to 4-bit CPU

(4-bit CPU: NEC μcom-43)

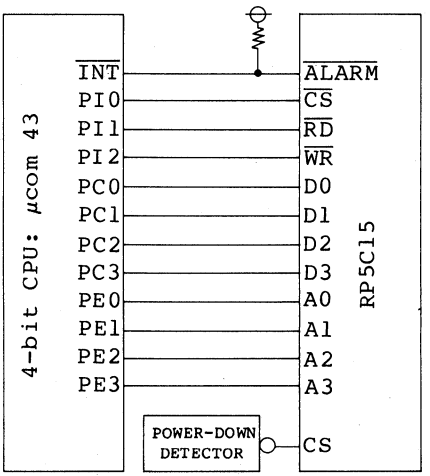
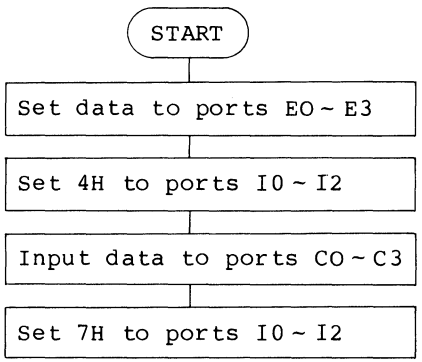


Fig. 5-14 Connection of RP5C15 to 4-bit CPU

(4-bit CPU: NEC μcom-43)

An example of data readout is given below for connection to a 4-bit CPU

Data readout flowchart for RP5C01 (when arranged as shown in Fig. 5-13)



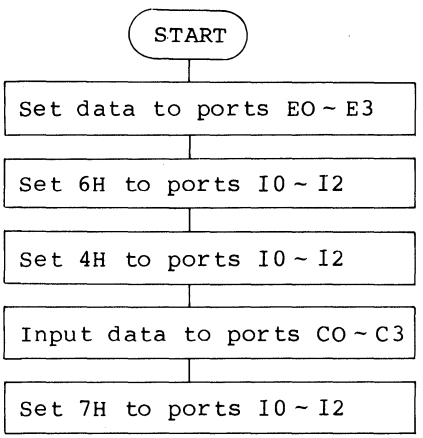
[Explanation]

(Set addresses)

($\overline{CS}$ = $\overline{RD}$ = low, $\overline{WR}$ = high)

($\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = high)

Data readout flowchart for RP5C15 (when arranged as shown in Fig. 5-14)



(Set addresses)

($\overline{CS}$ = low, $\overline{RD}$ = $\overline{WR}$ = high) (NOTE 1)

($\overline{CS}$ = $\overline{RD}$ = low, $\overline{WR}$ = high)

($\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = high)

(NOTE 1) When reading out data with the RP5C15, do not set $\overline{CS}$ and $\overline{RD}$ to low simultaneously, and when writing data, do not set $\overline{CS}$ and $\overline{WR}$ to low simultaneously, so as to obtain the minimum value of tAC.

When using a 4-bit CPU, care should be taken with the AC characteristics tcc (max.) (See pages 12 and 21). The specified value of tcc (max.) for the RP5C01 is 10 μsec., and the specified value of tccR (max.) and tccW (max.) for the RP5C15 is 13 μsec. The meaning of tcc (max.) is that if the data is not read out within the specified time, the CPU may read out incorrect data. This does not mean that the data of the RP5C01 or RP5C15 is destroyed. When reading out data with a 4-bit CPU, it is thus necessary for the CPU to take in the data from the RP5C01 or RP5C15 within tcc (max.) after $\overline{CS}$ and $\overline{RD}$ have become active. For this reason, the interrupt service routine, which may make tcc longer than tcc (max.), should be disabled during read/write operations (Note 3-1).

If the backup power supply is arranged as in Fig. 5-15, the supply voltage of the RP5C01 and RP5C15 will be about 0.6V lower than the system supply voltage at 25°C, and the maximum value of the input voltage VIN will be Vcc + 0.6V. Thus the DC electrical characteristic VIN (max.) = Vcc + 0.3V will not be satisfied. The arrangement shown in Fig. 5-15 does not meet the DC specifications. (This is identical to CMOS static RAM.)

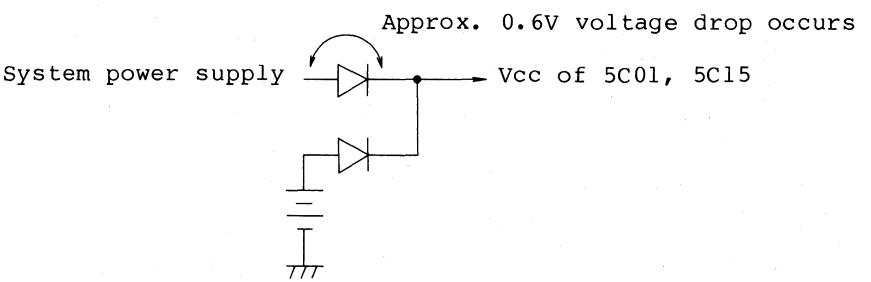
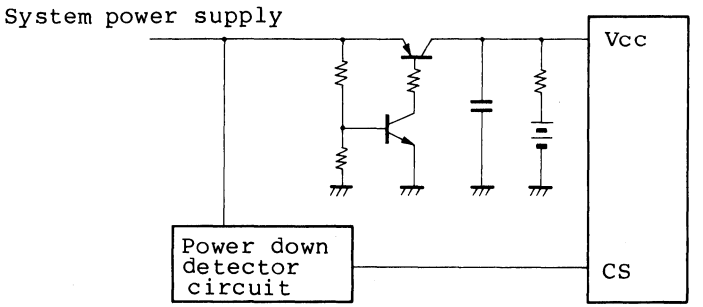


Fig. 5-15

(Note 3-1) The interrupt service makes tcc exceed tcc (max.) when the interrupt service routine begins at the status where data is not read out, although $\overline{RD}$ and $\overline{CS}$ are active.

Ideal backup power supply



(6) CS and $\overline{CS}$ terminals

Some of the functions of CS and $\overline{CS}$ are different between the RP5C01 and RP5C15.

(6-1) In the case of the RP5C15:
When CS = low or $\overline{CS}$ = high
(1) External $\overline{WR}$ or $\overline{RD}$ signals are not accepted.
(2) No through current flows at the input buffer transistor even if the input terminals are allowed to float.

Fig. 6-1 shows the above functions of CS and $\overline{CS}$. As this figure shows, terminal CS cannot be allowed to float.

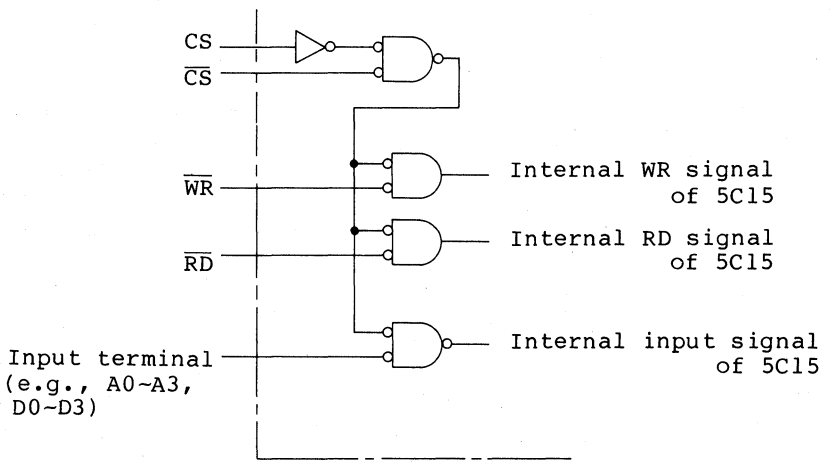


Fig. 6-1

The following points should be noted about CS and $\overline{CS}$:

(I) $\overline{CS}$ can be allowed to float when CS = low.

(II) CS cannot be allowed to float under any circumstances. If it is allowed to do so, a current will flow at the input buffer and cause rapid battery power consumption at battery start-up. Thus the voltage input to CS must be set to Vcc or GND at all times, regardless of whether or not the system is actually operating. The voltage level input to $\overline{CS}$ should therefore be set by connecting the CPU address decoder and the power-failure detection circuit to CS.

CS is sometimes used in the pull-up mode on other systems. However, when the system supply voltage is shut off as a result of main power failure or some other cause, the CPU can go into abnormal operation and produce the state $\overline{CS}$ = $\overline{WR}$ = low in the RP5C01 and RP5C15, with possible destruction of the RP5C01 and RP5C15's data because CS is always high. Terminal CS should therefore be set to low immediately after the system supply voltage is shut off.

(6-2) In the case of the RP5C01:

The RP5C01 differs from the RP5C15 in the following two respects:

(1) The input terminals of the RP5C01 should not be allowed to float, but should be pulled up or down to Vcc or GND at all times, regardless of the state of CS or $\overline{CS}$.

(2) When CS = low, the ADJUST signal is not accepted.

Fig. 6-2 shows above (1) and (2).

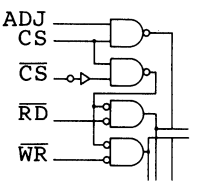


Fig. 6-2

(7) Reading clock data

A possible source of error in reading out the clock data occurs when the clock counts up during readout, causing the CPU to read out incorrect data.
Example 7-1 shows the situation that occurs when the CPU starts to read out the clock data at 59 min., 59 sec. past the hour. If the clock counts up while the CPU is still reading out the data, the CPU will read the hour incorrectly.

Time at which CPU starts to read out data: 1 0 : ⑤ ⑨ : ⑤ ⑨
Time at which CPU finishes reading out data: ① ① : 0 0 : 0 0

Data read by CPU: 1 1 : 5 9 : 5 9
(Note: circled figures are values read by CPU)

Example 7-1

There are following three methods -- (7-1) through (7-3) -- to avoid this problem.
(7-1) Stop the clock. (Set bit 3 of address D to 0.)
(7-2) Read the clock data twice.
(7-3) Read the data in synchronization with a 1Hz signal which is output from an $\overline{\text{ALARM}}$ terminal.

A detailed explanation of the above three methods follows. See Section 16 for the flowchart.

(7-1) Stopping the clock
To stop the clock, write 0 to the Timer Enable F/F (bit 3 of address D). (Fig. 7-1)
If 0 is written to the Timer Enable F/F, the internal Clock Hold circuit of the RP5C01 or RP5C15 is brought into operation (see block diagram), and a 1Hz pulse generated while the clock is stopped is stored for a maximum of 1 sec. in the Clock Hold circuit.

The following points should be noted if the clock is stopped:

(7-1-1) The 1-sec. signal stored in the internal Clock Hold circuit will be revised within 100 μsec. after 1 is written to the Timer Enable F/F. To prevent the data from being read incorrectly, the clock data cannot be read out during this 100 μsec. period.

(7-1-2) If the power supply is shut off for more than 1 sec. while the Timer Enable F/F is set to 0, the clock will be delayed. If power shutoff is detected, the Timer Enable F/F should therefore immediately be set to 1, restarting the clock, and terminal CS should be set to low.

D	MODE register	Timer EN	ALARM EN	M1	M0

Fig. 7-1 (Mode register is allocated at address D)

(7-2) Using software to read the clock data twice

This method prevents the necessity to stop the clock. The clock data is read once and then a second time, and the two readings are compared. If the readings are different, this indicates that the clock data changed during the readout procedure, and it is therefore necessary to read the data again.

(7-3) Reading out the clock data in synchronization with a 1Hz signal.

The RP5C15 can be made to output a 1Hz signal from the CKOUT terminal by setting the internal CKOUT Selection Register (Address 0 of Bank 0) or the $\overline{\text{ALARM}}$ terminal. The timing of the 1Hz signal and the internal counter is as follows:

The clock data is altered after (a) the leading edge of the 1Hz signal in the case of the CKOUT terminal, or (b) about 96μsec.

after the trailing edge of the 1Hz signal in the case of the $\overline{\text{ALARM}}$ terminal. Because of this, 1Hz signals output from the CKOUT and $\overline{\text{ALARM}}$ terminals will be approximately 180° out of phase. But an interrupt to CPU should be requested at the leading edge. With the RP5C01, a 1Hz signal can be output from the $\overline{\text{ALARM}}$ terminal only, so the clock data should be read out at the leading edge of this signal if this method is adopted. 1Hz signals output from the $\overline{\text{ALARM}}$ terminals of the RP5C01 or RP5C15 will be exactly in phase.

(8) Writing clock data

The correct clock data will not be written if the data changes during the writing operation. As with reading the clock data, there are three possible methods of ensuring that the data does not change during the writing operation. These are as follows:

(8-1) Stop the clock by writing 0 to the internal Timer Enable F/F

(8-2) Reset the internal 15-stage divider (by setting the internal Timer Reset F/F of address F of bit 1) and write the clock data within 1 sec.

(8-3) Write in synchronization with a 1Hz signal

The procedure for (8-1) and (8-3) is the same as for reading the clock data. However, it is recommended that, if method (8-1) is adopted, the 15-stage dividers be reset before writing data in the same way as for method (8-2). This is because, if a 1-sec. signal is generated internally while data is being written, a 1Hz pulse is stored in the internal Clock Hold circuit, and the data is revised upwards by 1 sec. in the 100 μsec. immediately after the write operation is finished and the clock is restarted by setting the Timer Enable F/F. The first second after restarting the clock thus appears to pass extremely quickly.

In method (8-2), resetting the 15-stage divider stops the clock data from being altered for 1 sec. With both the RP5C01 and RP5C15, writing 1 to the Timer Reset F/F generates an internal one-shot reset signal, and there is thus no need to write 0 to the Timer Reset F/F after the reset operation. The internal reset pulse width is about 100 μsec with the RP5C15 and is the duration of $\overline{WR}$ = low with the RP5C01.

When writing the clock data, the following two items should always be set at the same time:

(1) Set the hour counter to either the 12 or the 24 hour system.

(2) Set the Leap-Year counter (details of this are given later).

Care should also be taken that the software does not write impossible clock data (e.g., 10 or more to the second counter), since there is nothing in the hardware of either the RP5C01 or the RP5C15 to prevent this.

(9) Use of alarm

(9-1) Structure of $\overline{\text{ALARM}}$ terminal

For the internal structure of the $\overline{\text{ALARM}}$ terminal, see Fig. 9-1.

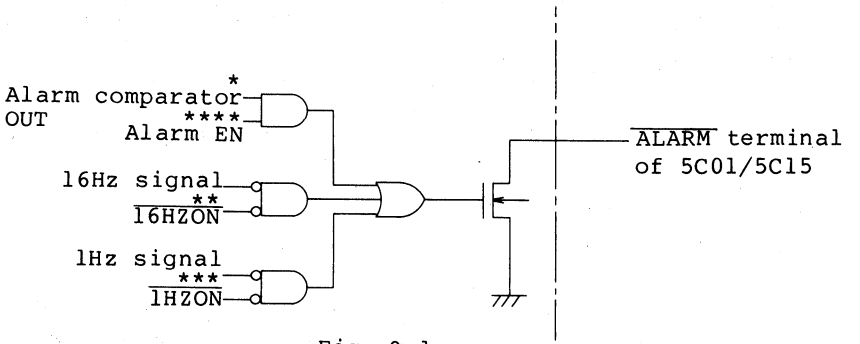


Fig. 9-1

(*) A detailed explanation of the Alarm Comparator is given in (9-2)

(**) $\overline{\text{16HZON}}$ is in bit 2 of the Reset Controller (address F)

(***) $\overline{\text{1HZON}}$ is in bit 3 of the Reset Controller (address F)

(****) Alarm EN is in bit 2 of the Mode Register (address D)

As shown in Fig. 9-1, the 16Hz signal, the 1Hz signal and the alarm signal can all be output independently.
For example, setting Alarm EN = 1, $\overline{\text{16HZON}}$ = 0 and $\overline{\text{1HZON}}$ = 0 will cause the alarm signal, the 1Hz signal and the 16Hz signal to be output simultaneously from the $\overline{\text{Alarm}}$ terminal.

(9-2) Alarm Comparator OUT

The Alarm Comparator OUT signal is an internally-generated signal, and it is output when the contents of the Alarm Register and the Clock Counter match completely. (Fig. 9-2)

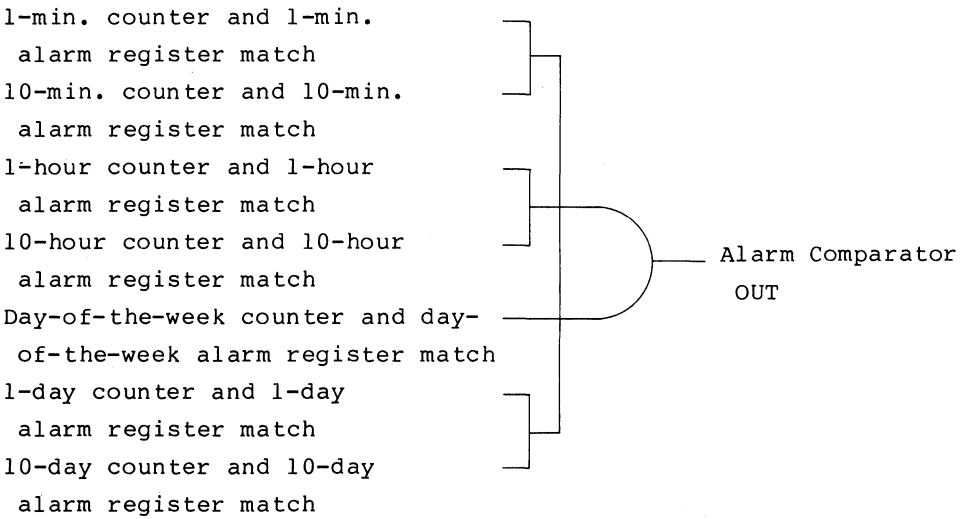


Fig. 9-2

However, if the structure shown in Fig. 9-2 is adopted, the required software is extremely cumbersome if, for example, it is desired to output the alarm signal from the $\overline{\text{Alarm}}$ terminal at 10:00 daily. The reason for this is that, in order to match all the items, the contents of the day-of-the-week, 1-day and 10-day Alarm Registers must be rewritten by CPU every day. To reduce the amount of software required, the Alarm Reset function can be used, by writing 1 to bit 0 of address F.

When "1" is written in the alarm reset, all four contents of the alarm register are set at "0". This means the resister is open and ready for resetting, erasing the previous alarm setting. Thus, for example if you write "5" into the minute counter only, the alarm output sounds for one minute at five minutes past every hour.

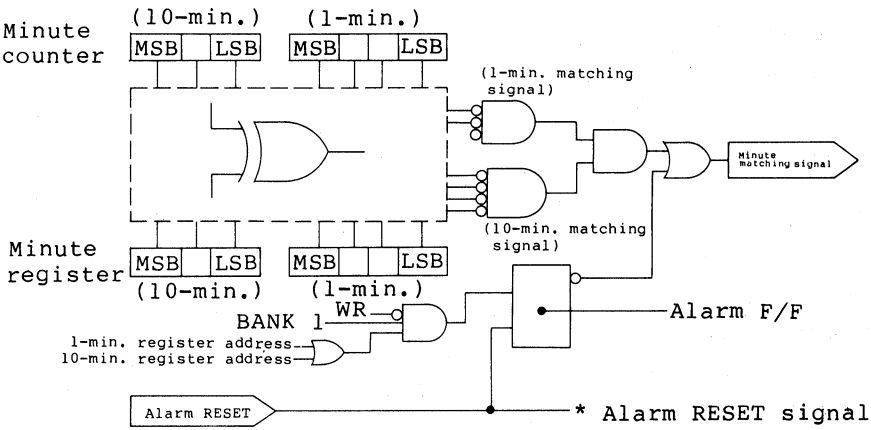


Fig. 9-3

Fig. 9-3 is a block diagram of the matching circuit for the 1-min. register and 1-min. counter of the RP5C01. It is almost the same as for the RP5C15 except for the way in which Alarm F/Fs are set. Each Alarm Register contains an Alarm F/F, and the Alarm Reset signal resets all the Alarm F/Fs as shown in Fig. 9-3. The following precautions should be taken when resetting the Alarm F/Fs:

(1) When the Alarm F/Fs are reset, the contents of all the Alarm Registers are treated as matching the corresponding clock counters, and an $\overline{\text{ALARM}}$ signal will be output externally. Alarm EN should therefore be set to 0 before resetting the alarm.

(2) In the case of the RP5C15, no data can be written to the Alarm Register for 100 μsec. after the Alarm F/Fs have been reset. This is because an Alarm Reset signal lasting a maximum of 100 μsec. is generated internally after the leading edge of $\overline{WR}$. In contrast to this, the Alarm Reset signal in the RP5C01 is generated within the duration of $\overline{WR}$ = low, making it possible to write data into the Alarm Registers immediately (See Fig. 9-4).

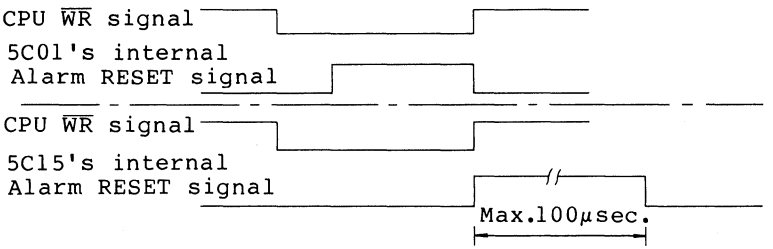


Fig. 9-4

(9-3) Alarm function when battery backed-up

Alarm can be used when battery is backed-up.
The characteristics between VOL and IOL and ALARM terminal (open-drain output) at the temperature of Ta = 25°C is shown in Fig. 9-5.

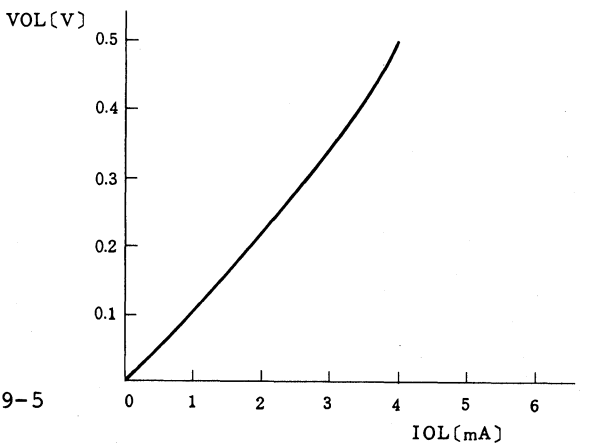


Fig. 9-5

(10) Setting leap years

Initial setting of leap years is necessary for both the RP5C01 and RP5C15.
The Leap-Year Counter consists of a Mod 4 count-up counter which counts up at exactly midnight on 31 December in the same way as the year counter. Twenty-nine days are counted in February when the Leap-Year Counter is 00.
Table 10-1 illustrates the relation between the Leap-Year Counter and the leap year.

Leap-Year Counter

D1	D0	
0	0	The current year is a leap year
0	1	A leap year is due 3 years from now
1	0	A leap year is due 2 years from now
1	1	Next year is a leap year

Table 10-1

If the Leap-Year Counter is initialized correctly, and provided that the contents of the counter are not destroyed by battery failure or other causes, the date will be adjusted automatically for leap years up to the year 2099. (The year 2100 is not a leap year.)

(11) Test Register

The Test Register is for high-speed function testing of the RP5C01 and RP5C15 when shipped by Ricoh, and its contents must be set to (0,0,0,0) for correct clock operation. With the RP5C15, it is immaterial how many times 0 is written to this register, but with the RP5C01, there is a danger of destroying the clock data depending on the particular CPU in use. This problem may arise with CPUs that do not satisfy the AC characteristics tWDL = max. 40 nsec., but will not arise with Z80, 6809, 8085, 6800 or 6502 CPUs. Some 8-bit single-chip microcomputers do not satisfy tWDL.

It is therefore recommended that with the RP5C01, the Test Register should be cleared immediately before clock data is written at the initialization of the RP5C01, rather than each time the power is turned on. For details, please refer to the flowchart.

(12) Week counter

The week counter is a Mod 7 count-up counter.
The relation between the counter value and the day of the week can be chosen freely by the user.

(13) Year counter

The year counter is a Mod 100 counter (two Mod 10 counters.)
It can be used for either the Japanese calendar (Showa era) or the Western calendar.

(14) State of the RP5C01 and RP5C15 at switch-on

None of the bit-values of either the RP5C01 or the RP5C15 are fixed at switch-on. They should therefore be initialized by software. Particular care should be taken to set the Test Register to 0 as mentioned in (11) above. If the RP5C01 or RP5C15 are properly backed up, none of their data will be destroyed.

(15) Adjustment function

The RP5C01 has an ADJUST terminal and can be adjusted directly as shown in Fig. 15-1, but in the case of the RP5C15, the adjustment function is effected by an internal register. Commands must therefore be written to this register from the CPU. Fig. 15-2 shows an example of adjusting the RP5C15 using the CPU interrupt.

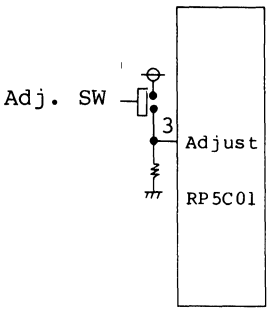


Fig. 15-1 Connection of adjust terminal of RP5C01

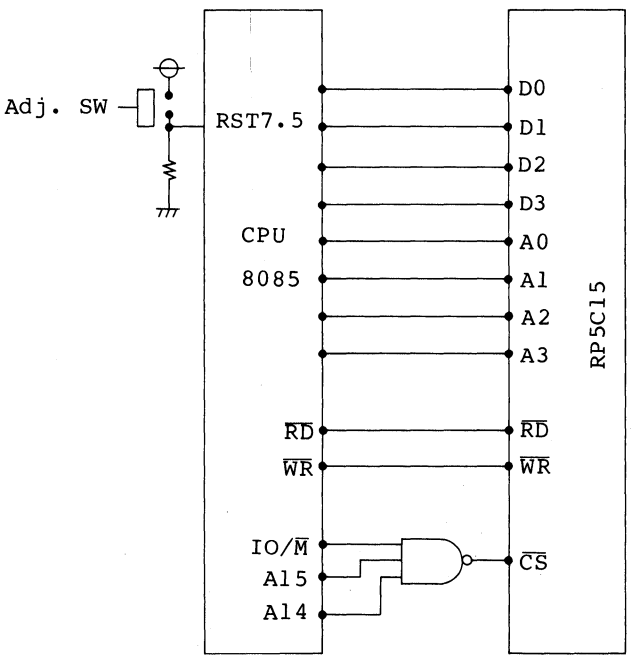
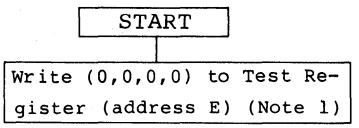


Fig. 15-2 Example of connection of adjust terminal of RP5C15 (with CPU8085)

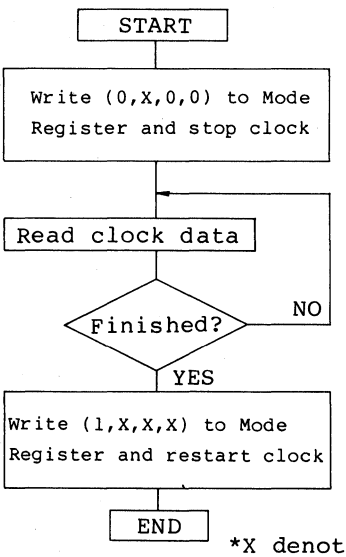
(16) Flowchart

(16-1) When system power is switched on



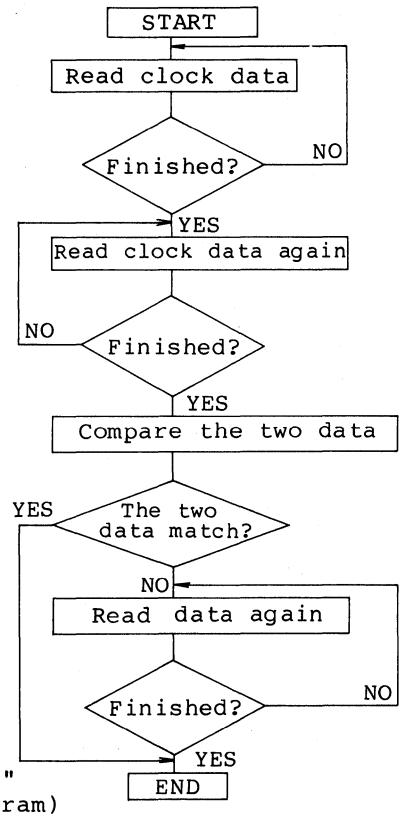
(16-2) Read clock data

(16-2-1) When stopping clock to read data (Note 2)



*X denotes "1" or "0" (determined by program)

(16-2-2) When reading clock data twice (Note 3)



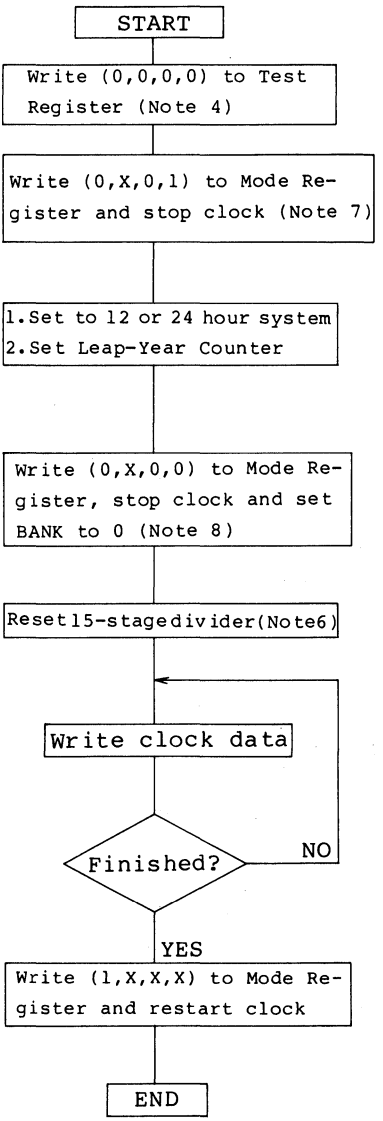
(Note 1) The above flowchart applies to the RP5C15 when used with any CPU. When the RP5C01 is used with a CPU that does not satisfy the AC characteristics tWDL(max.) = 40 nsec., however, the Test Register should be cleared whenever the clock data is rewritten. (Refer to 16-3.)

(Note 2) When a power failure is detected, the clock should be started immediately.

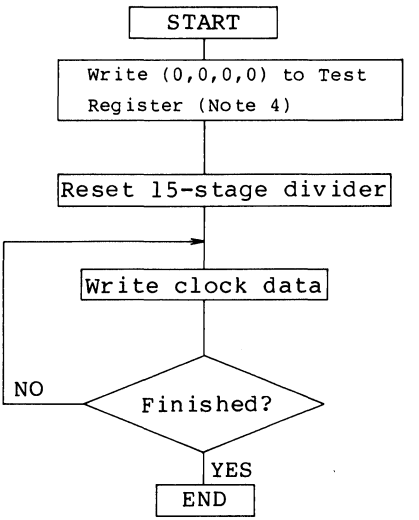
(Note 3) When reading out the clock data twice, there is a possibility of incorrect data being read out only when the seconds count is '9'. There is no possibility of this when the seconds count is other than '9', so it is not necessary to read the clock data twice.

(16-3) Writing clock data

(16-3-1) When stopping clock to write data



(16-3-2) When writing data without stopping clock (Note 5)



(Note 4) This step is unnecessary if 0 is written to the Test Register when the power is switched on.

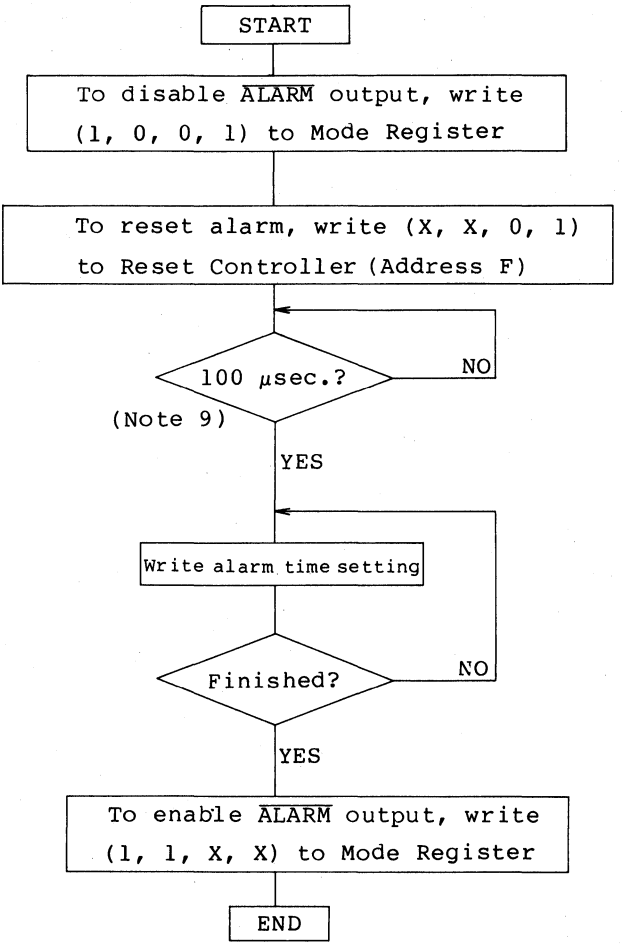
(Note 5) When clock data is written without stopping the clock, the writing operation must be completed within 1 sec. including any time for which the power is shut off, and must be set to the 12/24 hour system and Leap-Year Counter.

(Note 6) Write '1' to bit 1 of address F so that the 15-stage dividers are reset.

(Note 7) (0,X,0,1) applies to the RP5C01 only. For the RP5C15, read (0,X,X,1).

(Note 8) BANK 0 applies to the RP5C15, MODE 00 to the RP5C01.

(16-4) Setting alarm



(Note 9) The 100 μsec. wait time is necessary with the RP5C15 only, not with the RP5C01 (See pages 56 and 57).

(Note 10) When using the RP5C01 with a CPU which does not satisfy the AC characteristic tWDL = max. 40 nsec., special care must be taken when writing to addresses D, E, and F. The sales department of Ricoh should be consulted for technical advice in this case.

(17) Items to check after program preparation

(17-1) When the clock only is to be used (not the alarm)

(a) Has the hour counter been set to either the 12-hour or the 24-hour system? (Address A of Bank 1)
(b) Has the Leap-Year Counter been set? (Address B of Bank 1)
(c) Has (0,0,0,0) been written to the Test Register? (Address E)

Note: "Bank 1" is used in the RP5C15 and "Mode 01" in the RP5C01.

(17-2) When using the alarm

(a) Was the Alarm F/F reset before writing data to the Alarm Register (bit 0 of address F)?
(b) Was the alarm disabled before being reset (bit 2 of address D)?
(c) Is there a wait time of at least 100 μsec. between resetting the Alarm F/F and writing data to the Alarm Register? (only needed with the RP5C15.)

(18) Malfunction during testing

(18-1) Clock data advances extremely fast.

Possible causes:

(1) 0H has not been written to the Test Register -- see Section 11.

(2) The clock is oscillating incorrectly -- see Section 3.

Check point:

Output a standard clock signal from the $\overline{\text{ALARM}}$ terminal (in the case of the RP5C01 and RP5C15) or CKOUT terminal (in the case of the RP5C15) and check whether or not the clock is oscillating correctly. For the RP5C01, the bypass condenser set between pin 17 and GND is sometimes effective for external noise. Its value should be less than 60 PFr according to the measurements carried out by Ricoh.

(18-2) The hour counter goes past 52 and up to 60.

Possible cause:

(1) The 12/24 Register has not been set when data is written. This fault occurs because the clock is set to the 12-hour system when the power is switched on, and hour data from 12 ~ 23 is written into the hour counter.
-- See Section 17.

Check point:

Check whether the clock has been set to the 12 or 24 hour system.

(18-3) The alarm does not function correctly.

Possible cause:

(1) The alarm has not been reset.
-- See Section 9.

Check point:

Check whether the alarm is being reset before data is written into the Alarm Register.

(18-4) The $\overline{\text{ALARM}}$ terminal remains at low.

Possible causes:

(1) The pull-up resistor is not properly connected.
-- See Section 9.

(2) The alarm is being reset internally when the power switched on (when not in the battery back-up mode), and the Alarm EN F/F is also being enabled, causing the $\overline{\text{ALARM}}$ terminal to go low. -- See Section 9.

Check points:

(1) Check the pull-up resistor.

(2) If the alarm is being used, write data into the Alarm Register. If the alarm is not being used, the Alarm EN F/F should be disabled.

(19) Power supply

(19-1) Battery backup

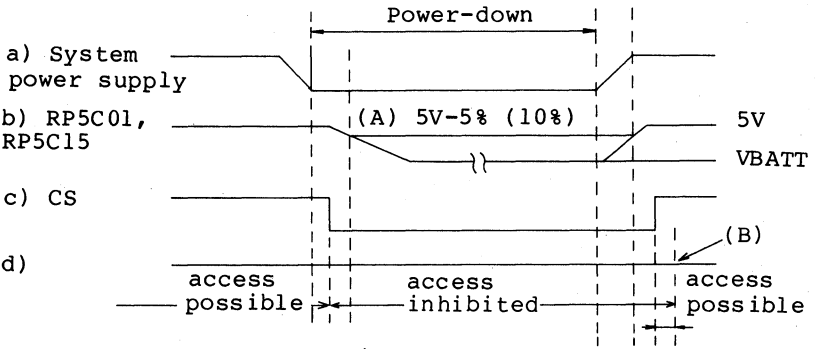


Fig. (19-1)

(Note) VBATT means battery backup voltage and tAC is one of AC electrical characteristics.

With both the RP5C01 and the RP5C15, the time taken for the power supply Vcc to rise or fall depends mainly on the relative timing of the power-down signal CS and Vcc. It therefore depends strongly on the structure of the power-down detection circuit. If, for example, either the RP5C01 or RP5C15 is being used with Vcc $\pm$ 5% (10%) as the standard, CS must go low by the time Vcc crosses point (A) of Fig. 19-1, and high after the time Vcc crosses point (B). In other words, the rise time of Vcc must be set so that the output of CS can satisfy these conditions. As long as this is done, there are no other particular restriction on the rise and fall of Vcc.

However, so as to keep within the usual limits for CMOS-ICs, the input voltage to all terminals, VIN, should always satisfy the following relation:

$$VIN \leqq Vcc + 0.3$$

When constructing the circuit, the timing shown in Fig. 19-1 ca be achieved by suitable selection of the capacitance of the bypass condenser shown in Fig. 19-2.

The best way of simplifying the circuit for generating CS is usually to make the decay time of Vcc long and the rise time short.

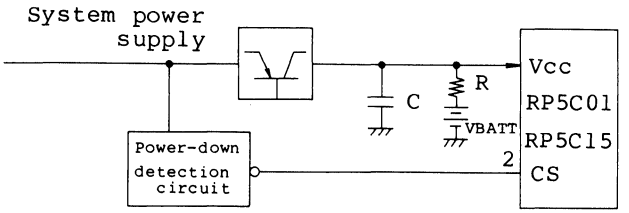


Fig. 19-2

It is also important to ensure that no voltage exceeding Vcc + 0.3V is applied to any of the terminals of the RP5C01 or RP5C15, especially while Vcc is going positive or negative as the switch is turned on. It is therefore recommended that the RP5C01 or RP5C15 be accessed via a CMOS driver, open-collector buffer or open-drain buffer using a common power supply for Vcc.

(20) Differences between RP5C01 and RP5C15

The design of the RP5C15 is based on that of the RP5C01, but the following differences exist:

(a) The RP5C15 has no 26 x 4-bit RAM
(b) Pin 3 is the ADJUST input terminal in the case of the RP5C01, but the CKOUT output terminal in the case of the RP5C15. The adjustment function is carried out by an internal register in the case of the RP5C15.
(c) It is necessary to pull up or pull down the address bus and other input terminals and the data bus and other output terminals in the case of the RP5C01, but not in the case of the RP5C15.
(d) A 100kΩ resistor is needed for the OSCOUT terminal of the oscillation circuit in the RP5C01, but not in the RP5C15.
(e) The definition of the AC characteristic tAC is different for the two clocks. In the RP5C01, it is defined as the time between address valid and the trailing edge of $CS \cdot \overline{CS} \cdot \overline{RD}/\overline{WR}$, while in the RP5C15, it is defined as the time from CS = high, $\overline{CS}$ = low and address valid to the trailing edge of $CS \cdot \overline{CS} \cdot \overline{RD}/\overline{WR}$. (See Section 5).

Compatibility of RP5C01 and RP5C15

The RP5C01 and RP5C15 were designed to be compatible in terms of both software and hardware. If an RP5C15 currently in use satisfies the following conditions, it can be replaced by an RP5C15 without modifications.

(1) The RAM is not being used.
(2) The adjustment function is not being used.
(3) The alarm function is not being used. However, if the $\overline{\text{ALARM}}$ terminal (pin 15) is being used to output a 1Hz or 16Hz clock signal only, then satisfying conditions (1), (2) and (4) is sufficient to guarantee software and hardware compatibility.
(4) The AC characteristic tAC of the RP5C15 is satisfied.

The reason why the alarm functions of the RP5C01 and RP5C15 are not compatible is as follows:

(a) The RP5C01 allows data to be written to the Alarm Register immediately after the alarm has been reset (bit 0 of address F is Alarm Reset F/F).
(b) With the RP5C15, data cannot be written to the Alarm Register for 100 μs after the alarm has been reset (bit 0 of address F). However, if the RP5C01 is programmed so as not to allow data to be written to the Alarm Register for 100 μs after the alarm has been reset, the two clocks will be software-compatible even if the alarm function is used. As stated above, pin 3 is an input terminal for the RP5C01 and an open-drain output terminal for the RP5C15, so if its ADJUST terminal is pulled down (i.e., if the adjustment function is not being used), there will be no problem in replacing an RP5C01 by an RP5C15, even if the open-drain output of the latter is pulled down.

Real Time Clock RP/RF 5C62

Application Manual

Version 1.1

EA-012-8904

Contents

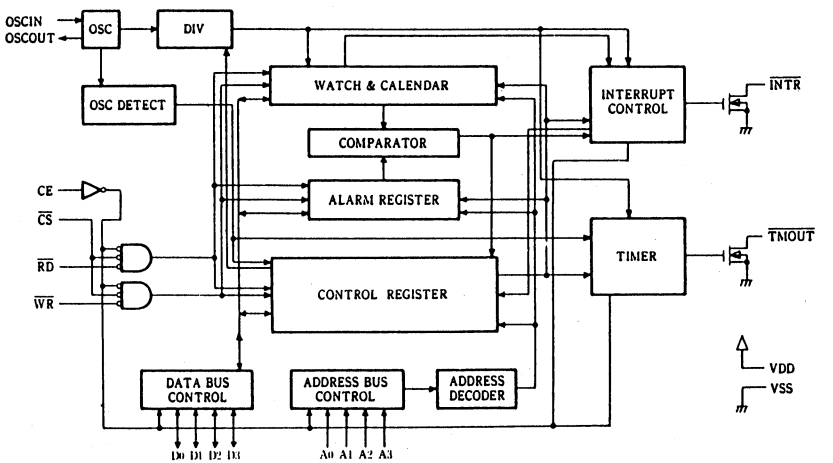
CHAPTER 1 SPECIFICATIONS

RP5C62 and RF5C62 are CMOS real time clock LSIs for microcomputers. RP5C62 and RF5C62 have clock, calendar, and alarm functions. They can be directly connected to the data buses of 8 bit or 16 bit CPUs such as 8086, Z80, 6809, 6502 and 68000. With a built-in timer counter, they can be used as watch-dog-timer or interrupt timer.

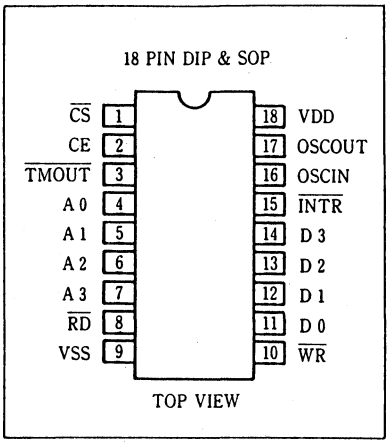
■ FEATURES

- Directly connected to CPU, enabling fast access.
- 4 bit bidirectional data bus, and 4 bit address bus
- The oscillator is driven by a constant voltage, so the oscillation frequency is stable (within ±1 ppm) even when the power supply voltage fluctuates.
- Built-in timer counter using internal clock
- Generates cyclic CPU interrupts, and generates alarm-match interrupts.
- Interrupt flag and interrupt inhibit
- Clock (hour, minute, second), calendar (leap year, year, month, day, day of the week), alarm (hour, minute)
- 12- or 24-hour mode is selectable.
- Recognizes leap years automatically.
- All clock and alarm data expressed in BCD codes
- ±30 seconds adjustment function
- Determines whether clock data is valid or invalid.
- Consumes very low power due to CMOS technology, so it can be backed up by batteries.
- 5V single power supply
- Package: 18-pin DIP for RP5C62, 18-pin SOP for RF5C62.

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Symbol	Name	Function
$\overline{CS}$ CE	Chip select Chip enable input	$\overline{CS}$ and CE are used when interfacing external devices. They may be accessed when $\overline{CS}$ is low and CE is high. CE is connected to a power down detector on the system power supply side, and $\overline{CS}$ is connected to the microcomputer address bus.
$\overline{TMOUT}$	Timer output	Timer output may be used as an interrupt free-run timer or watchdog timer. When CE is low (running on battery backup), operation stops (there is no output). It is N-ch open drain output.
A0~A3	Address input	Address input is connected to the CPU address bus. It is gated internally with CE.
$\overline{RD}$	Read control input	When $\overline{RD}$ is set low, the contents of the counters or registers specified by A0~A3 are output to D0~D3. It is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
$\overline{WR}$	Write control input	When $\overline{WR}$ is low or rises from low to high, the contents of D0~D3 are written to registers or counters specified by A0~A3. $\overline{WR}$ is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
D0~D3	Bi-directional data bus	D0~D3 are connected to the CPU data bus. The input section is gated internally with CE. It is CMOS input/output.
$\overline{INTR}$	Interrupt output	$\overline{INTR}$ outputs timing CLOCK interrupts or alarm match interrupts to CPU. It also operates when CE is low (at battery backup). It is N-ch open drain output.
OSCIN OSCOUT	Oscillator circuit input/output	Crystal oscillator of 32.768 KHz must be connected between OSCIN and OSCOUT. Capacitance is connected externally between VDD and OSCIN and VDD and OSCOUT, forming the oscillator circuit.
VDD VSS	Power supply	VDD connects to +5V and VSS to ground.

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
VDD	Supply Voltage	VSS=0	−0.3 ~ +7.0	V
VI	Input Voltage		−0.3 ~ VDD+0.3	V
VO	Output Voltage		−0.3 ~ VDD+0.3	V
PD	Maximum Power Consumption	TA = 25°C	300	mW
TA	Operating Temperature		−20 ~ +70	°C
TSTG	Storage Temperature		−40 ~ +125	°C

■ RECOMMENDED OPERATING CONDITION

(VSS = 0V, TA = −20 ~ +70°C)

Symbol	Parameter	Condition	MIN.	Typ.	MAX.	Unit
VDD	Supply Voltage			5.0	6.0	V
VCLK	Supply Voltage of Clock		2.0		6.0	V
fXT	Crystal Oscillation Frequency			32.768		kHz

■ DC CHARACTERISTICS

Symbol	Parameter	Pin Name	Condition		MIN.	Typ.	MAX.	Unit
VIH1	"H" input voltage	A0~A3, D0~D3			2.2		VDD+0.3	V
VIL1	"L" input voltage	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$			−0.3		0.8	V
VIH2	"H" input voltage	CE			0.8*VDD		VDD+0.3	V
VIL2	"L" input voltage				−0.3		0.2*VDD	V
VOH1	"H" output voltage	D0~D3	IOH1 = −400μA		2.4			V
VOL1	"L" output voltage		IOL1 = 2mA				0.4	V
VOL2	"L" output voltage	$\overline{INTR}$, $\overline{TMOUT}$	IOL2 = 2mA				0.4	V
IILK	Input leak current	A0~A3, CE, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$	VILK = VDD or VSS		−1		1	μA
IOZ1	Output off leak current	D0~D3	VOZ1 = VDD or VSS		−5		5	μA
IOZ2		$\overline{INTR}$, $\overline{TMOUT}$	VOZ2 = VDD		−2		2	μA
IDD1	Consumption current for back-up	VDD	VDD=2.5V	Input: VDD or VSS			3	μA
IDD2	Consumption current for stand-by	VDD	VDD=5.5V	Output: OPEN			8	μA
∂f	Oscillation frequency drift for voltage drift	OSCIN OSCOUT	VDD=2.5~5.5V Ta=25°C		−1		1	PPM

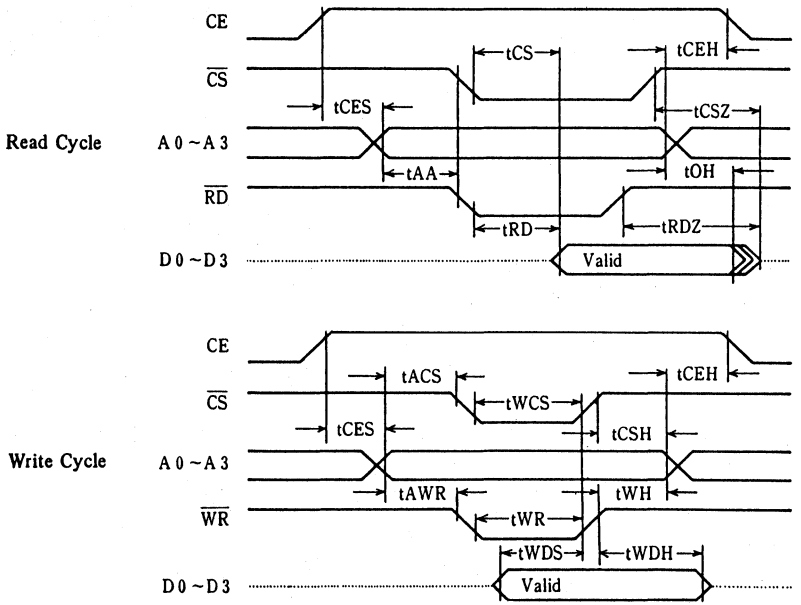
(Unless Noted, VSS = OV, VDD = 5V ± 10%, TA = −20 ~ +70°C,
X'tal = 32.768 kHz (CI ≦ 35 KΩ), CG = 5 pF, CD = 10 pF)

■ AC CHARACTERISTICS

(V_{SS} = 0V, T_A = −20 ~ 70°C, Note1; V_{DD} = 5V ± 10%, Note2; V_{DD} = 3V ± 10%, Note3; V_{DD} = 5V ± 20%)

Symbol	Parameter	Description	Note1	Note2	Note3	Unit
tCES	CE setup time	Time for which CE must be kept "H" before the address is determined.	MIN 500	MIN 1000	MIN 500	nS
tCEH	CE hold time	Time for which CE must be kept "H" until the address finishes changing.	MIN 500	MIN 1000	MIN 500	nS
tAA	Address setup time (RD)	Time for which the address must be determined before $\overline{CS}$ = $\overline{RD}$ = "L".	MIN 20	MIN 20	MIN 20	nS
tCS	$\overline{CS}$ setup time (RD)	Time between the trailing edge of $\overline{CS}$ and data output, after the address is determined and $\overline{RD}$ = "L" (CL = 100 pF).	MAX 120	MAX 295	MAX 150	nS
tRD	$\overline{RD}$ setup time (RD)	Time between the trailing edge of $\overline{RD}$ and data output, after the address is determined and $\overline{CS}$ = "L" (CL = 100 pF)	MAX 120	MAX 295	MAX 150	nS
tOH	Data hold time (RD)	Time for which data does not change though the address changes, when $\overline{CS}$ = $\overline{RD}$ = "L".	MIN 10	MIN 10	MIN 10	nS
tCSZ	$\overline{CS}$ output delay time (RD)	Time between the rising edge of $\overline{CS}$ and the data bus line becoming high impedance.	MAX 70	MAX 95	MAX 75	nS
tRDZ	$\overline{RD}$ output delay time (RD)	Time between the rising edge of $\overline{RD}$ and the data bus line becoming high impedance.	MAX 70	MAX 95	MAX 75	nS
tACS	$\overline{CS}$ setup time (WR)	Time for which the address must be determined before the trailing edge of $\overline{CS}$ while $\overline{WR}$ is "L".	MIN 20	MIN 20	MIN 20	nS
tAWR	$\overline{WR}$ setup time (WR)	Time for which the address must be determined before the trailing edge of $\overline{WR}$ while $\overline{CS}$ is "L".	MIN 20	MIN 20	MIN 20	nS
tWCS	$\overline{CS}$ pulse width (WR)	Pulse width when writing by $\overline{CS}$ while $\overline{WR}$ is "L".	MIN 120	MIN 195	MIN 150	nS
tWR	$\overline{WR}$ pulse width (WR)	Pulse width when writing by $\overline{WR}$ while $\overline{CS}$ is "L".	MIN 120	MIN 195	MIN 150	nS
tWDS	Data setup time (WR)	Time for which the data must be determined before the rising edge of $\overline{CS}$ or $\overline{RD}$.	MIN 60	MIN 95	MIN 75	nS
tCSH	Address $\overline{CS}$ hold time (WR)	Time for which the address needs to be held after the rising edge of $\overline{CS}$.	MIN 10	MIN 10	MIN 10	nS
tWH	Address $\overline{WR}$ hold time (WR)	Time for which the address needs to be held after the rising edge of $\overline{WR}$.	MIN 10	MIN 10	MIN 10	nS
tWDH	Data hold time (WR)	Time for which the data needs to be held after the rising edge of $\overline{CS}$ or $\overline{WR}$.	MIN 10	MIN 10	MIN 10	nS

■ TIMING DIAGRAM

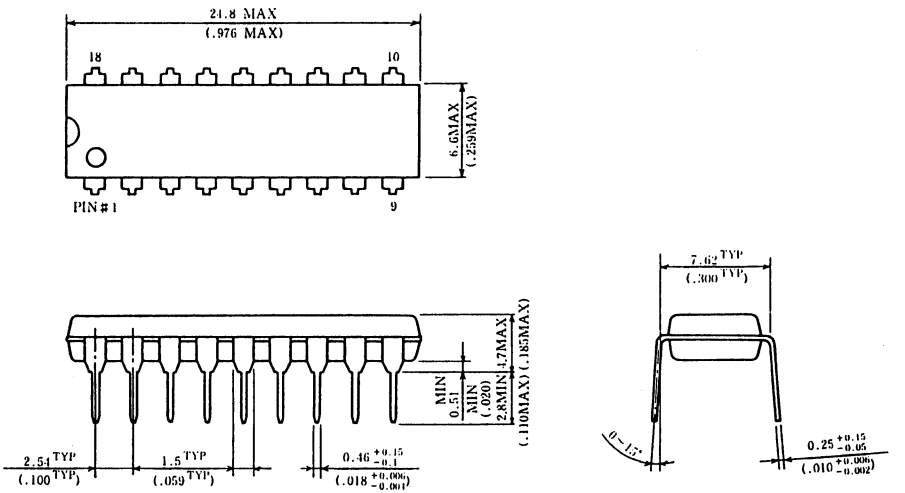


Input/Output Condition

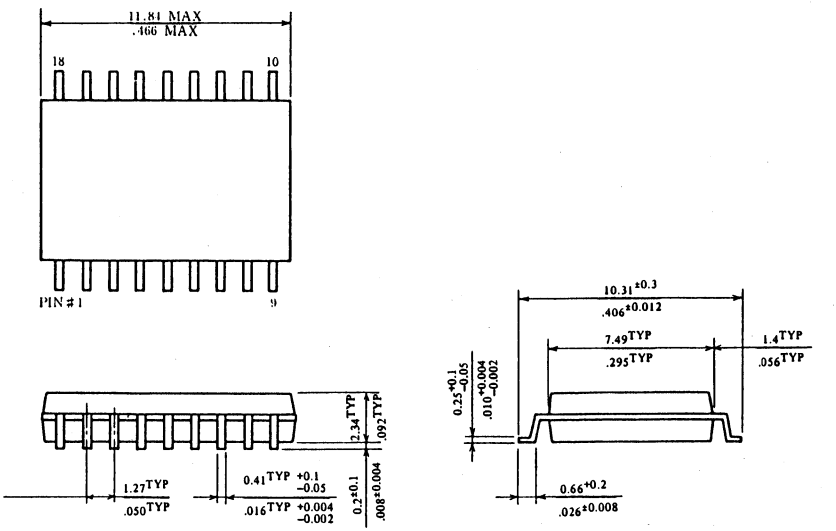
(VDD = 5V ± 10%)	(VDD = 3V ± 10%)	(VDD = 5V ± 20%)
VIH = 2.2V	VIH = 0.8 × VDD	VIH = 2.4V
VIL = 0.8V	VIL = 0.2 × VDD	VIL = 0.4V
VOH ≧ 2.2V	VOH = 0.8 × VDD	VOH ≧ 2.4V
VOL ≦ 0.8V	VOL = 0.2 × VDD	VOL ≦ 0.4V

■ PACKAGE DIMENSION (Unit: mm/inch)

- RP5C62 (18pin DIP)



- RF5C62 (18pin SOP)



■ FUNCTIONAL DESCRIPTION

1. Addressing

	Address Bus				BANK 0 (BANK = 0)						BANK 1 (BANK = 1)				
	A3	A2	A1	A0	Description		D3	D2	D1	D0	Description		D3	D2	D1	D0
0	0	0	0	0	Second Counter	R/W	S_8	S_4	S_2	S_1	Cyclic interrupt select Reg.	W/O	CT_3	CT_2	CT_1	CT_0
1	0	0	0	1	10 sec.	↑		S_{40}	S_{20}	S_{10}	Adjust Reg.	W/O				ADJ
2	0	0	1	0	1 min.	↑	M_8	M_4	M_2	M_1	Alarm 1 min. Reg.	R/W	AM_8	AM_4	AM_2	AM_1
3	0	0	1	1	10 min.	↑		M_{40}	M_{20}	M_{10}	↑ 10 min.	↑		AM_{40}	AM_{20}	AM_{10}
4	0	1	0	0	1 hour	↑	H_8	H_4	H_2	H_1	↑ 1 hour	↑	AH_8	AH_4	AH_2	AH_1
5	0	1	0	1	10 hour	↑			P/$\overline{A}$ or H_{20}	H_{10}	↑ 10 hour	↑			AP/$\overline{A}$ or AH_{20}	AH_{10}
6	0	1	1	0	day of week	↑		W_4	W_2	W_1						
7	0	1	1	1	1 day	↑	D_8	D_4	D_2	D_1						
8	1	0	0	0	10 day	↑			D_{20}	D_{10}						
9	1	0	0	1	1 month	↑	MO_8	MO_4	MO_2	MO_1						
A	1	0	1	0	10 month	↑				MO_{10}	$\overline{12}$/24 select Reg.	W/O				$\overline{12}$/24
B	1	0	1	1	1 year	↑	Y_8	Y_4	Y_2	Y_1	Leap Year Reg.	R/O R/W		$\overline{LYE}$	LY_1	LY_0
C	1	1	0	0	10 year	↑	Y_{80}	Y_{40}	Y_{20}	Y_{10}	Timer Clock Select Reg.	W/O R/O	TM_3 TM_3	TM_2	TM_1	TM_0 TMFG
D	1	1	0	1	Control Reg. 1	W/O	WTEN	ALEN	TMR	BANK	Control Reg. 1	W/O	WTEN	ALEN	TMR	BANK
E	1	1	1	0	Control Reg. 2	R/O R/W	BSY	CTFG	ALFG	XSTP	Control Reg. 2	R/O R/W	BSY	CTFG	ALFG	XSTP
F	1	1	1	1	Control Reg. 3	W/O	$\overline{TSTA}$	$\overline{TSTB}$	WTRST		Control Reg. 3	W/O	$\overline{TSTA}$	$\overline{TSTB}$	WTRST	

Note 1) R/W bits can be read and written. R/O bits can only be read. W/O bits can only be written.
Note 2) It is no problem to attempt writing to R/O bits and don't care bits, but the attempt will fail.
Note 3) If W/O bits and don't care bits are read, the returned value is 0.

2. Counter/register functions

1) Clock and calendar counter (addresses 0 to C of BANK 0) (read and write)

- The clock is in units of hour, minute, and second. The calendar function includes year, month, day and day of the week.
- Data is expressed in BCD codes.
- 12- or 24-hour time display is selectable for clock output. The display in the hour counter is as follows:

  12-hour display: AM12→AM1→···→AM11→PM12→PM1→···→PM11→AM12
  (The P/$\overline{A}$ bit indicates AM when 0 and PM when 1.)

  24-hour display: 0→···→23→0
- Write to the hour counter after selecting 12- or 24-hour time display by the 12/24 select register.
- The day-of-week counter is a septinary counter, and is incremented when carried to the day counter.
  (Count $W_4 \cdot W_2 \cdot W_1 = 000 \rightarrow 001 \rightarrow 010 \rightarrow \cdots \rightarrow 110 \rightarrow 000$)

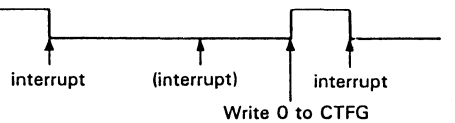
Note 1) DO NOT write values which are not valid (such as AM15, or February 30). This causes misoperation.

2) Cyclic interrupt select register (BANK 1 address 0) (write only)

- Selects the cycle for cyclic interrupt based on the $\overline{INTR}$ output and the output mode.

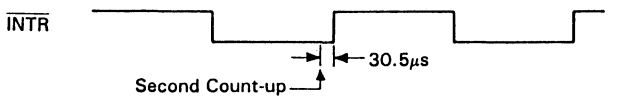
CT_3	CT_2	CT_1	CT_0	$\overline{INTR}$	Description
*	0	0	0	"OFF"	Inhibit cyclic interrupt
*	0	0	1	2048 Hz	Cycle T 0.488 ms (2048 Hz)
*	0	1	0	1024 Hz	↑ 0.977 ms (1024 Hz)
*	0	1	1	128 Hz	↑ 7.813 ms (128 Hz)
*	1	0	0	16 Hz	↑ 62.5 ms (16 Hz)
*	1	0	1	1 Hz	↑ 1 s (1 Hz)
*	1	1	0	1/60 Hz	↑ 60 s (1/60 Hz)
*	1	1	1	"ON"	$\overline{INTR}$ Output = "L"
0	*	*	*	Pulse mode	Cyclic pulse duty 50%
1	*	*	*	Level mode	Note 1)

Note 1) $\overline{INTR}$

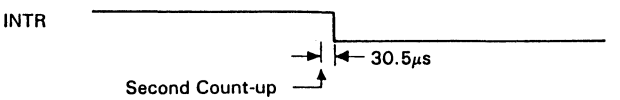


Note 2) $\overline{INTR}$ and Second Count-up

①pulse mode (1 Hz or 1/60 Hz select)



②level mode (1 Hz or1/60 Hz select)



3) Adjustment register (BANK 1 address 1) (write only)

- The adjustment register is for correcting seconds of clock and calendar counters. The second is adjusted by writing 1 to the ADJ bit.
  (a) When the second is 00 to 29: Makes the second counter 00, and does not carry to the minutes counter.
  (b) When the second is 30 to 59: Makes the second counter 00, and carries to the minutes counter.
- It takes 122.1 μs at most to complete the adjustment after writing 1 to the ADJ bit. The BSY bit of the control register 2 is set to 1 until adjustment is completed. During that time, do not write to or read from the clock or calendar counter.

4) Alarm register (BANK 1 addresses 2 to 5) (read and write)
- This register stores hours and minutes for the alarm.
- Data is expressed in BCD codes.
  (DO NOT write invalid values such as AM15. This causes misoperation.)

5) $\overline{12}$/24 select register (BANK 1 address A) (write only)
- When the $\overline{12}$/24 bit of the $\overline{12}$/24 select register is 1, the 12-hour time display selected. If it is 0, the 24-hour time display is selected.
- Set the 12- or 24-hour time display before adjusting the clock or setting the alarm.

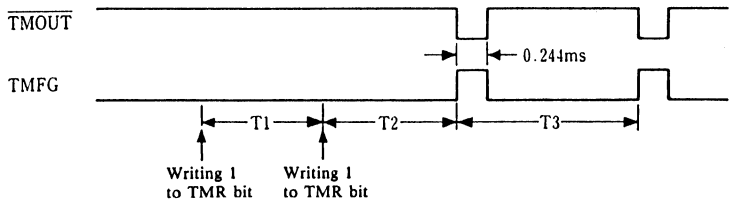
6) Leap year register (BANK 1 address B) (write and read)
- This register indicates leap years. When $LY_1 = LY_0 = 0$, it is a leap year. (LY_1 and LY_0 are read only.)
  Every time the year counter is incremented, LY_1 and LY_0 change as follows: 00→01→10→11→00.
- Setting the year counter automatically sets the leap year register. (A leap year is set when 84, 88, ··· and 00 are set to the year counter.)
- The $\overline{LYE}$ bit can be written to. It performs leap year operation when set to 0, and does not when set to 1. Writing to the year counter sets the $\overline{LYE}$ bit to 0.

7) Timer clock select register (BANK 1 address C) (write and read)
- Selects the input clock for the timer counter (in the write mode).

TM_3	TM_2	TM_1	TM_0	T1 Note 1)	T2 Note 2)	T3 Note 3)
0	*	*	*	Timer Inhibit Note 5) ($\overline{TMOUT}$ = OFF)	←	←
1	0	0	0	562 ms	562 ~ 626 ms	625 ms
1	0	0	1	281 ms	281 ~ 313 ms	312.5 ms
1	0	1	0	140 ms	140 ~ 157 ms	156.3 ms
1	0	1	1	70.3 ms	70.3 ~ 78.2 ms	78.13 ms
1	1	0	0	35.1 ms	35.1 ~ 39.1 ms	39.06 ms
1	1	0	1	17.5 ms	17.5 ~ 19.6 ms	19.53 ms
1	1	1	0	8.78 ms	8.78 ~ 9.77 ms	9.766 ms
1	1	1	1	4.39 ms	4.39 ~ 4.89 ms	4.833 ms

Note 1) The maximum time for the reset cycle (maximum reset cycle when used as a watch-dog timer) not to output L from the $\overline{TMOUT}$ output after resetting the timer counter (writing 1 to the TMR bit of the control register 1).
Note 2) Time between the timer counter reset and the "L" pulse output from the $\overline{TMOUT}$ output.
Note 3) The cycle of a pulse output from the $\overline{TMOUT}$ output when the timer counter is not reset (That is, when used as a free-run timer. However, the time between the timer counter reset and the first pulse output from the $\overline{TMOUT}$ output is T2. The cycle for the second and subsequent pulses is T3).
Note 4) When CE = "L" (battery backup), the timer stops ($\overline{TMOUT}$ output = OFF).
Note 5) When oscillation stop is detected (XSTP bit = 1), the TM_3 bit is reset to 0 and the timer is inhibited ($\overline{TMOUT}$ output = OFF).
Note 6) When TM_3 bit = 0, the timer counter is reset.

• When the $\overline{\text{TMOUT}}$ output is "L", the TMFG bit is "H" (in read mode).



8) Control register 1 (address D of BANK 0 or 1) (write only)

• Correspondence with data buses

D3	D2	D1	D0
WTEN	ALEN	TMR	BANK

①WTEN bit ..... When the WTEN bit is 1, clock counting is valid. When it is 0, clock counting is disabled (carrying of seconds is inhibited). This bit is also used when reading the time. (To read time, this bit is set to 0, then returned to 1 after reading. If a carry pulse is input to the seconds' counter while WTEN = 0, the seconds' counter is incremented by only +1 for compensation when WTEN bit is returned to 1. Only one carry is compensated correctly by +1. Even when there are two carries, only one carry is compensated.) When the CE input terminal is "L", this bit is set to 1.

②ALEN bit ..... When the ALEN bit is 1, the $\overline{\text{INTR}}$ output becomes "L" if the specified alarm time and the actual time match (alarm match operation). When this bit is 0, the alarm match operation is disabled.

③TMR bit ..... Writing 1 to this bit resets the timer counter. This bit is used for watch-dog timers.

④BANK bit ..... The BANK bit is for switching the address banks. When this bit is set to 0, BANK 0 is selected. When set to 1, BANK 1 is selected.

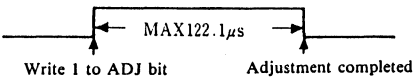
9) Control register 2 (address E of BANK 0 or 1) (read, partially write)

- Correspondence with data buses

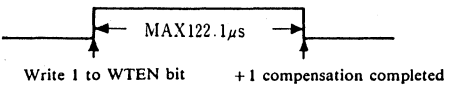
D3	D2	D1	D0
BSY	CTFG	ALFG	XSTP

①BSY bit ..... When the BSY bit is 1, DO NOT read or write the time or calendar. The BSY bit is read only.
This bit is set to 1 in the following cases:

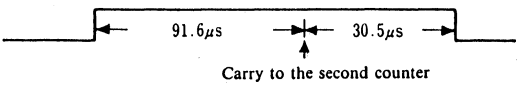
(i) ±30 second adjustment



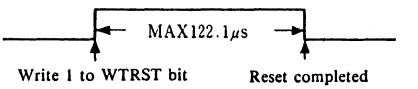
(ii) +1 compensation
(When one second is carried for compensation when returning WTEN from 0 to 1.)



(iii) Normal one second carry

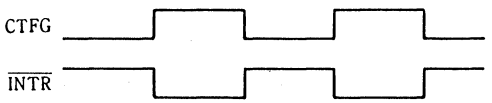


(iv) WTRST
(Resetting the 8 Hz to 1 Hz dividers)

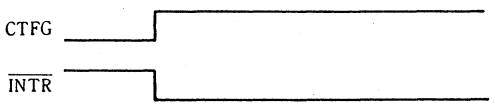


②CTFG bit .....The CTFG bit is set to 1 when cyclic interrupts occur (INTR = "L"). The CTFG can be read. Only 0 can be written to it. A value of 1 cannot be written to it.

When CT_3 bit = 0
(pulse mode)

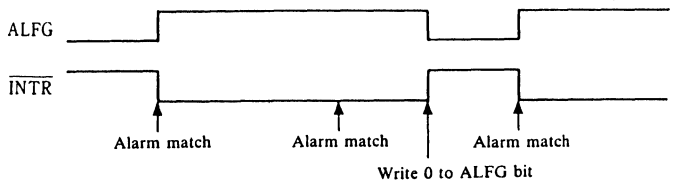


When CT_3 bit = 1
(level mode)



When CT_3 = 1 (level mode), writing 0 to this bit makes the $\overline{INTR}$ output "OFF" (in pulse mode, a write is not possible).

③ALFG bit ..... The ALFG bit is set to 1 when there is an alarm match interrupt ($\overline{INTR}$ = "L"). The ALFG can be read. Only 0 can be written to it. 1 cannot be written to it.



When ALFG = 1, writing 0 to this bit makes the $\overline{INTR}$ output "OFF".

④XSTP bit ..... The XSTP bit is an oscillator stop detection bit, and is set to 1 once oscillation stops. This value is maintained even after oscillation restarts. When power is initially applied, this bit is set to 1 before oscillation starts. This bit can be used for determining whether the clock or alarm data is valid. The XSTP bit can be read. Only 0 can be written to it. A value of 1 cannot be written to it. When an oscillation stop is detected, the TM_3 bit of the timer clock select register is reset to 0, and the timer is inhibited ($\overline{TMOUT}$ output = OFF).

10) Control register 3 (Address F of BANK 0 or 1) (write only)

- Correspondence with data buses

D3	D2	D1	D0
$\overline{TSTA}$	$\overline{TSTB}$	WTRST	

①$\overline{TSTA}$ bit ..... The TSTA bit is a test bit. Writing 0 to this bit sets the test mode. Set this bit to 1 at initialization. This bit is set to 1 when CE = "L".

②$\overline{TSTB}$ bit ..... The TSTB bit is a test bit. Writing 0 to this bit sets the test mode. Set this bit to 1 at initialization. This bit is set to 1 when CE = "L".

③WTRST bit ..... Writing 1 to the WTRST bit resets 8 Hz to 1 Hz dividers. The reset is released and counting starts a maximum of 122.1 μs after 1 is written to this bit. This bit is used to adjust the values of the seconds and lower counter.

CHAPTER 2 DATA SHEET

1. OSCILLATOR

1) Oscillator circuit

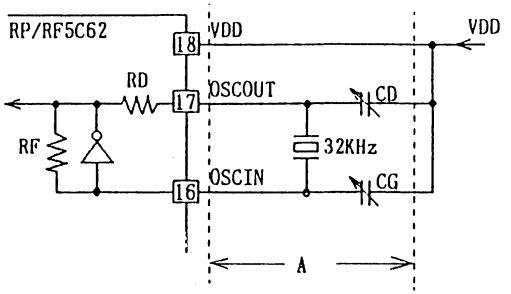


Figure 1

Recommended crystal oscillator is:
32768 Hz CI value ≦ 35 kΩ
Recommended working ranges of CG and CD are:
CG: 5 pF to 35 pF
CD: 5 pF to 35 pF
RF: Typical 8 MΩ built in
RD: Typical 250 kΩ built in

The oscillation circuit for 5C62 can be made up from a 32 kHz crystal oscillator and two capacitors externally attached as shown in Figure 1. The 5C62 has a feedback resistor (RF), a stabilizing resistor (RD), and an inverter built in.
A crystal oscillator with CI (series resistance) value equal to or smaller than 35 kΩ is recommended. To fine-adjust the oscillation frequency, use either CG or CD as a trimmer capacitor. The oscillator circuit of the IC is driven by a constant voltage circuit using VDD as reference, so connect one side of the oscillation capacitor to VDD, not to VSS.

2) Note in design using the oscillator circuit

To design a PC board around the oscillator, consider the following:

(a) Locate the crystal, CG, and CD as close to the IC as possible.
(b) DO NOT route a signal line or power line near the oscillator (especially near segment A in Figure 1).
(c) Raise the impedance between the OSCIN and OSCOUT terminals and the PC board sufficiently.
(d) DO NOT route OSCIN and OSCOUT in parallel or with long conductor runs.
(e) When there is a possibility of condensation on the PC board due to changes in the environment, it is recommended to coat the soldered part of pins 16 and 17, crystal oscillator, CG, and CD on the PC board and the routing of OSCIN and OSCOUT with dampproofing materials. This is because condensation often stops the oscillation. When the oscillation stops, the oscillation detection flag is set and the timer is disabled at the same time. So, to use the functions of the oscillation detection flag or the timer, take precautions to prevent oscillation from stopping due to condensation.

3) Measurement of oscillation frequency

To check the frequency of the crystal oscillation, set the internal registers as indicated below. Use a frequency counter to measure the clock output from the $\overline{\text{INTR}}$ terminal. DO NOT attach a probe directly to the OSCIN or OSCOUT terminal; the C_G and C_D values change after a probe is attached, affecting the oscillation frequency, so it cannot be measured correctly.

Control register 1 ← (1)H	ALEN bit is 0, BANK bit is 1.
Control register 3 ← (C)H	$\overline{\text{TSTA}}$ and $\overline{\text{TSTB}}$ bits are 1.
Control register 2 ← (0)H	CTFG and ALFG bits are 0.
Cyclic interrupt select register ← (1)H	CT_3, CT_2, and CT_1 bits are 0, and CT_0 bit is 1.

To write to a register, set the CE terminal to H. After the above processing, a 2048 Hz clock signal is output from the $\overline{\text{INTR}}$ terminal (which must be pulled up to VDD with a resistor). (To measure the frequency in a precision of about 1 ppm, use a frequency counter with a six to seven digit display.)

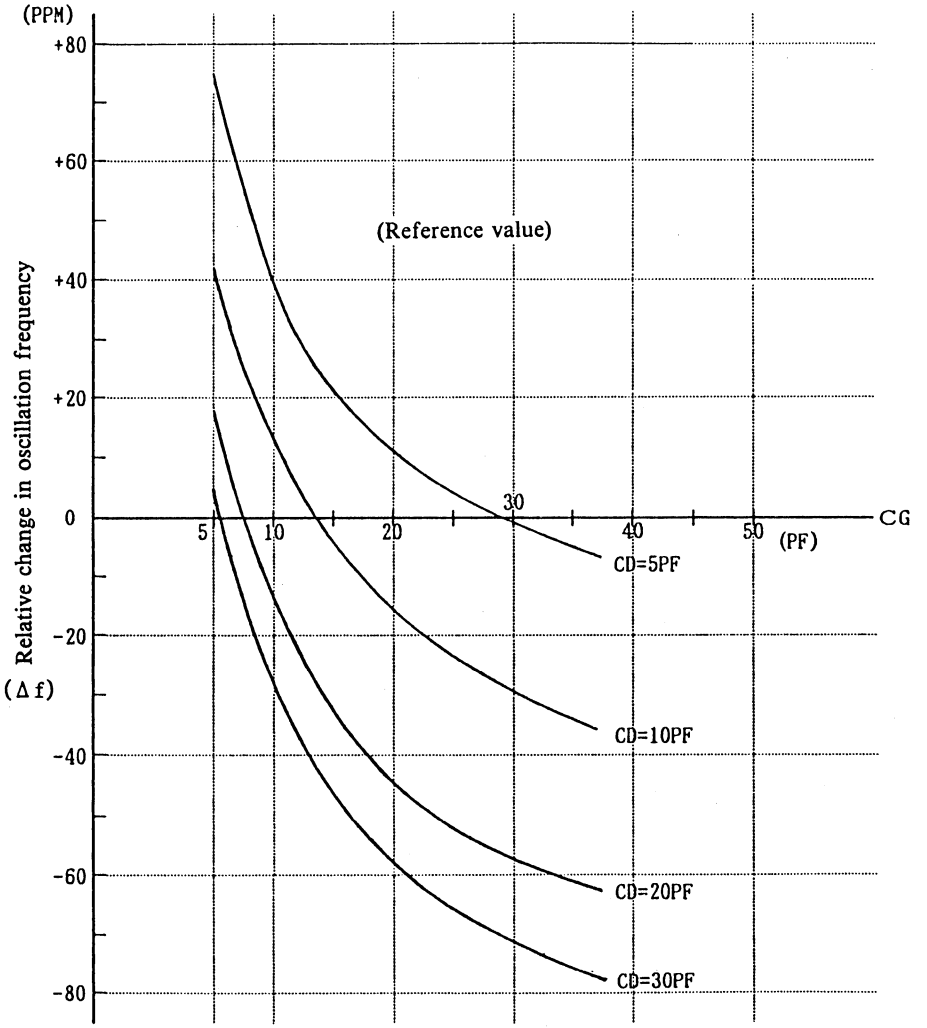
4) Fluctuation in oscillation frequency

After mounting the crystal oscillator, the crystal oscillation frequency fluctuates according to the externally attached oscillation circuit capacity (C_G, C_D), power supply voltage, and changes in the ambient temperature. Figures 2 to 5 show examples of these typical characteristics.

Figure 2 Typical oscillation frequency characteristics when C_D is fixed and C_G is varied
Figure 3 Typical oscillation frequency characteristics when C_G is fixed and C_D is varied
Figure 4 Typical oscillation frequency characteristics when VDD is changed
Figure 5 Typical oscillation frequency characteristics when the ambient temperature is changed

Note) Figures 2 to 5 do not indicate absolute deviation of oscillation frequency (that is, precision); they indicate relative deviation from a certain base point.

Figure 2 Typical oscillation frequency characteristics VS C_G



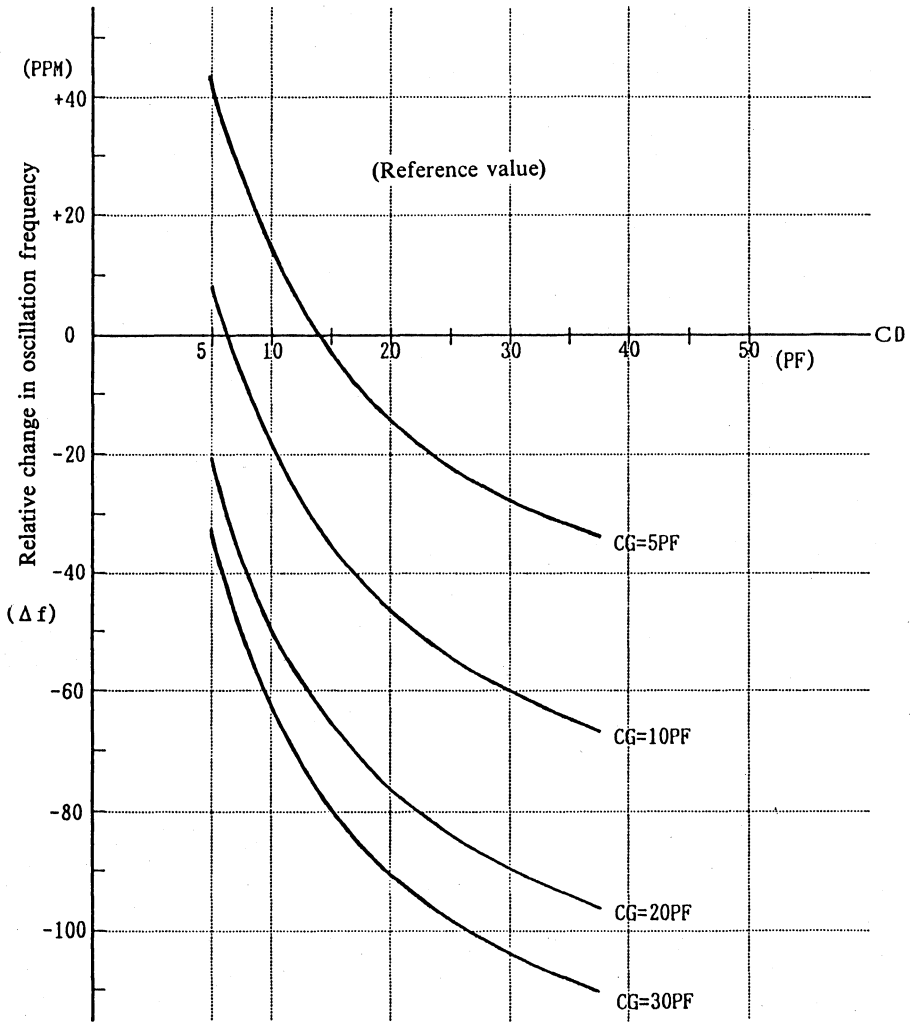
Notes) 1. VDD = 3V, TA = 25°C, measured with crystal oscillator type KF-38G, manufactured by Kyocera

2. The relative change in oscillation frequency (ppm) is expressed by Δf. Δf is the amount of change relative to the oscillation frequency at $C_G = 14$ pF, which is the middle value of the recommended operation range of C_G (5 to 35 pF) when $C_D = 10$ pF.

$$\Delta f = \frac{\text{fosc } (C_G, C_D) - \text{fosc } (C_G = 14 \text{ pF}, C_D = 10 \text{ pF})}{\text{fosc } (C_G = 14 \text{ pF}, C_D = 10 \text{ pF})} \times 10^6 \text{ (PPM)}$$

3. The absolute deviation of the oscillation frequency depends on the frequency deviation of the crystal oscillator. Use the above figure as a reference for the relative changes by C_G.

Figure 3 Typical oscillation frequency characteristics VS C_D



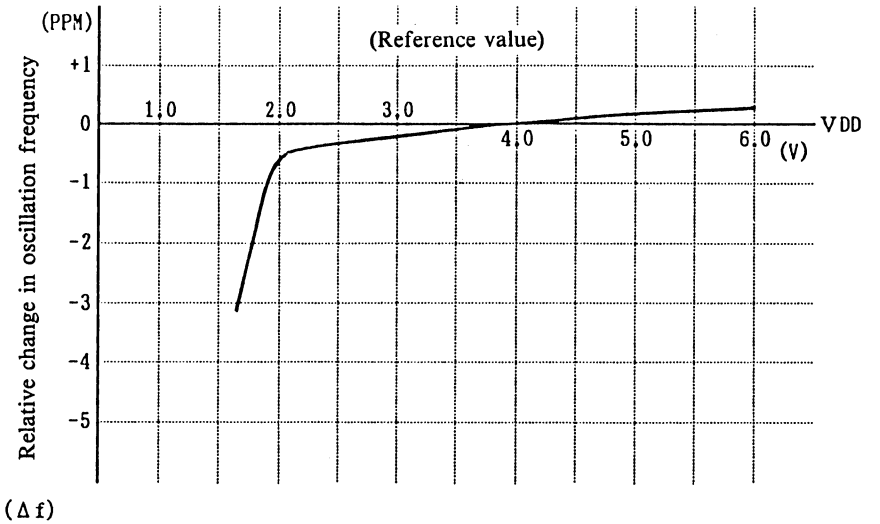
Notes) 1. VDD = 3V, TA = 25°C, measured with crystal oscillator type KF-38G, manufactured by Kyocera

2. The relative change in oscillation frequency (ppm) is expressed by Δf. Δf is the amount of change relative to the oscillation frequency at $C_D = 14$ pF, which is the middle value of the recommended operation range of C_D (5 to 35 pF) when $C_G = 5$ pF.

$$\Delta f = \frac{\text{fosc } (C_G, C_D) - \text{fosc } (C_G = 5 \text{ pF}, C_D = 14 \text{ pF})}{\text{fosc } (C_G = 5 \text{ pF}, C_D = 14 \text{ pF})} \times 10^6 \text{ (PPM)}$$

3. The absolute deviation of the oscillation frequency depends on the frequency deviation of the crystal oscillator. Use the above figure as a reference for the relative changes by C_D.

Figure 4 Typical oscillation frequency characteristics VS VDD



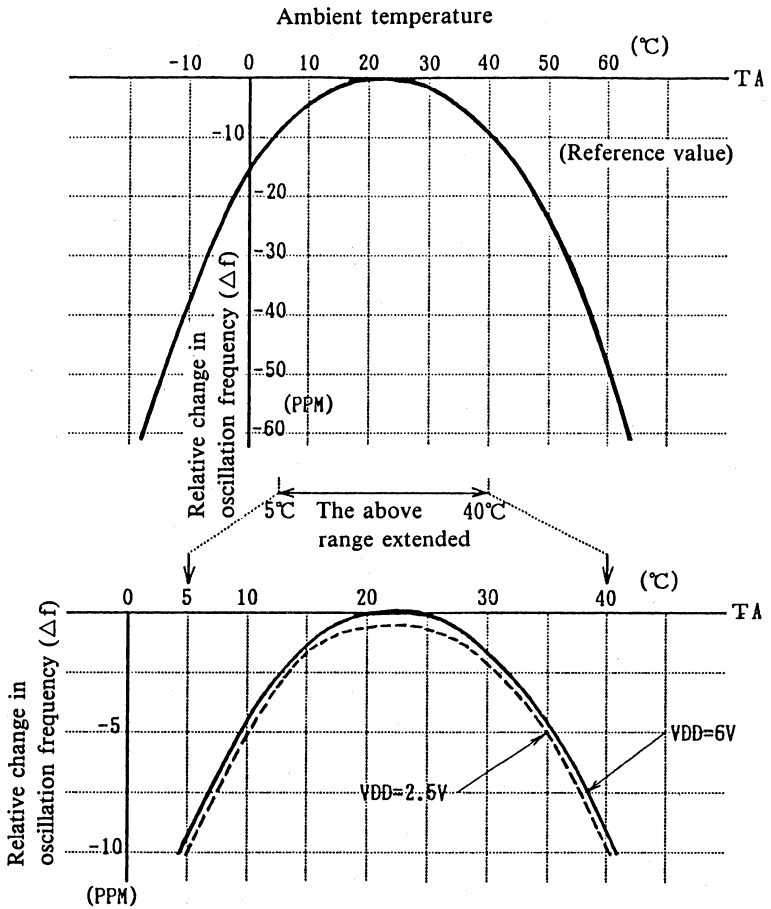
Notes) 1. TA = 25°C, C_G = 5 pF, C_D = 10 pF, measured with crystal oscillator KF-38G, manufactured by Kyocera

2. The amount of relative change in oscillation frequency (ppm) is expressed by Δf. Δf is the amount of change relative to the oscillation frequency at VDD = 4V.

$$\Delta f = \frac{\text{fosc (VDD)} - \text{fosc (VDD = 4V)}}{\text{fosc (VDD = 4V)}} \times 10^6 \text{ (PPM)}$$

3. The relative change amount is rather large around 2V, because the oscillation circuit is driven by a regulator of about 2V. Voltage driving the oscillation circuit is out of the constant voltage range of the regulator at around 2V. The change has almost flat characteristics above about 2.5V, which is in the constant voltage range.

Figure 5 Typical oscillation frequency characteristics VS ambient temperature



Notes) 1. VDD = 2.5 to 6V, C_G = 5 pF, C_D = 10 pF, measured with crystal oscillator KF-38G, manufactured by Kyocera

2. The amount of relative change in oscillation frequency (ppm) is expressed by Δf. Δf is the amount of change relative to the peak value when VDD = 6V and TA = 22.5°C.

$$\Delta f = \frac{fosc\ (VDD, TA) - fosc\ (VDD = 6V, TA = 22.5°C)}{fosc\ (VDD = 6V, TA = 22.5°C)} \times 10^6\ (PPM)$$

3. The lower figure shows an enlarged view of the range 5°C to 40°C from the upper figure.

4. The temperature characteristics of the oscillation frequency mainly represents characteristics of the crystal oscillator itself. Generally, the oscillation frequency temperature change amount (Δf) of a 32 kHz crystal oscillator is expressed as follows:

$\Delta f = K(TO - TA)^2$ K: temperature coefficient

TO: temperature at peak value for the oscillation frequency (around room temperature)

K and T0 vary with the crystal used.
Reference) KF-38G was used, and the values are as shown below:
$K = -0.038$ (PPM/°C) TYP ($TA = -15$ to 60°C)

5) Adjusting the oscillation frequency

The crystal oscillation frequency is determined by the following six items:

(i) Frequency deviation of the crystal oscillator itself
(ii) Values of external C_G and C_D
(iii) Floating capacity of the PC board to be mounted
(iv) Oscillation circuit characteristics of the IC
(v) Working power supply voltage
(vi) Ambient operating temperature

One of the keys to improving the clock accuracy is to match the frequency rankings*1) of the crystal oscillator to IC and mounting PC board. The following explanation on the general method to adjust the oscillation frequency takes it into consideration.

*1) For 32 kHz crystal oscillators, oscillation frequencies are usually classified into several rankings based on the dispersion in manufacturing. This is because 32 kHz crystal oscillators are often used for clocks, which require high accuracy, and their frequencies must be matched to those of ICs. Variation in one ranking is ±20 PPM in most cases. The crystal manufacturer, however, determines the rankings according to the load capacity values in a standard circuit, and rankings generally overlap.

① Using fixed C_G and C_D

Prepare a crystal whose frequency ranking is known (it is best to use one with a central value in the ranking). Mount the crystal on the actual PC board together with the IC, C_G, and C_D. Change the C_G and C_D values and measure the oscillation frequency to look for appropriate C_G and C_D values. Note, however, that larger C_G and C_D values are apt to make the oscillation start time at the initial power-on longer (not including power rise from a backup voltage, when the circuit has performed oscillation once). In general, the fixed C_G and C_D values may set to about 5 to 20 pF (Figure 16 shows an example of measurement at the oscillation start time). If the oscillation frequency is not in the desired range, it is recommended to use a crystal with a different frequency ranking. After changing the frequency ranking of the crystal, repeat the above procedure to determine the C_G and C_D values. Consumed current varies a little with the C_G and C_D values. See Figures 8 and 9 for reference.

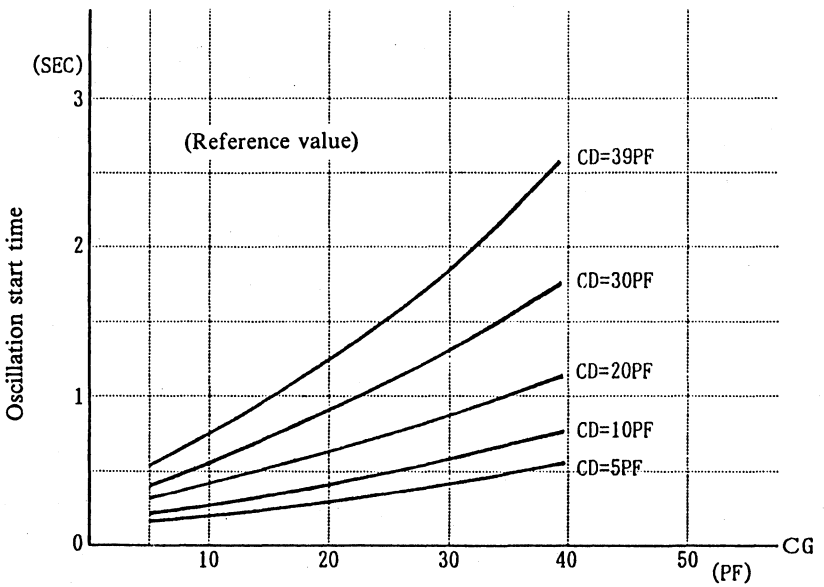
② Using a trimmer capacitor for C_G to fine-adjust the frequency (with fixed C_D)

Prepare a crystal whose frequency ranking is known (it is best to use one with a central value in the ranking). Mount the crystal on the actual PC board together with the IC, C_G, and C_D. Set the rotation of the trimmer capacitor to be little less than central, as the center of frequency deviation falls at about 14 pF when C_G is from 5 to 35 pF. Change the C_D value and measure the oscillation frequency to look for the appropriate C_D value. Taking Figures 6, 8 and 9 into consideration, the C_D value may be set from about 7 to 15 pF. If the oscillation frequency is not in the desired range, it is recommended to use a crystal with a different frequency ranking.

After changing the crystal, repeat the above procedure to determine the C_D value. After the C_D value and frequency ranking are determined as above, the oscillation frequency can be fine-adjusted by a trimmer capacitor. The 32 kHz crystal oscillator frequency falls when the ambient temperature rises or falls, so it is recommended to adjust the oscillation frequency a bit higher when adjusting it at room temperature (for higher accuracy, it should be 0 to 1 PPM faster).

③ Using a trimmer capacitor for C_D to fine-adjust the frequency (with fixed C_G)
When using a trimmer capacitor for C_D, the procedure is the same as ②. The fixed C_G value may be 5 to 15 pF.

Figure 6 Oscillation start time VS C_G

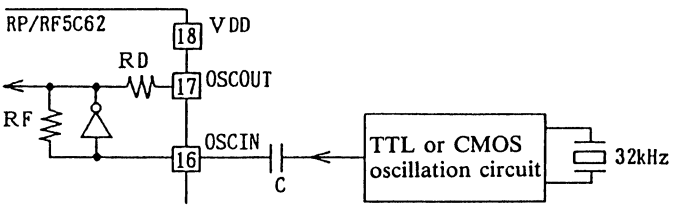


Notes) 1. VDD = 4.5V, TA = 25°C, crystal (CI ≦ 35 kΩ)
2. The oscillation start time is defined as the time between the power on and the clock output to the $\overline{\text{INTR}}$ output (at the same time as power on, the internal register is set to output a clock from the INTR output.) The average values of three trials are plotted on the graph.
3. The oscillation start time varies with the crystal oscillator and the PC board to be used. Use the above graph as a reference only. (When VDD has a smaller value than that in section 1., or when the ambient temperature is low, the oscillation start time is apt to be longer than shown in the above graph.)

6) Others

① Operating 5C62 by a 32 kHz signal from an external oscillation circuit

The inverter of the 5C62 oscillation circuit is driven at a constant voltage by a regulator of about 2V. Direct input to the OSCIN terminal by DC connection is not possible. The oscillation circuit inverter has internal negative feedback, biased to the center. Input by AC connection is possible.



C = about 20 to 50pF

Figure 7

Consider the following:

When using an external clock, the oscillation stop detection circuit is out of the guaranteed operation range. DO NOT use the oscillation detection flag (XSTP bit). When the oscillation stop detection circuit detects an oscillation stop by mistake due to noise from an external circuit, the TM3 bit of the timer clock select register is reset and the timer is stopped. Keep this in mind when using the timer. When the timer is stopped (TM3 bit is 0), resetting the XSTP bit to 0 and setting the timer clock select register reactivates the timer.

② Driving another IC from the oscillation output (OSCOUT output) of 5C62

The oscillation circuit of 5C62 is driven at a constant voltage of about 2V, so the amplitude of the oscillation output waveform is about 1.6 to 2V. The oscillation circuit operates at low power, so DO NOT use the OSCOUT output for another circuit.

③ The oscillation circuit of 5C62 operates at low power. After oscillation has started, touching the OSCIN or OSCOUT line by hand may stop oscillation temporarily. DO NOT touch the OSCIN or OSCOUT line after oscillation has started.

2. CONSUMED CURRENT

1) Rest current consumption

Backup current consumption ..... VDD = 2.5V, CE = "L", output open

Standby current consumption ..... VDD = 5.5V, input: VDD or VSS, output open

Here, the rest current consumption (equivalent to backup current consumption and standby current consumption) is defined as the current consumption when there is no access from the CPU. The consumed current varies with C_G, C_D, VDD, and ambient temperature. Figures 8 to 11 show these typical characteristics.

Figure 8 Typical rest current consumption characteristics when C_D is fixed and C_G is varied

Figure 9 Typical rest current consumption characteristics when C_G is fixed and C_D is varied

Figure 10 Typical rest current consumption characteristics when VDD is varied

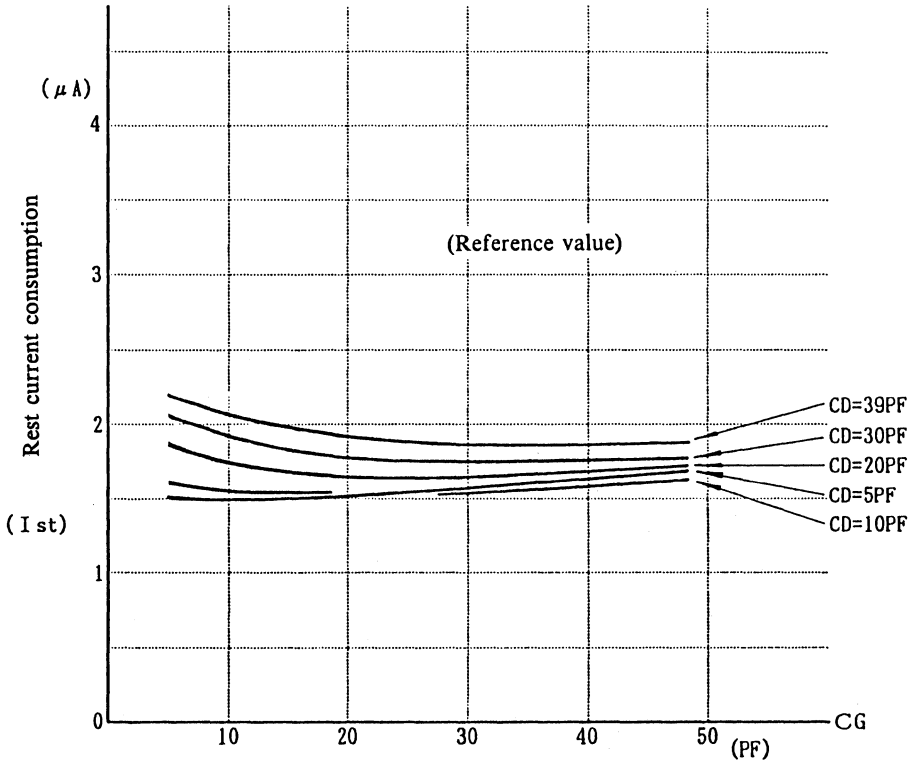
Figure 11 Typical rest current consumption characteristics when ambient temperature is varied

When the CE input is at VSS level, the terminals for interface to the CPU ($\overline{CS}$, $\overline{RD}$), $\overline{WR}$, A3 to A0, D3 to D0) are disabled. The rest current consumption does not increase according to the input voltage level of the signal input to those terminals. When the CE input is at VDD level, the interface terminals are enabled. When the input voltage level of the interface terminals is an intermediate voltage other than VDD and VSS levels, current flows in the input circuit, increasing the current consumption. At that time to reduce the current consumption, set the input voltage level to either VDD or VSS level.

2) Operating current consumption

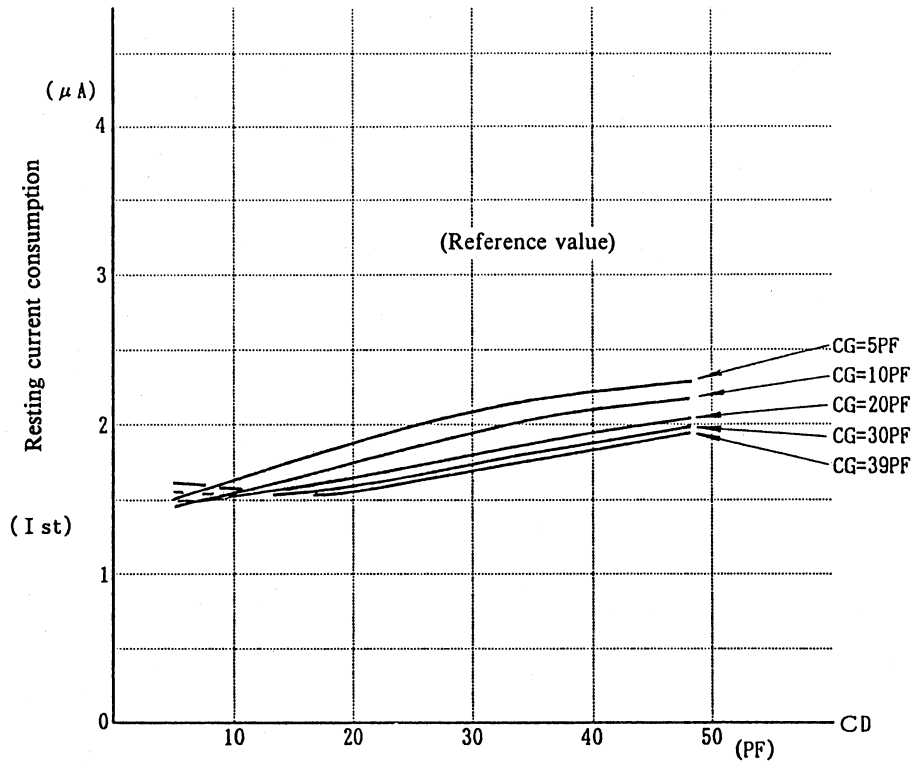
Operating current consumption is defined as the current consumption when there is access from the CPU. The consumed current varies with clock rate and input logic level of the signal accessed from the CPU. Figure 12 shows an example of the relationship between the clock rate of the signal accessed from CPU and the current consumption during CPU access.

Figure 8 Typical rest current consumption characteristics VS C_G (With fixed C_D)



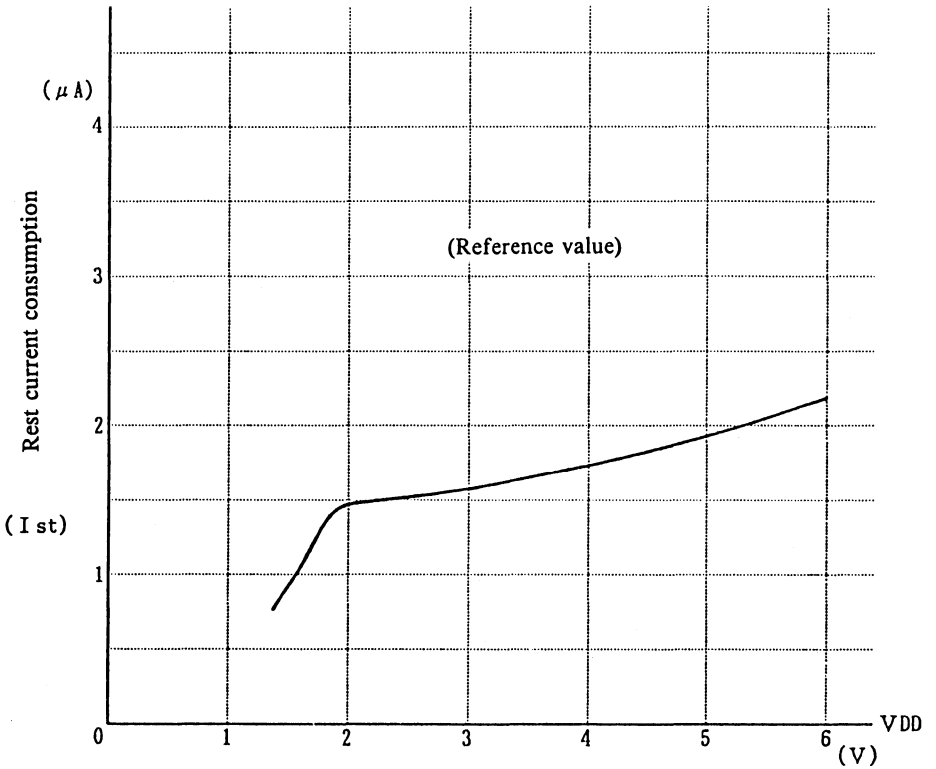
Notes) 1. VDD = 3V, TA = 25°C, crystal (CI ≦ 35 kΩ)
2. The above figure shows typical characteristics. Use it for reference only.

Figure 9 Typical rest current consumption characteristics VS C_D (With fixed C_G)



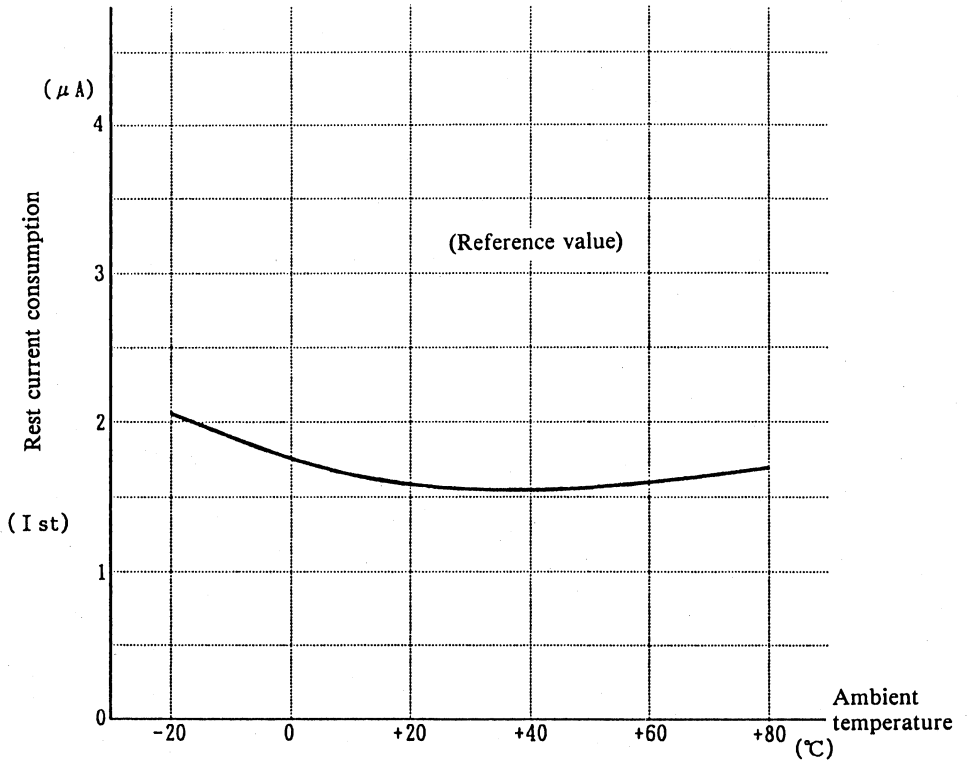
Notes) 1. VDD = 3V, TA = 25°C, crystal (CI ≦ 35 kΩ)
2. The above figure shows typical characteristics. Use it for reference only.

Figure 10 Typical rest current consumption characteristics VS VDD



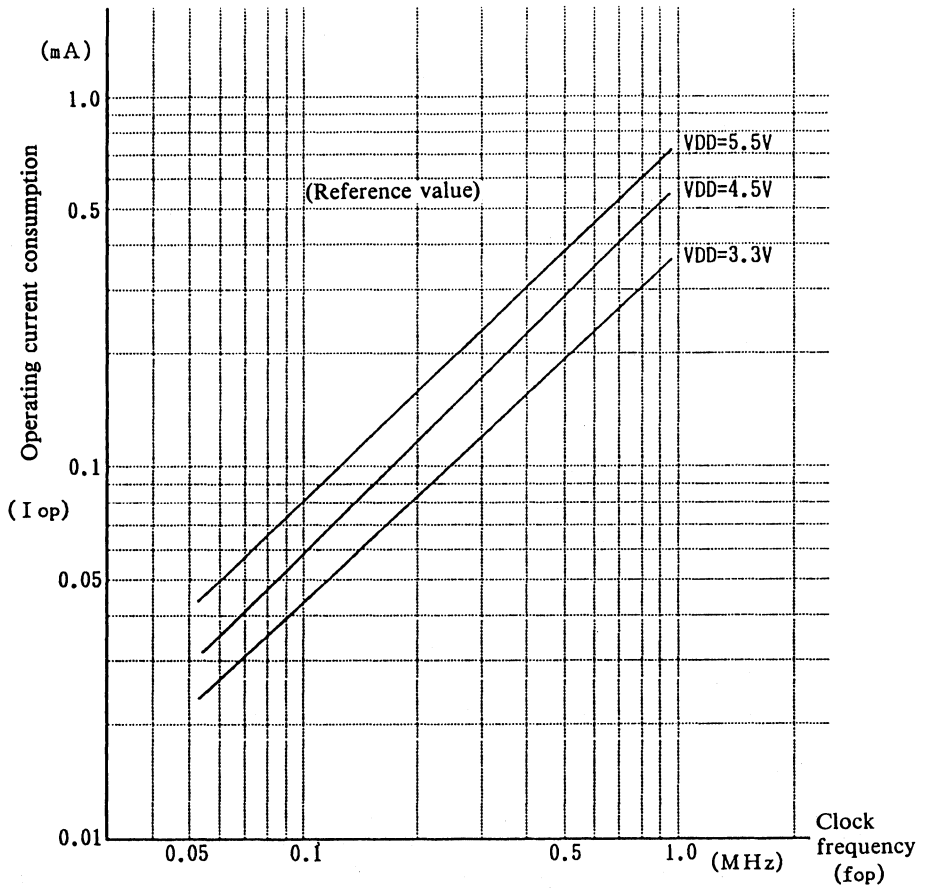
Notes) 1. $C_G = 5$ pF, $C_D = 10$ pF, TA = 25°C, crystal (CI ≦ 35k Ω)
2. The change in current consumption is rather large around 2V, because the regulator which drives the oscillation circuit is out of its constant voltage range. Current consumption changes smoothly above about 2.5V, which is in the constant voltage range.
3. The above figure shows typical characteristics. Use it for reference only.

Figure 11 Typical rest current consumption characteristics VS. ambient temperature



Notes) 1. $C_G = 5$ pF, $C_D = 10$ pF, VDD = 2.5V, crystal (CI ≦ 35 kΩ)
2. The above figure shows typical characteristics. Use it for reference only.

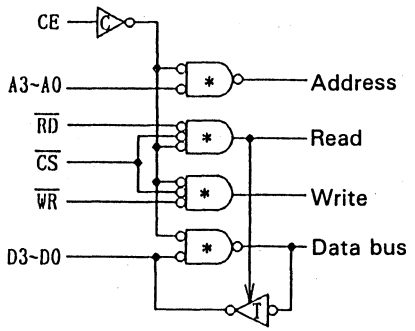
Figure 12 Measurement operating current consumption during CPU access



Notes) 1. $C_G = 5$ pF, $C_D = 10$ pF, $T_A = 25°C$, crystal ($C_l \leqq 35$ kΩ)
2. Clock is input to $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A3 to A0 at the CMOS level. The graph shows an example of the relationship between the clock frequency and operating current consumption.

3. CONNECTION TO CPU

1) I/O interface circuit



Note) C : CMOS logic input
* : TTL logic input
T : TTL fan out of 1

Figure 13

When the CE input is at "H" level (0.8 VDD or more), the device enters the operation mode and the CPU can access to the device. When reading, there is no problem if the $\overline{RD}$ and $\overline{CS}$ inputs become "H" → "L" → "H" in the same cycle. When CE is "L", the device enters non-access mode, and even when the A3 to A0, $\overline{RD}$, $\overline{CS}$, $\overline{WR}$, and D3 to D0 terminals are floating, no through current flows in the input circuit. The "L" level for the CE input is 0.2 VDD or less. But if it is higher than the VSS level, through current may flow in the inverter "C" shown in Figure 13. So, when making the consumed current very small, set the CE input "L" level to the VSS level. Connect the output of the CPU system power reduction detection circuit to the CE input.

2) CPU connection circuit

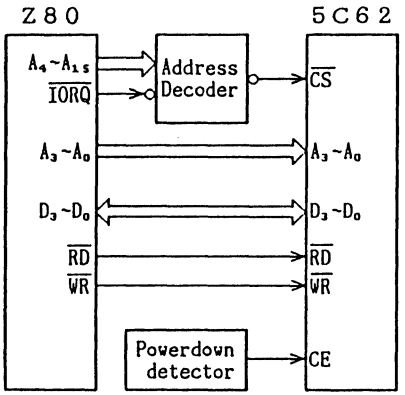
Figure 14 shows an example circuit for connecting 5C62 to an 8-bit or 16-bit CPU.
If the CPU is fast, the timing in the example of Figure 14 may not be adequate. Check the operation speed of the CPU to be used and the AC timing characteristics of 5C62.

3) AC timing

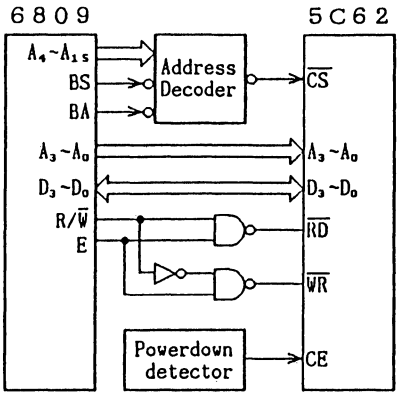
According to the voltage of VDD, three AC timing standards are set: VDD = 3V (± 10%), VDD = 5V① (± 10%), and VDD = 5V② (± 20%). To operate the system with low power consumption, an effective method is to reduce VDD. For that purpose, an AC timing standard of 3V is set.

Figure 14 Example of CPU connection

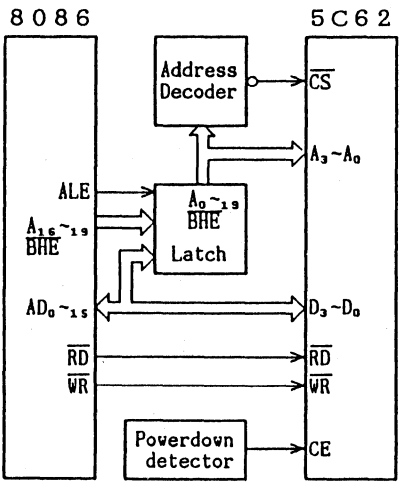
Z80 and 5C62



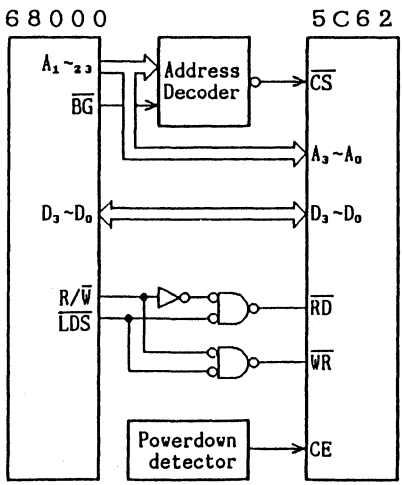
6809 and 5C62



8086 and 5C62



68000 and 5C62



4. POWER SUPPLY CIRCUIT

1) Power supply switching sequence

There are two types of power supply: the supply for system operation and the battery for system stand-by. To switch between these supplies, vary the CE input terminal level as shown in Figure 15.

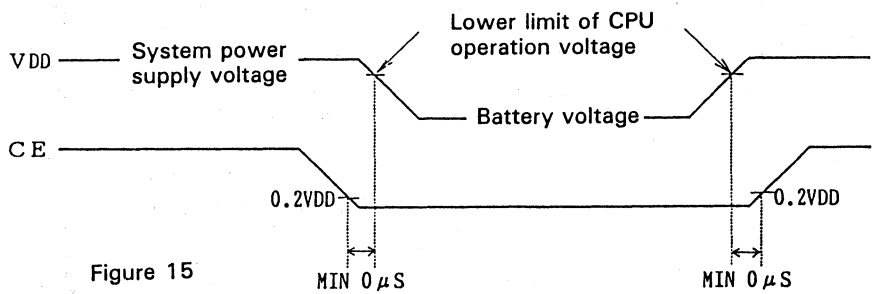


Figure 15

To switch to the battery voltage, decrease CE to the "L" level before the voltage goes lower than the CPU operation voltage. To switch to the system power supply, wait until VDD is higher than the operating voltage of the CPU and set the CE input to "H" level.

2) Power supply switching circuit

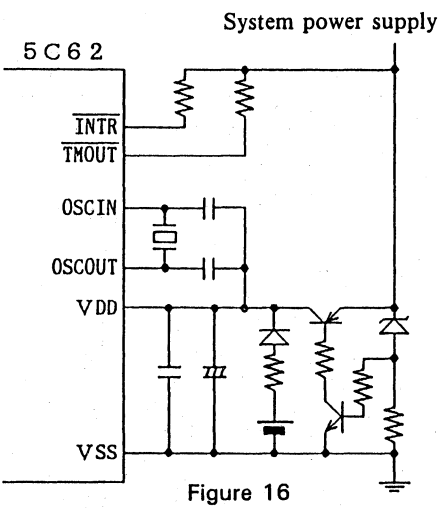


Figure 16

Figure 16 shows an example of the circuit around the power supply circuit. In the example, a lithium battery is used. Locate the capacitor as close to the IC as possible (if possible, use a ceramic capacitor of 0.01μF or more and a tantalum capacitor in parallel). Connect one side of the oscillation circuit capacitor to VDD (the oscillation circuit is driven by a negative regulator from VDD, with VDD as reference).

Pull up the $\overline{\text{INTR}}$ and $\overline{\text{TMOUT}}$ outputs to the system power supply side so that no invalid current flows from the battery during battery backup (the $\overline{\text{INTR}}$ output operates when CE = "L", and the $\overline{\text{TMOUT}}$ output does not operate when CE = "L").

5. EXPLANATION OF OPERATIONS

1) Operation

(a) Write

To write values to the internal counter register, set the CE terminal "H" and specify the counter register address at terminals A0 to A3. Then set the $\overline{CS}$ terminal "L" and set the $\overline{WR}$ terminal "H" → "L" → "H" ($\overline{CS}$ and $\overline{WR}$ may become "L" at the same time, or $\overline{WR}$ may become "L" first). Likewise, the data input to D0 to D3 terminals are written internally. Read-only bits are not affected by this write operation.

(b) Read

To read the internal counter register, set the CE terminal "H" and specify the counter register address at A0 to A3 terminals. Then set the $\overline{CS}$ terminal "L" and set the $\overline{RD}$ terminal "H" → "L" ($\overline{CS}$ and $\overline{RD}$ may become "L" at the same time, or $\overline{RD}$ may become "L" first). Likewise, internal data can be read from D0 to D3 terminals. Write-only bits are reset to 0 by this read operation.

(c) Clock, calendar

5C62 has an hours/minutes/seconds counter in BCD code for the clock and a leap year/year/month/day/week register and counter for the calendar. When the year is specified by the dominical year, leap year operation is automatically performed. After setting the year, you can set the leap-year register not to perform the leap-year operation.

(d) Alarm

5C62 has alarm registers (hours and minutes) for generating interrupts at specified time. These registers may be used for daily alarms. An alarm interrupt can operate even when the CE terminal is "L" (such as during battery backup), and is output from the $\overline{INTR}$ terminal. Alarm interrupt and clock interrupt are ORed together and output from the $\overline{INTR}$ terminal.

(e) Clock interrupt

A timing clock interrupt or level interrupt can be output from the $\overline{INTR}$ terminal every 0.448 msec to 60 sec. The counter for this interrupt is the same as the counter for the clock, so the clock interrupt cannot restart. 0.488, 0.997, 7.813 and 62.5 ms interrupt cycles are not affected by clock operations. The 1-sec interrupt cycle is affected when 1 is written to the ADJ bit or the WTRST bit. The 60-sec interrupt cycle is affected when 1 is written to the ADJ bit (for the effect of the ADJ bit, see the next section, Software Processing, ±30 sec adjustment of the seconds digit. When operating the WTRST bit, the change timing of the $\overline{INTR}$ output is the same as that of the ADJ bit). Clock interrupt is output even when CE is "L" (such as during battery backup).

(f) Timer interrupt

5C62 has an independent timer counter. You can select a timer interval from 4.883 ms to 625 ms. The timer output is output from the $\overline{TMOUT}$ terminal. The timer can restart, and can be used not only as an ordinary timer but also as a free run timer or a watch-dog timer. When CE is "L", the $\overline{TMOUT}$ terminal is OFF and timer operation stops temporarily. When CE becomes "H", the timer restarts and it outputs pulses. When the XSTP bit is set to 1 upon detection of oscillation stop, the timer operation is disabled. (At that time the D3 bit of the timer clock set register is reset, and the timer is reset.) The timer is affected by the output of the oscillation stop detection circuit, so set the XSTP bit to 0 when using the timer (if the oscillation is not stopped, the timer starts operation when the timer clock select register is set even when XSTP=0). For a fail-safe system using a timer, it is

recommended to have a routine to write the timer cycle setting data occasionally to the timer clock select register.

(g) Oscillation stop detection

5C62 has a built-in circuit to detect oscillation. When the oscillation detection circuit detects an oscillation stop, the internal XSTP bit is set. This bit is set to 1 when the power supply voltage decreases and the oscillation stops, and is maintained at 1 even if oscillation restarts. This bit is also set to 1 at power-on, and is maintained at 1 even if the oscillation restarts. The minimum working voltage for oscillation is about equal to the sum of the threshold voltage of MOSTr of Pch and Nch. Internal data is held as long as oscillation is maintained.

The XSTP bit can be used to judge whether the system has risen from 0V or from the battery voltage, or whether the backup batteries are weak. To use the XSTP bit, consider the following: condensation on the PC board may stop the oscillation and make the XSTP bit 1. Prevent condensation around the oscillator beforehand. Also, take care to prevent temporary power failure and check the layout of the PC board around the oscillation circuit.

2) Software processing

The following is an example of software processing. Flowcharts are shown later.

(a) Processing when power is turned on.

At initial power on, internal conditions are not determined, initialization is required. There are two flowcharts for processing at power on: one does not use the XSTP bit, the other uses it. The XSTP bit can be used to judge the validity of the internal data at initial power on. In the second example, the XSTP bit is used for judging the necessity of initialization routine.

(b) Read and write of clock and calendar

The clock and calendar must be written to only while a carry is not performed. When writing data, stop the clock by setting the WTEN bit to 0, and check that a carry is not being performed, using the BSY bit. Also, the clock and calendar must be read only while a carry is not performed, because wrong data may be read while carry is performed. To prevent this, it is recommended to use one of the following three methods for reading:

① Stop the clock temporarily, and read the value while the clock is stopped. If the clock is stopped for 1 sec or less, the clock does not delay and there is no problem (even if the system enters the backup mode while the clock is stopped, the clock starts counting when the CE terminal becomes "L". If it does not become "L", counting must be started by the software).

② Use a clock interrupt to read the value.

③ Read the clock twice, and judge it correct if the two values match.

(c) Writing to alarm clock

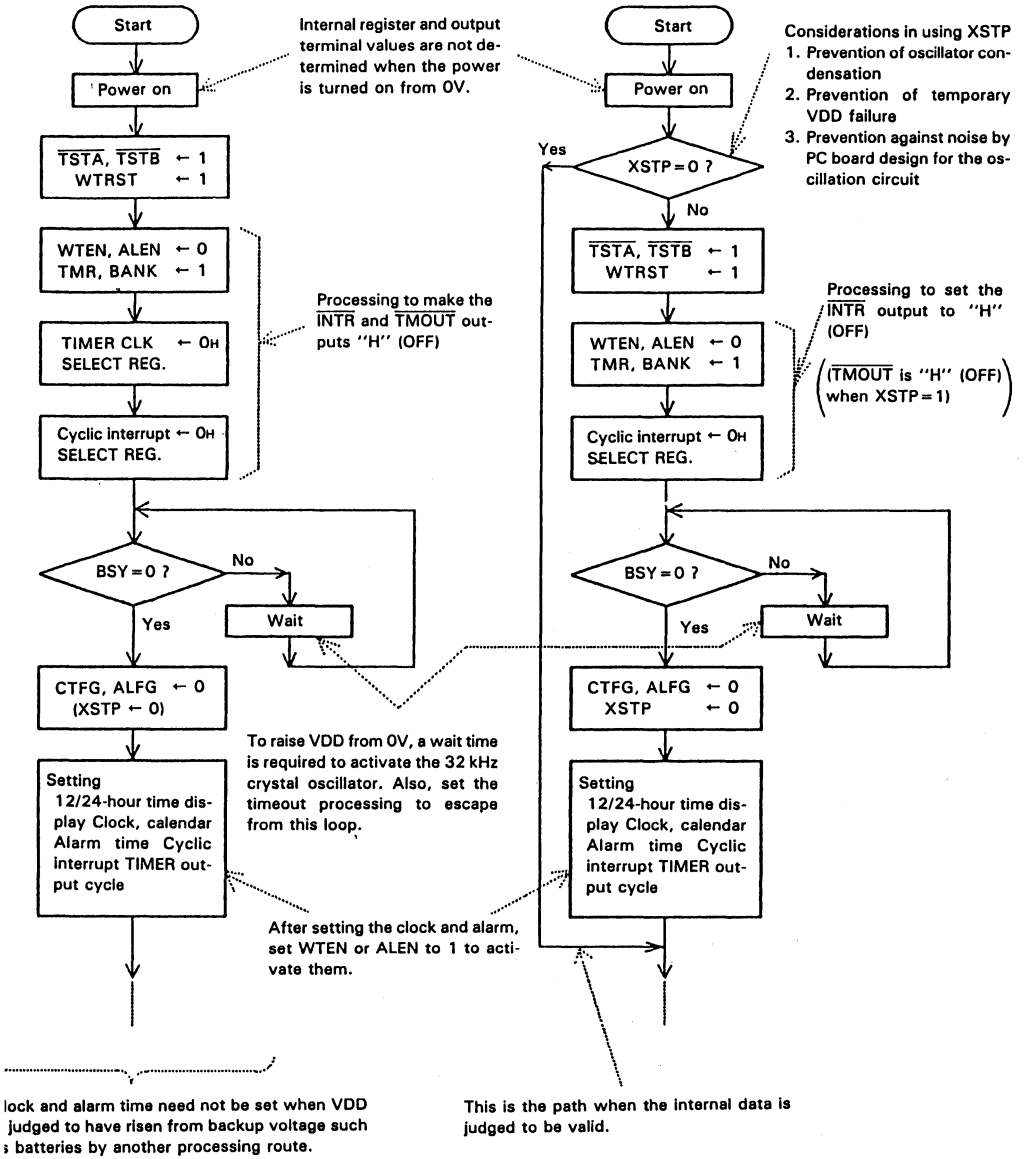
Example of writing the alarm time.

(d) ±30 seconds adjustment of the seconds digit

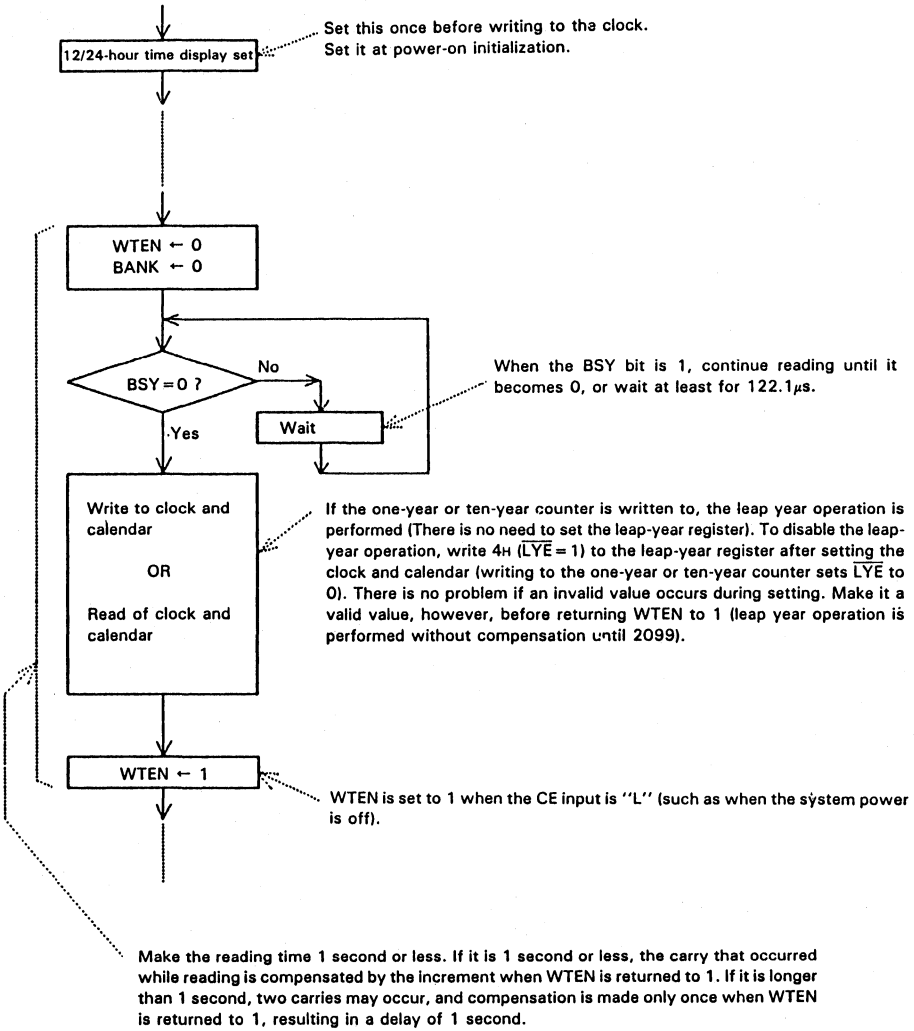
Shows an example of ±30 seconds adjustment of the seconds digit.

Power on procedure ① (XSTP bit is not used) (Initialization follow)

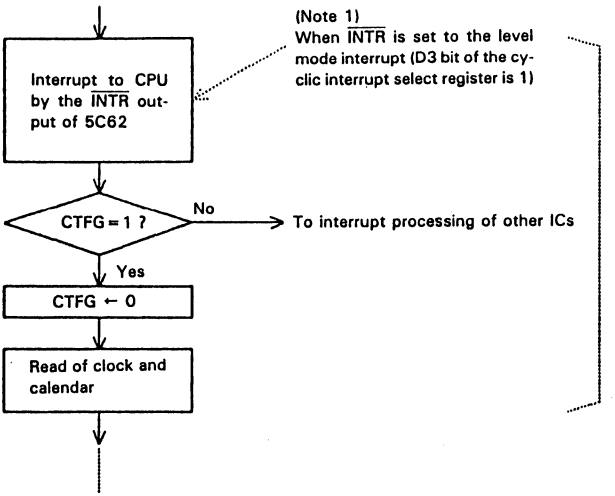
Power-on procedure ② (XSTP bit is used) (as when batteries are used)



Write of clock and calendar or read of clock and calendar ①



Read of clock and calendar ②

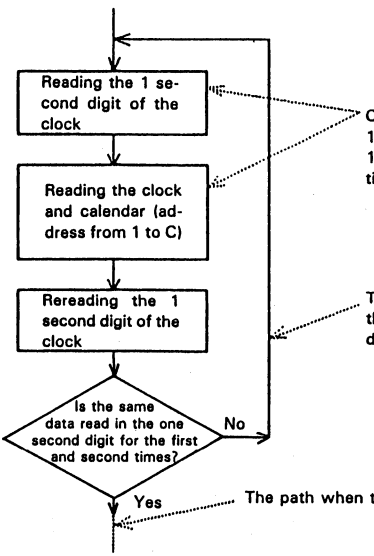


(Note 1)
When $\overline{INTR}$ is set to the level mode interrupt (D3 bit of the cyclic interrupt select register is 1)

(Note 2)
When reading the clock and calendar finishes within ($\overline{INTR}$ set cycle − 30.5μs) after the $\overline{INTR}$ output goes "L". (To prevent reading mistakes due to a carry during read)

* This read is possible when the above two conditions (notes 1 and 2) are met. If the $\overline{INTR}$ set interrupt cycle is short, be careful of the interrupt processing time.

Read of clock and calendar ③

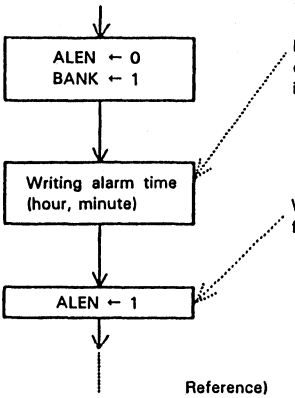


Carry of the clock and the calendar is performed in the following order: 1 second digit (address 0) → 10 seconds digit (address 1) → . . . → 1 year digit (address B) → 10 years digit (address C). (including delay time). Read the clock in the order from address 1 to address C.

The path for re-reading to prevent wrong values from being read, when the first 1 second digit data does not match the second data because data is read before and after the carry.

The path when the values are correctly read.

Write of alarm time

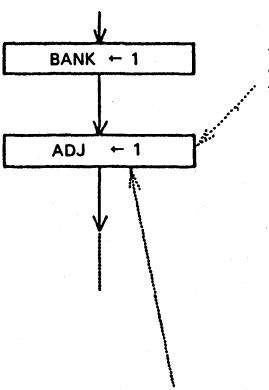


If an invalid value is set in the alarm register, it is no problem; the alarm match operation is just not performed. After setting ALEN to 1, however, set an invalid value.

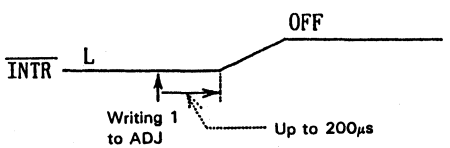
When the alarm time is set to the same time as the clock, either of the following occurs:
ALEN = 0: ALFG is 0.
ALEN = 1: ALFG is set to 1 and $\overline{INTR}$ to "L" within 61.1μs.

Reference)
When the ALEN bit is 1 and the clock matches the alarm time, ALFG = 1 and $\overline{INTR}$ = "L". There are two ways to set $\overline{INTR}$ = "OFF" and ALFG = 0: writing 0 to the ALFG bit and writing 0 to the ALEN bit. After writing 0 to the ALEN bit, returning the ALEN bit from 0 to 1 while the clock matches the alarm time, ALFG becomes 1 and $\overline{INTR}$ becomes "L" within 61.1μs at most.

±30 seconds adjustment of the seconds digit



The 8 Hz to 1 Hz divider below the digit of second is reset and restarted. When a clock interrupt of 1-second or 60-second cycle is set and $\overline{INTR}$ = "L", $\overline{INTR}$ becomes OFF in the timing shown below.
(There is no effect on $\overline{INTR}$ if the cycle is other than 1-second or 60-second.)



Up to 122.1μs is required to finish the adjustment. During the adjustment, the BSY bit is 1.

2-Dimension Filter 5C67

User Manual

NO. EU-005-8908

■ Space filtering

Space filtering means to extract specific information and elements required for input image data. It is analogous to general FIR type filters (such as low-pass and band-pass filters for communications), performed on image data that consists of i × j dot matrix.

To perform image filtering on pixel m in Figure 1, output M is calculated by equation (1) from point m and from data of surrounding points (neighbor pixel areas, for example, from point a to point y).

$$M = a \times W_{11} + b \times W_{12} + ... + m \times W_{33} + ... + y \times W_{55} \quad ..... (1)$$

W_{ij} is a two-dimensional filter coefficient as shown in Figure 2. Performing the operation on all input pixels enables space filtering.

Space filtering enables various image processing, for example, smoothing images, extracting edges, and enhancing edges. To smooth images, specify filter coefficients as shown in Figure 3. The neighbor pixel data items are averaged by equation (1) as follows:

$$M = \frac{1}{25} (a + b + c + ... + m + ... + y)$$

With the output of the average value, pixels are smoothed. This operation can be used to eliminate fine noise on images.

Figure 4 shows the filter coefficients for edge enhancement, which displays characters clearly.

Space filtering can be applied to various types of processing by changing filter coefficients.

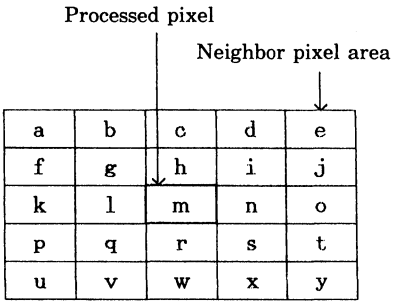


Figure 1 Input pixels

W_{11}	12	13	14	15
21	22	23	24	25
31	32	W_{33}	34	35
41	42	43	44	45
51	52	53	54	55

Figure 2 Filter coefficients

1/25	1/25	1/25	1/25	1/25
1/25	1/25	1/25	1/25	1/25
1/25	1/25	1/25	1/25	1/25
1/25	1/25	1/25	1/25	1/25
1/25	1/25	1/25	1/25	1/25

Figure 3 Filter coefficient example

-1	-1	-1	-1	-1
-1	-1	-1	-1	-1
-1	-1	25	-1	-1
-1	-1	-1	-1	-1
-1	-1	-1	-1	-1

Figure 4 Filter coefficient example

■ Outline of 5C67

Space filtering takes a long processing time when performed on a general-purpose CPU or DSP. So it is necessary to write all image data to memory before filtering, which makes it difficult to perform real-time filtering. Also, when a special IC for filtering is designed with gate arrays, filter coefficients must be fixed because the circuit scale is large, which means different gate arrays must be made for different types of processing. RICHO's two-dimensional image filter RF5C67 solves these problems. RF5C67 is a special LSI that performs space filtering on 5 × 5 pixel area quickly and flexibly.

- High speed: 25 ns/pixel max.
- Flexible: Possible to change filter coefficients

■ 5C67 Features

- 5 × 5 image area flat surface filtering
- Operating frequency: 20 MHz
- Processing speed: 25 ns/pixel (Odd-Even mode, two 5C67s use)
  50 ns/pixel (Serial mode, one 5C67 use)
- Pixel data: 6-bit, integer
- Coefficient data: 7-bit, two's compliment, changeable
- Number of input data items: 10 (Odd-Even mode)
  5 (Serial mode)
- CMOS process
- +5 V single power supply
- Package: 100-pin flat package
- Rounding: When the calculation result is a positive value and overflows, it is rounded to 63 (maximum value).
  When the calculation result is a negative value:
  Rounded to 0
  Absolute value is taken } Selectable

■ Operation

RF5C67 contains 15 multipliers, a divider, and an FA block that performs rounding. Figure 4 shows the internal block diagram.

(1) Product sum calculation unit

Performs product sum calculation of five data items for each main scanning line.

(2) Addition unit

Adds the resultant data of the product sum operation for five lines.

(3) Division unit

Divides the resultant data of the product sum operation of 25 pixels.

(4) FA block

Rounds the final result of space filtering, and obtains the final output result.

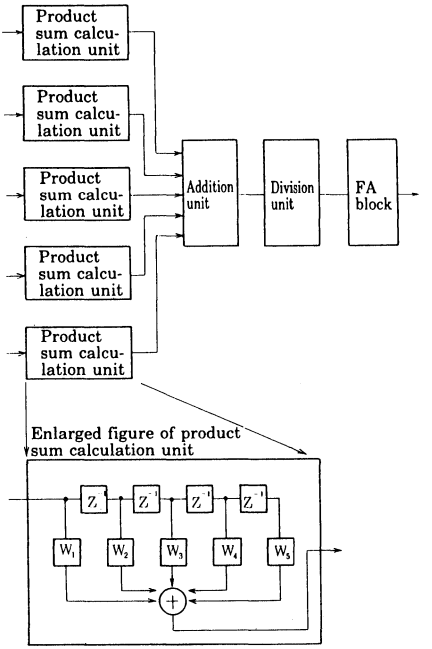


Figure 4 Block diagram

(a) Filter coefficient

To perform MTF compensation (edge enhancement) with the coefficients shown in Figure 5, regard these coefficients as shown in Figure 6. Specify coefficients 0, −1, −2, and 32 to the 15 multipliers and coefficient 1/16 to the divider.

To specify coefficients to multipliers and dividers, use address inputs A_0 to A_4 and CS and WS terminals.

Filter coefficients must be symmetrical, or with reverse sign, to the sub scanning lines, including the attention pixel. So there are 15 coefficients as shown in Figure 7. For specification, enter those 15 coefficients and 10 plus and minus signs.

		$\frac{1}{16}$		
	$-\frac{1}{16}$	$\frac{1}{8}$	$-\frac{1}{16}$	
$\frac{1}{16}$	$\frac{1}{8}$	2	$\frac{1}{8}$	$\frac{1}{16}$
	$-\frac{1}{16}$	$\frac{1}{8}$	$-\frac{1}{16}$	
		$-\frac{1}{16}$		

Figure 5

		-1		
	-1	-2	-1	
-1	-2	32	-2	-1
	-1	-2	-1	
		-1		

Figure 6

W_{11}	W_{12}	W_{13}	$\pm W_{12}$	$\pm W_{11}$
W_{21}	W_{22}	W_{23}	$\pm W_{22}$	$\pm W_{21}$
W_{31}	W_{32}	W_{33}	$\pm W_{32}$	$\pm W_{31}$
W_{41}	W_{42}	W_{43}	$\pm W_{42}$	$\pm W_{41}$
W_{51}	W_{52}	W_{53}	$\pm W_{52}$	$\pm W_{51}$

Figure 7

(b) Serial mode and Odd-Even mode

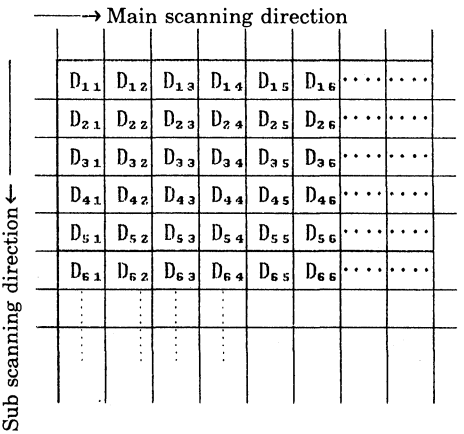
RF5C67 performs space filtering in two modes:

① Serial mode

② Odd-Even mode

In the serial mode, one pixel data item is entered for each of the five main scanning lines (totally five data items) simultaneously, and one pixel processing result is output. The processing speed is 50 ns/pixel max.

In the Odd-Even mode, two pixel data items are entered for each of the five main scanning lines (totally ten data items) simultaneously, and two filtering results are output for one line simultaneously. This gives processing twice as fast as that in the serial mode: 25 ns/pixel. However, in the Odd-Even mode, two RF5C67 filters must be used.



The following explains the processing of the image data shown in the above figures in the serial and Odd-Even modes:

① Serial mode

Figure 8 shows a 5 × 5 area, with the pixel to be filtered at the center. Enter the five pixel data items on the same sub scanning line in order, and synchronized with the clock. The processing results are output in order, after a certain delay time, in synchronization with the clock.

For example, when pixel data items are entered in the following order: (D_{11}, D_{21}, D_{31}, D_{41}, D_{51}), (D_{12}, D_{22}, D_{32}, D_{42}, D_{52}), (D_{13}, D_{23}, D_{33}, D_{43}, D_{53}), ..., filtering results are output as follows: F(D_{33}), F(D_{34}), F(D_{35}), ... The same pixel data item must be entered to two terminals, for example, data for the first line to input terminal DAI and DAII, and the data for the second line to DBI and DBII.

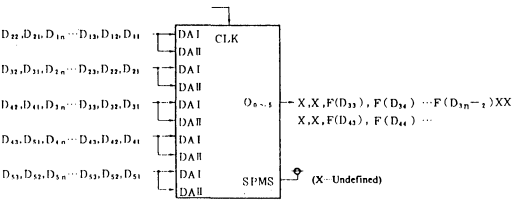


Figure 8

② Odd-Even mode

As shown in Figure 9, enter two continuous pixel data items (Odd data and Even data) for the five main scanning lines (10 data items altogether) simultaneously into two RF5C67 filters, in synchronization with the clock. One RF5C67 (Odd mode) outputs filtering results of Odd data, and the other RF5C67 outputs the filtering results of Even data at the same time.

For example, when pixel data items are entered in the following order: (D_{11}, D_{12}, D_{21}, D_{22}, D_{31}, D_{32}, D_{41}, D_{42}, D_{51}, D_{52}), (D_{13}, D_{14}, D_{23}, D_{24}, D_{33}, D_{34}, D_{43}, D_{44}, D_{53}, D_{54})..., Odd mode RF5C67 outputs (D_{33}), and F(D_{35}), and Even mode RF5C67 outputs (D_{34}) and F (D_{36}) simultaneously.

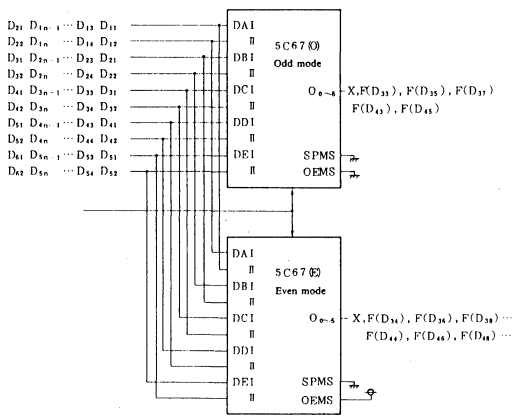


Figure 9

The Odd and Even modes are switched by OEMS (Odd-Even-Mode Select) input. When the OEMS terminal is LOW-input, RF5C67 is in the Odd mode. When the OEMS terminal is HIGH-input, RF5C67 is in the Even mode.

For the Odd mode, enter pixel data as follows:

D_{11}, D_{13}, D_{15}, ... to DAI

D_{12}, D_{14}, D_{16}, ... to DAII

For the Even mode, enter pixel data as follows:

D_{11}, D_{13}, D_{15}, ... to DAII

D_{12}, D_{14}, D_{16}, ... to DAI

The same thing goes for pixel data for the second to the fifth lines. The serial and Odd-Even modes are switched by SPMS (Serial/Parallel Mode Select) input.

The table below shows the SPMS terminal input and OEMS terminal input used in each mode:

Mode		SPMS	OEMS
Serial Mode		H	X
Odd-Even	Odd	L	L
	Even	L	H

X: don't care

(c) Value format

The following explains the value format for input data, coefficient data, and output data.

① Input pixel data

Input data is a positive 6-bit integer.

$0 \leqq D \leqq 63$

② Coefficient data

Coefficient data is a 7-bit integer, and expressed as two's compliment.

$-64 \leqq W \leqq 63$

③ Internal intermediate calculation (product sum calculation)

The results of internal product sum calculation are expressed by 13-bit integers as two's compliment.

$-4096 \leqq X \leqq 4095$

④ Output pixel data

Output pixel data is expressed by a positive 6-bit integer. Filter operation results (divider output) are expressed by 13-bit integers as described in step ③, but they are rounded to positive 6-bit integers in final output.

- Rounding of positive values:

Positive values equal to or larger than 64 are rounded to 63. When rounding occurs, the OVR output terminal becomes "H".

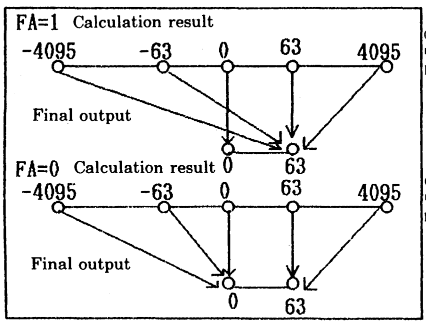
- Rounding of negative values:

There are two ways to round negative values, selected by FA input:

When FA = "H": Negative values are expressed in absolute values. Values equal to or smaller than −64 are rounded to 263.

When FA = "L": All negative values are rounded to 0.

When the operation result is a negative value, the SGN output terminal becomes "H". Figure 10 shows the relationship.



FA="H"

Calculation result	-4095····-64-63-62····-1	0	1 ···62 63 64 ···4095
Final output	63··· 63 63 62··· 1	0	1 ···62 63 63 ···63
OVR	1··· 1 0 0··· 0	0	0 ··· 0 0 1 ··· 1
SGN	1··· 1 1 1··· 1	0	0 ··· 0 0 0 ··· 0

FA="L"

Calculation result	-4095····-64-63-62····-1	0	1 ···62 63 64 ···4095
Final output	0··· 0 0 0··· 0	0	1 ···62 63 63 ···63
OVR	1··· 1 0 0··· 0	0	0 ··· 0 0 1 ··· 1
SGN	1··· 1 1 1··· 1	0	0 ··· 0 0 0 ··· 0

Figure 10

(d) Entering coefficient data

To perform filtering using RF5C67, specify 15 multiplication coefficients and division coefficients. Use terminals A_0 to A_4 and D_0 to D_7, and input terminals CS and WR.

A_0 to A_4 are input terminals for selecting internal coefficient registers.

D_0 to D_7 are data buses to enter coefficient data.

Coefficient data can be written with the CPU directly connected.

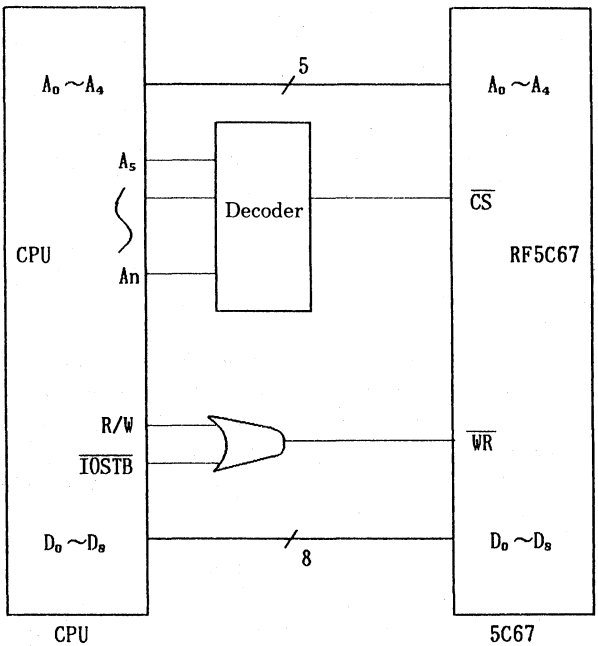


Figure 11 Connection to CPU

① Multiplication coefficient

8-bit data is specified. Address input to select a coefficient register for each multiplier is expressed in the table below:

The content of the 8-bit data is as follows:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
PM	Y						

Y is 7-bit integer data expressed by two's compliment as W_{i1}, W_{i2}, or W_{i3}. PM indicates whether the sign of W_{i4} and W_{i5} is the same as that of W_{i1} and W_{i2} or is reversed.

When PM=0, $W_{i5}=W_{i1}$ or $W_{i4}=W_{i2}$

When PM=1, $W_{i5}=-W_{i1}$ or $W_{i4}=-W_{i2}$

For example, to enter as follows:

$W_{11} = 3$

$W_{12} = 3$

$W_{13} = 3$

$W_{14} = 3$

$W_{15} = -3$

Enter data as shown below:

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
W_{11}	1	0	0	0	0	0	1	1

↑ $W_{11}=3$

└ $W_{15}=-W_{11}$

W_{12}	0	0	0	0	0	0	1	1

↑ 3

└ $W_{15}=W_{12}$

W_{13}	×	1	1	1	1	1	0	1

↑ -3

Don't Care

A					Odd-even mode	Serial mode
4	3	2	1	0		
0	0	0	0	0	W_{11}	W_{12}
0	0	0	0	1	W_{12}	W_{11}
0	0	0	1	0	W_{13}	W_{13}
0	0	0	1	1	W_{21}	W_{22}
0	0	1	0	0	W_{22}	W_{21}
0	0	1	0	1	W_{23}	W_{23}
0	0	1	1	0	W_{31}	W_{32}
0	0	1	1	1	W_{32}	W_{31}
0	1	0	0	0	W_{33}	W_{33}
0	1	0	0	1	W_{41}	W_{42}
0	1	0	1	0	W_{42}	W_{41}
0	1	0	1	1	W_{43}	W_{43}
0	1	1	0	0	W_{51}	W_{52}
0	1	1	0	1	W_{52}	W_{51}
0	1	1	1	0	W_{53}	W_{53}

Filter Coefficient

② Division coefficient

The divider used in RF5C67 consists of shifters and adders/subtracters. To specify coefficients, enter data to three registers.

1) Divider operation principle

Figure 12 shows the block diagram of a divider.

Shifters 1 and 2 shift data to the right arithmetically by 0 to 4 bits, and shifter 3 by 0 to 5 bits. For adders/subtracters, use each PM input to select to perform addition of A + B (PM = 0) or subtraction of A − B (PM = 1). When SW1 and SW2 inputs are 0, the input of the A-side of the adder/subtracter becomes 0, and the input from the B-side is output as is.

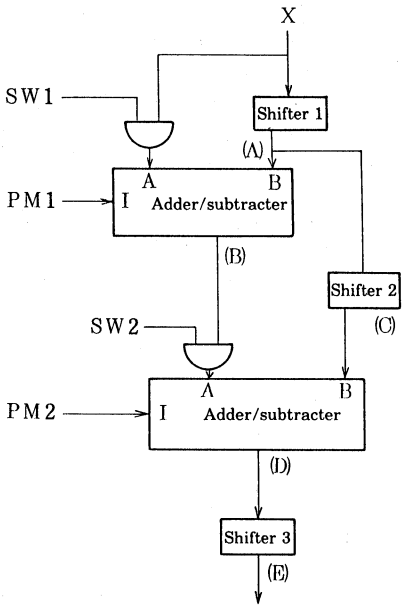


Figure 12 Divider block diagram

When input data is X,
Amount of shift 1 is p,
Amount of shift 2 is q,
Amount of shift 3 is r,
SW1 = SW2 = 1, and
PM1 = PM2 = 0,
Data at (A), (B), (C), (D), and (E) in Figure 12 are:

$(A) = 2^{-p} \cdot X$
$(B) = X + 2^{-p} \cdot X = (1 + 2^{-p})X$
$(C) = (2^{-p} \cdot X) \cdot 2^{-q} = 2^{-(p+q)} \cdot X$
$(D) = X + 2^{-p} \cdot X + 2^{-(p+q)} \cdot X = (1 + 2^{-p} + 2^{-(p+q)}) \cdot X$
$(E) = 2^{-r}(D)$
$\therefore Y = (2^{-r} + 2^{-(p+r)} + 2^{-(p+q+r)})X$

Therefore, $2^{-r} + 2^{-(p+r)} + 2^{-(p+r+q)}$ is the coefficient of the division.
As an example, let's divide 1 by 25.
1/25 can be described as follows:
$1/25 = 2^{-5} + 2^{-7} + 2^{-11} + 2^{-12} + 2^{-13} + \ldots$
As seen in (E), the divider can express three items of power of two. So we can say that 1/25 is roughly to $2^{-5} + 2^{-7} + 2^{-10}$ (=0.040039).

At that time,

$$r = 5 \quad p = 2$$
$$p + r = 7 \quad q = 3$$
$$p + q + r = 10 \quad r = 5$$

So, to perform the division of 1/25, the amount of shift 1 must be 2 bits, shift 2 must be 3 bits, and shift 3 must be 5 bits. (For other division coefficients, see the data sheet of 5C67.)

2) Specifying coefficients

To perform division, specify the three shifter amount values described above and the values of SW1, SW2, PM1, and PM2 to three registers.

The table on the right shows address input to select the three registers.

A					
4	3	2	1	0	
1	0	0	0	0	LATCH1
1	0	0	0	1	LATCH2
1	0	0	1	0	LATCH3

LATCH1

D_7	6	5	4	3	2	1	D_0
X	PM1	SW1	Shift 1				

LATCH2

D_7	6	5	4	3	2	1	D_0
X	PM2	SW2	Shift 2				

LATCH3

D_7	6	5	4	3	2	1	D_0
X	X	Shift 3					

X:Don't Care

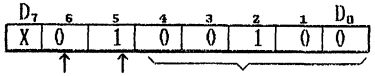
Substitute 0 or 1 for PM1, PM2, SW1, and SW2. For shifters 1, 2, and 3, enter the following data according to the amount of shift:

0	0	0	0	0	1	0-bit shift
0	0	0	0	1	0	1-bit shift
0	0	0	1	0	0	2-bit shift
0	0	1	0	0	0	3-bit shift
0	1	0	0	0	0	4-bit shift
1	0	0	0	0	0	5-bit shift

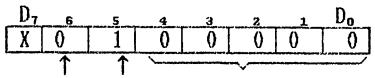
Note: Be sure to enter one of the above data items for shift amount. Inputting any other data results in misoperation.

The following example indicates data to specify the coefficient for the division of 1/25. As described before, PM1 = 0, PM2 = 0, SW1 = 1, SW2 = 1, shift 1 = 1 bit, shift 2 = 3 bits, and shift 3 = 5 bits, so the following data must be input to each register:

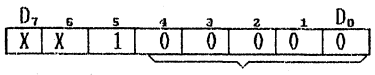
LATCH1



LATCH2



LATCH3



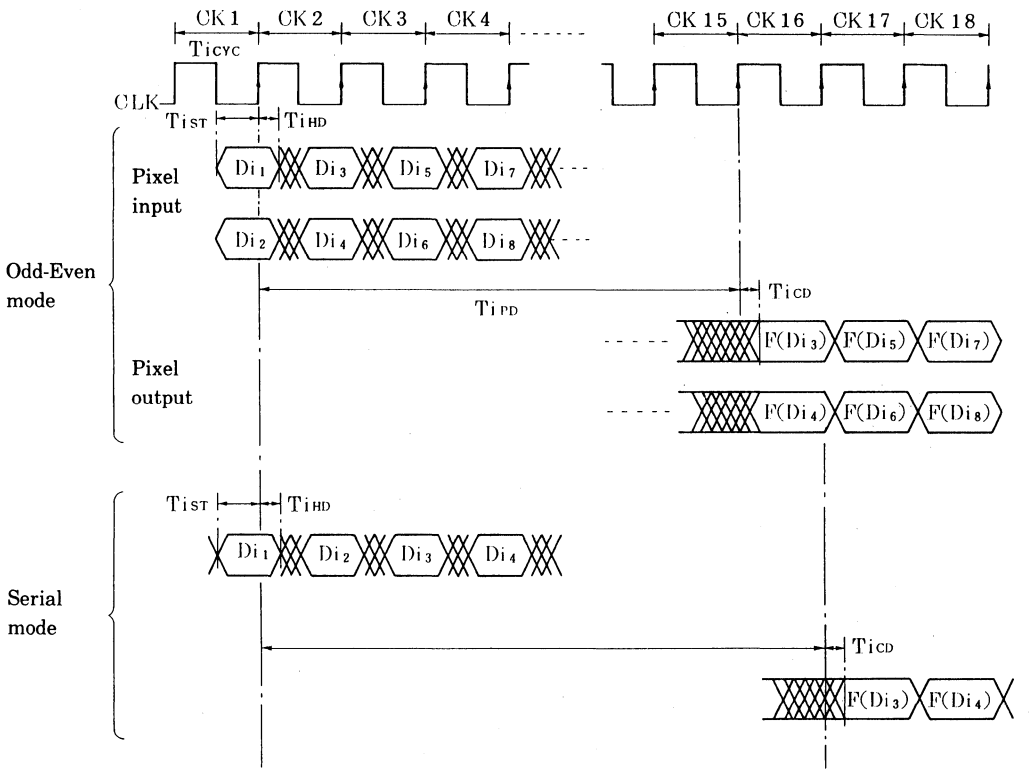
The table below shows data input for each register to perform 1/25, 1/15, 1/9, 1/3, and 1/8.

Division coefficient	Address	Input data								
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
1/25	10	X	0	1	0	0	1	0	0	24
	11	X	0	1	0	1	0	0	0	28
	12	X	X	1	0	0	0	0	0	20
1/15	10	X	0	0	0	0	0	0	0	00
	11	X	0	1	1	0	0	0	0	30
	12	X	X	0	1	0	0	0	0	10
1/9	10	X	1	1	0	1	0	0	0	68
	11	X	0	1	0	1	0	0	0	28
	12	X	X	0	0	1	0	0	0	08
1/3	10	X	0	1	0	0	1	0	0	24
	11	X	0	1	0	0	1	0	0	24
	12	X	X	0	0	0	1	0	0	04
1/8	10	X	0	0	0	0	0	0	1	01
	11	X	0	0	0	0	0	0	1	01
	12	X	X	0	0	1	0	0	0	08

X: Don't Care

■ Timing chart

The figure below shows the timing chart and related to the clock and input/output pixels and AC characteristics:

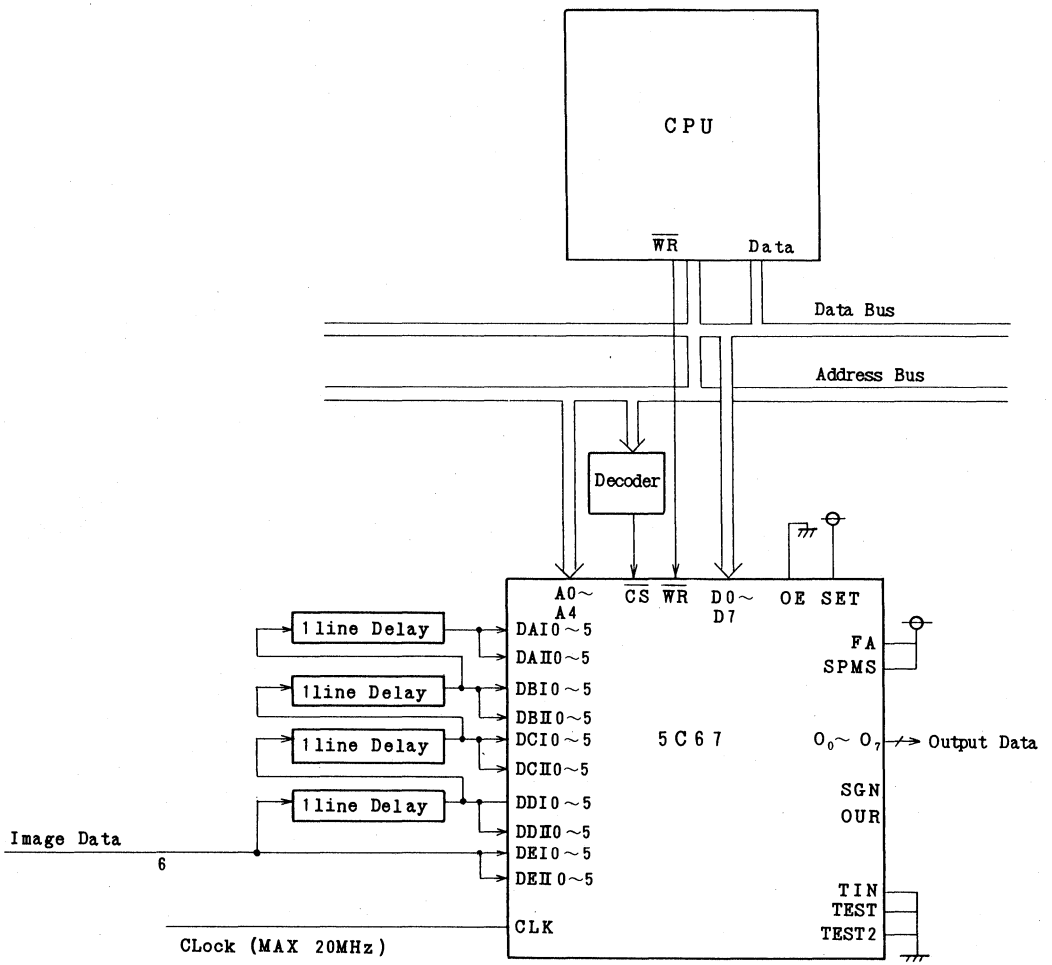


Parameter	Symbol	MIN	MAX	Unit
Clock Cycle	Ticyc	50	-	ns
Input pixel Set-up Time	TiST	30	-	ns
Input pixel Hold Time	TiHD	5	-	ns
Output pixel Delay Time	TiCD	-	30	ns
Output pixel Pipeline Delay Time	TiPD	Odd-Even mode 14		clock
		Serial mode 15		clock

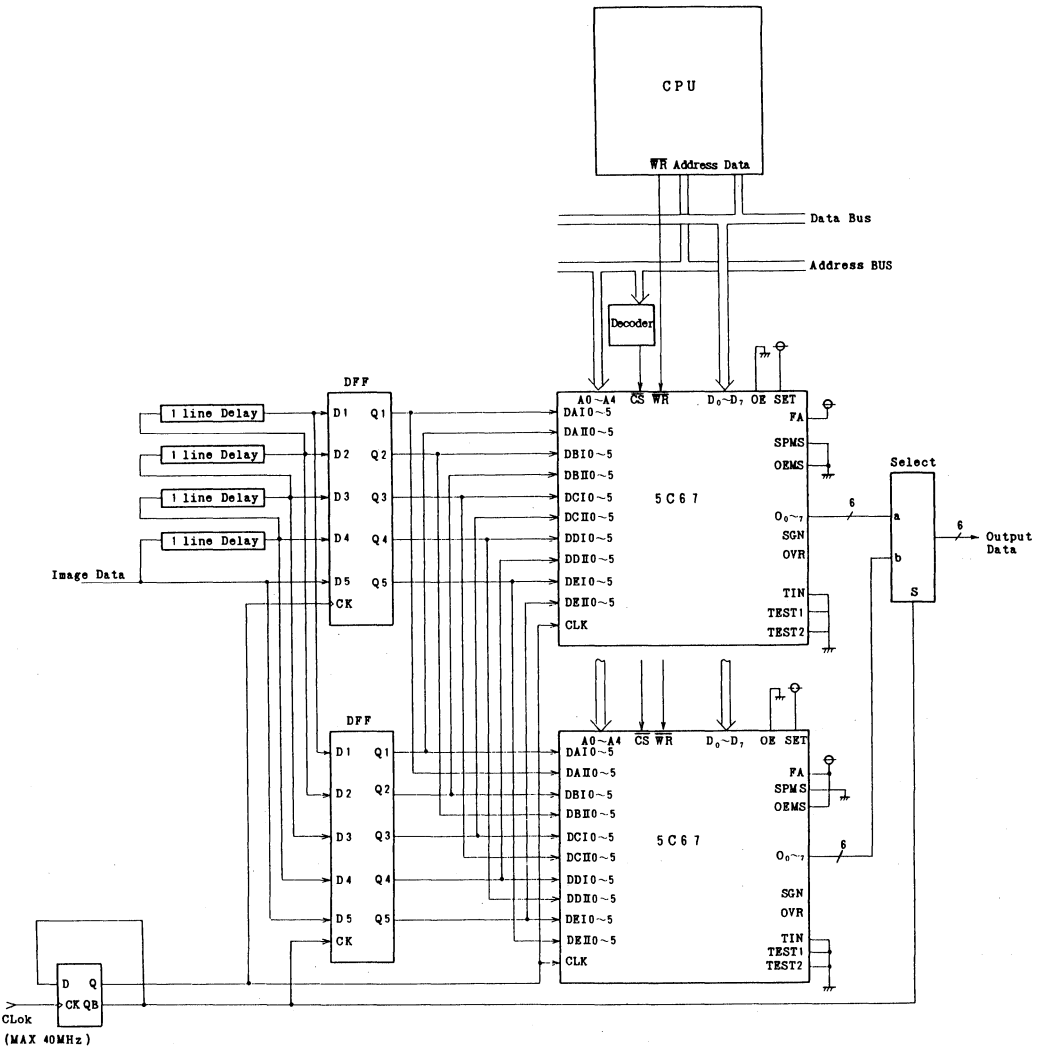
See data sheet for detail

■ System configuration example

1 For operation in the serial mode



2 For operation in the Odd-Even mode



Voltage Detector RX5VA series
Application Manual

Version 1.0

NO. EA-8-8809

RX5VA Application Manual

Contents

§1 Specifications

■ Outline

RX5VA series, developed with C-MOS processing technology are accurate, low-power-consumption voltage detectors. The detectors include comparators, output drivers and hysteresis circuit.

The value of detect voltage is set internally, and is accurately controlled by Laser Trimming.

There are three types of output: N-ch open-drain, P-ch open-drain, and C-MOS. There are two convenient packages: mini-power-mold and TO-92. The RX5VA series can be used as a reference voltage supply for ICs in many applications.

■ Features

- Extremely low power consumption ..... TYP. 1.0μA (VDD=3.0V)
- Wide voltage range ..... 1.5V to 10.0V
- Variety of detect voltage ..... 0.1V step
- High accuracy ..... ±2.5%
- Good temperature characteristic for detect voltage ..... TYP. ±100 PPM/°C
- Output Options ..... N-ch open drain, P-ch open drain, CMOS
- Compact Package ..... TO-92, min-power-mold

■ Applications

- Resets circuit of P-ch, N-ch, and C-MOS microcomputers
- Battery checker
- Logic circuit reset
- Level discriminator
- Waveform shaping circuit
- Switching circuit for battery backup
- Power failure detector

■ Block Diagram

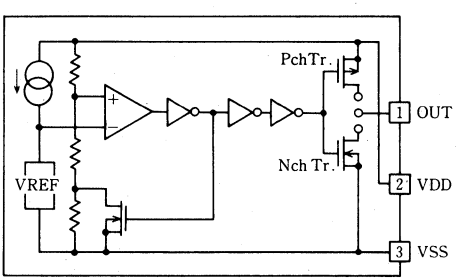


Fig. 1 Block Diagram

■ Pin Configuration

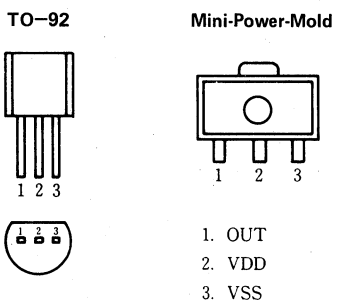


Fig. 2 Pin Configuration

■ System Block Diagrams

Figure 2 is block diagrams of RX5VA series and shows the system with three terminals. The system has three types of output drive : N-ch open-drain, P-ch open-drain, and C-MOS.

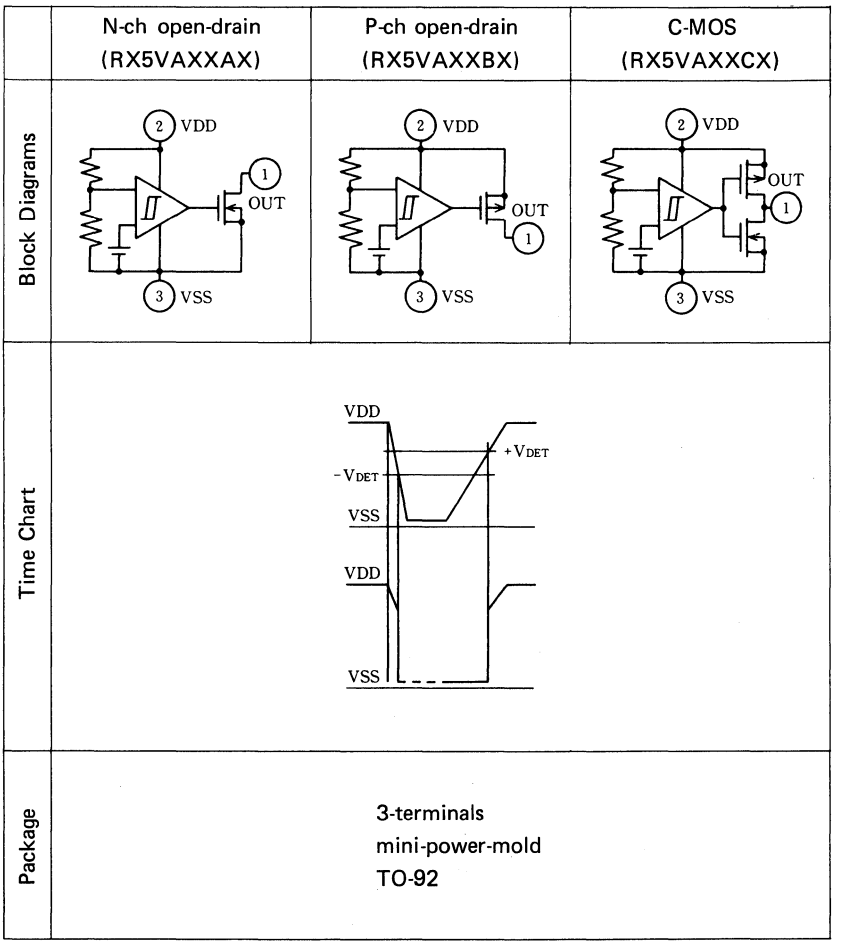


Fig. 3 System Block Diagram

■ Absolute Maximum Ratings

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	VDD	12	V
Output Voltage	VOUT	VSS−0.3～VDD+0.3	
Output Current	IOUT	70	mA
Power Dissipation	Pd	300	mW
Operating Temperature Range	Topr	−30～+80	°C
Storage Temperature Range	Tstg	−40～+125	
Soldering Temperature	Tsolder	260°C (10 Sec)	

■ Electrical Characteristics

Topr : 25°C

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Detect Voltage	−VDET		(−VDET) × 0.975		(−VDET) × 1.025	V
Hysteresis	VHYS			(−VDET) × 0.05		V
Supply Current	Iss	VDD= 2.0V		0.9	2.7	μA
		3.0V		1.0	3.0	
		4.5V		1.15	3.45	
		6.0V		1.3	3.9	
		10.0V		1.7	5.1	
Operating Voltage	VDD		1.5		10.0	V
Output Current	IOUT	Nch VDS=0.5V VDD:1.0V		0.5		mA
		2.4V		3.6		
		3.6V		6.5		
		4.6V		8.6		
		6.0V		11.6		
		10.0V		19.6		
		Pch VDS=2.1V VDD:4.5V	0.04			
Temperature Coefficient	Δ(−VDET) /ΔTa	−30°C ≦ Ta ≦ 80°C		±100		PPM/°C

■ Functional Description

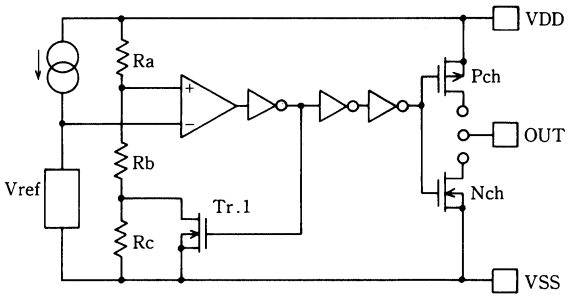


Fig. 4 Block Diagram

- In the case of the RX5VAXXA type, the drain of the Nch. transistor is connected to the OUT terminal.
- In the case of the RX5VAXXB type, the drain of the Pch. transistor is connected to the OUT terminal.
- In the case of the RX5VAXXC type, the drain of the Nch. transistor and the drain of the Pch. transistor are connected to the OUT terminal.

Operating Conditions

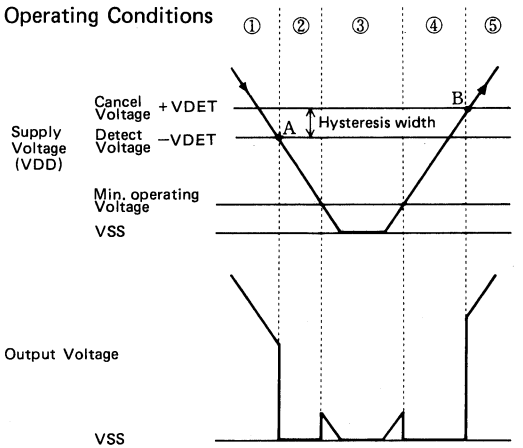


Fig. 5 Operating State Description

Internal Conditions

Operating State		①	②	③	④	⑤
Comparator (+) Input Voltage		I	II	II	II	I
Comparator Output		H	L	L	L	H
Tr..1		OFF	ON	ON	ON	OFF
Output Tr.	Pch	ON	OFF	X: Unstable	OFF	ON
	Nch	OFF	ON	X: Unstable	ON	OFF

I. $\frac{Rb+Rc}{Ra+Rb+Rc} \cdot VDD$

II. $\frac{Rb}{Ra+Rb} \cdot VDD$

Description of Operation

① Output voltage is equal to supply voltage (VDD).

② On the A point, Vref ≧ VDD · (Rb + Rc) / (Ra + Rb + Rc) and then the output of the comparator is inverted to VSS.
The A point shows the detect voltage (-VDET).

③ When the supply voltage is smaller than the minimum operating voltage, the output transistor becomes "Unstable" and outputs VDD voltage if the output is pulled up.

④ Output voltage is equal to VSS.

⑤ On the B point, Vref ≦ VDD . Rb/(Ra + Rb) and then the output of the comparator is inverted to VDD.
The B point shows the cancel voltage (+VDET).
The hysteresis width is the difference between the cancel voltage (+VDET) and the detect voltage (-VDET).

■ Measurement Circuit

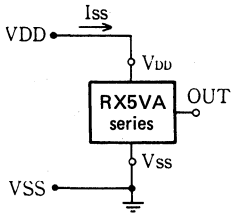


Fig. 6 Consumption Current Measurement Circuit

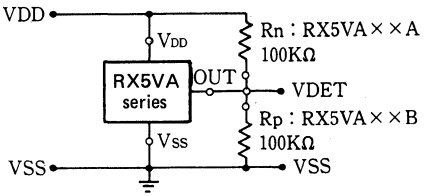


Fig. 7 Voltage Detect Measurement Circuit

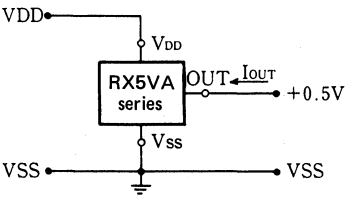


Fig. 8 Nch Driver Output Current Measurement Circuit

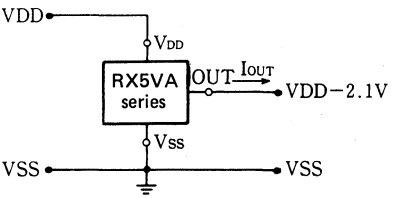


Fig. 9 Pch Driver Output Current Measurement Circuit

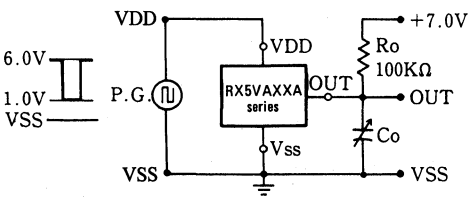


Fig. 10 Propagation Delay Time Measurement Circuit (1)

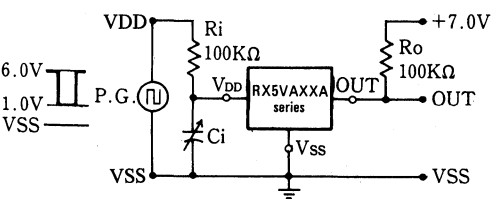


Fig. 11 Propagation Delay Time Measurement Circuit (2)

■ Example of the RE5VA40C

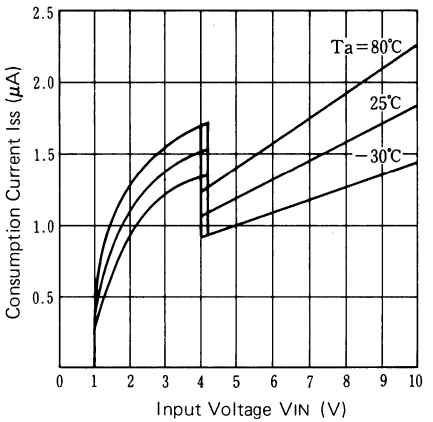


Fig. 12 Consumption Current – Input Voltage

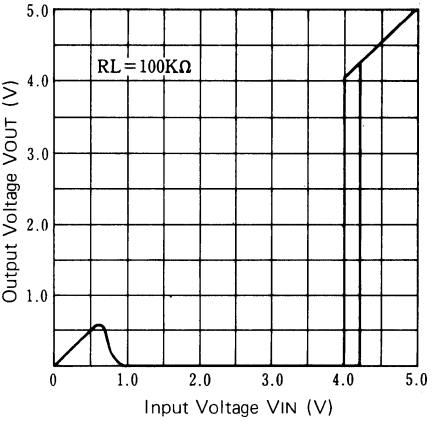


Fig. 13 Output Voltage – Input Voltage

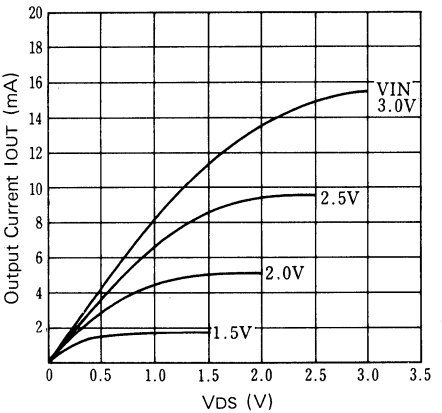


Fig. 14 Nch Driver Output Current – VDS

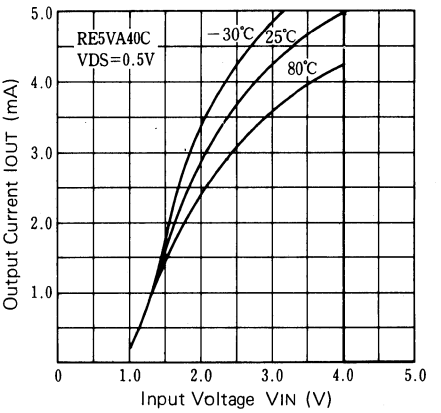


Fig. 15 Nch Driver Output Current – Input Voltage

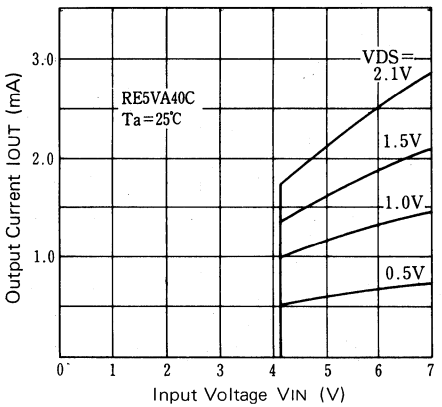


Fig. 16 Pch Driver Output Current – Input Voltage

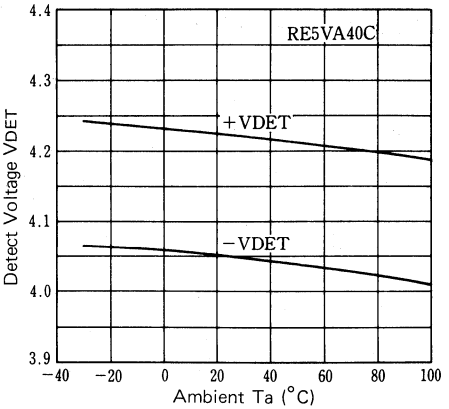


Fig. 17 Detect Voltage – Ambient Temperature

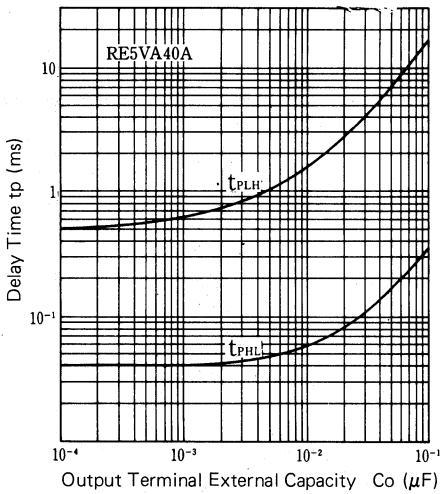


Fig. 18 Propagation Delay Time – Output Terminal External Capacity

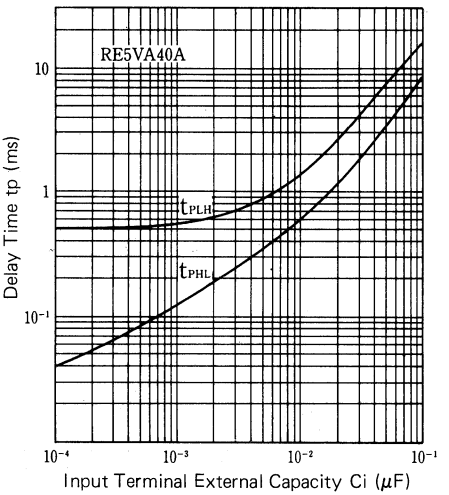


Fig. 19 Propagation Delay Time – Input Terminal External Capacity

■ Package Information

* SOT–89 Mini-Power-Mold · Plastic Package

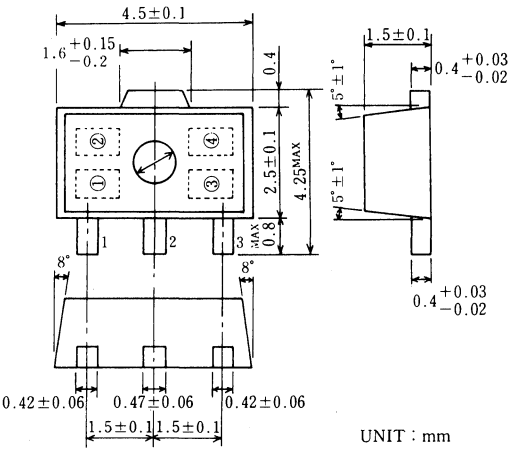


Fig. 20

- Pin Configuration

1 : OUT
2 : VDD
3 : VSS

- Mark

①② : Type Number (Code Number)
③④ : Lot Number

* TO–92 Plastic Package

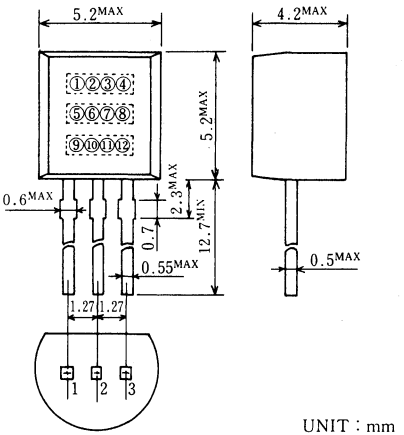


Fig. 21

* TO–92 Plastic Package for Taping Method

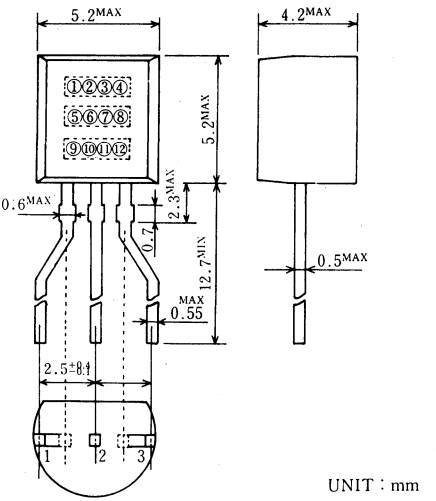


Fig. 22

- Pin Configuration

1 : OUT
2 : VDD
3 : VSS

- Mark

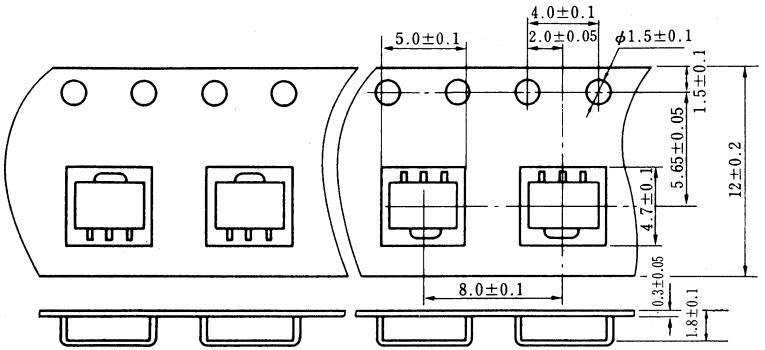
①②③④⑤⑥⑦⑧ : Type Number
⑨⑩⑪⑫ : Lot Number

■ Taping Specification

* SOT–89 Mini-Power-Mold · Plastic Package

● Tape Dimension and Direction

2 kinds of taping method (T1, T2) are available.

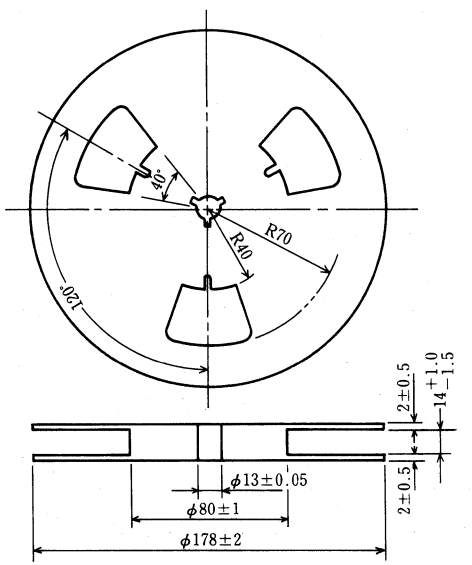


T1 Type T2 Type UNIT : mm

Fig. 23

● Reel Dimension

1000 pieces can be contained in one reel.



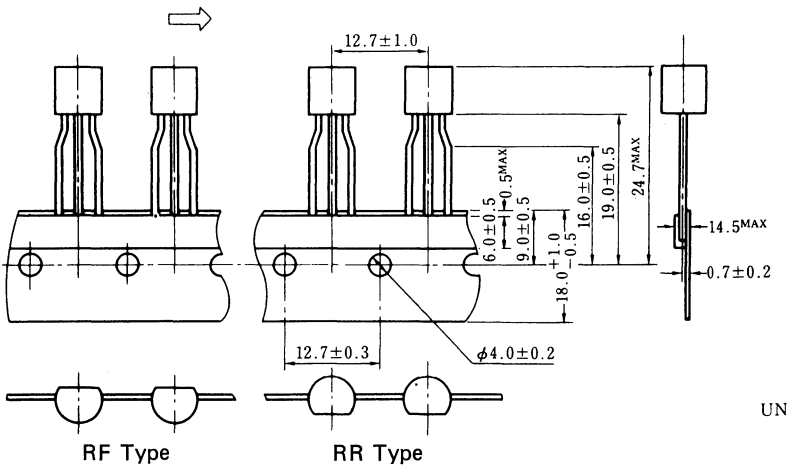
UNIT : mm

Fig. 24

* TO–92 Plastic Package

● Tape Dimension and Direction

2 kinds of Taping Method (RF, RR) are available.

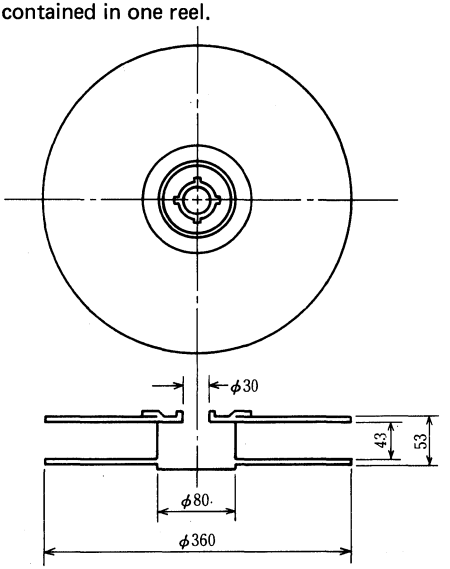


UNIT : mm

Fig. 25

● Reel Dimension

2000 pieces can be contained in one reel.

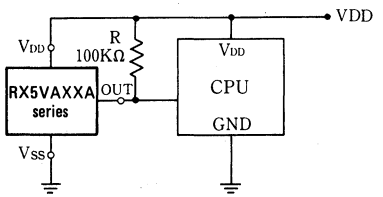


UNIT : mm

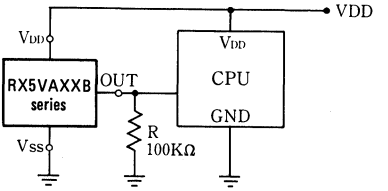
Fig. 26

§2 Application

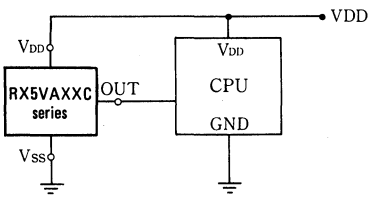
■ RX5VAXXA Standard Circuit
(Nch Open drain)



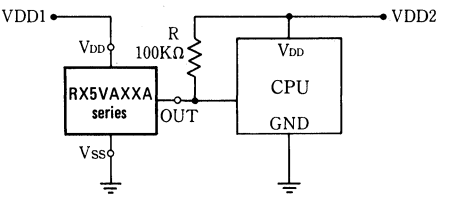
■ RX5VAXXB Standard Circuit
(Pch Open drain)



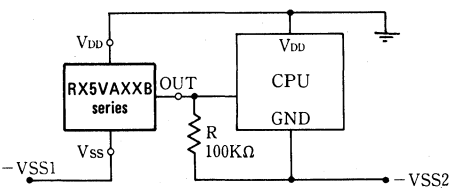
■ RX5VAXXC Standard Circuit
(C–MOS Output)

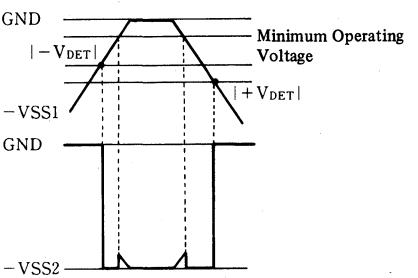


■ RX5VAXXA Sprit VDD Sources
(Nch Open drain)

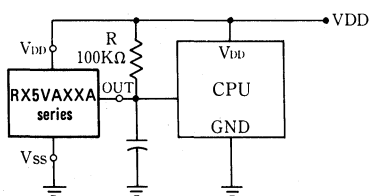


■ RX5VAXXB Sprit Vss Sources
(Pch Open drain)

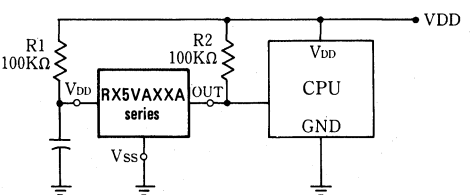




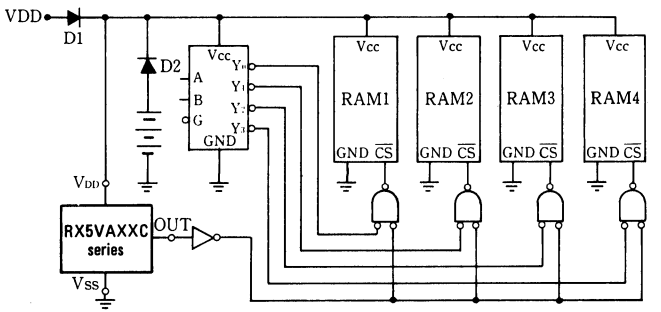
■ RX5VAXXA Propagation Delay Circuit (1)
(Nch Open drain)



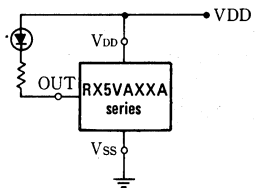
■ RX5VAXXA Propagation Delay Circuit (2)
(Nch Open drain)



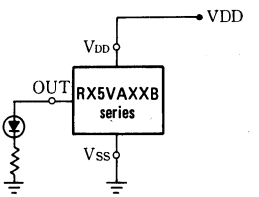
■ Memory · Backup Circuit



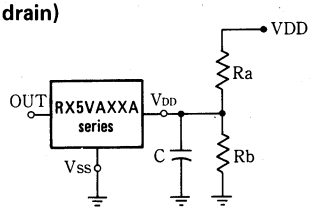
■ Voltage Level Indicator LED Driver Circuit (Nch Open drain)



■ Voltage Level Indicator LED Driver Circuit (Pch Open drain)



■ Higher Voltage Detector (Nch Open drain)

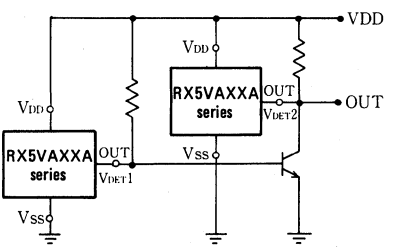


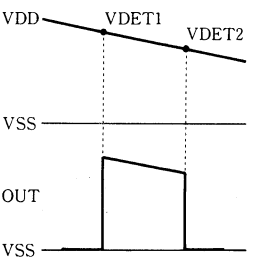
$$\text{Detect Voltage} = \frac{Ra+Rb}{Rb} \cdot (-VDET)$$

$$\text{Hysteresis Voltage} = \frac{Ra+Rb}{Rb} \cdot (-VHYS)$$

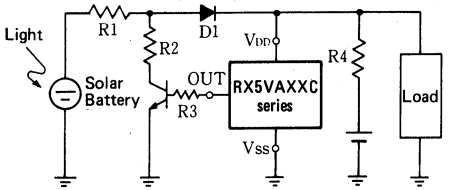
Note) The detect voltage may be different from the calculated voltage value due to the voltage drop that derives from increase of the current at the Ra of the IC when the value of Ra is large.

■ Window Comparator Circuit (Nch Open drain)





■ Over-Charge Protection



* Note

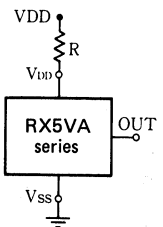


Fig. 27

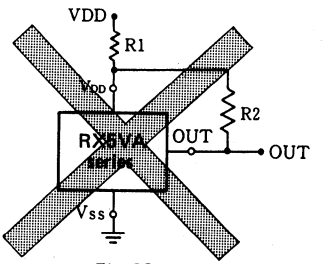


Fig. 28

1. Don't connect an impedance between VDD and V_{DD} of the RX5VAXXB or the RX5VAXXC as shown in Fig. 27, or oscillation may happen.

   In use of the RX5VAXXA series, the detect voltage may change due to the voltage drop that derives from increase of the current in the IC when R is large.

2. Don't connect as shown as Fig. 28 in all RX5VA series, or oscillation may happen.

§3 Selection Guide

■ Selection Guide

You can define several options, including output driver type, package and packing method with the RX5VA series.

The devices are defined by the following characters.

R X 5 V A X X X X ← Type number

↑ ↑ ↑ ↑

a b c d

Character	Meaning
a	Defines the packaging type E : TO-92 H : Mini-power-mold
b	Defines the voltage value that is to be monitored (−VDET) The monitor range is 2.00V to 6.00V in 0.1V units, with an accuracy of ±2.5%
c	Defines the output type A : N-ch open drain B : P-ch open drain C : C-MOS
d	Defines the packing method A-T1 : Taping-T1 type A-T2 : Taping-T2 type A-RF : Taping-RF type A-RR : Taping-RR type B : Gluing (Gluing is for mini power mold package as a sample) C : Electric conductive bagging (for TO-92)

Table 1

● Type Number Example

Type number	Voltage Detect (−VDET)			Output Driver			Package	Packing method
	MIN.(V)	TYP.(V)	MAX.(V)	N-ch Open-Drain	P-ch Open-Drain	C-MOS		
RX5VA20AX RX5VA20BX RX5VA20CX	1.950	2.000	2.050	○	○	○	E: TO-92 H: Minipower mold (SOT-89)	A: Taping B: Gluing C: Electric Conductive bagging
RX5VA21AX RX5VA21BX RX5VA21CX	2.048	2.100	2.152	○	○	○		
RX5VA27AX RX5VA27BX RX5VA27CX	2.633	2.700	2.767	○	○	○		
RX5VA45AX RX5VA45BX RX5VA45CX	4.388	4.500	4.612	○	○	○		
RX5VA47AX RX5VA47BX RX5VA47CX	4.583	4.700	4.817	○	○	○		
RX5VA55AX RX5VA55BX RX5VA55CX	5.363	5.500	5.637	○	○	○		

Table 2

* Consult the guide to determine specifications other than those shown in Table 2. Use the type number.

Voltage Regulator RX5RAseries
Application Manual

Version 1.0

EA-7-8809

Contents

§ 1 Specifications

■ OUTLINE

The RX5RA series, developed with C-MOS processing technology, are highly accurate, low-power-consumption, fixed three terminal voltage regulators. They include reference voltage supply, error amplifier, control transistor, and resistor network to control the output voltage. The output voltage is fixed in the IC.
The RX5RA series are both available in two different types of package: mini-power-mold and TO-92.

■ FEATURES

- Extremely low power consumption ..... TYP. 1.0μA Vout = 3.0V
- Small input-output voltage difference ..... TYP. 60mV Iout = 1.0mA
- Low temperature coefficient for output voltage ..... TYP. ±100PPM/°C
- Stable input rate ..... TYP. 0.1%/V
- Accurate output voltage ..... ±2.5%
- Variety of output voltage levels ..... 0.1V step
- Compact package ..... TO-92, mini power mold

■ APPLICATIONS

- Constant-voltage power supply for battery-powered devices
- Constant-voltage power supply for camera, communication, and video equipment
- Stable standard voltage supply

■ BLOCK DIAGRAM

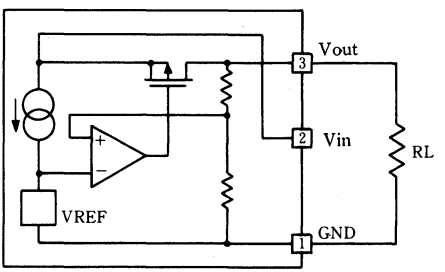


Fig. 1 Block Diagram

■ PIN CONFIGURATION

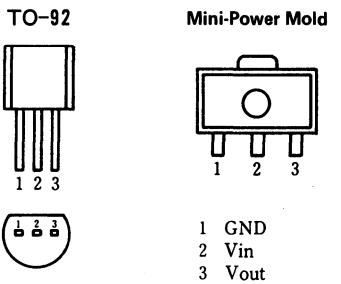


Fig. 2 Pin Configuration

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage	Vin	+12	V
Output Current	Iout	150	mA
Output Voltage	Vout	Vin+0.3～−0.3	V
Power Dissipation	Pd	300	mW
Operating Temperature Range	Topr	−30～+80	℃
Storage Temperature Range	Tstg	−40～+125	
Soldering Temperature	Tsolder	260℃ 10Sec	

■ ELECTRICAL CHARACTERISTICS

Topr : 25℃

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vout	Iout=10mA	(Vout) ×0.975		(Vout) ×1.025	V
Output Current	Iout	Vin−Vout =2.0V Vout =3.0V Vout =5.0V		40 60		mA
Load Regulation	△Vout	Vin−Vout =2.0V Vout =3.0V 1mA≦Iout≦20mA Vout =5.0V 1mA≦Iout≦40mA		60 40		mV
Input-Output Voltage Difference	Vdif	Iout=1mA Vout =3.0V =5.0V		60 30		mV

■ ELECTRICAL CHARACTERISTICS

Topr : 25℃

Type Number	Output Voltage				Output Current				Load Regulation				Input-Output Voltage Difference				Quiescent Current			
	Vout (V)				Iout (mA)				△Vout (mV)				Vdif (mV)				Iss (μA)			
	Condition	MIN.	TYP.	MAX.	Condition	MIN.	TYP.	MAX.	Condition	MIN.	TYP.	MAX.	Condition	MIN.	TYP.	MAX.	Condition	MIN.	TYP.	MAX.
RX5RA20A×	Vin-Vout =2.0V Iout =10mA	1.950	2.000	2.050	Vin-Vout =2.0V	20	30		Vin-Vout =2.0V 1mA≦Iout≦20mA		60	90	Iout=1mA		80	160	Vin-Vout =2.0V		1.0	3.0
RX5RA21A×		2.048	2.100	2.152																
RX5RA22A×		2.145	2.200	2.255																
RX5RA23A×		2.243	2.300	2.357																
RX5RA24A×		2.340	2.400	2.460											70					
RX5RA25A×		2.438	2.500	2.562																
RX5RA26A×		2.535	2.600	2.665																
RX5RA27A×		2.633	2.700	2.767																
RX5RA28A×		2.730	2.800	2.870											60					
RX5RA29A×		2.828	2.900	2.972																
RX5RA30A×		2.925	3.000	3.075		27	40		Vin-Vout =2.0V 1mA≦Iout≦40mA						50	100			1.1	3.3
RX5RA31A×		3.023	3.100	3.177																
RX5RA32A×		3.120	3.200	3.280																
RX5RA33A×		3.218	3.300	3.382																
RX5RA34A×		3.315	3.400	3.485																
RX5RA35A×		3.413	3.500	3.587																
RX5RA36A×		3.510	3.600	3.690											40					
RX5RA37A×		3.608	3.700	3.792																
RX5RA38A×		3.705	3.800	3.895																
RX5RA39A×		3.705	3.900	3.997																

Topr : 25℃

Type Number	Output Voltage				Output Current				Load Regulation				Input-Output Voltage Difference				Quiescent Current			
	Vout〔V〕				Iout〔mA〕				△Vout〔mV〕				△Vdif〔mV〕				Iss〔μA〕			
	Condition	MIN.	TYP.	MAX.	Condition	MIN.	TYP.	MAX.	Condition	MIN.	TYP.	MAX.	Condition	MIN.	TYP.	MAX.	Condition	MIN.	TYP.	MIX.
RX5RA40A×	Vin-Vout =2.0V Iout =10mA	3.900	4.000	4.100	Vin-Vout =2.0V				Vin-Vout =2.0V				Iout= 1mA				Vin-Vout =2.0V			
RX5RA41A×		3.998	4.100	4.202																
RX5RA42A×		4.095	4.200	4.305																
RX5RA43A×		4.193	4.300	4.407																
RX5RA44A×		4.290	4.400	4.510		33	50												1.2	3.6
RX5RA45A×		4.388	4.500	4.612																
RX5RA46A×		4.485	4.600	4.715																
RX5RA47A×		4.583	4.700	4.817																
RX5RA48A×		4.680	4.800	4.920																
RX5RA49A×		4.778	4.900	5.022																
RX5RA50A×		4.875	5.000	5.125					1mA≦ Iout ≦20mA		40	60			30	60				
RX5RA51A×		4.973	5.100	5.227																
RX5RA52A×		5.070	5.200	5.330																
RX5RA53A×		5.168	5.300	5.432																
RX5RA54A×		5.265	5.400	5.535																
RX5RA55A×		5.363	5.500	5.637		40	60												1.3	3.9
RX5RA56A×		5.460	5.600	5.740																
RX5RA57A×		5.558	5.700	5.842																
RX5RA58A×		5.655	5.800	5.945																
RX5RA59A×		5.753	5.900	6.047																
RX5RA60A×		5.850	6.000	6.150																

■ OPERATIONAL EXPLANATION

OPERATION

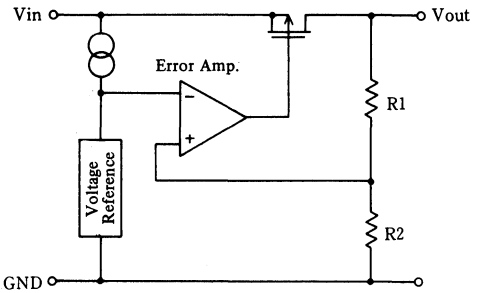


Fig. 3 Block Diagram

The variation of output voltage, Vout, is sent to an error amplifier by feedback resistors R1 and R2. The error amplifier compares the variation with reference voltage, compensates it to the opposite direction, and adjusts the Regulator to nominal output voltage.

■ MEASUREMENT CIRCUIT

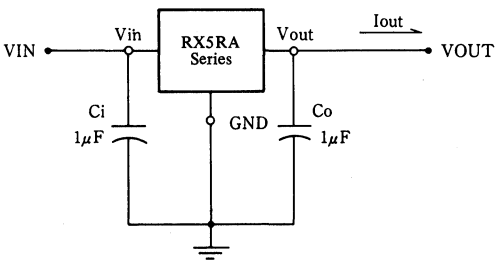


Fig. 4 Measurement Circuit

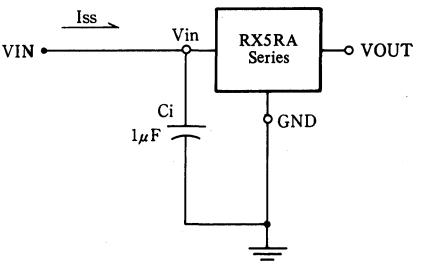


Fig. 5 Quiescent Current Measurement Circuit

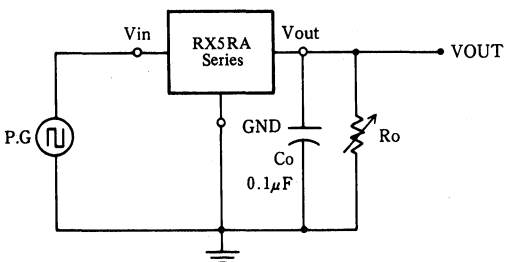


Fig. 6 Input Transition Responce Measurement Circuit

■ TYPICAL CHARACTERISTICS CURVES (Example of the RH5RA50A)

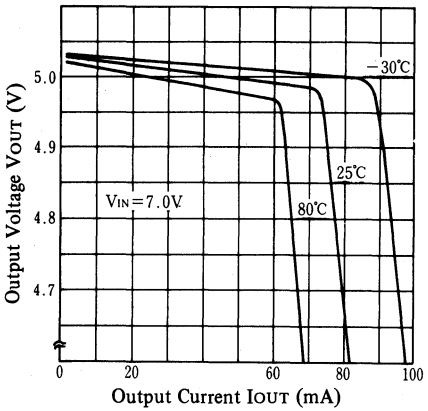


Fig. 7 Output Voltage–Output Current

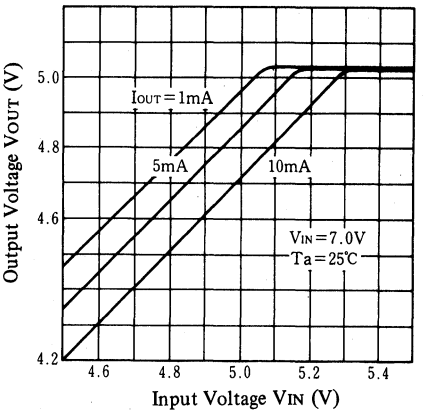


Fig. 8 Output Voltage–Input Voltage

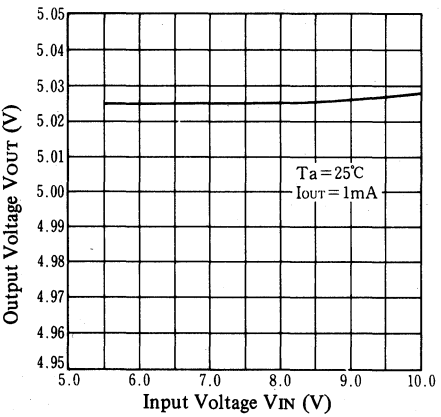


Fig. 9 Output Voltage–Input Voltage

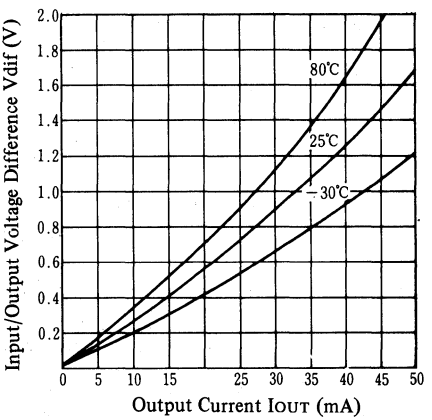


Fig. 10 Input/Output Voltage Difference–Output Current

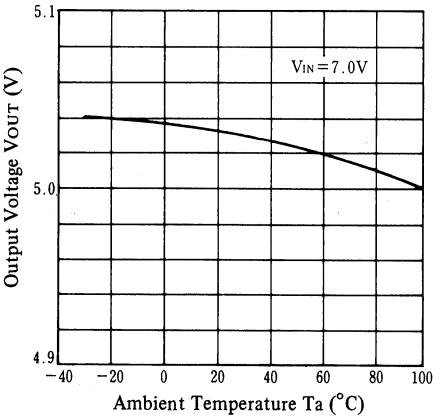


Fig. 11 Output Voltage–Ambient Temperature

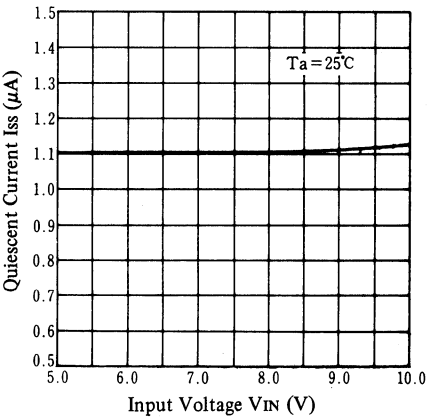


Fig. 12 Quiescent Current–Input Voltage

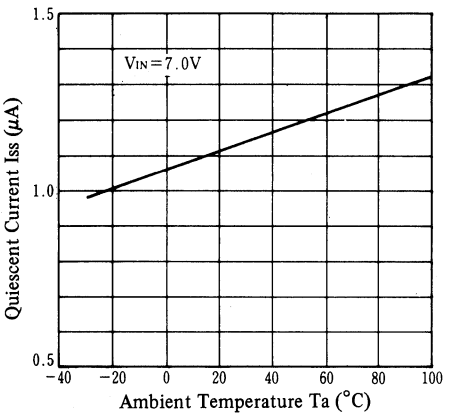


Fig. 13 Quiescent Current–Ambient Temperature

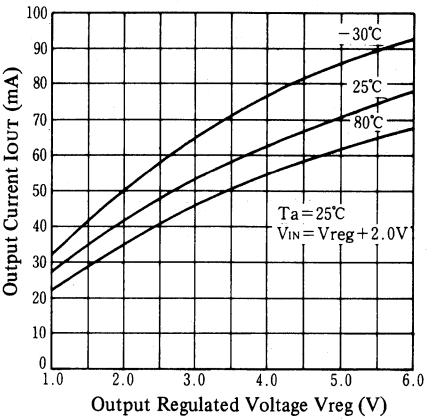


Fig. 14 Output Current–Output Regulated Voltage

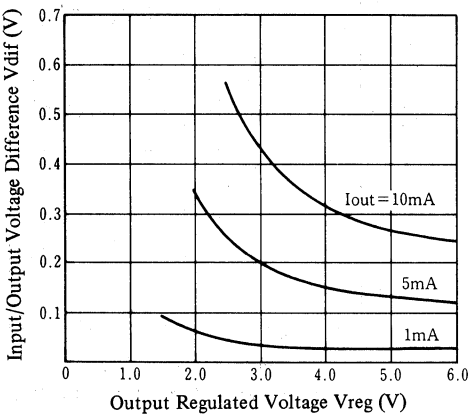


Fig. 15 Input/Output Voltage Difference–Output Regulated Voltage

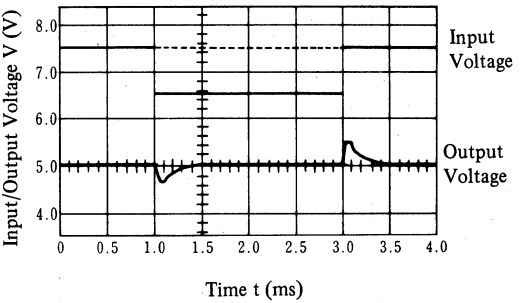


Fig. 16 Input Transition Responce 1 (Iout = 1 mA)

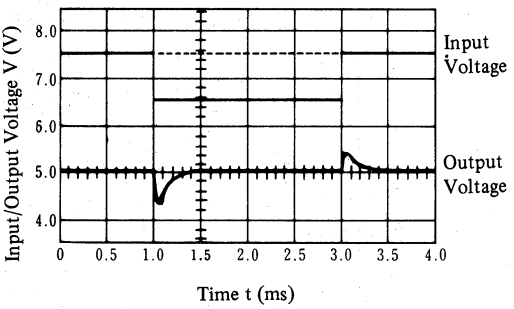


Fig. 17 Input Transition Responce 2 (Iout = 10 mA)

■ PACKAGE INFORMATION

* SOT-89 Mini-Power-Mold · Plastic Package

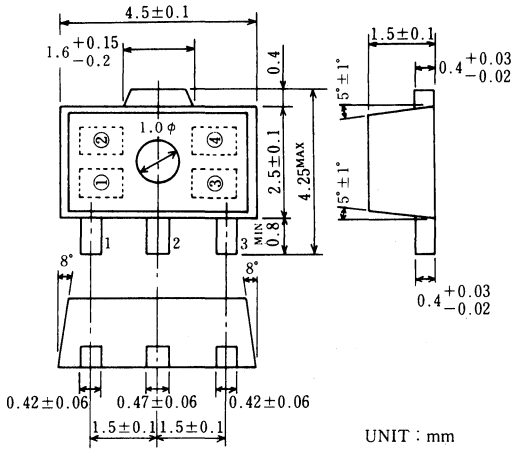


Fig. 18 SOT-89

• Pin Configuration

1 : GND
2 : Vin
3 : Vout

• Mark

①② : Code Number
③④ : Lot Number

* TO-92 Plastic Package

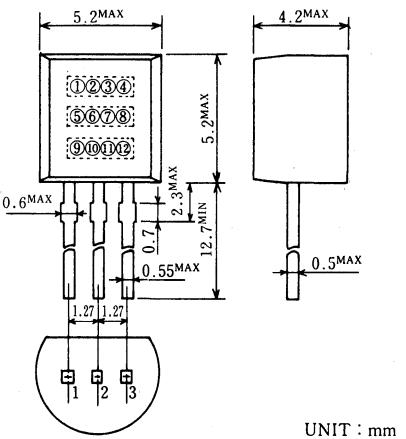


Fig. 19 TO-92

* TO-92 Plastic Package for Taping Method

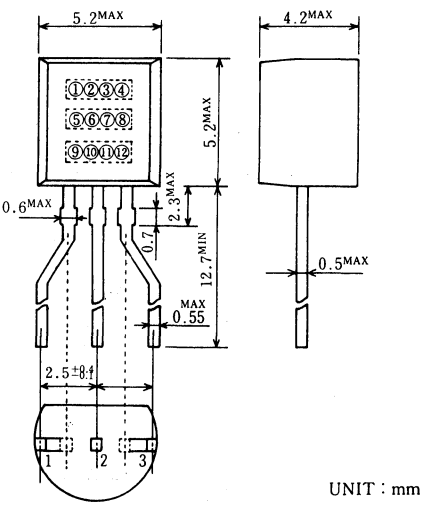


Fig. 20 TO-92

• Pin Configuration

1 : GND
2 : Vin
3 : Vout

• Mark

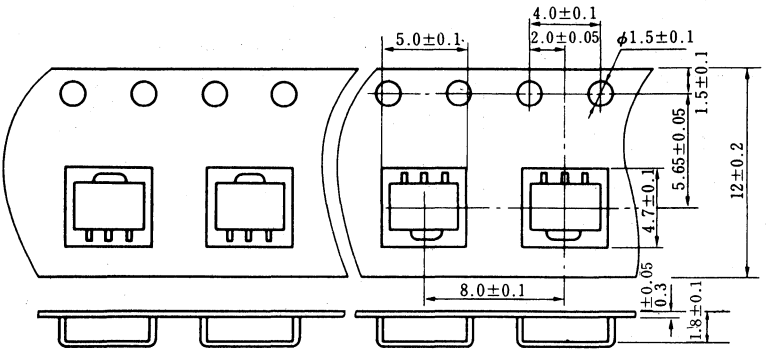
①②③④⑤⑥⑦⑧ : Type Number
⑨⑩⑪⑫ Lot Number

■ TAPING SPECIFICATION

* SOT-89 Mini-Power-Mold · Plastic Package

- Tape Dimension and Direction

2 Kinds of Taping Method (T1, T2) are available.

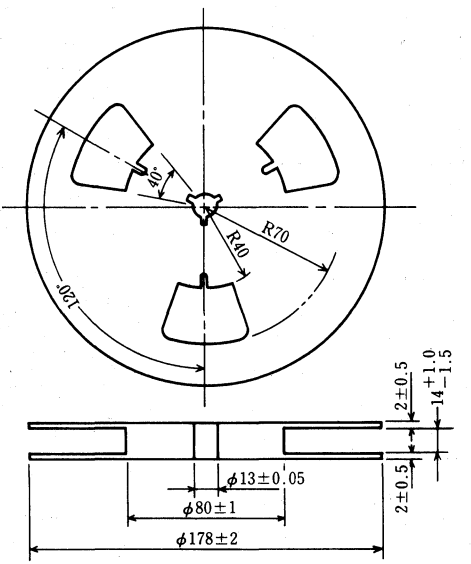


T1 Type T2 Type UNIT : mm

Fig. 21

- Reel Dimension

1000 pieces can be contained in one reel.



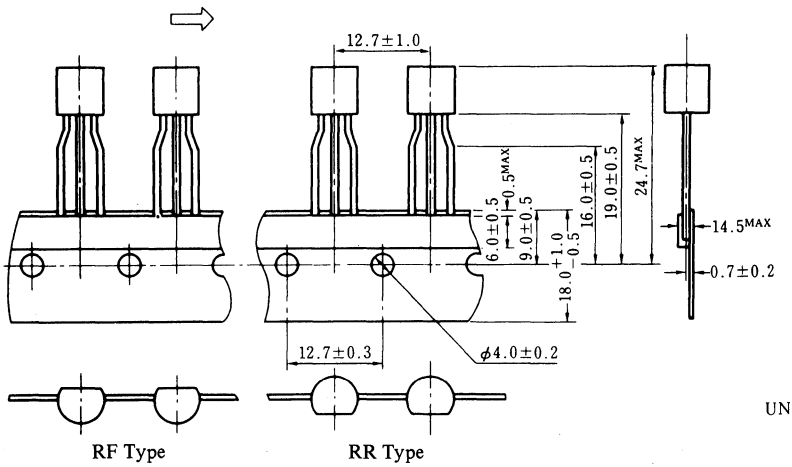
UNIT : mm

Fig. 22

* TO-92 Plastic Package

- Tape Dimension and Direction

2 Kinds of Taping Method (RF, RR) are available.

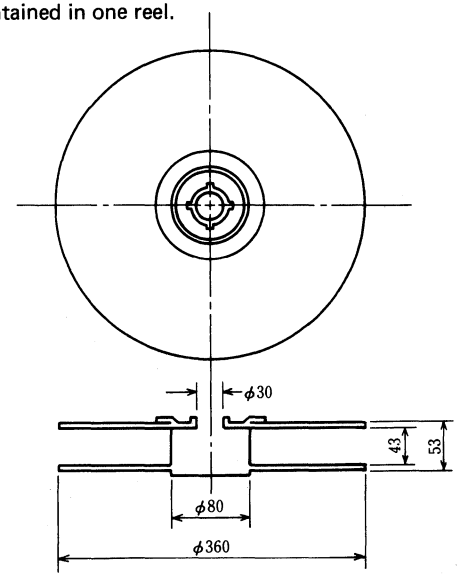


UNIT : mm

Fig. 23

- Reel Dimension

2000 pieces can be contained in one reel.

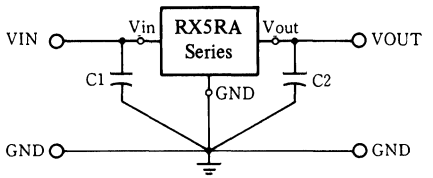


UNIT : mm

Fig. 24

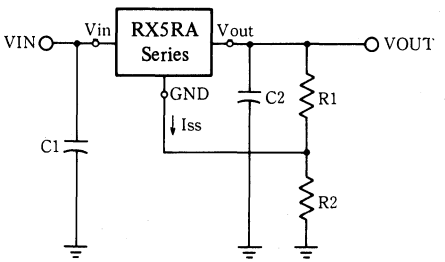
§2 Application

■ STANDARD CIRCUIT



RX5RA series can regulate voltage without capacitor C1 and C2. When the input wire is long, use capacitor C1. Capacitor C2 makes the transient of output load variation smaller.
Keep the wiring as short as possible when putting capacitor C1 and C2 of 0.1 μF to 2.0 μF between regulator terminals and GND terminal.

■ INCREASED VOLTAGE CIRCUIT



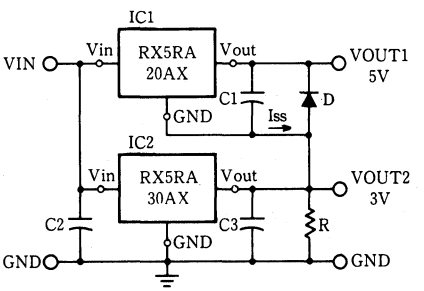
The following equation explains the output voltage.

$$VOUT = Vreg_{*}(1 + R2/R1) + Iss \cdot R2$$

The RX5RA series use low supply current, so R1 and R2 can be set high (several hundred k ohms) and supply current of the whole circuit itself can be kept low.
RX5RA works with constant current, so the input voltage scarcely affects supply current of the circuit.

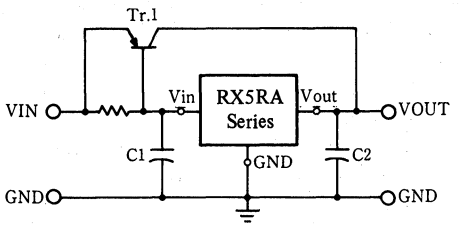
* Vreg: Fixed output voltage of RX5RA series

■ DUAL VOLTAGE CIRCUIT



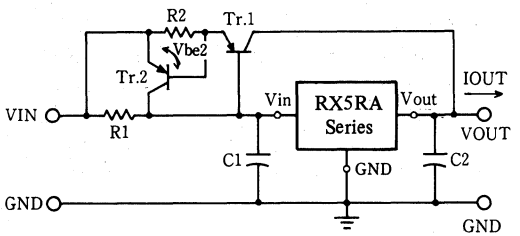
As the figure shows, two RX5RA devices can be made into a dual power circuit.
The figure shows examples with output of 3V and 5V. R is not needed when the minimum load current of IC2 is larger than Iss of IC1. Diode D protects IC1 when VOUT2 larger than VOUT1.

■ CURRENT BOOST CIRCUIT



When an output voltage more above 60 mA is necessary, construct a current boost circuit as shown in the figure.

■ CURRENT BOOST CIRCUIT with OVER-CURRENT PROTECTION



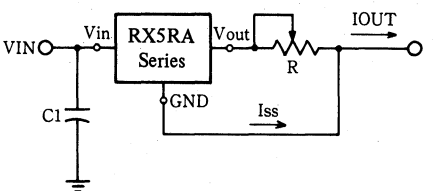
The figure on the left explains the circuit construction to protect Tr.1 from short output circuit or over current.

By adding Tr.2 and R2 to current boost circuit (above figure), voltage drops to Vbe2 of Tr.2 because of current through R2 (≒ IOUT). When it drops, Tr.2 will be on and will supply current to Tr.1 base. Tr.1 will be off and will limit output current.

The following equation explains the operation current of the overcurrent protection circuit.

IOUT = Vbe/R2

■ CONSTANT CURRENT POWER SUPPLY



As the figure shows, the construction can be used as constant current power supply. Output current, IOUT, can be found by the following equation.

IOUT = Vreg/R + Iss

Do not exceed the allowable current.

Vreg: Fixed output voltage of RX5RA series

§3 Selection Guide

■ SELECTION GUIDE

You can define the output voltage and package of the RX5RA series.
The devices are defined by the following characters.

R X 5 R A X X X X ← Type number

↑ ↑ ↑ ↑
a b c d

No.	Meaning
a	Defines the packaging type E : TO-92 H : Mini power mold (SOT-89)
b	Defines output voltage (Vout) The range for Vout is 2.0V to 6.0V in units of 0.1V, with an accuracy of ±2.5%.
c	Defines the output current type A : Standard type
d	Defines the packaging method for shipment A-T1 : Taping-T1 type (See Fig. 2) A-T2 : Taping-T2 type (See Fig. 2) A-RF : Taping-RF type (See Fig. 2) A-RR : Taping-RR type (See Fig. 2) B : Gluing (Gluing is for mini power mold package as a sample) C : Electric conductive bagging (for TO-92)

Table 1

- Type Number Example

Type numbers	output voltage(Vout)			Package	Packing method
	MIN.(V)	TYP.(V)	MAX.(V)		
RX5RA21AX	2.048	2.100	2.152	E:TO-92 H:Mini power mold	A:Taping B:Gluing C:Electric conductive bagging
RX5RA30AX	2.925	3.000	3.075		
RX5RA33AX	3.218	3.300	3.382		
RX5RA37AX	3.608	3.700	3.792		
RX5RA40AX	3.900	4.000	4.100		
RX5RA50AX	4.875	5.000	5.125		
RX5RA60AX	5.850	6.000	6.150		

Table 2

* Following the selection guide, determine specification other than those shown in Table 2. Use the type number.

Voltage Regulator RX5REseries
Application Manual

EA-016-8911

RX5RE Application Manual

Contents

§1 Specification

The RX5RE series, developed with CMOS processing technology, are highly accurate, low power consumption, large output current 3-terminal voltage Regulators. They include reference voltage supply, error amplifier, control transistor, and resistor network to control the output voltage. Because of small input-output voltage difference, effective constant-voltage power supply can be designed. The RX5RE series have a current control circuit to protect themself from the destruction due to over current. The output voltage is fixed in the device. The RX5RE series are both available in two different types of package: mini-power-mold and TO-92.

■ FEATURES

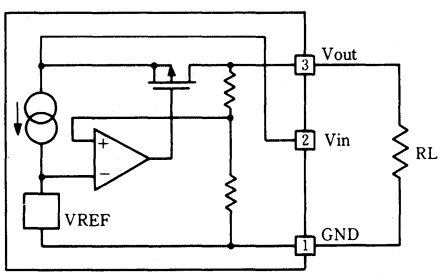
- Extremely low power consumption ..... TYP. 1.1μA (RX5RE30X, Vin = 5.0V)
- Small input-output voltage difference ..... TYP. 0.5V Iout = 60mA (RX5RE50X)
- Large output current ..... TYP. 120mA (RX5RE50X)
- Low temperature coefficient for output voltage ... TYP. ±100PPM/°C
- Wide operating voltage range ..... MAX. 10.0V
- Stable input rate ..... TYP. 0.1%/V
- Accurate output voltage ..... ±2.5%
- Variety of output voltage levels ..... 0.1V step (Note)
- Compact package ..... TO-92, mini power mold

(Note: RX5RE30X and RX5RE50X are standard. Custom type is also available.)

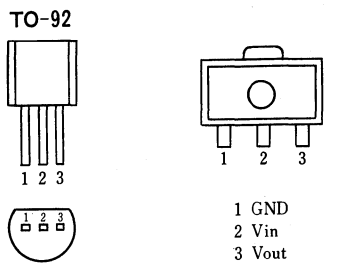
■ APPLICATIONS

- Constant-voltage power supply for battery-powered devices
- Constant-voltage power supply for camera, communication, and video equipment
- Stable standard voltage supply

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage	Vin	+12	V
Output Current	Iout	150	mA
Output Voltage	Vout	Vin+0.3～−0.3	V
Power Dissipation	Pd	300	mW
Operating Temperature Range	Topr	−30～+80	℃
Storage Temperature Range	Tstg	−40～+125	
Soldering Temperature	Tsolder	260℃ 10Sec	

■ RX5RE50X (Vout = 5.0V)

Topr : 25°C

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vout	Iout = 10mA	4.875	5.000	5.125	V
Output Current	Iout	Vin = 7.0V	80	120		mA
Load Regulation	ΔVout	Vin = 7.0V, 1mA ≦ Iout ≦ 80mA		40	80	mV
Input-Output Voltage Difference	Vdif	Iout = 60mA		0.5	0.7	V
Consumption Current	Iss	Vin = 7.0V		1.3	3.9	μA
Line Regulation	$\frac{\Delta Vout}{\Delta Vin \cdot Vout}$	Iout = 10mA | Vout | + 1.0V ≦ | Vin | ≦ 10V		0.1		%/V
Input Voltage	Vin				10	V
Limit Current	Ilim			240		mA
Temperature Coefficient	$\frac{\Delta Vout}{\Delta Topr}$	Iout = 10mA −30°C ≦ Topr ≦ 80°C		±100		$\frac{PPM}{°C}$

■ RX5RE30X (Vout = 3.0V)

Topr : 25°C

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vout	Iout = 10mA	2.925	3.000	3.075	V
Output Current	Iout	Vin = 5.0V	50	80		mA
Load Regulation	ΔVout	Vin = 5.0V, 1mA ≦ Iout ≦ 60mA		40	80	mV
Input-Output Voltage Difference	Vdif	Iout = 40mA		0.5	0.7	V
Consumption Current	Iss	Vin = 5.0V		1.1	3.3	μA
Line Regulation	$\frac{\Delta Vout}{\Delta Vin \cdot Vout}$	Iout = 10mA | Vout | + 1.0V ≦ | Vin | ≦ 10V		0.1		%/V
Input Voltage	Vin				10	V
Limit Current	Ilim			240		mA
Temperature Coefficient	$\frac{\Delta Vout}{\Delta Topr}$	Iout = 10mA −30°C ≦ Topr ≦ 80°C		±100		$\frac{PPM}{°C}$

■ DESCRIPTION OF OPERATION

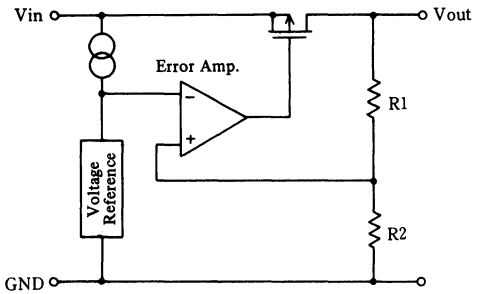


Fig. 3 Block Diagram

The variation of output voltage, Vout, is sent to an error amplifier by feedback resistors R1 and R2. The error amplifier compares the variation with reference voltage, compensates it to the opposite direction, and adjusts the Regulator to nominal output voltage.

■ MEASUREMENT CIRCUIT

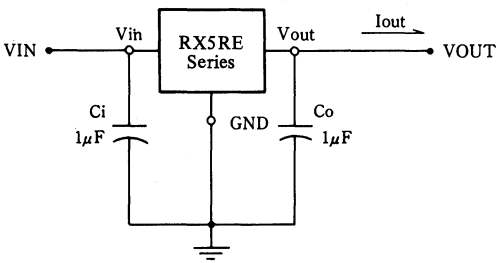


Fig. 4 Measurement Circuit

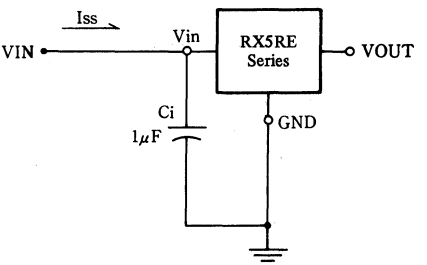


Fig. 5 Quiescent Current Measurement Circuit

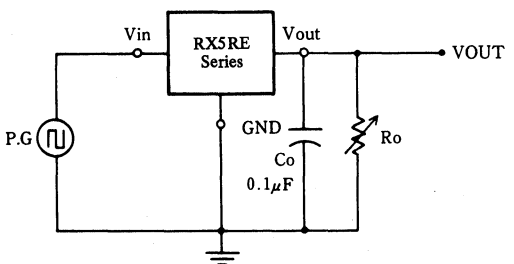


Fig. 6 Input Transition Responce Measurement Circuit

■ TYPICAL CHARACTERISTICS (Example of RH5RE50X)

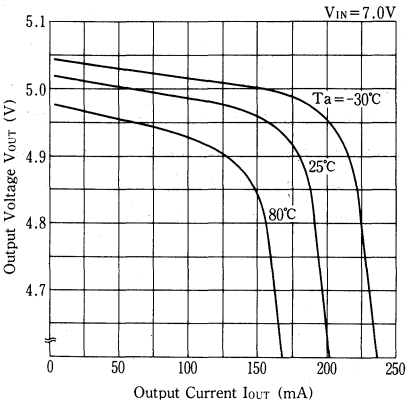


Fig. 7 Output Voltage VS. Output Current(1)

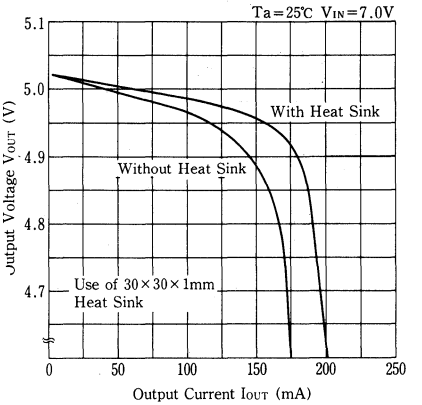


Fig. 8 Output Voltage VS. Output Current(2)

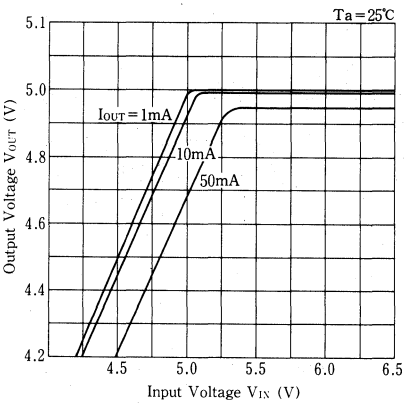


Fig. 9 Output Voltage VS. Input Voltage

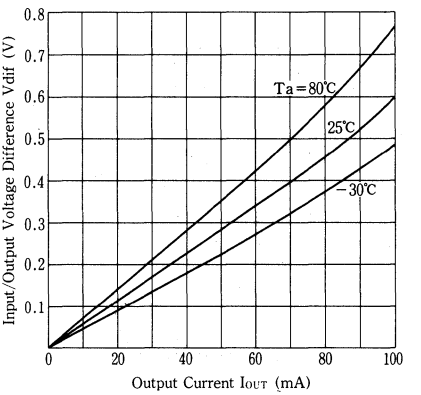


Fig. 10 Input/Output Voltage Difference VS. Output Current

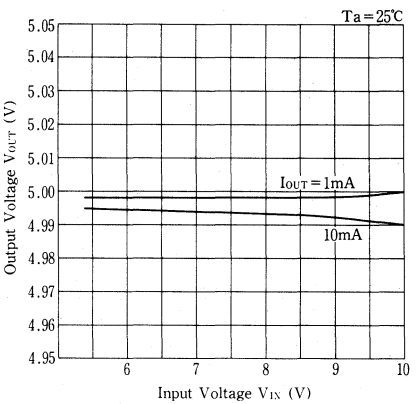


Fig. 11 Output Voltage VS. Input Voltage

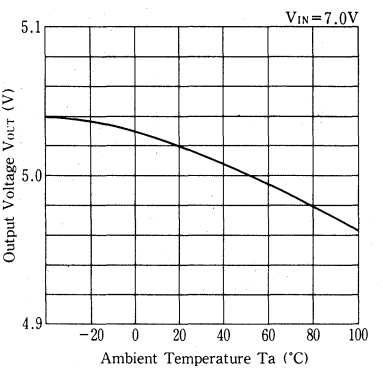


Fig. 12 Output Voltage VS. Ambient Temperature

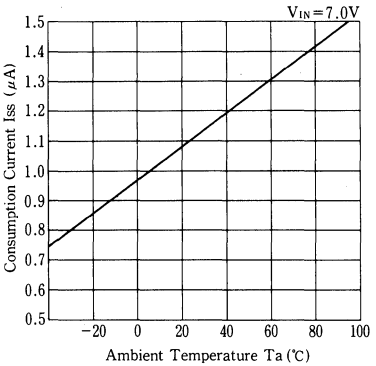


Fig. 13 Consumption Current VS. Ambinet Temperature

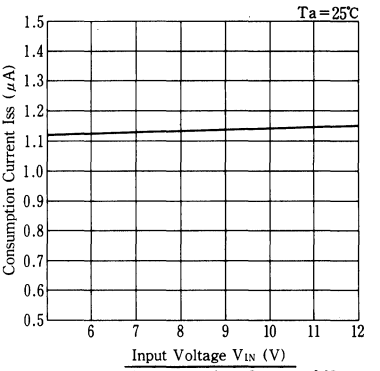


Fig. 14 Consumption Current VS. Input Voltage

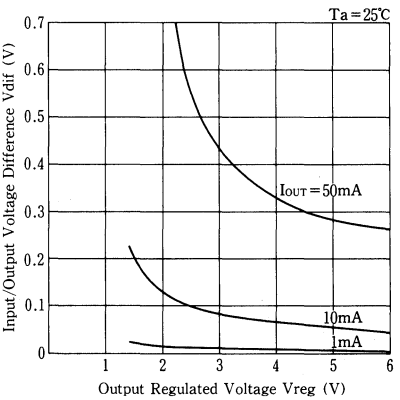


Fig. 15 Input/Output Voltage Difference VS. Output Regulated Voltage

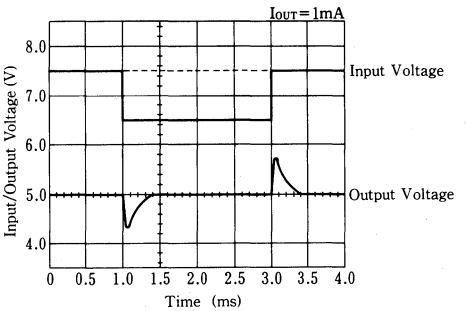


Fig. 16 Input Transition Responce (1)

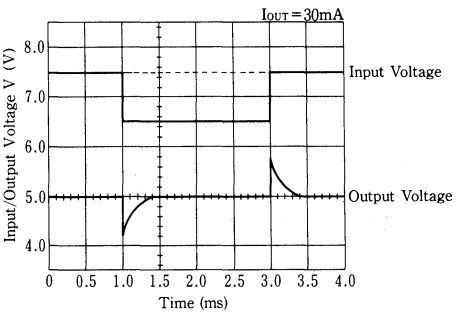


Fig. 17 Input Transition Responce (2)

■ PACKAGE INFORMATION

* SOT-89 Mini-Power-Mold · Plastic Package

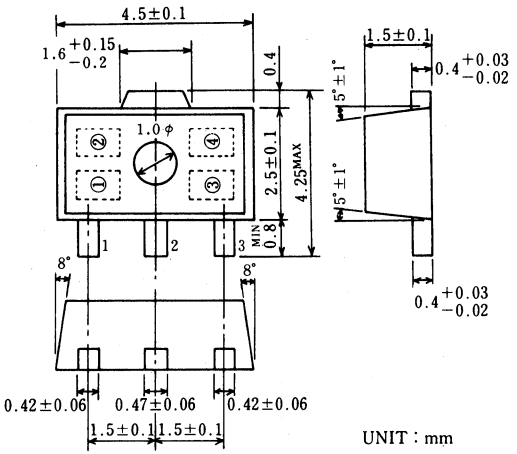


Fig. 18 SOT-89

• Pin Configuration

1 : GND
2 : Vin
3 : Vout

• Mark

①② : Code Number
③④ : Lot Number

* TO-92 Plastic Package

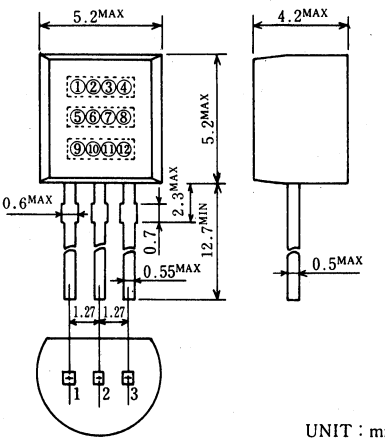


Fig. 19 TO-92

* TO-92 Plastic Package for Taping Method

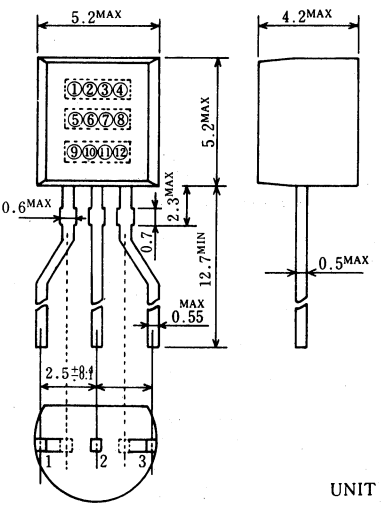


Fig. 20 TO-92

• Pin Configuration

1 : GND
2 : Vin
3 : Vout

• Mark

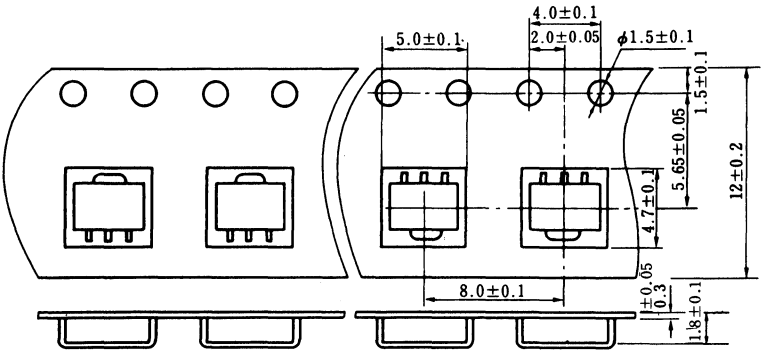
①②③④⑤⑥⑦⑧ : Type Number
⑨⑩⑪⑫ Lot Number

■ TAPING SPECIFICATION

* SOT-89 Mini-Power-Mold · Plastic Package

• Tape Dimension and Direction

2 Kinds of Taping Method (T1, T2) are available.

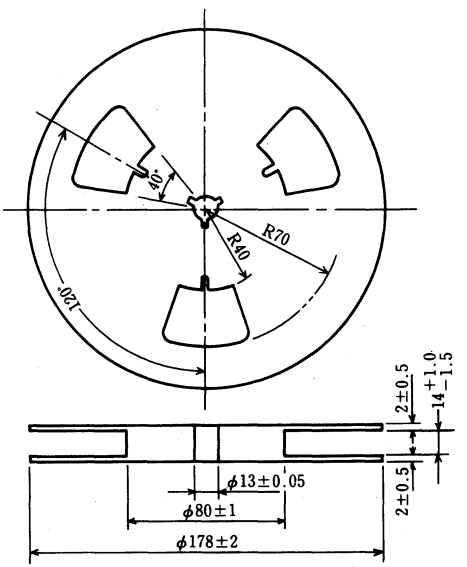


T1 Type T2 Type UNIT : mm

Fig. 21

• Reel Dimension

1000 pieces can be contained in one reel.



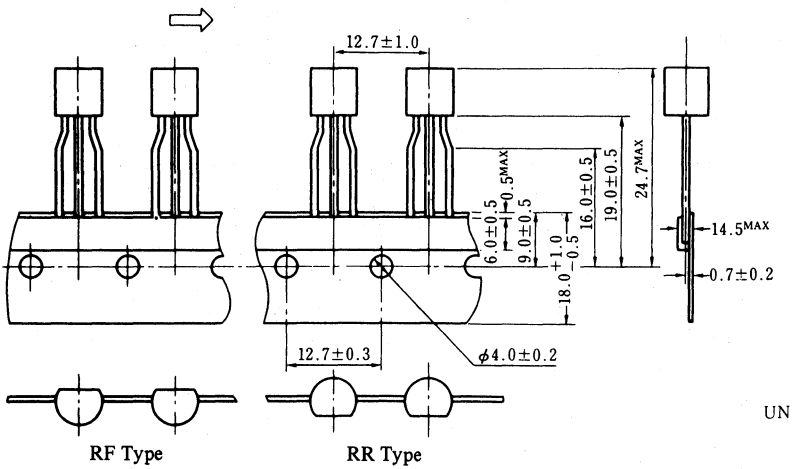
UNIT : mm

Fig. 22

* TO-92 Plastic Package

- Tape Dimension and Direction

2 Kinds of Taping Method (RF, RR) are available.

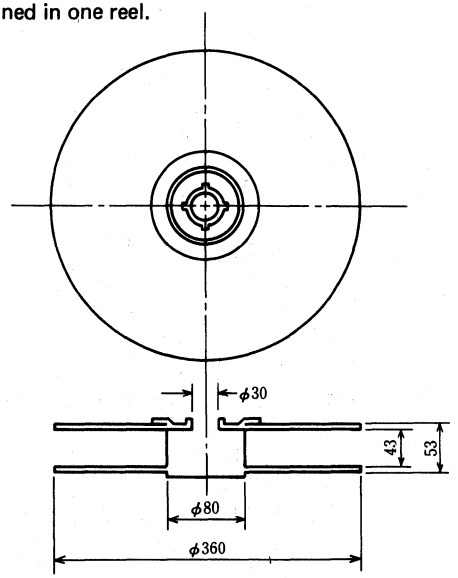


UNIT : mm

Fig. 23

- Reel Dimension

2000 pieces can be contained in one reel.

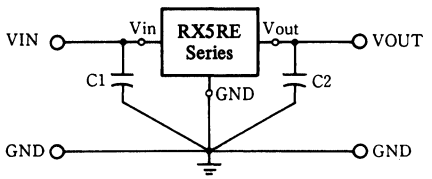


UNIT : mm

Fig. 24

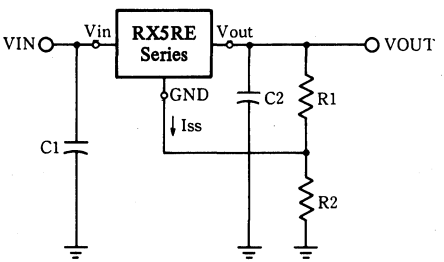
§2 Applications

■ STANDARD CIRCUIT



RX5RE series can regulate voltage without capacitor C1 and C2. When the input wire is long, use capacitor C1. Capacitor C2 makes the transient of output load variation smaller.
Keep the wiring as short as possible when putting capacitor C1 and C2 of 0.1 μF to 2.0 μF between regulator terminals and GND terminal.

■ INCREASED VOLTAGE CIRCUIT



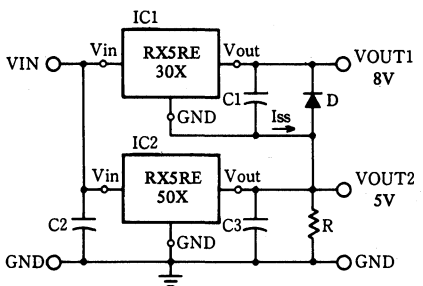
The following equation explains the output voltage.

$$VOUT = Vreg_{*}(1 + R2/R1) + Iss \cdot R2$$

The RX5RE series use low supply current, so R1 and R2 can be set high (several hundred k ohms) and supply current of the whole circuit itself can be kept low.
RX5RE works with constant current, so the input voltage scarcely affects supply current of the circuit.

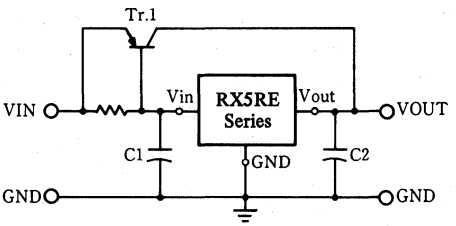
* Vreg: Fixed output voltage of RX5RE series

■ DUAL VOLTAGE CIRCUIT



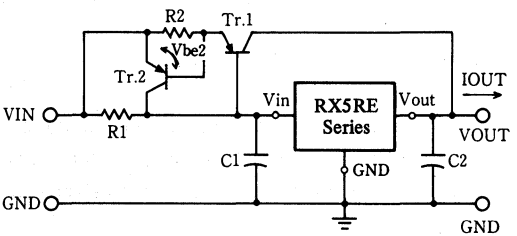
As the figure shows, two RX5RE devices can be made into a dual power circuit.
The figure shows examples with output of 8V and 5V. R is not needed when the minimum load current of IC2 is larger than Iss of IC1. Diode D protects IC1 when VOUT2 larger than VOUT1.

■ CURRENT BOOST CIRCUIT



When an output voltage more above 120 mA is necessary, construct a current boost circuit as shown in the figure.

■ CURRENT BOOST CIRCUIT with OVER-CURRENT PROTECTION



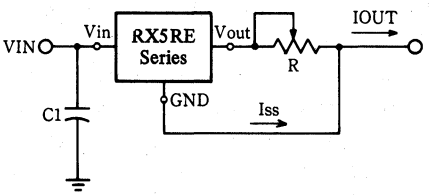
The figure on the left explains the circuit construction to protect Tr.1 from short output circuit or over current.

By adding Tr.2 and R2 to current boost circuit (above figure), voltage drops to Vbe2 of Tr.2 because of current through R2 (≒ IOUT). When it drops, Tr.2 will be on and will supply current to Tr.1 base. Tr.1 will be off and will limit output current.

The following equation explains the operation current of the overcurrent protection circuit.

IOUT = Vbe/R2

■ CONSTANT CURRENT POWER SUPPLY



As the figure shows, the construction can be used as constant current power supply. Output current, IOUT, can be found by the following equation.

IOUT = Vreg/R + Iss

Do not exceed the allowable current.

Vreg: Fixed output voltage of RX5RE series

§3 Selection Guide

■ SELECTION GUIDE

You can define the output voltage and package of the RX5RE series.
The devices are defined by the following characters.

R X 5 R E X X X ← Type number

↑ ↑ ↑
a b c

No.	Meaning
a	Defines the packaging type E : TO-92 H : Mini power mold (SOT-89)
b	Defines output voltage (Vout) The range for Vout is 2.0V to 6.0V in units of 0.1V, with an accuracy of ±2.5%.
c	Defines the packaging method for shipment A : Taping (Taping Method, T1/T2, RF/RR Types) B : Gluing (Gluing is for mini power mold package as a sample) C : Electric conductive bagging (for TO-92)

STEP-UP DC/DC CONVERTER
RH5RCseries
Application Manual

EA-015-8908

Contents

RH5RC301/302/501/502 are compact step-up DC/DC converter ICs, developed with the CMOS process technology. They consist of reference voltage source, error amplifier, control transistor, oscillation circuit, and output voltage setting resistor. As external parts, a coil, a diode, and a capacitor are available for obtaining a constant output voltage (3V, 5V) higher than the input voltage.

The package is a compact three-terminal mini power mold type.

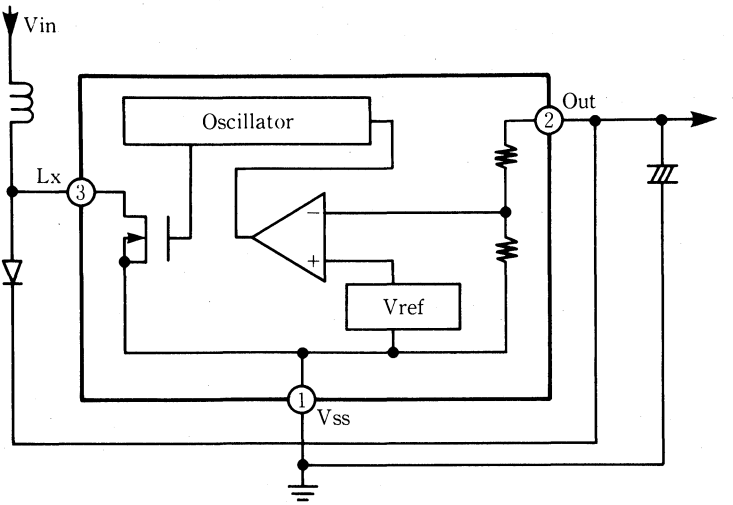
■ Features

- RH5RC301 ..... 3V output, normal type
  RH5RC302 ..... 3V output, low input voltage type
  RH5RC501 ..... 5V output, normal type
  RH5RC502 ..... 5V output, low input voltage type
- Small invalid current ..... 2.5μA (Typ., no step-up, RH5RC301/302)
- Low voltage operation ..... Input voltage Vin ≧ 0.9V (RH5RC302/502)
- High efficiency ..... 80% (Typ.)
- High output voltage accuracy ..... ±5%
- Small temperature drift of output voltage ..... ±50ppm (Typ.)
- Compact package ..... Mini power mold (SOT-89)

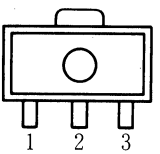
■ Application

Constant voltage source for battery-operated devices.
Constant voltage source for cameras, communications equipment, and videos.
Local regulator for different operating voltages.

■ Block Diagram



■ Pin Configuration



■ Pin Description

Pin No.	Name	Function
1	Vss	Ground
2	Out	Voltage Output
3	Lx	Switching pin

■ Absolute Maximum Ratings

(Vss=0V)

Parameter	Symbol	Limit	Unit
Input Voltage	Vin	7	V
Output Voltage	Vout	7	V
Output Current of Lx pin	ILx	120	mA
Power Dissipation	Pd	300	mW
Operating Temperature	Topr	-20 ~ +70	°C
Storage Temperature	Tstg	-40 ~ +125	°C

■ Electrical Characteristics

1. RH5RC301

(Ta = 25°C, Vss = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				6	V	
Starting Voltage	Vst	No Load			1.0	V	1
Holding Voltage	Vhld	No Load			0.6	V	1
Current Consumption	Iin	Vin = 5V		2.5	6	μA	
		Vin = 1.5V		7.5	20	μA	1
Output Voltage	Vout		2.85		3.15	V	1
Output Current of Lx pin	ILx	VOL = 0.4V	40			mA	
Leakage Current of Lx pin	ILxL				2	μA	
Oscillating Frequency	fosc		60		90	KHz	
Duty Ratio of Oscillation	Df			50		%	

2. RH5RC302

(Ta = 25°C, Vss = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				2	V	
Starting Voltage	Vst	No Load			0.9	V	1
Holding Voltage	Vhld	No Load			0.5	V	1
Current Consumption	Iin	Vin = 5V		2.5	6	μA	
		Vin = 1.5V		7.5	20	μA	1
Output Voltage	Vout		2.85		3.15	V	1
Output Current of Lx pin	ILx	VOL = 0.4V	40			mA	
Leakage Current of Lx pin	ILxL				2	μA	
Oscillating Frequency	fosc		60		100	KHz	
Duty Ratio of Oscillation	Df			25		%	2

3. RH5RC501

(Ta = 25°C, Vss = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				6	V	
Starting Voltage	Vst	No Load			1.0	V	1
Holding Voltage	Vhld	No Load			0.6	V	1
Current Consumption	Iin	Vin = 7V		3.5	9	μA	
		Vin = 2.4V		12	32	μA	1
Output Voltage	Vout		4.75		5.25	V	1
Output Current of Lx pin	ILx	VOL = 0.4V	60			mA	
Leakage Current of Lx pin	ILxL				9	μA	
Oscillating Frequency	fosc		100		140	KHz	
Duty Ratio of Oscillation	Df			50		%	

4. RH5RC502

(Ta = 25°C, Vss = 0V)

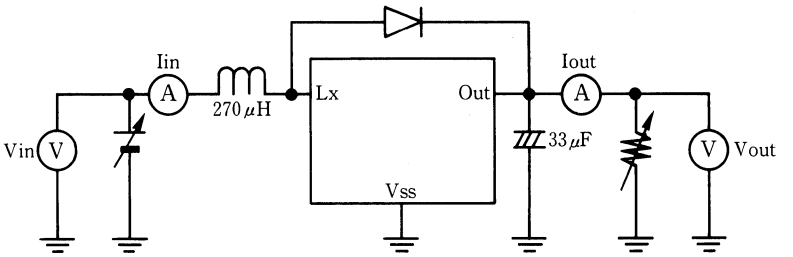
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	Vin				2	V	
Starting Voltage	Vst	No Load			0.9	V	1
Holding Voltage	Vhld	No Load			0.5	V	1
Current Consumption	Iin	Vin = 7V		3.5	9	μA	
		Vin = 2.4V		12	32	μA	1
Output Voltage	Vout		4.75		5.25	V	1
Output Current of Lx pin	ILx	VOL = 0.4V	60			mA	
Leakage Current of Lx pin	ILxL				2	μA	
Oscillating Frequency	fosc		110		150	KHz	
Duty Ratio of Oscillation	Df			25		%	2

Note: 1. The above table assumes that L=270μH (Sumida Electric Company LTD. CM-5), D=MA721 (Matsushita Electronics), and C=33μF Tantaru Capacitor, or equivalent products are used for external parts.

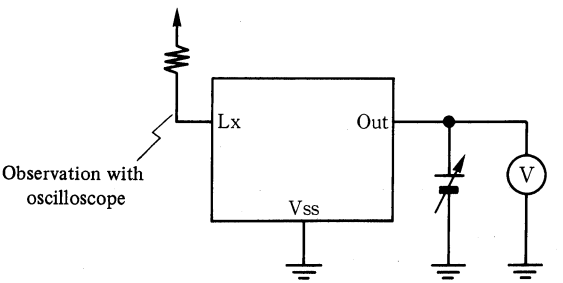
2. Duty Ratio of oscillation Df is expressed as follows: :

$$Df = \frac{t_H}{t_H + t_L} \times 100(\%)$$

■ **Measurement**



Circuit-1



Circuit-2

1) Starting voltage (circuit-1)

Gradually raise input voltage Vin from 0 V, and find out the point where Vout exceeds Vin (Vin < Vout). The voltage at that point is the starting voltage.

2) Operation hold voltage (circuit-1)

While the specified voltage (2.85 V to 3.15 for 301/302) is output, gradually lower the input voltage and find the point where the output voltage becomes smaller than the specified voltage. The voltage at that point is the operation hold voltage.

3) Consumption current (circuit-1)

The RH5RC IC uses the input current as the consumption current. So when Vin ≦ Vout, rush current flows at intervals. Rectify it by inserting an L–C configuration line filter, and use the averaged current as the consumption current.

4) Maximum oscillation frequency (circuit-2)

To measure the maximum oscillation freqency, apply power to RH5RC between Out and Vss. When Vout (voltage applied to the Out terminal) is smaller than the specified voltage, the Lx terminal outputs oscillation waveforms. The maximum oscillation frequency is the waveform output from the Lx terminal when Vout = specified voltage –50 mV.

5) Oscillation duty ratio

Use the duty ratio of the oscillation waveform output from the Lx terminal when the maximum oscillation frequency is measured.

■ Packing

1. You can select packing method from Taping and conductive bag.

The devices are defined by the following characters.

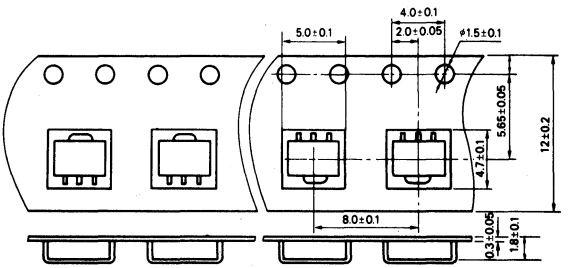
RH5RC301A-T1: Taping

RH5RC301A-T2: Taping

RH5RC301C__: Conductive bag (for sample use only)

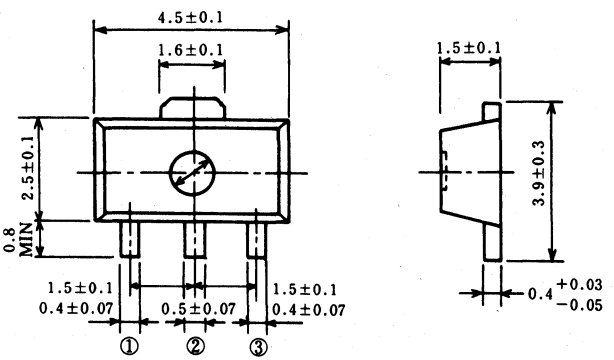
definition of the packing method.

2. Taping



T1 type T2 type

■ Package Dimension



■ DC/DC Converter

RH5RC can be regarded as a DC/DC converter, in that it generates a direct current from another direct current. DC/DC converters are largely classified into two according to their power supply conversion type:

DC/DC converter
- Charge-pump type
- Switching regulator type

RH5RC is a switching regulator type IC. The switching regulator type ICs are further classified into two according to the insulation between the primary and secondary power supplies:

Switching regulator
- Uninsulated type (chopper type)
- Insulated type (converter type)

In RH5RC, input and output are separated only by a diode and cannot be isolated electrically. So the IC is an uninsulated chopper type switching regulator.

Therefore, RH5RC cannot be used as a line-operated type power supply with commercial power supplies. For input power supply, use batteries or a power supply which has been reduced and rectified by a commercial power transformer.

■ Principle of Step-up Operation

Figure 1 shows the basic circuit configuration of the step-up operation of the IC. In that configuration, when the transistor 1 (Tr. 1) is entirely OFF, the output voltage Vout is the value of the input voltage Vin minus the voltage reduced by coil L and diode D.

When Tr. 1 has been ON for time ton and is suddenly turned off, voltage V_L is generated at the edges of L because of the energy accumulated during the ton period. Therefore, the peak value of the voltage generated at that time is Vin + V_L, and it is stored in the output capacitor C via D. This generates the step-up output voltage Vout that is equal to or larger than Vin.

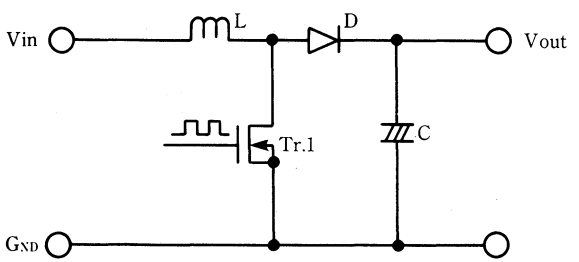


Figure 1

■ Operation

1) Control system

Figure 2 shows the control system of RH5RC, which regulates the step-up output voltage Vout, obtained by the principle explained in the previous section, to generate a constant voltage source.

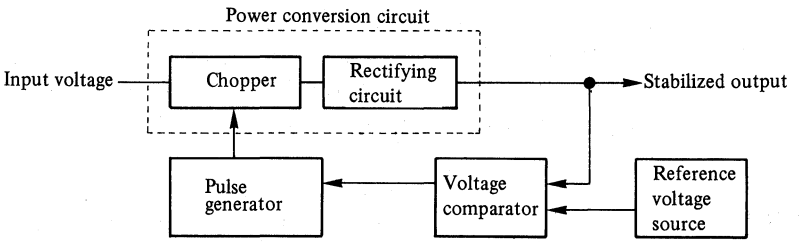


Figure 2

The volgage is stabilized by detecting the fluctuation of the output by the reference voltage source and the voltage comparator and operating the pulse generator at intervals. RH5RC consumes less current than other types, because there is no need to operate the pulse generator constantly.

In general, there are two types of switching regulator control method: pulse-width modulation (a) and frequency modulation (b). RH5RC can be regarded as a modified pulse-width modulation type, since the chopper drive period (ON-time) is constant and the period that the pulse generator is not operated (OFF-time) is varied according to the input voltage and load.

2) Starting operation

RH5RC does not have a V_{DD} (+ power supply) terminal. The Out terminal is used as the output, + power supply, and output voltage detection terminals.

When power is applied, the input voltage is provided to the Out terminal via coil L and diode D. Once operation is started with the provided power, the IC operates by the step-up voltage generated by itself. Therefore the step-up voltage is used as the gate drive voltage of the control transistor. This reduces the MOSFET ON resistance and enables large current drive by a small transistor, which then enables mounting to a three-terminal mini power mold (SOT-89).

Due to the circuit configuration described above, load applied at power-on increases the forward voltage V_F of the diode, and reduces the actual activation voltage of the IC. So we recommend you to take measures such as attaching low-power reset function to the load circuit, so that only small load is applied when power is turned on or the output voltage is lowered.

When an input power supply having high impedance Z_B is used, the starting voltage tends to be higher than usual. This is because the control transistor switch current I_{LX} and Z_B decrease the actual activation voltage of the IC. The IC is designed to prevent excessive I_{LX} (soft start), but we recommend you to use an input power supply with Z_B equal to or smaller than 5Ω.

3) Steady-state operation

After power is turned on and the output voltage has reached the specified voltage (3 V or 5 V), the control transistor is switched in frequencies corresponding to the input voltage and load to maintain a constant output voltage. When no load is applied, the IC needs to step up only the power that it consumes by itself, so the switching operation is performed with a very low frequency (lower than 10 Hz).

In steady-state operation, when the control transistor has been ON for ton period, switching current I_{LX} flows from input power supply Vin through coil L. I_{LX} increases proportionally to time, so it is expressed as follows:

$$I_{LX} = \frac{Vin}{Lx} \cdot ton \quad \cdots\cdots (1)$$

(L_X is the inductance of the coil, and the voltage decrease due to the ON-resistance of the transistor is ignored.)

For recommended coils (see p.13), the ton period is set inside the IC so that I_{LX} does not exceed the rated value (120 mA). Always check the I_{LX} value according to the operation conditions.

■ Design of the DC/DC Converter

1) Output current

In the circuit configuration of RH5RC, output is obtained by accumulating energy in the coil while the control transistor is ON and superimposing it on the input power supply while the control transistor is OFF.

The electric power Pon accumulated in the coil when the control transistor is switched once is expressed as follows:

$$Pon = \int_0^{t\,on} \frac{Vin^2}{Lx}\, tdt \quad \cdots\cdots (2)$$

(ton is the ON-time of the control transistor, Vin is the input voltage, and Lx is the coil inductance.)

RH5RC uses the OFF-time control method, in which the ton time is constant and a pulse is sent when the output voltage becomes smaller than the specified value VT (= Vout). Therefore, when the load is heavy or the input voltage is low, switching is performed fosc (maximum oscillation frequency) times at maximum. The power P_L accumulated in the coil at that time is expressed as follows:

$$P_L = Pon \cdot fosc \quad \cdots\cdots (3)$$

At that time, the following relationship is established in RH5RC301 and 501:

$$ton = toff = \frac{1}{2 \cdot fosc} \quad \cdots\cdots (4)$$

And the following relationship is established in RH5RC302 and 502:

$$ton = 3 \cdot toff = \frac{3}{4 \cdot fosc} \quad \cdots\cdots (5)$$

From expressions (1) to (5), the maximum output current Iout in a design of DC/DC converter using RH5RC is as follows:

For RH5RC301 and 501:

$$Iout = \frac{P_L}{(Vout - Vin)} \quad \cdots\cdots (6)$$

$$= \frac{Vin^2}{8 \cdot fosc \cdot Lx \cdot (Vout - Vin)} \quad \cdots\cdots (7)$$

For RH5RC302 and 502:

$$Iout = \frac{9 \cdot Vin^2}{32 \cdot fosc \cdot Lx \cdot (Vout - Vin)} \quad \cdots\cdots (8)$$

Due to such matters as efficiency, the actual output voltage will be 50% to 80% of the results of expressions (6) and (8).

Therefore, to increase the output current, the inductance Lx of the coil must be smaller. However, if the inductance is too small, the I_{LX} value will exceed the ratings as described in the previous section, Operation description–3) Rated operation. In general, the appropriate inductance is:

$$Lx = 82 \sim 270 \mu H \quad \cdots\cdots (9)$$

2) Ripple characteristics

Ripples that appear in the output of a DC/DC converter using RH5RC are classified into four:

(1) Ripples due to coil switching.

(2) Ripples due to fluctuation of the voltage accumulated in output capacitor C.

(3) Ripples due to the characteristics of output capacitor C.

(4) Ripples due to wiring.

The ripples of (1) occur at the moment the control transistor is turned off. The frequency spectrum spreads very widely (over several MHz) and the amplitude is several tens of mV. The main cause is the floating capacity on the Lx terminal and the turn-on time of the diode. Place the Lx terminal, coil and diode as close together as possible, and use a diode with short turn-on time. The ripples can also be reduced by inserting a capacitor of several tens of pF between the anode and cathode (see Figure 3).

The ripples of (2) are the disadvantage of the off-time control method used by RH5RC. They are caused because even under small load, the same potential as that for the maximum load is applied to the output capacitor at every switching. So use a coil with as large an inductance as possible within the desired range of the output current capacity.

The ripples can also be reduced by increasing the capacity of the output capacitor. This is easy to see since the ripple Vp is expressed as follows:

$$Vp = \int \frac{1}{C} iDdt \quad \cdots\cdots (10)$$

(iD is the current flowing in the diode.)

Ripples of (3) are caused by equivalent resistance and frequency response of the output capacitor. The capacitor impedance Zc is expressed as follows:

$$Zc = R + \omega L + \frac{1}{\omega C} \quad \cdots\cdots (11)$$

Zc causes ripples in combination with the charged current. Against this type of ripple, insert a capacitor of about 0.1μF in parallel with output capacitor C (see Figure 3).

Ripples of (4) are caused mainly by the routing of the power supply grounding. The grounding must be one-point and routed as short as possible to avoid any excessive impedance (especially R and L elements) (see Figure 3).

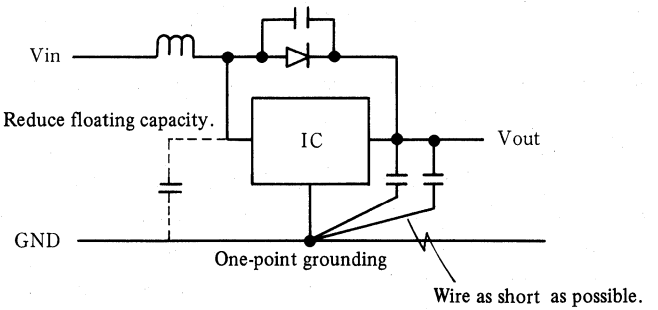


Figure 3

3) Efficiency

There are two major causes to degrade the efficiency in a DC/DC converter using RH5RC:

(1) Power loss in diode

(2) Power loss in control transistor

Loss of (1) Pd is expressed as follows:

$$Pd = Vf \cdot Iout \quad \text{..... (12)}$$

To improve the efficiency, use a diode with a small Vf value.

Loss of (2) PT is expressed as follows from equation (1):

$$Pt = I_{LX} \cdot RT \quad \text{..... (13)}$$

$$= \frac{Vin}{Lx} \cdot ton \cdot RT \quad \text{..... (14)}$$

(RT is the ON-resistance of the control transistor.)

To improve the efficiency, use a coil with a large Lx value.

■ Selection of External Parts

1) Coil

To select choke coils, consider the following points:

- The core must not be saturated magnetically.
- There must be a sufficient margin of the rated current.
- DC resistance must be sufficiently low.
- The allowable loss must be sufficiently large.

For RH5RC, the following coils are recommended:

- CMD-6L (Sumida Electric Company Ltd., Model 6303-014, 015, 016, 017)
- CM-5 (Sumida Electric Company Ltd., Model 6301-064, 065, 066)
- CP-4LBM (Sumida Electric Company Ltd., Model 5201-053, 055, 066)

2) Diode

To select diodes, consider the following points:

- The forward voltage must be small.
- The turn-on time must be short.
- There must be a sufficient margin of the rated current.

In general, a schottky diode is suitable. Be careful, because some of them may have increased reverse current at a high temperature.

3) Capacitor

To select capacitors, consider the following points:

- The capacity must be comparatively large.
- The equivalent resistance must be small.

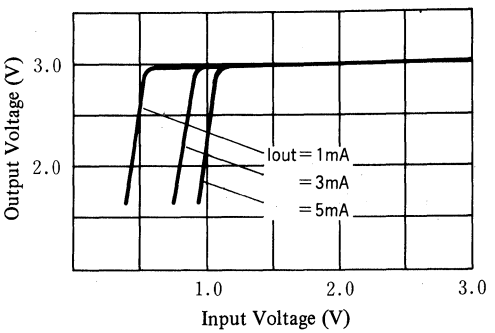
In general, tantalum (aluminum) electrolytic capacitors and layered ceramic capacitors are suitable.

■ Characteristics

1) Output Voltage VS. Input Voltage (Ta = 25°C)

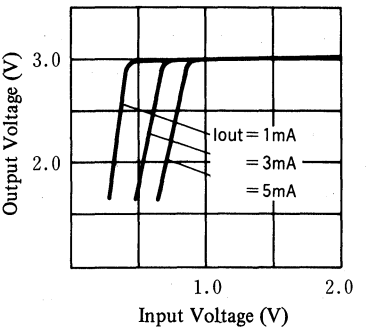
(1) RH5RC301

L=82μH(CM-5), D=MA721

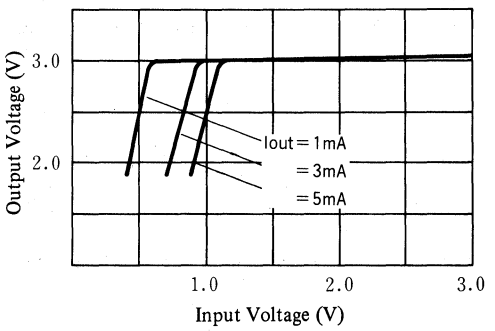


(2) RH5RC302

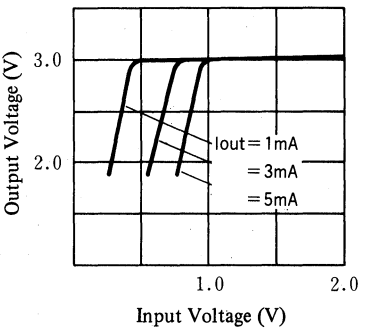
L=82μH(CM-5), D=MA721



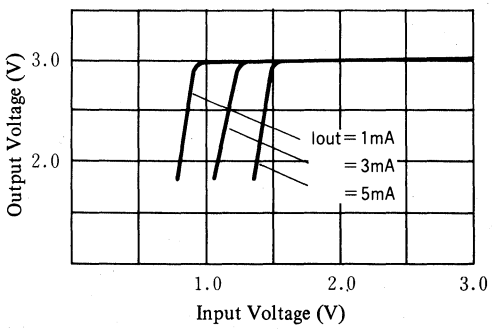
L=120μH(CM-5), D=MA721



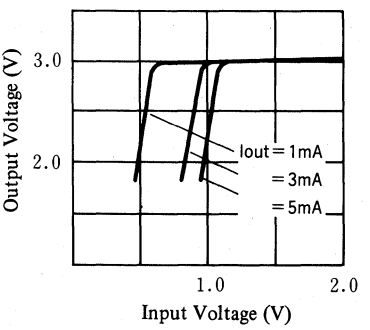
L=120μH(CM-5), D=MA721



L=270μH(CM-5), D=MA721

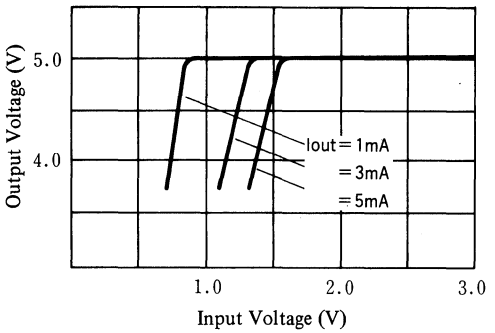


L=270μH(CM-5), D=MA721

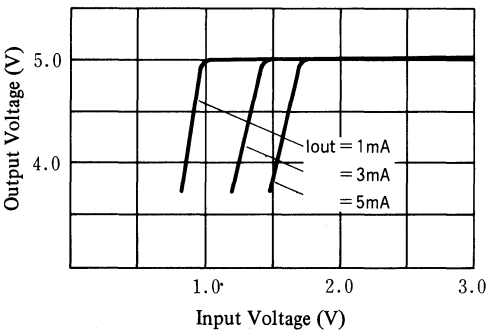


(3) RH5RC501

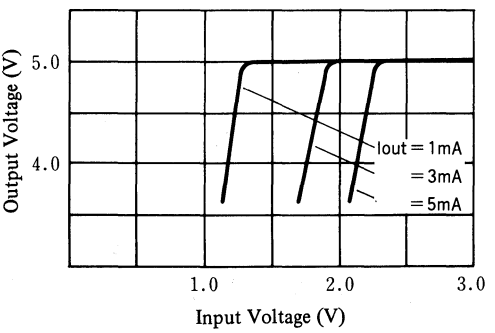
L=82μH(CM-5), D=MA721



L=120μH(CM-5), D=MA721

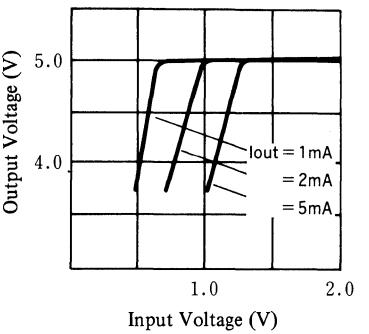


L=270μH(CM-5), D=MA721

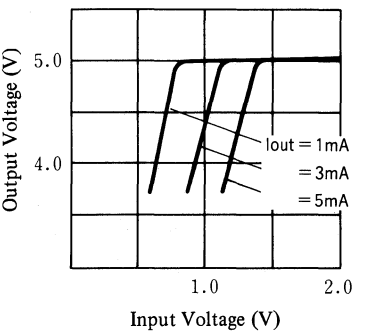


(4) RH5RC502

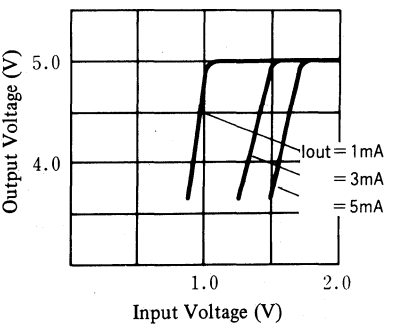
L=82μH(CM-5), D=MA721



L=120μH(CM-5), D=120μH

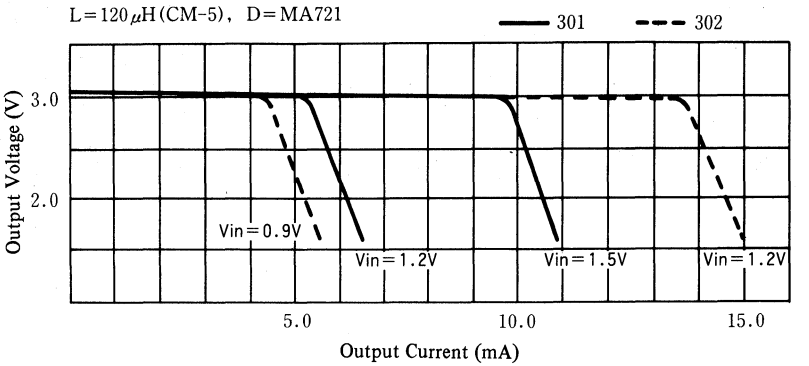


L=270μH(CM-5), D=MA721

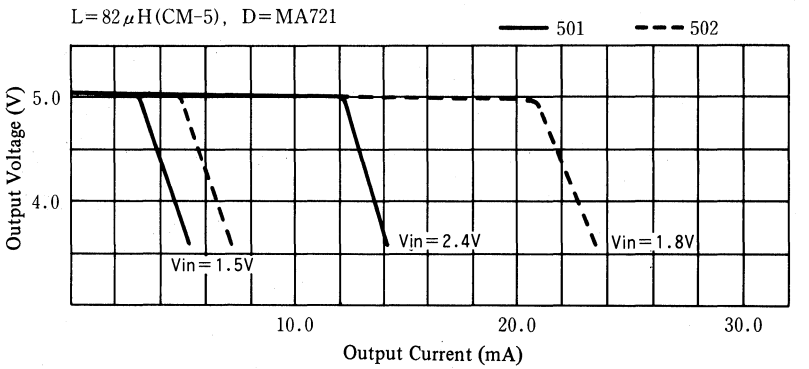


2) Output Voltage VS. Output Current (Ta = 25°C)

(1) RH5RC301, 302

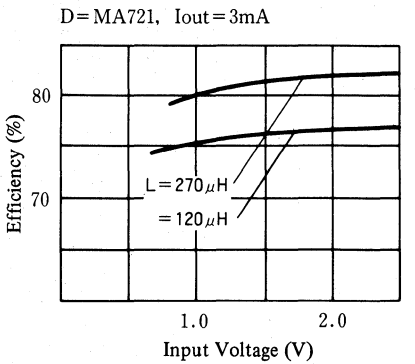


(2) RH5RC501, 502

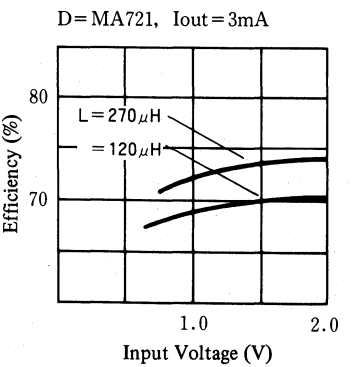


3) Efficiency VS. Input Voltage (Ta = 25°C)

(1) RH5RC301

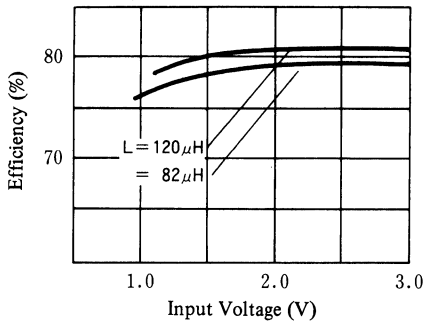


(2) RH5RC302



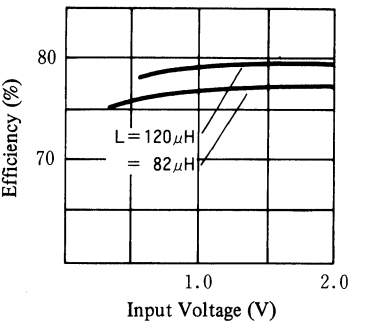
(3) RH5RC501

L=120μH(CM-5), D=MA721, Iout=1mA



(4) RH5RC502

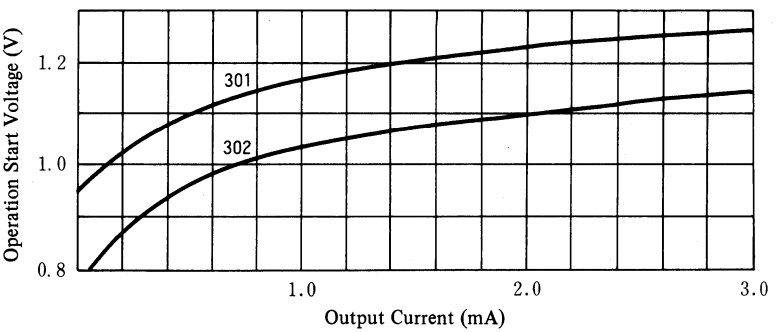
L=120μH(CM-5), D=MA721, Iout=1mA



4) Operation Start Voltage VS. Output Current (resistance load) (Ta = 25°C)

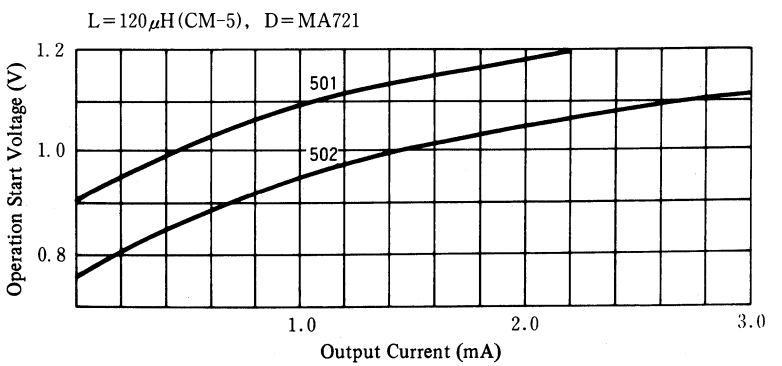
(1) RH5RC301, 302

L=120μH(CM-5), D=MA721



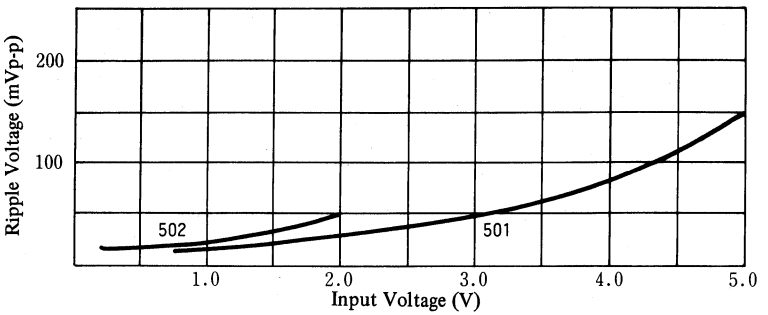
(2) RH5RC501, 502

L=120μH(CM-5), D=MA721



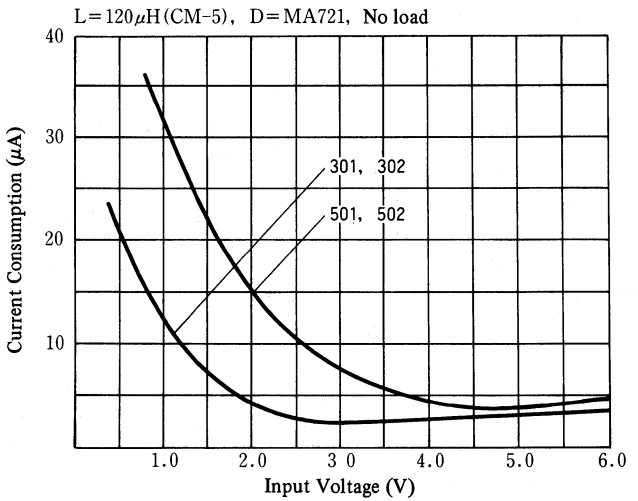
(2) RH5RC501, 502

L=120μH(CM-5), D=MA721, Iout=1mA, C=33μF, except spike



5) Current Consumption VS. Input Voltage (Ta = 25°C)

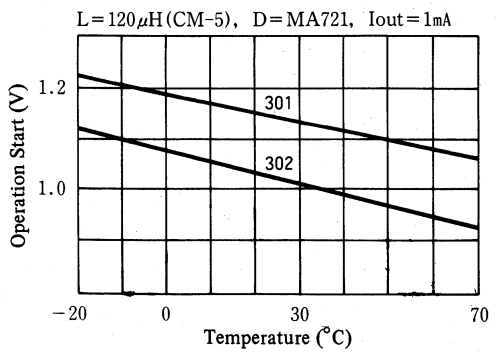
L=120μH(CM-5), D=MA721, No load



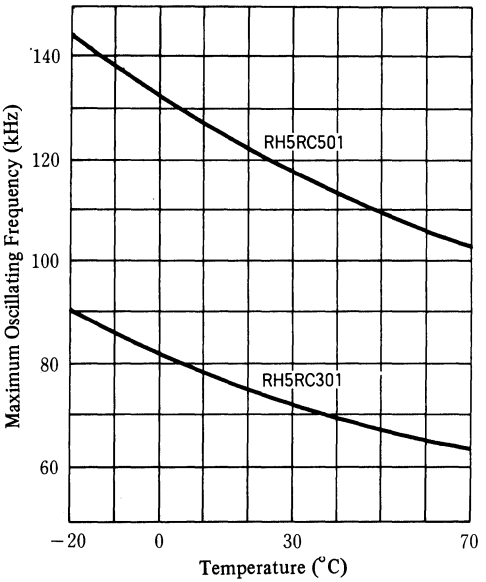
6) Operation Start Voltage VS. Temperature

(1) RH5RC301, 302

L=120μH(CM-5), D=MA721, Iout=1mA



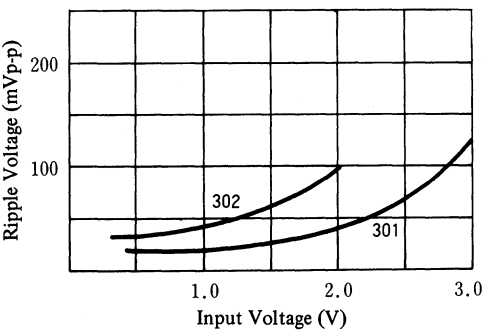
7) Maximum Oscillating Frequency VS. Temperature



8) Ripple Voltage VS. Input Voltage (Ta = 25°C)

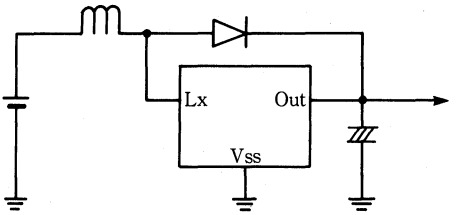
(1) RH5RC301, 302

L=120μH(CM-5), D=MA721, Iout=1mA, C=33μF, Except Spike

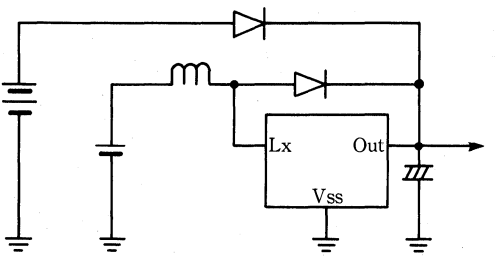


■ Application Circuit

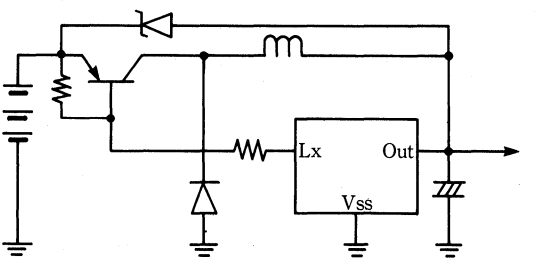
• Step-up DC/DC Converter



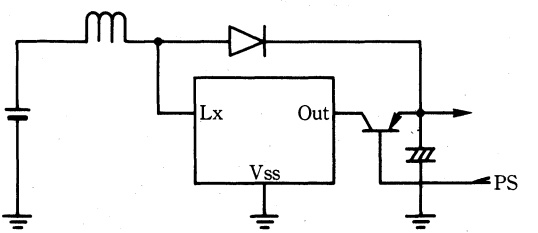
• Power Switching Circuit



• Step-down DC/DC Converter



• Power Saving Circuit



STEP-UP/STEP-DOWN DC/DC CONVERTER RF5RD Series Application Manual

EA-017-8912

RF5RD301/501 are compact DC/DC converter ICs developed with the CMOS process technology. When the input voltage is sufficiently high, they work as series regulators. When the input voltage falls down, they work as step-up switching regulators.

They consist of a step-up switching regulator circuit and series regulator circuit. The switching regulator circuit consists of the reference voltage source, error amplifier, control transistor, oscillation circuit, and output voltage setting resistor. The series regulator circuit consists of the reference voltage source (shared with the switching regulator circuit), error amplifier, output transistor, and output voltage setting resistor.

As external parts, a coil, a diode, and a capacitor are available for making the output voltage constant even when the input voltage changes across the output voltage.

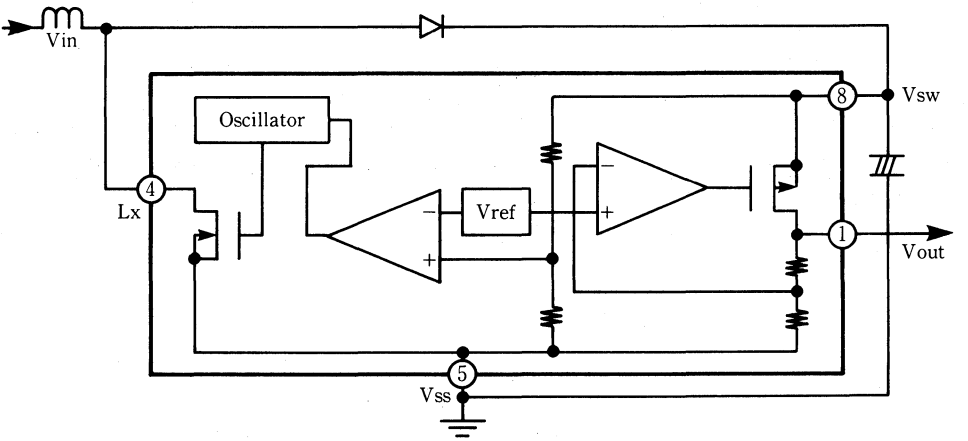
■ Features

- RF5RD301 ..... Output voltage 3V (Typ.)
  RF5RD501 ..... Output voltage 5V (Typ.)
- Low idle current ..... 4.0μA (Typ., no step up, RF5RD301)
- Small idle current ..... Input voltage Vin ≧ 1.2V (no load)
- High efficiency ..... 70% (Typ., step up)
- High output voltage accuracy ..... ±5%
- Small temperature drift of output voltage ..... ±100ppm (Typ.)
- Small package ..... 8-pin SOP

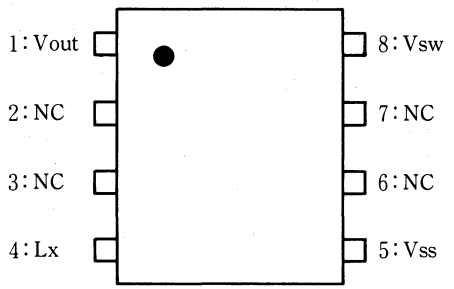
■ Application

- Constant voltage source for battery-operated devices.
- Constant voltage source for cameras, communication equipment, and videos.
- Local regulator for different operating voltages.

■ Block Diagram



■ Pin Configuration



■ Pin Description

Pin No.	Name	Function
1	Vout	Output Voltage
2, 3	NC	No Connection
4	Lx	Switching pin
5	Vss	Ground
6, 7	NC	No Connection
8	Vsw	Step-up Output

■ Absolute Maximum Ratings

(Vss=0V)

Parameter	Symbol	Limit	Unit
Input Voltage	Vin	12	V
Output Voltage	Vout	12	V
Output Current of Lx pin	ILx	100	mA
Power Dissipation	Pd	300	mW
Operating Temperature	Topr	-20 ~ +70	°C
Storage Temperature	Tstg	-40 ~ +125	°C

■Electrical Characteristics

● RF5RD301 (3V Output)

(Ta = 25°C Vss = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage	Vin				8	V
Starting Voltage	Vst	No Load	1.2			V
Holding Voltage	Vhld	No Load	0.8			V
Current Consumption	Iin	No Load, Vin = 5V		4	9	μA
		No Load, Vin = 2.4V		7	20	μA
Output Voltage	Vout		2.85		3.15	V
Output Current	Iout	Vin = 5V		40		mA
		Vin = 2.4V		15		mA
Output Current of Lx pin	ILx	Vol = 0.4V	40			mA
Leakage Current of Lx pin	ILXL				1	μA
Oscillating Frequency	fosc		60		90	KHz

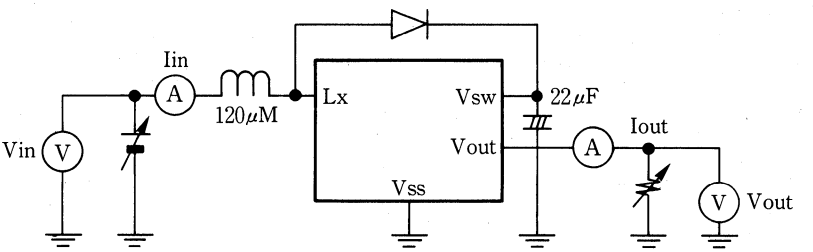
● RF5RD501 (5V Output)

(Ta = 25°C Vss = 0V)

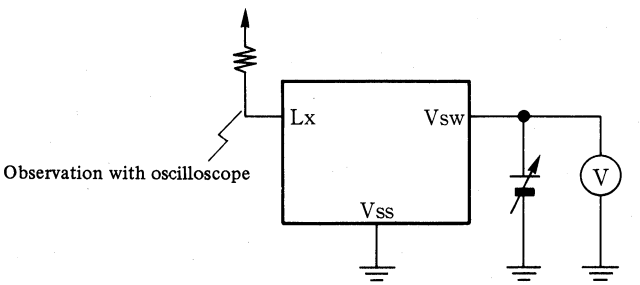
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage	Vin				8	V
Starting Voltage	Vst	No Load	1.2			V
Holding Voltage	Vhld	No Load	0.8			V
Current Consumption	Iin	No Load, Vin = 7V		6	11	μA
		No Load, Vin = 3.6V		15	40	μA
Output Voltage	Vout		4.75		5.25	V
Output Current	Iout	Vin = 7V		40		mA
		Vin = 3.6V		20		mA
Output Current of Lx pin	ILx	Vol = 0.4V	60			mA
Leakage Current of Lx pin	ILxl				1	μA
Oscillating Frequency	fosc		100		140	KHz

Note: The above table assumes that L = 120μH (CMD6L), MA721 diode or equivalent, and C = 22μF are used for external parts.

■ **Measurement**



Circuit–1



Circuit–2

1) Operation start voltage (circuit–1)

Raise input voltage Vin from 0V gradually, and find out the point where Vout exceeds Vin. The input voltage at that point is the operation start voltage.

2) Operation hold voltage (circuit–1)

Keep the output to be the specified voltage (2.85V to 3.15V for 301). Lower the input voltage gradually, and find out the point where the output voltage becomes lower than the specified voltage. The input voltage at that point is the operation hold voltage.

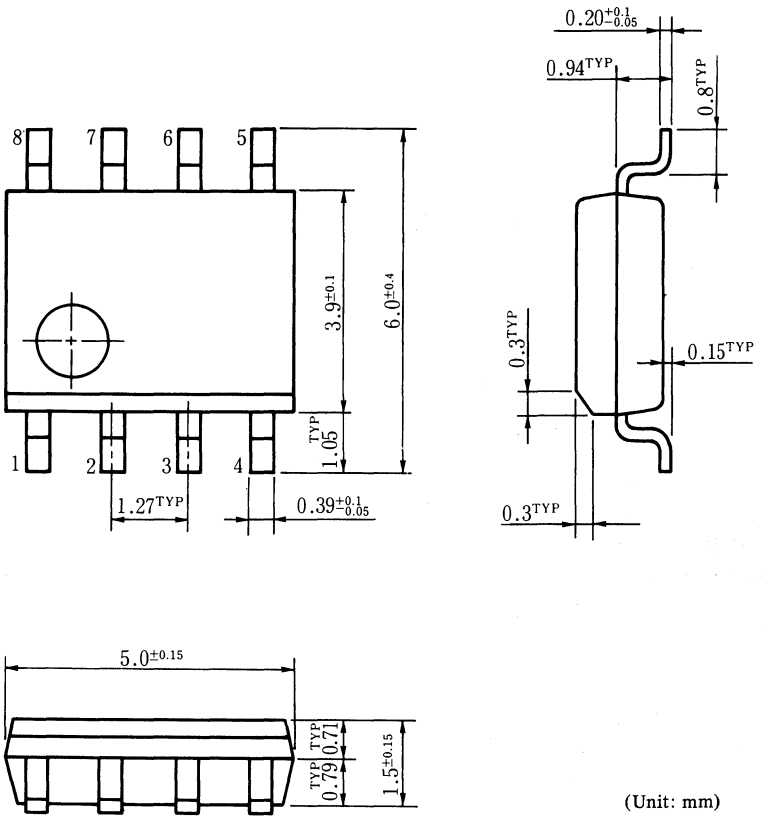
3) Consumed current (circuit–1)

For the RF5RD301 and RF5RD501, the input current is the consumed current. Therefore, rush current intermittently flows when Vin is equal to or lower than Vout. So rectify the current by, for example, inserting a line filter of L/C configuration, and use the average current for the consumed current.

4) Maximum oscillation frequency (circuit–2)

To measure the maximum oscillation frequency, set the power supply for the RF5RD301 and RF5RD501 to within Vsw and Vss. An oscillation waveform is output to the Lx terminal when the voltage Vsw applied to the Vsw terminal is lower than the specified voltage. The maximum oscillation frequency is the waveform output from the Lx terminal when Vsw = specified voltage -50mV.

■ Package -Dimension



(Unit: mm)

■ Operation

1) Switching between step-up and step-down operations

The RF5RD301 and RF5RD501 perform step-down operation when the input voltage is sufficiently higher than the specified output voltage, and work as series regulators. They perform step-up operation when the input voltage is lower than the specified output voltage, and work as step-up switching regulators + series regulators.

The input voltage $V_{IN U/D}$ that causes switching of the step-up and step-down operations is:

$$V_{IN U/D} = V_{SW} + V_F \quad \cdots\cdots (1)$$

(V_{SW} is the specified step-up output voltage, V_F is the forward voltage of the diode.)

To suit the capacity of the output transistor of the series regulator, V_{SW} is set in the IC chip as:

$$V_{SW} \simeq V_{OUT} + 0.5(V) \quad \cdots\cdots (2)$$

(V_{OUT} is the specified output voltage.)

From (1) and (2), $V_{IN U/D}$ is expressed as follows:

$$V_{IN U/D} \simeq V_{OUT} + V_F + 0.5(V) \quad \cdots\cdots (3)$$

2) Control system

The RF5RD301 and RF5RD501 use the control system shown in Figure 2 to obtain regulated constant voltage from the output voltage V_{OUT} obtained from the step-up and step-down operations above.

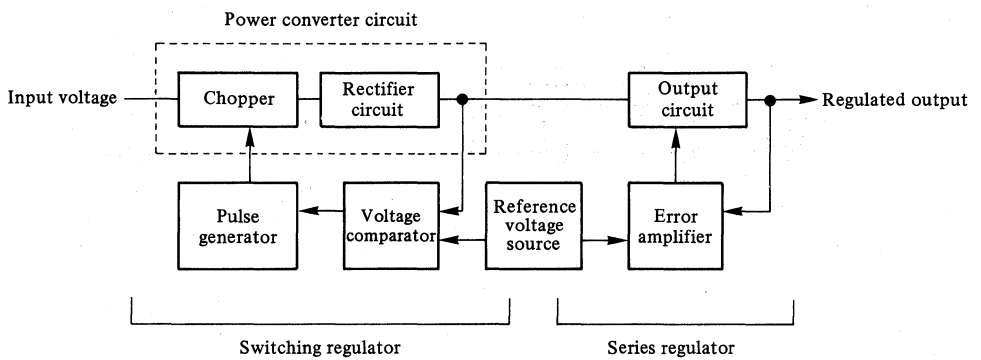


Figure 2

When V_{in} is higher than $V_{inU/D}$, the RF5RD301 and RF5RD501 perform step-down operation and the pulse generator does not work. So the input voltage goes through the power converter circuit as is, and is applied to the series regulator. Then the regulated output is obtained.

When V_{in} is equal to or lower than $V_{inU/D}$, the RF5RD301 and RF5RD501 perform step-up operation and the step-up switching regulator works. The step-up voltage is applied to the series regulator and the regulated output is obtained. At that time, the step-up DC/DC converter uses the reference voltage source and the voltage comparator to detect the amount of fluctuation in the step-up output, and operates the pulse generator intermittently. This eliminates the need to constantly operate the pulse generator, enabling low power consumption in step-up operation as well as in step-down operation.

3) Operation start

The RF5RD301 and RF5RD501 do not have a V_{DD} terminal (+power supply terminal). The V_{SW} terminal is used as the step-up output terminal, +power supply terminal, and step-up output voltage detection terminal.

At power on, the input voltage is applied to the V_{SW} terminal via coil L and diode D, and the IC starts operation.

When V_{in} is equal to or smaller than $V_{inU/D}$, the IC starts operation as a step-up switching regulator. If a heavy load is applied to the output terminal at power on, the forward voltage V_F of diode D increases and causes lowering of the actual activation voltage of the IC. So take some measure to lower the load at power on and at low output voltage, for example by attaching the low voltage reset (low power) function.

When an input power supply with high power supply impedance Z_B is used, the operation start voltage tends to be higher than usual. This is because the voltage is lowered by the switch current I_{Lx} and Z_B of the control transistor, and as a result the actual activation voltage of the IC is lowered. RF5RD301 and RF5RD501 are designed so that I_{Lx} does not become excessive at power on (soft start), but it is recommended to use an input power supply with Z_B lower than 5 Ω.

4) Steady-state operation

After the IC starts operation and the output voltage reaches the specified voltage, the output voltage is kept constant even when the input voltage sharply fluctuates across the specified output voltage. This is enabled by the comparatively fast step-up/down switching and the filtering effect of the externally attached L and C.

In the RF5RD301 and RF5RD501, the series regulator also works as a ripple filter in step-up operation. This suppresses the ripples generated by the step-up switching regulator, and constantly offers low-ripple output.

■ DC/DC Converter design

1) Output current

In designing a DC/DC converter using the RF5RD301 and RF5RD501, the output current Iout generally depends on the output current of the series regulator in step-down operation, and depends on the capability of the step-up switching regulator in step-up operation.

〈Step-down〉

In a series regulator of CMOS configuration, the output current I_{outR} is generally expressed as:

$$I_{out} = I_{outR} = KP \cdot (\text{Input/Output Voltage Difference}) \quad \cdots\cdots (4)$$

(KP is the conduction coefficient of the output transistor.)

In the RF5RD301 and RF5RD501, the input voltage of the series regulator is supplied via diode D, so Iout is expressed as:

$$I_{out} = KP \cdot (V_{in} - V_F - V_{out}) \quad \cdots\cdots (5)$$

〈Step-up〉

In step-up operation, the difference in the I/O voltages of the series regulator is fixed to about 0.5V. Therefore, I_{outR} is expressed as:

$$I_{outR} = 0.5 \cdot KP \quad \cdots\cdots (6)$$

The output current I_{outS} of the step-up switching regulator is expressed as:

$$I_{outS} = K \frac{V_{in}^2}{8 \cdot f_{osc} \cdot L_x \cdot (V_{out} + 0.5 - V_{in})} \quad \cdots\cdots (7)$$

(L_x is the inductance of the coil used, K=0.5 to 0.8.)

Therefore, the output current of Iout of the switching regulator is limited by the smaller of expressions (6) and (7) (see the section below, the output current of the step-up switching regulator).

When Vin is comparatively high and (Vout − Vin) is small, $I_{outR} \leqq I_{outS}$. In other cases, $I_{outR} \geqq I_{outS}$.

— The output current of the step-up switching regulator—

The step-up switching regulator incorporated in the RF5RD301 and RF5RD501 has a circuit configuration that stores energy in the coil when the control transistor is on and takes out the output by superimposing the energy to the input power supply when the control transistor is off.

When the control transistor switches once, the power P_{ON} stored in the coil is expressed as:

$$P_{ON} = \int_0^{ton} \frac{Vin}{Lx} \, tdt \quad \cdots\cdots (8)$$

(t_{on} is the on-time of the control transistor, V_{in} is the input voltage, and Lx is the inductance of the coil.)

This circuit uses the off-time control method. The t_{on} is fixed, and pulses are sent when the step-up output voltage becomes lower than the specified value V_{sw} ($=V_{out}+0.5$). Therefore, when the load is heavy or input voltage is low, the transistor switches fosc (maximum oscillation frequency) times at maximum. At that time, the power PL stored in the coil is expressed as:

$$PL = P_{ON} \cdot fosc \quad \cdots\cdots (9)$$

At that time, the following relationship is established:

$$ton = toff = \frac{1}{2 \cdot fosc} \quad \cdots\cdots (10)$$

Thus, the maximum output current obtained by the step-up switching regulator is:

$$Iouts = \frac{Vin^2}{8 \cdot fosc \cdot Lx \cdot (Vout + 0.5 - Vin)} \quad \cdots\cdots (11)$$

In actual operation, the output current will be 50% to 80% of expression (11), due to such factors as efficiency.

As indicated above, the inductance value Lx of the coil must be small to increase the step-up output current. However, if the Lx value is too small, ILx may exceed the rated value (120mA) since the ILx is expressed as follows:

$$ILx = \frac{Vin}{Lx} \cdot ton \quad \cdots\cdots (12)$$

(Voltage lowered by the on-resistance of the transistor is ignored.)

Be careful of the ILx value.

Generally, the appropriate value is:

$$Lx = 82 \sim 470\mu H \quad \cdots\cdots (13)$$

2) Efficiency characteristics

There are three factors that worsen the efficiency characteristics of the DC/DC converter using the RF5RD301 or RF5RD501:

(1) Power loss in the series regulator
(2) Power loss in the diode
(3) Power loss in the control transistor

In step-down operation, the step-up switching regulator is not operating. So the worsening factors are (1) and (2).

In the RF5RD301 and RF5RD501, the power consumption of the IC itself is very small. If it is ignored, the efficiency ηD in step-down operation is:

$$\eta D = \frac{Vout}{Vin + V_F} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (14)$$

In step-up operation, the step-up switching regulator is operating. So all of (1), (2), and (3) are worsening factors. Efficiency ηR due to loss (1) is:

$$\eta R = \frac{Vout}{Vout + 0.5} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (15)$$

Loss of (2) PD is:

$$PD = V_F \cdot Iout \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (16)$$

Loss of (3) PT is expressed as follows with the on-resistance of the control transistor as R_T:

$$PT = \frac{Vin}{Lx} \cdot ton \cdot R_T \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (17)$$

Therefore, the efficiency ηU of the DC/DC converter in step-up operation is:

$$\eta U = \frac{1-(PD+PT)}{Vin \cdot Iout} \cdot \frac{Vout}{Vout + 0.5} \quad \cdots\cdots\cdots\cdots\cdots (18)$$

■ **Selecting external parts**

1) Coil

In selecting the choke coil, the following should be satisfied:

- The core does not suffer magnetic saturation.
- There is a sufficient margin in the rated current.
- DC resistance is sufficiently low.
- Allowable loss is sufficiently large.

The following coils are recommended:

- CMD-6L (Sumida Electric Company Ltd., Model 6303-014, 015, 016 and 017)
- CM-5 (Sumida Electric Company Ltd., Model 6301-064, 065 and 066)
- CP-4LBM (Sumida Electric Company Ltd., Model 5201-053, 055, 066)

2) Diode

In selecting the diode, the following should be satisfied:

- The forward voltage is low.
- The turn-on time is short.
- There is a sufficient margin in the rated current.

Generally, Schottoky diodes are appropriate. Some, however, may increase the reverse current at high temperature.

3) Capacitor

In selecting capacitors, consider the following:

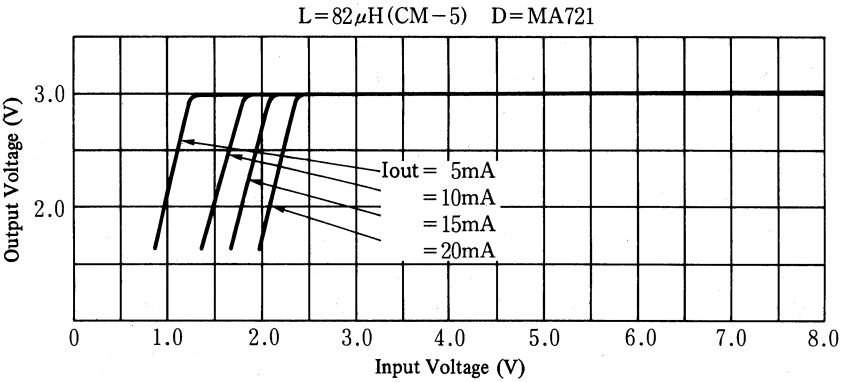
- The capacity is relatively large.
- The equivalent resistance is small.

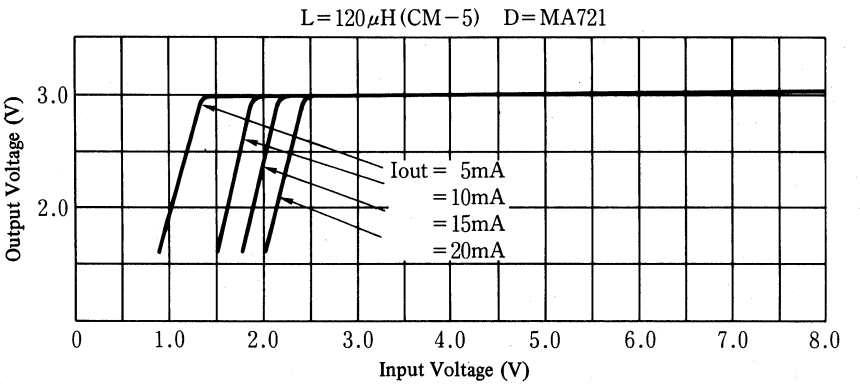
Generally, tantalum (aluminum) electrolytic capacitors and laminated ceramic capacitors are appropriate.

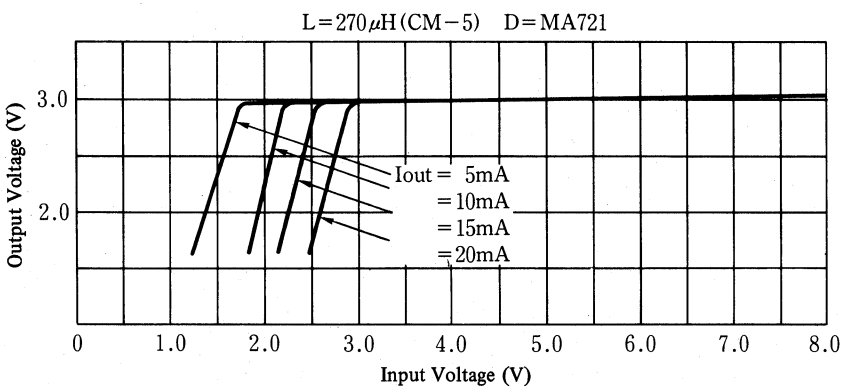
■ Characteristics

1) Output Voltage VS. Input Voltage (Ta=25°C)

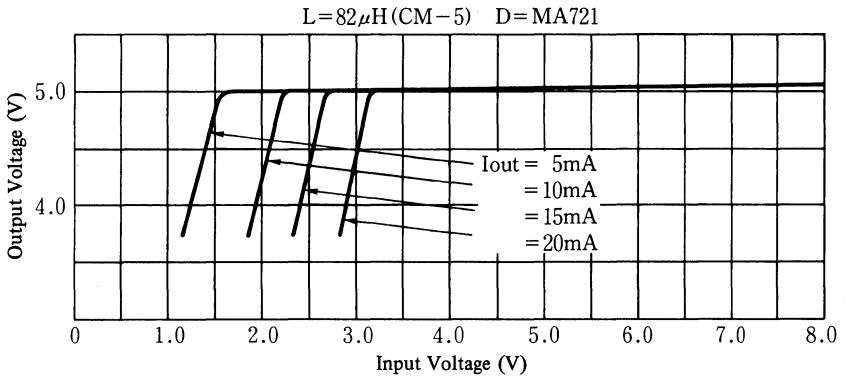
(1)RF5RD301

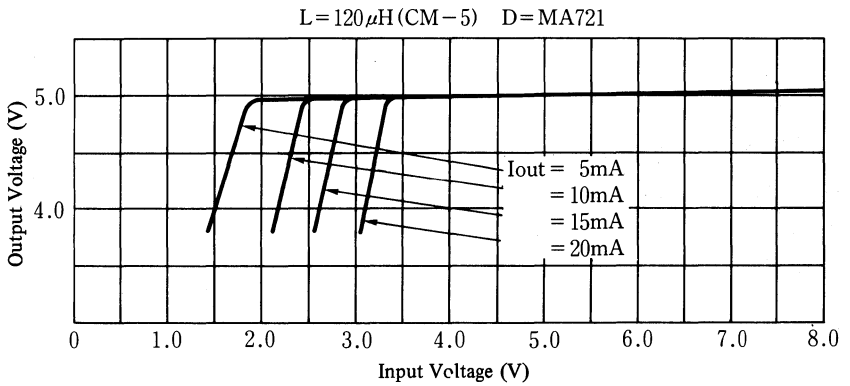


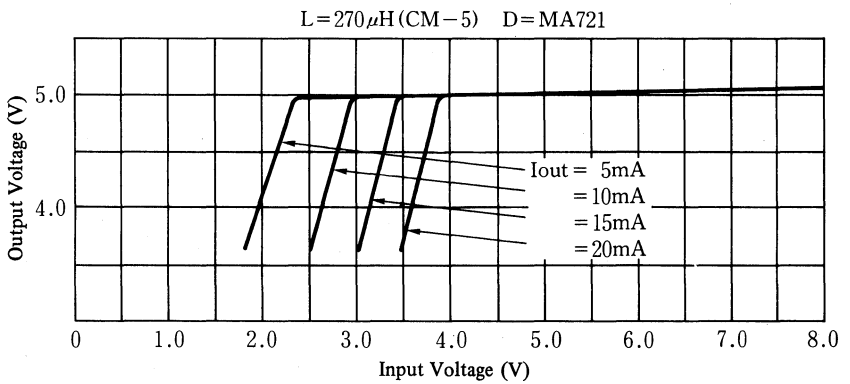




(2) RF5RD501

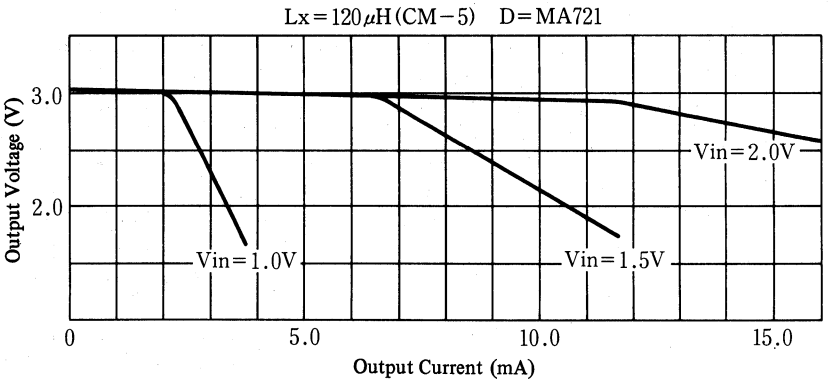

L=82μH(CM−5) D=MA721
Output Voltage (V)
5.0
4.0
Iout = 5mA
=10mA
=15mA
=20mA
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
Input Voltage (V)


L=120μH(CM−5) D=MA721
Output Voltage (V)
5.0
4.0
Iout = 5mA
=10mA
=15mA
=20mA
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
Input Voltage (V)

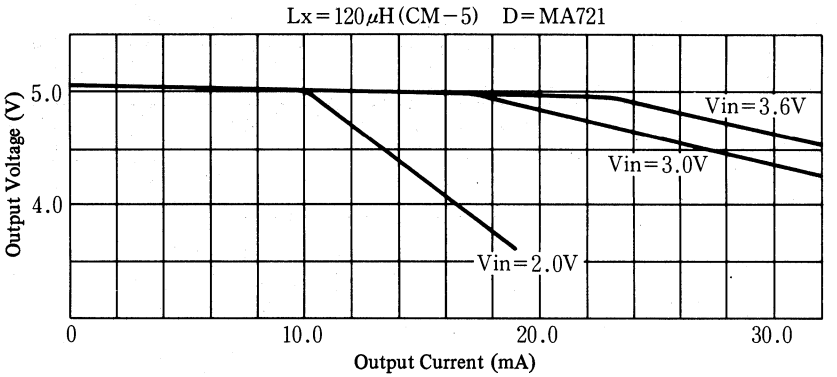

L=270μH(CM−5) D=MA721
Output Voltage (V)
5.0
4.0
Iout = 5mA
=10mA
=15mA
=20mA
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
Input Voltage (V)

2) Output Voltage VS. Output Current (Ta=25°C)

(1) RF5RD301

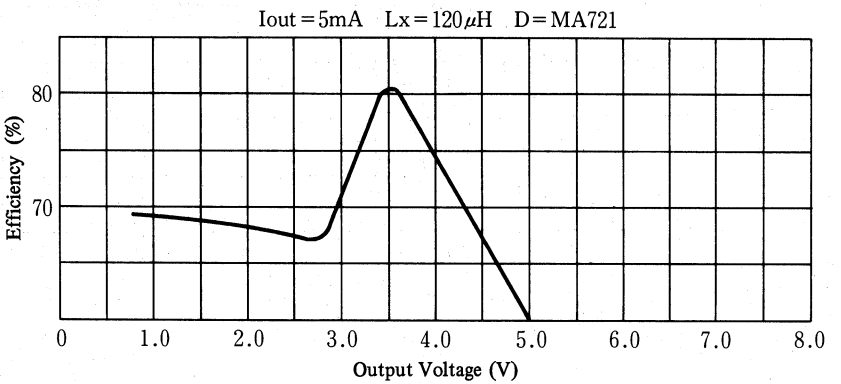


(1) RF5RD501

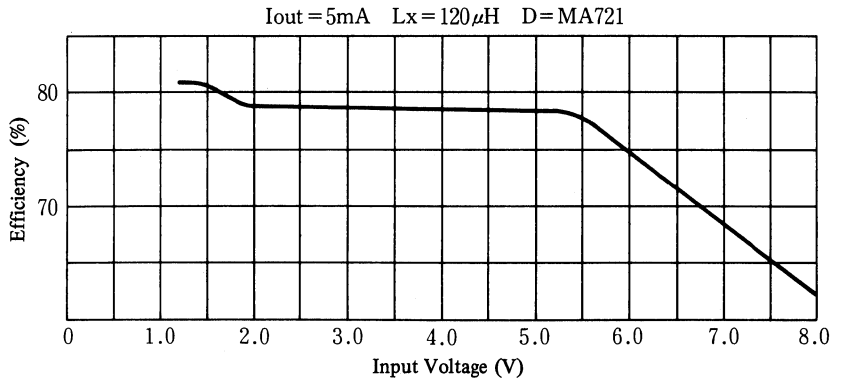


3) Efficiency VS. Input Voltage (Ta=25°C)

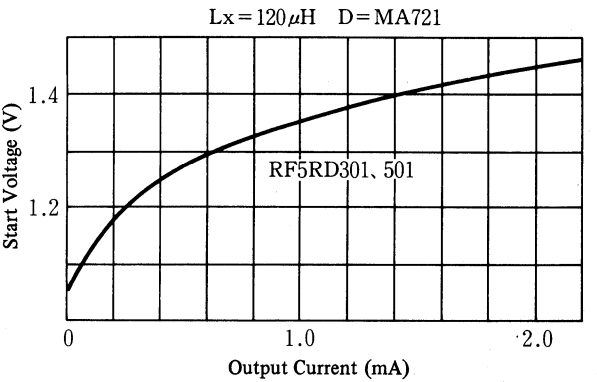
(1) RF5RD301



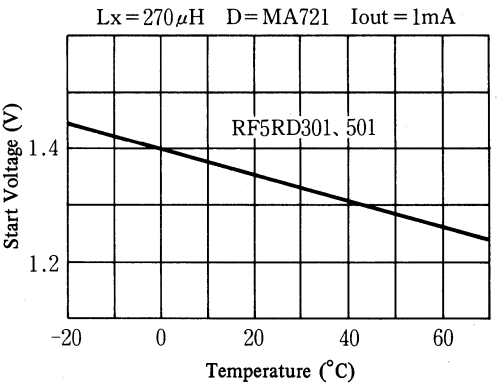
(2) RF5RD501



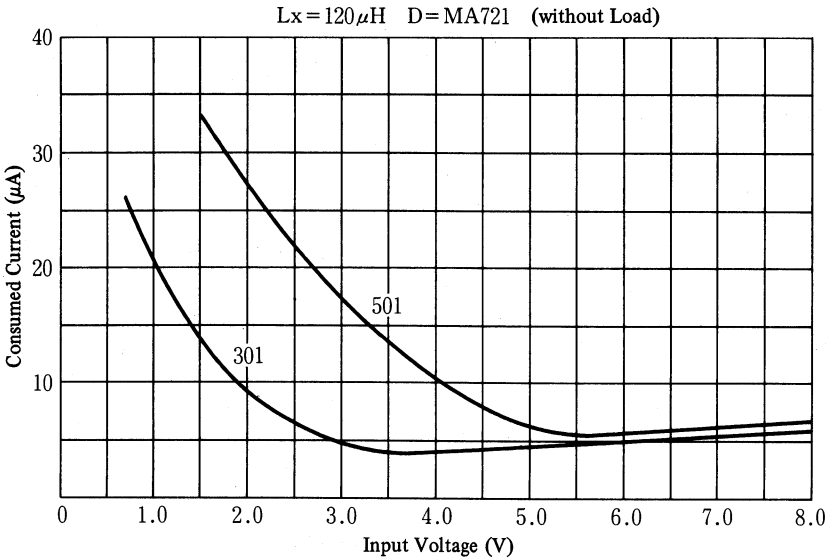
4) Start Voltage VS. Output Current (with Load) (T_a=25°C)



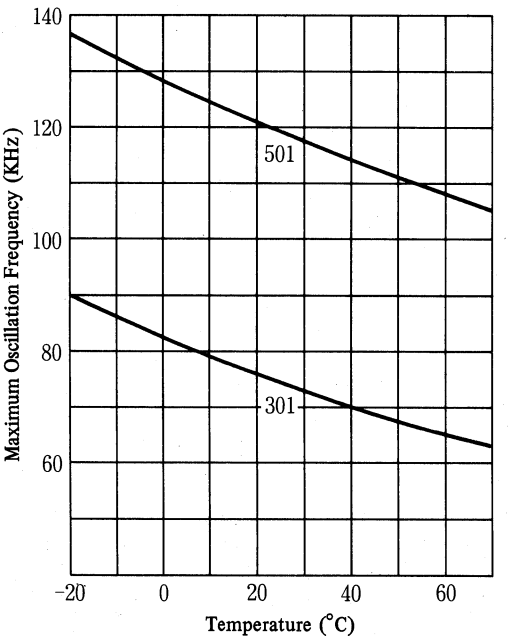
5) Start Voltage VS. Temperature



6) Consumed Current VS. Input Voltage (Ta=25°C)



7) Maximum Oscillation Frequency VS. Temperature



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