Rockwell

R65C19 Microcomputer

INTRODUCTION

SUMMARY

The Rockwell R65C19 Microcomputer (MCU) is a complete 8-bit microcomputer fabricated on a single chip using an N-well silicon gate CMOS process. The R65C19 complements an industry standard line of R6500 and R65C00 microprocessors, R6500/* and R65CXX microcomputers, and compatible peripheral devices. The R65C19 has a wide range of microcomputer applications where high 8-bit performance, minimal chip count and low power consumption is required.

The R65C19 consists of an enhanced 6502 Central Processing Unit (CPU), 16K bytes of mask programmable read only memory (ROM), 512 bytes of random access memory (RAM), two 16-bit counter/timers with four selectable modes each, two 17-bit precision time generators, an asynchronous/synchronous serial port, an expansion port, and 44 input and/or output lines. Three 8-bit parallel input/output ports, one 8-bit port with 4 I/O pins and 4 input only pins, one 8-bit output port, and one 4-bit output port comprise the 44 individual lines. Forty-two I/O lines can be assigned to special purpose functions under software control.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, result in system cost-effectiveness and a wide range of computational power. These features make the R65C19 a leading candidate for low-power single-chip microcomputer applications.

Hardware enhancements of the R65C19 include a software-controlled memory access function, a counter/timer clock prescaler, and an ultra-low-power Stop and Idle mode.

FEATURES

- Enhanced R6502 CPU
  - 12 new bit manipulation and branching instructions to shorten code and speed up execution
  - 21 new arithmetic processing instructions to optimize arithmetic processing
  - 10 new direct threaded code instructions to support high level languages that compile linked machine instructions
- Internal Memory
  - Internal masked ROM: 16484 bytes
  - RAM: 512 bytes
  - Dual port general purpose RAM for host bus interface (15 bytes) or 16450 emulation
- 44 general purpose I/O lines
  - 28 bidirectional input/output (ports A, B, C, and D) with data latches and direction registers
  - 4 input only lines (Port D)
  - 12 output only lines with data latches (Ports E and F)
  - 42 I/O lines can be software assigned to special purpose functions
- Two identical 16-bit programmable counter/timers with latches
  - Four modes
    - Interval Timer
    - Pulse Generation
    - Pulse Width Measurement
    - Event Counter
  - Selectable divide-by-32 prescaler
  - Timer interrupt can be vectored to either ROM or page 1 RAM
  - I/O port interface
- Two 17-bit precision time generators (PTGs) with latches
  - Increment/decrement capability
  - Counter option (clear accumulator on overflow)
  - Interrupt enables
  - Output port interface

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ROCKS002

- USART Serial I/O
  - Asynchronous features
    - 5-, 6-, 7-, or 8-bit characters
    - Even, odd, stuff or no parity bit generation and detection
    - 1, 1-1/2 or 2 stop bit generation with 3/4 or 7/8 stop bit control
    - False start bit detection
    - Interrupt enables
    - Line break generation and detection
  - Synchronous features
    - Serial input (SIN) timing – internal, external or Transmit Clock (TXCLK)
    - Serial output (SOUT) timing – internal or external
    - 5-, 6-, 7-, or 8-bit characters
    - Automatic word sync on first 1 to 0 transition

Interrupt enables for Serial Input Clock (SICLK) and Serial Output Clock (SOCLK)

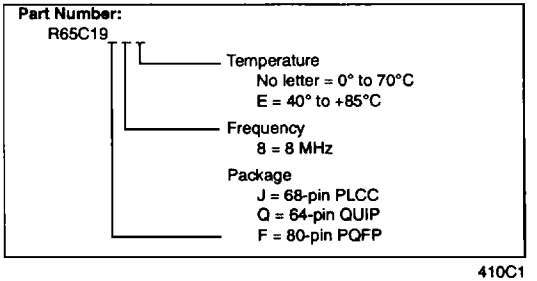
- Bus Expansion
  - Software selectable expansion bus address range
    - 64K bytes, 16 address lines (A15 mask option)
    - 32K bytes, 15 address lines
    - 16K bytes, 14 address lines
    - 8K bytes, 13 address lines
    - 256 bytes, 8 address lines
  - 8-bit data bus (D0-D7) multiplexed with addresses A4-A11
  - A0 through A3 software selectable on Port F (PF0-PF3)
  - A12 through A14 software selectable on Port F (PF4-PF6)
  - Address Latch Enable (ALE) pin for latching A4 through A11
  - Four external chip select lines (ES1-ES4) software selectable
    - ES1 - 32K, 24K (Mask Option)
    - ES2 - 8K, 12K (Mask Option)
    - ES3 - 4K, 8K (Mask Option)
    - ES4 - 2K
  - Clocks
    - $\overline{RT}$ - Read strobe
    - $\overline{WT}$ - Write strobe
- Eight levels of prioritized, vectored interrupts
  - RESET (highest priority)
  - Non-mask interrupt (NMI)
  - Six prioritized interrupt requests (IRQ1-IRQ6)
    - Six IRQ ROM vectors
    - Two software selectable Timer IRQ page 1 RAM vectors
- Internal 1 MHz to 8 MHz clock with crystal or clock input
  - 250 ns minimum execution time at 8 MHz
  - Internal divide-by-1 or divide-by-2 mask option
  - 2 MHz to 16 MHz crystal input
  - Stop mode, software enabled
    - Oscillator stopped, internal (C1) clock held high
    - Ultra-low power dissipation, power-on sequence to normal operation
    - Cleared by RESET
    - Cleared to idle mode by logic one on PB3, software enabled.
    - Full operation from idle mode resumes following a negative transition on PB3, software enabled
  - Idle mode, software enabled
    - Oscillator runs, C1 clock held high
    - Low power dissipation, immediate normal operation resumption
    - Cleared by negative transition on logic term (PD4 + PD5), software enabled
    - Cleared by PB3 negative transition, software enabled
    - Cleared by RESET
  - Requires external capacitors with crystal input
- Available packages
  - 64-pin quad in-line package (QUIP)
  - 68-pin plastic leaded chip carrier (PLCC)
  - 80-pin plastc quad flat pack (PQFP)
- +5 V ±10% power
- Emulator Device
  - 68-pin PLCC with A13 through A15 and SYNC output pins

ROMLESS VERSIONS

There are two ROM-less versions of the R65C19. These parts have the options necessary to provide prototyping devices for system development and to be used in production systems when on-board ROM is not required. Both devices are in 68-pin PLCC J-lead packages,

The two devices are the C1999J and the C1997J. THe only differences in these devices are their mask coded options. See Appendix B for option information.

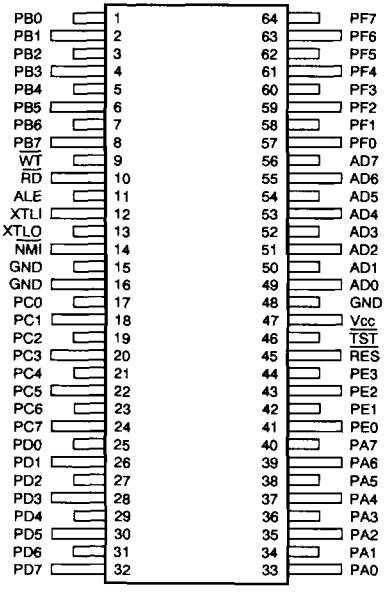
ORDERING INFORMATION



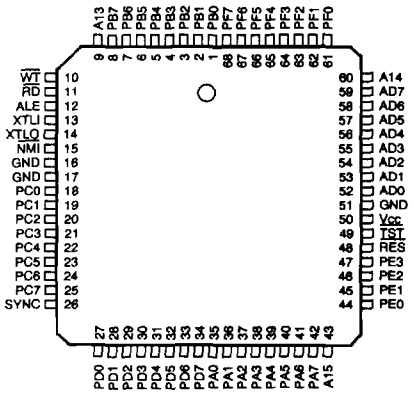
INTERFACE DESCRIPTION

The R65C19 pin assignments are shown in Figure 2-1.

The I/O signals are shown in Figure 2-2 along with the major interfacing R65C19 functions. The I/O pin signals are defined in Table 2-1.



a. 64-Pin QUIP



b. 68-Pin PLCC

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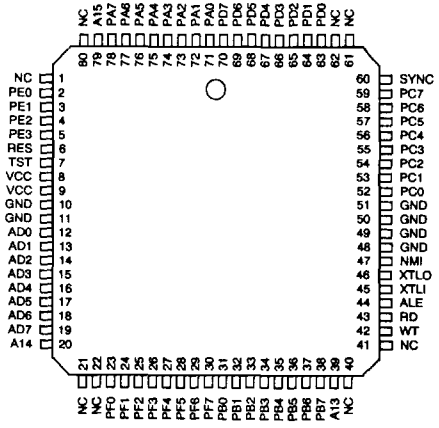

c. 80-Pin PQFP

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Figure 2-1. R65C19 Pin Assignments

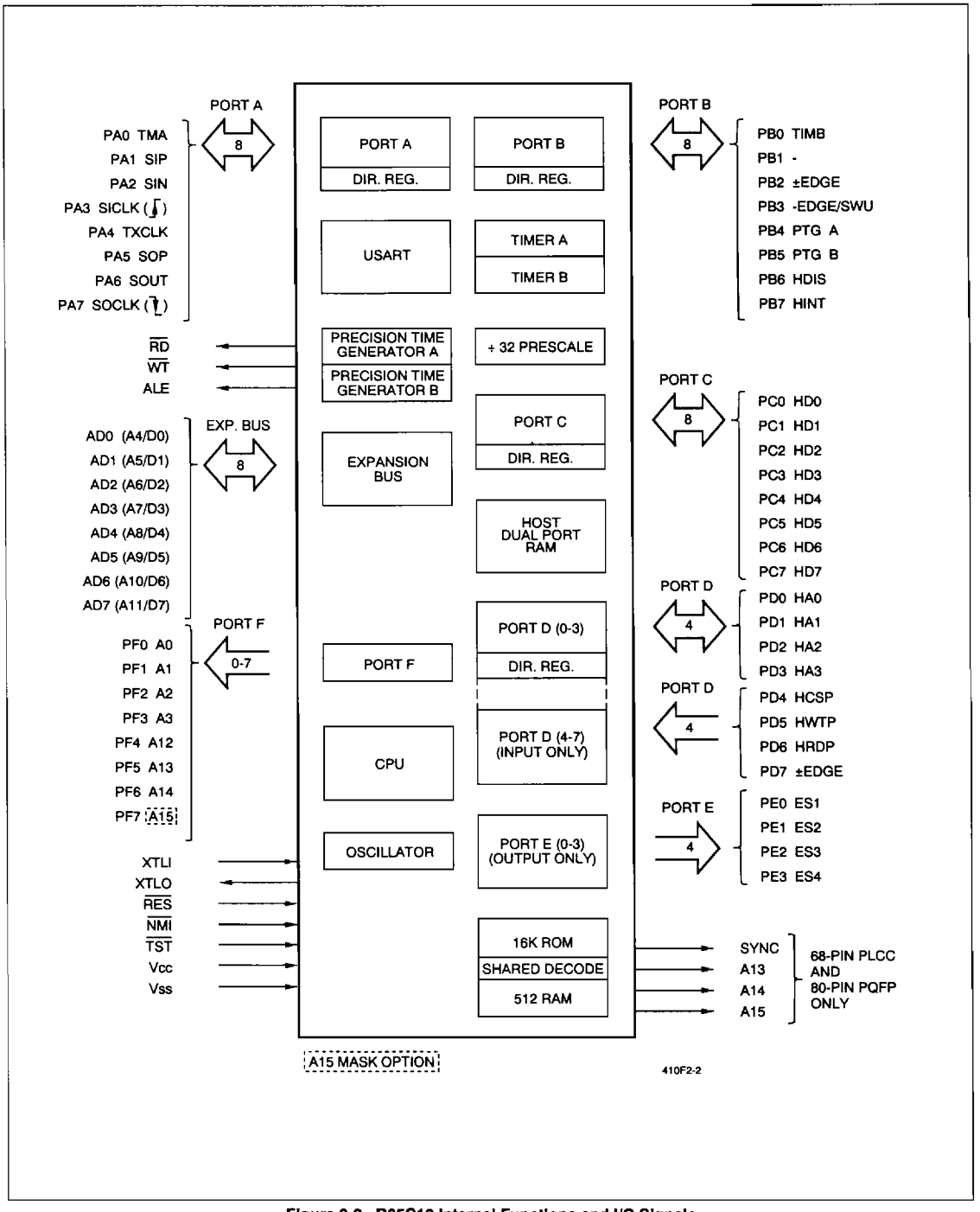


Figure 2-2. R65C19 Internal Functions and I/O Signals

SYSTEM ARCHITECTURE

The top level memory maps in Figures 3-1 and 3-2 show major boundaries between I/O, internal ROM, internal RAM, and external addresses for the R65C19. Figure 3-2 shows the memory map for internal ROM and expansion bus external selects ES1, ES2, ES3 and ES4. The map shows how the size of ES1, ES2 and ES3 can be modified by a user selectable mask option.

CENTRAL PROCESSING UNIT (CPU)

The central processing unit (CPU) is an enhanced 8-bit 6502 CPU. The CPU executes stored instructions fetched from memory (usually internal masked ROM) sequentially unless a jump to a new location is specified in the instruction or an interrupt occurs. Operation of the new instructions are described in Appendix A. The R65C19 is 6502 instruction compatible except "(indirect, X)" addressing mode changed to "(indirect)", and "(indirect), Y" changed to "(indirect), X".

The R65C19 CPU registers are the same as the 6502 CPU with the addition of the W-register and I-register.

The data flow for the CPU registers is illustrated in Figure 3-3.

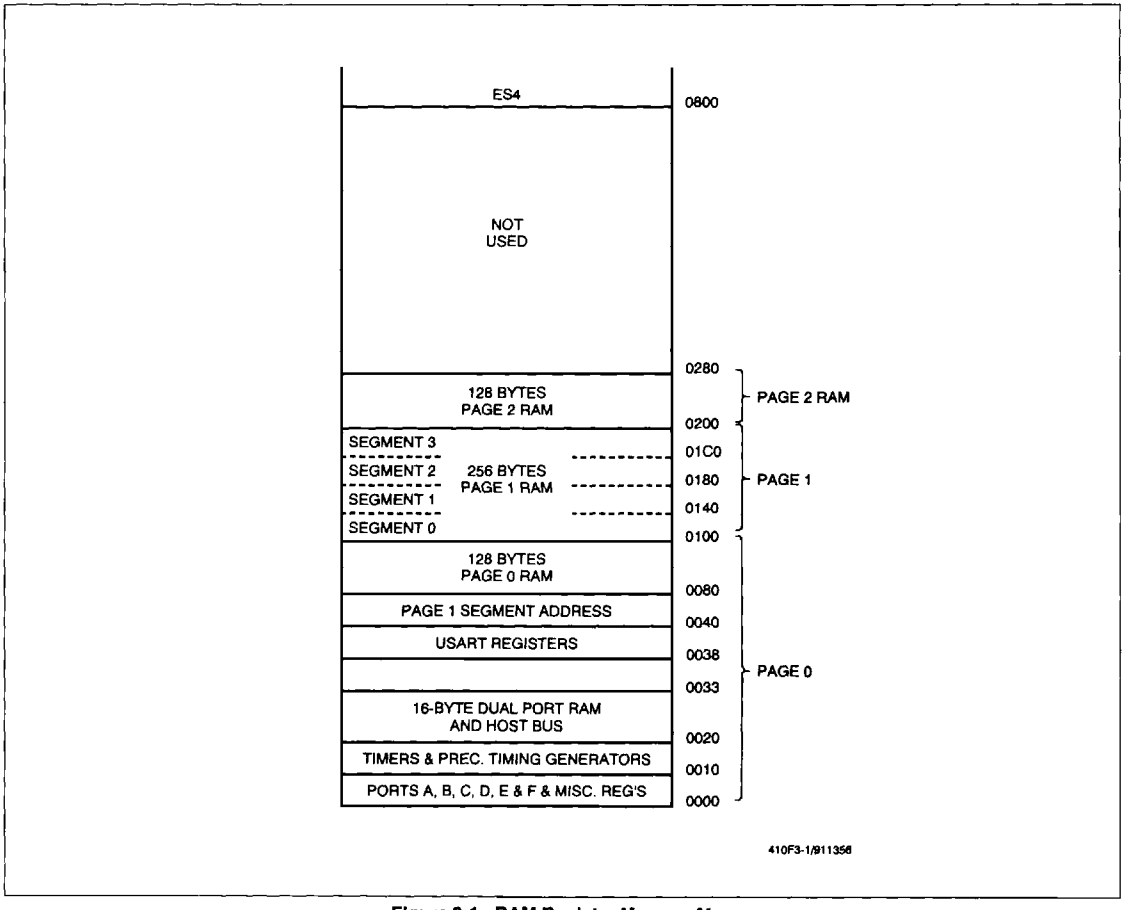


Figure 3-1. RAM Register Memory Map

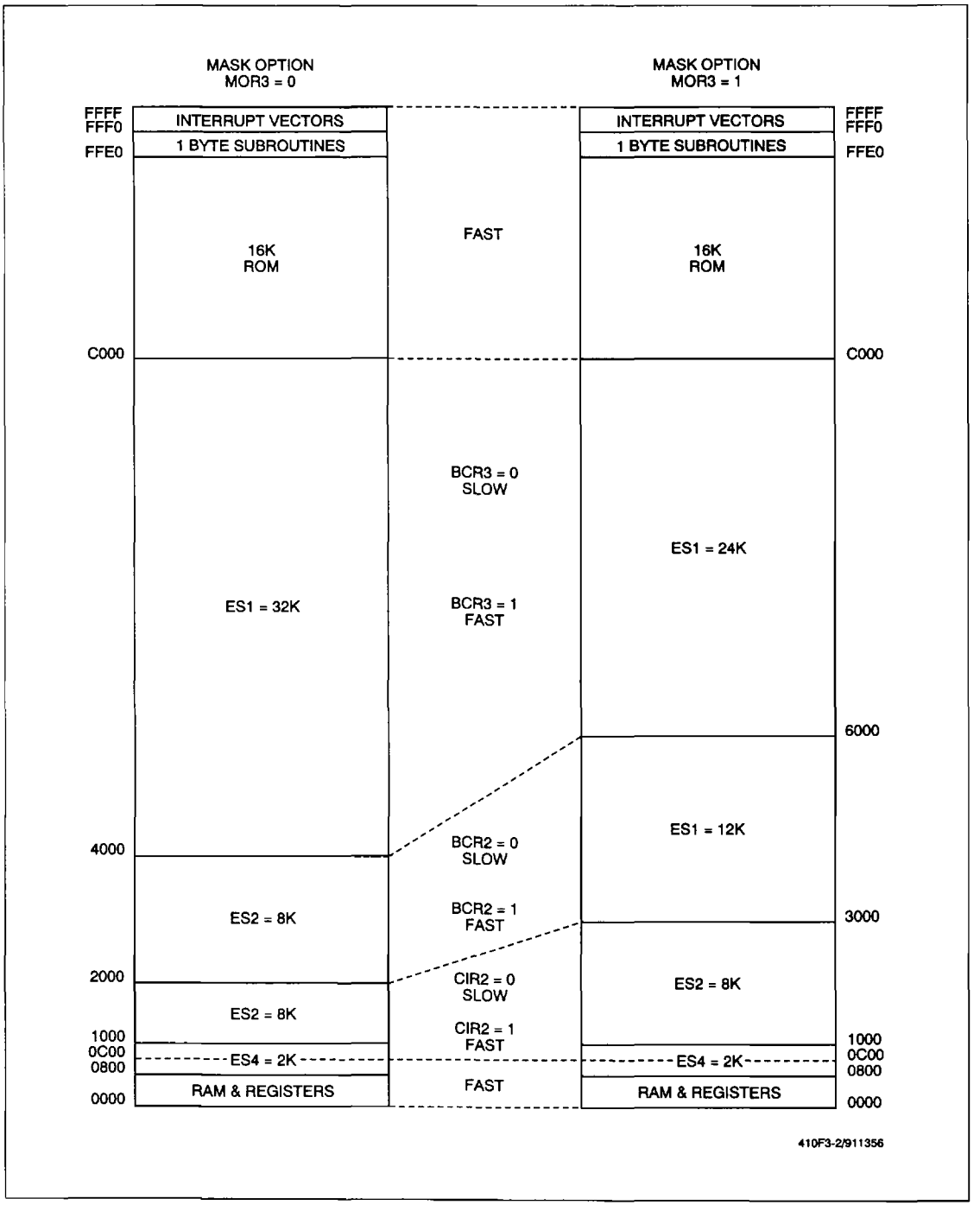


Figure 3-2. Expansion Bus Memory Map

Index Registers

There are two 8-bit index registers: X and Y. Either index register can be used as a base to modify the program counter contents and thus obtain a new address — the sum of the program counter contents and the index register contents. When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Stack Pointer

The Stack Pointer is an 8-bit register that controls access to the stack. The stack is initialized under software control usually to the top of Page 1 RAM. The stack length can be up to 256 bytes ($1FF down to $100).

The Stack Pointer is automatically incremented and decremented under control of the CPU to perform stack manipulation in response to program instructions, a reset, a non-maskable interrupt (NMI), an internally generated interrupt request (IRQ), or execution of the CPU Break (BRK) instruction. The Stack Pointer must be initialized by the user program. The JSR, JPI, PIA, BRK, RTI, and RTS instructions use the stack and the Stack Pointer.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data is placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic 0; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

Accumulator (A)

The Accumulator (A) is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the Accumulator usually contains one of the two data bytes used in these operations.

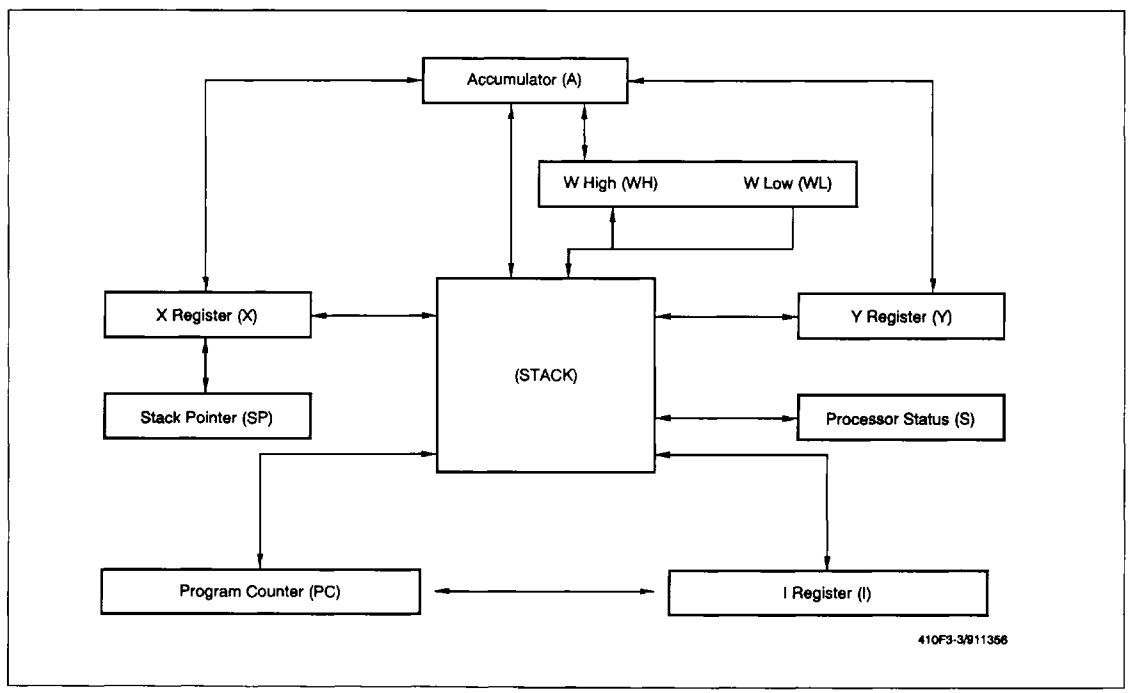


Figure 3-3. CPU Registers and Data Flow

Program Counter (PC)

The 16-bit Program Counter (PC) provides the addresses that step the processor through sequential instructions in a program. Each time the processor fetches an instruction from the program memory, the least significant byte of the Program Counter (PCL) is placed on the eight low-order lines of the internal address bus and the most significant byte of the Program Counter (PCH) is placed on the eight high-order lines of the internal address bus. The Program Counter is incremented each time an instruction or data byte is fetched from program memory.

Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the internal data bus. These instructions are latched then decoded along with timing and interrupt signals to generate control signals for the various registers.

W Register (W)

The 16-bit W register is used exclusively to perform the accumulate function during execution of the Multiply Accumulate (MPA) instruction.

I Register (I)

The 16-bit I register is used for threaded code instructions. Note that the I register should not be confused with the CPU Instruction register which is not addressable.

Processor Status Register (PSR)

The 8-bit Processor Status Register (Figure 3-4) contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user program and the CPU. The instruction set contains a number of conditional branch instructions which allow testing of these flags.

CLOCK OSCILLATOR

The Clock Oscillator provides the basic timing signals used by the R65C19 internal circuits. The reference frequency can be supplied by either a parallel resonant crystal or a clock input.

Divide-by-2 or Divide-by-1

The input frequency is divided either by 2 or by 1 to generate the internally $\phi 2$ clock. Divide-by-2 or divide-by-1 is a mask option. The divide-by-2 option must be selected when an external crystal is used.

Typical clock oscillator input circuits are shown in Figure 3-5.

An external parallel resonant crystal should be selected with an R_S of less than or equal to 15 ohms. C_2 (Figure 3-5) should be selected to be 1.2 to 2.1 times greater than C_1, where C_1 will be in the range of 18 pF to 33 pF. Values of C_1 and C_2 will need to be adjusted due to variance in stray board capacitance.

For EMI considerations the crystal leads and loading capacitors C_1 and C_2 should be located as close to the XTLI and XTLO pins as possible.

Stop Mode

The Stop Mode of operation is selectable under software control for ultra-low power dissipation. Bits in the Bus Control Register (BCR) initiate Stop and Idle modes. In the Stop mode, the clock oscillator is halted with the internal $\phi 2$ clock held low (C1 high). Stop Mode is invoked by writing a 1 to BCR7. Normal operation is initiated either by reset or by a high on PB3 for at least 4 ms when BCR5 is a logic 1. The clock oscillator requires 4 ms to stabilize before normal operation is attained (the same as the power turn-on requirements). When PB3 is used to terminate Stop, the oscillator is turned on when PB3 switches from low (0) to high (1), and internal timing starts when PB3 makes a high (1) to low (0) transition.

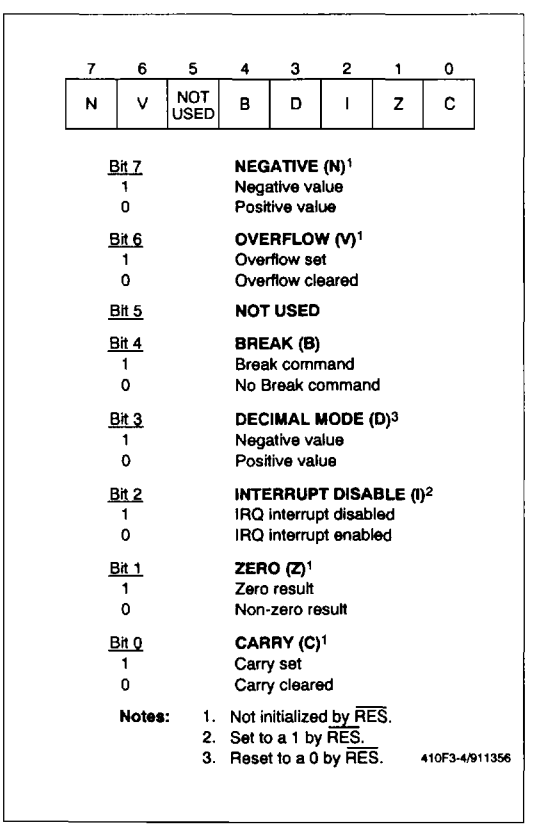


Figure 3-4. Processor Status Register

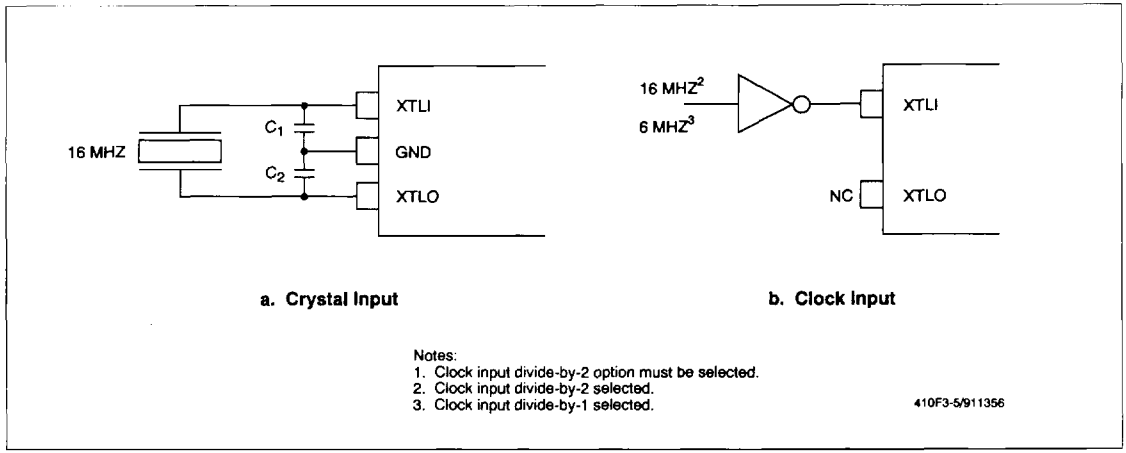


Figure 3-5. Clock Oscillator Input Options

Idle Mode

The low-power Idle Mode of operation is also selectable under software control. In the Idle Mode, the internal $\phi 2$ clock is halted low (C1 high), however, the clock oscillator continues to run allowing immediate return to normal operation since clock oscillator turn-on time is not required as in the Stop Mode. Idle mode is invoked by writing a 1 to BCR6 and a 1 to BCR4 and/or BCR5. Normal operation is resumed by a high-to-low transition on PB3 when BCR5 is a logic 1, or by a high-to-low transition by the logic term (PD4 + PD5) when BCR4 is a logic 1. When both BCR4 and BCR5 are set to logic 1s, idle is cleared by either a high-to-low transition on PB3 or by a high-to-low transition of the logic term (PD4 + PD5).

IRQ INTERRUPT LOGIC

The IRQ Interrupt Logic prioritizes the individual interrupt requests (IRQ1-IRQ6) from the various sources and passes a single IRQ along with an IRQ number (1-6) and the IRQ vector page indicator to the CPU Interrupt Logic. Figure 3-6 illustrates the IRQ Interrupt Logic interface.

If simultaneous IRQs occur on IRQ1-IRQ6 lines, the number of the highest priority IRQ (1=highest) is passed to the CPU. When the interrupt flag causing the IRQ is cleared by the IRQ interrupt service subroutine, the IRQ number of the highest pending IRQ is passed.

The selection of ROM or RAM IRQ interrupt vectors for Timer A (IRQ5) and Timer B (IRQ3) is determined by bits 5 and 6 in the Timer A Mode and Timer B Mode registers, respectively.

CPU Interrupt Logic

CPU interrupt logic controls the sequencing of the $\overline{\text{RES}}$, $\overline{\text{NMI}}$, and IRQ activated interrupts and the CPU BRK instruction.

RES Sequencing

A low-to-high transition on $\overline{\text{RES}}$ causes the Interrupt Disable (I) bit in the Processor Status Register to set and program execution to begin at the address fetched from the RES vector ($FFFE and $FFFF).

NMI Sequencing

At the first operation code fetch following the high-to-low transition of the $\overline{\text{NMI}}$ input, the interrupt logic forces execution of the Break (BRK) instruction and subsequent execution from the address vector stored at $FFFC and $FFFD. Simultaneous with the execution of the BRK instruction, the Interrupt Disable bit in the Processor Status Register is set to disable an IRQ.

IRQ Sequencing

An IRQ interrupt occurs when the Interrupt Disable (I) bit of the Process Status Register is cleared (0) and $\overline{\text{IRQ}}$ has been asserted from the IRQ Interrupt Logic. Upon IRQ interruption, the BRK instruction is forced and subsequent program execution begins at the IRQ interrupt service subroutine location specified by the IRQ interrupt vector corresponding to the IRQ number (1-6). The IRQ vector is located in one of six locations in ROM ($FFF0-$FFFB) or one of four locations in RAM ($0102-$0103, $0106-$0107, $0108-$0109, or $010A-$010B). The page 1 RAM IRQ vectors are Timer A and Timer B options, respectively.

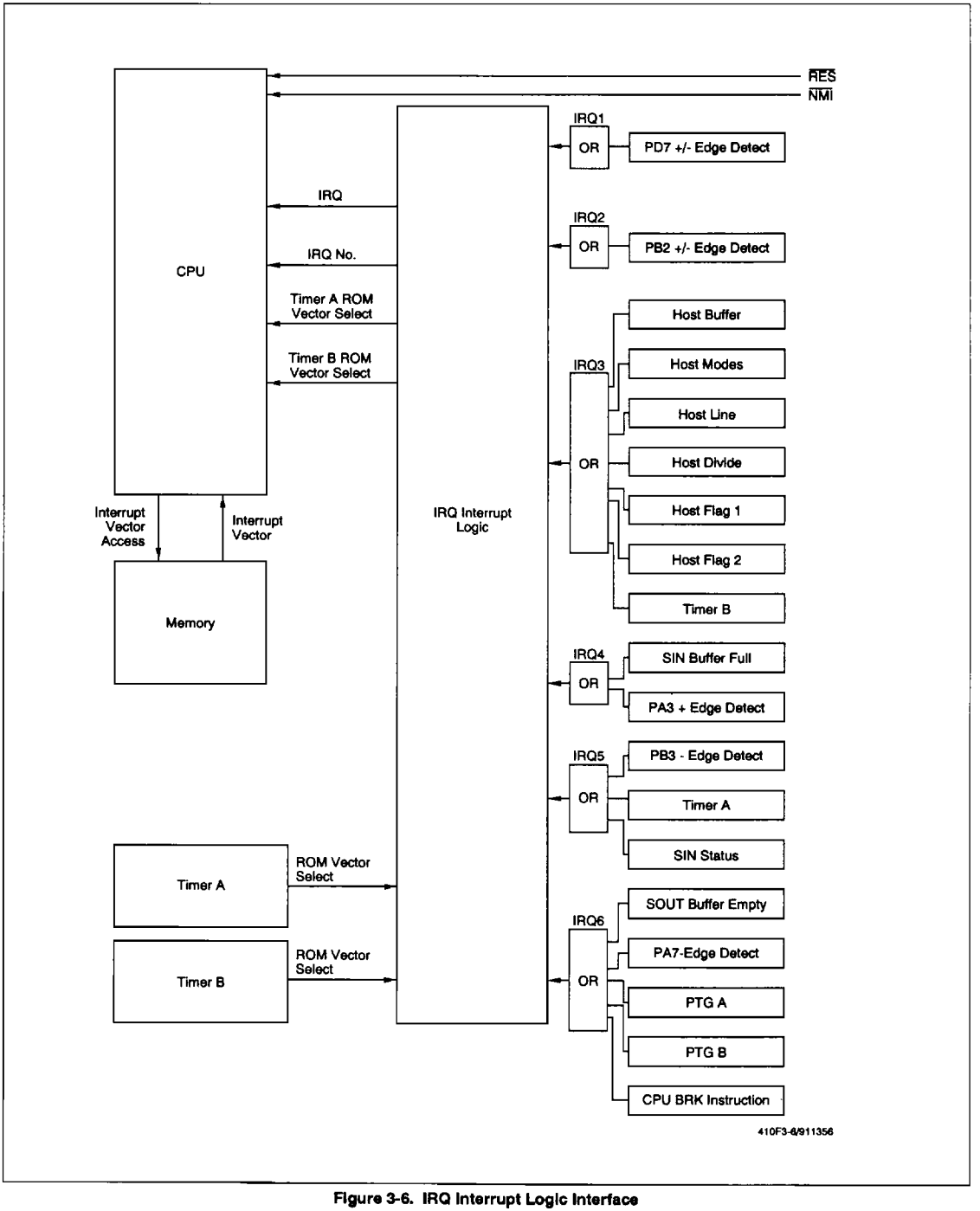


Figure 3-6. IRQ Interrupt Logic Interface

The I bit is set to inhibit further IRQ interruption until completion of the IRQ interrupt service subroutine, at which time the I bit is automatically cleared by the RTI instruction. The I bit can also be cleared under program control with the CLI instruction.

For each IRQ that has multiple sources of interruption, the IRQ service subroutine must determine the source of the interrupt by examining applicable interrupts flags. The interrupt flag causing the IRQ should also be cleared after processing the interrupt and before before returning to the interrupted routine.

INTERNAL ROM

The internal Read Only Memory (ROM) usually contains the user's program instructions and other fixed constants. These program instructions and constants are mask-programmed during fabrication.

The R65C19 ROM size is 16484 bytes and is memory mapped from $C000 to $FFFF.

INTERNAL RAM

The internal Random Access Memory (RAM) contains the user program stack and is used for scratch pad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data. In the event that execution stops, RAM data is retained until execution resumes.

The RAM size is 512 bytes. The first 128 bytes are assigned to page 0 ($80 to $FF). The next 256 bytes are mapped on page 1 ($100 to $1FF). Another 128 bytes are mapped on page 2 ($200 to $27F).

PARALLEL INPUT/OUTPUT PORTS

The R65C19 parallel input/output interface consists of five 8-bit ports. Ports A, B and C contain 24 bidirectional lines with the data direction determined by the direction registers. Port D has 4 bidirectional lines (0-3) with the data direction determined by its direction register, and 4 input only lines (4-7). Ports E and F support 12 output-only lines. All 44 port lines can be used for general purpose functions except when pre-assigned by a mask option. Forty-two I/O lines can be assigned special functions under software control.

Output Mode

The data written to each output pin is loaded into an output data latch. The data will remain in the output latch until new data is written to the port address or until power is removed.

The output latches are individually connected to output drivers. The output drivers are double-ended, push-pull type. The drivers force the output pins high (2.4V) if the output data bit is a logic 1, or low (0.4V) if the output data bit is a logic 0. The output drivers are TTL compatible.

The External Interrupt Register (EIR) and Clear Interrupt Register (CIR) are associated with port B and D lines (see Figures 3-7 and 3-8, respectively). The CIR bits are cleared by writing zero to the register.

Bidirectional Ports A, B, and C

Ports A, B, and C consist of 24 general purpose bidirectional input/output lines. The data direction for each I/O line is controlled by an associated direction register bit. For each direction register bit that is a logic 1, the corresponding port line is an output. Conversely, a 0 in a direction register bit defines the corresponding port line as an input. The direction register bits are initialized to a 0 by reset causing the I/O ports to be inputs.

All port A, B and C lines can alternatively be assigned to special purpose functions either during operation under software control or permanently as a mask option.

The port A lines can be assigned to special functions under software control. PA3 and PA7 have associated edge detect logic that can generate an IRQ interrupt.

Seven port B lines can be assigned to special functions under software control and one line can be permanently masked to a special function. PB2 and PB3 have associated edge detect logic that can generate an IRQ interrupt.

All eight port C lines can be assigned to host bus data lines under software control.

Bidirectional and Input Only Port D

The eight port D lines are grouped as four general purpose bidirectional input/output lines and as four input only lines. PD7 has associated edge detect logic that can generate an IRQ interrupt. Seven lines (PD0-PD6) can be assigned by software as host bus address and control line inputs. The direction register control bits for port D must be set high (1) for output and low (0) for input. The direction register control bits are initialized to 0 by reset.

Output Port E

The four port E lines (PE0-PE3) are general or special purpose output only. Lines PE0-PE3 can be permanently assigned to ES1-ES4 chip select functions by the ES mask option. Port E output latches are initialized low upon reset. The Port E output drivers tri-state (float) during reset active low.

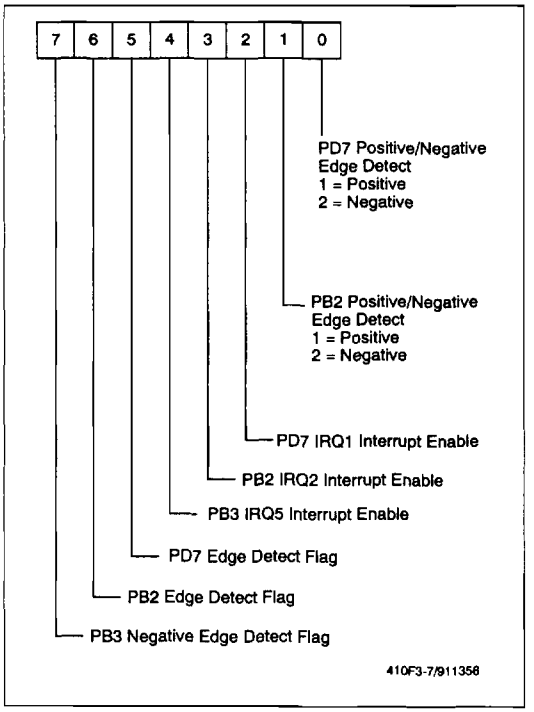


Figure 3-7. External Interrupt Register (EIR) - $000A

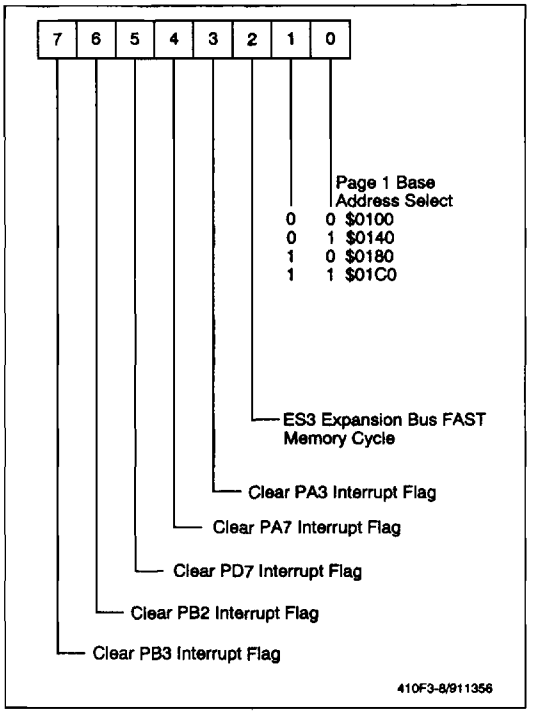


Figure 3-8. Clear Interrupt Register (CIR) - $000B

Output Port F

The eight port F lines (PF0-PF7) can be used as address extension, general purpose or test/emulate outputs. Address extension is controlled by BCR0 and BCR1 (3.10). These lines are assigned to address extension upon reset since BCR0 and BCR1 are initialized to 0 by reset. PF7 can be permanently masked to the A15 output.

When the $\overline{TST}$ pin input is grounded (Test Mode), the PF0-PF4 outputs are forced to A0-A3 and A12, respectively.

COUNTER/TIMERS

There are two separate 16-bit counter/timer systems in the C19: Counter/Timer A (called Timer A) and Counter/Timer B (called Timer B). Operation of the two counter/timers is identical except for register addresses, the generated IRQ (and priority level) and the interfacing I/O port. The operation of Timer A is described in detail followed by a description of Timer B differences. Block diagrams of Timer A and Timer B are shown in Figures 3-9 and 3-10, respectively. The Timer A and Timer B Mode Registers are shown in Figure 3-11.

A divide-by-32 counter connected to $\phi 2$ clock is shared by both timers. The counter provides a $\phi 2/32$ clock that can be individually selected by each timer.

Timer A Registers

Timer A is composed of a 16-bit latch, a 16-bit counter and an 8-bit snapshot register (Figure 3-9). The latch consists of two 8-bit registers, Timer A Upper Latch (TAUL) and Timer A Lower Latch (TALL). The counter also consists of two 8-bit registers, Timer A Upper Counter (TAUC) and Timer A Lower counter (TALC). The snapshot register is referred as Timer A Snapshot (TAS). Timer A operation is controlled and monitored using the Timer A Mode Register.

When Timer A underflows, the Timer A Interrupt Flag bit in the (TAM7) is set to a logic 1. This bit can be used to assert IRQ5.

The Interrupt vector for Timer A may be in either ROM ($FFF2) or in RAM ($0102), depending on Timer A Mode Register bit 6.

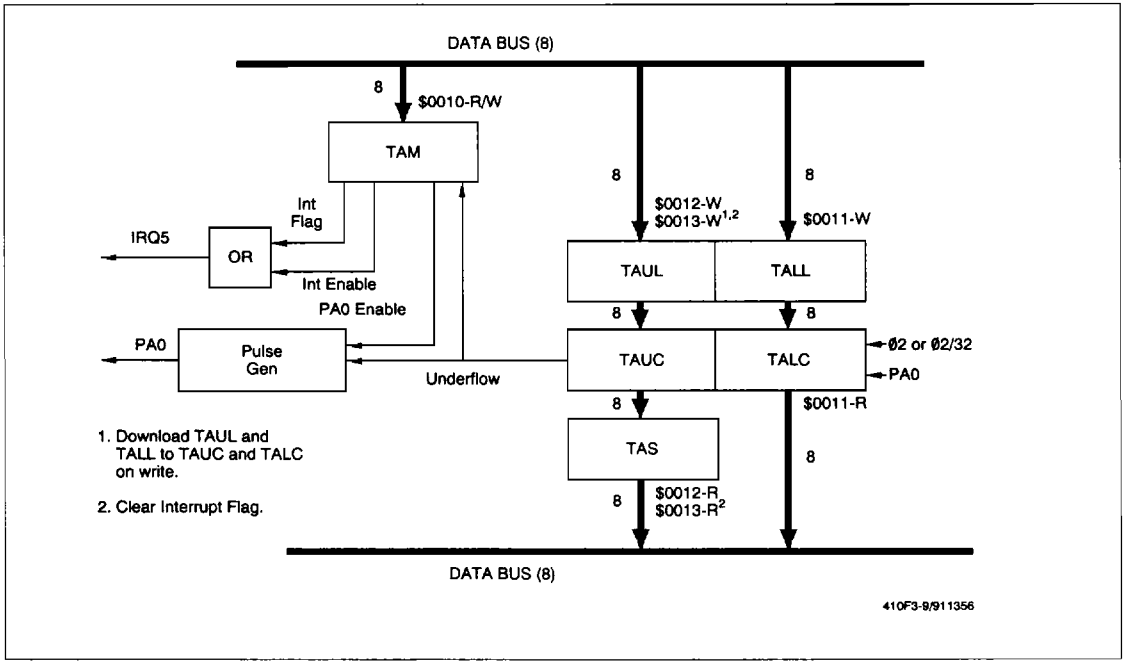


Figure 3-9. Counter/Timer A Block Diagram

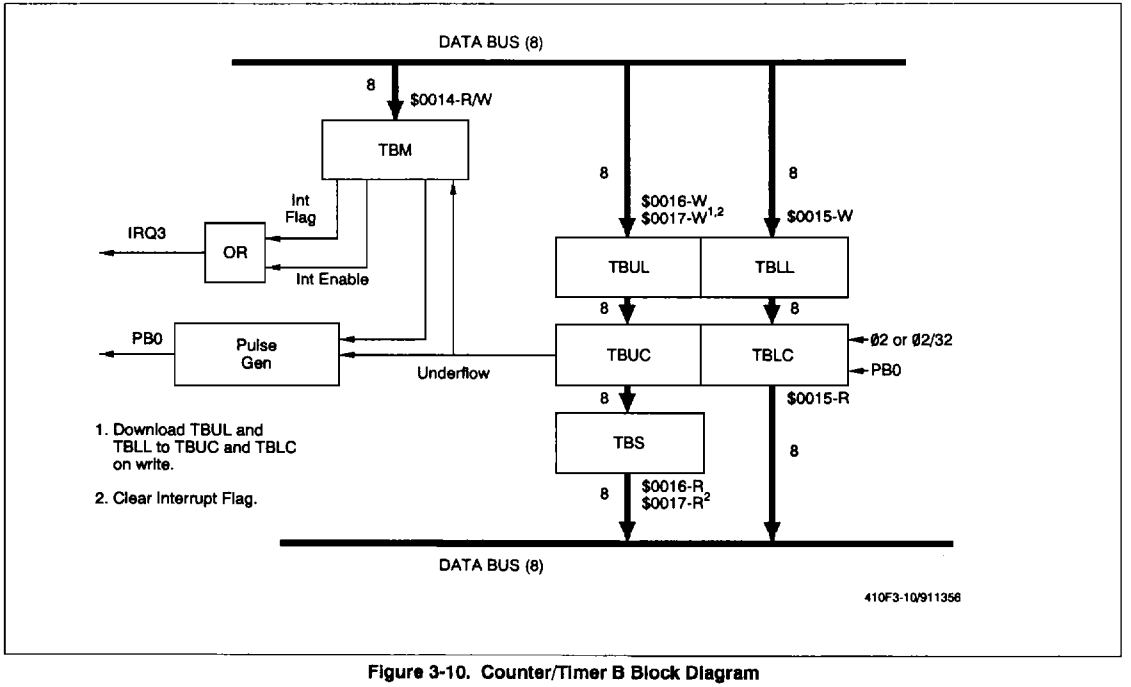


Figure 3-10. Counter/Timer B Block Diagram

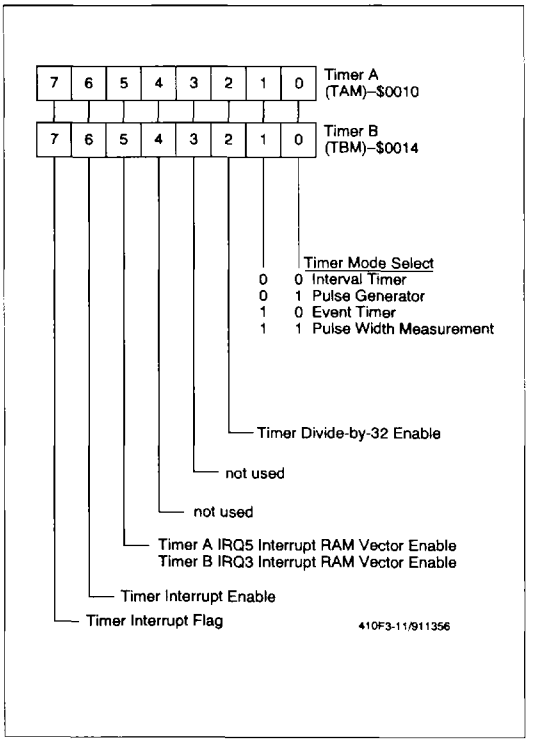


Figure 3-11. Timer A and Timer B Mode Registers

Timer B Registers

Timer B (Figure 3-9) is structured identical to Timer A. Timer B registers are located at $0014-$0019. When the Timer B Underflow Flag is set (TBM7) and enabled (TBM5 and TBM6), IRQ3 is asserted. Timer B interfaces with I/O port PB0 rather than PA0.

The Interrupt Vector for Timer B may be in either ROM ($FFF6) or in RAM ($0106), depending on Timer B Mode Register bit 6.

Timer Modes

Since mode operation of both counter/timers is similar, mode operation is described for Timer A with Timer B operation indicated in parentheses.

Mode 0 - Interval Timer

Writing to TAUL (TBUL) transfers the 16-bit latch value to the counter. The counter counts down at the $\phi 2$ or $\phi 2/32$ rate. When the counter counts through zero, the TAIF (TBIF) is set to a 1, the value in the latches is transferred to the counter and the counter continues to count down.

Mode 1 - Pulse Generation

The PAD0 (PBD0) direction register bit must be set to a 1 to establish PA0 (PB0) as an output pin before starting this mode. Writing to TAUL (TBUL) forces the PA0 (PB0) output low and starts the timer. Each time the timer counts through zero, the PA0 (PB0) output changes state to generate a square wave at a rate dependent upon the value loaded into the latches. The timer counts at either the $\phi 2$ or $\phi 2/32$ rate. Each time the counter counts through zero, the latch values are automatically transferred to the timer registers and the TAIF (TBIF) is set to a 1.

Mode 2 - Event Counter

The PAD0 (PBD0) direction register bit must be set to 0 to establish PA0 (PB0) as an input pin. The TAM2 (TBM2) clock divide-by-32 bit must be set to a 0 to select divide-by-1. The counter is initialized with the latch value when the TAUL (TBUL) value is written to address $0013 ($0017). The timer decrements by 1 at each positive transition on input port PA0 (PB0). TAIF (TBIF) is set to a 1 when the counter counts through zero. At the same time the latch value is reloaded into the counter. The maximum rate of the signal of PA0 (PB0) is one-half the timer clock rate.

Mode 3 - Pulse Width Measurement

The PAD0 (PAD0) direction register bit must be set to an 0 to establish PA0 (PB0) as an input pin. Writing to TAUL (TBUL) at $0013 ($0017) transfers the 16-bit latch value to the counter. The value in the timer is decremented at the $\phi 2$ or $\phi 2/32$ rate when the PA0 (PB0) signal is low. Each time the PA0 (PB0) signal goes high, the counter stops and then continues when the signal is low again. If the counter counts through zero, TAIF (TBIF) is set to a 1 and the latch value transfers to reinitialize the counter. The countdown continues as long as PA0 (PB0) is low.

PRECISION TIME GENERATORS

There are two identical 17-bit precision time generators in the C19: Precision Time Generator A (PTGA) and Precision Time Generator B (PTGB). Each PTG can be used for such functions as timing event interrupts, generating an external pulse train or as a source for synchronous USART timing.

Only PTGA is discussed since both precision timer generators are identical in structure. Only the differences in I/O port addresses and IRQ interfaces are described. Block diagrams of PTGA and PTGB are shown in Figures 3-12 and 3-13, respectively. The PTGA and PTGB mode registers are shown in Figure 3-14.

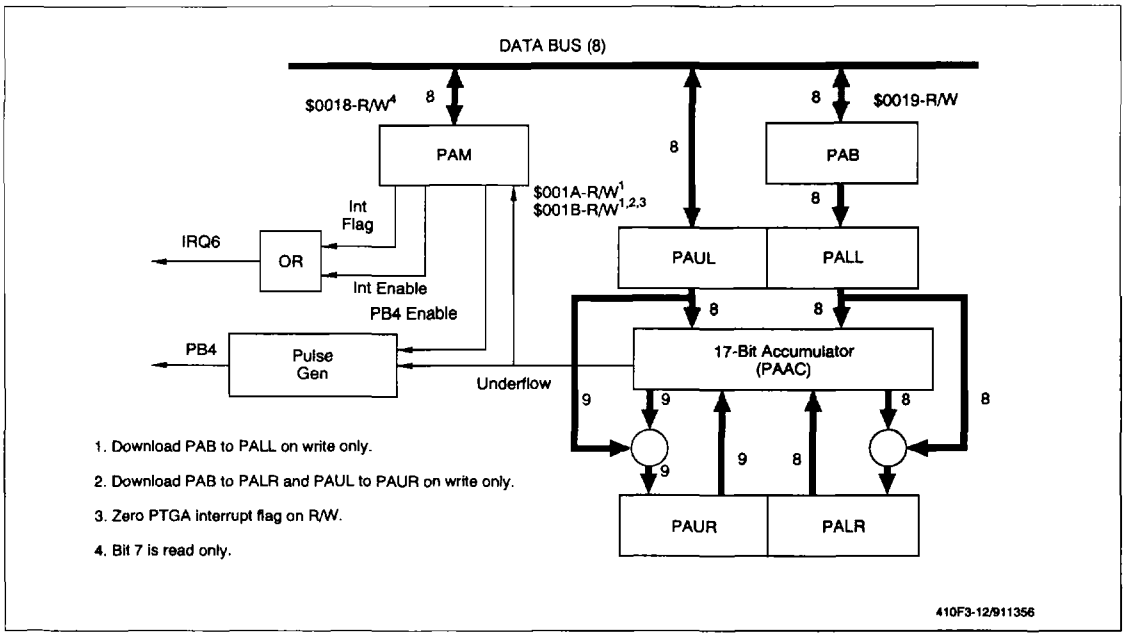


Figure 3-12. Precision Time Generator A

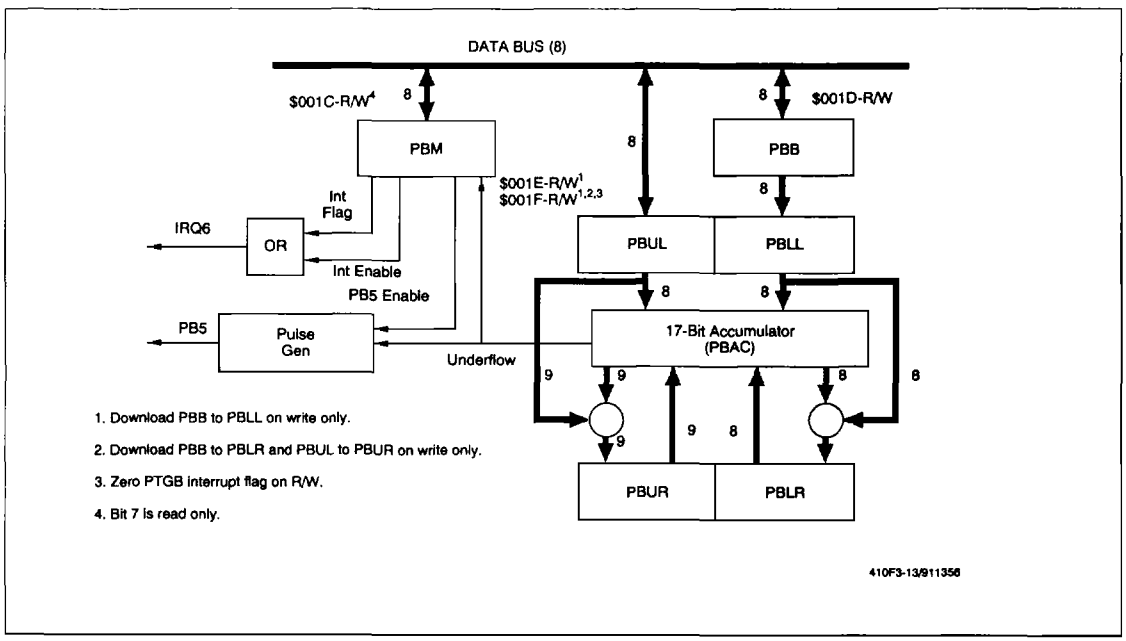


Figure 3-13. Precision Time Generator B

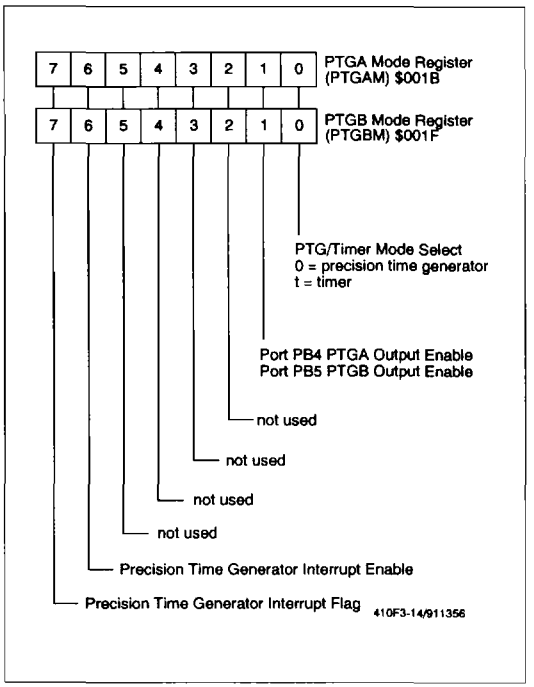


Figure 3-14. PTGA and PTGB Mode Registers

Precision Time Generator A

PTGA consists of five 8-bit registers and a 17-bit pulse accumulator located at addresses $0019-$001B (Figure 3-14). The three input registers—PTGA Buffer (PAB), PTGA Lower Latch (PALL) and PTGA Upper Latch (PAUL)—are all 8-bit. There are two output registers: an 8-bit PTGA Lower Residue (PALR) and a 9-bit PTGA Upper Residue (PAUR). The PTGA Accumulator (PAAC)is 17-bits long. Operation is controlled by the PTGA Mode Register (PAM) located at $0018.

Precision Time Generator B

PTGB consists of five 8-bit registers and a 17-bit pulse accumulator located at addresses $001D-$001F (Figure 3-14). The three input registers-PTGB Buffer (PBB), PTGB Lower Latch (PBLL) and PTGB Upper Latch (PBUL), PTGB Lower Residue (PBLR) and a 9-bit PTGB Upper Residue (PBUR). The PTGB Accumulator (PBAC) is 17-bits long. Operation is controlled by the PTGB Mode Register (PBM) located at $001F.

Operation of PTGB is identical to PTGA with the exception of register addresses, and the port B interface line.

Precision Time Generator Port Option and Timer Mode

Timer Mode

When PAM0 (PBM0) is set to a logic 1, PTGA (PTGB) operates in the timer mode. In this mode, each accumulator overflow causes PALL and PAUL (PBLL and PBUL) to down load to the PALR and PAUR (PBUR and PBUR). This removes the residue remaining in the accumulator at overflow thereby causing the overflow rate to occur at fixed intervals.

Port Output

When PAM1 (PBM1) is set to a logic 1, a PTGA (PTGB) pulse train is output on port PB4 (PB5). A positive pulse is generated each time the PTGA (PTGB) accumulator overflows. The width of the positive pulse is two $\phi 2$ periods.

UNIVERSAL SYNCHRONOUS/ ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

The R65C19 provides a full-duplex serial universal synchronous/asynchronous receiver/transmitter (USART) interface with programmable operating modes and data rates. A block diagram of the USART is shown in Figure 3-15. The supporting registers are shown in Figure 3-16 through 3-20.

General Operation

Internal timing for both asynchronous and synchronous operation can be referenced to either Timer B or the Precision Timing Generators under software control. Synchronous serial input (SIN) timing can also be derived externally by an external serial input clock (SICLK) on PA3 or an external TXCLK on PA4. Synchronous serial output (SOUT) timing can be generated from an external SOCLK on PA7. Note that the direction registers for PA1 through PA7 (PAD1 - PAD7) must be set correctly for the mode selected. Table 3-16 shows how standard data rates can be generated internally using either Timer B or the Precision Timing Generators A and B.

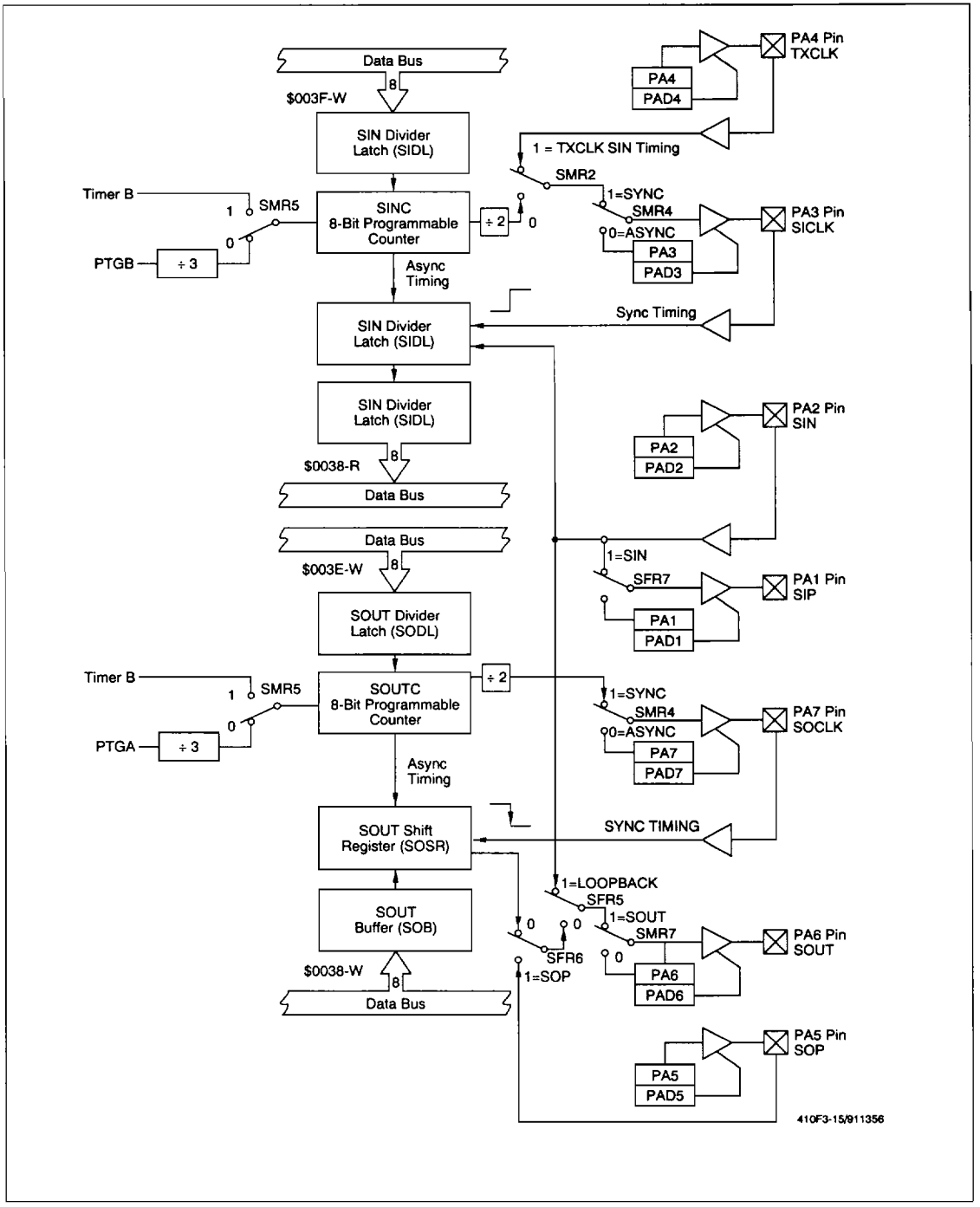


Figure 3-15. USART Block Diagram

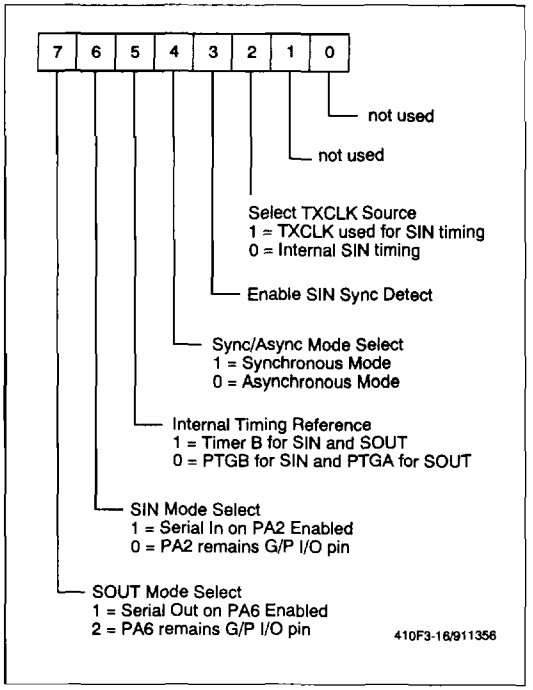


Figure 3-16. Serial Mode Register (SMR) - $003A

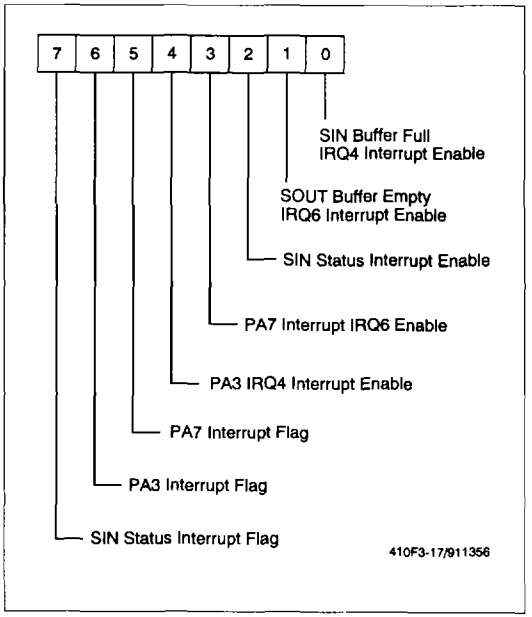


Figure 3-17. Serial Interrupt Register (SIR) - $0039

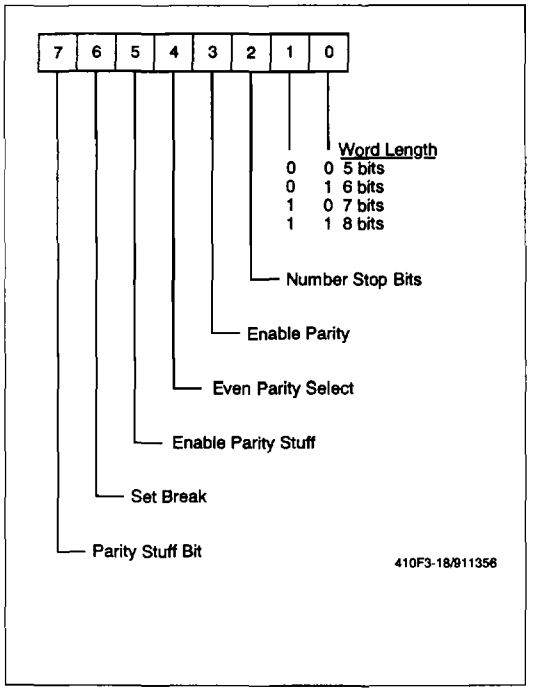


Figure 3-18. Serial Line Register (SLR) - $003B

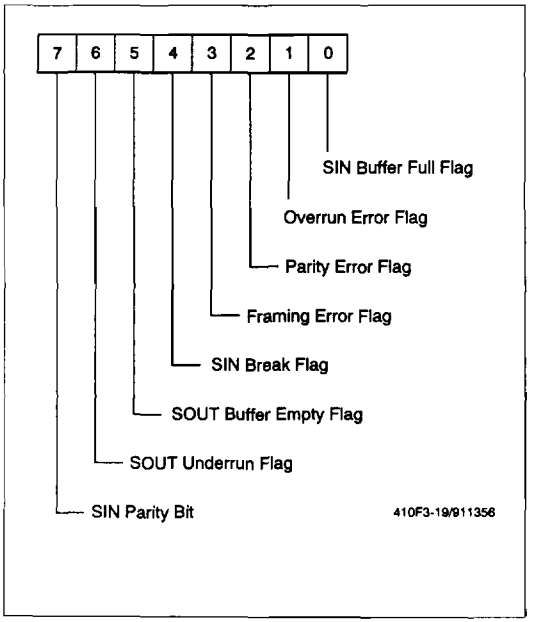


Figure 3-19. Serial Status Register (SSR) - $003C

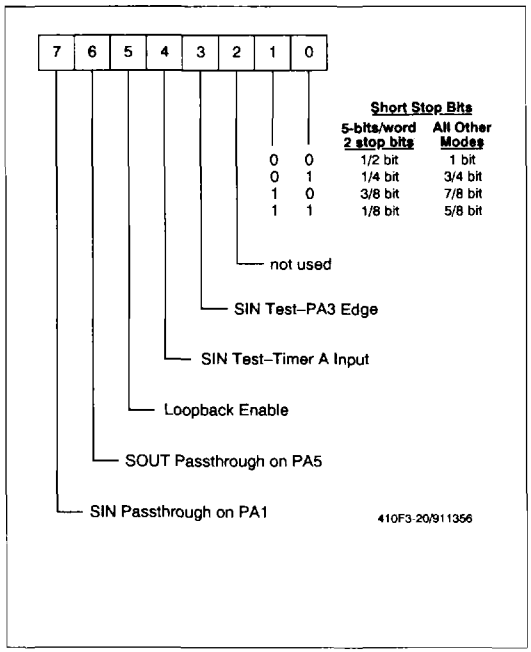


Figure 3-20. Serial Form Register (SFR) - $003D

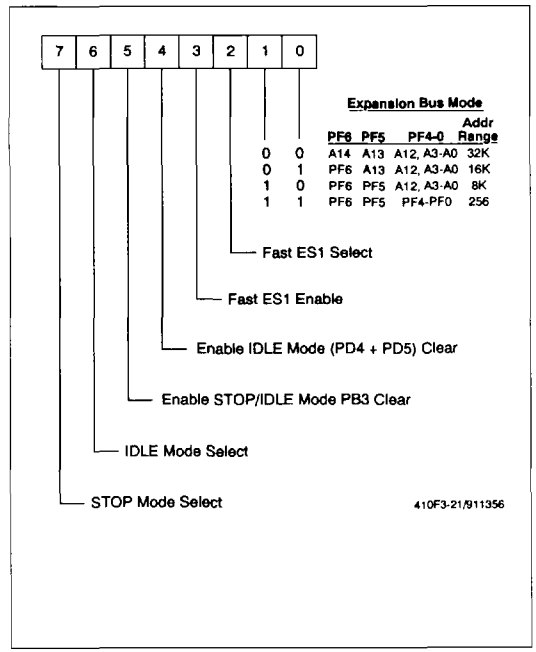


Figure 3-21. Bus Control Register (BCR) - $0009

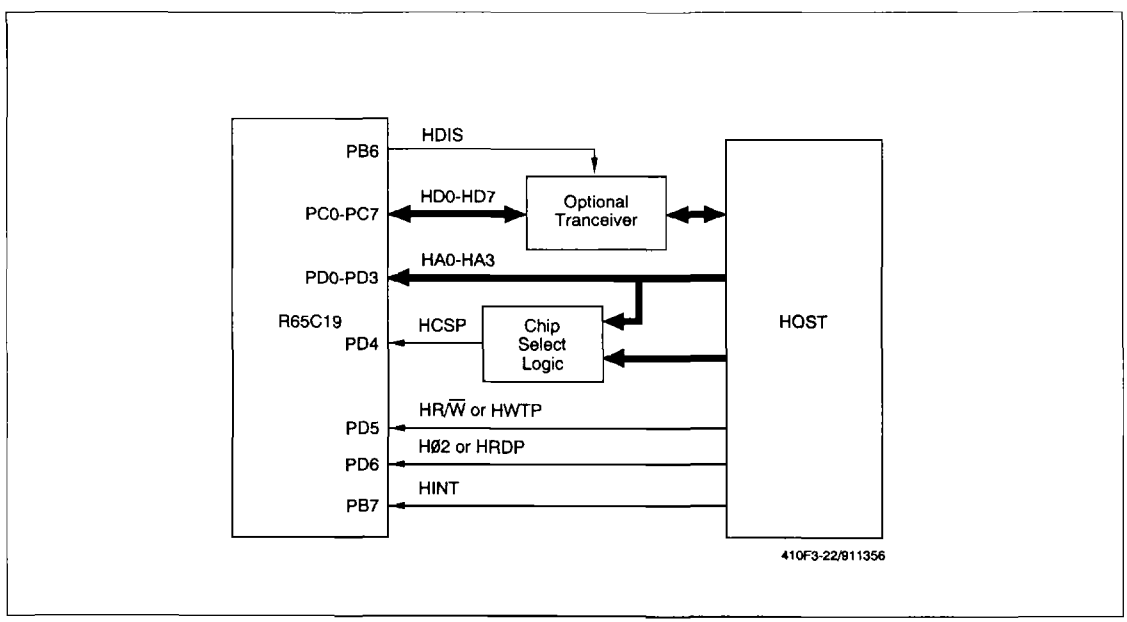


Figure 3-22. Host Bus Interface

The serial interface registers are located at addresses $0034-$003F. The CPU may read or write any of the serial interface registers with the exception of Serial Out Divider Latch (SODL) and Serial In Divider Latch (SIDL) which are write only. The serial Status Register is read-only. Reading and/or writing to some of the registers also causes clearing of interrupt bits or data downloading actions.

EXPANSION BUS

The Bus Control Register is shown in Figure 3-21. The expansion bus extends internal address, data and control bus lines outside the R65C19. This allows the R65C19 to operate as a microprocessor by interfacing with external memory and/or other peripheral devices.

Dedicated expansion bus lines (D0/A4-D7/A11) provide a multiplexed 8-bit address (A4-A11) with the 8-bit data bus (D0-D7). These lines are always active and reflect the data and address on the internal data and address lines.

The expansion bus lines (D0/A4-D7/A11), Port F lines (A0-A3, A12-A15) and the ES lines (ES1-ES4) tri-state (float) when the reset pin is active low. The $\overline{RD}$ and $\overline{WT}$ output signals are maintained in a logic 1 state when the reset pin is active low.

Read ($\overline{RD}$), Write ($\overline{WT}$), and Address Latch Enable (ALE) outputs are active at all times. ALE is strobed low when the address is valid on the multiplexed D0/A4-D7/A11 lines. Since the expansion bus is multiplexed, external latches must be supplied to latch the address when ALE goes low. The user should note the behavior of these signals during extended memory cycles.

Address Extension

Seven additional address lines can be output on port F lines under control of BCR bits 0 and 1 to provide a finer resolution of addresses (A0-A3) and a larger address range (A12-A14). These address lines have the same timing as A0-A11.

External Select Outputs

The External Select outputs (ES1-ES4) are active low chip select signals on PE0-PE3 output lines that are enabled by a user selected mask option. The ES1-ES4 outputs reflect the address range of the address lines. The size of ES1, ES2, and ES3 can be changed by an ES1 mask option (Figure 3-2).

ES1, ES2, and ES3 can independently be set under software control to operate in either normal (full speed) or extended (half speed) memory cycles. ES1 is controlled by BCR3, ES2 by BCR2, and ES3 by CIR2. Extended half speed cycles are selected by a logic 0, normal cycles by a logic 1. Reset forces extended (half speed) memory operation. The top half (1K) of ES4 operates at the speed selected for ES3. The bottom half (1K) always operates at full speed.

HOST BUS INTERFACE AND DUAL PORT RAM - GP INTERFACE

The host bus interface software option (HCR2 = 1) provides a $\overline{RD}/\overline{WT}$ bus compatible interface between the R65C19 and a host microprocessor (Figure 3-22). This interface allows the R65C19 to act like a standard peripheral device connected to the host bus under control of the host processor. Under R65C19 software control, this interface can be a general purpose user defined interface or a user implemented emulation of the 16450 UART. The Host Handshake and Host Control registers are shown in Figures 3-23 and 3-24, respectively.

Built-in hardware registers and control signals allow a 16450 UART compatible interface to be presented to the host bus.

Host Bus Interface Signals and Registers

When the host bus interface software option is selected, the following host bus signals are supported instead of the general purpose I/O lines on ports C (8 lines), D (7 lines) and B (2 lines):

- 8-bit bidirectional data bus (HD0-HD7)
- 4-bit address bus (HA0-HA3), HA3 remains a GP I/O in the 16450 mode.
- 1 chip select (HCSP)
- 2 bus timing signals (HWTP and HRDP)
- 1 host interrupt line (HINT)
- 1 driver disable line (HDIS)

The host bus waveforms are illustrated in Appendix D. The host bus interrupt timing waveforms for the general purpose RAM mode and the 16450 emulation mode are also shown in Appendix D.

General Purpose Host Bus Register and Dual Port RAM

If the general purpose interface mode is selected (HCR1 = 0 and HCR2 = 1), the 16 dual port RAM locations are accessable to both the R65C19 CPU and the external host bus. 15 RAM locations ($0020-$002E) are available for application definition and one RAM location is the Host Handshake Register ($002F). All bits of the Host Control Register are initialized to zero at reset.

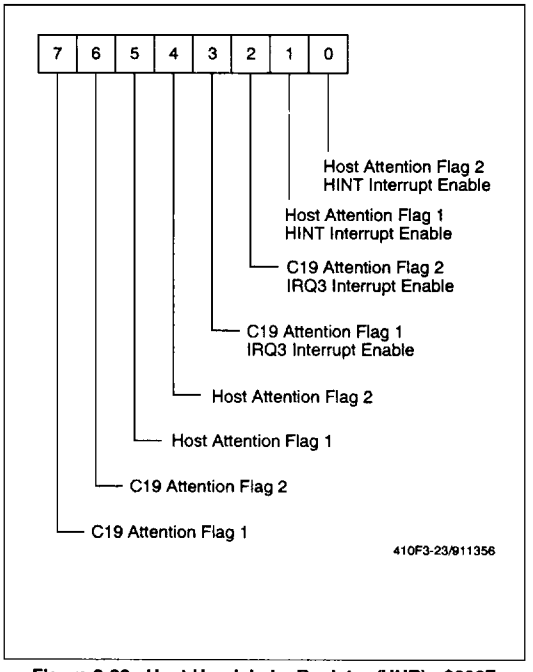


Figure 3-23. Host Handshake Register (HHR) - $002F

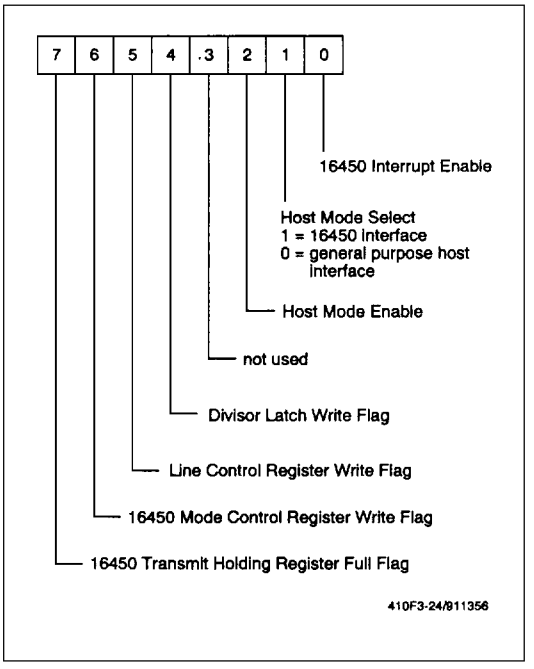


Figure 3-24. Host Control Register (HCR) - $0032

HOST BUS INTERFACE AND DUAL PORT RAM - 16450 MODE

When the 16450 mode is selected (HCR1 = 1 and HCR2 = 1), the Host Bus Interface can be made to emulate the 16450 UART device. This is done through a combination of built-in hardware features and user-supplied software.

Emulation of the 16450 is equivalent when 16450 input signals $\overline{CS0}$ and CS1 are tied high and DISTR, D0STR and $\overline{ADS}$ are tied low. Table 3-1 shows the equivalence between R65C19 and 16450 signals. All 16450 signals not included in Table 3-1 are not required for R65C19 16450 operation.

The R65C19 16450 register set and associated addresses are shown in Table 3-2. The supporting registers are shown in Figures 3-25 through 3-28.

The Line Status Register (LSR), Modem Status Register (MSR), Interrupt Enable Register (IER) and Interrupt Identification Register (IDR) are implemented with dedicated hardware. The remaining 16450 registers are mapped directly into dual port RAM locations. Additionally, the Host Control Register provides the means to allow the R65C19 to control and monitor the 16450 interface.

MASK OPTION REGISTER (MOR)

The Mask Option Register (MOR) at location $0008 reports the selected mask options (Figure 3-29).

Bit 7: Not Used. Reads as a logic 0.

Bit 6: Not Used. Reads as a logic 0.

Bit 5: A15 Line Selected. This bit is a logic 1 when the A15 line option is masked. This bit is a logic 0 when the A15 line option is not masked (PF7 is a general purpose I/O line).

Bit 4: ES Enabled. This bit is a logic 1 when PE0-PE3 are used for ES1-ES4. This bit is a logic 0 when PE0-PE3 are GP outputs.

Bit 3: ES1 Size = 24K. This bit is a logic 1 when the size of ES1 is selected for 24K bytes. This bit is a logic 0 when the size of ES1 is selected for 32K bytes.

Bit 2: Not Used. Reads as a logic 0.

Bit 1: Clock Divide-By-1. This bit is a logic 1 when the clock divide-by-1 option is masked. This bit is a logic 0 when the clock divide-by-2 option is masked.

Bit 0: Not Used. Reads as a logic 0.

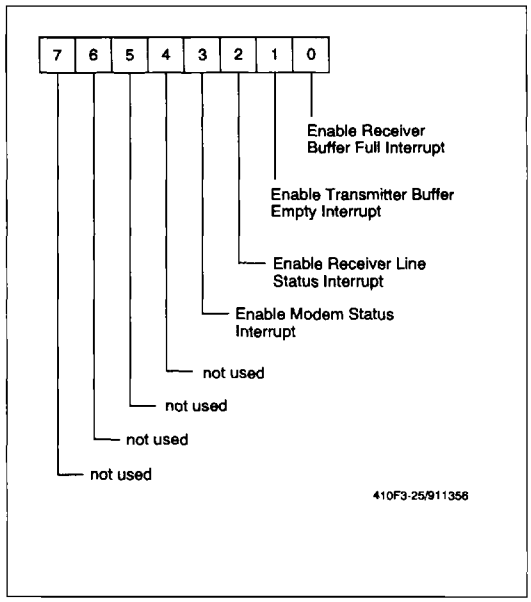


Figure 3-25. Interrupt Enable Register (IER)

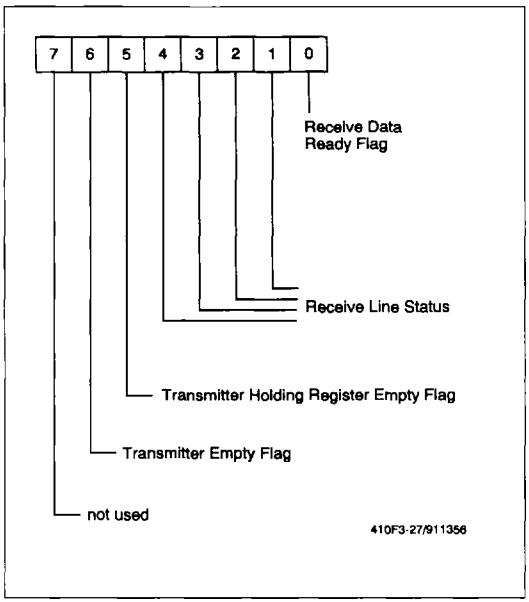


Figure 3-27. Line Status Register (LSR) - $0030

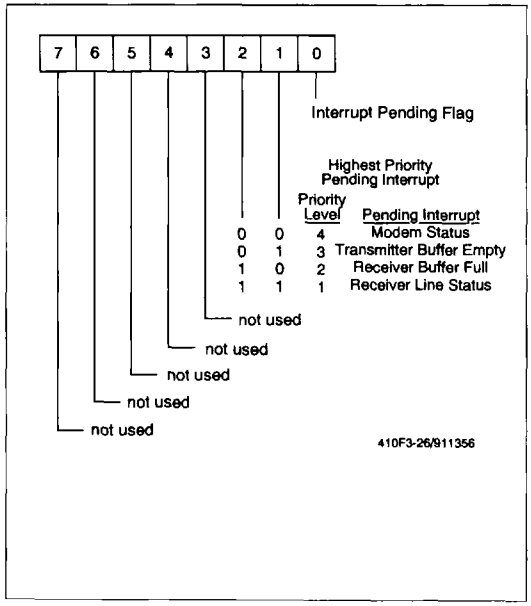


Figure 3-26. Interrupt Identifier Register (SLR)

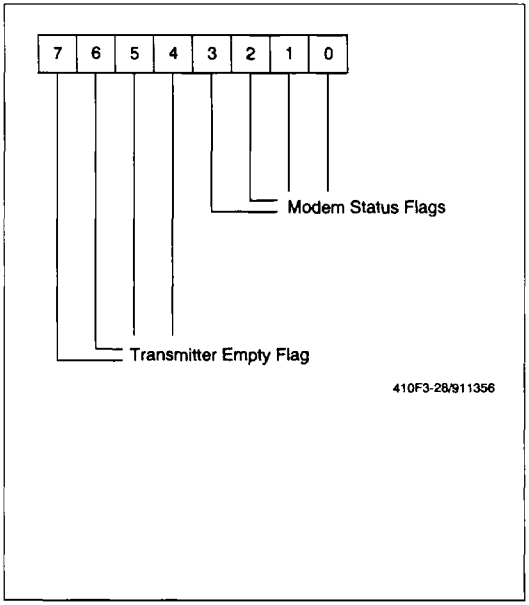


Figure 3-28. Modem Status Register (MSR) - $0031

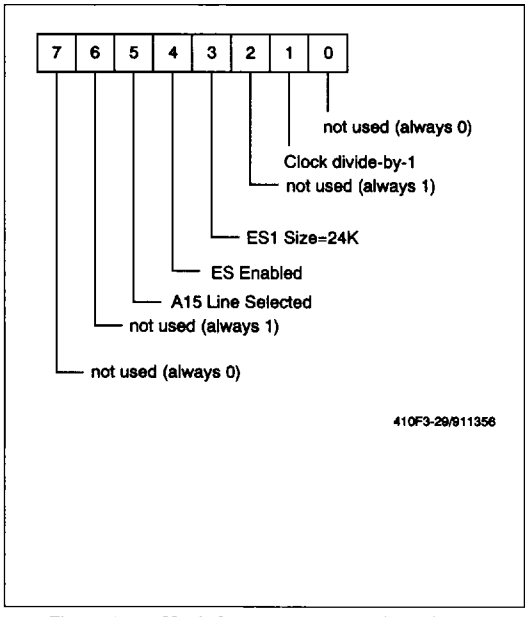


Figure 3-29. Mask Option Register (MOR) - $0008

Table 3-1. R65C19/16450 Signal Equivalence

R65C19 Pin Assignment Label	Signal Names	
	R65C19	16450
PB6	HDIS	DDIS
PB7	HINT	INTRPT
PC0-PC7	HD0-HD7	D0-D7
PD0-PD2	HA0-HA2	A0-A2
PD4	$\overline{\text{HCS}}$	$\overline{\text{CS2}}$
PD5	$\overline{\text{HWT}}$	$\overline{\text{DISTR}}$
PD6	$\overline{\text{HRD}}$	$\overline{\text{DOSTR}}$
$\overline{\text{RES}}$	$\overline{\text{RESET}}$ (Active low)	MR
–	Implemented in software	OUT 1
–	Implemented in software	OUT 2

Table 3-2. Memory Map - $0020-$0032 - 16450 Emulation Mode

R65C19 Address	Internal Access (HCR1 = 1)				Host Access (HCR1 = 1)	
	Read	Write	DLAB	ADDR	Read	Write
0020	Receiver Buffer	Receiver Buffer[1]	0	0	Receiver Buffer	–[4]
0021	Transmitter Buffer[2]	*	0	0	–[4]	Transmitter Buffer
—	–[4]	–[4]	0	1	Interrupt Enable	Interrupt Enable
—	–[4]	–[4]	X	2	Interrupt Ident	–[4]
0022	SP RAM[2]	SP RAM[2]	—	—	–[4]	–[4]
0023	Line Control[2]	*	X	3	Line Control	Line Control
0024	Modem Control[2]	*	X	4	Modem Control	Modem Control
0025	SP RAM 5	SP RAM 5	—	—	–[4]	–[4]
0026	SP RAM 6	SP RAM 6	—	—	–[4]	–[4]
0027	SP RAM 7[2]	*	X	7	SP RAM 7	SP RAM 7
0028	Divide-LSB[2]	*	1	0	Divide-LSB	Divide-LSB
0029	Divide-MSB[2]	*	1	1	Divide-MSB	Divide-MSB
002A	SP RAM A	SP RAM A	—	—	–[4]	–[4]
002B	SP RAM B	SP RAM B	—	—	–[4]	–[4]
002C	SP RAM C	SP RAM C	—	—	–[4]	–[4]
002D	SP RAM D	SP RAM D	—	—	–[4]	–[4]
002E	SP RAM E	SP RAM E	—	—	–[4]	–[4]
002F	Handshake	Handshake	—	—	–[4]	–[4]
0030	Line Status	Line Status	X	5	Line Status[3]	Line Status[4]
0031	Modem Status	Modem Status	X	6	Modem Status[3]	Modem Status[4]
0032	Host Control Register	Host Control Register	—	—	–[4]	–[4]

LEGEND: — = No assigned function.
* = Do not write to this location

NOTES:
1. LSR0 = 0. Write handshake required to guarantee valid Host read data.
2. Read until data repeats.
3. During simultaneous R65C19 write the Host will read old value.
4. During simultaneous R65C19 write/Host read, or Host write/R65C19 read, the read operation will not interfere

TEST MODE

The Test mode is selected by applying a low voltage to the $\overline{TST}$ pin.

In the Test mode, the internal ROM is deactivated and the expansion bus activated when ROM addresses are selected. The Port F lines PF0-PF6 are automatically dedicated to expansion address lines A0-A3 and A12-A14, respectively.

Reads from addresses $000C-$000F are mapped to the expansion port for growth application.

Internal reads from Page 0, 1 and 2 are mapped externally on the expansion bus whenever the $\overline{TST}$ pin is active. This provides for monitoring of internal reads operations.

POWER ON/INITIALIZATION

Power On Timing

After application of VCC power to the device, $\overline{RES}$ must be held low for at least two $\phi 2$ clock cycles after VCC reaches operating range. Figure 3-30 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

Power On Reset

When $\overline{RES}$ goes from low to high, the device sets the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiates a reset vector fetch at address $FFFE and $FFFF to begin user program execution.

Reset ($\overline{RES}$) Conditioning

When $\overline{RES}$ is driven from low to high, the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 3-3.

All RAM and other CPU registers will initialized in a random, non-repeatable, data pattern upon power on.

Initialization

Any initialization process for the device should include a reset, as indicated in the preceding paragraphs. After stabilization of the internal clock (if a power on situation), an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required

A typical initialization subroutine could be as follows:

```
LDX   Load stack pointer starting address into
      X Register
TXS   Transfer X Register value to Stack Pointer
SEC   Set Carry Flag
...   Set-up Mode Control and special function
....  register and clear RAM as required
```

Table 3-3. Reset Initialization of Registers

Register	Bit 7	6	5	4	3	2	1	0
Processor Status	–	–	–	–	0	1	–	–
Stack Pointer	–	–	–	–	–	–	–	–
Port A, B, C Direction	0	0	0	0	0	0	0	0
Port D Direction	0	0	0	0	–	–	–	–
Port E	0	0	0	0	0	0	0	0
Port F (address extension)	–	–	–	–	–	–	–	–
Bus Control	0	0	0	0	0	0	0	0
External Interrupt	0	0	0	0	0	0	0	0
Clear Interrupt	–	–	–	–	–	0	0	0
Timer A, B Mode	–	0	0	–	–	0	0	0
PTG A, B Mode	–	0	–	–	–	–	0	0
Host Control	0	0	0	0	0	0	0	0
Serial Interrupt Enable	0	0	0	0	0	0	0	0
Serial Mode	0	0	0	0	0	0	0	0
Serial Line	0	0	0	0	0	0	0	0
Serial Status	0	0	0	0	0	0	0	0
Serial Form	–	–	–	–	–	–	–	–
Serial Out Divider Latch	–	–	–	–	–	–	–	–
Serial In Divider Latch	–	–	–	–	–	–	–	–

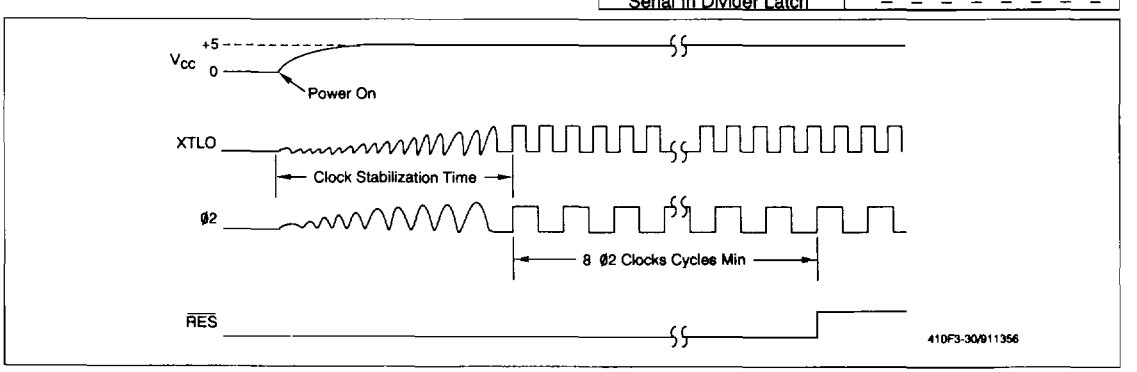


Figure 3-30. Power Turn On Timing Detail

APPENDIX A
INSTRUCTION SET SUMMARY

This appendix summarizes the R65C19 instruction set.

Table A-1 is a matrix of instructions and addressing modes arranged by operation code. R65C19 instruction addressing modes and execution times are defined in the R65C19 Technical Reference Manual (Order No. 400). For basic information about R6502 CPU instruction operation, consult the R6500 Programming Manual (Order No. 202).

Table A-2 lists the instruction mnemonics and titles by mnemonic code in Table A-1.

Table A-3 summarizes the operation of the new instructions incorporated in the R65C19 as referenced to the R6502 CPU.

Table A-4 summarizes the differences in operation between the R65C19 CPU and the R6502 CPU.

Table A-5 summarizes the R65C19 threaded code instructions.

Table A-1. R65C19 Instruction Set Operation Code Matrix

MSD	LSD 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND) 2 5	MPY Implied 1 6	TIP Implied 1 2		ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2	JSB0 (FFE0) 1 6	JPI Implied 3 5	ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5[b]	0
1	BPL Relative 2 2[b]	ORA (IND), X 2 5[a]	MPA Implied 1 6	LAB Accum 1 3		ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4[a]	NEG Accum 1 2	JSB1 (FFE2) 1 6		ORA ABS, X 3 4[a]	ASL ABS, X 3 7	BBR1 ZP 3 5[b]	1
2	JSR Absolute 3 5	AND (IND) 2 5	PSH Implied 1 5	PHW Implied 1 4	BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2	JSB2 (FFE4) 1 6	BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5[b]	2
3	BMI Relative 2 2[b]	AND (IND), X 2 5[a]	PUL Implied 1 6	PLW Implied 1 5		AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4[a]	ASR Accum 1 2	JSB3 (FFE6) 1 6		AND ABS, X 3 4[a]	ROL ABS, X 3 7	BBR3 ZP 3 5[b]	3
4	RTI Implied 1 6	EOR (IND) 2 5	RND Implied 1 2			EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2	JSB4 (FFE8) 1 6	JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5[b]	4
5	BVC Relative 2 2[b]	EOR (IND), X 2 5[a]	CLW Implied 1 2			EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4[a]	PHY Implied 1 3	JSB5 (FFEA) 1 6		EOR ABS, X 3 4[a]	LSR ABS, X 3 7	BBR5 ZP 3 5[b]	5
6	RTS Implied 1 5	ADC (IND) 2 5[c]	TAW Implied 1 2		ADD ZP 2 3[c]	ADC ZP 2 3[c]	ROR ZP 2 5	RMB6 ZP 2 6	PLA Implied 1 4	ADC IMM 2 2[c]	ROR Accum 1 2	JSB6 (FFEC) 1 6	JMP (ABS) 3 5	ADC ABS 3 4[c]	ROR ABS 3 6	BBR6 ZP 3 5[b]	6
7	BVS Relative 2 2[b]	ADC (IND), X 2 5[a,c]	TWA Implied 1 2		ADD ZP, X 2 4[c]	ADC ZP, X 2 4[c]	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4[a,c]	PLY Implied 1 4	JSB7 (FFEE) 1 6	JMP (ABS, X) 3 6	ADC ABS, X 3 4[a,c]	ROR ABS, X 3 7	BBR7 ZP 3 5[b]	7
8	BRA Relative 2 3[a]	STA (IND) 2 5			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2	ADD IMM 2 2[c]	TXA Implied 1 2	NXT Implied 1 4	STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5[b]	8
9	BCC Relative 2 2[b]	STA (IND), X 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2	LII Implied 1 5		STA ABS, X 3 5		BBS1 ZP 3 5[b]	9
A	LDY IMM 2 2	LDA (IND) 2 5	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2	LAN Implied 1 3	LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5[b]	A
B	BCS Relative 2 2[b]	LDA (IND), X 2 5[a]	STI ZP 3 4		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SBM3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4[a]	TSX Implied 1 2	INI Implied 1 3	LDY ABS, X 3 4[a]	LDA ABS, X 3 4[a]	LDX ABS, Y 3 4[a]	BBS3 ZP 3 5[b]	B
C	CPY IMM 2 2	CMP (IND) 2 5	RBA ABS 4 7		CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2	PHI Implied 1 4	CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5[b]	C
D	BNE Relative 2 2[b]	CMP (IND), X 2 5[a]	SBA ABS 4 7		EXC ZP, X 2 5	CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4[a]	PHX Implied 1 3	PLI Implied 1 6		CMP ABS, X 3 4[a]	DEC ABS, X 3 7	BBS5 ZP 3 5[b]	D
E	CPX IMM 2 2	SBC (IND) 2 5[c]	BAR ABS 5 7[b]		CPX ZP 2 3	SBC ZP 2 3[c]	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2[c]	NOP Implied 1 2	LAI Implied 1 3	CPX ABS 3 4	SBC ABS 3 4[c]	INC ABS 3 6	BBS6 ZP 3 5[b]	E
F	BEQ Relative 2 2[b]	SBC (IND), X 2 5[a,c]	BAS ABS 5 7[b]			SBC ZP, X 2 4[c]	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4[a,c]	PLX Implied 1 4	PIA Implied 1 6		SBC ABS, X 3 4[a,c]	INC ABS, X 3 7	BBS7 ZP 3 5[b]	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

LSD

0

0 | BRK / Implied / 1 7 — OP Code / Addressing Mode / No. of Instruction Bytes; No. of Machine Cycles

[a]Add 1 to N if page boundary is crossed.

[b]Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

[c]Add 1 to N if in decimal mode.

Table A-2. R65C19 Instruction Set by Mnemonic

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	MPA*	Multiply and Accumulate
ADD*	Add Memory to Accumulator without Carry	MPY*	Multiply
AND	"AND" Memory with Accumulator		
ASL	Shift Left One Bit (Memory or Accumulator)	NEG*	Negate Accumulator
ASR*	Accumulator Shift Right One Bit, Sign Extend	NOP	No Operation
		NXT*	Next Instruction
BAR*	Branch On Bit(s) Reset		
BAS*	Branch On Bit(s) Set	ORA	"OR" Memory with Accumulator
BBR*	Branch On Bit Reset (8)		
BBS*	Branch On Bit Set (8)	PHA	Push Accumulator on Stack
BCC	Branch on Carry Clear	PHI*	Push I on Stack
BCS	Branch on Carry Set	PHP	Push Processor Status on Stack
BEQ	Branch on Equal	PHW*	Push W on Stack
BIT	Test Bits in Memory with Accumulator	PHX*	Push Index X on Stack
BMI	Branch on Minus	PHY*	Push Index Y on Stack
BNE	Branch on Not Zero	PIA*	Pull I from Stack, Load Accumulator
BPL	Branch on Plus	PLA	Pull Accumulator from Stack
BRA*	Branch Always	PLI*	Pull I from Stack
BRK	Break Command	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear	PLW	Pull W from Stack
BVS	Branch on Overflow Set	PLX*	Pull Index X from Stack
		PLY*	Pull Index Y from Stack
CLC	Clear Carry Flag	PSH*	Push A, X and Y on Stack
CLD	Clear Decimal Mode	PUL*	Pull Y, X and A from Stack
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	RBA*	Reset Bit(s) in Memory
CLW*	Clear W Register and Overflow Flag	RMB*	Reset Memory Bit (8)
CMP	Compare Memory and Accumulator	RND*	Round
CPX	Compare Memory and Index X	ROL	Rotate Left One Bit (Memory or Accumulator)
CPY	Compare Memory and Index Y	ROR	Rotate Right One Bit (Memory or Accumulator)
		RTI	Return from Interrupt
DEC	Decrement Memory by One	RTS	Return from Subroutine
DEX	Decrement Index X by One		
DEY	Decrement Index Y by One	SBA*	Set Bit(s) in Memory
		SBC	Subtract Memory from Accumulator with Borrow
EOR	"Exclusive-Or" Memory with Accumulator	SEC	Set Carry Flag
EXC*	Exchange Accumulator and Memory	SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
INC	Increment Memory by One	SMB*	Set Memory Bit (8)
INI*	Increment I by One	STA	Store Accumulator in Memory
INX	Increment Index X by One	STI*	Store Immediate to Memory
INY	Increment Index Y by One	STX	Store Index X in Memory
		STY	Store Index Y in Memory
JMP*	Jump to New Location		
JPI*	Jump Indirect with Return in I	TAW*	Transfer Accumulator to W
JSB*	Jump to Subroutine (8)	TAX	Transfer Accumulator to Index X
JSR	Jump to New Location Saving Return Address	TAY	Transfer Accumulator to Index Y
		TIP*	Transfer I to Program Counter
LAB*	Load Absolute to Accumulator	TSX	Transfer Stack Pointer to Index X
LAI*	Load Accumulator Indirect through I	TWA*	Transfer W to Accumulator
LAN*	Load Accumulator Indirect and Increment I	TXA	Transfer Index X to Accumulator
LDA	Load Accumulator with Memory	TXS	Transfer Index X to Stack Pointer
LDX	Load Index X with Memory	TYA	Transfer Index Y to Accumulator
LDY	Load Index Y with Memory		
LII*	Load I Indirect through I		
LSR	Logical Shift Right One Bit (Memory or Accumulator)		

* = New instruction or addressing mode

Table A-3. R65C19 New Instructions From R6502

Nine Basic Instructions

Mnemonic	Operation	Addressing Modes	No. Bytes	No. Cycles
SMB	Set Memory Bit (8)	ZP	2	5
RMB	Clear Memory Bit (8)	ZP	2	5
BBS	Branch On Bit Set (8)	ZP	3	5, 6, 7
BBR	Branch On Bit Clear (8)	ZP	3	5, 6, 7
BRA	Branch Always	Rel	2	2, 3, 4
PHX	Push X	Implied	1	3
PHY	Push Y	Implied	1	3
PLX	Pull X	Implied	1	4
PLY	Pull Y	Implied	1	4

Fifteen Filter Enhancement Instructions

Mnemonic	Operation	Addressing Modes	No. Bytes	No. Cycles
ASR	Shift A Right, Sign Extend	Accum	1	2
CLW	Clear W, V	Implied	1	2
EXC	Swap A, M	ZP, X	2	5
JSB	Jump to Subroutine (8)	(FFE_)	1	6
LAB	$\|A\| \rightarrow A$	Accum	1	2
MPA	$(A \times Y) + W \rightarrow W$; signed	Implied	1	6
MPY	$(A \times Y) \rightarrow A, Y$; signed	Implied	1	6
PSH	Push A, X, Y	Implied	1	5
PUL	Pull Y, X, A	Implied	1	6
RND	Round W, $W_H \rightarrow A$	Implied	1	2
TAW	$A \rightarrow W_H$, $0 \rightarrow W_L$	Implied	1	2
TWA	$W_H \rightarrow A$	Implied	1	2
NEG	2s complement A	Accum	1	2
PHW	Push W_H, W_L	Implied	1	4
PLW	Pull W_L, W_H	Implied	1	5

Ten Direct Threaded Code Instructions

Mnemonic	Operation	Addressing Modes	No. Bytes	No. Cycles
NXT	$(I) \rightarrow PC, I + 2 \rightarrow I$	Implied	1	4
LII	$(I) \rightarrow I$	Implied	1	5
LAI	$(I) \rightarrow A$	Implied	1	3
INI	$I + 1 \rightarrow I$	Implied	1	3
PHI	Push I	Implied	1	4
PLI	Pull I	Implied	1	6
JPI	$PC + 1 \rightarrow I, (I) \rightarrow PC, I + 2 \rightarrow I$	Implied	3	5
TIP	$I \rightarrow PC$	Implied	1	2
PIA	Pull I, $(I) \rightarrow A, I + 1 \rightarrow I$	Implied	1	6
LAN	$(I) \rightarrow A, I + 1 \rightarrow I$	Implied	1	3

Seven Controller Instructions

Mnemonic	Operation	Addressing Modes	No. Bytes	No. Cycles
BAR	Branch On Bit(s) Clear	ABS	5	7, 8, 9
BAS	Branch On Bit(s) Set	ABS	5	7, 8, 9
JMP	Jump	(ABS, X)	3	6
STI	Move IMM to Memory	ZP	3	4
RBA	Reset Bit(s) in Memory	ABS	4	7
SBA	Set Bit(s) in Memory	ABS	4	7
ADD	Add without Carry	IMM	2	2
ADD	Add without Carry	ZP	2	3
ADD	Add without Carry	ZP, X	2	4

Table A-4. R65C19 CPU Instruction Enhancements

Function	NMOS R6502 Microprocessor	CMOS R65C19 Microprocessor
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments.
Read/modify/write instructions at effective address.	One read cycle and two write cycles.	Two read cycle's and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D = 0) after reset.
Decimal ADD/SUB execution time.	Same execution time as binary.	One additional cycle for decimal correct.
Flags after decimal ADD/SUB.	N, V and Z flags are invalid.	N, V and Z flags are valid.
Interrupt coincident with BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	Interrupt is executed, then BRK is executed.
JSR instruction.	Stacked address points to last byte of JSR instruction.	Stacked address points to next op code.. Instruction is one cycle shorter.
RTS instruction.	Return address is incremented before use.	Return address is ready for use. Instruction is one cycle shorter.
Indirect Addressing Opcodes changed.	(INDIRECT, X)	(INDIRECT)
Indirect Addressing Opcodes changed.	(INDIRECT), Y	(INDIRECT), X

Table A-5. R65C19 Threaded Code Instructions

Mnemonic	Instruction	Operation	Description
NXT	Next Instruction	(I) → PC I+2 → I	The I register points to an address. The two bytes at that address are loaded into the Program Counter. The contents of the I register are incremented by 2.
LII	Load I Indirect through I	(I) → I	The I register points to an address. The two bytes at that address are loaded into the I register.
LAI	Load A Indirect through I	(I) → A	The I register points to an address. The byte at that address is loaded into the Accumulator.
INI	Increment I by One	I+1 → I	The I register is incremented by 1.
PHI	Push I on Stack	I → (stack) SP–2 → SP	The contents of the I register are pushed onto the stack, high byte first.
PLI	Pull I from Stack	(stack) → I SP+2 → SP	The two bytes pointed to by the Stack Pointer are loaded into the I register, low byte first.
JPI (Operand)	Jump Indirect with Return in I	PC+1 → I (I) → PC I+2 → I	The contents of the Program Counter (the address of the JPI instruction) +1 are loaded into the I register. I now points to the two byte operand of the JPI instruction. This operand is used as an indirect pointer to the next execution address. I is incremented by 2 to point to the next opcode following the JPI instruction. This instruction functions as a JSR indirect with the return address in the I register.
TIP	Transfer I to Program Counter	I → PC	Transfer the contents of the I register to the Program Counter. This instruction functions as an RTS to the JPI instruction.
PIA	Pull I from Stack, Load A	(stack) → I SP+2 → SP (I) → A I+1 → I	Load the I register with the two bytes pointed to by the Stack Pointer, low byte first. Increment the Stack Pointer by 2. Load the byte pointed to by the I register into the Accumulator. Increment the I register by 1.
LAN	Load A Indirect and Increment I	(I) → A I+1 → I	Load the byte pointed to by the I register into the Accumulator. Increment the I register by 1.

APPENDIX B
OPTIONS

SELECTABLE MASK OPTIONS

The following mask options are selectable upon production part order:

1. Address line A15 or general purpose I/O on PF7.
2. Port E selected for ES signals or general purpose outputs.
3. Changes ES1 address range from 32K to 24K.
4. Divide-by-1 or divide-by-2 system clock.

ROMLESS MICROCONTROLLERS STRAP OPTIONS

C1999J

- Port F pin 7 selected for A15.
- ES1 external size selected for 32K.
- Port E selected for general purpose outputs.
- Clock divide by 2 selected.

C1997J

- Port F pin 7 selected for A15.
- ES1 external size selected for 24K.
- Port E selected for ES1 through ES4 outputs.
- Clock divide by 2 selected.

APPENDIX C
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	V_{DC}
Input Voltage	V_{IN}	–0.3 to V_{CC} +0.3	V_{DC}
Operating Temperature	T_A	0 to 70	°C
Storage Temperature Range	T_{STG}	– 55 to +150	°C

DC CHARACTERISTICS
(VCC = 5V ±5%, TV>A = 0°C to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Reset, NMI					
Input High Voltage	V_{IH}	2.4		V_{CC}	V
Input Low Voltage	V_{IL}	–0.3		+0.8	V
$\overline{TST}$					
Input High Voltage	V_{IH}	4.5		V_{CC}	V
Input Low Voltage	V_{IL}	–0.3		+0.2	V
For Ports A-F					
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}	–0.3		+0.8	V
Tri-state (Off) Input Current (Vin = 0.8 to 4.5V at 500 KHz	I_{TSI}		10	µADC	
For Ports A-F Outputs					
Output High Voltage (I_{LOAD} = –100 µA)	V_{OH}	2.4	—	V_{DC}	
Output Low Voltage (I_{LOAD} = 1.6 mA)	V_{OL}	—	0.4	V_{DC}	
Power Dissipation (Frequency = ϕ2 clock rate)	P_D				
Operating			20	30	mW/MHz
IDLE Mode			3.5	5.0	mW/MHz
Stop Mode			0.6	1.0	mW

APPENDIX D
TIMING REQUIREMENTS AND SPECIFICATIONS

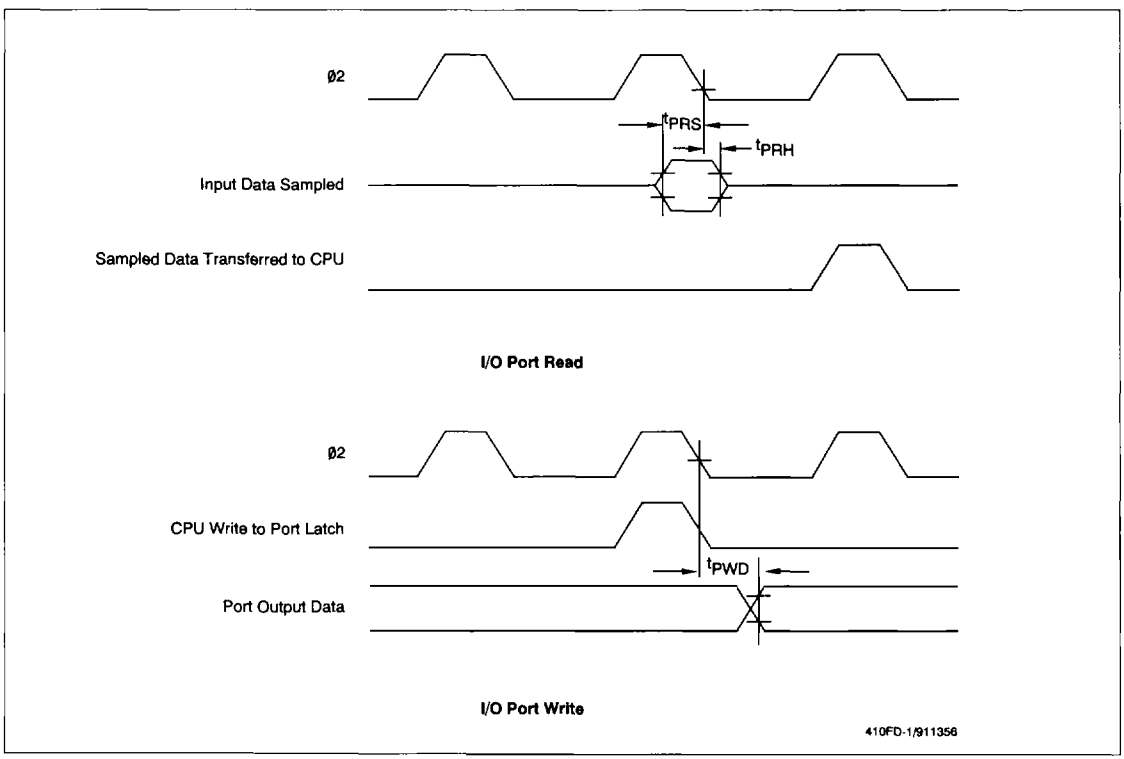
For all timing specifications, the following conditions apply:

1. T_A = 0°C to 70°C
2. V_{CC} = 5V ± 5%
3. Output loads = 50 pF + one TTL load.
   AD bus, Port E and Port F output loads = 70 pF + TTL load.
4. All times in nanoseconds (ns) except where noted.

GENERAL I/O PORTS (A, B, C, D, E, and F)

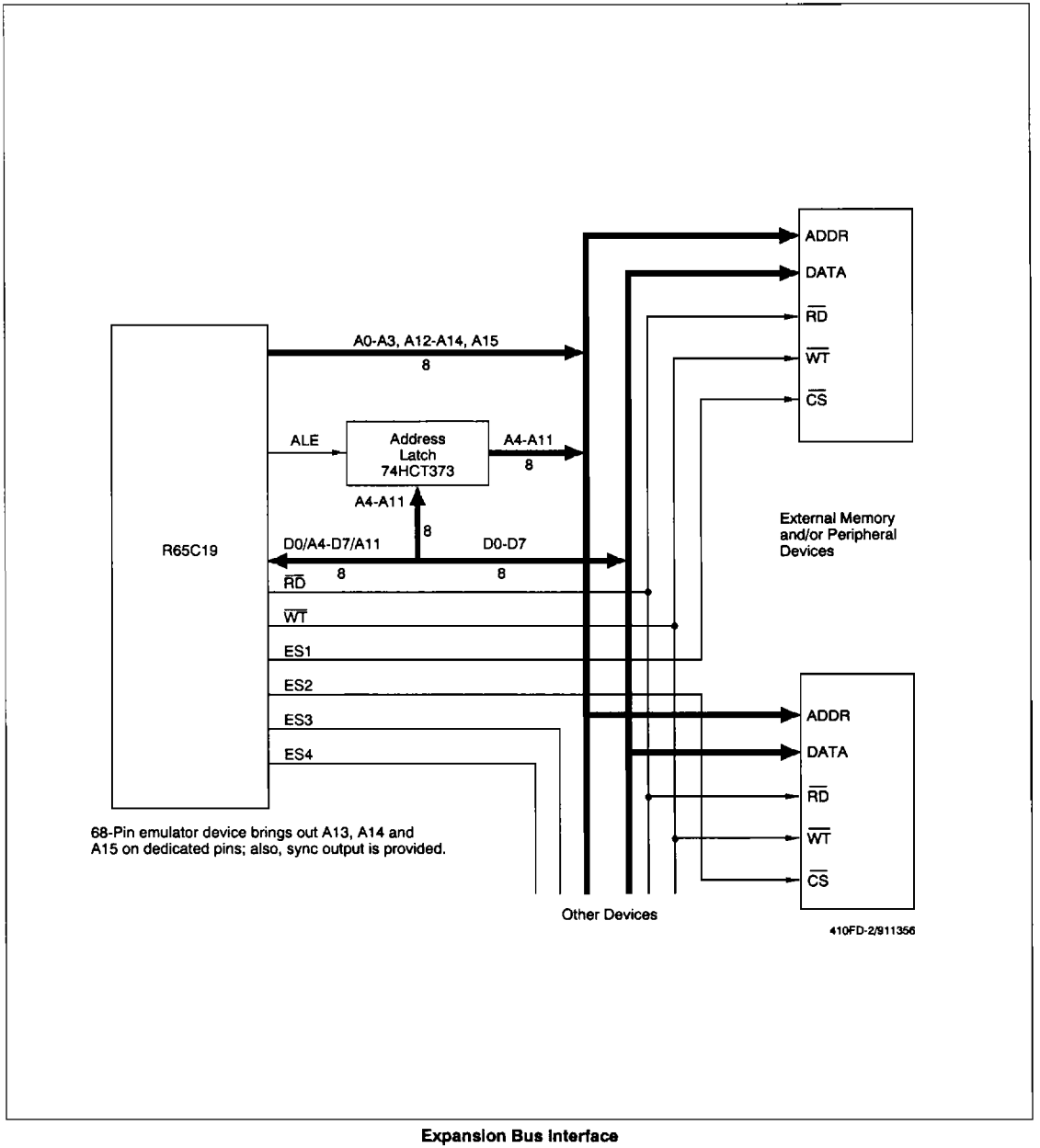
General I/O Timing

Symbol	Parameter	Min	Max	Units
t_{PRS}	Input Data Setup Time	25	–	ns
t_{PRH}	Input Data Hold Time	5	–	ns
t_{PWD}	Output Data Delay Time	–	30	ns



General I/O Waveforms

EXPANSION BUS



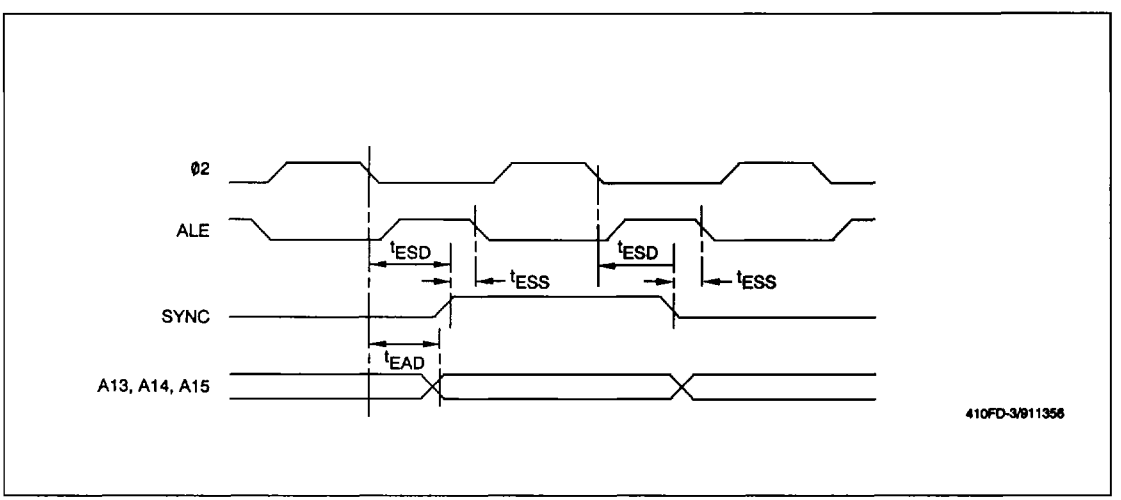
Expansion Bus Interface

Expansion Bus Timing

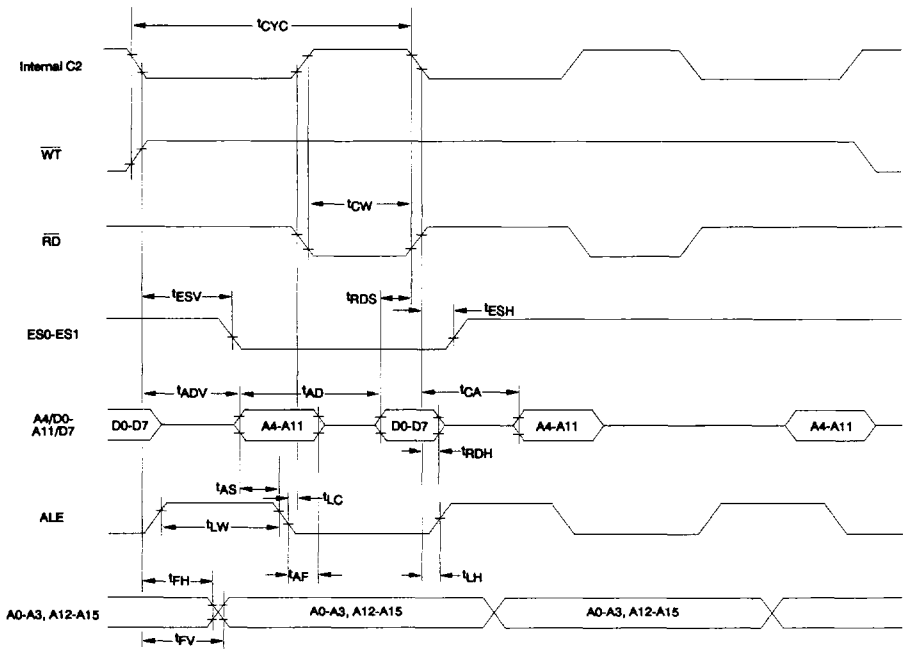
Symbol	Parameter	Min	Max	Units
t_{CYC}	Internal Operating Cycle	125	–	ns
t_{AD}	Addr Valid to Read Data Valid			
	Normal Cycle	–	75	ns
	Extended Cycle	–	200	ns
t_{AF}	ALE to Address Float	10	20	ns
t_{AS}	Address Valid to ALE	20	–	ns
t_{ADV}	($\overline{RD}$ or $\overline{WT}$) to Address Valid	–	35	ns
t_{CW}	($\overline{RD}$ or $\overline{WT}$) to ($\overline{RD}$ or $\overline{WT}$)			
	Normal Cycle	58	–	ns
	Extended Cycle	180	–	ns
t_{ESH}	($\overline{RD}$ or $\overline{WT}$) to ES	10	–	ns
t_{ESV}	($\overline{RD}$ or $\overline{WT}$) to ES	–	35	ns
t_{FH}	($\overline{RD}$ or $\overline{WT}$) to PFi Hold	10	–	ns
t_{FV}	($\overline{RD}$ or $\overline{WT}$) to PFi Valid	–	30	ns
t_{LC}	ALE to ($\overline{RD}$ or $\overline{WT}$)	0	–	ns
t_{LH}	($\overline{RD}$ or $\overline{WT}$) to ALE	5	–	ns
t_{LW}	ALE to ALE	35	–	ns
t_{RDH}	$\overline{RD}$ to Read Data Hold	0	–	ns
t_{RDS}	Read Data Valid to $\overline{RD}$ –	12	–	ns
t_{RWH}	ϕ2 to RW Hold	10	–	ns
t_{RWV}	ϕ2 to RW Valid	–	35	ns
t_{WTD}	$\overline{WT}$ to write Data Valid			
	Normal Cycle	–	30	ns
	Extended Cycle	–	30	ns
t_{WTH}	$\overline{WT}$ or Write Data Hold	10	–	ns

Expansion Bus Timing - R65C19 Emulator

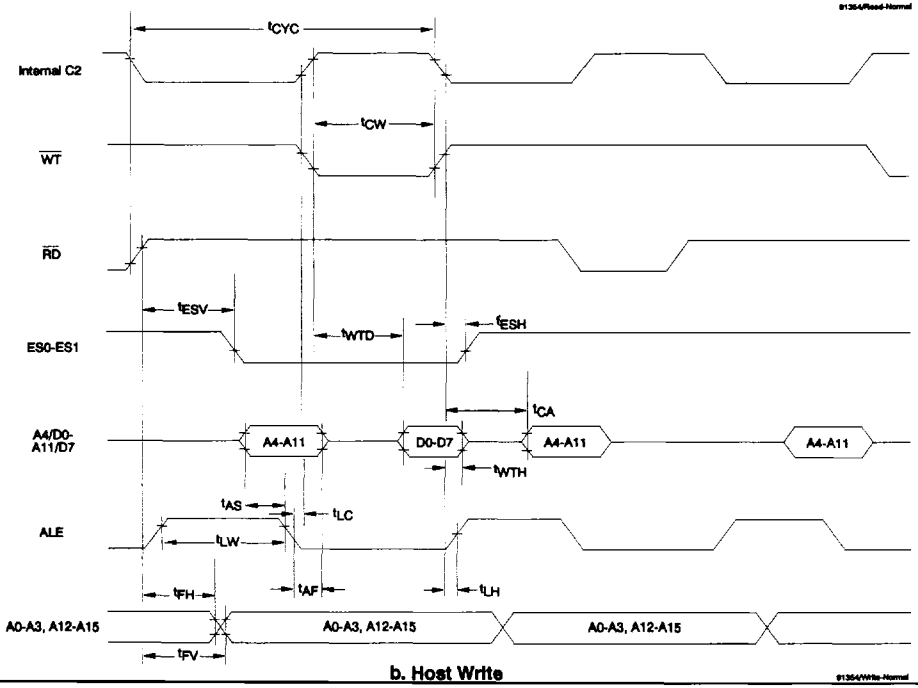
Symbol	Parameter	Min	Max	Units
t_{ESD}	Sync Setup	–	40	ns
t_{EAD}	Address Setup	–	30	ns



Expansion Bus Waveforms - R65C19 Emulator

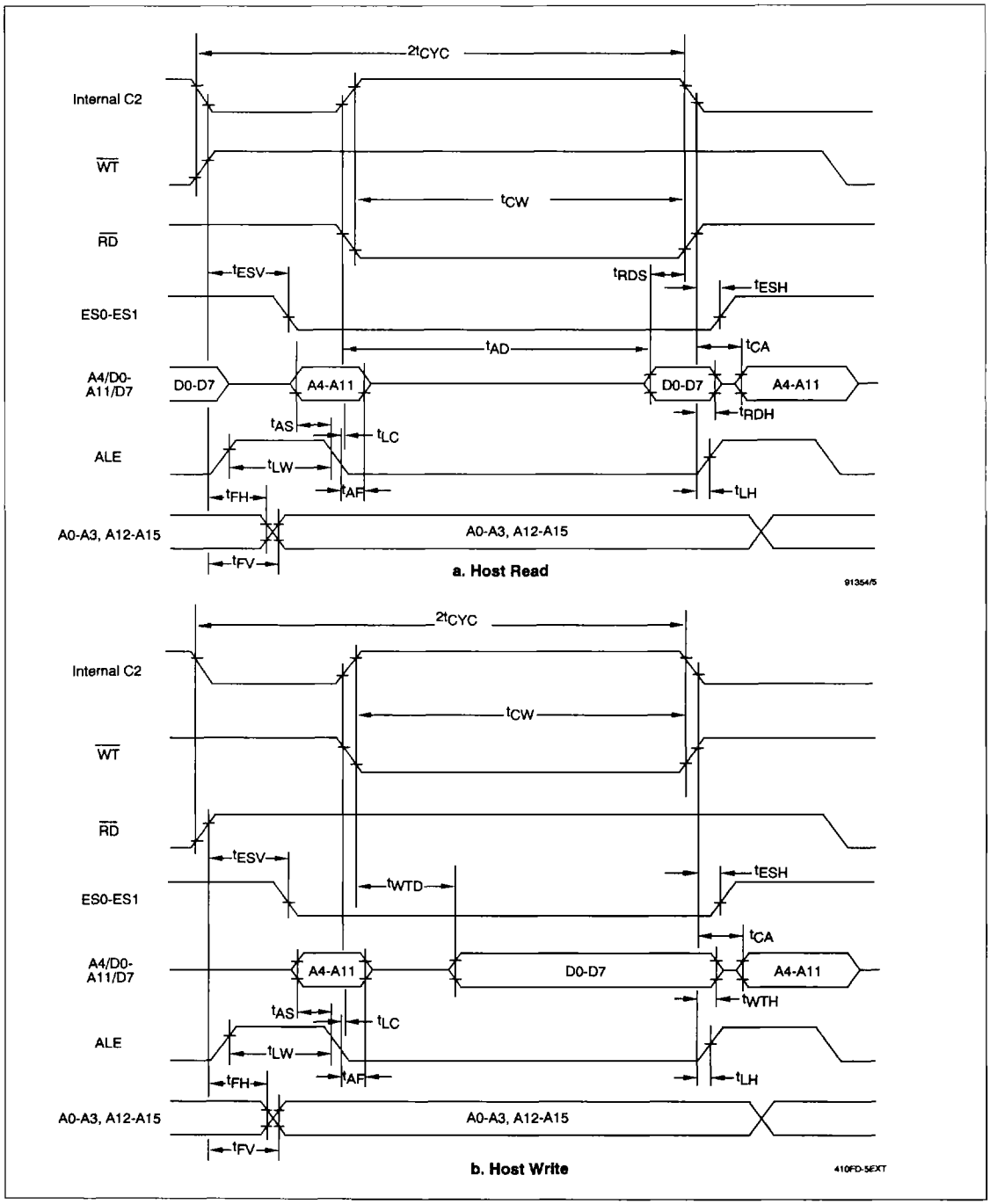


a. Host Read



b. Host Write

Expansion Bus Timing - Normal

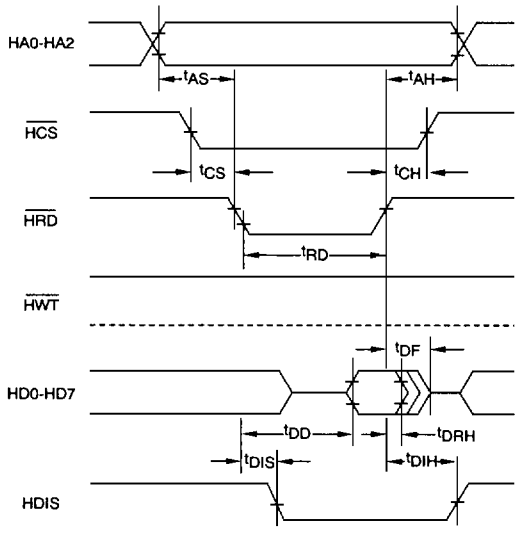


Expansion Bus Timing - Extended

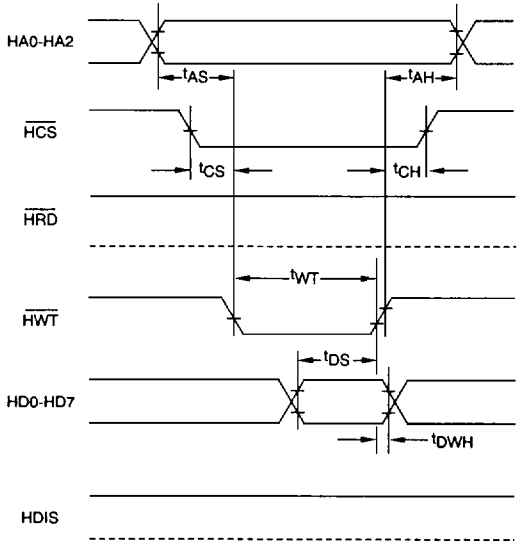
HOST BUS INTERFACE

Host Bus Timing

Symbol	Parameter	Min	Max	Units
t_{AS}	Address Setup	25	–	ns
t_{AH}	Address Hold	0	–	ns
t_{CS}	Chip Select Setup	10	–	ns
t_{CH}	Chip Select Hold	0	–	ns
t_{RD}	Read Strobe Width	100	–	ns
t_{DD}	Delay HRD to Data	–	75	ns
t_{DRH}	HRD Hold to Data	10	–	ns
t_{WT}	Write Strobe Width	75	–	ns
t_{DS}	Write Data Setup	30	–	ns
t_{DWH}	Write Data Hold	10	–	ns
t_{DF}	HRD to Driver Off	–	30	ns
t_{DIS}	HDIS Enable	–	40	ns
t_{DIH}	HDIS Hold	10	–	ns
t_{INH}	Interrupt Hold	–	100	ns

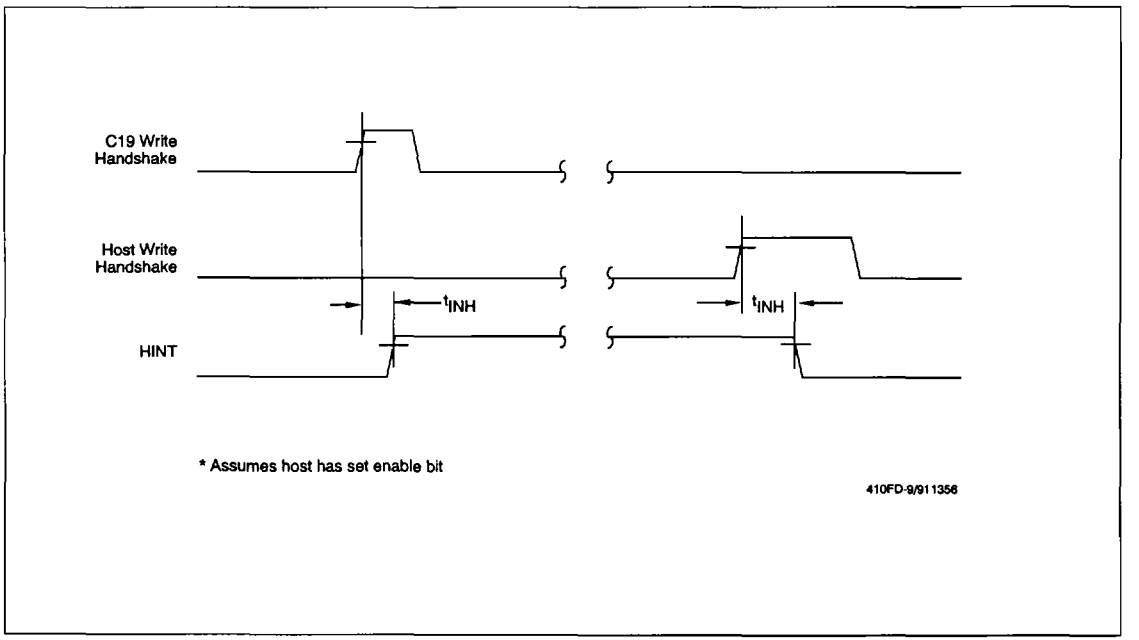


a. Host Read

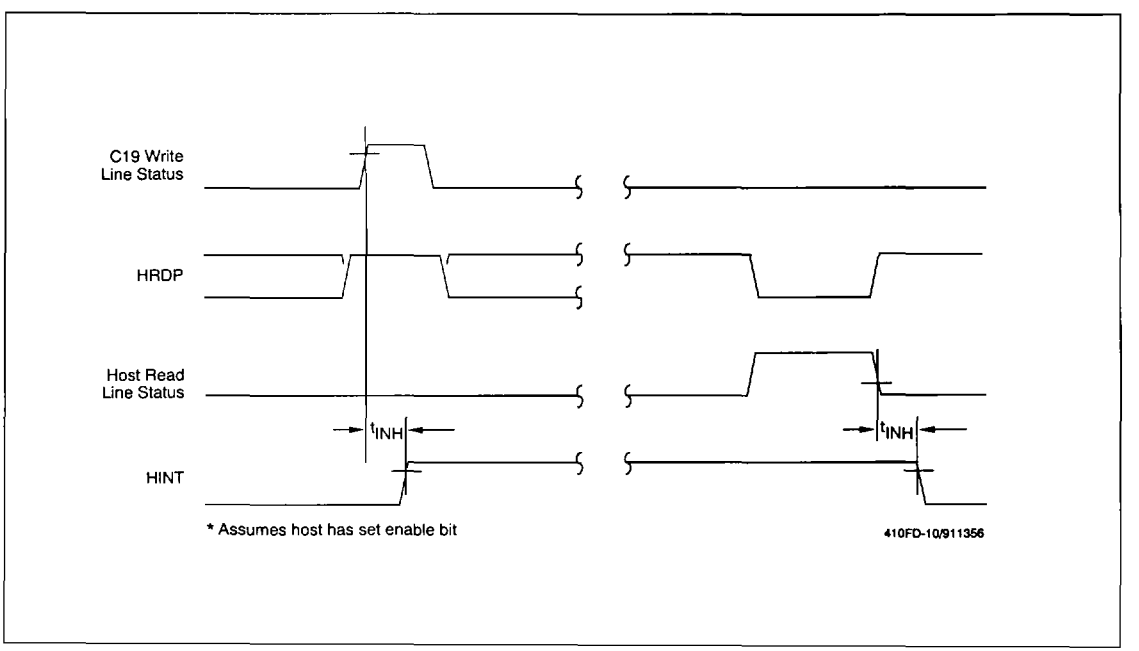


b. Host Write

Host Bus Interface Waveforms - RD & WT Strobes

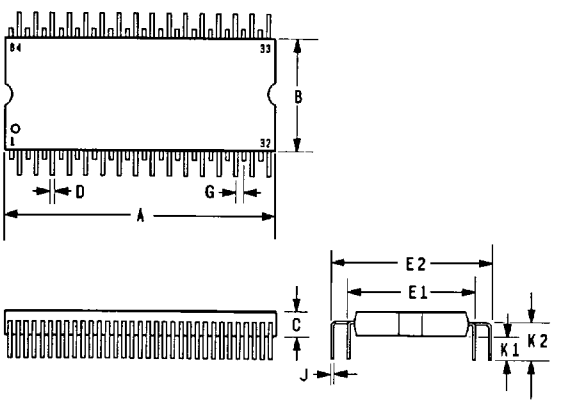


Host Bus Interrupt Timing - GP RAM Mode



Host Bus Interrupt Timing - 16450 Mode

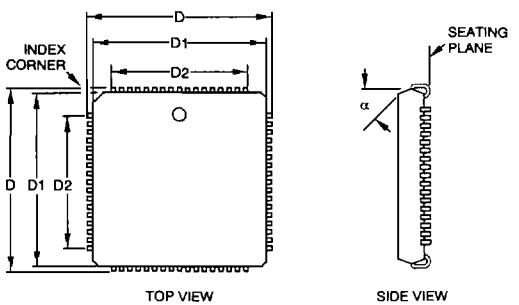
APPENDIX E
PACKAGE DIMENSIONS

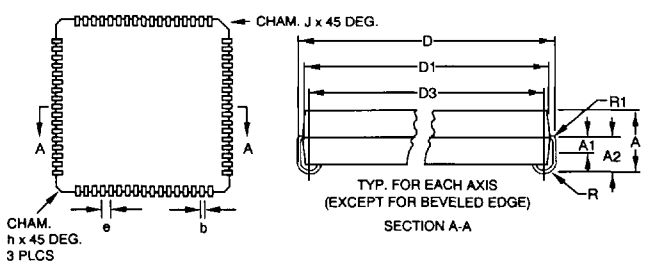


Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	41.10	41.61	1.618	1.638
B	17.02	17.53	0.670	0.690
C	3.56	4.06	0.140	0.160
D	0.48	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.18	0.33	0.007	0.013
K1	3.25	3.81	0.130	0.150
K2	5.08	5.84	0.200	0.230

REF: PD64Q/GP00-D188

64-Pin QUIP

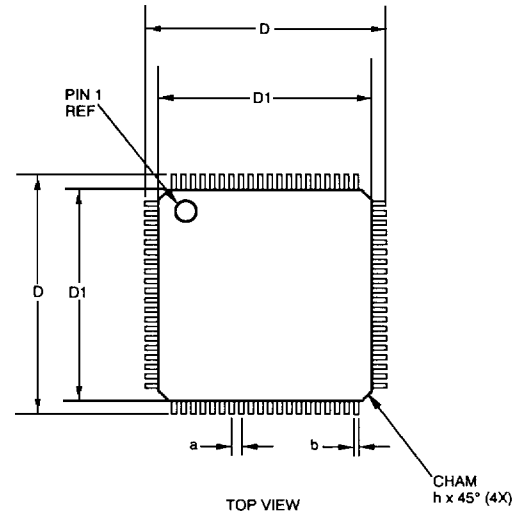




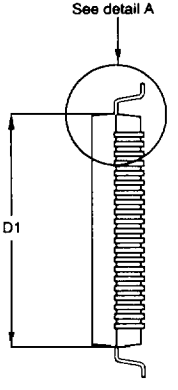
Dim.	Millimeters Min.	Max.	Inches Min.	Max.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25.27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0.805
D3	23.24	23.50	0.915	0.925
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	
Ref: PD68J/GP00-D164				

91710/2

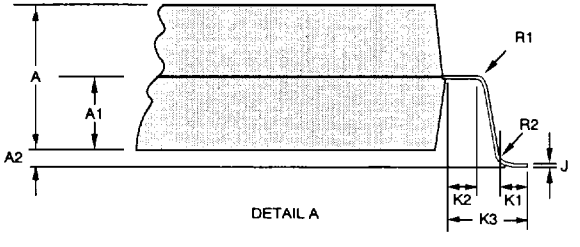
68-Pin PLCC



TOP VIEW



SIDE VIEW



DETAIL A

Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.95	2.05	0.077	0.081
A1	0.95	1.05	0.037	0.041
A2	0.15	0.25	0.006	0.010
D	17.05	17.35	0.671	0.683
D1	13.95	14.05	0.549	0.553
K1	0.70	0.90	0.028	0.035
K2	0.40	---	0.016	---
K3	1.60 REF		0.063 REF	
R1	0.13	---	0.005	---
R2	0.15	0.25	0.006	0.010
a	0.60	0.70	0.024	0.028
b	0.26	0.36	0.010	0.014
h	---	0.25	---	0.010
J	0.13	0.17	0.005	0.007
Ref: GP00-D227				

80-Pin PQFP

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