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Rockwell

R6500 Microcomputer System APPLICATION NOTE

R6531 Address Lines for Contiguous ROM

PURPOSE

The R6531 is a combination ROM-RAM-I/O Counter (RRIOC) device that can be combined with an 8 bit microprocessor to form a cost effective microcomputer system. By allowing the user to define the masking of the Chip Select Lines and Address Lines, a multi-chip system can be configured without any external address decoding.

The following design describes an 8-chip microcomputer system consisting of seven R6531's and a single R6502. The ROMs are designed to be a contiguous block extending from the highest address down. The RAM is a contiguous block extending from the lowest address up, and the I/O ports are located right above the RAM address space.

DESCRIPTION

MASK OPTIONS

The Address Masking chart in Table 1 shows all possible options for assigning the ROM, RAM and I/O addresses, and the address bits are further grouped as fields.

Table 1. Address Masking Options

R6531 FUNCTION	CHIP SELECTS			ADDRESS INPUTS (A0-A11)											
	CS3	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
ROM	X	X	X	X	2K ROM DECODE										
RAM	Y	Y	Y	Y	Y	Y	Y	Y	128 RAM DECODE						
I/O	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I/O DECODE			
				ROM SELECT (ROS)				RAM SELECT (RAS)			I/O SELECT (IOS)				

ROM Select Field (ROS) There are 16 possible codes for this field, one of which must be assigned to RAM and I/O, with the other 15 available to select 2K ROM blocks. However, if more than seven R6531's are used, the RAM and I/O must have distinct codes for this field, leaving 14 open codes for ROM selects.

RAM Select Field (RAS) There are 16 possible codes for this field, one of which must be assigned to I/O. The other 15 are available for selecting blocks of 128 bytes of RAM.

I/O Select Field (IOS) Eight possible codes are available for selecting the I/O registers. If different codes of ROS are used for RAM and I/O, then this field can be concatenated with RAS for even more flexibility of I/O address selections.

Note that the above description pertains to the situation where three different chip select lines are implemented. If there are only two chip select lines, then ROS still allows up to seven R6531's. If only one chip select line is implemented, three R6531's can be allowed, etc.

SELECTION OF ADDRESS CODES

Using the rules above, the number of address lines needed are determined. Then the system interconnect is as drawn in Figure 1, and the desired address ranges are simply assigned to the ROM, RAM and I/O for each R6531.

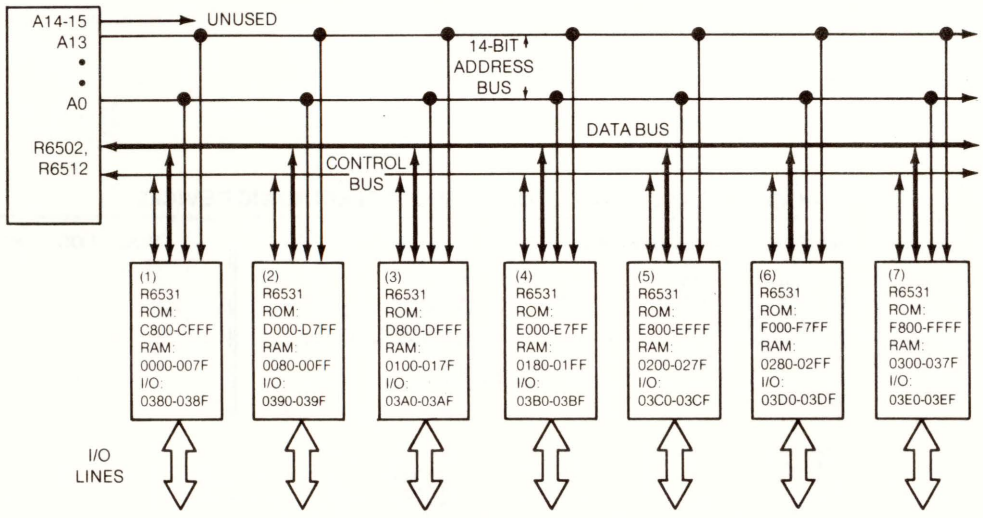

Figure 1. System Interconnect

From the System Interconnect diagram, the address masks can now be tabulated from the address ranges assigned to each R6531. Address Lines A12 and A13 are connected to CS1 and CS2 respectively, and the A0-A11 address lines from the processor are connected to A0-A11 of all the R6531 chips. Table 2 shows the final truth table for ROM, RAM and I/O selects.

The table below completes the design of the 8 chip microcomputer system. The address assignments chosen are just what is most general in programming practice. However, the designer is free to choose the address that is most meaningful to his system in terms of programming ease, upward expandability, and logical groupings of address lines for simple decoding if more specialized peripheral circuits are needed.

Table 2. Address Lines Selection

R6531 UNIT #	FUNCTIONAL ELEMENT	TRUTH TABLE									
		CS2	CS1	A11	A10	A9	A8	A7	A6	A5	A4
1	ROM	0	0	1	—	—	—	—	—	—	—
2		0	1	0	—	—	—	—	—	—	—
3		0	1	1	—	—	—	—	—	—	—
4		1	0	0	—	—	—	—	—	—	—
5		1	0	1	—	—	—	—	—	—	—
6		1	1	0	—	—	—	—	—	—	—
7		1	1	1	—	—	—	—	—	—	—
1	RAM	0	0	0	0	0	0	0	—	—	—
2		0	0	0	0	0	0	1	—	—	—
3		0	0	0	0	0	1	0	—	—	—
4		0	0	0	0	0	1	1	—	—	—
5		0	0	0	0	1	0	0	—	—	—
6		0	0	0	0	1	0	1	—	—	—
7		0	0	0	0	1	1	0	—	—	—
1	I/O	0	0	0	0	1	1	1	0	0	0
2		0	0	0	0	1	1	1	0	0	1
3		0	0	0	0	1	1	1	0	1	0
4		0	0	0	0	1	1	1	0	1	1
5		0	0	0	0	1	1	1	1	0	0
6		0	0	0	0	1	1	1	1	0	1
7		0	0	0	0	1	1	1	1	1	0