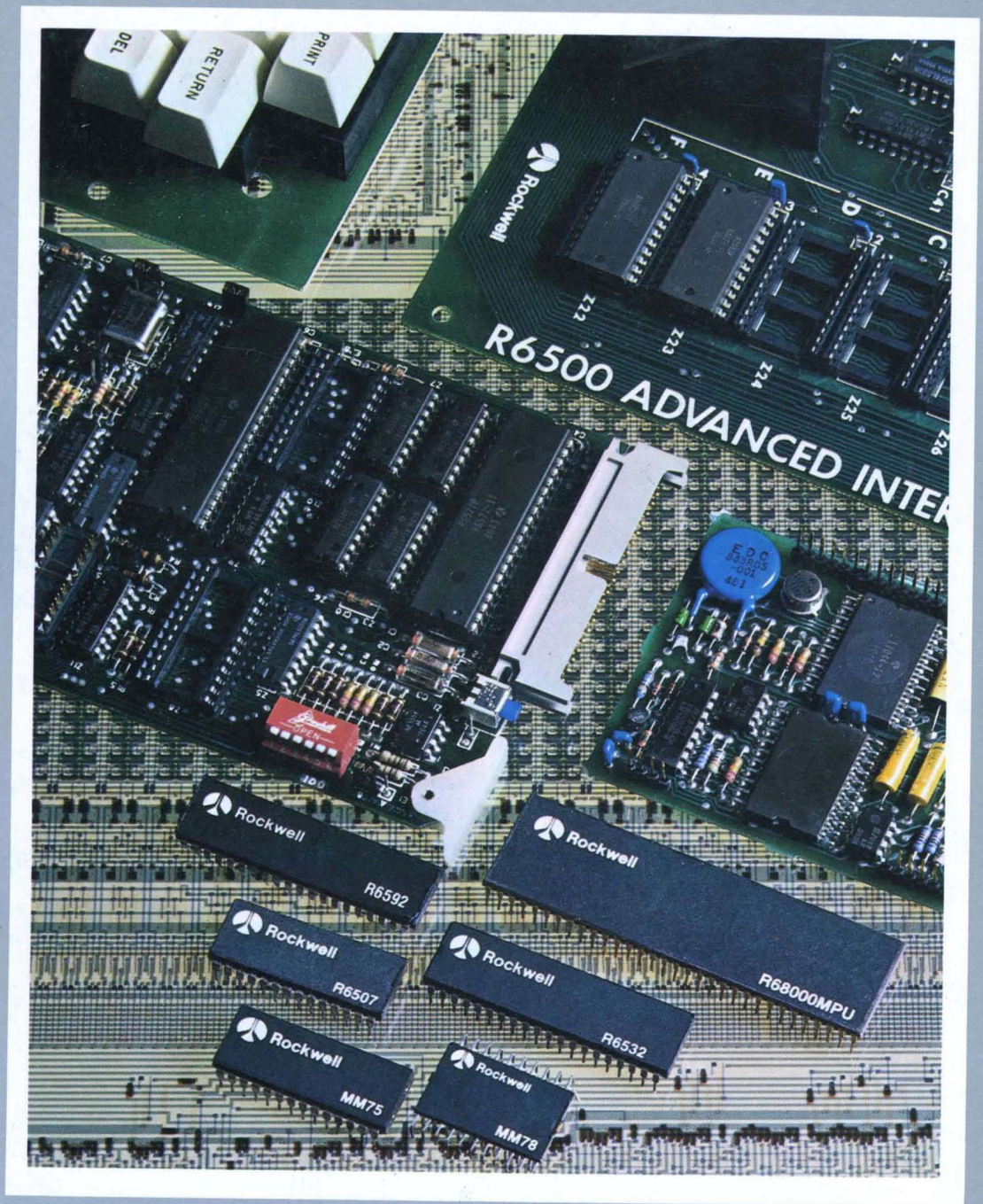


Electronic Devices Division
data catalog

Rockwell International

...where science gets down to business

Rockwell International

Electronic Devices Division
Data Catalog

R6500 NMOS μPs & μCs

R6500 I/O DEVICES

R6500 MEMORY-I/O COMBOS

AIM 65 MICRO-COMPUTER

RM65 BOARD PRODUCTS

SYSTEM 65 DEVELOPMENT SYSTEM

NMOS MEMORY PRODUCTS

R68000 16-BIT μP PRODUCTS

PPS-4/1 PMOS μCs

INTEGRAL MODEMS

TELECOM DEVICES

FILTER PRODUCTS


FILTER PRODUCTS
TELECOM DEVICES
INTEGRAL MODEMS
PPS-4/1 PMOS μCs
R68000 16-BIT μP PRODUCTS
NMOS MEMORY PRODUCTS
SYSTEM 65 DEVELOPMENT SYSTEM
RM65 BOARD PRODUCTS
AIM 65 MICRO-COMPUTER
R6500 MEMORY-I/O COMBOS
R6500 I/O DEVICES
R6500 NMOS μPs & μCs

TABLE OF CONTENTS

NMOS MEMORY PRODUCTS

R2316 2048 x 8 Static ROMs
R2332 4096 x 8 Static ROMs
R2332-xL 4096 x 8 Low-Power Static ROMs
R2364A 8192 x 8 Static ROMs
R2364B 8192 x 8 Static ROMs
R8104/R8114 1024 x 8 Static RAMs

R68000 16-BIT μP PRODUCTS

R68000 Microprocessing Unit
R68120 Intelligent Peripheral Controller (IPC)
R68451 Memory Management Unit (MMU)
R68450 DMA Controller (DMAC)
R68561 Multi-Protocol Communications Controller (MPCC)

PPS-4/1 PMOS μCs

PPS-4/1 Brochure
MM75 Microcomputer
MM76EL Low-Power Microcomputer
MM78 Microcomputer
MM78L Low-Power Microcomputer
MM78LA Low-Power Microcomputer
Serial Communication Protocol for Multiple PPS-4/1 Systems
Using PPS-4/1 to Operate a Liquid Crystal Display

INTEGRAL MODEMS

R24 2400 BPS Modular Modem
R24 DC 2400 BPS Direct Connect Modem
V96P/1 Multi-Configuration 9600 BPS Modem

TELECOM DEVICES

MOS/LSI Telecommunication Products Flyer
CRC8000,8001 Binary to Dial Pulse Dialer
CRC8030 Dual Tone Multi-Frequency Detector
R8040 T-1 Tri-Port Memory
R8050 T-1 Serial Transmitter
R8060 T-1 Serial Receiver

FILTER PRODUCTS

Rockwell-Collins Disc Wire Mechanical Filters
Collins Low Frequency Mechanical Filters
Collins USB-LSB-AM Mechanical Filters
F455FD Low-Cost Mechanical Filters
Disc Wire Mechanical Filters Standard Products
Low Frequency Narrowband Mechanical Filters Standard Products

R6500
NMOS
μPs & μCs

R6500 NMOS μPs & μCs

R6500

MICROCOMPUTER SYSTEM

R6500

Rockwell International

Printed in the U.S.A.

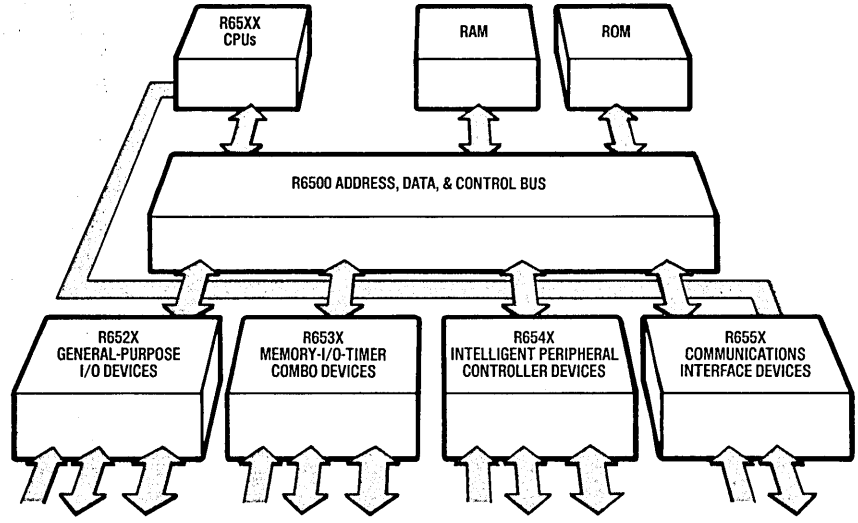
The R6500 Family

R6500 Family

A family of 10 software-compatible CPUs and 11 I/O, ROM, RAM and one-chip memory-I/O-timer circuits operating at proven 1 MHz and 2 MHz speeds with a single 5V power supply, provides you with economic system solutions for a broad range of applications.

The R6500/1 provides you with CPU, ROM, RAM, interrupts, counter and bi-directional data ports on a single chip. And it's totally software compatible with all other members of the R6500 family.

The R6500 promises you boosted performance and improved economics through its third generation architecture, which includes 13 powerful addressing modes, and its innovative circuit design and processing technology which reduce chip size and power consumption.



Rockwell is solidly backing the R6500

Rockwell has dedicated facilities for the high volume manufacturing of R6500 circuits produced with its own depletion load, silicon-gate N-channel process.

And Rockwell provides complete system development support: Rockwell's SYSTEM 65, a floppy-disk based, powerful yet low-cost complete development system. Plus AIM 65, TIM or timesharing program, complete documentation and extensive applications engineering support.

For the future, Rockwell is developing new R6500 devices that will enhance your own product development opportunities.

CPUs

Rockwell's R650X CPU options offer a selection of features in 40- and 28-pin versions to meet your system needs (see table below). The R6502 - R6507 Series has on-chip clock generation. The R6512 - R6515 Series allows the user to generate and control the clock externally.

Why the R6500 is a cost performance winner

- Proven 1 MHz or 2 MHz performance
- Pipeline architecture for fast operation with fewer cycles
- Single 5-volt power supply
- On-the-chip clock or an external clock
- 56 instructions
- 13 addressing modes and true indexing capability
- Decimal/binary arithmetic mode selection
- Bi-directional Data Bus (compatible with the MC 6800)
- Addressable memory range up to 65K bytes
- Multi-level interrupts – maskable/non-maskable
- Use with any type or speed memory
- Programmable stack pointer and variable length stack
- 40- and 28-pin DIP package options

R6500 CPU Options

	40-Pin DIP		28-Pin DIP				
	R6502	R6512	R6503 R6513	R6504 R6514	R6505 R6515	R6506	R6507
Memory Address Space	65K	65K	4K	8K	4K	4K	8K
Interrupts—Maskable	Yes	Yes	Yes	Yes	Yes	Yes	No
—Non-Maskable	Yes	Yes	Yes	No	No	No	No
SYNC—Output indicates op code fetch cycle	Yes	Yes	No	No	No	No	No
RDY—Single step and slow memory synchronization	Yes	Yes	No	No	Yes	No	Yes
$\emptyset_1$ Clock Output	Yes	Yes	No	No	No	Yes	No
DBE—Extended Data Bus Hold Time	No	Yes	No	No	No	No	No

The 40-pin versions provide full functional capability for memory intensive systems with extensive I/O requirements. The 28-pin versions offer flexibility in selecting the lowest cost CPU best suited to your application. 28-pin packages also provide denser board layout.

Thirteen addressing modes + true indexing = R6500 software power

The R6500 features 13 addressing modes. The first byte of each instruction is the operation code specifying both the instruction and the addressing mode. The addressing modes are summarized below.

- ACCUMULATOR ADDRESSING – A one byte instruction, operating on the accumulator.
- IMMEDIATE ADDRESSING – The operand is in the second byte of the instruction.
- ABSOLUTE ADDRESSING – The second and third bytes of the instruction specify the effective address in 65K bytes of addressable memory.
- ZERO PAGE ADDRESSING – Allows shorter code and execution times by assuming a zero page address.
- INDEXED ZERO PAGE ADDRESSING (X or Y, indexing.) – Zero page addressing used with an index register.
- INDEXED ABSOLUTE ADDRESSING (X or Y, indexing) – Absolute addressing used with X or Y index registers.
- IMPLIED ADDRESSING – The register containing the operand is implicitly stated in the operation code.
- RELATIVE ADDRESSING – Used only with branch instructions. The second byte is an "Offset" added to the contents of the program counter.
- INDEXED INDIRECT ADDRESSING – Uses an indirect zero page address indexed by X to fetch the effective address.
- INDIRECT INDEXED ADDRESSING – Uses a zero page address to fetch the effective base address to be indexed by Y.
- ABSOLUTE INDIRECT – Used only with JMP, the second and third bytes point to a two-byte effective address.

R6500 Microprocessor Instruction Set

		Execution Time (clock cycles)											
		Accumulator	Immediate	Zero Page	Zero Page, X	Zero Page, Y	Absolute	Absolute, X	Absolute, Y	Implied	Relative	(Indirect, X)	(Indirect), Y	Absolute Indirect
ADC	Add Memory to Accumulator with Carry	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
AND	"AND" Memory with Accumulator	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
ASL	Shift Left One Bit (Memory or Accumulator)	2	•	5	6	•	6	7	•	•	•	•	•	•
BCC	Branch on Carry Clear	•	•	•	•	•	•	•	•	•	2**	•	•	•
BCS	Branch on Carry Set	•	•	•	•	•	•	•	•	•	2**	•	•	•
BEQ	Branch on Result Zero	•	•	•	•	•	•	•	•	•	2**	•	•	•
BIT	Test Bits in Memory with Accumulator	•	•	3	•	•	4	•	•	•	•	•	•	•
BMI	Branch on Result Minus	•	•	•	•	•	•	•	•	•	2**	•	•	•
BNE	Branch on Result not Zero	•	•	•	•	•	•	•	•	•	2**	•	•	•
BPL	Branch on Result Plus	•	•	•	•	•	•	•	•	•	2**	•	•	•
BRK	Force Break	•	•	•	•	•	•	•	•	•	•	•	•	•
BVC	Branch on Overflow Clear	•	•	•	•	•	•	•	•	•	2**	•	•	•
BVS	Branch on Overflow Set	•	•	•	•	•	•	•	•	•	2**	•	•	•
CLC	Clear Carry Flag	•	•	•	•	•	•	•	•	2	•	•	•	•
CLD	Clear Decimal Mode	•	•	•	•	•	•	•	•	2	•	•	•	•
CLI	Clear Interrupt Disable Bit	•	•	•	•	•	•	•	•	2	•	•	•	•
CLV	Clear Overflow Flag	•	•	•	•	•	•	•	•	2	•	•	•	•
CMP	Compare Memory and Accumulator	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
CPX	Compare Memory and Index X	•	2	3	•	•	4	•	•	•	•	•	•	•
CPY	Compare Memory and Index Y	•	2	3	•	•	4	•	•	•	•	•	•	•
DEC	Decrement Memory by One	•	•	5	6	•	6	7	•	•	•	•	•	•
DEX	Decrement Index X by One	•	•	•	•	•	•	•	•	2	•	•	•	•
DEY	Decrement Index Y by One	•	•	•	•	•	•	•	•	2	•	•	•	•
EOR	"Exclusive OR" Memory with Accumulator	•	2	3	4	•	4	4*	4*	•	•	6	5	•
INC	Increment Memory by One	•	•	5	6	•	6	7	•	•	•	•	•	•
INX	Increment Index X by One	•	•	•	•	•	•	•	•	2	•	•	•	•
INY	Increment Y by One	•	•	•	•	•	•	•	•	2	•	•	•	•
JMP	Jump to New Location	•	•	•	•	•	3	•	•	•	•	•	•	5
JSR	Jump to New Location saving Return Address	•	•	•	•	•	6	•	•	•	•	•	•	•
LDA	Load Accumulator with Memory	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
LDX	Load Index X with Memory	•	2	3	•	4	4	•	4*	•	•	•	•	•
LDY	Load Index Y with Memory	•	2	3	4	•	4	4*	•	•	•	•	•	•
LSR	Shift Right One Bit (Memory or Accumulator)	2	•	5	6	•	6	7	•	•	•	•	•	•
NOP	No Operation	•	•	•	•	•	•	•	•	2	•	•	•	•
ORA	"OR" Memory with Accumulator	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
PHA	Push Accumulator on Stack	•	•	•	•	•	•	•	•	3	•	•	•	•
PHP	Push Processor Status on Stack	•	•	•	•	•	•	•	•	3	•	•	•	•
PLA	Pull Accumulator from Stack	•	•	•	•	•	•	•	•	4	•	•	•	•
PLP	Pull Processor Status from Stack	•	•	•	•	•	•	•	•	4	•	•	•	•
ROL	Rotate One Bit Left (Memory or Accumulator)	2	•	5	6	•	6	7	•	•	•	•	•	•
ROR	Rotate One Bit Right (Memory or Accumulator)	2	•	5	6	•	6	7	•	•	•	•	•	•
RTI	Return from Interrupt	•	•	•	•	•	•	•	•	6	•	•	•	•
RTS	Return from Subroutine	•	•	•	•	•	•	•	•	6	•	•	•	•
SBC	Subtract Memory from Accumulator with Borrow	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
SEC	Set Carry Flag	•	•	•	•	•	•	•	•	2	•	•	•	•
SED	Set Decimal Mode	•	•	•	•	•	•	•	•	2	•	•	•	•
SEI	Set Interrupt Disable Status	•	•	•	•	•	•	•	•	2	•	•	•	•
STA	Store Accumulator in Memory	•	•	3	4	•	4	5	5	•	•	6	6	•
STX	Store Index X in Memory	•	•	3	•	4	4	•	•	•	•	•	•	•
STY	Store Index Y in Memory	•	•	3	4	•	4	•	•	•	•	•	•	•
TAX	Transfer Accumulator to Index X	•	•	•	•	•	•	•	•	2	•	•	•	•
TAY	Transfer Accumulator to Index Y	•	•	•	•	•	•	•	•	2	•	•	•	•
TSX	Transfer Stack Pointer to Index X	•	•	•	•	•	•	•	•	2	•	•	•	•
TXA	Transfer Index X to Accumulator	•	•	•	•	•	•	•	•	2	•	•	•	•
TXS	Transfer Index X to Stack Pointer	•	•	•	•	•	•	•	•	2	•	•	•	•
TYA	Transfer Index Y to Accumulator	•	•	•	•	•	•	•	•	2	•	•	•	•

*Add one cycle if indexing across page boundary
**Add one cycle if branch is taken, and one additional cycle if branching operation crosses page boundary

R6500/1 One-Chip Microcomputer

The R6500/1

In the R6500/1, Rockwell has combined the high-performance R6502 CPU with such versatile features as 2048 bytes of ROM, 64 bytes of RAM, 32 bi-directional I/O lines, four interrupts and a 16-bit programmable counter (with four separate interval/event modes) — all in a single 40-pin package.

The R6500/1 also has on-the-chip 1 MHz or 2 MHz clock operation with external single clock, crystal or RC frequency input.

The R6500/1 includes a separate power pin that maintains RAM on 10% of the operating power. In the event power is lost, this standby power retains RAM data until execution is resumed.

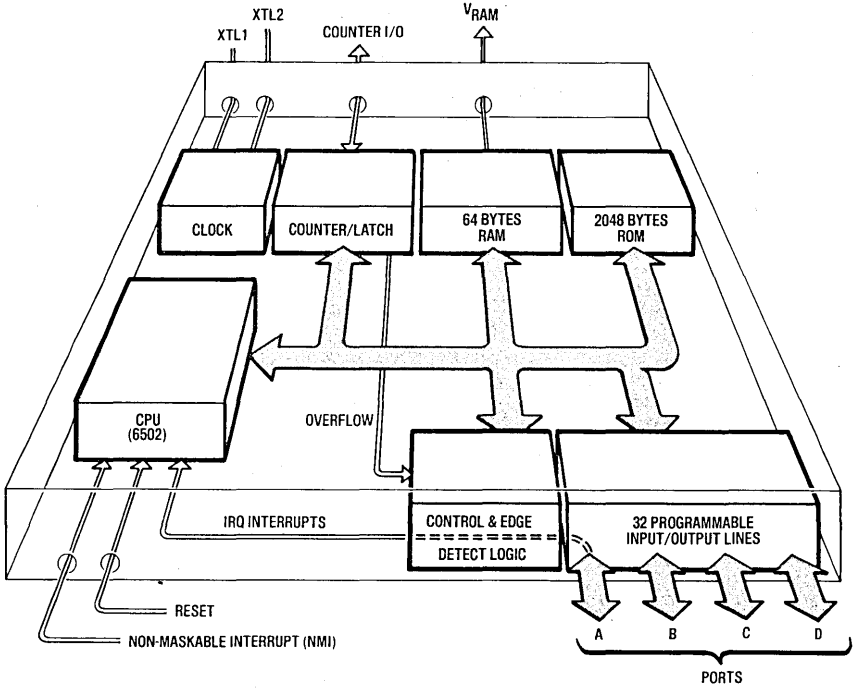
Rockwell backs up the R6500/1 with solid system development support in two ways:

The R6500/1E, a 64-pin emulator device with 40 pins electrically identical to the R6500/1, may be used for program development and prototyping with external EPROM or RAM.

A Personality option to SYSTEM 65 customizes Rockwell's popular microcomputer development system for complete R6500/1 software and hardware development.

R6500/1 Features

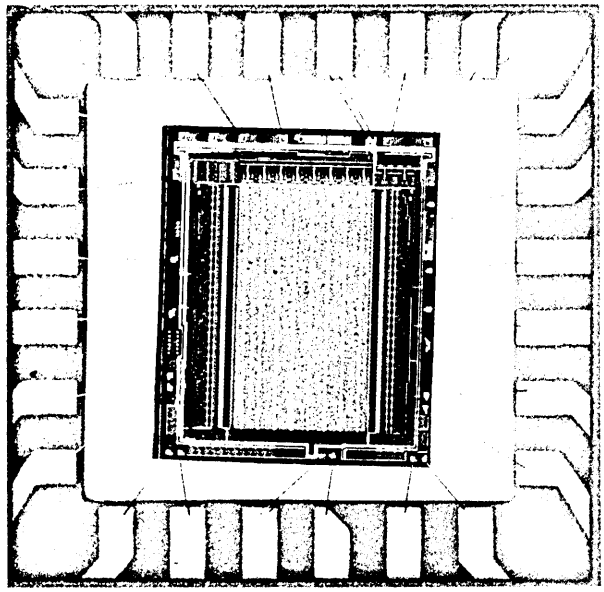
- 2K-Byte Mask Programmable ROM
- 64-Byte Static RAM
- R6502 CPU
- Four 8-Bit Bidirectional I/O Ports
- 16-Bit Programmable Counter/Latch With Four Modes:
  - — Interval Timer
  - — Pulse Generator
  - — Event Counter
  - — Pulse Width Measurement
- Five Interrupts
- Fully Upward/Downward Compatible With 6500 Family
- 64-Pin PROM-compatible Emulator Device Available



Standard Memory Devices

The R6500 system bus enables you to use low cost, widely available standard memory devices. For your convenience, Rockwell now offers the five memory devices, described below. All are completely TTL compatible, fully static — no clocks or refresh strobes required — and operate from a single + 5 V power supply

- **R2114 4K STATIC RAM**
  1024 x 4 in high-density 18-pin package with common data I/O; 450ns access and cycle time; fully static — no clocks or strobes required; single + 5V power supply; total TTL compatibility. (Industry standard.)
- **R2316B 16K STATIC ROM**
  2048 x 8 in standard 24-pin package; pin-compatible with 2708 EPROM; 450 ns. max. cycle time; three chip selects. (Industry standard; replaces *two* 8K EPROMs.)
- **R2332 32K STATIC ROM**
  The industry's first static 4096 x 8 N-channel ROM; standard 24-pin package; 450 ns. max. cycle time; two chip selects.
- **R2332-3 32K STATIC ROM**
  Same as R2332, but has 300 ns. max. cycle time.



Input/Output Devices

General-Purpose I/O Devices

These versatile peripheral controllers allow effective trade-offs between software and hardware, enabling implementation of complex R6500 microcomputer systems at minimum overall cost. Both are available in 1 MHz and 2 MHz versions. All R6500 I/O devices—including the memory-I/O combos—have TTL and CMOS compatible peripheral lines with transistor drive capability and high-impedance, tri-state data outputs.

- **R6520 Peripheral Interface Adapter (PIA)**
  40-pin package, two 8-bit bi-directional I/O ports, four peripheral control/interrupt input lines, fully automatic data transfers between processor and peripheral devices.

The PIA provides individual I/O line control for keyboard strobes and returns, driving displays and discrete indicators as well as 8-bit parallel communications in *handshake* or clocked control modes.

- **R6522 Versatile Interface Adapter (VIA)**
  40-pin package, has R6520 PIA features plus two 16-bit programmable interval timers/counters, data latching on I/O ports, 8-bit buffered shift register for serial I/O interfacing.
  The enhanced features of the VIA provide a serial interface for inter-system communications, ASCII serial data generation, pulse width modulation, and waveform synthesis. The two timers work in conjunction with the serial channel or may provide interval timing for real time applications.

Input/Output Devices

Memory-I/O-Timer Combination Devices

By combining an R650X Series CPU with one-chip memory, I/O and timer combination devices, the designer nets a powerful, cost-effective two chip microcomputer system which can also be the base configuration for modular, expandable applications.

- **R6530 ROM-RAM-I/O-Timer (RRIOT)**
  40-pin package; 1 MHz operation; 1024 x 8 ROM; 64 x 8 static RAM; two 8-bit bi-directional data I/O ports; two progammable data direction registers; programmable 8-bit interval timer with prescale and interrupt control.
- **R6531 ROM-RAM-I/O-Counter (RRIOC)**
  40-pin package; 1 MHz or 2 MHz operation; 2048 x 8 ROM; 128 x 8 static RAM; 8-bit serial data channel; two bi-directional I/O ports, with a total of 15 data lines, including four external interrupts and handshake control.

  The RRIOC also provides a fully-buffered 16-bit counter/timer with four program selectable modes — interval timer, pulse generator, event counter and pulse width measurement.

  A separate 52-pin version of RRIOC offers expanded I/O in additional 8-bit output port and 4-bit input port.
- **R6532 RAM-I/O-Timer (RIOT)**
  40-pin package; 1 MHz operation; 128 x 8 static RAM; two 8-bit bi-directional data ports; two programmable data direction registers; programmable 8-bit interval timer with prescale and interrupt control; programmable edge detect interrupt, for fast service of critical events.
- **R6534 ROM-I/O-Counter (RIOC)**
  40-pin package; 1 MHz operation; 4096 x 8 ROM; 8-bit serial data channel; two bi-directional data I/O ports, with a total of 14 data lines, including four external interrupts and handshake control.

  The RIOC also provides a programmable 16-bit counter/latch with interval timer, pulse generator and event counter modes.

  A separate 52-pin version of RIOC offers an additional 8-bit output port, 3-bit input port and one additional I/O line.

Intelligent Peripheral Controller Devices

The devices listed below get your interface design off to a solid start.

- **R6541 Programmable Keyboard/Display Controller (PKDC)**
  40-pin package, 8-character FIFO/Sensor RAM for keyboard entries, two CPU-addressable 16-byte display RAMs.

  The PKDC is a general-purpose keyboard and segmented display interface device. The keyboard portion can scan up to 128 matrix-type key switches, and can also interface with an array of 64 sensors or a strobed interface keyboard. The display portion provides a buffered scanned display interface with LED, fluorescent, Borroughs SELF-SCAN®, and other display technologies.
- **R6545 CRT Controller (CRTC)**
  40-pin package, refresh RAM, fully-programmable scanning and cursor, light pen register.

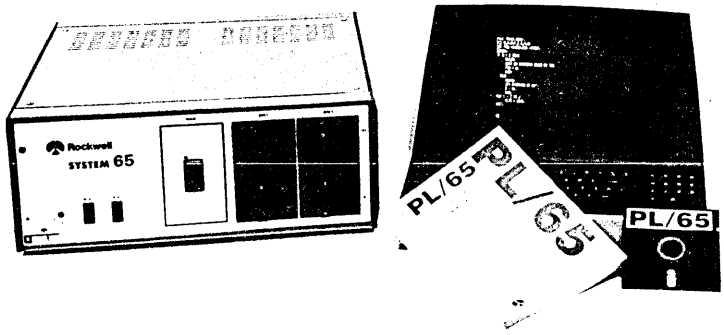
  The CRTC is designed to interface an 8-bit microprocessor to CRT raster scan video displays. It provides refresh memory addresses and character generator row addresses, which allow up to 16K characters with 32 scan lines per character to be addressed. Refresh memory may be addressed in either straight binary or by row/column.

Communications Interface Device

- **R6551 Asynchronous Communication Interface Adapter (ACIA)**
  28-pin package provides the interface between R6500-based systems and serial communication data sets and modems. With its on-chip baud rate generator, the ACIA is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16X an external clock rate.

  The ACIA has programmable word lengths of 5, 6, 7 or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 stop bits.

Product Development



Rockwell's SYSTEM 65

SYSTEM 65 is a new easy to use, powerful, complete development system for the R6500 family of microcomputers. The basic configuration includes two built-in, mini-floppy disk drives, 16K bytes of user memory and 16K bytes of resident operating system.

Monitor commands are self-prompting whenever memory, peripheral, or disk file assignment is required. Text editor provides line, string, and character editing functions. A resident two-pass assembler and dynamic debug package complete the operating system. Both source and object code may be maintained in memory for fast editing, assembling, and checkout. Since the total monitor, editor, debug and assembler are resident in ROM, 100% of the disk storage and drive utilization is available to the user.

The mini-floppy diskettes may be used as storage for source and object code and documentation. Each diskette has the capacity for 78K bytes of information in a maximum of 60 files.

SYSTEM 65 supports a vareity of terminals with serial data from 100 baud to 9600 baud. Connectors are provided for both RS-232 C and current loop interfacing. Reader ON/OFF signals and RTS/CTS control signals are standard. Included is a parallel port providing automatic control to high speed printers, such as Diablo, Centronics and Tally.

And Rockwell offers these options to SYSTEM 65:

- PL/65 High-Level Language
- USER 65 in-circuit emulation option
- PROM Programmer Module, for programming a 2704/2708/2716/2758 PROM device from the front panel socket
- R6500/1 Personality option, for developing with the R6500/1 single-chip microcomputer
- 16K x 8 Static RAM Modules
- PROM/ROM Module, accepts 2316/2332 ROM or 2708/2716/2758 PROM devices
- Wire-wrap Design Prototyping Module
- Extender Card for circuit probing

PL/65 High-Level Language

A high-level language resembling PL/1 and ALGOL is now available to designers developing programs for the R6500 microprocessor family using the SYSTEM 65 development system.

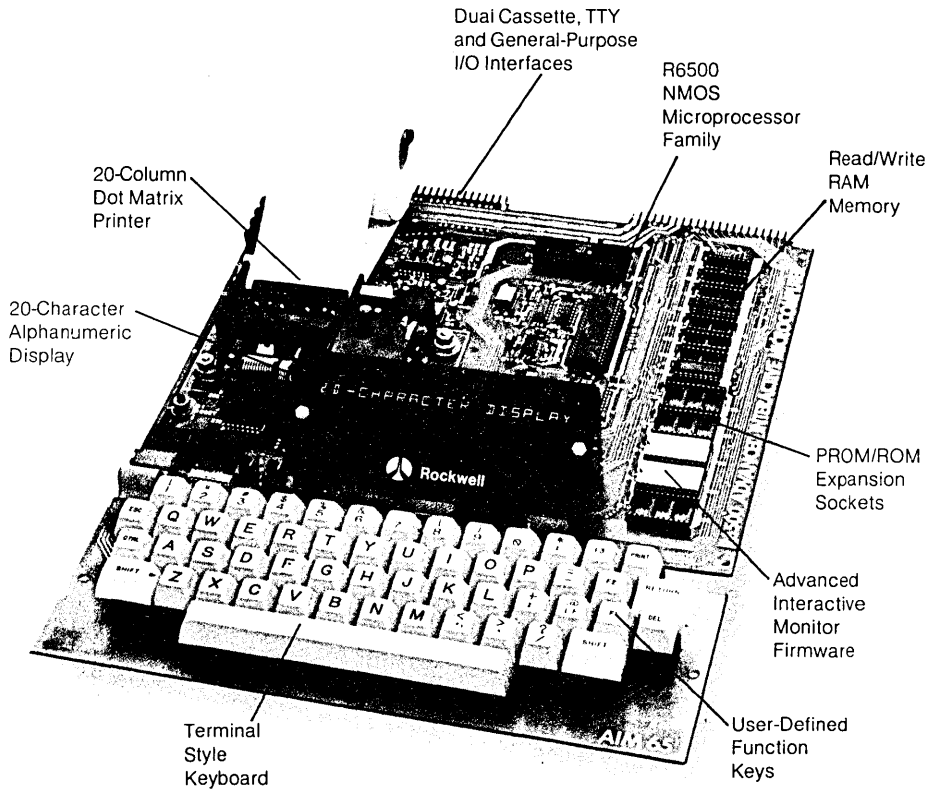
Designated PL/65, the language is considerably easier to use than assembly language or object code, thus increasing programmer productivity while reducing software development time and costs. The PL/65 compiler outputs source code to the SYSTEM 65's resident assembler. This permits enhancing or debugging at the assembler level before object code is generated. In addition, PL/65 statements may be mixed with assembly language instructions for timing or code optimization.

The PL/65 compiler is available to SYSTEM 65 users as a preprogrammed mini-floppy diskette. No additional memory is required other than the standard 16K bytes of RAM.

The PL/65 language supports modular program design. Its general control structures for conditional and iterative looping allow the language to be used effectively for structured programs. Other language features include: assignment, integer arithmetic, conditional execution, collective execution, linear array manipulation, data area declaration and array initialization. Block structures, subscripts and parenthetical expressions are also supported.

AIM 65

For learning, designing, work or just plain fun. . . .



Rockwell's R6500 Advanced Interactive Microcomputer (AIM 65) can get you into the exciting world of microcomputers a lot easier and at a lot lower cost than you may have thought possible.

As a learning aid, AIM 65 gives you an assembled, tested and warranted R6502-based microcomputer system with a full-sized keyboard, an alphanumeric 20-character display and, uniquely, an alphanumeric 20-column thermal printer.

An on-board Advanced Interactive Monitor program provides extensive control and program development functions. You'll be writing your programs in assembly language — there's no need to memorize "opcodes". And for more specialized applications, we offer a two-pass, symbolic assembler and a BASIC interpreter as plug-in ROM options.

You'll master fundamentals rapidly. Then you'll appreciate the fact that unlike the computer "toys" on the market, AIM 65 offers flexibility and expandability you would expect to find only in a sophisticated microcomputer development system.

Literature

How to make it all work for you

Rockwell has put together a complete set of documentation and reference manuals to help you implement the R6500 microprocessor family.

- **R6500 Hardware Manual**
  A detailed description of each chip in the family, how they interface, how the peripherals are controlled, as well as the design techniques facilitating system operation, testing and maintenance. Special emphasis is on "bringing up" a system with testing techniques, scope synchronizing and general trouble-shooting procedures — $5.
- **R6500 Programming Manual**
  Defines the architecture of the R6500 Series, the function of each instruction and valuable programming information. Special emphasis is on the sophisticated addressing modes of the family — $5.
- **Cross-Assembler Manual**
  Cross-Assembler directives are described as used in time-share and batch operations, with special aids on understanding and resolving error messages — $5.
- **SYSTEM 65 User's Manual**
  Instructs the user in operating the SYSTEM 65 Microcomputer Development System and its application in developing a working microprocessor system — $5.
- **PL/65 User's Manual**
  A complete guide to PL/65, the high-level language for the R6500 family — $10.
- **AIM 65 User's Guide**
  Full technical details tell you everything you need to operate the AIM 65 — $5.
- **AIM 65 BASIC Language Reference Manual**
  A how-to guide for using AIM 65 with the BASIC language ROM option installed—$5.
- **TIM Manual**
  Defines how to apply the Teletype I/O Monitor — $2.
- **R6500 Data Sheets**
  Provides quick understanding of the capabilities and characteristics of each available R6500 device and support equipment. To order data sheets simply specify the part number or the name of the support equipment.

Where to get more on the R6500

Rockwell's normal procedure is to provide you with free data sheets so that you can select the R6500 devices and support equipment of most interest to you. A nominal charge is made for reference manuals.

For data, devices or support equipment contact the nearest Rockwell office or distributor listed on the back page of this brochure. For in-depth assistance, obtain the name of your nearest Rockwell sales representative from any Rockwell office.

DOCUMENT NO. 29000 D39
REV. 3, FEBRUARY 1979

PART NUMBER
R650X and R651X

Rockwell

R6500 Microcomputer System DATA SHEET

R6500 MICROPROCESSORS (CPU's)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon Gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides memory and microcomputer system . . . as well as low-cost design aids and documentation.

R6500 MICROPROCESSOR (CPU) CONCEPT

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz and 2 MHz) and temperature (commercial, industrial and military) versions.

MEMBERS OF THE R6500 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

Model	Addressable Memory
R6502	65K Bytes
R6503	4K Bytes
R6504	8K Bytes
R6505	4K Bytes
R6506	4K Bytes
R6507	8K Bytes

Microprocessors with External Two Phase Clock Output

Model	Addressable Memory
R6512	65K Bytes
R6513	4K Bytes
R6514	8K Bytes
R6515	4K Bytes

FEATURES

- Single +5V supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit Bidirectional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz and 2 MHz operation
- Choice of external or on-chip clocks
- On-the-chip clock options
  - External single clock input
  - RC time base input
  - Crystal time base input
- Commercial, industrial and military temperature versions
- Pipeline architecture

Ordering Information

Order Number: R65XX_ _ _

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = −40°C to +85°C (Industrial)
  - MT = −55°C to +125°C (Military)
  - M = MIL-STD-883, Class B
- Package:
  - C = Ceramic
  - P = Plastic (Not Avaible for M or MT suffix)
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz
- Model Designator:
  - XX = 02, 03, 04, ... 15

NOTE: Contact your local Rockwell Representative concerning availability.

R6500 MICROPROCESSORS (CPU's)

Specifications subject to change without notice

R6500 Signal Description

Clocks (ϕ_1, ϕ_2)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A0-A15)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (D0-D7)

Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)

This input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as fast (max. 2 cycle) Direct Memory Access (DMA).

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ register to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A negative going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1 and must be externally synchronized.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

ADDRESSING MODES

ACCUMULATOR ADDRESSING – This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING – In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING – In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING – The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING – In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING – Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING – In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING – In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT – The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index X by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

NOP No Operation

ORA "OR" Memory with Accumulator

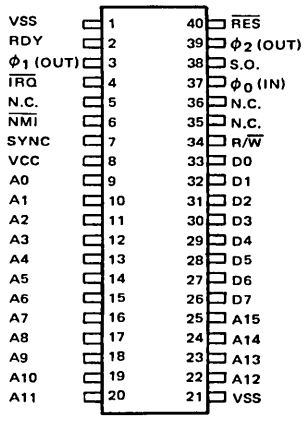
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Register
TYA Transfer Index Y to Accumulator

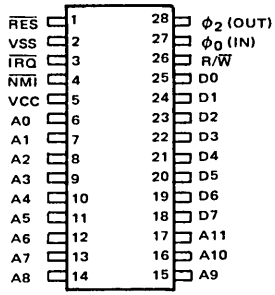
R6502 – 40 Pin Package



Features of R6502

- 65K Addressable Bytes of Memory (A0-A15)
- IRQ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- NMI Interrupt

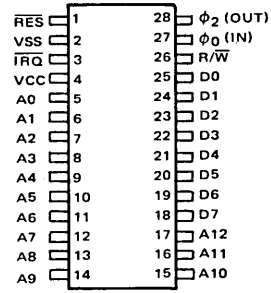
R6503 – 28 Pin Package



Features of R6503

- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bidirectional Data Bus

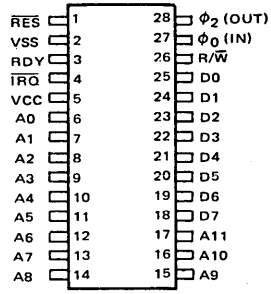
R6504 – 28 Pin Package



Features of R6504

- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- IRQ Interrupt
- 8 Bit Bidirectional Data Bus

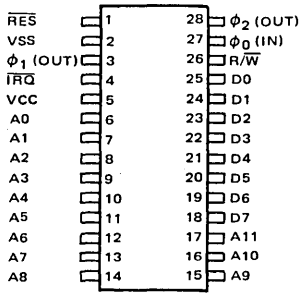
R6505 – 28 Pin Package



Features of R6505

- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- IRQ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus

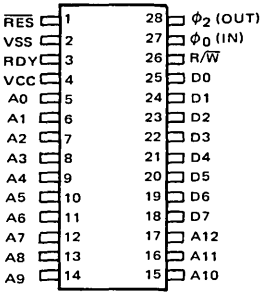
R6506 – 28 Pin Package



Features of R6506

- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- Two phase output clock for timing of support chips
- 8 Bit Bidirectional Data Bus

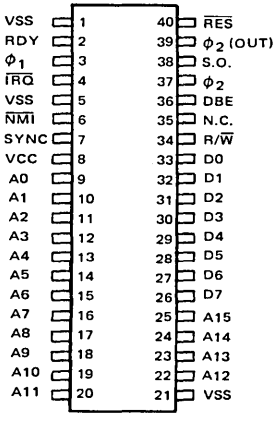
R6507 – 28 Pin Package



Features of R6507

- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- RDY Signal
- 8 Bit Bidirectional Data Bus

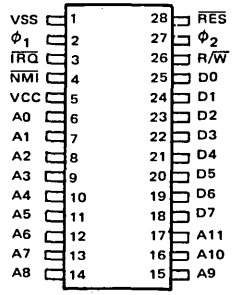
R6512 – 40 Pin Package



Features of R6512

- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus
- SYNC Signal
- Two phase clock input
- Data Bus Enable

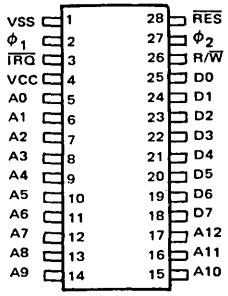
R6513 – 28 Pin Package



Features of R6513

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bidirectional Data Bus

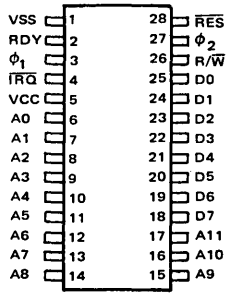
R6514 – 28 Pin Package



Features of R6514

- 8K Addressable Bytes of Memory (A0-A12)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- 8 Bit Bidirectional Data Bus

R6515 – 28 Pin Package



Features of R6515

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus

INSTRUCTION SET

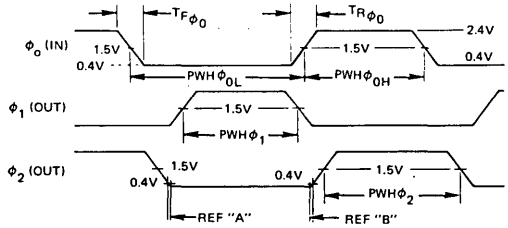
INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS. X			ABS. Y			RELATIVE			INDIRECT			Z. PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V * B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V · · · · Z C	ADC
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N · · · · · Z ·	AND
ASL	C ← 7 6 5 4 3 2 1 0 ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N · · · · · Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2								· · · · · · · ·	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2								· · · · · · · ·	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2								· · · · · · · ·	BEQ
BIT	A ∧ M				2C	4	3	24	3	2																															M7 M6 · · · · Z ·	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2								· · · · · · · ·	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2								· · · · · · · ·	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2								· · · · · · · ·	BPL
BRK	BREAK													00	7	1																									· · · · 1 · 1 · ·	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2								· · · · · · · ·	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2								· · · · · · · ·	BVS
CLC	0 → C													18	2	1																									· · · · · · · 0	CLC
CLD	0 → D													D8	2	1																									· · · · 0 · · ·	CLD
CLI	0 → I													58	2	1																									· · · · · 0 · ·	CLI
CLV	0 → V													B8	2	1																									· 0 · · · · · ·	CLV
CMP	A - M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N · · · · · Z C	CMP
CPX	X - M	E0	2	2	EC	4	3	E4	3	2																															N · · · · · Z C	CPX
CPY	Y - M	C0	2	2	CC	4	3	C4	3	2																															N · · · · · Z C	CPY
DEC	M - 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N · · · · · Z ·	DEC
DEX	X - 1 → X													CA	2	1																									N · · · · · Z ·	DEX
DEY	Y - 1 → Y													88	2	1																									N · · · · · Z ·	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N · · · · · Z ·	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N · · · · · Z ·	INC
INX	X + 1 → X													E8	2	1																									N · · · · · Z ·	INX
INY	Y + 1 → Y													C8	2	1																									N · · · · · Z ·	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				· · · · · · · ·	JMP
JSR	JUMP SUB				20	6	3																																		· · · · · · · ·	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N · · · · · Z ·	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N · · · · · Z ·	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N · · · · · Z ·	LDY
LSR	0 → 7 6 5 4 3 2 1 0 → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 · · · · · Z C	LSR
NOP	NO OPERATION													EA	2	1																									· · · · · · · ·	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N · · · · · Z ·	ORA
PHA	A → Ms S - 1 → S													48	3	1																									· · · · · · · ·	PHA
PHP	P → Ms S - 1 → S													08	3	1																									· · · · · · · ·	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N · · · · · Z ·	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	7 6 5 4 3 2 1 0 ← C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N · · · · · Z C	ROL
ROR	C → 7 6 5 4 3 2 1 0				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N · · · · · Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									· · · · · · · ·	RTS
SBC	A - M - C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V · · · · Z (3)	SBC
SEC	1 → C													38	2	1																									· · · · · · · 1	SEC
SED	1 → D													F8	2	1																									· · · · 1 · · ·	SED
SEI	1 → I													78	2	1																									· · · · · 1 · ·	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										· · · · · · · ·	STA
STX	X → M				8E	4	3	86	3	2																													96	4	2	· · · · · · · ·	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																· · · · · · · ·	STY
TAX	A → X													AA	2	1																									N · · · · · Z ·	TAX
TAY	A → Y													A8	2	1																									N · · · · · Z ·	TAY
TSX	S → X													BA	2	1																									N · · · · · Z ·	TSX
TXA	X → A													8A	2	1																									N · · · · · Z ·	TXA
TXS	X → S													9A	2	1																									· · · · · · · ·	TXS
TYA	Y → A													98	2	1																									N · · · · · Z ·	TYA

(1) ADD 1 to 'N' IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO 'N' IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO 'N' IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE, Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

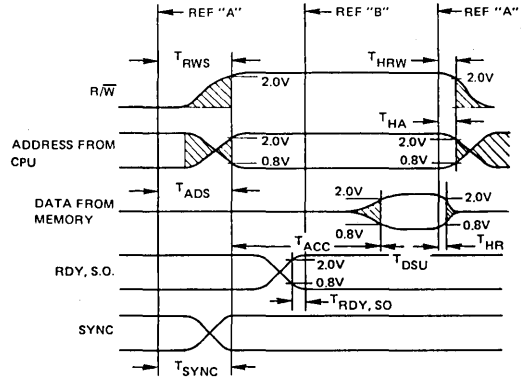
X	INDEX X	+	ADD
Y	INDEX Y	-	SUBTRACT
A	ACCUMULATOR	∧	AND
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR
Ms	MEMORY PER STACK POINTER	∨	EXCLUSIVE OR

M7	MEMORY BIT 7
M6	MEMORY BIT 6
n	NO. CYCLES
#	NO. BYTES

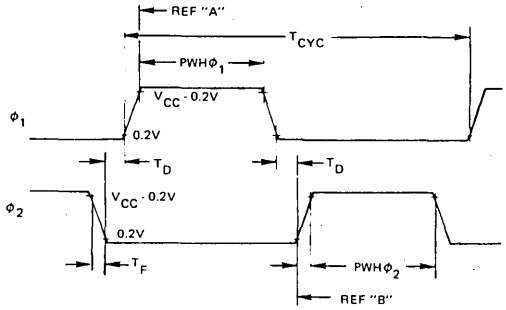
Clock Timing – R6502, 03, 04, 05, 06, 07



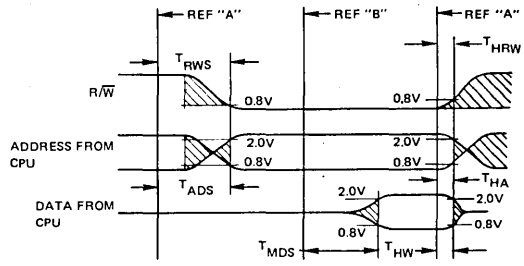
Timing for Reading Data from Memory or Peripherals



Clock Timing – R6512, 13, 14, 15

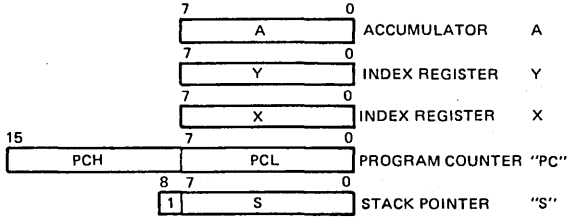


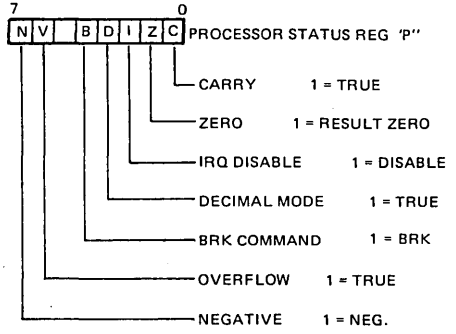
Timing for Writing Data to Memory or Peripherals



Note: "REF." means Reference Points on clocks.

PROGRAMMING MODEL





1 MHz Timing

Clock Timing — R6502, 03, 04, 05, 06, 07

Characteristic	Symbol	Min	Typ	Max	Units
Cycle Time	T_{CYC}	1.0	–	10.0	µs
$\phi_{o(IN)}$ Pulse Width (measured at 1.5V)	$PWH\phi_o$	460	–	520	ns
$\phi_{o(IN)}$ Rise, Fall Time	$TR\phi_o, TF\phi_o$	–	–	10	ns
Delay Time Between Clocks (measured at 1.5V)	T_D	5	–	–	ns
$\phi_{1(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\phi_1$	$PWH\phi_{oL}$-20	–	$PWH\phi_{oL}$	ns
$\phi_{2(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\phi_2$	$PWH\phi_{oH}$-40	–	$PWH\phi_{oH}$-10	ns
$\phi_{1(OUT)}$, $\phi_{2(OUT)}$ Rise, Fall Time (measured at 0.8V to 2.0V) (Load = 130 pF + 1 TTL)	T_R, T_F	–	–	25	ns

2 MHz Timing

Clock Timing — R6502, 03, 04, 05, 06, 07

Characteristic	Symbol	Min	Typ	Max	Units
Cycle Time	T_{CYC}	0.5	–	10.0	µs
$\phi_{o(IN)}$ Pulse Width (measured at 1.5V)	$PWH\phi_o$	240	–	260	ns
$\phi_{o(IN)}$ Rise, Fall Time	$TR\phi_o, TF\phi_o$	–	–	10	ns
Delay Time Between Clocks (measured at 1.5V)	T_D	5	–	–	ns
$\phi_{1(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\phi_1$	$PWH\phi_{oL}$-20	–	$PWH\phi_{oL}$	ns
$\phi_{2(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\phi_2$	$PWH\phi_{oH}$-40	–	$PWH\phi_{oH}$-10	ns
$\phi_{1(OUT)}$, $\phi_{2(OUT)}$ Rise, Fall Time (measured at 0.8V to 2.0V) (Load = 130 pF + 1 TTL)	T_R, T_F	–	–	25	ns

* The lowest operating frequency for the commercial temperature range CPU's is 100 KHz, which corresponds to a maximum cycle time (T_{CYC}) of 10 µs. The lowest operating frequency for the industrial and military temperature range CPU's is 250 KHz, which corresponds to a maximum cycle time (T_{CYC}) of 4 µs.

Clock Timing — R6512, 13, 14, 15

Characteristic	Symbol	Min	Typ	Max	Units
Cycle Time	T_{CYC} *	1000	–	–	ns
Clock Pulse Width (Measured at Vcc - 0.2V) φ1 / φ2	PWH φ1 / PWH φ2	430 / 470	–	–	ns
Fall Time (Measured from 0.2V to Vcc - 0.2V)	T_F	–	–	25	ns
Delay Time between Clocks (Measured at 0.2V)	T_D	0	–	–	ns

Clock Timing — R6512, 13, 14, 15

Characteristic	Symbol	Min	Typ	Max	Units
Cycle Time	T_{CYC} *	500	–	–	ns
Clock Pulse Width (Measured at Vcc - 0.2V) φ1 / φ2	PWH φ1 / PWH φ2	215 / 235	–	–	ns
Fall Time (measured from 0.2V to Vcc - 0.2V)	T_F	–	–	12	ns
Delay Time between Clocks (measured at 0.2V)	T_D	0	–	–	ns

Read/Write Timing **

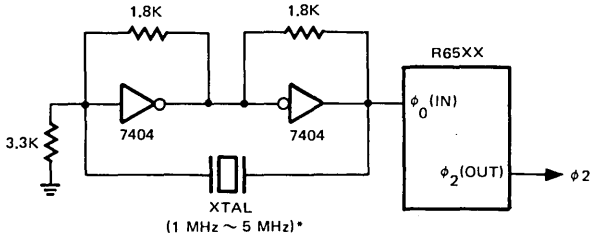
Characteristic	Symbol	Min	Typ	Max	Units
Read/Write Setup Time from R6500	T_{RWS}	–	100	225	ns
Address Setup Time from R6500	T_{ADS}	–	100	225	ns
Memory Read Access Time	T_{ACC}	–	–	650	ns
Data Stability Time Period	T_{DSU}	100	–	–	ns
Data Hold Time — Read	T_{HR}	10	–	–	ns
Data Hold Time — Write	T_{HW}	60	90	–	ns
Data Setup Time from R6500	T_{MDS}	–	150	175	ns
RDY, S.O. Setup Time	T_{RDY}	100	–	–	ns
SYNC Setup Time from R6500	T_{SYNC}	–	–	225	ns
Address Hold Time	T_{HA}	30	60	–	ns
R/$\overline{W}$ Hold Time	T_{HRW}	30	60	–	ns

Read/Write Timing **

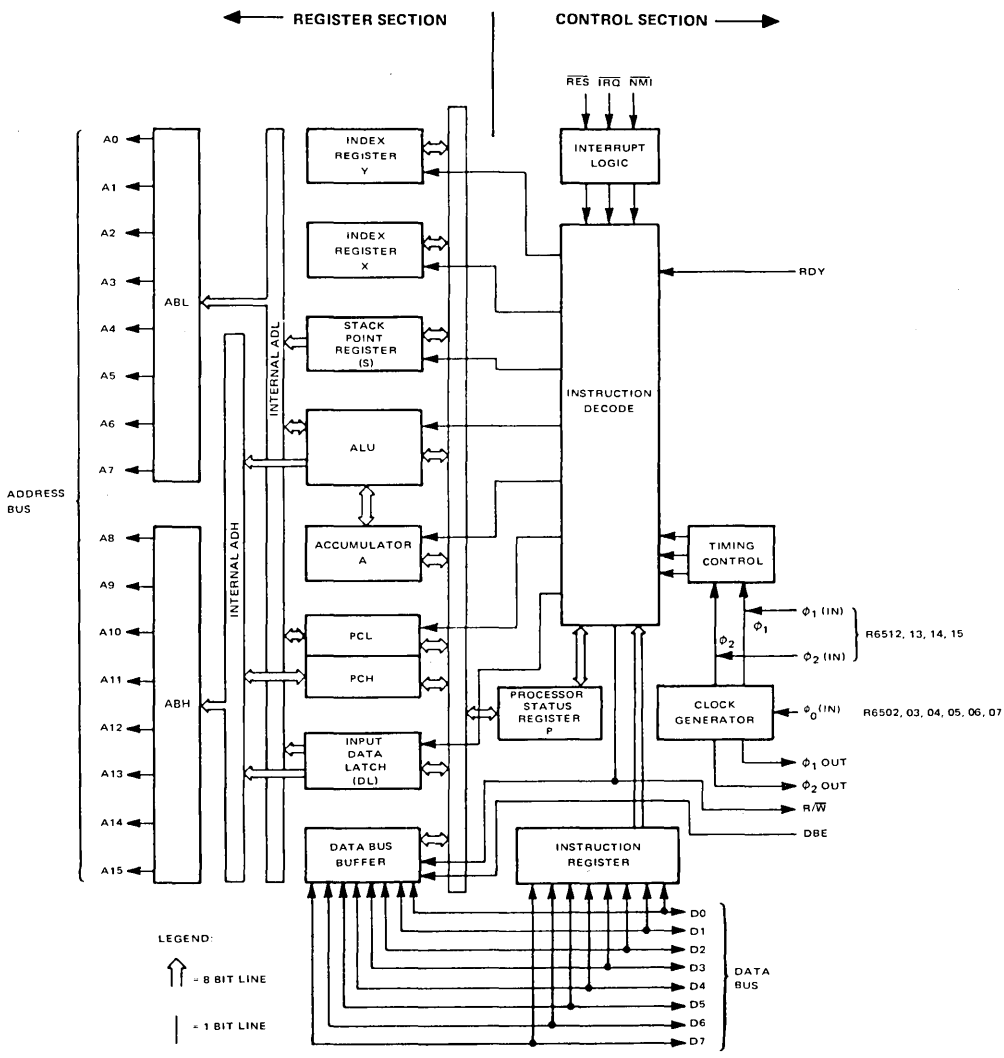
Characteristic	Symbol	Min	Typ	Max	Units
Read/Write Setup Time from R6500A	T_{RWS}	–	75	140	ns
Address Setup Time from R6500A	T_{ADS}	–	75	140	ns
Memory Read Access Time	T_{ACC}	–	–	310	ns
Data Stability Time Period	T_{DSU}	50	–	–	ns
Data Hold Time — Read	T_{HR}	10	–	–	ns
Data Hold Time — Write	T_{HW}	60	90	–	ns
Data Setup Time from R6500A	T_{MDS}	–	75	100	ns
RDY, S.O. Setup Time	T_{RDY}	50	–	–	ns
SYNC Setup Time from R6500A	T_{SYNC}	–	–	150	ns
Address Hold Time	T_{HA}	30	60	–	ns
R/$\overline{W}$ Hold Time	T_{HRW}	30	60	–	ns

** Load Conditions = 1 TTL Load + 130 pf

RECOMMENDED TIME BASE GENERATION



*CRYSTAL: CTS KNIGHTS MP SERIES, OR EQUIVALENT



Note: 1. Clock Generator is not included on R6512, 13, 14, 15
2. Addressing Capability and control options vary with each of the R6500 Products.

R6500 Internal Architecture

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature	T_A		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Military		-55 to +125	
Storage Temperature	T_{STG}	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics

(V_{CC} = 5.0±5%, V_{SS} = 0)

ϕ_1, ϕ_2 applies to R6512, 13, 14, 15, $\phi_{o(in)}$ applies to R6502, 03, 04, 05, 06 and 07.

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}				Vdc
Logic, $\phi_{o(in)}$		V_{SS} + 2.4	–	V_{CC}	
ϕ_1, ϕ_2		V_{CC} - 0.3	–	V_{CC} + 0.25	
Input Low Voltage	V_{IL}				Vdc
Logic, $\phi_{o(in)}$		V_{SS} - 0.3	–	V_{SS} + 0.4	
ϕ_1, ϕ_2		V_{SS} - 0.3	–	V_{SS} + 0.4	
Input High Threshold Voltage	V_{IHT}				Vdc
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		V_{SS} + 2.0	–	–	
Input Low Threshold Voltage	V_{ILT}				Vdc
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		–	–	V_{SS} + 0.8	
Input Leakage Current	I_{in}				μA
(V_{in} = 0 to 5.25V, V_{CC} = 0)					
Logic (Excl. RDY, S.O.)		–	–	2.5	
ϕ_1, ϕ_2		–	–	100	
$\phi_{o(in)}$		–	–	10.0	
Three-State (Off State) Input Current	I_{TSI}				μA
(V_{in} = 0.4 to 2.4V, V_{CC} = 5.25V)					
Data Lines		–	–	10	
Output High Voltage	V_{OH}				Vdc
(I_{LOAD} = -100 μAdc, V_{CC} = 4.75V)					
SYNC, Data, A0-A15, R/$\overline{W}$, ϕ_1, ϕ_2		V_{SS} + 2.4	–	–	
Output Low Voltage	V_{OL}				Vdc
(I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V)					
SYNC, Data, A0-A15, R/$\overline{W}$, ϕ_1, ϕ_2		–	–	V_{SS} + 0.4	
Power Dissipation	P_D				W
Commercial temp. versions		–	0.25	0.575	
Industrial and military temp. versions		–	0.50	0.700	
Capacitance at 25°C	C				pF
(V_{in} = 0, f = 1 MHz)					
Logic	C_{in}	–	–	10	
Data		–	–	15	
A0-A15, R/W, SYNC	C_{out}	–	–	12	
$\phi_{o(in)}$	$C_{\phi o(in)}$	–	–	15	
ϕ_1	$C_{\phi 1}$	–	30	50	
ϕ_2	$C_{\phi 2}$	–	50	80	

Note: $\overline{IRQ}$ and $\overline{NMI}$ require 3K pull-up resistors.

DOCUMENT NO. 29000 D51
REVISION 3, JUNE 1979

PART NUMBER
R6500/1

Rockwell

R6500 Microcomputer System
DATA SHEET

R6500/1 ONE-CHIP MICROCOMPUTER

INTRODUCTION

The Rockwell R6500/1 is a complete, high-performance 8-bit NMOS microcomputer on a single chip, and is totally upward/downward software compatible with all members of the R6500 family.

The R6500/1 consists of an R6502 CPU, an internal clock oscillator, 2048 bytes of Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and flexible interface circuitry. The interface circuitry includes a 16-bit programmable counter/latch with four operating modes, 32 bidirectional input/output lines (including two edge-sensitive lines), five interrupts and a counter I/O line.

PRODUCT SUPPORT

To allow prototype circuit development, Rockwell offers a PROM compatible 64-pin Emulator device. This device provides all R6500/1 interface lines plus routing the address bus, data bus, and associated control lines off the chip to be connected to external memory.

To facilitate system and program development for the R6500/1, Rockwell offers extensive product support. The SYSTEM 65 Microcomputer Development System with the R6500/1 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/1 Personality Module allows total system test and evaluation.

Regularly scheduled designer's courses are offered at regional centers.

The support products available are:

- SYSTEM 65 Microcomputer Development System — P/N S65-101
- 1 MHz R6500/1 Personality Module — P/N M65-081
- 2 MHz R6500/1 Personality Module — P/N M65-082
- 1 MHz R6500/1 Emulator Device — P/N R6500/1EC
- 2 MHz R6500/1 Emulator Device — P/N R6500/1EAC
- R6500/1 Evaluation Module — P/N PS01-D100

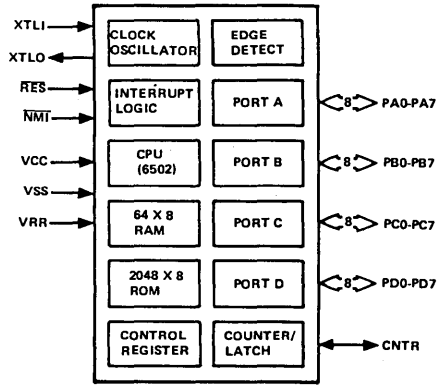
ORDERING INFORMATION

Order Number	Package Type	Frequency Option	Temperature Range
R6500/1P	Plastic	1 MHz	0°C to 70°C
R6500/1C	Ceramic	1 MHz	0°C to 70°C
R6500/1AP	Plastic	2 MHz	0°C to 70°C
R6500/1AC	Ceramic	2 MHz	0°C to 70°C
R6500/1PE	Plastic	1 MHz	−40°C to +85°C
R6500/1CE	Ceramic	1 MHz	−40°C to +85°C
R6500/1ACE	Ceramic	2 MHz	−40°C to +85°C

Note: The RC frequency option is available only in the 1 MHz R6500/1.

FEATURES

- R6502 CPU
  - Software upward/downward compatibility
  - Decimal or binary arithmetic modes
  - 13 addressing modes
  - True direct and indirect indexing
  - Memory addressable I/O
- 2048 x 8 mask programmable ROM
- 64 x 8 static RAM
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 bi-directional TTL compatible counter I/O line
- 16-bit programmable counter/latch with four modes
  - Interval Timer
  - Pulse Generator
  - Event Counter
  - Pulse Width Measurement
- Five Interrupts
  - Reset
  - Non-maskable
  - Two external edge sensitive
  - Counter
- 1 of 3 frequency references
  - Crystal
  - Clock
  - RC (resistor only)
- 4 MHz max crystal or clock external frequency
- 2 MHz or 1 MHz internal clock
- 1 µs minimum instruction execution
- N-channel, silicon gate, depletion load technology
- Single +5V power supply
- 500 mW operating power
- Separate power pin for RAM
- 40 pin DIP
- 64 pin PROM compatible Emulator device



Interface Diagram

R6500/1 ONE-CHIP MICROCOMPUTER

Specifications subject to change without notice

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING UNIT (CPU)

Clock Oscillator

The Clock Oscillator provides the basic timing signals used by the R6500/1 CPU. The reference frequency is provided by an external source, and can be from a crystal, clock or RC network input. The RC network mode is a mask option. The external frequency can vary from 200 kHz to 4 MHz. The internal Phase 2 (Ø2) frequency is one-half the external reference frequency. A 4.7K ohm resistor will provide nominal 2 MHz oscillation and 1 MHz internal operation in the RC mask option (±35%).

Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. Each data transfer which takes place between the registers is caused by decoding the contents of both the Instruction Register and Timing Control Logic.

Program Counter

The 16-bit Program Counter provides the addresses which step the CPU through sequential instructions in a program. The Program Counter is incremented each time an instruction or data is fetched from memory.

Instruction Register and Decode

Instructions fetched from memory are gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter).

Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers

There are two 8-bit index registers, X and Y. These registers can be used for general purpose storage, or as a displacement to modify the base address and thus obtain a new effective address. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer

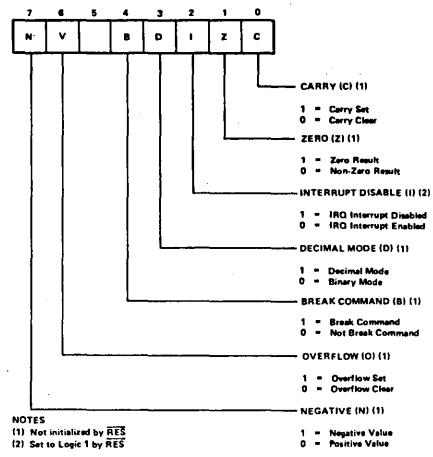
The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the CPU to perform stack manipulation under direction of either the program or interrupts $\overline{NMI}$ and $\overline{IRQ}$. The stack allows simple implementation of nested subroutines and multiple level interrupts.

Processor Status Register

The 8-bit Processor Status Register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The R6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of three conditions: Counter Overflow, PA0 Positive Edge Detected, and PA1 Negative Edge Detected.



Processor Status Register

MEMORY

2048 x 8 ROM

The 2048 byte Read-Only Memory (ROM) contains the program instructions and other fixed constants. These program instructions and constants are mask programmed into the ROM during fabrication of the R6500/1 device. The R6500/1 ROM is memory mapped from 800 to FFF.

64 x 8 RAM

The 64 byte Random Access Memory (RAM) is used for read/write memory during system operation, and contains the stack. This RAM is completely static in operation and requires no clock or dynamic refresh. A standby power pin, VRR, allows RAM memory to be maintained on 10% of the operating power in the event that VCC power is lost.

In order to take advantage of efficient zero page addressing capabilities, the RAM is assigned memory addresses 0 to 03F.

INPUT/OUTPUT

Bidirectional I/O Ports

The R6500/1 provides four 8-bit input/output ports (PA, PB, PC, and PD). Associated with the I/O ports are four 8-bit registers located on page zero. See the system memory map for specific addresses. Each I/O line is individually selectable as an input or an output without line grouping or port association restrictions.

An internal active transistor drives each I/O line to the low state. An internal passive resistance pulls the I/O lines to the high state, eliminating the need for external pull-up resistors.

An option is available to delete the internal pull-up resistance on 8-bit port groups or on the CNTR line at mask time. This option is employed to permanently assign an 8-bit port group to input functions, to interface with CMOS drivers, or to interface with external pull-up devices.

Inputs

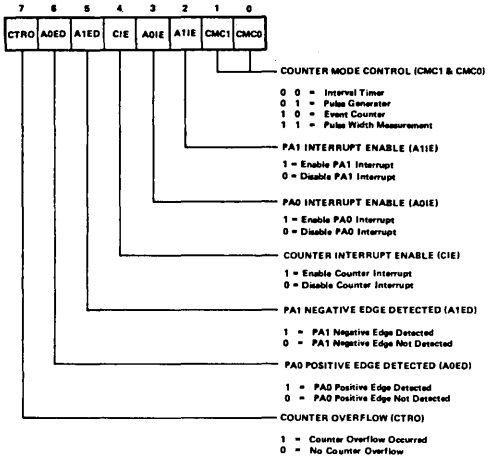
Inputs are enabled by setting the appropriate bit of the I/O port to the high state (Logic 1). A low input signal causes a logic 0 to be read. A high input signal causes a logic 1 to be read. $\overline{RES}$ loads Logic 1 into the I/O ports, thereby initializing all I/O lines as inputs.

Outputs

Outputs are set by loading the desired bit pattern into the corresponding I/O ports. A Logic 1 selects a high output; a Logic 0 selects a low output.

CONTROL REGISTER

The Control Register (CR) controls four Counter operating modes and three maskable interrupts. It also reports the status of three interrupt conditions. There are five control bits and three status bits. The control bits are set to Logic 1 or cleared to Logic 0 by writing the desired state into the respective bit positions. The Control Register is cleared to Logic 0 by the occurrence of $\overline{RES}$.



Control Register

EDGE DETECT CAPABILITY

There is an asynchronous edge detect capability on two of the Port A I/O lines. This capability exists in addition to and independently from the normal Port A I/O functions. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. The edge detect logic is continuously active. Each edge detect signal is associated with a maskable interrupt.

PA0 Positive Edge Detection

A positive (rising) edge is detectable on PA0. When this edge is detected, the PA0 Positive Edge Detected bit – Bit 6 in the Control Register – is set to Logic 1. When both this bit and the PA0 Interrupt Enable Bit – Bit 3 of the Control Register – are set to Logic 1, an IRQ interrupt request is generated. The PA0 Positive Edge Detected bit is cleared by writing to address 089.

PA1 Negative Edge Detection

A negative (falling) edge is detectable on PA1. When this edge is detected, the PA1 Negative Edge Detected bit – Bit 5 of the Control Register – is set to Logic 1. When both this bit and the PA1 Interrupt Enable bit – Bit 2 of the Control Register – are set to Logic 1, an $\overline{IRQ}$ interrupt request is generated. The PA1 Negative Edge Detected bit is cleared by writing to address 08A.

COUNTER/LATCH

The Counter/Latch consists of a 16-bit decrementing Counter and a 16-bit Latch. The Counter is comprised of two 8-bit registers. Address 086 contains the Upper Count (UC) and address 087 contains the Lower Count (LC). The Counter counts either $\phi 2$ clock periods or occurrences of an external event, depending on the selected counter mode. The UC and LC can be read at any time without affecting counter operation.

The Latch contains the Counter preset value. The Latch consists of two 8-bit registers. Address 084 contains the Upper Latch (UL) and address 085 contains the lower latch (LL). The 16-bit Latch can hold a count from 0 to 65,535. The Latch can be accessed as two write-only memory locations.

The Latch registers can be loaded at any time by storing into UL and LL. The UL can also be loaded by writing into address 088.

The Counter can be preset at any time by writing to address 088. Presetting the Counter in this manner causes the contents of the accumulator to be stored into the UL before the 16-bit value in the Latch (UL and LL) is transferred in the Counter (UC and LC).

The Counter is preset to the Latch value when the Counter overflows. When the counter decrements from 0000, Counter overflow occurs causing the next counter value to be the Latch value, not FFFF.

When the Counter overflows, Counter Overflow bit – Bit 7 of the Control Register – is set to Logic 1. When both this bit and the Counter Interrupt Enable bit – Bit 4 of the Control Register – are set, an $\overline{IRQ}$ interrupt request is generated. The Counter Overflow bit in the Control Register can be examined in an $\overline{IRQ}$ interrupt service routine to determine that the $\overline{IRQ}$ was generated by Counter overflow.

The Counter Overflow bit is cleared when the LC is read or Counter preset is performed by writing into address 088.

COUNTER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

Mode	CMC 1	CMC 0
Interval Timer	0	0
Pulse Generator	0	1
Event Counter	1	0
Pulse Width Measurement	1	1

The Interval Timer, Pulse Generator, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In this mode the Counter is free running and decrements at the $\phi 2$ clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

The CNTR line is held in the high state.

Pulse Generator (Mode 1)

In this mode the Counter is free running and decrements at the $\phi 2$ clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

The CNTR line toggles from one state to the other when Counter overflow occurs. Writing to address 088 will also toggle the CNTR line.

A symmetric or asymmetric output waveform can be generated on the CNTR line in this mode. A one-shot waveform can easily be generated by changing from Mode 1 to Mode 0 after only one occurrence of the output toggle condition.

Event Counter (Mode 2)

In this mode the CNTR line is used as an event input line. The Counter decrements each time a rising edge is detected on CNTR. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

Pulse Width Measurement (Mode 3)

This mode allows the accurate measurement of the duration of a low state on the CNTR line. The Counter decrements at the $\phi 2$ clock rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state. If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device will cause the CNTR input to be in the high state.

RESET CONSIDERATIONS

The occurrence of $\overline{RES}$ going from low to high causes initialization of various conditions in the R6500/1. All of the I/O ports (PA, PB, PC, and PD) and CNTR are forced to the high (Logic 1) state. All bits of the Control Register are reset to Logic 0, causing the Interval Timer Mode (Mode 0) to be selected and all interrupt enabled bits to be cleared. Neither the Latch nor the Counter registers are initialized by $\overline{RES}$. The Interrupt Disable bit in the CPU Processor Status Register is set and the program starts execution at the address contained in the Reset Vector location.

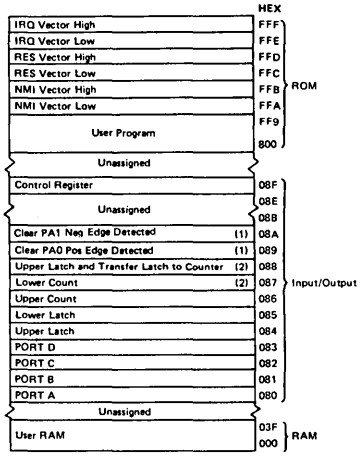
TEST LOGIC

Special test logic provides a method for thoroughly testing the R6500/1. Applying a +10V signal to the $\overline{RES}$ line places the R6500/1 in the test mode. While in this mode, all memory fetches are made from Port PC. External test equipment can use this feature to test internal CPU logic and I/O. A program can be loaded into RAM allowing the contents of the instruction ROM to be dumped to any port for external verification.

All R6500/1 microcomputers are tested by Rockwell using this feature.

MEMORY ADDRESSABLE I/O

The I/O ports, registers, and commands are treated as memory and are assigned specific addresses. See the system memory map for the addresses. This I/O technique allows the full set of CPU instructions to be used in the generation and sampling of I/O commands and data. When an instruction is executed with an I/O address and appropriate R/$\overline{W}$ state, the corresponding I/O function is performed.

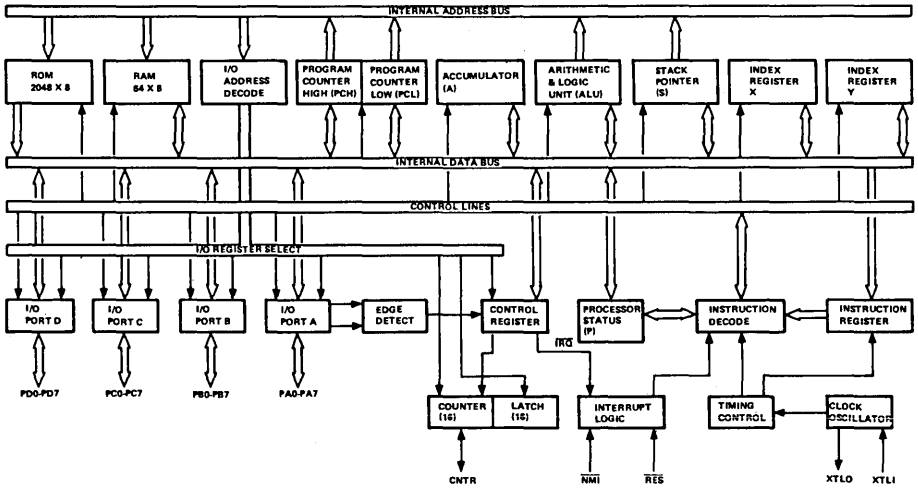


Notes:
(1) I/O command only; i.e., no stored data.
(2) Clears Counter Overflow – Bit 7 in Control Register.

System Memory Map

SIGNAL DESCRIPTIONS

SIGNAL NAME	PIN NO.	DESCRIPTION
VCC	30	Main power supply +5V
VRR	1	Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data.
VSS	12	Signal ground
XTLI	10	Crystal, clock or RC network input for internal clock oscillator.
XTLO	11	Crystal or RC network output from internal clock oscillator.
$\overline{RES}$	39	The Reset input is used to initialize the R6500/1. This signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized. +10V input enables the test mode.
$\overline{NMI}$	40	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	38-31 29-22 20-13 9-2	Four 8-bit ports used for either input/output. Each line consists of an active transistor to VSS and a passive pull-up to +5V. The two lower bits of the PA port (PA0 and PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	21	This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes.



R6500/1 Block Diagram

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

ADDRESSING MODES

ACCUMULATOR ADDRESSING – This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING – In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING – In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits.

ZERO PAGE ADDRESSING – The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING – In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

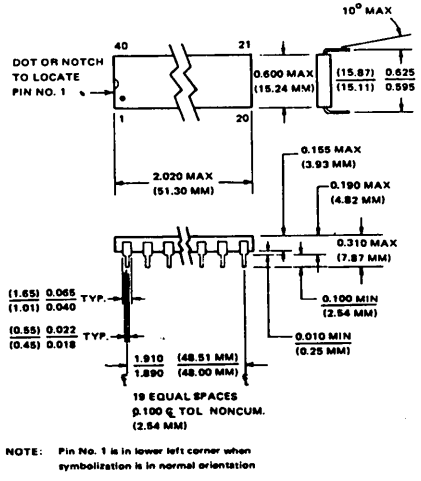
RELATIVE ADDRESSING – Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING – In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

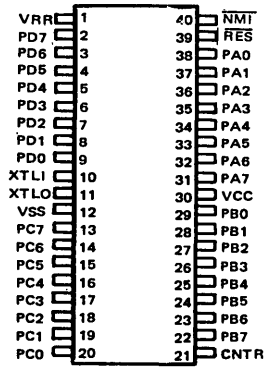
INDIRECT INDEXED ADDRESSING – In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT – The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.



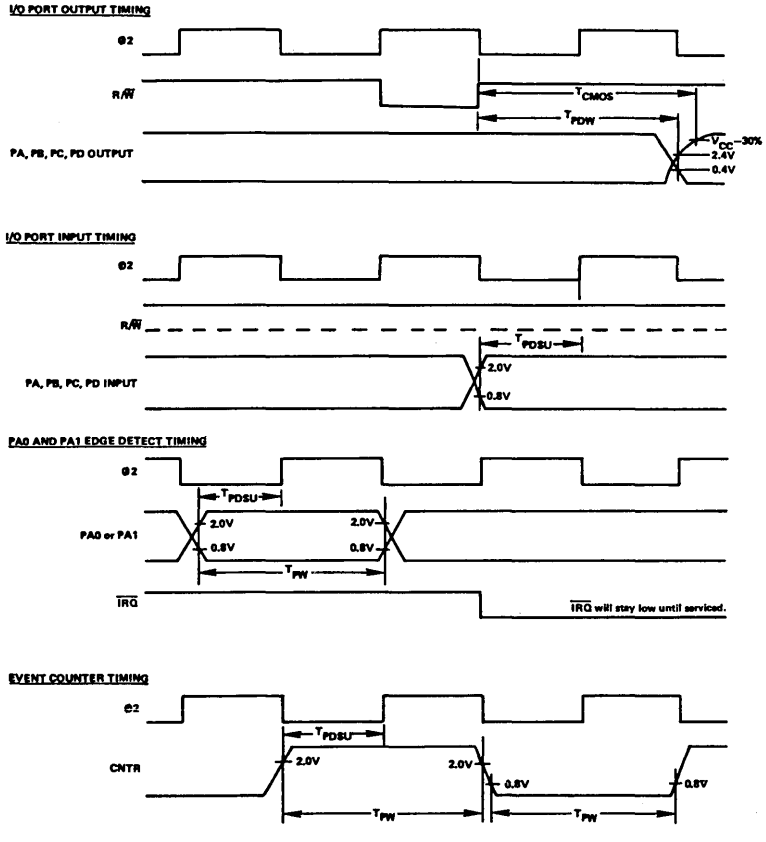
NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

Packaging Diagram



Pin Configuration

TIMING CHARACTERISTICS



SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Storage Temperature Range	T_{stg}	-55 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Static D.C. Characteristics (V_{CC} = 5V ±10% for R6500/1, V_{CC} = 5V ±5% for R6500/1A)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High)	P_D				mW
0°C to +70°C		–	500	–	
-40°C to +85°C		–	550	–	
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	–	V_{CC}	Vdc
RAM Standby Current (Retention Mode)	I_{RR}				mAdc
0°C to +70°C		–	10	–	
-40°C to +85°C		–	12	–	
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	–	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	–	+0.8	Vdc
Input Leakage Current	I_{IN}				µAdc
V_{in} = 0 to 5.0 Vdc $\overline{RES}$, $\overline{NMI}$			±1.0	±2.5	
Input High Voltage (XTLI)	V_{IHXT}	+4.0	–	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	-0.3	–	+0.8	Vdc
Input Low Current (V_{IL} = 0.4 Vdc)	I_{IL}	–	-1.0	-1.6	mAdc
Output High Voltage (V_{CC} = min, I_{Load} = -100 µAdc)	V_{OH}	-2.4	–	–	Vdc
Output High Voltage (V_{CC} = min)	V_{CMOS}	V_{CC} - 30%	–	–	Vdc
Output Low Voltage (V_{CC} = min, I_{Load} = 1.6 mAdc)	V_{OL}	–	–	+0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 Vdc)	I_{OH}	-100		–	µAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	–	–	mAdc
Input Capacitance (V_{in} - 0, T_A = 25°C, f = 1.0 MHz)	C_{in}				pF
PA, PB, PC, PD, CNTR		–	–	10	
XTLI, XTLO		–	–	50	
Output Capacitance (V_{in} - 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	10	pF
I/O Port Resistance PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, CNTR	R_L	3.0	6.0	11.5	KΩ

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC Characteristics (V_{CC} = 5V ±10% for R6500/1, V_{CC} = 5V ±5% for R6500/1A)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	µsec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		µsec
Internal Write to Peripheral Data Valid (CMOS)	T_{CMOS}	2.0		1.0		µsec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		µsec

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← 7 6 5 4 3 2 1 0 ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2								• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2								• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2								• • • • • • • •	BEQ
BIT	A ∧ M				2C	4	3	24	3	2																																M7 M6 • • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2								• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2								• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2								• • • • • • • •	BPL
BRK	BREAK													00	7	1																									• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2								• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2								• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • •	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																															N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																															N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																			• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → 7 6 5 4 3 2 1 0 → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	7 6 5 4 3 2 1 0 ← C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	C → 7 6 5 4 3 2 1 0				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									• • • • • • • •	RTS
SBC	A − M − C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	F0	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																														96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																	• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													98	2	1																									N • • • • • Z •	TYA

(1) ADD 1 to "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE, Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

+ ADD
− SUBTRACT
∧ AND
∨ OR
∀ EXCLUSIVE OR

M7 MEMORY BIT 7
M6 MEMORY BIT 6
n NO. CYCLES
NO. BYTES

DOCUMENT NO. 29000D51S
REV. 1, APRIL 1979

PART NUMBER
R6500/1E

Rockwell

R6500 Microcomputer System DATA SHEET SUPPLEMENT

R6500/1E EMULATOR DEVICE

INTRODUCTION

To aid in designing R6500/1 microcomputer systems, Rockwell has developed a PROM compatible, 64-pin, R6500/1E Emulator device. The architecture of the Emulator device is basically the same as the R6500/1 except that the address, data, and associated control lines are routed off the chip for connection to an external memory.

The functions and operation of the Emulator device are identical to the R6500/1 with only some minor differences, described herein. The R6500/1 data sheet (Document No. 2900D51) contains the description of R6500/1 and R6500/1 common interface signals and functions.

ORDERING INFORMATION

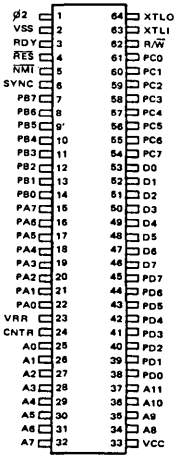
Order Number	Package Type	Frequency Option	Temperature Range
R6500/1EC	Ceramic	1 MHz	0°C to 70°C
R6500/1EAC	Ceramic	2 MHz	0°C to 70°C

SIGNAL DESCRIPTIONS

All R6500/1 interface signals are provided in the Emulator device. While the Emulator pin assignments are different from the R6500/1 in order to accommodate the 64-pin Emulator package, the interface electrical characteristics are identical. The Emulator device provides 24 additional signals to route the address bus (12 lines), the data bus (8 lines), and control signals (4 lines) off the chip for connection to external memory.

MEMORY MAP

An additional 1024 bytes of memory (400-7FF) are addressable in the Emulator device to support software development.



R6500/1E Pin Configuration

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock — the RC option is not available in the Emulator device.

I/O PORT PULLUPS

The R6500/1E has the internal I/O port pullup resistance only.

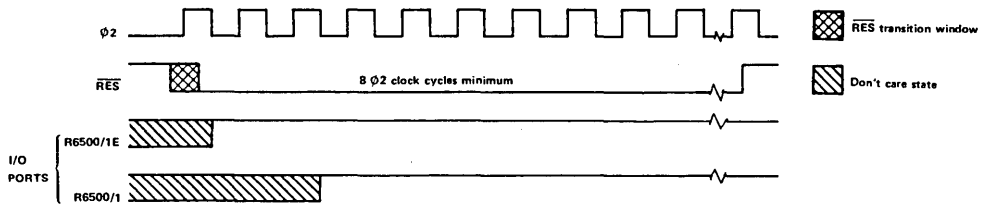
R6500/1E DEVICE ADDITIONAL SIGNALS

Signal Name	Pin No.	Description
R/$\overline{W}$	62	Read/Write. The Read/Write output controls the direction of data transfer between the R6500/1E Emulator CPU and external memory. This line is high when reading data from memory and low when writing data to memory.
RDY	3	Ready. The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on any cycle except a write cycle. A negative transition to the low state during the φ2 clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent φ2 clock pulse in which the RDY line is low.
SYNC	6	Sync. The Sync signal is provided to identify those cycles in which the CPU is performing an OP CODE fetch. SYNC goes high during φ2 clock-low pulse during an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the φ2 clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.
φ2	1	Phase 2 (φ2) clock pulse. Data transfer can take place only during φ2 clock pulse.
A0-A11	25-32 34-37	Address Bus Lines. The address bus buffers on the R6500/1E are push/pull type drivers capable of driving at least 130 pf and one standard TTL load. The address bus always contains known data. The addressing technique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O addresses are also placed on these lines.
D0-D7	53-46	Data Bus Lines. All transfers of instructions and data between the CPU and external memory take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.

Specifications subject to change without notice

R6500/1E I/O PORT INITIALIZATION

Ports A, B, C and D and the CNTR line in R6500/1E are initialized to the logic high state two $\phi 2$ clock cycles earlier than in the R6500/1. It is still required, however, that the $\overline{RES}$ line to the R6500/1E be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range.



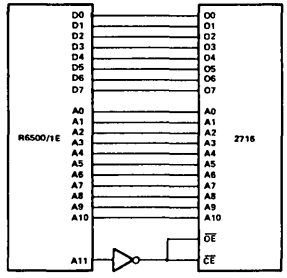
TYPICAL R6500/1E PROGRAM MEMORY INTERCONNECTIONS

Shown below are two typical connections between the R6500/1E and program memory (in this case, type 2716 and 2708 PROMS). Example 1 shows a connection to a 2K 2716 PROM. Since the R6500/1 has a 2K ROM capacity, the contents of the PROM could be masked directly into the production R6500/1 ROM.

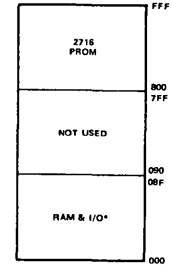
Example 2 shows a connection to 3K of 2708 PROMS. The extra 1K PROM allows expanded or additional programs be used during R6500/1 firmware development. The production program, however, must be reduced to 2K maximum (between addresses 800 and FFF) before committing to R6500/1 ROM.

EXAMPLE 1: R6500/1E Connected to One 2716 PROM (2K Bytes)

Connection Diagram

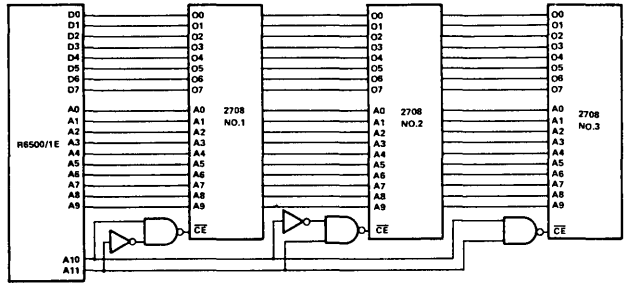


Memory Map

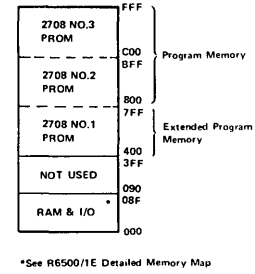


EXAMPLE 2: R6500/1E Connected to Three PROMS (3K Bytes)

Connection Diagram



Memory Map



*See R6500/1E Detailed Memory Map

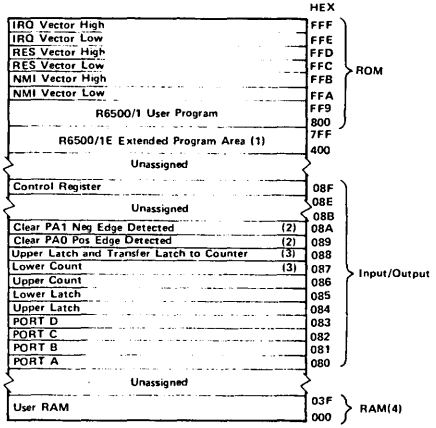
Truth Table

Address		PROM Select			
A11	A10	2708 No. 3 $\overline{CE}$	2708 No. 2 $\overline{CE}$	2808 No. 1 $\overline{CE}$	Selected Address Range
0	0	1	1	1	000-3FF
0	1	1	1	0	400-7FF
1	0	1	0	1	800-BFF
1	1	0	1	1	C00-FFF

R6500/1 EMULATOR DEVICE TIMING

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
R/$\overline{W}$ setup time from CPU	T_{RWS}		300		200	ns
Address setup time from CPU	T_{ADS}		300		200	ns
Memory read access time	T_{ACC}		525		225	ns
Data stabilization time	T_{DSU}	150		75		ns
Data hold time — Read	T_{HR}	10		10		ns
Data hold time — Write	T_{HW}	30		30		ns
Data delay time from CPU	T_{MDS}		200		150	ns
RDY setup time	T_{RDY}	100		50		ns
SYNC delay time from CPU	T_{SYNC}		350		175	ns
Address hold time	T_{HA}	30		30		ns
R/$\overline{W}$ hold time	T_{HRW}	30		30		ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

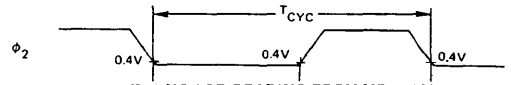
R6500/1E DETAILED MEMORY MAP



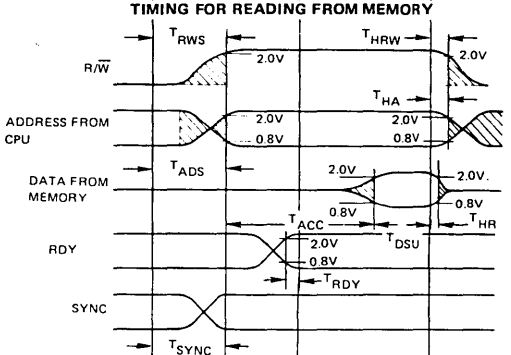
NOTES
(1) Additional 1024 bytes are decoded for external memory addressing by the R6500/1E Emulator Device. This area can be used during debug, but cannot be used in a masked ROM R6500/1.
(2) I/O command only; i.e., no stored data.
(3) Clears Counter Overflow — Bit 7 in Control Register
(4) CAUTION: The R6500/1E allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however allows RAM mapping only at 000-03F.

R6500/1E TIMING DIAGRAMS

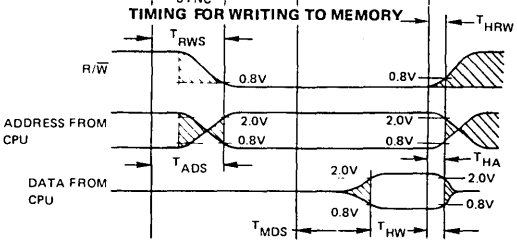
PHASE 2 ($\phi 2$) TIMING REFERENCE



TIMING FOR READING FROM MEMORY



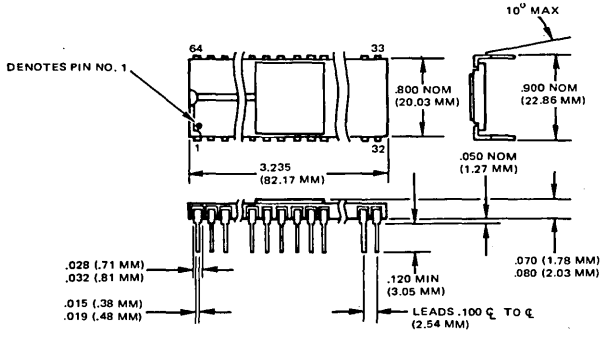
TIMING FOR WRITING TO MEMORY



ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7, RDY,	V_{IHT}	V_{SS} + 2.4	–	–	Vdc
Input Low Threshold Voltage D0-D7, RDY,	V_{ILT}	–	–	V_{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V_{CC} = 5.25V) D0-D7	I_{TSI}	–	–	10	μA
Output High Voltage (I_{LOAD} = 100μ Adc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, φ2	V_{OH}	V_{SS} + 2.4	–	-	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, φ2	V_{OL}	–	–	V_{SS} + 0.6	Vdc
Power Dissipation	P_D	–	0.75	1.20	W
Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz) RDY D0-D7 A0-A11, R/$\overline{W}$, SYNC φ2	C C_{in} C_{out} $C_{\phi 2}$	 – – – –	 – – – 50	 10 15 12 80	pF
I/O Port Pull-up Resistance	R_L	3.0	6.0	11.5	kohm



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

Packaging Diagram

DOCUMENT NO. 29000 D60
FEBRUARY, 1980

PART NUMBER
R6500/1EB

Rockwell

R6500 Microcomputer System
DATA SHEET

R6500/1EB BACKPACK EMULATOR

INTRODUCTION

The Rockwell R6500/1EB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/1 one-chip microcomputer. Like the R6500/1, the R6500/1EB is totally upward/downward compatible with all members of the R6500 family. The R6500/1EB is designed to accept standard 5-volt, 24-pin PROMs, EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, re-programmed, then reinserted as often as desired.

The R6500/1EB has the same pinouts as the masked-ROM R6500/1 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/1, with some minor differences (described herein). The R6500/1 Microcomputer Data Sheet (Rockwell Document No. 29000D51) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/1 provides 2K bytes of read-only memory, the R6500/1EB will address 3K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

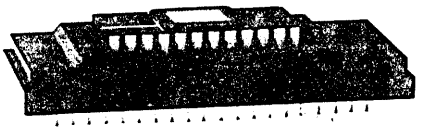
ORDERING INFORMATION

ORDER NUMBER	MEMORY CAPACITY	COMPATIBLE MEMORIES	TEMPERATURE RANGE
R6500/1EB-1	2K	2716,2516, 82S2708, 2316B	0°C to 70°C
R6500/1EB-2	3K	2532,2332, 82S2708	0°C to 70°C
R6500/1EB-3	3K	2732, 82S2708	0°C to 70°C
R6500/1EB-4	1K	2758, 82S2708	0°C to 70°C

PRODUCT SUPPORT

The R6500/1EB Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/1. Additional support products include the R6500/1E, a 64-pin emulator device with interface lines for connecting external memory. Another support product is the R6500/1 Evaluation Module, which has 40 R6500/1-compatible pins and provision for inserting external memory.

Further, the SYSTEM 65 Microcomputer Development System with R6500/1 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/1 Personality Module allows total system test and evaluation. With the optional PROM Programmer, SYSTEM 65 can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 2K ROM of the R6500/1. In addition to support products, Rockwell offers regularly-secheduled designers courses at regional centers.



The available support products include:

- SYSTEM 65 Microcomputer Development System — P/N S65-101
- PROM Programmer Module — P/N M65-040
- 1-MHz R6500/1 Personality Module — P/N M65-081
- 2-MHz R6500/1 Personality Module — P/N M65-082
- 1-MHz R6500/1 Emulator Device — P/N R6500/1EC
- 2-MHz R6500/1 Emulator Device — P/N R6500/1EAC
- R6500/1 Evaluation Module — P/N M65-089

FEATURES

- PROM version of the R6500/1
- Completely pin compatible with R6500/1 single-chip microcomputers
- Profile approaches 40 pin DIP of R6500/1
- Accepts 5 volt, 24 pin industry-standard EPROMs, PROMs, ROMs
  - 4K memories – 2532, 2732, 2332 (3K bytes addressable)
  - 2K memories – 2716, 2516, 2316B
  - 1K memories – 2758, 82S2708
- Use as prototyping tool or for low volume production
- 3K bytes of memory capacity (1K, 2K, 4K memories)
- 64 x 8 static RAM
- Separate power pin for RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 bi-directional TTL compatible counter I/O line
- 16 bit programmable counter/latch with four modes (interval timer, pulse generator, event counter, pulse width measurement)
- 5 interrupts (reset, non-maskable, two external edge sensitive, counter)
- Crystal or extenal time base
- Single +5V power supply

R6500/1EB CONFIGURATIONS

The R6500/1EB is available in four different versions, to accommodate various 24-pin 1K-, 2K- and 4K-memories. All four versions provide 64 bytes of RAM and I/O, as well as 24 signals to support the external memory "backpack" socket. The 24 backpack signals differ somewhat between versions (due to memory pin differences) but always consist of the address bus (12 lines), the data bus (8 lines) and the $\overline{OE}$, Vcc, Vrr and Vss signals (one line each). See Interface Diagram.

The external memories must always occupy the upper 1K of available memory (addresses 800 through FFF) for implementation of interrupt vectors. See Memory Map. The R6500/1EB provides a read block to the external memory where internal RAM or I/O are located at the same addresses as that occupied by external memory.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock — the RC option is not available in the emulator device.

I/O PORT PULLUPS

The R6500/1EB has the internal I/O port pullup resistance only.

TEST MODE DELETED

The test mode of the R6500/1 is not available on the R6500/1EB.

R6500/1EB I/O PORT INITIALIZATION

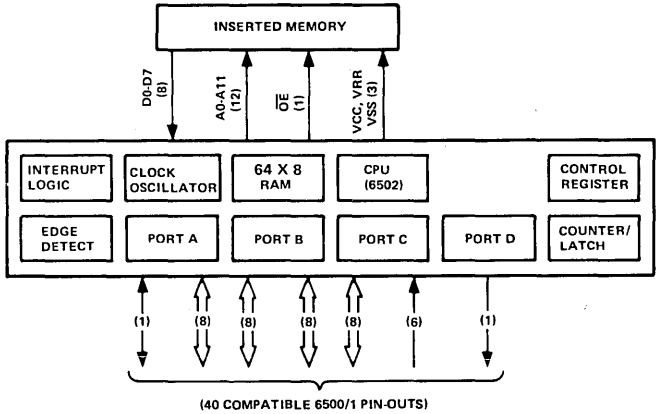
Ports A, B, C, and D and the CNTR line in the R6500/1EB are initialized to the logic high state two Ø2 clock cycles earlier than in the R6500/1. The $\overline{RES}$ line to the R6500/1EB must, however, still be held low for at least eight Ø2 clock cycles after Vcc reaches operating range. See timing diagram.

RAM MAPPING

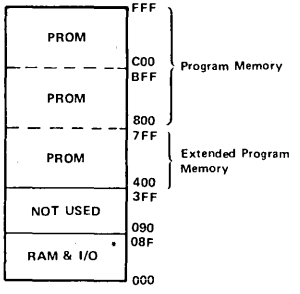
The R6500/1EB allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F and 340-37F, as well as 000-03F. The production R6500/1, however, allows RAM mapping only at 000-03F. This means that a write to location 40, for example, will write to location 0 in the R6500/1EB, and to invalid RAM in the R6500/1 production port.

R6500/1EB BACKPACK MEMORY SIGNAL DESCRIPTIO.

SIGNAL NAME	PIN NO.	DESCRIPTION
D0-D7	9S-11S, 13S-17S	Data Bus LInes. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition
A0-A9	1S-8S, 23S,24S	Address Bus LInes. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
A10	19S	Address Bus Line 10. This address line has the same characteristics and functions as Lines A0-A9. However, in the R6500/1EB-4, pin 19S is tied to Vss instead of to the address bus.
A11	18S+21S	Address Bus Line 11. This address line has the same characteristics and function as Lines A0-A9. In the R6500/1EB-1 and -4 versions, A11 is inverted by a standard TTL inverter before reaching pin 18S. In the R6500/1EB-2, A11 is connected directly to pin 18S. In the R6500/1EB-3, A11 is routed to pin 21S and pin 18S is tied to Vss.
$\overline{OE}$	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by the R/$\overline{W}$ signal from the CPU and then inverted by a standard TTL inverter, to form $\overline{OE}$.
Vcc	24S	Main Power Supply +5V. This pin is tied directly to pin 30 (Vcc).
Vpp	21S	Main Power Supply +5V. This pin is tied directly to pin 30 (Vcc), except in the R6500/1EB-3, where it is tied to A11. During backup power, power is supplied only to the RAM memory, and not to the PROMs.
Vss	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 12 (Vss).



R6500/1EB Interface Diagram

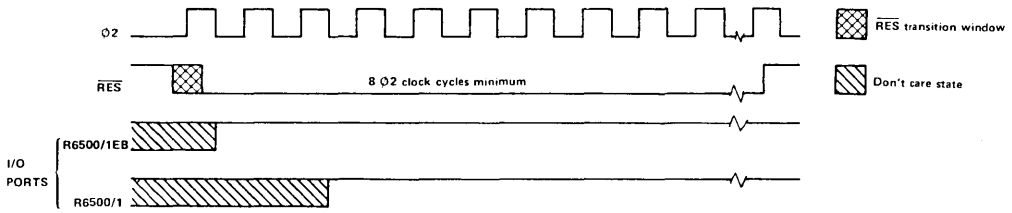


*See R6500/1EB Detailed Memory Map

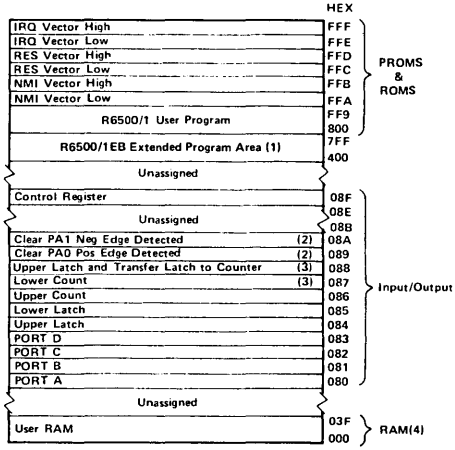
Memory Map

R6500/1EB DEVICE TIMING

Signal	Symbol	1 MHz Min.	1 MHz Max.	Unit
$\overline{OE}$ setup time from CPU	T_{OES}		300	ns
Address setup time from CPU	T_{ADS}		300	ns
Memory read access time	T_{ACC}		525	ns
Data stabilization time	T_{DSU}	150		ns
Data hold time – Read	T_{HR}	10		ns
Address hold time	T_{HA}	30		ns
$\overline{OE}$ hold time	T_{HOE}	30		ns
Cycle Time	T_{CYC}	1.0	10.0	μs

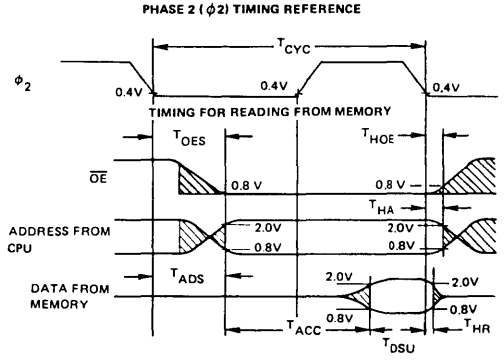


R6500/1EB I/O Port Initialization Timing Diagram



NOTES
(1) Additional 1024 bytes are decoded for external memory addressing by the R6500/1EB Emulator Device. This area can be used during debug, but cannot be used in a masked ROM R6500/1.
(2) I/O command only; i.e., no stored data.
(3) Clears Counter Overflow – Bit 7 in Control Register
(4) CAUTION: The R6500/1EB allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however allows RAM mapping only at 000-03F.

R6500/1EB Detailed Memory Map

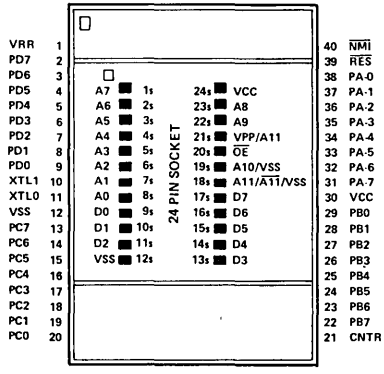


R6500/1EB Timing Diagram

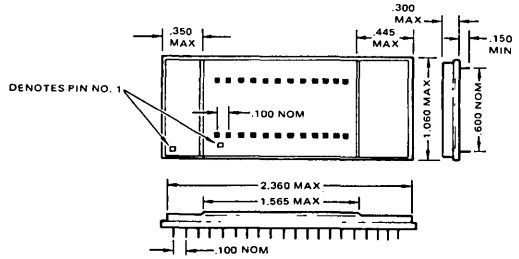
ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ±5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7	V_{IHT}	V_{SS} + 2.4	–	–	Vdc
Input Low Threshold Voltage D0-D7	V_{ILT}	–	–	V_{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V_{CC} = 5.25V) D0-D7	I_{TSI}	–	–	10	μA
Output High Voltage (I_{LOAD} = 100μ Adc, V_{CC} = 4.75V) D0-D7, A0-A11, $\overline{OE}$	V_{OH}	V_{SS} + 2.4	–	–	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V) D0-D7, A0-A11, $\overline{OE}$	V_{OL}	–	–	V_{SS} + 0.6	Vdc
Power Dissipation	P_D	–	0.80	1.30	W
Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz) D0-D7 A0-A11	C C_{in} C_{out}	– –	– –	15 12	pF
I/O Port Pull-up Resistance	R_L	3.0	6.0	11.5	kohm



R6500/1EB Pin Configuration



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

Packaging Diagram

PART NUMBER
R6500/1-11

R6500 Microcomputer System
PRODUCT PREVIEW

R6500/1-11 ONE-CHIP MICROCOMPUTER

INTRODUCTION

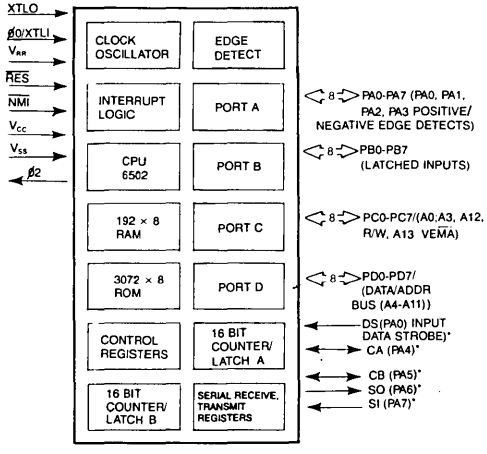
The Rockwell R6500/1-11 is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip, and is compatible with all members of the R6500 family.

The R6500/1-11 consists of an enhanced 6502 CPU, an internal clock oscillator, 3072 bytes of Read-Only Memory, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

DEVELOPMENT SUPPORT

To allow prototype circuit development, Rockwell offers a PROM-compatible 64-pin Emulator device. This device, the R6500/2-11, provides all R6500/1-11 interface lines, plus the address bus, data bus and control lines to interface with external memory. The R6500/2-11 may also be used as a CPU-RAM-I/O counter device in multichip systems.

Rockwell supports development of the R6500/1-11 with the System 65 Microcomputer Development System and the R6500/1-11 Personality Module. Complete in-circuit emulation with the R6500/1-11 Personality Module allows total system test and evaluation.



*MULTIPLEXED FUNCTION PINS (Software Selectable)

Interface Diagram

FEATURES

- Enhanced 6502 CPU
  - —Four new instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 3K-byte mask-programmable ROM
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - —Pulse measurement
  - —Pulse generation
  - —Interval timer
  - —Event counter
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Synchronous shift register mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Programmable bit rates to 62.5 bits/sec (@ 2 MHz)
- Four edge-sensitive lines; two positive, two negative
- Ten interrupts
  - —Reset
  - —Non-maskable
  - —Four external, edge-sensitive
  - —Two counter
  - —Serial data received
  - —Serial data transmitted
- Bus expandable to 16K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at two or four times internal frequency
  - —External clock input divided by one, two or four
- 1 μs minimum instruction execution time
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 16 mW stand-by power for 32 bytes of the 192-byte RAM
- 40-pin DIP

Specifications subject to change without notice
Document No. 29000 D64
Rev. 1, October 1980

ELECTRICAL SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial Industrial	T	0 to +70 −40 to +85	°C
Storage Temperature Range	T_{sts}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D. C. Characteristics (V_{CC} = 5V ±5% V_{SS} = 0)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High) Commercial @ 25°C Industrial @ 25°C	P_D	 — —		 1000 1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C Industrial @ 25°C	I_{RR}	 — —	 4 5.2	 — —	mAdc
Input High Voltage (Except XTLI)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current (RES, NMI) V_{in} = 0 to 5.0 Vdc	I_{IN}		 ±1.0	 ±2.5	μAdc
Input Low Current PA, PB, PC, PD (V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage Except XTLO (I_{Load} = .100 μAdc)	V_{OH}	+2.4	—	—	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance (V_{in}-0, T_A = 25°C, 1=1.0 MHz) PA, PB, PC, PD XTLI, XTLO	C_{in}	 — —	 — —	 10 50	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	R_L	3.0	6.0	11.5	KΩ

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC Characteristics (V_{CC} = 5V ±5% V_{SS} = 0)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	μ sec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		μ sec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		μ sec

PART NUMBER
R6500/1-11Q

Rockwell

R6500 Microcomputer System
PRODUCT PREVIEW

R6500/1-11Q ONE-CHIP MICROCOMPUTER

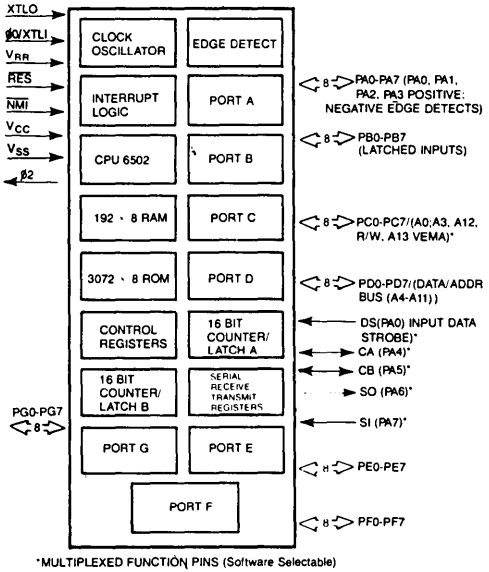
INTRODUCTION

The Rockwell R6500/1-11Q is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip, and is compatible with all members of the R6500 family.

The R6500/1-11Q consists of an enhanced 6502 CPU, an internal clock oscillator, 3072 bytes of Read-Only Memory, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 56 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

DEVELOPMENT SUPPORT

To allow prototype circuit development, Rockwell offers a PROM-compatible 64-pin Emulator device. This device, the R6500/2-11, provides all R6500/1-11Q interface lines (except Ports E, F and G), plus the address bus, data bus and control lines to interface with external memory. The R6500/2-11 may also be used as a CPU-RAM-I/O counter device in multichip systems.



*MULTIPLEXED FUNCTION PINS (Software Selectable)

Interface Diagram

Rockwell supports development of the R6500/1-11Q with the System 65 Microcomputer Development System and the R6500/1-11 Personality Module. Complete in-circuit emulation with the R6500/1-11Q Personality Module allows total system test and evaluation.

FEATURES

- Enhanced 6502 CPU
  - —Four new instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 3K-byte mask-programmable ROM
- 192-byte static RAM
- 56 bidirectional, TTL-compatible I/O lines (seven ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port has Darlington drive capability
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - —Pulse measurement
  - —Pulse generation
  - —Interval timer
  - —Event counter
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Synchronous shift register mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Programmable bit rates to 62.5 bits/sec (@ 2 MHz)
- Four edge-sensitive lines; two positive, two negative
- Ten interrupts
  - —Reset
  - —Non-maskable
  - —Four external, edge-sensitive
  - —Two counter
  - —Serial data received
  - —Serial data transmitted
- Bus expandable to 16K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at two or four times internal frequency
  - —External clock input divided by one, two or four
- 1 μs minimum instruction execution time
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 16 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP

Specifications subject to change without notice
Document No. 29000 D65
Rev. 1, October 1980

ELECTRICAL SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{In}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial Industrial	T	0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. Characteristics (V_{CC} = 5V ±5% V_{CC} = 0)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High) Commercial @ 25°C Industrial @ 25°C	P_D	— —		1000 1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C Industrial @ 25°C	I_{RR}	— —	4 5.2	— —	mAdc
Input High Voltage (Except XTLI)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current (RES, NMI) V_{In} = 0 to 5.0 Vdc	I_{IN}		±1.0	±2.5	μAdc
Input Low Current PA, PB, PC, PD, PF, and PG (V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage Except XTLO (I_{Load} = .100 μAdc)	V_{OH}	+2.4	—	—	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Darlington Current Drive, PE0~PE7 (V_o = 1.5 Vdc)	I_{OH}	−1.0	—	—	mAdc
Output Low Voltage, PE0~PE7 (I_{Load} = 10 mAdc sink)	V_{OL}	—	—	1.0	Vdc
Input Capacitance (V_{In}-0, T_A = 25°C, f = 1.0 MHz) PA, PB, PC, PD, PF, and PG XTLI, XTLO	C_{in}	 — —	 — —	 10 50	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, PF0-PF7 & PG0-PG7	R_L	3.0	6.0	11.5	KΩ

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC Characteristics (V_{CC} = 5V ±5% V_{SS} = 0)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	μ sec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		μ sec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		μ sec

PART NUMBER
R6500/2-11

Rockwell

R6500 Microcomputer System
PRODUCT PREVIEW

R6500/2-11 EXTENDED MICROPROCESSOR

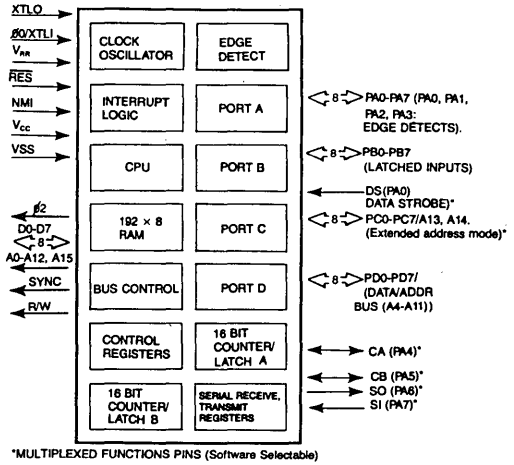
INTRODUCTION

The Rockwell R6500/2-11 is a CPU-I/O-RAM-counter/timer device on a single chip. Interfacing it with external memory makes a powerful two-chip microcomputer system. The R6500/2-11 features an enhanced 6502 instruction set that is software-compatible with all members of the R6500 family.

The R6500/2-11 consists of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel and ten interrupts.

DEVELOPMENT SUPPORT

The R6500/2-11 can be used to support development of both the R6500/1-11 and R6500/1-11Q single-chip microcomputers. These microcomputer devices are described in Rockwell Documents 29000 D64 and 29000 D65, respectively. Rockwell also offers development support, including in-circuit emulation, with the System 65 Microcomputer Development System and the R6500/1-11 Personality Module.



*MULTIPLEXED FUNCTIONS PINS (Software Selectable)

Interface Diagram

FEATURES

- Enhanced 6502 CPU
  - —Four new instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
  - —65K-byte addressing
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - —Pulse measurement
  - —Pulse generation
  - —Interval timer
  - —Event counter
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Synchronous shift register mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Programmable bit rates to 62.5 bits/sec (@ 2 MHz)
- Four edge-sensitive lines; two positive, two negative
- Ten interrupts
  - —Reset
  - —Non-maskable
  - —Four external, edge-sensitive
  - —Two counter
  - —Serial data received
  - —Serial data transmitted
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at two or four times internal frequency
  - —External clock input divided by one, two or four
- 1 μs minimum instruction execution time
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 16 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP

Specifications subject to change without notice
Document No. 29000 D66
November 1980

ELECTRICAL SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{In}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial Industrial	T	0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D. C. Characteristics (V_{CC} = 5V ±5% V_{SS} = 0)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High) Commercial @ 25°C Industrial @ 25°C	P_D	— —		1000 1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C Industrial @ 25°C	I_{RR}	— —	4 5.2	— —	mWdc
Input High Voltage Except XTLI	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3	—	+0.8	Vbc
Input Leakage Current (RES, NMI) V_{In} = 0 to 5.0 Vdc	I_{IN}		±1.0	±2.5	μAdc
Input Low Current PA, PB, PC, PD (V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mWdc
Output High Voltage Except XTLO (I_{Load} = .100 μAdc)	V_{OH}	+2.4	—	—	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance (V_{In}-0, T_A = 25°C, t=1.0 MHz) PA, PB, PC, PD XTLI, XTLO	C_{In}	— —	— —	10 50	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	R_L	3.0	6.0	11.5	KΩ

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC Characteristics (V_{CC} = 5V ±5% V_{SS} = 0)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	μ sec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		μ sec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		μ sec

R6500
I/O
DEVICES

DOCUMENT NO. 29000 D40
REVISION 2, OCT. 1978

PART NUMBER
R6520

Rockwell

R6500 Microcomputer System
DATA SHEET

PERIPHERAL INTERFACE ADAPTER (PIA)

DESCRIPTION

The R6520 Peripheral Interface Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500 family of microprocessors, the R6520 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.

Ordering Information

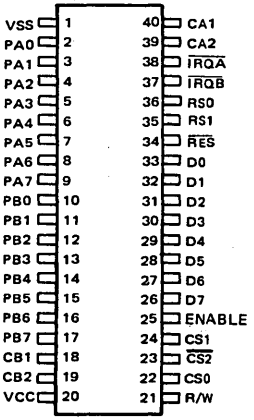
Order Number: R6520 – – –

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = -40°C to +85°C (Industrial)
  - MT = -55°C to +125°C (Military)
  - M = MIL-STD-883, Class B
- Package:
  - C = Ceramic
  - P = Plastic (Not Available for M or MT suffix)
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2MHz

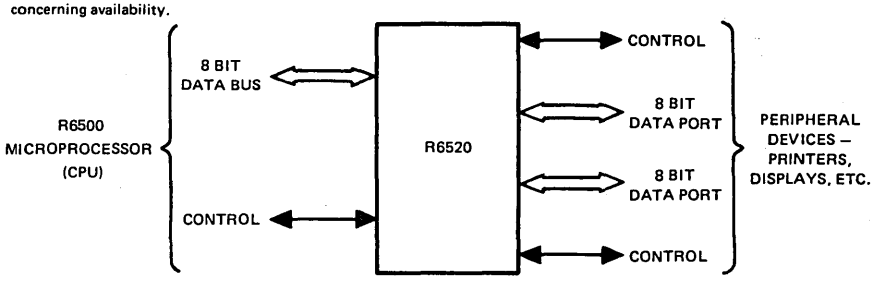
NOTE: Contact your local Rockwell Representative concerning availability.

FEATURES

- High performance replacement for Motorola/AMI/MOSTEK/ Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows positive control of data transfers between processor and peripheral devices.
- Commercial, industrial and military temperature range versions.



Pin Configuration



Basic R6520 Interface Diagram

Specifications subject to change without notice

SUMMARY OF R6520 OPERATION

See Rockwell Microcomputer Hardware Manual for detailed description of R6520 operation.

CA1/CB1 Control

CRA (CRB)		Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
Bit 1	Bit 0		
0	0	Negative	Disable — remain high
0	1	Negative	Enable — goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable — remain high
1	1	Positive	Enable — as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 Input Modes

CRA (CRB)			Active Transition of Input Signal*	IRQA (IRQB) Interrupt Output
Bit 5	Bit 4	Bit 3		
0	0	0	Negative	Disable — remains high
0	0	1	Negative	Enable — goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable — remains high
0	1	1	Positive	Enable — as explained above

Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 Output Modes

CRA			Mode	Description
Bit 5	Bit 4	Bit 3		
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 Output Modes

CRB			Mode	Description
Bit 5	Bit 4	Bit 3		
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

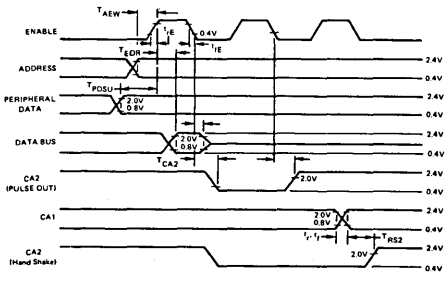
A.C. CHARACTERISTICS

Read Timing Characteristics (Loading 130 pF and one TTL load)

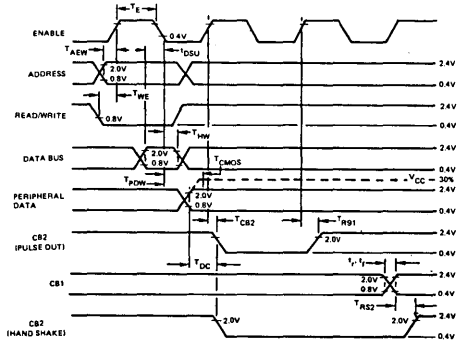
Characteristics	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	–	90	–	ns
Delay Time, Enable positive transition to Data valid on bus	T_{EDR}	–	395	–	190	ns
Peripheral Data Setup Time	T_{PDSU}	300	–	150	–	ns
Data Bus Hold Time	T_{HR}	10	–	10	–	ns
Delay Time, Enable negative transition to CA2 negative transition	T_{CA2}	–	1.0	–	0.5	μs
Delay Time, Enable negative transition to CA2 positive transition	T_{RS1}	–	1.0	–	0.5	μs
Rise and Fall Time for CA1 and CA2 input signals	t_r, t_f	–	1.0	–	0.5	μs
Delay Time from CA1 active transition to CA2 positive transition	T_{RS2}	–	2.0	–	1.0	μs
Rise and Fall Time for Enable input	t_{rE}, t_{fE}	–	25	–	25	ns

Write Timing Characteristics

Characteristics	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Enable Pulse Width	T_E	0.470	25	0.235	25	μs
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	–	90	–	ns
Delay Time, Data valid to Enable negative transition	T_{DSU}	300	–	150	–	ns
Delay Time, Read/Write negative transition to Enable positive transition	T_{WE}	130	–	65	–	ns
Data Bus Hold Time	T_{HW}	10	–	10	–	ns
Delay Time, Enable negative transition to Peripheral Data valid	T_{PDW}	–	1.0	–	0.5	μs
Delay Time, Enable negative transition to Peripheral Data valid CMOS (V_{CC} - 30%) PA0-PA7, CA2	T_{CMOS}	–	2.0	–	1.0	μs
Delay Time, Enable positive transition to CB2 negative transition	T_{CB2}	–	1.0	–	0.5	μs
Delay Time, Peripheral Data valid to CB2 negative transition	T_{DC}	0	1.5	0	0.75	μs
Delay Time, Enable positive transition to CB2 positive transition	T_{RS1}	–	1.0	–	0.5	μs
Rise and Fall Time for CB1 and CB2 input signals	t_r, t_f	–	1.0	–	0.5	μs
Delay Time, CB1 active transition to CB2 positive transition	T_{RS2}	–	2.0	–	1.0	μs



Read Timing Characteristics



Write Timing Characteristics

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Military		-55 to +125	
Storage Temperature Range	T_{STG}	-55 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Static D.C. Characteristics

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	–	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	–	+0.8	Vdc
Input Threshold Voltage	V_{IT}	0.8	–	2.0	Vdc
Input Leakage Current	I_{in}				μAdc
V_{in} = 0 to 5.0 Vdc R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Φ2		–	±1.0	±2.5	
Three-State (Off State Input Current) (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) D0-D7, PB0-PB7, CB2	I_{TSI}	–	±2.0	±10	μAdc
Input High Current (V_{IH} = 2.4 Vdc) PA0-PA7, CA2	I_{IH}	-100	-250	–	μAdc
Input Low Current (V_{IL} = 0.4 Vdc) PA0-PA7, CA2	I_{IL}	–	-1.0	-1.6	mAdc
Output High Voltage (V_{CC} = min, I_{Load} = -100 μAdc)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (V_{CC} = min, I_{Load} = 1.6 mAdc)	V_{OL}	–	–	+0.4	Vdc
Output High Current (Sourcing)	I_{OH}				
(V_{OH} = 2.4 Vdc)		-100	-1000	–	μAdc
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7, CB2		-1.0	-2.5	–	mAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	–	–	mAdc
Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$	I_{off}	–	1.0	10	μAdc
Power Dissipation	P_D	–	200	500	mW
Input Capacitance	C_{in}				pF
(V_{in} - 0, T_A = 25°C, f = 1.0 MHz)					
D0-D7, PA0-PA7, PB0-PB7, CA2, CB2		–	–	10	
R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$,		–	–	7.0	
CA1, CB1, Φ2		–	–	20	
Output Capacitance (V_{in} - 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	10	pF

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

Rockwell

R6500 Microcomputer System DATA SHEET

VERSATILE INTERFACE ADAPTER (VIA)

- Two 8-Bit Bidirectional I/O Ports
- Two 16-Bit Programmable Timer/Counters
- Serial Data Port
- Single +5V Power Supply
- TTL Compatible
- CMOS Compatible Peripheral Control Lines
- Expanded "Handshake" Capability Allows Positive Control of Data Transfers Between Processor and Peripheral Devices
- Latched Output and Input Registers
- 1 MHz and 2 MHz Operation

The R6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

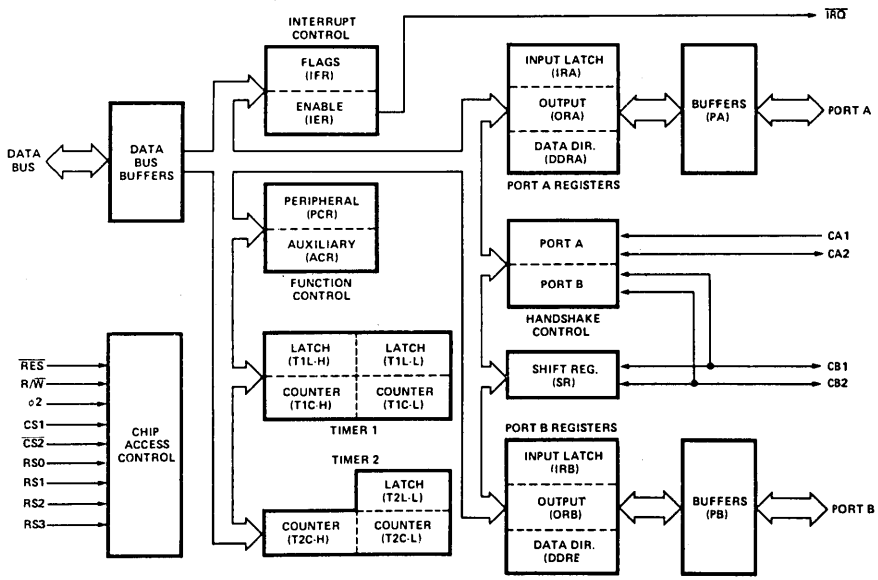


Figure 1. R6522 Block Diagram

Document No. 2900 D47
Rev. 3, February 1981

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range	T		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Military		-55 to +125	
Storage Temperature Range	T_{STG}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0-70°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage (all except $\phi 2$)	2.4	V_{CC}	V
V_{CH}	Clock High Voltage	2.4	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.4	V
I_{IN}	Input Leakage Current – V_{IN} = 0 to 5 Vdc R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, $\Phi 2$	–	±2.5	μA
I_{TSI}	Off-state Input Current – V_{IN} = .4 to 2.4V V_{CC} = Max, D0 to D7	–	±10	μA
I_{IH}	Input High Current – V_{IH} = 2.4V PA0-PA7, CA2, PB0-PB7, CB1, CB2	-100	–	μA
I_{IL}	Input Low Current – V_{IL} = 0.4 Vdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	–	-1.6	mA
V_{OH}	Output High Voltage V_{CC} = min, I_{load} = -100 μAdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	2.4	–	V
V_{OL}	Output Low Voltage V_{CC} = min, I_{load} = 1.6 mAdc	–	0.4	V
I_{OH}	Output High Current (Sourcing) V_{OH} = 2.4V V_{OH} = 1.5V (PB0-PB7)	 -100 -1.0	 – –	 μA mA
I_{OL}	Output Low Current (Sinking) V_{OL} = 0.4 Vdc	1.6	–	mA
I_{OFF}	Output Leakage Current (Off state) $\overline{IRQ}$	–	10	μA
C_{IN}	Input Capacitance – T_A = 25°C, f = 1 MHz (R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7) (CB1, CB2) ($\Phi 2$ Input)	 – – –	 7.0 10 20	 pF pF pF
C_{OUT}	Output Capacitance – T_A = 25°C, f = 1 MHz	–	10	pF
P_D	Power Dissipation	–	700	mW

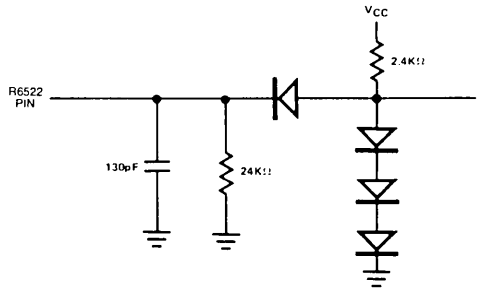


Figure 2. Test Load (for all Dynamic Parameters)

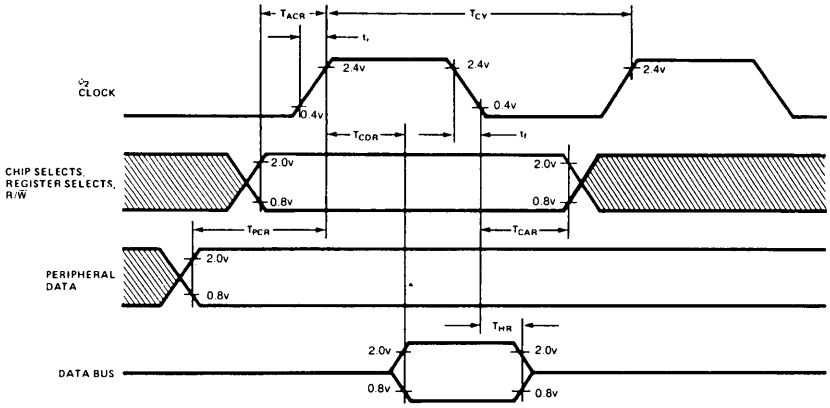


Figure 3. Read Timing Characteristics

READ TIMING CHARACTERISTICS (FIGURE 3)

Symbol	Parameter	R6522		R6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

NOTE: tr, tf = 10 to 30ns.

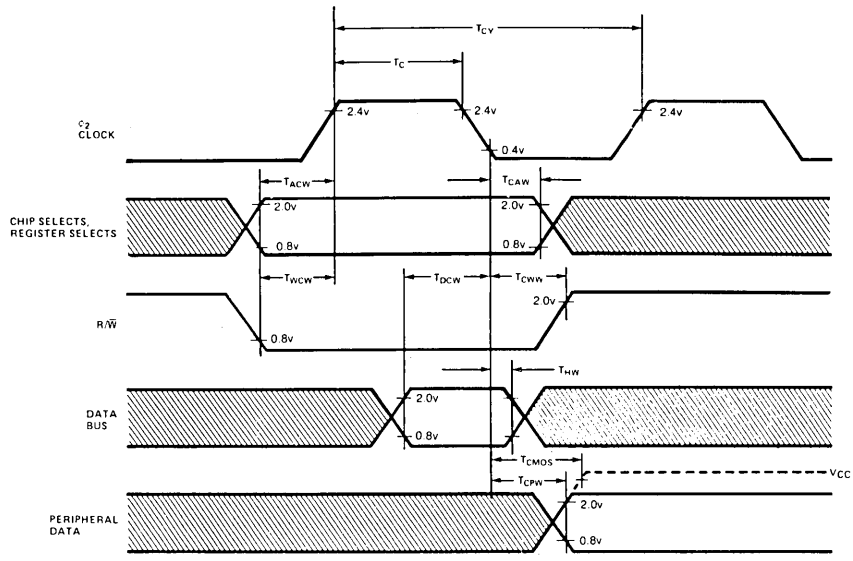


Figure 4. Write Timing Characteristics

WRITE TIMING CHARACTERISTICS (FIGURE 4)

Symbol	Parameter	R6522		R6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	ϕ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	300	–	200	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

NOTE: tr, tf = 10 to 30ns.

PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Characteristic	Min.	Max.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2, and CB2 Input Signals	–	1.0	μs	–
T_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	–	1.0	μs	5a, 5b
T_{RS1}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	–	1.0	μs	5a
T_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	–	2.0	μs	5b
T_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0	μs	5c, 5d
T_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1.5	μs	5c, 5d
T_{RS3}	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	–	1.0	μs	5c
T_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	–	2.0	μs	5d
T_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	–	ns	5d
T_{IL}	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	–	ns	5e
T_{SR1}	Shift-Out Delay Time – Time from ϕ_2 Falling Edge to CB2 Data Out	–	300	ns	5f
T_{SR2}	Shift-In Setup Time – Time from CB2 Data In to ϕ_2 Rising Edge	300	–	ns	5g
T_{SR3}	External Shift Clock (CB1) Setup Time Relative To ϕ_2 Trailing Edge	100	T_{CY}	ns	5g
T_{IPW}	Pulse Width – PB6 Input Pulse	2	–	μs	5i
T_{ICW}	Pulse Width – CB1 Input Clock	2	–	μs	5h
I_{IPS}	Pulse Spacing – PB6 Input Pulse	2	–	μs	5i
I_{ICS}	Pulse Spacing – CB1 Input Pulse	2	–	μs	5h

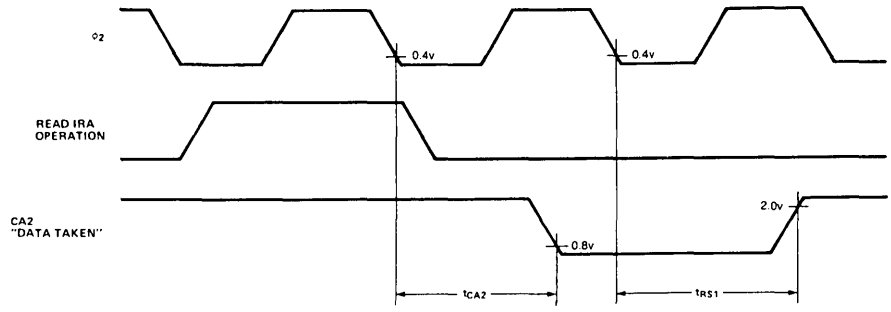


Figure 5a. CA2 Timing for Read Handshake, Pulse Mode

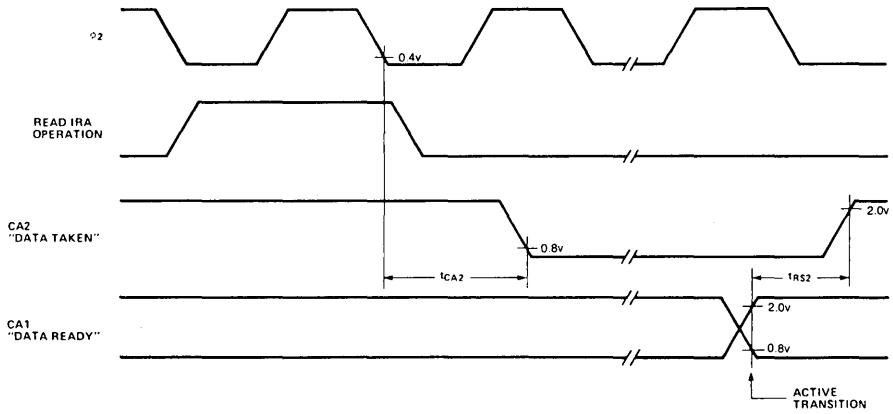


Figure 5b. CA2 Timing for Read Handshake, Handshake Mode

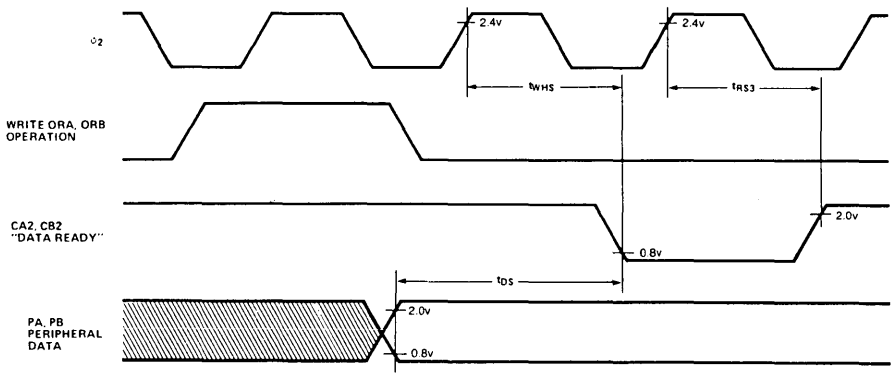


Figure 5c. CA2, CB2 Timing for Write Handshake, Pulse Mode

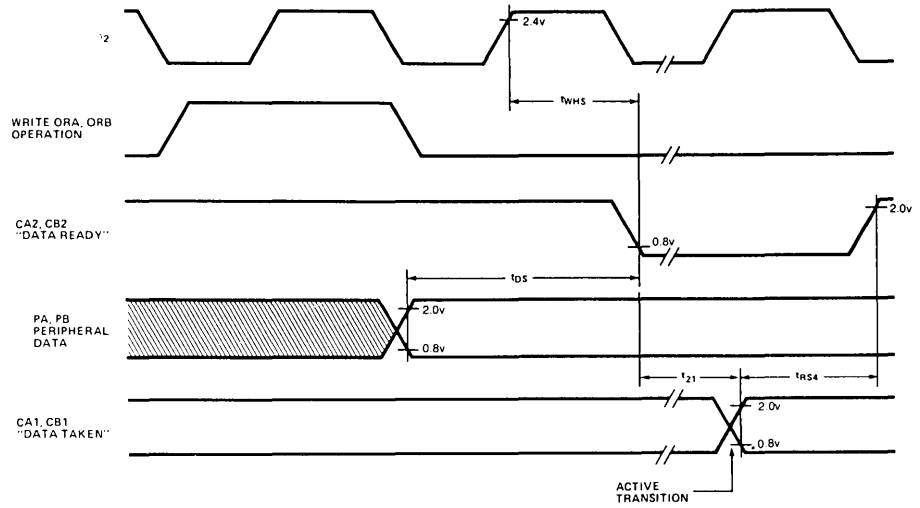


Figure 5d. CA2, CB2 Timing for Write Handshake, Handshake Mode

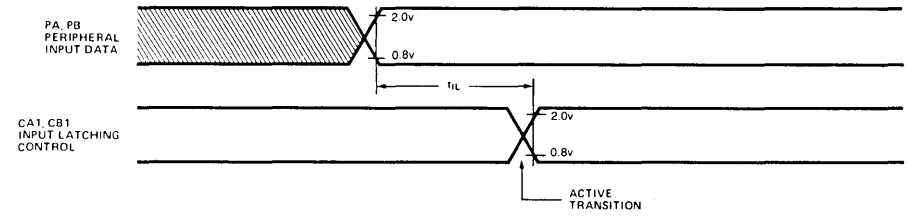


Figure 5e. Peripheral Data Input Latching Timing

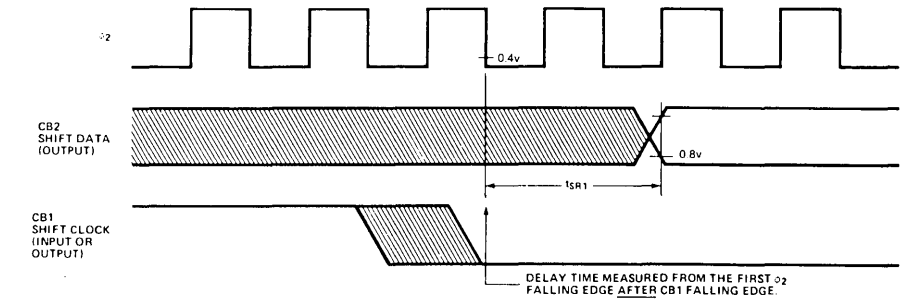


Figure 5f. Timing for Shift Out with Internal or External Shift Clocking

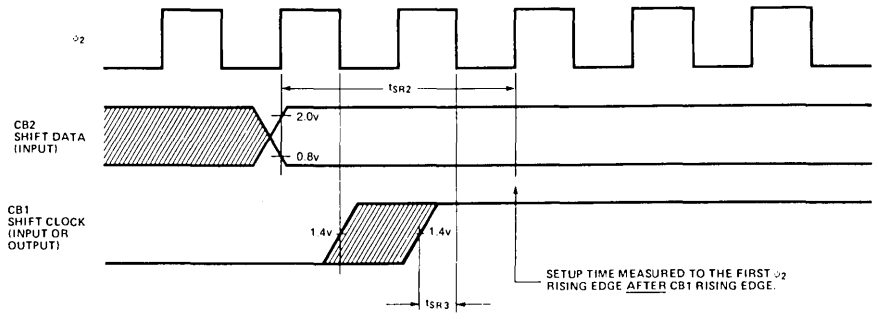


Figure 5g. Timing for Shift In with Internal or External Shift Clocking

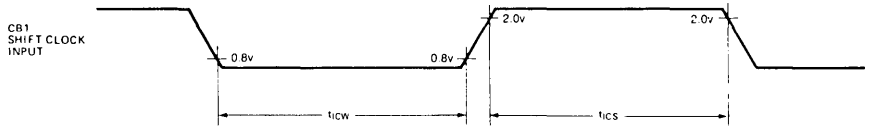


Figure 5h. External Shift Clock Timing

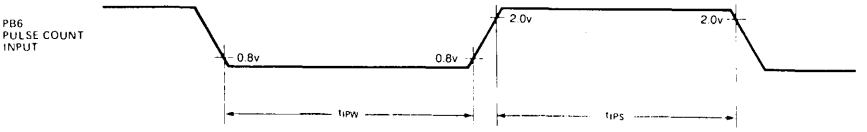


Figure 5i. Pulse Count Input Timing

PIN DESCRIPTIONS

RES (Reset)

The reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

ϕ2 (Input Clock)

The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system processor and the R6522.

R/W (Read/Write)

The direction of the data transfers between the R6522 and the system processor is controlled by the R/W line. If R/W is low, data will be transferred out of the processor into the selected R6522 register (write operation). If R/W is high and the chip is selected, data will be transferred out of the R6522 (read operation).

DB0-DB7 (Data Bus)

The eight bi-directional data bus lines are used to transfer data between the R6522 and the system processor. During read cycles, the contents of the selected R6522 register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the R6522 is unselected, the data bus lines are high-impedance.

CS1, CS2 (Chip Selects)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected R6522 register will be accessed when CS1 is high and CS2 is low.

RS0-RS3 (Register Selects)

The four Register Select inputs permit the system processor to select one of the 16 internal registers of the R6522, as shown in Figure 6.

Register Number	RS Coding				Register Desig.	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No "Handshake"	

Figure 6. R6522 Internal Register Summary

IRQ (Interrupt Request)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system.

PA0-PA7 (Peripheral A Port)

The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 7 illustrates the output circuit.

CA1, CA2 (Peripheral A Control Lines)

The two Peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines. CA1 is a high-impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

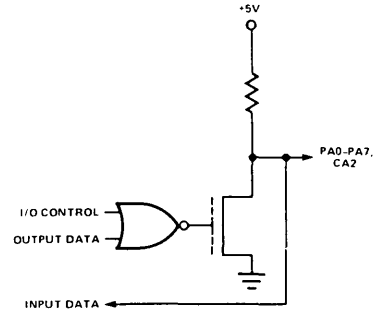


Figure 7. Peripheral A Port Output Circuit

PB0-PB7 (Peripheral B Port)

The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0mA at 1.5VDC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 8 is the circuit schematic.

CB1, CB2 (Peripheral B Control Lines)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Unlike PB0-PB7, CB1 and CB2 cannot drive Darlington transistor circuits.

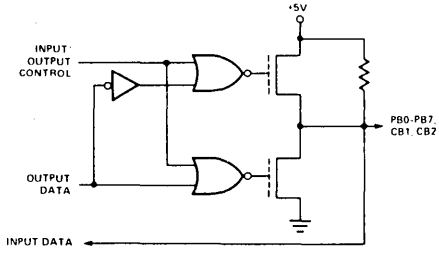


Figure 8. Peripheral B Port Output Circuit

FUNCTIONAL DESCRIPTION

Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and an Input Register (IRA, IRB). When the pin is programmed as an output, the voltage on the pin is controlled by the cor-

responding bit of the Output Register. A 1 in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

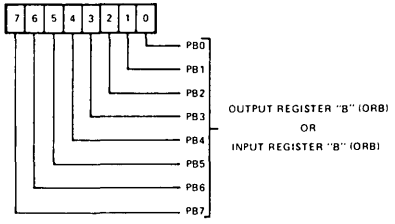
The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the level on the pin determines whether a 0 or a 1 is sensed. When reading IRB, however, the bit stored in the output register, ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 9, 10, and 11 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 16.)

Handshake Control of Data Transfers

The R6522 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

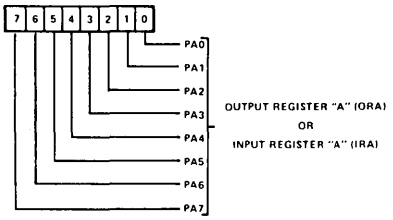
REG 0 – ORB/IRB



Pin Data Direction Selection	WRITE	READ
DDRB = "1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no affect.
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed.	MPU reads input level on PB pin.
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 9. Output Register B (ORB), Input Register B (IRB)

REG 1 – ORA/IRA



Pin Data Direction Selection	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 2 (DDRB) AND REG 3 (DDRA)

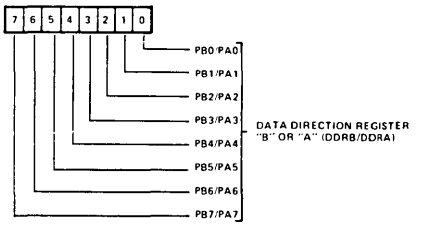


Figure 11. Data Direction Registers (DDRB, DDRA)

Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

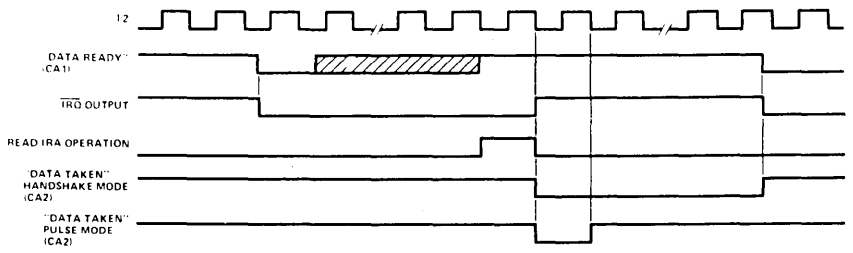


Figure 12. Read Handshake Timing (Port A, Only)

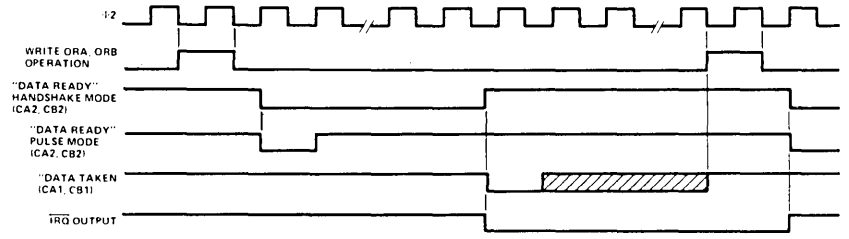


Figure 13. Write Handshake Timing

In the R6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 12 which illustrates the normal Read Handshaking sequence.

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the R6522 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the R6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and cleaning the "Data Ready" output. This sequence is shown in Figure 13.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 14).

Timer Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at Φ2 clock rate. Upon reaching zero, an interrupt flag will be set, and $\overline{IRQ}$ will go low if the interrupt is enabled. The timer will then disable any further interrupts, or will automatically transfer the contents of the latches into the counter and will continue to decrement. In addition, the timer may be programmed to invert the output signal on a peripheral pin each time it "times-out". Each of these modes is discussed separately below.

The T1 counter is depicted in Figure 15 and the latches in Figure 16.

REG 12 – PERIPHERAL CONTROL REGISTER

7	6	5	CB2 CONTROL
0	0	0	INPUT NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE
0	1	0	INPUT POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT POS EDGE
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

CB1 INTERRUPT CONTROL
0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

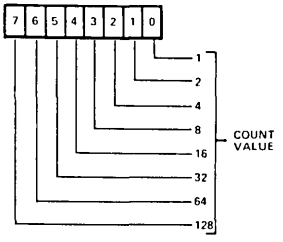
CA1 INTERRUPT CONTROL
0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

3	2	1	CA2 CONTROL
0	0	0	INPUT NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE
0	1	0	INPUT POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT POS EDGE
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

Figure 14. CA1, CA2, CB1, CB2 Control

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating modes. The four possible modes are depicted in Figure 17.

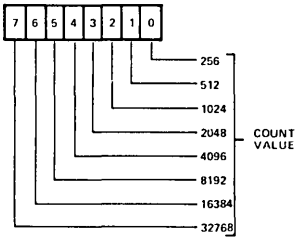
REG 4 – TIMER 1 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T1 LOW ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

REG 5 – TIMER 1 HIGH-ORDER COUNTER

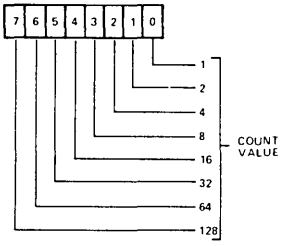


WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER. T1 INTERRUPT FLAG ALSO IS RESET.

READ – 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 15. T1 Counter Registers

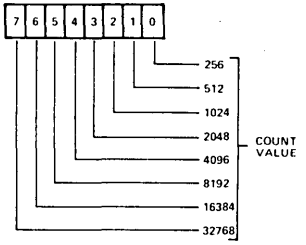
REG 6 – TIMER 1 LOW-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 LOW ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAT A WRITE INTO REG 4.

READ – 8 BITS FROM T1 LOW ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

REG 7 – TIMER 1 HIGH-ORDER LATCHES

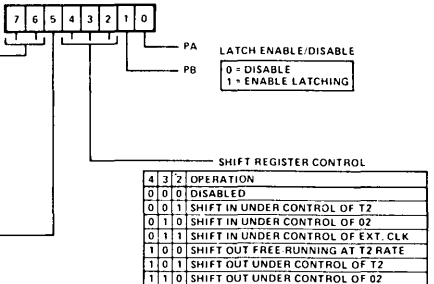


WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH TO COUNTER TRANSFERS TAKE PLACE.

READ – 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers

REG 11 – AUXILIARY CONTROL REGISTER



T1 TIMER CONTROL

7	6	OPERATION	PB7
0	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	DISABLED
0	1	CONTINUOUS INTERRUPTS	
1	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	ONE SHOT OUTPUT
1	1	CONTINUOUS INTERRUPTS	SQUARE WAVE OUTPUT

T2 TIMER CONTROL

5	OPERATION
0	TIMED INTERRUPT
1	COUNT DOWN WITH PULSES ON PB6

4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF 02
0	1	1	SHIFT IN UNDER CONTROL OF EXT. CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF 02
1	1	1	SHIFT OUT UNDER CONTROL OF EXT. CLK

Figure 17. Auxiliary Control Register

Note: The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

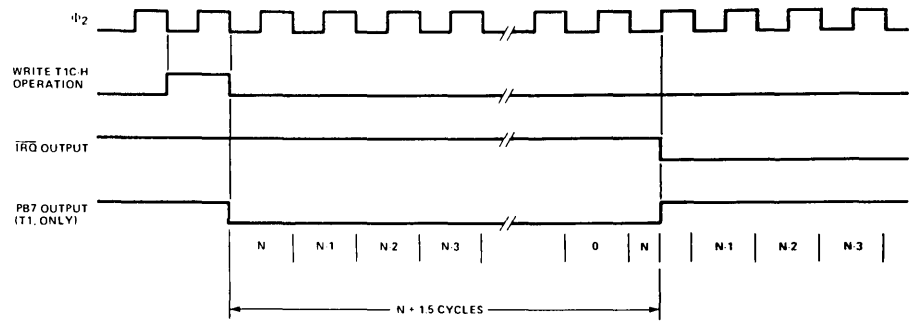


Figure 18. Timer 1 and Timer 2 One-Shot Mode Timing

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7=1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

In the one-shot mode, writing into the high order latch has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter, the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the phase two following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

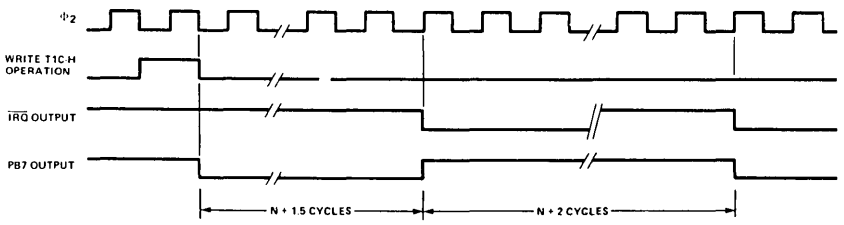
Timing for the R6522 interval timer one-shot modes is shown in Figure 18.

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the R6522 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 19.



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and the other is 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 19. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-slot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at Φ2 rate. Figure 20 illustrates the T2 Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

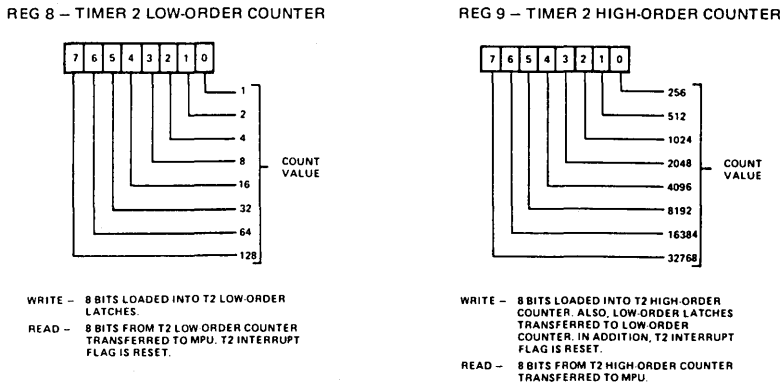


Figure 20. T2 Counter Registers

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on subsequent down-counting operations. Timing for this mode is shown in Figure 21. The pulse must be low on the leading edge of Φ2.

Shift Register Operation

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 22 illustrates the configuration of the SR data bits and the SR control bits of the ACR.

Figures 23 and 24 illustrate the operation of the various shift register modes.

Interrupt Operation

Controlling interrupts within the R6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-or'ed" with other devices in the system to interrupt the processor.

In the R6522, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

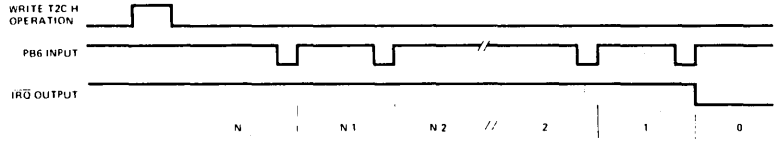
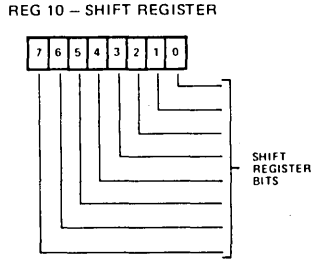
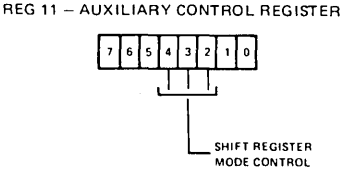


Figure 21. Timer 2 Pulse Counting Mode



NOTES:
1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF Φ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF Φ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

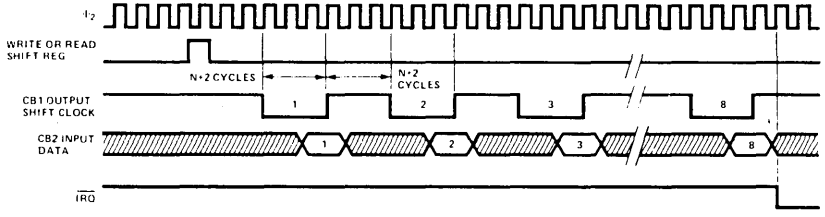
SR Disabled (000)

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operation is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

Shift in Under Control of T2 (001)

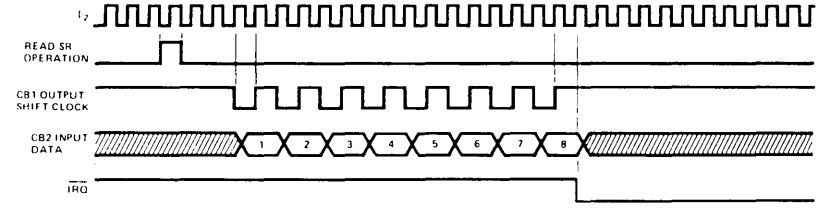
In the 001 mode the shifting rate is controlled by the low order 8 bits of T2. Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the ϕ_2 clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will be set and $\overline{IRQ}$ will go low.



Shift in Under Control of ϕ_2 (010)

In mode 010 the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each ϕ_2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.



Shift in Under Control of External CB1 Clock (011)

In mode 011 CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

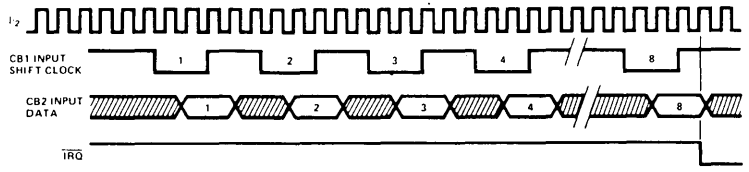
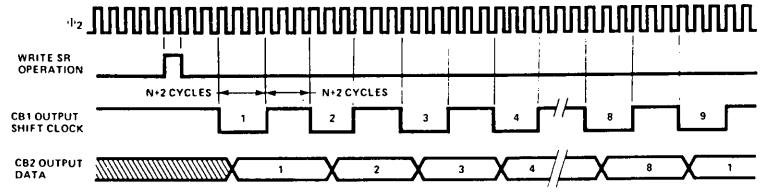


Figure 23. Shift Register Input Modes

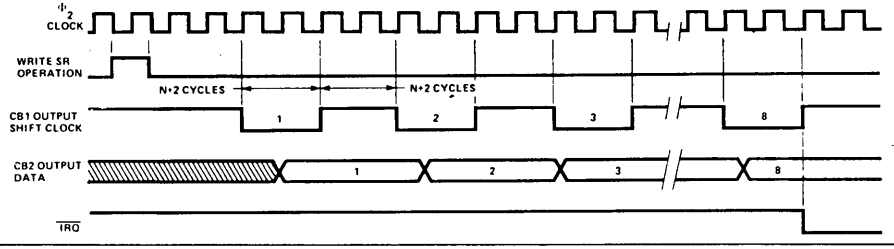
Shift Out Free-Running at T2 Rate (100)

Mode 100 is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.



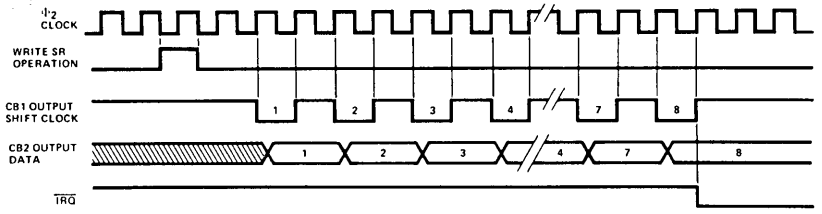
Shift Out Under Control of T2 (101)

In mode 101 the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.



Shift Out Under Control of ϕ_2 (110)

In mode 110, the shift rate is controlled by the ϕ_2 system clock.



Shift Out Under Control of External CB1 Clock (111)

In mode 111 shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

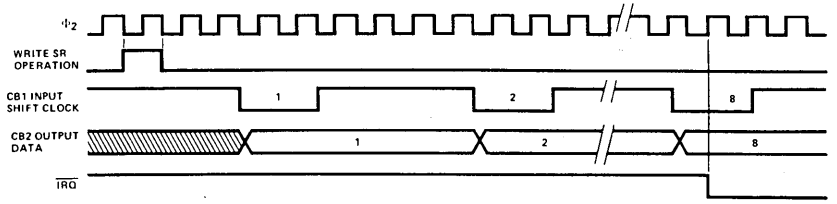


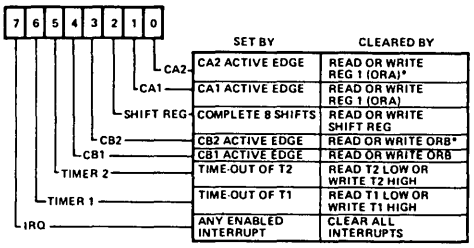
Figure 24. Shift Register Output Modes

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) are depicted in Figures 25 and 26, respectively.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the IRQ output. This bit corresponds to the logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: X = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

REG 13 – INTERRUPT FLAG REGISTER



* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

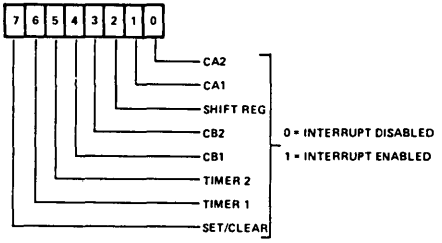
Figure 25. Interrupt Flag Register (IFR)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can be set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/W line high. Bit 7 will be read as a logic 0.

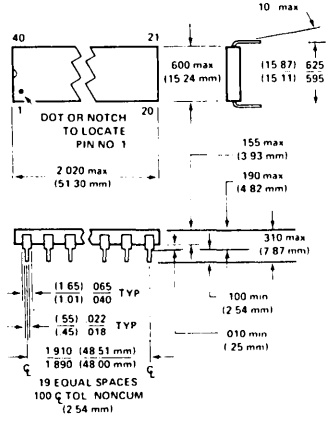
REG 14 – INTERRUPT ENABLE REGISTER



NOTES:
1. IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT.
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
3. IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "0" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

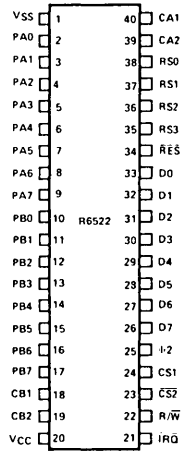
Figure 26. Interrupt Enable Register (IER)

PACKAGE OUTLINE



NOTE Pin No 1 is in lower left corner when symbolization is in normal orientation

PIN CONFIGURATION



Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6522P	Plastic	1 MHz	0^{o}C to $+70^{o}$C
R6522AP	Plastic	2 MHz	0^{o}C to $+70^{o}$C
R6522C	Ceramic	1 MHz	0^{o}C to $+70^{o}$C
R6522AC	Ceramic	2 MHz	0^{o}C to $+70^{o}$C
R6522PE	Plastic	1 MHz	-40^{o}C to $+85^{o}$C
R6522APE	Plastic	2 MHz	-40^{o}C to $+85^{o}$C
R6522CE	Ceramic	1 MHz	-40^{o}C to $+85^{o}$C
R6522ACE	Ceramic	2 MHz	-40^{o}C to $+85^{o}$C

Rockwell

R6500 Microcomputer System
DATA SHEET

CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545-1 CRT Controller (CRTC) is designed to interface an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500 products.

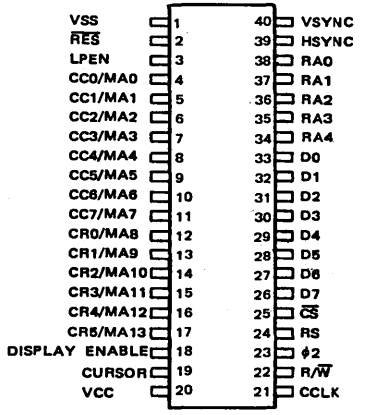
The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows non-interlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable Vertical Sync Width
- Fully programmable display (rows, columns, character matrix)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-Pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 ±5% Volt Power Supply



R6545-1 Pin Configuration

ORDERING INFORMATION

Part Number	Package Type	Frequency	Temperature Range
R6545-1P	Plastic	1 MHz	0°C to +70°C
R6545-1AP	Plastic	2 MHz	0°C to +70°C
R6545-1C	Ceramic	1 MHz	0°C to +70°C
R6545-1AC	Ceramic	2 MHz	0°C to +70°C

Specifications subject to change without notice
Document No. 29000 D67
December 1980

INTERFACE SIGNAL DESCRIPTION

CPU INTERFACE

ϕ2 (Phase 2 Clock)

The input clock is the system Phase 2 (ϕ2) clock and is used to trigger all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable ϕ2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545-1, a low on the R/$\overline{W}$ pin allows data on data lines D0-D7 to be written into the R6545-1.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes (R/$\overline{W}$ = low) into the Address Register and reads (R/$\overline{W}$ = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0-D7 (Data Bus)

D0-D7 are the eight data lines used to transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\overline{CS}$ = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE signal is an active-high output used to indicate when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE can be delayed one character time by setting bit 4 of R8 equal to 1.

CURSOR (Cursor Coincidence)

The CURSOR signal is an active-high output used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to A "1".

LPEN (Light Pen Strobe)

The LPEN signal is an edge-sensitive input used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK (Clock)

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency. $\overline{RES}$ may also be used to synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 signals are active-high outputs used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = "0"), characters are stored in successive memory locations. Thus, the software must be designed such that row and column character coordinates are translated into sequentially-numbered addresses. In the row/column mode (R8, Mode Control, bit 2 = "1"), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

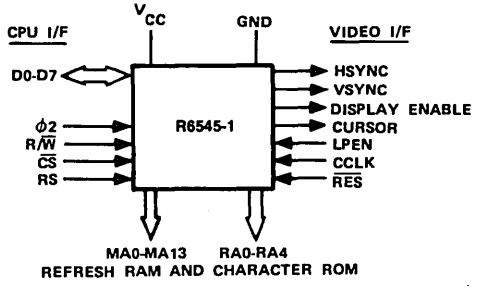
RA0-RA4 (Raster Address Lines)

These 5 signals are active-high outputs used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

INTERNAL REGISTER ORGANIZATION

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Reg. No.	Register Name	Register Units	Read ($R/\overline{W}$ = High)	Write ($R/\overline{W}$ = Low)	Register Bit 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X												
0	0	X	X	X	X	X	X	Address Register	Register No.		✓				4	3	2	1	0
0	0	X	X	X	X	X	X	Status Register	–	✓			6	5					
0	1	0	0	0	0	0	R0	Horizontal Total Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	R1	Horizontal Displayed Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	R2	Horizontal Sync Position	Character Position		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	R3	YSYNC, HSYNC Widths	No. of Scan Lines, Characters		✓	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	R4	Vertical Total Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	0	1	R5	Vertical Total Adjust Lines	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	0	1	1	0	R6	Vertical Displayed Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	1	1	R7	Vertical Sync Position	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	1	0	0	0	R8	Mode Control	–		✓	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	R9	Scan Line	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	1	0	1	0	R10	Cursor Start Line	Scan Line No.		✓		6	5	4	3	2	1	0
0	1	0	1	0	1	1	R11	Cursor End Line	Scan Line No.		✓				4	3	2	1	0
0	1	0	1	1	0	0	R12	Display Start Address (H)	–		✓			5	4	3	2	1	0
0	1	0	1	1	0	1	R13	Display Start Address (L)	–		✓	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	R14	Cursor Position Address (H)	–	✓	✓			5	4	3	2	1	0
0	1	0	1	1	1	1	R15	Cursor Position Address (L)	–	✓	✓	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	R16	Light Pen Register (H)	–	✓				5	4	3	2	1	0
0	1	1	0	0	0	1	R17	Light Pen Register (L)	–	✓		7	6	5	4	3	2	1	0

Table 1. Overall Register Structure and Addressing



R6545-1 Interface Diagram

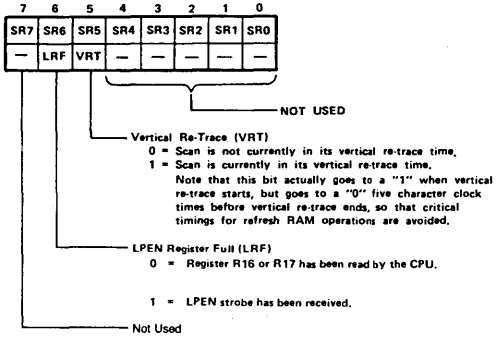
INTERNAL REGISTER DESCRIPTION

ADDRESS REGISTER

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. Its contents is the number of the desired register (0-17). When $\overline{CS}$ and RS are low, then this register may be loaded; when $\overline{CS}$ is low and RS is high, then the register selected is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

This 8-bit register contains the status of the CRTC. Only two bits are assigned, as follows:



NOTE: The Status Register takes the State, [–][0][1][–][–][–][–][–] immediately after power (V_{CC}) turn-on.

R0—HORIZONTAL TOTAL CHARACTERS

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

R1—HORIZONTAL DISPLAYED CHARACTERS

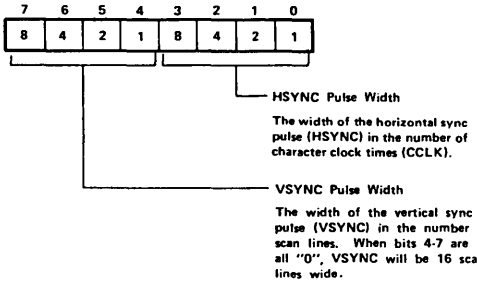
This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

This 8-bit write-only register contains the position of the horizontal SYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allows the R6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

The Vertical Total Line Adjust Register (R5) is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

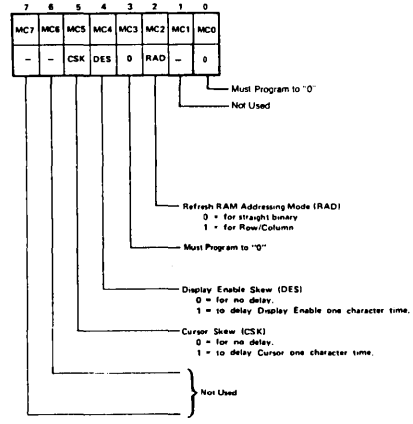
This 7-bit write-only register contains the number of displayed character rows in each frame.

R7—VERTICAL SYNC POSITION

This 7-bit write-only register is used to select the character row time at which the vertical SYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

This 8-bit write-only register selects the operating modes of the R6545-1, as follows:



R9—ROW SCAN LINES

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE
R11—CURSOR END LINE

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

Bit 6	Bit 5	Cursor Blink Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

R12—DISPLAY START ADDRESS HIGH
R13—DISPLAY START ADDRESS LOW

These registers form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

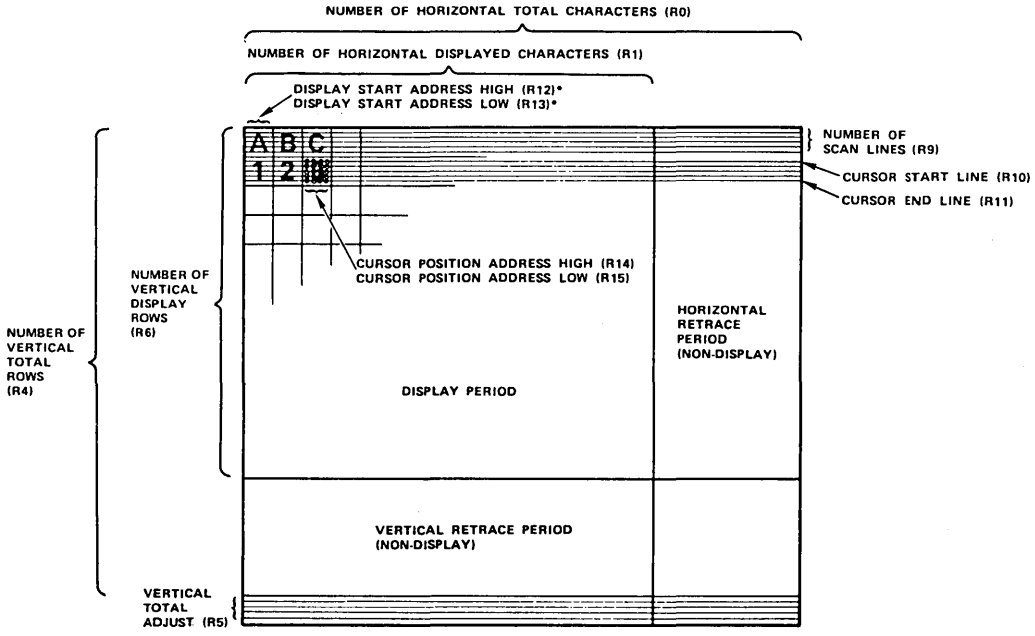


Figure 1. Video Display Format

R14—CURSOR POSITION HIGH
R15—CURSOR POSITION LOW

These registers form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

R16—LIGHT PEN HIGH
R17—LIGHT PEN LOW

These registers form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, and R16/R17 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = "0".

(2) Row/Column, if register R8, bit 2 = "1". In this case the low byte is the Character Column and the high byte is the Character Row.

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 1 indicates the relationship of the various program registers in the R6545-1 and the resultant video display.

Non-displayed areas of the Video Display are used for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and are used to trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

Shared Memory Mode (R8, bit 3 = "0")

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5).

ADDRESSING MODES

Row/Column

In this mode, the CRTC address lines (MA0-MA13) are generated as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM.

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity is increased since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential.

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545-1 permits the use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 2 illustrates Refresh RAM addressing for the case of binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	3		76	77	78	79	80	81	89
80	81	82	83		156	157	158	159	160	161	169
160	161	162				237	238	239	240		249
240	241	242				317	318	319	320		329
1680	1681	1682				1757	1758	1759	1760		1769
1760	1761	1762				1837	1838	1839	1840		1849
1840	1841	1842				1917	1918	1919	1920		1929
1920	1921	1922				1997	1998	1999	2000		2009
2000	2001	2002				2077	2078	2079	2080		2089
2640	2641	2642				2717	2718	2720			2729

Figure 2. Memory Addressing Example (80 x 24)

CURSOR OPERATION

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

Bits 5 and 6 in the Cursor Start Line High Register (R10) control the cursor display and blink rate as follows:

Bit 6	Bit 5	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

The cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

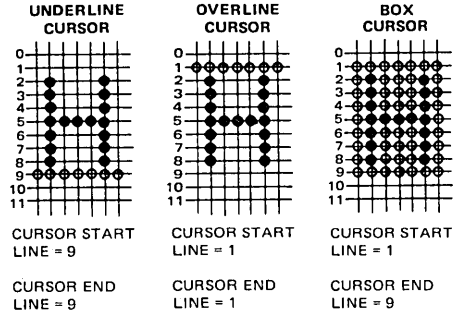


Figure 3. Cursor Display Scan Line Control Examples

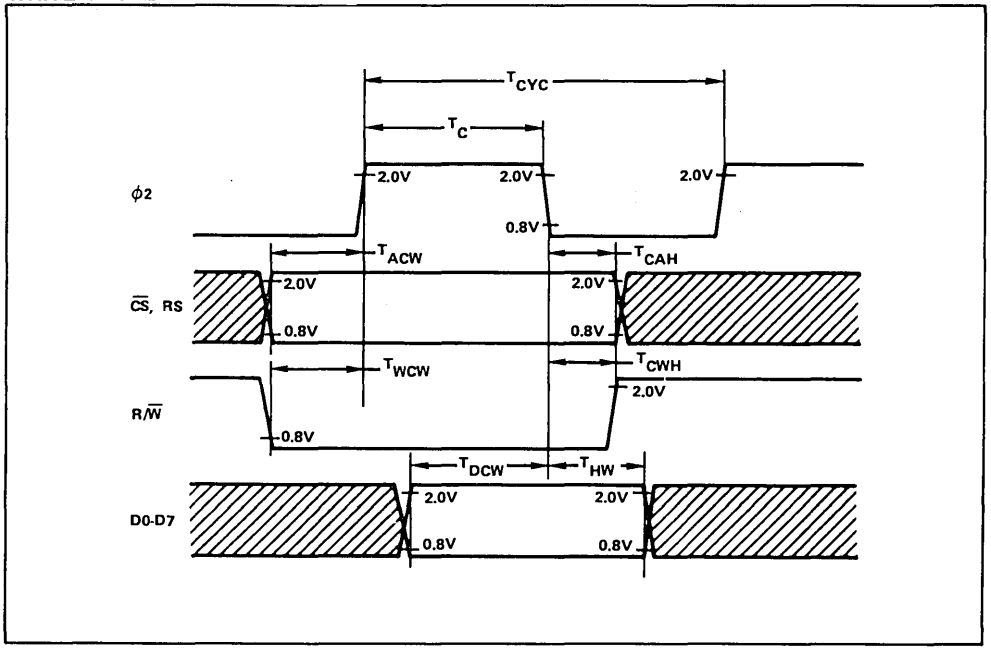
MPU WRITE TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACW}	180	–	90	–	ns
Address Hold Time	T_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCW}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	T_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	T_{DCW}	265	–	100	–	ns
Data Bus Hold Time	T_{HW}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

WRITE CYCLE



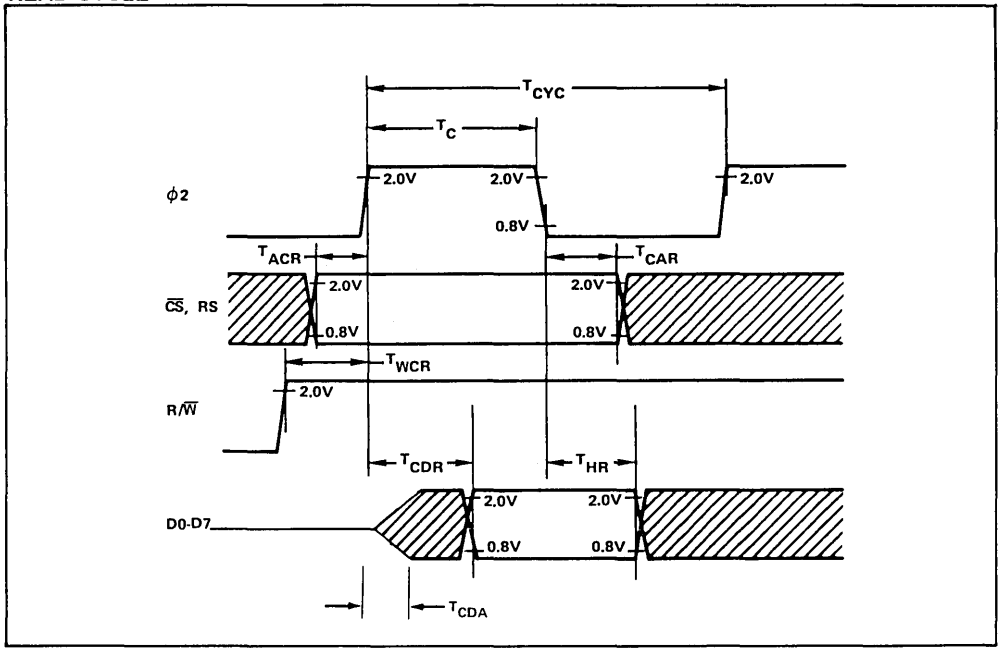
MPU READ TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACR}	180	–	90	–	ns
Address Hold Time	T_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCR}	180	–	90	–	ns
Read Access Time	T_{CDR}	–	340	–	150	ns
Read Hold Time	T_{HR}	10	–	10	–	ns
Data Bus Active Time (Invalid Data)	T_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

READ CYCLE



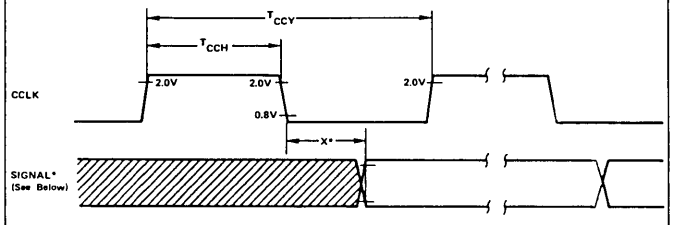
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
Char. Clock Cycle Time	T_{CCY}	0.4	40	0.4	40	µs
Char. Clock Pulse Width	T_{CCH}	200	--	200	--	ns
MA0-MA13 Propagation Delay	T_{MAD}	--	300	--	300	ns
RA0-RA4 Propagation Delay	T_{RAD}	--	300	--	300	ns
DISPLAY ENABLE Prop. Delay	T_{DTD}	--	450	--	450	ns
HYSNC Propagation Delay	T_{HSD}	--	450	--	450	ns
VSYNC Propagation	T_{VSD}	--	450	--	450	ns
Cursor Propagation Delay	T_{CDD}	--	450	--	450	ns
LPEN Strobe Width	T_{LPH}	150	--	150	--	ns
LPEN to CCLK Delay	T_{LP1}	20	--	20	--	ns
CCLK to LPEN Delay	T_{LP2}	0	--	0	--	ns

t_r, t_f = 20 ns (max)

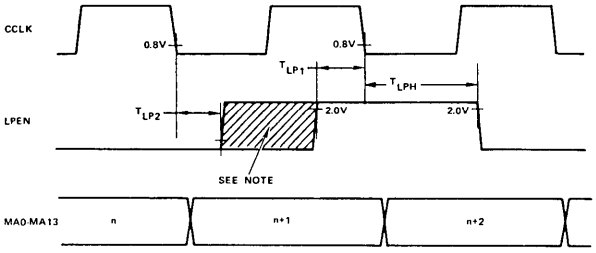
SYSTEM TIMING DEFINITIONS



*

SIGNAL	SIGNAL SYMBOL (X)
MA0-MA13	T_{MAD}
RA0-RA4	T_{RAD}
DISPLAY ENABLE	T_{DTD}
HSYNC	T_{HSD}
VSYNC	T_{VSD}
CURSOR	T_{CDD}

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE:

SLASH AREA DEFINES THE "WINDOW" IN WHICH AN LPEN POSITIVE EDGE WILL CAUSE ADDRESS N+2 TO LOAD INTO LIGHT PEN REGISTER. TRANSITIONS ON EITHER SIDE OF THIS "WINDOW" WILL RESULT IN UNPREDICTABLE VALUES BEING LOADED INTO THE LIGHT PEN REGISTER.

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to 150	°C

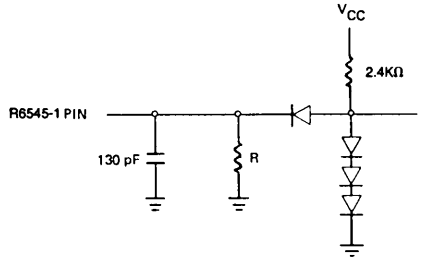
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be taken to prevent unnecessary application of voltages in excess of the allowable limits.

Electrical Characteristics

(V_{CC} = 5.0V ±5%, T_A = 0-70°C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage	V_{IL}	0.3	0.8	Vdc
Input Leakage (Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	I_{IN}	–	2.5	μAdc
Three-State Input Leakage (D0-D7) (V_{IN} = 0.4 to 2.4V)	I_{TSI}	–	10.0	μAdc
Output High Voltage I_{LOAD} = 205 μAdc (D0-D7) I_{LOAD} = 100 μAdc (all others)	V_{OH}	2.4	–	Vdc
Output Low Voltage I_{LOAD} = 1.6 mAdc	V_{OL}	–	0.4	Vdc
Power Dissipation	P_D	–	1000	mW
Input Capacitance				
Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK	C_{IN}	–	10.0	pF
D0-D7		–	12.5	pF
Output Capacitance	C_{OUT}	–	10.0	pF

TEST LOAD



R=11KΩ FOR D0-D7
=24KΩ FOR ALL OTHER OUTPUTS

Rockwell

R6500 Microcomputer System
PRODUCT DESCRIPTION

R6551 Asynchronous Communications Interface Adapter (ACIA)

SECTION 1
INTRODUCTION

The Rockwell R6551 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The R6551 has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times the external clock rate. The R6551 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1-1/2, or 2 stop bits.

The R6551 is designed for maximum programmed control from the CPU, to simplify hardware implementation. Three separate registers permit the CPU to easily select the R6551's operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{\text{RTS}}$ line, receiver interrupt control, and the state of the $\overline{\text{DTR}}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source and baud rate.

The Status Register indicates the states of the $\overline{\text{IRQ}}$, $\overline{\text{DSR}}$, and $\overline{\text{DCD}}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the R6551 Transmit and Receiver circuits.

FEATURES

- Compatible with 8-bit microprocessors
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 2 MHz or 1 MHz operation
- Single 5V ± 5% power supply
- 28-pin plastic or ceramic DIP
- Full TTL compatibility

Specifications subject to change without notice
Document No. 29650 N90
May 1981

SECTION 2
R6551 INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6551 ACIA. Figure 2-1 is the Interface Diagram and Figure 2-2 shows the pin-out configuration for the R6551.

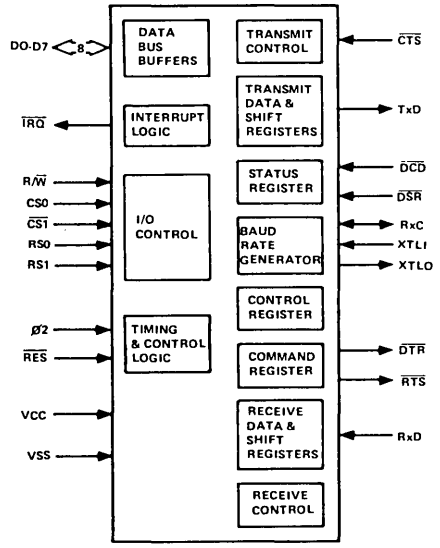


Figure 2-1. R6551 INTERFACE DIAGRAM

2.1 MICROPROCESSOR INTERFACE SIGNAL DESCRIPTION

RES (Reset) (4)

During system initialization a low on the RES input will cause a hardware reset to occur. The Command Register and the Control Register will be cleared. The Status Register will be cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the DSR and DCD lines, and the transmitter Empty bit, which will be set. RES must be held low for one Ø2 clock cycle for a reset to occur.

Ø2 (Input Clock) (27)

The input clock is the system Ø2 clock and is used to clock all data transfers between the system microprocessor and the R6551.

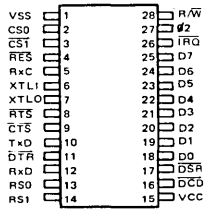


Figure 2-2. R6551 PIN CONFIGURATION

R/W (Read/Write) (28)

The R/W input, generated by the microprocessor, is used to control the direction of data transfers. A high on the R/W pin allows the processor to read the data supplied by the R6551, a low allows a write to the R6551.

IRQ (Interrupt Request) (26)

The IRQ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common IRQ microprocessor input. Normally a high level, IRQ goes low when an interrupt occurs.

D0-D7 (Data Bus) (18-25)

The D0-D7 pins are the eight data lines used to transfer data between the processor and the R6551. These lines are bi-directional and are normally high-impedance except during Read cycles when the R6551 is selected.

CS0, CS1 (Chip Selects)(2,3)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The R6551 is selected when CS0 is high and CS1 is low.

RS0, CS1 (Register Selects)(13,14)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various R6551 internal registers. The following table shows the internal register select coding.

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status register. The Control Register is unchanged by a Programmed Reset. It should be noted that the Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$); these differences are shown in Figures 3-2, 3-3, and 3-4.

2.2 ACIA/MODEM INTERFACE SIGNAL DESCRIPTION

XTLI, XTLO (Crystal Pins) (6, 7)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates (see Section 4.5). Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data) (10)

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

RxD (Receive Data) (12)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

RxC (Receive Clock) (5)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send) (8)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send) (9)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready) (11)

This output pin is used to indicate the status of the R6551 to the modem. A low on $\overline{DTR}$ indicates the R6551 is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready) (17)

The $\overline{DSR}$ input pin is used to indicate to the R6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready".

$\overline{DCD}$ (Data Carrier Detect) (16)

The $\overline{DCD}$ input pin is used to indicate to the R6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

SECTION 3
INTERNAL ORGANIZATION

This section provides a functional description of the R6551. A block diagram of the R6551 is presented in Figure 3-1.

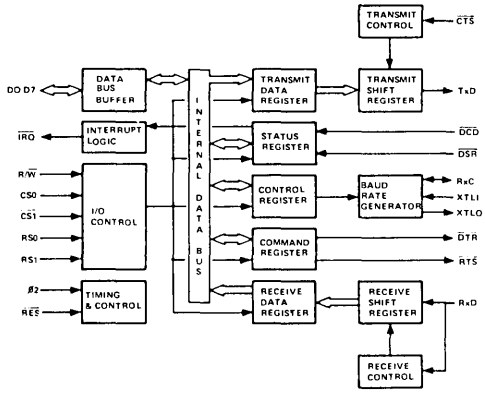


Figure 3-1. INTERNAL ORGANIZATION

3.1 DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{W}$ line is high and the chip is selected, the Data Bus Buffer passes the data from the system data lines to the R6551 internal data bus. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the internal data bus to the system data bus.

3.2 INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

3.3 I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select and Chip Select and Read/Write lines as described in Table 2-3 previously.

3.4 TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system Ø2 clock input. The chip will perform data transfers to or from the microcomputer data bus during the Ø2 high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

3.5 TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the R6551 Transmit and Receive Circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

3.6 STATUS REGISTER

Figure 3-2 indicates the format of the R6551 Status Register. A description of each status bit follows.

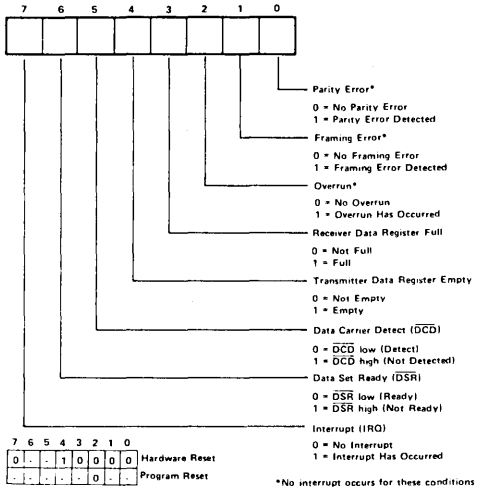


Figure 3-2. STATUS REGISTER FORMAT

3.6.1 Receiver Data Register Full (Bit 3)

This bits goes to a "1" when the R6551 transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a "0" when the processor reads the Receiver Data Register.

3.6.2 Transmitter Data Register Empty (Bit 4)

This bits goes to a "1" when the R6551 transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a "0" when the processor writes new data onto the Transmitter Data Register.

3.6.3 Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the R6551. A "0" indicates a low level (true condition) and a "1" indicates a high (false). Whenever either of these inputs change state, an immediate processor interrupt occurs, unless the R6551 is disabled (bit 0 of the Command Register is a "0"). When the interrupt occurs, the status bits will indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new input levels.

3.6.4 Framing Error (Bit 1), Overrun (2), and Parity Error (Bit 0)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified.

3.6.5 Interrupt (Bit 7)

This bit goes to a "0" when the Status Register has been read by the processor, and goes to a "1" whenever any kind of interrupt occurs.

3.7 CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

3.7.1 Selected Baud Rate (Bits 0, 1, 2, 3)

These bits, set by the processor, select the Transmitter baud rate, which can be at 1/16 an external clock rate or one of 15 other rates controlled by the internal baud rate generator as shown in Figure 3-3.

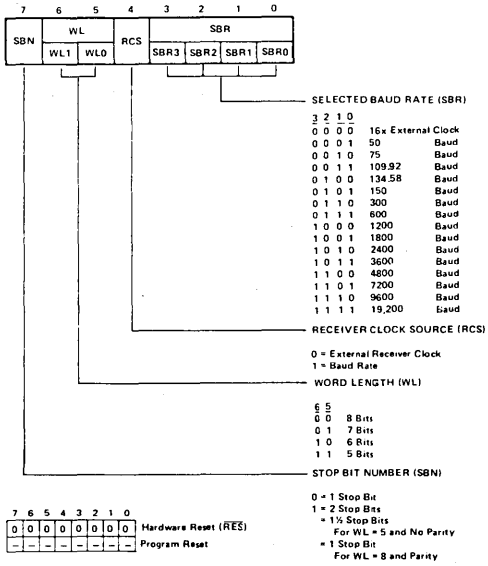


Figure 3-3. R6551 CONTROL REGISTER

3.7.2 Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A "0" causes the Receiver to operate at a baud rate of 1/16 an external clock. A "1" causes the Receiver to operate at the same baud rate as is selected for the transmitter as shown in Figure 3-3.

3.7.3 Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits). Figure 3-3 shows the configuration for each number of bits desired.

3.7.4 Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A "0" always indicates one stop bit. A "1" indicates 1-1/2 stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

3.8 COMMAND REGISTER

The Command Register controls specific modes and functions.

3.8.1 Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A "0" indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A "1" indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low.

3.8.2 Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a "1". The Receiver interrupt is enabled when this bit is set to a "0" and Bit 0 is set to a "1".

3.8.3 Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt. Figure 3-4 shows the various configurations of the $\overline{RTS}$ line and Transmit Interrupt bit settings.

3.8.4 Receiver Echo Mode (Bit 4)

This bit enables the Receiver Echo Mode. Bits 2 and 3 must also be zero. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time. A "1" enables the Receiver Echo Mode. A "0" bit disables the mode.

3.8.5 Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A "0" disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A "1" bit enables generation and checking of parity bits.

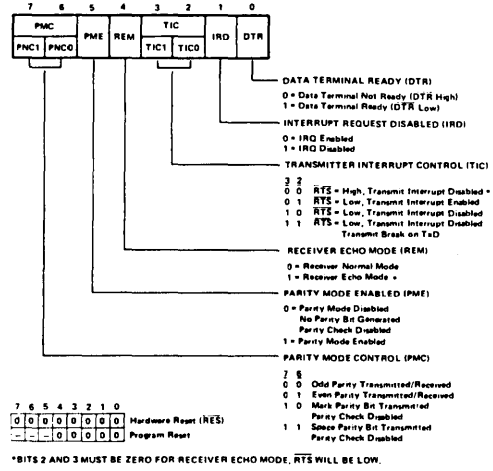


Figure 3-4. R6551 COMMAND REGISTER

3.8.6 Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check). Figure 3-4 shows the possible bit configurations for the Parity Mode Control bits.

3.9 TRANSMITTER AND RECEIVER

Bits 0-3 of the Control Register select divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the R6551. Figure 3-5 shows the transmitter and Receiver layout.

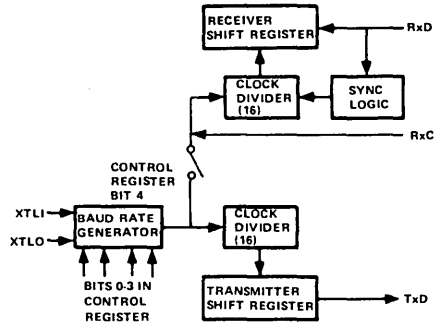


Figure 3-5. TRANSMITTER/RECEIVER CLOCK CIRCUITS

SECTION 4
OPERATION

4.1 TRANSMITTER AND RECEIVER OPERATION

4.1.1 Continuous Data Transmit (Figure 4-1)

In the normal operating mode, the processor interrupt ($\overline{IRQ}$) is used to signal when the R6551 is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the R6551, the interrupt is cleared. The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted.

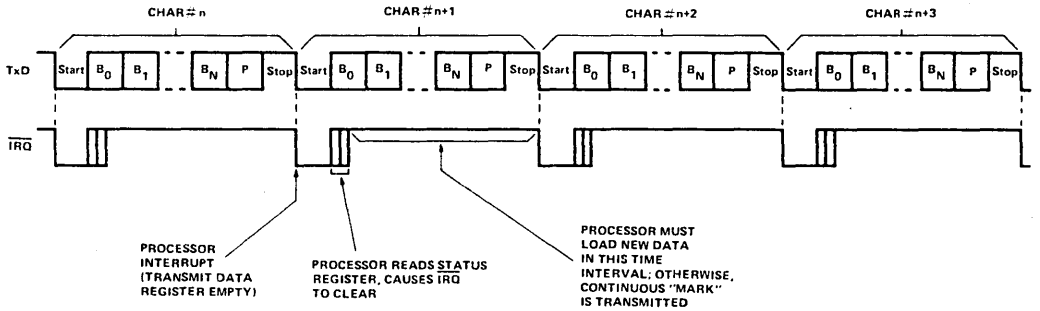


Figure 4-1. CONTINUOUS DATA TRANSMIT

4.1.2 Continuous Data Receive (Figure 4-2)

Similar to the above case, the normal mode is to generate a processor interrupt when the R6551 has received a full data word. This occurs at about the 9/16 point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs.

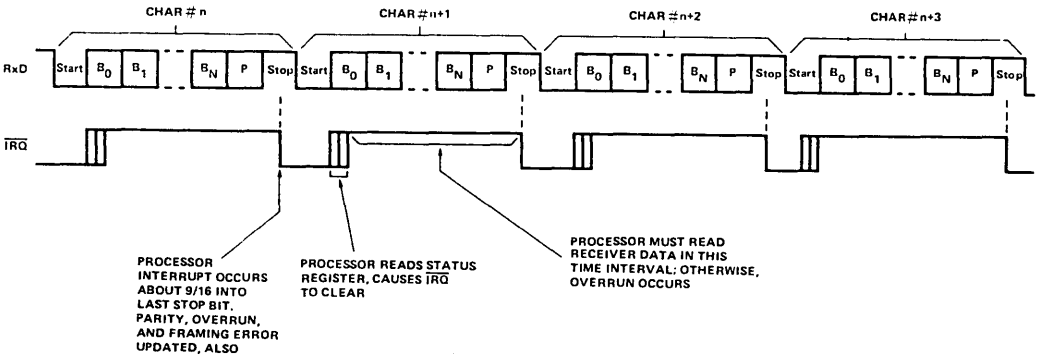


Figure 4-2. CONTINUOUS DATA RECEIVE

4.1.3 Transmit Data Register Not Loaded by Processor (Figure 4-3)

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line will go to the "MARK" condition until the data is loaded. Processor interrupts continue to occur at the same rate as previously, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word.

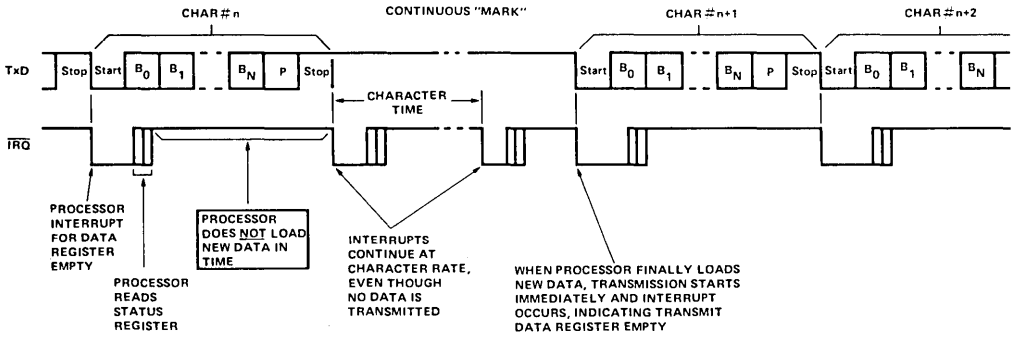


Figure 4-3. TRANSMIT DATA REGISTER NOT LOADED BY PROCESSOR

4.1.4 Effect of $\overline{CTS}$ on Transmitter (Figure 4-4)

$\overline{CTS}$ is the Clear-to-Send Signal generated by the modem. It is normally low (True State) but may go high in the event of some modem problems. When this occurs, the TxD line immediately goes to the "MARK" condition. Interrupts continue at the same rate, but the Status Register does not indicate that the Transmit Data Register is empty. Since there is no status bit for $\overline{CTS}$, the processor must deduce that $\overline{CTS}$ has gone to the FALSE (high) state. This is covered later in this note. $\overline{CTS}$ is a transmit control line only, and has no effect on the R6551 Receiver Operation.

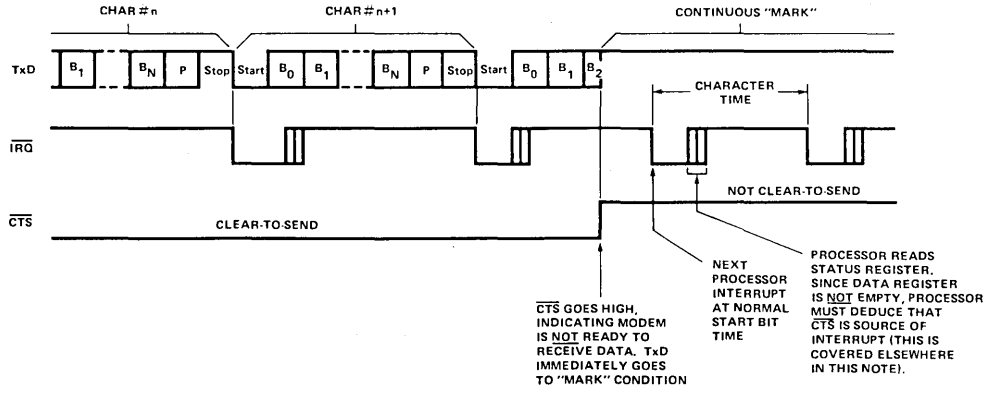


Figure 4-4. EFFECT OF CTS ON TRANSMITTER

4.1.5 Effect of Overrun on Receiver (Figure 4-5)

See 4. 1. 2 for normal Receiver operation. If the processor does not read the Receiver data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost.

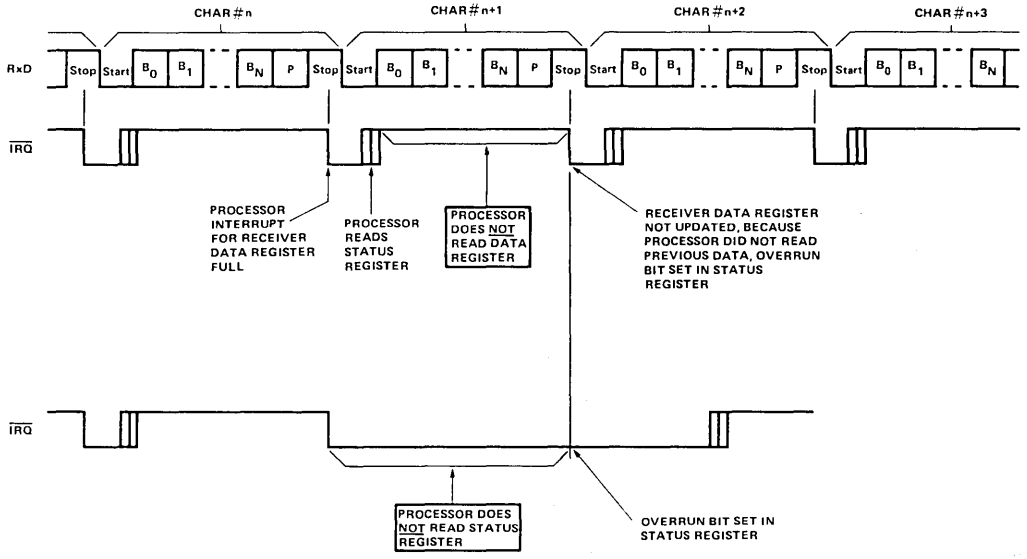


Figure 4-5. EFFECT OF OVERRUN ON RECEIVER

4.1.6 Echo Mode Timing (Figure 4-6)

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by 1/2 of the bit time.

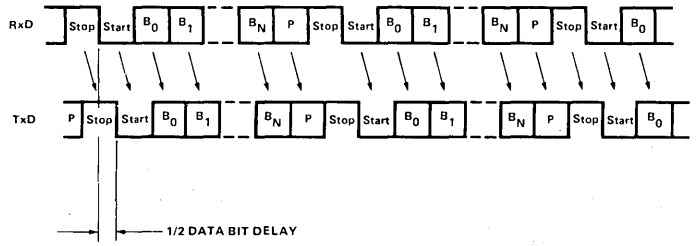


Figure 4-6. ECHO MODE TIMING

4.1.7 Effect of $\overline{CTS}$ on Echo Mode Operation (Figure 4-7)

See 4.1.4 for the effect of $\overline{CTS}$ on the Transmitter. Receiver operation is unaffected by $\overline{CTS}$, so, in Echo Mode, the Transmitter is affected in the same way as 4.1.4. In this case, however, the processor interrupts signify that the Receiver Data Register is full, so the processor has no way of knowing that the Transmitter has ceased to echo.

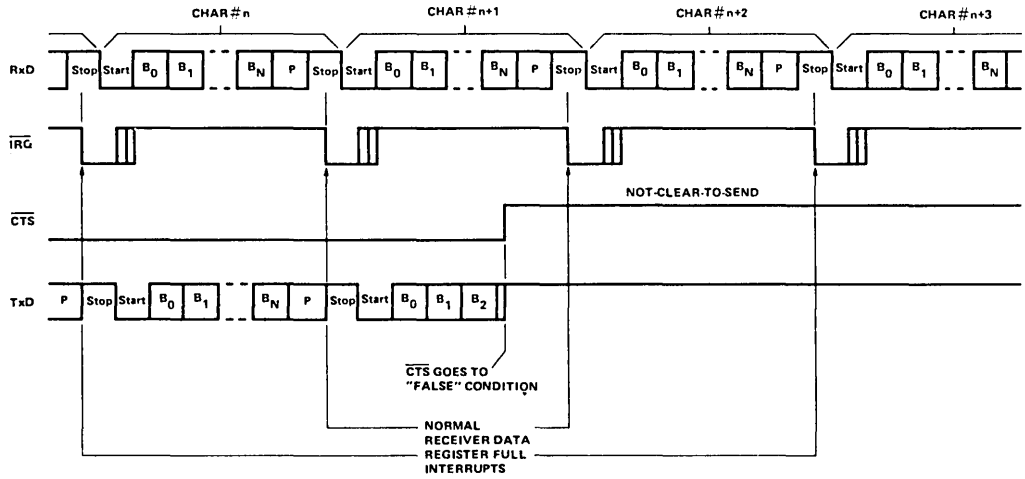


Figure 4-7. EFFECT OF CTS ON ECHO MODE

4.1.8 Overrun in Echo Mode (Figure 4-8)

If Overrun occurs in Echo Mode, the Receiver is affected the same way as described in 4.1.5. For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor.

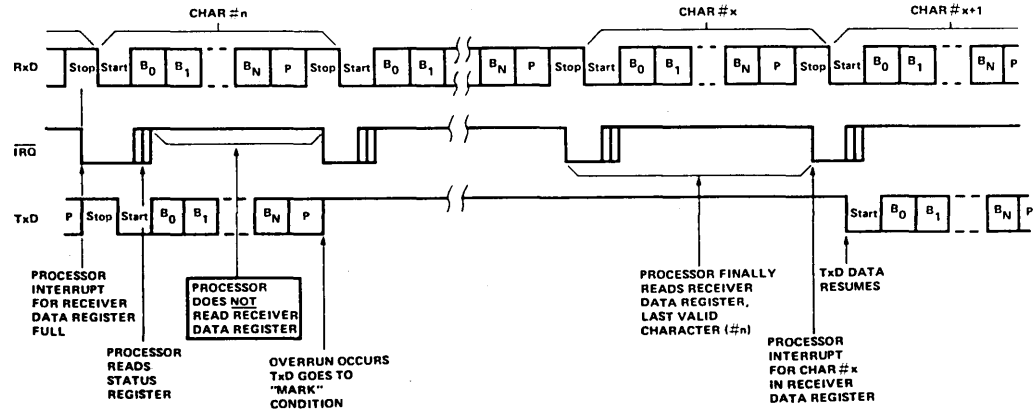


Figure 4-8. OVERRUN IN ECHO MODE

4.1.9 Framing Error (Figure 4-9)

Framing Error is caused by the absence of Stop Bit(s) on received data. The status bit is set when the processor interrupt occurs. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received.

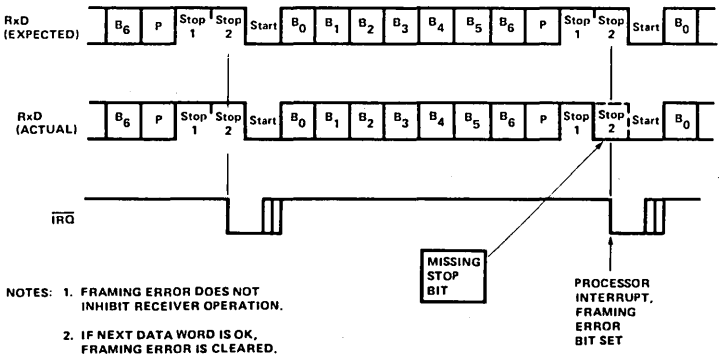


Figure 4-9. FRAMING ERROR

4.1.10 Effect of $\overline{DCD}$ on Receiver (Figure 4-10)

$\overline{DCD}$ is a modem output used to indicate the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data (RxD on the R6551) some time later. The R6551 will cause a processor interrupt whenever $\overline{DCD}$ changes state and will indicate this condition via the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the R6551 automatically checks the level of the $\overline{DCD}$ line, and if it has changed, another interrupt occurs.

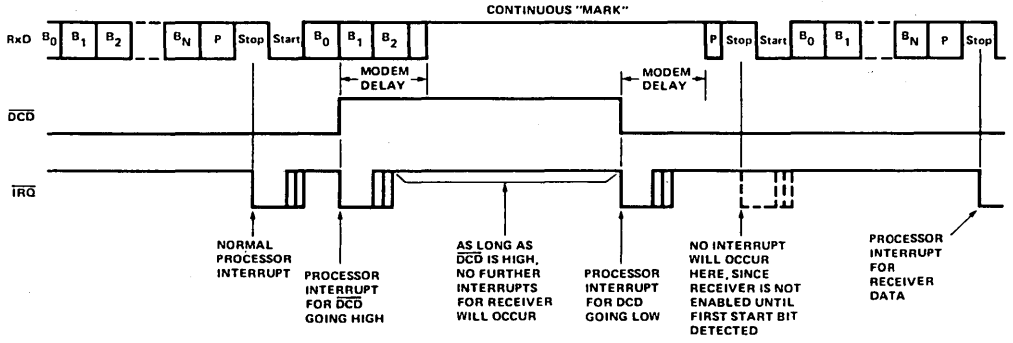


Figure 4-10. EFFECT OF $\overline{DCD}$ ON RECEIVER

4.1.11 Timing with 1-1/2 Stop Bits (Figure 4-11)

It is possible to select 1-1/2 Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the processor interrupt for Receiver Data Register Full occurs in halfway through the trailing half-Stop Bit.

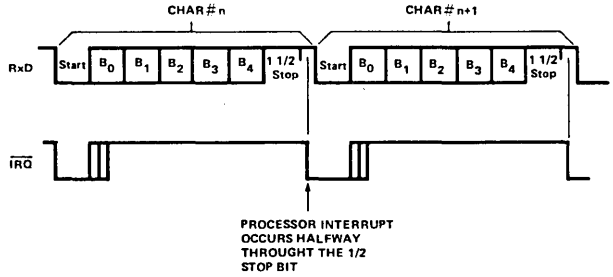


Figure 4-11. TIMING WITH 1-1/2 STOP BITS

4.1.12 Transmit Continuous "BREAK" (Figure 4-12)

This mode is selected via the R6551 Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume.

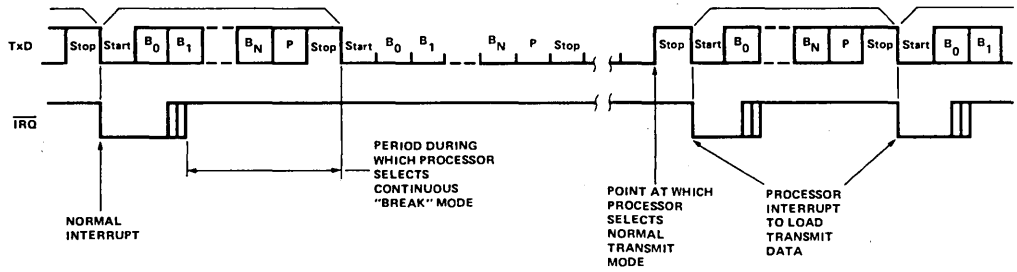


Figure 4-12. TRANSMIT CONTINUOUS "BREAK"

4.1.13 Receive Continuous "BREAK" (Figure 4-13)

In the event the modem transmits continuous "BREAK" characters, the R6551 will terminate receiving. Reception will resume only after a Stop Bit is encountered by the R6551.

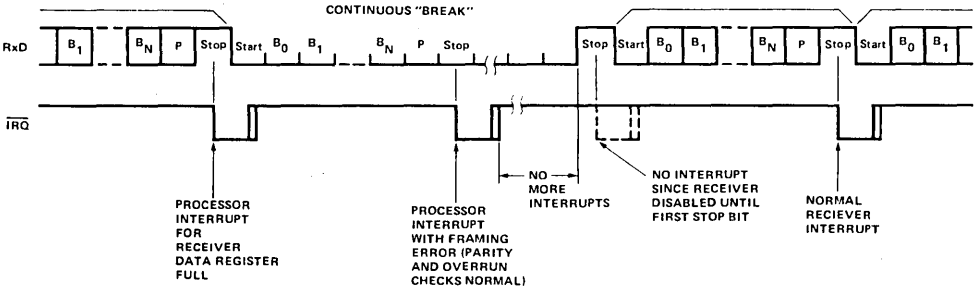


Figure 4-13. RECEIVE CONTINUOUS "BREAK"

4.2 STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the R6551 should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 ($\overline{IRQ}$). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check IRQ Bit

   If not set, interrupt source is not the R6551.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both "0" (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2)

   Only if Receiver Data Register is full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above, then $\overline{CTS}$ must have gone to the FALSE (high) state.

4.3 PROGRAMMED RESET OPERATION

A program reset occurs when the processor performs a write operation to the R6551 with RS0 low and RS1 high. The program reset operates somewhat different from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. The data sheet indicates the effect of a program reset on internal registers.
2. The $\overline{DTR}$ line goes high immediately.
3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.
4. $\overline{DCD}$ and $\overline{DSR}$ interrupts disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.
5. Overrun cleared, if set.

4.4 MISCELLANEOUS NOTES ON OPERATION

1. If Echo Mode is selected, $\overline{RTS}$ goes low.
2. If Bit 0 of Command Register is "0" (disabled), then:
   a) All interrupts disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Transmitter disabled immediately.
   c) Receiver disabled, but a character currently being received will be completed first.

3. Odd parity occurs when the sum of all the "1" bits in the data word (including the parity bit) is odd.
4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but is used to generate parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.
6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the R6551 does not interpret this as a Start Bit, but samples the line again halfway into the bit to determine if it is a true Start Bit or a false one. For false Start Bit detection, the R6551 does not begin to receive data, instead, only a true Start Bit initiates receiver operation.
7. Precautions to consider with the crystal oscillator circuit:
   a) The external crystal to be used should be a "series" mode crystal.
   b) The XTALI input may be used a an external clock input. The unused pin must be floating and may not be used for any other function.
8. $\overline{DCD}$ and $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no affect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to GND or V_{CC}.

4.5 GENERATION OF NON-STANDARD BAUD RATES

4.5.1 Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the R6551 Control Register.

The divisors, then, are determined by bits 0-3 in the Control Register and their values are shown in Figure 4-14.

4.5.2 Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the R6551 with an off-chip oscillator to achieve the same thing. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

CONTROL REGISTER BITS 3	2	1	0	DIVISOR SELECTED FOR THE INTERNAL COUNTER	BAUD RATE GENERATED WITH 1.8432 MHz CRYSTAL	BAUD RATE GENERATED WITH A CRYSTAL OF FREQUENCY (F)
0	0	0	0	No Divisor Selected	16 × External Clock at Pin R × C	16 × External Clock at Pin R × C
0	0	0	1	36.864	$\frac{1.8432 \times 10^6}{36.864} = 50$	$\frac{F}{36.864}$
0	0	1	0	24.576	$\frac{1.8432 \times 10^6}{24.576} = 75$	$\frac{F}{24.576}$
0	0	1	1	16.769	$\frac{1.8432 \times 10^6}{16.769} = 109.92$	$\frac{F}{16.769}$
0	1	0	0	13.704	$\frac{1.8432 \times 10^6}{13.704} = 134.51$	$\frac{F}{13.704}$
0	1	0	1	12.288	$\frac{1.8432 \times 10^6}{12.288} = 150$	$\frac{F}{12.288}$
0	1	1	0	6.144	$\frac{1.8432 \times 10^6}{6.144} = 300$	$\frac{F}{6.144}$
0	1	1	1	3.072	$\frac{1.8432 \times 10^6}{3.072} = 600$	$\frac{F}{3.072}$
1	0	0	0	1.536	$\frac{1.8432 \times 10^6}{1.536} = 1.200$	$\frac{F}{1.536}$
1	0	0	1	1.024	$\frac{1.8432 \times 10^6}{1.024} = 1.800$	$\frac{F}{1.024}$
1	0	1	0	768	$\frac{1.8432 \times 10^6}{768} = 2.400$	$\frac{F}{768}$
1	0	1	1	512	$\frac{1.8432 \times 10^6}{512} = 3.600$	$\frac{F}{512}$
1	1	0	0	384	$\frac{1.8432 \times 10^6}{384} = 4.800$	$\frac{F}{384}$
1	1	0	1	256	$\frac{1.8432 \times 10^6}{256} = 7.200$	$\frac{F}{256}$
1	1	1	0	192	$\frac{1.8432 \times 10^6}{192} = 9.600$	$\frac{F}{192}$
1	1	1	1	96	$\frac{1.8432 \times 10^6}{96} = 19.200$	$\frac{F}{96}$

Figure 4-14. DIVISOR SELECTION FOR THE R6551

4.6 DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating an R6551 ACIA is shown in Figure 4-15.

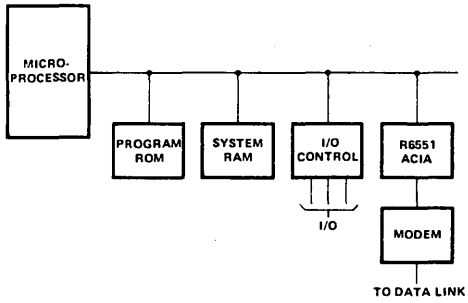


Figure 4-15. SIMPLIFIED SYSTEM DIAGRAM

Occasionally it may be desirable to include in the system a facility for "loop-back" diagnostic testing, of which there are two kinds:

1. Local Loop-Back

   Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

2. Remote Loop-Back

   Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

The R6551 does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry.

Figure 4-16 indicates the necessary logic to be used with the R6551.

The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

1. Disables outputs TxD, $\overline{\text{DTR}}$, and $\overline{\text{RTS}}$ (to Modem).
2. Disables inputs RxD, $\overline{\text{DCD}}$, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs:
   a) TxD to RxD
   b) $\overline{\text{DTR}}$ to $\overline{\text{DCD}}$
   c) $\overline{\text{RTS}}$ to $\overline{\text{CTS}}$

LLB may be tied to a peripheral control pin (from an R6520 or R6522, for example) to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

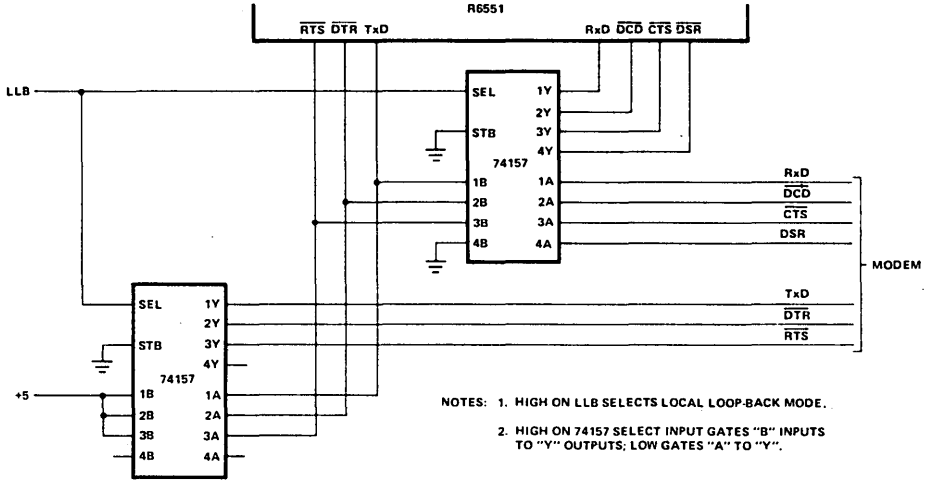


Figure 4-16. LOOP-BACK CIRCUIT SCHEMATIC

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

1. Control Register bit 4 must be "1", so that the transmitter clock = receiver clock.
2. Command Register bit 4 must be "1" to select Echo Mode.
3. Command Register bits 3 and 2 must be "1" and "0", respectively to disable $\overline{IRQ}$ interrupt to transmitter.
4. Command Register bit 1 must be "0" to disable $\overline{IRQ}$ interrupt for receiver.

In this way, the system re-transmits received data without any effect on the local system.

4.7 $\overline{DCD}$ AND $\overline{DSR}$ AS SWITCH SENSE INPUTS

The R6551 (Asynchronous Communication Interface Adapter) has several special-purpose control pins. Among them are the input signals, $\overline{DCD}$ (Data Carrier Detect) and $\overline{DSR}$ (Data Set Ready). The normal functions of these pins are adequately described in the R6551 data sheet and are not covered here. However, it is possible to use these pins as switch sense inputs; that is, as input pins used to detect the state of switches or circuit jumpers in the system.

An important requirement of the use of $\overline{DCD}$ and $\overline{DSR}$ as sense inputs is that they must not normally change state during system operation. If they do, and if the R6551 is enabled, then immediate processor interrupts will occur and normal operation will be interrupted. If, however, these pins are connected to switches or circuit-board jumper wires which do not change state during operation, then they can be sensed by the processor and may be used to select special operating modes.

The circuit connections are quite simple and are outlined in Figure 4-17.

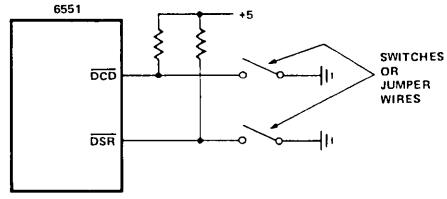


Figure 4-17. CIRCUIT CONNECTIONS FOR $\overline{DCD}$ AND $\overline{DSR}$

Note that pull-up resistors are required, since $\overline{DCD}$ and $\overline{DSR}$ are high-impedance inputs on the R6551.

In order to sense the state of the inputs, it is necessary to do the following:

1. Disable the R6551 by setting bit 0 of the Command Register to a "0".
2. Read the R6551 Status Register. Bits 5 and 6 will then indicate the levels on $\overline{DCD}$ and $\overline{DSR}$, respectively. A "0" is a low level and a "1" is a high.

As long as the R6551 is disabled, the Status Register will reflect the levels on the pins and no interrupts will occur, even if the pins change state. However, if the R6551 is enabled, then changes of state of the $\overline{DCD}$ and $\overline{DSR}$ levels cause immediate interrupts and the Status Register indicates the levels taken on the interrupt. Subsequent level changes are not indicated by the Status Register until the interrupt is serviced. Thus, it is not convenient to use DCD and DSR as general switching inputs, but they may easily be used as inputs which do not change regularly.

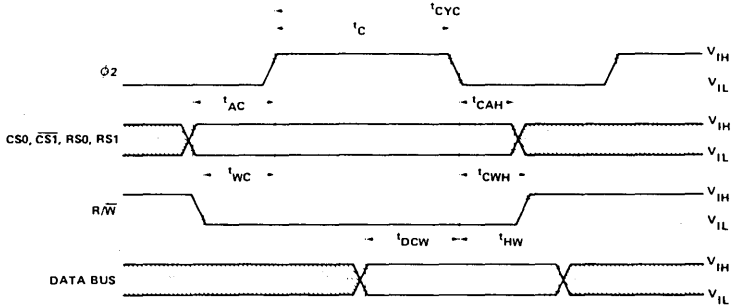
APPENDIX
CHARACTERISTICS AND RATINGS

READ/WRITE CYCLE CHARACTERISTICS

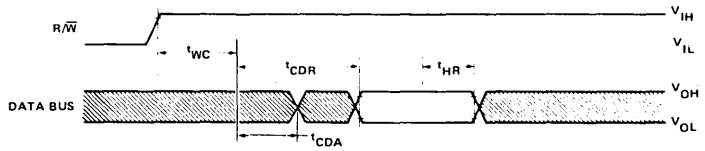
(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	μs
Ø2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{AC}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WC}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)



Write Timing Characteristics



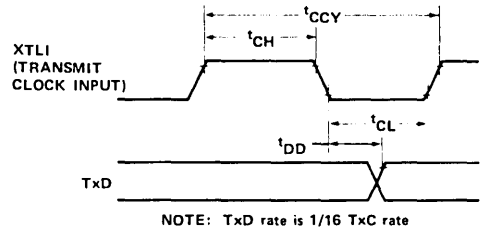
Read Timing Characteristics

TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTLI to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
$\overline{RTS}$ Propagation Delay	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

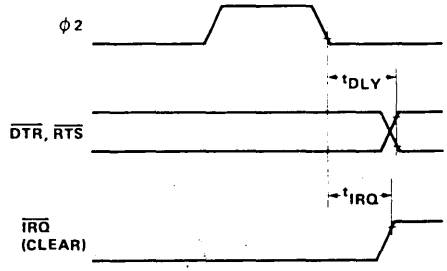
(t_r, t_f = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

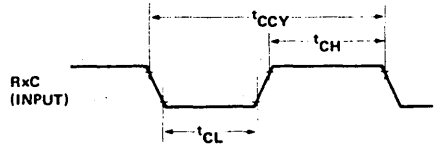


NOTE: TxD rate is 1/16 TxC rate

Transmit Timing with External Clock



Interrupt and Output Timing

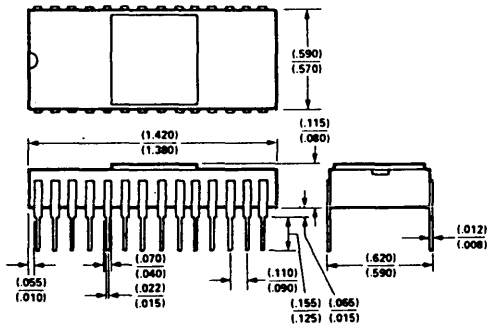


NOTE: RxD rate is 1/16 RxC rate

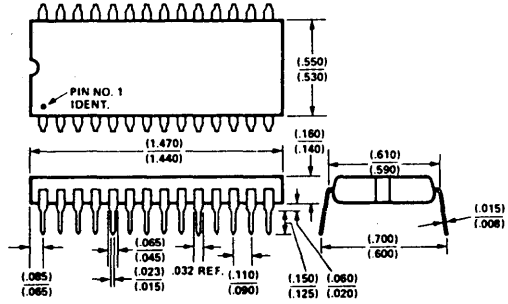
Receive External Clock Timing

PACKAGE OUTLINES

28 LEAD CERAMIC



28 LEAD PLASTIC



SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature	T	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics

(V_{CC} = 5.0 ±5%, T_A = 0-70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}				V
(Except XTLI and XTLO)		2.0	–	V_{CC}	
(XTLI and XTLO)		2.4	–	V_{CC}	
Input Low Voltage	V_{IL}				V
(Except XTLI and XTLO)		V_{SS}	–	0.8	
(XTLI and XTLO)		V_{SS}	–	0.4	
Input Leakage Current: V_{IN} = 0 to 5V. (Ø2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	–		±2.5	µA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	–		±10.0	µA
Output High Voltage: I_{LOAD} = -100 µA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	2.4	–	–	V
Output Low Voltage: I_{LOAD} = 1.6 mA (D0-D7), TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	–	–	0.4	V
Output High Current (Sourcing): V_{OH} = 2.4V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	-100		–	µA
Output Low Current (Sinking): V_{OL} = 0.4V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	I_{OL}	1.6	–	–	mA
Output Leakage Current (off state): V_{OUT} = 5V ($\overline{IRQ}$)	I_{OFF}	–		10.0	µA
Clock Capacitance (Ø2)	C_{CLK}	–	–	20	pF
Input Capacitance (except XTLI and XTLO)	C_{IN}	–	–	10	pF
Output Capacitance	C_{OUT}	–	–	10	pF
Power Dissipation	P_D	–	170	300	mW

DOCUMENT NO. 29000D58
JUNE 1979

PART NUMBER
R6592

Rockwell

R6500 Microcomputer System
DATA SHEET

SINGLE-CHIP PRINTER CONTROLLER

INTRODUCTION

The Rockwell R6592 is a single-chip printer controller for eight different EPSON* dot-matrix impact printers, models 210, 220, 240, 511L, 512, 522, 541L, and 542. The R6592 offers the flexibility to support any of these models with a minimum of circuitry. Generation of 96 standard ASCII upper and lower case characters and 6 special characters is provided. In addition, up to 10 ASCII control commands are accepted, depending upon the printer. Logic is included in the R6592 to print up to 26 columns on the 210, 220, and 240 models, and up to 40 columns on the 511L, 512, 522, 541L, and 542 models.

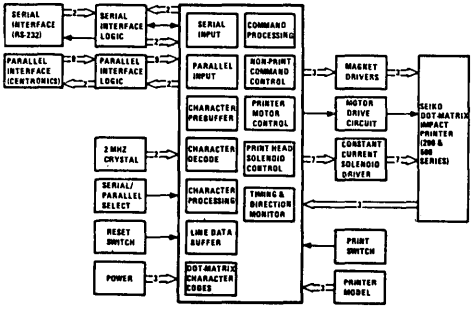
Input data may be selected to be in the RS-232 serial format with selectable baud rate from 50 to 7200 bits/second or the parallel format. External circuitry is required to convert RS-232 logic levels to R6592 interface logic levels. An external latch may be required for the R6592 to sample parallel data. If both selectable serial and parallel data interface capability is desired, two external multiplexers are required; one to combine four serial baud select lines and four parallel data interface lines into four R6592 input lines and the other to combine two serial data/control lines and two parallel control lines into two other R6592 input lines.

This data sheet summarizes the interface specifications of the R6592. Product Description 29650N56 describes the operation of the R6592 in detail.

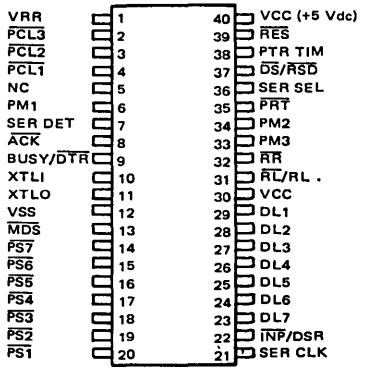
*EPSON is a trade name of Shinshu Seiki Co., Ltd., a member of the Seiko Group. EPSON printers are distributed in the United States by C. Itoh Electronics, Inc. The R6592 meets the printer specifications listed in this data sheet.

FEATURES

- Controls EPSON Dot-Matrix Impact Printers:
  - Model 210
  - Model 220
  - Model 240
  - Model 511L
  - Model 512
  - Model 522
  - Model 541L
  - Model 542
- Minimal Support Circuitry Required
- On-Chip 5 x 7 Dot-Matrix Character Generation
- 96 Standard Upper and Lower Case ASCII Characters (7 Bit Code)
- Six Special ASCII Characters (7 Bit Code)
- Up to 10 ASCII Commands Accepted (Printer Dependent)
- Selectable Serial or Parallel Input Data Operation
- Centronics Standard Parallel Interface
  - Seven Data Lines Plus Data Strobe and Input Drive Input
  - Busy and Acknowledge Output
- RS-232C Serial Interface
  - Baud Rate from 50 to 7200 Bits per Second
  - Received Data and Data Set Ready Input
  - Data Terminal Ready Output
- Single +5V ±10% power supply
- 40 pin plastic or ceramic DIP
- 1 MHz operation (2 MHz external crystal)



R6592 Interface Diagram



R6592 Pin Configuration

SINGLE-CHIP PRINTER CONTROLLER

Specifications subject to change without notice

INTERFACE SIGNALS

PRINTER SOLENOID 1 ($\overline{PS1}$)
PRINTER SOLENOID 2 ($\overline{PS2}$)
PRINTER SOLENOID 3 ($\overline{PS3}$)
PRINTER SOLENOID 4 ($\overline{PS4}$)
PRINTER SOLENOID 5 ($\overline{PS5}$)
PRINTER SOLENOID 6 ($\overline{PS6}$)

Active low output signals used to command seven constant current print head solenoid drivers. When low, the respective solenoid will be energized to print a dot; and when high, the solenoid will be de-energized to not print a dot. Each solenoid line corresponds to a dot position on the seven row print head. Line $\overline{PS1}$ corresponds to the top dot and $\overline{PS7}$ corresponds to the bottom dot. The output lines are activated by the positive edge of the timing signal (TIM). The TIM signal should also be used to gate PS1 through PS7 to the current drivers and to de-energize the current driver inputs within 600 ± 20 μsec of the start of the TIM signal by means of a one-shot flip-flop.

PRINTER CONTROL LINE 1 ($\overline{PCL1}$)
PRINTER CONTROL LINE 2 ($\overline{PCL2}$)
PRINTER CONTROL LINE 3 ($\overline{PCL3}$)

Active low output control lines used to issue various non-print commands to the printer. These lines are inputs to +24V drivers. When low, these lines cause magnets to be energized in the printer; when high, the magnets are to be de-energized. These lines are assigned to specific signals depending upon printer model:

Printer Model	R6592 Signal Name		
	PCL1	PCL2	PCL3
210	NA	Paper Feed	Change Color
220	Paper Feed (R)	Paper Feed (L)	
240	NA	Paper Feed	Slip Release
511L	NA	Paper Feed	NA
512	NA	Paper Feed	NA
522	Paper Feed (R)	Paper Feed (L)	Stamp & Cut Paper
541L	NA	Paper Feed	Paper Release
542	NA	Paper Feed	Paper Release
NA = Not Assigned			

TIMING (TIM)
RESET LEFT ($\overline{RL}$/RL)
RESET RIGHT ($\overline{RR}$)

Input signals used to indicate print cycle Timing. The R6592 initiates a print cycle on the leading edge (positive transition) of the TIM signal information to the R6592. The RESET signals are active low for the 500 series ($\overline{RR}$ and $\overline{RL}$) and are active high for the 200 series (RL). The printer timing and reset lines are assigned as follows:

Printer Model	R6592 Signal		
	TIM	$\overline{RL}$/RL	$\overline{RR}$
210	T Detector	R Detector (RL)	NA
220	T Detector	R Detector (RL)	NA
240	T Detector	R Detector (RL)	NA
511L	Timing Signal	Reset Signal R-L ($\overline{RL}$)	NA
512	Timing Signal	Reset Signal R-L ($\overline{RL}$)	Reset Signal R-R ($\overline{RR}$)
522	Timing Signal	Reset Signal R-L ($\overline{RL}$)	Reset Signal R-R ($\overline{RR}$)
541L	Timing Signal	Reset Signal R-L ($\overline{RL}$)	NA
542	Timing Signal	Reset Signal R-L ($\overline{RL}$)	Reset Signal R-R ($\overline{RR}$)

See Detail Timing Diagrams in Printer Specifications.

MOTOR DRIVE SIGNAL ($\overline{MDS}$)

Active low output signal used to control application of power from a driver circuit to the printer motor. When high, the motor drive is turned off and when low, the motor drive is turned on. The driver circuit for the 500 series must supply 10 to 30 ma at TTL levels. The driver circuit for the 200 series must additionally provide motor braking.

PRINTER MODEL 1 (PM1)
PRINTER MODEL 2 (PM2)
PRINTER MODEL 3 (PM3)

Encoded input lines used to determine which printer model is connected to the R6592. A connection to GND (low) causes "0" to be read. An open input (high) causes logic "1" to be read. The encoding for the printer model is:

Printer Model	Printer Model Line		
	PM3	PM2	PM1
210	0	0	0
220	0	0	1
240	0	1	0
511L	0	1	1
512	1	0	0
522	1	0	1
541L	1	1	0
542	1	1	1

PRINT ($\overline{PRT}$)

Active low input line used to command R6592 to print a line. When low (GND) print commands will continue to be issued. If the print buffer is partially filled, a line will be printed. Line feeds will subsequently be issued while $\overline{PRT}$ is low. When high (open), print commands will not be issued.

SERIAL SELECT (SER SEL)

Active high input line used to indicate the desired data transmission mode to the R6592. When high (open), input data will be received and processed from the serial interface (RS-232C). When low (GND), input data will be received and processed from the parallel interface (Centronics).

If both transmission modes are to be implemented (but not simultaneously), the SER SEL line should be used to select either serial or parallel signals through multiplexer circuits. If either serial or parallel data transmission is exclusively used, multiplexing of the indicated serial/parallel signals is not required.

DATA LINE 1/BAUD RATE 1 (DLI/BR1)
DATA LINE 2/BAUD RATE 2 (DL2/BR2)
DATA LINE 3/BAUD RATE 3 (DL3/BR3)
DATA LINE 4/BAUD RATE 4 (DL4/BR4)

Active high input signals used as parallel data lines if parallel data transfer mode is selected, or used as baud rate select lines if serial data transfer mode is selected.

If parallel data transfer mode is selected (SER SEL = low) these lines represent four of the seven total data lines (see below). DL1/BR1 represents the least significant bit when ASCII characters are decoded.

If serial data transfer mode is selected (SER SEL = high), the data transfer baud rate in bits per second is:

Baud	Data Line/Baud Rate Line			
	DL4/BR4	DL3/BR3	DL2/BR2	DL1/BR1
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
135	0	0	1	1
150	0	1	0	0
300	0	1	0	1
600	0	1	1	0
1200	0	1	1	1
1800	1	0	0	0
2400	1	0	0	1
3600	1	0	1	0
4800	1	0	1	1
7200*	1	1	0	0

Note: 1 = High (open), 0 = Low (GND).
*Data cannot be sent to the R6592 while the print head is moving.

DATA LINE 5 (DL3)
DATA LINE 6 (DL4)
DATA LINE 7 (DL7)

Active high input signals used as data lines when parallel data transfer mode is selected (SER SEL = low). DL7 represents the most significant bit (MSB) when ASCII characters are decoded. Not used when serial data transfer mode is selected (SER SEL = high).

INPUT PRIME ($\overline{IP}$)/DATA SET READY (DSR)

Input line multiplexed between a parallel communications control line (INPUT PRIME) and a serial communications control line (DATA SET READY).

If the parallel data transfer mode is selected (SER SEL = low), this line is assigned to INPUT PRIME ($\overline{IP}$). When $\overline{IP}$/DSR is high, the R6592 issues prints commands to the printer in a normal fashion. When $\overline{IP}$/DSR is low, the R6592 will disable printing. This line can, therefore, be used as a print disable line to selected printers in a multiprinter system.

If the serial data transfer mode is selected (SER SEL = high), the line is assigned to DATA SET READY (DSR). When high, DSR indicates that the transmitter is operative and the R6592 will accept data. When low, DSR indicates that the transmitter is not ready to operate and the R6592 will not accept serial data.

DATA STROBE ($\overline{DS}$)/RECEIVED SERIAL DATA ($\overline{RSD}$)

Input line multiplexed between a parallel communications control line (DATA STROBE) and the serial communications data line (RECEIVED SERIAL DATA).

If the parallel data transfer mode is selected (SER SEL = low), this line is assigned to the DATA STROBE ($\overline{DS}$). When $\overline{DS}$ goes low, the R6592 detects the negative transition, and samples the data on the parallel data lines. The data must be present on the data lines for at least 50 µsec after $\overline{DS}$ goes low.

If the serial data transfer mode is selected (SER SEL = high), the line is assigned to RECEIVED SERIAL DATA ($\overline{RSD}$). The data is processed in accordance with the selected baud rate. The data must be converted from RS-232 logic levels to R6592 logic levels. The R6592 logic state is inverted from RS-232 logic state.

BUSY/DATA TERMINAL READY (BUSY/$\overline{DTR}$)

Output line multiplexed between a parallel communication control line (BUSY) and a serial communication control line (DATA TERMINAL READY).

If the parallel data transfer mode is selected (SER SEL = low), this line is assigned to BUSY. When high, BUSY indicates that the R6592 cannot receive data. When low, BUSY indicates that the R6592 is ready to receive data. BUSY is switched high during character print and while non-print commands are being processed.

If the serial data transfer mode is selected (SER SEL = high), this line is assigned to DATA TERMINAL READY ($\overline{DTR}$). When high, $\overline{DTR}$ indicates that the R6592 cannot receive data. When low, $\overline{DTR}$ indicates that the R6592 is ready to receive data. $\overline{DTR}$ is switched high during character print and while non-print commands are being processed.

ACKNOWLEDGE ($\overline{ACK}$)

Active low output signal used to inform the parallel data transmitter that an input character has been received. $\overline{ACK}$ is switched low for 5 µsec to indicate receipt of a character.

SERIAL CLOCK (SER CLK)

A bi-directional line used to detect the start of the received serial data and to then clock in the serial data bits. When DET ENA is low, this line monitors the input serial data stream for the start bit. When the leading (falling) edge of the start bit is detected, the DET ENA is switched high and this line is switched to an output. Output pulses are generated on this line to clock the received serial data into the R6592 at the selected baud rate.

SERIAL DETECT ENABLE (DET ENA)

Active high output used to enable the received serial data onto the SER CLK line. Upon detection of the received serial start bit, this line is switched low to disable the received serial data from being placed on the SER CLK line.

PRIMARY POWER (VCC)

R6592 primary power supply: +5V ±10%. Supplies power to CPU, I/O, timer and supporting circuitry.

RAM POWER (VRR)

R6592 RAM power supply: +5V ±10%. Supplies power to the internal R6592 RAM. This line should be connected to VCC power supply.

SIGNAL GROUND (VSS)

R6592 power and signal ground.

XTLI

Input from 2 MHz crystal.

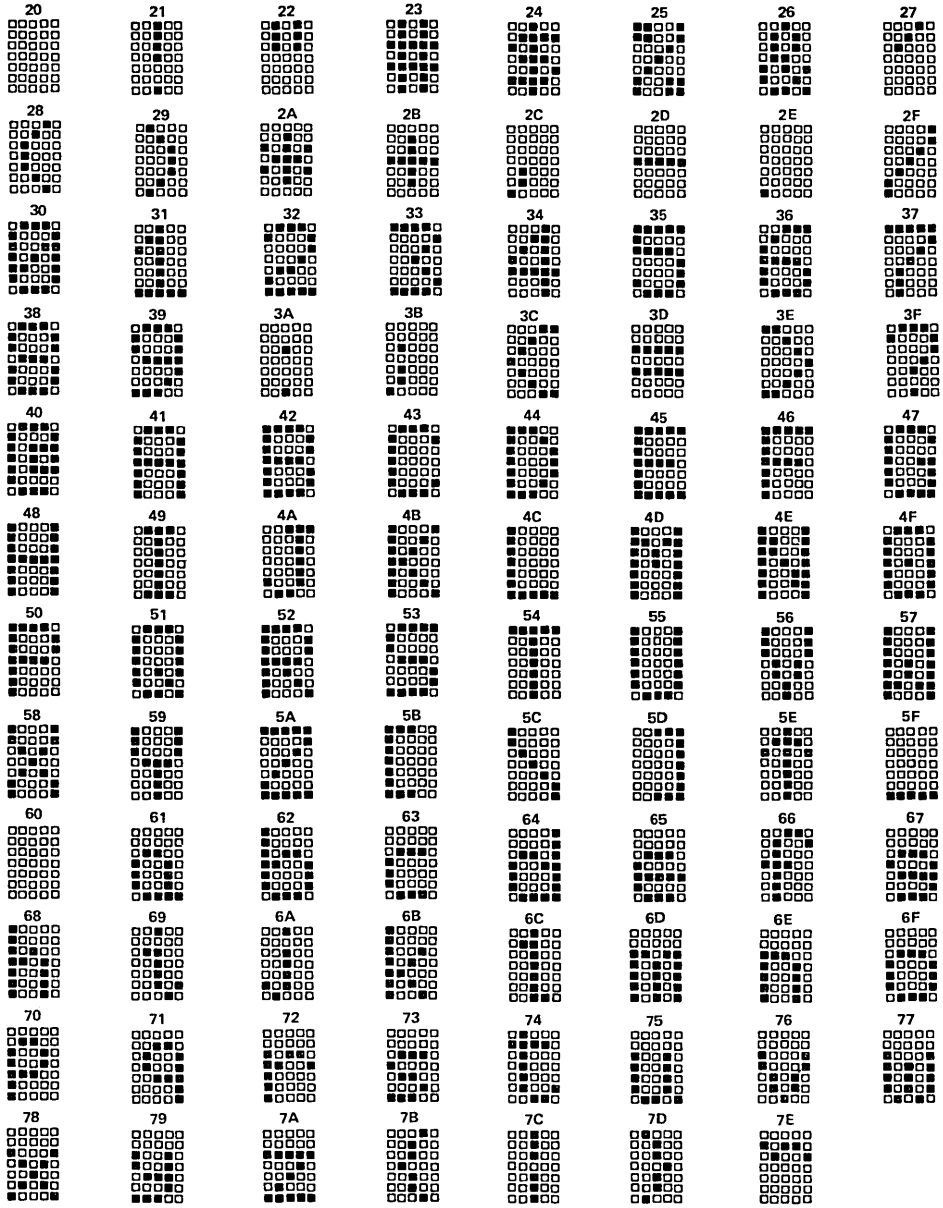
XTLO

Output to 2 MHz crystal.

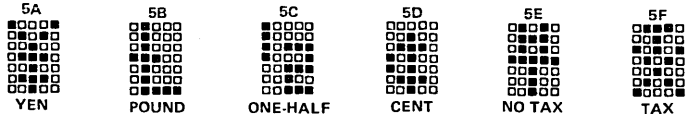
RESET ($\overline{RES}$)

Active low signal used to reset and initialize the R6592. Must be held low for at least 8 µsec after VCC reaches operating voltage and the clock frequency on XTLO has stabilized.

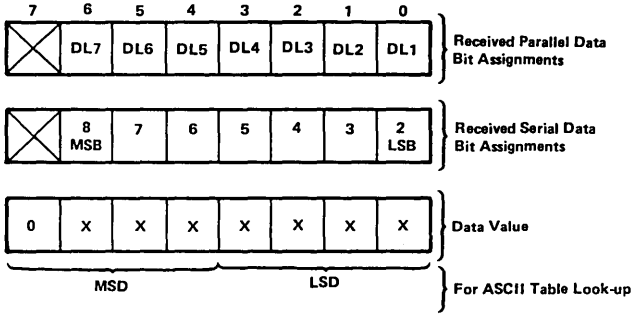
Standard 96 Character 5x7 Matrix Dot Patterns



Special 6 Character 5x7 Matrix Dot Patterns



R6592 Internal Data Format for 7-Bit ASCII Table Character Look-up



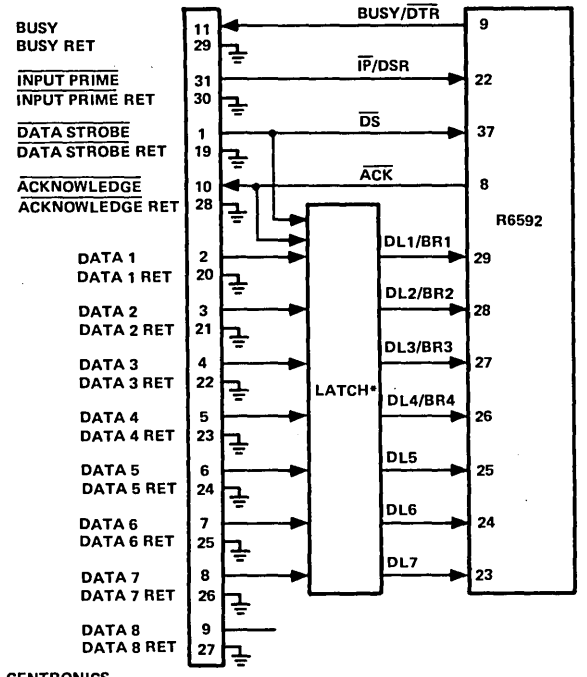
ASCII 7-Bit Code Character Set Table

LSD	MSD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000			SP	0	@	P		p
1	0001		DC1	!	1	A	Q	a	q
2	0010		DC2	"	2	B	R	b	r
3	0011		DC3	#	3	C	S	c	s
4	0100		DC4	$	4	D	T	d	t
5	0101			%	5	E	U	e	u
6	0110			&	6	F	V	f	v
7	0111			'	7	G	W	g	w
8	1000		CAN	(	8	H	X	h	x
9	1001			)	9	I	Y	i	y
A	1010	LF	¥	*	:	J	Z	j	z
B	1011	VT	t	+	;	K	[	k	{
C	1100	FF	1_2	,	<	L	\	l	|
D	1101	CR	¢	–	=	M	]	m	}
E	1110		NT	.	>	N	↑	n	~
F	1111		TX	/	?	O	←	o	DEL

LF – Line Feed
VT – Vertical Tabulation
FF – Form Feed
CR – Carriage Return
DC1 – Device Control 1
DC2 – Device Control 2
DC3 – Device Control 3
DC4 – Device Control 4
CAN – Cancel
¥ – Yen
t – Pound
¢ – Cent
1_2 – One-Half
NT – No Tax
TX – Tax

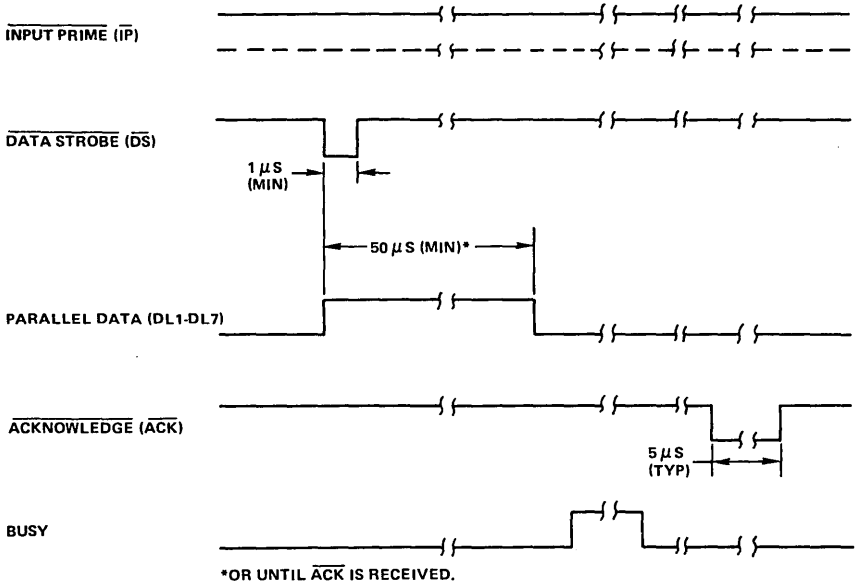
Note: Valid control commands are dependent upon printer model.

Parallel Data Interface



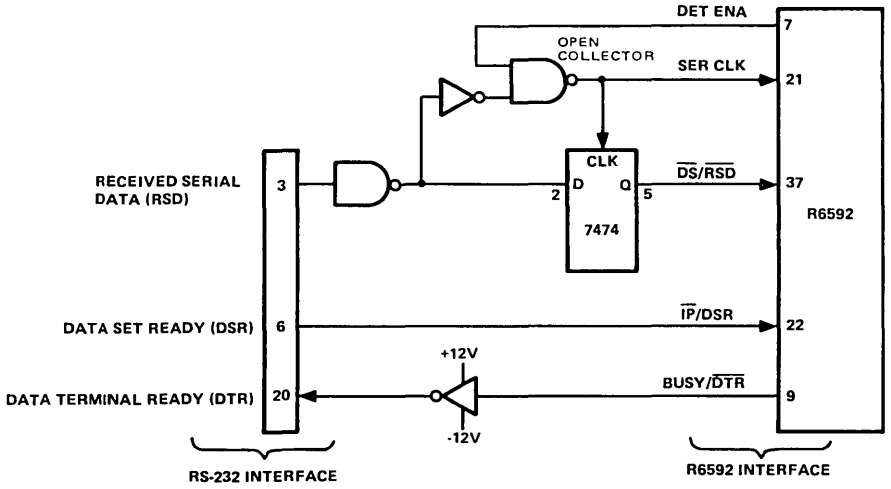
*NOT REQUIRED IF PARALLEL DATA IS HELD FOR ≥50μS AFTER LEADING EDGE OF $\overline{DS}$ OR UNTIL $\overline{ACK}$ IS RECEIVED.

Parallel Data Timing

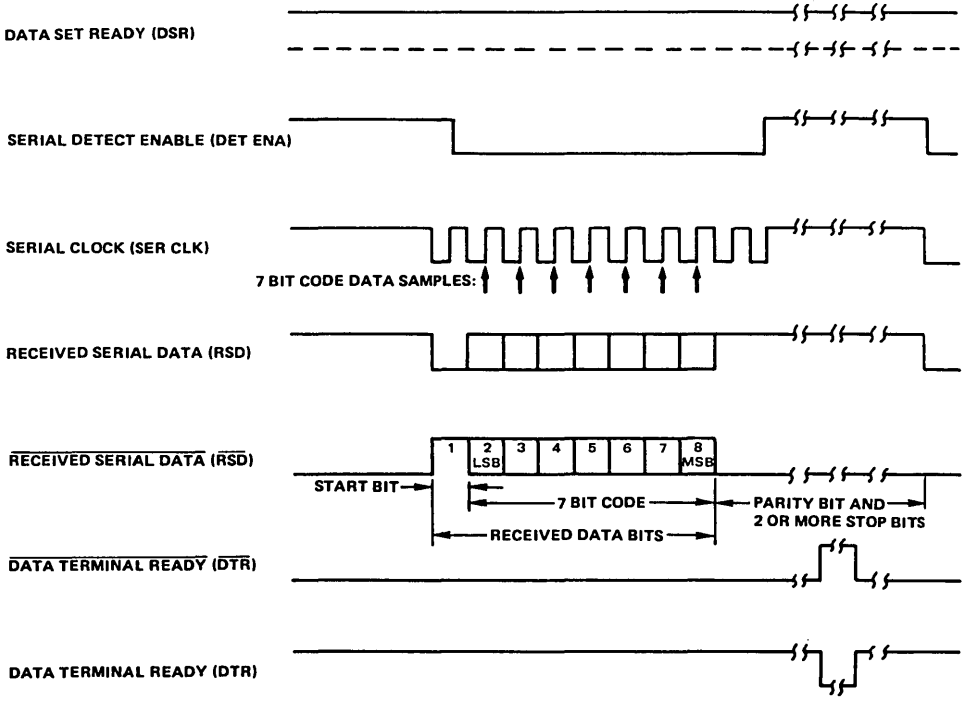


*OR UNTIL $\overline{ACK}$ IS RECEIVED.

Serial Data Interface



Serial Data Timing



PRINTER INTERFACE SPECIFICATIONS

The R6592 is designed to meet the interface requirements stated in the following printer specifications:

Model-210 Impact Dot Matrix Mini-Printer (Preliminary) Rev. 4, AUGUST 30, 1978

Model-220 Impact Dot Matrix Mini-Printer, SEPTEMBER 18, 1978

Model-240 Impact Dot Matrix Mini-Printer, SEPTEMBER 18, 1978

Model-511L Impact Dot Matrix Printer (Enlarged Character) Revision 1, JULY 13, 1978

Model 512 Dot-Matrix Impact Printer (P512DF), APRIL 10, 1978

Model 522 Dot-Matrix Impact Printer (P522DF), MARCH 1, 1978

Model 541L Impact Dot Matrix Printer (Enlarged Character), Revision 1, JULY 19, 1978

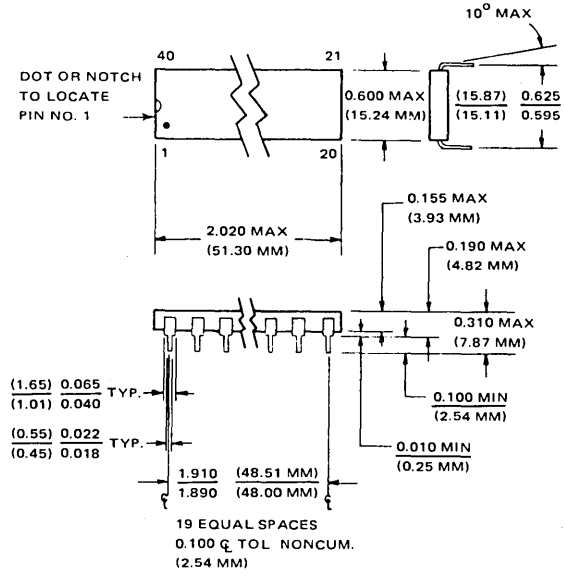
Model 542 Dot-Matrix Impact Printer (P542DF), MARCH 1, 1978

For further printer information, contact:

EPSON America, Inc.
23844 Hawthorne Blvd. Ltd.
Torrance, CA 90505
Phone: (213) 378-2220
TWX: 910-344-7390

C. Itoh Electronics, Inc.
5301 Beethoven Street
Los Angeles, Calif. 90066
Phone: (213) 390-7778
Telex: WU 65-2451

C. Itoh Electronics, Inc.
280 Park Avenue
New York, New York, 10017
Phone: (212) 682-0420
Telex: WUD-12-5059



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

R6592 Plastic Packaging Diagram

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Static D.C. Characteristics V_{CC} = 5V ±10%

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High)	P_D	–	500	–	mW
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	–	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	–	+0.8	Vdc
Input Threshold Voltage	V_{IT}	0.8	–	2.0	Vdc
Input Leakage Current	I_{IN}				μAdc
V_{in} = 0 to 5.0 Vdc		–	±1.0	±2.5	
$\overline{RES}$					
Input High Voltage (XTLI)	V_{IHXT}	+4.0	–	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	-0.3	–	+0.8	Vdc
Input Low Current	I_{IL}				
(V_{IL} = 0.4 Vdc)		–	-1.0	-1.6	mAdc
Output High Voltage	V_{OH}				
(V_{CC} = min, I_{Load} = -100 μAdc)		2.4	–	–	Vdc
Output Low Voltage	V_{OL}				
(V_{CC} = min, I_{Load} = 1.6 mAdc)		–	–	+0.4	Vdc
Output High Current (Sourcing)	I_{OH}				
(V_{OH} = 2.4 Vdc)		-100		–	μAdc
Output Low Current (Sinking)	I_{OL}				
(V_{OL} = 0.4 Vdc)		1.6	–	–	mAdc
Input Capacitance	C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)					
Pins 2-9, 13-29 and 31-38		–	–	10	
XTLI, XTLO		–	–	50	
Output Capacitance	C_{out}				
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)		–	–	10	pF

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

R6500
MEMORY I/O
COMBOS

DOCUMENT NO. 29000 D41
REV. 4, FEBRUARY 1979

PART NUMBER
R6530

Rockwell

R6500 Microcomputer System
DATA SHEET

ROM-RAM-I/O-INTERVAL TIMER DEVICE (RRIOT)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-channel, Silicon-Gate technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips — the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices. Rockwell also provides memory and I/O devices that further enhance the cost-effectivity of the R6500 microcomputer system . . . as well as low-cost design aids and documentation.

FEATURES

- 8 bit bidirectional Data Bus for direct communication with the microprocessor
- 1024 x 8 ROM
- 64 x 8 static RAM
- Two 8 bit bidirectional data ports for interface to peripherals
- Two programmable Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Bus
- Allows up to 7K contiguous bytes of ROM with no external decoding

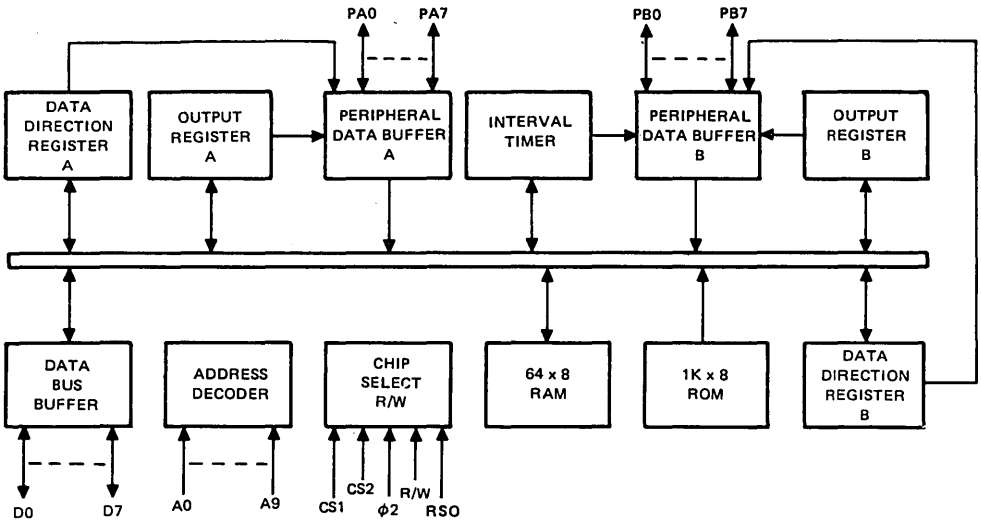
DESCRIPTION

The R6530 is designed to operate in conjunction with the R6500 Microprocessor Family. It is comprised of a mask programmable 1024 x 8 ROM, a 64 x 8 static RAM, two software controlled 8 bit bidirectional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

Ordering Information

Order Number	Package Type	Temperature Range
R6530P	Plastic	0°C to +70°C
R6530C	Ceramic	0°C to +70°C

A custom number will be assigned by Rockwell.



R6530 Block Diagram

Specifications subject to change without notice

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an off state during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Read/Write (R/W)

The R/W signal is supplied by the microprocessor and is used to control the transfer of data to and from the microprocessor and the R6530. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6530. A low on the R/W pin allows a write (with proper addressing) to the R6530.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the Data Direction Register. The pin will be normally high with a low indicating an interrupt from the R6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pullup may be omitted with a mask option.

Data Bus (D0-D7)

The R6530 has eight bidirectional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor. The output buffers remain in the off state except when selected for a Read operation.

Peripheral Data Ports

The R6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0-PA7 and PB0-PB7. PB5, PB6 and PB7 also have other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the Data Direction Register. A "1" into the Data Direction Register will cause its corresponding bit to be an output. When in the input mode, the Peripheral Data Buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the R6530 it receives data stored in the Output Register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts (for a "1") or less than 0.8 volts (for a "0") as the peripheral pins are all TTL compatible.

Address Lines (A0-A9)

There are 10 address pins (A0-A9). In addition, there is the ROM Select pin (RSO). Further, pins PB5 and PB6 are mask programmable, and can be used either individually or together as chip selects. When used as peripheral data pins they cannot be used as chip selects.

INTERNAL ORGANIZATION

The R6530 is divided into four basic sections: RAM, ROM, I/O and Timer. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an Output Register.

ROM 1K Byte (8K Bits)

The 8K ROM is in a 1024 x 8 configuration. Address lines A0-A9, as well as RS0 are needed to address the entire ROM. With the addition of CS1 and CS2, seven R6530's may be addressed, giving 7168 x 8 bits of contiguous ROM.

RAM – 64 Bytes (512 Bits)

A 64 x 8 static RAM is contained on the R6530. It is addressed by A0-A5 (Byte Select), RS0, A6, A7, A8, A9 and, depending on the number of chips in the system, CS1 and CS2.

Internal Peripheral Registers

There are four internal registers, two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Therefore, anything then written into the Output Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the Output Register. For example, a "1" loaded into Data Direction Register A, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two Data Output Registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor.

During a Read operation the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output Register. The only way the Output Register data can be changed is by a microprocessor Write operation. The Output Register is not affected by a Read of the data on the peripheral pins.

Interval Timer

The Timer section of the R6530 contains three basic parts: prescale divide down register, programmable 8-bit register and interrupt logic.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Timer Register.

At the same time that data is being written to the Interval Timer, the counting interval (1, 8, 64 or 1024T) is decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A_3 = 1 enables IRQ on PB7, A_3 = 0 disables IRQ on PB7. When PB7 is to be used as an interrupt flag with the interval timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

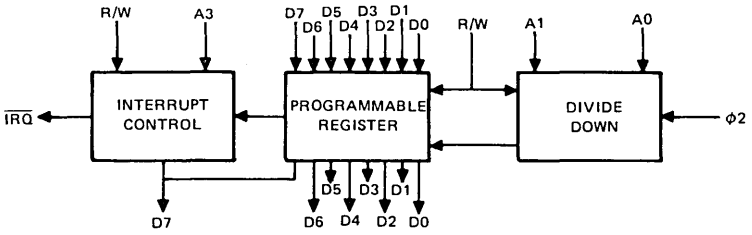
When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the Timer Register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in one's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1 = 27

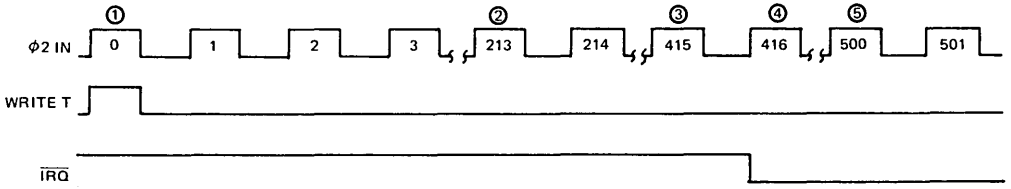
Thus, to arrive at the total elapsed time, merely do a one's complement and add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 417T + 27T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flag is read on DB7 all other DB outputs (DB0 thru DB6) go to "0".

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.



Basic Elements of Interval Timer



1. Data written into interval timer is 0 0 1 1 0 1 0 0 = 52_{10}

2. Data in Interval timer is 0 0 0 1 1 0 0 1 = 25_{10}
   $52 - \frac{213}{8} - 1 = 52\text{-}26\text{-}1 = 25$

3. Data in Interval timer is 0 0 0 0 0 0 0 0 = 0_{10}
   $52 - \frac{415}{8} - 1 = 52\text{-}51\text{-}1 = 0$

4. Interrupt has occurred at Ø2 pulse #416
   Data in Interval timer = 1 1 1 1 1 1 1 1

5. Data in Interval timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 0 1 1 = 83_{10}
   $83 + (52 \times 8) + 1 = 500_{10}$

ADDRESSING

Addressing of the R6530 offers many variations to the user for greater flexibility. The user may configure his system with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0-A9). In addition, there is the possibility of 3 additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are chip-selects 1 and 2 (CS1 and CS2). The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as a chip-select. The third additional address line is RSO. The R6502 and R6530 in a 2-chip system would use RSO to distinguish between ROM and non-ROM sections of the R6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Below is an example of a 1-chip and a 7-chip R6530 Addressing Scheme.

One-Chip Addressing

A 1-chip system decode for the R6530 is illustrated on the top of the following page.

Seven-Chip Addressing

In the 7-chip system the objective would be to have 7K of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14 and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between addresses 65,535 and 58,367. The 2 pins designated as chip-select or I/O would be masked programmed as chip-select pins. Pin RSO would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12 respectively. See illustration below.

The two examples shown would allow addressing of the ROM and RAM; however, once the I/O or timer has been addressed, further decoding is necessary to select which of the I/O registers are desired, as well as the coding of the interval timer.

I/O Register – Timer Addressing

Addressing Decode for I/O Register and Timer illustrates the address decoding for the internal elements and timer programming. Address lines A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

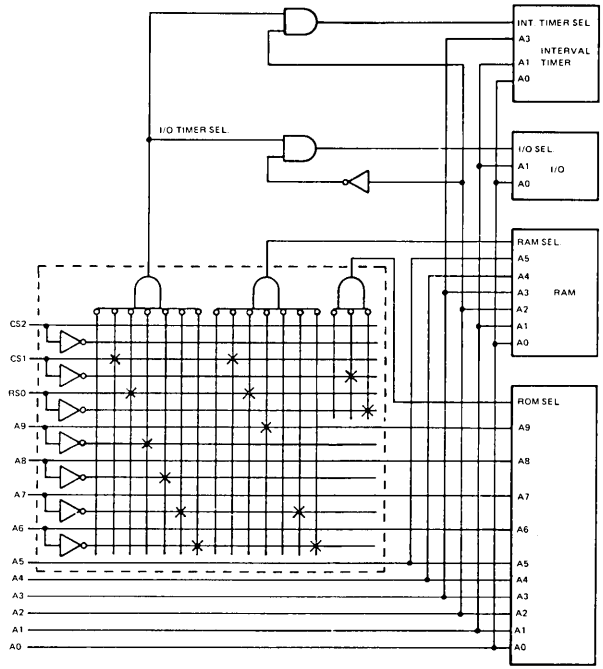
When the timer is selected A1 and A0 decode the divide by matrix. In addition, Address A3 is used to enable the interrupt flag to PB7.

R6530 Seven Chip Addressing Scheme

The addressing of the ROM select, RAM select and I/O Timer select lines would be as follows:

		CS2 A12	CS1 A11	RS0 A10	A9	A8	A7	A6
R6530 #1,	ROM SELECT	0	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	0
	I/O TIMER	0	0	0	1	0	0	0
R6530 #2,	ROM SELECT	0	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	1
	I/O TIMER	0	0	0	1	0	0	1
R6530 #3,	ROM SELECT	0	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	0
	I/O TIMER	0	0	0	1	0	1	0
R6530 #4,	ROM SELECT	1	0	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	1
	I/O TIMER	0	0	0	1	0	1	1
R6530 #5,	ROM SELECT	1	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	0
	I/O TIMER	0	0	0	1	1	0	0
R6530 #6,	ROM SELECT	1	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	1
	I/O TIMER	0	0	0	1	1	0	1
R6530 #7,	ROM SELECT	1	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	1	0
	I/O TIMER	0	0	0	1	1	1	0

*RAM select for R6530 #5 would read = $\overline{A12} \bullet \overline{A11} \bullet \overline{A10} \bullet \overline{A9} \bullet A8 \bullet \overline{A7} \bullet \overline{A6}$



A. X indicates mask programming
i.e. ROM select = $\overline{CS1} \bullet RS0$
RAM select = $\overline{CS1} \bullet \overline{RS0} \bullet \overline{A9} \bullet A7 \bullet A6$
I/O TIMER SELECT = $\overline{CS1} \bullet \overline{RS0} \bullet A9 \bullet A8 \bullet A7 \bullet A6$

B. Notice that A8 is a don't care for RAM select

C. CS2 can be used as PB5 in this example.

R6530 One Chip Address Encoding Diagram

Addressing Decode for I/O Register and Timer

	Addressing Decode							
	ROM Select	RAM Select	I/O Timer Select	R/W	A3	A2	A1	A0
Read ROM	1	0	0	1	X	X	X	X
Write RAM	0	1	0	0	X	X	X	X
Read RAM	0	1	0	1	X	X	X	X
Write DDRA	0	0	1	0	X	0	0	1
Read DDRA	0	0	1	1	X	0	0	1
Write DDRB	0	0	1	0	X	0	1	1
Read DDRB	0	0	1	1	X	0	1	1
Write Per. Reg. A	0	0	1	0	X	0	0	0
Read Per. Reg. A	0	0	1	1	X	0	0	0
Write Per. Reg. B	0	0	1	0	X	0	1	0
Read Per. Reg. B	0	0	1	1	X	0	1	0
Write Timer								
÷1T	0	0	1	0	*	1	0	0
÷8T	0	0	1	0	*	1	0	1
÷64T	0	0	1	0	*	1	1	0
÷1024T	0	0	1	0	*	1	1	1
Read Timer	0	0	1	1	*	1	X	0
Read Interrupt Flag	0	0	1	1	X	1	X	1

*A_3 = 1 Enables IRQ to PB7
A_3 = 0 Disables IRQ to PB7

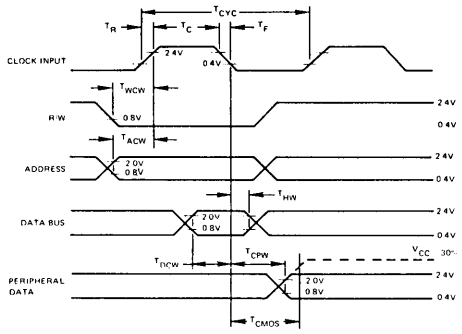
Write Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Period	T_{CYC}	1		10	μS
Rise & Fall Times	T_R, T_F			25	ns
Clock Pulse Width	T_C	470			ns
R/W valid before positive transition of clock	T_{WCW}	180			ns
Address valid before positive transition of clock	T_{ACW}	180			ns
Data Bus valid before negative transition of clock	T_{DCW}	300			ns
Data Bus Hold Time	T_{HW}	10			ns
Peripheral data valid after negative transition of clock	T_{CPW}			1	μS
Peripheral data valid after negative transition of clock driving CMOS (Level = VCC - 30%)	T_{CMOS}			2	μS

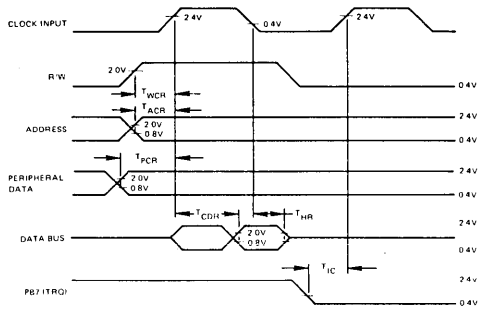
Read Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
R/W valid before positive transition of clock	T_{WCR}	180			ns
Address valid before positive transition of clock	T_{ACR}	180			ns
Peripheral data valid before positive transition of clock	T_{PCR}	300			ns
Data Bus valid after positive transition of clock	T_{CDR}			395	ns
Data Bus Hold Time	T_{HR}	10			ns
IRQ (Interval Timer Interrupt) valid before positive transition of clock	T_{IC}	200			ns

Loading = 30 pF + 1 TTL load for PA0-PA7, PB0-PB7
= 130 pF + 1 TTL load for D0-D7



Write Timing Characteristics



Read Timing Characteristics

PROGRAMMING INSTRUCTIONS

The Rockwell R6530 utilizes computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on mini-floppy diskettes prepared on the SYSTEM 65, or paper tape, or standard 80-column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Mask options should be noted on the ROM order form and in the title cards.

Title Cards

A set of six Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These six Title Cards must contain the following information:

	Column	Information
First Card	1-30	Customer Name
	31-50	Customer Part Number
	60-72	Rockwell Order Number (Example: R6530XX)
Second Card		Customer Contact Name, Customer Contact Phone Number
Third Card (2)		Pin 17 = $\overline{IRQ}$/PB7 with Pull-up or $\overline{IRQ}$/PB7 without Pull-up. Pin 18 = CS1 or PB6, Pin 19 = CS2 or PB5 (Example: Pin 17 = IRQ NO PULL-UP, PIN 18 = CS1, PIN 19 = PB5)
Fourth Card (2)	(1)	ROM SEL, RS0 = X, CS1 = X, CS2 = X (Example: ROM SEL, CS1 = H, RS0 = H, CS2 = N)
Fifth Card (2)	(1)	RAM SEL, RS0 = X, CS1 = X, CS2 = X, A9 = X, A8 = X, A7 = X, H6 = X (Example: RAM SEL, CS1 = L, CS2 = N, RS0 = L, A9 = L, A8 = N, A7 = H, A6 = H)

NOTE:
$\overline{IRQ}$ is keypunched as IRQ

Sixth Card (2)	(1)	I/O SEL, RS0 = X, CS1 = X, CS2 = X, A9 = X, A8 = X, A7 = X, A6 = X (Example: I/O SEL, CS1 = L, RS0 = L, CS2 = N, A9 = H, A8 = H, A7 = H, A6 = H)

(1) X = H or L or N
H = +2.4 Volts L = +0.4 Volts N = No Effect
(2) Free Format — Delimiters are commas or blanks

Data Card Format

The required data card format is generated by the Cross Assembler. All addresses are coded in hexadecimal form (0 through FFFF). All output words are coded both in binary and octal forms. Output 8 (DB7) is the MSB, and Output 1 (DB0) is the LSB.

The format for all cards in a file, except the last card, is as follows:

$$;3S_2S_1S_0\text{b}N_1N_0\text{b}A_3A_2A_1A_0\underbrace{D_1D_0}_{1}\underbrace{D_1D_0}_{2}\text{b}X_3X_2X_1X_0$$

The format for the last card in a file is as follows:

;40000

EXAMPLE:

```
;30001 10 0000 6964656475647964006D4C047D4C0479 054F
;30102 10 0010 4C0461647164296425643564396400 2D 0463
;30003 10 0037 24642C4C04000000000000000000000000 0104
;40100
```

Paper Tape Format

Rockwell can accept ROM coding in paper tape prepared using SYSTEM 65, Cross Assembler or AIM 65 output. Mask options should be noted on the ROM order form. The format for paper tape is as follows:

$$;N_1N_0A_3A_2A_1A_0\underbrace{D_1D_0}_{1}\underbrace{D_1D_0}_{2}X_3X_2X_1X_0CRLF$$

The format for the last record in a file is as follows:

$;00C_3C_2C_1C_0X_3X_2X_1X_0$

NOTE 1

1. 00 = zero bytes of data in this record. This identifies this as the final record in a file.
2. $C_3C_2C_1C_0$ = the total number of records (in hexadecimal) in this file, including the last record.
3. The valid record is identified by the starting delimitor (;) and terminated by the check sum ($X_3X_2X_1X_0$). All other characters such as the CR and LF are not processed. The next semi-colon initiates the next record.

EXAMPLE:

```
;18F000CA86004C00F0FDF9212D21FF292D8F2161F5F7FF657D677D0D40
;18F018E564672DFD7575E50000CF4112F800925198D200539192F20C98
;18F03008DB02890810DE12D894189AC2830E9800FB06232F087F650AA5
;0000030003
```

Unless otherwise stated, the field definitions are defined as follows:

1. All Characters (N,A,D,X) are the ASCII characters 0 through F, each representing a hexadecimal (hex) digit.
2. ; is a record mark indicating the start of a record.
3. N_1N_0 = the number of bytes of data in this record (in hex). Each pair of hex characters (D_1D_0) represents a single byte in the record.

4. $A_3A_2A_1A_0$ = the hex starting address for the record. A_3 represents address bits 15 through 12, etc. The 8-bit byte represented by $(D_1D_0)_1$ stored in address $A_3A_2A_1A_0$; $(D_1D_0)_2$ stored in $(A_3A_2A_1A_0) + 1$, etc.

5. (D_1D_0) = two hex digits representing an 8-bit byte of data. (D_1 = high-order 4 binary bits and D_0 = low-order 4 bits). A maximum of 18 (hex) or 24 (decimal) bytes of data per record is permitted.

6. $X_3X_2X_1X_0$ = record check sum. This is the hex sum of all characters in the record, excluding the record mark and the check sum characters. To generate the check sum, each byte of data (represented by two ASCII characters), is treated as 8 binary bits. The binary sum of these 8-bit bytes is truncated to 16 binary bits (4 hex digits) and is then represented in the record as four ASCII characters ($X_3X_2X_1X_0$).

7. $S_2S_1S_0$ = the hex sequence number for the card record.

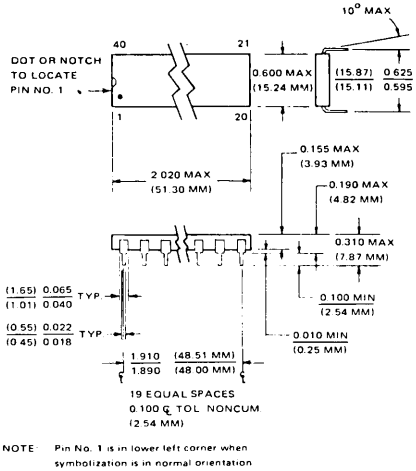
8. CR = ASCII character for Carriage return.

9. LF = ASCII character for line feed.

10. ␣ = Space character

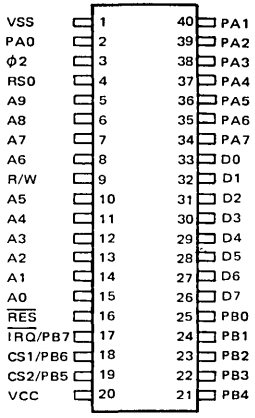
Mini-Floppy Diskette Format

Rockwell can accept ROM coding on mini-floppy diskettes prepared using the SYSTEM 65 Assembler output. The format is similar to the Paper Tape format shown in the preceding paragraph. Title card information should be recorded using the file name "TITLE." Data information should be recorded using the file name "DATA." Mask options should be noted on the ROM Order form.



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation.

Packaging Diagram



Pin Configuration

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Voltage	Unit
Supply Voltage	VCC	-0.3 to +7.0	V
Input/Output Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_{OP}	0 to 70	^{o}C
Storage Temperature Range	T_{STG}	-55 to +150	^{o}C

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

Electrical Characteristics

(VCC=5.0%, VSS=0V, T_A=25^{o}C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.4		VCC	V
Input Low Voltage	V_{IL}	V_{SS} - 0.3		V_{SS} + 0.4	V
Input Leakage Current; V_{IN} = V_{SS} + 5V A0-A9, RS, R/W, $\overline{RES}$, 02, PB6*, PB5*	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN} = 0.4V to 2.4V; D0-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PA0-PA7, PB0-PB7	I_{IH}	-100.	-300.		μA
Input Low Current; V_{IN} = 0.4V PA0-PA7, PB0-PB7	I_{IL}		-1.0	-1.6	MA
Output High Voltage VCC = MIN, I_{LOAD} ≤ -100 μA (PA0-PA7, PB0-PB7, D0-D7) I_{LOAD} ≤ -3 MA (PA0-PB0)	V_{OH}	 VSS + 2.4 VSS + 1.5			V
Output Low Voltage VCC = MIN, I_{LOAD} ≤ 1.6 MA	V_{OL}			VSS + 0.4	V
Output High Current (Sourcing); VOH ≥ 2.4V (PA0-PA7, PB0-PB7, D0-D7) ≥ 1.5V Available for other than TTL (Darlingtons) (PB0, PB7)	I_{OH}	 -100 -3.0	 -1000 -5.0		 μA MA
Output Low Current (Sinking); VOL ≤ 0.4V (PA0-PA7) (PB0-PB7)	I_{OL}	1.6			MA
Clock Input Capacitance	C_{Clk}			30	pF
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF
Power Dissipation	P_D		500	1000	MW

*When programmed as address pins
All values are D.C. readings

DOCUMENT NO. 29000D52
REV. 3, NOVEMBER 1979

PART NUMBER
R6531

Rockwell

R6500 Microcomputer System DATA SHEET

ROM-RAM-I/O-COUNTER (RRIOC)

SYSTEM ABSTRACT

The ROM-RAM-I/O Counter (RRIOC), Part Number R6531, further enhances the cost-effectivity of the R6500 NMOS 8-bit microcomputer system by providing a powerful, flexible two-chip minimum system option. Produced with N-channel depletion load, silicon gate technology, the R6500 system employs advanced architecture, including 13 instruction addressing modes to achieve third generation performance speeds and smaller chips, the key to lower hardware and design costs. Included in the R6500 system are 10 software-compatible microprocessor (CPU) options, a growing number of memory and I/O devices, a very efficient, low-cost SYSTEM 65 development aid and complete documentation.

DESCRIPTION

The R6531 is primarily designed to provide innovative Equipment Designers with a wide span of two-chip minimum systems in combination with the R6500 family of 10 CPUs. It can also be combined in a variety of multi-chip system configurations with other R6531's, ROMs, RAMs and other I/O devices.

There are two R6531 versions: a 40-pin dual-in-line package; another with expanded I/O in a compact 52-pin quad-in-line package – see Table 1. Both versions contain a 2048 x 8 mask-programmable ROM, a 128 x 8 static RAM, a software programmable multi-mode counter, an 8-bit serial data channel, and 15 bidirectional data lines (two ports) with a handshake control mode and four interrupt inputs. The 52-pin version has an 8-bit output port and a 4-bit input port for a total of 27 I/O lines. Several mask options are available tp provide a RAM standby power pin and chip selects for multi-chip systems – see Figure 1.

Prototyping circuits are available in both the 40- and 52-pin packages, and in 1- and 2-MHz versions. They are offered as part numbers R6531-098 and R6531-098A for the 40-pin part, and as part numbers R6531-099 and R6531-099A for the 52-pin part.

FEATURES

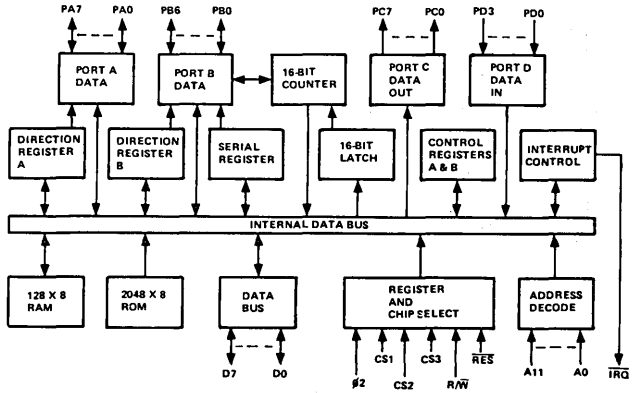
- 2048 x 8 mask programmable ROM
- 128 x 8 static RAM
- 16-bit multi-mode counter/latch
  - interval timer (one shot or free running)
  - pulse generator (one shot or free running)
  - event counter
  - external trigger
- 8-bit serial channel
- TTL compatible I/O, drive one TTL load
- 15 bidirectional I/O lines (2 ports – 40 pin package)
- Expansion 8-bit output port and 4-bit input port (52 pin package)
- I/O handshake control
- Four edge sensitive interrupt inputs
- 2 MHz or 1 MHz operation
- Single +5V power supply

Table 1 Ordering Information

Order Number: R6531

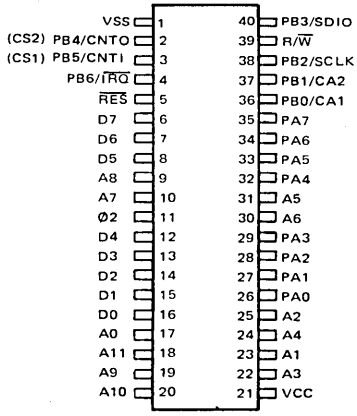
- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = −40°C to +85°C (Industrial)
- Package:
  - C = 40-Pin DIP, Ceramic
  - P = 40-Pin DIP, Plastic
  - Q = 52-Pin QUIP, Plastic
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz

NOTE: Contact your local Rockwell representative for availability.

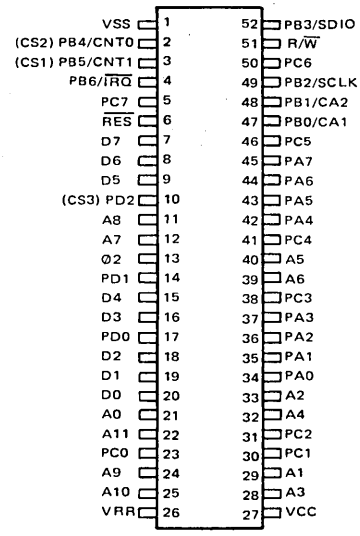


R6531 Block Diagram

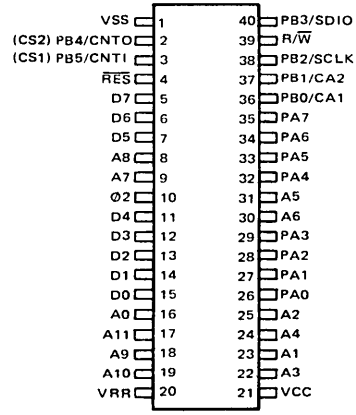
Specifications subject to change without notice



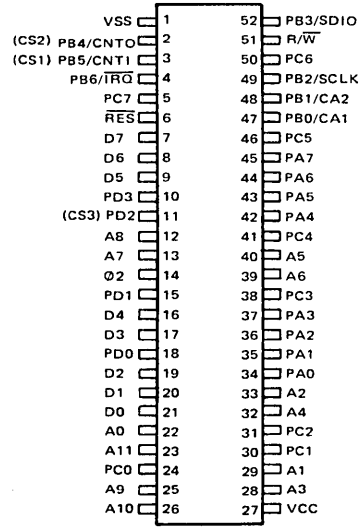
40- Pin Configuration
R6531, PB6 Option



52-Pin Configuration
R6531Q, VRR Option



40-Pin Configuration
R6531, VRR Option



52-Pin Configuration
R6531Q, PD3 Option

Figure 1. R6531 Pin Configuration Options

INTERFACE SIGNALS

RESET ($\overline{RES}$)

This active low signal is used to initialize the R6531. It clears all internal registers (except the counter and serial registers) to logic zero. This action places all bidirectional I/O lines in the input state and the Port C outputs in the high state. The timer, shift register, and interrupts are disabled. The $\overline{RES}$ signal must be low for at least four clock periods when reset is required.

ADDRESS BUS (A0-A11) AND CHIP SELECTS (CS1-CS3)

Memory and register selection is accomplished using the 12 address lines and, in multiple device systems, also using one or more of the three Chip Select mask options. When PB4, PB5, or PD2 are chosen as chip selects, they cannot be used as peripheral I/O pins.

DATA BUS (D0-D7)

The R6531 has eight data bus lines, which allow data to be transferred to or from the microprocessor. The output buffers remain in the off-state except when the R6531 is selected for a read operation.

READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ signal is supplied by the microprocessor and is used to control the transfer of data to and from the microprocessor and the R6531. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the data supplied by the R6531. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the R6531.

PERIPHERAL DATA PORTS (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD3)

Both versions of the R6531 have 15 pins available for peripheral I/O operations. Each pin is software programmable to act as an input or an output. The pins are grouped into an 8-bit port, PA0-PA7, and a 7-bit port, PB0-PB6. The lines of the PB port may serve other functions. Ports PA and PB have associated data direction registers.

The expanded I/O of the 52-pin version provides an 8-bit output only port, PC0-PC7, and a 4-bit input only port, PD0-PD3. PD2 and PD3 may be assigned other functions as described herein.

The outputs are push/pull type drivers capable of driving a single TTL load. When inputs are selected the drivers float. If PB6 is programmed as the $\overline{IRQ}$ request output, the line is driven low and requires an external pull-up, thus allowing the wire OR-ing of $\overline{IRQ}$ from other devices.

RAM RETENTION VOLTAGE (VRR)

A separate pin for a power supply for the read/write memory is available as a mask option. This allows the retention of RAM data by using a battery back-up for the RAM only. Pin PB6 in the 40-pin version or PD3 in the 52-pin version is mask programmable as the VRR pin. Address line A10 must be held in the logic state which deselects RAM (user-defined) in order to protect the RAM data when VCC falls below the specified level or is turned off.

INTERNAL ORGANIZATION

The R6531 is divided into three basic functions: ROM, RAM, and I/O. The selection of any one of these three is accomplished by issuing the appropriate address information on the address bus when the chip is selected.

ADDRESSING

Addressing of the R6531 offers many variations to the user for system configuration flexibility. Combination with other R6531's, ROMs, RAMs or I/O devices is possible without need for external address decoding. Each of the three basic functions on the device has its own decode mask for unique selection.

The specific address ranges and chip selects are defined by the user and are dependent on the number of chips in the system. The programmed options to be fixed by masking are:

R6531 Function	Chip Selects			Address Inputs (A0-A11)											
	CS3	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
ROM	X	X	X	X	2K ROM Decode										
RAM	Y	Y	Y	Y	Y	Y	Y	Y	Y	128 RAM Decode					
I/O	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I/O Decode		

The X, Y, and Z bits may be selected as high, low or no effect.

The chip select pins are also discrete I/O pins PB5, PB4, and PD2. The pins are independent of each other in that any one may be used as a chip select. The user specifies as mask options which pins are to be used as I/O and which as chip selects.

ROM – 2K BYTES (16K BITS)

The 16K ROM is a 2048 x 8 bit configuration. An address on lines A0-A10 uniquely selects one byte of ROM. Additionally, address line A11 and the chip selects are required to select the ROM function on a given chip. In a system with multiple R6531's, the CS1, CS2, and CS3 mask options allow up to seven devices with 14K bytes of ROM without the need for external decoding.

RAM – 128 BYTES (1024 BITS)

The 128 x 8 static RAM of a given R6531 is addressed by lines A0-A6. Additionally, address lines A7-A11 and chip selects CS1, CS2, and CS3 provide selection of the RAM section of the device as well as the device itself when additional RAM devices or R6531's are in the system.

R6531 40 PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-098 (1 MHz) and R6531-098A (2 MHz) are packaged in a 40-pin dual in-line package that has the same pinouts as the 40-pin R6531 with PB6 option. In this prototyping circuit, the ROM is disabled and there is no VRR option.

Access codes for this prototyping circuit are shown in the table below.

R6531-098 Function	Chip Selects		Address Inputs (A0 - A11)											
	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
RAM	N	N	L	L	L	N	L	128 RAM Decode						
I/O	N	N	L	H	H	H	L	L	L	L	I/O Decode			

In the above table, N means No Effect, H means High (2.0 volts or greater) and L means Low (0.8 volt or less).

R6531 52-PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-099 (1 MHz) and R6531-099A (2 MHz) are packaged in the 52-pin quad in-line package, with VRR option. PD2 is used as a chip select (CS3), and PB4 and PB5 are available as I/O lines.

Access codes for the prototyping circuit are shown in the table below.

R6531-099 Function	Chip Selects			Address Inputs (A0-A11)											
	CS3	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
ROM	H	N	N	H	2K ROM Decode										
RAM	L	N	N	L	L	L	N	L	128 RAM Decode						
I/O	L	N	N	L	H	H	H	L	L	L	L	I/O Decode			

The 128 words of RAM have been mapped into the first half of both Page 0 and Page 1, to accomodate zero page addressing and stack operations. The full I/O capabilities described for the R6531 are available in the prototyping circuit, except that I/O lines PD2 and PD3 are dedicated to the VRR and CS3 mask options.

INPUT/OUTPUT

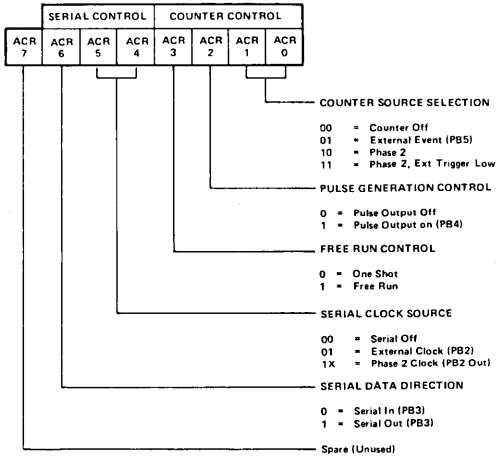
The input/output section is comprised of the data ports, direction registers, counter and associated latches, control registers, and interrupt registers. These I/O functions are all accessible by the R6502 CPU's instruction set using address bits A0-A3 for the specific function of the device. Address bits A4-A11 and CS1, CS2, and CS3 additionally may be decoded to select a given R6531 device in a multichip system. The addresses of the 15 internal peripheral registers are:

A3	A2	A1	A0	Register
0	0	0	0	Port A
0	0	0	1	Port B
0	0	1	0	Port C (write only)
0	0	1	1	Port D (read only)
0	1	0	0	Read Lower Counter/Write Lower Latch
0	1	0	1	Read Upper Counter/Write Upper Latch and Download
0	1	1	0	Write Lower Latch
0	1	1	1	Write Upper Latch
1	0	0	0	Serial Data Register
1	0	0	1	Interrupt Flag Register
1	0	1	0	Interrupt Enable Register
1	0	1	1	Auxiliary Control Register
1	1	0	0	Peripheral Control Register
1	1	0	1	*Data Direction Register — Port A
1	1	1	0	*Data Direction Register — Port B

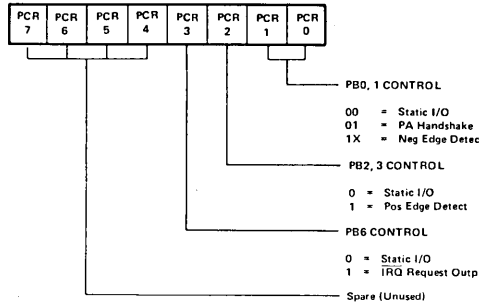
* Write Only

CONTROL REGISTERS

Two control registers, Peripheral Control and Auxiliary Control, are provided for software selection of various I/O functions. The Peripheral Control Register is primarily associated with Port B functions and the Auxiliary Control Register is associated with the counter and serial data functions which also affect Port B. The register bit assignments are:



Auxiliary Control Register (ACR)



Peripheral Control Register (PCR)

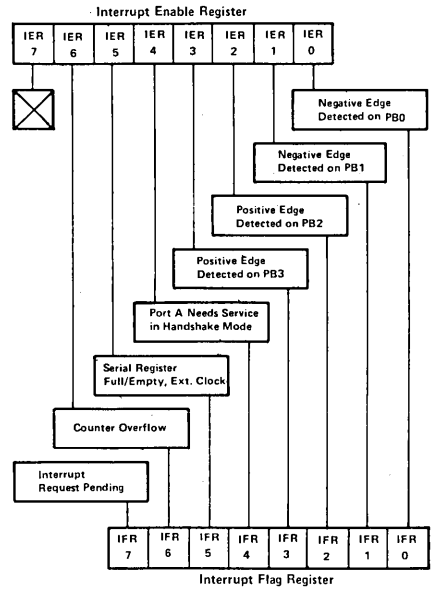
INTERRUPT ENABLE AND FLAG REGISTERS

Two registers are provided for interrupt control. Corresponding b in the enable and flag registers are logically ANDed to set the Interru Request Pending flag. If the pending flag is set and PB6 is selected an $\overline{\text{IRQ}}$ Request Output, then PB6 will be set low to request the R65t CPU to service $\overline{\text{IRQ}}$.

The interrupt enable bits are set or reset by writing into the Interru Enable Register. The interrupt flag bits IFR0-IFR6 can be cleare directly by writing a byte to the flag register which has 1's in tho bit positions to be cleared.

IFR4 and IFR5 may also be cleared by reading or writing the Port or Serial Data Registers respectively. IFR6 may also be cleared b reading the lower counter with I/O address hex 4 or writing the upp latch with I/O addresses hex 5 or 7.

These registers and their bit assignments are:



PERIPHERAL DATA PORTS

Each line of the 8-bit data Port A may be individually selected as an input or output. Associated with the port is Data Direction Register – Port A (DDRA). Each line of the 7-bit date Port B may be individually selected as an input or an output. This port also has a Data Direction Register (DDRB). The two data direction registers (A and B) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral pin as an output. Therefore, anything written into the data register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the data register. For example, a "1" loaded into DDRA, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and would be in a float state.

Note that when lines in the PB port are used alternately as control lines for other on-chip functions, Direction Register B must also be loaded to set up the proper direction – the Control Registers have no effect on data direction.

The 8-bit data Port C is an output only port. The 4-bit data Port D is an input only port.

For those lines being used as outputs, the data registers are used to latch data from the Data Bus during a Write operation so the peripheral device can read the data supplied by the microprocessor.

For the lines being used as inputs, the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output data.

EDGE DETECT LOGIC

Operating in parallel with the I/O operation of PB0-PB3 is edge detect logic that is enabled by Peripheral Control Register bits 1 and 2. PCR1 enables logic that upon detection of a negative edge on PB0 or PB1 will set a corresponding flag in the Interrupt Flag Register. PCR2 enables logic that upon detection of a positive edge on PB2 or PB3 will set corresponding flags in the Interrupt Flag Register. If corresponding bits are set in the Interrupt Enable Register, then the Interrupt Request Pending flag will be set.

MULTI-MODE COUNTER/LATCH

The R6531 contains a 16-bit counter with an associated 16-bit latch whose modes are software selectable by setting appropriate bits in the Auxiliary Control Register. The latch holds the counter preset value and all 16 bits download to the counter simultaneously upon command (I/O address hex 5) of the software or automatically in free run modes upon overflow of the counter. The counter is a decrementing counter and causes the setting of a flag in the Interrupt Flag Register when it overflows. This interrupt flag, bit 6, is logically ANDed with a corresponding counter overflow interrupt enabled bit to set the Interrupt Request Pending flag. The Auxiliary Control Register is used to set four basic modes which specify the source of the count information, and to select two mode modifiers that apply equally to the three active modes.

Mode 0 – Counter Off

Mode 1 – Event Counter – counts external event inputs (negative transitions) at PB5

Mode 2 – Interval Timer – counts Ø2 system clock pulses.

Mode 3 – External Trigger – counts Ø2 system clock pulses starting with a negative transition on PB5.

Mode Modifier A – Pulse Generation Control – causes the output level on PB4 to switch low each time the counter is loaded using I/O address hex. 5. At counter overflow, PB4 switches high. If in the free run mode, PB4 continues to toggle at each subsequent counter overflow; otherwise there are no further transitions until the counter is reactivated by the software.

Mode Modifier B – Free Run Control – causes the full 16-bit latch to be downloaded to the counter, continues to count, and sets the counter overflow flag bit every time the counter overflows. Otherwise the counter is a one shot mode in which the counter overflow flag is set one time only until the counter is reactivated by the software.

SERIAL DATA CHANNEL

The R6531 has an 8-bit serial channel. PB2 and PB3 are software selectable as the serial clock (SCLK) and serial data (SDIO) lines respectively.

The software sets Auxiliary Control Register bits 4 and 5 to enable the serial channel and to specify the source of the shift clock. Selection of the internal clock will shift data at one half the system Ø2 clock rate. If the external clock is used, data may be shifted at any rate up to one half the system Ø2 clock rate. In the external clock mode, the counter may be operated in the free run pulse generator mode using the CNTO line externally connected to the SCLK line to provide the desired shift rate.

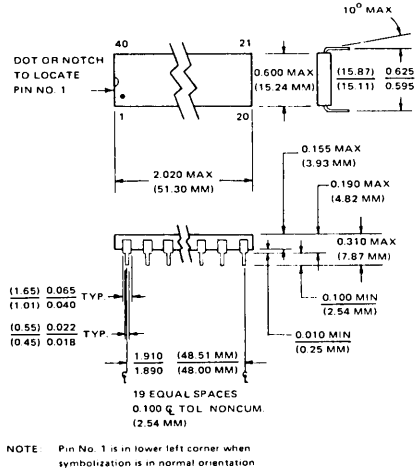
Auxiliary Control Register bit 6 sets the serial data direction. Data are shifted in or out, most significant bit first, under control of the shift clock.

In the external clock mode, the completion of eight shifts of the serial register will set bit 5 of the interrupt flag register. If the corresponding bit of the Interrupt Enable Register is also set an Interrupt Request Pending flag will be set.

HANDSHAKE OPERATIONS

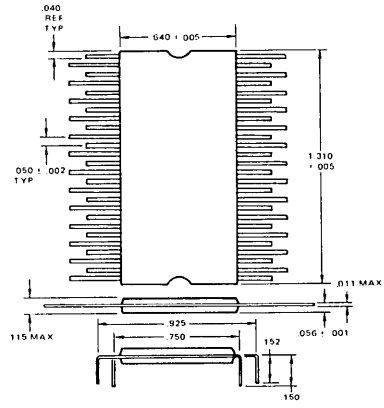
PB0 and PB1 may be used as handshake control lines for date transmissions over Port PA; see PCR definition. PB0 is a control input, PB1 is a control output. PB1 switches low on a read or write to Port PA, and switches high in response to a negative transition on PB0.

IFR4 in the Flag Register is set by a negative transition on PB0, and cleared by a Read or Write to Port PA; see Handshake Timing Diagram for timing details.

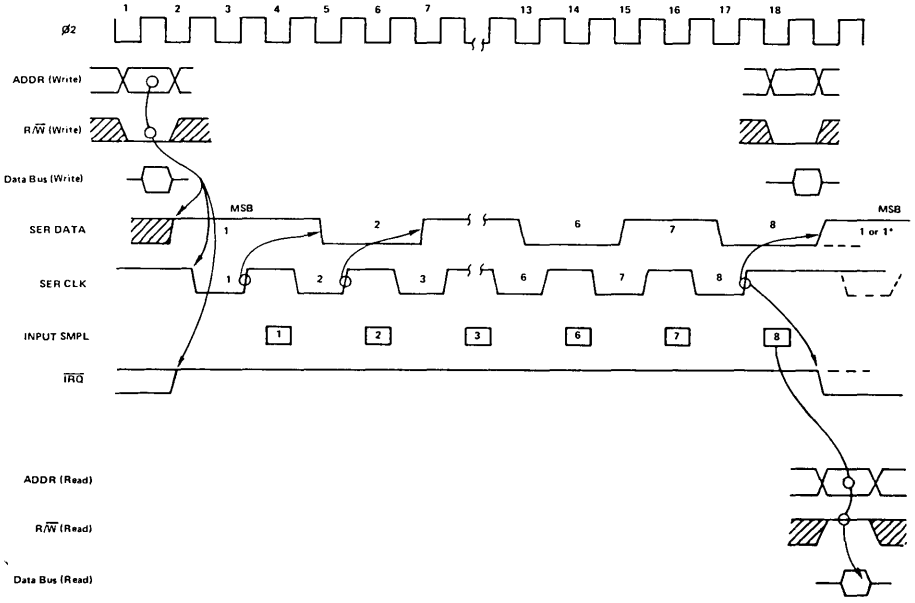


NOTE Pin No. 1 is in lower left corner when symbolization is in normal orientation

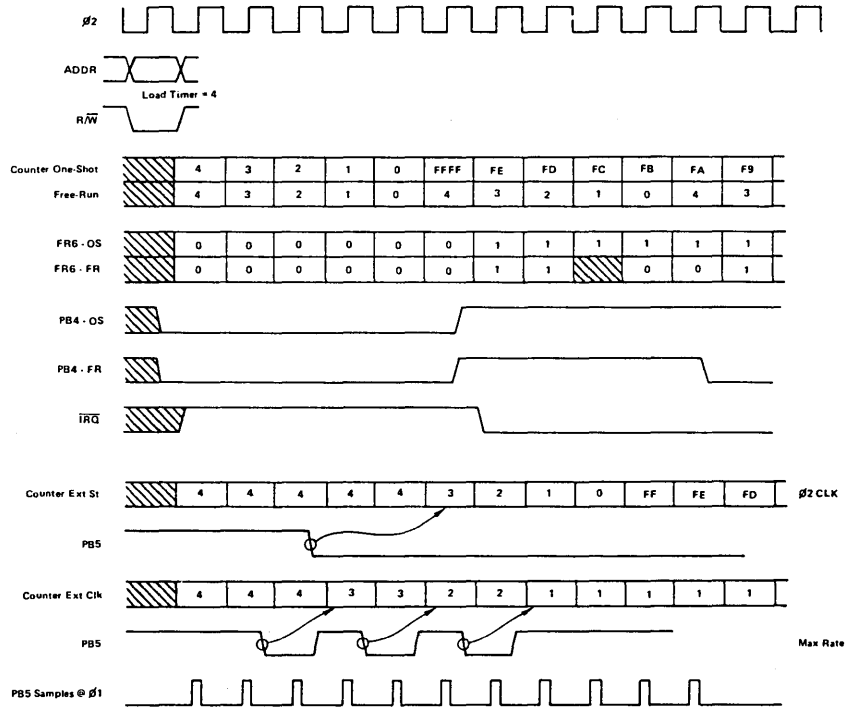
40-Pin Packaging Diagram



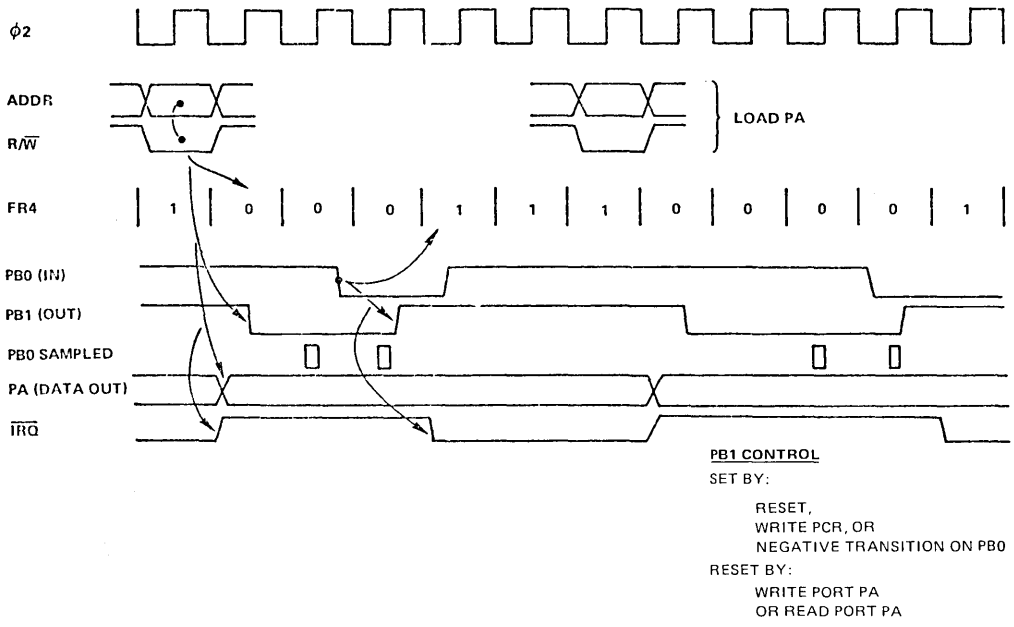
52-Pin Packaging Diagram



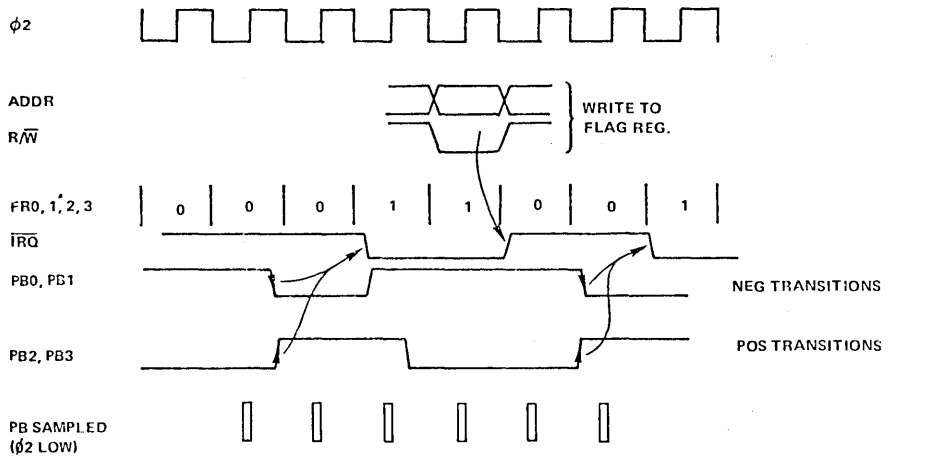
R6531 Serial Timing



R6531 Counter/Timer Timing



R6531 Timing for Handshake Mode



R6531 Timing for Interrupt Mode

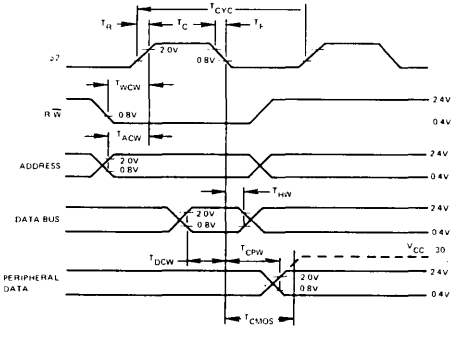
Write Timing Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Clock Period	T_{CYC}	1	10	0.5	10	μs
Rise & Fall Times	T_R, T_F		25		15	ns
Clock Pulse Width	T_C	470		235		ns
R/$\overline{W}$ valid before positive transition of clock	T_{WCW}	180		120		ns
Address valid before positive transition of clock	T_{ACW}	180		120		ns
Data Bus valid before negative transition of clock	T_{DCW}	270		135		ns
Data Bus Hold Time	T_{HW}	10		10		ns
Peripheral data valid after negative transition of clock	T_{CPW}		900		450	ns

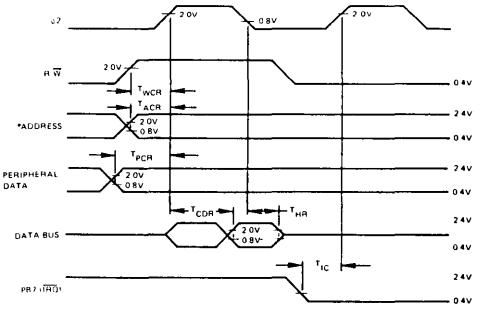
Read Timing Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
R/$\overline{W}$ valid before positive transition of clock	T_{WCR}	180		120		ns
Address valid before positive transition of clock	T_{ACR}	180		120		ns
Peripheral data valid before positive transition of clock	T_{PCR}	270		135		ns
Data Bus valid after positive transition of clock	T_{CDR}		350		180	ns
Data Bus Hold Time	T_{HR}	10		10		ns
IRQ valid after negative transition of clock	T_{IC}		900		450	ns

Loading = 100 pF + 1 TTL load for PA0-PA7, PB0-PB6, PC0-PC7
= 100 pF + 1 TTL load for D0-D7 (R6531A)
= 130 pF + 1 TTL load for D0-D7 (R6531)



Write Timing Characteristics



Read Timing Characteristics

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Electrical Characteristics

(VCC = 5V ± 10% for R6531, VCC = 5V ± 5% for R6531A)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	VCC	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Input Leakage Current; $V_{IN} = V_{SS} + 5V$, $V_{CC} = +5V$ A0-A11, CS1-CS3 R/$\overline{W}$, $\overline{RES}$, $\phi 2$, PD0-PD3	I_{IN}		2.5	μA
Leakage Current for High Impedance State, $V_{CC} = +5V$ (Three State); $V_{IN} = 0.4V$ to 2.4V; D0-D7, PA0-PA7, PB0-PB6	I_{TSI}		±10.0	μA
Output High Voltage VCC = MIN, $I_{LOAD} \leq -200$ μA (PA0-PA7, PB-PB6, D0-D7)	V_{OH}	VSS + 2.4		V
Output Low Voltage VCC = MIN, $I_{LOAD} \leq 2.1$ mA	V_{OL}		VSS + 0.4	V
Output High Current (Sourcing); VOH ≥ 2.4V (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD3, D0-D7)	I_{OH}	-200		μA
Output Low Current (Sinking); $V_{OL} \leq 0.4V$ (PA0-PA7) (PB0-PB6) (PC0-PC7)	I_{OL}	2.1		mA
Clock Input Capacitance, $V_{CC} = 5V$	C_{Clk}		20	pF
Input Capacitance, $V_{CC} = 5V$	C_{IN}		10	pF
Output Capacitance, $V_{CC} = 5V$, chip deselected	C_{OUT}		10	pF
Power Dissipation	P_D		1.0	W

*When programmed as address pins

All values are D.C. readings

DOCUMENT NO. 29000 D42
REV. 2, FEBRUARY 1978

PART NUMBER
R6532

Rockwell

R6500 Microcomputer System
DATA SHEET

RAM, I/O, INTERVAL TIMER DEVICE (RIOT)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon-Gate technology. Its performance speeds are enhanced by advanced system architecture which enables multiple addressing. Its innovative architecture results in smaller chips — the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices. Rockwell also provides memory and I/O devices that further enhance the cost-effectivity of the R6500 microcomputer system-. . . as well as low-cost design aids and documentation.

DESCRIPTION

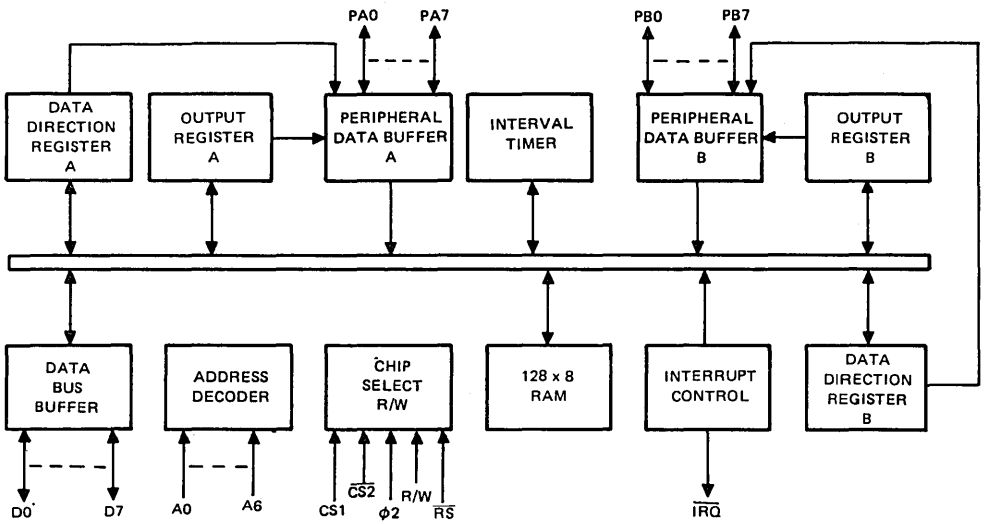
The R6532 is designed to operate in conjunction with the R6500 Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software controlled 8 bit bidirectional data ports allowing direct interfacing between the microcomputer and peripheral devices, a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge detect circuit.

FEATURES

- 8 bit bidirectional Data Bus for direct communication with the microprocessor
- 128 x 8 static RAM
- Two 8 bit bidirectional data ports for interface to peripherals
- Two programmable Data Direction Registers
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Bus
- Programmable edge-sensitive interrupt

Ordering Information

Order Number	Package Type	Temperature Range
R6532P	Plastic	0°C to +70°C
R6532C	Ceramic	0°C to +70°C



R6532 Block Diagram

Specifications subject to change without notice

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least two clock periods when reset is required.

Read/Write (R/W)

The R/W signal is supplied by the microprocessor and is used to control the transfer of data to and from the microprocessor and the R6532. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6532. A low on the R/W pin allows a write (with proper addressing) to the R6532.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high with a low indicating an interrupt from the R6532. An external 3K pull-up resistor is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

Data Bus (D0-D7)

The R6532 has eight bidirectional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when the R6532 is selected for a Read operation.

Peripheral Data Ports (PA0-PA7, PB0-PB7)

The R6532 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PA7 also has other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the R6532 it receives data stored in the output register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PB0-PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.

Address Lines (A0-A6)

There are 7 address pins. In addition to these 7, there is the $\overline{RAM\ SELECT}$ ($\overline{RS}$) pin. The pins A0-A6 and $\overline{RAM\ SELECT}$ are always used as addressing pins. There are two additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$.

INTERNAL ORGANIZATION

The R6532 is divided into four basic sections, RAM, I/O, TIMER, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an Output Register.

RAM – 128 Bytes (1024 Bits)

The 128 x 8 Read/Write memory acts as a conventional static RAM. Data can be written into the RAM from the microprocessor by selecting the chip (CS1=1, $\overline{CS2}$ = 0) and by setting $\overline{RS}$ to a logic 0 (0.4V). Address lines A0 through A6 are the used to select the desired byte of storage.

Internal Peripheral Registers

The Peripheral A I/O port consist. of eight lines which can be individually programmed to act as either an input or an output. A logic zero in a bit of the Data Direction Register (DDRA) causes the corresponding line of the PA port to act as an input. A logic one causes the corresponding PA line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Output Register (ORA).

Data is read directly from the PA pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Output Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Output Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the peripheral pin to act as an output.

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition will set the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag will cause $\overline{IRQ}$ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

Setting of the PA7 interrupt flag will occur on an active transition even if the pin is being used as a normal input or as a peripheral control output. The flag will also be set by an active transition if interrupting from PA7 is disabled. The reset signal ($\overline{RES}$) will disable the PA7 interrupt and will set the active transition to negative (high to low). During the system initialization routine, it is possible to set the interrupt flag by a negative transition. It may also be set by changing the polarity of the active interrupt. It is therefore recommended that the interrupt flag be cleared before enabling interrupting from PA7.

Clearing of the PA7 Interrupt Flag occurs when the micorprocessor reads the Interrupt Flag Register.

The operation of the Peripheral B Input/Output port is exactly the same as the normal I/O operation of the Peripheral A port. The eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Output Register (ORB).

The primary difference between the PA and the PB ports is in the operation of the output buffers which drive these pins. The PB output buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V. This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read PB" operation, sufficient logic is provided in the chip to allow the microprocessor to read the Output Register instead of reading the peripheral pin as on the PA port.

Interval Timer

The Timer section of the R6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.

The interval timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A3 = 1 enables $\overline{IRQ}$, A3 = 0 disables $\overline{IRQ}$. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

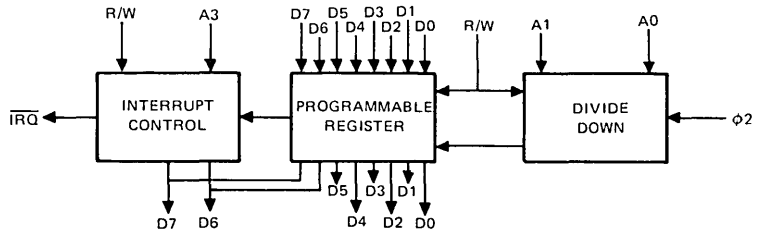
When the timer has counted thru 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in two's complement, but remember that interrupt occurred on count number one. Therefore, we must subtract 1.

Value read	=	1 1 1 0 0 1 0 0
Complement	=	0 0 0 1 1 0 1 1
ADD 1	=	0 0 0 1 1 1 0 0 = 28 Equals two's complement of register
SUB 1	=	0 0 0 1 1 0 1 1 = 27

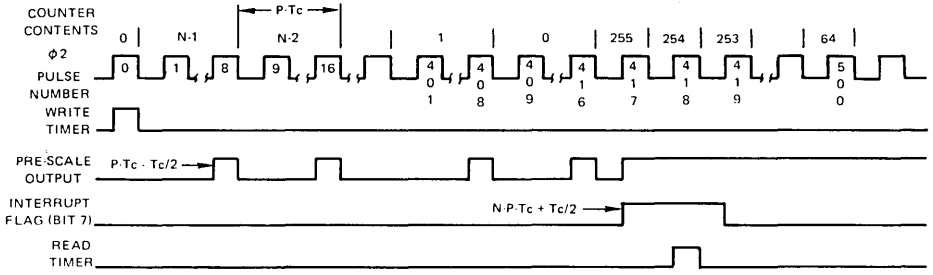
Thus, to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 27T = 443T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (D7 for the timer, D6 for the edge detect) data bus lines D0-D5 go to 0.

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.



Basic Elements of Interval Timer



ASSUME 52 LOADED INTO TIMER WITH A DIVIDE BY 8.
THE COUNTER CONTENTS AND THE CLOCK PULSE NUMBERS WILL COINCIDE.
Prescale, P = 8
Cycle Time, Tc = 1 μsec (for 1 MHz)
Count, N = 52

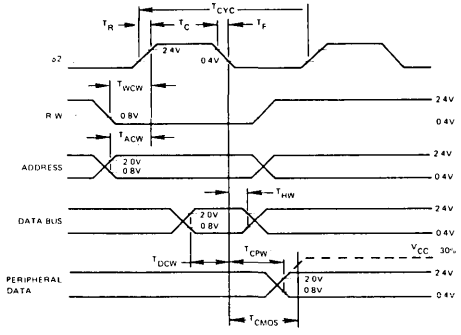
Write Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Period	T_{CYC}	1		10	μS
Rise & Fall Times	T_R, T_F			25	ns
Clock Pulse Width	T_C	470			ns
R/W valid before positive transition of clock	T_{WCW}	180			ns
Address valid before positive transition of clock	T_{ACW}	180			ns
Data Bus valid before negative transition of clock	T_{DCW}	300			ns
Data Bus Hold Time	T_{HW}	10			ns
Peripheral data valid after negative transition of clock	T_{CPW}			1	μS
Peripheral data valid after negative transition of clock driving CMOS (Level = VCC - 30%)	T_{CMOS}			2	μS

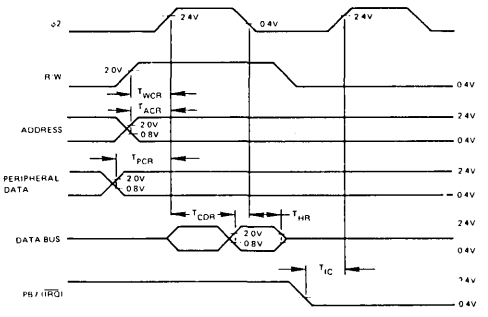
Read Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
R/W valid before positive transition of clock	T_{WCR}	180			ns
Address valid before positive transition of clock	T_{ACR}	180			ns
Peripheral data valid before positive transition of clock	T_{PCR}	300			ns
Data Bus valid after positive transition of clock	T_{CDR}			395	ns
Data Bus Hold Time	T_{HR}	10			ns
IRQ (Interval Timer Interrupt) valid before positive transition of clock	T_{IC}	200			ns

Loading = 30 pF + 1 TTL load for PA0-PA7, PB0-PB7
= 130 pF + 1 TTL load for D0-D7



Write Timing Characteristics



Read Timing Characteristics

RAM Addressing

$\overline{RS}$ = 0
A0-A6 select RAM address

I/O Addressing

$\overline{RS}$ = 1 A2 = 0
R/W = 1 to read, 0 to write

	A1	A0
PA data	0	0
PA data direction	0	1
PB data	1	0
PB data direction	1	1

Write Edge Detect Control

$\overline{RS}$, A2 = 1 R/W, A4 = 0

A1 = 1, enable interrupt from PA7
A1 = 0, disable interrupt from PA7
A0 = 1, positive edge detect (PA7)
A0 = 0, negative edge detect (PA7)

Read and Clear Interrupt Flag

$\overline{RS}$, R/W, A2, A0 = 1
Bit 7 = Timer Flag
Bit 6 = PA7 Flag

Read Interval Timer

$\overline{RS}$, A4, A2, R/W, A0 = 1

Read Interval Timer Overflow

$\overline{RS}$, A4, A2, R/W = 1, A0 = 0

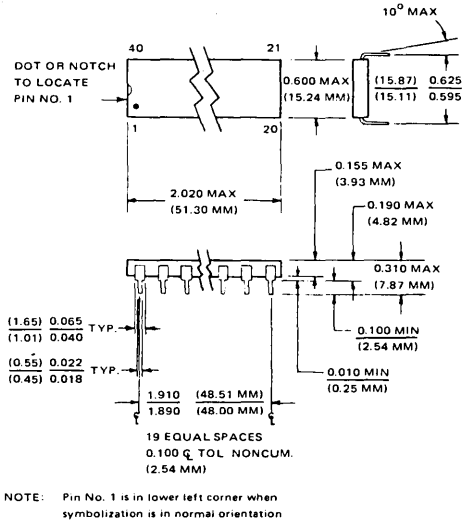
Write Count to Interval Timer

$\overline{RS}$, A4, A2 = 1, R/W = 0

	A1	A0
÷1	0	0
÷8	0	1
÷64	1	0
÷1024	1	1

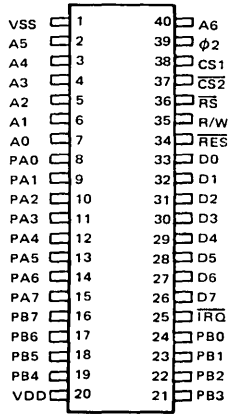
A3 = 1, enable timer interrupt
A3 = 0, disable timer interrupt

NOTE: For all operations CS1 = 1, $\overline{CS2}$ = 0.



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

Packaging Diagram



Pin Configuration

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Voltage	Unit
Supply Voltage	VCC	-0.3 to +7.0	V
Input/Output Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_{OP}	0 to 70	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

Electrical Characteristics

(VCC=5.0%, VSS=0V, T_A=25°C)

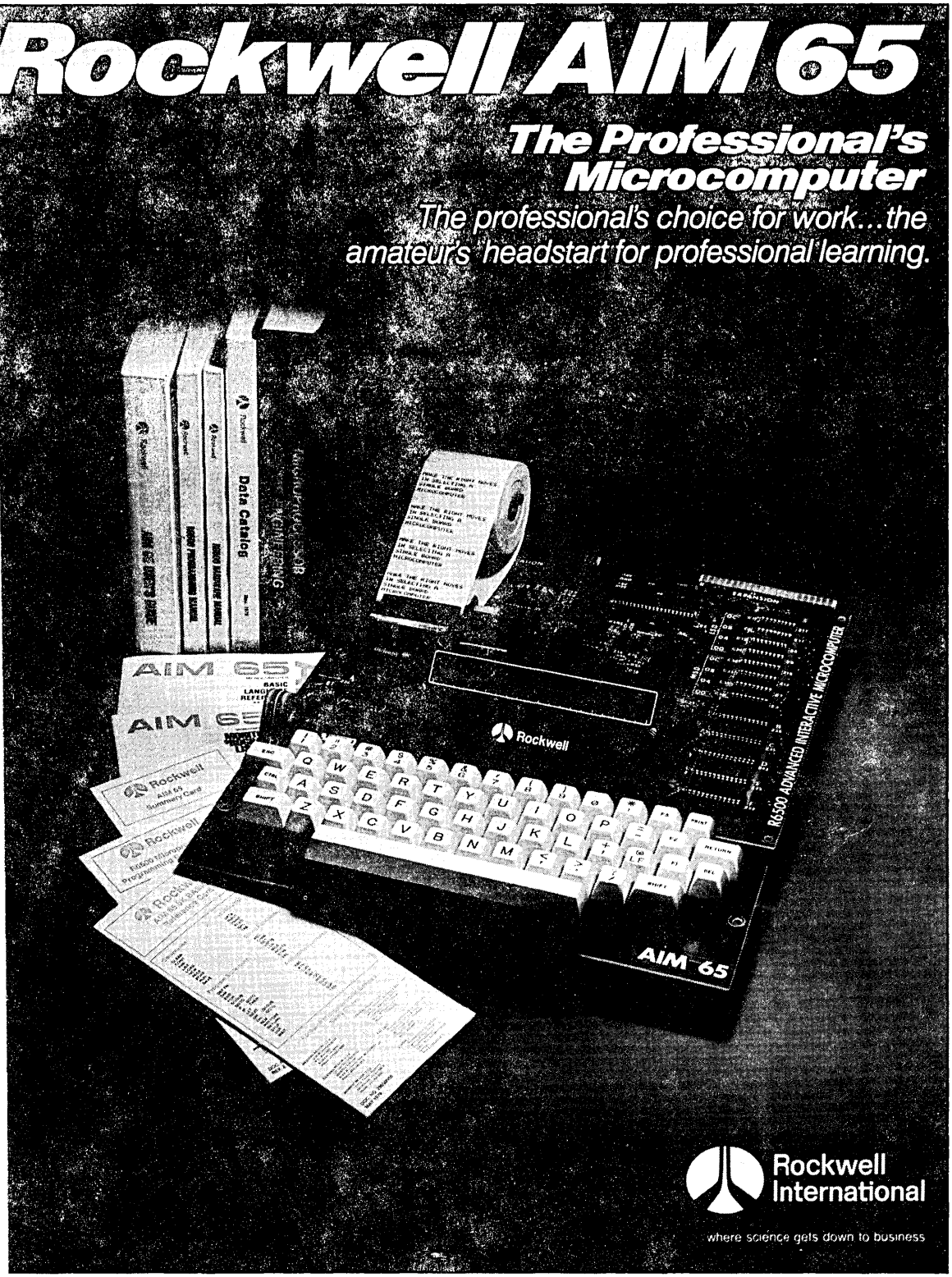
Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.4		VCC	V
Input Low Voltage	V_{IL}	V_{SS} - 0.3		V_{SS} + 0.4	V
Input Leakage Current; V_{IN} = V_{SS} + 5V A0-A6, RS, R/W, $\overline{RES}$, ϕ2, CS1, $\overline{CS2}$	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN} = 0.4V to 2.4V; D0-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PA0-PA7, PB0-PB7	I_{IH}	-100.	-300.		μA
Input Low Current; V_{IN} = 0.4V PA0-PA7, PB0-PB7	I_{IL}		-1.0	-1.6	MA
Output High Voltage VCC = MIN, I_{LOAD} ≤ -100 μA (PA0-PA7, PB0-PB7, D0-D7) I_{LOAD} ≤ -3 MA (PB0-PB7)	V_{OH}	 VSS + 2.4 VSS + 1.5			V
Output Low Voltage VCC = MIN, I_{LOAD} ≤ 1.6 MA (D0-D7)	V_{OL}			VSS + 0.4	V
Output High Current (Sourcing); VOH ≥ 2.4V (PA0-PA7, PB0-PB7, D0-D7) ≥ 1.5V Available for other than TTL (Darlingtons) (PB0-PB7)	I_{OH}	 -100 -3.0	 -1000 -5.0		 μA MA
Output Low Current (Sinking); VOL ≤ 0.4V (PA0-PA7) (PB0-PB7)	I_{OL}	1.6			MA
Clock Input Capacitance	C_{Clk}			30	pF
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF
Power Dissipation	P_D		500	1000	mW

All values are D.C. readings

AIM 65
MICRO-
COMPUTER

AIM 65
MICRO-
COMPUTER

AIM 65
MICRO-
COMPUTER


Rockwell AIM 65
The Professional's Microcomputer
The professional's choice for work...the amateur's headstart for professional learning.
Data Catalog
Rockwell
AIM 65
R6500 ADVANCED INTERACTIVE MICROCOMPUTER
Rockwell International
where science gets down to business

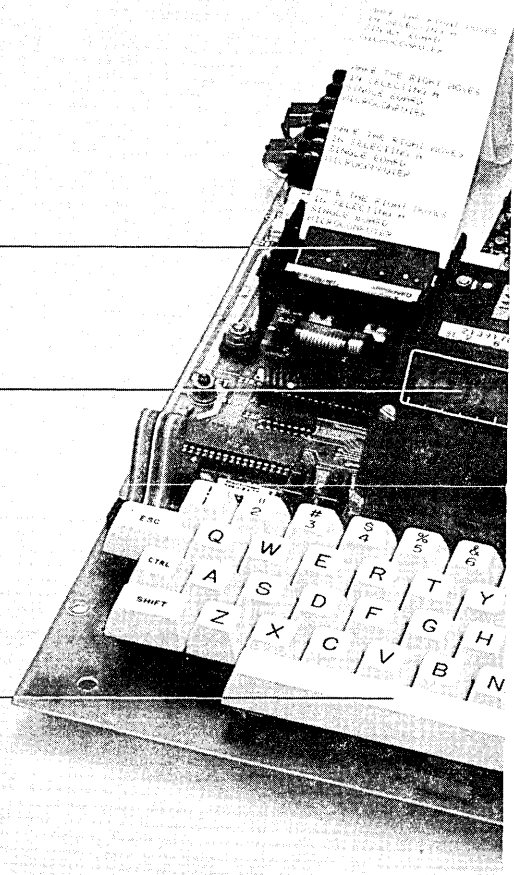
Rockwell AIM 65...gifted

System Applications Connector
44-pin connector lets you connect peripherals interfaced with AIM 65's versatile I/O capabilities — for example, one or two cassette tape recorders, a Teletypewriter (20ma current loop), switches and sensors using serial and parallel TTL-level interfaces, timing and control functions via built-in 16-bit timer/counter system functions, and more.

120-Line/Min. 20-Column, Hard-Copy Printer
On-board thermal printer is unique among comparable micro-computers. Easy-read 5x7 dot matrix, 64-character ASCII format.

Large, 20-Character Alphanumeric Display
High contrast, 16-segment characters for optimum readability. 64-character ASCII format.

54-Key Alphanumeric Terminal-Style Keyboard
Provides 70 different alphabetic, numeric, control and special functions.



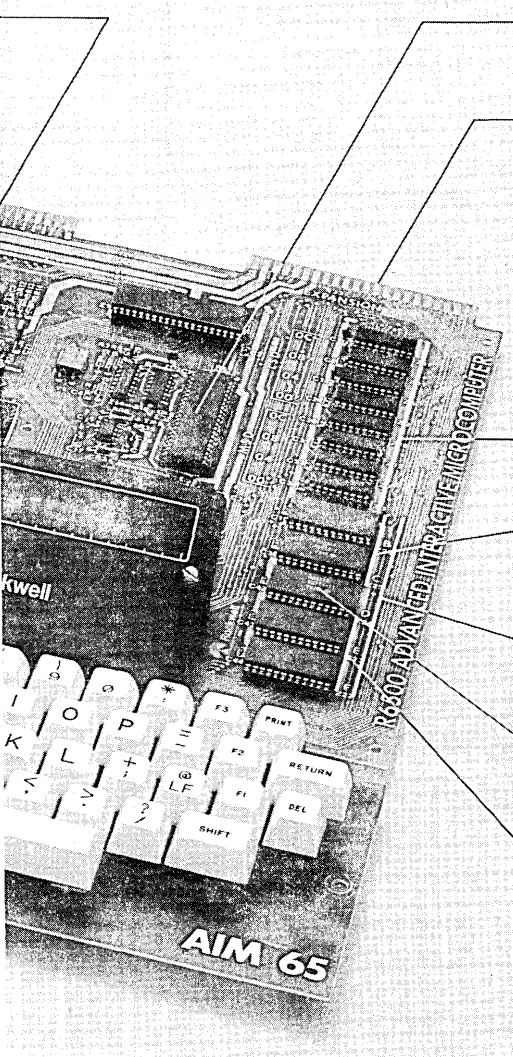
Among personal computers, AIM 65 stars as the professional's microcomputer. It's gifted with professional features for those seriously interested in applying or learning microprocessors.

And it's priced so low that most everybody can afford it.

Third-generation processor architecture; versatile, broad interfacing capabilities; expandable memory; minicomputer-like instructions, multi-mode addressing; interactive, self-prompting software; on-board printer and display...AIM 65 is the professional's microcomputer for system development and products, the amateur's headstart for professional learning.

Harnessed for work, AIM 65 as a "bare-board" microcomputer out-performs in its price category — and in much higher priced categories — as an intelligent, programmable stand-alone or terminal controller or processor. By itself, it's an economically feasible system for small-volume products or one-of-a-kind work projects.

...with professional features.



Third-Generation, High Performance 1-MHz 6502 Microprocessor
The 6502 is quickly becoming the world's most popular CPU; has minicomputer-like features. More details on Page 6.

Full-Bus System Expansion Connector
44-pin connector extends address, data, control bus; lets you add on prototyping boards, PROM programmer, additional memory boards, floppy disk, Rockwell bubble memory modules, Rockwell modular modem analog interface boards and other subsystem modules.

Plug-In Sockets for 4K-Bytes RAM
Sockets for up to eight industry standard 2114 static read/write RAM memory devices.

BASIC Interpreter Firmware
Contained on two R2332 ROMS; simplifies programming; easy to learn. (Optional)

Plug-In Sockets for 20K-Bytes of ROM or PROM
Plug-in sockets for five industry-standard 2332 (4K-byte) Read-Only Memory (ROM) or compatible Programmable ROM (PROM) devices, or optional program firmware.

Symbolic Assembler Firmware
Contained on one R2332 ROM, the two-pass Assembler is accessed with the Monitor and allows symbolic coding for speedier programming. (Optional)

Advanced Interactive Monitor Firmware
Contained on two R2332 ROMs, Interactive Monitor Program is the heart of AIM 65's innovative software. A Text Editor is also contained on these ROMs. For full details, see Pages 4 and 5.

As the beginner's choice for professional learning, AIM 65's gifted features are exploited through inspired software.

AIM 65's available software includes easily-learned, easily-used BASIC. But AIM 65 also makes easy the mastering of microcomputer fundamentals. Its software gives you self-prompting program entry and listing, single-step debugging and other development features normally found only on equipment costing thousands of dollars; AIM 65 costs but hundreds.

No comparable microcomputer has an on-board printer. Yet hard copies of exercises are mandatory for learning and teaching program development.

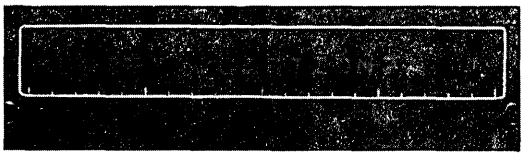
Study AIM 65's gifted professional features and inspired software. Note that it's generally priced lower than most personal computers and its price is only a fraction of those of data terminals. You'll quickly see why AIM 65 is the choice of practicing professionals, and of beginners seriously intent on becoming professionals.

Rockwell AIM 65...inspired

AIM 65's gifted features are realized by its owners through truly inspired software which is made available as "firmware" contained on ROMs. Software packages include:

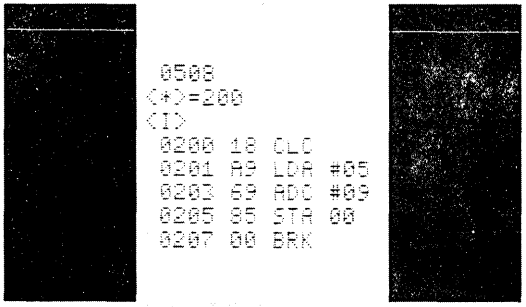
Advanced Interactive Monitor
The heart of AIM 65's software, this program provides you with a comprehensive set of single-keystroke commands — see "Monitor Commands" at right.

All commands are self-prompting: each displays an appropriate message when more information is required, or if you happen to make a mistake, an error code is displayed.



Self-prompting program development.

Included in the Interactive Monitor is a *Mnemonic Assembler* program that translates instructions in simple three-letter abbreviations (called "mnemonics") that we humans easily understand, into binary codes that the microprocessor understands. The Mnemonic Assembler frees you from hassling with the confusing array of hexadecimal "opcodes" that most low-priced microcomputers use.



Mnemonic input for an addition program.

With only the Interactive Monitor installed, you can assemble simple microcomputer programs based on mnemonic entries. This is the best way to start learning how a microcomputer "thinks."

AIM 65's Interactive Monitor contains single-stroke commands enabling you to interface with a powerful but simple-to-use *Text Editor,* or with higher level programming languages — *Symbolic Assembler, BASIC Interpreter, PL/65 Compiler* — all of which are available now and are described later — and with other higher level languages whose firmware is being developed. Applicable commands are shown at right.

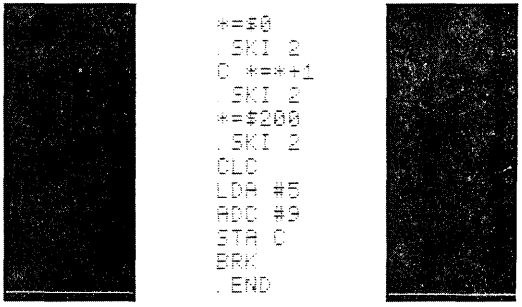
While the Mnemonic and Symbolic Assembler gives aspiring professionals easier-understanding of the fundamentals of programming, the higher level languages facilitate and speed up the process. An analogy is that assembly language programming is like building a house with boards and nails, while high level language programming is like using pre-fabricated sections.

Examples of the programming simplicity that AIM 65's Interactive Monitor software gives you, are the following functions you can command with single keystrokes:

- ☐ Print step-by-step program listings on the on-board printer or on an attached TTY or terminal;
- ☐ Display and change selected Registers and Memory;
- ☐ Set breakpoints, and trace program execution for debugging in single-step modes;
- ☐ Transfer data from attached TTY or cassette recorders, including manipulating programs from one tape to another;
- ☐ Store programs in on-board or external RAM, ROM, PROM, or in other external memories such as tapes, floppy disks, bubbles, etc.

Text Editor
This program is stored as firmware on the same ROMs containing the Interactive Monitor. It gives you the advantages of displayed or printed program entries and listings which are translated by the Symbolic Assembler and the PL/65 Compiler into machine codes. It also gives you superior debug capabilities. Most of the Text Editor's commands—see right—are word-processor-like. The Text Editor even includes a command that automatically locates instructions, comments and labels in the program being developed.

With the Text Editor, you can add, delete and change instructions anywhere in the program without affecting any other portion.



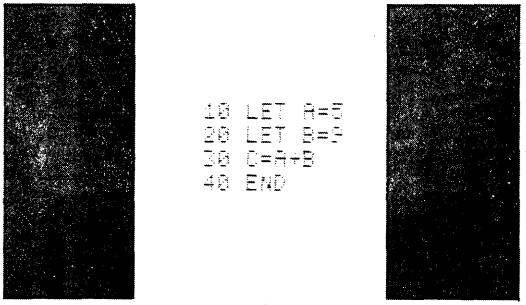
Symbolic input to the Text Editor for same addition program.

Symbolic Assembler
Firmware is contained on a separate ROM. The Symbolic Assembler software gives practicing professionals a highly efficient means for developing the most complex programs permitting the shortcutting of programming time and documentation by assigning labels to instructions, subroutines and data locations.

At the same time, it introduces students to the fundamentals of microcomputer programming in a basically simple fashion.

professional software.

The software inspiration in the AIM 65 approach is that the Interactive Monitor and the Text Editor work together with the Symbolic Assembler to provide displayed and printed details of entries, listings and debug operations.



BASIC version of the same addition program.

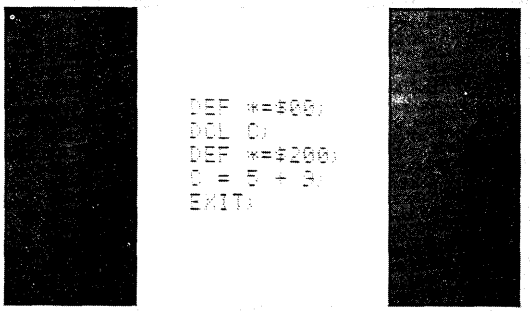
BASIC Interpreter

Firmware is contained on separate ROMs. AIM 65's high-level BASIC is the most effective 8K version developed by Microsoft.

The practicing professional will use BASIC to speed up programming microcomputers designed as systems for many computational and processing applications.

BASIC, which stands for Beginner's All-purpose Symbolic Instructions Code, is also the easy-use language offered by most amateur personal computers for fun and games. Which says that when you want diversion from professional work or learning, your AIM 65's ready.

BASIC is universally recognized as the most easily learned computer programming language. Even a complete microprocessor novice should be able to begin writing BASIC programs after only a few hours of study.



PL/65 version of the same addition program.

PL/65 Compiler

Firmware is contained on two separate ROMs. PL/65 is a high-level language that practicing professionals and advanced students use when large programs have to be developed very rapidly—where software development costs are important.

Rockwell's Future Software Plans

Rockwell is developing firmware for the AIM 65 that will provide owners with high-level languages facilitating a variety of development projects.

Single-Keystroke Monitor Commands

Major Function Entry
(RESET Button)—Enter and initialize Monitor
ESC—Re-enter Monitor
E —Enter and initialize Text Editor
T —Re-enter Text Editor
N —Enter Symbolic Assembler
5 —Enter and initialize BASIC Interpreter
6 —Re-enter BASIC Interpreter

Instruction Entry and Disassembly
I —Enter mnemonic instruction entry mode
K —Disassemble memory

Display/Alter Registers and Memory
* —Alter Program Counter to (address)
A —Alter Accumulator to (byte)
X —Alter X Register to (byte)
Y —Alter Y Register to (byte)
P —Alter Processor Status to (byte)
S —Alter Stack Pointer to (byte)
R —Display all registers
M—Display four memory locations, starting at (address)
(SPACE)—Display next four memory locations
/ —Alter current memory location

Manipulate Breakpoints
—Clear all breakpoints
4 —Toggle breakpoint enable on/off
B —Set one to four breakpoint addresses
? —Display breakpoint addresses

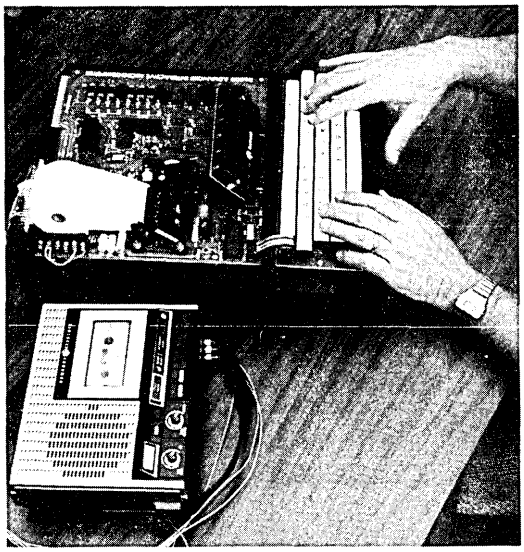
Control Instruction/Trace
G—Execute user's program
Z —Toggle instruction trace mode on/off
V —Toggle register trace mode on/off
H —Trace Program Counter history

Control Peripheral Devices
L —Load object code into memory from peripheral I/O device
D —Dump object code to peripheral I/O device
1 —Toggle Tape 1 control on/off
2 —Toggle Tape 2 control on/off
3 —Verify tape checksum
CTRL PRINT—Toggle Printer on/off
LF—Line Feed
PRINT—Print Display contents

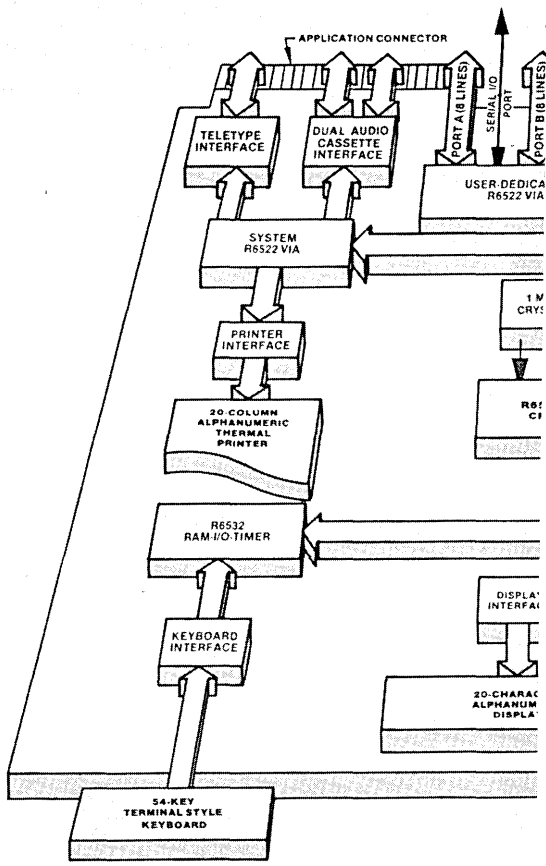
Call User-Defined Functions
F1—Call User Function 1
F2—Call User Function 2
F3—Call User Function 3

Text Editor Commands
R —Read lines into text buffer from peripheral I/O device
I —Insert line into text buffer from Keyboard
K —Delete current line of text
(SPACE)—Display current line of text
L —List lines of text to peripheral I/O device
U—Move up one line
D—Move down one line
T —Go to top line of text
B —Go to bottom line of text
F —Find character string
C—Change character string
Q—Quit Text Editor, return to Monitor

Rockwell AIM 65...more fe



Directly hook up one or two cassette recorders.



Third-Generation R6500 Microprocessor System

Functional heart of the AIM 65 microcomputer is an R6502 CPU (Central Processing Unit). The high-performance 8-bit R6502 has 65K-byte memory addressability and the power of a 56-command, 13-addressing mode, minicomputer-like instruction set.

The R6502 is supported with selected R6500 microprocessor family devices to implement AIM 65's internal system and to provide versatile, used-dedicated applications' interfaces.

An R6522 Versatile Interface Adapter (VIA) provides AIM 65 users with two Input/Output (I/O) ports, each with eight lines, an 8-bit serial I/O port, and access to two on-chip 16-bit interval-timer/event counters.

Broad Applications Options

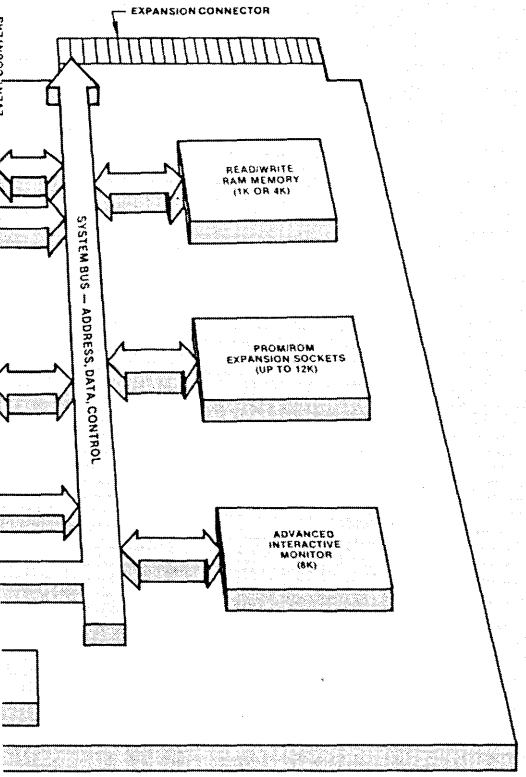
This I/O capability gives you an amazingly broad range of applications options. You can easily interface with sensors and switches to perform item or batch response functions. You can readily include D-A/A-D converters and provide audio and other functions in an AIM 65-based system. (AIM 65 has a nine octave music synthesis capability.)

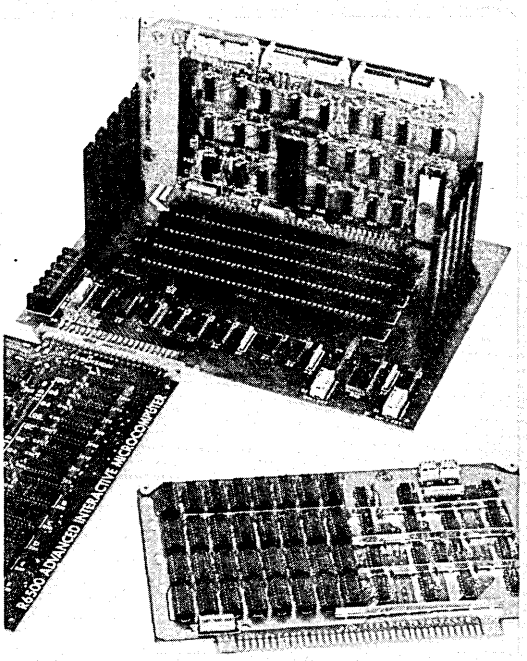
An Application Note is available so that you can interface AIM 65 to a CRT monitor or TV set.

Ingenious professionals also use AIM 65's inspired software to increase its applications potentials. For example, one engineer uses the Text Editor to list and look up stored telephone numbers so that his AIM 65 functions as an automatic telephone dialler.

AIM 65's I/O abilities also allow you to directly hook up one or two cassette recorders. One use of cassette recorders is permanently storing programs you develop for bookkeeping, home environmental and security control, student education, etc. When you want to use your AIM 65 for a special purpose, you simply load the applicable taped program into RAM.

tures for professionals.





Expansion motherboard plugs on to connector.

:xpansion Motherboard Available
'or System Add-On Modules

asily attached to AIM 65's full-bus System Expansion 'onnector is a Motherboard with five slots that hold many tandard and special modules available from Motorola, urr-Brown, Rockwell and other manufacturers.

AIM 65's Expansion Connector and Motherboard carry ıe microcomputer's full system bus lines — address, data nd control — fully buffered to provide ample drive capacity. ddress decode logic for mapping internal and external ddresses in 4K-byte increments is provided.

Using the Expansion Connector and/or the Mother-oard, you can readily enlarge your system to include PROM rogrammer module, PROM modules, floppy disk controller ıodule, RAM modules and other subsystem modules.

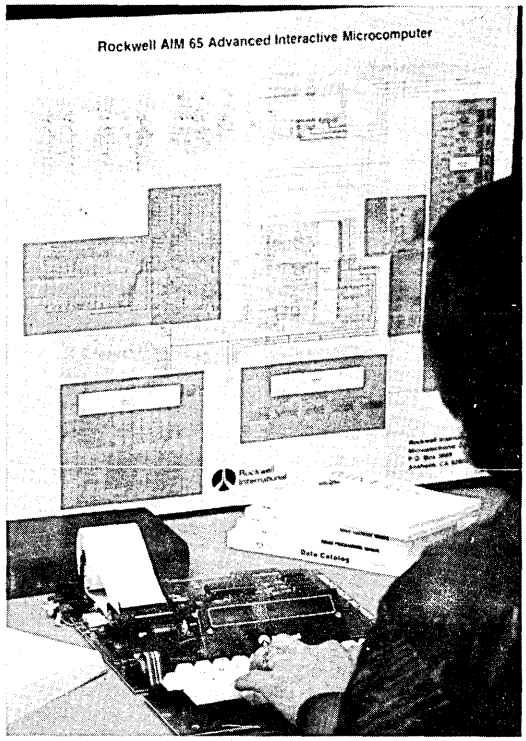
For developing and prototyping systems, you can add Prototyping and Personality Boards designed for the Rockwell SYSTEM 65 (6502 microprocessor) and the Motorola EXORciser® (6800 microprocessor).

To convert your processor or controller into an intelligent terminal, you can easily add a Rockwell R24 Modufar Modem (2400 bps) or slower board modems. This means you can use your AIM 65 to "talk" over ordinary telephone lines to other computers or other AIM 65s.

And your AIM 65 is now ready to let you use the emerging memory generation — Bubble Domain Memories. Under available software control, your AIM 65 can address all 128K-bytes of a Rockwell Bubble Memory module, providing you with a magnificent file directory.

®EXORciser is a registered trademark of Motorola

Rockwell AIM 65...for working



Professionally written texts.

Professionally Written Texts

With your AIM 65, you're supplied with all required explanatory and operating documentation.

AIM 65 texts include: 1) *AIM 65 User's Guide*—450 pages; everything you need to know about operating your AIM 65 in clear, concise language. 2) *AIM 65 Monitor Program Listing*—118 pages; a complete commented listing of AIM 65's ROM-resident Monitor software, with both a symbol table and a cross-reference index. 3) *AIM 65 Summary Card*—pocket size; handy summary of Monitor, Text Editor and Assembler commands, the System Memory Map, R6522 VIA and Monitor subroutines. 4) *AIM 65 Schematic*—A poster-size circuit diagram. 5) *R6500 Programming Manual*—260 pages; reference guide to 6502 assembly language programming; covers many of the I/O and other 6500 family devices. 6) *R6500 Hardware Manual*—208 pages; reference guide to the microprocessors, I/O and other 6500 devices. 7) *R6500 Programming Reference Card*—pocket size; summarizes all instructions and addressing modes for the 6502 CPU. 8) *AIM 65 BASIC Reference Manual*—89 pages; a complete reference guide. By special arrangement with the publishers, Rockwell also offers two excellent books to AIM 65 customers, at reduced prices: 1) *Microprocessor Systems Engineering*—641 pages; college level textbook by R. C. Camp, T. A. Smay and C. J. Triska; generally recognized as an outstanding text for all seriously interested in acquiring professional understanding of microprocessing and microcomputers. 2) *6502 Software Design*—270 pages; tutorial book by L. J. Scanlon; gives a step-by-step approach to programming 6502 microprocessor-based computers in assembly language, with special emphasis on the AIM 65.

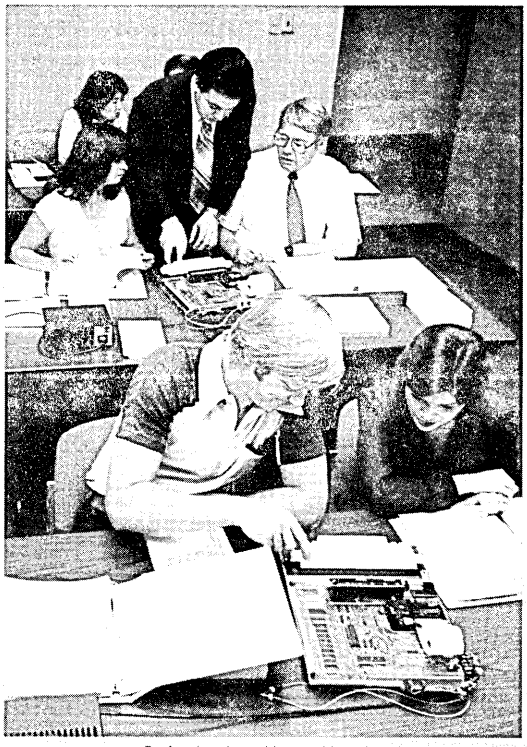
Rockwell Keeps You Current

Your purchase of AIM 65 entitles you to become a subscriber to *Interactive*, a professional newsletter Rockwell publishes regularly to keep AIM 65 owners up to date on innovative design ideas, programming shortcuts and other professional applications data. Subscription price is minimal.

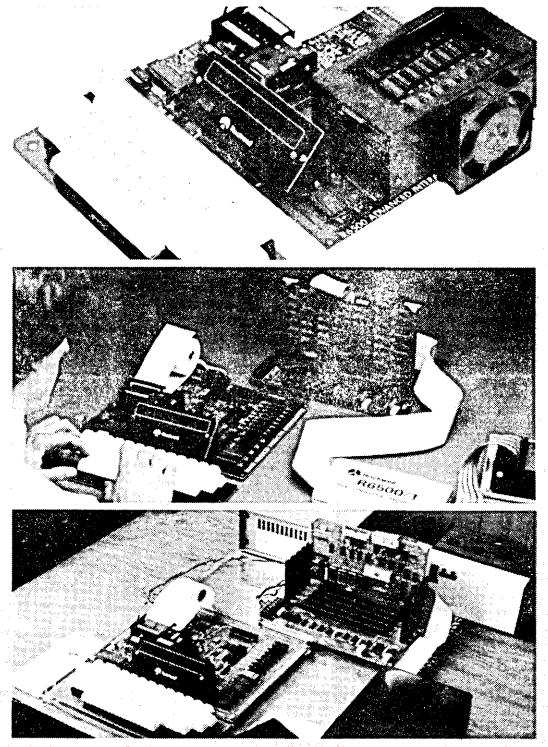
Applications Notes

Rockwell is continually producing Applications Notes which

and learning professionals.



Professional teaching and learning.



Professional microcomputer development.

are available to AIM 65 owners at no charge. New Applications Notes will be described in issues of *Interactive.* Typical of existing Applications Notes are: "Interfacing KIM-4 to AIM 65"—Document R6500 N11; "Using KIM-1 Tapes with AIM 65"—R6500 N19; "Preparing an AIM 65 BASIC Program for PROM/ROM Operation"—R6500 N15; "SYSTEM 65 to AIM 65 Interface"—R6500 N04, "A CRT Monitor or TV Interface for AIM 65"—R6500 N12; "R232C Interface for AIM 65"—R6500 N08.

Professional Teaching and Learning

AIM 65 is tops in any class for microprocessor learning. And its special educational features come at a low price school budgets can afford. Its on-board printer produces hard copies of exercises for easy checking by student and instructor. Interactive Monitor software prompts students each step of the way in learn-through-doing education.

Microcomputer Design Courses

Rockwell offers 6500 microcomputer design courses that include using the AIM 65. For details, schedules, locations, contact Rockwell Offices—see back cover of this brochure.

Professional Microcomputer Development

Now for a few hundred dollars—instead of many thousands—AIM 65 functions as a complete programming and system development aid. Personality modules are available. You can develop your program in RAM, store it on tape or floppy disk for debugging and prototyping, then transfer it into PROM for field testing.

Rockwell AIM 65...fo

AIM 65 MICRO-COMPUTER

Process control and management, chemical mixing and control, test equipment and instrumentation, data logging and computing... AIM 65 as a "bare-board" microcomputer is already being used in an astonishing variety of work assignments.

For a few hundred dollars, the "bare-board" AIM 65 gives you dedicated or programmable controllers or processing systems that duplicate functions now being performed with minicomputers costing thousands of dollars.

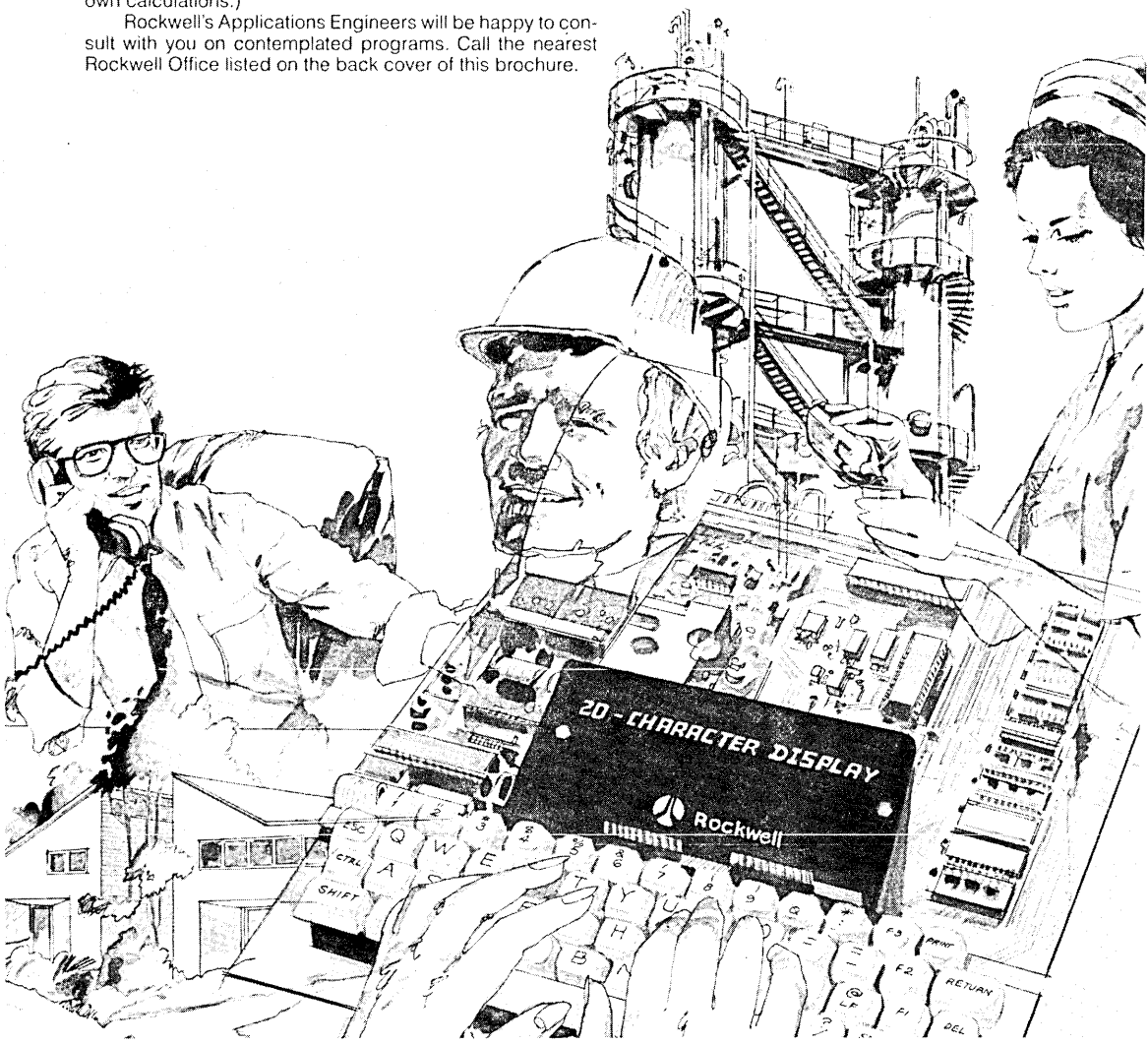
And today the "bare-board" AIM 65 has proved to be economically feasible as the implementing system of control and processing products designed for low-volume use. (100 units a year is a generalized rule of thumb, but do your own calculations.)

Rockwell's Applications Engineers will be happy to consult with you on contemplated programs. Call the nearest Rockwell Office listed on the back cover of this brochure.

Bare-Board AIM 65 Is Now Being Used in Low-Volume Products Like:

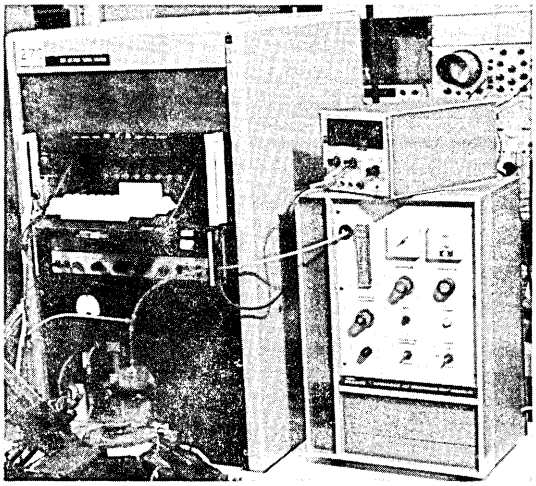
Electronic Components Testers	Radio Burst Testers
Energy Management Systems	Machine Tool Controllers
Card and Badge Readers	Digital Plotting Systems
Chemical Mixing Controllers	Coin Counters
Hotel Wake-Up Systems	Medical Equipment
Manufacturing Controllers	Postal Scales
Industrial Appliance Controllers	Label Printers

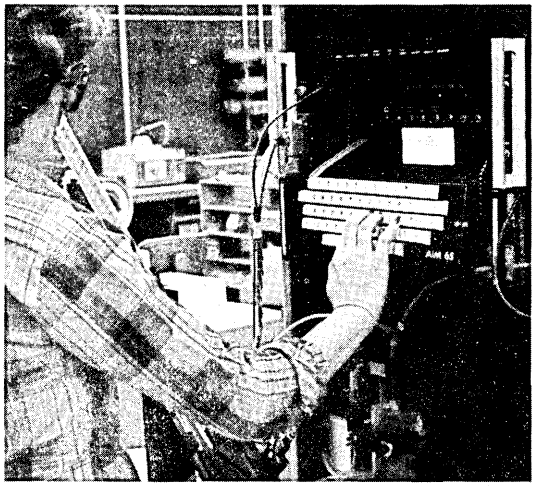
AIM 65 Lets Professional Imaginations Fly but Keeps Product Costs on the Ground...



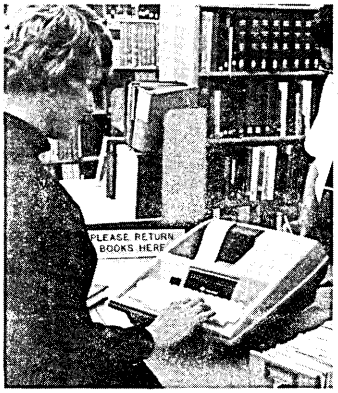
...professional work.

Designed in Days instead of Months...Costing Hundreds instead of Thousands of Dollars...AIM 65-based Systems Record, File, Retrieve, Analyze, Compare Data...Monitor and Control Processes and Operations

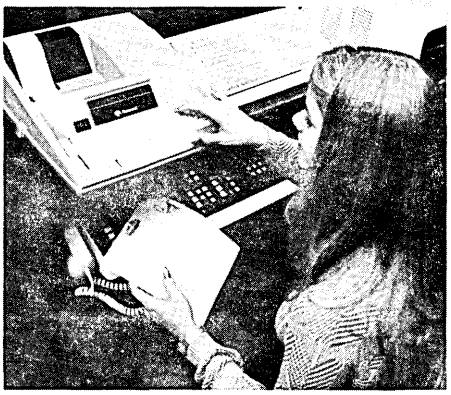




Programmable Machining Controller.

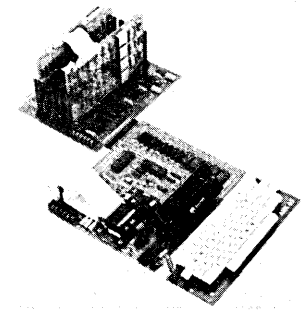


Data Logger and Retrieval.



Office Computer and Hotel Wake-Up.

Programmable Process Controller.



AIM 65 with a million bits of Rockwell bubble memory

AIM 65 puts a roomfull of computing power in your hands

AIM 65
The Professional's Microcomputer...
more of the power in
ROCKWELL MICROPOWER

AIM 65 MICRO-COMPUTER

DQCUMENT NO. 29650 N57
MAY 1979

PART NUMBER
A65-009

Rockwell

R6500 Microcomputer System
PRODUCT DESCRIPTION

AIM 65 EXPANSION MOTHERBOARD

OVERVIEW

The AIM 65 Expansion Motherboard (Part No. A65-009) is used to extend the AIM 65 system bus to external add-on modules. Its five on-board connectors support all modules designed for Rockwell's SYSTEM 65 or Motorola's Exorcisor®, as well as other modules offered by Rockwell, Motorola, Burr-Brown and a variety of other manufacturers.

The AIM 65 system bus lines (address, data and control) are buffered to provide ample drive capability. Address decode logic for mapping internal and external addresses in 4K-byte increments is also provided.

® "Exorcisor" is a registered trademark of Motorola, Inc.

FEATURES

- AIM 65 bus expansion
- Accepts up to five compatible modules
- Address selection in 4K-byte increments
- System bus lines are fully buffered
- DMA logic provided

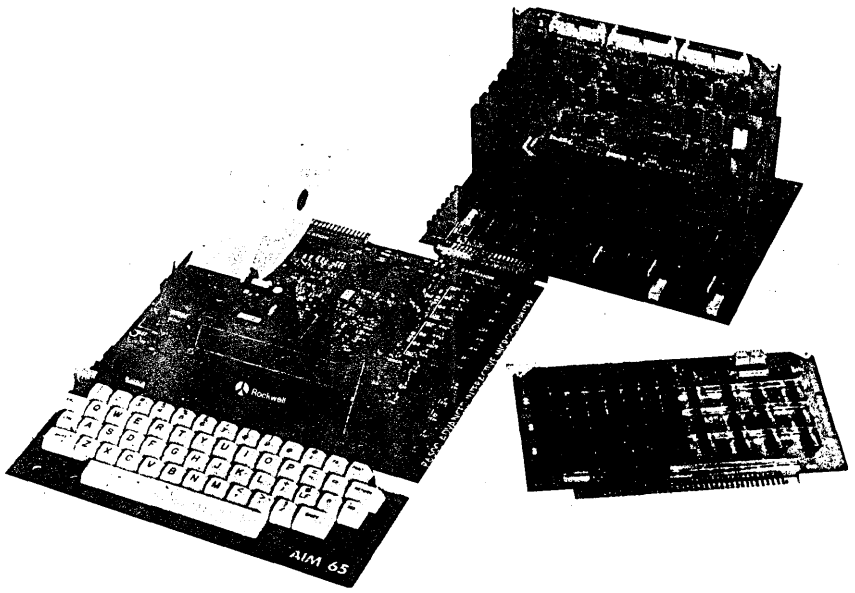
FUNCTIONAL DESCRIPTION

In reading the following text, refer to the attached schematic, PA00-X143.

The Address Bus lines A0-A15 and Control Bus lines Ø2, SYNC, R/$\overline{W}$ and Ø1 from the AIM 65 are buffered with 8T97 devices Z3, Z4, Z5 and Z6. The Data Bus lines D0-D7 are buffered and inverted with 8T26A devices Z1 and Z2. The address, data and R/$\overline{W}$ lines are controlled by the external $\overline{DMA}$ line. If $\overline{DMA}$ is high, the address, data and R/$\overline{W}$ buffers are enabled to drive. If $\overline{DMA}$ is low, these buffers are placed in the off state, allowing an external controller to drive the address, data and R/$\overline{W}$ lines. The remaining buffered lines, Ø1, Ø2 and SYNC, are unaffected by the state of $\overline{DMA}$.

Control lines RDY, $\overline{RES}$, $\overline{NMI}$, $\overline{IRQ}$ and S.O. are unbuffered, but are brought directly to the AIM 65 Expansion Connector.

Address decoding is provided on the AIM 65 Expansion Motherboard. Device Z10 (SN74159) is used to decode the four high-order address lines, A12-A15. The one-of-16 outputs are connected to a set of 16 switches, S1 and S2. When one or more of the switches are closed/opened, the decode logic (Z11, Z7, $\overline{Z8}$ and Z9) enables/disables Data Bus drivers Z1 and Z2. The R/$\overline{W}$ line determines the direction of data flow.



SWITCHES AND JUMPERS

Internal/External Address Selection Switches

Sixteen switches on the AIM 65 Expansion Motherboard permit the user to define whether each 4K-byte portion of the system address space is internal or external to the AIM 65. When a switch is set to ON, its corresponding 4K address range is external (i.e., on the AIM 65 Expansion Motherboard). Conversely, when a switch is set to OFF, its corresponding 4K address range is internal (i.e., on the AIM 65 Microcomputer). Table 1 shows the address range corresponding to each switch on the Expansion Motherboard.

CAUTION

Be careful in assigning external address space, since it may conflict with internal functions of the AIM 65. See Section 7.3.2 of the AIM 65 User's Guide for AIM 65 address assignments.

Table 1. Address Selection Table

Switch	Address Range (Hex)
S2-1	0000 to 0FFF
-2	1000 to 1FFF
-3	2000 to 2FFF
-4	3000 to 3FFF
-5	4000 to 4FFF
-6	5000 to 5FFF
-7	6000 to 6FFF
-8	7000 to 7FFF
S1-8	8000 to 8FFF
-7	9000 to 9FFF
-6	A000 to AFFF
-5	B000 to BFFF
-4	C000 to CFFF
-3	D000 to DFFF
-2	E000 to EFFF
-1	F000 to FFFF

DC Power Selection Jumpers

Power for the AIM 65 Expansion Motherboard can be supplied in either of two ways. For add-on modules with current requirements of less than 0.5 amp, the DC power (+5, +12 and -12 Vdc) brought in on AIM 65 Expansion Connector J3 is adequate. For higher current requirements, DC power should be supplied through Expansion Connector power strip TB1, and Jumpers W1 (+5 Vdc), W2 (+12 Vdc) and W3 (-12 Vdc) should be removed.

Ø2 Clock Jumper

AIM 65 Expansion Motherboard connectors J2 through J6 provide the Ø2 clock on Pin J. This clock signal can be optionally provided on Pin L as well, by installing Jumper W4 on the Expansion Motherboard.

INSTALLATION

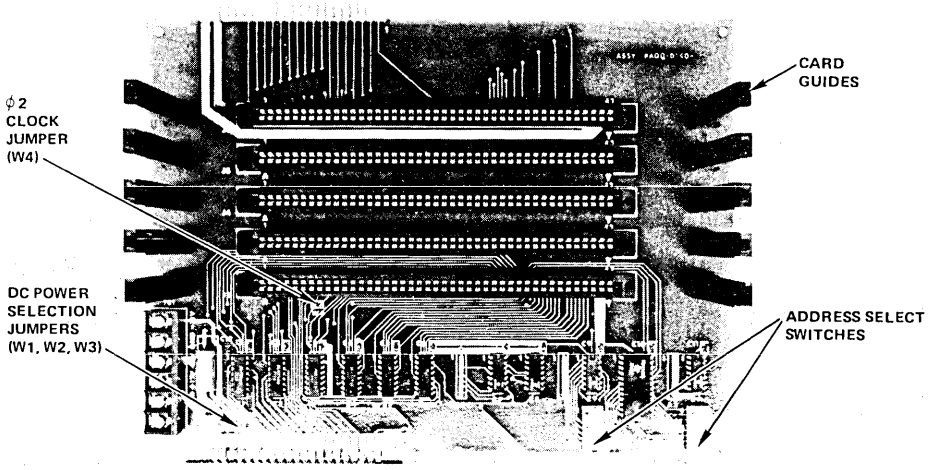
The following procedure should be used to install the AIM 65 Expansion Motherboard onto the AIM 65 Microcomputer:

1. Mount the ten supplied card guides on the AIM 65 Expansion Motherboard with the screws provided (two screws per guide), with one card guide on each end of connectors J2 through J6.
2. The kit includes five self-adhesive rubber feet. Install a rubber foot in each corner of the Expansion Motherboard, and one foot in the center.
3. Remove jumpers W1, W2 and W3, if required. See DC Power Selection Jumpers.
4. Certain add-on modules access the Ø2 clock on Pin L. Install Jumper W4 if your add-on modules have this requirement.
5. Connect Expansion Motherboard Connector P1 to AIM 65 Expansion Connector J3.

CAUTION

Never install or remove the AIM 65 Expansion Motherboard or add-on modules with system power on. It may cause damage to the AIM 65, the Expansion Module or the add-on module.

6. Install the add-on modules into any of the slots on the AIM 65 Expansion Motherboard, J2 through J6, with the component side of each add-on module facing the AIM 65.
7. Configure address selection Switches S1 and S2, as appropriate to your system. See Internal/External Address Selection Switches.
8. Apply power to the AIM 65 and, if required, to the AIM 65 Expansion Motherboard.



USING MULTIPLE EXPANSION MOTHERBOARD

Edge connector J1 on the AIM 65 Expansion Motherboard permits you to install additional Expansion Motherboards in your system. The pinouts on J1 are the same as on P1, except that the Data Bus signals are inverted on J1. Therefore, on each additional Expansion Motherboard the socketed Data Bus driver devices, Z1 and Z2, must be replaced with the 8T28 noninverting drivers before installing those Expansion Motherboards in the system.

Further, address selection switches S1 and S2 on the first Expansion Motherboard must have all external address ranges of its own, as well as all subsequent modules, selected. Similarly, the second Expansion Motherboard must have all external address ranges of its own and subsequent modules selected, and so on.

For example, consider a system with three AIM 65 Expansion Motherboards. In this system, addresses $4000 through $4FFF are dedicated to devices on Expansion Motherboard #1 (the Module connected to the AIM 65), addresses $7000 through $8FFF are dedicated to devices on Expansion Motherboard #2 and addresses $9000 through $9FFF are dedicated to devices on Expansion Motherboard #3. The switch settings for the three Expansion Motherboards are as follows:

- On Expansion Motherboard #1, Switches S2-5, S2-8, S1-8 and S1-7 must be ON; all other switches must be OFF.
- On Expansion Motherboard #2, Switches S2-8, S1-8, and S1-7 must be ON; all other switches must be OFF.
- On Expansion Motherboard #3, Switches S1-7 must be ON; all other switches must be OFF.

EXPANSION MOTHERBOARD PIN ASSIGNMENTS

Connectors P1 and J1

Connector P1, the interface to the AIM 65 microcomputer, is a 44-pin connector with pin assignments given in Table 2.

The same bus signals are extended out to Edge Connector J1 on the AIM 65 Expansion Motherboard except that the Data Bus signals D0 through D7 on connector pins 15 through 8 are presented in inverted form ($\overline{D0}$-$\overline{D7}$) on Connector J1.

Connectors J2 through J6

Table 3 shows the pin assignments for Connectors J1 through J6 on the AIM 65 Expansion Motherboard. **Unused pin locations are interconnected on Connectors J2 through J6.**

Table 2. Pin Assignments for Connector P1

PIN	SIGNAL	PIN	SIGNAL
22	GND	Z	RAM R/$\overline{W}$
21	+5V	Y	$\overline{\emptyset 2}$
20	$\overline{CSA}$	X	TEST
19	$\overline{CS9}$	W	R/$\overline{W}$
18	$\overline{CS8}$	V	SYS R/$\overline{W}$
17	+12V	U	SYS Ø2
16	-12V	T	A15
15	D0	S	A14
14	D1	R	A13
13	D2	P	A12
12	D3	N	A11
11	D4	M	A10
10	D5	L	A9
9	D6	K	A8
8	D7	J	A7
7	$\overline{RES}$	H	A6
6	$\overline{NMI}$	F	A5
5	S.O.	E	A4
4	$\overline{IRQ}$	D	A3
3	Ø1	C	A2
2	RDY	B	A1
1	SYNC	A	A0

Table 3. Pin Assignments for Connectors J2-J6

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	+5 VDC	23		A	+5 VDC	$\overline{A}$	SYNC
2	+5 VDC	24	GND	B	+5 VDC	$\overline{B}$	GND
3	+5 VDC	25		C	+5 VDC	$\overline{C}$	S. O.
4		26	GND	D	$\overline{IRQ}$	$\overline{D}$	DMA
5	$\overline{RES}$	27	RDY	E	$\overline{NMI}$	$\overline{E}$	
6	R/W	28	WP7*	F		$\overline{F}$	
7	Ø1	29	D1	H	GND	$\overline{H}$	$\overline{D3}$
8	GND	30	$\overline{D5}$	J	Ø2	$\overline{J}$	$\overline{D7}$
9	GND	31	$\overline{D0}$	K	GND	$\overline{K}$	$\overline{D2}$
10	***	32	$\overline{D4}$	L	(Ø2)**	$\overline{L}$	$\overline{D6}$
11	-12 VDC	33	A15	M	-12 VDC	$\overline{M}$	A14
12		34	A12	N		$\overline{N}$	A13
13		35	A11	P		$\overline{P}$	A10
14		36	A8	R		$\overline{R}$	A9
15		37	A7	S		$\overline{S}$	A6
16	+12 VDC	38	A4	T	+12 VDC	$\overline{T}$	A5
17		39	A3	U		$\overline{U}$	A2
18		40	A0	V		$\overline{V}$	A1
19	WP4*	41	GND	W		$\overline{W}$	GND
20	WP5*	42	GND	X	WP1*	$\overline{X}$	GND
21		43	GND	Y	WP3*	$\overline{Y}$	GND
22	WP6*			Z	WP2*		

*Tied directly to ground, disabling write-protect feature.
**If jumper W4 installed.
***3K pull-up RESISTOR to +5 VDC.

SPECIFICATIONS

Motherboard Dimensions:	11.3 in. x 8.95 in.
Expansion Capacity:	Five modules
Interfaces:	AIM 65 and SYSTEM 65 compatible
Edge Connectors:	44 pins on 0.156 in. centers
Expansion Connectors:	86 pins on 0.156 in. centers
Operating Temperature:	$0^{o}C$ to $+70^{o}C$
Power Requirements (Module Only):	+5 Vdc ±5% @ 0.8 amp

LOGIC LEVELS

$T_A = 0^{o}C$ to $+70^{o}C$, $V_{CC} = +5V \pm 5\%$

Characteristic	Symbol	Min	Max	Unit	Conditions
Inputs					
A0-A15, D0-D7, Ø2, Ø1, SYNC, R/$\overline{W}$	V_{IL}		0.8	V	I_{IL} = -400 µA
$\overline{D0}$-$\overline{D7}$	V_{IH}	2.0	V_{CC}	V	I_{IH} = 40 µA
Outputs					
D0-D7	V_{OL}		0.5	V	I_{OL} = 20 ma
	V_{OH}	2.4		V	I_{OH} = -2 mA
$\overline{D0}$-$\overline{D7}$	V_{OL}		0.5	V	I_{OL} = 48 ma
	V_{OH}	2.4		V	I_{OH} = 10 ma
A0-A15, Ø2, Ø1	V_{OL}		0.5	V	I_{OL} = 48 ma
SYNC, R/$\overline{W}$	V_{OH}	2.4		V	I_{OH} = -5.2 ma

PART NUMBER
A65-901

Rockwell

AIM 65 DATA SHEET

AIM 65 PROM PROGRAMMER AND CO-ED MODULE

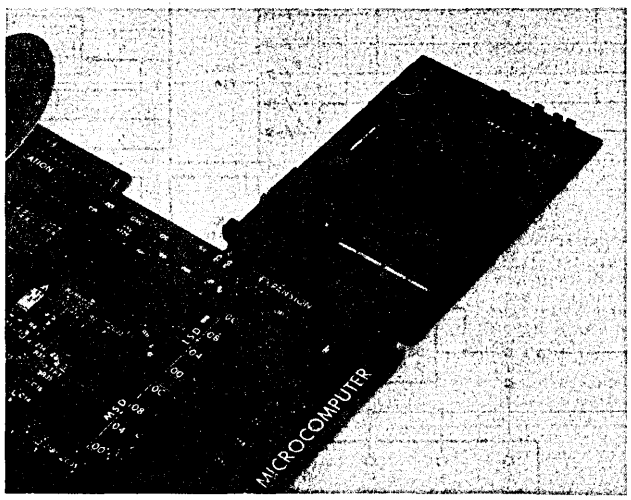
The AIM 65 PROM Programmer and CO-ED Module (A65-901) programs 1K-, 2K-, and 4K-byte PROMs that can be installed in the AIM 65 or in a Microflex 65 16K PROM/ROM Module. The PROM Programmer provides check, program, verify and read functions.

The utility of the Module is enhanced through the included Object Code Editor (CO-ED). CO-ED allows you to edit object code in much the same way as you can edit source code for the AIM 65 Assembler, using AIM 65's Text Editor. With CO-ED, patches can be made directly in your program without having to go through the time-consuming process of re-assembling.

The AIM 65 PROM Programmer and CO-ED Module also supports data load, verify and dump with offset functions. And the Module plugs directly into the AIM 65 Expansion Connector.

FEATURES

- Plugs directly onto the AIM 65 Expansion Connector
- Programs the following 5 volt PROMs (or equivalents):
  - Intel 2758, 2716 and 2732
  - TI TMS 2508, 2516 and 2532
- Provides programming functions to check, program, verify and read PROM
- Includes utility functions to load, verify, dump, fill and and invert memory
- Incorporates object code editor (CO-ED) functions to control program pointers; search for operands, jumps/branches and strings; and to modify instructions with automatic address adjustment
- 1K bytes of Static RAM are included to allow single-pass programming of a 4K-byte PROM when used with a 4K RAM version of AIM 65
- Zero insertion force (ZIF) socket for PROM being programmed
- On-board DC/DC Converter allows +5V-only operation
- Fully assembled, tested and warranted



Specifications subject to change without notice
Document No. RMA65 N17
September 1980

FUNCTIONAL DESCRIPTION

The R6520 Peripheral Interface Adapter (PIA) is the primary interface device between the AIM 65 Expansion Connector and the 24-pin Zero Insertion Force PROM socket and control circuits. During PROM programming, PROM address, PROM data and programming control signals are transmitted to the PIA on the AIM 65 Expansion Connector data lines. During PROM check, verify and read operations, only PROM address and control signals are issued to the PIA from the AIM 65.

Four PIA I/O Lines carry the most significant address signals to the PROM. Eight other PIA I/O lines multiplex the PROM data and least significant address signals. One output line controls the Tri-State Data Latch. Five other PIA I/O Lines control the Power Switches.

During PROM programming, PROM data is transferred to the tri-state Data Latch, which drives the latched data to the PROM. The PROM address is then sent to the PROM on the eight multiplexed data/address lines and the four dedicated address lines. The Power Switches are then turned on to apply the proper voltage levels for the required time duration to transfer the 8-bits of data into one PROM location. The process is repeated until the specified PROM address range is fully programmed. The tri-state Data Buffer is disabled during programming.

During PROM read operations, the PIA sets the address lines to the PROM. The tri-state Data Buffer drives the PROM data onto the AIM 65 Expansion Connector data lines. The Data Latch is disabled at this time.

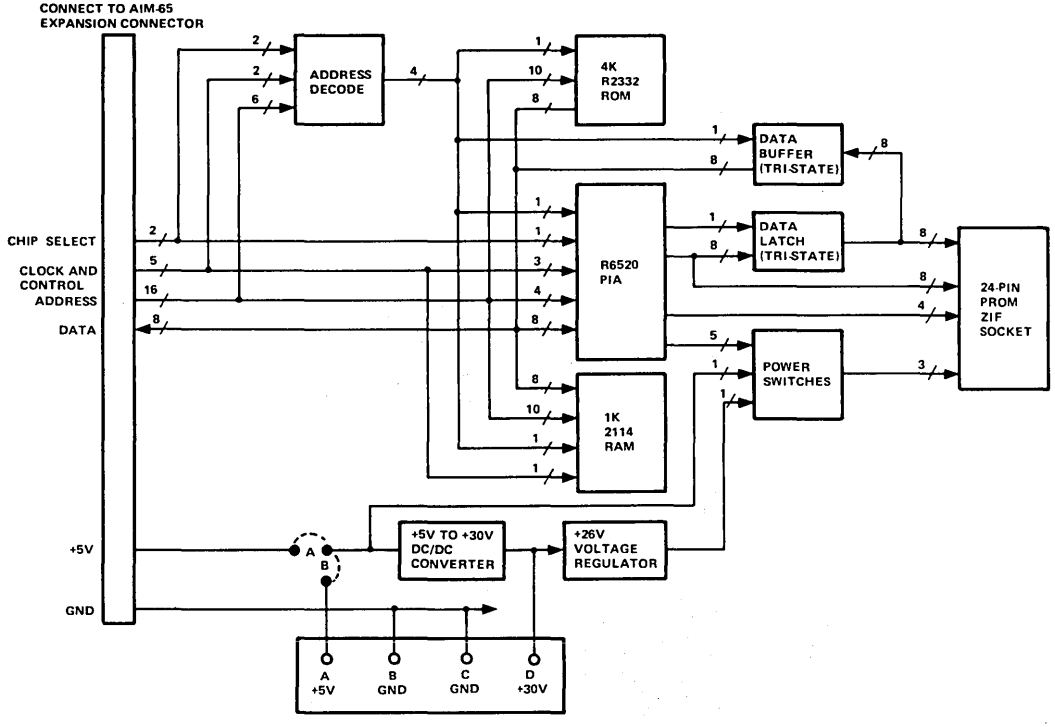
The Power Switches drive +5V or +26V onto three PROM socket programming lines depending on the PROM type selected.

The 4K R2332 ROM contains the PROM Programmer and CO-ED firmware.

1K bytes of on-board RAM are provided for use by the PROM Programmer and CO-ED software. The RAM is mapped from $1000-$13FF to provide contiguous addressing from the top of a 4K RAM AIM 65.

The Address Decode circuitry generates individual chip select signals to the RAM, ROM, PIA and the Data Buffer.

The PROM Programmer and CO-ED Module may be powered from the AIM 65 or from an external +5V power supply. A DC/DC Voltage Converter generates +30V from +5V. The +30V is regulated to +26V for on-board use. The +30V may be connected to an external power supply to minimize current drain on the +5V supply.



AIM 65 PROM Programmer and CO-ED Module Block Diagram

AIM 65 Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
SYNC	*Sync	O	1	A	A0	Address Bit 0	I
RDY	*Ready	I	2	B	A1	Address Bit 1	I
$\phi 1$	*Phase 1 Clock	O	3	C	A2	Address Bit 2	I
$\overline{IRQ}$	*Interrupt Request	I	4	D	A3	Address Bit 3	I
S.O.	*Set Overflow	I	5	E	A4	Address Bit 4	I
$\overline{NMI}$	*Non-Maskable Interrupt	I	6	F	A5	Address Bit 5	I
$\overline{RES}$	Reset	I	7	H	A6	Address Bit 6	I
D7	Data Bit 7	I/O	8	J	A7	Address Bit 7	I
D6	Data Bit 6	I/O	9	K	A8	Address Bit 8	I
D5	Data Bit 5	I/O	10	L	A9	Address Bit 9	I
D4	Data Bit 4	I/O	11	M	A10	Address Bit 10	I
D3	Data Bit 3	I/O	12	N	A11	Address Bit 11	I
D2	Data Bit 2	I/O	13	P	A12	Address Bit 12	I
D1	Data Bit 1	I/O	14	R	A13	Address Bit 13	I
D0	Data Bit 0	I/O	15	S	A14	Address Bit 14	I
-12V	*-12 Vdc		16	T	A15	Address Bit 15	I
+12V	*+12Vdc		17	U	SYS $\phi 2$	System Phase 2 Clock	O
$\overline{CS8}$	Chip Select 8	O	18	V	SYS R/$\overline{W}$	System Read/Write	O
$\overline{CS9}$	Chip Select 9	O	19	W	R/$\overline{W}$	Read/Write "Not"	O
$\overline{CSA}$	*Chip Select A	O	20	X	TEST	Test	O
+5V	+5 Vdc		21	Y	$\overline{\phi 2}$	Phase 2 Clock "Not"	O
GND	Ground		22	Z	RAM R/$\overline{W}$	RAM Read/Write	O

NOTE:

* = Not used on this module.

PROM Programmer Commands

Category	Command	Function
ENTRY/EXIT	F1	ENTER PROM PROGRAMMER
	F2	RE-ENTER PROM PROGRAMMER
	ESC	ESCAPE TO MONITOR
BASE ADDRESS	B	PROM BASE ADDRESS
	O	RAM BASE ADDRESS
PROM	C	CHECK PROM
	P	PROGRAM PROM
	V	VERIFY PROM
	R	READ PROM
MEMORY	L	LOAD MEMORY
	T	VERIFY MEMORY
	D	DUMP MEMORY
	M	FILL MEMORY
	I	INVERT MEMORY
RECORDER CONTROL	1	TOGGLE RECORDER CONTROL LINE 1 ON/OFF
	2	TOGGLE RECORDER CONTROL LINE 2 ON/OFF

CO-ED Commands

Category	Command	Function
ENTRY/EXIT	F3	ENTER CO-ED
	/	EXIT CO-ED
	ESC	ESCAPE TO MONITOR
POINTER CONTROL	W	LOCATE PROGRAM
	T	MOVE TO TOP OF PROGRAM
	B	MOVE TO BOTTOM OF PROGRAM
	U	MOVE UP ONE INSTRUCTION
	D	MOVE DOWN ONE INSTRUCTION
	G	GO TO ADDRESS
	X	EXCHANGE POINTERS
SEARCH	F	FIND AN OPERAND
	J	FIND JUMPS AND BRANCHES
	S	FIND A STRING
PROGRAM MODIFICATION	I	INSERT AN INSTRUCTION
	$	STRIKEOUT AN INSTRUCTION
	A	ADJUST INSTRUCTION BLOCK
	C	CHANGE INSTRUCTION
	M	MOVE INSTRUCTION/DATA BLOCK
	R	RELOCATE
UTILITY	!	FILL MEMORY
	K	DISASSEMBLE MEMORY

PROM Programmer and CO-ED Module Physical and Electrical Characteristics

Characteristic	Value
Dimensions	
Width	4.4 in. (111 mm)
Length	6.3 in. (160 mm)
Height	0.75 in. (19 mm)
Weight	5.3 oz. (150 g)
Environment	
Operating Temperature	$0^{o}C$ to $70^{o}C$
Storage Temperature	$-40^{o}C$ to $85^{o}C$
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
With DC/DC Converter	+5V ±5%, 1.1 A (5.5 W) – Maximum
Without DC/DC Converter	+5V ±5%, 0.75 A (3.75 W) – Maximum +30V ±5%, 0.04A (1.2 W) – Maximum
Memory Map	
User RAM:	$1000 – $13FF
I/O:	$8800 – $8FFF
ROM:	$9000 – $9FFF

Implement Your Designs with . . .

Rockwell

AIM 65 FORTH

- APPLICATION ORIENTED
- EXTENSIBLE LANGUAGE
- OVER 200 PRE-DEFINED FUNCTIONS
- INTERACTIVE COMPILATION
- REVERSE POLISH NOTATION
- ROM RESIDENT
- COMPACT MEMORY USAGE
- HIGH SPEED EXECUTION
- EASY DEBUGGING
- STACK IMPLEMENTATION
- SHORTENS SOFTWARE DEVELOPMENT TIME
- BUILD-IN STRUCTURED ASSEMBLER

AIM 65 Forth is a unique programming language that is well suited to a variety of applications. Because it was originally developed for real-time control applications, Forth has features that make it ideal for machine and process control, energy management, data acquisition, automatic testing, robotics and other applications where assembly language was previously considered to be the only possible language choice.

Forth vs. Other Languages

Forth actually provides the best of two worlds. It has the looping and branching constructs of high-level languages (DO . . . LOOP, BEGIN . . . END, IF . . . THEN and IF . . . ELSE . . . THEN) and the code efficiency of machine and assembly languages. And programmers will be pleased to know that Forth allows you to specify addresses, operands and data in hexadecimal, octal, binary or any other number base from two to 40—a distinct advantage over languages like Basic, where all information must be in decimal.

In most time-critical applications, at least part of the program must be written in assembly language. AIM 65 Forth has a built-in 6502 macro assembler, and lets you drop into assembly language at almost any point in your program, without separate assembly and load steps or awkward machine level linkage. Forth programs typically run up to ten times faster than other interpretive languages, and can even approach the speed of machine language programs for some applications.

Developing Forth Programs

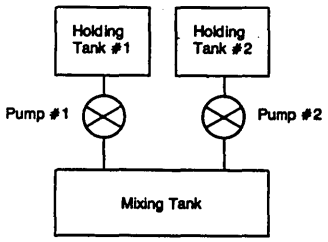
Forth is built on subroutine-like functions, called "words." These words are linked together to form a "dictionary," which is the central core of the language. Writing a program in Forth consists of using several predefined words to define each new word. Once the new word has been added to the system dictionary, it becomes as much a part of the language as any other word that has been previously defined. In this way new features and extensions can be added by simply defining one or more new words. Adding new features to conventional languages like Basic or Pascal requires the language system to be completely reassembled or recompiled.

Forth is a stack-oriented language, and is programmed in Reverse Polish Notation (RPN), the notation that is used in Hewlett-Packard scientific calculators. Using a data stack is an extremely efficient way of passing variables back and forth between operations. A data stack eliminates the need to tie up memory locations with variable tables, and allows you to use only as much memory as you need.

Forth programs are developed using "top-down/bottom-up" techniques. That is, the programmer begins by defining the program in very general terms, then systematically breaks these definitions down into more and more detailed sub-modules. When the lowest levels of sub-modules have been defined, he starts coding, in Forth, at those levels, working back up toward the top of the program, in pyramid fashion. Each sub-module is a stand-alone component of the program, and can be completely debugged without having the complete program in the system. This type of software development is difficult, if not impossible, to do with most other high-level languages.

A Forth Example Program

As an example of a Forth application, suppose we have a chemical processing plant that includes two holding tanks that pump into a mixing tank. When the mixing tank is full, both pumps must shut off and allow the liquid to mix for ten minutes. Here's a block diagram of this part of the system:



The functional steps needed to perform the operation are:

1. Start Pump #1
2. Start Pump #2
3. Wait until the Mixing Tank is full
4. Stop Pump #1
5. Stop Pump #2
6. Mix for 10 minutes

With the major operations now defined, we can begin writing our Forth program. Let's call the program MIX-BATCH. It would look like this:

```
: MIX-BATCH

    START-PUMP1
    START-PUMP2
    WAIT-TIL-TANK-FULL
    STOP-PUMP1
    STOP-PUMP2
    FOR-10-MINUTES
    MIX ;
```

Document No. 29650 N88
October 1980

Notice how similar this program is to our functional breakdown. It's also very readable. The colon (:) tells Forth that we are defining a new word; MIX-BATCH, in this case. The semicolon (;) on the last line, after MIX, indicates the end of the definition. The words between MIX-BATCH and the semicolon represent the operations that will be performed when the word MIX-BATCH is executed. All of these words—START-PUMP1, START-PUMP2, WAIT-TIL-TANK-FULL and so on—must have been previously defined using AIM 65 Forth words or other, user-defined words.

For instance, START-PUMP1 may be constructed from two general input/output control words for the AIM 65's user-dedicated R6522 VIA, as follows:

```
: START-PUMP1   PORTB1=OUTPUT   SET-B1=HIGH ;
```

In this definition, PORTB1=OUTPUT establishes Bit 1 of the VIA as an output and SET-B1=HIGH sets the output to a +5V level, which turns on the pump motor. Either of these words (or any other Forth words) could be defined in either Forth or assembly language. Existing assembly language programs and subroutines may be directly used by Forth.

What You Get With AIM 65 Forth

AIM 65 Forth is contained on two 4K ROMs, which plug into sockets on the AIM 65 board. Because Forth uses memory and I/O so efficiently, complex programs can be developed on AIM 65 with just 4K bytes of RAM and one cassette recorder. Forth also comes with a complete and easy-to-use reference manual. For more information, or to order AIM 65 Forth (Part No. A65-050), contact

Marketing Services
ROCKWELL INTERNATIONAL
P.O. Box 3669, RC55
Anaheim, CA 92803

or call 800/854-8099 (in California, 800/422-4230).

AIM 65 FORTH WORDS

ni = 16-bit signed number on the stack (n1 is the deepest value).
di = 32-bit signed number on the stack (d1 is the deepest value).
ui = 16-bit unsigned number on the stack (u1 is the deepest value).

STACK MANIPULATION

DUP	Duplicate top of stack.
2DUP	Duplicate top two stack items.
DROP	Delete top of stack.
2DROP	Delete top two stack items.
SWAP	Exchange top two stack items.
OVER	Copy second item to top.
ROT	Rotate third item to top.
-DUP	Duplicate only if non-zero.
>R	Move top item to return stack.
R>	Retrieve item from return stack.
R	Copy top of return stack onto stack.
PICK	Copy the nth item to top.
SP@	Return address of stack position.
RP@	Return address of return stack pointer.
SO	Return address of pointer to bottom of stack.
BOUNDS	Convert "address count" to "end-address start-address."
.S	Print contents of stack.

NUMERIC REPRESENTATION

DECIMAL	Set decimal base.
HEX	Set hexadecimal base.
BASE	Set number base.
DIGIT	Convert ASCII to binary.
0	The number zero.
1	The number one.
2	The number two.
3	The number three.

COMPARISON OPERATORS

<	True if n1 less than n2.
>	True if n1 greater than n2.
=	True if top two numbers are equal.
0<	True if top number negative.
0=	True if top number zero.
U<	True if u1 less than u2.
NOT	Same as 0=.

ARITHMETIC AND LOGICAL

+	Add.
D+	Add double-precision numbers.
-	Subtract (n1 - n2).
*	Multiply.
/	Divide (n1/n2).
MOD	Modulo (i.e. remainder from division).
/MOD	Divide, giving remainder and quotient.
*/MOD	Multiply, then divide (n1*n2/n3), with double intermediate.
*/	Like */MOD, but give quotient only.
U*	Unsigned multiply leaving double product.
U/	Unsigned divide.
M	Signed multiplication leaving double product.
M/	Signed remainder and quotient from double dividend.
M/MOD	Unsigned divide leaving double quotient and remainder from double dividend and single divisor.
MAX	Maximum.
MIN	Minimum.
+-	Set sign.
D+-	Set sign of double-precision number.
ABS	Absolute value.
DABS	Absolute value of double-precision number.
NEGATE	Change sign.
DNEGATE	Change sign of double-precision number.
S->D	Sign extend to double-precision number.
1+	Increment value on top of stack by 1.
2+	Increment value on top of stack by 2.
1-	Decrement value on top of stack by 1.
2-	Decrement value on top of stack by 2.
AND	Logical AND (bitwise).
OR	Logical OR (bitwise).
XOR	Logical exclusive OR (bitwise).

AIM 65 FORTH WORDS (con't)

CONTROL STRUCTURES

DO . . . LOOP	Set up loop, given index range.
DO . . . +LOOP	Like DO . . . LOOP, but adds stack value to index.
I	Place current index value on stack.
LEAVE	Terminate loop at next LOOP or +LOOP.
BEGIN . . . UNTIL	Loop back to BEGIN until true at UNTIL.
BEGIN . . . WHILE . . . REPEAT	Loop while true at WHILE; REPEAT loops unconditionally to BEGIN.
BEGIN . . . AGAIN	Unconditional loop.
IF . . . THEN	If top of stack true, execute following clause THEN continue; otherwise continue at THEN.
IF . . . ELSE . . . THEN	If top of stack true, execute ELSE clause THEN continue; otherwise execute following clause, THEN continue.

INPUT-OUTPUT

CR	Carriage return.
SPACE	Type one space.
SPACES	Type n spaces.
." . . . . "	Print text string (terminated by ").
DUMP	Dump n2 words starting at address.
TYPE	Type string of n1 characters starting at address n2.
?TERMINAL	True if terminal break request present.
KEY	Read key, put ASCII value on stack.
EMIT	Output ASCII value from stack.
EXPECT	Read n1 characters from input to address n2.
WORD	Read one word from input stream, until delimiter.
IN	User variable contained within TIB.
HOLD	Waits for KEY.
BAUD	Set BAUD rate.
BL	Output a SPACE character.
C/L	Number of characters/line.
TIB	Pointer to terminal input buffer start address.
B/SCR	Number of blocks/editing screen.
QUERY	Input text from terminal.
ID.	Print <name> from name # field address (nfa).

MEMORY

@	Fetch value addressed by top of stack.
!	Store n1 at address n2.
C@	Fetch one byte only.
C!	Store one byte only.
?	Print contents of address.
+!	Add second number on stack to contents of address on top.
CMOVE	Move n3 bytes starting at address n1 to area starting at address n2.
FILL	Put byte n3 into n2 bytes starting at address n1.
ERASE	Fill n2 bytes in memory with zeroes, beginning at address n1.
BLANKS	Fill n2 bytes in memory with blanks, beginning at address n1.
TOGGLE	Mask memory with bit pattern.

OUTPUT FORMATTING

NUMBER	Convert string at address to double-precision number.
<#	Start output string.
#	Convert next digit of double-precision number and add character to output string.
#S	Convert all significant digits of double-precision number to output string.
SIGN	Insert sign of n into output string.
#>	Terminate output string (ready for TYPE).
HOLD	Insert ASCII character into output string.
HLD	Hold pointer, user variable.
-TRAILING	Suppress trailing blanks.
.LINE	Display line of text from mass storage.
COUNT	Change length of byte string to type form. Print number on top of stack.
.R	Print number n1 right justified n2 places.
D.	Print double-precision number n2 n1.
D.R.	Print double-precision number n2 n1 right justified n3 places.
DPL	Number of digits to the right of decimal point.

MONITOR & CASSETTE I/O

COLD	AIM 65 FORTH cold start.
MON	Exit to AIM 65 Monitor.
?TTY	Switch: true = TTY; false = KB.
CHAIN	Chain tape file.
CLOSE	Close tape file.
?IN	Set to active input device (AID).
?OUT	Set to active output device (AOD).
GET	Input a character from the AID.
PUT	Output a character to the AOD.
READ	Input n2 characters from AID to address n1.
WRITE	Output n2 characters to AOD at address n1.
SOURCE	Compile from the AID.
FINIS	Terminate compile from SOURCE.
-CR	Output CR to printer only.

VIRTUAL STORAGE

LOAD	Load mass storage screen (compile or execute).
BLOCK	Read mass storage block to memory address.
B/BUF	System constant giving mass storage block size in bytes.
BLK	System variable containing current block number.
SCR	System variable containing current screen number.
UPDATE	Mark last buffer accessed as updated.
FLUSH	Write all updated buffers to mass storage.
EMPTY-BUFFERS	Erase all buffers.
+BUF	Increment buffer address.
BUFFER	Fetch next memory buffer.
R/W	User read/write linkage.
USE	Variable containing address of next buffer.
FIRST	Leaves address of first block buffer.
OFFSET	User variable block offset to mass storage.
PREV	Variable containing address of latest buffer.

AIM 65 FORTH WORDS (con't)

MISCELLANEOUS AND SYSTEM

(<comment>)	Begin comment (terminate by right parentheses on same line).
IN	System variable containing offset into input buffer.
LIMIT	Top of memory.
QUIT	Clear return stack and return to terminal.

COMPILER-TEXT INTERPRETER

—>	Interpret next screen.
;S	Stop interpretation.
COMPILE	Compile following <name> into dictionary.
LITERAL	Compile a number into a literal.
DLITERAL	Compile a double-precision number into a literal.
EXECUTE	Execute the definition on top of stack.

DICTIONARY CONTROL

FORGET	FORGET all definitions from <name> on.
HERE	Returns address of next unused byte in the dictionary.
ALLOT	Leave a gap of n bytes in the dictionary.
TASK	A dictionary marker.
'	Find the address of <name> in the dictionary.
-FIND	Search dictionary for <name>.
DP	User variable containing the dictionary pointer.
C,	Store byte into dictionary.
,	Compile a number into the dictionary.
PAD	Pointer to temporary buffer.

DEFINING WORDS

: <name>	Begin colon definition of <name>.
;	End colon definition.
VARIABLE <name>	Create a variable named <name> when initial value n; returns address when executed.
CONSTANT <name>	Create a constant named <name> with value n; returns value when executed.
CODE <name>	Begin definition of assembly-language primitive operation named <name>.
;CODE	Used to create a new defining word, with execution-time "code routine" for this data type in assembly.
<BUILDS . . . DOES>	Used to create a new defining word, with execution-time routine for this data type in higher-level FORTH.
CREATE	Create a dictionary header.
USER	Create a user variable.

VOCABULARIES

CONTEXT	Returns address of pointer to CONTEXT vocabulary.
CURRENT	Returns address of pointer to CURRENT vocabulary.
FORTH	Main FORTH vocabulary.
ASSEMBLER	Assembler vocabulary.
VOCABULARY <name>	Create new vocabulary.
VLIST	Print names of all words in CONTEXT vocabulary.
VOC-LINK	Most recently defined vocabulary.

SECURITY

ABORT	Error; operation terminates.
ERROR	Execute error notification and restart system.
MESSAGE	Displays message.
WARNING	Pointer to message routine.
FENCE	Prevents forgetting below this point.
WIDTH	Controls significant characters of <name>.

PRIMITIVES

OBRANCH	Run-time conditional branch.
BRANCH	Run-time unconditional branch.
PUT	Stores registers and jumps to next.
ENCLOSE	Text scanning primitive used by WORD.
RO	Location of return Stack.
RP!	Initializes return Stack.
SO	Initial value of stack pointer.
SP!	Initialize stack pointer.
NEXT	The FORTH virtual machine.

Software Development is Fast and Easy With...

Rockwell

PL/65
A High-Level Language for the AIM 65 Advanced Interactive Microcomputer

AIM 65 MICRO-COMPUTER

- PL/65 Resembles PL/1 and Algol
- PL/65 ROMs Plug into AIM 65 Board
- Generates 6500 Assembly Language, for Post-Compilation Editing and Assembling
- Upward-Compatible With System 65 PL/65
- Has Control Structures for Conditional and Iterative Looping
- Drop Down to Assembly Language, For Optimal Coding Efficiency

In Rockwell's AIM 65, you have not only a low-cost, general-purpose microcomputer, but also the basis for a cost-efficient, low-end development system. By coupling AIM 65 with the advanced PL/65 Compiler option (Rockwell Part No. A65-030), you're even further ahead with valuable savings in time, effort and cost.

Resembling PL/1 and ALGOL in general form, PL/65 is designed to improve your productivity and efficiency by simplifying the overall software development effort.

The coding is easier, since PL/65's powerful, high level language statements enable you to implement even complex applications with minimal programming.

Program readability is enhanced by the self-documenting nature of PL/65. This results in programs that are easier to understand. These programs are easier to update, too, which means lower maintenance costs.

PL/65 = Software Simplification

All language features are aimed at improving productivity by simplifying software development. PL/65's structured programming support features encourage modular program design, and its general control structure for conditional and iterative looping allows the language to be applied to highly structured programs.

Coding Flexibility...When You Need It Most

PL/65 allows you to freely mix assembly language instructions in portions of the program where timing or code optimization requirements are critical.

This flexibility carries through the compile cycle: The PL/65 compiler outputs source code to AIM 65's optional assembler, rather than object code. You'll be able to enhance or debug at the assembler level and indeed to drop into assembly language whenever you desire. PL/65 thereby provides the structuring potential and programming simplicity of a high-level language, while retaining the power and flexibility of an assembler.

The PL/65 Package

PL/65 for AIM 65 (Part No. A65-030) comes on two pre-programmed 4K-byte ROMs, and is supplied with a comprehensive PL/65 User's Manual. It's available now from your local Rockwell Distributor. For the name of your nearest Distributor, call toll-free 800-854-8099 (within California, 800-422-4230).

For more information on PL/65, SYSTEM 65, AIM 65, or the rapidly growing family of R6500 products, contact

ROCKWELL INTERNATIONAL
P.O. Box 3669, RC55
Anaheim, CA 92803
Attn: Marketing Services, D/727

PL/65 Language Statements

Declaration

DECLARE
DEFINE
DATA

Assignment

Direct Single Byte Move
Indirect Single Byte Move
Direct Multiple Byte Move

Imperative

SHIFT
ROTATE
ASSEMBLY CODE
INC
INCW
DEC
DECW
STACK
UNSTACK

Looping

FOR-TO-BY
WHILE

Specification

ENTRY
EXIT
TFILE
DFILE

Conditional Execution

IF-THEN-ELSE

Branching

GOTO
CALL
RETURN
RTI
BREAK
HALT

Block

BEGIN
DO
END

Miscellaneous

Comment
Tab

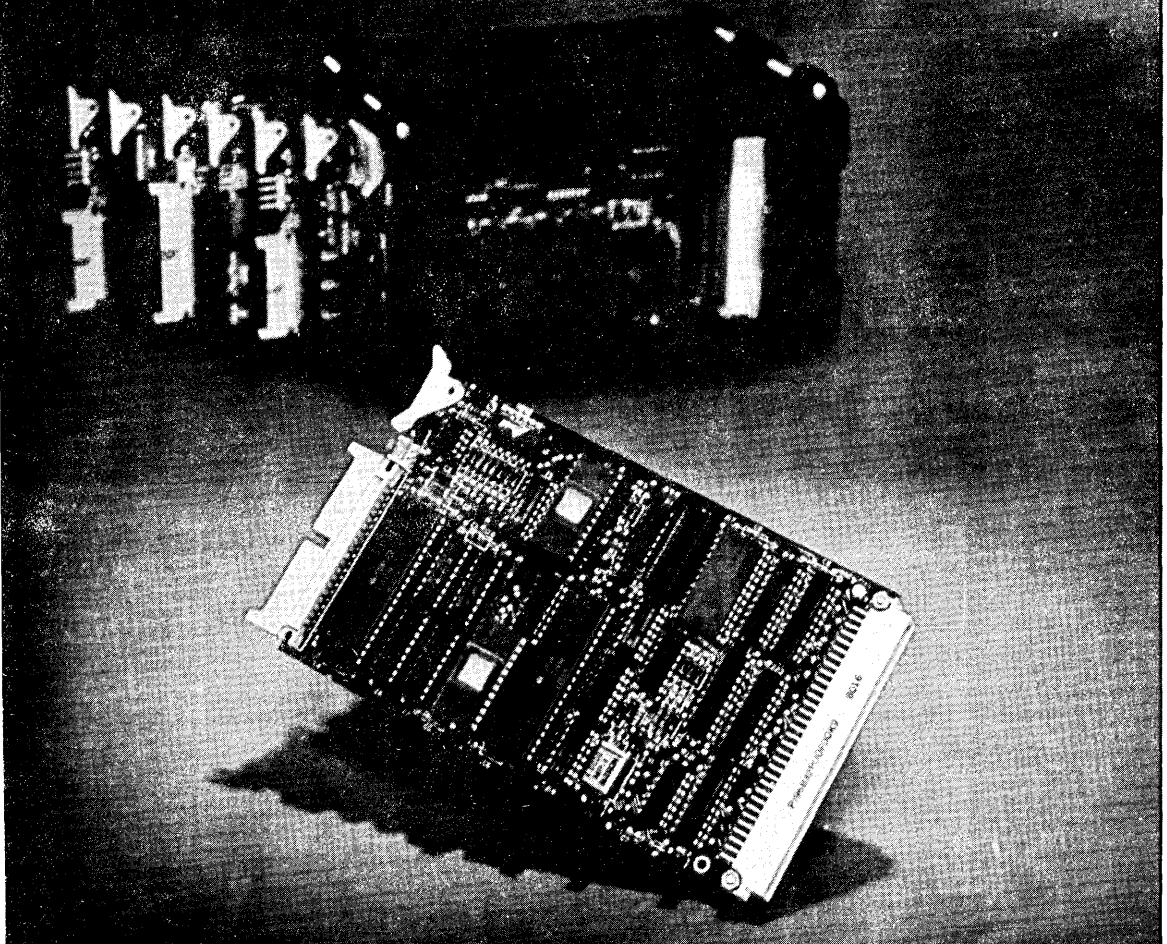
AIM 65
MICRO-
COMPUTER

RM65
BOARD
PRODUCTS

Rockwell RM 65

Modular Microcomputer

A family of compact size, board-level products.
Cut costs . . . increase productivity



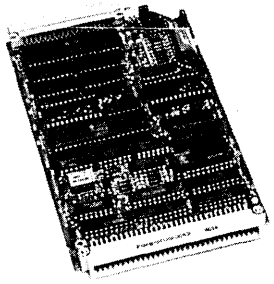
Rockwell International

where science gets down to business

Rockwell
International

RM 65 Modula

Standard size boards • Buy only what y
• Proven R6502 microprocessor



Single Board Compu

RM65-1000
The Single Board Computer is the
configurations. This single module inc
static RAM, 16K bytes PROM/ROM ca
8-bit parallel ports with handshake con
serial shift register. This module alone
makes a custom RM 65 microcompu

The Rockwell RM 65 microcomputer consists of hardware modules and software packages designed for OEM and end-user applications. The modules are compact functionally-oriented boards that provide state-of-the-art performance at off-the-shelf cost. The software packages include high level language interpreters and peripheral drivers.

The RM 65 microcomputer provides an "already complete" flexible design concept that allows you to build, and expand, a system exactly to your needs. By using standard hardware and software, you reduce engineering costs, shorten product introduction cycles, buy only what you need as you need it.

Modules

8K Static RAM Module
RM65-3108, RM65-3108N
Static RAM memory configurable as one 8192 byte block or as two 4096 byte blocks. On board switches select bank and address assignments. (RM65-3108N less RAM devices)

32K Dynamic RAM Module
RM65-3132, RM65-3132N
32,768 bytes of dynamic RAM, transparent refresh maintains performance. Bank selection in 16K blocks, address in 4K blocks, switch selectable. (RM65-3132N less RAM devices)

CRT Controller (CRTC) Module
RM65-5102
Provides an R6545 CRT device for timing and control. 2K bytes refresh RAM and 2K bytes ROM software. The module outputs HSYNC, VSYNC, and video signals as well as composite video. Provides alphanumeric and limited graphics characters.

IEEE-488 Bus Controller Module
RM65-7102
Implements standard general purpose interface bus, communicates with up to 15 peripherals. On-board ROM software implements talk, listen, and controller functions.

16K PROM/ROM Module
RM65-3216
Socketed to accept 2K, 4K or 8K 24-pin-devices up to a total of 16K bytes of memory. May be assigned to one of two memory banks, switch selectable in 4K byte sections.

Floppy Disk Controller (FDC) Module
RM65-5101
Controls up to four 8" single density or 5 ¼" single or double density disk drives, single or double sided. Software in on-board 4K ROM.

General Purpose Input/Output and Timer Module
RM65-5222
Total of 40 buffered I/O lines. Two R6522 devices provide four 8-bit parallel ports with hand-shake, four multi-mode 16-bit timers, two 8-bit shift registers.

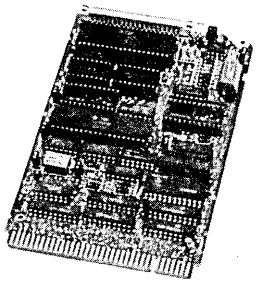
Asynchronous Communications Interface Adapter (ACIA) Module
RM65-5451
For RS232C serial interface. Two R6551 ACIA devices control two independent RS232C ports with programmable rates from 50 to 19,200 baud. 20ma TTY interface. Handshake for modems.

Modules

Microcomputer

eed, when you need it • Cut design costs
v cost AIM 65 development system

oint for all RM 65 microcomputer
opular R6502 CPU with 2K bytes of
d an R6522 VIA which provides two
ulti-mode 16-bit timers and an 8-bit
ne or more memory or I/O modules.



Features: 100mm × 160mm (3.9" × 6.3") RM 65 modules are size efficient with each providing a needed microcomputer function. There is no need for buying unwanted electronics. The boards are available with a high-reliability European DIN compatible 64-pin connector or a lower cost edge connector. Quality is built-in — all components are pre-tested and all finished assemblies are burned-in.

RM 65 microcomputer software packages are designed for incorporation into the application end-product. The intelligent peripheral controller modules include associated software; at the system level a BASIC language interpreter is provided. And, only Rockwell offers the AIM 65 as a low-cost complete development system, to support the design using RM 65 microcomputer products.

RM65 BOARD PRODUCTS

Software

Software drivers for peripheral I/O devices and higher level language interpreters make fitting the RM 65 microcomputer to your application both easy and flexible. You can interface directly with the software drivers or the programmable devices. You can turn your RM 65 microcomputer into a BASIC machine.

CRT Controller Software Package
CRT driver, screen generation and test subroutines.

FDC Software Package
Disk driver, file management and test subroutines.

IEEE-488 Software Package
Subroutines implement 1978 standards and module test.

BASIC Run Time Software Package
Directly compatible with AIM 65 BASIC, 8K byte ROM resident. Universally recognized as the most easily learned programming language.

Accessories

4-, 8-, and 16-Slot Card Cages
RM65-7004, RM65-7008, RM65-7016
Modules insert into card cage, edge or pin connector style mother boards, power supplies connect to screw-down terminals.

Single Card Adapter
RM65-7101
Attach a single RM 65 module to the AIM 65 microcomputer.

Adapter/Buffer Module
RM65-7104
Allows connection of multiple RM 65 modules to the AIM 65 microcomputer.

Cable Driver Adapter/Buffer
RM65-7116
Remotely locate RM 65 modules from AIM 65.

Design Prototyping Module
RM65-7201
Allows custom circuit fabrication. Power and return lines pre-routed through module. Plated-through hole pattern permits manual or automatic wire-wrap.

Extender Module
RM65-7211
Maintains electrical continuity with RM 65 bus while troubleshooting, extends any module outside the card cage.

Prototyping/Troubleshooting

AIM 65 Microcomputer
The low-cost AIM 65 microcomputer can be used as a complete development system for the RM 65 microcomputer. The AIM 65 functionally replaces the Single Board Computer for in-circuit evaluation of the RM 65 microcomputer system in the application. The PROM Programmer and CO-ED module, BASIC interpreter, PL/65 compiler and 2-pass assembler are all options.

SYSTEM 65 Development System
SYSTEM 65 offers the more traditional microprocessor development system. SYSTEM 65 comes with dual floppy disk drives, RS232C interface, parallel interface to printers, plus debug, text editor and two-pass assembler. Options include PL/65 compiler, BASIC interpreter, PROM programmer and User 65 module.

Development

PART NUMBER
RM65-1000(E)

Rockwell

RM 65
DATA SHEET

SINGLE BOARD COMPUTER (SBC) MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The Single Board Computer Module (SBC) allows users to design their products into compact modular stacks. The SBC module plugs into a single slot in an RM 65 card cage/motherboard and controls other memory and I/O modules. The heart of the SBC module is an R6502 CPU, which is capable of addressing 65K bytes of memory. In addition, the SBC module contains bank address logic which allows addressing of one or two 65K byte memory banks. Sockets on the module accept up to 16K bytes of PROM/ROM. 2K bytes of static RAM are also provided.

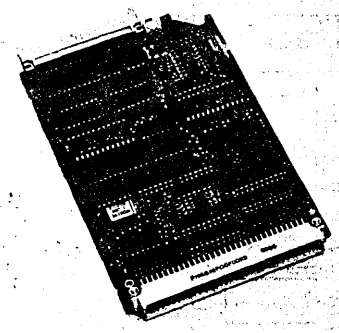
An R6522 Versatile Interface Adapter (VIA) provides two 8-bit parallel I/O data lines, two 2 bit control lines, two counter-timers and an 8-bit shift register. On-board switches assign memory sections to 4K byte blocks. All address, data and control lines are buffered.

FEATURES

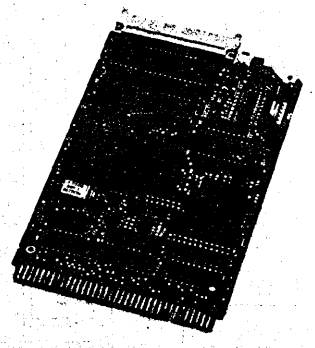
- Compact size – about 4" x 6½" (100 mm x 160 mm)
- Edge connector and Eurocard versions
- On-board R6502 CPU
- 2K of 2114 static RAM
- Two sockets for up to 16K PROM/ROM
- Supports the following PROM/ROM or equivalents
  - TI TMS 2516, TMS 2532 and Motorola MCM68764 PROMs
  - Rockwell R2316, R2332, or R2364 ROMs
- R6522 Versatile Interface Adapter (VIA) and I/O Interface
- Fully Buffered Address, Data, and Control lines for RM 65 Bus
- Separate switches allow RAM, PROM/ROM, and VIA to be individually dedicated to one or two 65K byte memory banks
- Jumpers allow selection of the following
  - 2K, 4K or 8K PROM/ROMs
  - RAM, PROM/ROM and I/O starting address to 4K byte boundary
  - On-board or External bank addressing source
  - Programmable DMA Terminate
  - On-board or external clock source
- +5V operation
- Fully assembled, tested and warranted

ORDERING INFORMATION

The SBC Module is available in an Edge Connector version (RM65-1000) and a Eurocard version (RM65-1000E).



Eurocard Version
RM65-1000E



Edge Connector Version
RM65-1000

SINGLE BOARD COMPUTER (SBC) MODULE

RM65 BOARD PRODUCTS

Specifications subject to change without notice
Document No. RMA65 N10
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

The Clock Circuit uses a crystal-controlled oscillator to provide a stable 1-MHz clock reference. A jumper selects between the internal clock reference or an external clock (to 1 MHz) as the source for the R6502 and the derived system clock.

The Reset Control circuit conditions the Reset signal to drive the R6502 Reset line. A reset can be generated by either the on-board reset pushbutton or an external switch. This circuitry also generates a reset automatically, upon power-up.

The R6502 Central Processing Unit (CPU) is the heart of the SBC Module and any interfacing Modules connected to the RM 65 Bus. The R6502 controls all program execution by means of the address, data, control, and timing lines. All internal R6502 operations are synchronized to the clock source.

The Bank Select Control circuit detects when the SBC Module's assigned memory bank is addressed, by comparing the Bank Address signal to the Bank Select Enable and Bank Select switches. The Bank Select Enable Switches allow all on-board PROM/ROM, RAM, & VIA to be independently assigned common to both Bank 0 (lower 65K) and Bank 1 (upper 65K) or dedicated to either Bank 0 or Bank 1, depending on the Bank Select switches. A jumper allows the Bank Address signal to be driven by the on-board R6522 VIA or from another module.

The Base Address Decoder uses the six most-significant address bits and the Base Address Jumpers to generate chip selects for the on-board PROM/ROM, RAM, and VIA. The RAM and VIA can be independently mapped into any 4K block of the selected 65K bank. The PROM/ROMs may be mapped into any 4K or 8K block of the selected bank.

The 16K PROM/ROM section has two sockets which can accept 2K, 4K or 8K PROM/ROM devices. The size and type of PROM or ROM is specified by the Base Address selection jumpers and the PROM/ROM type jumpers.

The 2K RAM section uses four 1K x 4 RAM devices to provide on-board read/write memory.

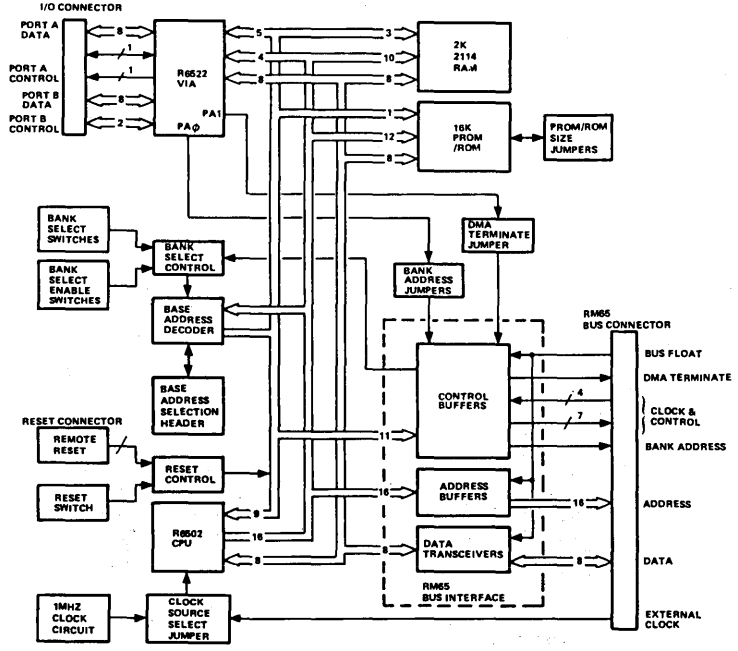
The R6522 Versatile Interface Adapter (VIA) provides input-output capability to the SBC Module. The VIA provides two 8-bit I/O ports each with two control lines. Both ports and control lines are brought out to a connector for user applications.

The SBC Module can control up to 15 additional support modules by means of the RM 65 Bus. There are three groups of signals on the RM 65 Bus: data, address, and control.

The Data Transceivers invert and transfer eight bits of parallel data between the SBC Module and the RM 65 bus. The direction of the transceivers is controlled by the read/write signal from the R6502. The transceivers are disabled when the on-board PROM/ROM RAM, or VIA is addressed or when the Bus Float signal from the RM 65 Bus is active.

The Address Buffers invert and transfer 16 parallel address bits from the SBC Module to the RM 65 bus.

The Control Buffers buffer all control and clock signals between the SBC Module and the RM 65 bus. The Non-Maskable Interrupt, Interrupt Request, Set Overflow, External Clock (Ø0), Ready and Bus Float input lines are buffered coming from the RM 65 bus into the SBC Module. The DMA Terminate, Reset and Phase 1 Clock (Ø1) output lines are always driven from the SBC Module onto the RM 65 Bus. The other six output lines for Read/Write, Phase 2 Clock, sync, and Bank Address are also buffered, but are tri-stated (disabled) when the Bus Float signal is active.



SBC Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5-Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	Buffered Sync
BSO	Buffered Set Overflow	14a	14c	BDRQ1/	*Buffered DMA Request 1
BRDY	Buffered Ready	15a	15c	GND	Ground
	* User Spare 1	16a	16c	-12V/-V	* -12 Vdc/-V
+12V/+V	* +12 Vdc/+V	17a	17c		* User Spare 2
GND	Ground Line	18a	18c	BFLT/	Buffered Bus Float
BDMT/	Buffered DMA Terminate	19a	19c	BØ0	Buffered External Phase 0 Clock
	* User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	*Buffered DMA Request 2
	* System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	* Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

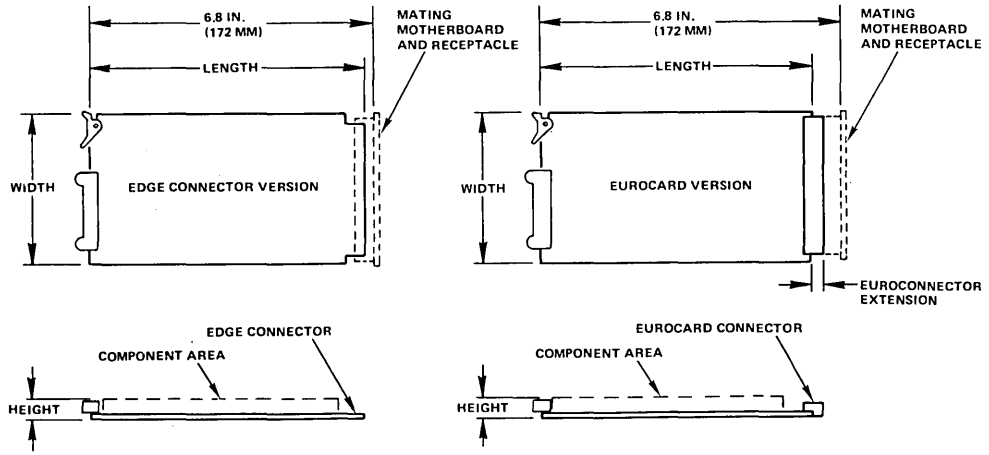
* Not used on this module.

SBC Module Physical and Electrical Characteristics

Characteristic	Value	
Physical characteristics (See Notes)	Edge Connector Version	Eurocard Version
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	5.3 oz. (150 g)	5.6 oz. (160 g)
Environment		
Operating Temperature	$0^{\circ}C$ to $70^{\circ}C$	
Storage Temperature	$-40^{\circ}C$ to $+85^{\circ}C$	
Relative Humidity	0% to 85% (without condensation)	
Power Requirements	+5 Vdc ±5%, 0.75 A (3.5 W) – Typical 1.2 A (6.0 W) – Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Connector Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row B not installed)	
I/O Connector	40-pin 3M mass termination (0.100 in. centers)	
RESET Switch Connector	2 vertical pins (0.3 in. high) on 0.200 in. center	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

PART NUMBER
RM65-5101(E)

Rockwell

RM 65
DATA SHEET

FLOPPY DISK CONTROLLER (FDC) MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The RM 65 Floppy Disk Controller (FDC) Module controls up to four standard (8") or mini- (5¼") floppy disk drives, single or double sided, soft sectored with either single density (FM) or double density (MFM) format. Software control of media density allows single or double density disks to be used in any connected drives.

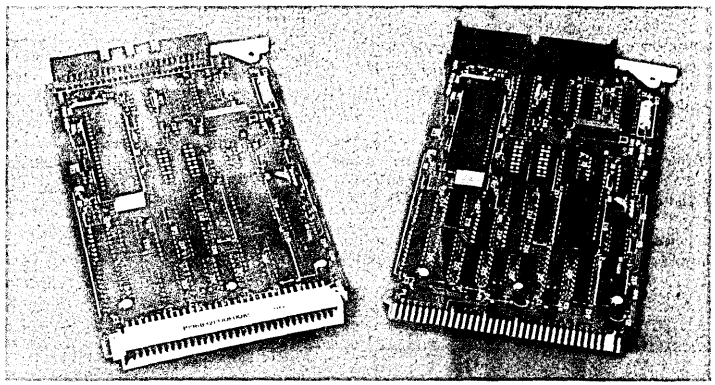
Two DIP headers configure the FDC to interface with either standard or mini-floppy disk drives. An on-board jumper selects single or double sided drives and a switch disables on-board ROM. The FDC directly interfaces to most popular drives with only switch and/or header changes. Bank Select and Bank Select Enable switches allow the FDC module to be dedicated to one of two 65K memory banks or assigned common to both banks. The FDC module I/O can be assigned to any page (256 bytes) using a standard PROM if the ROM is deselected.

FEATURES

- Compact size – about 4" x 6¼" (100 mm x 160 mm)
- Edge Connector and Eurocard versions
- RM 65 Bus compatible
- Buffered address, data and control lines
- Supports single or double sided, standard or mini-floppy disk drives
- Controls up to four disk drives
- Interfaces directly to Shugart SA-850 or SA-450 disk drives, with user options for other popular floppy disk drives
- Supports single-density IBM 3740 (FM) or double-density IBM System 34 (MFM) formats
- DMA data transfer capability
- Supports interrupt-driven or polled operation
- Bipolar PROM Base Address decoding
- Switches or jumpers for
  - Bank Selection to one or two banks
  - Double or Single sided operation
  - Select or deselect ROM
  - Module disable
- On-board header configures I/O for 8" or 5¼" drive interface
- On-board Program ROM containing disk utility and file management functions
- Fully assembled, tested and warranted.

ORDERING INFORMATION

The Floppy Disk Controller Module is available in an Edge Connector version (RM65-5101) and a Eurocard version (RM65-5101E).



Eurocard Version
RM65-5101E

Edge Connector Version
RM65-5101

Specifications subject to change without notice
Document No. RMA65 N15
March 1981

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bits of parallel data between the FDC module and the RM 65 bus, based on control signals from the Base Address Decoder and the Control Buffers. The read/write control line determines the direction, while the bus active enables the Data Transceivers.

The Address Buffers invert and transfer 12 of the 16 parallel address lines from the RM 65 bus to the Base Address Decoder, the Program ROM and the Floppy Disk Controller (FDC) device.

The Control Buffers invert and transfer phase 2 clock, reset, and read/write control signals from the RM 65 bus onto the module.

The Bank Select Control circuit detects when the module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch assigns the module to be active in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The Interrupt and DMA Control circuit enables operation in either an interrupt driven mode or under DMA control. Both Interrupt generation and DMA requests can be disabled under program control. The DMA request is jumper selectable for either of two DMA request lines connected to the RM 65 bus.

The Base Address Decoder, with the Base Address Select PROM, the Bank Select Control circuit, the ROM Disable switch, and the phase 2 and read/write signals control device selection on the module. The Base Address Select PROM compares the eight most significant address lines to the programmed addresses to generate device select signals to the Program ROM and the I/O devices. The ROM Disable switch assigns the module to be active either in a 256 byte page (disabled) or in a 4K byte block (enabled). A separate Module Disable switch allows the entire module to be disabled.

When the ROM is disabled, only the I/O devices are active, in the 256 byte page that matches all eight Base Address Select bits. For the I/O devices, the three least significant address lines, along with the phase 2 clock and read/write control signals, drive register select lines to the FDC device, and device select lines to the Drive Status Buffer and Drive Control Register.

When the ROM is enabled, the module is active in the 4K byte block that matches the four most significant Base Address select bits. The program ROM is selected except when the address matches the four least significant Base Address Select bits, in which case the I/O device select lines are selected.

The Controller Clock derives a reference frequency for the FDC device from a crystal controlled oscillator. The frequency is 1 MHz or 2 MHz, depending on the Drive Configuration Header position.

The FDC device, in conjunction with the Data Separator and Precompensation Circuitry, interfaces the RM 65 bus to the Floppy Disk medium. The circuitry supports 5¼" or 8", single or double sided disk drives, with choice of single or double density, soft sector formats. The FDC features powerful commands, including single or multiple record read/write with selectable record lengths. Write precompensation circuitry ensures reliable data recovery in double density formats. The Precompensation jumper selects precompensation on all tracks, only on tracks 44 and greater, or no precompensation at all.

The Drive Configuration header selects the I/O connector and FDC circuitry for either 5¼" mini-floppy or 8" standard floppy disk formats. The 50-pin I/O receptacle connects the FDC module to a mass terminated cable connected to the installed disk drives. A 34-pin cable and mating connector can be used to connect the 5¼" mini-floppy drives while a 50-pin cable and mating connector is needed to connect to the 8" floppy drives.

The Drive Status Buffer allows detection of the Drive Configuration header and Single/Double Sided Drive jumper positions, as well as selected density and side information.

The Drive Control Register provides control of the side and drive selection, motor on, head load, double density, and interrupt disable. The Active Side 0 Level jumper allows the use of various drives without modification.

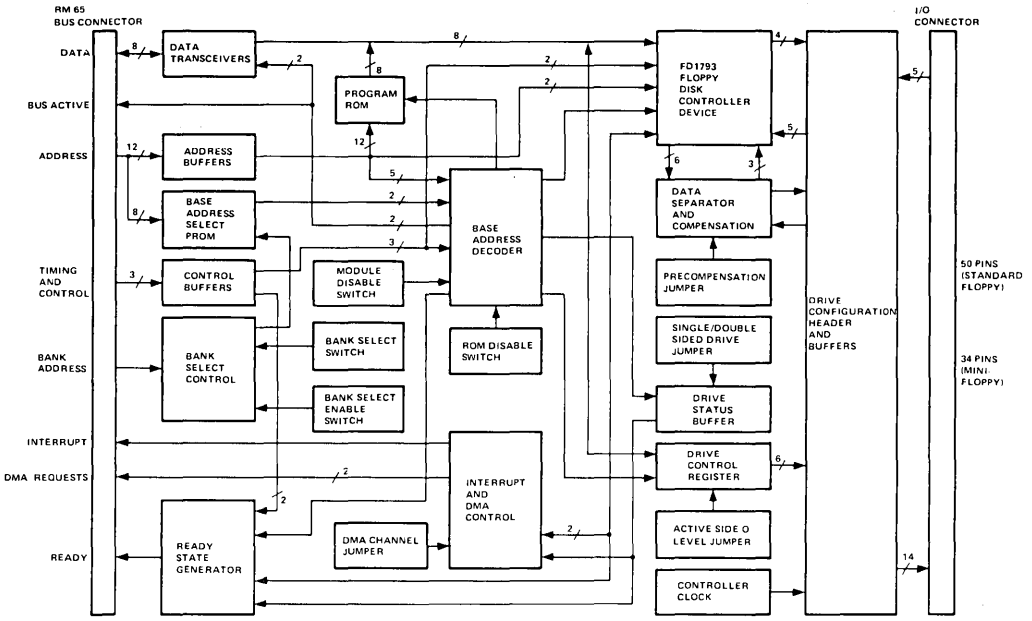
The Ready State Generator provides wait states as required by the FDC device.

The Program ROM contains the firmware to support operations with up to four disk drives (single or double side, single or double density), including:

Format a Disk
Read or Write a Sector
Seek or Verify Seek of a Track
Re-zero the Head
Read or Write Multiple Sectors
Read or Write a Track
Turn Motor On or Off
Select or De-select any Drive
Read I.D.
Reset

Included file management routines support up to 44 files on any disk side, independent of the disk size or density. These routines include:

Initialize or List a Directory
Create, Delete, or Rename a File Name
Open, Close, or Purge a File
Read from or Write to a File
Write a Modified Sector
Copy File
Copy Disk



Floppy Disk Controller Module Block Diagram

I/O Connector Pin Assignments

FDC Module I/O Connector Pin	Standard Floppy Disk Drive Interface Cable Connector		Mini-Floppy Disk Drive Interface Cable Connector (2)	
	Pin	Signal Name	Pin	Signal Name
2	2	Track >43 (Remex & MFE or equivalents)		
4	4	N.C.		
6	6	N.C.		
8	8	Track >43 (Caldisk or equivalents)		
10	10	N.C.		
12	12	N.C.		
14	14	2nd Side Select		
16	16	N.C.		
18	18	Head Load	2	N.C.
20	20	Index	4	N.C.
22	22	Drive Ready	6	Drive Select #4
24	24	N.C.	8	Index
26	26	Drive Select #1	10	Drive Select #1
28	28	Drive Select #2	12	Drive Select #2
30	30	Drive Select #3	14	Drive Select #3
32	32	Drive Select #4	16	Motor On
34	34	Direction In	18	Direction In
36	36	Step Pulse	20	Step Pulse
38	38	Write Data	22	Write Data
40	40	Write Gate	24	Write Gate
42	42	Track Zero	26	Track Zero
44	44	Write Protected	28	Write Protected
46	46	Read Data	30	Read Data
48	48	N.C.	32	2nd Side Select
50	50	N.C.	34	N.C.

NOTES:

1. All odd numbered pins are GND.
2. Pin 1 of the 34-pin mini-floppy disk drive interface cable connector should be keyed to pin 17 of the FDC module I/O connector.

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	* Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	* Buffered Sync
BSO	* Buffered Set Overflow	14a	14c	BDRQ1/	Buffered DMA Request 1
BRDY	Buffered Ready	15a	15c	GND	Ground
	* User Spare 1	16a	16c	-12V/-V	* -12 Vdc/-V
+12V/+V	+12 Vdc	17a	17c		* User Spare 2
GND	Ground Line	18a	18c	BFLT/	* Buffered Bus Float
BDMT/	* Buffered DMA Terminate	19a	19c	BØ0	* Buffered External Phase 0 Clock
	* User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	Buffered DMA Request 2
	* System Spare	22a	22c	BR/$\overline{W}$	* Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	*Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	*Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

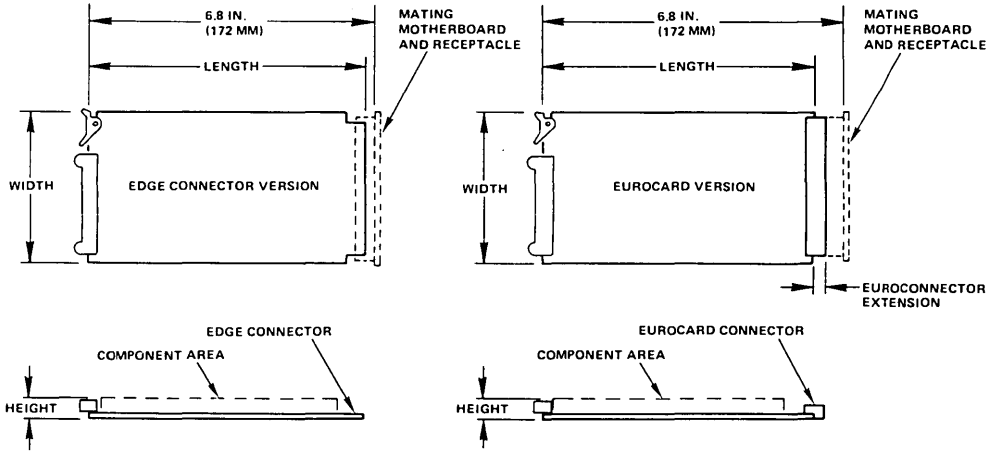
*Not used on this module

Floppy Disk Controller (FDC) Module Physical and Electrical Characteristics

Characteristic	Value	
Physical Characteristics (See Notes)	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	4.8 oz. (135 g)	5.2 oz. (145 g)
Environment		
Operating Temperature	$0^{\circ}C$ to $70^{\circ}C$	
Storage Temperature	$-40^{\circ}C$ to $+85^{\circ}C$	
Relative Humidity	0% to 85% (Without condensation)	
Power Requirements	+5 Vdc ±5% @ 600 mA – Typical 900 mA – Maximum	
	+12 Vdc ±5% @ 60 mA – Typical 100 mA – Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)	
I/O Interface	50-pin mass terminated connector (0.100 in. centers) Mates with I&B/Ansley Part No. 609-5001M or equivalent	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include the added extension due to the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

RM65
BOARD
PRODUCTS

PART NUMBER
RM65-5451(E)

Rockwell

RM 65
DATA SHEET

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA) MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

The ACIA Module is available in an Edge Connector version (RM65-5451) and a Eurocard version (RM65-5451E).

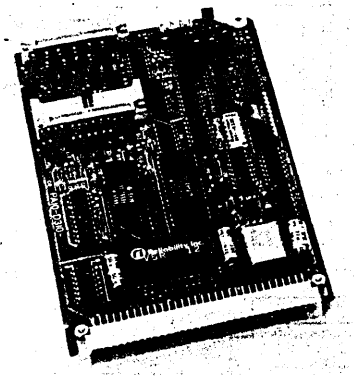
FEATURES

- Compact size – Approximately 4" x 6¼" (100 mm x 160 mm)
- Buffered address, data and control lines
- Two independent channels
- On-board 1.8432 MHz crystal frequency reference
- Programmable baud rate selection of 15 different rates (50, 75, 109.92, 134.58, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, or 19,200 bits per second)
- Programmable control of:
  - Word length (5, 6, 7 or 8 bits)
  - Number of stop bits (1, 1½, 2)
  - Parity (odd, even or none)
- Address select switch allows the starting address of the serial channel I/O to be assigned to a page boundary.
- On-board DC/DC Converter allows +5V only operation for RS-232 interface.

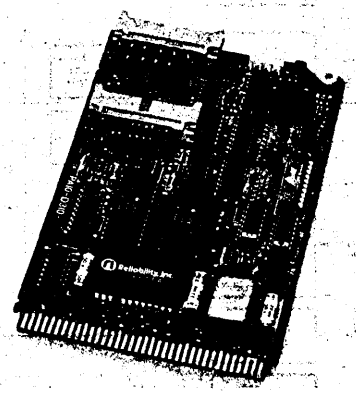
PRODUCT OVERVIEW

The Asynchronous Communications Interface Adapter (ACIA) Module interfaces two independent, asynchronous serial I/O channels to the RM 65 Bus. Each channel may operate as a data terminal or a data set, as selected by jumpers on the module. Both RS-232C and 20 ma TTY current loop interfaces are provided on Channel No. 1. An RS-232C interface is provided on Channel No. 2.

Each I/O channel performs serial-to-parallel and parallel-to-serial data conversons using an R6551 Asynchronous Communication Interface Adapter (ACIA). Both receiver and transmitter may operate with a programmable word length of 5, 6, 7, or 8 bits. Further, each channel can transmit and receive at 15 different program-selectable rates, between 50 and 19,200 baud. The receive rate is the same as the transmit rate.



Eurocard Version
RM65-5451E



Edge Connector Version
RM65-5451

Specifications subject to change without notice
Document No. RMA65 N08
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bits of parallel data between the R6551 ACIA devices and the RM 65 Bus depending on the state of the transceiver enable and read/write signals. During a write operation, the data received from the bus are written into the addressed ACIA device. During a read operation, the data read from the addressed ACIA device are driven onto the bus. When the ACIA module is not addressed, the transceivers are disabled.

The Address Buffers invert and transfer the three least significant address lines to the ACIA devices. Two lines generate the register address while one line selects one of the two ACIA devices.

The Control Buffers invert and drive the bank address, clock and read/write signals from the bus onto the module and drive the bus active and interrupt request lines onto the bus.

The ACIA module may be assigned to common banks (both Bank 0 and Bank 1) or to a dedicated bank (either Bank 0 or Bank 1), depending on the Bank Select and Bank Select Enable switch positions. The Bank Select Control circuit detects when the ACIA module is bank-addressed, by comparing the bank address control signal from the RM 65 Bus with the Bank Select switch position. If a match occurs and the Bank Select Enable switch is on, base address decoding is enabled.

The Base Address Buffer/Comparator buffers the eight most significant address lines from the bus and compares them to the Base Address Select switches. When a match occurs, the ACIA module is enabled.

Two R6551 ACIA devices convert data from serial-to-parallel format for input to the RM 65 Bus and from parallel-to-serial format for output from the bus. Each ACIA device contains a programmable control register to allow baud rate, word length and the number of stop bits to be programmed. A command register allows ACIA interrupt and parity modes to be specified under program control. A status register may be interrogated to determine the status of the data transfer and the cause for an interrupt request.

The RS-232 Interface circuit contains line receivers and line drivers, to convert signals from internal TTL levels to external RS-232C levels. Jumpers are provided to specify Data Set or Data Terminal operation. Jumpers are also provided to simulate RS-232 control signals that are not available from the interfacing equipment.

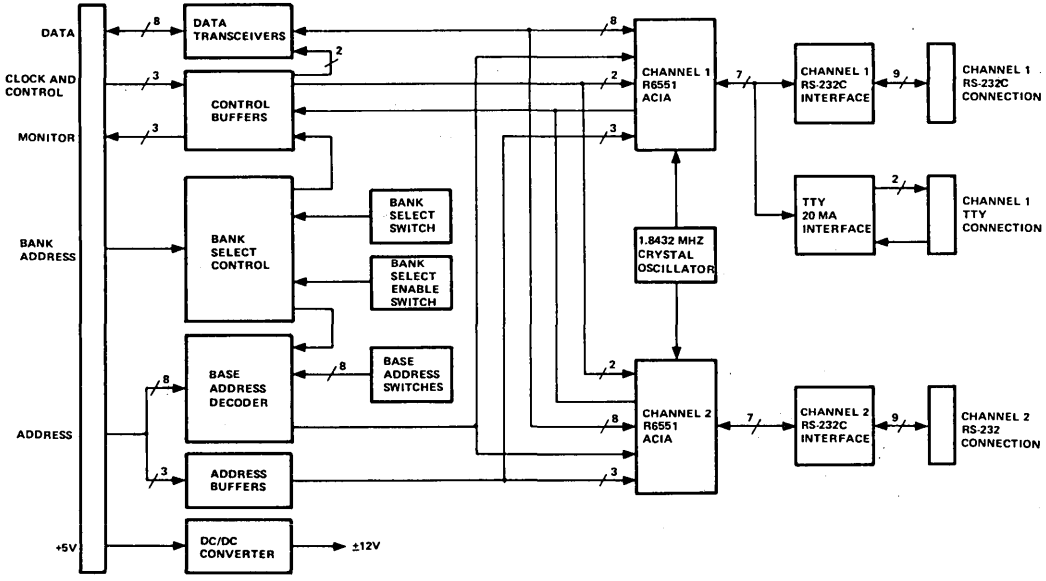
Opto-couplers in the TTY Interface circuit provide 20 ma current loop sourcing and sinking between the ACIA module and an external TTY.

A 1.8432 MHz crystal generates the data transmission frequency reference, which the ACIA devices convert to the desired baud rate under program control.

The DC/DC Converter generates ±12 Vdc from +5 Vdc for RS-232 operation.

Power Source for TTY Operation

For TTY operation, the ±12 Vdc must be obtained from the RM 65 Bus, by removing the DC/DC voltage converter and installing two jumpers.



ACIA Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
	Not Connected (See Note)		Wa	Wc		Not Connected (See Note)	
+5V	+5 Vdc Line (See Note)		Xa	Xc	+5V	+5 Vdc (See Note)	
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	I	2a	2c	BA15/	Buffered Address Bit 15	I
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	I
BA13/	Buffered Address Bit 13	I	4a	4c	BA12/	Buffered Address Bit 12	I
BA11/	Buffered Address Bit 11	I	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	I	6a	6c	BA9/	Buffered Address Bit 9	I
BA8/	Buffered Address Bit 8	I	7a	7c	BA7/	*Buffered Address Bit 7	
GND	Ground		8a	8c	BA6/	*Buffered Address Bit 6	
BA5/	*Buffered Address Bit 5		9a	9c	BA4/	*Buffered Address Bit 4	
BA3/	*Buffered Address Bit 3		10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	I	11a	11c	BA1/	Buffered Address Bit 1	I
BA0/	Buffered Address Bit 0	I	12a	12c	Bø1	*Buffered Phase 1 Clock	
GND	Ground		13a	13c	BSYNC	*Buffered Sync	
BSO	*Buffered Set Overflow		14a	14c	BDRQ1/	Buffered DMA Request 1	
BRDY	*Buffered Ready		15a	15c	GND	Ground	
	*User Spare 1		16a	16c	-12V/-V	-12 Vdc/-V	
+12V/+V	+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	*Buffered Bus Float	
BDMT/	*Buffered DMA Terminate		19a	19c	Bø0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/$\overline{W}$/	Buffered Read/Write "Not"	I	21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/$\overline{W}$	*Buffered Read/Write	
GND	Ground		23a	23c	BACT/	Buffered Bus Active	O
BIRQ/	Buffered Interrupt Request	O	24a	24c	BNMI/	*Buffered Non-Maskable Interrupt	
Bø2/	Buffered Phase 2 "Not" Clock	I	25a	25c	GND	Ground	
Bø2	*Buffered Phase 2 Clock		26a	26c	BRES/	Buffered Reset	I
BD7/	Buffered Data Bit 7	I/O	27a	27c	BD6/	Buffered Data Bit 6	I/O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	I/O
BD4/	Buffered Data Bit 4	I/O	29a	29c	BD3/	Buffered Data Bit 3	I/O
BD2/	Buffered Data Bit 2	I/O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	I/O	31a	31c	BD0/	Buffered Data Bit 0	I/O
+5V	+5 Vdc		32a	32c	GND	Ground	
+5V	+5 Vdc (See Note)		Ya	Yc	+5V	+5 Vdc (See Note)	
	Not Connected (See Note)		Za	Zc		Not Connected (See Note)	

NOTE
Pins Wa, Wc, Xa, Xc, Ya, Yc, Za, Zc are not used on the Eurocard version.
*Not used on this module.

I/O Connector J1 — TTY Interface

Pin	Signal Mnemonic	Signal Name	Input/Output
1	RTS	Request-To-Send	O
2	TD	Transmit Data	O
3	RD	Receive Data	I
4	-12V	-12 Vdc	

I/O Connector J2 and J3 — RS-232 Interface

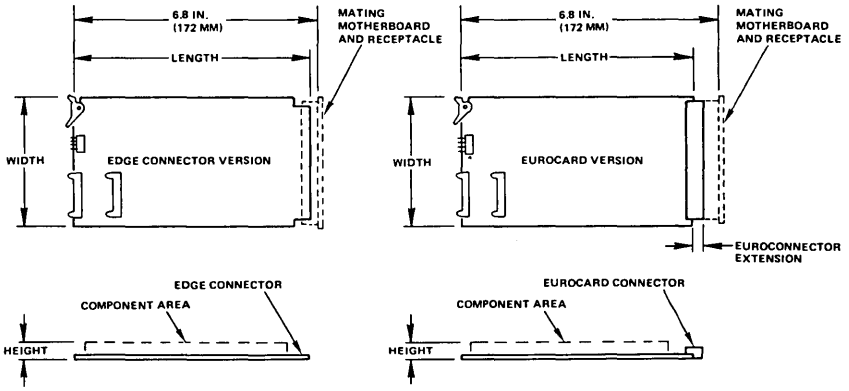
Pin	Signal Mnemonic	Signal Name	Input/Output	
			Data Set	Data Terminal
1	GND	Ground		
2	$\overline{TD}$	Transmit Data	I	O
3	$\overline{RD}$	Receive Data	O	I
4	RTS	Request-To-Send	I	O
5	CTS	Clear-To-Send	O	I
6	DSR	Data-Set-Ready	O	I
7	GND	Ground		
8	DCD	Data-Carrier-Detected	O	I
9-19		Not Used		
20	DTR	Data-Terminal-Ready	I	O
21-26		Not Used		

ACIA Module Physical and Electrical Characteristics

Characteristics	Value	
Physical Characteristics (See Notes):	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	4.9 oz. (135 g)	5.2 oz. (145 g)
Environment		
Operating Temperature	$0^{\circ}C$ to $70^{\circ}C$	
Storage Temperature	$-40^{\circ}C$ to $+85^{\circ}C$	
Relative Humidity	0% to 85%, without condensation	
Power Requirements		
RS-232 Interface Operation, with DC/DC Converter	+5 Vdc ±5% @ 0.4A (2.0W) – Typical 0.7A (3.5W) – Maximum	
TTY Operation, without DC/DC Converter	+5 Vdc ±5% @ 0.5A (2.5W) – Maximum +12 Vdc ±10% @ 0.12A (1.4W) – Maximum -12 Vdc ±10% @ 0.12A (1.4W) – Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in centers)	
Eurocard Version	64-pin plug (0.100 in centers) per DIN 41612 (Row b not installed)	
I/O Interface		
RS-232	26-pin mass termination connector (0.100 in centers)	
TTY	4-pin plug (0.156 in centers)	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.)
2. The length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

PART NUMBER
RM65-5222(E)

Rockwell

RM 65
DATA SHEET

GENERAL PURPOSE INPUT/OUTPUT & TIMER (GPIO & TIMER) MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The RM 65 GPIO & Timer Module provides a parallel I/O interface to the RM 65 Bus. Two R6522 Versatile Interface Adapter (VIA) devices provide four 8-bit bidirectional data ports and four 2-bit control ports; 40 I/O lines in all. Two multi-mode 16-bit timer/counters extend the versatility of the module. All I/O lines are TTL buffered.

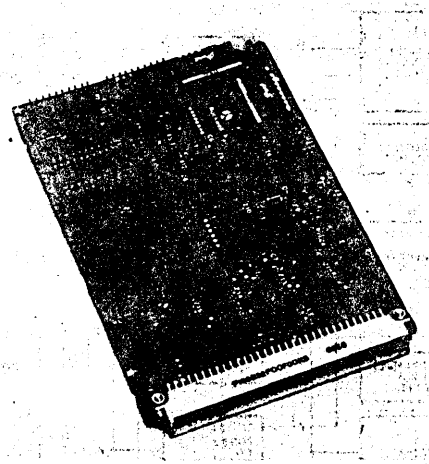
The GPIO & Timer Module I/O can be assigned either to one of two 65K byte memory banks or common to both banks. Eight switches allow I/O addresses to be set to any page (256 bytes). Eight switches (two per I/O port) manually set the I/O transceiver data direction or allow software control using the associated port control lines. Twelve jumpers specify the direction of the control lines.

ORDERING INFORMATION

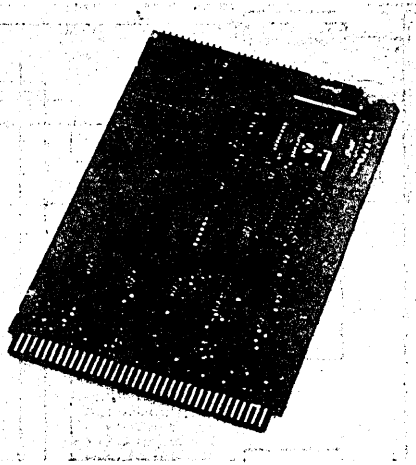
The GPIO & Timer Module is available in an Edge Connector version (RM65-5222) and a Eurocard version (RM-5222E).

FEATURES

- Compact size – about 4" x 6¼" (100 mm x 160 mm)
- Edge connector or Eurocard version
- RM 65 Bus compatible
- Fully buffered address, data and control bus interface lines
- Fully buffered data and control I/O lines
- Four 8-bit parallel bidirectional data ports
- Four 2-bit control ports
- Four programmable 16-bit counter/timers
- Two 8-bit shift registers for synchronous serial communications
- Manually or software-controlled data line direction
- Jumper-selectable control line direction
- Bank select switches assign I/O addresses to one or two 65K banks
- I/O base address switch selectable to a page boundary
- Four I/O connectors
- +5V operation
- Fully assembled, tested and warranted



Eurocard Version
RM65-5222E



Edge Connector Version
RM65-5222

Specifications subject to change without notice
Document No. RMA65 N12
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

The heart of the GPIO & Timer module is two R6522 Versatile Interface Adapter (VIA) devices. Each VIA provides two 8-bit bidirectional input/output ports, four I/O control lines, two fully programmable 16-bit timer/counters and an 8-bit shift register for serial interface. There is also control of interrupt generation from independent I/O conditions.

The two 8-bit input/output peripheral ports are fully bidirectional. Data direction registers allow each peripheral pin to independently act as either an input or an output. The four control lines can also be used for I/O or can provide handshaking for the associated data ports. Each control input can be programmed to interrupt the microprocessor on detection of a rising or falling edge.

The two 16-bit counter/timers are capable of many complex timing and counting functions. One timer provides four modes of operation: free running, with pulsed or toggled output, one-shot interval timer with a low-level output on a peripheral port line, or one-shot interval timer with a toggle output on a peripheral port line. The three modes of the second 16-bit timer provide a one-shot interval timer, a count of external pulses, or a clock for serial shift register. The shift register can shift in, or shift out, data at the system clock rate, the timer clock rate, or an external clock rate. Both timers and the shift register can be programmed to interrupt the microprocessor upon time-out or shift completion.

The Data Transceivers invert and buffer 8-bits of parallel data between the RM 65 Bus and the two R6522 VIA devices. The Data Transceivers are enabled when a valid address is present at the Base Address Decoders. During a read operation, data is transferred from the addressed R6522 to the RM 65 Bus. During a write operation, data is transferred from the RM 65 Bus to the addressed R6522.

The Address Buffers invert the five least significant address bits used to select the R6522 devices and registers.

The Bank Control circuit detects when the GPIO & Timer Module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 Bus to the Bank Select Enable and Bank Select switches. The Bank Select Enable switch allows the module to be assigned common to either both banks, or to Bank 0 (lower 65K) or Bank 1 (upper 65K) depending on the Bank Select switch.

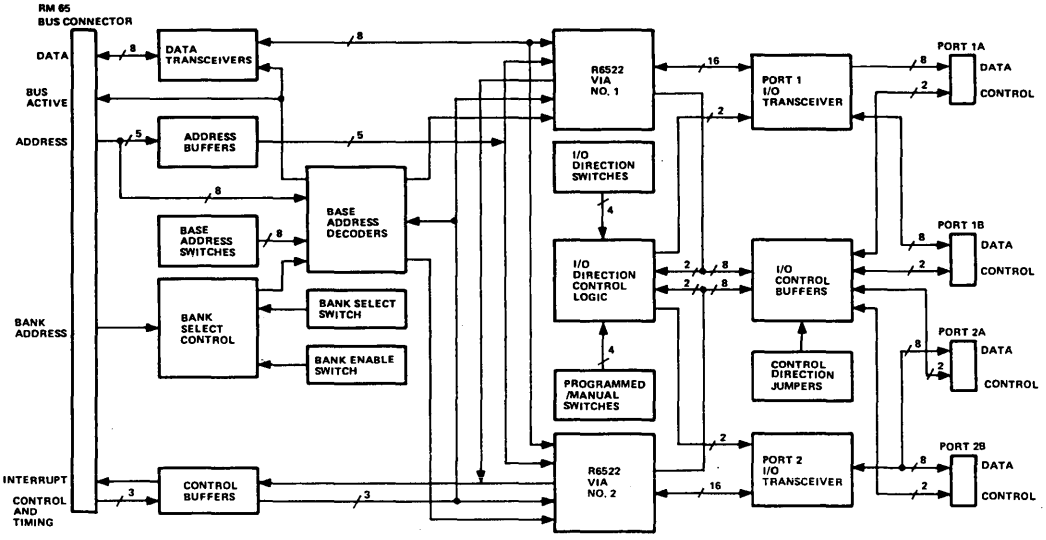
The Control Buffers drive read/write, phase 2 clock, and reset signals from the RM 65 Bus to the GPIO & Timer Module. The interrupt request and bus active signals are driven from the GPIO & Timer Module.

The Base Address Decoders use the eight most significant address lines to assign the 32 I/O addresses to a page (256 bytes) boundary. When an address is within range of the Base Address switches and the Bank Control is enabled, a chip select is generated to one of the R6522 devices.

Twelve Control Direction Jumpers allow the three bidirectional control lines (CA1, CB1, and CB2) on each R6522 to be configured for either input or output mode.

Four I/O Direction Switches provide direction control to each of the Port I/O transceivers. Four Programmed/Manual Select switches allow the direction control to be established from the Direction Control switches in the Manual mode or from a R6522 control line in the Programmed mode.

The I/O Transceivers buffer each of four 8-bit I/O ports. The direction is determined by the Direction Control logic. There are also eight buffers provided for the control lines (2 per I/O port), six of which can be configured for input or output as determined by the Handshake Direction Buffers.



GPIO & Timer Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	•Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	•Buffered Address Bit 6
BA5/	• Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	•Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	•Buffered Sync
BSO	•Buffered Set Overflow	14a	14c	BDRQ1/	*Buffered DMA Request 1
BRDY	•Buffered Ready	15a	15c	GND	Ground
	• User Spare 1	16a	16c	-12V/-V	•-12 Vdc/-V
+12V/+V	•+12 Vdc/+V	17a	17c		• User Spare 2
GND	Ground Line	18a	18c	BFLT/	•Buffered Bus Float
BDMT/	• Buffered DMA Terminate	19a	19c	BØ0	•Buffered External Phase 0 Clock
	• User Spare 3	20a	20c	GND	Ground
BR/W/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	*Buffered DMA Request 2
	• System Spare	22a	22c	BR/W	• Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	•Buffered Non-Maskable Interrupt
BØ2/	•Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

*Not used on this module.

All I/O data and control signals are brought out to four connectors that will each accept a 20-pin mass terminated ribbon cable (cable and mass terminated connectors are not supplied with the GPIO & Timer Module). Each connector is dedicated to one port with 8 data, 2 control and 10 ground lines.

I/O Connector Pin Assignments

PIN	SIGNAL
1	Port 1A Data 0
3	Port 1A Data 1
5	Port 1A Data 2
7	Port 1A Data 3
9	Port 1A Data 4
11	Port 1A Data 5
13	Port 1A Data 6
15	Port 1A Data 7
17	Port 1A Control CA1
19	Port 1A Control CA2

NOTES:

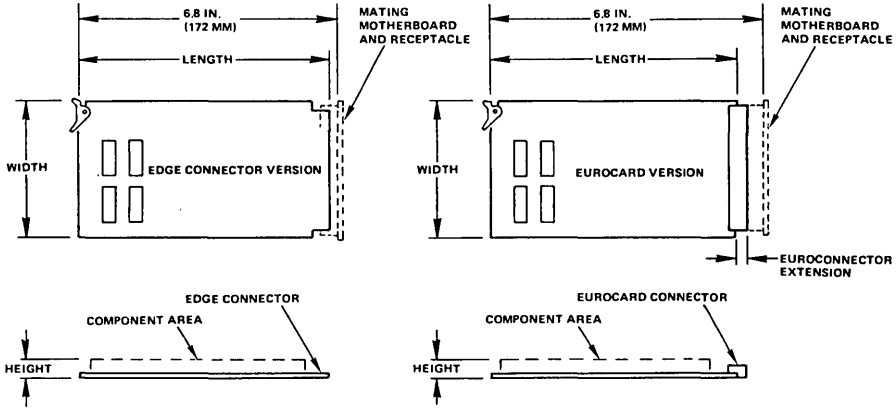
1. Similar for ports 1B, 2A and 2B
2. Even Pins 2-20 are ground

GPIO & Timer Module Physical and Electrical Characteristics

Characteristic	Value	
Physical characteristics (See Notes)	Edge Connector Version	Eurocard Version
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	4.6 oz (130 g)	5.0 oz (140 g)
Environment		
Operating Temperature	$0^{\circ}C$ to $70^{\circ}C$	
Storage Temperature	$-40^{\circ}C$ to $85^{\circ}C$	
Relative Humidity	0% to 85% (without condensation)	
Power Requirements	+5 Vdc ±5% 0.52 A (2.6 W) – Maximum +5 Vdc ±5% 0.94 A (4.70 W) – Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)	
I/O Interface		
I/O Connectors (4)	20-pin vertical mass termination plug (0.3 in. pins on 0.100 in. centers)	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. The Eurocard dimensions conform to DIN 41612.
4. The module dimensions are referenced to:



Module Dimensions

PART NUMBER
RM65-7102(E)

Rockwell

RM 65
DATA SHEET

IEEE-488 BUS INTERFACE MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The RM 65 IEEE-488 Bus Interface Module connects an AIM 65 or RM 65 SBC based system to the IEEE-488 General Purpose Interface Bus (GPIB). Complete controller, talker and listener functions, as defined in the IEEE-488, 1978 Standard, are implemented. The module also supports extended addressing and multiple bus controllers. On-board ROM firmware implements all 12 functions specified by the interface standard. Features not defined in the standard, but also supported, include manual talk or listen disable, dual primary addressing, and an external trigger line. Switches select the Device Talk/Listen Address, Enable Dual Primary Addressing Mode, Disable Talk, Disable Listen, and System Controller mode. The bus interface transceivers meet the electrical specifications of the IEEE-488 interface standard. An 8-inch ribbon cable mates the IEEE-488 module to the IEEE-488 bus with a standard 24-pin connector.

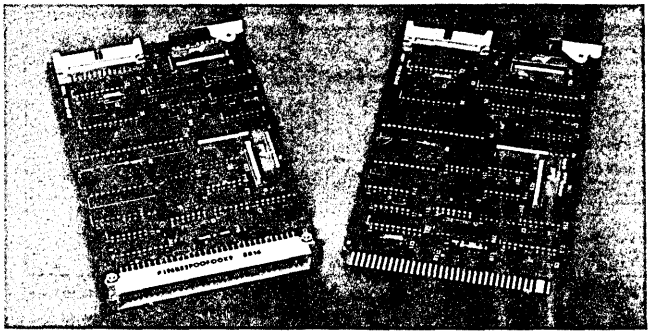
Standard RM 65 features include switches to dedicate the module to one of two 65K byte memory banks, or to assign it common to both banks. A jumper allows the on-board ROM to be enabled or disabled. Base address select switches allow the module I/O address to be assigned to any page (256 bytes) if the ROM is disabled.

ORDERING INFORMATION

The IEEE-488 Bus Interface Module is available in an Edge Connector version (RM65-7102) and a Eurocard version (RM65-7102E).

FEATURES

- Compact size — about 4" x 6½" (100 mm x 160 mm)
- Edge Connector and Eurocard versions
- RM 65 Bus compatible
- Buffered address, data and control lines
- Listen, talk, and controller functions
- IEEE-488, 1978 standard fully implemented
- Uses TI 9914 GPIB Adapter device
- On-board ROM contains bus protocol and utility firmware
- Switches for
  - Device Talk/Listen Address
  - Disable Talk
  - Disable Listen
  - Enable Dual Primary Addressing mode
  - System Controller
  - Base Address to page boundary for I/O
  - Bank Selection to one or both 65K banks
- Jumper for ROM enable/disable
- LEDs show current address register contents
- Supports DMA data transfers
- +5V operation
- Fully assembled, tested and warranted



Eurocard Version
RM65-7102E

Edge Connector Version
RM65-7102

IEEE-488 BUS INTERFACE MODULE

RM65 BOARD PRODUCTS

Specifications subject to change without notice
Document No. RMA65 N13
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bits of parallel data between the IEEE-488 Bus Interface Module and the RM 65 bus, based on data direction signals from the Base Address Decoder.

The Address Buffers invert and transfer the 16-bit parallel address lines from the RM 65 bus to the Base Address Decoders, to the R2332 ROM and to the GPIB Adapter.

The Control Buffers invert and transfer phase 2 clock, reset, and read/write control signals from the RM 65 bus onto the module. The interrupt request is buffered and driven onto the RM 65 bus.

The Bank Select Control circuit detects when the module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows the board to reside in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The DMA Control circuit allows DMA requests from the TI 9914 GPIB Adapter device to be driven on the RM 65 bus or disabled under program control. This line is jumper selectable for either of two DMA request lines on the RM 65 bus.

The Base Address Decoder compares the eight most significant address lines to the eight Base Address switches. The ROM Disable jumper allows the module to be active in a 4K block when enabled or active in a page (256 locations) when disabled. When an address for the selected bank matches the four most significant switches and the ROM is enabled, the Data Transceivers are enabled and the bus active signal is generated. When this address also matches the four least significant switches the GPIB Adapter and I/O are selected. When there is no match on the four least significant switches, the ROM is selected. When the GPIB Adapter and I/O are selected, the four least significant address lines, phase 2 clocks, and read/write control lines are used to derive register selects for the GPIB Adapter, device selects for the GPIB Status Latch, GPIB Sense Buffers, System Controller Select, and DMA Control Circuits. The read/write control lines also determine the direction for the Data Transceivers.

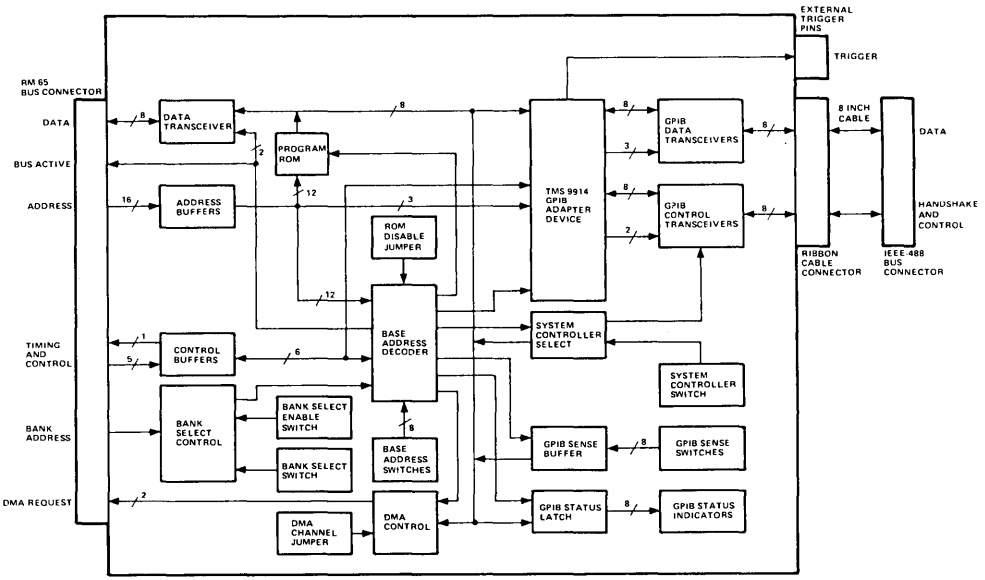
The TMS 9914 GPIB Adapter device provides hardware control of the IEEE-488 bus interface, using firmware subroutines provided in ROM. All bus interface lines are buffered by the GPIB Data and Control Transceivers, to conform to the electrical specifications of the IEEE-488 Standard. These lines are brought out through a cable to a standard IEEE-488 connector. An additional connector provides an external trigger output not defined by the IEEE-488 Standard.

The System Controller Select circuit allows manual selection of System Controller capabilities in multiple controller configurations.

The GPIB Sense Buffer allows the GPIB Sense Switches to be read for Device Talk/Listen Address, Talk or Listen Disable, and Dual Primary Address Mode selection. The GPIB Status Latch latches the positions of the GPIB Sense Switches and displays them on the GPIB Status Indicators. This allows a visual verification of the Device Talk/Listen Address and Operating modes.

On-Board Program ROM Firmware

The Program ROM firmware completely supports all 12 Bus functions described in the IEEE-488, 1978 Standard, as well as features of the TMS 9914 GPIB Adapter device not defined in the Standard. These utility functions make both the Bus protocol and the GPIB Adapter device transparent to the programmer. The firmware, organized as subroutines, is linked to the user program through a jump table. Many of these routines are interrupt-driven, to minimize the processor time in servicing the module. User-alterable vectors and parameters are located in RAM, to allow custom applications. Output data or commands for the Bus are handled as tables, easing the set-up and transfer of information. Extensive error checking by the utility subroutines allow resident or user-provided error handling routines to ensure proper operation of the module, the IEEE-488 Bus and status of data transfer. Two self-test routines verify proper module operation.



IEEE-488 Bus Interface Module Block Diagram

External Trigger Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output
1	TRIG	Trigger Out	O
2	GND	Ground	

IEEE-488 Bus Interface Connector Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/ Output	Pin	Signal Mnemonic	Signal Name	Input/ Output
1	DI01	Data Input/Output 1	I/O	13	DI05	Data Input/Output 5	I/O
2	DI02	Data Input/Output 2	I/O	14	DI06	Data Input/Output 6	I/O
3	DI03	Data Input/Output 3	I/O	15	DI07	Data Input/Output 7	I/O
4	DI04	Data Input/Output 4	I/O	16	DI08	Data Input/Output 8	I/O
5	EOI	End or Identify	I/O	17	REN	Remote Enable	I/O
6	DAV	Data Available	I/O	18	GND	Ground	N/A
7	NRFD	Not Ready for Data	I/O	19	GND	Ground	N/A
8	NDAC	Not Data Accepted	I/O	20	GND	Ground	N/A
9	IFC	Interface Clear	I/O	21	GND	Ground	N/A
10	SRQ	Service Request	I/O	22	GND	Ground	N/A
11	ATN	Attention	I/O	23	GND	Ground	N/A
12	SHIELD	Ground	N/A	24	GND	Logic Ground	N/A

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	• Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	• Buffered Sync
BSO	• Buffered Set Overflow	14a	14c	BDRQ1/	Buffered DMA Request 1
BRDY	• Buffered Ready	15a	15c	GND	Ground
	• User Spare 1	16a	16c	-12V/-V	• -12 Vdc/-V
+12V/+V	• +12 Vdc/+V	17a	17c		• User Spare 2
GND	Ground	18a	18c	BFLT/	• Buffered Bus Float
BDMT/	• Buffered DMA Terminate	19a	19c	BØ0	• Buffered External Phase 0 Clock
	• User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	Buffered DMA Request 2
	• System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	• Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

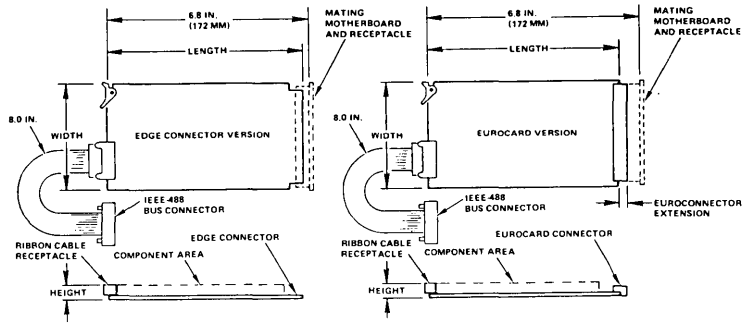
* Not used on this module.

IEEE-488 Bus Interface Module Physical and Electrical Characteristics

Characteristic	Value	
Physical Characteristics (See Notes)	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	4.6 oz. (130 g)	5.0 oz. (140 g)
Environment		
Operating Temperature	$0^{\circ}C$ to $70^{\circ}C$	
Storage Temperature	$-40^{\circ}C$ to $+85^{\circ}C$	
Relative Humidity	0% to 85% (without condensation)	
Power Requirements	+5 Vdc ±5% @ 0.65A (3.25W) -- Typical 1.0A (5.25 W) -- Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)	
Module I/O Interface		
Cable Receptacle	26-pin mass terminated (0.100 in. centers)	
Trigger Connector	Two vertical wire wrap pins (0.3 in. high on 0.200 in. centers)	
IEEE-488 Bus Interface Cable		
IEEE-488 Bus Connector	24-pin mass terminated (2.16 mm centers) with metric thread lock screws (Amphenol 57 or equivalent)	
Module Connector	26-pin mass terminated (0.100 in. centers)	
Cable Length	8 inches	
Type	Flat ribbon	
Number of Conductors	24	
Wire Size	#28 AWG	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include the added extension due to the module ejector
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

PART NUMBER
RM65-3108(E)

Rockwell

RM 65
DATA SHEET

8K STATIC RAM MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

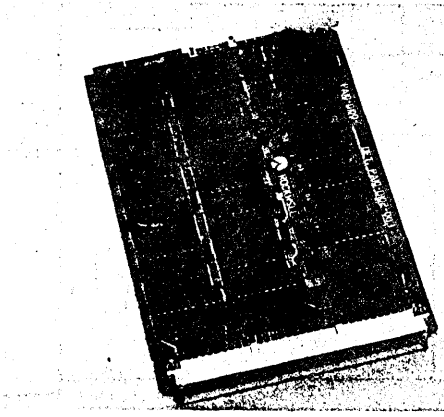
The 8K Static RAM Module is available in an Edge Connector version (RM65-3108) and a Eurocard version (RM65-3108E). These modules may also be ordered without the RAM devices installed, as part numbers RM65-3108N and RM65-3108NE, respectively.

FEATURES

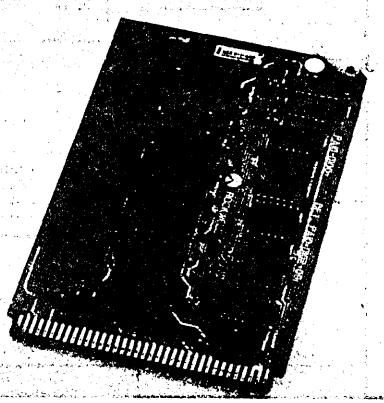
- Compact size – about 4" x 6¼" (100 mm x 160 mm)
- Edge Connector and Eurocard versions
- RM 65 Bus compatible
- Buffered address, data and control lines
- Two separately addressable 4K byte sections
- 16 socketed 2114 static RAM devices
- Write-protect switch for each memory section
- Bank Select and Enable switches
- +5V operation
- Fully assembled, tested and warranted.

PRODUCT OVERVIEW

The RM 65 8K Static RAM Module contains 8192 8-bit bytes of Random Access Memory (RAM), in sixteen 2114 static RAM devices. The memory is arranged as two separately addressable 4K memory sections. The starting address of each 4K section is selectable by on-board address switches. A Bank Select switch allows the RAM module to be assigned to one of two 64K memory banks.



Eurocard Version
RM65-3108E



Edge Connector Version
RM65-3108

RM65 BOARD PRODUCTS

8K STATIC RAM MODULE

Specifications subject to change without notice
Document No. RMA65 N01
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

8K bytes of static 2114 RAM are divided into two separately addressable 4K blocks. Two devices per 1K bytes are required since each device is 1K x 4 bits.

The Data Transceivers invert and transfer 8-bits of parallel data between the RAM devices and the RM 65 Bus, based on data direction signals from the Data Transceiver Control Circuit.

The Address Buffers invert and transfer 16 address bits from the RM 65 Bus to the RAM devices, to the Base Address Decoders and to the Chip Select Decoder.

The Control Buffers invert and transfer phase 2 clock and read/write control signals from the RM 65 Bus onto the RAM module, and drive the bus active signal onto the RM 65 Bus.

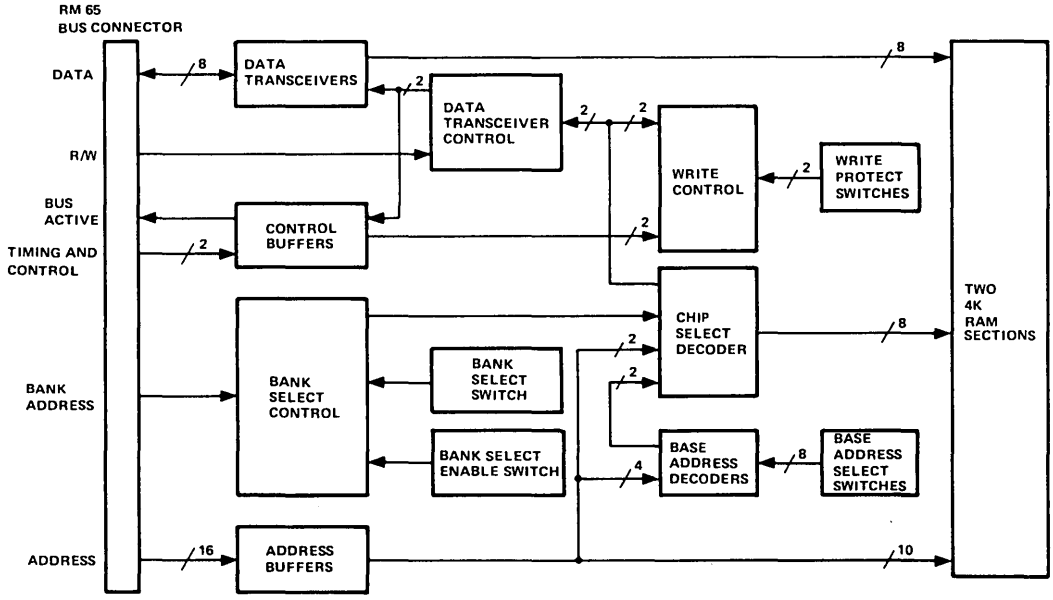
The Bank Select Controller detects when the RAM module's assigned memory bank is addressed, by comparing the bank address signal from the RM 65 Bus to the settings of the Bank Select and Bank Select Enable switches. If the addressed bank is the same as the selected memory bank, an enable signal is sent to the Chip Select Decoder.

Two Base Address Decoders detect when either 4K RAM Section (1 or 2) is addressed, by comparing the address lines to Base Address Select switch settings. When a match occurs, an enable signal is sent to the Chip Select Decoder.

The Chip Select Decoder uses outputs from the Bank Select Control circuit, the Base Address Decoders, and the PROM/ROM size jumpers as well as address lines A11 and A10 to generate one of eight chip select lines to the RAM devices. A signal indicating that a chip select line is active is also sent to the Write Control and Data Transceiver Control circuits.

The Write Control circuit generates the write enable signals to the RAM devices and to the Data Transceiver Control circuit. If the corresponding write protect switch is off, the write enable signal is activated. If the Write Protect switch is on, the Data Transceivers are disabled.

The Data Transceiver Control circuit determines whether a valid read or write operation is in progress, and provides transceiver enable and data direction signals to the Data Transceivers. The Data Transceivers are enabled if both the bank address and the address lines correspond to the selected bank and a selected base address, respectively.



8K Static RAM Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
	Not Connected (See Note)		Wa	Wc		Not Connected (See Note)	
+5V	+5 Vdc Line (See Note)		Xa	Xc	+5V	+5 Vdc (See Note)	
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	I	2a	2c	BA15/	Buffered Address Bit 15	I
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	I
BA13/	Buffered Address Bit 13	I	4a	4c	BA12/	Buffered Address Bit 12	I
BA11/	Buffered Address Bit 11	I	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	I	6a	6c	BA9/	Buffered Address Bit 9	I
BA8/	Buffered Address Bit 8	I	7a	7c	BA7/	Buffered Address Bit 7	I
GND	Ground		8a	8c	BA6/	Buffered Address Bit 6	I
BA5/	Buffered Address Bit 5	I	9a	9c	BA4/	Buffered Address Bit 4	I
BA3/	Buffered Address Bit 3	I	10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	I	11a	11c	BA1/	Buffered Address Bit 1	I
BA0/	Buffered Address Bit 0	I	12a	12c	BØ1	*Buffered Phase 1 Clock	
GND	Ground		13a	13c	BSYNC	*Buffered Sync	
BSO	*Buffered Set Overflow		14a	14c	BDRQ1/	*Buffered DMA Request 1	
BRDY	*Buffered Ready		15a	15c	GND	Ground	
	*User Spare 1		16a	16c	-12V/-V	*-12 Vdc/-V	
+12V/+V	*+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	*Buffered Bus Float	
BDMT/	*Buffered DMA Terminate		19a	19c	BØ0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/$\overline{W}$/	Buffered Read/Write "Not"	I	21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/$\overline{W}$	Buffered Read/Write	I
GND	Ground		23a	23c	BACT/	Buffered Bus Active	O
BIRQ/	*Buffered Interrupt Request		24a	24c	BNMI/	*Buffered Non-Maskable Interrupt	
BØ2/	Buffered Phase 2 "Not" Clock	I	25a	25c	GND	Ground	
BØ2	*Buffered Phase 2 Clock		26a	26c	BRES/	*Buffered Reset	
BD7/	Buffered Data Bit 7	I/O	27a	27c	BD6/	Buffered Data Bit 6	I/O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	I/O
BD4/	Buffered Data Bit 4	I/O	29a	29c	BD3/	Buffered Data Bit 3	I/O
BD2/	Buffered Data Bit 2	I/O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	I/O	31a	31c	BD0/	Buffered Data Bit 0	I/O
+5V	+5 Vdc		32a	32c	GND	Ground	
+5V	+5 Vdc (See Note)		Ya	Yc	+5V	+5 Vdc (See Note)	
	Not Connected (See Note)		Za	Zc		Not Connected (See Note)	

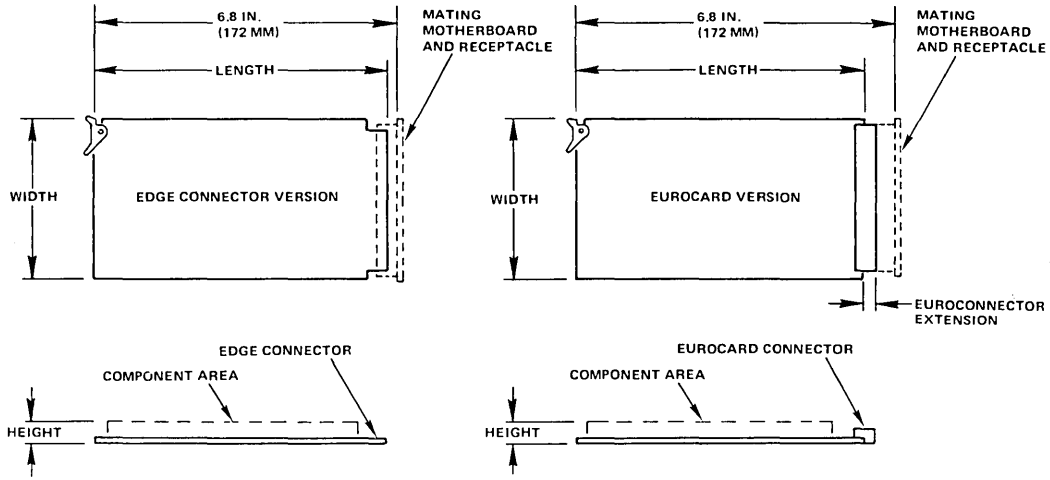
NOTE
Pins Wa, Wc, Xa, Xc, Ya, Yc, Za, Zc are not used on the Eurocard version.
*Not used on this module.

8K Static RAM Module Physical and Electrical Characteristics

Characteristic	Value	
Physical Characteristics (See Notes)		
	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	4.9 oz. (135 g)	5.3 oz. (145 g)
Environment		
Operating Temperature	$0^{o}C$ to $70^{o}C$	
Storage Temperature	$-40^{o}C$ to $+85^{o}C$	
Relative Humidity	0% to 85% (Without condensation)	
Power Requirements	+5 Vdc ±5% @ 1.0A (5.0W) – Typical 1.9A (9.5W) – Maximum	
Access Time	450 ns – Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in centers)	
Eurocard Version	64-pin plug (0.100 in centers) per DIN 41612 (Row b not installed)	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include the added extension due to the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

PART NUMBER
RM65-3132(E)

Rockwell

RM 65
DATA SHEET

32K DYNAMIC RAM MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The 32K Dynamic RAM module provides 32K bytes of read/write memory using 16 16K bit x 1 dynamic RAM (DRAM) devices. Two bank select switches allow the board to be dedicated to either one of two 65K Banks, or to be assigned common to both banks. A 24-pin DIP header allows each of the eight 4K sections to be independently mapped into any 4K block of the selected 65K bank. The independent addressing of blocks provides flexibility with system memory maps. An on-board switch allows the entire board to be write-protected.

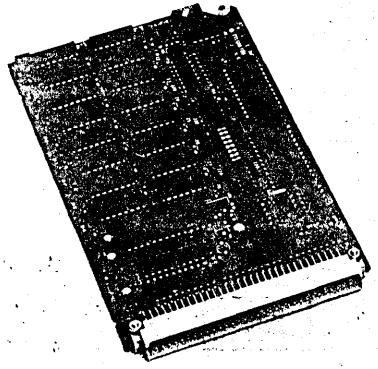
All refreshing of the dynamic RAM chips is automatic and completely transparent to the RM 65 Bus, thus providing low power performance at no loss of bus speed.

FEATURES

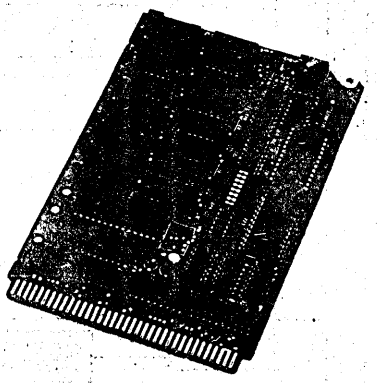
- Compact size — about 4" x 6¼" (100 mm x 160 mm)
- Edge connector or Eurocard Versions
- RM 65 bus compatible
- Buffered data, address, and control lines
- Internal Refresh controller is completely transparent to the Microflex 65 bus
- On-board switch allows write protection
- Base Address Header allows each 4K memory section to be assigned to any 4K block as a selected bank
- Bank select switches allow the entire board to be mapped into either or both 65K banks
- On-board DC-DC converter for -5 volt power supply
- Requires +5 and +12 volt power from the RM 65 bus
- Fully assembled, tested, and warranted

ORDERING INFORMATION

The 32K Dynamic RAM is available in an Edge Connector version (RM65-3132) and a Eurocard version (RM65-3132E). These modules may also be ordered without the RAM devices installed, as part numbers RM65-3132N and RM65-3132NE, respectively.



Eurocard Version
RM65-3132E



Edge Connector Version
RM65-3132

Specifications subject to change without notice
Document No. RMA65 N11
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bit parallel data between the selected DRAMs to the RM 65 bus. During a read operation, data from the DRAMs are latched and driven by the transceivers onto the RM 65 bus. During a write operation, data from the RM 65 bus drives the DRAMs. The transceivers are disabled when the module is not addressed.

The Address Buffers invert and transfer 16-bit parallel address lines from the RM 65 bus into the DRAM module.

The Bank Select Control circuit detects when the DRAM module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows the board to reside in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The Control Buffers buffer the control and timing signals used from the RM 65 bus.

The DRAM devices require 3 voltages. Two of these (+5 and +12 volts) are available directly from the RM 65 bus. The third voltage (-5 volts) is generated on board with a DC/DC converter.

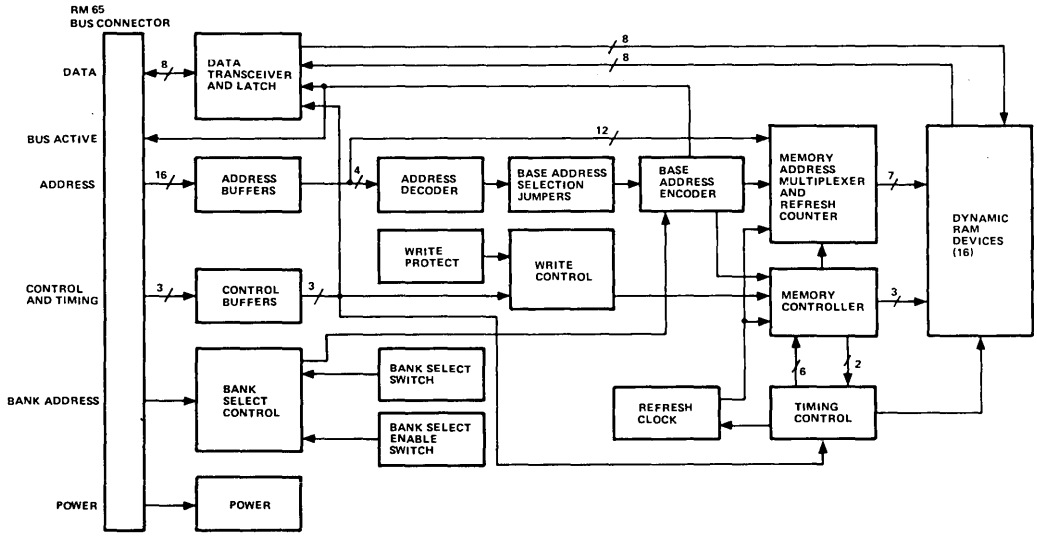
The Address Decoder uses the four MSB address lines to decode and enable one of 16 lines, each of which correspond to 4K blocks. The Base Address Selection Jumpers are placed in a 28 pin socket which consists of 16 lines from the Address Decoder, four lines from +5 volts, and 8 lines to the Base Address Encoder. The Base Address Selection is made by connecting each of the eight encoder inputs to any one of the 16 decoder outputs or to +5 volts. This allows each 4K block to be addressed anywhere in the selected 65K memory bank or disabled. The Base Address Encoder produces a 3 bit code for the enabled line and an additional signal for any line active (Board Select). The 3 bit code from the encoder becomes the 3 MSB address bits for the Memory Address Multiplexer. The Board Select line and a valid Bank Select signal are used to enable the Memory Controller and Data Transceivers, as well as create a Data Bus Active Signal.

The Write Control logic uses the Write Protect switch and the Read/Write line to enable writing into the DRAMs. If the Write Protect switch is off, the Read/Write signal is transferred directly to the Memory Controller. If the Write Protect switch is on, the Memory Controller forces a read operation so that the contents of the DRAMs will not be altered.

The Timing Control generates all the clocks required by the Memory Controller, Memory Address Multiplexer, and the Refresh Clock. The Refresh Clock generates a refresh cycle for every seven RM 65 clock cycles.

The Memory Controller uses the clocks derived in the timing control to sequence the signals to the DRAM devices. During normal read or write cycles, the Memory Controller allows Row Address, then Column Address information to be applied to the addressed DRAMs and generates the read/write signal. When a refresh is required, the timing is controlled so that the refresh is transparent to the RM 65 bus.

The Memory Address Multiplexer and Refresh Counter multiplexes Row, Column, or Refresh Addresses onto the DRAM address lines in response to the Memory Controller. There is also a Refresh Counter which is incremented by the Refresh Clock.



32K Dynamic RAM Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	* Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	* Buffered Sync
BSO	* Buffered Set Overflow	14a	14c	BDRQ1/	*Buffered DMA Request 1
BRDY	* Buffered Ready	15a	15c	GND	Ground
	* User Spare 1	16a	16c	-12V/-V	* -12 Vdc/-V
+12V/+V	+12 Vdc/+V	17a	17c		* User Spare 2
GND	Ground Line	18a	18c	BFLT/	* Buffered Bus Float
BDMT/	* Buffered DMA Terminate	19a	19c	BØ0	*Buffered External Phase 0 Clock
	* User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	*Buffered DMA Request 2
	* System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	*Buffered Interrupt Request	24a	24c	BNMI/	* Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	* Buffered Phase 2 Clock	26a	26c	BRES/	* Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

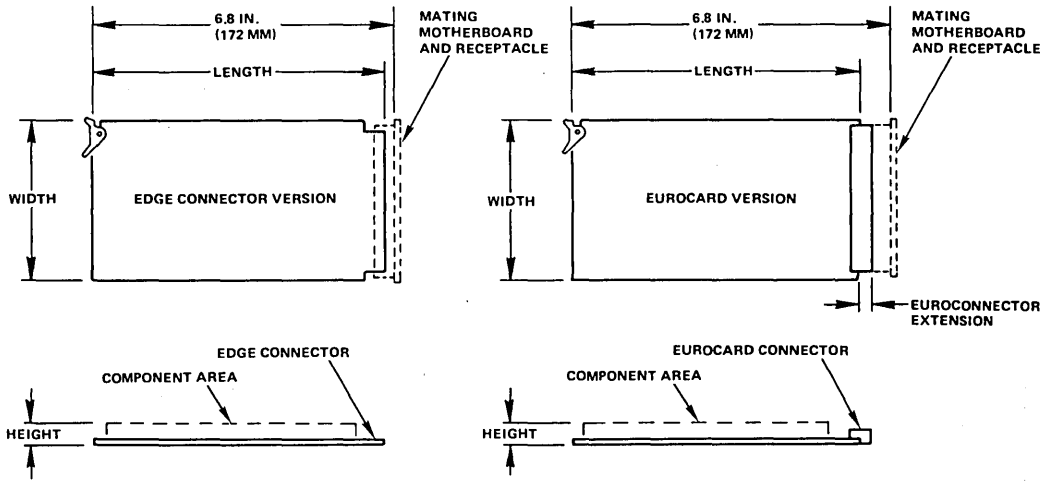
*Not used on this module

32K Dynamic RAM Module Physical and Electrical Characteristics

Characteristic	Value	
Physical Characteristics (see note)	Edge Connector Version	Eurocard Version
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (165 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	4.4 oz. (125 g)	4.5 oz. (140 g)
Environment		
Operating Temperature	$0^{o}C$ to $70^{o}C$	
Storage Temperature	$-40^{o}C$ to $85^{o}C$	
Relative Humidity	0% to 85% (without condensation)	
Power Requirements	+5 Vdc ±5% 1.4 A (7.0 W) – Maximum +12 Vdc ±5% 170 mA (2.1 W) – Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

PART NUMBER
RM65-3216(E)

Rockwell

RM 65
DATA SHEET

16K PROM/ROM MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

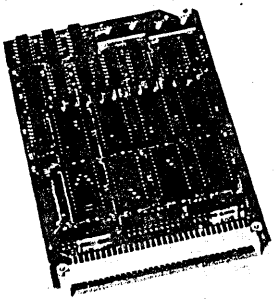
The 16K PROM/ROM Module is available in an Edge Connector version (RM65-3216) and a Eurocard version (RM65-3216E).

FEATURES

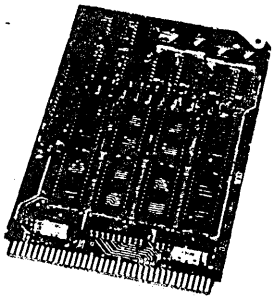
- Compact size – about 4" x 6¼" (100 mm x 160 mm)
- Edge connector and Eurocard versions
- RM 65 Bus compatible
- Buffered address, data and control lines
- Supports the following PROMs/ROMs or equivalents:
  Intel 2716 or 2732 PROMs
  TI TMS 2516 or 2532 PROMs
  Rockwell R2316, R2332 or R2364 ROMs
- Low-power PROM operation selectable by individual socket jumpers
- Jumpers allow selection of 2K, 4K or 8K byte devices
- Starting address selectable for each of four 4K memory blocks
- Separate switch allows 8K to be dedicated to one or two memory bank operation
- +5V operation
- Fully assembled, tested and warranted.

PRODUCT OVERVIEW

The RM 65 16K PROM/ROM Module has eight, 24-pin sockets to accept up to 16K bytes of either programmable read-only memory (PROM) or masked read-only memory (ROM) devices. On-board jumpers permit selection of 2K, 4K or 8K byte PROM/ROM devices. Switches allow setting of the starting address for independent 4K byte blocks of memory. All 16K bytes can be assigned to two memory banks, or 8K can be assigned to common memory while the other 8K can be dedicated to one or two 65K memory banks. Low power operation is jumper selectable for PROMs that have this option.



Eurocard Version
RM65-3216E



Edge Connector Version
RM65-3216

Specifications subject to change without notice
Document No. RMA65 N02
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

The PROM/ROM module has eight 24-pin sockets which can accept up to 16K of either 2K, 4K, or 8K PROM or ROM.

The Data Buffers invert and transfer 8-bits of parallel data from the selected PROM/ROM devices to the RM 65 Bus during read operations.

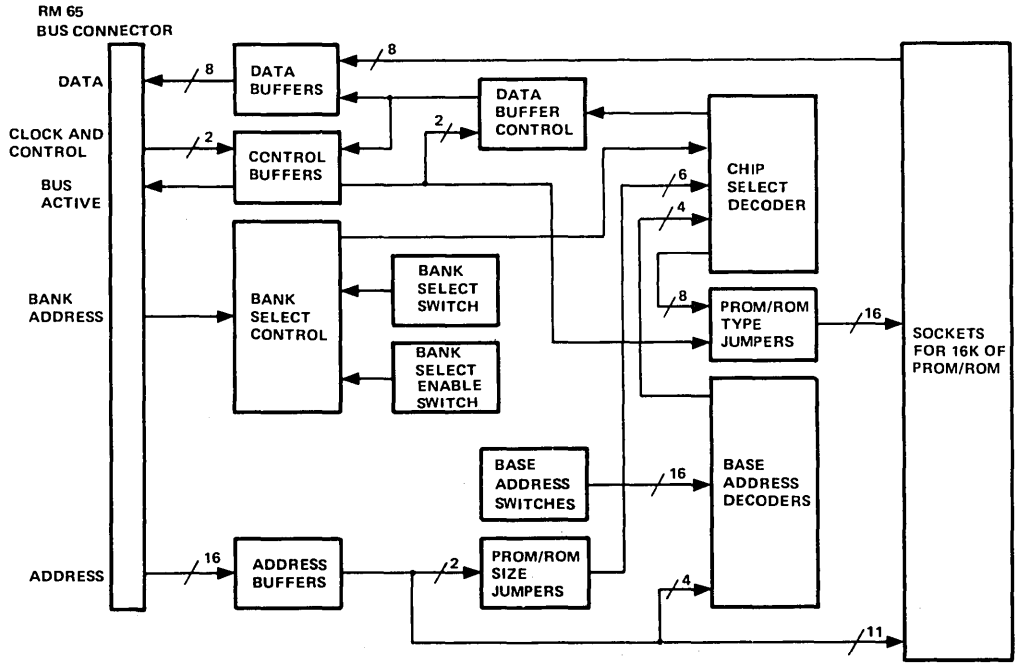
The Control Buffers invert and transfer phase 2 clock, and read/write control signals from the RM 65 Bus onto the PROM/ROM module, and drive the bus active signal onto the RM 65 Bus.

The Bank Select control circuit detects when the PROM/ROM module's assigned memory bank is addressed, by comparing the bank address signal from the RM 65 Bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows 8K of the PROM/ROM to be common memory (addressable in both Bank 0 and Bank 1) while the remaining 8K is assigned either to Bank 0 or Bank 1, as determined by the Bank Select switch.

Four Base Address Decoders allow 4K PROM/ROM sections to be independently addressed on any 4K boundary within the selected bank. When an address falls within any section (per the Base Address switches), an enable signal is sent to the Chip Select Decoder.

The Chip Select Decoder uses outputs from the Bank Select Control circuit, the Base Address Decoders, and the PROM/ROM size jumpers as well as the address lines to generate chip selects to the PROM/ROM devices. The PROM/ROM type jumpers route the chip select lines to the correct pins on the PROM/ROM sockets.

The Data Buffer Control circuit enables the Data Buffers during a read operation when an address corresponding to a selected base address is decoded and the selected PROM/ROM memory bank is addressed.



16K PROM/ROM Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
	Not Connected (See Note)		Wa	Wc		Not Connected (See Note)	
+5V	+5 Vdc Line (See Note)		Xa	Xc	+5V	+5 Vdc (See Note)	
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	I	2a	2c	BA15/	Buffered Address Bit 15	I
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	I
BA13/	Buffered Address Bit 13	I	4a	4c	BA12/	Buffered Address Bit 12	I
BA11/	Buffered Address Bit 11	I	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	I	6a	6c	BA9/	Buffered Address Bit 9	I
BA8/	Buffered Address Bit 8	I	7a	7c	BA7/	Buffered Address Bit 7	I
GND	Ground		8a	8c	BA6/	Buffered Address Bit 6	I
BA5/	Buffered Address Bit 5	I	9a	9c	BA4/	Buffered Address Bit 4	I
BA3/	Buffered Address Bit 3	I	10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	I	11a	11c	BA1/	Buffered Address Bit 1	I
BA0/	Buffered Address Bit 0	I	12a	12c	BØ1	*Buffered Phase 1 Clock	
GND	Ground		13a	13c	BSYNC	*Buffered Sync	
BSO	*Buffered Set Overflow		14a	14c	BDRQ1/	*Buffered DMA Request 1	
BRDY	*Buffered Ready		15a	15c	GND	Ground	
	*User Spare 1		16a	16c	-12V/-V	*-12 Vdc/-V	
+12V/+V	*+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	*Buffered Bus Float	
BDMT/	*Buffered DMA Terminate		19a	19c	BØ0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/$\overline{W}$/	*Buffered Read/Write "Not"		21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/$\overline{W}$	Buffered Read/Write	I
GND	Ground		23a	23c	BACT/	Buffered Bus Active	O
BIRQ/	*Buffered Interrupt Request		24a	24c	BNMI/	*Buffered Non-Maskable Interrupt	
BØ2/	*Buffered Phase 2 "Not" Clock		25a	25c	GND	Ground	
BØ2	*Buffered Phase 2 Clock		26a	26c	BRES/	*Buffered Reset	
BD7/	Buffered Data Bit 7	O	27a	27c	BD6/	Buffered Data Bit 6	O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	O
BD4/	Buffered Data Bit 4	O	29a	29c	BD3/	Buffered Data Bit 3	O
BD2/	Buffered Data Bit 2	O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	O	31a	31c	BD0/	Buffered Data Bit 0	O
+5V	+5 Vdc		32a	32c	GND	Ground	
+5V	+5 Vdc (See Note)		Ya	Yc	+5V	+5 Vdc (See Note)	
	Not Connected (See Note)		Za	Zc		Not Connected (See Note)	

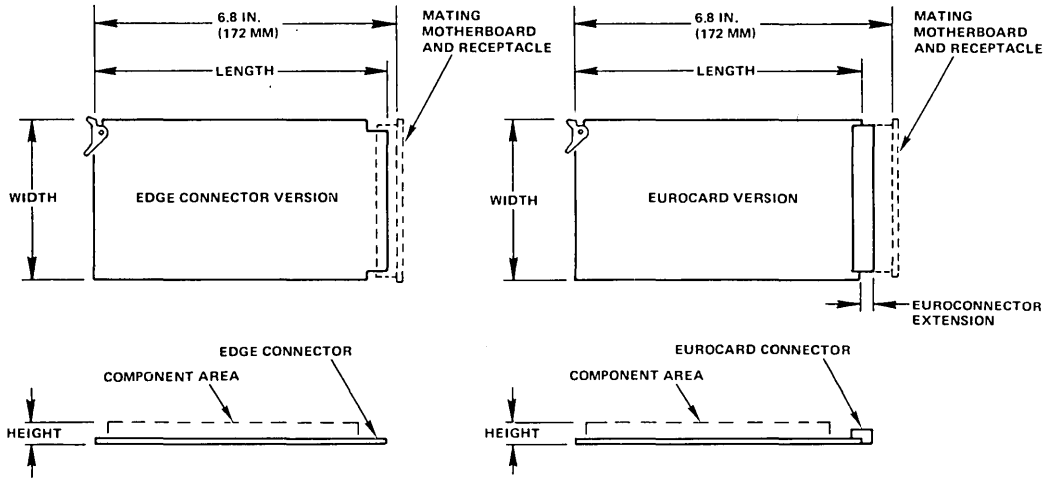
NOTE
Pins Wa, Wc, Xa, Xc, Ya, Yc, Za, Zc are not used on the Eurocard version.
*Not used on the 16K PROM/ROM module.

16K PROM/ROM Module Physical and Electrical Characteristics

Characteristic	Value	
Physical Characteristics (See Notes)		
	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	4.6 oz. (130 g)	5.0 oz. (140 g)
Environment		
Operating Temperature	$0^{o}C$ to $70^{o}C$	
Storage Temperature	$-40^{o}C$ to $85^{o}C$	
Relative Humidity	0% to 85% (without condensation)	
Power Requirements w/o PROM/ROM Devices	+5 Vdc ±5% 0.17A (0.85W) – Typical 0.27A (1.35W) – Maximum	
Access Time	450 nanoseconds (max)	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include the added extension due to the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

PART NUMBER
RM65-7101(E)

Rockwell

RM 65
DATA SHEET

SINGLE CARD ADAPTER

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

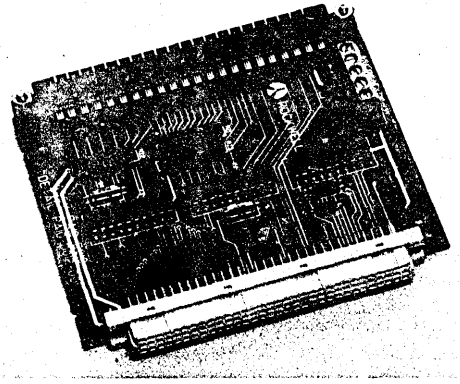
The Single Card Adapter is available in an Edge Connector version (RM65-7101) and a Eurocard version (RM65-7101E).

FEATURES

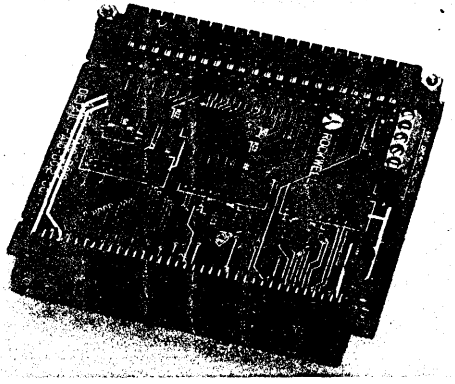
- Drives one RM 65 Bus-compatible module
- Provision for power and ground routing
- Extends address, data and control lines
- Edge connector and Eurocard versions
- Fully assembled, tested and warranted

PRODUCT OVERVIEW

The RM 65 Single-Card Adapter allows one RM 65 Bus compatible module to be connected to the AIM 65 Master Module, through the AIM 65 Expansion connector. The Adapter routes the AIM 65 address, data and control lines from the AIM 65 Expansion connector pin assignments to the RM 65 Bus pin assignments. Drive circuitry is included on the address and data lines.



Eurocard Version
RM65-7101E



Edge Connector Version
RM65-7101

Specifications subject to change without notice
Document No. RMA65 N03
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

The Single Card Adapter interfaces AIM 65 Expansion Connector signals to an attached RM 65 Bus receptacle. Data and address lines are buffered, whereas control lines are directly wired. All signals are routed from the AIM 65 Expansion Connector positions to corresponding RM 65 Bus receptacle pin positions. Ground is connected to the interspersed RM 65 Bus GND pins.

The Data Transceivers invert and drive 8-bits of parallel data between the AIM 65 Expansion Connector and the RM 65 Bus interface. During a write operation, data received from the AIM 65 Expansion Connector are driven into the interfacing RM 65 module. During a read operation, data read from the RM 65 module are transmitted into the AIM 65. When the RM 65 module is not addressed, the transceivers are disabled.

The Address Buffers invert and buffer 16 parallel address bits from the AIM 65 to the connected RM 65 module. The bank address line is held high to address Bank 0 (lower 65K) in the interfacing RM 65 module.

Eleven control and timing signals are directly connected between the AIM 65 Expansion Connector and the RM 65 module. The read/write, phase 2 clock, phase 1 clock, sync and reset AIM 65 output lines are routed directly to the RM 65 receptacle. The ready, interrupt request, set overflow and non-maskable interrupt lines from the RM 65 receptacle are connected straight through to the AIM 65 Expansion Connector interface.

A terminal block allows external +5V, +12V/+V, and -12V/-V power supplies to be connected as required. An on-board jumper allows the +5V for the RM 65 module to originate from the AIM 65 Expansion Connector or from the external +5V power supply.

POWER CONNECTION

+5V Power Connection

The +5V required for the Single Card Adapter can be provided from the AIM 65 microcomputer through the AIM 65 Expansion Connector or directly from an external power supply through a connection to the on-board terminal board (TB1). Jumper A/B routes the +5V power from the selected source.

CAUTION

Turn off the external power supply before connecting power leads to the Single Card Adapter.

AIM 65 +5V Power Source Connection

(1) Install Jumper A/B in the A position.

(2) Disconnect the +5V lead of the external power supply from the +5V connection on TB1.

WARNING

If the mating RM 65 module draws over 0.5A, the external connection to +5V must be used or the AIM 65 Master Module may be damaged.

External +5V Power Source Connection

(1) Install Jumper A/B in the B position.

(2) Connect the +5V lead from the external power supply to the +5V connection on TB1.

(3) Connect the ground lead from the external +5V power supply to either of the two GND connections on TB1.

±12V/±V Power Connection

Connection points are provided on TB1 for ±12 Vdc, or other voltages, as required by the mating RM 65 module.

(1) Connect the +12V/+V lead from the external power supply to the TB1 connection marked +15V or +V. This terminal is connected to connector J1 pin 17a.

(2) Connect the -12V/-V lead from the external power supply to the TB1 connection marked -15V or -V. This terminal is connected to connector J1 pin 16c.

INSTALLING THE SINGLE CARD ADAPTER

Before installing the module, ensure that it is not damaged and is free of grease, dirt, liquid or other foreign material.

CAUTION

Prior to module installation, turn off power to the AIM 65 and, if applicable, the optional external +5V and/or ±12V/±V power supply input to the Adapter.

a. Align pin 1 of J3 on the SCA with pin 1 of the Expansion Connector on the AIM 65 Master Module (component side up).

b. Carefully insert the Adapter into the Expansion Connector.

c. Press in firmly until all pins are securely seated.

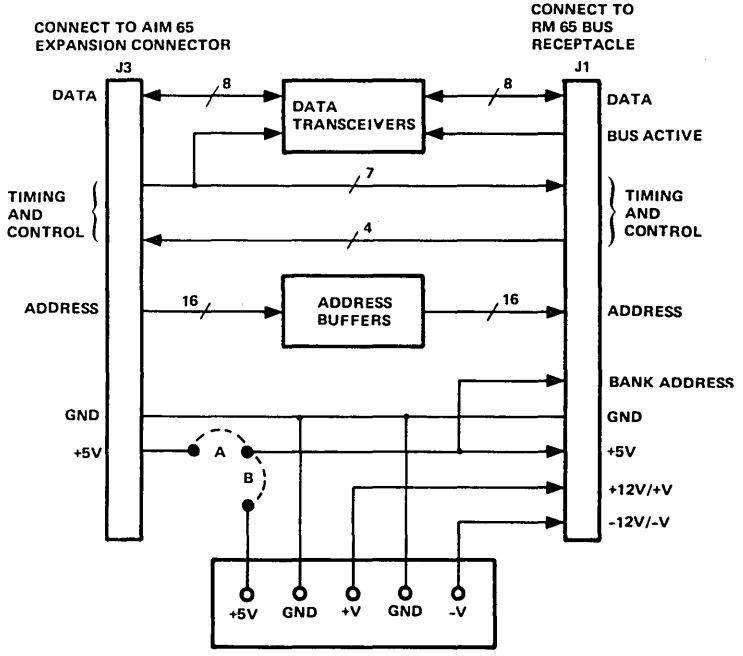
d. Install the RM 65 module into the J1 connector on the Adapter using installation procedures described in the documentation for the particular module. Ensure that Bank Select switches on the add-on module are positioned to Bank Select 0 or Bank Select Disable, as appropriate.

e. Turn on power to the AIM 65 and, if applicable, turn on external +5 Vdc and/or ±12V/±V to the SCA module.

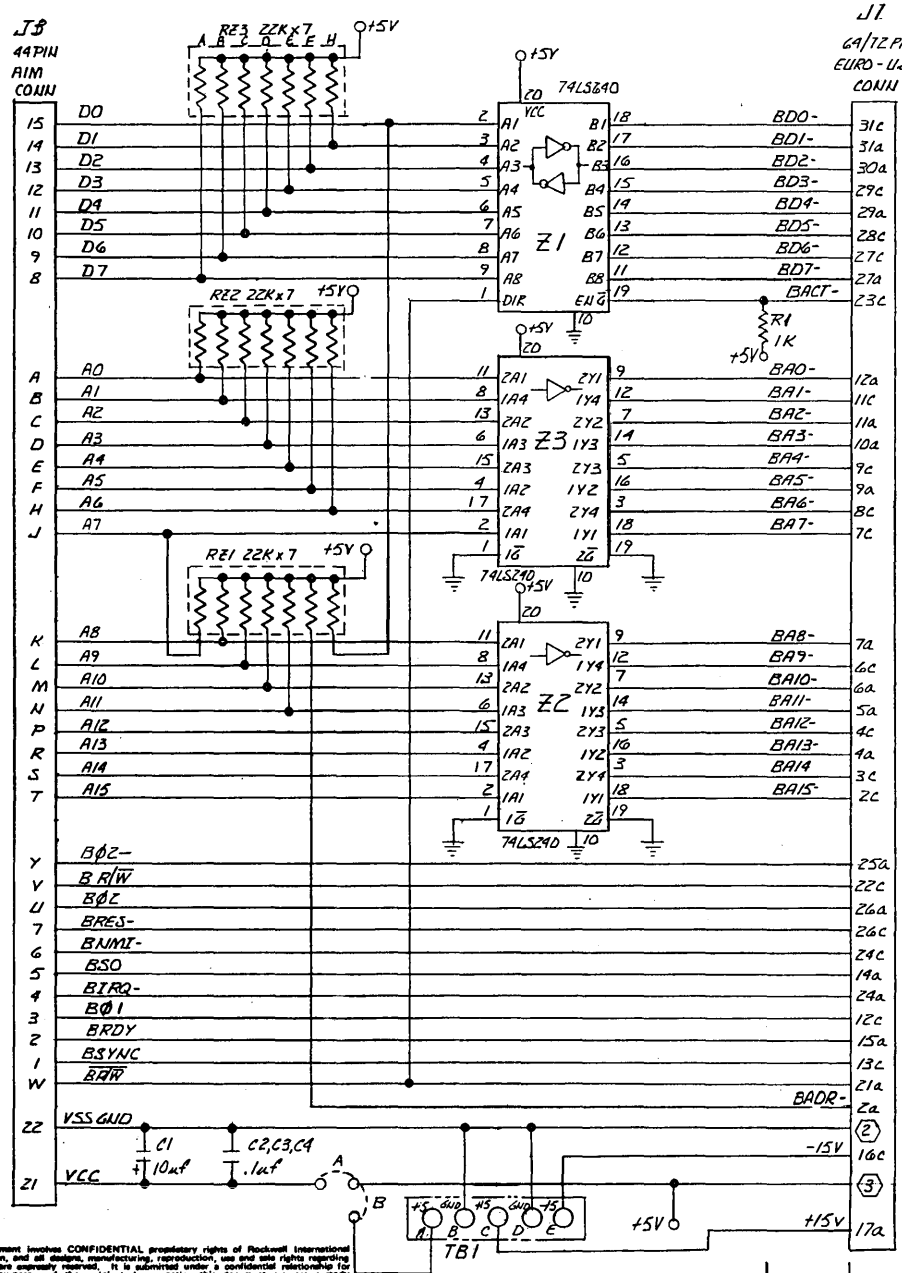
REMOVING THE SINGLE CARD ADAPTER

a. Turn off power to the AIM 65 and if applicable, to the external ±12V/±V power supplies.

b. Pull the Adapter straight back while moving it slightly from side to side to disconnect it from the AIM 65 Expansion Connector.



Single Card Adapter Block Diagram



NC 52280

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

NOTE: UNLESS OTHERWISE SPECIFIED

1. REF ASSY DWG PAIO-D010
2. PINS 1a, 3a, 5c, 8a, 10c, 13a, 15c, 18a, 20c, 23a, 25c, 28a, 30c, 32c SHALL BE CONNECTED TO GROUND.
3. PINS 1c, 32a ON EURO CONNECTOR AND PINS Xa, Xc, Ya, Yc, 1c, 32a ON U.S. CONNECTOR SHALL BE TIED TO +5V.

PAIO-X011

RM65 BOARD PRODUCTS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX = ± .03 .XXX = ± .010 ANGLES ± 30'	AUTHORIZATION NO.	PART NO.	
	DR BY Reed 3-3-80	ROCKWELL INTERNATIONAL CORPORATION MICROELECTRONIC DEVICES 3310 MIRALOMA AVE., ANAHEIM, CA 92803	
	CHK BY	SCHEMATIC - SINGLE CARD ADAPTER	
	APPD BY		
HEAT TREAT	APPD BY	SIZE C / CODE IDENT NO. 34576 / DRAWING NO. PAIO-X011	
FINISH		SCALE	SHEET

183-G-13 Rev. 8-78

RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
	Not Connected (See Note)		Wa	Wc		Not Connected (See Note)	
+5V	+5 Vdc Line (See Note)		Xa	Xc	+5V	+5 Vdc (See Note)	
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	O	2a	2c	BA15/	Buffered Address Bit 15	O
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	O
BA13/	Buffered Address Bit 13	O	4a	4c	BA12/	Buffered Address Bit 12	O
BA11/	Buffered Address Bit 11	O	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	O	6a	6c	BA9/	Buffered Address Bit 9	O
BA8/	Buffered Address Bit 8	O	7a	7c	BA7/	Buffered Address Bit 7	O
GND	Ground		8a	8c	BA6/	Buffered Address Bit 6	O
BA5/	Buffered Address Bit 5	O	9a	9c	BA4/	Buffered Address Bit 4	O
BA3/	Buffered Address Bit 3	O	10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	O	11a	11c	BA1/	Buffered Address Bit 1	O
BA0/	Buffered Address Bit 0	O	12a	12c	BØ1	Buffered Phase 1 Clock	O
GND	Ground		13a	13c	BSYNC	Buffered Sync	O
BSO	Buffered Set Overflow	I	14a	14c	BDRQ1/	*Buffered DMA Request 1	
BRDY	Buffered Ready	I	15a	15c	GND	Ground	
	*User Spare 1		16a	16c	-12V/-V	-12 Vdc/-V	
+12V/+V	+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	*Buffered Bus Float	
BDMT/	*Buffered DMA Terminate		19a	19c	BØ0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/$\overline{W}$/	Buffered Read/Write "Not"	O	21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/$\overline{W}$	Buffered Read/Write	O
GND	Ground		23a	23c	BACT/	Buffered Bus Active	I
BIRQ/	Buffered Interrupt Request	I	24a	24c	BNMI/	Buffered Non-Maskable Interrupt	I
BØ2/	Buffered Phase 2 "Not" Clock	O	25a	25c	GND	Ground	
BØ2	Buffered Phase 2 Clock	O	26a	26c	BRES/	Buffered Reset	O
BD7/	Buffered Data Bit 7	I/O	27a	27c	BD6/	Buffered Data Bit 6	I/O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	I/O
BD4/	Buffered Data Bit 4	I/O	29a	29c	BD3/	Buffered Data Bit 3	I/O
BD2/	Buffered Data Bit 2	I/O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	I/O	31a	31c	BD0/	Buffered Data Bit 0	I/O
+5V	+5 Vdc		32a	32c	GND	Ground	
+5V	+5 Vdc (See Note)		Ya	Yc	+5V	+5 Vdc (See Note)	
	*Not Connected (See Note)		Za	Zc		Not Connected (See Note)	

NOTE
Pins Wa, Wc, Xa, Xc, Ya, Yc, Za, Zc are not used on the Eurocard version.
*Not used on this module.

AIM 65 Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
SYNC	Sync	I	1	A	A0	Address Bit 0	I
RDY	Ready	O	2	B	A1	Address Bit 1	I
Ø1	Phase 1 Clock	I	3	C	A2	Address Bit 2	I
$\overline{IRQ}$	Interrupt Request	O	4	D	A3	Address Bit 3	I
S.O.	Set Overflow	O	5	E	A4	Address Bit 4	I
$\overline{NMI}$	Non-Maskable Interrupt	O	6	F	A5	Address Bit 5	I
$\overline{RES}$	Reset	I	7	H	A6	Address Bit 6	I
D7	Data Bit 7	I/O	8	J	A7	Address Bit 7	I
D6	Data Bit 6	I/O	9	K	A8	Address Bit 8	I
D5	Data Bit 5	I/O	10	L	A9	Address Bit 9	I
D4	Data Bit 4	I/O	11	M	A10	Address Bit 10	I
D3	Data Bit 3	I/O	12	N	A11	Address Bit 11	I
D2	Data Bit 2	I/O	13	P	A12	Address Bit 12	I
D1	Data Bit 1	I/O	14	R	A13	Address Bit 13	I
D0	Data Bit 0	I/O	15	S	A14	Address Bit 14	I
-12V	*-12 Vdc		16	T	A15	Address Bit 15	I
+12V	*+12 Vdc		17	U	SYS Ø2	System Phase 2 Clock	I
$\overline{CS8}$	*Chip Select 8		18	V	SYS R/$\overline{W}$	System Read/Write	I
$\overline{CS9}$	*Chip Select 9		19	W	R/$\overline{W}$	Read/Write "Not"	I
$\overline{CSA}$	*Chip Select A		20	X	*TEST	Test	
+5V	+5 Vdc		21	Y	$\overline{Ø2}$	Phase 2 Clock "Not"	I
GND	Ground		22	Z	*RAM R/$\overline{W}$	RAM Read/Write	

NOTE:

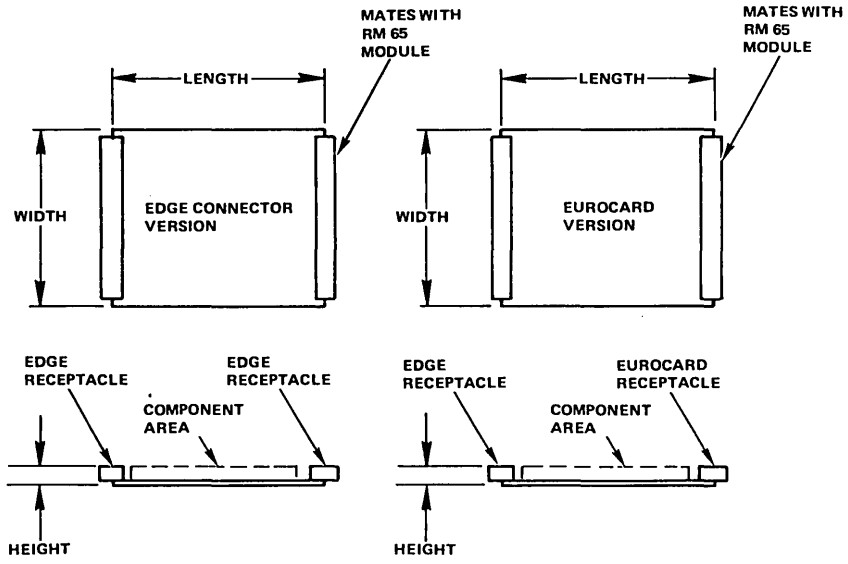
* = Not used on this module.

Single Card Adapter Module Physical and Electrical Characteristics

Characteristic	Value	
Physical Characteristics (See Notes)		
	Edge Connector	Eurocard
Width	4.4 in. (111 mm)	4.4 in. (111 mm)
Length	3.7 in. (93 mm)	3.7 in. (93 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	3.2 oz. (95 g)	3.0 oz. (90 g)
Environment		
Operating Temperature	$0^{o}C$ to $70^{o}C$	
Storage Temperature	$-40^{o}C$ to $85^{o}C$	
Relative Humidity	0% to 85% (without condensation)	
Power Requirements	+5V ±5% 110 mA (0.55W) — Typical 200 mA (1.00W) — Maximum	
Interface		
AIM 65 Expansion Connector	22/44 — edge receptacle (0.156 in. centers)	
RM 65 Bus		
Edge Connector Version	72-pin edge receptacle (0.100 in. centers)	
Eurocard Version	64-pin receptacle (0.100 in. centers) per DIN 41612 (Row b is not installed)	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include extensions beyond the edge of the module due to connectors.



Module Dimensions

PART NUMBER
RM65-7104(E)

Rockwell

RM 65
DATA SHEET

ADAPTER/BUFFER

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

The Adapter/Buffer is available in an Edge Connector Version (RM65-7104) and a Eurocard version (RM65-7104E).

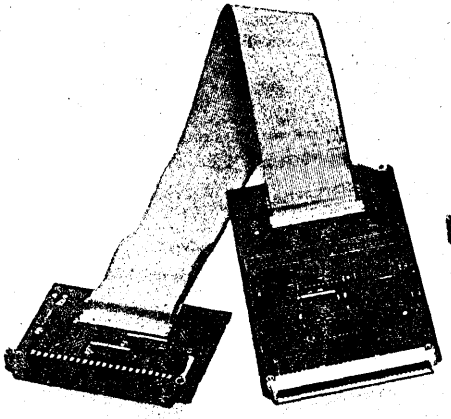
FEATURES

- RM 65 Bus Compatible
- Buffered address data and control lines
- Drives up to 15 modules
- Edge connector and Eurocard versions
- Fully assembled, tested and warranted

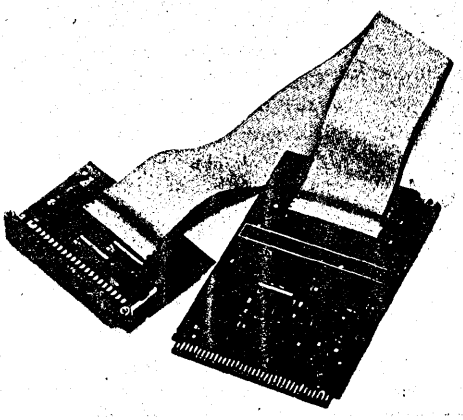
PRODUCT OVERVIEW

The Adapter/Buffer extends the RM 65 Bus from the AIM 65 Expansion Connector to a compatible motherboard that is situated up to 16 inches away. Included circuitry permits the Adapter/Buffer to drive up to 15 RM 65 Bus-compatible modules. (The similar Cable Driver Adapter/Buffer, Part Number RM65-7116, provides the same drive capability for applications in which the motherboard is up to six feet from the Expansion Connector.)

The Adapter/Buffer consists of an adapter module, a buffer module and two 16-inch interconnect cables. Both cables are flexible, so the motherboard may be installed in a wide variety of locations and orientations relative to the AIM 65.



Eurocard Version
RM65-7104E



Edge Connector Version
RM65-7104

RM65 BOARD PRODUCTS

ADAPTER/BUFFER

Specifications subject to change without notice
Document No. RMA65 N04
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

The Adapter/Buffer consists of two modules and two interconnect cables. The Adapter module connects to the AIM 65 Expansion connector and the Buffer module connects to an RM 65 Bus motherboard receptacle.

The Adapter module transfers data, address and control lines from AIM 65 Expansion Connector to the interconnect cables. The eight data and 16 address lines are routed directly, without buffering. The read/write, clock, sync and reset AIM 65 output control lines are also routed directly through the Adapter. The ready, set overflow, interrupt request and non-maskable interrupt AIM 65 input lines are buffered on the module.

Two 16-inch 40 conductor flat ribbon cables connect the Adapter module to the Buffer module. The cables are mass terminated at each end, and are permanently attached to the interfacing module.

The Buffer module buffers and routes all interface signals between the interconnect cables and the RM 65 Bus connector.

The Data Transceivers invert and drive 8-bits of parallel data. During a write operation, data received from the cables are driven onto the RM 65 Bus. During a read operation, data received from the RM 65 Bus are driven onto the cables. The bus active signal enables the Transceivers. When the bus float signal is active, the Transceivers are disabled.

The Address Buffers invert and transfer 16 parallel address lines from the interconnect cable to the RM 65 Bus. When the bus float signal is active, the Buffers are disabled.

Jumper E1 selects the source for the bank address line (BADR/) – either the buffer module or an external module. When the buffer module is the source (position A), the bank address line is held high to address Bank 0 (Lower 65K) on the Bus; this line is disabled when the bus float line is active. For an external source (position B), the bank address line is not used by the buffer module, and must be controlled by another module on the Bus.

The seven read/write, clock, sync and reset lines from the cables to the bus are buffered by the Control Drivers. All of these lines, except reset and phase 1, are disabled when the bus float line is active. The ready, set overflow, interrupt request and non-maskable lines from the bus to the interconnect cables are also buffered by the Control Drivers.

Jumper E2 selects the source for the DMA Terminate line (BDMT/) – either the buffer module or an external module. When the buffer module is the source (position A), the DMA terminate line is held high (inactive). For an external source (position B), the DMA terminate line is not used by the buffer module, and must be controlled by another module on the bus.

INSTALLATION

Installing the Adapter/Buffer

Before installing the module, ensure that it is not damaged and is free of grease, dirt, liquid or other foreign material.

a. Before installing the Adapter/Buffer, turn off power to the AIM 65 and the interfacing RM 65 Bus motherboard.

b. Configure Jumpers E1 and E2, per the Functional Description.

c. Align the Adapter module connector J3 pin 1 with the AIM 65 Expansion Connector J3 pin 1.

d. Plug the Adapter module onto the Expansion Connector. Press in firmly on the end of module until all pins are securely seated.

e. Install connector P1 of the Buffer module into the desired slot on the mating RM 65 Bus motherboard.

CAUTION

RM 65 Bus connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and connector alignment of the module. Forcing the module improperly into the receptacle may damage the receptacle and/or the module.

f. Apply power to the AIM 65 and to the mating RM 65 Bus motherboard.

Removing the Adapter/Buffer

a. Turn off power to the AIM 65 and to the RM 65 Bus motherboard.

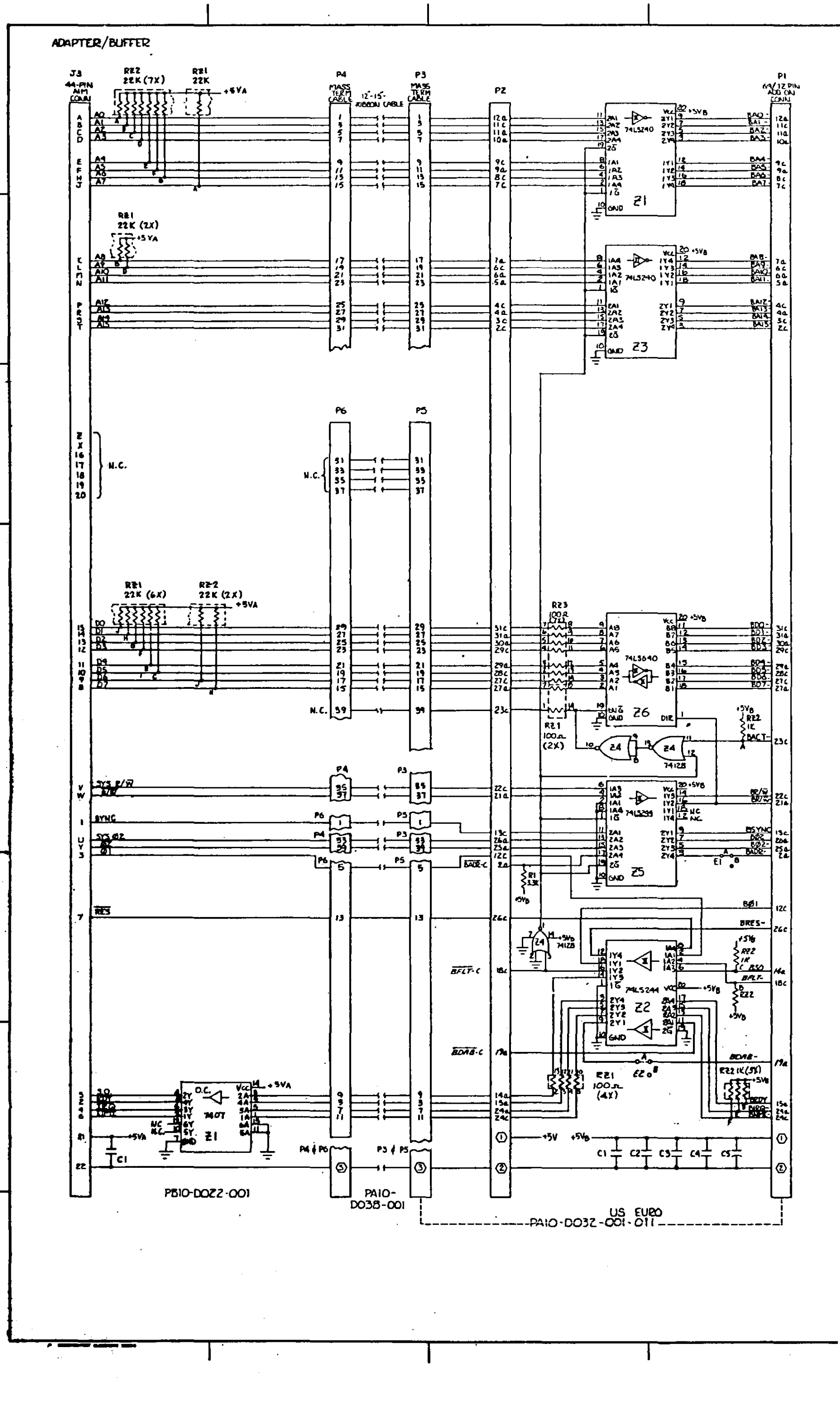
b. Lift up on the Buffer module ejector tab to release the module from the mating RM 65 Bus receptacle. Pull the module straight back until it is free from the card slot guides.

c. Pull back on the Adapter module while moving it slightly from side to side until it is free from the AIM 65 Expansion Connector.

Buffer Module to RM 65 Bus Connector Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
	Not Connected (See Note)		Wa	Wc		Not Connected (See Note)	
+5V	+5 Vdc Line (See Note)		Xa	Xc	+5V	+5 Vdc (See Note)	
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	O	2a	2c	BA15/	Buffered Address Bit 15	O
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	O
BA13/	Buffered Address Bit 13	O	4a	4c	BA12/	Buffered Address Bit 12	O
BA11/	Buffered Address Bit 11	O	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	O	6a	6c	BA9/	Buffered Address Bit 9	O
BA8/	Buffered Address Bit 8	O	7a	7c	BA7/	Buffered Address Bit 7	O
GND	Ground		8a	8c	BA6/	Buffered Address Bit 6	O
BA5/	Buffered Address Bit 5	O	9a	9c	BA4/	Buffered Address Bit 4	O
BA3/	Buffered Address Bit 3	O	10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	O	11a	11c	BA1/	Buffered Address Bit 1	O
BA0/	Buffered Address Bit 0	O	12a	12c	BØ1	Buffered Phase 1 Clock	O
GND	Ground		13a	13c	BSYNC	Buffered Sync	O
BSO	Buffered Set Overflow	I	14a	14c	BDRQ1/	*Buffered DMA Request 1	
BRDY	Buffered Ready	I	15a	15c	GND	Ground	
	*User Spare 1		16a	16c	-12V/-V	*-12 Vdc/-V	
+12V/+V	*+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	Buffered Bus Float	I
BDMT/	Buffered DMA Terminate		19a	19c	BØ0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/$\overline{W}$/	Buffered Read/Write "Not"	O	21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/$\overline{W}$	Buffered Read/Write	O
GND	Ground		23a	23c	BACT/	Buffered Bus Active	I
BIRQ/	Buffered Interrupt Request	I	24a	24c	BNMI/	Buffered Non-Maskable Interrupt	I
BØ2/	Buffered Phase 2 "Not" Clock	O	25a	25c	GND	Ground	
BØ2	Buffered Phase 2 Clock	O	26a	26c	BRES/	Buffered Reset	O
BD7/	Buffered Data Bit 7	I/O	27a	27c	BD6/	Buffered Data Bit 6	I/O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	I/O
BD4/	Buffered Data Bit 4	I/O	29a	29c	BD3/	Buffered Data Bit 3	I/O
BD2/	Buffered Data Bit 2	I/O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	I/O	31a	31c	BD0/	Buffered Data Bit 0	I/O
+5V	+5 Vdc		32a	32c	GND	Ground	
+5V	+5 Vdc (See Note)		Ya	Yc	+5V	+5 Vdc (See Note)	
	Not Connected (See Note)		Za	Zc		Not Connected (See Note)	

NOTE
Pins Wa, Wc, Xa, Xc, Ya, Yc, Za, Zc are not used on the Eurocard version.
*Not used on this module.


ADAPTER/BUFFER
J3 44-PIN AIM CONN
P4 MASS TERM CABLE
12"-15" RIBBON CABLE
P3 MASS TERM CABLE
P2
P1
74LS240
Z1
Z3
74LS640
Z6
74128
74LS244
Z2
N.C.
PB10-D022-001
PA10-D038-001
US EURO
PA10-D032-001-011

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED

NOTE: UNLESS OTHERWISE SPECIFIED

1. PINS 1c, 32a ON EURO CONNECTOR AND PINS Xa, Xc, Ya, Yc, 1c, 32a, ON U.S. CONNECTOR SHALL BE TIED TO +5V
2. PINS 1a, 3a, 5c, 8a, 10c, 13a, 15c, 18a, 20c, 23a, 25c, 28a, 30c, 32c, SHALL BE TIED TO GND.
3. ALL EVEN NUMBER PINS (2 THRU 40) SHALL BE TIED TO GND.
4. ALL CAPACITORS ARE .10 UF ±20%, 50V.

QTY REQD	QTY REQD	QTY REQD	QTY REQD	QTY REQD	MEAS UNIT	ITEM NO.	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS .XX = ± [illegible] .XXX = ± [illegible] ANGLES ± [illegible]	AUTHORIZATION NO.	[illegible]
	DR BY: R. ANDERSON [illegible]	SCHEMATIC-ASSY ADAPTER/BUFFER 4 SLOT CARD CAGE
	CHK BY: [illegible] 6/24/7?	
MATERIAL	APPD BY: [illegible] 9?/?6	
	APPD BY	
HEAT TREAT		SIZE: E — CODE IDENT NO.: 34576 — DRAWING NO.: PAIO-X021
FINISH		SCALE: NONE — SHEET

DASH NO.	NEXT ASSY	USED ON
APPLICATION		

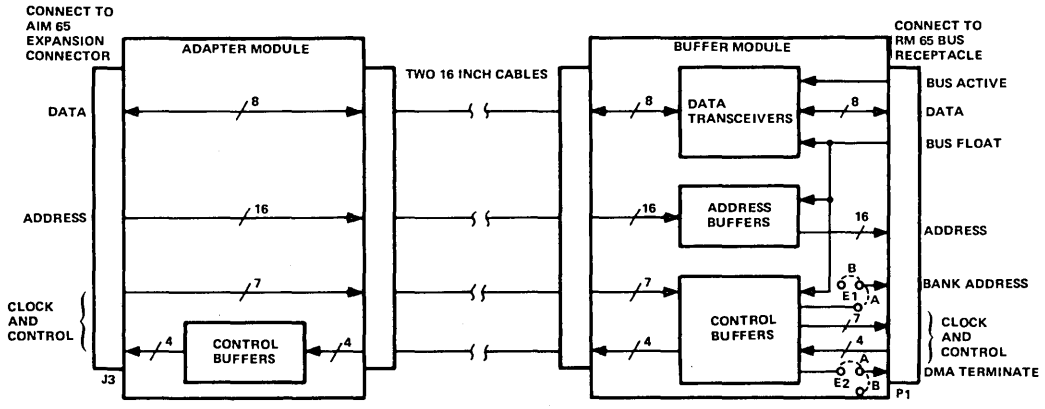
RM65 BOARD PRODUCTS

Adapter Module to AIM 65 Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
SYNC	SYNC	I	1	A	A0	Address Bit 0	I
RDY	Ready	O	2	B	A1	Address Bit 1	I
Ø1	Phase 1 Clock	I	3	C	A2	Address Bit 2	I
$\overline{IRQ}$	Interrupt Request	O	4	D	A3	Address Bit 3	I
S.O.	Set Overflow	O	5	E	A4	Address Bit 4	I
$\overline{NMI}$	Non-Maskable Interrupt	O	6	F	A5	Address Bit 5	I
$\overline{RES}$	Reset	O	7	H	A6	Address Bit 6	I
D7	Data Bit 7	I/O	8	J	A7	Address Bit 7	I
D6	Data Bit 6	I/O	9	K	A8	Address Bit 8	I
D5	Data Bit 5	I/O	10	L	A9	Address Bit 9	I
D4	Data Bit 4	I/O	11	M	A10	Address Bit 10	I
D3	Data Bit 3	I/O	12	N	A11	Address Bit 11	I
D2	Data Bit 2	I/O	13	P	A12	Address Bit 12	I
D1	Data Bit 1	I/O	14	R	A13	Address Bit 13	I
D0	Data Bit 0	I/O	15	S	A14	Address Bit 14	I
-12V	*-12 Vdc		16	T	A15	Address Bit 15	I
+12V	*+12 Vdc		17	U	SYS Ø2	System Phase 2 Clock	I
$\overline{CS8}$	*Chip Select 8		18	V	SYS R/$\overline{W}$	System Read/Write	I
$\overline{CS9}$	*Chip Select 9		19	W	R/$\overline{W}$	Read/Write "Not"	I
$\overline{CSA}$	*Chip Select A		20	X	TEST	*Test	
+5V	+5 Vdc		21	Y	$\overline{Ø2}$	Phase 2 Clock "Not"	I
GND	Ground		22	Z	RAM R/$\overline{W}$	*RAM Read/Write	

NOTE:

* = Not used on this module.



Adapter/Buffer Block Diagram

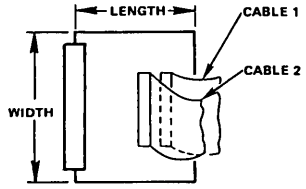
Adapter/Buffer Physical and Electrical Characteristics

Characteristics	Value	
Dimension (See Notes)		
Adapter Module		
Width	4.4 in. (111 mm)	
Length	2.6 in. (67 mm)	
Height	0.56 in. (14 mm)	
Buffer Module	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	6.9 oz. (195 g)	7.2 oz. (205 g)
Power		
Adapter Module	+5V ±5% 30 mA (0.15W) – Typical 50 mA (0.25W) – Maximum	
Buffer Module	+5V ±5% 190 mA (0.95W) – Typical 330 mA (1.7 W) – Maximum	
Environment		
Operating Temperature	$0^{o}C$ to $70^{o}C$	
Storage Temperature	$-40^{o}C$ to $85^{o}C$	
Relative Humidity	0% to 85% (without condensation)	
Propagation Time	20 ns – Maximum	
Interface Connectors		
AIM 65 Expansion Connector	22/44 – edge receptacle (0.156 in. centers)	
RM 65 Bus		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not installed)	
Interface Cables		
Number of Cables	Two	
Cable Length	16 inches	
Type	Flat ribbon	
Number of conductors per cable	40	
Wire Size	#28 AWG	

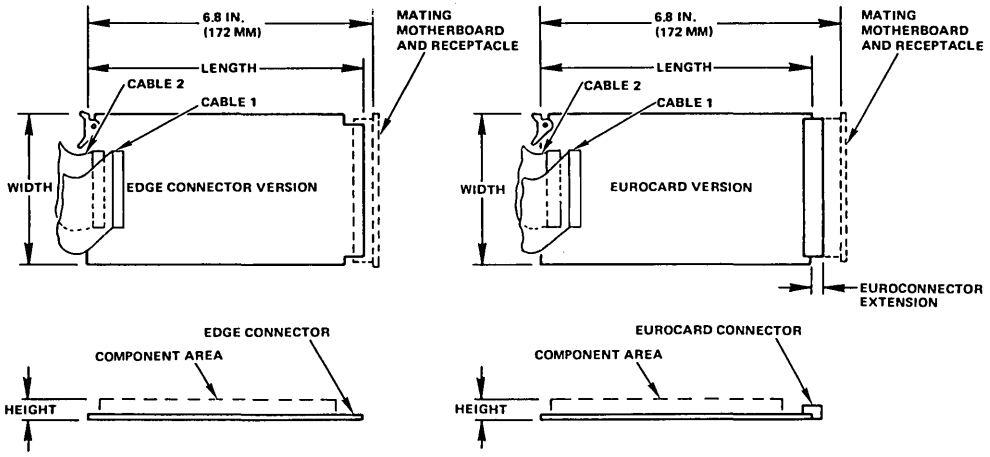
NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.)
2. The length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. The Eurocard dimensions conform to DIN 41612.

ADAPTER MODULE



BUFFER MODULE



Module Dimensions

PART NUMBER
RM65-7116(E)

Rockwell

RM 65
DATA SHEET

CABLE DRIVER ADAPTER/BUFFER

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

FEATURES

- RM 65 Bus compatible
- Buffered address data and control lines
- Drives up to 15 modules
- Long cable for distances of up to 6 feet
- Edge connector and Eurocard versions
- Fully assembled, tested and warranted

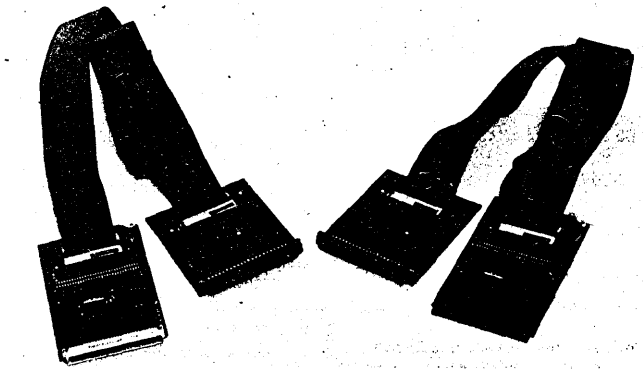
PRODUCT OVERVIEW

The Cable Driver Adapter/Buffer extends the RM 65 Bus from the AIM 65 Expansion Connector to a compatible motherboard that is situated up to six feet away. Included circuitry permits the Cable Driver Adapter/Buffer to drive up to 15 RM 65 Bus-compatible modules. (The similar Adapter/Buffer, Part Number RM65-7104, provides the same drive capability for applications in which the motherboard need not be more than 16 inches from the Expansion Connector.)

The Cable Driver Adapter/Buffer consists of a cable driver adapter module, a buffer module, and two 6-foot interconnect cables. Both cables are flexible, so the motherboard may be installed in a wide variety of locations and orientations relative to the AIM 65.

ORDERING INFORMATION

The Cable Driver Adapter/Buffer is available in an Edge Connector Version (RM65-7116) and a Eurocard version (RM65-7116E).



Eurocard Version
RM65-7116E

Edge Connector Version
RM65-7116

CABLE DRIVER ADAPTER/BUFFER

RM65 BOARD PRODUCTS

Specifications subject to change without notice
Document No. RMA65 N22
March 1981

FUNCTIONAL DESCRIPTION

The Cable Driver Adapter/Buffer consists of two modules and two interconnect cables. The Adapter Module connects to the AIM 65 Expansion connector and the Buffer module connects to an RM 65 Bus motherboard receptacle.

The Cable Driver Adapter module buffers data, address and control lines between the AIM 65 Expansion Connector and the interconnect cables.

The Data Transceivers drive 8-bits of parallel data. During a write operation, data received from the AIM 65 are driven onto the cables. During a read operation, data received from the cables are driven into the AIM 65. The bus active signal enables the Data Transceivers.

The Address Buffers drive 16-bits of parallel data from the AIM 65 onto the cables.

The Control Buffers transfer the timing and control signals between the AIM 65 and the cables. The seven read/write, clock, sync, and reset lines are driven from the AIM 65 onto the cables. The four ready, set overflow, interrupt request and non-maskable interrupt lines are driven from the cables onto the AIM 65.

Two 6-foot 40 conductor flat ribbon cables connect the Cable Driver Adapter module to the Buffer module. The cables are mass terminated at each end, and are permanently attached to the interfacing module.

The Buffer module buffers and routes all interface signals between the interconnect cables and the RM 65 Bus connector.

The Data Transceivers invert and drive 8-bits of parallel data. During a write operation, data received from the cables are driven onto the RM 65 Bus. During a read operation, data received from the RM 65 Bus are driven onto the cables. The bus active signal enables the Transceivers. When the bus float signal is active, the Transceivers are disabled.

The Address Buffers invert and transfer 16 parallel address lines from the interconnect cable to the RM 65 Bus. When the bus float signal is active, the Buffers are disabled.

Jumper E1 selects the source for the bank address line (BADR/) – either the buffer module or an external module. When the buffer module is the source (position A), the bank address line is held high to address Bank 0 (lower 65K) on the Bus; this line is disabled when the bus float line is active. For an external source (position B), the bank address line is not used by the buffer module, and must be controlled by another module on the Bus.

The seven read/write, clock, sync and reset lines from the cables to the bus are buffered by the Control Buffers. All of these lines, except reset and phase 1, are disabled when the bus float line is active. The ready, set overflow, interrupt request and non-maskable lines from the bus to the interconnect cables are also buffered by the Control Buffers.

Jumper E2 selects the source for the DMA Terminate line (BDMT/) – either the buffer module or an external module. When the buffer module is the source (position A), the DMA terminate line is held high (inactive). For an external source (position B), the DMA terminate line is not used by the buffer module, and must be controlled by another module on the bus.

INSTALLATION

Installing the Cable Driver Adapter/Buffer

Before installing the module, ensure that it is not damaged and is free of grease, dirt, liquid or other foreign material.

a. Before installing the Cable Driver Adapter/Buffer, turn off power to the AIM 65 and the interfacing RM 65 Bus motherboard.

b. Configure Jumpers E1 and E2, per the Functional Description.

c. Align Cable Driver Adapter module connector J3 pin 1 with the AIM 65 Expansion Connector J3 pin 1.

d. Plug the Cable Driver Adapter module onto the Expansion Connector. Press in firmly on the end of module until all pins are securely seated.

e. Install connector P1 of the Buffer module into the desired slot on the mating RM 65 Bus motherboard.

CAUTION

RM 65 Bus connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and connector alignment of the module. Forcing the module improperly into the receptacle may damage the receptacle and/or the module.

f. Apply power to the AIM 65 and to the mating RM 65 Bus motherboard.

Removing the Cable Driver Adapter/Buffer

a. Turn off power to the AIM 65 and to the RM 65 Bus motherboard.

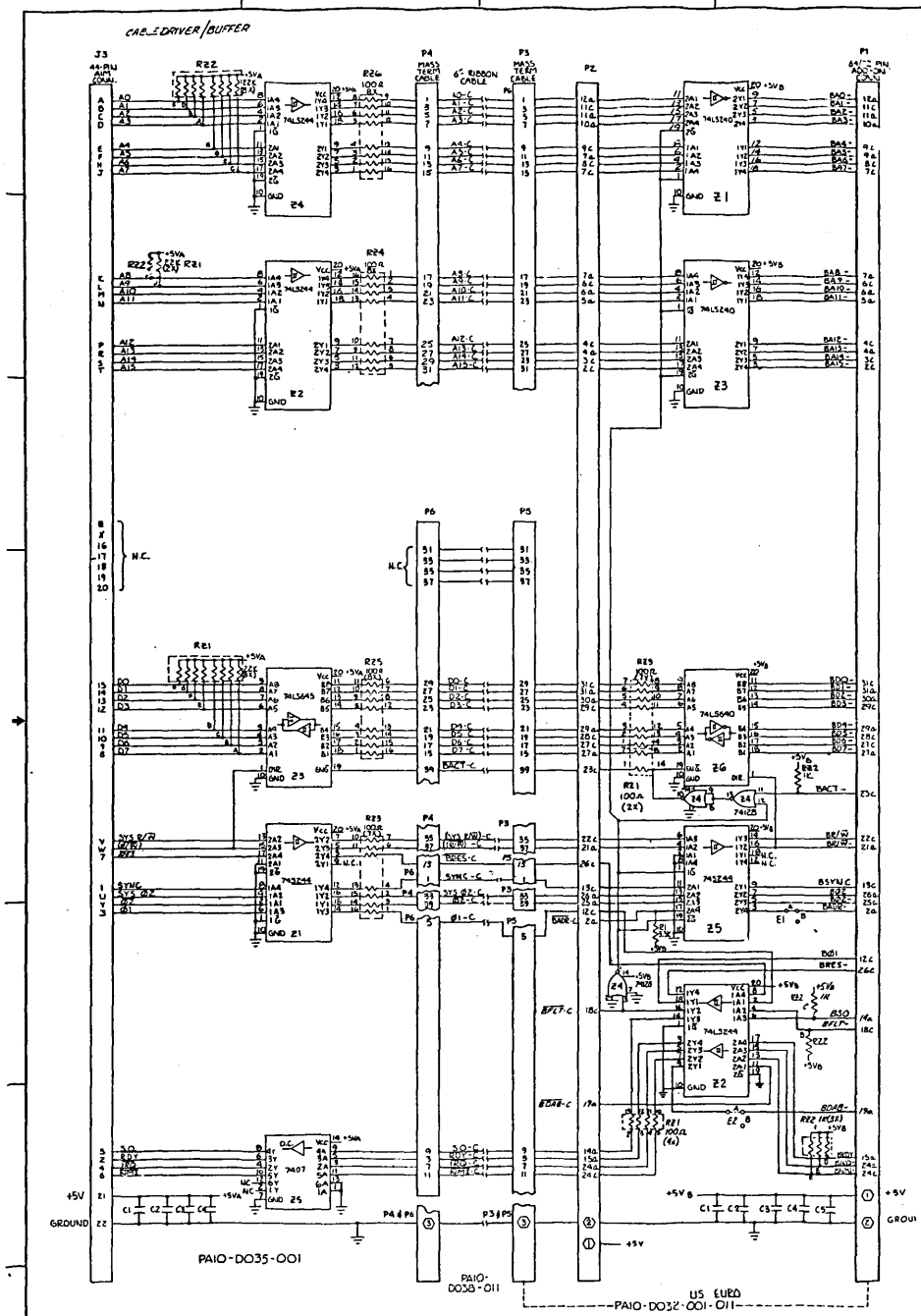
b. Lift up on the Buffer module ejector tab to release the module from the mating RM 65 Bus receptacle. Pull the module straight back until it is free from the card slot guides.

c. Pull back on the Cable Driver module while moving it slightly from side to side until it is free from the AIM 65 Expansion Connector.

Buffer Module to RM 65 Bus Connector Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
	Not Connected (See Note)		Wa	Wc		Not Connected (See Note)	
+5V	+5 Vdc Line (See Note)		Xa	Xc	+5V	+5 Vdc (See Note)	
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	O	2a	2c	BA15/	Buffered Address Bit 15	O
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	O
BA13/	Buffered Address Bit 13	O	4a	4c	BA12/	Buffered Address Bit 12	O
BA11/	Buffered Address Bit 11	O	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	O	6a	6c	BA9/	Buffered Address Bit 9	O
BA8/	Buffered Address Bit 8	O	7a	7c	BA7/	Buffered Address Bit 7	O
GND	Ground		8a	8c	BA6/	Buffered Address Bit 6	O
BA5/	Buffered Address Bit 5	O	9a	9c	BA4/	Buffered Address Bit 4	O
BA3/	Buffered Address Bit 3	O	10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	O	11a	11c	BA1/	Buffered Address Bit 1	O
BA0/	Buffered Address Bit 0	O	12a	12c	BØ1	Buffered Phase 1 Clock	O
GND	Ground		13a	13c	BSYNC	Buffered Sync	O
BSO	Buffered Set Overflow	I	14a	14c	BDRQ1/	*Buffered DMA Request 1	
BRDY	Buffered Ready	I	15a	15c	GND	Ground	
	*User Spare 1		16a	16c	-12V/-V	*-12 Vdc/-V	
+12V/+V	*+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	Buffered Bus Float	I
BDMT/	Buffered DMA Terminate		19a	19c	BØ0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/$\overline{W}$/	Buffered Read/Write "Not"	O	21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/$\overline{W}$	Buffered Read/Write	O
GND	Ground		23a	23c	BACT/	Buffered Bus Active	I
BIRQ/	Buffered Interrupt Request	I	24a	24c	BNMI/	Buffered Non-Maskable Interrupt	I
BØ2/	Buffered Phase 2 "Not" Clock	O	25a	25c	GND	Ground	
BØ2	Buffered Phase 2 Clock	O	26a	26c	BRES/	Buffered Reset	O
BD7/	Buffered Data Bit 7	I/O	27a	27c	BD6/	Buffered Data Bit 6	I/O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	I/O
BD4/	Buffered Data Bit 4	I/O	29a	29c	BD3/	Buffered Data Bit 3	I/O
BD2/	Buffered Data Bit 2	I/O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	I/O	31a	31c	BD0/	Buffered Data Bit 0	I/O
+5V	+5 Vdc		32a	32c	GND	Ground	
+5V	+5 Vdc (See Note)		Ya	Yc	+5V	+5 Vdc (See Note)	
	Not Connected (See Note)		Za	Zc		Not Connected (See Note)	

NOTE
Pins Wa, Wc, Xa, Xc, Ya, Yc, Za, Zc are not used on the Eurocard version.
*Not used on this module.


CABLE DRIVER/BUFFER
PA10-D035-001
PA10-D038-011
US EURO
PA10-D032-001-011

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

NOTE: UNLESS OTHERWISE SPECIFIED

1. PINS 1C, 32a ON EURO CONNECTOR AND PINS Xa, Xc, Ya, Yc, 1C, 32a ON U.S. CONNECTOR SHALL BE TIED TO +5V
2. PINS 1a, 3a, 5c, 8a, 10c, 13a, 15c, 18a, 20c, 23a, 25c, 28a, 30c, 32a, SHALL BE TIED TO GND.
3. ALL EVEN NUMBER PINS (2 THRU 40) SHALL BE TIED TO GND.
4. ALL CAPACITORS ARE .10UF ±20%, 50V.

QTY REQD	QTY REQD	QTY REQD	QTY REQD	QTY REQD	MEAS UNIT	ITEM NO.	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS .XX = ± .03 .XXX = ± .010 ANGLES ± 30'	AUTHORIZATION NO.	ROCKWELL INTERNATIONAL CORPORATION ELECTRONIC DEVICES DIVISION — MICROELECTRONIC DEVICES [illegible] MIRALOMA AVE., ANAHEIM, CA [illegible]
MATERIAL:	DR BY CHK BY [signature] 6/24/80 APPD BY [signature] 6/25/80 APPD BY	SCHEMATIC-ASSY CABLE DRIVER / BUFFER 16 SLOT CARD CAGE
HEAT TREAT		SIZE E · CODE IDENT NO. 34576 · DRAWING NO. PAIO-XO31
FINISH		SCALE NONE · — · SHEET

DASH NO.	NEXT ASSY	USED ON
APPLICATION		

PAIO-XO31

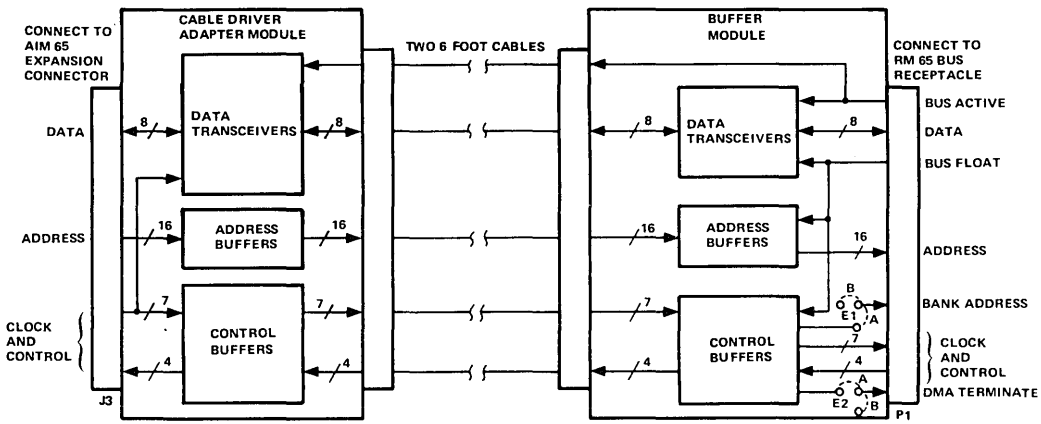
RM65 BOARD PRODUCTS

Cable Driver Adapter Module to AIM 65 Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
SYNC	SYNC	I	1	A	A0	Address Bit 0	I
RDY	Ready	O	2	B	A1	Address Bit 1	I
Ø1	Phase 1 Clock	I	3	C	A2	Address Bit 2	I
$\overline{IRQ}$	Interrupt Request	O	4	D	A3	Address Bit 3	I
S.O.	Set Overflow	O	5	E	A4	Address Bit 4	I
$\overline{NMI}$	Non-Maskable Interrupt	O	6	F	A5	Address Bit 5	I
$\overline{RES}$	Reset	O	7	H	A6	Address Bit 6	I
D7	Data Bit 7	I/O	8	J	A7	Address Bit 7	I
D6	Data Bit 6	I/O	9	K	A8	Address Bit 8	I
D5	Data Bit 5	I/O	10	L	A9	Address Bit 9	I
D4	Data Bit 4	I/O	11	M	A10	Address Bit 10	I
D3	Data Bit 3	I/O	12	N	A11	Address Bit 11	I
D2	Data Bit 2	I/O	13	P	A12	Address Bit 12	I
D1	Data Bit 1	I/O	14	R	A13	Address Bit 13	I
D0	Data Bit 0	I/O	15	S	A14	Address Bit 14	I
-12V	*-12 Vdc		16	T	A15	Address Bit 15	I
+12V	*+12 Vdc		17	U	SYS Ø2	System Phase 2 Clock	I
$\overline{CS8}$	*Chip Select 8		18	V	SYS R/$\overline{W}$	System Read/Write	I
$\overline{CS9}$	*Chip Select 9		19	W	R/$\overline{W}$	Read/Write "Not"	I
$\overline{CSA}$	*Chip Select A		20	X	TEST	*Test	
+5V	+5 Vdc		21	Y	$\overline{Ø2}$	Phase 2 Clock "Not"	I
GND	Ground		22	Z	RAM R/$\overline{W}$	*RAM Read/Write	

NOTE:

* = Not used on this module.



Cable Driver Adapter/Buffer Block Diagram

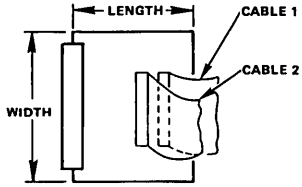
Cable Driver Adapter/Buffer Physical and Electrical Characteristics

Characteristics	Value	
Dimension (See Notes)		
Cable Driver Adapter Module		
Width	4.4 in. (111 mm)	
Length	5 in. (127 mm)	
Height	0.56 in. (14 mm)	
Buffer Module	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	1.0 lb (450 g)	
Power		
Cable Driver Adapter Module	+5V ±5% 30 mA (0.15W) – Typical 275 mA (0.25W) – Maximum	
Buffer Module	+5V ±5% 190 mA (0.95W) – Typical 330 mA (1.7W) – Maximum	
Environment		
Operating Temperature	$0^{o}C$ to $70^{o}C$	
Storage Temperature	$-40^{o}C$ to $85^{o}C$	
Relative Humidity	0% to 85% (without condensation)	
Propagation Time	50 ns – Maximum	
Interface Connectors		
AIM 65 Expansion Connector	22/44 – edge receptacle (0.156 in. centers)	
RM 65 Bus		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not installed)	
Interface Cables		
Number of Cables	Two	
Cable Length	6 feet	
Type	Flat ribbon	
Number of conductors per cable	40	
Wire Size	#28 AWG	

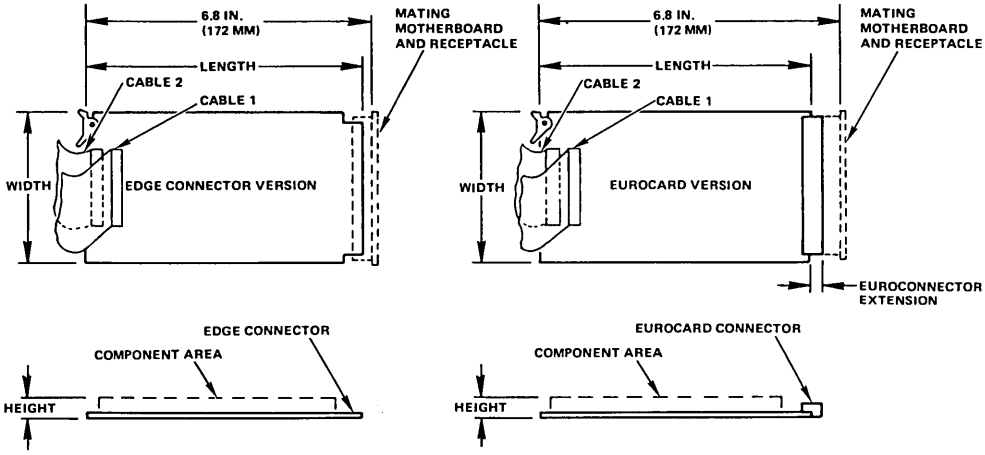
NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.)
2. The length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. The Eurocard dimensions conform to DIN 41612.

CABLE DRIVER ADAPTER MODULE



BUFFER MODULE



Module Dimensions

PART NUMBER
RM65-7201(E)

Rockwell

RM 65
DATA SHEET

DESIGN PROTOTYPING MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems.can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

The Design Prototyping Module is available in an Edge Connector version (RM65-7201) and a Eurocard version (RM65-7201E).

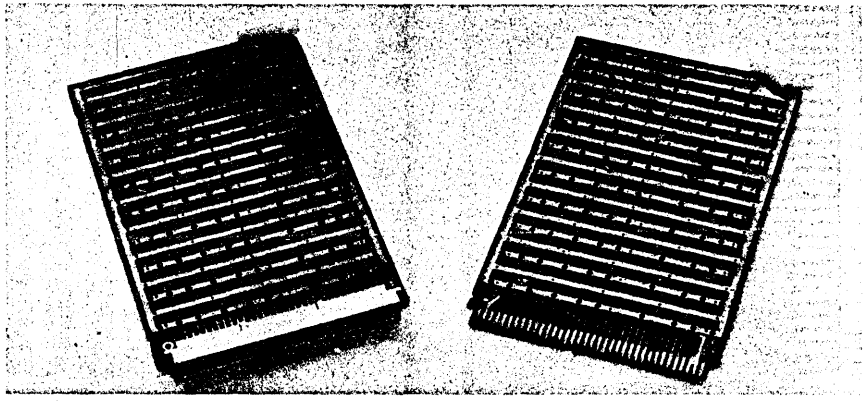
FEATURES

- Compact size — approximately 4" x 6¼" (100 mm x 160 mm)
- Provision for mounting mass-terminated cable connectors
- All wire-wrap holes pre-drilled on 0.100 in. centers
- Provision for installing decoupling capacitors
- Spacing for 0.300, 0.400 and 0.600 in. wide components
- +5V and ground extended throughout the module
- Isolated power strips allow connection to other supply voltages
- Edge Connector and Eurocard versions

PRODUCT OVERVIEW

The Design Prototyping Module allows you to develop custom application circuits for installation in any RM 65 motherboard.

Power and return lines are prerouted throughout the module. Plated-through holes, spaced beside the power lines, permit wire-wrap sockets to be installed. The hole pattern allows manual or automatic wire-wrapping. The holes at the I/O end of the module accept a variety of wire-wrap flat ribbon cable connectors. Additional pre-drilled holes permit mounting of decoupling capacitors.



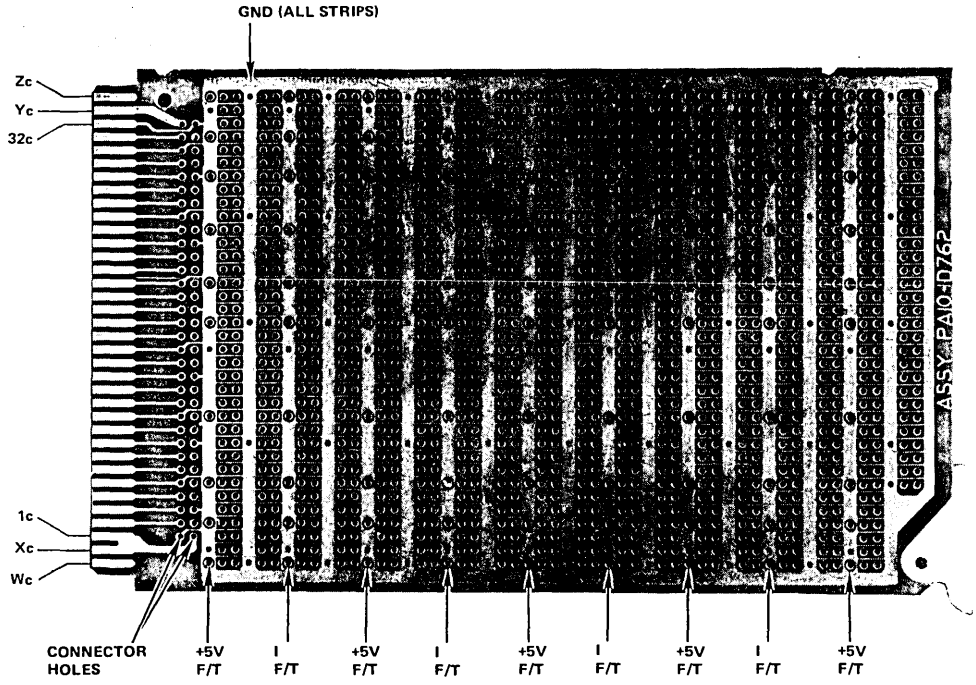
Eurocard Version
RM65-7201E

Edge Connector Version
RM65-7201

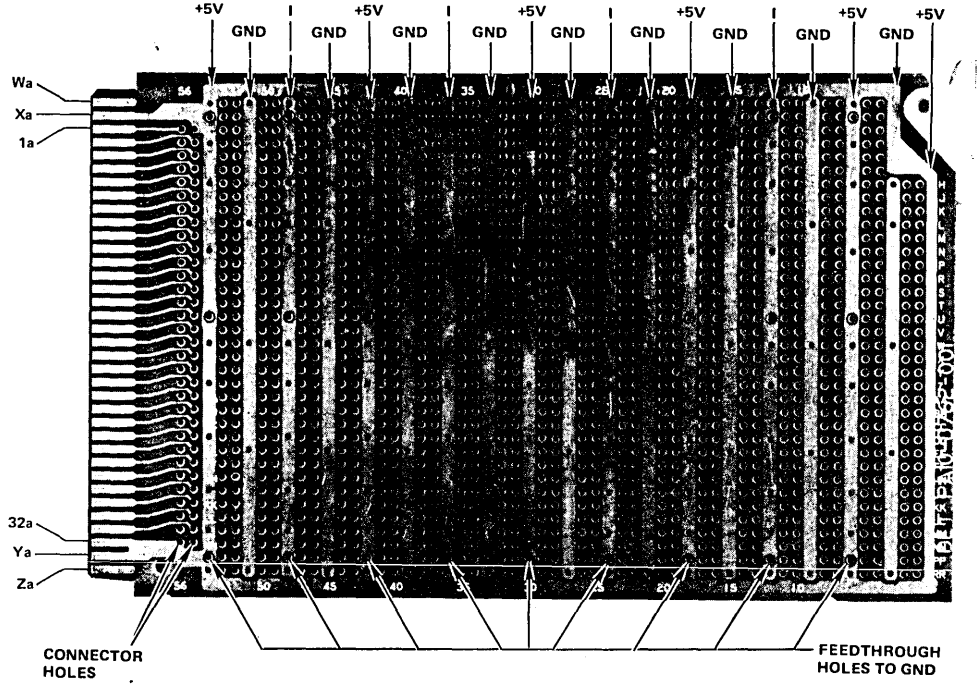
DESIGN PROTOTYPING MODULE

RM65 BOARD PRODUCTS

Specifications subject to change without notice
Document No. RMA65 N06
Rev. 2, March 1981



Design Prototyping Module — Edge Connector (Component Side)



I = ISOLATED POWER STRIPS

F/T = FEEDTHROUGH HOLES

Design Prototyping Module — Edge Connector (Wirewrap Side)

RM 65 Bus Connector Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	Buffered Sync
BSO	Buffered Set Overflow	14a	14c	BDRQ1/	Buffered DMA Request 1
BRDY	Buffered Ready	15a	15c	GND	Ground
	User Spare 1	16a	16c	-12V/-V	-12 Vdc/-V
+12V/+V	+12 Vdc/+V	17a	17c		User Spare 2
GND	Ground Line	18a	18c	BFLT/	Buffered Bus Float
BDMT/	Buffered DMA Terminate	19a	19c	BØ0	Buffered External Phase 0 Clock
	User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	Buffered DMA Request 2
	System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE
Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

INSTALLATION

1. Solder jumpers between the isolated power strips and the power (+5V, +12V/+V, or -12V/-V) traces as required.

CAUTION

Before proceeding, ensure that the power strips are not shorted to GND.

2. Solder power filter capacitors as required between the power strips and GND.

3. Install and wire components on the Design Prototype Module:

   a. Insert wire-wrap sockets into the desired holes. Solder two pins (on opposite ends of the socket) to the associated feed-through to hold the socket in place.

   b. Insert the solder stakes for mounting of discrete components, power connection and test points into the desired holes and solder to the associated feedthroughs.

   c. Insert and solder individual or strip stakes into connector holes for all RM 65 bus signals used on the module.

   d. Wire wrap wires between the protruding pins and other pins or power/GND traces as required.

4. Double check the hookup to ensure proper connection.

CAUTION

Ensure that no power lines are shorted to GND before installation into the RM 65 bus. Shorting power to ground may damage your circuitry, module, power supply and/or interfacing modules unless proper current limiting protection is provided.

5. Install components into sockets as required.

6. Remove power from the RM 65 bus.

CAUTION

Never install or remove modules with power on — it may cause damage to your module and/or host system.

7. Insert the module in the RM 65 Bus motherboard or single card adapter receptacle.

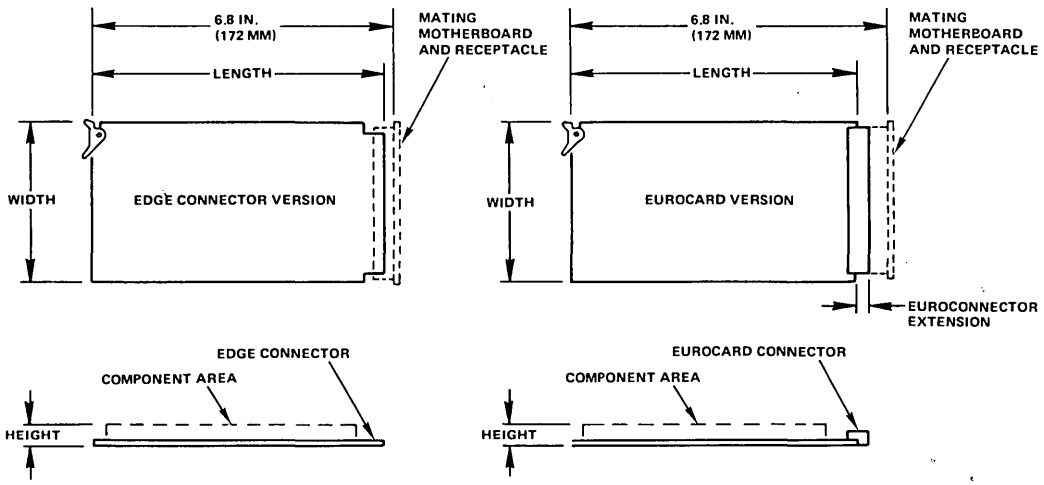
8. Apply power to the RM 65 bus.

Design Prototyping Module Physical and Electrical Characteristics

Characteristic	Value	
Physical Characteristics (See Notes):	Edge Connector Version	Eurocard Version
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.06 in. (1.6 mm)	0.56 in. (14 mm)
Weight	2.0 oz. (55 g)	2.5 oz. (65 g)
RM 65 Bus Interface		
Edge Connector	72-pin edge connector (0.100 in. centers)	
Eurocard	64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not installed)	
Component Mounting Area:		
Number of Component Hole Columns:	36	
Number of Component Hole Rows:	36	
Number of +5V power strips:	6	
Number of isolated power strips:	4	
Number of ground strips:	9	
Vertical hole spacing:	0.100 in.	
Horizontal hole spacing:	0.100 in.	

NOTES:

1. The height includes the maximum values for component height above the board suface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include the added extensions due to the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

PART NUMBER
RM65-7211(E)

Rockwell

RM 65
DATA SHEET

EXTENDER MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable, or desktop microcomputer applications.

ORDERING INFORMATION

The Extender Module is available in an Edge Connector version (RM65-7211) and a Eurocard version (RM65-7211E).

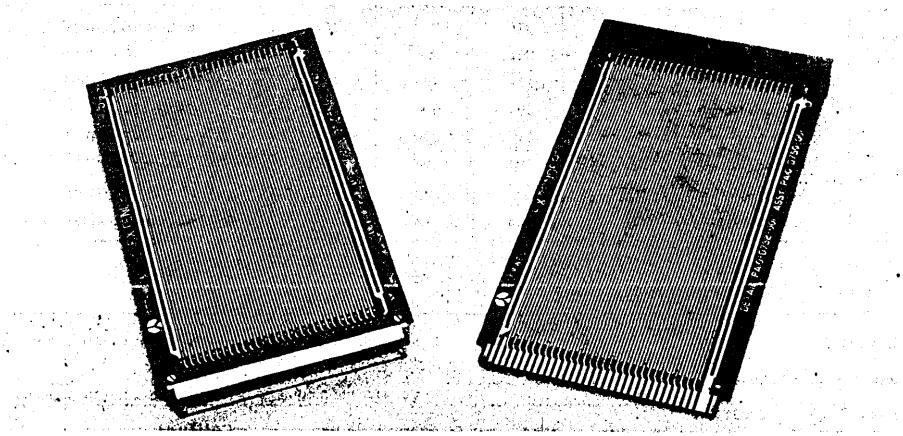
FEATURES

- Extends all RM 65 Bus Lines
- Terminals for GND and +5V
- Edge and Eurocard Connector versions
- Assembled, tested and warranted

PRODUCT OVERVIEW

The RM 65 Extender Module physically extends a module that is electrically connected to an RM 65 motherboard. This simplifies signal tracing and troubleshooting by providing access to the module outside of its card cage or enclosure.

The RM 65 Extender Module consists of a series of bus lines connecting the RM 65 connector plug on one end, to an RM 65 compatible connector receptacle on the other end. The lines are connected pin-for-pin between the plug and receptacle.



Eurocard Version
RM65-7211E

Edge Connector Version
RM65-7211

RM65 BOARD PRODUCTS

EXTENDER MODULE

Specifications subject to change without notice
Document No. RMA65 N07
Rev. 1, March 1981

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	Buffered Sync
BSO	Buffered Set Overflow	14a	14c	BDRQ1/	Buffered DMA Request 1
BRDY	Buffered Ready	15a	15c	GND	Ground
	User Spare 1	16a	16c	-12V/-V	-12 Vdc/-V
+12V/+V	+12 Vdc/+V	17a	17c		User Spare 2
GND	Ground Line	18a	18c	BFLT/	Buffered Bus Float
BDMT/	Buffered DMA Terminate	19a	19c	BØ0	Buffered External Phase 0 Clock
	User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	Buffered DMA Request 2
	System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE
Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

INSTALLATION

1. Turn power off to the RM 65 bus.

CAUTION

Never install or remove modules with power on — it may cause damage to the host system or the modules being connected or disconnected.

2. Remove module to be extended from the RM 65 card cage (if present).
3. Insert the Extender Module in a vacant card slot in the card cage and connect it to the motherboard.
4. Connect the module to be extended to J1 of the Extender Module.

CAUTION

Be sure the extended module is properly supported to prevent damage to the module and/or the Extender Module.

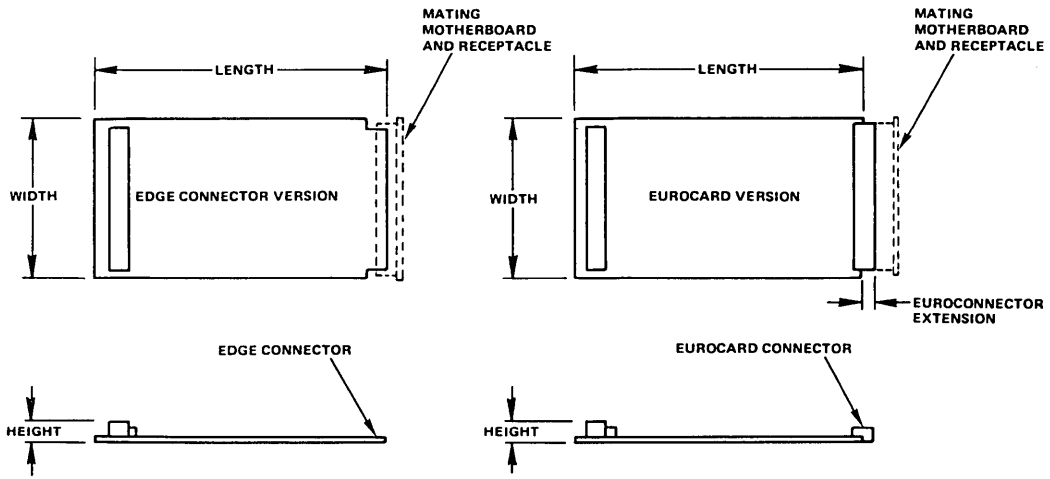
5. Apply power to the RM 65 bus.

Extender Module Physical and Electrical Characteristics

Characteristics	Value	
Physical Characteristics (see Notes)	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	7.3 in. (184 mm)	7.4 in. (187 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
	3.2 oz (90 g)	3.2 oz (90 g)
RM 65 Bus Interface:		
Edge Connector	72-pin edge connector (0.100 in. centers)	
Eurocard	64 pin plug (0.100 in. centers) per DIN 41612 (Row b is not used)	
RM 65 Module Interface:		
Edge Connector	72-pin plug (0.100 in. centers)	
Eurocard	64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not used)	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include the added extension due to the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

PART NUMBER
RM65-7004(E)

Rockwell

RM 65
DATA SHEET

4- SLOT PIGGYBACK MODULE STACK (PMS)

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

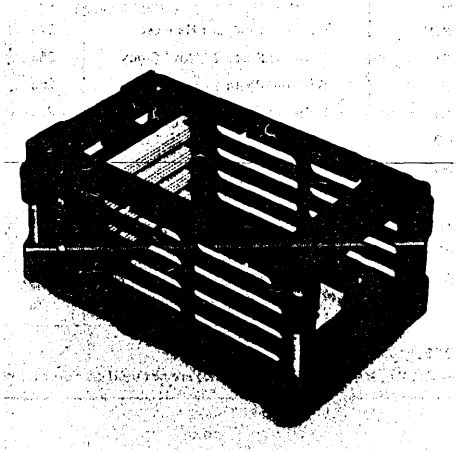
The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A set of card cages allows a broad variety of packaging options. RM 65 products may also be used with Rockwell's AIM 65 Advanced Interactive Microcomputer for product development and desktop microcomputer applications.

FEATURES

- 4-slot card cage with integral module guides
- Rugged, but lightweight construction
- Accepts axial module cooling fan
- Screw-down terminals for connecting external power (+5V, +12V/+V, -12V/-V, GND)
- Predrilled holes for various mounting configura - tions.
- Assembled, tested and warranted.

PRODUCT OVERVIEW

The 4-slot Piggyback Module Stack (PMS) consists of a 4-slot RM 65 Bus compatible motherboard in a card cage. Memory, I/O or special functions may be added to AIM 65 by use of the PMS. When connected to the AIM 65 through the Buffer/Adapter Module, the PMS may be mounted over, under, or behind the AIM 65 in a variety of orientations to meet unique application requirements. The form factor of the PMS allows low profile placement in a table top or terminal style enclosure.



ORDERING INFORMATION

Rockwell offers all RM 65 modules in both Edge Connector and Eurocard versions. If you plan to use Edge Connector modules, order the RM65-7004 model of the Piggyback Module Stack. Conversely, if you plan to use Eurocard modules, order the RM65-7004E model of the Piggyback Module Stack.

Specifications subject to change without notice
Document No. RMA65 N05
Rev. 1, March 1981

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	Buffered Sync
BSO	Buffered Set Overflow	14a	14c	BDRQ1/	Buffered DMA Request 1
BRDY	Buffered Ready	15a	15c	GND	Ground
	User Spare 1	16a	16c	-12V/-V	-12 Vdc/-V
+12V/+V	+12 Vdc/+V	17a	17c		User Spare 2
GND	Ground Line	18a	18c	BFLT/	Buffered Bus Float
BDMT/	Buffered DMA Terminate	19a	19c	BØ0	Buffered External Phase 0 Clock
	User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	Buffered DMA Request 2
	System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

INSTALLATION

1. Connect power to TB1. The power lines should be long enough to allow the PMS to be oriented and positioned as required.

WARNING

Ensure that the external power supplies are turned off before connecting to TB-1.

a. Connect +5V from an external power supply to the terminal marked "+5". "+5" is connected to all +5V pins on all module receptacles.

b. Connect GND from the power supply to either terminal marked "G". Both of these terminals are connected to all GND pins on all module receptacles.

c. Connect +12V/+V from an external power supply to the terminal marked "+V". "+V" is connected to Pin 17a on each module receptacle.

d. Connect GND from the +12V/+V power supply to either "G" terminal.

e. Connect -12V/-V from an external power supply to the terminal marked "-V". "-V" is connected to Pin 16c on each module receptacle.

f. Connect GND from the -12V/-V power supply to either "G" terminal.

2. Install the PMS in the desired position. Mounting holes are provided to allow attachment at the top or bottom of the PMS.

CAUTION

Ensure that neither the left nor right side of the PMS is blocked such that the flow of forced cooling air is impeded.

NOTE

If the PMS is positioned on the AIM 65 Master Module, ensure that the PMS feet rest in areas free of components.

3. Attach an axial cooling fan to the left side of the PMS. Connect the cooling fan power leads to the required power supply.

4. To install a module in the PMS:

CAUTION

Ensure that power is turned off to the PMS motherboard before installing a module.

a. Position the module, component side up, in front of the desired card slot.

Card slot No. 1 (top-most slot) has 0.85 inch of component clearance whereas the other three slots are on 0.6 inch centers. If a module is higher than 0.4 inches above the surface of the module, install it in card slot No. 1.

b. Insert the module into the card guide and slide the module straight in until it touches the mating motherboard receptacle.

NOTE

The card slot guides may be snug on the inserted module.

c. Ensure that the module connector is positioned properly against the mating receptacle.

d. Press in firmly on the exposed edge of the module until it is firmly seated.

5. To remove a module from the PMS:

CAUTION

Remove power from the PMS motherboard before removing a module.

a. Lift up on the module ejector tab, if installed; otherwise grasp the exposed edge of the module and pull, to release the module from the mating receptacle.

b. Pull the module straight back until it is free from the card slot guides.

RECOMMENDED 3-5/8" COOLING FANS

ETRI Inc
(704) 289-5423

- Model 760-99XW-182-11115*
  115 VAC, 50/60 Hz, 6 watts
  2500 RPM, 30 CFM
  10 oz.
- Model 760-99XW-181-11220*
  220 VAC, 50/60 Hz, 6 watts
  2500 RPM, 30 CFM
  10 oz.

*Requires plug-in power cord, 30" long Model 760-9601-6.

ROTRON Inc
(914) 657-6661

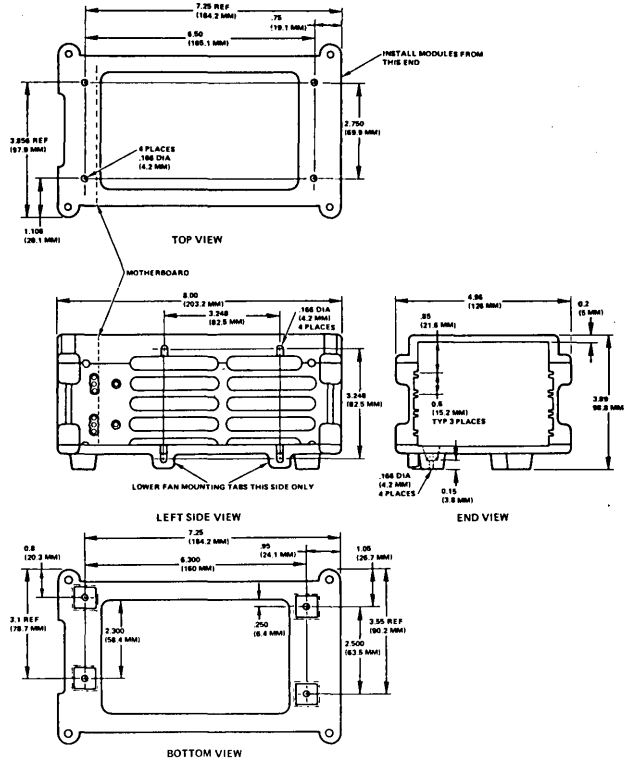
- Model WA2F79**
  115 VAC, 50/60 Hz, 13 watts
  3000 RPM, 33 CFM
  9 oz.
- Model WA2F77**
  220 VAC, 50/60 Hz, 13 watts
  3000 RPM, 33 CFM
  9 oz.

**Includes two 6" power leads.

NOTE

ETRI Finger guard Model 760-9901-43 may be used with any of the above fans.

CHARACTERISTICS	VALUE
Outer Dimensions:	
Width	4.96 in. (126 mm)
Length	8.00 in. (203 mm)
Height	3.89 in. (99 mm)
Module Separation:	
Slot 1: Center line to Inside Top Cover	0.85 in. (22 mm)
Other Slots: Centerline to Centerline	0.6 in. (15 mm)
Weight	13 oz. (370 g)



PART NUMBER
RM65-7008(E)

Rockwell

RM 65
DATA SHEET

8-SLOT CARD CAGE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

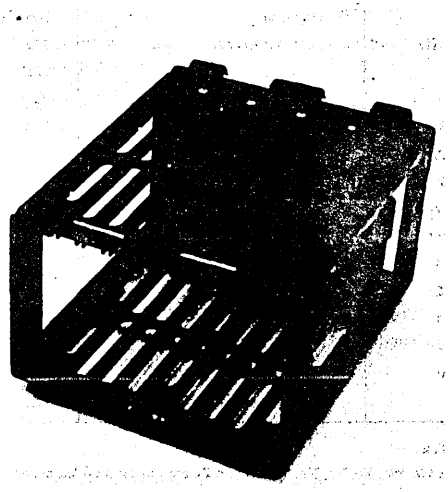
The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A set of card cages allows a broad variety of packaging options. RM 65 products may also be used with Rockwell's AIM 65 Advanced Interactive Microcomputer for product development and desktop microcomputer applications.

FEATURES

- 8-slot card cage with integral module guides
- Rugged, but lightweight construction
- Accepts axial module cooling fan
- Screw-down terminals for connecting external power (+5V, +12V/+V, -12V/-V, GND)
- Predrilled holes for various mounting configurations
- Assembled, tested and warranted
- Removable jumpers on motherboard support ±12V as well as ±V.

PRODUCT OVERVIEW

The 8-slot card cage consists of an 8-slot RM 65 Bus compatible motherboard in a card cage. Memory, I/O or special functions may be added to AIM 65 by use of the 8-slot card cage. When connected to the AIM 65 through the Buffer/Adapter Module, the card cage may be mounted over, under, or behind the AIM 65 in a variety of orientations to meet unique application requirements. The form factor of the 8-slot card cage allows low profile placement in a table top or terminal style enclosure.



ORDERING INFORMATION

Rockwell offers all RM 65 modules in both Edge Connector and Eurocard versions. If you plan to use Edge Connector modules, order the RM65-7008 model of the 8-card cage. Conversely, if you plan to use Eurocard modules, order the RM65-7008E model of the 8-slot card cage.

Specifications subject to change without notice
Document No. RMA65 N09
Rev. 1, March 1981

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	Buffered Sync
BSO	Buffered Set Overflow	14a	14c	BDRQ1/	Buffered DMA Request 1
BRDY	Buffered Ready	15a	15c	GND	Ground
	User Spare 1	16a	16c	-12V/-V	-12 Vdc/-V
+12V/+V	+12 Vdc/+V	17a	17c		User Spare 2
GND	Ground Line	18a	18c	BFLT/	Buffered Bus Float
BDMT/	Buffered DMA Terminate	19a	19c	BØ0	Buffered External Phase 0 Clock
	User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	Buffered DMA Request 2
	System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

INSTALLATION

1. Connect power to TB1 and/or TB2. The power lines should be long enough to allow the card cage to be oriented and positioned as required.

WARNING

Ensure that the external power supplies are turned off before connecting to TB-1 or TB-2.

a. Connect +5V from an external power supply to either terminal marked "+5". "+5" is connected to all +5V pins on all module receptacles.

b. Connect GND from the power supply to either terminal marked "G". Both of these terminals are connected to all GND pins on all module receptacles.

c. Connect +12V/+V from an external power supply to the terminal marked "+V". "+V" is connected to Pin 17a on each module receptacle.

NOTES

1. If both +12V and +V (e.g., +15V) are required, remove the soldered jumper corresponding to pin 17a between receptacle 3 and 4 on the soldered side of the motherboard. Connect +12V to TB1 if three or less modules require +12V, or to TB2 if more than three modules require +12V. Connect +V to the other terminal strip.
2. If the jumper has been removed and only one voltage is required (i.e., +12V or +V), connect the power lead to both TB1 and TB2.

d. Connect GND from the +12V/+V power supply to either "G" terminal.

e. Connect -12V/-V from an external power supply to the terminal marked "-V". "-V" is connected to Pin 16c on each module receptacle.

NOTES

1. If both -12V and -V (e.g., -15V) are required, remove the soldered jumper corresponding to pin 16c between receptacle 3 and 4 on the soldered side of the motherboard. Connect -12V to TB1 if three or less modules require -12V or to TB2 if more than three modules require -12V. Connect -V to the other terminal strip.
2. If the jumper has been removed and only one voltage is required (i.e., -12V or -V) connect the power lead to both TB1 and TB2.

f. Connect GND from the -12V/-V power supply to either "G" terminal.

2. Install the card cage in the desired position. Mounting holes are provided to allow attachment at the top or bottom of the card cage.

CAUTION

Ensure that neither the left nor right side of the card cage is blocked such that the flow of forced cooling air is impeded.

3. To install a module in the card cage:

CAUTION

Ensure that power is turned off to the card cage motherboard before installing a module.

a. Position the module, component side facing TB1 end, in front of the desired card slot.

Card slot No. 1 (slot closest to TB1) has 0.85 inch of component clearance whereas the other seven slots are 0.6 inch centers. If a module is higher than 0.4 inch above the surface of the module, install it in card slot No. 1.

CAUTION

If ±12V and ±V have been connected to different terminal strips (TB1 or TB2), ensure that any modules requiring ±12V or ±V are installed in the slots corresponding to the proper voltage.

b. Insert the module into the card guide and slide the module straight in until it touches the mating motherboard receptacle.

NOTE

The card slot guides may be snug on the inserted module.

c. Ensure that the module connector is positioned properly against the mating receptacle.

CAUTION

A key is installed in each edge connector receptacle between pin 5 and pin 6. Forcing an edge connector module without a corresponding slot in the plug may damage the receptacle and/or the module.

d. Press in firmly on the exposed edge of the module until it is firmly seated.

4. To remove a module from the card cage:

CAUTION

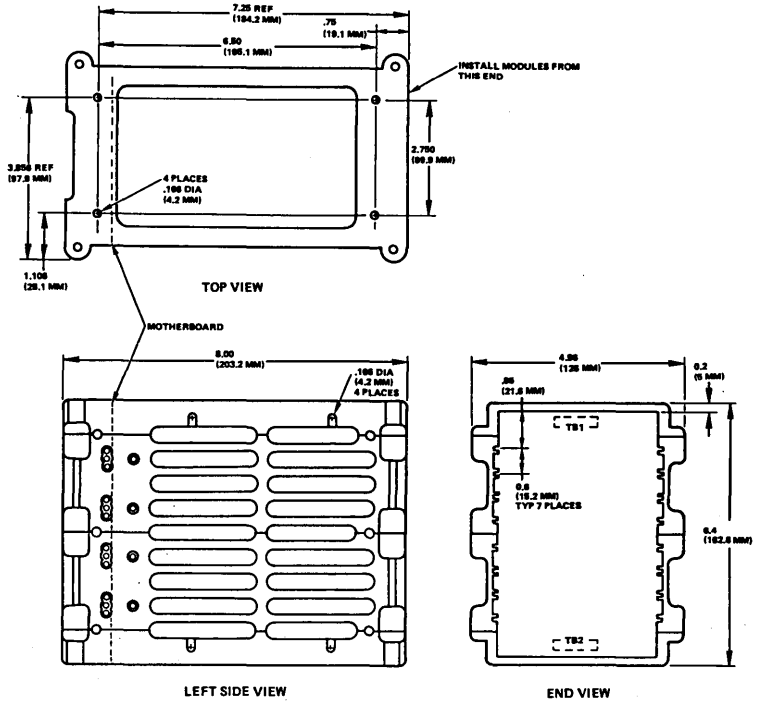
Remove power from the card cage motherboard before removing a module.

a. Lift up on the module ejector tab, if installed; otherwise grasp the exposed edge of the module and pull, to release the module from the mating receptacle.

b. Pull the module straight back until it is free from the card slot guides.

Module Specification Table

Characteristics	Value
Outer Dimensions	
Width	4.96 in. (126 mm)
Length	8.00 in. (203 mm)
Height	6.40 in. (162.6 mm)
Module Separation:	
Slot 1: Center line to Inside Top Cover	0.85 in. (22 mm)
Other Slots: Centerline to Centerline	0.6 in. (15 mm)
Weight	1 lb. 6 oz. (624 g)



PART NUMBER
RM65-7016(E)

Rockwell

RM 65
DATA SHEET

16-SLOT CARD CAGE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

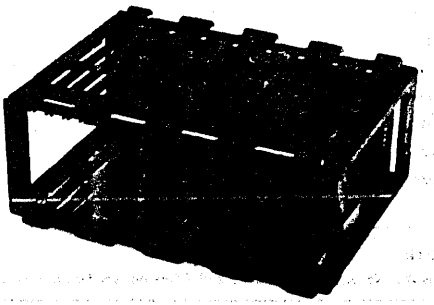
The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A set of card cages allows a broad variety of packaging options. RM 65 products may also be used with Rockwell's AIM 65 Advanced Interactive Microcomputer for product development and desktop microcomputer applications.

FEATURES

- 16-slot card cage with integral module guides
- Rugged, yet lightweight construction
- Screw-down terminals for connecting external power (+5V, +12V/+V, -12V/-V, GND)
- Predrilled holes for various mounting configurations
- Assembled, tested and warranted
- Removable jumpers on motherboard support ±12V as well as ±V.

PRODUCT OVERVIEW

The 16-slot card cage consists of a 16-slot RM 65 Bus compatible motherboard in a card cage. Memory, I/O or special functions may be added to AIM 65 by use of the 16-slot card cage. When connected to the AIM 65 through the Adapter/Buffer, the card cage may be mounted over, under, or behind the AIM 65 in a variety of orientations to meet unique application requirements. The form factor of the 16-slot card cage allows low profile placement in a table top or terminal style enclosure.



ORDERING INFORMATION

Rockwell offers all RM 65 modules in both Edge Connector and Eurocard versions. If you plan to use Edge Connector modules, order the RM65-7016 model of the card cage. Conversely, if you plan to use Eurocard modules, order the RM65-7016E model of the card cage.

Specifications subject to change without notice
Document No. RMA65 N18
April 1981

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	**Signal Name**	**Pin**	**Pin**	**Signal Mnemonic**	**Signal Name**
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	Buffered Sync
BSO	Buffered Set Overflow	14a	14c	BDRQ1/	Buffered DMA Request 1
BRDY	Buffered Ready	15a	15c	GND	Ground
	User Spare 1	16a	16c	-12V/-V	-12 Vdc/-V
+12V/+V	+12 Vdc/+V	17a	17c		User Spare 2
GND	Ground Line	18a	18c	BFLT/	Buffered Bus Float
BDMT/	Buffered DMA Terminate	19a	19c	BØ0	Buffered External Phase 0 Clock
	User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	Buffered DMA Request 2
	System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

INSTALLATION

1. Connect power to TB1 and/or TB2. The power lines should be long enough to allow the card cage to be oriented and positioned as required.

WARNING

Ensure that the external power supplies are turned off before connecting to TB-1 or TB-2.

a. Connect +5V from an external power supply to either terminal marked "+5". "+5" is connected to all +5V pins on all module receptacles.

b. Connect GND from the power supply to either terminal marked "G". Both of these terminals are connected to all GND pins on all module receptacles.

c. Connect +12V/+V from an external power supply to the terminal marked "+V". "+V" is connected to Pin 17a on each module receptacle.

NOTES

1. If both +12V and +V (e.g., +15V) are required, remove the soldered jumper corresponding to pin 17a between receptacle 6 and 7 on the soldered side of the motherboard. Connect +12V to TB1 if six or less modules require +12V, or to TB2 if more than six modules require +12V. Connect +V to the other terminal strip.
2. If the jumper has been removed and only one voltage is required (i.e., +12V or +V), connect the power lead to both TB1 and TB2.

d. Connect GND from the +12V/+V power supply to either "G" terminal.

e. Connect -12V/-V from an external power supply to the terminal marked "-V". "-V" is connected to Pin 16c on each module receptacle.

NOTES

1. If both -12V and -V (e.g., -15V) are required, remove the soldered jumper corresponding to pin 16c between receptacle 6 and 7 on the soldered side of the motherboard. Connect -12V to TB1 if six or less modules require -12V or to TB2 if more than six modules require -12V. Connect -V to the other terminal strip.
2. If the jumper has been removed and only one voltage is required (i.e., -12V or -V) connect the power lead to both TB1 and TB2.

f. Connect GND from the -12V/-V power supply to either "G" terminal.

2. Install the card cage in the desired position. Mounting holes are provided to allow attachment at the top or bottom of the card cage.

CAUTION

Ensure that adequate cooling is provided to keep the temperature of the installed modules within specified operating limits.

3. To install a module in the card cage:

CAUTION

Ensure that power is turned off to the card cage motherboard before installing a module.

a. Position the module, component side facing TB1 end, in front of the desired card slot.

Card slot No. 1 (slot closest to TB1) has 0.85 inch of component clearance whereas the other fifteen slots are 0.6 inch centers. If a module is higher than 0.4 inch above the surface of the module, install it in card slot No. 1.

CAUTION

If ±12V and ±V have been connected to different terminal strips (TB1 or TB2), ensure that any modules requiring ±12V or ±V are installed in the slots corresponding t the proper voltage.

b. Insert the module into the card guide and slide the module straight in until it touches the mating motherboard receptacle.

NOTE

The card slot guides may be snug on the inserted module.

c. Ensure that the module connector is positioned properly against the mating receptacle.

CAUTION

A key is installed in each edge connector receptacle between pin 5 and pin 6. Forcing an edge connector module without a corresponding slot in the plug may damage the receptacle and/or the module.

d. Press in firmly on the exposed edge of the module until it is firmly seated.

4. To remove a module from the card cage:

CAUTION

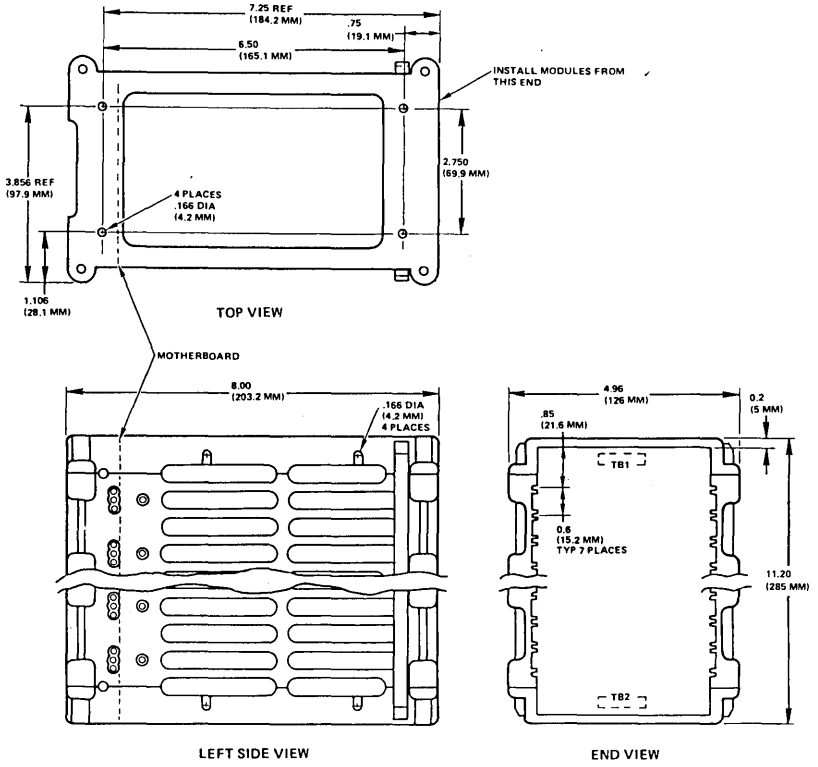
Remove power from the card cage motherboard before removing a module.

a. Lift up on the module ejector tab, if installed; otherwise grasp the exposed edge of the module and pull, to release the module from the mating receptacle.

b. Pull the module straight back until it is free from the card slot guides.

Module Specification Table

Characteristics	Value
Outer Dimensions	
Width	4.96 in. (126 mm)
Length	8.00 in. (203 mm)
Height	11.20 in. (285 mm)
Module Separation:	
Slot 1: Center line to Inside Top Cover	0.85 in. (22 mm)
Other Slots: Centerline to Centerline	0.6 in. (15 mm)
Weight	2 lb. 10 oz. (1.20 kg)



SYSTEM 65
DEVELOPMENT
SYSTEM

SYSTEM 65
DEVELOPMENT
SYSTEM

Rockwell
Rockwell
Rockwell
Rockwell
Rockwell
Rockwell
Rockwell
Rockwell

The Third-Generation
R6500 Microcomputer System
Puts the Economics on Your Side . . .
Rockwell Adds
Solid Development Support

with the

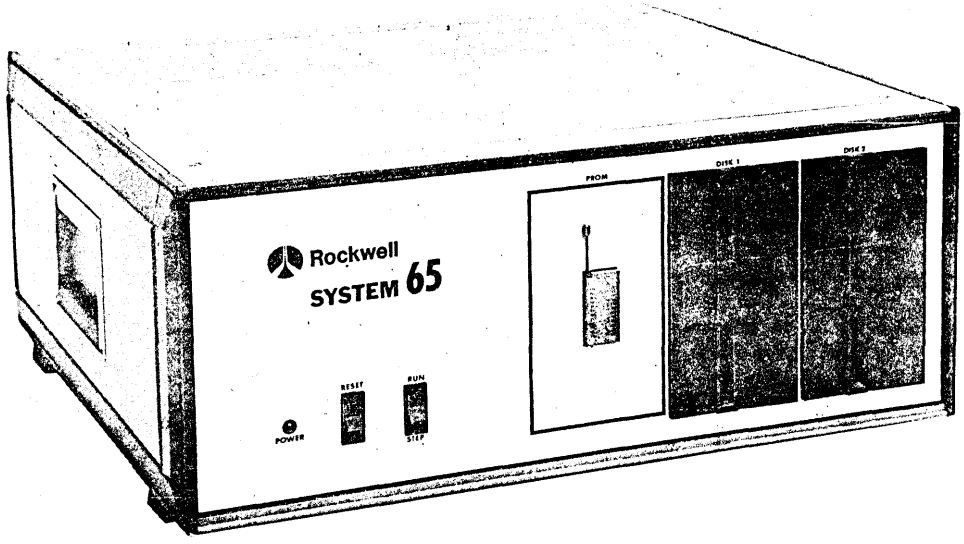
SYSTEM65

SYSTEM 65 DEVELOPMENT SYSTEM

MICROCOMPUTER DEVELOPMENT SYSTEM

Rockwell
Rockwell
Rockwell
Rockwell
Rockwell
Rockwell
Rockwell

Printed in the U.S.A.



SYSTEM 65 has been designed by Rockwell to meet all of the development needs of the R6500 Microcomputer System.

Rockwell

SYSTEM65

Rockwell

Rockwell

We Think It's More Practical than Any Other Microcomputer Development System . . . And with a Disk Operating System at Under $5500, You Know the Price is Right . . .

Rockwell has included in the SYSTEM 65 every design requirement we've encountered in our long microprocessor experience. (We've been selling microprocessors since 1972, and most industry analysts rate us among the technology's leaders.)

We designed SYSTEM 65 around Rockwell's powerful R6502 CPU. We included two mini-floppy disk drives and a 16K byte static NMOS RAM memory for your software. And we didn't cheat you out of any of this program storage. Our line-oriented, symbolic Text Editor with character and string functions, and our two-pass Assembler and symbolic Debug/Monitor Package are totally stored in ROM. The disk and RAM storage is yours to use.

We made our system software commands easy to use — they're initiated with a single keystroke and they automatically send back meaningful prompts if any additional information is required.

From intimate knowledge of the interfacing requirements Designers encounter during microcomputer development, we included RS-232C and current loop interfaces to accept serial input terminals with operating speeds of between 110 baud and 9600 baud. We added an 8-bit parallel port to permit automatic interfacing to high-speed printers. And because we know how the imaginations of Designers grow as they work with a microcomputer system as versatile as the R6500, we provided six vacant slots in the SYSTEM 65 chassis so that system memory and I/O capability can be expanded at will.

Rockwell

Here's a Summary of Reasons Why SYSTEM 65 is Just What You're Looking For . . .

- Rockwell R6502 microprocessor (CPU) operates at 1 MHz or (optionally) 2 MHz, and has 65K byte addressing and multi-level interrupts.
- Dual, user-dedicated mini-floppy disk drives. Each drive has a 60-file, 78K byte storage capacity
  User-dedicated 16K byte static RAM memory, expandable in 16K byte increments
- Integral power supply
- System firmware resides in static ROM, fast operation with no loading or reloading required
  - — Symbolic Text Editor performs line, string and character editing functions
  - — Two-pass Assembler can accept source input from either RAM memory or disk and direct object output to any system device
  - — Symbolic Debug/Monitor package operates in single step or real-time
- Eight software breakpoints, for debugging
- Hardware breakpoint on any fetch, read or write to a specified memory location. Scope sync pulse on rear panel connector with each occurance of hardware breakpoint, for real-time debugging.
- Individual RS-232C and current loop interfaces support serial input terminals from 110 baud to 9600 baud
- 8-bit parallel port provides automatic support of high-speed printers for hard copy
- Six vacant circuit board slots tied to system bus, for memory and I/O expansion

Rockwell's optional USER 65 (User System EvaluatoR) module allows . . .
the full power of the SYSTEM 65 to be extended into the user's system. By removing the R6500 CPU from the user system and connecting the USER 65 cable into the CPU socket, the SYSTEM 65 Debug firmware can be used to test and troubleshoot microprocessor systems.

Here Are the SYSTEM 65's Hardware Details

The SYSTEM 65 enclosure contains four printed circuit modules:

- CPU Module holds the R6502 microprocessor and its supporting circuits, and serial baud rate select switch
- Monitor Module contains 1K bytes of static RAM and 14K bytes of static ROM, which holds all system software
- RAM Memory Module contains 16K bytes of user-dedicated static RAM
- I/O Module provides the hardware interface to the system input/output devices

Note that since all RAM memory is static, the processor is not required to provide the clock and strobe functions associated with dynamic memory.

The SYSTEM 65 enclosure also has six vacant slots, which allow users to add any combination of memory and I/O interfaces in building a customized development system.

The built-in mini-floppy disk drives can each hold up to 60 files with a per drive storage capacity of 78K bytes. Like the RAM memory, the mini-floppy disk drives are 100% user-dedicated.

The RUN/STEP switch on the front panel allows you to select either single step execution or real-time execution of programs.

The back panel has four device connectors: an 8-bit parallel port for connecting a high-speed printer, an RS-232C serial interface connector, a current loop serial interface connector and a scope sync connector. The CPU Module has a rotary switch to select any of eight baud rates — 110, 150, 300, 600, 1200, 2400, 4800 or 9600 baud — for compatability with the serial input/output device.

And Rockwell offers these options to SYSTEM 65:

- PL/65 High-Level Language
- USER 65 in-circuit emulation option
- PROM Programmer Module, for programming a 2704/2708/2716/2758 PROM device from the front panel socket
- R6500/1 Personality option, for developing with the R6500/1 single-chip microcomputer
- 16K x 8 Static RAM Modules
- PROM/ROM Module, accepts 2316/2332 ROM or 2708/2716/2758 PROM devices
- Wire-wrap Design Prototyping Module
- Extender Card for circuit probing

Here Are the SYSTEM 65's Software Details

The Text Editor

The SYSTEM 65 Text Editor is used to prepare user programs for assembly. The Text Editor writes the program source code into RAM memory from any system device and, when editing has been completed, writes it to any system device. The editing operation can include line editing, string editing and character editing.

The line-oriented commands provide overall control in finding lines to be edited, and specify the system devices for input and output of text. The string-oriented commands can be used to insert program source code into memory, or to search for an existing character string — perhaps a program label or a certain opcode/operand combination — and (if desired) provide a substitute for that string. The character-oriented commands provide control over the cursor position on a line and a character delete command.

Text Editor Command Summary

Line-Oriented Commands

R - Read lines into text buffer from [device]
I - Insert one line from system terminal
K - Delete [count] lines of text, starting with current line
U - Backspace [count] lines of text
D - Advance [count] lines of text
T - Go to top (beginning) line of text; i.e., re-enter Text Editor
B - Go to bottom (last) line of text
L - List [count] lines on [output device]
? - Show address of current and last lines
G - Go to line [number]
(sp) - Show current line

String-Oriented Commands

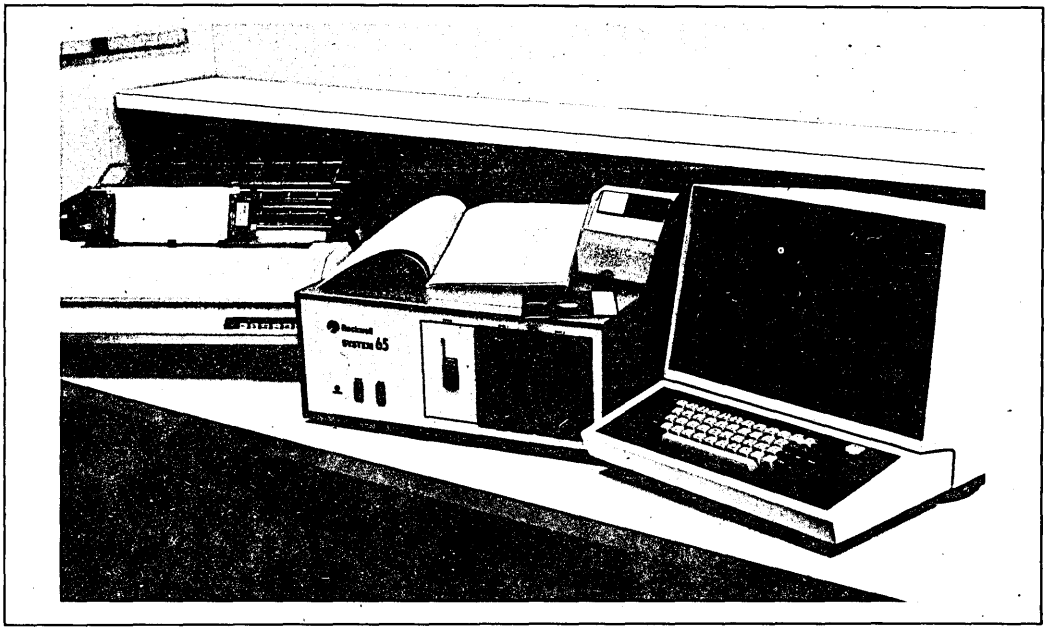
F - Find [string], starting with current line
C - Find [string], starting with current line, and change it to [string]
A - Add [string] to line, starting with current cursor position

Character-Oriented Commands

/ - Delete current character
+ - Advance cursor [count] positions
– - Backspace cursor [count] positions

Miscellaneous

Q - Exit to Debug



The Assembler

The SYSTEM 65 Assembler is a two-pass assembler that includes the option to list only the errors detected, if any. This "errors-only" option generates a display of all source statements that contain syntax errors, unresolved references and the like. With the results of this quick check, the Text Editor can be used to make the proper corrections before the Assembler generates the full assembly listing, symbol table and object code. The "errors-only" option can prove to be quite a time- and paper-saver.

The Assembler can accept input from either RAM memory or disk, and has a powerful chaining feature that allows multiple disk files of a large program to be assembled in one operation. These files may reside on either disk, or even on a disk that has not been mounted (the Assembler will direct you to mount it).

For output, the Assembler gives the user complete control over the extent of the listing, which system device will receive the output and whether the entire text of ASCII strings is to be output.

The Debug/Monitor Package

The SYSTEM 65 Debug/Monitor package provides a comprehensive set of easy-to-use commands and functions for debugging development programs in either single step or real-time mode.

The register commands allow you to display the current contents of the Processor registers, and to selectively alter any of these registers.

The memory commands allow you to display the contents of memory in blocks of eight locations, to alter one or more consecutive locations and to write protect any 8K block of addresses in memory. Further, memory can be loaded from or output to any system device.

Debug also has a compliment of breakpoints, to give you an easy way to trace program execution. Upon encountering a breakpoint the program displays a symbolic disassembly of the label (if any), opcode and operand field at the breakpoint location. This important feature ties the symbol table, created by the Assembler, with the Debug software. This means that all debugging is done at the assembler language level — without the need to plod through machine code printouts. There are eight software breakpoints and one hardware breakpoint (in addition to the BRK instruction in the R6500 instruction set).

The Debug command set includes all the commands necessary to set and clear software breakpoints, as well as to enable and disable them.

Debug also makes disk management virtually transparent, reducing functions like initializing, compressing, opening and deleting files to single keystroke commands.

Debug/Monitor Command Summary

Invoke Assembler/Editor
E - Enter Text Editor
T - Re-enter Text Editor, to edit current source
N - Invoke Assembler

Display/Alter Registers
R - Display registers (Program Counter, Accumulator, X, Y, Status and Stack Pointer)
* - Alter Program Counter to [address]
A - Alter Accumulator to [byte]
X - Alter X Register to [byte]
Y - Alter Y Register to [byte]
P - Alter Processor Status to [byte]
S - Alter Stack Pointer to [byte]

Display/Alter Memory
M - Display eight memory locations, starting with [address]
(sp) - Display next eight memory locations
/ - Alter current memory locations, starting with [address]
W - Display/alter write protect status

Load/Dump Memory
L - Load object code into memory from [input device]
D - Dump memory from [address] to [address[to [output device]

Manipulate Breakpoints
- Clear all software breakpoints
4 - Toggle software breakpoint enable on/off
B - Set/clear software breakpoint addresses
? - Display software breakpoint addresses
C - Display/alter hardware breakpoint

Control Execution/Trap
G - Execute user's program, at currect Program Counter address
Z - Toggle instruction trace mode on/off
V - Toggle register printout on trapping on/off
J - Print register header
H - Display trace history stack, 10 addresses

Disk Functions
1 - Special disk functions (compress, list, rename, recover, initialize)
2 - List disk directory
3 - Delete file

Program Development — The Easy SYSTEM 65 Way

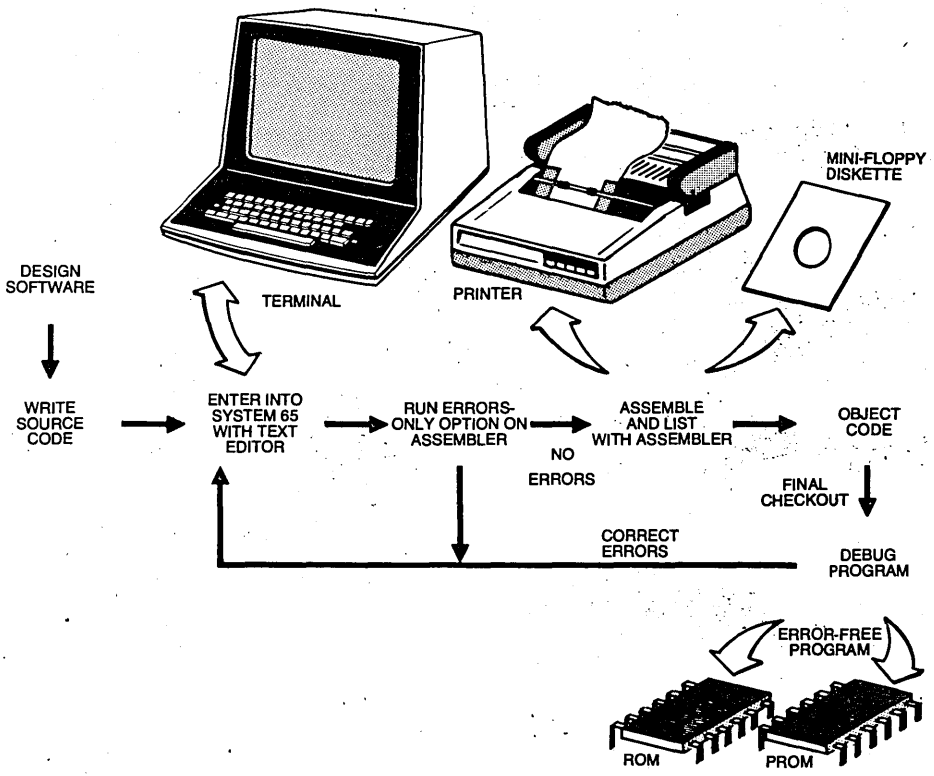
SYSTEM 65 means productivity by making your program development easy from start to finish. The flowchart at the right shows you how it's done.

After designing the program and writing the source code, you will be using the Text Editor to enter the code into RAM memory. Like all system software, the Text Editor is resident in the system ROM, so there is no need to load it from any external source. The Text Editor is line-oriented, but also has string and character manipulation functions. It includes the capability of searching for a specified character string — for example, a label or an opcode-and-operand combination — and replacing it with a different string.

If a program is small relative to available memory (most programs will fit in the standard 16K bytes of RAM) it can remain there through the editing, assembling and debugging processes. Very large programs are usually developed in pieces, stored on disk, and later linked together by the Assembler. SYSTEM 65 is designed to permit easy communication with disk, by handling all files by their logical names and automatically creating each file when its filename is first used.

With the source code entered and edited (and if necessary stored on disk), it can now be assembled. The SYSTEM 65 resident Assembler is called by a single key stroke. The Assembler is a two-pass assembler that includes the option to list only the errors detected. This "errors-only" option is usually used as a first quick, easy check on the integrity of your program. If errors are found, they can be corrected by recalling the Text Editor.

When all errors have been eliminated, the Assembler is used to generate a full assembly listing, symbol table and object code. At this point the symbolic Debug program is used to test and correct the program. Debug may use the symbol table produced by the Assembler, so your original source code labels can be carried through to the debug process. When the program is in completed form and error-free, you can run one more assembly to generate a listing for documentation purposes. The object output can also be put on PROM via the optional PROM Programmer, or sent to Rockwell for storage on ROM.



Where to Get More on SYSTEM 65

To order SYSTEM 65, or to get a copy of the SYSTEM 65 User's Manual (nominal $5 charge), contact the nearest Rockwell office or distributor listed on the back of this brochure. For in-depth assistance, obtain the name of your nearest Rockwell sales representative from any Rockwell office.

ROCKWELL DISTRIBUTORS U.S./CANADA

ALABAMA

Hamilton/Avnet Electronics
805 Oster Drive N.W.
Huntsville, Alabama 35805
(205) 533-1170

ARIZONA

Hamilton/Avnet Electronics
2615 S. 21st Street
Phoenix, Arizona 85034
(602) 275-7851 (ext 2507)

CALIFORNIA

Hamilton Electro Sales
10912 Washington Blvd.
Culver City, California 90230
(213) 558-2020

Avnet Electronics
350 McCormick
Costa Mesa, California 92626
(714) 754-6111

Hamilton/Avnet Electronics
International Group
10950 Washington Blvd.
Culver City, California 90230
(213) 558-2441

Hamilton/Avnet Electronics
8917 Complex Drive
San Diego, California 92123
(714) 279-2421 (ext 2504)

Hamilton/Avnet Electronics
575 E. Middlefield
Mountain View, California 94040
Sales (415) 961-7000

CANADA

Hamilton/Avnet Electronics
3688 Nashua Dr. Units G&H
Mississauga, Ontario
Canada L4V 1M5
(416) 677-7432

Hamilton/Avnet Electronics
1735 Courtwood Crescent
Ottawa, Ontario
Canada K2C 3J2
(613) 226-1700

Hamilton/Avnet Electronics
2670 Paulus Street
St. Laurent
Montreal, Quebec
Canada H4S 1G2
(514) 331-6443

CONNECTICUT

Hamilton/Avnet Electronics
643 Danbury Road
Georgetown, Connecticut 06829
(203) 762-0361

COLORADO

Hamilton/Avnet Electronics
5921 N. Broadway
Denver, Colorado 80216
(303) 534-1212

FLORIDA

Hamilton/Avnet Electronics
6800 N.W. 20th Avenue
Fort Lauderdale, Florida 33309
(303) 971-2900

GEORGIA

Hamilton/Avnet Electronics
6700 1-85 Suite 1-E
Norcross, Georgia 30071
(404) 448-0800

ILLINOIS

Hamilton/Avnet Electronics
3901 No. 25th Avenue
Schiller Park, Illinois 60176
(312) 678-6310

KANSAS

Hamilton/Avnet Electronics
9900 Pflumm Road - Suite 37
Lenexa, Kansas
(913) 888-8900

MARYLAND

Hamilton/Avnet Electronics
7235 Standard Drive
Hanover, MD. 21076
Baltimore: (301) 796-5000
Washington: (301) 953-7010

MASSACHUSETTS

Hamilton-Avnet Electronics
100 E. Commerce Way
Woburn, Massachusetts 01801
(617) 933-8000

MICHIGAN

Hamilton/Avnet Electronics
32487 Schoolcraft Rd.
Livonia, Mich. 48150
(313) 522-4700

MINNESOTA

Hamilton-Avnet Electronics
7683 Washington Avenue S.
Edina, Minnesota 55435
(612) 941-3801

MISSOURI

Hamilton-Avnet Electronics
396 Brookes Lane
Hazelwood, Missouri 63042
(314) 731-1144

NEW JERSEY

Hamilton/Avnet Electonics
218 Little Falls Road
Cedar Grove, New Jersey 07009
(201) 239-0800

Hamilton/Avnet Electronics
113 Gaither Drive
East Gate Industrial Park
Mount Laurel, New Jersey 08057
(609) 234-2133

NEW MEXICO

Hamilton/Avnet Electronics
2450 Baylor Drive S.E.
Albuquerque, New Mexico 87106
(505) 765-1500

NEW YORK

Hamilton/Avnet Electronics
5600 Joy Road
East Syracuse, New York 13057
(315) 437-2641

Hamilton/Avnet Electronics
167 Clay Road
Rochester, New York 14623
(716) 442-7820

Hamilton/Avnet Electronics
70 State Street
Westbury, L.I. New York 11590
(516) 333-5800

NORTH CAROLINA

Hamilton-Avnet Electronics
2803 Industrial Drive
Raleigh, North Carolina 27609
(919) 829-8030

OHIO

Hamilton/Avnet Electronics
76 Beta Drive - Suite E
Cleveland, Ohio 44143
(216) 461-1400

Hamilton/Avnet Electronics
954 Senate Dr.
Dayton, Ohio 45459
(513) 433-0610

TEXAS

Hamilton/Avnet Electronics
4445 Sigma Road
Dallas, Texas 75240
(214) 661-8661

Hamilton/Avnet Electronics
3939 Ann Arbor
Houston, Texas 77063
(713) 780-1771

UTAH

Hamilton/Avnet Electronics
1585 West, 2100 South
Salt Lake City, Utah 84119
(801) 972-2800

WASHINGTON

Hamilton/Avnet Electronics
13407 Northrup Way
Bellevue, Washington 98005
(206) 746-8750

WISCONSIN

Hamilton/Avnet Electronics
2975 Moriland Rd
New Berlin, WI. 53151
(414) 784-4510

EUROPE

BENELUX

Famatra
P.O. Box 721
Breda, Netherlands 4300 NL
Ginnekenweg 128
(076) 13 34 57
Telex: 54521 fatra

DENMARK

Micronor
Tindbergvej 16
DK-8600 Silkeborg
Denmark
(06) 83 62 11
Telex: 63243

FINLAND

Micronor OY
Box 22
00211 Helsinki 21
Finland
(90) 803 1965
Telex: 12-1394

FRANCE

REA
9 Rue Ernest Cognacq
92301 Levallois-Perret
France
(01) 758-11-11
Telex: 620 630 radif

ITALY

Dott. ing. G. De Mico S.P.A.
Via Manzoni 31
20121 Milano
Italy
(02) 65 31 31
Telex: 33035 demico

NORWAY

Micronor
Box 96
1321 Stabekk, Norway
(02) 54 51 30
Telex: 16101 sigpen

SPAIN

Comelta
Orense 9-5 0 Izq.
Madrid - 20, Spain
(01) 254-9831
Telex: 42007 cetae

SWITZERLAND

Aumann & Company AG
Forchstrasse 282
8029 Zurich
Switzerland
(01) 53 54 00
Telex: 56228 auco ch

UNITED KINGDOM

Pelco Electronics, Ltd.
Enterprise House
83-85 Western Road
Hove
Sussex BN 3 1JB
England
0273-722155
Telex: 87323

WEST GERMANY

System Kontakt
Siemenstrasse 5
7107 Bad Friedrichshall, Germany
07136 5031
Telex: 728563 syko

FAR EAST/AUSTRALIA

JAPAN

Matsushita Electric Trading Company
P.O. Box, 18 Trade Center
32nd Floor, World Trade Center Bldg.
4-1 Hamamatsu-cho 2-chome
Minato-ku
Tokyo 105, Japan
(03) 435-4552
Telex: J2 4647 (Matsuelo)

Matsushita Electric Trading Company
71 Kawaramachi, 5-chome
Higashi-ku
Osaka 541, Japan
(06) 204-5563
Telex: J63380

Marubeni Corporation
4-2 Ohtemachi 1-chome
Chiyoda ku
Tokyo, Japan
282-3446

Nihon Unicon, Inc.
1-12-5 Maruyama Nakano-ku
Tokyo, Japan
(03) 388-1921
Telex: 232-3130

Kyokuto Boeki Kaisha, Ltd.
Rm. 706 Mainichi Osaka Kaikan Kitakan
53, Dojima-Funadaikumachi, Kita-ku
Osaka, Japan
(06) 344-1121

Kyokuto Boeki Kaisha, Ltd.
7th Floor, New Otemachi Bldg.
2-1, 2-chome, Otemachi, Chiyoda-ku
Tokyo, Japan
(03) 244-3803

Nissho Electronics, Ltd.
Peripheral Equipment Dept.
12-22, 1 Tsukiji, Chuo-ku
Tokyo 104, Japan
(03) 355-8398

TAIWAN

Enterprex Corporation
6th Floor Huey Maw Bldg.
127-1 Sung Chiang Road
Taipei, Taiwan
538-375-7
Telex: 11732 Taipei

HONGKONG

Caduceus Ltd.
Room 1204, Hang Lung Centre
2-20 Paterson St., Causeway Bay
Hong Kong
5-770504-5
TWX: (708) 83640 CADUX HX

KOREA

Caduceus Ltd.
Sindo Bldg., Room 508
65-4, 2-Ka Chung Mu Ro
Chung-ku
Seoul, Korea
777-2325
TWX: K(787)26453 NAMSTRA

AUSTRALIA

AMPEC Engineering Company
42 The Strand
Croyden NSW 2132
P.O. Box 18
Strathfield 2135, Australia
(02) 748063
Telex: AA27136

DOCUMENT NO. 29650 N43
REV. 1, NOVEMBER 1979

PART NOs.
M65-001, M65-002

Rockwell

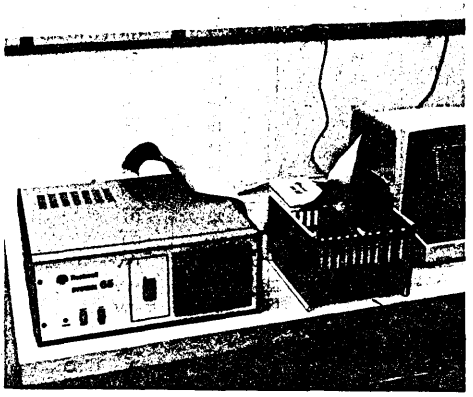
R6500 Microcomputer System
PRODUCT DESCRIPTION

USER 65 OPTION

OVERVIEW

The USER 65 permits users who are developing R6500-based products to extend the full power of SYSTEM 65 into their equipment for in-circuit emulation. Available in both 1- and 2-MHz versions (M65-001 and 002), USER 65 supports all ten R6500 CPU's.

USER 65 consists of two modules — a Host Module and a Buffer Module — and two interconnect cables. The USER 65 Host Module replaces the CPU Module in the SYSTEM 65 chassis; it performs all CPU Module functions, plus several external functions. The USER 65 Buffer Module extends the SYSTEM 65 bus lines (address, data and control) to the user equipment.



FUNCTIONAL DESCRIPTION

USER 65 HOST MODULE

The USER 65 Host Module (shown in block diagram form in Figure 1) replaces the CPU Module in the SYSTEM 65 chassis. It is capable of performing all functions of the CPU Module, plus external address selection, automatic power up, and external clock selection. The schematic of the Host Module is PS00-X183. The Host Module interface signals are listed in Table 1.

The heart of the Host Module is the R6502 (Z11) microprocessor. It controls all functions of the SYSTEM 65 and the user's external equipment. Crystal Y1 (1 or 2 MHz) generates the internal clock for the R6502 CPU. Switch S3 is used to select either the internal generated clock or an externally provided clock input.

The Host Module has automatic power-up circuit consisting of an NE555 timer (Z3) and associated discrete capacitors and resistors. This circuit will generate a 100 msec reset pulse following power-up.

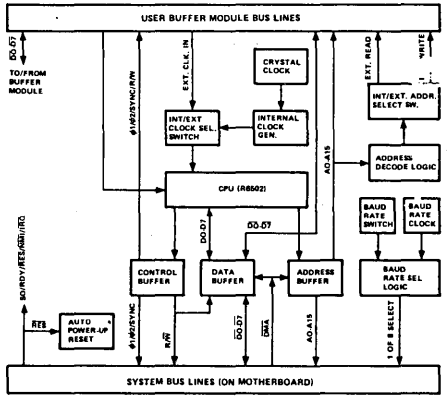


Figure 1. USER 65 Host Module Functional Block Diagram

The Host Module also contains the RS-232C and TTY baud rate generator circuitry. Crystal Y2 (1.8432 MHz) and baud rate generator MC14411 (Z13) generate a baud rate clock. The Clock rate is multiplied by 16 (x16) to provide a selectable output baud rate from 110 to 9600. Switch S4 and the SN74152 (Z12) select the baud rate. This output is then provided to the SYSTEM 65 bus to be used by the Monitor Module.

The internal/external address selection is based on a decode of A15-A12, using an SN74159N (Z1) decoder. This device has sixteen active low outputs. Each output represents a 4K address space and is selected by Switches S1 and S2. The outputs are ORed together and inverted by SN7406 (Z2). This enable signal is then gated with R/$\overline{W}$ signal to form a READ signal and a WRITE signal, which are used in the USER 65 Buffer Module.

The address lines and control lines Ø1, Ø2, $\overline{DMA}$, and SYNC are buffered with I.C.'s 8T97 (Z8-Z10, Z5). The data lines are inverted and buffered with I.C.8T26 (Z6, Z7). All of these lines are brought to the SYSTEM 65 bus and are also taken out to the USER 65 Buffer Module through series terminators (A1-A4).

The Control lines S.O., RDY, $\overline{RES}$, $\overline{NMI}$, $\overline{IRQ}$ are brought to the SYSTEM 65 bus and are also brought from the USER 65 Host Module, then buffered with open collector buffers SN7407(Z15). These inputs come only from the user's equipment; the RESET switch on the front panel will not reset the external equipment.

SYSTEM 65 bus line $\overline{DMA}$ is used to control the address and data bus lines. This line is pulled up internally with a 3K resistor. By pulling $\overline{DMA}$ low, the address, data and R/W lines are set to the float state, allowing an external board to control them for DMA operations. The $\overline{DMA}$ line does not stop the CPU — this must be done by controlling the RDY line as outlined in the R6500 Microprocessor Data Sheet (29000 D39).

Table 1. USER 65 Host Board to Buffer Board Interface Signals

Note: Even-numbered pins are connected to Ground.

CONNECTOR J1		CONNECTOR J2	
PIN	SIGNAL	PIN	SIGNAL
1	A0	1	EXT. CLOCK
3	A1	3	Ø2
5	A2	5	Ø1
7	A3	7	GATED READ
9	A4	9	GATED WRITE
11	A5	11	$\overline{D7}$
13	A6	13	$\overline{D6}$
15	A7	15	$\overline{D5}$
17	A8	17	$\overline{D4}$
19	A9	19	$\overline{D3}$
21	A10	21	$\overline{D2}$
23	A11	23	$\overline{D1}$
25	A12	25	$\overline{D0}$
27	A13	27	+5V
29	A14	29	+5V
31	A15	31	+5V
33	SYNC	33	+5V
35	R/$\overline{W}$	35	+5V
37	RDY	37	+5V
39	$\overline{RESET}$	39	+5V
41	$\overline{NMI}$		
43	$\overline{IRQ}$		
45	SO		

USER 65 BUFFER MODULE

The USER 65 Buffer Module receives the address, data and control lines from the USER 65 Host Module, buffers these signals and interfaces them to the user's equipment. Figure 2 is a block diagram. The schematic of the USER 65 Buffer Board is P500-X193.

The address lines, SYNC and R/$\overline{W}$ lines are buffered with I.C.'s 8T97 (Z1-Z3). The control lines RDY, $\overline{RES}$, $\overline{NMI}$, $\overline{IRQ}$, and S.O. are buffered with open collector I.C.'s SN7407 (Z4). The data lines are inverted and buffered with I.C.'s 8T26A (Z7 and Z8). They have series terminators of 150 ohms (Z9).

The Ø1 and Ø2 clocks are buffered by 8T97 (Z5). To use an external clock, jumper N must be installed. To use Ø1, jumper M must be installed. The DBE signal is provided for use during emulation of the R6512 CPU. This line has an internal pullup resistor of 3K. When brought low it will disable the data bus drivers.

Two other signals, READ and WRITE, are buffered by Z5. The READ signal is generated by the Host Module and is high when the R/$\overline{W}$ line is high and an external address is active. The WRITE signal, also generated by the Host Module, is high when R/$\overline{W}$ line is low and an external address is active. These two lines control the data bus buffers Z7 and Z8.

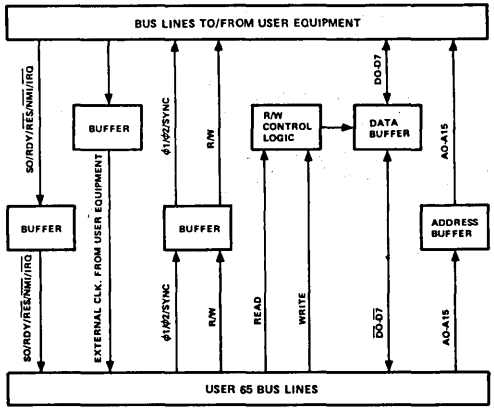


Figure 2. USER 65 Buffer Module Functional Block Diagram

USER 65 CABLES

The cable assembly supplied with the USER 65 option provides the signal paths between the USER 65 Host and Buffer Modules, and between the Buffer Module and the user's equipment. Since the USER 65 option is designed to emulate all versions of the R6500 Family of CPU's, both a 40-pin cable and two 28-pin types of cables are provided.

INSTALLATION

USER 65 HOST MODULE INSTALLATION

Install the USER 65 Host Module in the SYSTEM 65 as follows:

1. Turn SYSTEM 65 power off.

   CAUTION

   Never install or remove modules with SYSTEM 65 power on – it may cause damage to the module and/or to the system.

2. Remove the top cover of the SYSTEM 65.
3. Remove the CPU Module.
4. Set switches S1, S2, S3 and S4 on the USER 65 Host Module per Table 2. The switch positions are shown in Figure 3.
5. Plug the USER 65 Host Module into any convenient slot in the SYSTEM 65 chassis.
6. Route the cables from the Buffer Module through the back panel of SYSTEM 65, through the slot provided.
7. Connect the 40- and 50-pin cables from the Buffer Module to the top of the Host Module (the connectors are keyed with arrows).
8. Set switches S1 and S2 on the RAM Module per Tables 3 and 4 to enable/disable and to select the address range of the internal SYSTEM 65 RAM.

   NOTE

   If external RAM addresses are selected on the USER 65 and the same addresses are selected and enabled on the SYSTEM 65 internal RAM board(s), the internal RAM will override and prevent proper operation of the external RAM.

9. Install the top cover of the SYSTEM 65.

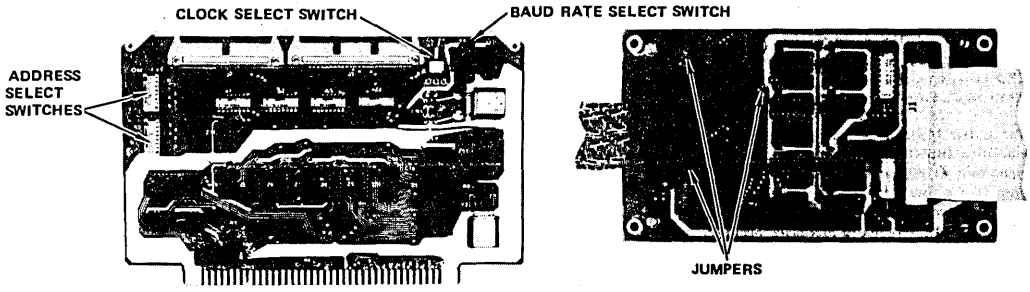


Figure 3. USER 65 Host and Buffer Modules

Table 2. USER 65 Host Module Switches

SWITCH	FUNCTION
S1/S2	ADDRESS SELECT These switches determine whether address selection is internal or external for each 4K byte portion of memory space. External memory is selected when the switch is ON, internal memory is selected when the switch is OFF. S1 Switch — Address Range 1 — $0000 - $0FFF 2 — $1000 - $1FFF 3 — $2000 - $2FFF 4 — $3000 - $3FFF 5 — $4000 - $4FFF 6 — $5000 - $5FFF 7 — $6000 - $6FFF 8 — $7000 - $7FFF S2 Switch — Address Range 1 — $8000 - $8FFF 2 — $9000 - $9FFF 3 — $A000 - $AFFF 4 — $B000 - $BFFF 5 — $C000 - $CFFF 6 — $D000 - $DFFF 7 — $E000 - $EFFF 8 — $F000 - $FFFF
S3	CLOCK SELECT Switch S3 selects either the SYSTEM 65 clock (INT) or an external, user-supplied clock (EXT). If an external supplied clock is used, the frequency must be 1 or 2 MHz + 1% if operation of the SYSTEM 65 mini-floppy disks is required. It must always be a TTL level, square wave, clock input.
S4	BAUD RATE SELECT This switch determines the baud rate for either the RS-232C or TTY ports. Switch settings are: (S4) POSITION — BAUD RATE 0 — 110 1 — 150 2 — 300 3 — 600 4 — 1200 5 — 2400 6 — 4800 7 — 9600

Table 3. RAM Module Enable/Disable Switch Definition

Switch S1/S2-4 Position	RAM Enable/Disable State
Up	RAM Disabled (Deselected)
Down	RAM Enabled (Selected)

Table 4. RAM Address Range Select Switch Settings

Switch S1/S2 Position			
-1	-2	-3	8K Address Range Selected
Up	Up	Up	$0000 - $1FFF
Down	Up	Up	$2000 - $3FFF
Up	Down	Up	$4000 - $5FFF
Down	Down	Up	$6000 - $7FFF
Up	Up	Down	$8000 - $9FFF
Down	Up	Down	$A000 - $BFFF
Up	Down	Down	$C000 - $DFFF
Down	Down	Down	$E000 - $FFFF

Note: "Up" is toward the top edge of the module

USER 65 BUFFER MODULE INSTALLATION

Since the Buffer Module is designed to support all CPU's in the R6500 family, specific jumpers or straps must be inserted to support the exact CPU being emulated. Table 5 gives the strapping requirements. Jumper locations are shown in Figure 3.

The Buffer Module has two modes for the R/W line. For 40-pin CPU emulation (R6502 and R6512), the R/W line is connected to the user's equipment as is. Since the 28-pin CPU's do not provide all the address lines to the user's equipment, address conflicts can occur during SYSTEM 65 Monitor execution. A gated R/W line is provided to prevent these conflicts; this line is normally high, and goes low only when an external address is present and R/W is low.

The Buffer Module also has straps for clock selection. One strap allows the Ø1 (OUT) signal to go to the user's equipment. The other strap is used to allow an external clock [Ø0 (IN) or Ø2 (IN)] to be used. Switch S3 on the Host Module must be set to EXT when the external clock is used.

The Buffer Module is provided with three sockets and three cables. The 40-pin socket (J3) should be used for either of the 40-pin CPU's, R6502 or R6512. The cable labeled PS00-D603-001 should be used to connect from J3 to the user's equipment. The other two sockets (J4 and J5) are for use with the 28-pin CPU's. Table 5 correlates the socket and 28-pin cable to be used for each of the 28-pin CPU versions.

The DBE (Data Bus Enable) line for the R6512 is available to the user's equipment. There is an internal 3K pullup resistor in the Buffer Module, so it can be left open if desired. To disable the data output drivers, pull the DBE line low.

The installation procedure is:

1. Remove the top of the USER 65 Buffer Module assembly.
2. Insert the desired jumpers, per Table 5.
3. Connect either the 40-pin cable to plug J3 or the 28-pin cable to plug J4 or J5, as appropriate.
4. Reinstall the top of the Buffer Module assembly.
5. Plug the free connector of the cable into the user's equipment.

NOTE

Any conductive foam must be removed from the CPU plug pins to allow proper SYSTEM 65 operation even when the CPU plug is not connected to user equipment.

6. Turn SYSTEM 65 and user's equipment power on.

Table 5. USER 65 Buffer Module Connection Requirements

User Equipment CPU	Buffer Module Socket	Cable To User Equipment	Jumper	Signal	User's CPU Pin
R6502	J3	PS00-D603-001	R	R/W	34
			M	Ø1 (OUT)	3
			N*	Ø0 (IN)	37
R6503	J4	PS00-D605-001	P	R/W	26
			B	$\overline{RES}$	1
			D	VSS	2
			E	$\overline{IRQ}$	3
			F	$\overline{NMI}$	4
			A	Ø2 (OUT)	28
			N*	Ø0 (IN)	27
R6504	J5	PS00-D605-001	P	R/W	26
			B	$\overline{RES}$	1
			D	VSS	2
			E	$\overline{IRQ}$	3
			A	Ø2 (OUT)	28
			N*	Ø0 (IN)	27
R6506	J4	PS00-D605-001	P	R/W	26
			B	$\overline{RES}$	1
			D	VSS	2
			K	RDY	3
			S	$\overline{IRQ}$	4
			A	Ø2 (OUT)	28
			N*	Ø0 (IN)	27
R6506	J4	PS00-D605-001	P	R/W	26
			B	$\overline{RES}$	1
			D	VSS	2
			L	Ø1 (OUT)	3
			S	$\overline{IRQ}$	4
			A	Ø2 (OUT)	28
			M	Ø1 (OUT)	3
			N*	Ø0 (IN)	27
R6507	J5	PS00-D605-001	P	R/W	26
			B	$\overline{RES}$	1
			D	VSS	2
			K	RDY	3
			A	Ø2 (OUT)	28
			N*	Ø0 (IN)	27
R6512	J3	PS00-D603-001	R	R/W	34
			N*	Ø2 (IN)	37
R6513	J4	PS00-D604-001	P	R/W	26
			C	VSS	1
			E	$\overline{IRQ}$	3
			F	$\overline{NMI}$	4
			T	$\overline{RES}$	28
			N*	Ø2 (IN)	27
R6514	J5	PS00-D604-001	P	R/W	26
			C	VSS	1
			E	$\overline{IRQ}$	3
			T	RES	28
			N*	Ø2 (IN)	27
R6515	J4	PS00-D604-001	P	R/W	26
			C	VSS	1
			J	RDY	2
			L		
			S	$\overline{IRQ}$	4
			T	$\overline{RES}$	28
			N*	Ø2 (IN)	27

*Jumper N is required with an external clock. Switch S3 on the USER 65 Host Module must be positioned to the EXT position when the extended clock or frequency reference is used.

USER 65 TYPICAL APPLICATION

A typical application for the USER 65 option is depicted in Figure 4.

The user's system may include any combination of ROM's, PROM's, RAM's, I/O devices, and a 40- or 28-pin CPU socket. For emulation purposes, the USER 65 option is installed in the CPU socket instead of a CPU. The user must provide page 0($0000-$00FF) and page 1($0100-$01FF) either internally or externally for use by the SYSTEM 65 Monitor. For system development purposes, the user's ROM may be emulated with one or more RAM modules provided in the SYSTEM 65 chassis. This permits easy manipulation, debugging, and reassembly of the user's program during the development phase. For editing and assembling of the source program, the user may use the SYSTEM 65 RAM or may provide his own RAM modules externally.

The USER 65 option may be used with the SYSTEM 65 Monitor enabled or disabled. With SYSTEM 65 Monitor enabled, the full resources of the SYSTEM 65 Monitor are available for program checkout and debugging. In this mode the SYSTEM 65 uses addresses $C000-$FFFF; these addresses cannot be used by the programmer.

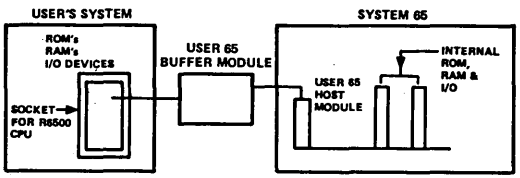


Figure 4. USER 65 Option Hook-up

USER 65 HOST AND BUFFER MODULE SPECIFICATIONS

Common Specifications

Operating Frequency: 1 MHz or 2 MHz

Operating Temperature: 0^{o} to $70^{o}C$

Power Requirements: +5 VDC ± 5% @ 1.5A

Host Module Specifications

Module Dimensions: 9.75 in. wide x 7.50 in. high

Edge Contacts: 86 pins on 0.156 in. centers

Edge Contact Signals: SYSTEM 65 compatible

Buffer Module Specifications

Module Dimensions: 4.125 in. wide x 7.375 in. high

Cable Lengths:

To	SYSTEM 65	60 in.
To	User Equipment	12 in.

SYSTEM 65
DEVELOPMENT
SYSTEM

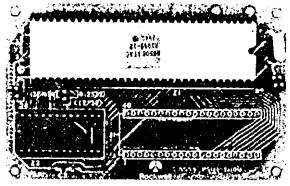
DOCUMENT NO. 29650 N59
REV. 1, MAY 1980

PART NUMBER
M65-089

Rockwell

R6500 Microcomputer System
PRODUCT DESCRIPTION

R6500/1 EVALUATION MODULE



INTRODUCTION

The R6500/1 Evaluation Module allows a computer program developed for R6500/1 Single Chip Microcomputer to be executed in a stand-alone manner using the R6500/1EAC Emulator Device and an associated PROM. With this capability, the computer program can be validated before being masked into the R6500/1 ROM.

The R6500/1 Evaluation Module consists of:

- An R6500/1 Emulator Board containing:
  - — One R6500/1EAC Emulator Device
  - — One 2-MHz crystal
  - — One 7404 Hex Inverter
  - — Seven jumper positions
  - — One 24-pin socket for a PROM
- A 40-conductor ribbon cable terminated at each end with a 40-pin connector

REFERENCE DOCUMENTS

R6500/1 One-Chip Microcomputer Data Sheet, 29000 D51
R6500/1E Emulator Device Data Supplement, 29000 D51S
R6500/1 One-Chip Microcomputer Product Description, 29650 N48

Document 29000 D51S describes operational differences between the R6500/1 Microcomputer and the R6500/1E Emulator Device.

INSTALLATION PROCEDURE

CAUTION

Ensure power is disconnected from the R6500/1 socket in the user circuit before connecting the R6500/1 Evaluation Module or damage may occur to the user circuit and/or the R6500/1 Evaluation Module.

1. Plug the PROM containing the R6500/1E program into socket Z2 while carefully observing the Pin 1 position. Any of the following PROMs (or compatible equivalents) may be used:

PROM	NO. OF BYTES	INSTALLED ADDRESS RANGE
Intel 2716	2K	$800-$FFF
TI TMS2516	2K	$800-$FFF
Intel 2732	4K	$400-$FFF*
TI TMS2532	4K	$400-$FFF*

*Addresses $400-$FFF may be used only with the R6500/1E and are not available in the R6500/1 ROM. Note that only the upper 3K bytes of a 4K-byte PROM may be used.

2. Install the jumpers as follows:

a. Jumpers D and E—Clock Select

Jumpers D and E select the desired crystal or clock configuration.

FREQUENCY REFERENCE	JUMPER D	JUMPER E
R6500/1 Emulator Module Crystal	OUT	OUT
User Circuit Crystal*	IN	IN
User Circuit Clock*	IN	OUT

*Disconnect Crystal Y1 from the R6500/1E Emulator Device by unsoldering the crystal leads from posts E1 and E2. Users who install a 4MHz crystal must use a PROM with an access time less than 225 ns.

b. Jumpers A, B, C, F, and G—PROM Select

Jumpers A, B, C, F and G configure the Emulator Module to operate with the desired PROM.

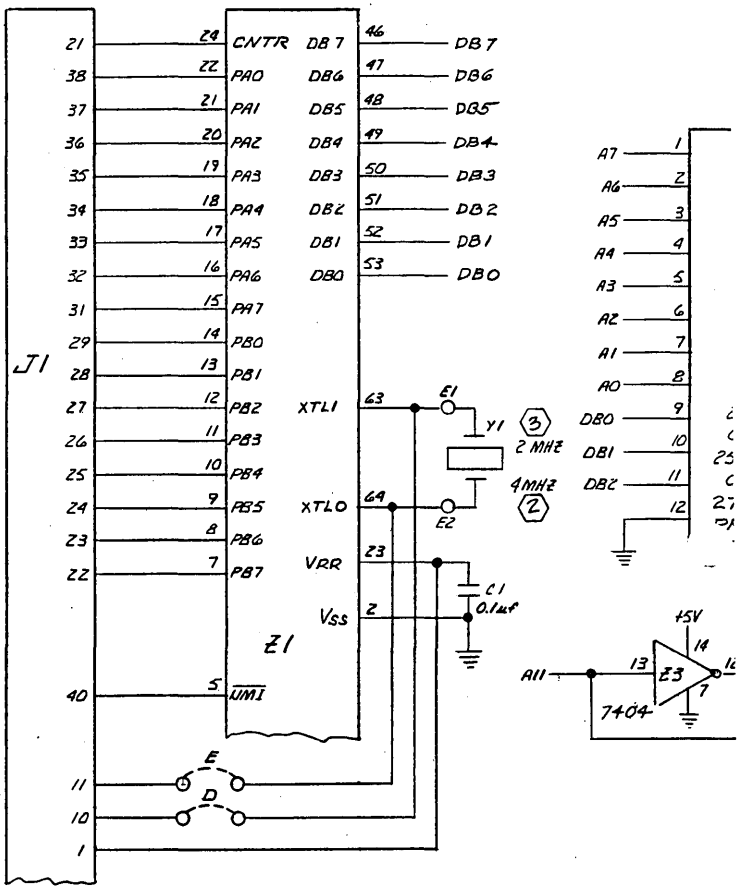
PROM	JUMPERS A	B	C	F	G
2516	IN	OUT	OUT	OUT	IN
2716	IN	OUT	OUT	OUT	IN
2532	OUT	IN	OUT	OUT	IN
2732	OUT	OUT	IN	IN	OUT

3. Connect the R6500/1 Emulator Module to the user circuit in either of two ways:

   a. Connect P1 of the interface cable into J1 of the R6500/1 Emulator Module and J1 of the interface cable into the R6500/1 socket in the user circuit.

   b. Directly connect the extended pins of J1 on the R6500/1 Emulator Module into the R6500/1 socket in the user circuit.

4. Apply power to the user circuit.



NOTE: UNLESS OTHERWISE SPECIFIED

1. REFERENCE ASSEMBLY DRAWING P501-D100

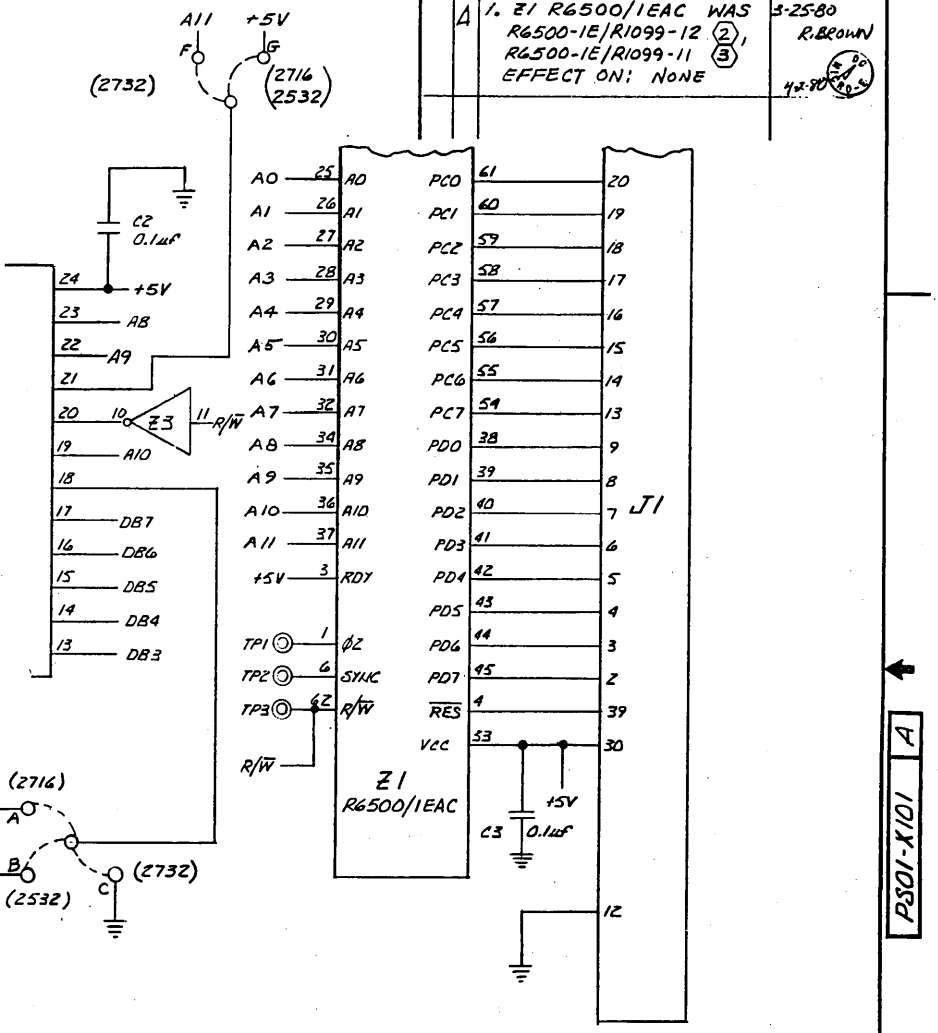
(2) USED ON -001 ASSY

(3) USED ON -011 ASSY

(4) -001 ASSEMBLY REQUIRES A PROM DEVICE WITH ACCESS TIME LESS THAN 225 ns

NC 7-25-79

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	1. ECI R6500/1EAC WAS R6500-1E/R1099-12 (2), R6500-1E/R1099-11 (3) EFFECT ON: NONE	3-25-80	R. BROWN



PS01-X101 A

SYSTEM 65 DEVELOPMENT SYSTEM

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX = ± .03 .XXX = ± .010 ANGLES ± 30'	AUTHORIZATION NO.	PART NO.
MATERIAL:	DR BY Acero 4-2-79	ROCKWELL INTERNATIONAL CORPORATION MICROELECTRONIC DEVICES 3310 MIRALOMA AVE., ANAHEIM, CA 92803
HEAT TREAT	CHK BY 7-18-79	SCHEMATIC DIAGRAM- R6500/1 EVALUATION MODULE
FINISH	APPD BY 7/18/79	SIZE C · CODE IDENT NO. 34576 · DRAWING NO. PS01-X101
NEXT ASSY / USED ON	APPD BY	SCALE NONE · REV A · SHEET
APPLICATION		

183-G-13 Rev. 5-78

JUMPER DESCRIPTION

JUMPER A — Connects address line A11 to pin 18 of the PROM after inverting for 2716 operation.

JUMPER B — Connects address line A11 directly to pin 18 of the PROM for 2532 operation.

JUMPER C — Connects GND to pin 18 of the PROM for 2732 operation.

JUMPER D — Connects the high side of the external clock or crystal to pin 63 (XTLI) of the R6500/1E Emulator Device.

JUMPER E — Connects the low side of the external clock or crystal to pin 64 (XTLO) of the R6500/1E Emulator Device.

JUMPER F — Connects address line A11 to pin 21 of the PROM for 2732 operation.

JUMPER G — Connects +5V to pin 21 of the PROM for 2716 or 2532 operation.

PROM SOCKET INTERFACE SIGNALS

PROM Socket Pin Number	PROM Device Type			
	TI TMS2532	INTEL 2732	TI TMS2516	INTEL 2716
1	A7	A7	A7	A7
2	A6	A6	A6	A6
3	A5	A5	A5	A5
4	A4	A4	A4	A4
5	A3	A3	A3	A3
6	A2	A2	A2	A2
7	A1	A1	A1	A1
8	A0	A0	A0	A0
9	Q1	O0	Q1	O0
10	Q2	O1	Q2	O1
11	Q3	O2	Q3	O2
12	VSS	GND	VSS	GND
13	Q4	O3	Q4	O3
14	Q5	O4	Q5	O4
15	Q6	O5	Q6	O5
16	Q7	O6	Q7	O6
17	Q8	O7	Q8	O7
18	A11	$\overline{CE}$	PD/PGM	$\overline{CE}$/PGM
19	A10	A10	A10	A10
20	PD/$\overline{PGM}$	$\overline{OE}$/VPP	$\overline{CS}$	$\overline{OE}$
21	VPP	A11	VPP	VPP
22	A9	A9	A9	A9
23	A8	A8	A8	A8
24	VCC	VCC	VCC	VCC

COMPONENT DESCRIPTION

Connector J1 — Connector with extended pins that allows the R6500/1 Evaluation Module to be directly plugged into the R6500/1 connector in the user circuit or to be connected to the user circuit R6500/1 connector through the 40 conductor interface cable assembly.

Socket Z1 — 64-pin DIP socket that contains the R6500/1 EAC 2-MHz Emulator Device.

Socket Z2 — 24-pin DIP socket, which accepts the user-supplied program PROM

Crystal Y1 — A 2-MHz crystal, which is used to operate the R6500/1EAC Emulator Device at 1 MHz.

Inverter Z3 — Inverts R/$\overline{W}$ to provide a low on pin 20 of the PROM when R/W is high.

— Inverts A11 when jumper A is installed to provide a low on pin 18 ($\overline{CS}$) when 2716 is used.

Capacitors C1, C2, and C3—Bypass Capacitors.

Test Point TP1—Test point to monitor ø2.

Test Point TP2—Test point to monitor SYNC.

Test Point TP3—Test point to monitor R/$\overline{W}$.

Post E1—Crystal solder post to XTLI.

Post E2—Crystal solder post to XTLO.

DOCUMENT NO. 29650 N46
AUGUST 1978

PART NUMBERS
M65-031, M65-032

Rockwell

R6500 Microcomputer System PRODUCT DESCRIPTION

16K STATIC RAM MODULE

OVERVIEW

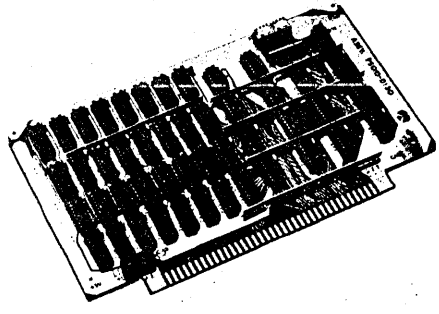
The Static RAM Module contains 16K (16,384) bytes of Random Access Memory (RAM), implemented with 32 R2114 1024 x 4 Static RAM devices. The Module also includes address decoding and selection, write protection and data buffering circuitry.

The Module's 16K bytes of RAM memory are segmented into two independent 8K-byte sections. Each 8K section is controlled by an enable/disable switch and three address range select switches, located at the top of the Module. Each 8K section can be independently write-protected via special lines.

The Static RAM Module is directly compatible with Rockwell's SYSTEM 65 Microcomputer Development System, and can be used to increase the System's read/write memory capacity from 16K bytes to 48K bytes, without hardware modification. The Module may also be installed into user-designed equipment, via the Auxiliary Card Cage.

FEATURES

- SYSTEM 65 compatible
- Available in 1 MHz (450 ns access) and 2 MHz (250 ns access) versions.
- 16K bytes of Random Access Memory, with two independent 8K sections
- Separate write protect capability for each 8K section
- Static — no clocks or strobes required
- 9.75 in. x 6.00 in. module
- Single +5V supply



FUNCTIONAL DESCRIPTION

In reading the text to follow, refer to the Functional Block Diagram below and the attached schematics:

- PS00-X131, the -001 assembly of the RAM Module
- PS00-X133, the -071 assembly of the RAM Module

The edge connector pin assignments for the RAM Module are compatible with the Motherboard pin assignments given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).

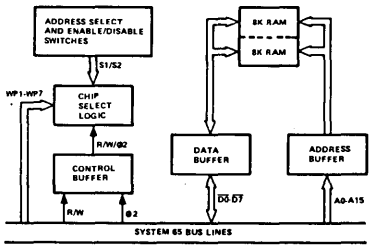
The RAM Module's 16K bytes of read/write memory are provided by 32 R2114 1024 x 4-bit Static RAM devices.

Address Buffers Z47, Z46 and Z33 and Data Buffers Z32 and Z45 present a single TTL load to the Motherboard edge connector. The data signals are inverted to make them compatible with the SYSTEM 65 Data Bus ($\overline{D0}$-$\overline{D7}$).

Module Switches S1 and S2 provide independent 8K RAM section enable/disable and address selection. S1-4 and S2-4 permit each 8K section of RAM to be enabled or disabled. S1-1, -2 and -3 and S2-1, -2 and -3 select the base address to which the respective 8K sections will respond. These switch settings are compared to upper address bits A13, A14 and A15 in Address Comparator devices Z10 and Z21. The Comparator outputs enable or disable 1-of-8 Decoder devices Z9 and Z20 to provide the input chip select signals to the two 8K RAM sections.

Write protection is controlled by seven Write Protect lines, WP1-WP7, one line for each 8K section of memory (the lowest section, addresses $0000-$1FFF, may not be write protected; note that Z48-2 is tied to ground to permanently enable writing to this section). A low voltage on WP1-WP7 enables writing into the associated 8K section.

When the Address Comparator enables the RAM Device Select Decoders, Address Select switches S1-1 through S1-3 and S2-1 through S2-3 are used by Z35 and Z36 to select one of the seven Write Protect lines. The selected line controls the RAM Write Control signals, Z34-6 and Z34-8.



RAM Module Functional Block Diagram

INSTALLATION

The procedure below should be used to install 16K Static RAM Modules in the SYSTEM 65 or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn SYSTEM 65 power off.

   CAUTION

   Never install or remove modules with SYSTEM 65 power on — It may cause damage to the module and/or to the System.

2. Remove the top cover of the SYSTEM 65.

3. The RAM Module has two banks of switches — S1 and S2 — one bank for each 8K section of RAM. Using Tables 1 and 2, select the enable/disable and address range characteristics for each 8K section.

   NOTES

   For proper SYSTEM 65 operation . . .

   a. Page 0 (address range $0000-$00FF) and Page 1 ($0100-$01FF) must be provided in RAM — either internal RAM or external RAM as interfaced by USER 65 or its equivalent.

   b. RAM addresses in the range $C000-$FFFF are used by the SYSTEM 65 Monitor Board, and must not be enabled in RAM Modules.

4. Insert the RAM Module(s) into any vacant slot(s) in the SYSTEM 65 chassis.

5. Install the top cover of the SYSTEM 65.

6. Turn SYSTEM 65 power on.

Table 1. RAM Enable/Disable Switch Settings

Switch S1/S2-4 Position	RAM Enable/Disable State
Up (Off)	RAM Disabled (Deselected)
Down (On)	RAM Enabled (Selected)

Table 2. RAM Address Range Select Switch Settings

Switch S1/S2 Position			
-1	-2	-3	8K Address Range Selected
Up	Up	Up	$0000 - $1FFF
Down	Up	Up	$2000 - $3FFF
Up	Down	Up	$4000 - $5FFF
Down	Down	Up	$6000 - $7FFF
Up	Up	Down	$8000 - $9FFF
Down	Up	Down	$A000 - $BFFF
Up	Down	Down	$C000 - $DFFF
Down	Down	Down	$E000 - $FFFF

NOTE: "Up" is toward the top edge of the Module.

SPECIFICATIONS

Memory Size:	16K bytes
Word Length:	8 bits
Interface:	SYSTEM 65 compatible
Max. Access Time:	450 ns (P/N M65-031) 250 ns (P/N M65-032)
Module Components:	32 R2114 Static 1024 x 4-bit RAM devices
Module Dimensions:	9.75 in. wide x 6.00 in. high
Edge Connector:	86 pins on 0.156-in. centers
Operating Temperature:	0^{o}C to +70^{o}C
Power Requirements:	+5 VDC ±5% @ 3.0 amps (typical)

LOGIC LEVELS

$T_A = 0^{o}C$ to $+70^{o}C$, $V_{CC} = +5V$ ±5%

Characteristic	Symbol	Min	Max	Unit	Condition
Inputs ($\overline{D0}$-$\overline{D7}$), A0-A15, WP1-WP7, Ø2, R/$\overline{W}$)					
Input Low Voltage	V_{IL}		0.8	V	$I_{IL} = 400\ \mu a$
Input High Voltage	V_{IH}	2.0	V_{CC}	V	$I_{IH} = 40\ \mu a$
Outputs ($\overline{D0}$-$\overline{D7}$)					
Output Low Voltage	V_{OL}		0.5	V	$I_{OL} = 48$ ma
Output High Voltage	V_{OH}	2.4	V_{CC}	V	$I_{OH} = 10$ ma

DOCUMENT NO. 29650 N42
REV. 2, FEBRUARY 1980

PART NUMBER
M65-040

Rockwell

R6500 Microcomputer System PRODUCT DESCRIPTION

PROM PROGRAMMER MODULE

OVERVIEW

The PROM Programmer Module provides SYSTEM 65 users with a means to program, verify, read and check Programmable Read Only Memory (PROM) devices, and supports 2704, 2708, 2716, 2516, 2532 and 2758 devices. The PROM Programmer Module connects directly to the PROM Socket on the front panel of the SYSTEM 65 chassis, via supplied cable.

The Module is supplied with a mini-floppy diskette which holds a set of software routines that allow the user to check a PROM for proper initialization, program the PROM from SYSTEM 65 memory, verify the PROM with SYSTEM 65 memory, and read the contents of the PROM into memory. Utility functions to load, verify and dump memory are also supplied.

FEATURES

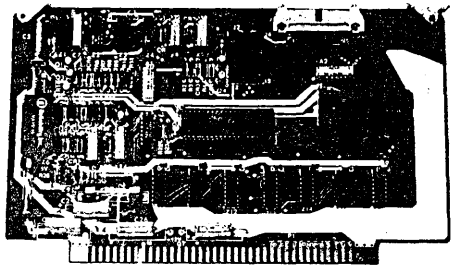
- SYSTEM 65 compatible
- Supports programming of 2704, 2708, 2516, 2532, 2716 (Intel and Texas Instruments) and 2758 PROM devices.
- Comes with software on mini-floppy diskette

FUNCTIONAL DESCRIPTION

In reading the text to follow, refer to the Functional Block Diagram in Figure 1 and the attached schematic, PS00-X201. The edge connector pin assignments for the PROM Programmer Module are identical to the Motherboard pin assignments given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).

Table 1 summarizes the PROM Socket interface, and applies to both the PROM socket located on the PROM Programmer Module and the PROM socket located on the SYSTEM 65 front panel.

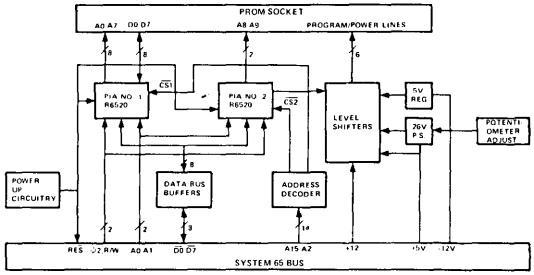
The PROM Programmer Module consists of two R6520 Peripheral Interface Adapters (PIAs), data buffers, address decoders, 26V power supply, level shifters and power-up circuitry.



The power-up circuitry (Z9) generates an automatic reset during power-up. A reset signal may also come from the Reset line of the SYSTEM 65 Bus.

The PROM Programmer Module contains data bus buffers, Z12 and Z13, to provide a logical inversion and a single TTL load to the SYSTEM 65 bus signals. The two R6520 PIAs, Z5 and Z8, are used to store the address, data and control information for the PROM device. The address, Read/Write (R/$\overline{W}$), and $\phi 2$ signals are buffered and decoded by Z10, Z11, Z14, Z15 and Z16. PIA No. 1 is addressed at locations $C018-$C01B. PIA No. 2 is addressed at locations $C01C-$C01F.

The PROM device receives address lines A0-A9 and data lines D0-D7 directly from the PIA devices. The program lines (see Table 1, PROM socket pin nos. 18, 19 and 20) are level-shifted to provide either 0V, +5V, +12V, +25V or +26V to the PROM device, depending on the device type. The 26-volt power is generated from the +5-volt power through a DC-DC converter, Z6, and an adjustable voltage regulator, Z1. Relays XR1 through XR4 are used to switch the power lines (see Table 1, PROM socket pin nos. 21 and 23) to +5V, +12V and -5V to the PROM device, depending on the device type. The -5V power is generated from the -12V power line through a voltage regulator, Q9.



Note: All examples were prepared using SYSTEM 65 Operating System Version 3

Figure 1. PROM Programmer Functional Block Diagram

Specifications subject to change without notice

Table 1. SYSTEM 65 PROM Socket Interface Summary

PROM Socket Pin Number	PROM Device Type							Connector J1 Pin Number
	2704	Intel 2708	Intel 2758	Intel 2716	T.I. 2716	T.I. 2516	T.I. 2532	
1	A7	A7	A7	A7	A7	A7	A7	21
2	A6	A6	A6	A6	A6	A6	A6	19
3	A5	A5	A5	A5	A5	A5	A5	17
4	A4	A4	A4	A4	A4	A4	A4	15
5	A3	A3	A3	A3	A3	A3	A3	23
6	A2	A2	A2	A2	A2	A2	A2	25
7	A1	A1	A1	A1	A1	A1	A1	26
8	A0	A0	A0	A0	A0	A0	A0	24
9	D0	D0	D0	D0	Q1	Q1	Q1	22
10	D1	D1	D1	D1	Q2	Q2	Q2	20
11	D2	D2	D2	D2	Q3	Q3	Q3	18
12	GND	GND	GND	GND	VSS	VSS	VSS	16
13	D3	D3	D3	D3	Q4	Q4	Q4	10
14	D4	D4	D4	D4	Q5	Q5	Q5	8
15	D5	D5	D5	D5	Q6	Q6	Q6	6
16	D6	D6	D6	D6	Q7	Q7	Q7	2
17	D7	D7	D7	D7	Q8	Q8	Q8	4
18	PGM	PGM	$\overline{CE}$/PGM	$\overline{CE}$/PGM	$\overline{CS}$/PGM	PD/PGM	A11	13
19	VDD	VDD	GND	A10	VDD	A10	A10	11
20	$\overline{CS}$/WE	$\overline{CS}$/WE	$\overline{OE}$	$\overline{OE}$	A10	$\overline{CS}$	PD/$\overline{PGM}$	9
21	VBB	VBB	VPP	VPP	VBB	VPP	VPP	7
22	GND	A9	A9	A9	A9	A9	A9	5
23	A8	A8	A8	A8	A8	A8	A8	3
24	VCC	VCC	VCC	VCC	VCC(PE)	VCC	VCC	1

MODULE INSTALLATION

Install the PROM Programmer Module as follows:

1. Turn SYSTEM 65 power off.

CAUTION

Never install or remove modules with SYSTEM 65 power on it may cause damage to the module and/or to the System.

2. Remove the top cover of the SYSTEM 65.
3. Insert the PROM Programmer Module into any vacant slot in the SYSTEM 65 chassis.
4. Connect one end of the supplied cable to the connector on top of the PROM Programmer Module and the other end to the connector mounted on the inside front panel of SYSTEM 65. Observe the correct polarity of the plugs and sockets; i.e., align the arrows marked on the plugs and sockets.
5. Install the top cover of the SYSTEM 65.
6. Set the SYSTEM 65 RUN/STEP Switch to RUN.

NOTE

The PROM Programmer will not operate properly if the RUN/STEP Switch is in the STEP position.

7. Turn SYSTEM 65 power on.
8. The PROM Programmer Module has an automatic reset feature. The standard power-up message should appear on the system terminal device at power-on. A manually-initiated reset may, however, be performed whenever required.

PROM DEVICE INSERTION/REMOVAL

CAUTION

The PROM device is fragile, and dropping, twisting or uneven pressure may break it. Never press down on the window area of the chip

The PROM device may be inserted into SYSTEM 65 front panel socket or into the socket located on the PROM Programmer Module.

CAUTION

Only one PROM device should be installed at a time -- in either the SYSTEM 65 socket or the PROM Programmer Module socket. Programming with PROM devices installed in both locations may cause erroneous results and/or damage to the PROM.

PROM INSERTION/REMOVAL ON THE SYSTEM 65 FRONT PANEL

To insert the PROM device:

1. Push the PROM socket lever out from the SYSTEM 65 front panel, to release pin pressure.
2. Position the PROM device in front of the socket, being careful to observe the Pin 1 location.

CAUTION

Incorrect PROM installation may cause PROM damage and/or may blow Fuses F1 and F2 on the PROM Programmer Module.

3. Insert the PROM into the socket, then push up and in on the socket lever to apply pressure to the pins.

To remove the PROM device, grasp the PROM device at each end, then push the socket lever away from the SYSTEM 65 front panel to release pin pressure.

PROM INSERTION/REMOVAL ON PROM PROGRAMMER MODULE

To insert the PROM device, position the PROM device in front of the socket, being careful to observe the PIN 1 location.

CAUTION

Incorrect PROM installation may cause PROM damage and/or may blow Fuses F1 and F2 on the PROM Programmer Module.

With the PROM properly oriented, gently start all pins evenly into the socket pin guides. Then press firmly and evenly on the device (avoiding contact with the light window) until the device is securely seated.

To remove the PROM device, exert an even, upward force on both sides of the device while counteracting with a lesser, evenly-applied downward force. This will prevent the PROM device from popping out one side and bending or breaking pins still engaged at the other end of the socket.

OPERATION

The PROM Programmer software allows checking, reading, verifying and programming 2704, 2708, 2758, 2516, 2532 or 2716 type devices. The data/instructions are copied to/from the SYSTEM 65 RAM memory in the address range specified by the user. The user can then transfer this information to/from the diskette (or other I/O device) using SYSTEM 65 software routines.

LOADING THE PROM PROGRAMMER ROUTINES

There is one PROM programmer object file supplied on the PROM Programmer diskette, PROM*n, where "n" is the program release revision letter. File PROM*n occupies from $0200 to $0FFF. User programs can be loaded starting at $1000. To load the PROM*n program, use the SYSTEM 65 Load Command L. Then enter the file name (PROM*n) and disk drive number desired. Since the PROM*n program may occupy the same memory area in which user's data may reside, an offset may be applied to the user's data to locate it to $1000 or above (See Load, Verify and Dump functions with offset). PROM*n uses page 0 ($0080–$009A) and page 1 ($0100–$01FF).

NOTE

The SYSTEM 65 RUN/STEP switch must be in the Run position for PROM programming.

After the program is loaded, use the five (5) key to start the PROM Programmer routines for a 1 MHz system or the six (6) key for a 2 MHz system. The 5 (or 6) key may also be used for reentry into the PROM Programmer routines. Once the routines are entered, the only way to exit back to the SYSTEM 65 monitor is to press the ESC key, if the program is waiting for input, or the Reset switch.

The PROM Programmer PROGRAM PROM (P) and VERIFY PROM (V) functions require that the data to be programmed and/or verified be in RAM memory prior to execution. If the program data resides on diskette (or other media), use the SYSTEM 65 Monitor L command to load the object code into memory before entering the PROM programmer functions with key 5 (or 6). Alternatively, use the PROM Programmer L command to load the program data with optional offset after the PROM Programmer functions have been entered.

PROM PROGRAMMER OPERATION

Before entering any of the PROM Programmer functions to follow, ensure that the required PROM device is installed in the desired PROM socket – the SYSTEM 65 front panel socket or the PROM Programmer Module's PROM socket – per the PROM Device Insertion/Removal instructions. The PROM Programmer functions may be entered in the absence of an installed PROM device, but this may cause verify errors.

CAUTIONS

1. Insert a PROM device only when SYSTEM 65 power is on and either the Monitor prompt (<) or the PROM Programmer prompt (=) is the last character displayed on the system terminal. Failure to do so may cause damage to the PROM device.
2. DC power to the PROM device installed in the PROM socket is set to zero upon SYSTEM 65 power-up or depression of the Reset switch. During a PROM Programmer function, DC power is supplied to the PROM socket after entry of the last address, then the commanded PROM programming function is performed. The DC power is removed upon completion of the programming function, before the next PROM Programmer prompt character (=) is displayed.

Once started, the routines will ask the user for certain information. This information should be entered on the system terminal. For numbers or addresses, type in the number followed by a space o. carriage return to terminate the number. Leading zeros are not necessary. Only the last four digits of the number are used. If a mistake is made before pressing the space bar or carriage return, reenter the correct number (all four digits). If a mistake is made after entering a number, exit the PROM Programmer routines using the ESC key or Reset switch on the front panel and restart with key 5 (or 6). If an invalid command or number is entered the routines will print WHAT? and ask you to reenter.

Figure 2 is an example of a PROM Programmer load and initialization along with the user's response.

Next, the data to be copied to the PROM device can be loaded using the L command. In this example, the file USERIN was loaded. Type 5 (or 6) to start the routines. Next, enter the device type. If a 2716 was entered, the message TMS 2716 (Texas Instruments) PROM? will be printed. Enter Y for yes or N for no. The routines will reprint the device type for verification each time a new function is requested. A single character should now be entered to indicate the function requested as outlined in the subsequent text.

```
<L>OFFSET=0000 IN=F  FILE=PROM*F  DISK=1
DONE

<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
  OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 2. Power-Up and Loarling Responses

PROM PROGRAMMER RE-ENTRY

After initialization by the (5) or (6) entry and selection of a PROM type, the PROM Programmer function may be re-entered from the SYSTEM 65 Monitor by typing 7. This allows the Monitor to be entered from the PROM Programmer to perform utility functions then the PROM Programmer quickly re-entered to continue PROM operations. Initial entry using key 5 or 6 must be used, however, to change PROM type selection. The message WHAT? will be displayed if Key 7 is typed prior to initialization of the PROM Programmer function.

ADDRESS SELECTION

The addresses entered are the hexadecimal locations of the RAM memory used for checking, programming, reading, or verifying. The upper address bits are then stripped off to form the address for the PROM devices. In general, the addresses must comply with the following restrictions:

1. Cannot be Page 0 ($0000–$00FF) or Page 1 ($0100–$01FF).
2. Cannot overlap the PROM Programmer routine for file name PROM*n ($0200–$0FFF).
3. The last address must be greater than or equal to the first address entered.
4. The address range from first to last must not exceed the size of the PROM being programmed.

In addition, there are further restrictions on certain PROM devices, imposed by the PROM manufacturer. The 2704, 2708, and TI TMS-2716 must be programmed using their total address space during one programming. This means that the 2704, 2708, and TI TMS2716 must start on a 1/2K, 1K or 2K address boundary, respectively. They also have to extend 1/2K, 1K or 2K bytes in length, respectively. The 2516, 2532, 2758 and Intel 2716 do not have this requirement. Therefore, single byte or multi-bytes may be programmed within the address range of the device. The routines are designed to check for any invalid address entered and will print WHAT? and ask for the address again.

PROGRAM FUNCTION (THE P COMMAND)

The Program Function (P) loads the contents of SYSTEM 65 memory into PROM. It is entered by pressing the P key in response to the ENTER command message. The routines will ask where any errors detected during verifying should be printed. This is indicated by the message ERROR LIST OUT=. Enter any of the standard I/O device characters (space for CRT, P for Printer, etc.).

After the first and last address is entered, the routines will check to

see if the PROM is initialized. Since these PROMs are initialized to an all-ones condition by placing them under an ultraviolet light, a check is made prior to programming for an all-one's condition. If any zero is detected in the bounds of the address range entered, the messages PROM NOT INITIALIZED and CONTINUE Y or N will be printed. The user has the option of aborting the programming (type N for no) and initializing the PROM properly or continuing with the programming by typing the Y (yes) key.

It is possible to change a 1 to 0 with the PROM programmer, but the PROM must be exposed to an ultraviolet light to set the bits back to one's according to the respective manufacturer's specifications. If the PROM is initialized or "Y" entered, a star will be printed every 1-5 seconds, indicating programming in progress. After programming, the message VERIFYING will be printed and the PROM device will be verified against the specified RAM locations. This is automatically done every time. If there are no errors detected, the message DONE will be printed and the next operation requested. Any errors detected will be printed on the selected I/O device.

Figure 3 shows an example of the Program Function.

NOTES

1. A verification error showing a series of 1's in a specific PROM bit position after programming may indicate a poor connector contact caused by improper PROM installation in the PROM socket. See the PROM Device Insertion/Removal instructions.
2. If fuse F1 or F2 on the PROM Programmer Module is blown, the PROM may not verify correctly. Verify that both are good if a verify error occurs.


```
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
=P
PROGRAM
ERROR LIST
OUT=L
ENTER FIRST ADDRESS
=2000
ENTER LAST ADDRESS
=27FF
PROM NOT INITIALIZED
CONTINUE(Y OR N)
=Y
**********************************************************************
DONE
VERIFYING

DONE

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 3. Program Function Example

VERIFY FUNCTION (THE V COMMAND)

The Verify Function (V) verifies the contents of the PROM with the contents of SYSTEM 65 RAM. It is entered by pressing the V key in response to the ENTER command message.

The routines will request where any errors detected should be printed. This is indicated by the message ERROR LIST OUT=. Enter any of the standard I/O device characters defined in the SYSTEM 65 User's Manual (space for CRT, P for Printer, etc.). Next, type in the first and last addresses. As soon as the last address is entered, power will be applied to the PROM device and the contents of the PROM compared to the respective content of the RAM. If no errors are found, the message DONE will be printed, and the next operation requested. If errors are detected, the address, contents of PROM, and contents of RAM in disagreement will be displayed/printed on the selected I/O device. Figure 4 shows an example of the Verify Function with errors.

```
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
=V
VERIFY
ERROR LIST
OUT=L
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF
ERROR
ADDR PROM RAM
1000  C0   20
1400  C0   4C
17FF  C0   15

DONE

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 4. Verify Function Example with Errors

READ FUNCTION (THE R COMMAND)

The Read Function (R) reads the contents of PROM into SYSTEM 65. RAM. It is entered by pressing the R key in response to the ENTER command message.

After the first and last addresses are entered, power will be applied to the PROM and the contents copied into the specified RAM locations. When completed, the message DONE will be printed and the next operation requested. Figure 5 shows an example of a Read Function.

The PROM Programmer READ function reads program data into SYSTEM 65 RAM memory from PROM. After reading is complete, save the PROM data on diskette (or other media) using the SYSTEM 65 Monitor D Command after exiting the PROM Programmer functions. Alternatively, use the PROM Programmer D command to dump the data with optional offset before the PROM Programmer functions are exited. The amount to be stored or loaded at one time is limited only by the RAM locations available.

```
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
=R
READ
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF

DONE

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 5. Read Function Example

CHECK FUNCTION (THE C COMMAND)

The Check Function (C) is used to check that the PROM is initialized. It is entered by pressing the C key in response to the ENTER command message.

After the first and last addresses are entered, power is applied to the device and all specified locations are checked for $FF. The message PROM NOT INITIALIZED will be printed if all locations do not contain $FF. The message DONE will be printed when the Check Function is complete.

Figure 6 is an example of a successful Check Function.

```
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
=C
CHECK
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF
PROM NOT INITIALIZED

DONE

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 6. Check Function Example

LOAD MEMORY WITH OFFSET FUNCTION (THE L COMMAND)

The Load Memory with Offset Function (L) copies data from an input object code file into memory addresses offset by an entered amount from the addresses on the input file. The entered offset value is additive with carry from bit 15 ignored, e.g.;

Input File Address	Offset Value	Address in Memory
$1000	0	$1000
$1000	$2000	$3000
$7000	$A000	$1000
$E000	$2000	$1000

Figure 7 is an example of the Load Memory with Offset Function.

```
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
=L
LOAD
OFFSET=D000  IN=F  FILE=AIMBAS  DISK=2

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 7. Load Memory with Offset Function Example

VERIFY MEMORY WITH OFFSET FUNCTION (THE F COMMAND)

The Verify Memory with Offset Function (F) compares the contents of an object code file with the contents of memory at addresses in memory offset by an entered amount from the addresses on the reference object code file. The entered offset is additive in the same manner as the Load with Offset function. The contents of both memory (MEM) and reference file (FILE) are displayed/printed along with the address (ADDR) if any differences in value are detected.

Figure 8 is an example of the Verify Memory with Offset Function showing two detected errors.

```
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
=F
VERIFY
OFFSET=D000  IN=F  FILE=AIMBAS  DISK=2
ERROR LIST
OUT=L  ADDR/MEM/FILE
2000 E0 58  2200 4C 52

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 8. Verify Memory with Offset Function Example with Errors

DUMP MEMORY WITH OFFSET FUNCTION (THE D COMMAND)

The Dump Memory with Offset Function (D) copies data from memory to an output object code file with addresses in the output file offset an entered amount from the addresses in memory. The entered offset value is additive from the output file to memory with carry from bit 15 ignored; e.g.:

Output File Address (FROM=)	Offset Value	Address in Memory
$1000	0	$1000
$4000	$D000	$1000
$1000	$8000	$9000
$A000	$1000	$B000

Figure 9 is an example of the Dump Memory with Offset Function.

```
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
=D
DUMP
OFFSET=D000  OUT=F  FILE=PRMOUT  DISK=2
FROM=4000  TO=47FF

MORE?N
**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 9. Dump Memory with Offset Function Example

MEMORY FILL FUNCTION (THE M COMMAND)

The Memory Fill Function (M) allows a user selected range of RAM to be initialized to an entered bit pattern. The desired PROM object code can then be loaded. All unloaded memory in the PROM address range will remain initialized with the previously filled bit pattern. This allows PROM codes over a total PROM address range to be easily verified without invalid data errors being indicated due to random bit patterns in unused addresses.

Figure 10 is an example of the Memory Fill Function. Enter the bit pattern to be loaded in hexadecimal in response to the MEM FILL= prompt. The last two digits entered will be accepted. Terminate the entry with a carriage return. Then enter the starting and ending addresses in hexadecimal of the RAM to be filled. Terminate entries with a carriage return. The last four digits entered will be accepted.

```
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
=M
MEM FILL=00
FROM=1000   TO=13FF

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 10. Memory Fill Function Example

INVERT MEMORY (THE I COMMAND)

The Invert Memory Function (I) allows selected bits to be inverted within a selected address range. This function allows the contents of RAM to be easily one's complemented if the PROM code is to be inverted from the ROM code.

Figure 11 is an example of the Invert Memory Function. Enter the bit pattern to be exclusively or'ed with memory. A "1" in a bit position will invert the bit value while a "0" will leave the bit value unchanged. Enter "FF" to invert all bit values and "00" to invert none of the bit values. Terminate the entry with a carriage return. The last two digits entered will be accepted. Enter the starting and ending addresses as described for the MEM FILL function.

```
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704,2708,2758,2716,2516,2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
=I
INVERT BITS=FF
FROM=1000   TO=13FF

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),DUMP(D),MEM FILL(M),INVERT(I)
```

Figure 11. Invert Bits Function Example

SPECIFICATIONS

PROM Devices Supported:	2704, 2708, 2758, Intel 2716 and Texas Instruments 2716
Programming Time (approximately):	2704 – 100 sec. 2708 – 200 sec. 2758 – 60 sec. Intel 2716 – 120 sec. T.I. 2716 – 400 sec. 2516 – 120 sec. 2532 – 240 sec.
Interface:	SYSTEM 65 compatible
Module Dimensions:	9.75 in. wide x 6.00 in. high
Edge Connector:	86 pins on 0.156-in. centers
Operating Temperature:	0^{o} to + 70^{o}C
Power Requirements:	+5 VDC ± 5% @ 750 ma (fused at 2 amps) +12 VDC ± 5% @ 50 ma (fused at ½ amp) -12 VDC ± 5% @ 50 ma.
Fuse Description:	F1 – AGC ½A–250V (Bussman) F2 – AGC 2A–250V (Bussman)

DOCUMENT NO. 29650 N47
AUGUST 1978

PART NUMBER
M65-045

R6500 Microcomputer System PRODUCT DESCRIPTION

PROM/ROM MODULE

OVERVIEW

The PROM/ROM Module (Part Number M65-045) permits system read only memory to be increased by up to 16K bytes. The Module provides 16 24-pin DIP sockets for accepting industry-standard 2708, 2716 or 2758 PROM devices, or 2316 or 2332 ROM devices. PROMs and ROMs cannot be mixed on the Module.

The PROM/ROM Module's 16K-byte address space is segmented into four independent 4K-byte sections. Each 4K-byte section is provided with a switch for selecting its base address. Further, each socket has an individual enable/disable switch, providing resolution down to 1K bytes.

FEATURES

- SYSTEM 65 compatible
- 16K-byte read only memory capacity
- Accepts 2708, 2716 or 2758 PROM devices
- Accepts 2316 or 2332 ROM devices
- Sockets can be individually enabled/disabled
- Base address is switch-selectable for each 4K-byte address space
- Single +5V supply

FUNCTIONAL DESCRIPTION

In reading the text to follow, refer to the Functional Block Diagram below and the attached schematics:

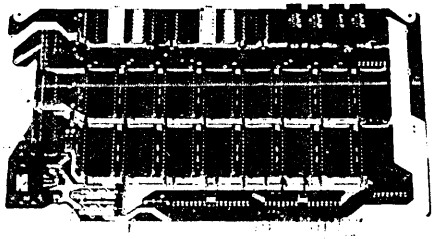
- PS00-X-141, the -001 version of the PROM/ROM Module
- PS00-X-143, the -011 version of the PROM/ROM Module

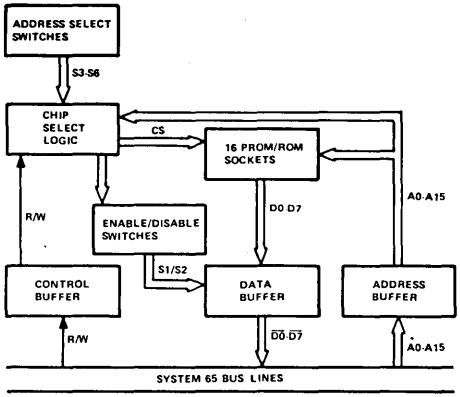
The edge connector pin assignments for the PROM/ROM Module are identical to the Motherboard pin assignments given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).

The PROM/ROM Module comes with 16 sockets for accepting the following types of memory devices:

- Up to four 2332 ROMs, or
- Up to eight 2316 ROMs, or
- Up to eight 2716 PROMs, or
- Up to 16 2708 or 2758 PROMs

The address switches on the Module are set in accordance with the type and number of PROM or ROM devices installed. Each socket may also be selected by a switch. Further, each 4K address space also has a separate switch for selection of its base address. The Chip Select Logic specifies the PROM/ROM to be accessed and the address lines from the System bus select the memory location. The selected PROM/ROM device responds by placing 8 bits of data on the data lines ($\overline{D0}$ through $\overline{D7}$) for transfer to the CPU.





PROM/ROM Module Functional Block Diagram

Specifications subject to change without notice

SWITCHES AND JUMPERS

The PROM/ROM Module can accommodate a variety of standard PROM and ROM devices. The user must configure the Module for his specific application, and does so with various switches and jumpers on the Module itself.

The PROM/ROM Module has a total address space of 16K bytes, divided into four 4K-byte sections. Each 4K section has a separate base address select switch, S3 through S6, which must be set to the desired hexadecimal value (0 - F). For example, if Switch S3 is set to C, the base address for Sockets Z4, Z5, Z6 and Z7 is $C000 (where $ indicates hexadecimal). Further, each individual socket can be enabled or disabled from driving the Data Bus by setting/resetting Switches S1 and S2.

There is a further restriction for ROMs: Since ROMs have chip selects, they will only work in the proper sockets with proper base address switch settings. For example, a 2316 ROM with CS3=1, CS2=0 and CS1=1 will work only in Socket Z22 (see Table 4) and with a selected base address value of 2, 6, A or E.

As mentioned above, the PROM/ROM Module must also be jumper-configured for the device being used. Jumper information is given with switch select tables. The function of each jumper is summarized in Table 1.

Table 1. PROM/ROM Board Jumper Functions

Jumper No.	Jumper Function
1	Connects A12 to Pin 18 of all sockets
2	Enables 1K address selection
3	Connects +12VDC to Pin 19 of all sockets
4	Enables 2K address selection
5	Connects A13 to Pin 21 of all sockets
6	Connects A10 to Pin 19 of all sockets
7	Connects A11 to Pin 21 of all sockets
8	Connects +5VDC to Pin 21 of all sockets
9	Connects A11 to Pin 18 of all sockets
10	Connects -5VDC to Pin 21 of all sockets
11	Connects GND to Pin 18 of all sockets
12	Enables active low chip selects on Sockets Z7, Z14, Z22 and Z29

Table 2. Switch Settings for 2716 PROM Operation

Base Address (A15, A14, A13, A12)	Address A11	Socket	Enable/Disable Switch
S3 (0-F)	0	Z5	S1-2
	1	Z7	S1-4
S4 (0-F)	0	Z11	S1-6
	1	Z14	S1-8
S5 (0-F)	0	Z18	S2-2
	1	Z22	S2-4
S6 (0-F)	0	Z24	S2-6
	1	Z29	S2-8

For 2716 PROMs, add Jumpers 4, 6, 8, 11 and 12.

Table 3. Switch Settings for 2708 or 2758 PROM Operations

Base Address (A15, A14, A13, A12)	Address A11 A10	Socket	Enable/Disable Switch
S3 (0-F)	0 0	Z4	S1-1
	0 1	Z5	S1-2
	1 0	Z6	S1-3
	1 1	Z7	S1-4
S4 (0-F)	0 0	Z10	S1-5
	0 1	Z11	S1-6
	1 0	Z13	S1-7
	1 1	Z14	S1-8
S5 (0-F)	0 0	Z17	S2-1
	0 1	Z18	S2-2
	1 0	Z21	S2-3
	1 1	Z22	S2-4
S6 (0-F)	0 0	Z23	S2-5
	0 1	Z24	S2-6
	1 0	Z28	S2-7
	1 1	Z29	S2-8

For 2708 PROMs, add Jumpers 2, 3, 4, 11 and 12 **and** add Capacitors C6-C9, C14-C17, C21-C24, C29-C32, C37-C40, C45-C48, C52-C55 and C59-C62. All capacitors are 0.1 μf.

For 2758 PROMs, add Jumpers 2, 8, 11 and 12 **and** jumper left post of Jumper 3 to right post of Jumper 4.

Table 4. Switch Settings for 2316 ROM Operation

Base Address (A15, A14, A13, A12)	ROM Chip Selects* A13 CS3	A12 CS2	A11 CS1	Socket	Enable/Disable Switch
S3 (0, 4, 8, C)	0	0	0	Z5	S1-2
	0	0	1	Z7	S1-4
S4 (1, 5, 9, D)	0	1	0	Z11	S1-6
	0	1	1	Z14	S1-8
S5 (2, 6, A, E)	1	0	0	Z18	S2-2
	1	0	1	Z22	S2-4
S6 (3, 7, B, F)	1	1	0	Z24	S2-6
	1	1	1	Z29	S2-8

*Assumes CS1=A11, CS2=A12 and CS3=A13

For 2316 ROMs, add Jumpers 1, 4, 5 and 6

Table 5. Switch Settings for 2332 ROM Operation

Base Address (A15, A14, A13, A12)	ROM Chip Selects* A13 S2	A12 S1	Socket	Enable/Disable Switch
S3 (0, 4, 8, C)	0	0	Z7	S1-4
S4 (1, 5, 9, D)	0	1	Z14	S1-8
S5 (2, 6, A, E)	1	0	Z22	S2-4
S6 (3, 7, B, F)	1	1	Z29	S2-8

*Assumes S1=A12 and S2=A13

For 2332 ROMs, add Jumpers 2, 5, 6 and 9

INSTALLATION

The procedure below should be used to install PROM/ROM Modules in the SYSTEM 65 chassis or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn SYSTEM 65 power off.

CAUTION

Never install or remove modules with SYSTEM 65 power on — it may cause damage to the module and/or to the System.

2. Remove the top copver of the SYSTEM 65.
3. Set the switches on the PROM/ROM module per Tables 2 through 5. The base memory addresses are assigned by four hexadecimal switches, S3 through S6. Individual sockets are enabled/disabled by Switches S1 and S2.
4. Install the required jumpers per directions given with the switch table.
5. Install the required PROM or ROM devices in their appropriate sockets.
6. Insert the PROM/ROM Module(s) into any vacant slot(s) in the SYSTEM 65 chassis.
7. Install the top cover of the SYSTEM 65.
8. Turn SYSTEM 65 power on.

SPECIFICATIONS

Memory Capacity:	16K bytes
Word Length:	8 bits
Interface:	SYSTEM 65 compatible
Module Components:	16 24-pin DIP sockets
Module Dimensions:	9.75 in. wide x 6.00 in. high
Edge Connector:	86 pins on 0.156-in. centers
Operating Temperature:	$0^{\circ}C$ to $+70^{\circ}C$
Power Requirements:	+5 VDC + 5% @ 500 ma. with no devices installed

LOGIC LEVELS

$T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = +5V + 5\%$

Characteristic	Symbol	Min	Max	Unit	Condition
Inputs ($\overline{D0}$-$\overline{D7}$, A0-A15, $\phi 2$, R/$\overline{W}$)					
Input Low Voltage	V_{IL}		0.8	V	$I_{IL} = 400\ \mu a$
Input High Voltage	V_{IH}	2.0	V_{CC}	V	$I_{IH} = 40\ \mu a$
Outputs ($\overline{D0}$-$\overline{D7}$)					
Output Low Voltage	V_{OL}		0.5	V	$I_{OL} = 48$ ma
Output High Voltage	V_{OH}	2.4	V_{CC}	V	$I_{OH} = 10$ ma

PART NUMBER
M65-071

Rockwell

R6500 Microcomputer System
PRODUCT DESCRIPTION

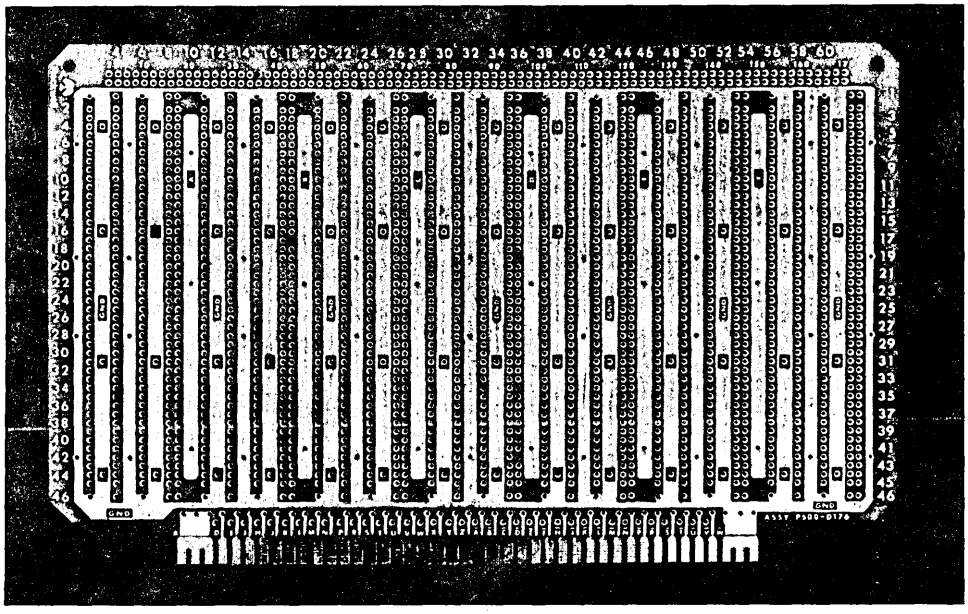
DESIGN PROTOTYPING MODULE

OVERVIEW

The Designing Prototyping Module (Part Number M65-071) allows development of custom circuits for installation in either Rockwell's SYSTEM 65 Microcomputer Development System or in user-designed equipment, via the Auxiliary Card Cage.

This Module is a SYSTEM 65-compatible printed circuit module with no mounted components, but with pre-routed power bus and power return lines. Spaced beside the power lines are plated-through holes that permit wire-wrap sockets to be installed. Additional holes, at the top edge of the Module, permit a variety of wire-wrap flat ribbon cable connectors to be installed.

The pin assignments for the Design Prototyping Module's 86-pin edge connector are identical to the Motherboard pin assignments given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).



DESIGN PROTOTYPING MODULE

SYSTEM 65 DEVELOPMENT SYSTEM

Specifications subject to change without notice
Document No. 29650 N45
Rev. 1, November 1980

INSTALLATION

The procedure below should be used to install a Design Prototyping Module in the SYSTEM 65 or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn SYSTEM 65 power off.

CAUTION

Never install or remove modules with SYSTEM 65 power on — it may cause damage to the module and/or to the System.

2. Remove the top cover of the SYSTEM 65.
3. Insert the Design Prototyping Module into any vacant slot in the SYSTEM 65 chassis.

CAUTION

Installation of improperly-operating circuits may cause malfunction and/or damage to the SYSTEM 65.

4. Install the top cover of the SYSTEM 65.
5. Turn SYSTEM 65 power on.

SPECIFICATIONS

Component Mounting Area:	
Number of Component Rows:	14
Number of Hole Rows:	35
Vertical Hole Spacing:	46 holes on 0.1-in. centers
Horizontal Hole Spacing:	35 holes on either 0.3- in. or 0.1-in. centers
Flat Ribbon Connector Mounting Area:	
Number of Pins Per Connector	170
Module Dimensions:	7.50 in. high x 9.75 in. wide x 0.062 in. thick
Edge Connector:	86 pins on 0.156-in. centers

DOCUMENT NO. 29650 N41
AUGUST 1978

PART NUMBER
M65-060

R6500 Microcomputer System
PRODUCT DESCRIPTION

EXTENDER CARD

OVERVIEW

The Extender Card is used to provide easy access to a printed circuit module installed in its system enclosure, for signal tracing or troubleshooting. In that context, the Extender Card consists of a series of bus lines connecting the Card's standard contact edge, on one end, and a connector used for accepting the standard contact edge of an 86-pin system module.

This contact edge and the edge connector pins are connected pin-for-pin via the bus lines on the Card. Each of the bus lines is provided with a clip-on terminal to allow test equipment to be readily connected. With the module under test connected to the Extender Card and this assembly installed in the system's Auxiliary Card Cage or SYSTEM 65 chassis, the user is given free access to both sides of the module being tested.

The edge connector pin assignments for the SYSTEM 65 Motherboard are given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).

SPECIFICATIONS

Edge Contacts:	86 pins on 0.156-in. centers
Edge Connector:	86 pins on 0.156-in. centers
Extender Card Dimensions:	9.75 in. wide x 9.00 in. high x 0.062 in. thick

INSTALLATION

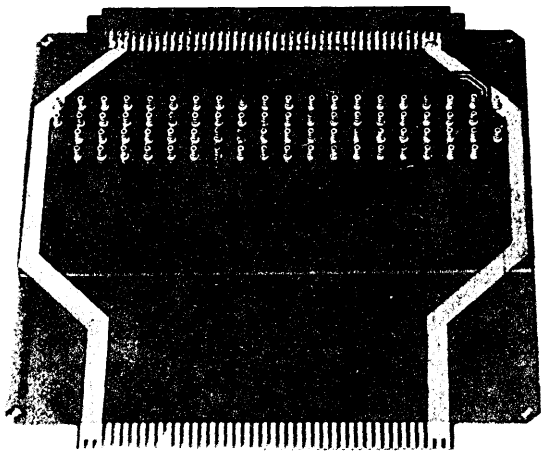
The procedure below should be used to install an Extender Card in the SYSTEM 65 chassis or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn SYSTEM 65 power off.

CAUTION

Never install or remove modules with SYSTEM 65 power on – it may cause damage to the module and/or to the System.

2. Remove the top cover of the SYSTEM 65.
3. Remove the desired circuit module from SYSTEM 65, if installed.
4. Insert the Extender Card into any vacant slot in the SYSTEM 65 chassis.
5. Insert the desired circuit module into the plug on top of the Extender Card.
6. Turn SYSTEM 65 power on.



Specifications subject to change without notice

SYSTEM 65
DEVELOPMENT
SYSTEM

Cut the Cost of Your System Development With . . .

Rockwell

R6500 Macro Assembler and Linking Loader

Macro Assembler Features
- Macro definition and call
- Absolute and relocatable object code
- Conditional assembly capability
- Symbol cross-reference table

Linking Loader Features
- Interactive or command file input
- Generates load map and absolute object code

The R6500 Macro Assembler and Linking Loader (Part No. M65-650) is a minifloppy diskette-based software package to support the Rockwell SYSTEM 65 Microcomputer Development System. The R6500 Macro Assembler translates symbolic source code into absolute or relocatable object code.

The absolute code may be directly executed on any 6500-family CPU—6502, 6503, 6504, etc.— or on the R6500/1 single-chip microcomputer. Absolute and relocatable object files generated by the Macro Assembler can be subsequently combined into a single object file, or "load module", using the Linking Loader. The Macro Assembler and Linking Loader are both written in assembly language, to maximize system efficiency.

The Macro Assembler

The Macro Assembler has all of the features of SYSTEM 65's ROM-resident, two-pass assembler, plus a variety of additional features that are aimed at increasing your programming productivity. It enables a programmer to call repeatedly-used instruction sequences with a single "macro" statement. It also allows large programs to be developed in small, easy-to-handle modules.

And a conditional assembly feature permits sections of source code to be included in (or excluded from) the assembly, depending on certain user-specified parameters. Besides object code, the Macro Assembler generates a cross reference synbol table, which lists the memory address where each label is defined, and the line number of each instruction that references that label.

Assembler Directives

Assembly Listing Control

.TTL	Title	.SKI	Skip
.SBTTL	Subtitle	.ERR	Error
.PAG	Page		

Source File Control

.END	End of Assembly
.FILE	Next File
.INCL	Include

Data Storage

.BYTE	Initialize byte memory location
.WORD	Generate 16-bit address
.DBYTE	Generate 16-bit data word
.SBYTE	Initialize ASCII string

Equate

=	Assign value to symbol

Option Control

.OPT Option

LIST/NOLIST	Assembly listing
GEN/NOGEN	Object code listing
ERR/NOERR	Error generation
SYM/NOSYM	Symbol generation
CREF/NOCREF	Cross reference generation
ABS	Absolute object code
REL	Relocatable object code
MEM	Absolute object code to memory
TOC/NOTOC	Table of contents
OBJ/NOOBJ	Object code generation
MD/NOMD	Macro definition
ME/NOME	Macro expansion
CC/NOCC	Conditional list
PLEN	Page length
LLEN	Line length
FF/NOFF	Form feed
CLS	Clear definitions

.RAD Radix
2, 8, 10, or 16

Relocation/Linking

.DEF	Internal definition
.REF	External reference
.ZREF	Zero page reference
.PSECT	Program section
.IDENT	Module identification

Conditional

.IF	Condition
.ELSE	Complementary condition
.EIF	End of conditional

Macro

.MACRO	Define Macro
.ENDM	End of macro definition
.MEXIT	End of macro expansion
.NARG	Number of passed arguments

SYSTEM 65 DEVELOPMENT SYSTEM

Document No. 29650 N64 April, 1980

The Linking Loader

The Linking Loader combines independently-assembled object modules (absolute or relocatable) into a single, executable object file. Linking commands can be entered interactively from the system terminal or from a previously-prepared command file.

For More Information . . .

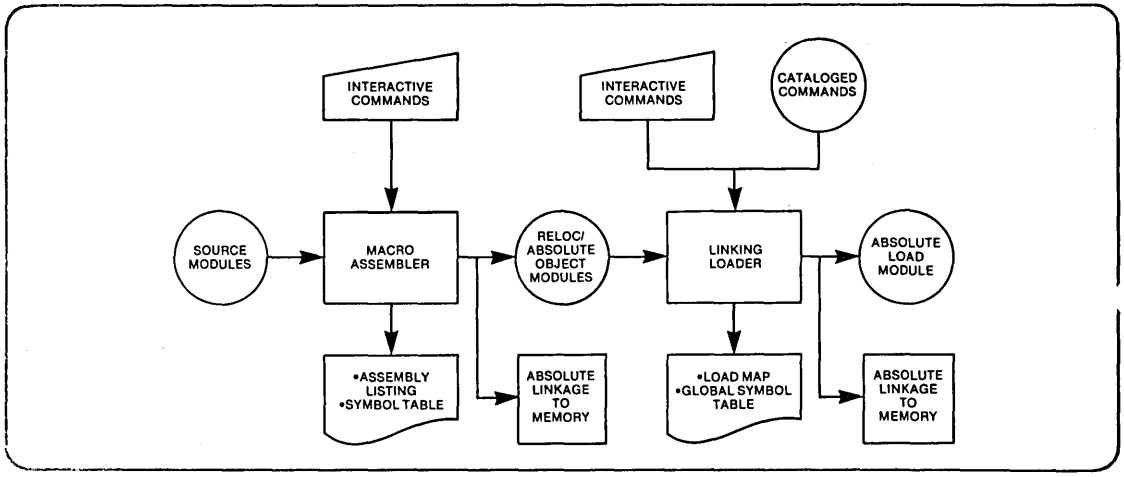
On the R6500 Macro Assembler and Linking Loader (Part No. M65-650), SYSTEM 65, AIM 65 or the rapidly growing family of R6500 products, contact

ROCKWELL INTERNATIONAL
P.O. Box 3669, RC55
Anaheim, CA 92803
Attn: Marketing Services

or phone 714/632-3729.

Linking Loader Directives

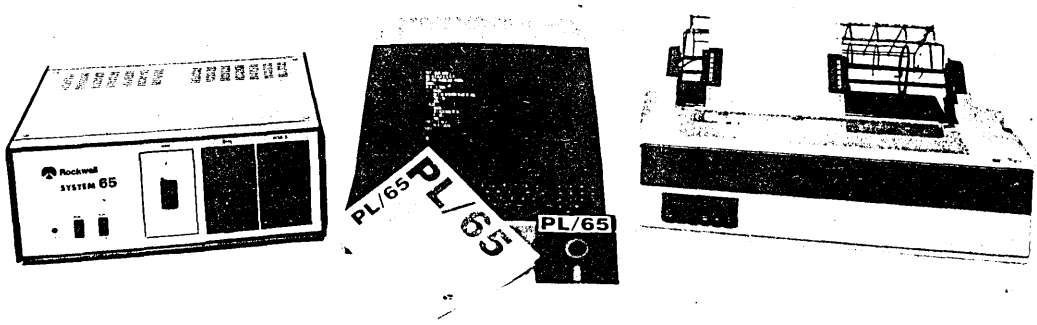
ERR	Errors destination
OBJ	Object code generation
MAP	Load map generation
CALS	Symbol table location
SYM	Global symbol table
DEBUG	Debug symbol table
ORG	Origin
ORDER	Section order
DEF	Symbol definition
LOAD	Load code specification
END	Command file end



Now Rockwell Cuts The Low-Cost of R6500 Designing . . .

Rockwell

PL/65
A High-Level Language for the R6500 Microprocessor Family



In Rockwell's SYSTEM 65, you have one of the industry's most cost-effective microcomputer development systems. By coupling SYSTEM 65 with the advanced low-cost PL/65 Compiler option, you're even further ahead with valuable savings in time, effort and cost.

Resembling PL/1 and ALGOL in general form, PL/65 is designed to improve your productivity and efficiency by simplifying the overall software development effort.

The coding is easier, since PL/65's powerful, high level language statements enable you to implement even complex applications with minimal programming.

Program readability is enhanced by the self-documenting nature of PL/65. This results in programs that are easier to understand. These programs are easier to update, too, which means lower maintenance costs.

Rockwell International

PL/65 = Software Simplification

All language features are aimed at improving productivity by simplifying software development. PL/65's structured programming support features encourage modular program design, and its general control structure for conditional and iterative looping allows the language to be applied to highly structured programs.

Coding Flexibility . . . When You Need It Most

PL/65 allows you to freely mix assembly language instructions in portions of the program where timing or code optimization requirements are critical.

This flexibility carries through the compile cycle: The PL/65 compiler outputs source code to SYSTEM 65's resident assembler, rather than object code. You'll be able to enhance or debug at the assembler level and indeed to drop into assembly language whenever you desire — a big plus in structured programming. PL/65 thereby provides the structuring potential and programming simplicity of a high-level language, while retaining the power and flexibility of an assembler.

No "Hidden" Memory Costs With PL/65

And while other microcomputer high-level languages require adding more memory to the host development system, PL/65 runs with only 16K bytes of RAM — and that comes **standard** with every SYSTEM 65 as do the dual minifloppy disk drives.

For PDP 11 Users

A PL/65 Compiler and an R6500 cross-assembler are also available for installation using the RT-11 operating system.

The PL/65 Package

A pre-programmed minifloppy diskette and the comprehensive PL/65 User's Manual is available now from Rockwell and your local Hamilton/Avnet distributor.

For more information on PL/65, SYSTEM 65, AIM 65, or the rapidly growing family of R6500 products, contact

ROCKWELL INTERNATIONAL
Microelectronic Devices
P.O. Box 3669
Anaheim, CA 92803
Attn: Marketing Services
D/727 RC55

or phone 714/632-3729.

PL/65 LANGUAGE STATEMENTS

Declaration	Specification
DECLARE	ENTRY
DEFINE	EXIT
DATA	
Comment	Conditional
Assignment	IF-THEN-ELSE
	IF-THEN
Single-Byte Move	BEGIN-END
Multiple-Byte Move	CASE
Imperative	Branching
SHIFT	GOTO
ROTATE	CALL
CLEAR	RETURN
SET	RTI
CODE	BREAK
HALT	
WAIT	Looping
STACK	
UNSTACK	FOR-TO-BY
INC	WHILE
INCW	
DEC	
DECW	
PULSE	

NMOS MEMORY PRODUCTS

NMOS
MEMORY
PRODUCTS

DOCUMENT NO. 29000 D43
REVISION 3, MAY 1979

PART NUMBERS
R2316B and R2316E

Rockwell

R6500 Microcomputer System
DATA SHEET

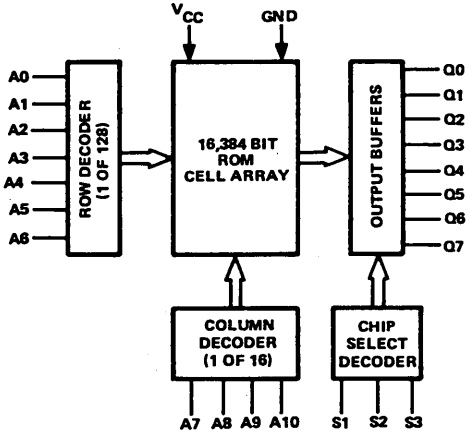
2048 X 8 STATIC READ ONLY MEMORY

DESCRIPTION

The R2316B and R2316E high performance read only memories are organized 2048 words by 8 bits with access times of less than 450 ns. These ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

The R2316B and R2316E operate totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. The R2316E features a high-speed chip select response for use in time-critical applications such as multiplexed control lines. Both devices offer three-state output buffers for memory expansion.

Designed to replace two 2708 8K EPROMs, the R2316B and R2316E can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.



Block Diagram

FEATURES

- 2048 x 8 Bit Organization
- Single +5Volt Supply
- Max. Access Time — 450 ns
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- Chip Select Times
  - — 250 ns max for R2316B
  - — 120 ns max for R2316E

Ordering Information

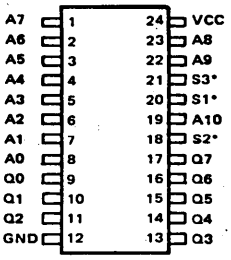
Order Number: R2316 ___

Temperature Range:
- No suffix = 0°C to +70°C
- E = -40°C to +85°C (Industrial)
- MT = -55°C to +125°C (Military)
- M = MIL-STD-883, Class B

Package:
- C = Ceramic
- P = Plastic (Not Available for M or MT suffix)

Model:
- B = 2316B
- E = 2316E

NOTE: Contact your local Rockwell Representative for availability.



*Mask Programmable Option S/$\overline{S}$/NC

Pin Configuration

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature	T_A		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Military		-55 to +125	
Storage Temperature	T_{STG}	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics

V_{CC} = 5.0V ±10% (unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	Volts	V_{CC} = 4.5V, I_{OH} = -200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	μA	V_{CC} = 5.5V, 0V ≤ V_{in} ≤ 5.5V
I_{LO}	Output Leakage Current		±10	μA	Chip Deselected, V_{CC} = 5.5V V_{out} = +0.4V to V_{CC}
I_{CC}	Power Supply Current		65	mA	0°C to 70°C
			75		-40°C to +85°C
			80		-55°C to +125°C
					Output Unloaded
					V_{CC} = 5.5V, V_{in} = V_{CC}
C_I	Input Capacitance		7	pF	All pins except pin under test tied to AC ground except V_{CC} = 5.5V
C_O	Output Capacitance		10	pF	T_A = 25°C, f = 1.0 MHz, See Note 2

Note 1: Input levels that swing more negative than -0.5V may be clamped and may cause damage to the device.

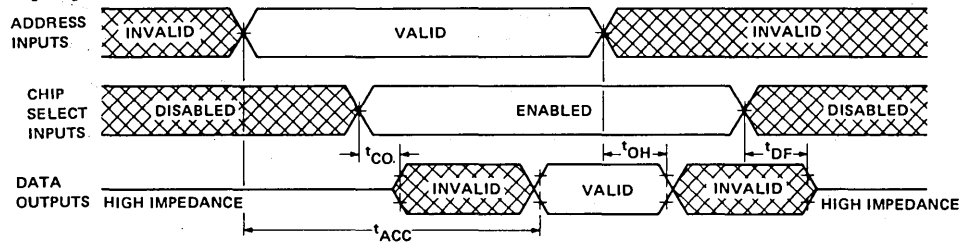
Note 2: This parameter is periodically sampled and is not 100% tested.

Timing Characteristics

V_{CC} = 5.0V ±10% (unless otherwise specified)

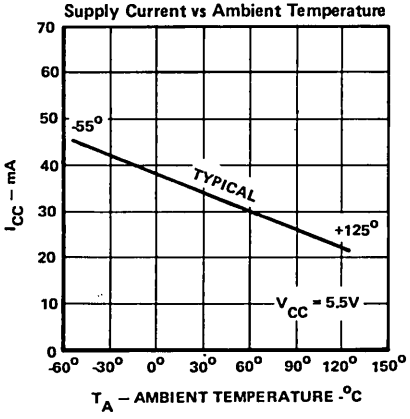
Symbol	Parameter	R2316B		R2316E		Units	Test Conditions
		Min	Max	Min	Max		
t_{ACC}	Address Access Time		450 475 550		450 475 550	ns	0°C to 70°C -40°C to 85°C -55°C to 125°C Output load: 1 TTL load and 100 pF
t_{CO}	Chip Select Delay		250		120	ns	
t_{DF}	Chip Deselect Delay	10	250		100	ns	Input transition time: 20 ns
t_{OH}	Previous Data Valid After Address Change Delay	20		20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

Timing Diagram

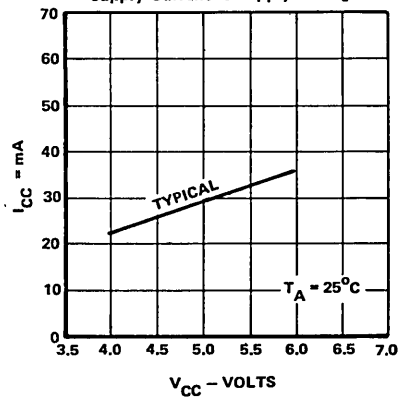


Typical Characteristics

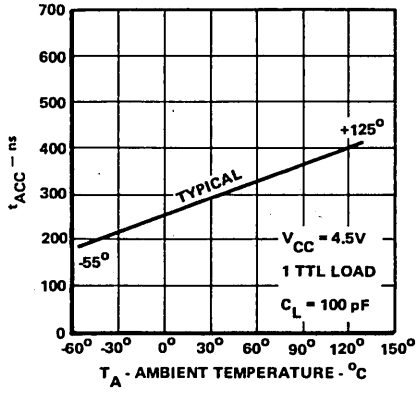
Supply Current vs Ambient Temperature



Supply Current vs Supply Voltage



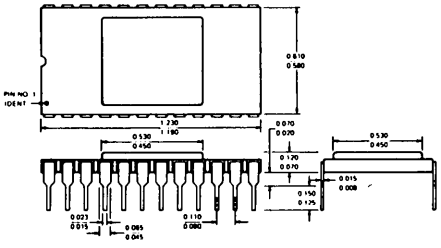
Access Time vs Ambient Temperature



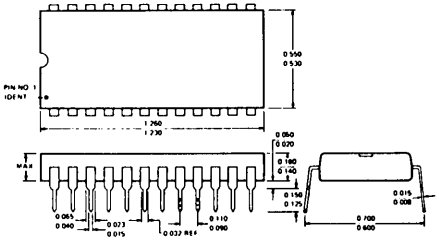
NMOS MEMORY PRODUCTS

Packaging Diagram

Ceramic Package



Plastic Package



NMOS
MEMORY
PRODUCTS

Rockwell

DATA SHEET

4096 X 8 STATIC READ ONLY MEMORY

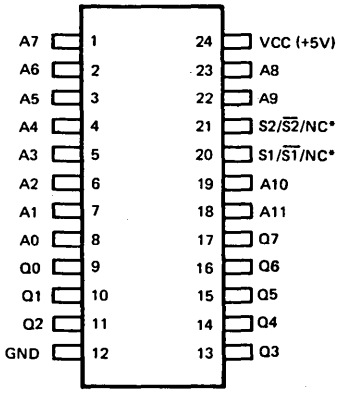
DESCRIPTION

The R2332 is a high performance, 32,768-bit static Read Only Memory, organized as 4,096 eight-bit bytes. It is available in two versions: R2332-25, which has a 250-ns access time, and R2332-3, which has a 300-ns access time. The device is an industry standard, 24-pin, dual-in-line package, and is available in ceramic or low cost plastic packages. This fully static 32K ROM is compatible with all eight bit N-channel microprocessors including the R6500 family of microprocessors.

The R2332 operates totally asynchronously; no clock input is required. Two mask-programmable chip select inputs allow up to four R2332 32K ROMs to be OR-tied without external decoding. The device provides three-state output buffers for memory expansion. The R2332 offers TTL input and output levels with a minimum noise immunity of 0.4 volts.

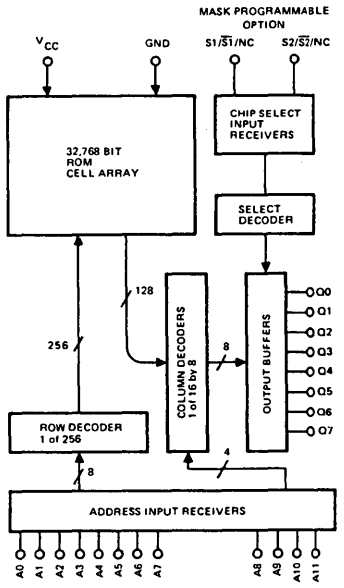
FEATURES

- 32,768 bits, organized in 4,096 8-bit words
- Max access time: 250 ns for R2332-25
  300 ns for R2332-3
- Typical power dissipation is 350 mW
- Drives one TTL load and 100 pF
- Single +5-volt power input
- Totally static operation, no clock input required
- Completely TTL compatible
- Two mask-programmable chip select inputs
- Three state outputs for memory expansion
- Identical cycle and access time



*Mask-programmable option

R2332 Pin Configuration



R2332 Block Diagram

Order Number: R2332-

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = −40°C to +85°C (industrial)
- Package:
  - C = Ceramic
  - P = Plastic
- Access Time (Max):
  - 25 = 250 ns t_{ACC}
  - 3 = 300 ns t_{ACC}

NOTE: Contact your local Rockwell Representative for availability. Submit ROM codes using the Rockwell NMOS ROM Code Order Form, Document No. 29650 N80.

Specifications subject to Change without notice
Document No. 29000 D48
Rev. 4, August 1980

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{in}	-0.5 to +7.0	Vdc
Operating Temperature	T_A		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Storage Temperature	T_{STG}	-65 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics

V_{CC} = 5.0V ± 5% (unless otherwise specified)

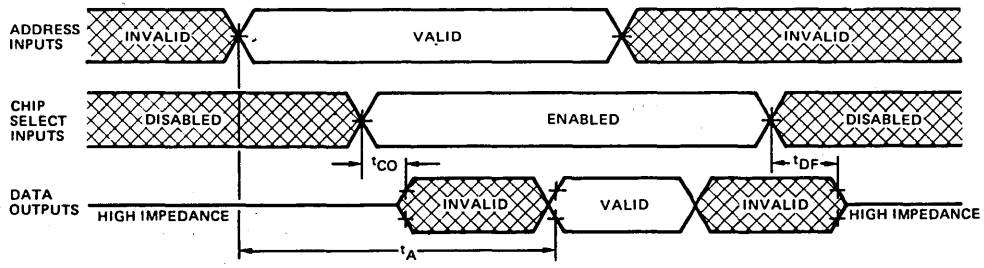
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	Volts	V_{CC} = 4.75V, I_{OH} = -200 µA
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5		0.8	Volts	
I_{LI}	Input Load Current			10	µA	V_{CC} = 5.25V, 0V ≤ V_{in} ≤ 5.25V
I_{LO}	Output Leakage Current			±10	µA	Chip Deselected, V_{CC} = 5.25V, V_{out} = +0.4V to V_{CC}
I_{CC}	Power Supply Current				mA	V_{CC} = 5.25V
	Commercial Temp		70	135		
	Industrial Temp		70	150		
C_I	Input Capacitance			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C, f = 1 MHz
C_O	Output Capacitance			10	pF	

Timing Characteristics

V_{CC} = 5.0V ± 5% (unless otherwise specified)

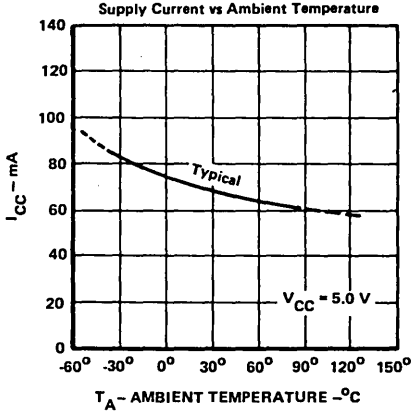
Symbol	Parameter	R2332-25 Max	R2332-3 Max	Units	Test Conditions
t_A	Address Access Time	250	300	ns	Output load: 1 TTL load, 100 pf Input transition time: 20 ns
t_{CO}	Chip Select Delay	150	150	ns	Timing reference levels: Input: 1.5V
t_{DF}	Chip Deselect Delay	150	150	ns	Output: 0.8V & 2.0V

Timing

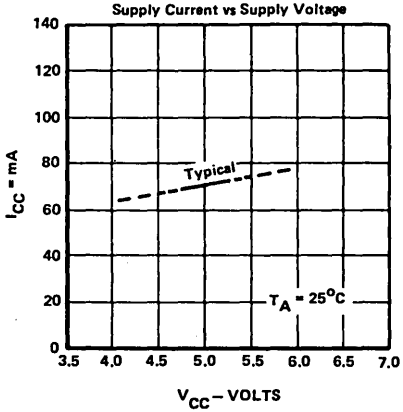


Typical Characteristics

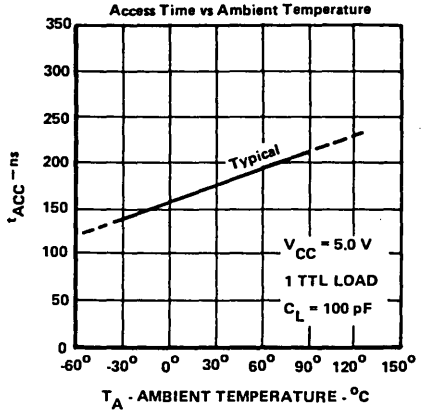
Supply Current vs Ambient Temperature



Supply Current vs Supply Voltage



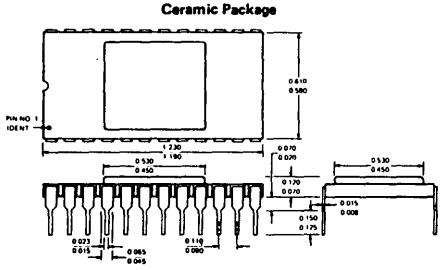
Access Time vs Ambient Temperature



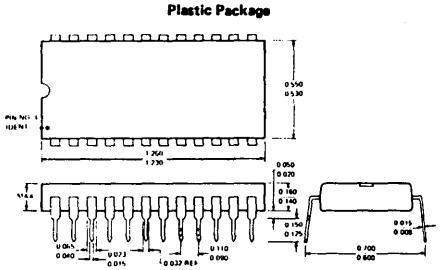
NMOS MEMORY PRODUCTS

Packaging Diagram

Ceramic Package



Plastic Package



NMOS
MEMORY
PRODUCTS

Rockwell

DATA SHEET

LOW-POWER
4096 x 8 STATIC READ ONLY MEMORY

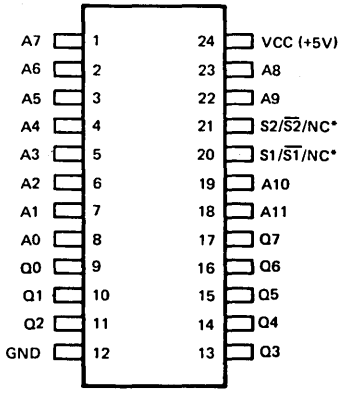
DESCRIPTION

The R2332-L, R2332-4L and R2332-35L are 32,768-bit static Read Only Memories (ROMs), organized as 4,096 eight-bit bytes, that offer maximum access times of 450, 400 and 350 nanoseconds, respectively. Like their high-speed counterparts, the R2332-25 and the R2332-3 (see Rockwell Document No. 29000 D48), these ROMs are in industry-standard, 24 pin, dual in-line packages, and are available in ceramic or low-cost plastic. However, R2332-xL series ROMs operate with a typical power dissipation of only 240 mW.

All three R2332-xL ROMs operate asynchronously, and require no clock input. Two mask-programmable chip select inputs allow up to four 32K ROMs to be OR-tied without external decoding. These devices provide tri-state output buffers for memory expansion. The R2332-xL ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

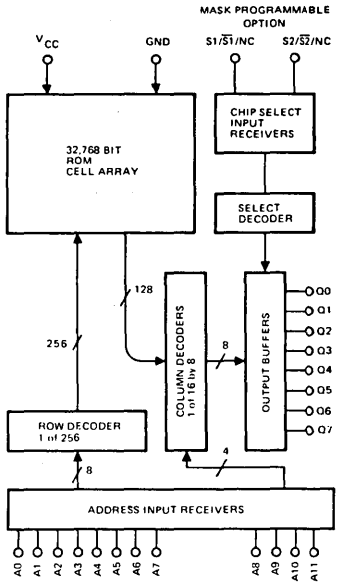
FEATURES

- 32,768 bits, organized in 4,096 8-bit bytes
- Max access time: 450 ns for R2332-L
  400 ns for R2332-4L
  350 ns for R2332-35L
- Typical power dissipation is 240 mW
- Drives two TTL loads and 100 pF
- Single +5-volt power input
- Totally static operation, no clock input required
- Completely TTL compatible
- Two mask-programmable chip select inputs
- Three state outputs for memory expansion
- Identical cycle and access time



*Mask-programmable option

R2332 Pin Configuration



R2332 Block Diagram

Ordering Information

Order Number: R2332-_ _L_ _

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = -40°C to +85°C (Industrial, available only for R2332-L)
- Package:
  - C = Ceramic
  - P = Plastic
- Access Time (Max):
  - No prefix = 450 ns t_{ACC}
  - 4 = 400 ns t_{ACC}
  - 35 = 350 ns t_{ACC}

NOTE: Contact your local Rockwell Representative for availability. Submit ROM codes using the Rockwell NMOS ROM Code Order Form, Document No. 29650 N80.

LOW-POWER 4096 x 8 STATIC READ ONLY MEMORY

NMOS MEMORY PRODUCTS

Specifications subject to change without notice
Document No. 29000 D61
August 1980

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{in}	-0.5 to +7.0	Vdc
Operating Temperature	T_A		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Storage Temperature	T_{STG}	-65 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics for R2332-L and R2332-4L

V_{CC} = 5.0V ±10% (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	Volts	V_{CC} = 4.5V, I_{OH} = -240 µA
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = 4.5V, I_{OL} = 3.7 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5		0.8	Volts	
I_{LI}	Input Load Current			10	µA	V_{CC} = 5.5V, 0V ≤ V_{in} ≤ 5.5V
I_{LO}	Output Leakage Current			±10	µA	Chip Deselected, V_{CC} = 5.5V, V_{out} = +0.4V to V_{CC}
I_{CC}	Power Supply Current				mA	V_{CC} = 5.5V
	Commercial Temp		48	87		
	Industrial Temp		48	101		
C_I	Input Capacitance			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C, f = 1 MHz
C_O	Output Capacitance			10	pF	

Electrical Characteristics for R2332-35L

V_{CC} = 5.0V ± 5% (unless otherwise specified)

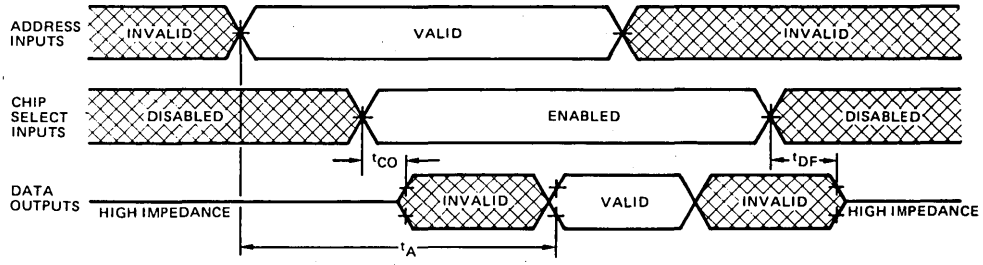
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	Volts	V_{CC} = 4.75V, I_{OH} = -240 µA
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = 4.75V, I_{OL} = 3.7 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5		0.8	Volts	
I_{LI}	Input Load Current			10	µA	V_{CC} = 5.25V, 0V ≤ V_{in} ≤ 5.25V
I_{LO}	Output Leakage Current			±10	µA	Chip Deselected, V_{CC} = 5.25V, V_{out} = +0.4V to V_{CC}
I_{CC}	Power Supply Current				mA	V_{CC} = 5.25V
	Commercial Temp		48	87		
C_I	Input Capacitance			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C, f = 1 MHz
C_O	Output Capacitance			10	pF	

Timing Characteristics

V_{CC} = 5.0V ±10% for R2332-L and R2332-4L, V_{CC} = 5.0V ±5% for R2332-35L

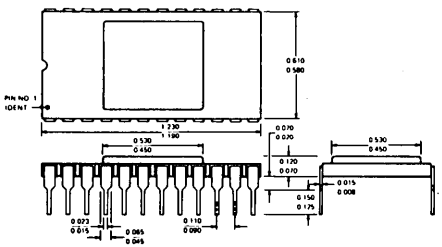
Symbol	Parameter	R2332-L Max	R2332-4L Max	R2332-35L Max	Units	Test Conditions
t_A	Address Access Time				ns	Output load:
	Commercial Temp	450	400	350		2 TTL loads, 100 pF
	Industrial Temp	450	–	–		Input transition time: 20 ns
t_{CO}	Chip Select Delay	120	120	120	ns	Timing reference levels:
						Input: 1.5V.
t_{DF}	Chip Deselect Delay	100	100	100	ns	Output: 0.8V & 2.0V

Timing

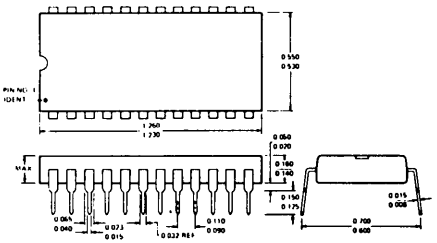


Packaging Diagram

Ceramic Package

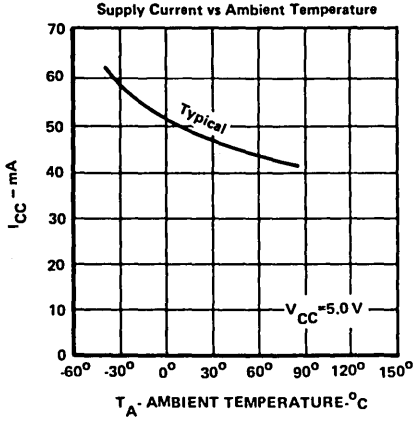


Plastic Package

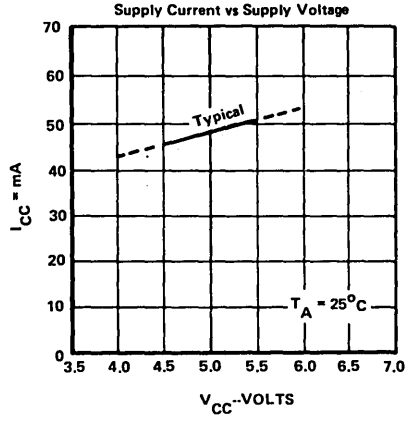


Typical Characteristics

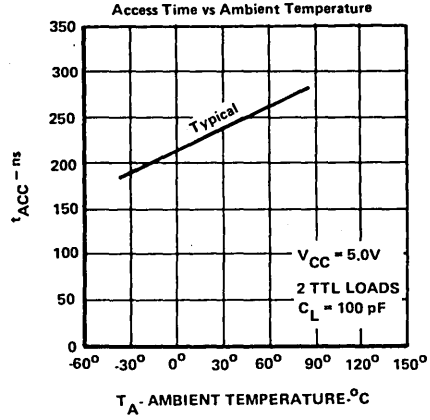
Supply Current vs Ambient Temperature



Supply Current vs Supply Voltage



Access Time vs Ambient Temperature



PART NUMBERS
R2364A2, R2364A25, R2364A3

Rockwell

PRODUCT PREVIEW

8192 X 8 STATIC READ ONLY MEMORY

The R2364A2, R2364A25 and R2364A3 are 65,536-bit static Read-Only Memories (ROMs), organized as 8,192 eight-bit bytes, that offer maximum access times of 200, 250 and 300 nanoseconds, respectively. These ROMs are in industry-standard 28-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 64K-bit ROMs are compatible with all eight-bit N-channel microprocessors, including the R6500 family of microprocessors.

All three R2364A ROMs operate totally asynchronously, and require no clock input. These devices provide tri-state output buffers for memory expansion. The R2364A ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The mask-programmable chip enable input (E) may be programmed to function as a chip select with no power down or as a chip select with power down (standby mode). The active level of the enable input is also programmable.

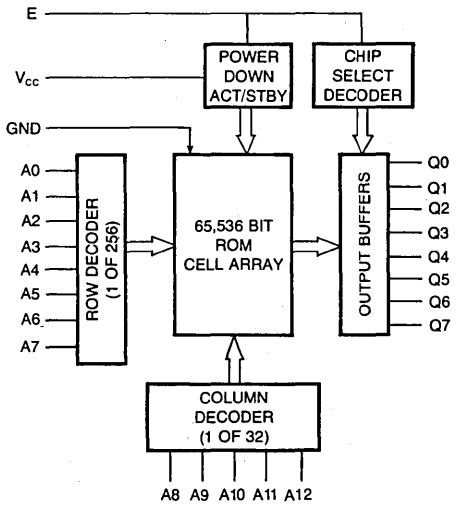
FEATURES

- 65,536 bits, organized as 8,192 eight-bit bytes
- Max. access time: 200 ns for R2364A2
  250 ns for R2364A25
  300 ns for R2364A3
- Low typical power dissipation is 125 mW active, 37.5 mW standby
- Drives two TTL loads and 100 pf
- Single +5-volt power input
- Totally static operation, no input clock required
- Completely TTL compatible
- Mask-programmable chip enable
- Three state outputs for memory expansion
- Identical cycle and access time

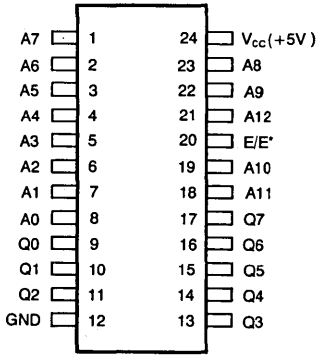
Ordering Information

Order Number: R2364A

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = −40°C to +85°C (industrial)
- Package:
  - C = Ceramic
  - P = Plastic
- Access Time (Max):
  - 2 = 200 ns t_{ACC}
  - 25 = 250 ns t_{ACC}
  - 3 = 300 ns t_{ACC}



R2364A Block Diagram



*Mask-programmable option

R2364A Pin Configuration

8192 X 8 STATIC READ ONLY MEMORY (ROM)

NMOS MEMORY PRODUCTS

Specifications subject to change without notice
Document No. 29000 D63
September 1980

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{in}	−0.5 to +7.0	Vdc
Operating Temperature	T		°C
Commercial		0 to +70	
Industrial		−40 to +85	
Storage Temperature	T_{STG}	−65 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics

V_{CC} = 5.0V ± 10% (unless otherwide specified)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	Volts	V_{CC} = 4.5V, I_{OH} = −400 μA
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = 4.5V, I_{OL} = 3.3 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	Volts	
V_{IL}	Input LOW Voltage	−0.5		0.8	Volts	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{in} ≤ 5.5V
I_{LO}	Output Leakage Current			±10	μA	Chip Deselected, V_{CC} = 5.5V, V_{out} = +0.4V to V_{CC}
I_{CC}	Power Supply Current, Active		25	55	mA	V_{CC} = 5.5V, −40°C to +85°C
I_{SB}	Power Supply Current, Standby		7.5	16	mA	V_{CC} = 5.5V, −40°C to +85°C
C_I	Input Capacitance		5		pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C
C_O	Output Capacitance		7		pF	f = 1MHz

Rockwell

PRODUCT PREVIEW

8192 X 8 STATIC READ ONLY MEMORY

The R2364B2, R2364B25 and R2364B3 are 65,536-bit static Read-Only Memories (ROMs), organized as 8,192 eight-bit bytes, that offer maximum access times of 200, 250 and 300 nanoseconds, respectively. These ROMs are in industry-standard 28-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 64K-bit ROMs are compatible with all eight-bit N-channel microprocessors, including the R6500 family of microprocessors.

All three R2364G ROMs operate totally asynchronously, and require no clock input. Three mask-programmable chip select inputs allow up to eight 64K ROMs to be OR-tied without external decoding. These devices provide tri-state output buffers for memory expansion. The R2364B ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The mask-programmable chip enable input (E) may be programmed to function as a chip select with no power down or as a chip select with power down (standby mode). The active level of the enable input is also programmable.

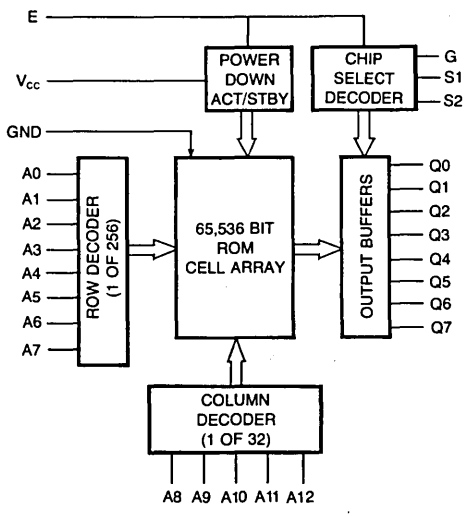
FEATURES

- 65,536 bits, organized as 8,192 eight-bit bytes
- Max. access time: 200 ns for R2364B2
  250 ns for R2364B25
  300 ns for R2364B3
- Low typical power dissipation is 125 mW active, 37.5 mW standby
- Drives two TTL loads and 100 pf
- Single +5-volt power input
- Totally static operation, no input clock required
- Completely TTL compatible
- Three mask-programmable chip select inputs
- Mask-programmable chip enable
- Three state outputs for memory expansion
- Identical cycle and access time

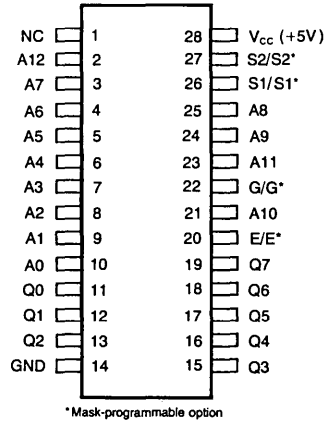
Ordering Information

Order Number: R2364B ___

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = −40°C to +85°C (industrial)
- Package:
  - C = Ceramic
  - P = Plastic
- Access Time (Max):
  - 2 = 200 ns t_{ACC}
  - 25 = 250 ns t_{ACC}
  - 3 = 300 ns t_{ACC}



R2364B Block Diagram



*Mask-programmable option

R2364B Pin Configuration

8192 X 8 STATIC READ ONLY MEMORY (ROM)

NMOS MEMORY PRODUCTS

Specifications subject to change without notice
Document No. 29000 D62
September 1980

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{in}	−0.5 to +7.0	Vdc
Operating Temperature	T		°C
Commercial		0 to +70	
Industrial		−40 to +85	
Storage Temperature	T_{STG}	−65 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics

V_{CC} = 5.0V ± 10% (unless otherwide specified)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	Volts	V_{CC} = 4.5V, I_{OH} = −400 μA
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = 4.5V, I_{OL} = 3.3 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	Volts	
V_{IL}	Input LOW Voltage	−0.5		0.8	Volts	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{in} ≤ 5.5V
I_{LO}	Output Leakage Current			±10	μA	Chip Deselected, V_{CC} = 5.5V, V_{out} = +0.4V to V_{CC}
I_{CC}	Power Supply Current, Active		25	55	mA	V_{CC} = 5.5V, −40°C to +85°C
I_{SB}	Power Supply Current, Standby		7.5	16	mA	V_{CC} = 5.5V, −40°C to +85°C
C_I	Input Capacitance		5		pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C
C_O	Output Capacitance		7		pF	f = 1MHz

PART NUMBERS
R8104-R8114

Rockwell

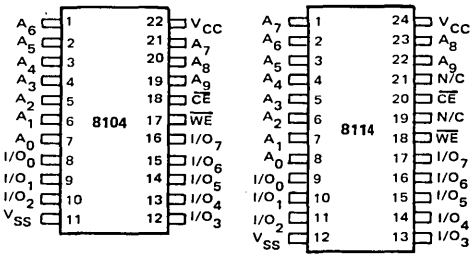
DATA SHEET

1024 X 8 STATIC RAMs

GENERAL DESCRIPTION

The R8104 and R8114 devices are 1024 x 8 "byte-wide" static RAMs. Both devices are available with a maximum access time of 200, 300 or 400 nanoseconds.

The non-latched write function allows input data to be stable after WE is asserted — a feature ideally suited for microprocessor applications. Chip Enable ($\overline{CE}$) latches the address, while data-in is latched by the trailing edge of Write Enable ($\overline{WE}$). The devices provide common data input/output pins for connection to a data bus. It operates on a single +5V power supply and all input/outputs are TTL compatible. The device dissipates less than 30 mW when in standby mode with $\overline{CE}$ negated.



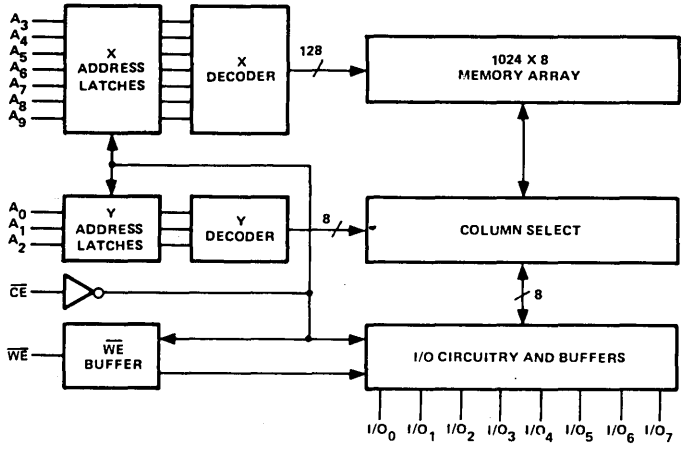
Pin Configurations

FEATURES

- 1024 bytes
- EPROM, PROM, ROM pinout compatible
- Non-latched Write Function
- Ideal for microprocessor applications
- Common I/O bus
- Single +5V power supply
- 200, 300, 400 nsec access times
- Less than 30 mW power (disabled)
- Less than 135 mW power (enabled)
- Available in either 22-pin or 24-pin dual-in-line packages

Order Number: R8104- or R8114- ___

- Package:
  - C = Ceramic
  - P = Package
- Max. Enabled Current
  - No suffix = 50 mA
  - L = 25 mA
- Access Time (Max.)
  - 2 = 200 ns
  - 3 = 300 ns
  - 4 = 400 ns



R8104/R8114 Block Diagram

Specifications subject to change without notice
Document No. 29000 D69
June 1981

Recommended Operating Conditions: (T_{AMB} = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Level	V_{IH}	2.0	–	5.25	V
Input Low Level	V_{IL}	-0.5	–	0.8	V

DC Characteristics: T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise noted

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Output HIGH Voltage	V_{OH}	2.4	–	5.25	V	I_{OH} = -200 μA (NOTE 1)
Output LOW Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 2.1 mA (NOTE 2)
Output Leakage Current	I_{LO}	-10	–	+10	μA	V_{OL} = 0.4V to V_{CC} $\overline{CE}$ = $\overline{WE}$ = 2.0V
Input Leakage Current	I_{LI}	-10	–	+10	μA	V_{IN} = 0 to 5.25V (A_n, CE, WE, Only)
Power Supply Current (Device Disabled) 8104/8114	I_{CC1}	–	5	10	mA	$\overline{CE}$ ≥2.0V
Power Supply Current (Device Enabled) 8104/8114	I_{CC2}	–	25	50	mA	$\overline{CE}$ ≤0.8V
Power Supply Current (Device Disabled) 8104L/8114L	I_{CC1}	–	–	5	mA	$\overline{CE}$ ≥2.0V
Power Supply Current (Device Enabled) 8104L/8114L	I_{CC2}	–	–	25	mA	$\overline{CE}$ ≤0.8V

AC Characteristics: T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise noted

Read Cycle

CHARACTERISTICS	SYMBOL	8104/8114-2		8104/8114-3		8104/8114-4		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	T_C	350	–	450	–	700	–	nS
Chip Enable Pulse Width	T_{CE}	200	∞	300	∞	400	∞	nS
Chip Enable Rise and Fall Time (NOTE 2)	T_{CR}, T_{CF}	–	100	–	100	–	100	nS
Address Set Up Time	T_{AS}	0	–	0	–	0	–	nS
Access Time	T_A	–	200	–	300	–	400	nS
Address Hold Time	T_{AH}	100	–	100	–	200	–	nS
Output Hold Time	T_{OH}	20	100	20	100	20	100	nS
Recovery Time	T_P	130	–	130	–	280	–	nS

Write Cycle

CHARACTERISTICS	SYMBOL	8104/8114-2		8104/8114-3		8104/8114-4		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	T_C	350	–	450	–	700	–	nS
Chip Enable Pulse Width	T_{CE}	200	∞	300	∞	400	∞	nS
Chip Enable Rise and Fall Time (NOTE 2)	T_{CR}, T_{CF}	–	100	–	100	–	100	nS
Address Set Up Time	T_{AS}	0	–	0	–	0	–	nS
Address Hold Time	T_{AH}	100	–	100	–	200	–	nS
Recovery Time	T_P	130	–	130	–	280	–	nS
Write Enable Pulse Width	T_{WP}	175	–	175	–	225	–	nS
Write Enable Delay Time	T_{WD}	–	25	–	25	–	25	nS
Write Data Hold Time	T_{DH}	15	–	15	–	15	–	nS
Data Set Up Time	T_{DS}	75	–	75	–	100	–	nS

Capacitance

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
Input Capacitance	C_{IN}	–	5	pF	$\overline{CE}$ = 2V
Output Capacitance	C_{OUT}	–	5	pF	$V_{I/O}$ = 0.4V

NOTE 1: Output terminated per Test Output Load diagram. Any valid combination of input voltages, V_{CC}, and temperature

NOTE 2: Typical Chip Enable Rise and Fall Time (T_{CR} and T_{CF}) is 10 nS for Read and Write Cycle

Absolute Maximum Ratings

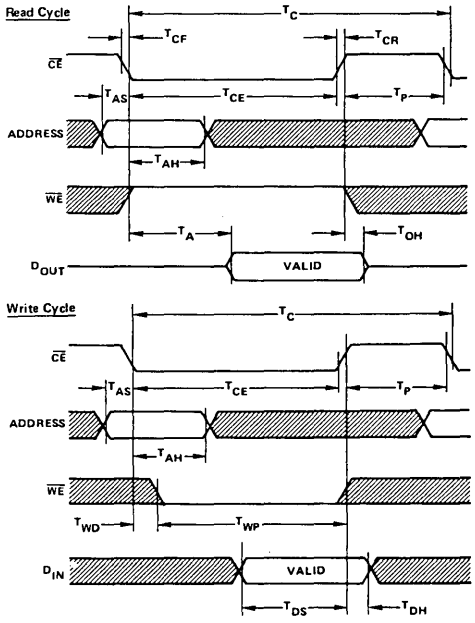
(See NOTE 1) (Referenced to V_{SS})

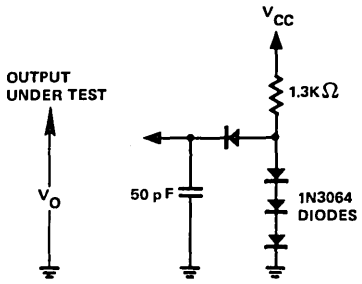
Rating	Value	Unit
Voltage to Any Pin With Respect to V_{SS}	-0.5 to +7.0	Vdc
Power Dissipation	1.6 (NOTE 2)	W
Current Into/From Output	50	mA
Operating Ambient Temperature Range (T_{AMB})	0 to 70	°C
Storage Temperature (T_{STOR})	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25°C Ambient Derate 13.5 mW/°C.





Test Output Load

FUNCTIONAL DESCRIPTION

The R8104 and R8114 are 8192-bit Static RAMs with memory cells organized in eight arrays of 128 rows by 8 columns (1024 x 8 bits). Each eight-bit byte is addressed by simultaneously decoding the X addresses (A3 through A9) for the rows, and the Y addresses (A0 through A2) for the columns. Data is written or read in parallel on eight common input/output pins. Operation of the 8104 and 8114 is controlled by Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$).

When $\overline{CE}$ is high, all outputs are in a high impedance state, and power is supplied only to the memory elements. When $\overline{CE}$ is low, the memory is enabled for reading and writing.

The negative going edge of $\overline{CE}$ begins timing for a read or a write cycle. Address and $\overline{WE}$ must be stable for T_{AS} prior to $\overline{CE}$ being asserted. Data on address pins A0-A9 are latched into "D" type flip-flops and no longer need to be held stable. $\overline{WE}$, however, must be held stable throughout the cycle. For a read cycle ($\overline{WE}$ = high), data will be available on the data I/O pins within time T_A of $\overline{CE}$ asserted, and will remain valid until time T_{OH} after $\overline{CE}$ is negated.

For a write cycle ($\overline{WE}$ = low), data being written must be stable for T_{DS} prior to $\overline{CE}$ returning high, and must remain stable for time T_{DH}.

Truth Table

$\overline{CE}$	$\overline{WE}$	I/O_n	Status	Mode
H	Don't Care	High Z	Disabled	Standby
L	H	Data	Enabled	Read
L	L	L	Enabled	Write 0
L	L	H	Enabled	Write 1

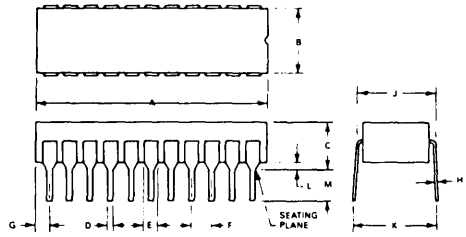
PACKAGING DIMENSIONS

R8104 (22 Pin) Dimensions

PLASTIC PACKAGE

Dim.	Millimeters		Inches	
	Min	Max	Min	Max
A	27.940	29.718	1.100	1.170
B	8.636	9.144	0.340	0.360
C	4.318	5.080	0.150	0.180
D	0.356	0.559	0.014	0.022
E	1.016	1.778	0.040	0.070
F	2.413	2.667	0.095	0.105
G	1.016	2.032	0.040	0.080
H	0.203	0.305	0.008	0.012
J	9.144	10.160	0.360	0.400
K	10.160	REF.	0.400	REF.
L	0.508	1.016	0.020	0.040
M	2.540	3.937	0.100	0.155

Typical Outline Drawing

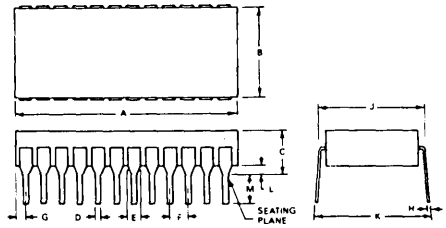


R8114 (24 Pin) Dimensions

PLASTIC PACKAGE

Dim.	Millimeters		Inches	
	Min	Max	Min	Max
A	31.369	32.131	1.235	1.265
B	12.954	13.462	0.510	0.530
C	3.937	5.588	0.155	0.215
D	0.381	0.584	0.015	0.023
E	1.016	1.651	0.040	0.065
F	2.286	2.794	0.090	0.110
G	0.381	1.270	0.015	0.050
H	0.203	0.305	0.008	0.012
J	15.240	15.748	0.600	0.620
K	15.748	16.764	0.640	0.660
L	0.381	1.016	0.015	0.040
M	2.540	4.064	0.100	0.160

Typical Outline Drawing



R68000
16-BIT μP
PRODUCTS

R68000
16-BIT μP
PRODUCTS

Rockwell

R68000 Microcomputer System
PRODUCT DESCRIPTION

16-BIT MICROPROCESSING UNIT

Advances in semiconductor technology have provided the capability to place on a single silicon chip a microprocessor at least an order of magnitude higher in performance and circuit complexity than has been previously available. The R68000 is the first of a family of such VLSI microprocessors from Rockwell. It combines state-of-the-art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessor.

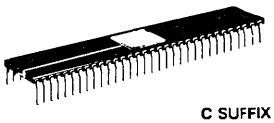
The resources available to the R68000 user consist of the following:

- 32-Bit Data and Address Registers
- 16 Megabyte Direct Addressing Range
- 56 Powerful Instruction Types
- Operations on Five Main Data Types
- Memory Mapped I/O
- 14 Addressing Modes

As shown in the programming model, the R68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0-A6) and the system stack pointer may be used as software stack pointers and base address registers. In addition, these registers may be used for word and long word address operations. All 17 registers may be used as index registers.

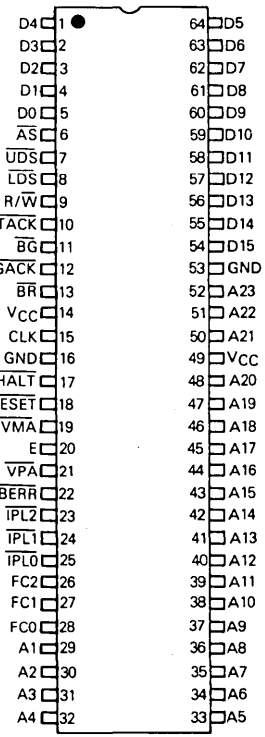
The R68000 microprocessor is available in three models:

- R68000C4 (4 MHz)
- R68000C6 (6 MHz)
- R68000C8 (8 MHz)

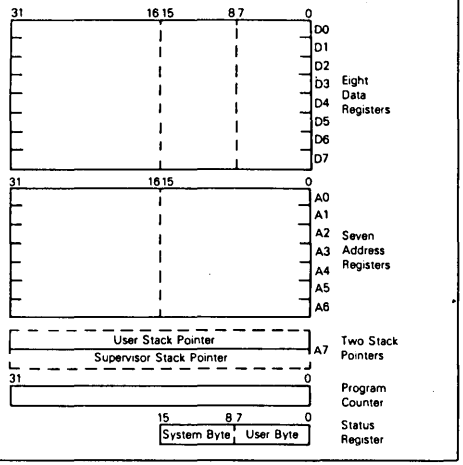


C SUFFIX
CERAMIC PACKAGE

PIN ASSIGNMENT



PROGRAMMING MODEL



16-BIT MICROPROCESSING UNIT

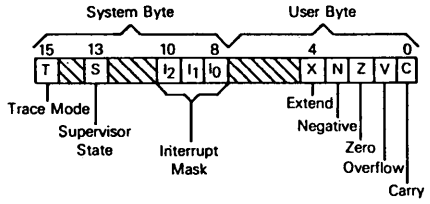
R68000 16-BIT μP PRODUCTS

Specifications subject to change without notice
Document No. 68650 N01
Rev. 1, March 1981

A 23-bit address bus provides a memory addressing range of greater than 16 megabytes. This large range of addressing capability, coupled with a memory management unit, allows large, modular programs to be developed and operated without resorting to cumbersome and time consuming software bookkeeping and paging techniques.

The status register contains the interrupt mask (eight levels available) as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and/or in a supervisor (S) state.

STATUS REGISTER



Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4-bits)
- Bytes (8-bits)
- Words (16-bits)
- Long Words (32-bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided for in the instruction set.

The 14 addressing modes, shown in Table 1, include six basic types:

- Register Direct
- Register Indirect
- Absolute
- Immediate
- Program Counter Relative
- Implied

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting and indexing. Program counter relative mode can also be modified via indexing and offsetting.

TABLE 1 — DATA ADDRESSING MODES

Mode	Generation
Register Direct Addressing	
Data Register Direct	EA = Dn
Address Register Direct	EA = An
Absolute Data Addressing	
Absolute Short	EA = (Next Word)
Absolute Long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA = (PC) + d_{16}
Relative with Index and Offset	EA = (PC) + (Xn) + d_8
Register Indirect Addressing	
Register Indirect	EA = (An)
Postincrement Register Indirect	EA = (An), An ← An + N
Predecrement Register Indirect	An ← An − N, EA = (An)
Register Indirect with Offset	EA = (An) + d_{16}
Indexed Register Indirect with Offset	EA = (An) + (Xn) + d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA = SR, USP, SP, PC

NOTES:

EA = Effective Address
An = Address Register
Dn = Data Register
Xn = Address or Data Register used as Index Register
SR = Status Register
PC = Program Counter
( ) = Contents of
d_8 = Eight-bit Offset (displacement)
d_{16} = Sixteen-bit Offset (displacement)
N = 1 for Byte, 2 for Words and 4 for Long Words
← = Replaces

The 68000 instruction set is shown in Table 2. Some additional instructions are variations, or subsets, of these and they appear in Table 3. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations, BCD arithmetic and expanded operations (through traps).

TABLE 2 — INSTRUCTION SET

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
B_{CC}	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DB_{CC}	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive Or
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral Data
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical Or
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
S_{CC}	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

TABLE 3 — VARIATIONS OF INSTRUCTION TYPES

Instruction Type	Variation	Description
ADD	**ADD**	Add
	ADDA	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX	Add with Extend
AND	**AND**	Logical And
	ANDI	And Immediate
CMP	**CMP**	Compare
	CMPA	Compare Address
	CMPM	Compare Memory
	CMPI	Compare Immediate
EOR	**EOR**	Exclusive Or
	EORI	Exclusive Or Immediate
MOVE	**MOVE**	Move
	MOVEA	Move Address
	MOVEQ	Move Quick
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	**NEG**	Negate
	NEGX	Negate with Extend
OR	**OR**	Logical Or
	ORI	Or Immediate
SUB	**SUB**	Subtract
	SUBA	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX	Subtract with Extend

DATA ORGANIZATION AND ADDRESSING CAPABILITIES

The following paragraphs describe the data organization and addressing capabilities of the 68000.

OPERAND SIZE

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each instruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. All explicit instructions support byte, word or long word operands. Implicit instructions support some subset of all three sizes.

DATA ORGANIZATION IN REGISTERS

The eight data registers support data operands of 1, 8, 16, or 32 bits. The seven address registers together with the active stack pointer support address operands of 32 bits.

DATA REGISTERS. Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31.

When a data register is used as either a source or destination operand, only the appropriate low-order portion is changed; the remaining high-order portion is neither used nor changed.

ADDRESS REGISTERS. Each address register and the stack pointer is 32 bits wide and holds a full 32 bit address. Address registers do not support byte sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

DATA ORGANIZATION IN MEMORY

Bytes are individually addressable with the high order byte having an even address the same as the word, as shown in Figure 1. The low order byte has an odd address that is one count higher than the word address. Instructions and multibyte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address n+2.

The data types supported by the 68000 are bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in Figure 2.

ADDRESSING

Instructions for the 68000 contain two kinds of information: the type of function to be performed, and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

Instructions specify an operand location in one of three ways:

- Register Specification – the number of the register is given in the register field of the instruction.
- Effective Address – use of the different effective address modes.
- Implicit Reference – the definition of certain instructions implies the use of specific registers.

FIGURE 1 – WORD ORGANIZATION IN MEMORY

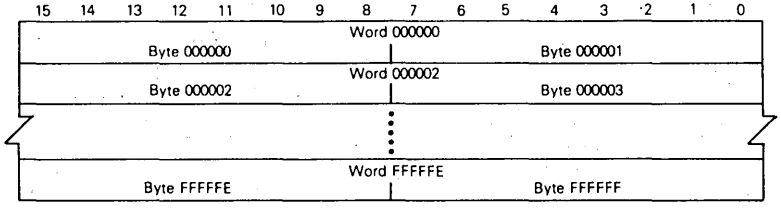
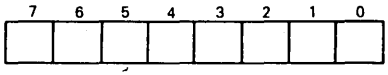
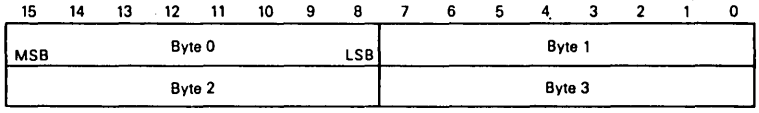


FIGURE 2 — DATA ORGANIZATION IN MEMORY

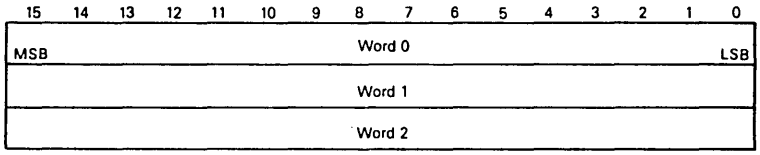
Bit Data
1 Byte = 8 Bits



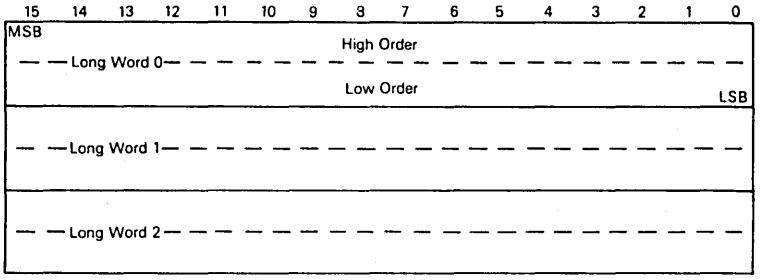
Integer Data
1 Byte = 8 Bits



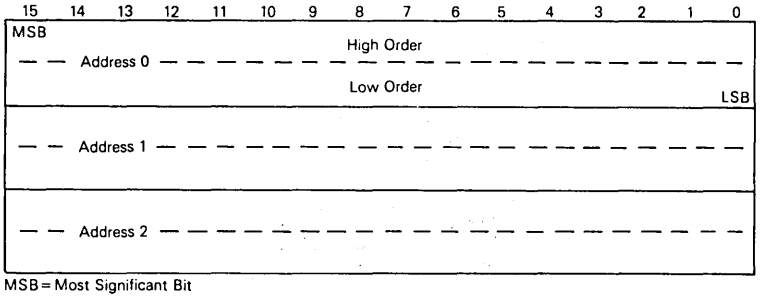
1 Word = 16 Bits



1 Long Word = 32 Bits

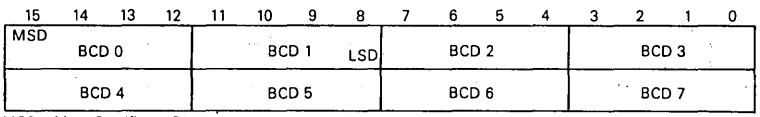


Addresses
1 Address = 32 Bits



MSB = Most Significant Bit
LSB = Least Significant Bit

Decimal Data
2 Binary Coded Decimal Digits = 1 Byte



MSD = Most Significant Digit
LSD = Least Significant Digit

INSTRUCTION FORMAT

Instructions are from one to five words in length, as shown in Figure 3. The length of the instruction and the operation to be performed is specified by the first word of the instruction which is called the operation word. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

PROGRAM/DATA REFERENCES

The 68000 separates memory references into two classes: program references, and data references. Program references, as the name implies, are references to that section of memory that contains the program being executed. Data references refer to that section of memory that contains data. Generally, operand reads are from the data space. All operand writes are to the data space.

REGISTER SPECIFICATION

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

EFFECTIVE ADDRESS

Most instructions specify the location of an operand by using the effective address field in the operation word. For example, Figure 4 shows the general format of the single effective address instruction operation word. The effective address is composed of two 3-bit fields: the mode field, and the register field. The value in the mode field selects the different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction, as shown in Figure 3. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

REGISTER DIRECT MODES. These effective addressing modes specify that the operand is in one of the 16 multifunction registers.

Data Register Direct. The operand is in the data register specified by the effective address register field.

Address Register Direct. The operand is in the address register specified by the effective address register field.

MEMORY ADDRESS MODES. These effective addressing modes specify that the operand is in memory and provide the specific address of the operand.

Address Register Indirect. The address of the operand is in the address register specified by the register field. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Postincrement. The address of the operand is in the address register specified by the register field. After the operand address is used, it is incremented by one, two, or four depending upon whether the size of the operand is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

Address Register Indirect With Predecrement. The address of the operand is in the address register specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

Address Register Indirect With Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Index. This address mode requires one word of extension. The address of the operand

FIGURE 3 — INSTRUCTION FORMAT

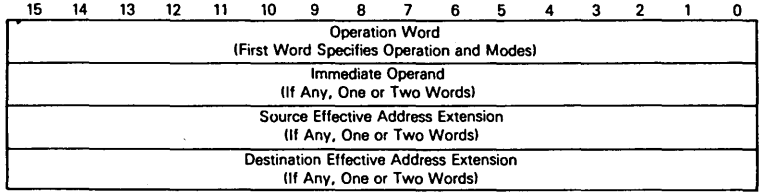
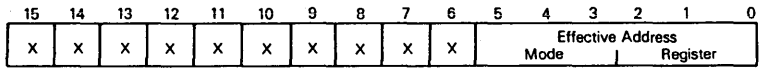


FIGURE 4 — SINGLE-EFFECTIVE-ADDRESS INSTRUCTION OPERATION WORD GENERAL FORMAT



is the sum of the address in the address register, the sign-extended displacement integer in the low order eight bits of the extension word, and the contents of the index register. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

SPECIAL ADDRESS MODES. The special address modes use the effective address register field to specify the special addressing mode instead of a register number.

Absolute Short Address. This address mode requires one word of extension. The address of the operand is the extension word. The 16-bit address is sign extended before it is used. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Absolute Long Address. This address mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high-order part of the address is the first extension word; the low-order part of the address is the second extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Program Counter With Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the program counter and the sign-extended 16-bit displacement integer in the extension word. The value in the program counter is the address of the extension word. The reference is classified as a program reference.

Program Counter With Index. This address mode requires one word of extension. The address is the sum of the address in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The value in the program counter is the address of the extension word. This reference is classified as a program reference.

Immediate Data. This address mode requires either one or two words of extension depending on the size of the operation.

Byte operation – operand is low order byte of extension word

Word operation – operand is extension word

Long word operation – operand is in the two extension words, high-order 16 bits are in the first extension word, low-order 16 bits are in the second extension word.

Condition Codes or Status Register. A selected set of instructions may reference the status register by means of the effective address field. These are:

ANDI to CCR
ANDI to SR
EORI to CCR
EORI to SR
ORI to CCR
ORI to SR

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 4 is a summary of the effective addressing modes discussed in the previous paragraphs.

IMPLICIT REFERENCE

Some instructions make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), or the status register (SR). Table 5 provides a list of these instructions and the registers implied.

SYSTEM STACK. The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S-bit in the status register. If the S-bit indicates supervisor state, SSP is the active system stack pointer, and the USP cannot be referenced as an address register. If the S-bit indicates user state, the USP is the active system stack pointer, and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

TABLE 4 – EFFECTIVE ADDRESS ENCODING SUMMARY

Addressing Mode	Mode	Register
Data Register Direct	000	register number
Address Register Direct	001	register number
Address Register Indirect	010	register number
Address Register Indirect with Postincrement	011	register number
Address Register Indirect with Predecrement	100	register number
Address Register Indirect with Displacement	101	register number
Address Register Indirect with Index	110	register number
Absolute Short	111	000
Absolute Long	111	001
Program Counter with Displacement	111	010
Program Counter with Index	111	011
Immediate or Status Register	111	100

TABLE 5 – IMPLICIT INSTRUCTION REFERENCE SUMMARY

Instruction	Implied Register(s)
Branch Conditional (B_{CC}), Branch Always (BRA)	PC
Branch to Subroutine (BSR)	PC, SP
Check Register against Bounds (CHK)	SSP, SR
Test Condition, Decrement and Branch (DB_{CC})	PC
Signed Divide (DIVS)	SSP, SR
Unsigned Divide (DIVU)	SSP, SR
Jump (JMP)	PC
Jump to Subroutine (JSR)	PC, SP
Link and Allocate (LINK)	SP
Move Condition Codes (MOVE CCR)	SR
Move Status Register (MOVE SR)	SR
Move User Stack Pointer (MOVE USP)	USP
Push Effective Address (PEA)	SP
Return from Exception (RTE)	PC, SP, SR
Return and Restore Condition Codes (RTR)	PC, SP, SR
Return from Subroutine (RTS)	PC, SP
Trap (TRAP)	SSP, SR
Trap on Overflow (TRAPV)	SSP, SR
Unlink (UNLK)	SP

INSTRUCTION SET SUMMARY

The following paragraphs contain an overview of the form and structure of the 68000 instruction set. The instructions form a set of tools that include all the machine functions to perform the following operations:

- Data Movement
- Integer Arithmetic
- Logical
- Shift and Rotate
- Bit Manipulation
- Binary Coded Decimal
- Program Control
- System Control

The complete range of instruction capabilities combined with the flexible addressing modes described previously provide a very flexible base for program development.

DATA MOVEMENT OPERATIONS

The basic method of data acquisition (transfer and storage) is provided by the move (MOVE) instruction. The move instruction and the effective addressing modes allow both address and data manipulation. Data move instructions allow byte, word, and long word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long word operand transfers and ensure that only legal address manipulations are executed. In addition to the general move instruction there are several special data movement instructions: move multiple registers (MOVEM), move peripheral data (MOVEP), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), unlink stack (UNLK), and move quick (MOVEQ). Table 6 is a summary of the data movement operations.

TABLE 6 — DATA MOVEMENT OPERATIONS

Instruction	Operand Size	Operation
EXG	32	Rx ↔ Ry
LEA	32	EA → An
LINK	–	An → SP@ – SP → An SP + d → SP
MOVE	8, 16, 32	(EA)s → EAd
MOVEM	16, 32	(EA) → An, Dn An, Dn → EA
MOVEP	16, 32	(EA) → Dn Dn → EA
MOVEQ	8	#xxx → Dn
PEA	32	EA → SP@ –
SWAP	32	Dn[31:16] ↔ Dn[15:0]
UNLK	–	An → Sp SP@ + → An

NOTES:
s = source
d = destination
[ ] = bit numbers
@ – = indirect with predecrement
@ + = indirect with postdecrement

INTEGER ARITHMETIC OPERATIONS

The arithmetic operations include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV) as well as arithmetic compare (CMP), clear (CLR), and negate (NEG). The add and subtract instructions are available for both address and data operations, with data operations accepting all operand sizes. Address operations are limited to legal address size operands (16 or 32 bits). Data, address, and memory compare operations are also available. The clear and negate instructions may be used on all sizes of data operands.

The multiply and divide operations are available for signed and unsigned operands using word multiply to produce a long word product, and a long word dividend with word divisor to produce a word quotient with a word remainder.

Multiprecision and mixed size arithmetic can be accomplished using a set of extended instructions. These instructions are: add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX).

A test operand (TST) instruction that will set the condition codes as a result of a compare of the operand with zero is also available. Test and set (TAS) is a synchronization instruction useful in multiprocessor systems. Table 7 is a summary of the integer arithmetic operations.

TABLE 7 — INTEGER ARITHMETIC OPERATIONS

Instruction	Operand Size	Operation
ADD	8, 16, 32 16, 32	Dn + (EA) → Dn (EA) + Dn → EA (EA) + #xxx → EA An + (EA) → An
ADDX	8, 16, 32 16, 32	Dx + Dy + X → Dx Axa@ – + Ay@ – + X → Ax@
CLR	8, 16, 32	0 → EA
CMP	8, 16, 32 16, 32	Dn – (EA) (EA) – #xxx Ax@ + – Ay@ + An – (EA)
DIVS	32 ÷ 16	Dn/(EA) → Dn
DIVU	32 ÷ 16	Dn/(EA) → Dn
EXT	8 → 16 16 → 32	(Dn)8 → Dn16 (Dn)16 → Dn32
MULS	16*16 → 32	Dn*(EA) → Dn
MULU	16*16 → 32	Dn*(EA) → Dn
NEG	8, 16, 32	0 – (EA) → EA
NEGX	8, 16, 32	0 – (EA) – X → EA
SUB	8, 16, 32 16, 32	Dn – (EA) → Dn (EA) – Dn → EA (EA) – #xxx → EA An – (EA) → An
SUBX	8, 16, 32	Dx – Dy – X → Dx Ax@ – – Ay@ – – X → Ax@
TAS	8	(EA) – 0, 1 → EA[7]
TST	8, 16, 32	(EA) – 0

NOTE: [ ] = bit number

LOGICAL OPERATIONS

Logical operation instructions AND, OR, EOR, and NOT are available for all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provide these logical operations with all sizes of immediate data. Table 8 is a summary of the logical operations.

TABLE 8 — LOGICAL OPERATIONS

Instruction	Operand Size	Operation
AND	8, 16, 32	Dn∧(EA) → Dn (EA)∧Dn → EA (EA)∧#xxx → EA
OR	8, 16, 32	Dn v (EA) → Dn (EA) v Dn → EA (EA) v #xxx → EA
EOR	8, 16, 32	(EA) ⊕ Dy → EA (EA) ⊕ #xxx → EA
NOT	8, 16, 32	~(EA) → EA

NOTE: ~ = invert

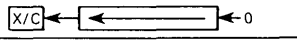
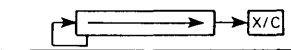
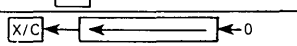
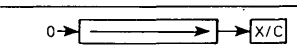
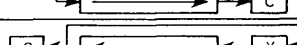
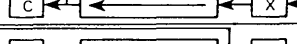
SHIFT AND ROTATE OPERATIONS

Shift operations in both directions are provided by the arithmetic instructions ASR and ASL and logical shift instructions LSR and LSL. The rotate instructions (with and without extend) available are ROXR, ROXL, ROR, and ROL. All shift and rotate operations can be performed in either registers or memory. Register shifts and rotates support all operand sizes and allow a shift count specified in the instruction of one to eight bits, or 0 to 63 specified in a data register.

Memory shifts and rotates are for word operands only and allow only single-bit shifts or rotates.

Table 9 is a summary of the shift and rotate operations.

TABLE 9 — SHIFT AND ROTATE OPERATIONS

Instruction	Operand Size	Operation
ASL	8, 16, 32	
ASR	8, 16, 32	
LSL	8, 16, 32	
LSR	8, 16, 32	
ROL	8, 16, 32	
ROR	8, 16, 32	
ROXL	8, 16, 32	
ROXR	8, 16, 32	

BIT MANIPULATION OPERATIONS

Bit manipulation operations are accomplished using the following instructions: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). Table 10 is a summary of the bit manipulation operations. (Bit 2 of the status register is Z.)

TABLE 10 — BIT MANIPULATION OPERATIONS

Instruction	Operand Size	Operation
BTST	8, 32	~bit of (EA) → Z
BSET	8, 32	~bit of (EA) → Z 1 → bit of EA
BCLR	8, 32	~bit of (EA) → Z 0 → bit of EA
BCHG	8, 32	~bit of (EA) → Z ~bit of (EA) → bit of EA

BINARY CODED DECIMAL OPERATIONS

Multiprecision arithmetic operations on binary coded decimal numbers are accomplished using the following instructions: add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 11 is a summary of the binary coded decimal operations.

TABLE 11 — BINARY CODED DECIMAL OPERATIONS

Instruction	Operand Size	Operation
ABCD	8	$Dx_{10} + Dy_{10} + X \rightarrow Dx$ $Ax@-_{10} + Ay@-_{10} + X \rightarrow Ax@$
SBCD	8	$Dx_{10} - Dy_{10} - X \rightarrow Dx$ $Ax@-_{10} - Ay@-_{10} - X \rightarrow Ax@$
NBCD	8	$0 - (EA)_{10} - X \rightarrow EA$

PROGRAM CONTROL OPERATIONS

Program control operations are accomplished using a series of conditional and unconditional branch instructions and return instructions. These instructions are summarized in Table 12.

The conditional instructions provide setting and branching for the following conditions:

CC	— carry clear	LS	— low or same
CS	— carry set	LT	— less than
EQ	— equal	MI	— minus
F	— never true	NE	— not equal
GE	— greater or equal	PL	— plus
GT	— greater than	T	— always true
HI	— high	VC	— no overflow
LE	— less or equal	VS	— overflow

TABLE 12 — PROGRAM CONTROL OPERATIONS

Instruction	Operation
Conditional	
B_{CC}	Branch conditionally (14 conditions) 8- and 16-bit displacement
DB_{CC}	Test condition, decrement, and branch 16-bit displacement
S_{CC}	Set byte conditionally (16 conditions)
Unconditional	
BRA	Branch always 8- and 16-bit displacement
BSR	Branch to subroutine 8- and 16-bit displacement
JMP	Jump
JSR	Jump to subroutine
Returns	
RTR	Return and restore condition codes
RTS	Return from subroutine

TABLE 13 — SYSTEM CONTROL OPERATIONS

Instruction	Operation
Privileged	
RESET	Reset external devices
RTE	Return from exception
STOP	Stop program execution
ORI to SR	Logical OR to status register
MOVE USP	Move user stack pointer
ANDI to SR	Logical AND to status register
EORI to SR	Logical EOR to status register
MOVE EA to SR	Load new status register
Trap Generating	
TRAP	Trap
TRAPV	Trap on overflow
CHK	Check register against bounds
Status Register	
ANDI to CCR	Logical AND to condition codes
EORI to CCR	Logical EOR to condition codes
MOVE EA to CCR	Load new condition codes
ORI to CCR	Logical OR to condition codes
MOVE SR to EA	Store status register

SYSTEM CONTROL OPERATIONS

System control operations are accomplished by using privileged instructions, trap generating instructions, and instructions that use or modify the status register. These instructions are summarized in Table 13.

SIGNAL AND BUS OPERATION DESCRIPTION

The following paragraphs contain a brief description of the input and output signals. A discussion of bus operation during the various machine cycles and operations is also given.

SIGNAL DESCRIPTION

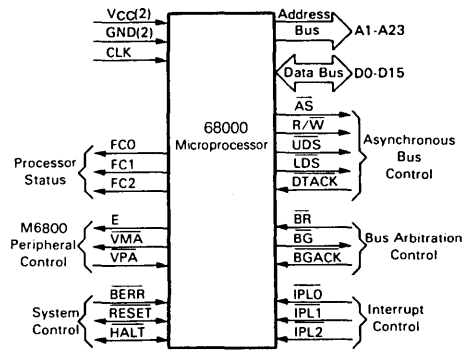
The input and output signals can be functionally organized into the groups shown in Figure 5. The following paragraphs provide a brief description of the signals and also a reference (if applicable) to other paragraphs that contain more detail about the function being performed.

ADDRESS BUS (A1 THROUGH A23). This 23-bit, unidirectional, three-state bus is capable of addressing 8 megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are all set to a logic high.

DATA BUS (D0 THROUGH D15). This 16-bit, bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-D7.

ASYNCHRONOUS BUS CONTROL. Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

FIGURE 5 — INPUT AND OUTPUT SIGNALS



Address Strobe ($\overline{AS}$). This signal indicates that there is a valid address on the address bus.

Read/Write (R/$\overline{W}$). This signal defines the data bus transfer as a read or write cycle. The R/$\overline{W}$ signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Upper And Lower Data Strobes ($\overline{UDS}$, $\overline{LDS}$). These signals control the data on the data bus, as shown in Table 14. When the R/$\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R/$\overline{W}$ line is low, the processor will write to the data bus as shown.

TABLE 14 — DATA STROBE CONTROL OF DATA BUS

$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D8-D15	D0-D7
High	High	–	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7*	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15*

*These conditions are a result of current implementation and may not appear on future devices.

Data Transfer Acknowledge ($\overline{DTACK}$). This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

BUS ARBITRATION CONTROL. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Bus Request ($\overline{BR}$). This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

Bus Grant ($\overline{BG}$). This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge ($\overline{BGACK}$). This input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

1. a bus grant has been received
2. address strobe is inactive which indicates that the microprocessor is not using the bus
3. data transfer acknowledge is inactive which indicates that either memory or the peripherals are not using the bus
4. bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. The least significant bit is given in $\overline{IPL0}$ and the most significant bit is contained in $\overline{IPL2}$.

SYSTEM CONTROL. The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus Error ($\overline{BERR}$). This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices
2. interrupt vector number acquisition failure
3. illegal access request as determined by a memory management unit
4. other application dependent errors.

The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retried.

Refer to **BUS ERROR AND HALT OPERATION** paragraph for additional information about the interaction of the bus error and halt signals.

Reset ($\overline{RESET}$). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of a RESET instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external halt and reset signals applied at the same time. Refer to **RESET OPERATION** paragraph for additional information about reset operation.

Halt ($\overline{HALT}$). When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state. Refer to **BUS ERROR AND HALT OPERATION** paragraph for additional information about the interaction between the halt and bus error signals.

When the processor has stopped executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped.

R6500 PERIPHERAL CONTROL. These control signals are used to allow the interfacing of synchronous R6500 peripheral devices with the asynchronous 68000. These signals are explained in the following paragraphs.

Enable (E). This is the standard enable signal commonly called Ø2 in R6500 peripheral devices. The period for this output is ten 68000 clock periods (six clocks low; four clocks high).

Valid Peripheral Address ($\overline{VPA}$). This input indicates that the device or region addressed is a R6500 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt. Refer to INTERFACE WITH R6500 PERIPHERALS.

Valid Memory Address ($\overline{VMA}$). This output is used to indicate to R6500 peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address ($\overline{VPA}$) input which indicates that the peripheral is a R6500 family device.

PROCESSOR STATUS (FC0, FC1, FC2). These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 15. The information indicated by the function code outputs is valid whenever address strobe ($\overline{AS}$) is active.

TABLE 15 — FUNCTION CODE OUTPUTS

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

CLOCK (CLK). The clock input is a TTL compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input shall be a constant frequency.

SIGNAL SUMMARY. Table 16 is a summary of all the signals discussed in the previous paragraphs.

TABLE 16 — SIGNAL SUMMARY

Signal Name	Mnemonic	Input/Output	Active State	Three State
Address Bus	A1-A23	output	high	yes
Data Bus	D0-D15	input/output	high	yes
Address Strobe	$\overline{AS}$	output	low	yes
Read/Write	R/$\overline{W}$	output	read-high write-low	yes
Upper and Lower Data Strobes	$\overline{UDS}$, $\overline{LDS}$	output	low	yes
Data Transfer Acknowledge	$\overline{DTACK}$	input	low	no
Bus Request	$\overline{BR}$	input	low	no
Bus Grant	$\overline{BG}$	output	low	no
Bus Grant Acknowledge	$\overline{BGACK}$	input	low	no
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	input	low	no
Bus Error	$\overline{BERR}$	input	low	no
Reset	$\overline{RESET}$	input/output	low	no*
Halt	$\overline{HALT}$	input/output	low	no*
Enable	E	output	high	no
Valid Memory Address	$\overline{VMA}$	output	low	yes
Valid Peripheral Address	$\overline{VPA}$	input	low	no
Function Code Output	FC0, FC1, FC2	output	high	yes
Clock	CLK	input	high	no
Power Input	V_{CC}	input	–	–
Ground	GND	input	–	–

*open drain

BUS OPERATION

The following paragraphs explain control signal and bus operation during data transfer operations, bus arbitration, bus error and halt conditions, and reset operation.

DATA TRANSFER OPERATIONS. Transfer of data between devices involves the following leads:

- Address Bus A1 through A23
- Data Bus D0 through D15
- Control Signals

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the 68000 for interlocked multiprocessor communications.

NOTE

The terms **assertion** and **negation** will be used extensively. This is done to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The term assert or assertion is used to indicate that a signal is active or true independent of whether that voltage is low or high. The term negate or negation is used to indicate that a signal is inactive or false.

Read Cycle. During a read cycle, the processor receives data from memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both bytes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions it internally.

A word read cycle flow chart is given in Figure 6. A byte read cycle flow chart is given in Figure 7. Read cycle timing is given in Figure 8 and Figure 9 details word and byte read cycle operation.

FIGURE 6 — WORD READ CYCLE FLOW CHART

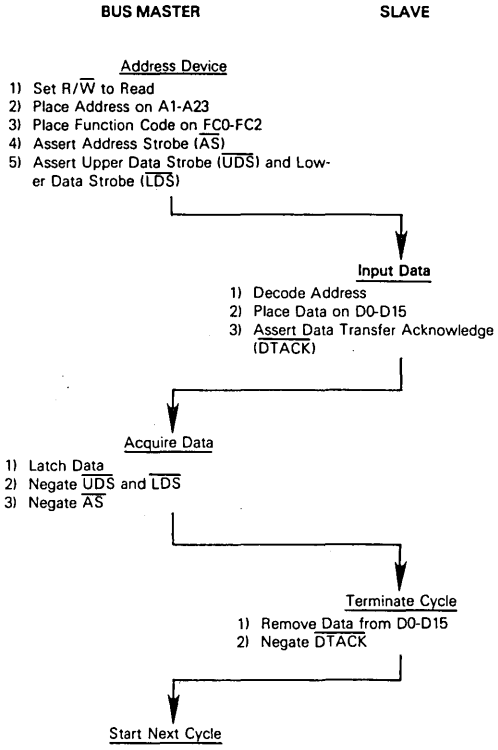


FIGURE 7 — BYTE READ CYCLE FLOW CHART

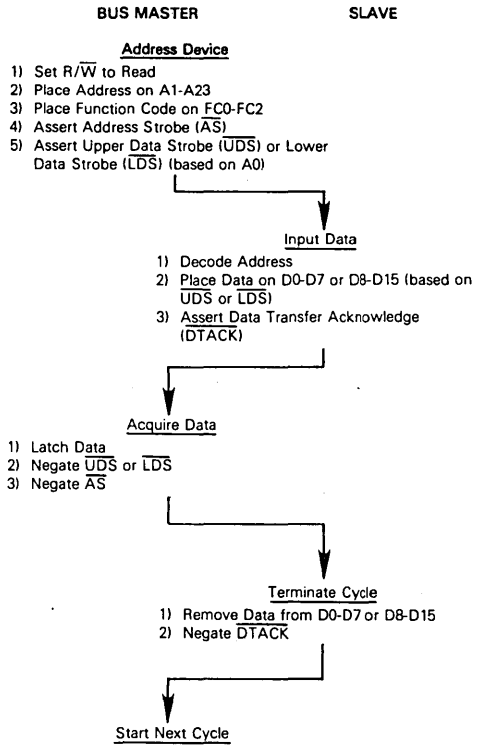


FIGURE 8 — READ AND WRITE CYCLE TIMING DIAGRAM

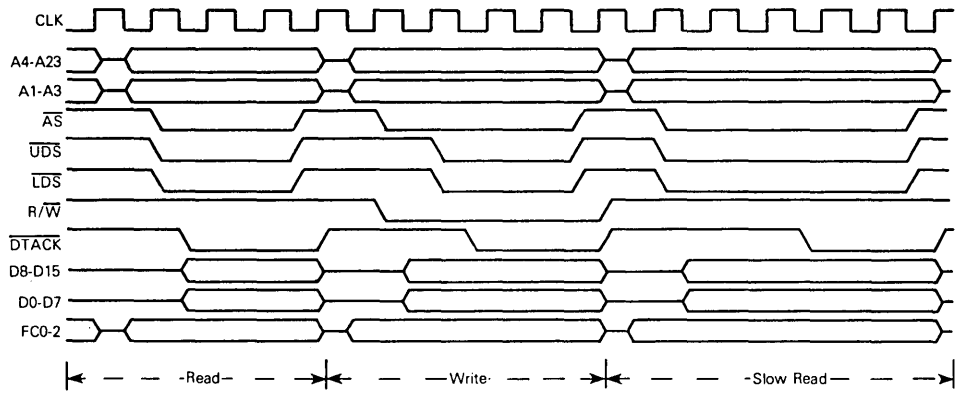
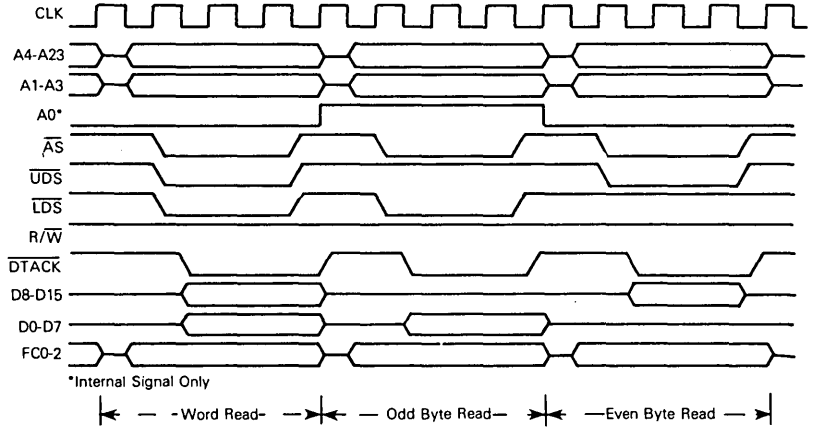


FIGURE 9 — WORD AND BYTE READ CYCLE TIMING DIAGRAM



Write Cycle. During a write cycle, the processor sends data to memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued. A word write cycle flow chart is given in Figure 10. A byte write cycle flow chart is given in Figure 11. Write cycle timing is given in Figure 8 and Figure 12 details word and byte write cycle operation.

FIGURE 10 — WORD WRITE CYCLE FLOW CHART

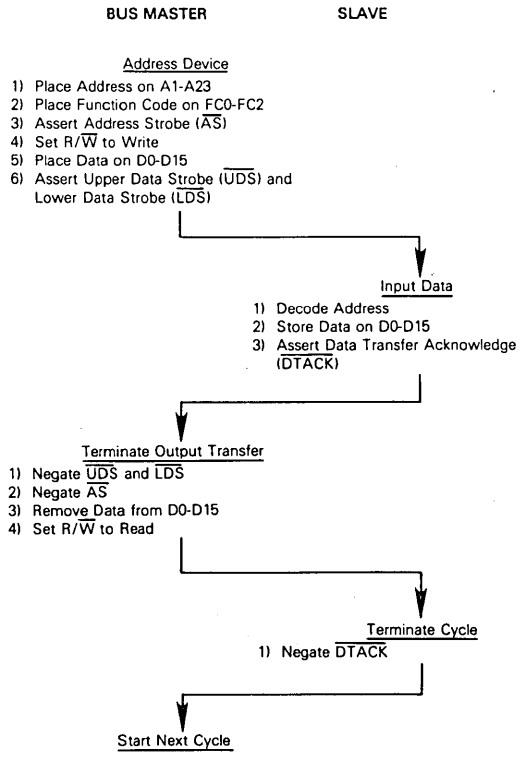


FIGURE 11 — BYTE WRITE CYCLE FLOW CHART

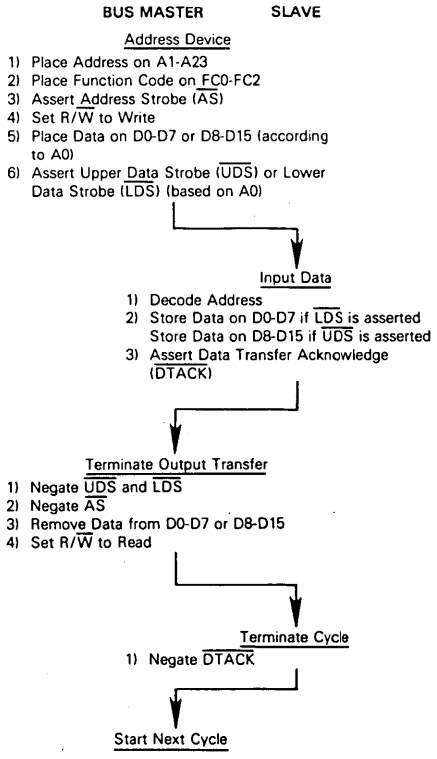
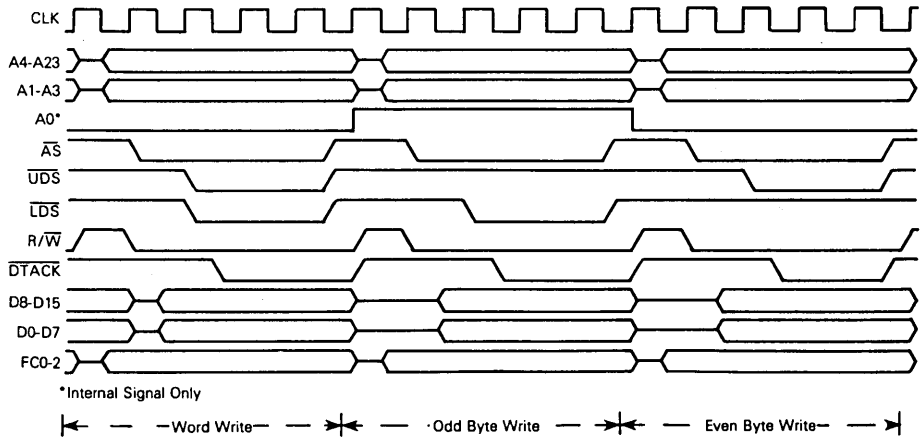


FIGURE 12 — WORD AND BYTE WRITE CYCLE TIMING DIAGRAM



Read-Modify-Write Cycle. The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the 68000 this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write cycles are byte operations. A read-modify-write cycle flow chart is given in Figure 13 and a timing diagram is given in Figure 14.

FIGURE 13 – READ-MODIFY-WRITE CYCLE FLOW CHART

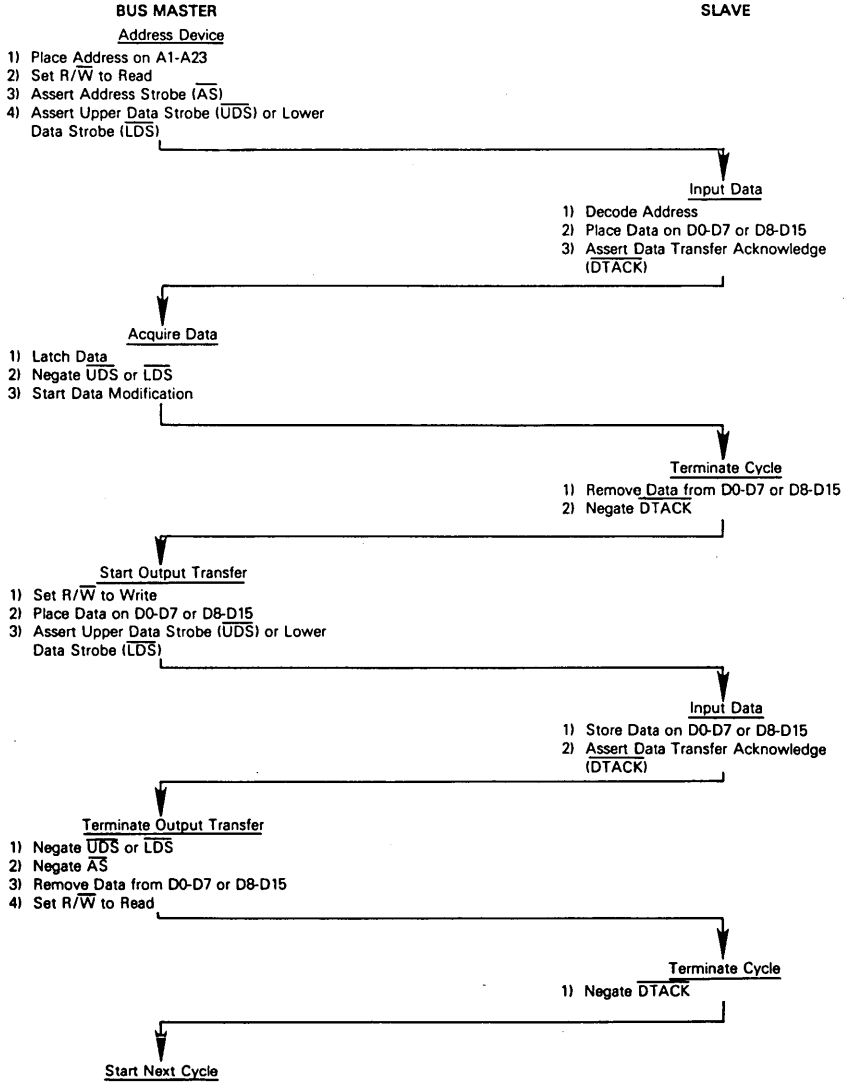
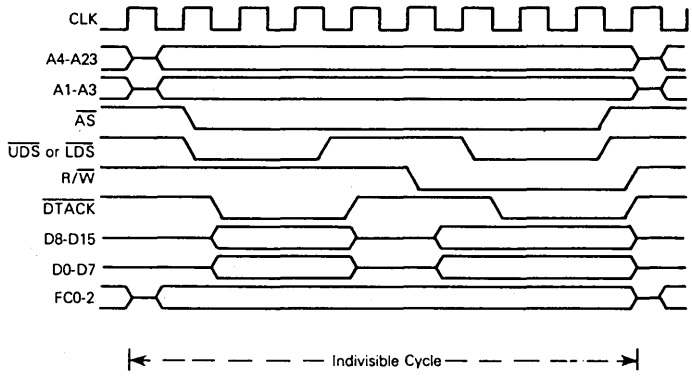


FIGURE 14 — READ-MODIFY-WRITE CYCLE TIMING DIAGRAM



BUS ARBITRATION. Bus arbitration is a technique used by master-type devices to request, be granted, and acknowledge bus mastership. In its simplest form, it consists of:

1. Asserting a bus mastership request.
2. Receiving a grant that the bus is available at the end of the current cycle.
3. Acknowledging that mastership has been assumed.

Figure 15 is a flow chart showing the detail involved in a request from a single device. Figure 16 is a timing diagram for the same operations. This technique allows processing of bus requests during data transfer cycles.

The timing diagram shows that the bus request is negated at the time that an acknowledge is asserted. This type of operation would be true for a system consisting of the processor and one device capable of bus mastership. In systems having a number of devices capable of bus mastership, the bus request line from each device is wire ORed to the processor. In this system, it is easy to see that there could be more than one bus request being made. The timing diagram shows that the bus grant signal is negated a few clock cycles after the transition of the acknowledge (BGACK) signal.

However, if the bus requests are still pending, the processor will assert another bus grant within a few clock cycles after it was negated. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

FIGURE 15 — BUS ARBITRATION CYCLE FLOW-CHART

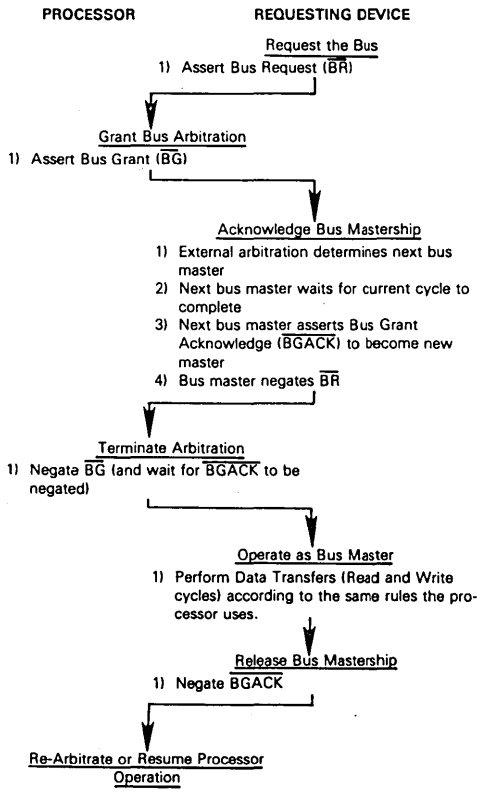
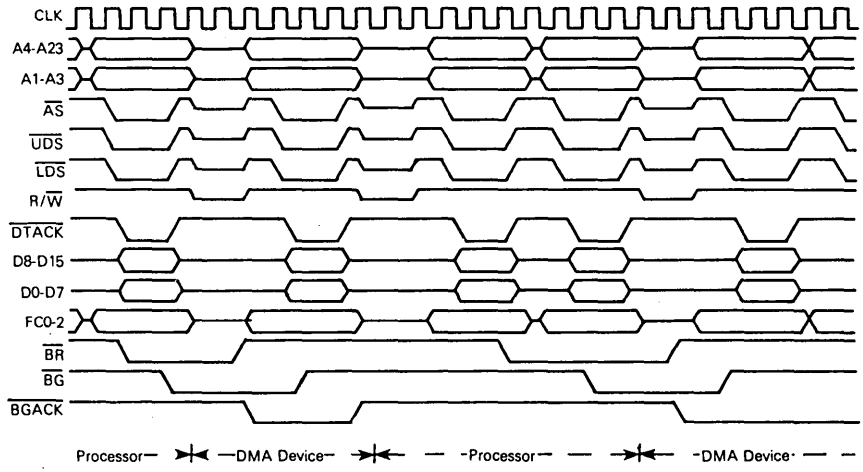


FIGURE 16 — BUS ARBITRATION CYCLE TIMING DIAGRAM



Requesting the Bus. External devices capable of becoming bus masters request the bus by asserting the bus request (BR) signal. This is a wire ORed signal (although it need not be constructed from open collector devices) that indicates to the processor that some external device requires control of the external bus. The processor is effectively at a lower bus priority level than the external device and will relinquish the bus after it has completed the last bus cycle it has started.

When no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows ordinary processing to continue if the arbitration circuitry responded to noise inadvertently.

Receiving the Bus Grant. The processor asserts bus grant (BG) as soon as possible. Normally this is immediately after internal synchronization. The only exception to this occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe (AS) signal. In this case, bus grant will not be asserted until one clock after address strobe is asserted to indicate to external devices that a bus cycle is being executed.

The bus grant signal may be routed through a daisy-chained network or through a specific priority-encoded network. The processor is not affected by the external method of arbitration as long as the protocol is obeyed.

Acknowledgement of Mastership. Upon receiving a bus grant, the requesting device waits until address strobe, data transfer acknowledge, and bus grant acknowledge are negated before issuing its own BGACK. The negation of the address strobe indicates that the previous master has completed its cycle, the negation of bus grant acknowledge indicates that the previous master has released the bus. (While address strobe is asserted no device is allowed to "break into" a cycle.) The negation of data transfer acknowledge indicates the previous slave has terminated its connection to the previous master. Note that in some applications data transfer acknowledge might not enter into this function. General purpose devices would then be connected such that they were only dependent on address strobe. When bus grant acknowledge is issued the device is bus master until it negates bus grant acknowledge. Bus grant acknowledge should not be negated until after the bus cycle(s) is (are) completed. Bus mastership is terminated at the negation of bus grant acknowledge.

The bus request from the granted device should be dropped when bus grant acknowledge is asserted. If bus request is still asserted after bus grant acknowledge is negated, the processor performs another arbitration sequence and issues another bus grant. Note that the processor does not perform any external bus cycles before it re-asserts bus grant.

BUS ERROR AND HALT OPERATION. In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems will require a different maximum response time, a bus error input is provided. External circuitry must be used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error signal is received, the processor has two options: initiate a bus error exception sequence or try running the bus cycle again.

Exception Sequence. The bus error exception sequence is entered when the processor receives a bus error signal and the halt pin is inactive. Figure 17 is a timing diagram for the exception sequence. The sequence is composed of the following elements:

1. Stacking the program counter and status register
2. Stacking the error information
3. Reading the bus error vector table entry
4. Executing the bus error handler routine

The stacking of the program counter and the status register is the same as if an interrupt had occurred. Several additional items are stacked when a bus error occurs. These items are used to determine the nature of the error and correct it, if possible. The bus error vector is vector number two located at address $000008. The processor loads the new program counter from this location. A software bus error handler routine is then executed by the processor. Refer to **EXCEPTION PROCESSING** for additional information.

Re-Running the Bus Cycle. When the processor receives a bus error signal and the halt pin is being driven by an external device, the processor enters the re-run sequence. Figure 18 is a timing diagram for re-running the bus cycle.

The processor completes the bus cycle, then puts the address, data and function code output lines in the high-impedance state. The processor remains "halted," and will not run another bus cycle until the halt signal is removed by external logic. Then the processor will re-run the previous bus cycle using the same address, the same function codes, the same data (for a write operation), and the same controls. The bus error signal should be removed before the halt signal is removed.

FIGURE 17 — BUS ERROR TIMING DIAGRAM

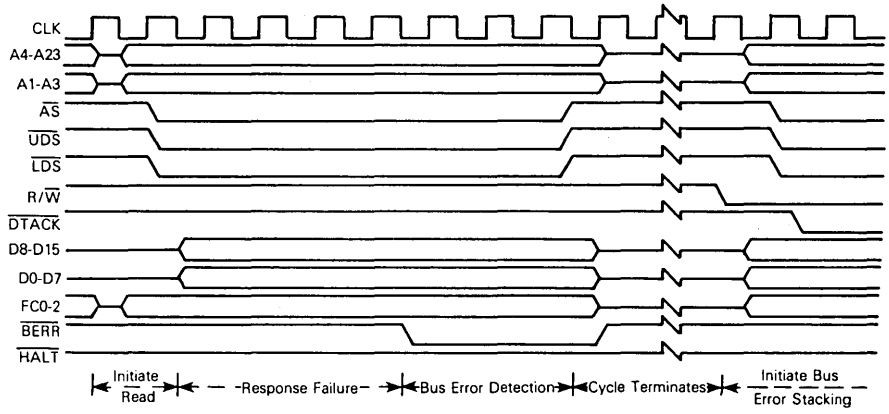
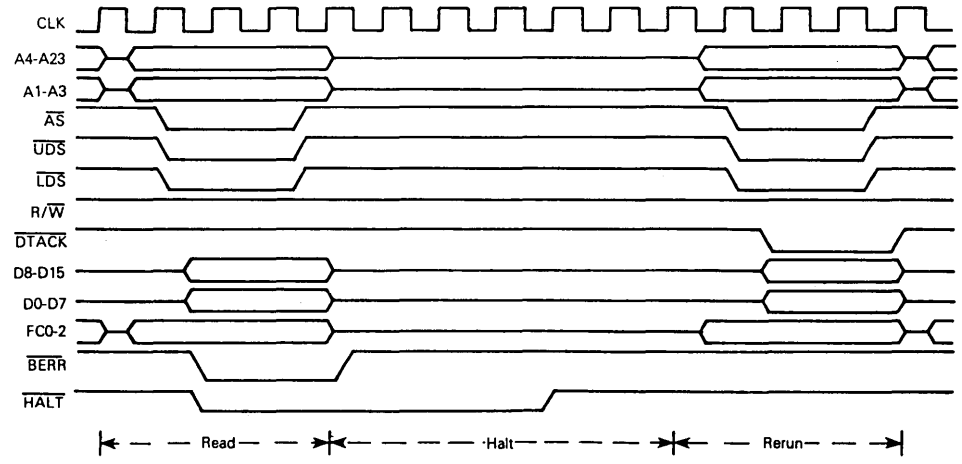


FIGURE 18 — RE-RUN BUS CYCLE TIMING INFORMATION



NOTE

The processor will not re-run a read-modify-write cycle. This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a Test-and-Set operation is performed without ever releasing $\overline{AS}$.

Halt Operation with No Bus Error. The halt input signal to the 68000 performs a Halt/Run/Single-Step function in a similar fashion to the M6800 halt function. The halt and run modes are somewhat self explanatory in that when the halt signal is constantly active the processor "halts" (does nothing) and when the halt signal is constantly inactive the processor "runs" (does something).

The single-step mode is derived from correctly timed transitions on the halt signal input. It forces the processor to execute a single bus cycle by entering the "run" mode until the processor starts a bus cycle then changing to the "halt" mode. Thus, the single-step mode allows the user to proceed through (and therefore debug) processor operations one bus cycle at a time.

Figure 19 details the timing required for correct single-step operations. Some care must be exercised to avoid harmful interactions between the bus error signal and the halt pin when using the single cycle mode as a debugging tool. This is also true of interactions between the halt and reset lines since these can reset the machine.

When the processor completes a bus cycle after recognizing that the halt signal is active, most three-state signals are put in the high-impedance state. These include:

1. address lines
2. data lines
3. function code lines

This is required for correct performance of the re-run bus cycle operation.

Note that when the processor honors a request to halt, the function codes are put in the high-impedance state (their buffer characteristics are the same as the address buffers). While the processor is honoring the halt request, bus arbitration performs as usual. That is, halting has no effect on bus arbitration. It is the bus arbitration function that removes the control signals from the bus.

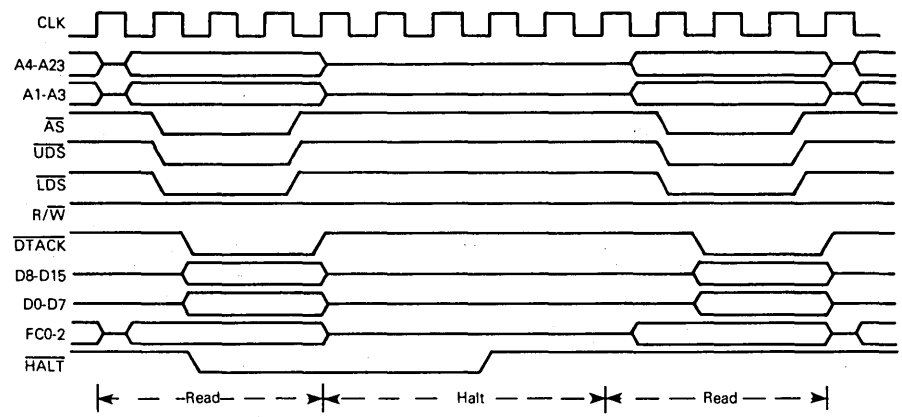
The halt function and the hardware trace capability allow the hardware debugger to trace single bus cycles or single instructions one at a time. These processor capabilities, along with a software debugging package, give total debugging flexibility.

Double Bus Faults. When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row. This is commonly referred to as a double bus fault. When a double bus fault occurs, the processor will halt. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

Note that a bus cycle which is re-run does not constitute a bus error exception, and does not contribute to a double bus fault. Note also that this means that as long as the external hardware requests it, the processor will continue to re-run the same bus cycle.

The bus error pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor.

FIGURE 19 — HALT SIGNAL TIMING CHARACTERISTICS



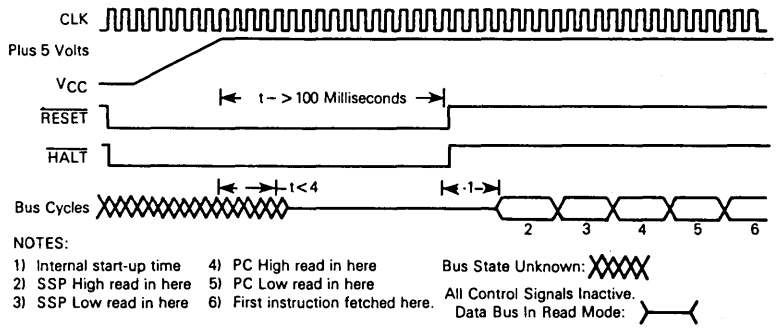
RESET OPERATION. The reset signal is a bidirectional signal that allows either the processor or an external signal to reset the system. Figure 20 is a timing diagram for reset operations. Both the halt and the reset lines must be applied to ensure total reset of the processor.

When the reset and halt lines are driven by an external device, it is recognized as an entire system reset, including the processor. The processor responds by reading the reset vector table entry (vector number zero, address $000000) and loads it into the supervisor stack pointer (SSP). Vector table entry number one at address $000004 is read next and loaded into the program counter. The processor initializes the status register to an interrupt level of seven. No other registers are affected by the reset sequence.

When a RESET sequence is executed, the processor drives the reset pin for 124 clock pulses. In this case, the processor is trying to reset the rest of the system. Therefore, there is no effect on the internal state of the processor. All of the processor's internal registers and the status register are unaffected by the execution of a RESET instruction. All external devices connected to the reset line should be reset at the completion of the RESET instruction.

When V_{CC} is initially applied to the processor, an external reset must be applied to the reset pin for 100 milliseconds.

FIGURE 20 — RESET OPERATION TIMING DIAGRAM



EXCEPTION PROCESSING

The following paragraphs describe the actions of the 68000 which are outside the normal processing associated with the execution of instructions. The functions of the bits in the supervisor portion of the status register are covered: the supervisor/user bit, the trace enable bit, and the processor interrupt priority mask. Finally, the sequence of memory references and actions taken by the processor on exception conditions is detailed.

PROCESSING STATES

The 68000 is always one of three processing states: normal, exception, or halted. The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further memory references are made.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

PRIVILEGE STATES

The processor operates in one of two states of privilege: the "user" state or the "supervisor" state. The privilege state determines which operations are legal, is used by the external memory management device to control and translate accesses, and is used to choose between the supervisor stack pointer and the user stack pointer in instruction references.

The privilege state is a mechanism for providing security in a computer system. Programs should access only their own code and data areas, and ought to be restricted from accessing information which they do not need and must not modify.

The privilege mechanism provides security by allowing most programs to execute in user state. In this state, the accesses are controlled, and the effects on other parts of the system are limited. The operating system executes in the supervisor state, has access to all resources, and performs the overhead tasks for the user state programs.

SUPERVISOR STATE. The supervisor state is the higher state of privilege. For instruction execution, the supervisor state is determined by the S-bit of the status register; if the S-bit is asserted (high), the processor is in the supervisor state. All instructions can be executed in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly access the supervisor stack pointer.

All exception processing is done in the supervisor state, regardless of the setting of the S-bit. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the supervisor stack pointer.

USER STATE. The user state is the lower state of privilege. For instruction execution, the user state is determined by the S-bit of the status register; if the S-bit is negated (low), the processor is executing instructions in the user state.

Most instructions execute the same in user state as in the supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the STOP instruction, or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole status register are privileged. To aid in debugging programs which are to be used as operating systems, the move to user stack pointer (MOVE USP) and move from user stack pointer (MOVE from USP) instructions are also privileged.

The bus cycles generated by an instruction executed in user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in the user privilege state, those instructions which use either the system stack pointer implicitly, or address register seven explicitly, access the user stack pointer.

PRIVILEGE STATE CHANGES. Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception processing, the current setting of the S-bit of the status register is saved and the S-bit is asserted, putting the processing in the supervisor state. Therefore, when instruction execution resumes at the address specified to process the exception, the processor is in the supervisor privilege state.

REFERENCE CLASSIFICATION. When the processor makes a reference, it classifies the kind of reference being made, using the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. Table 17 lists the classification of references.

TABLE 17 — REFERENCE CLASSIFICATION

Function Code Output			Reference Class
FC2	FC1	FC0	
0	0	0	(Unassigned)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

EXCEPTION PROCESSING

Before discussing the details of interrupts, traps, and tracing, a general description of exception processing is in order. The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made, and the status register is set for exception processing. In the second step the exception vector is determined, and the third step is the saving of the current processor context. In the fourth step a new context is obtained, and the processor switches to instruction processing.

EXCEPTION VECTORS. Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length (Figure 21), except for the reset

FIGURE 21 — EXCEPTION VECTOR FORMAT

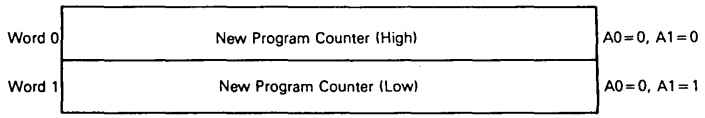
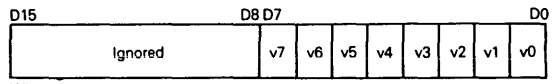


FIGURE 22 — PERIPHERAL VECTOR NUMBER FORMAT



Where:
v7 is the MSB of the Vector Number
v0 is the LSB of the Vector Number

vector, which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an eight-bit number which, when multiplied by four, gives the address of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8-bit vector number (Figure 22) to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 24-bit address, as shown in Figure 23. The memory layout for exception vectors is given in Table 18.

As shown in Table 18, the memory layout is 512 words long (1024 bytes). It starts at address 0 and proceeds through address 1023. This provides 255 unique vectors; some of these are reserved for TRAPS and other system functions. Of the 255, there are 192 reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the systems designer.

KINDS OF EXCEPTIONS. Exceptions can be generated by either internal or external causes. The externally generated exceptions are the interrupts and the bus error and reset requests. The interrupts are requests from peripheral devices for processor action while the bus error and reset inputs are used for access control and processor restart. The internally generated exceptions come from instructions, or from ad-

FIGURE 23 — ADDRESS TRANSLATED FROM 8-BIT VECTOR NUMBER

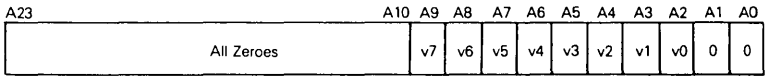


TABLE 18 — EXCEPTION VECTOR ASSIGNMENT

Vector Number(s)	Address			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset: Initial SSP
–	4	004	SP	Reset: Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned, reserved)
13*	52	034	SD	(Unassigned, reserved)
14*	56	038	SD	(Unassigned, reserved)
15	60	03C	SD	(Unassigned, reserved)
16-23*	64	04C	SD	(Unassigned, reserved)
	95	05F		–
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors
	191	0BF		–
48-63*	192	0C0	SD	(Unassigned, reserved)
	255	0FF		–
64-255	256	100	SD	User Interrupt Vectors
	1023	3FF		–

*Vector numbers 12, 13, 14, 16 through 23 and 48 through 63 are reserved for future enhancements. No user peripheral devices should be assigned these numbers.

dress errors or tracing. The trap (TRAP), trap on overflow (TRAPV), check register against bounds (CHK) and divide (DIV) instructions all can generate exceptions as part of their instruction execution. In addition, illegal instructions, word fetches from odd addresses and privilege violations cause exceptions. Tracing behaves like a very high priority, internally generated interrupt after each instruction execution.

EXCEPTION PROCESSING SEQUENCE. Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S-bit is asserted, putting the processor into the supervisor privilege state. Also, the T-bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch, classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the address of the exception vector.

The third step is to save the current processor status, except for the reset exception. The current program counter value and the saved copy of the status register are stacked using the supervisor stack pointer. The program counter value stacked usually points to the next unexecuted instruction, however for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented from the address of the instruction which caused the error. Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

MULTIPLE EXCEPTIONS. These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The Group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted, and the exception processing to commence at the next minor cycle of the processor. The Group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The Group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, CHK, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while Group 2 exceptions have lowest priority. Within Group 0, reset has highest priority, followed by bus error and then address error. Within Group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and privilege violation. Since only one instruction can be executed at a time, there is no priority relation within Group 2.

The priority relation between two exceptions determines which is taken, or taken first, if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is aborted. In another example, if an interrupt request occurs during the execution of an instruction while the T-bit is asserted, the trace exception has priority, and is processed first. Before instruction processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine. A summary of exception grouping and priority is given in Table 19.

TABLE 19 — EXCEPTION GROUPING AND PRIORITY

Group	Exception	Processing
0	Reset Bus Error Address Error	Exception processing begins at the next minor cycle
1	Trace Interrupt Illegal Privilege	Exception processing begins before the next instruction
2	TRAP, TRAPV, CHK, Zero Divide	Exception processing is started by normal instruction execution

EXCEPTION PROCESSING DETAILED DISCUSSION

Exceptions have a number of sources, and each exception has processing which is peculiar to it. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

RESET. The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation, and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered. The processor is forced into the supervisor state, and the trace state is forced off. The processor interrupt priority mask is set at level seven. The vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space. Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The power-up/restart code should be pointed to by the initial program counter.

The RESET instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

INTERRUPTS. Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the processor. Interrupt priority levels

are numbered from one to seven, level seven being the highest priority. The status register contains a three-bit mask which indicates the current processor priority, and interrupts are inhibited for all priority levels less than or equal to the current processor priority.

An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not force immediate exception processing, but are made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in a following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. First a copy of the status register is saved, and the privilege state is set to supervisor, tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus. If external logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the program counter and status register on the supervisor stack. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine. A flow chart for the interrupt acknowledge sequence is given in Figure 24; a timing diagram is given in Figure 25.

FIGURE 24 — INTERRUPT ACKNOWLEDGE SEQUENCE FLOW CHART

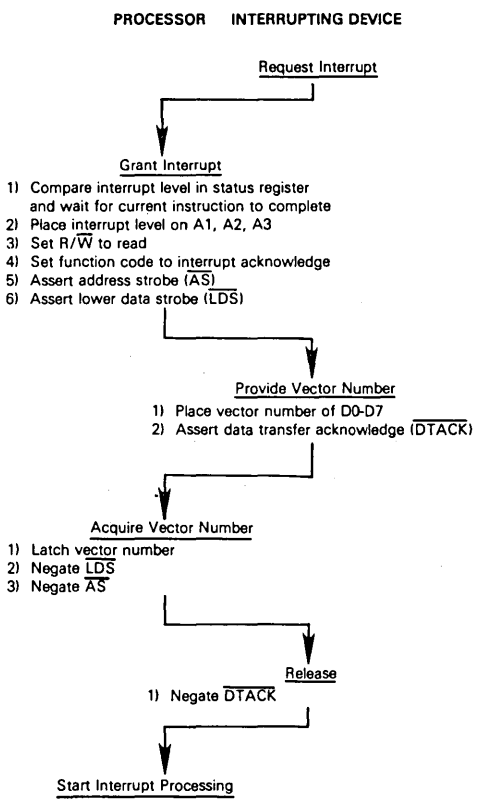
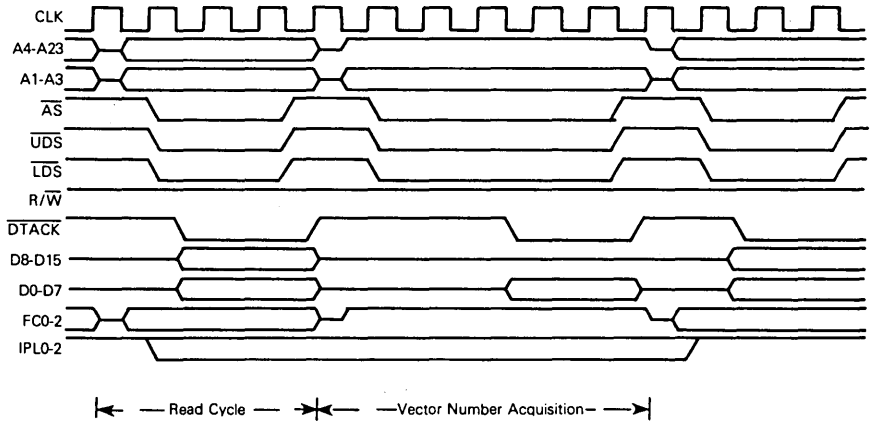


FIGURE 25 — INTERRUPT ACKNOWLEDGE SEQUENCE TIMING DIAGRAM



Priority level seven is a special case. Level seven interrupts cannot be inhibited by the interrupt priority mask, thus providing a "non-maskable interrupt" capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven. Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction.

INSTRUCTION TRAPS. Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception, and is useful for implementing system calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithmetic overflow or a subscript out of bounds.

The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

ILLEGAL AND UNIMPLEMENTED INSTRUCTIONS. Illegal instruction is the term used to refer to any of the word bit patterns which are not the bit pattern of the first word of a legal instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs.

Word patterns with bits 15 through 12 equaling 1010 or 1111 are distinguished as unimplemented instructions and separate exception vectors are given to these patterns to permit efficient emulation. This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.

PRIVILEGE VIOLATIONS. In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

STOP	AND (word) Immediate to SR
RESET	EOR (word) Immediate to SR
RTE	OR (word) Immediate to SR
MOVE to SR	MOVE USP

TRACING. To aid in program development, the 68000 includes a facility to allow instruction by instruction tracing. In the trace state, after each instruction is executed an exception is forced, allowing a debugging program to monitor the execution of the program under test.

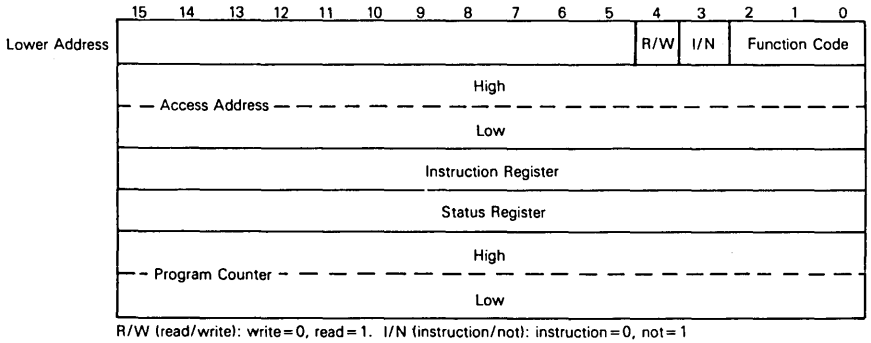
The trace facility uses the T-bit in the supervisor portion of the status register. If the T-bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T-bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated after the execution of that instruction is completed. If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is indeed executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception. If, during the execution of the instruction, an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

BUS ERROR. Bus error exceptions occur when the external logic requests that a bus error be processed by an exception. The current bus cycle which the processor is making is then aborted. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing.

Exception processing for bus error follows the usual sequence of steps. The status register is copied, the supervisor state is entered, and the trace state is turned off. The vector number is generated to refer to the bus error vector. Since the processor was not between instructions when the bus error exception request was made, the context of the processor is more detailed. To save more of this context, additional information is saved on the supervisor stack. The program counter and the copy of the status register are of course saved. The value saved for the program counter is advanced by some amount, two to ten bytes beyond the ad-

FIGURE 26 — SUPERVISOR STACK ORDER



R/W (read/write): write=0, read=1. I/N (instruction/not): instruction=0, not=1

dress of the first word of the instruction which made the reference causing the bus error. If the bus error occurred during the fetch of the next instruction, the saved program counter has a value in the vicinity of the current instruction, even if the current instruction is a branch, a jump, or a return instruction. Besides the usual information, the processor saves its internal copy of the first word of the instruction being processed, and the address which was being accessed by the aborted bus cycle. Specific information about the access is also saved: whether it was a read or a write, whether the processor was processing an instruction or not, and the classification displayed on the function code outputs when the bus error occurred. The processor is processing an instruction if it is in the normal state or processing a Group 2 exception; the processor is not processing an instruction if it is processing a Group 0 or a Group 1 exception. Figure 26 illustrates how this information is organized on the supervisor stack. Although this information is not sufficient in general to effect full recovery from the bus error, it does allow software diagnosis. Finally, the processor commences instruction processing at the address contained in the vector. It is the responsibility of the error handler routine to clean up the stack and determine where to continue execution.

If a bus error occurs during the exception processing for a bus error, address error, or reset, the processor is halted, and all processing ceases. This simplifies the detection of catastrophic system failure, since the processor removes itself from the system rather than destroy all memory contents. Only the RESET pin can restart a halted processor.

ADDRESS ERROR. Address error exceptions occur when the processor attempts to access a word or a long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted, and the processor ceases whatever processing it is currently doing and begins exception processing. After exception processing commences, the sequence is the same as that for bus error including the information that is stacked, except that the vector number refers to the address error vector instead. Likewise, if an address error occurs during the exception processing for a bus error, address error, or reset, the processor is halted.

INTERFACE WITH R6500 PERIPHERALS

Rockwell's line of R6500 peripherals are directly compatible with the 68000. Some of these devices that are particularly useful are:

R6520 Peripheral Interface Adapter (PIA)

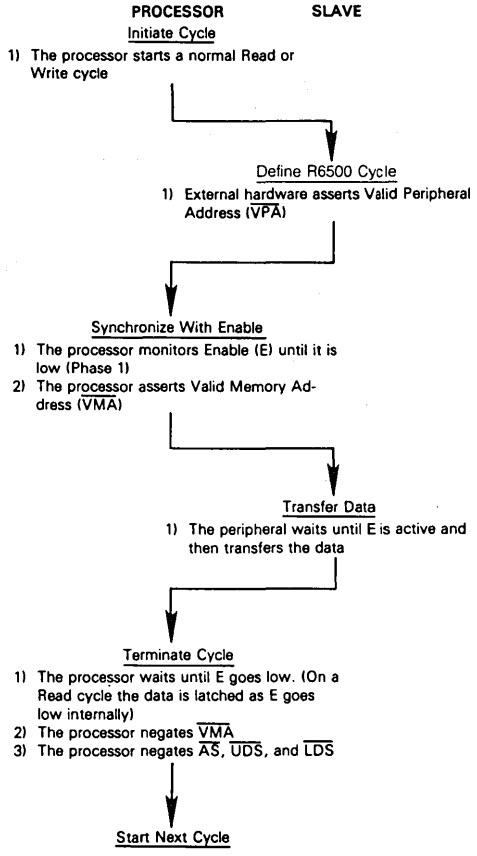
R6522 Versatile Interface Adapter (VIA)

R6545 CRT Controller

R6551 Asynchronous Communication Interface Adapter

To interface the synchronous R6500 peripherals with the asynchronous 68000, the processor modifies its bus cycle to meet the R6500 cycle requirements whenever an R6500 device address is detected. This is possible since both processors use memory mapped I/O. Figure 27 is a flow chart of the interface operation between the processor and R6500 devices. 6800 peripherals are also compatible with the 68000 processor.

FIGURE 27 — R6500 INTERFACING FLOW CHART



DATA TRANSFER OPERATION

Three signals on the processor provide the R6500 interface. They are: enable (E), valid memory address ($\overline{VMA}$), and valid peripheral address ($\overline{VPA}$). Enable corresponds to the E or $\phi 2$ signal in existing R6500 systems. It is the bus clock used by the frequency clock that is one tenth of the incoming 68000 clock frequency. The timing of E allows 1 MHz peripherals to be used with an 8 MHz 68000. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive $\overline{VPA}$ accesses on successive E pulses.

R6500 cycle timing is given in Figure 28. At state zero (S0) in the cycle, the address bus and function codes are in the high-impedance state. One half clock later, in state 1, the address bus and function code outputs are released from the high-impedance state.

During state 2, the address strobe ($\overline{AS}$) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/$\overline{W}$) signal is switched to low (write)

during state 2. One half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus.

The processor now inserts wait states until it recognizes the assertion of $\overline{VPA}$. The $\overline{VPA}$ input signals the processor that the address on the bus is the address of an R6500 device (or an area reserved for R6500 devices) and that the bus should conform to the $\phi 2$ transfer characteristics of the R6500 bus. Valid peripheral address is derived by decoding the address bus, conditioned by address strobe.

After the recognition of $\overline{VPA}$, the processor assures that the Enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the R6500 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal.

During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one half clock cycle later in state 7, and the Enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. During a write cycle, the data bus is put in the high-impedance state and the read/write signal is switched high at this time. The peripheral logic must remove $\overline{VPA}$ within one clock after address strobe is negated.

Figure 29 shows the timing required by R6500 peripherals, the timing specified for the R6500 and the corresponding timing for the 68000. For further details on peripheral timing, consult the current data sheet for the peripheral of interest. Notice that the 68000 $\overline{VMA}$ is active low. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting peripherals.

FIGURE 28 — R6500 CYCLE OPERATION

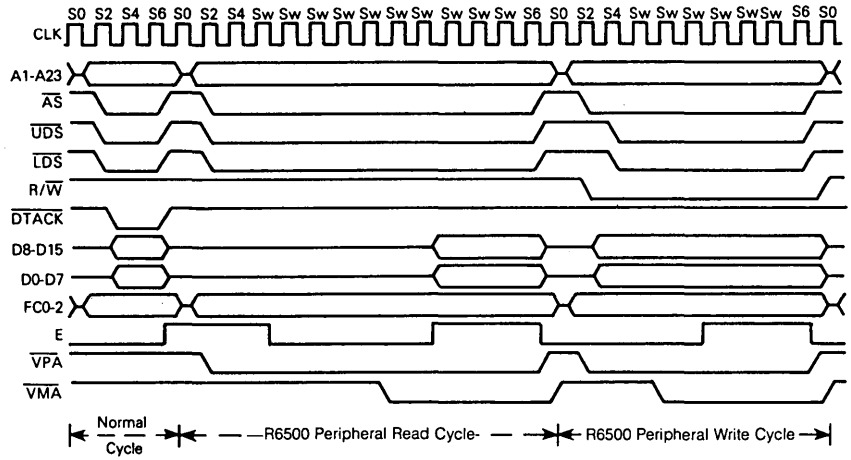
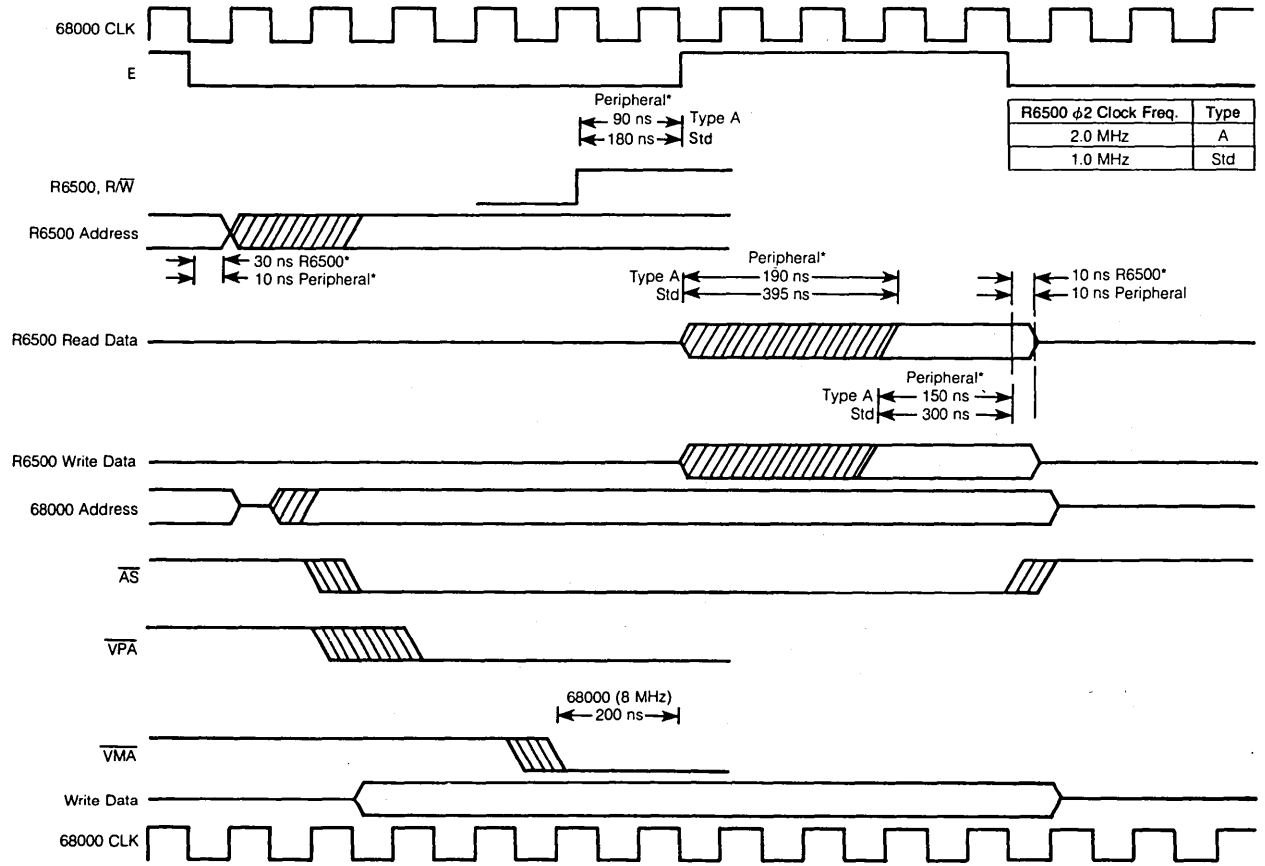


FIGURE 29 — 68000 TO R6500 PERIPHERAL TIMING DIAGRAM



*Times are expressed for different device clock frequencies

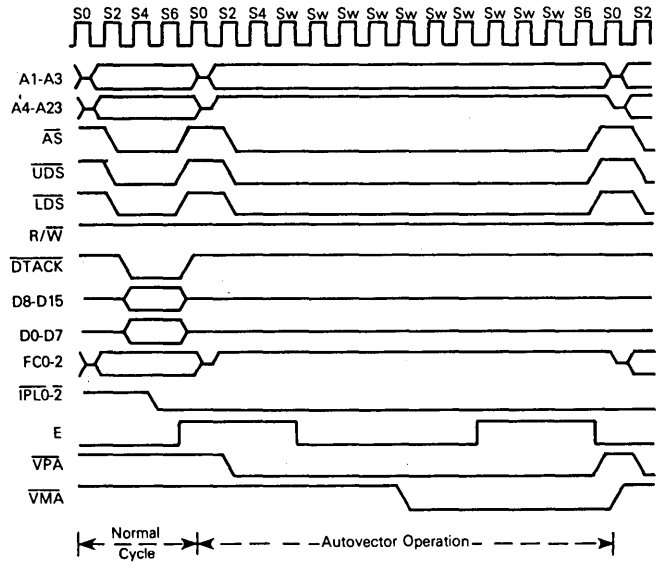
INTERRUPT INTERFACE OPERATION

During an interrupt acknowledge cycle while the processor is fetching the vector, if $\overline{VPA}$ is asserted, the 68000 will assert $\overline{VMA}$ and complete a normal R6500 read cycle as shown in Figure 30. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is known as autovectoring. The seven autovectors are vector numbers 25 through 31 (decimal).

This operates in the same fashion (but is not restricted to) the R6500 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the R6500 and the 68000's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since $\overline{VMA}$ is asserted during autovectoring, the R6500 peripheral address decoding should prevent unintended accesses.

FIGURE 30 — AUTOVECTOR OPERATION TIMING DIAGRAM



INSTRUCTION SET

The following paragraphs provide information about the addressing categories and instruction set of the 68000.

ADDRESSING CATEGORIES

Effective address modes may be categorized by the ways in which they may be used. The following classifications will be used in the instruction definitions.

Data — If an effective address mode may be used to refer to data operands, it is considered a data addressing effective address mode.

Memory — If an effective address mode may be used to refer to memory operands, it is considered a memory addressing effective address mode.

Alterable — If an effective address mode may be used to refer to alterable (writeable) operands, it is considered an alterable addressing effective address mode.

Control — If an effective address mode may be used to refer to memory operands without an associated size, it is considered a control addressing effective address mode.

Table 20 shows the various categories to which each of the effective address modes belong. Table 21 is the instruction set summary.

The status register addressing mode is not permitted unless it is explicitly mentioned as a legal addressing mode.

These categories may be combined, so that additional, more restrictive, classifications may be defined. For example, the instruction descriptions use such classifications as alterable memory or data alterable. The former refers to those addressing modes which are both alterable and memory addresses, and the latter refers to addressing modes which are both data and alterable.

TABLE 20 — EFFECTIVE ADDRESSING MODE CATEGORIES

Effective Address Modes	Mode	Register	Data	Addressing Categories		
				Memory	Control	Alterable
Dn	000	register number	X	–	–	X
An	001	register number	–	–	–	X
An@	010	register number	X	X	X	X
An@ +	011	register number	X	X	–	X
An@ –	100	register number	X	X	–	X
An@(d)	101	register number	X	X	X	X
An@(d, ix)	110	register number	X	X	X	X
xxx.W	111	000	X	X	X	X
xxx.L	111	001	X	X	X	X
PC@(d)	111	010	X	X	X	–
PC@(d, ix)	111	011	X	X	X	–
#xxx	111	100	X	X	–	–

TABLE 21 — INSTRUCTION SET

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	(Destination)$_{10}$ + (Source)$_{10}$ → Destination	*	U	*	U	*
ADD	Add Binary	(Destination) + (Source) → Destination	*	*	*	*	*
ADDA	Add Address	(Destination) + (Source) → Destination	–	–	–	–	–
ADDI	Add Immediate	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDX	Add Extended	(Destination) + (Source) + X → Destination	*	*	*	*	*
AND	AND Logical	(Destination) Λ (Source) → Destination	–	*	*	0	0
ANDI	AND Immediate	(Destination) Λ Immediate Data → Destination	–	*	*	0	0
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count> → Destination	*	*	*	*	*
B_{CC}	Branch Conditionally	If CC then PC + d → PC	–	–	–	–	–
BCHG	Test a Bit and Change	~(<bit number>) OF Destination → Z ~(<bit number>) OF Destination → <bit number> OF Destination	–	–	*	–	–
BCLR	Test a Bit and Clear	~(<bit number>) OF Destination → Z 0 → <bit number> → OF Destination	–	–	*	–	–
BRA	Branch Always	PC + d → PC	–	–	–	–	–
BSET	Test a Bit and Set	~(<bit number>) OF Destination → Z 1 → <bit number> OF Destination	–	–	*	–	–
BSR	Branch to Subroutine	PC → SP@ – ; PC + d → PC	–	–	–	–	–
BTST	Test a Bit	~(<bit number>) OF Destination → Z	–	–	*	–	–
CHK	Check Register against Bounds	If Dn <0 or Dn> (<ea>) then TRAP	–	*	U	U	U
CLR	Clear an Operand	0 → Destination	–	0	1	0	0
CMP	Compare	(Destination) – (Source)	–	*	*	*	*
CMPA	Compare Address	(Destination) – (Source)	–	*	*	*	*
CMPI	Compare Immediate	(Destination) – Immediate Data	–	*	*	*	*
CMPM	Compare Memory	(Destination) – (Source)	–	*	*	*	*
DB_{CC}	Test Condition, Decrement and Branch	If ~CC then Dn – 1 → Dn; if Dn ≠ – 1 then PC + d → PC	–	–	–	–	–
DIVS	Signed Divide	(Destination)/(Source) → Destination	–	*	*	*	0
DIVU	Unsigned Divide	(Destination)/(Source) → Destination	–	*	*	*	0
EOR	Exclusive OR Logical	(Destination) ⊕ (Source) → Destination	–	*	*	0	0
EORI	Exclusive OR Immediate	(Destination) ⊕ Immediate Data → Destination	–	*	*	0	0
EXG	Exchange Register	Rx ↔ Ry	–	–	–	–	–
EXT	Sign Extend	(Destination) Sign-extended → Destination	–	*	*	0	0
JMP	Jump	Destination → PC	–	–	–	–	–
JSR	Jump to Subroutine	PC → SP@ – ; Destination → PC	–	–	–	–	–
LEA	Load Effective Address	Destination → An	–	–	–	–	–
LINK	Link and Allocate	An → SP@ – ; SP → An; SP + d → SP	–	–	–	–	–
LSL, LSR	Logical Shift	(Destination) Shifted by <count> → Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source) → Destination	–	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source) → CCR	*	*	*	*	*
MOVE to SR	Move to the Status Register	(Source) → SR	*	*	*	*	*

* affected 0 cleared U defined
– unaffected 1 set

TABLE 21 — INSTRUCTION SET (CONTINUED)

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
MOVE from SR	Move from the Status Register	SR → Destination	–	–	–	–	–
MOVE USP	Move User Stack Pointer	USP → An; An → USP	–	–	–	–	–
MOVEA	Move Address	(Source) → Destination	–	–	–	–	–
MOVEM	Move Multiple Registers	Registers → Destination (Source) → Registers	–	–	–	–	–
MOVEP	Move Peripheral Data	(Source) → Destination	–	–	–	–	–
MOVEQ	Move Quick	Immediate Data → Destination	–	•	•	0	0
MULS	Signed Multiply	(Destination)*(Source) → Destination	–	•	•	0	0
MULU	Unsigned Multiply	(Destination)*(Source) → Destination	–	•	•	0	0
NBCD	Negate Decimal with Extend	$0-(\text{Destination})_{10}-X \rightarrow$ Destination	•	U	•	U	•
NEG	Negate	0 – (Destination) → Destination	•	•	•	•	•
NEGX	Negate with Extend	0 – (Destination) – X → Destination	•	•	•	•	•
NOP	No Operation	–	–	–	–	–	–
NOT	Logical Complement	~ (Destination) → Destination	–	•	•	0	0
OR	Inclusive OR Logical	(Destination) v (Source) → Destination	–	•	•	0	0
ORI	Inclusive OR Immediate	(Destination) v Immediate Data → Destination	–	•	•	0	0
PEA	Push Effective Address	Destination → SP@ –	–	–	–	–	–
RESET	Reset External Devices	–	–	–	–	–	–
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count> → Destination	–	•	•	0	•
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count> → Destination	•	•	•	0	•
RTE	Return from Exception	SP@ – → SR; SP@ + → PC	•	•	•	•	•
RTR	Return and Restore Condition Codes	SP@ + → CC; SP@ + → PC	•	•	•	•	•
RTS	Return from Subroutine	SP@ + → PC	–	–	–	–	–
SBCD	Subtract Decimal with Extend	$(\text{Destination})_{10}-(\text{Source})_{10}-X \rightarrow$ Destination	•	U	•	U	•
S_{CC}	Set According to Condition	If CC then 1's → Destination else 0's → Destination	–	–	–	–	–
STOP	Load Status Register and Stop	Immediate Data → SR; STOP	•	•	•	•	•
SUB	Subtract Binary	(Destination) – (Source) → Destination	•	•	•	•	•
SUBA	Subtract Address	(Destination) – (Source) → Destination	–	–	–	–	–
SUBI	Subtract Immediate	(Destination) – Immediate Data → Destination	•	•	•	•	•
SUBQ	Subtract Quick	(Destination) – Immediate Data → Destination	•	•	•	•	•
SUBX	Subtract with Extend	(Destination) – (Source) – X → Destination	•	•	•	•	•
SWAP	Swap Register Halves	Register [31:16] ↔ Register [15:0]	–	•	•	0	0
TAS	Test and Set an Operand	(Destination) Tested → CC; 1 → [7] OF Destination	–	•	•	0	0
TRAP	Trap	PC → SSP@ – ; SR → SSP@ – ; (Vector) → PC	–	–	–	–	–
TRAPV	Trap on Overflow	If V then TRAP	–	–	–	–	–
TST	Test an Operand	(Destination) Tested → CC	–	•	•	0	0
UNLK	Unlink	An → SP; SP@ + → An	–	–	–	–	–

[ ] = bit number

INSTRUCTION EXECUTION TIMES

The following paragraphs contain listings of the instruction execution times in terms of external clock (CLK) periods. In this timing data, it is assumed that the memory cycle time is no greater than four periods of the external processor clock input, which prevents the insertion of wait states in the bus cycle. The number of bus read and write cycles for each instruction is also included with the timing data. This data is enclosed in parenthesis following the execution periods and is shown as: (r/w) where r is the number of read cycles and w is the number of write cycles.

NOTE

The number of periods includes instruction fetch and all applicable operand fetches and stores.

EFFECTIVE ADDRESS OPERAND CALCULATION TIMING

Table 22 lists the number of clock periods required to compute an instruction's effective address. It includes fetching of any extension words, the address computation, and fetching of the memory operand. The number of bus read and write cycles is shown in parenthesis as (r/w). Note there are no write cycles involved in processing the effective address.

MOVE INSTRUCTION CLOCK PERIODS

Tables 23 and 24 indicate the number of clock periods for the move instruction. This data includes instruction fetch, operand reads, and operand writes. The number of bus read and write cycles is shown in parenthesis as: (r/w).

STANDARD INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 25 indicates the time required to perform the operations, store the results, and read the next instruction. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

In Table 25, the headings have the following meanings: An = address register operand, Dn = data register operand, ea = an operand specified by an effective address, and M = memory effective address operand.

IMMEDIATE INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 26 includes the time to fetch immediate operands, perform the operations, store the results, and read the next operation. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

In Table 26, the headings have the following meanings: # = immediate operand, Dn = data register operand, M = memory operand, and SR = status register.

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 27 indicates the number of clock periods for the single operand instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

TABLE 22 — EFFECTIVE ADDRESS CALCULATION TIMING

Addressing Mode		Byte, Word	Long
	Register		
Dn	Data Register Direct	0(0/0)	0(0/0)
An	Address Register Direct	0(0/0)	0(0/0)
	Memory		
An@	Address Register Indirect	4(1/0)	8(2/0)
An@+	Address Register Indirect with Postincrement	4(1/0)	8(2/0)
An@–	Address Register Indirect with Predecrement	6(1/0)	10(2/0)
An@(d)	Address Register Indirect with Displacement	8(2/0)	12(3/0)
An@(d, ix)*	Address Register Indirect with Index	10(2/0)	14(3/0)
xxx.W	Absolute Short	8(2/0)	12(3/0)
xxx.L	Absolute Long	12(3/0)	16(4/0)
PC@(d)	Program Counter with Displacement	8(2/0)	12(3/0)
PC@(d, ix)*	Program Counter with Index	10(2/0)	14(3/0)
#xxx	Immediate	4(1/0)	8(2/0)

*The size of the index register (ix) does not affect execution time.

TABLE 23 — MOVE BYTE AND WORD INSTRUCTION CLOCK PERIODS

Source	Destination								
	Dn	An	An@	An@ +	An@ –	An@(d)	An@(d,ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	9(1/1)	9(1/1)	9(1/1)	13(2/1)	15(2/1)	13(2/1)	17(3/1)
An	4(1/0)	4(1/0)	9(1/1)	9(1/1)	9(1/1)	13(2/1)	15(2/1)	13(2/1)	17(3/1)
An@	8(2/0)	8(2/0)	13(2/1)	13(2/1)	13(2/1)	17(3/1)	19(3/1)	17(3/1)	21(4/1)
An@ +	8(2/0)	8(2/0)	13(2/1)	13(2/1)	13(2/1)	17(3/1)	19(3/1)	17(3/1)	21(4/1)
An@ –	10(2/0)	10(2/0)	15(2/1)	15(2/1)	15(3/1)	19(3/1)	21(3/1)	19(3/1)	23(4/1)
An@(d)	12(3/0)	12(3/0)	17(3/1)	17(3/1)	17(3/1)	21(4/1)	23(4/1)	21(4/1)	25(5/1)
An@(d, ix)*	14(3/0)	14(3/0)	19(3/1)	19(3/1)	19(3/1)	23(4/1)	25(4/1)	23(4/1)	27(5/1)
xxx.W	12(3/0)	12(3/0)	17(3/1)	17(3/1)	17(3/1)	21(4/1)	23(4/1)	21(4/1)	25(5/1)
xxx.L	16(4/0)	16(4/0)	21(4/1)	21(4/1)	21(4/1)	25(5/1)	27(5/1)	25(5/1)	29(6/1)
PC@(d)	12(3/0)	12(3/0)	17(3/1)	17(3/1)	17(3/1)	21(4/1)	23(4/1)	21(4/1)	25(5/1)
PC@(d, ix)*	14(3/0)	14(3/0)	19(3/1)	19(3/1)	19(3/1)	23(4/1)	25(4/1)	23(4/1)	27(5/1)
#xxx	8(2/0)	8(2/0)	13(2/1)	13(2/1)	13(2/1)	17(3/1)	19(3/1)	17(3/1)	21(4/1)

*The size of the index register (ix) does not affect execution time.

TABLE 24 — MOVE LONG INSTRUCTION CLOCK PERIODS

Source	Destination								
	Dn	An	An@	An@ +	An@ –	An@(d)	An@(d,ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	14(1/2)	14(1/2)	16(1/2)	18(2/2)	20(2/2)	18(2/2)	22(3/2)
An	4(1/0)	4(1/0)	14(1/2)	14(1/2)	16(1/2)	18(2/2)	20(2/2)	18(2/2)	22(3/2)
An@	12(3/0)	12(3/0)	22(3/2)	22(3/2)	22(3/2)	26(4/2)	28(4/2)	26(4/2)	30(5/2)
An@ +	12(3/0)	12(3/0)	22(3/2)	22(3/2)	22(3/2)	26(4/6)	28(4/2)	26(4/2)	30(5/2)
An@ –	14(3/0)	14(3/0)	24(3/2)	24(3/2)	24(3/2)	28(4/2)	30(4/2)	28(4/2)	32(5/2)
An@(d)	16(4/0)	16(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
An@(d, ix)*	18(4/0)	18(4/0)	28(4/2)	28(4/2)	28(4/2)	32(5/2)	34(5/2)	32(5/2)	36(6/2)
xxx.W	16(4/0)	16(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
xxx.L	20(5/0)	20(5/0)	30(5/2)	30(5/2)	30(5/2)	34(6/2)	36(6/2)	34(6/2)	38(7/2)
PC@(d)	16(4/0)	16(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
PC@(d, ix)*	18(4/0)	18(4/0)	28(4/2)	28(4/2)	28(4/2)	32(5/2)	34(5/2)	32(5/2)	36(6/2)
#xxx	12(3/0)	12(3/0)	22(3/2)	22(3/2)	22(3/2)	26(4/2)	28(4/2)	26(4/2)	30(5/2)

*The size of the index register (ix) does not affect execution time.

TABLE 25 — STANDARD INSTRUCTION CLOCK PERIODS

Instruction	Size	op <ea>, An	op <ea>, Dn	op Dn, <M>
ADD	Byte, Word	8(1/0) +	4(1/0) +	9(1/1) +
	Long	6(1/0) + **	6(1/0) + **	14(1/2) +
AND	Byte, Word	–	4(1/0) +	9(1/1) +
	Long	–	6(1/0) + **	14(1/2) +
CMP	Byte, Word	6(1/0) +	4(1/0) +	–
	Long	6(1/0) +	6(1/0) +	–
DIVS	–	–	158(1/0) + *	–
DIVU	–	–	140(1/0) + *	–
EOR	Byte, Word	–	4(1/0)***	9(1/1) +
	Long	–	8(1/0)***	14(1/2) +
MULS	–	–	70(1/0) + *	–
MULU	–	–	70(1/0) + *	–
OR	Byte, Word	–	4(1/0) +	9(1/1) +
	Long	–	6(1/0) + **	14(1/2) +
SUB	Byte, Word	8(1/0) +	4(1/0) +	9(1/1) +
	Long	6(1/0) + **	6(1/0) + **	14(1/2) +

+ add effective address calculation time
** total of 8 clock periods for instruction if the effective address is register direct
* indicates maximum value
*** only available effective address mode is data register direct

TABLE 26 — IMMEDIATE INSTRUCTION CLOCK PERIODS

Instruction	Size	op #, Dn	op #, M	op #, SR
ADDI	Byte, Word	8(2/0)	13(2/1)+	—
	Long	16(3/0)	22(3/2)+	—
ADDQ	Byte, Word	4(1/0)	9(1/1)+	—
	Long	8(1/0)	14(1/2)+	—
ANDI	Byte, Word	8(2/0)	13(2/1)+	20(3/0)
	Long	16(3/0)	22(3/2)+	—
CMPI	Byte, Word	8(2/0)	8(2/0)+	—
	Long	14(3/0)	12(3/0)+	—
EORI	Byte, Word	8(2/0)	13(2/1)+	20(3/0)
	Long	16(3/0)	22(3/2)+	—
MOVEQ	Long	4(1/0)	—	—
ORI	Byte, Word	8(2/0)	13(2/1)+	20(3/0)
	Long	16(3/0)	22(3/2)+	—
SUBI	Byte, Word	8(2/0)	13(2/1)+	—
	Long	16(3/0)	22(3/2)+	—
SUBQ	Byte, Word	4(1/0)	9(1/1)+	—
	Long	8(1/0)	14(1/2)+	—

+ add effective address calculation time

TABLE 27 — SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Instruction	Size	Register	Memory
CLR	Byte, Word	4(1/0)	9(1/1)+
	Long	6(1/0)	14(1/2)+
NBCD	Byte	6(1/0)	9(1/1)+
NEG	Byte, Word	4(1/0)	9(1/1)+
	Long	6(1/0)	14(1/2)+
NEGX	Byte, Word	4(1/0)	9(1/1)+
	Long	6(1/0)	14(1/2)+
NOT	Byte, Word	4(1/0)	9(1/1)+
	Long	6(1/0)	14(1/2)+
Scc	Byte, False	4(1/0)	9(1/1)+
	Byte, True	6(1/0)	9(1/1)+
TAS	Byte	4(1/0)	11(1/1)+
TST	Byte, Word	4(1/0)	4(1/0)
	Long	4(1/0)	4(1/0)+

+ add effective address calculation time

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 28 indicates the number of clock periods for the shift and rotate instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 29 indicates the number of clock periods required for the bit manipulation instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 30 indicates the number of clock periods required for the conditional instructions. The number of bus read and write cycles is indicated in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Table 31 indicates the number of clock periods required for the jump, jump to subroutine, load effective address, push effective address, and move multiple registers instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w).

TABLE 28 — SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Instruction	Size	Register	Memory
ASR, ASL	Byte, Word	6 + 2n(1/0)	9(1/1)+
	Long	8 + 2n(1/0)	—
LSR, LSL	Byte, Word	6 + 2n(1/0)	9(1/1)+
	Long	8 + 2n(1/0)	—
ROR, ROL	Byte, Word	6 + 2n(1/0)	9(1/1)+
	Long	8 + 2n(1/0)	—
ROXR, ROXL	Byte, Word	6 + 2n(1/0)	9(1/1)+
	Long	8 + 2n(1/0)	—

TABLE 29 — BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Instruction	Size	Dynamic		Static	
		Register	Memory	Register	Memory
BCHG	Byte	—	9(1/1)+	—	13(2/1)+
	Long	8(1/0)*	—	12(2/0)*	—
BCLR	Byte	—	9(1/1)+	—	13(2/1)+
	Long	10(1/0)*	—	14(2/0)*	—
BSET	Byte	—	9(1/1)+	—	13(2/1)+
	Long	8(1/0)*	—	12(2/0)*	—
BTST	Byte	—	4(1/0)+	—	8(2/0)+
	Long	6(1/0)	—	10(2/0)	—

+ add effective address calculation time

* indicates maximum value

TABLE 30 — CONDITIONAL INSTRUCTION CLOCK PERIODS

Instruction	Displacement	Trap or Branch Taken	Trap or Branch Not Taken
B_{CC}	Byte	10(1/0)	8(1/0)
	Word	10(1/0)	12(2/0)
BRA	Byte	10(1/0)	—
	Word	10(1/0)	—
BSR	Byte	20(2/2)	—
	Word	20(2/2)	—
DB_{CC}	CC true	—	12(2/0)
	CC false	10(2/0)	14(3/0)
CHK	—	43(5/3)+*	8(1/0)+
TRAP	—	37(4/3)	—
TRAPV	—	37(5/3)	4(1/0)

+ add effective address calculation time

* indicates maximum value

TABLE 31 — JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Instr	Size	An@	An@+	An@–	An@(d)	An@(d, ix)*	xxx.W	xxx.L	PC@(d)	PC@(d, ix)*
JMP	–	8(2/0)	–	–	10(2/0)	14(3/0)	10(2/0)	12(3/0)	10(2/0)	14(3/0)
JSR	–	18(2/2)	–	–	20(2/2)	24(2/2)	20(2/2)	22(3/2)	20(2/2)	24(2/2)
LEA	–	4(1/0)	–	–	8(2/0)	12(2/0)	8(2/0)	12(3/0)	8(2/0)	12(2/0)
PEA	–	14(1/2)	–	–	18(2/2)	22(2/2)	18(2/2)	22(3/2)	18(2/2)	22(2/2)
MOVEM M→R	Word	12+4n (3+n/0)	12+4n (3+n/0)	– –	16+4n (4+n/0)	18+4n (4+n/0)	16+4n (4+n/0)	20+4n (5+n/0)	16+4n (4+n/0)	18+4n (4+n/0)
	Long	12+8n (3+2n/0)	12+8n (3+2n/0)	– –	16+8n (4+2n/0)	18+8n (4+2n/0)	16+8n (4+2n/0)	20+8n (5+2n/0)	16+8n (4+2n/0)	18+8n (4+2n/0)
MOVEM R→M	Word	8+5n (2/n)	– –	8+5n (2/n)	12+5n (3/n)	14+5n (3/n)	12+5n (3/n)	16+5n (4/n)	– –	– –
	Long	8+10n (2/2n)	– –	8+10n (2/2n)	12+10n (3/2n)	14+10n (3/2n)	12+10n (3/2n)	16+10n (4/2n)	– –	– –

n is the number of registers to move

* is the size of the index register (ix) does not affect the instruction's execution time

TABLE 32 — MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Instruction	Size	op Dn, Dn	op M, M
ADDX	Byte, Word	4(1/0)	19(3/1)
	Long	8(1/0)	32(5/2)
CMPM	Byte, Word	–	12(3/0)
	Long	–	20(5/0)
SUBX	Byte, Word	4(1/0)	19(3/1)
	Long	8(1/0)	32(5/2)
ABCD	Byte	6(1/0)	19(3/1)
SBCD	Byte	6(1/0)	19(3/1)

MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 32 indicates the number of clock periods for the multi-precision instructions. The number of clock periods includes the time to fetch both operands, perform the operations, store the results, and read the next instructions. The number of read and write cycles is shown in parenthesis as: (r/w).

In Table 32, the headings have the following meanings: Dn = data register operand and M = memory operand.

MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 33 indicates the number of clock periods for the following miscellaneous instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

EXCEPTION PROCESSING CLOCK PERIODS

Table 34 indicates the number of clock periods for exception processing. The number of clock periods includes the time for all stacking, the vector fetch, and the fetch of the first instruction of the handler routine. The number of bus read and write cycles is shown in parenthesis as: (r/w).

TABLE 33 — MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Instruction	Size	Register	Memory	Register → Memory	Memory → Register
MOVE from SR	—	6(1/0)	9(1/1)+	—	—
MOVE to CCR	—	12(2/0)	12(2/0)+	—	—
MOVE to SR	—	12(2/0)	12(2/0)+	—	—
MOVEP	Word	—	—	18(2/2)	16(4/0)
	Long	—	—	28(2/4)	24(6/0)
EXG	—	6(1/0)	—	—	—
EXT	Word	4(1/0)	—	—	—
	Long	4(1/0)	—	—	—
LINK	—	18(2/2)	—	—	—
MOVE from USP	—	4(1/0)	—	—	—
MOVE to USP	—	4(1/0)	—	—	—
NOP	—	4(1/0)	—	—	—
RESET	—	132(1/0)	—	—	—
RTE	—	20(5/0)	—	—	—
RTR	—	20(5/0)	—	—	—
RTS	—	16(4/0)	—	—	—
STOP	—	4(0/0)	—	—	—
SWAP	—	4(1/0)	—	—	—
UNLK	—	12(3/0)	—	—	—

+ add effective address calculation time

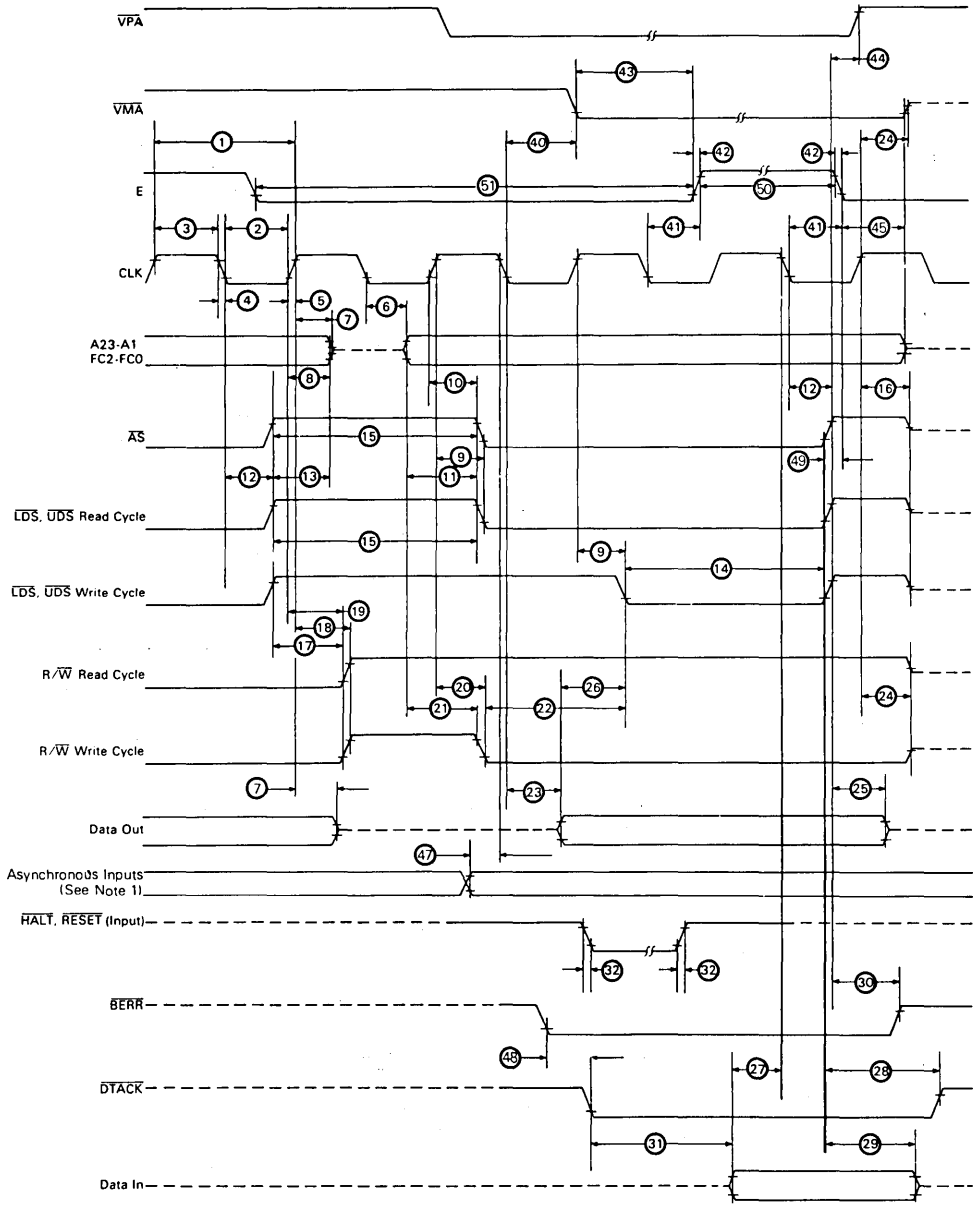
TABLE 34 — EXCEPTION PROCESSING CLOCK PERIODS

Exception	Periods
Address Error	57(4/7)
Bus Error	57(4/7)
Interrupt	47(5/3)*
Illegal Instruction	37(4/3)
Privileged Instruction	37(4/3)
Trace	37(4/3)

*The interrupt acknowledge bus cycle is assumed to take four external clock periods

FIGURE 31 — AC ELECTRICAL WAVEFORMS

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTE 1: Setup time for the asynchronous inputs BERR, BGACK, BR, DTACK, IPL0-IPL2, and VPA guarantees their recognition at the next falling edge of the clock.

NOTE 2: Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 volts, logic low = 0.8 volts.

AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figure 31)

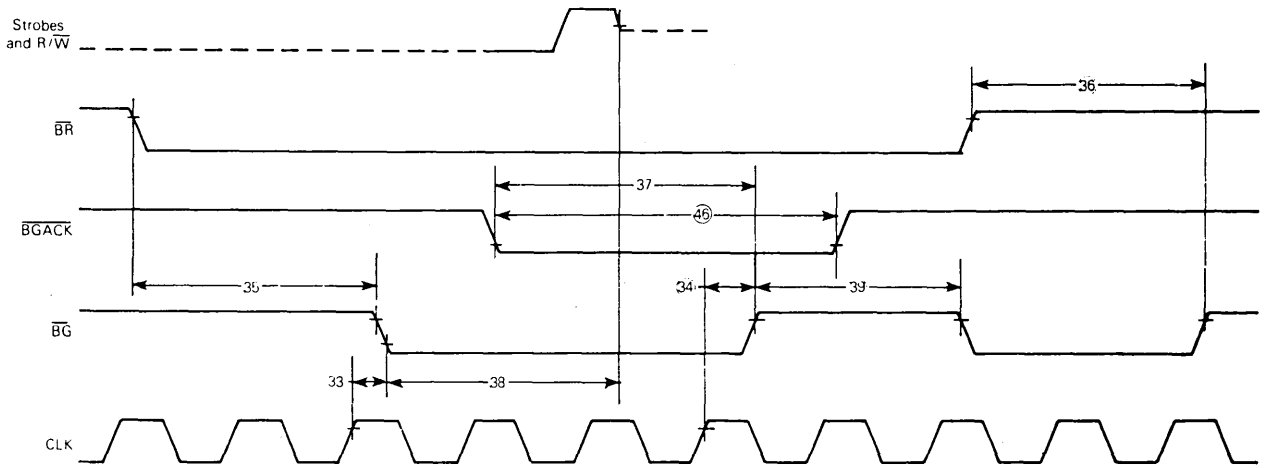
Number	Characteristic	Symbol	4 MHZ R68000C4		6 MHz R68000C6		8 MHz R68000C8		Unit
			Min	Max	Min	Max	Min	Max	
1	Clock Period	t_{cyc}	250	500	167	500	125	500	ns
2	Clock Width Low	t_{CL}	115	250	75	250	55	250	ns
3	Clock Width High	t_{CH}	115	250	75	250	55	250	ns
4	Clock Fall Time	t_{Cf}	—	10	—	10	—	10	ns
5	Clock Rise Time	t_{Cr}	—	10	—	10	—	10	ns
6	Clock Low to Address/FC Valid	t_{CLAV}	—	90	—	80	—	70	ns
7	Clock High to Address/FC/Data High Impedance (maximum)	t_{CHAZx}	—	120	—	100	—	80	ns
8	Clock High to Address/FC Invalid (minimum)	t_{CHAZn}	20	—	20	—	20	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Low (maximum)	t_{CHSLx}	—	80	—	70	—	60	ns
10	Clock High to $\overline{AS}$, $\overline{DS}$ Low (minimum)	t_{CHSLn}	20	—	20	—	20	—	ns
11[2]	Address/FC Valid to $\overline{AS}$, $\overline{DS}$ (read) Low	t_{AVSL}	55	—	35	—	30	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}	—	90	—	80	—	70	ns
13[2]	$\overline{AS}$, $\overline{DS}$ High to Address/FC Invalid	t_{SHAZ}	60	—	40	—	30	—	ns
14[2]	$\overline{AS}$, $\overline{DS}$ Width Low	t_{SL}	285	—	170	—	115	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width High	t_{SH}	285	—	180	—	150	—	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$ High Impedance	t_{CHSZ}	—	120	—	100	—	80	ns
17[2]	$\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	60	—	50	—	40	—	ns
18[1]	Clock High to R/$\overline{W}$ High (maximum)	t_{CHRH}	—	90	—	80	—	70	ns
19	Clock High to R/$\overline{W}$ High (minimum)	t_{CHRHn}	20	—	20	—	20	—	ns
20[1]	Clock High to R/$\overline{W}$ Low	t_{CHRL}	—	90	—	80	—	70	ns
21[2]	Address/FC Valid to R/$\overline{W}$ Low	t_{AVRL}	45	—	25	—	20	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Low (write)	t_{RLSL}	200	—	140	—	80	—	ns
23	Clock Low to Data Out Valid	t_{CLDO}	—	90	—	80	—	70	ns
24	Clock High to R/$\overline{W}$, $\overline{VMA}$ High Impedance	t_{CHRZ}	—	120	—	100	—	80	ns
25[2]	$\overline{DS}$ High to Data Out Invalid	t_{SHDO}	60	—	40	—	30	—	ns
26[2]	Data Out Valid to $\overline{DS}$ Low (write)	t_{DOSL}	55	—	35	—	30	—	ns
27	Data In to Clock Low (set up time)	t_{DICL}	30	—	25	—	15	—	ns
28[2]	$\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAH}	0	240	0	160	0	120	ns
29	$\overline{DS}$ High to Data Invalid (hold time)	t_{SHDI}	0	—	0	—	0	—	ns
30	$\overline{AS}$, $\overline{DS}$ High to $\overline{BERR}$ High	t_{SHBEH}	0	—	0	—	0	—	ns
31[2]	$\overline{DTACK}$ Low to Data In (setup time)	t_{DALDI}	—	180	—	120	—	90	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	t_{RHrf}	0	200	0	200	0	200	ns
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	—	90	—	80	—	70	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	—	90	—	80	—	70	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
38	$\overline{BG}$ Low to Bus High Impedance (with $\overline{AS}$ high)	t_{GLZ}	0	1.5	0	1.5	0	1.5	clk. per.
39	$\overline{BG}$ Width High	t_{GH}	1.5	—	1.5	—	1.5	—	clk. per.
40	Clock Low to $\overline{VMA}$ Low	t_{CLVML}	—	90	—	80	—	70	ns
41	Clock Low to E Transition	t_{CLE}	—	65	—	60	—	55	ns
42	E Output Rise and Fall Time	t_{Erf}	—	25	—	25	—	25	ns
43[2]	$\overline{VMA}$ Low to E High	t_{VMLEH}	325	—	240	—	200	—	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	t_{SHVPH}	0	240	0	160	0	120	ns
45	E Low to Address/$\overline{VMA}$/FC Invalid	t_{ELAI}	55	—	35	—	30	—	ns
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	—	1.5	—	1.5	—	clk. per.
47	Asynchronous Input Setup Time	t_{ASI}	30	—	25	—	20	—	ns
48	$\overline{BERR}$ Low to $\overline{DTACK}$ Low	t_{BELDAL}	50	—	50	—	50	—	ns
49	E Low to $\overline{AS}$, $\overline{DS}$ Invalid	t_{ELSI}	-80	—	-80	—	-80	—	ns
50	E Width High	t_{EH}	900	—	600	—	450	—	ns
51	E Width Low	t_{EL}	1400	—	900	—	700	—	ns

NOTE 1: For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the values given in these columns.

NOTE 2: Actual value depends on actual clock period.

FIGURE 32 – AC ELECTRICAL WAVEFORMS – BUS ARBITRATION

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



AC ELECTRICAL SPECIFICATIONS—BUS ARBITRATION (V_{DD} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figure 32)

Number	Characteristic	Symbol	4 MHZ R68000C4		6 MHz R68000C6		8 MHz R68000C8		Unit
			Min	Max	Min	Max	Min	Max	
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	—	90	—	80	—	70	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	—	90	—	80	—	70	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
38	$\overline{BG}$ Low to Bus High Impedance (with $\overline{AS}$ high)	t_{GLZ}	0	1.5	0	1.5	0	1.5	clk. per.
39	$\overline{BG}$ Width High	t_{GH}	1.5	—	1.5	—	1.5	—	clk. per.
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	—	1.5	—	1.5	—	clk. per.

NOTE 1: Setup time for the asynchronous inputs $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{IPL0}$-$\overline{IPL2}$, and $\overline{VPA}$ guarantees their recognition at the next falling edge of the clock.

NOTE 2: Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 volts, logic low = 0.8 volts.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A 0°C to 70°C, Figures 33, 34, 35)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	2.0	–	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} – 0.3	–	0.8	Vdc
Input Leakage Current	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{IPL0}$-$\overline{IPL2}$, $\overline{VPA}$	I_{in}	–	1.0	–	μAdc
	$\overline{HALT}$, $\overline{RESET}$		–	2.0	–	
Three-State (Off State) Input Current	$\overline{AS}$, A1-A23, D0-D15, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	–	7.0	–	μAdc
Output High Voltage (I_{OH} = –400 μAdc)	$\overline{AS}$, A1-A23, $\overline{BG}$, D0-D15, E, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OH}	2.4	–	–	Vdc
Output Low Voltage						
(I_{OL} = 1.6 mA)	$\overline{HALT}$	V_{OL}	–	–	0.5	Vdc
(I_{OL} = 3.2 mA)	A1-A23, $\overline{BG}$, E, FC0-FC2		–	–	0.5	
(I_{OL} = 5.0 mA)	$\overline{RESET}$		–	–	0.5	
(I_{OL} = 5.3 mA)	$\overline{AS}$, D0-D15, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$		–	–	0.5	
Power Dissipation (Clock Frequency = 8 MHz)		P_D	–	1.0	–	W
Capacitance (Package Type Dependent) (V_{in} = 0 Vdc; T_A = 25°C; Frequency = 1 MHz)		C_{in}	–	10.0	–	pF

FIGURE 33 – RESET TEST LOAD

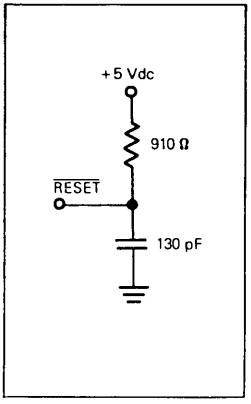


FIGURE 34 – HALT TEST LOAD

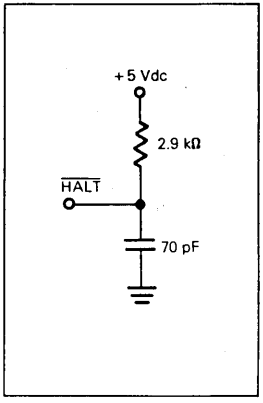


FIGURE 35 – TEST LOADS

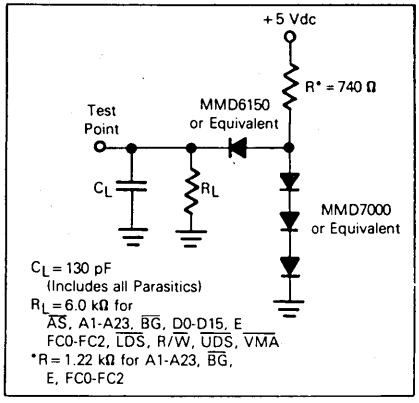
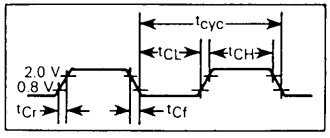


FIGURE 36 – INPUT CLOCK WAVEFORM

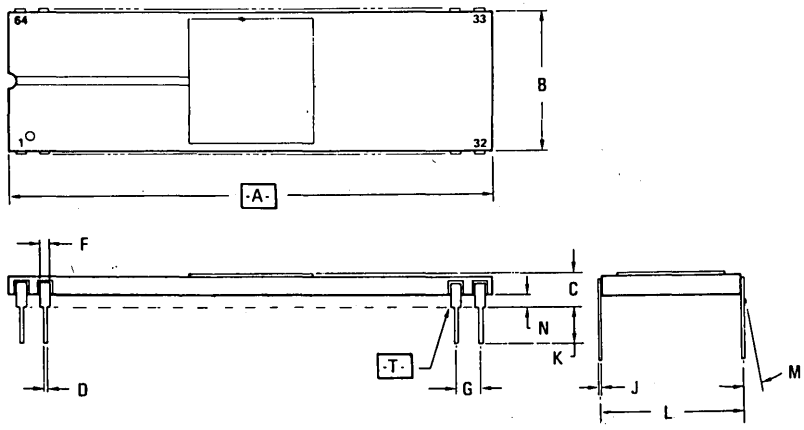


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	Vdc
Input Voltage	V_{in}	–0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

CLOCK TIMING (Figure 36)

Characteristic	Symbol	4 MHz R68000C4		6 MHz R68000C6		8 MHz R68000C8		Unit
		Min	Max	Min	Max	Min	Max	Unit
Frequency of Operation	F	2.0	4.0	2.0	6.0	2.0	8.0	MHz
Cycle Time	t_{cyc}	250	500	167	500	125	500	ns
Clock Pulse Width	t_{CL}	115	250	75	250	55	250	ns
	t_{CH}	115	250	75	250	55	250	
Rise and Fall Times	t_{Cr}	–	10	–	10	–	10	ns
	t_{Cf}	–	10	–	10	–	10	



NOTES:

1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	80.52	82.04	3.170	3.230
B	22.25	22.96	0.876	0.904
C	3.05	4.32	0.120	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	22.61	23.11	0.890	0.910
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

Rockwell

R68000 Microcomputer System
PRODUCT PREVIEW

INTELLIGENT PERIPHERAL CONTROLLER (IPC)

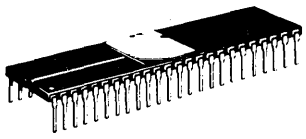
The R68120 Intelligent Peripheral Controller (IPC) is a general-purpose, user-programmable, peripheral controller. It contains a system interface, an 8-bit CPU, a serial communications interface, 21 parallel I/O lines, a 16-bit timer, 2048 bytes of ROM, and eight operating modes. In addition, the R68120 features 128 bytes of dual-ported RAM and six semaphore registers that are accessable to both the internal CPU and an external processor or device through the system interface. The R68120 provides all the control signals necessary to interface with the asynchronous bus of the R68000.

- Bus Compatible with the 16-Bit R68000 Microprocessor
- Bus Compatible with all 6500 and 6800 Family Processors and Peripherals
- TTL Compatible I/O
- Single 5-Volt Power Supply
- 8-Bit CPU
- 2K Bytes ROM
- 128 Bytes Dual-Ported RAM
- 6 Shared Semaphore Registers
- External Clock Input
- 16-Bit Timer
- 21 Parallel I/O and Two Handshake Lines
- Serial Communications Interface
- Interrupt Capability
- Operates in Single-Chip Mode or Expandable to 64K Byte Addressing Range
- DMA Capability
- 8 × 8 Bit Multiply
- Software Control of:
  - Semaphore Registers
  - 16-Bit Timer
  - Serial Communications Interface
  - Parallel I/O Ports
  - Interrupts

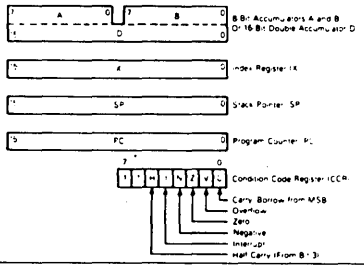
HMOS

(HIGH DENSITY N-CHANNEL, SILICON-GATE DEPLETION LOAD)

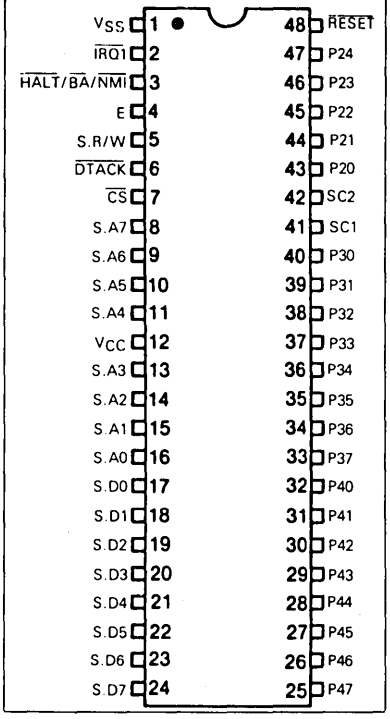
INTELLIGENT PERIPHERAL CONTROLLER



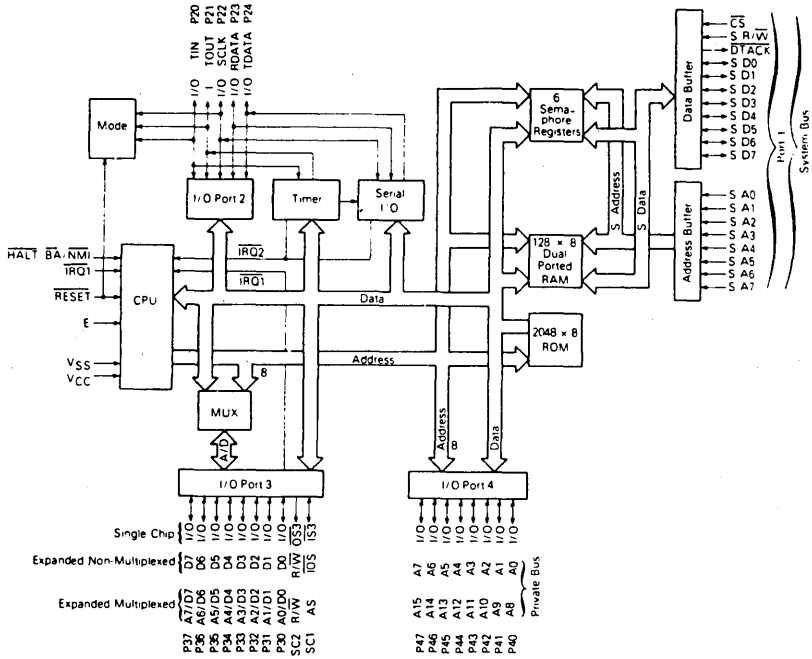
PROGRAMMING MODEL



PIN ASSIGNMENT



BLOCK DIAGRAM



SUMMARY OF OPERATING MODES

Common to all Modes:
- System Bus Interface
- Reserved Register Area
- 6 Semaphore Registers
- I/O Port 2
- 16-Bit Programmable Timer
- Serial Communications Interface
- 128 Bytes of Dual-Ported RAM

Single Chip Mode – Mode 7
- 2048 Bytes of ROM (Internal)
- Port 3 is a Parallel I/O Port with Two Control Lines
- Port 4 is a Parallel I/O Port
- SC1 is Input Strobe 3 (IS3)
- SC2 is Output Strobe 3 (OS3)

Expanded Non-Multiplexed Mode – Mode 5
- 2048 Bytes of ROM (Internal)
- 256 Bytes of External Memory Space
- Port 3 is an 8-Bit Data Bus
- Port 4 is an Address Bus
- SC1 is Input/Output Select (IOS)
- SC2 is Read/Write (R/W)

Expanded Multiplexed Modes – Modes 1, 2, 3, 6
- Four Memory Space Options (64K Address Space):
  - (1) MDOS Compatible
  - (2) No ROM
  - (3) External Vector Space
  - (4) ROM with Partial Address Bus
- External Memory Space Accessed Through:
  - Port 3 as a Multiplexed Address/Data Bus
  - Port 4 as an Address Bus (High)
- SC1 is Address Strobe (AS) Input
- SC2 is Read/Write (R/W)

Test Modes – Modes 0, 4
- Expanded Multiplexed Test Mode – May be Used to Test RAM and ROM
- Single Chip and Non-Multiplexed Test Mode – May be Used to Test Ports 3 and 4 as I/O Ports

AVAILABLE 4Q 1981

Rockwell International

Electronics Devices Division
P.O. Box 3669, RC55; Anaheim, CA 92803
Phone (714) 632-3729

Rockwell

R68000 Microcomputer System
PRODUCT PREVIEW

MEMORY MANAGEMENT UNIT (MMU)

The R68451 Memory Management Unit (MMU) provides address translation and protection of the 16 megabyte addressing space of the R68000. The MMU can be accessed by any potential bus master, such as instruction set processors, or DMA controllers. Each bus master (or processor) in the R68000 family provides a function code and an address during each bus cycle. The function code specifies an address space while the address specifies a location within that address space. The function codes are provided by the R68000 to distinguish between program and data spaces as well as supervisor and user spaces. This separation of address spaces provides the basis of protection in an operating system. By simplifying the programming model of the address space, the MMU also increases the reliability of a complex multi-process system.

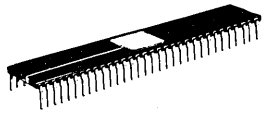
- Separates Address Spaces of System and User Resources
- Provides Write Protection
- Increases System Reliability
- Provides Efficient Memory Allocation
- Allows Interprocess Communication through Shared Resources
- Simplifies Programming Model of Address Space
- Minimizes Operating System Overhead with Quick Context Switches
- 32 Segments with Variable Segment Sizes
- Multiple MMU System Capability
- Supports both Paging and Segmentation
- DMA Compatible
- Provides Virtual Memory Support
- R68000 Bus Compatible

AVAILABLE 1Q 1982

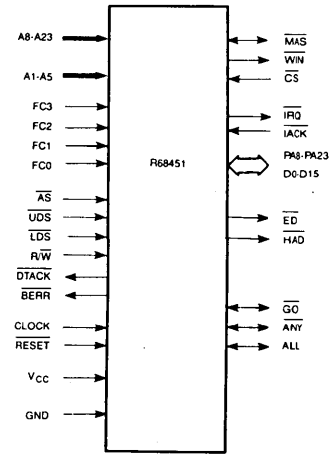
HMOS

(HIGH DENSITY N-CHANNEL, SILICON-GATE DEPLETION LOAD)

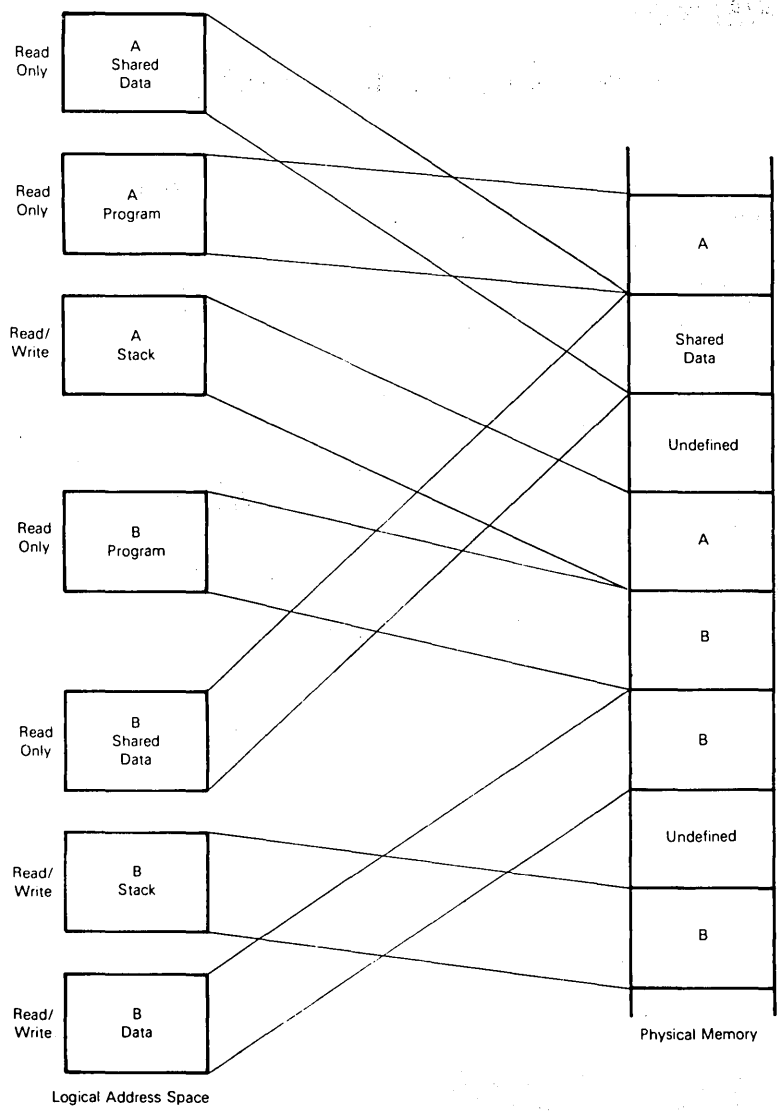
MEMORY MANAGEMENT UNIT



FUNCTIONAL DIAGRAM



MAPPING LOGICAL SEGMENTS TO PHYSICAL MEMORY



Rockwell International

Electronics Devices Division
P.O. Box 3669, RC55; Anaheim, CA 92803
Phone (714) 632-3729

Rockwell

R68000 Microcomputer System
PRODUCT PREVIEW

DIRECT MEMORY ACCESS CONTROLLER (DMAC)

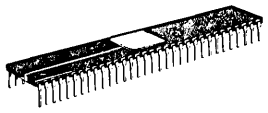
The R68450 Direct Memory Access Controller (DMAC) offers the system designer unparalleled performance where both speed and flexibility in data transfer are required. Sophisticated chaining techniques, memory-to-memory block transfers, and variable bus bandwith utilization result in optimum data transfers. Internal 32-bit address registers provide upward software compatibility with future R68000 Family processors.

- Compatible with both R68000 Family and 6500/6800 Peripherals
- Four, Fully-Independent Channels
- Single or Dual Address Transfers
- Byte, Word, or Long Word Transfers
- Memory-to-Memory Block Transfers
- Supports both Chained and Unchained Operations
- Transfer Rates up to 4 Megabytes Per Second
- Supports Vectored Interrupts
- Supports Array or Linked Array Chaining
- 16-Bit Data Bus
- Programmable Priorities

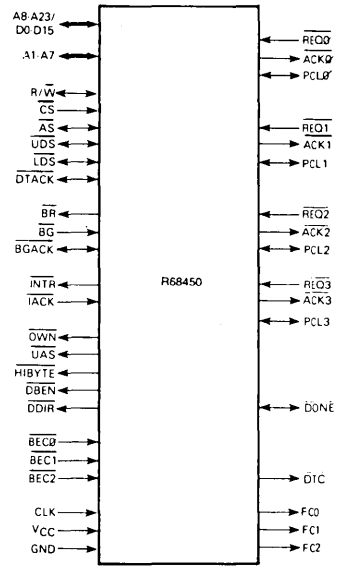
HMOS

(HIGH DENSITY N-CHANNEL, SILICON-GATE DEPLETION LOAD)

DMA CONTROLLER

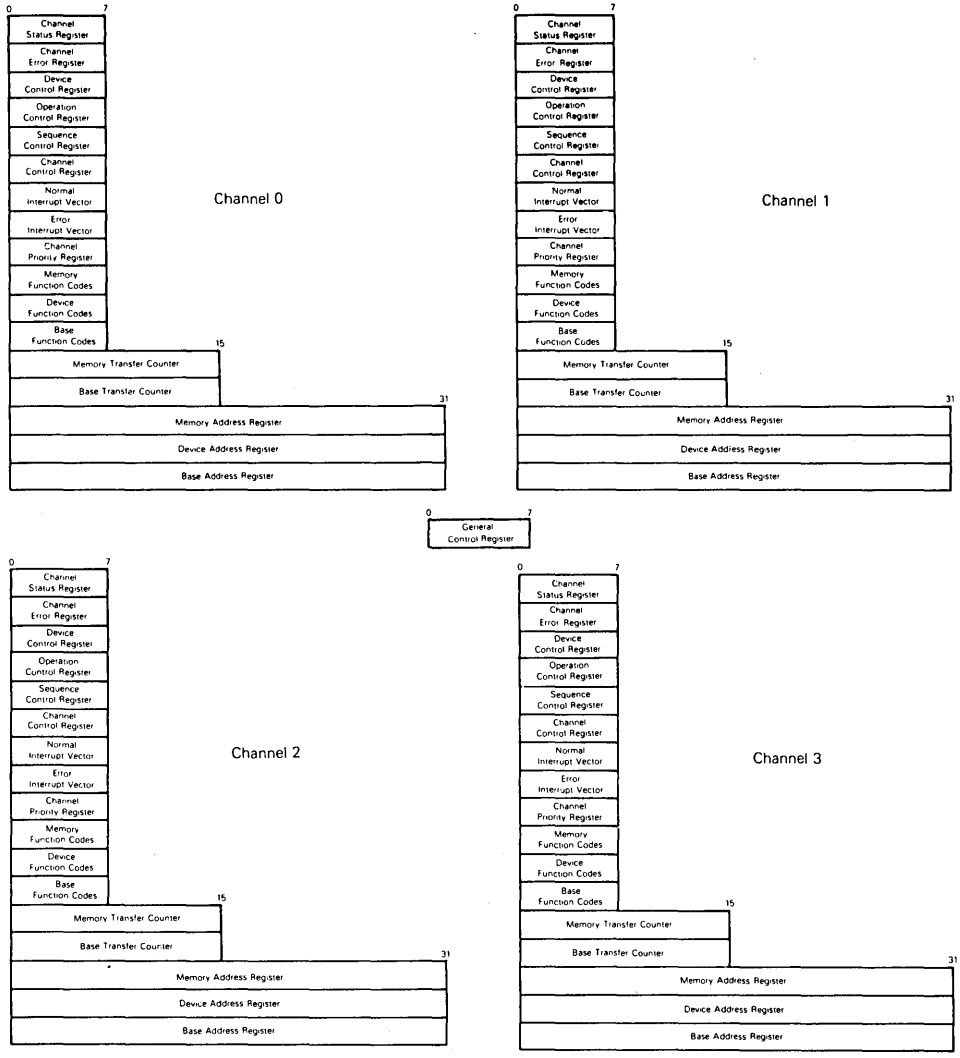


FUNCTIONAL DIAGRAM



AVAILABLE 2Q 1982

INTERNAL ORGANIZATION



Rockwell International

Electronics Devices Division
P.O. Box 3669, RC55; Anaheim, CA 92803
Phone (714) 632-3729

Rockwell

R68000 Microcomputer System
PRODUCT PREVIEW

MULTI-PROTOCOL COMMUNICATIONS CONTROLLER (MPCC)

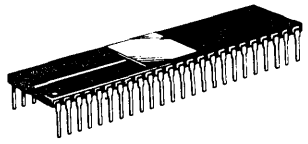
The R68561 Multi-Protocol Communication Controller (MPCC) is a serial data communications interface for the R68000 Family. This device meets the basic interface requirements of asynchronous, bit- and byte-oriented synchronous communication protocols. To keep device count low, the MPCC also contains an internal crystal oscillator and baud rate generator.

- Complete Data Communications Interface
- Line Protocols:
  Asynchronous
  Bit-Oriented Synchronous (X.25, SDLC, HDLC)
  Byte-Oriented Synchronous (BISYNC, DDCMP)
- Interface Compatible with R68450 DMAC
- Self Test Loop Mode
- Single 5-Volt Power Supply
- Full or Half Duplex Operation
- Multiple CRC Character Generation and Error Detection
- Internal Baud Rate Generator
- Internal Crystal Oscillator
- Complete Status Reporting Capability
- Buffered Transmit and Receive Registers
- Supports Vectored Interrupts
- R68000 Bus Compatible

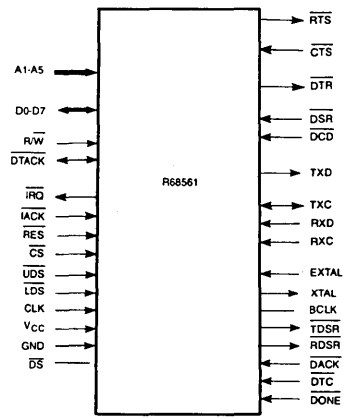
HMOS

(HIGH DENSITY N-CHANNEL, SILICON-GATE DEPLETION LOAD)

MULTI-PROTOCOL COMMUNICATIONS CONTROLLER



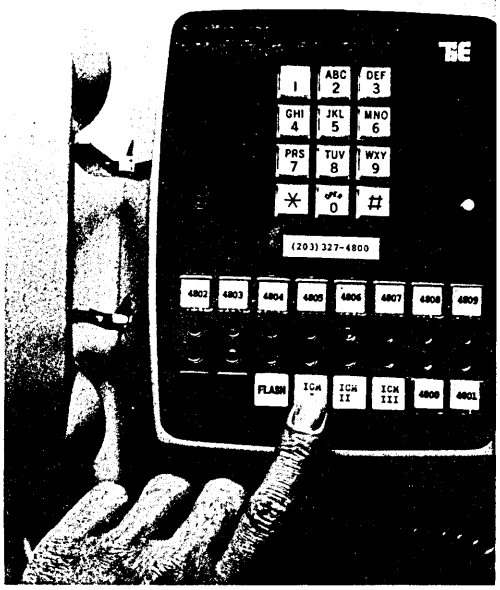
FUNCTIONAL DIAGRAM



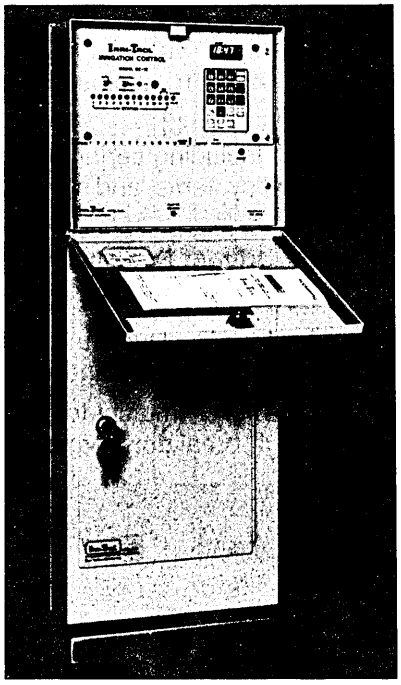
AVAILABLE 3Q 1982

when one-chip gets you more...It's a

Rockwell PPS-4/1



The common component in uncommon success — PPS-4/1 one-chip microcomputer



Rockwell International

. . . where science gets down to business

PPS-4/1 PMOS μCs

Why a Rockwell One-Chip PPS-4/1 Microcomputer Gets You More...

Lower Total System Cost

If you're designing manual-input equipment such as business machines, games, controllers or telephone terminals, Rockwell PPS-4/1 one-chip microcomputers have high promise of lowering your total system costs. These four-bit chips are so powerful they often fit applications where with ordinary one-chip microcomputers you'd need eight-bit devices at about twice the cost.
More than 10 million Rockwell one-chip microcomputers are in use worldwide. Study the chart at right. You'll quickly see why Rockwell PPS-4/1 microcomputers are so cost-conscious and so useful.

Highlights of Features

Instruction efficiency: Typically, instructions are executed in one byte in one cycle and in 10 microseconds — all you need for man-machine interfacing.

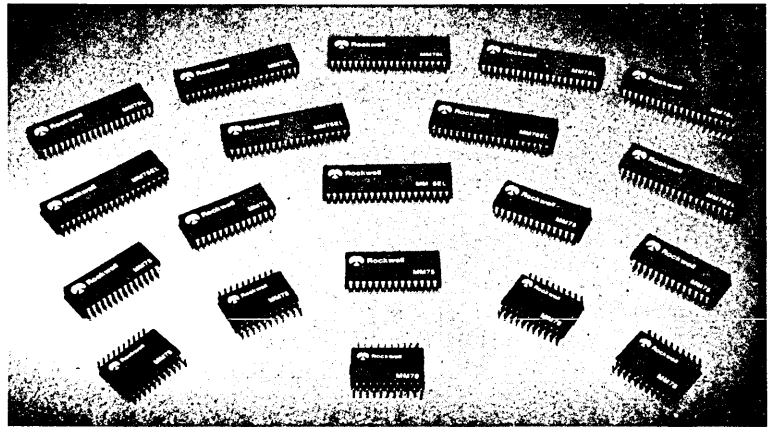
Lots of I/O Ports: Including serial ports for easy cascading or combining with host systems, and some I/O ports will source up to 10 milliamps.

On-Chip Display Drives: Directly drive VF or LED displays.

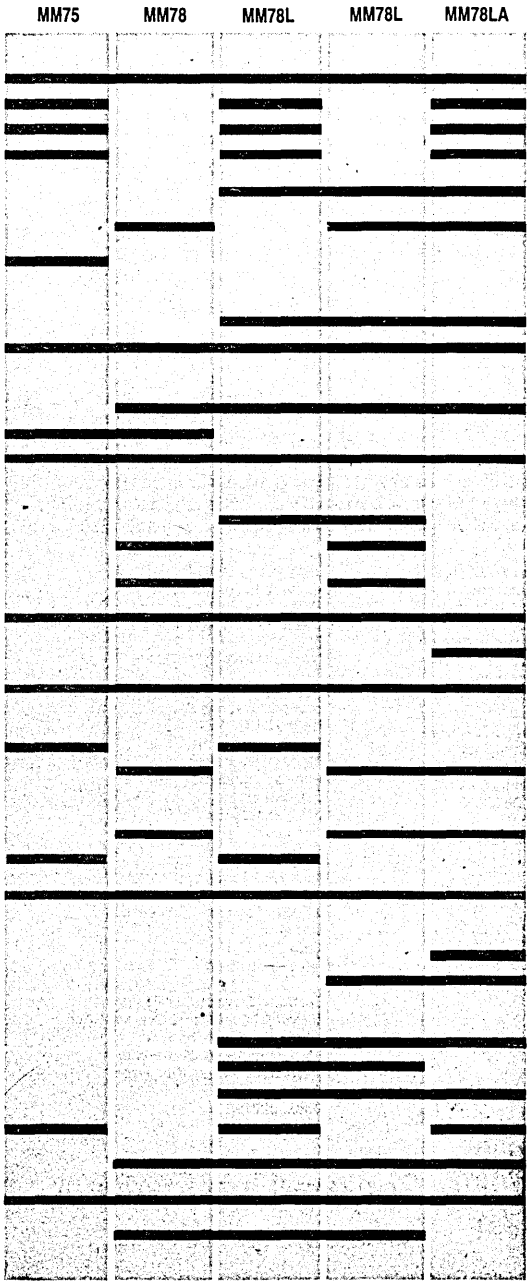
Battery Level Power: In a phrase, "CMOS power at PMOS prices."

Low Cost Designing: Rockwell fully supports you with applications engineering, designers' classes and ready-to-go software packages.

And Much More: High immunity to noise; broad operating voltage tolerances, and high breakdown voltage.



Applications Where Rockwell PPS-4/1 Microcomputers Get You More in End-Product Features for Less Cost



Rockwell PPS-4/1 Microcomputers Get You More Through Low-Cost Design Approaches

Prototype Devices

Rockwell provides a 64-pin DIP Emulation Device for each PPS-4/1 model. The Emulator is designed to interface with external PROM or ROM or RAM, and with peripherals of the total system. This enables you to test your system in real time, including software testing and debugging, and circuit hardware checking. You can even perform field analysis of the prototype equipment prior to submitting your ROM code for production.

XPO-1 Evaluation Module

At the low end of software development operations, Rockwell provides a sophisticated evaluation module with hexadecimal keyboard. Designated XPO-1, this module can be used for software development with a PPS-4/1 Emulator device. It has the advantage of low price — below $500. But developing a full program with it is time-consuming.

SUMMARY OF PPS-4/1 ONE-CHIP MICROCOMPUTER MODELS

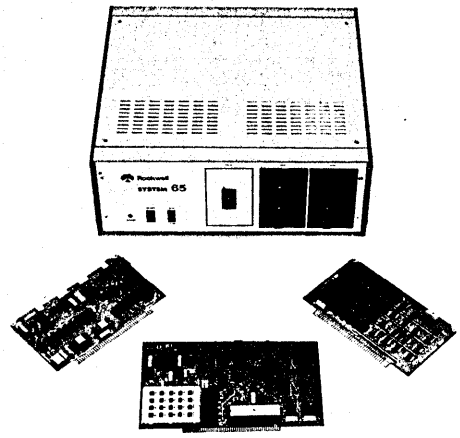
STANDARD MODELS

MM75	Has CPU, 640 x 8 ROM, 48 x 4 RAM, internal clock logic and 22 I/O lines. 28-pin dual in-line package.	A75XX (A7699)
MM78	Has CPU, 2048 x 8 ROM, 128 x 4 RAM, internal clock logic and 31 I/O lines. 42-pin quad in-line package.	A78XX (A7899)

LOW POWER/LOW VOLTAGE MODELS

MM76EL	Has CPU, 1024 x 8 ROM, 48 x 4 RAM, internal clock logic and 31 I/O lines. 40-pin dual in-line package.	B86XX (B8699)
MM78L	Same internal features as MM78. 40-pin dual in-line package.	B78XX (B7899)
M78LA	Has CPU, 2048 x 8 ROM, 128 x 4 RAM, internal clock logic and 35 I/O lines (including speaker and display I/O). 42-pin quad in-line package.	B90XX (B9099)

NOTE: PART NUMBERS IN BRACKETS ARE FOR PROTOTYPE DEVICES.



PPS-4/1 Personality Subsystem

For fast, complete development of programs for PPS-4/1 devices, Rockwell has developed a PPS-4/1 Personality Subsystem for use with our SYSTEM 65 Development System.

The PPS-4/1 Personality Subsystem serves as a cross-assembler for all PPS-4/1 devices. Similarly it enables in-circuit emulation. Debugging capability of the subsystem is total, including breakpoints, trace, up load/down load, register alter, program memory alter and single stepping. Full prototyping of the end-product's system and peripherals is also provided. This advanced development system, including SYSTEM 65, is priced well under $10,000.

Rockwell Services

Rockwell provides Applications Engineering assistance for all of its customers, usually at no cost. Designers' Courses are available. Rockwell is also ready to discuss designing your product's microelectronic system with its own resources. Module manufacturing is also available.

Rockwell PPS-4/1 One-Chip Microcomputers Give You More Because You Can Pick The Right Chip At The Right Price

Features/Models	MM75	MM78	MM76EL	MM78L	MM78LA
ROM (x 8)	640	2048	1024	2048	2048
RAM (x 4)	48	128	48	128	128
Speed (μs)	12.5	12.5	10.0	10.0	10.0
Total I/O Lines	22	31	31	31	35
Cond. Interrupt	1 + 1*	2	2	2	1*
Parallel Input	4	8	8	8	8
Parallel Output	—	—	—	—	14
Bidirectional Parallel	8	8	8	8	—
Discrete	9	10	10	10	10
Serial	—	3	3	3	—
Speaker	—	—	—	—	3
Programmable Logic Array (PLA)	16 x 8	—	16 x 8	—	32 x 14
Tone Generator Counter	—	—	—	—	8-bit
Package (In-Line)	28-pin dual	42-pin quad	40-pin dual	40-pin dual	42-pin quad
Power	**−15V @ 75 mw (typical)**		**−6.5 to −11V @ 15 mw (typical)**		

*Multiplexed

PART NUMBER
A75XX

Rockwell

PARALLEL PROCESSING SYSTEM (PPS) DATA SHEET

PPS-4/1 One-Chip Microcomputer Family

MM75

one-chip microcomputer system

INTRODUCTION

The Rockwell MM75 one-chip microcomputer is primarily designed to fit the lowest cost requirements of equipment designers. But in addition to cost advantage, it provides system functions not presently available in competitive microprocessors.

On a single LSI chip, the MM75 provides a complete 4-bit parallel microcomputer system – versatile Central Processing Unit (CPU), Instruction Decode, Program Save Register, Program Memory (ROM), Data Memory (RAM), Program Counter (P), Data Address Register (B), nine input/output discrete drivers/receivers, two 4-bit parallel input/output channels, one 4-bit parallel input channel, Interrupt and Control logic, and a self-contained Clock Generator circuit.

In addition to stand-alone system applications, the MM75 can be directly included in other multi-chip systems as a dedicated slave controller.

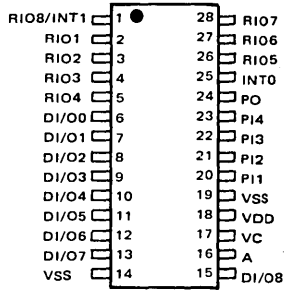
To facilitate system and program development, Rockwell provides powerful development aids listed under "Features" at right.

The MM75 is a member of the MM76 series of microcomputers. Consult the MM76 SERIES USER'S MANUAL for detailed hardware and software specifications (Document Number 29410N47). MM75 device codes may be submitted using the PMOS ROM CODE ORDER FORMS (Document Number 29000N33).

The MM75 may be ordered with combinations of the following features (not every combination is available).

Operating Temperature
- $0^{\circ}C$ to $+50^{\circ}C$ (Consumer)
- $0^{\circ}C$ to $+70^{\circ}C$ (Commercial)

Maximum Negative Voltage
- -30 Volts (Vacuum Fluorescent Drive)
- -15 Volts (Standard)



PPS-4/1 MM75 Pin Configuration

FEATURES

- 640 8-bit bytes of program memory (5120 bits)
- 48 4-bit data words (192 bits)
- 16 8-bit word decode matrix (128 bits)
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and four working registers
- 22 input/output ports
- Large instruction set – over 50 instructions
- Multifunction instructions increase throughput
- Single power supply operation (-15 volts ±5%)
- Low power (75 milliwatts typical, 125 milliwatts max)
- 28-pin, dual-in-line package
- Powerful development aids:
  - SYSTEM 65 with built in mini-floppy disks and PPS-4/1 Personality subsystem
  - XPO-1 Evaluation Microcomputer Module
  - Development Circuit (P/N A7699) provides address and/ device data lines so that the Program Memory can be in external PROM or RAM for emulating the MM75
  - Training Courses are available
  - International Applications Engineering Support

PPS-4/1 MICROCOMPUTER — MM75 SYSTEM

PPS-4 1
PMOS

Specifications subject to change without notice
Document No. 29000 D37
Rev. 4, May 1981

FUNCTIONAL DESCRIPTION

PROGRAM COUNTER (P) and SA REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory.

After PO reset, the program counter contains address Hex 1CO. This location must contain a NOP instruction.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides 640 8-bit words of storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

DATA ADDRESS REGISTER (B)

The Data Address Register is 6 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM and the discrete input/output ports are addressed by the 4 bits in BL and the 2 bits in BU.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

S REGISTER

The S Register is a 4-bit register which is used as a working register or an auxiliary storage register to the Accumulator. It can be used as a temporary storage register executing the XAS instruction.

ACCUMULATOR and ARITHMETIC LOGIC UNIT (A, ALU, and C)

The primary working register in the MM75 is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform either binary or decimal arithmetic. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel input or output data.

CLOCK CONTROL (VC, OSCILLATOR)

The internal Oscillator and Clock circuit generates a four-Phase clock signal used for all internal logic functions. The A clock term is also brought out so external logic can be synchronized. The clock frequency is a nominal 90 kHz ±40%.

An external clock mask option is available. If this option is chosen, the A clock becomes the external clock input and VC must be tied to VDD through the appropriate resistor.

DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 48 4-bit words. Data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc.

A BUFFER

The contents of the Accumulator or 4 of the bits from the 16 x 8 Decode Matrix may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or the Decode Matrix, or until the power is turned off.

B BUFFER

The 4-bit B Buffer functions the same as the A Buffer except it outputs the other 4 bits of the 16 x 8 Decode Matrix. The A and B Buffers combined provide the full eight outputs for the Decode Matrix.

CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port PI1 through PI4 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

CHANNEL A I/O PORTS (RI01 through RI04)

The four parallel input/output ports RI01 thru RI04 provide a masked input capability and an output from either the 16 x 8 Decode Matrix or directly from the Accumulator.

CHANNEL B I/O PORTS (RI05 through RI08)

The four parallel input/output ports of Channel B function the same as the four ports of Channel A. Together, they provide an 8-bit parallel output. RI08 also has the capability to be used as a conditional interrupt (INT1).

CONDITIONAL INTERRUPTS (INT0 and OPTIONAL INT1)

The conditional interrupts INT0 and RI08 (INT1) may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized with INT0 sampled at phase 3 and RI08 sampled at phase 1.

The conditional interrupts (edge detect) input lines in the PPS-4/1 family are very useful. The RI08 line can be used in two ways as part of the parallel I/O Channel B or as the INT1 line. When used as an interrupt line, RI08 will respond to the INT1H and DIN1 commands. When used as part of the bidirectional I/O Channel B, it is controlled with the IBM, OB and the SEG2 instructions.

DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O8)

There are nine discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

16 X 8 DECODE MATRIX

The Decode Matrix provides a means of decoding the contents of the Accumulator to provide an 8-bit output suitable for driving various displays or other external devices. The user may define any code desired. The Development device for the MM75 has a BCD to seven segment conversion provided. Accumulator contents of 0 thru F produce 0 thru 9, A, -, P, d, E and blank respectively. The carry flip-flop controls one independent output line.

PPS-4/1 MM75 INSTRUCTION SET

RAM Addressing Instructions

XAB	Exchange A with BL
LBA	Load BL from A
LB	Load BU=0, BL=Immediate
EOB	Exclusive OR BU
LBL	Load B Long
INCB	Increment B
DECB	Decrement B

Bit Manipulation Instructions

SB	Set Bit
RB	Reset Bit
SKBF	Skip on Bit False

Register to Register Instructions

XAS	Exchange A and S
LSA	Load S from A

Register Memory Instructions

L	Load A from Memory
X	Exchange A and Memory
XDSK	Exchange A with Memory. Decrement BL and Skip if BL Counts to 15
XNSK	Exchange A with Memory. Increment BL and Skip if BL Counts to 0

Arithmetic Instructions

A	Add Memory to A
AC	Add Memory with Carry to A
ACSK	Add Memory with Carry to A and Skip on No Carry-out
ASK	Add Memory to A and Skip on no Carry-out
DC	Decimal Correction
COM	Complement A
RC	Reset Carry
SC	Set Carry
SKNC	Skip on No Carry
LAI	Load A with Immediate Field
AISK	Add Immediate and Skip on No Carry-out

Logical Comparison Instructions

SKMEA	Skip if Memory Equals A
SKBEI	Skip if BL Equals Immediate Field
SKAEI	Skip if A Equals Immediate Field

Input/Output Instructions

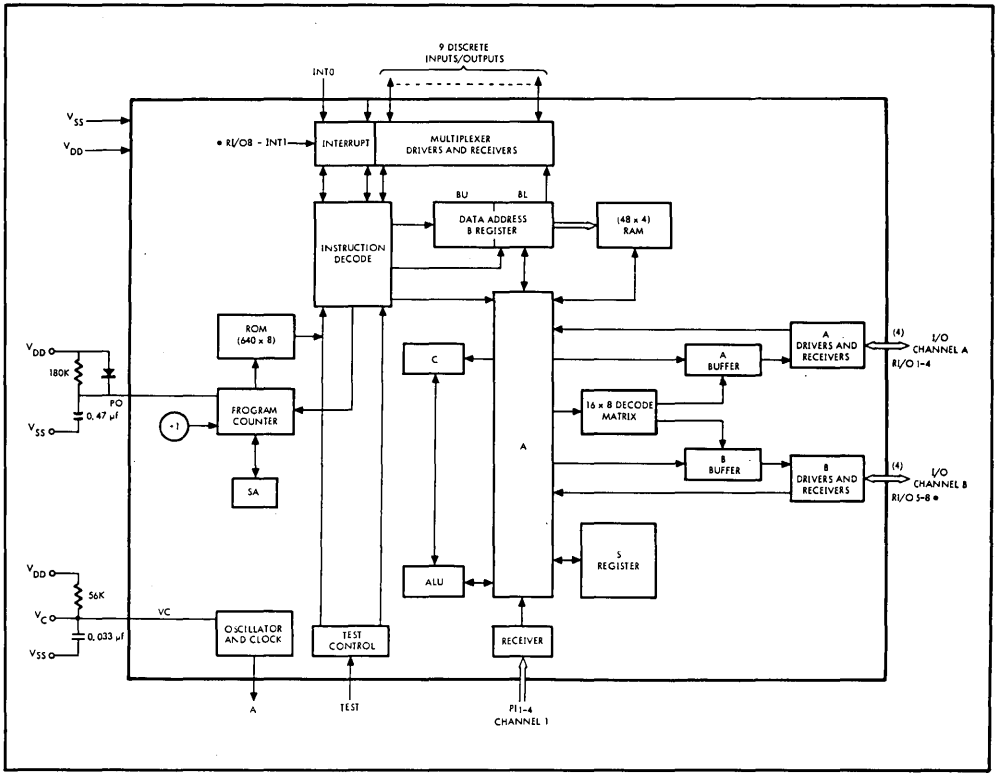
SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IBM	Input Channel B ANDed with A
OB	Output from A to Channel B
IAM	Input Channel A ANDed with A
OA	Output from A to Channel A
I1	Input Channel 1
INT1H	Skip if INT1 Input (RI08) is Low
DIN1	Skip if INT1 Flip-flop is Reset
INT0L	Skip if INT0 Input is High
DIN0	Skip if INT0 Flip-flop is Reset
SEG1	Decoder Matrix to Channel A
SEG2	Decoder Matrix to Channel B

Conditional Transfer Instructions

TC	Transfer on Carry Set
TNC	Transfer on No Carry Set
TLC	Transfer Long on Carry Set
TLNC	Transfer Long on No Carry Set
TBF	Transfer on Bit in Memory False
TBT	Transfer on Bit in Memory True
TLBF	Transfer Long on Bit in Memory False
TLBT	Transfer Long on Bit in Memory True
TE	Transfer on A = Memory
TNE	Transfer on A ≠ Memory
TLE	Transfer Long on A = Memory
TLNE	Transfer Long on A ≠ Memory
TIH	Transfer if Input High
TIL	Transfer if Input Low
TLIH	Transfer Long if Input High
TLIL	Transfer Long if Input Low

ROM Addressing Instructions

RT	Return from Subroutine
RTSK	Return and Skip
T	Transfer on Page
NOP	No Operation
TL	Transfer Long
TM	Transfer and Mark
TML	Transfer and Mark Long



PPS-4/1 MM75 System Block Diagram

SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:

VDD = -15 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)

VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies (Internal Clock):

90 kHz ±40% with external resistor

Max Operating Frequency (External Clock):

100 kHz

Device Power Consumption:

75 mw, typical

Input Capacitance:

< 5 pf

Input Leakage:

< 10 μa

Open Drain Driver Leakage (R OFF):

⩽ 10 μa at maximum voltage

Operating Ambient Temperature (TA):

0°C to 70°C (TA = 25°C unless otherwise specified.)

Storage Temperature:

-55°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts (vacuum fluorescent drive).

Maximum negative voltage on any pin -15 volts (standard).

Maximum positive voltage on any pin +0.3 volts.

INPUT/OUTPUT	SYMBOL	LIMITS (VSS = 0) MIN	TYP	MAX	LIMITS (VSS = +5V) MIN	TYP	MAX	TIMING (SAMPLE/ GOOD)	TEST CONDITIONS
Supply Current (Average) for VDD	IDD		5 ma	8 ma		5 ma	8 ma		VDD = -15.75V
Discrete I/O's (1)	V_{IH}	-1.0V			+4.0V			φ3-4	
DI/O 0-DI/O 8	V_{IL}			-4.2V			+0.8V		
DI/O 0-5	RON			500 ohms			500 ohms	φ4*	3.0 ma max.
DI/O 6-8	RON			400 ohms			400 ohms		
Channel 1 Input	V_{IH}	-1.5V			+3.5V			φ1	
PI1-PI4	V_{IL}			-4.2V			+0.8V		
I/O Channel A (1)	V_{IH}	-1.5V			+3.5V			φ3	
RI/O1-RI/O4	V_{IL}			-4.2V			+0.8V		
	RON			250 ohms			250 ohms	φ4*	6.0 ma max.
I/O Channel B (1)	V_{IH}	-1.5V			+3.5V			φ3	
RI/O5-RI/O8	V_{IL}			-4.2V			+0.8V		
	RON			250 ohms			250 ohms	φ4*	6.0 ma max.
INT0 (2)	V_{IH}	-1.5V			+3.5V			φ3	
	V_{IL}			-4.2V			+0.8V		
Clock	V_{OH}	-1.0V			+4.0V			-5.0V	CL = 50 pf (max)
A	V_{OL}			-10.0V			-5.0V		
VC									56K ±5%
PO	V_{IH}	-2.0V			+3.0V				Special circuit
	V_{IL}			-6.0V			-1.0V		

*State established by φ2 (minimum impedance during φ4).
(1)These pins only tested for leakage: <10 μa @ -30V.
(2)This pin only tested for leakage: <10 μa @ V_{DD}.

PART NUMBER
B86XX

Rockwell

PARALLEL PROCESSING SYSTEM (PPS) DATA SHEET

PPS-4/1 One-Chip Microcomputer Family

MM76EL

low-voltage, low power one-chip microcomputer system

SUMMARY

The Rockwell MM76EL microcomputer is a complete 4-bit parallel processing system. The MM76EL is a low voltage (6.5 to 11 volt range), very low power (15 milliwatts typical) version of the well known PPS-4/1 one-chip microcomputer. The MM76EL is especially desirable where low-cost battery operation as the primary or backup power source is required, or where power consumption or heat dissipation is a consideration, or where portability is required. The MM76EL is distinguished from competitive microprocessors by superior I/O capability, and by other functional features identified on this page.

On a single LSI chip, the MM76EL provides a complete system consisting of a versatile Central Processing Unit (CPU), Instruction Decode, one Program Save Register, Program Memory (ROM), Data Memory (RAM), Program Counter (P), Data Address Register (B), 10 I/O discrete Drivers/Receivers, two 4-bit parallel I/O channels, two 4-bit parallel input channels, a Serial I/O port, Interrupt and Control logic, and a self-contained four-phase Clock Generator circuit.

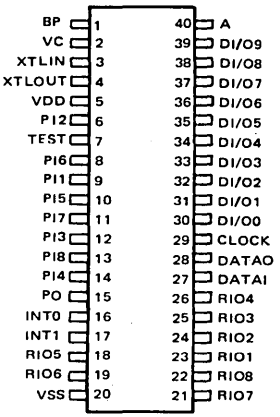
In addition to stand-alone applications, the MM76EL can be directly included in other multi-chip systems as a dedicated controller or in other functions. Also, two or more MM76EL microcomputers can be directly combined to perform parallel processing or control operations. In the design of families of end-products, a total range of features can be designed so that increasingly higher levels of performance can be produced by low-cost wiring changes and chip additions, minimizing design costs and production inventories.

The MM76EL may be ordered with combinations of the following features (not every combination is available).

Operating Temperature
- 0°C to +50°C (Consumer)
- 0°C to +70°C (Commercial)
- -40°C to +85°C (Industrial)

Maximum Negative Voltage
- -30 Volts (Vacuum Fluorescent Drive)
- -11 Volts (Standard)

Nominal Internal Clock Frequency
- 100 kHz (±30%) with VC to VDD



MM76EL Pin Configuration

ELECTRICAL FEATURES

- Battery Compatible (-6.5 to -11.0 volt operation)
- Low Power — 15 milliwatts nominal @ -8.5 volts
- 4 Clock Modes including external crystal
- Low Impedance Drivers
  - DI/O — less than 100 ohm @ 10 ma
  - RIO — less than 250 ohm @ 6 ma
- Mask Programmed Pull-down Resistors on Outputs
- Mask Programmed Enhancement FET Pull-downs on Inputs

FUNCTIONAL FEATURES

- Standard 40-pin Dual-In-Line (DIP) package
- 1024 8-bit bytes of program memory
- 48 4-bit words (192 bits) of data memory
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and four working registers
- 31 input/output ports
- Large instruction set — over 60 instructions
- Multifunction instructions increase throughput
- Single power supply operation (-8.5 volts -2.5, +2.0 volts)
- Low power (15 milliwatts typical)
- Powerful development aids:
  - SYSTEM 65 with built-in mini-floppy disks and PPS-4/1 Personality subsystem
  - XPO-1 Evaluation Microcomputer Module
  - Development Circuit (P/N B7699) provides address and data lines so that Program Memory can be in external PROM for emulation purposes
  - Scheduled and Special Training Courses
  - International Applications Engineering Support

Specifications subject to change without notice
Document No. 29000 D49
Rev. 3, February 1981

FUNCTIONAL DESCRIPTION

PROGRAM COUNTER (P) AND SA REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory. After PO reset, the program counter contains address hex 3C0. This location must contain a NOP instruction.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides 1024 bytes of storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

DATA ADDRESS REGISTER (B)

The Data Address Register is 6 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM and the discrete input/output ports are addressed by the 4 bits in BL and the 2 bits in BU.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

ACCUMULATOR AND ARITHMETIC LOGIC UNIT (A, ALU, and C)

The primary working register in the MM76EL is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform either binary or decimal arithmetic. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 48 4-bit words. Data memory can be used to buffer input or output values, hold intermediate results, or as a register for timers, counters, comparators, etc.

CLOCK CONTROL (VC, XTLIN, XTLOUT, A, AND BP)

The internal Oscillator and Clock Circuit generates a four-phase A and BP clock signal used for all internal logic functions. The A and BP clock terms are also brought out so external logic can be synchronized. The clock for the MM76EL can be selected to operate in one of four modes as shown by the table below. These options are selected by control voltages applied to the VC and XTLIN pins.

A BUFFER

The contents of the Accumulator or 4 of the bits from the 16 x 8 Decode Matrix may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or the Decode Matrix, or until the power is turned off.

B BUFFER

The 4-bit B Buffer functions the same as the A Buffer except it outputs the other 4 bits of the 16 x 8 Decode Matrix. The A and B Buffers combined provide the full eight outputs for the Decode Matrix.

CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port PI1 through PI4 will be loaded into the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

CHANNEL A I/O PORTS (RIO1 through RIO4)

The four parallel input/output ports RIO1 thru RIO4 provide a masked input capability and an output from either the 16 x 8 Decode Matrix or directly from the accumulator.

CHANNEL B I/O PORTS (RIO5 through RIO8)

The four parallel input/output ports of Channel B function the same as the four ports of Channel A. Together, they provide an 8-bit parallel output.

CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized.

DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

16 x 8 DECODE MATRIX

The Decode Matrix provides a means of decoding and contents of the Accumulator to provide an 8-bit output suitable for driving various displays or other external devices. The user may define any code desired. The Development Circuit version of the MM76EL has a BCD to seven segment conversion provided. Accumulator contents of 0 thru F produce 0 thru 9, A, –, P, d, E and blank respectively. The carry flip-flop controls one independent output line.

S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

Mode	V_C	Pins				Frequency
		XTLIN	XTLOUT	A I/O	BP I/O	
INTERNAL	*V_C	VSS	–	OUT	OUT	100 kHz ±30% @ 8.5V
EXTERNAL	GRD	CLOCK	–	OUT	OUT	400 – 800 kHz @ 8.0V
CRYSTAL**	GRD	XTAL	XTAL	OUT	OUT	≈ 800 kHz @ 8.0V
SLAVE	V_{DD}	V_{DD}	–	IN	IN	50 kHz – 100 kHz @ 8.5V

*Can be adjusted to vary frequency – Normally set to V_{DD}

**Suggest Murata part number CSB800A4 with 2-120 pF shunt capacitors.

PPS-4/1 MM76EL INSTRUCTION SET

RAM Addressing Instructions

XAB	Exchange A with BL
LBA	Load BL from A
LB	Load BU=0, BL=Immediate
EOB	Exclusive OR BU
LBL	Load B Long
INCB	Increment B
DECB	Decrement B

Bit Manipulation Instructions

SB	Set Bit
RB	Reset Bit
SKBF	Skip on Bit False

Register to Register Instructions

XAS	Exchange A and S
LSA	Load S from A

Register Memory Instructions

L	Load A from Memory
X	Exchange A and Memory
XDSK	Exchange A with Memory. Decrement BL and Skip if BL Counts to 15
XNSK	Exchange A with Memory.. Increment BL and Skip if BL Counts to 0

Arithmetic Instructions

A	Add Memory to A
AC	Add Memory with Carry to A
ACSK	Add Memory with Carry to A and Skip on No Carry-out
ASK	Add Memory to A and Skip if No Carry Overflow
DC	Decimal Correction
COM	Complement A
RC	Reset Carry
SC	Set Carry
SKNC	Skip on No Carry
LAI	Load A with Immediate Field
AISK	Add Immediate and Skip on No Carry-out

Logical Comparison Instructions

SKMEA	Skip if Memory Equals A
SKBEI	Skip if BL Equals Immediate Field
SKAEI	Skip if A Equals Immediate Field

Input/Output Instructions

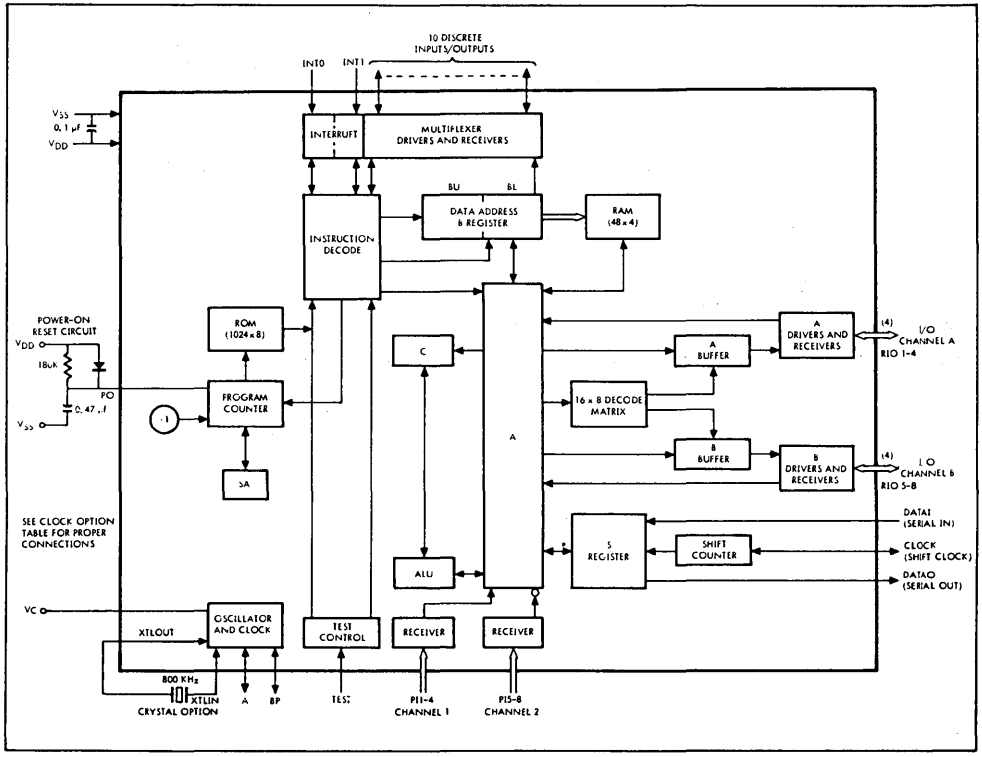
SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IBM	Input Channel B ANDed with A
OB	Output from A to Channel B
IAM	Input Channel A ANDed with A
OA	Output from A to Channel A
IOS	Serial Input/Output
I1	Input Channel 1
I2C	Input Channel 2 and Complement
INT1H	Skip if INT1 Input is Low
DIN1	Skip if INT1 Flip-flop is Reset
INT0L	Skip if INT0 Input is High
DIN0	Skip if INT0 Flip-flop is Reset
SEG1	Decoder Matrix Output to Channel A
SEG2	Decoder Matrix Output to Channel B

Conditional Transfer Instructions

TC	Transfer on Carry Set
TNC	Transfer on No Carry Set
TLC	Transfer Long on Carry Set
TLNC	Transfer Long on No Carry Set
TBF	Transfer on Bit in Memory False
TBT	Transfer on Bit in Memory True
TLBF	Transfer Long on Bit in Memory False
TLBT	Transfer Long on Bit in Memory True
TE	Transfer on A = Memory
TNE	Transfer on A ≠ Memory
TLE	Transfer Long on A = Memory
TLNE	Transfer Long on A ≠ Memory
TIH	Transfer if Input High
TIL	Transfer if Input Low
TLIH	Transfer Long if Input High
TLIL	Transfer Long if Input Low

ROM Addressing Instructions

RT	Return from Subroutine
RTSK	Return and Skip
T	Transfer on Page
NOP	No Operation
TL	Transfer Long
TM	Transfer and Mark
TML	Transfer and Mark Long



PPS-4/1 MM76EL System Block Diagram

SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:
V_{DD} = -8.5 Volts, -1.5, +2.0 Volts (MM76EL-1)
V_{DD} = -8.5 Volts, -2.5, +2.0 Volts (MM76EL)
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)
V_{SS} = 0 Volts (Gnd)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)
System Operating Frequencies:
(1) Internal: 100 kHz Nominal at V_{DD} = -8.5 V
(2) External 800 kHz Crystal: 100 kHz
Device Power Consumption: 15 mw, typical

Input Capacitance: <5 pf
Input Leakage: <10 μa
Open Drain Driver Leakage (R OFF): ≤10 μa at -30 Volts
Operating Ambient Temperature (T_A):
0°C to +70°C (Commercial): MM76EL
0°C to +50°C (Consumer): MM76EL-1
-40°C to +85°C (Industrial): MM76EL-2
Storage Temperature: -55°C to 125°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 Volts
Maximum positive voltage on any pin +0.3 Volts

TEST CONDITIONS: V_{DD} = -8.5V, T_A = 0-70°C

INPUT/OUTPUT	SYMBOL	LIMITS (VSS = 0) MIN	TYP	MAX	LIMITS (VSS = +5V)* MIN	TYP	MAX	TIMING (SAMPLE/ GOOD)	TEST CONDITIONS
Supply Current	IDD		1.75 ma	3 ma		1.75 ma	3 ma		Internal Clock
(Average) for VDD			3.0 ma	6 ma		3.0 ma	6 ma		Slave Clock
Discrete I/O's DI/O 0-9	V_{IH}	-1.0V			+4.0V			ϕ3, ϕ4	
	V_{IL}			-4.2V			+0.8V		
	RON			100 ohms			100 ohms	ϕ4*	10.0 ma max.
Channel 1 Input PI1-PI4	V_{IH}	-1.5V			+3.5V			ϕ1	
	V_{IL}			-4.2V			+0.8V		
Channel 2 Input PI5-PI8	V_{IH}	-1.5V			+3.5V			ϕ3	
	V_{IL}			-4.2V			+0.8V		
I/O Channel A RIO1-RIO4	V_{IH}	-1.5V			+3.5V			ϕ4	
	V_{IL}			-4.2V			+0.8V		
	RON			250 ohms			250 ohms	ϕ4*	6.0 ma max.
I/O Channel B RIO5-RIO8	V_{IH}	-1.5V			+3.5V			ϕ4	
	V_{IL}			-4.2V			+0.8V		
	RON			250 ohms			250 ohms	ϕ4*	6.0 ma max.
DATAI	V_{IH}	-1.0V			+4.0V			ϕ4	
	V_{IL}			-4.2V			+0.8V		
DATAO	RON			500 ohms			500 ohms	ϕ4**	3.0 ma max.
INT0	V_{IH}	-1.5V			+3.5V			ϕ3	
	V_{IL}			-4.2V			+0.8V		
INT1	V_{IH}	-1.5V			+3.5V			ϕ1	
	V_{IL}			-4.2V			+0.8V		
A, BP	V_{OH}	-0.3V			+4.7V				CL = 50 pf (max) Int, Ext or XTL Clock
	V_{OL}			-4.7V			+0.3V		
A, BP	V_{IH}	-0.6V			+4.4V				Slave Clock
	V_{IL}			-4.4V			+0.6V		
XTLIN	V_{IH}	-1.0V			+3.5V			-4.0V	
	V_{IL}			-6.0V			-1.0V		
CLOCK	V_{IH}	-1.0V			+4.0V			ϕ3, ϕ4	
	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4**	2.0 ma max.
VC	V_{IH}								V = 11.0V max.
	V_{IL}								
PO	V_{IH}	-2.5V			+2.5V				Special circuit
	V_{IL}			-5.0V			0V		

*State established by ϕ2 (minimum impedance during ϕ4).
**Same as above except ϕ4 minimum at ϕ2 of next cycle.

NOTES:

MASK PROGRAMMED PULL-DOWN RESISTORS ON OUTPUTS

Resistor pull-downs are available as an option on all RIO, CLOCK, DATAO and DI/O outputs. These pull-downs are connected to V_{DD}. The following values ±50% are available: 5K, 10K, 25K, or Open Circuit. The 5K ohm option is not available on the clock or DATAO outputs.

PULL-DOWNS ON INPUTS

MOS FET pull-downs are also available as an option on the PI, INT, and DATAI inputs. The output current is 50 μa ±35 μa with the input grounded and V_{DD} at -8.5 volts.

PART NUMBER
A78XX

Rockwell

PARALLEL PROCESSING SYSTEM (PPS) DATA SHEET

PPS-4/1 One-Chip Microcomputer Family

MM78

one-chip microcomputer system

SUMMARY

The Rockwell MM78 microcomputer is a complete, 4-bit parallel processing system. Its large instruction set is augmented by powerful multi-function instructions. 31 I/O ports further identify the power of this system. Serial I/O capability, which can be clocked simultaneously or externally controlled, extend their power.

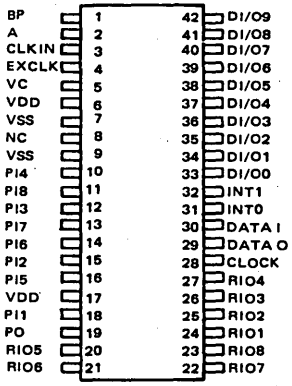
On a single LSI chip, the MM78 provides a complete 4-bit parallel processing system – Central Processing Unit (CPU), Program Memory (ROM), Data Memory (RAM), Program Counter (P), Instruction Decode, two Program Save registers, Data Address register (B), 10 I/O discrete drivers/receivers, two 4-bit parallel I/O channels, two 4-bit parallel input channels, a serial input/output port, interrupt and control logic, and a self-contained four-phase clock generator circuit.

In addition to stand-alone system applications, this microcomputer can be directly interfaced with other multi-chip systems as dedicated slave controllers or for other purposes. Also, two or more MM78 systems can be directly combined to perform parallel processing or control operations.

The MM78 may be ordered with combinations of the following features (not every combination is available).

Operating Temperature
- 0°C to +50°C (Consumer)
- 0°C to +70°C (Commercial)

Maximum Negative Voltage
- -30 Volts (Vacuum Fluorescent Drive)
- -15 Volts (Standard)



PPS–4/1 MM78 Pin Configuration

FEATURES

- 2048 8-bit bytes of program memory and 128 4-bit data words
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and six working registers
- Two-level subroutine nesting
- 31 input/output ports
- Easy circuit level testing by user
- Large instruction set – over 60 instructions
- Multifunction instructions increase throughput
- Single power supply operation (-15 volts ±5%)
- Low power (75 milliwatts typical, 125 milliwatts max)
- Powerful development aids:
  - SYSTEM 65 with built-in mini-floppy disks and PPS-4/1 Personality subsystem
  - XPO-1 Evaluation Microcomputer Module
  - Development Circuit (P/N A7899) provides address and data lines so that Program Memory can be in external PROM or RAM for emulation purposes
  - Scheduled and Special Training Courses
  - International Applications Engineering Support

Specifications subject to change without notice
Document No. 29000 D01
Rev. 6, May 1981

FUNCTIONAL DESCRIPTION

PROGRAM COUNTER (P), SA REGISTER, AND SB REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory. After PO reset, the program counter contains address hex 3C0. This location must contain a NOP instruction.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

The SB Register provides a second hardware stack register so that two levels of subroutines may be nested in the microcomputer.

PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides 2048 bytes of storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

DATA ADDRESS REGISTER (B)

The Data Address Register is 7 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM are addressed by all 7 bits and the discrete input/output ports are addressed by the 4 bits in BL when the value in BU is between 0 and 3.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

ACCUMULATOR AND ARITHMETIC LOGIC UNIT (A, ALU, AND C)

The Primary working register in the MM78 is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform binary arithmetic. By means of software routines, decimal arithmetic can be performed. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

A BUFFER

The contents of the Accumulator may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or until the power is turned off.

X BUFFER

The X Buffer comprises four latches which will output the last bit pattern loaded until either a new Output X Register command is executed or power is turned off.

X REGISTER

The X Register is an auxiliary register which may be used as temporary storage for 4 bits of data without reference to data memory. The X Register is also used as a data path to the X Buffer output register and from receiver inputs.

CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port P11 through P14 will be added to the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

CHANNEL A I/O PORTS (RI01 through RI04)

The contents of the Accumulator may be output for control or data transfer purposes through the A Buffer. The A Buffer will hold the data output until new data is output or power is turned off.

CHANNEL X I/O PORTS (R105 through R108)

The four parallel input/output ports of Channel X function as described in X Buffer and X Register paragraphs.

CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized with INT0 sampled at phase 3 and INT1 sampled at phase 1.

DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

CLOCK CONTROL (VC, CLKIN, EXCLK, AND OSCILLATOR)

The internal Oscillator and Clock circuit generates a four Phase A and $\overline{B}$ clock signal used for all internal logic functions. The A and $\overline{B}$ terms are also brought out so external logic can be synchronized. The clock frequency is a nominal 90 kHz ±40%. When precise timing is required, a reference frequency may be input at CLKIN.

DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 128 4-bit characters. Data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc., when the MM78 is used as a universal logic element.

S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S Register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

PPS-4/1 MM78 INSTRUCTION SET

RAM Addressing Instructions

XAB	Exchange A with BL
LBA	Load BL from A
LB	Load BL, BU → O
EOB	Exclusive OR BU
LBL	Load B Long
INCB	Increment B
DECB	Decrement B
SAG	Special Address Generation

Bit Manipulation Instructions

SB	Set Bit
RB	Reset Bit
SKBF	Skip on Bit False

Register to Register Instructions

LXA	Load X from A
XAS	Exchange A and S
XAX	Exchange A and X

Arithmetic Instructions

A	Add Memory to A
AC	Add Memory with Carry to A
ACSK	Add Memory with Carry to A and Skip on Carry-out
DC	Decimal Correction
COM	Complement A
RC	Reset Carry
SC	Set Carry
SKNC	Skip on No Carry
LAI	Load A with Immediate Field
AISK	Add Immediate and Skip on No Carry-out

ROM Addressing Instructions

RT	Return from Subroutine
RTSK	Return and Skip
T	Transfer on Page
NOP	No Operation
TL	Transfer Long
TLB	Transfer Long Banked
TM	Transfer and Mark
TML	Transfer and Mark Long
TMLB	Transfer and Mark Long Banked

Logical Comparison Instructions

SKMEA	Skip if Memory Equals A
SKBEI	Skip if BL Equals Immediate Field
SKAEI	Skip if A Equals Immediate Field
TAB	Table Look Up

Input/Output Instructions

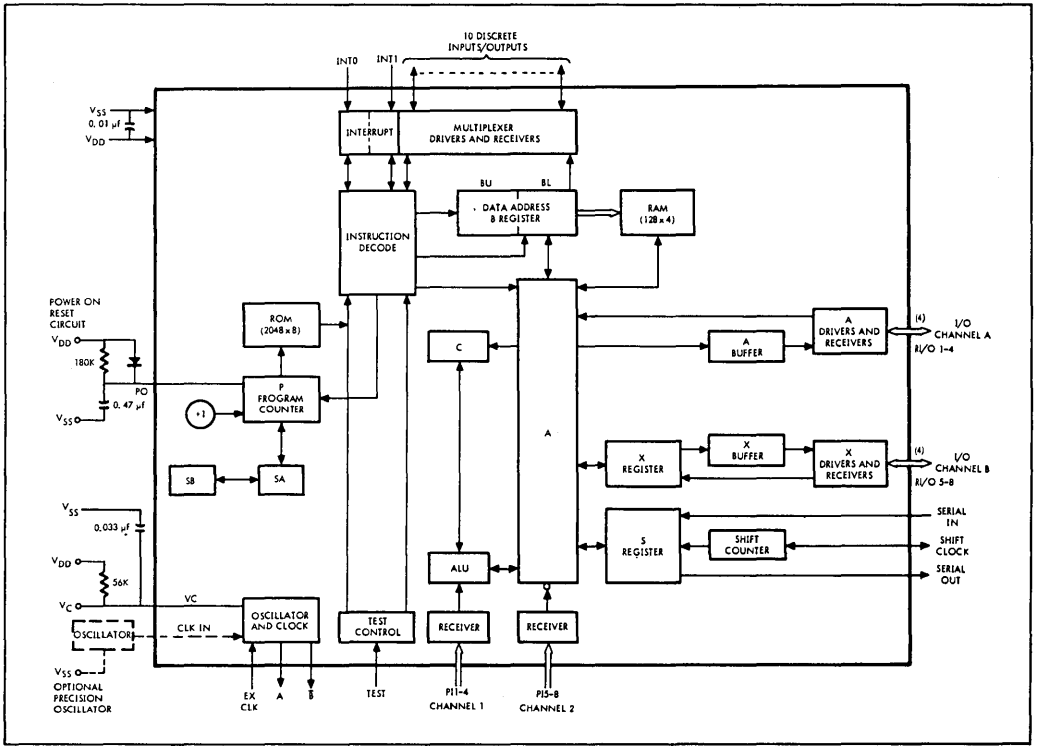
SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IX	Input X from RIO 5-8
OX	Output X to RIO 5-8
IOA	Input A Receivers to A and output A to RIO 1-4
IOS	Serial Input/Output
I1SK	Input Channel 1. Add to A, Skip if No Carry
I2C	Input Channel 2 and Complement
INT1L	Skip if INT1 Input is Low
INT0H	Skip if INT0 Input is High

Conditional Transfer Instructions

TC	Transfer on Carry Set
TNC	Transfer on No Carry Set
TLC	Transfer Long on Carry Set
TLNC	Transfer Long on No Carry Set
TBF	Transfer on Bit in Memory False
TBT	Transfer on Bit in Memory True
TLBF	Transfer Long on Bit in Memory False
TLBT	Transfer Long on Bit in Memory True
TE	Transfer on A = Memory
TNE	Transfer on A ≠ Memory
TLE	Transfer Long on A = Memory
TLNE	Transfer Long on A ≠ Memory
TIH	Transfer if Input High
TIL	Transfer if Input Low
TLIH	Transfer Long if Input High
TLIL	Transfer Long if Input Low

Register Memory Instructions

L	Load A from Memory
X	Exchange A and Memory
XDSK	Exchange A with Memory. Decrement BL and Skip if BL Counts to 15
XNSK	Exchange A with Memory. Increment BL and Skip if BL Counts to 0



PPS-4/1 MM78 System Block Diagram

SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage
V_{DD} = -15 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)
V_{SS} = 0 Volts (Gnd)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)
System Operating Frequencies:
90 kHz ±40% with external resistor
Device Power Consumption:
75 mw, typical
Input Capacitance:
<5 pf
Input Leakage:
<10 μa
Open Drain Driver Leakage (R OFF):
<10 μa at -30 Volts
Operating Ambient Temperature (T_A):
0°C to 70°C (Commercial)
0°C to 50°C (Consumer)
Storage Temperature:
-55°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 Volts
Maximum positive voltage on any pin +0.3 Volt

TEST CONDITIONS: V_{DD} = -15V ±5%, T_A = 0-70°C

FUNCTION	SYMBOL	LIMITS (VSS = 0) MIN	TYP	MAX	LIMITS (VSS = +5V) MIN	TYP	MAX	TIMING (SAMPLE/GOOD)	TEST CONDITIONS
Supply Current (Average) for VDD	IDD		5 ma	8 ma		5 ma	8 ma		
Discrete I/O's	V_{IH}	-1.0V			+4.0V			ϕ3	
DI/O 0-DI/O 9	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4*	3.0 ma max.
Channel 1 Input	V_{IH}	-1.5V			+3.5V			ϕ1	
PI1-PI4	V_{IL}			-4.2V			+0.8V		
Channel 2 Input	V_{IH}	-1.5V			+3.5V			ϕ3	
PI5-PI8	V_{IL}			-4.2V			+0.8V		
I/O Channel A	V_{IH}	-1.5V			+3.5V			ϕ3	
RI/O1-RI/O4	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4*	3.0 ma max.
I/O Channel X	V_{IH}	-1.0V			+4.0V			Not sync. Must be stable at ϕ1 and 2.	
RI/O5-RI/O8	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4*	3.0 ma max.
DATA I	V_{IH}	-1.0V			+4.0V			ϕ4	
	V_{IL}			-4.2V			+0.8V		
DATA O	RON							ϕ4**	
INT0	V_{IH}	-1.5V			+3.5V			ϕ3	
	V_{IL}			-4.2V			+0.8V		
INT1	V_{IH}	-1.5V			+3.5V			ϕ1	
	V_{IL}			-4.2V			+0.8V		
Clock	V_{OH}	-1.0V			+4.0V				CL = 50 pf (max.)
A, BP, ($\bar{B}$)	V_{OL}			-10.0V			-5.0V		
EXCLK	V_{IH}	-1.5V			+3.5V			STRAP	F max = 80 kHz
	V_{IL}			-7.0V			-2.0V		
CLK IN	V_{IH}	-1.0V			+4.0V				
	V_{IL}			-10.0V			-5.0V		
Shift Clock	V_{IH}	-1.0V			+4.0V			ϕ34	
Clock	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4**	2.0 ma max.
VC***	V_{IH}								56K ±5%
	V_{IL}								
PO	V_{IH}	-2.0V			+3.0V				Special circuit
	V_{IL}			-6.0V			-1.0V		

*State established by ϕ2 (minimum impedance during ϕ4).
**Same as above except ϕ4 minimum at ϕ2 of next cycle.
***Connect VC to VDD through a 56KΩ resistor for 90 kHz.

PART NUMBER
B86XX

Rockwell

PARALLEL PROCESSING SYSTEM (PPS) DATA SHEET

PPS-4/1 One-Chip Microcomputer Family

MM76EL

low-voltage, low power one-chip microcomputer system

SUMMARY

The Rockwell MM76EL microcomputer is a complete 4-bit parallel processing system. The MM76EL is a low voltage (6.5 to 11 volt range), very low power (15 milliwatts typical) version of the well known PPS-4/1 one-chip microcomputer. The MM76EL is especially desirable where low-cost battery operation as the primary or backup power source is required, or where power consumption or heat dissipation is a consideration, or where portability is required. The MM76EL is distinguished from competitive microprocessors by superior I/O capability, and by other functional features identified on this page.

On a single LSI chip, the MM76EL provides a complete system consisting of a versatile Central Processing Unit (CPU), Instruction Decode, one Program Save Register, Program Memory (ROM), Data Memory (RAM), Program Counter (P), Data Address Register (B), 10 I/O discrete Drivers/Receivers, two 4-bit parallel I/O channels, two 4-bit parallel input channels, a Serial I/O port, Interrupt and Control logic, and a self-contained four-phase Clock Generator circuit.

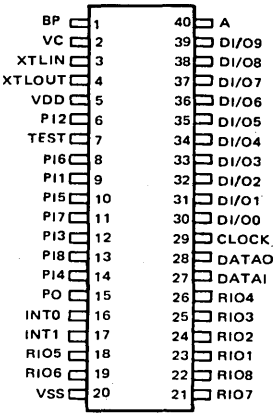
In addition to stand-alone applications, the MM76EL can be directly included in other multi-chip systems as a dedicated controller or in other functions. Also, two or more MM76EL microcomputers can be directly combined to perform parallel processing or control operations. In the design of families of end-products, a total range of features can be designed so that increasingly higher levels of performance can be produced by low-cost wiring changes and chip additions, minimizing design costs and production inventories.

The MM76EL may be ordered with combinations of the following features (not every combination is available).

Operating Temperature
- $0^{o}C$ to $+50^{o}C$ (Consumer)
- $0^{o}C$ to $+70^{o}C$ (Commercial)
- $-40^{o}C$ to $+85^{o}C$ (Industrial)

Maximum Negative Voltage
- -30 Volts (Vacuum Fluorescent Drive)
- -11 Volts (Standard)

Nominal Internal Clock Frequency
- 100 kHz (±30%) with VC to VDD



MM76EL Pin Configuration

ELECTRICAL FEATURES

- Battery Compatible (-6.5 to -11.0 volt operation)
- Low Power — 15 milliwatts nominal @ -8.5 volts
- 4 Clock Modes including external crystal
- Low Impedance Drivers
  - DI/O — less than 100 ohm @ 10 ma
  - RIO — less than 250 ohm @ 6 ma
- Mask Programmed Pull-down Resistors on Outputs
- Mask Programmed Enhancement FET Pull-downs on Inputs

FUNCTIONAL FEATURES

- Standard 40-pin Dual-In-Line (DIP) package
- 1024 8-bit bytes of program memory
- 48 4-bit words (192 bits) of data memory
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and four working registers
- 31 input/output ports
- Large instruction set — over 60 instructions
- Multifunction instructions increase throughput
- Single power supply operation (-8.5 volts -2.5, +2.0 volts)
- Low power (15 milliwatts typical)
- Powerful development aids:
  - SYSTEM 65 with built-in mini-floppy disks and PPS-4/1 Personality subsystem
  - XPO-1 Evaluation Microcomputer Module
  - Development Circuit (P/N B7699) provides address and data lines so that Program Memory can be in external PROM for emulation purposes
  - Scheduled and Special Training Courses
  - International Applications Engineering Support

Specifications subject to change without notice
Document No. 29000 D49
Rev. 3, February 1981

FUNCTIONAL DESCRIPTION

PROGRAM COUNTER (P) AND SA REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory. After PO reset, the program counter contains address hex 3C0. This location must contain a NOP instruction.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides 1024 bytes of storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

DATA ADDRESS REGISTER (B)

The Data Address Register is 6 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM and the discrete input/output ports are addressed by the 4 bits in BL and the 2 bits in BU.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

ACCUMULATOR AND ARITHMETIC LOGIC UNIT (A, ALU, and C)

The primary working register in the MM76EL is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform either binary or decimal arithmetic. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 48 4-bit words. Data memory can be used to buffer input or output values, hold intermediate results, or as a register for timers, counters, comparators, etc.

CLOCK CONTROL (VC, XTLIN, XTLOUT, A, AND BP)

The internal Oscillator and Clock Circuit generates a four-phase A and BP clock signal used for all internal logic functions. The A and BP clock terms are also brought out so external logic can be synchronized. The clock for the MM76EL can be selected to operate in one of four modes as shown by the table below. These options are selected by control voltages applied to the VC and XTLIN pins.

A BUFFER

The contents of the Accumulator or 4 of the bits from the 16 x 8 Decode Matrix may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or the Decode Matrix, or until the power is turned off.

B BUFFER

The 4-bit B Buffer functions the same as the A Buffer except it outputs the other 4 bits of the 16 x 8 Decode Matrix. The A and B Buffers combined provide the full eight outputs for the Decode Matrix.

CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port PI1 through PI4 will be loaded into the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

CHANNEL A I/O PORTS (RIO1 through RIO4)

The four parallel input/output ports RIO1 thru RIO4 provide a masked input capability and an output from either the 16 x 8 Decode Matrix or directly from the accumulator.

CHANNEL B I/O PORTS (RIO5 through RIO8)

The four parallel input/output ports of Channel B function the same as the four ports of Channel A. Together, they provide an 8-bit parallel output.

CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized.

DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

16 x 8 DECODE MATRIX

The Decode Matrix provides a means of decoding and contents of the Accumulator to provide an 8-bit output suitable for driving various displays or other external devices. The user may define any code desired. The Development Circuit version of the MM76EL has a BCD to seven segment conversion provided. Accumulator contents of O thru F produce 0 thru 9, A, –, P, d, E and blank respectively. The carry flip-flop controls one independent output line.

S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

Mode	V_C	Pins				Frequency
		XTLIN	XTLOUT	A I/O	BP I/O	
INTERNAL	*V_C	VSS	–	OUT	OUT	100 kHz ±30% @ 8.5V
EXTERNAL	GRD	CLOCK	–	OUT	OUT	400 – 800 kHz @ 8.0V
CRYSTAL**	GRD	XTAL	XTAL	OUT	OUT	≈ 800 kHz @ 8.0V
SLAVE	V_{DD}	V_{DD}	–	IN	IN	50 kHz – 100 kHz @ 8.5V

*Can be adjusted to vary frequency – Normally set to V_{DD}

**Suggest Murata part number CSB800A4 with 2-120 pF shunt capacitors.

PPS-4/1 MM76EL INSTRUCTION SET

RAM Addressing Instructions

XAB	Exchange A with BL
LBA	Load BL from A
LB	Load BU=0, BL=Immediate
EOB	Exclusive OR BU
LBL	Load B Long
INCB	Increment B
DECB	Decrement B

Bit Manipulation Instructions

SB	Set Bit
RB	Reset Bit
SKBF	Skip on Bit False

Register to Register Instructions

XAS	Exchange A and S
LSA	Load S from A

Register Memory Instructions

L	Load A from Memory
X	Exchange A and Memory
XDSK	Exchange A with Memory. Decrement BL and Skip if BL Counts to 15
XNSK	Exchange A with Memory.. Increment BL and Skip if BL Counts to 0

Arithmetic Instructions

A	Add Memory to A
AC	Add Memory with Carry to A
ACSK	Add Memory with Carry to A and Skip on No Carry-out
ASK	Add Memory to A and Skip if No Carry Overflow
DC	Decimal Correction
COM	Complement A
RC	Reset Carry
SC	Set Carry
SKNC	Skip on No Carry
LAI	Load A with Immediate Field
AISK	Add Immediate and Skip on No Carry-out

Logical Comparison Instructions

SKMEA	Skip if Memory Equals A
SKBEI	Skip if BL Equals Immediate Field
SKAEI	Skip if A Equals Immediate Field

Input/Output Instructions

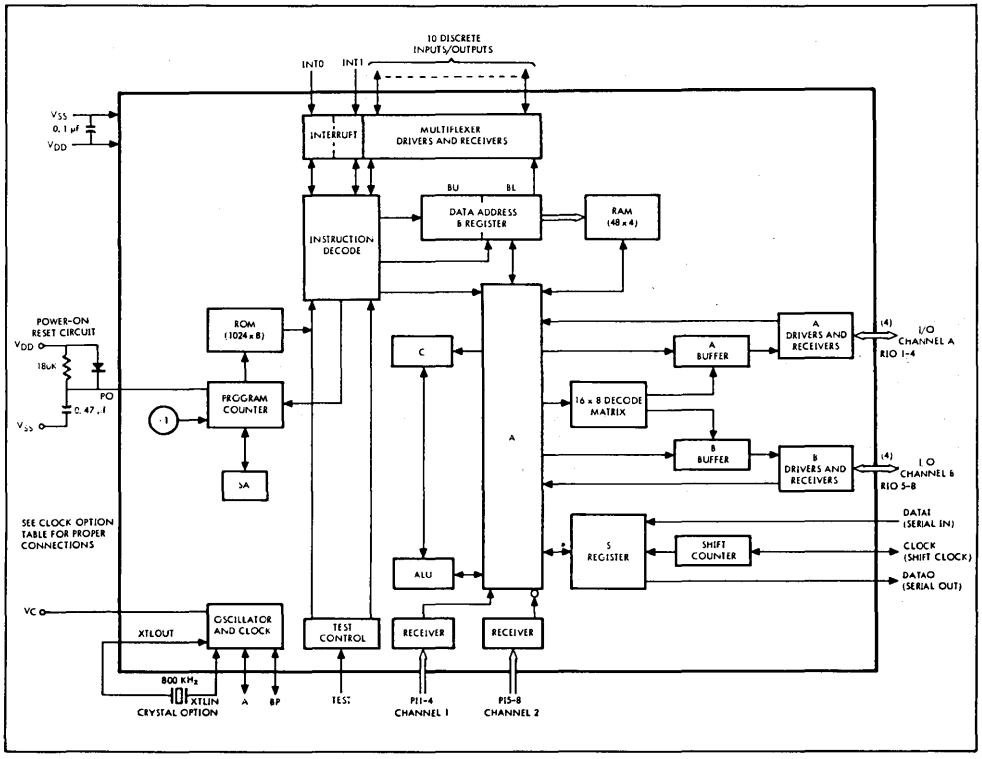
SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IBM	Input Channel B ANDed with A
OB	Output from A to Channel B
IAM	Input Channel A ANDed with A
OA	Output from A to Channel A
IOS	Serial Input/Output
I1	Input Channel 1
I2C	Input Channel 2 and Complement
INT1H	Skip if INT1 Input is Low
DIN1	Skip if INT1 Flip-flop is Reset
INT0L	Skip if INT0 Input is High
DIN0	Skip if INT0 Flip-flop is Reset
SEG1	Decoder Matrix Output to Channel A
SEG2	Decoder Matrix Output to Channel B

Conditional Transfer Instructions

TC	Transfer on Carry Set
TNC	Transfer on No Carry Set
TLC	Transfer Long on Carry Set
TLNC	Transfer Long on No Carry Set
TBF	Transfer on Bit in Memory False
TBT	Transfer on Bit in Memory True
TLBF	Transfer Long on Bit in Memory False
TLBT	Transfer Long on Bit in Memory True
TE	Transfer on A = Memory
TNE	Transfer on A ≠ Memory
TLE	Transfer Long on A = Memory
TLNE	Transfer Long on A ≠ Memory
TIH	Transfer if Input High
TIL	Transfer if Input Low
TLIH	Transfer Long if Input High
TLIL	Transfer Long if Input Low

ROM Addressing Instructions

RT	Return from Subroutine
RTSK	Return and Skip
T	Transfer on Page
NOP	No Operation
TL	Transfer Long
TM	Transfer and Mark
TML	Transfer and Mark Long



PPS-4/1 MM76EL System Block Diagram

SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:
- V_{DD} = -8.5 Volts, -1.5, +2.0 Volts (MM76EL-1)
- V_{DD} = -8.5 Volts, -2.5, +2.0 Volts (MM76EL)
- (Logic "1" = most negative voltage V_{IL} and V_{OL}.)
- V_{SS} = 0 Volts (Gnd)
- (Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies:
- (1) Internal: 100 kHz Nominal at V_{DD} = -8.5 V
- (2) External 800 kHz Crystal: 100 kHz

Device Power Consumption: 15 mw, typical

Input Capacitance: < 5 pf
Input Leakage: <10 μa
Open Drain Driver Leakage (R OFF): ⩽10 μa at -30 Volts
Operating Ambient Temperature (T_A):
- 0°C to +70°C (Commercial): MM76EL
- 0°C to +50°C (Consumer): MM76EL-1
- -40°C to +85°C (Industrial): MM76EL-2

Storage Temperature: -55°C to 125°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 Volts
Maximum positive voltage on any pin +0.3 Volts

TEST CONDITIONS: V_{DD} = -8.5V, T_A = 0-70°C

INPUT/OUTPUT	SYMBOL	LIMITS (VSS = 0) MIN	TYP	MAX	LIMITS (VSS = +5V)* MIN	TYP	MAX	TIMING (SAMPLE/ GOOD)	TEST CONDITIONS
Supply Current (Average) for VDD	IDD		1.75 ma 3.0 ma	3 ma 6 ma		1.75 ma 3.0 ma	3 ma 6 ma		Internal Clock Slave Clock
Discrete I/O's DI/O 0-9	V_{IH} V_{IL}	-1.0V		 -4.2V	+4.0V		 +0.8V	ϕ3, ϕ4	
	RON			100 ohms			100 ohms	ϕ4*	10.0 ms max.
Channel 1 Input PI1-PI4	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	ϕ1	
Channel 2 Input PI5-PI8	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	ϕ3	
I/O Channel A RIO1-RIO4	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	ϕ4	
	RON			250 ohms			250 ohms	ϕ4*	6.0 ms max.
I/O Channel B RIO5-RIO8	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	ϕ4	
	RON			250 ohms			250 ohms	ϕ4*	6.0 ms max.
DATAI	V_{IH} V_{IL}	-1.0V		 -4.2V	+4.0V		 +0.8V	ϕ4	
DATAO	RON			500 ohms			500 ohms	ϕ4**	3.0 ms max.
INT0	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	ϕ3	
INT1	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	ϕ1	
A, BP	V_{OH} V_{OL}	-0.3V		 -4.7V	+4.7V		 +0.3V		CL = 50 pf (max) Int, Ext or XTL Clock
A, BP	V_{IH} V_{IL}	-0.6V		 -4.4V	+4.4V		 +0.6V		Slave Clock
XTLIN	V_{IH} V_{IL}	-1.0V		 -6.0V	+3.5V		 -1.0V	-4.0V	
CLOCK	V_{IH} V_{IL}	-1.0V		- -4.2V	+4.0V		 +0.8V	ϕ3, ϕ4	
	RON			500 ohms			500 ohms	ϕ4**	2.0 ms max.
VC	V_{IH} V_{IL}								V = 11.0V max.
PO	V_{IH} V_{IL}	-2.5V		 -5.0V	+2.5V		 0V		Special circuit

*State established by ϕ2 (minimum impedance during ϕ4).
**Same as above except ϕ4 minimum at ϕ2 of next cycle.

NOTES:

MASK PROGRAMMED PULL-DOWN RESISTORS ON OUTPUTS

Resistor pull-downs are available as an option on all RIO, CLOCK, DATAO and DI/O outputs. These pull-downs are connected to V_{DD}. The following values ±50% are available: 5K, 10K, 25K, or Open Circuit. The 5K ohm option is not available on the clock or DATAO outputs.

PULL-DOWNS ON INPUTS

MOS FET pull-downs are also available as an option on the PI, INT, and DATAI inputs. The output current is 50 μa ±35 μa with the input grounded and V_{DD} at -8.5 volts.

PART NUMBER
A78XX

Rockwell

PARALLEL PROCESSING SYSTEM (PPS) DATA SHEET

PPS-4/1 One-Chip Microcomputer Family

MM78

one-chip microcomputer system

SUMMARY

The Rockwell MM78 microcomputer is a complete, 4-bit parallel processing system. Its large instruction set is augmented by powerful multi-function instructions. 31 I/O ports further identify the power of this system. Serial I/O capability, which can be clocked simultaneously or externally controlled, extend their power.

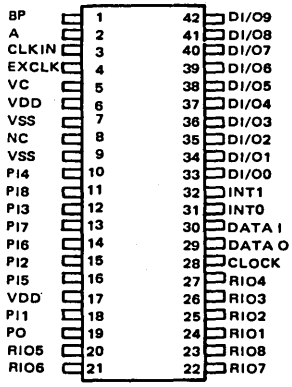
On a single LSI chip, the MM78 provides a complete 4-bit parallel processing system — Central Processing Unit (CPU), Program Memory (ROM), Data Memory (RAM), Program Counter (P), Instruction Decode, two Program Save registers, Data Address register (B), 10 I/O discrete drivers/receivers, two 4-bit parallel I/O channels, two 4-bit parallel input channels, a serial input/output port, interrupt and control logic, and a self-contained four-phase clock generator circuit.

In addition to stand-alone system applications, this microcomputer can be directly interfaced with other multi-chip systems as dedicated slave controllers or for other purposes. Also, two or more MM78 systems can be directly combined to perform parallel processing or control operations.

The MM78 may be ordered with combinations of the following features (not every combination is available).

Operating Temperature
- 0°C to +50°C (Consumer)
- 0°C to +70°C (Commercial)

Maximum Negative Voltage
- -30 Volts (Vacuum Fluorescent Drive)
- -15 Volts (Standard)



PPS—4/1 MM78 Pin Configuration

FEATURES

- 2048 8-bit bytes of program memory and 128 4-bit data words
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and six working registers
- Two-level subroutine nesting
- 31 input/output ports
- Easy circuit level testing by user
- Large instruction set — over 60 instructions
- Multifunction instructions increase throughput
- Single power supply operation (-15 volts ±5%)
- Low power (75 milliwatts typical, 125 milliwatts max)
- Powerful development aids:
  - SYSTEM 65 with built-in mini-floppy disks and PPS-4/1 Personality subsystem
  - XPO-1 Evaluation Microcomputer Module
  - Development Circuit (P/N A7899) provides address and data lines so that Program Memory can be in external PROM or RAM for emulation purposes
  - Scheduled and Special Training Courses
  - International Applications Engineering Support

Specifications subject to change without notice
Document No. 29000 D01
Rev. 6, May 1981

FUNCTIONAL DESCRIPTION

PROGRAM COUNTER (P), SA REGISTER, AND SB REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory. After PO reset, the program counter contains address hex 3C0. This location must contain a NOP instruction.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

The SB Register provides a second hardware stack register so that two levels of subroutines may be nested in the microcomputer.

PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides 2048 bytes of storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

DATA ADDRESS REGISTER (B)

The Data Address Register is 7 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM are addressed by all 7 bits and the discrete input/output ports are addressed by the 4 bits in BL when the value in BU is between 0 and 3.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

ACCUMULATOR AND ARITHMETIC LOGIC UNIT (A, ALU, AND C)

The Primary working register in the MM78 is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform binary arithmetic. By means of software routines, decimal arithmetic can be performed. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

A BUFFER

The contents of the Accumulator may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or until the power is turned off.

X BUFFER

The X Buffer comprises four latches which will output the last bit pattern loaded until either a new Output X Register command is executed or power is turned off.

X REGISTER

The X Register is an auxiliary register which may be used as temporary storage for 4 bits of data without reference to data memory. The X Register is also used as a data path to the X Buffer output register and from receiver inputs.

CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port P11 through P14 will be added to the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

CHANNEL A I/O PORTS (RI01 through RI04)

The contents of the Accumulator may be output for control or data transfer purposes through the A Buffer. The A Buffer will hold the data output until new data is output or power is turned off.

CHANNEL X I/O PORTS (R105 through R108)

The four parallel input/output ports of Channel X function as described in X Buffer and X Register paragraphs.

CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized with INT0 sampled at phase 3 and INT1 sampled at phase 1.

DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

CLOCK CONTROL (VC, CLKIN, EXCLK, AND OSCILLATOR)

The internal Oscillator and Clock circuit generates a four Phase A and $\overline{B}$ clock signal used for all internal logic functions. The A and $\overline{B}$ terms are also brought out so external logic can be synchronized. The clock frequency is a nominal 90 kHz ±40%. When precise timing is required, a reference frequency may be input at CLKIN.

DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 128 4-bit characters. Data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc., when the MM78 is used as a universal logic element.

S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S Register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

PPS-4/1 MM78 INSTRUCTION SET

RAM Addressing Instructions

XAB	Exchange A with BL
LBA	Load BL from A
LB	Load BL, BU → O
EOB	Exclusive OR BU
LBL	Load B Long
INCB	Increment B
DECB	Decrement B
SAG	Special Address Generation

Bit Manipulation Instructions

SB	Set Bit
RB	Reset Bit
SKBF	Skip on Bit False

Register to Register Instructions

LXA	Load X from A
XAS	Exchange A and S
XAX	Exchange A and X

Arithmetic Instructions

A	Add Memory to A
AC	Add Memory with Carry to A
ACSK	Add Memory with Carry to A and Skip on Carry-out
DC	Decimal Correction
COM	Complement A
RC	Reset Carry
SC	Set Carry
SKNC	Skip on No Carry
LAI	Load A with Immediate Field
AISK	Add Immediate and Skip on No Carry-out

ROM Addressing Instructions

RT	Return from Subroutine
RTSK	Return and Skip
T	Transfer on Page
NOP	No Operation
TL	Transfer Long
TLB	Transfer Long Banked
TM	Transfer and Mark
TML	Transfer and Mark Long
TMLB	Transfer and Mark Long Banked

Logical Comparison Instructions

SKMEA	Skip if Memory Equals A
SKBEI	Skip if BL Equals Immediate Field
SKAEI	Skip if A Equals Immediate Field
TAB	Table Look Up

Input/Output Instructions

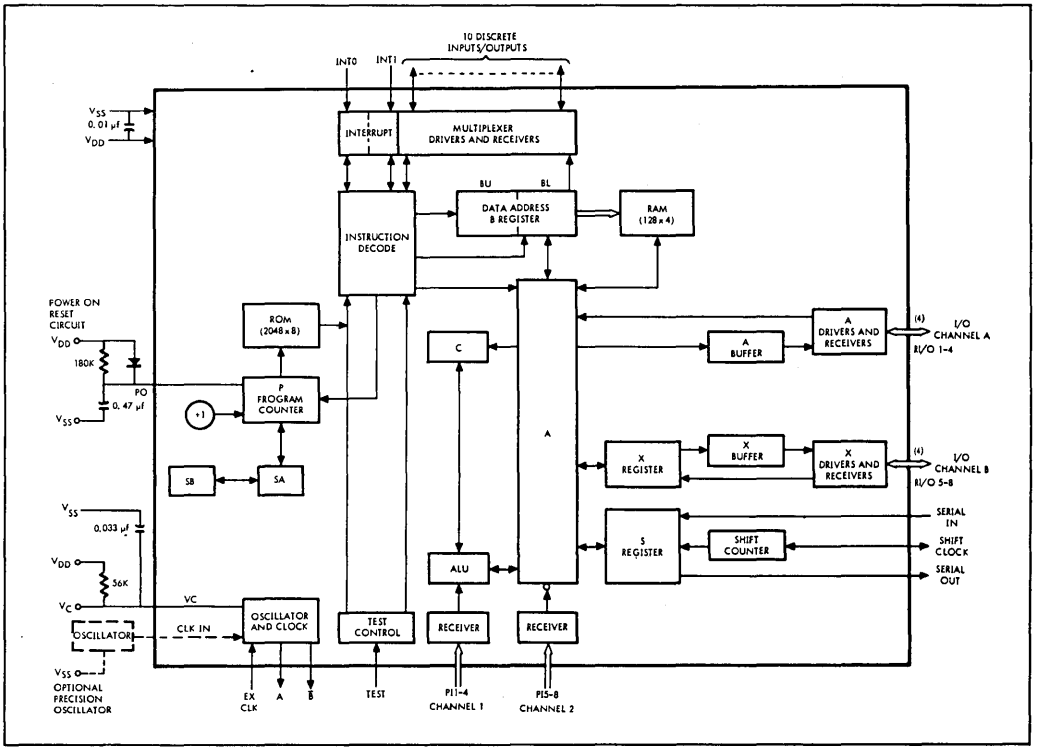
SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IX	Input X from RIO 5-8
OX	Output X to RIO 5-8
IOA	Input A Receivers to A and output A to RIO 1-4
IOS	Serial Input/Output
I1SK	Input Channel 1. Add to A, Skip if No Carry
I2C	Input Channel 2 and Complement
INT1L	Skip if INT1 Input is Low
INT0H	Skip if INT0 Input is High

Conditional Transfer Instructions

TC	Transfer on Carry Set
TNC	Transfer on No Carry Set
TLC	Transfer Long on Carry Set
TLNC	Transfer Long on No Carry Set
TBF	Transfer on Bit in Memory False
TBT	Transfer on Bit in Memory True
TLBF	Transfer Long on Bit in Memory False
TLBT	Transfer Long on Bit in Memory True
TE	Transfer on A = Memory
TNE	Transfer on A ≠ Memory
TLE	Transfer Long on A = Memory
TLNE	Transfer Long on A ≠ Memory
TIH	Transfer if Input High
TIL	Transfer if Input Low
TLIH	Transfer Long if Input High
TLIL	Transfer Long if Input Low

Register Memory Instructions

L	Load A from Memory
X	Exchange A and Memory
XDSK	Exchange A with Memory. Decrement BL and Skip if BL Counts to 15
XNSK	Exchange A with Memory. Increment BL and Skip if BL Counts to 0



PPS-4/1 MM78 System Block Diagram

SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage
V_{DD} = -15 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)
V_{SS} = 0 Volts (Gnd)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)
System Operating Frequencies:
90 kHz ±40% with external resistor
Device Power Consumption:
75 mw, typical
Input Capacitance:
<5 pf
Input Leakage:
<10 μa
Open Drain Driver Leakage (R OFF):
<10 μa at -30 Volts
Operating Ambient Temperature (T_A):
0°C to 70°C (Commercial)
0°C to 50°C (Consumer)
Storage Temperature:
-55°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 Volts
Maximum positive voltage on any pin +0.3 Volt

TEST CONDITIONS: V_{DD} = -15V ±5%, T_A = 0-70°C

FUNCTION	SYMBOL	LIMITS (VSS = 0) MIN	TYP	MAX	LIMITS (VSS = +5V) MIN	TYP	MAX	TIMING (SAMPLE/ GOOD)	TEST CONDITIONS
Supply Current (Average) for VDD	IDD		5 ma	8 ma		5 ma	8 ma		
Discrete I/O's	V_{IH}	-1.0V			+4.0V			ϕ3	
DI/O 0-DI/O 9	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4*	3.0 ma max.
Channel 1 Input	V_{IH}	-1.5V			+3.5V			ϕ1	
PI1-PI4	V_{IL}			-4.2V			+0.8V		
Channel 2 Input	V_{IH}	-1.5V			+3.5V			ϕ3	
PI5-PI8	V_{IL}			-4.2V			+0.8V		
I/O Channel A	V_{IH}	-1.5V			+3.5V			ϕ3	
RI/O1-RI/O4	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4*	3.0 ma max.
I/O Channel X	V_{IH}	-1.0V			+4.0V			Not sync. Must be stable at ϕ1 and 2.	
RI/O5-RI/O8	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4*	3.0 ma max.
DATA I	V_{IH}	-1.0V			+4.0V			ϕ4	
	V_{IL}			-4.2V			+0.8V		
DATA O	RON							ϕ4**	
INT0	V_{IH}	-1.5V			+3.5V			ϕ3	
	V_{IL}			-4.2V			+0.8V		
INT1	V_{IH}	-1.5V			+3.5V			ϕ1	
	V_{IL}			-4.2V			+0.8V		
Clock	V_{OH}	-1.0V			+4.0V				CL = 50 pf (max.)
A, BP, ($\bar{B}$)	V_{OL}			-10.0V			-5.0V		
EXCLK	V_{IH}	-1.5V			+3.5V			STRAP	F max = 80 kHz
	V_{IL}			-7.0V			-2.0V		
CLK IN	V_{IH}	-1.0V			+4.0V				
	V_{IL}			-10.0V			-5.0V		
Shift Clock	V_{IH}	-1.0V			+4.0V			ϕ34	
Clock	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4**	2.0 ma max.
VC***	V_{IH}								56K ±5%
	V_{IL}								
PO	V_{IH}	-2.0V			+3.0V				Special circuit
	V_{IL}			-6.0V			-1.0V		

*State established by ϕ2 (minimum impedance during ϕ4).
**Same as above except ϕ4 minimum at ϕ2 of next cycle.
***Connect VC to VDD through a 56KΩ resistor for 90 kHz.

DOCUMENT NO. 29410 N21
NOVEMBER 1977

Rockwell

PARALLEL PROCESSING SYSTEM (PPS)
APPLICATION NOTE

SERIAL COMMUNICATIONS PROTOCOL FOR MULTIPLE PPS-4/1 SYSTEMS

A simple communications protocol can be implemented between two PPS-4/1 microprocessors using only five interface lines. In order to prevent both units from attempting to transmit simultaneously, one processor must be designated as the Master and the other as the Slave. The Master initiates all communication. The Slave responds to commands and inquiries from the Master.

COMMUNICATIONS BUS

The Communications Bus consists of the Serial Channel lines — Serial Data Out (DATAO), Serial Data In (DATAI) and CLOCK — and two bi-directional handshake lines (DI/O). One of the handshake lines will be used to transmit the Data Ready control signal (DR), the other will be used to transmit the Xmit Acknowledge control signal (XA). The connection of these lines is shown in the Serial Communication Block Diagram.

The normal (inactive) state of the handshake lines is low (driver off), which results in a "wired-OR" arrangement that allows either processor to "raise" the line by turning on its output driver.

COMMUNICATIONS PHASES

Communications are normally conducted in two phases. During the Command Transmission Phase, the Master transmits a command or inquiry to the Slave. During the Data Transmission Phase, the Slave responds by transmitting one or more data words. The general sequence of events for each phase is described in the text to follow, and illustrated by the accompanying timing diagram.

Command Transmission Phase

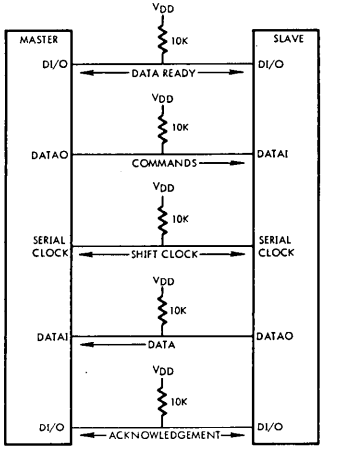
The sequence is:

1. Both handshake lines are low, indicating a "clear to send" condition.
2. Master transmits the command code to Slave via the Serial Channel. Eight cycles are needed to transmit four bits.
3. Master raises DR.
4. Slave senses DR high, saves command in RAM buffer and raises XA.
5. Master senses XA high, and drops DR.
6. Slave senses DR low, and drops XA.
7. Slave decodes command and performs required function.

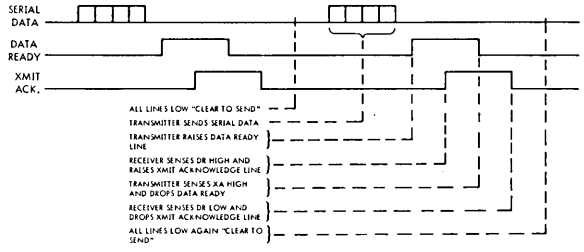
Data Transmission Phase

The sequence is:

1. Both handshake lines are low, indicating a "clear to send" condition.
2. Slave transmits data to Master via the Serial Channel. Eight cycles are needed to transmit four bits.
3. Slave raises DR.
4. Master senses DR high, saves data in RAM buffer and raises XA.
5. Slave senses XA high, and drops DR.
6. Master senses DR low, and drops XA.
7. Slave senses XA low, and steps 2 through 6 are repeated for the required number of data words, including a four-bit checksum value. In the event of a checksum error, Master will transmit a new command and the entire process will be repeated.



PPS-4/1 SERIAL COMMUNICATION BLOCK DIAGRAM



SERIAL DATA HANDSHAKE TIMING DIAGRAM

Rockwell Microelectronic Devices
P. O. Box 3669
Anaheim, Calif. 92803

DOCUMENT NO. 29410 N24
JULY 1979

Rockwell

PARALLEL PROCESSING SYSTEM (PPS)
APPLICATION NOTE

Using PPS-4/1 to Operate a Liquid Crystal Display

PURPOSE

This application note illustrates the use of a PPS-4/1 one-chip microcomputer to operate a liquid crystal display that is driven by a Hughes HLCD 0438 device. Although an MM78L is used as the microcomputer in the example interface, the material in this note can be easily adapted to the MM77, MM77L or MM78.

DESCRIPTION

Segment data from the display are loaded into the driver from the MM78L serial output port, as shown in Figure 1. Because the PPS-4/1 is a PMOS circuit and the HLCD is a CMOS circuit, VSS of the MM78L and VDD of the HLCD are connected to ground, and VDD of the MM78L and the ground pin of the HLCD are connected to -8.5V. For this example, DIO6 of the MM78L drives the HLCD load line and the HLCD internal oscillator is used to generate the AC frequency for the LCD wave forms.

Here is how the display is updated: New segment data are stored in the MM78L RAM. The data are then transferred to the HLCD shift register through the MM78L serial output port. Finally, the HLCD load line is pulsed by DIO6 to transfer the data to the HLCD latches and implement the new display pattern. Figures 2 and 3 show the flowchart and the PPS-4/1 coding for this procedure.

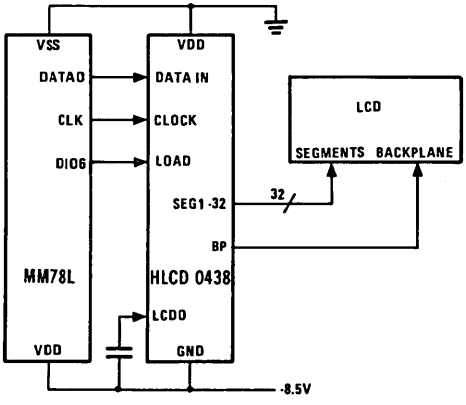


Figure 1. INTERFACE BLOCK DIAGRAM

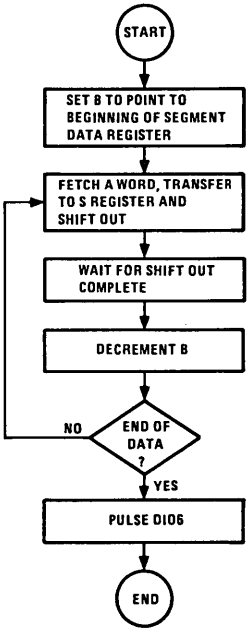
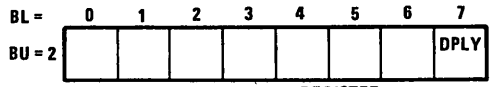


Figure 2. DRIVER FLOWCHART



SEGMENT DATA REGISTER

```
LLINE   EQU     6
DPLY    EQU     #27
        .
        .
        .
DISP    LBL     DPLY    POINT TO SEGMENT DATA REGISTER
DISP1   L               FETCH DATA
        XAS             TRANSFER TO SERIAL REGISTER
        IOS             OUTPUT
        NOP
        NOP             WAIT FOR SHIFT OUT
        NOP             COMPLETE
        NOP
        NOP
        DECB
        T       DISP1   REPEAT FOR REMAINDER OF DATA
        LB      LLINE
        SOS
        NOP
        ROS
        .
        .
        .
```

Figure 3. DISPLAY DRIVER

INTEGRAL MODEMS

PART NUMBER
R24

Rockwell

MODEM PRODUCTS DATA SHEET

R24 2400 BPS INTEGRAL MODEM

INTRODUCTION

The Rockwell R24 is a high performance synchronous serial 2400 bps DPSK modem. Utilizing extensive MOS/LSI technology, the R24 is implemented in three modular building blocks. It is innovatively designed to enable its economic integration by system designers in a broad range of communication, computer, and control equipment.

Having Bell 201 B/C and CCITT V.26 compatibility, the modular R24 offers the user sufficient flexibility to customize a 2400 bps modem to his specific packaging and functional requirements. With a minimum amount of interface circuitry, the modem can be configured for operation on leased lines or on the general switched network.

MODULE VERSATILITY

The versatility of the R24 design is achieved by dividing the modem's functions into three modules:

Transmitter — Module T
Receiver — Modules R1, R2

Each module can be plugged into standard connectors or can be wave soldered on one or more printed circuit boards. The pin spacing is on 100 mil centers. Modem modules are functionally independent.

MODEM OPERATION MODES

In general, the modules can be configured to operate in the following modes:

Simplex — Transmit only: Only the transmitter module (T) is used.

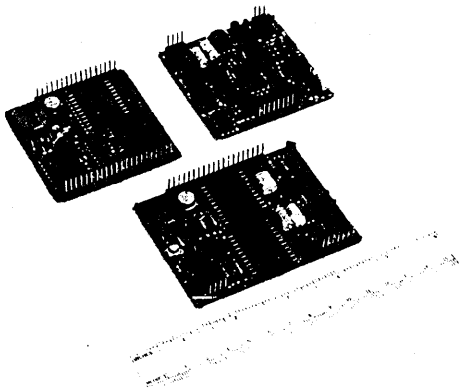
Simplex — Receive only: R1 and R2 modules are used to implement a complete receiver function.

Half Duplex (2-Wire): Requires both transmit and receive functions (although not simultaneously), therefore, all three modules are used.

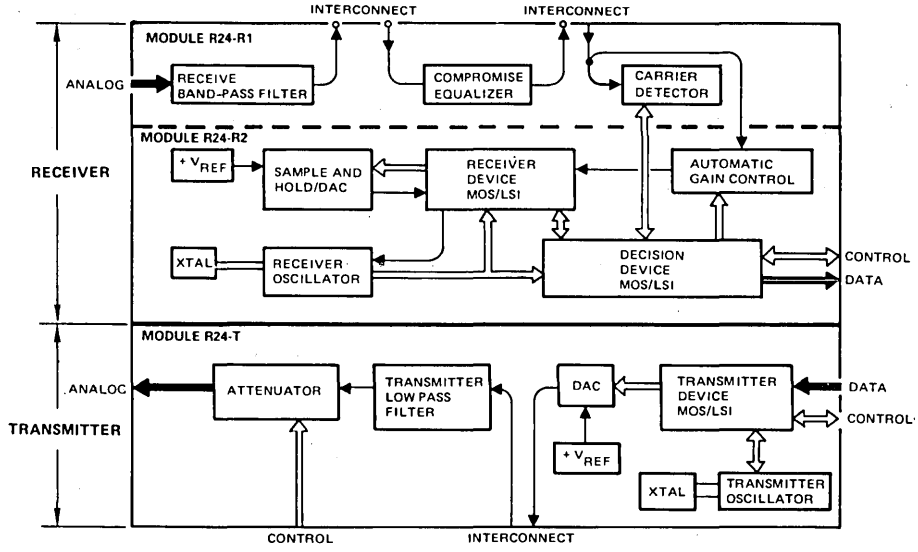
Full Duplex (4-Wire): Requires both transmit and receive functions simultaneously, again all three modules are used.

FEATURES/BENEFITS

- LSI high density; low power
- 2400/1200 bps modes
- Transmitter-Differential phase modulation
- Receiver-Coherent phase detection
- Bell 201 B/C, CCITT V.26 compatible
- CCITT A/B encoding options
- Operating modes:
  - Half duplex (2 wire)
  - Full duplex (4 wire)
  - Simplex (Transmit or Receive only)
- Outstanding performance over unconditioned lines
- LSTTL/CMOS compatible digital interface
- Fixed compromise equalizer
- V.27 compatible scrambler/descrambler
- Answer-back tone generation
- Clear-to-send delay options
- New sync option provides rapid resynchronization
- Typical power consumption 2 watts
- Total module area 25 sq. in.
- R24 Modem Evaluation Board facilitates evaluation and design-in tasks.



Specifications subject to change without notice
Document No. MD01
Rev. 2, March 1981



R24 Functional Diagram

TECHNICAL DESCRIPTION

Transmitter carrier frequency ..... 1800 Hz ±0.01%

Echo suppression and answer tone frequencies — 2100 Hz ±0.01% or 2025 Hz ±0.01%

Received signal frequency tolerance — The receiver can adapt to received frequency errors up to ±10 Hz with less than a 0.5 dB degradation in bit error rate.

Data signaling and modulation rate:

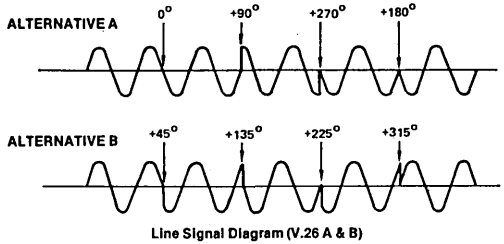
1) Normal: Signaling Rate — 1200 baud ±0.01%.
   Data Rate — 2400 bps ±0.01%
2) Fallback: Signaling Rate — 1200 baud ±0.01%.
   Data Rate — 1200 bps ±0.01%.

Transmitted Data Spectrum — The transmitted spectrum's bandwidth extends from 800 Hz to 2800 Hz. Phase distortion characteristics are within the limits specified in CCITT Recommendation V.26 bis. The out of band signal power limitations meet those specified by Part 68 or Tariff 261 of the FCC's regulations, and typically exceed the requirements of international regulatory bodies as well.

Data Encoding (DPSK) — At 2400 bps, differential four-phase modulation is used. The data stream is transmitted in pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the preceding signal element.

The R24 implements the phase A and B recommendations of CCITT V.26. The modulation coding in Bell 201 modems is the same as V.26B. Definition of these coding arrangements is shown in the following table:

2400 BPS		
DIBIT	PHASE CHANGE	
	V.26A	V.26B/Bell 201
0 0	0°	+45°
0 1	+90°	+135°
1 1	+180°	+225°
1 0	+270°	+315°



Line Signal Diagram (V.26 A & B)

At 1200 bps, differential two-phase modulation is used. Each bit is transmitted at a relative phase change to preceding signal element in accordance with CCITT V.26 bis.

1200 BPS	
BIT	PHASE CHANGE
0	+90°
1	+270°

Turn On Sequences — A total of twelve selectable turn on sequences can be generated by the transmitter module.

Turn Off Sequence — When the transmitter has been sending data and "Request to Send" is turned off, any remaining data bit information is transmitted within 6 milliseconds.

Ready for Sending (T106) Response Times — These response times are determined by the modem configuration selected and its associated turn on sequence.

Turn On Sequence Number	Ready for Sending Response Time	Configuration and Carrier Type
1	6.67 msec	Switched Carrier – 4-Wire (Bell 201)
2	8.33 msec	Switched Carrier – 4-Wire
3	30 msec	CCITT – 4-Wire
4	30 msec	CCITT – 4-Wire with Scrambler
5	90 msec	CCITT – 2-Wire
6	90 msec	CCITT – 2-Wire with Scrambler
7	148.3 msec	Switched Carrier – 2-Wire
8	148.3 msec	Switched Carrier – 2-Wire with Scrambler
9	220 msec	CCITT – 2-Wire Echo Protection
10	220 msec	Switched 2-Wire Echo Protection with Scrambler
11	800 msec	CCITT – 2-Wire Auto Call
12	800 msec	CCITT – 2-Wire Auto Call with Scrambler
Response Time tolerance (+0.9, -0.1) msec		

Scrambler/Descrambler — As a selectable option, the scrambler/descrambler may be inserted into the transmitter/receiver path. The purpose of this scrambler is to ensure that the line signal will evenly span the allocated bandwidth. This minimizes pattern sensitivity problems arising from simple fixed and periodic data sequences. The scrambler is V.27 or V.27 bis/ter compatible.

Carrier Detect (T109) — The modem receiver incorporates a line signal energy detector whose output responds to three selectable threshhold levels.

Set 1 (V.26 bis, switched network) — Greater than -43 dBm = ON
Less than -48 dBm = OFF

Set 2 (V.26 bis, switched network) — Greater than -33 dBm = ON
Less than -38 dBm = OFF

Set 3 (V.26, leased line) — Greater than -26 dBm = ON
Less than -31 dBm = OFF

NOTE: A minimum hysteresis of 2db exists between the actual turn-on and turn-off transition levels for each threshhold set.

Selectable T109 Response Times — This time is defined as the interval between the sudden connection or removal of the received line signal to the modems receive filter, and the subsequent transition of Carrier Detect (T109) from one state to the other.

Carrier Detect Transition	Response Time
OFF to ON (connection)	6 ±1 ms / 14 ±1 ms } Selectable
ON to OFF (removal)	8 ±3 ms / 22 ±3 ms } Selectable

Receive Level — The modem receives line signals from 0 to -43 dBm.

Transmit Timing — The modem generates a Transmit Clock (T114) having the following characteristics: Frequency — 2400 Hz ±.01% (1200 Hz ±.01% in fallback mode), duty cycle — 50 ±1%. The modem is also optionally capable of tracking an External Transmit Clock (T113) supplied by the modem user. T113 has similar characteristics to T114.

Receive Timing (T115) — The modem provides a data derived "Receive Clock" output in the form of a nominal squarewave (50 ±1% duty cycle). The modem timing recovery function is capable of tracking a ±0.01% frequency error in the associated transmit timing source.

Transmitter Output Levels — This output can be strap controlled in 2 ±0.2 dB steps from -1 dBm ± 1 dB to -15 dBm ± 1dB.

Answer Tone Generation — The modem generates a selectable answering tone of 2100 Hz ±0.01% or 2025 Hz ±0.01%. The 2100 Hz tone meets CCITT Recommendations G.161 and V.25, and the 2025 Hz tone meets Bell System requirements for both answering tone and echo suppressor disabling tone.

Equalizer — As a strap option, the modem contains a fixed compromise delay equalizer which can be used to improve performance over unconditioned schedule 3002 lines. This option is normally positioned in the receiver, but it can be repositioned in the transmitter or bypassed entirely. It is designed to compensate for the mean of the range of group delay distortions generally encountered in the United States. Its amplitude response is nominally flat at 0.0 dB.

Test Pattern Generation—The scrambler/descrambler function can be used to implement a 127-bit test pattern feature. For example, a constant mark input could be scrambled and transmitted as a pseudo-random signal to be descrambled at the receiver back to the constant mark. A transmission error would be represented as a space for the duration of an incorrect bit.

Multipoll Synchronization — The "new sync" (NSYNC) digital input can be pulsed to cause rapid resynchronization of the receiver for sequences of incoming messages. This feature is necessary in some polling applications. However, if the user's hardware/software does not support the use of "new sync" (NSYNC), then the optional "fast sync" (FSYNC) can be utilized to enable a fast resynchronization procedure.

Selectable Clamping Options —

1) Received Data (T104) — This output is clamped to a selectable constant (space or mark) when "Carrier Detect" is off, to prevent disturbances on the line from getting through the receiver to the data output.

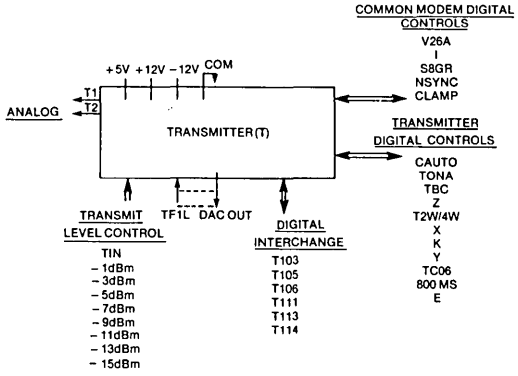
2) Carrier Detect (T109) Clamp — This output may be clamped OFF (squelched) in 2-wire applications during the time when "Request to Send" (T105) is on. An additional option extends this clamp for 148 msec beyond T105 transitioning off, providing echo protection.

3) Receive Clock (T115) — This clock output can be clamped OFF when "Carrier Detect" is off, thereby preventing any disturbances from propagating through the receiver to the receive clock output.

SYSTEM DESIGN

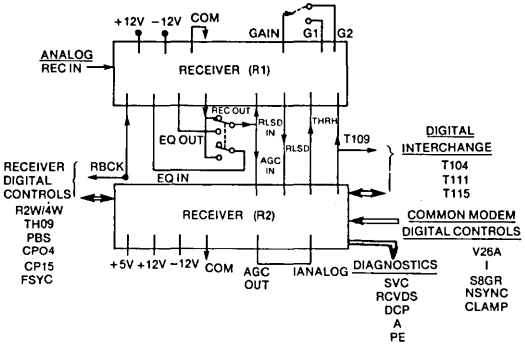
The R24 modem modules provide the user with sufficient flexibility to implement a wide range of modem functional configurations. This flexibility is achieved by digital control at the module interfaces. For a given application, such as a lease network V.26 Alternative B modem (Bell 201B), the complexity of the user interface can be significantly reduced by strapping those data interface inputs which do not change. The modem interface can also be under software control.

Figures 1 and 2 show the basic interface connections for the transmitter module (T) and the receiver modules (R1,R2). These diagrams are applicable for any operation mode of the modem-simplex, half-duplex, or full-duplex.



TRANSMITTER INTERFACES

Figure 1



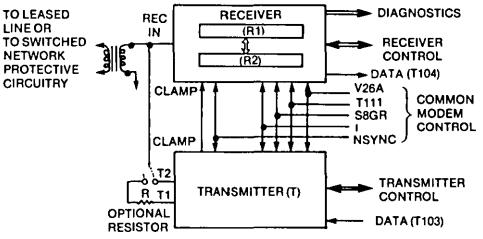
RECEIVER INTERCONNECTION

Figure 2

MODEM OPERATION — HALF OR FULL-DUPLEX

Figure 3 indicates the module interconnections necessary for half-duplex operation. For full-duplex operation, the transmitter/receiver interconnections are similar to the half-duplex case with the exception that "REC IN" is not connected to T2 or T1. In full-duplex operations, the transmission and receiver paths are independent.

As shown in the diagram, a transformer is sufficient to connect directly to a leased line in the U.S. For the switched network, registered protective circuitry or a data access arrangement (DAA) is generally required. Rockwell offers an FCC registered protective circuitry product to support this application. Requirements for line interface and protective circuitry vary internationally.

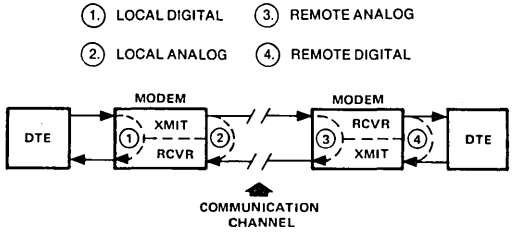


TRANSMITTER-RECEIVER INTERCONNECTION (HALF DUPLEX)

Figure 3

Secondary Channel — The modem modules provide the user with all the interface connections needed to add an external secondary channel if required. This data transmission channel would operate at a lower rate, and in a different portion of the available bandwidth than the primary. Additional external receive filtering would also have to be added to allow simultaneous operation of the primary and secondary channels.

Analog and Digital Loopback — To check out or diagnose the communication link, loopback testing is often performed. A test word is transmitted and "looped" back to the originating DTE. Typical types of loopback tests are:



DTE - Data Terminal Equipment

The modem modules provide the user with all the necessary interface connections to implement almost any loopback scheme desired. With a minimum amount of external circuitry, loopback testing can be controlled via a communications adapter/software approach or manually. For local analog, remote analog and remote digital loopback, the V.27 scrambler within the modem can be used to generate a 127-bit word.

INTERFACE DESCRIPTION

STANDARD DIGITAL INTERCHANGE

Term (CCITT V.24 Equivalent)	EIA RS232C Equivalent	Module Interface Input	Module Interface Output	Description
T103	BA	T-9		Transmitted Data
T104	BB		R2-5	Received Data
T105	CA	T-8		Request to Send
T106	CB		T-6	Ready for Sending (Clear to Send)
T109	CF	R1-4	R2-22	Data Channel Received Line Signal Detector (Carrier Detect)
T111	CH	T-12, R2-9		Data Signalling Rate Selector Selects 2400 bps or 1200 bps Mode
T113	DA	T-7		External Transmit Clock (Transmitted Signal Element Timing)
T114	DB		T-10	Transmit Clock (Transmitted Signal Element Timing)
T115	DD		R2-6	Receive Clock (Receive Signal Element Timing)

ANALOG LINE INTERFACES

Term	Module Interface Input	Module Interface Output	Description
REC IN	R1-12		Analog Line Signal Input (Receive Filter Input)
T1		T-1	Low Impedance Transmitter Output
T2		T-2	Standard Transmitter Output 600 ohms Impedance

COMMON MODEM DIGITAL CONTROLS

Term	Module Interface Input	Module Interface Output	Description
V26A	T-16 R2-13		Selects V.26A or V.26B Dibit Encoding
I S8GR	T-15 R2-12 T-17 R2-14		Controls for Scramble Operation
NSYNC	T-14 R2-11		Controls T109 to Force Rapid Resynchronization of the Receiver
CLAMP	R2-10	T-13	Implements Squelch for Carrier Detect (T109)

TRANSMITTER DIGITAL CONTROLS

Term	Module Interface Input	Module Interface Output	Description
CAUTO	T-3		Initiates Answer Tone
TONA		T-5	Indicates Completion of Transmission of Answer Tone
TBC		T-4	Transmitter Baud Clock
Z	T-28		Input Forcing Transmit Clock (T114) to Phase and Frequency Lock to External Transmit Clock (T113)
T2W/4W X K Y TC06 800MS E	T-11 T-24 T-25 T-26 T-27 T-29 T-30		Inputs Affecting Ready for Sending Response Times, Answer Tone Frequency and Carrier Detect (T109) Squelch

TRANSMITTER ANALOG CONTROLS

Term	Module Interface Input	Module Interface Output	Description
DAC OUT		T-22	Output of Digital to Analog Converter
TFIL	T-23		Input to Low Pass Filter. DAC OUT is Normally Connected to TFIL Unless Additional Filtering or an Equalizer is to be Inserted.
TIN	T-31		These Nine Signals Implement the Transmitter Output Level Attenuator. One of the Signals – 1dBm, . . . , – 15dBm is Strapped to TIN to Set the Desired Output Level.
– 1dBm		T-39	
– 3dBm		T-38	
– 5dBm		T-37	
– 7dBm		T-36	
– 9dBm		T-35	
– 11dBm		T-34	
– 13dBm		T-33	
– 15dBm		T-32	

RECEIVER DIGITAL CONTROLS

Term	Module Interface Input	Module Interface Output	Description
RBCK	R1-1	R2-25	Receiver Baud Clock
RLSD THRH R2W/4W TH09	R2-24 R1-3 R2-8 R2-18	R1-2 R2-23	Control Signals to Generate Carrier Detect (T109) and Implement T109 Threshold Set Select Function
TC09	R2-15		Determines Carrier Detect (T109) Off-to-On Response
PBS	R2-16		Determines Carrier Detect (T109) On-to-Off Response
CP04	R2-17		Clamps Received Data (T104) to a mark or space when Carrier Detect (T109) is Off
CP15	R2-19		Optional Clamping of Received Clock (T115)
FSYC	R2-20		Fast Sync Optional Fast Resynchronization Procedure

RECEIVER DIGITAL DIAGNOSTICS

Term	Module Interface Input	Module Interface Output	Description
SYC RCVDS DCP A PE		R2-1 R2-2 R2-4 R2-3 R2-7	Digital Outputs which Enable User to Generate Eye Pattern and Phase Error Information

RECEIVER ANALOG CONTROLS

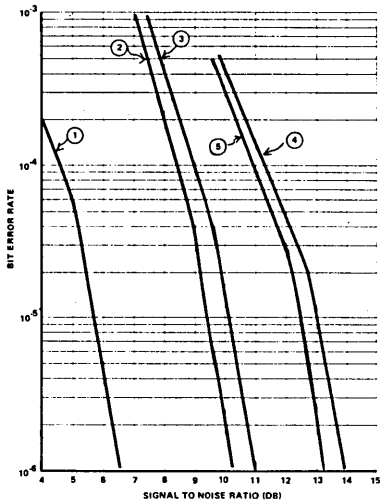
Term	Module Interface Input	Module Interface Output	Description
REC OUT	R1-7		Receive Filter Ouput
EQ IN	R1-8		Equalizer Input
EQ OUT	R1-6		Equalizer Output
RLSD IN	R1-5		Carrier Detect Circuitry Input
AGC IN	R2-21		Automatic Gain Control Circuitry Input
AGC OUT		R2-26	Automatic Gain Control Circuitry Output
GAIN G1 G2	R1-11 R1-9	R1-10	Optional Carrier Detect (T109) Threshold Selection Controls
IANALOG	R2-27		Sample and Hold Circuitry Input

MODEM PERFORMANCE

The R24 is a high performance synchronous 2400 bps DPSK modem, utilizing a coherent demodulation technique to achieve reliable operation over the switched network or unconditioned lines. This section contains a quantitative discussion of the R24's typical performance under varying test conditions.

Timing Jitter — The maximum steady state timing jitter of "receive clock" with respect to "transmit clock" is less than 10% p-p for an input signal-to-noise ratio of 12 dB.

Bit Error Rate — The following graph represents typical R24 performance:

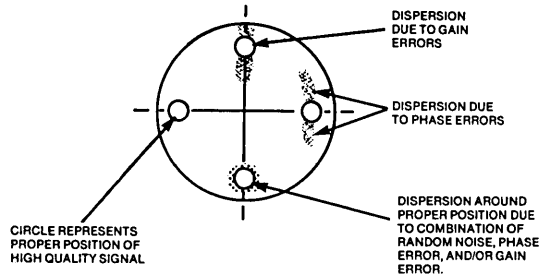


1 1200 BPS, BACK-TO-BACK, SCRAMBLER, NO EQUALIZER
2 2400 BPS, V.26A OR B, BACK-TO-BACK, SCRAMBLER, NO EQUALIZER
3 2400 BPS, V.26A OR B, 15°-150 HZ PHASE JITTER, NO SCRAMBLER, NO EQUALIZER
4 2400 BPS, V.26A OR B, 30°-120 HZ PHASE JITTER, NO SCRAMBLER, NO EQUALIZER
5 2400 PBS, V.26A OR B, 3002 UNCONDITIONED LINE, NO SCRAMBLER, EQUALIZER

Typical Bit Rate Performance

Phase Error — Phase error can be measured by using the modem's output signals PE, SYC, and A. With an external test circuit, a numerical value can be derived to indicate the quality of received data. This numerical value can be directly correlated to bit error rate performance. The required test circuit can be implemented with discrete circuitry or in software within a microcomputer.

Eye Pattern — By using the modems digital output signals RCVDS, SYC, and A along with an added test circuit, the user can generate an oscilloscope quadrature eye pattern. This pattern displays the received signal as a group of dots in the baseband signal plane; hence, it is a graphic representation of modem performance.



Typical Eye Pattern: 4 Phase-2400 bps-1200 Baud (V26A)

Phase error and eye pattern can be extremely useful for modem acceptance testing, product evaluation, and observation of line signal quality under actual operation.

ELECTRICAL CHARACTERISTICS

POWER REQUIREMENTS

Module	Voltage	Ripple	Maximum Current
T	+5 Vdc ±5% +12 Vdc ±5% -12 Vdc ±5%	100 mV p-p 50 mV p-p 50 mV p-p	38 mA 16 mA 48 mA
R1	+12 Vdc ±5% -12 Vdc ±5%	50 mV p-p 50 mV p-p	23 mA 16 mA
R2	+5 Vdc ±5% +12 Vdc ±5% -12 Vdc ±5%	100 mV p-p 50 mV p-p 50 mV p-p	64 mA 25 mA 78 mA

Maximum total power consumption approximately 3 watts.
Typical total power consumption approximately 2 watts.

DIGITAL INTERFACE

The R24 provides LS TTL or CMOS compatible logic levels that are functionally equivalent to EIA RS232/449 and CCITT V.24.

Input Logic	Allowed Input Voltage Levels
Low	-12.0V to +0.8V Sinking <10 μA
High	+4.0V to +5.0V Sourcing <10 μA

Digital inputs are directly CMOS compatible. Interfacing with standard TTL or low-power Schottky TTL requires an external pull-up resistor.

Output Logic	Allowed Output Voltage Levels
Low	0.0V to +0.4V Sinking 0.36 mA
High	+4.0V to +5.0V Sourcing 100 μA

Digital outputs are directly CMOS or low-power Schottky TTL compatible.

TRANSMISSION LINE INTERFACE

The R24 provides an analog interface that must generally be transformer coupled to ensure normal telephone line isolation. Through appropriate selection of transformers and other interface circuitry, the R24 can be configured to operate on leased or dial-up telephone lines, or on other special private networks. For the dial-up line interface, Rockwell offers an FCC registered module that allows direct connection to this network. For the leased line interface, only transformers with characteristics similar to those utilized on the R24 modem evaluation board are required for this connection.

The receiver and transmitter line interfaces are single-ended (non-transformer coupled) signals with the following characteristics:

Transmitter Output (Normal)

Output Impedance: 600 ohms ±2%
Maximum output level: ≤ 0.0 dBm

Transmitter Output (Alternate) Low Impedance:

Output Impedance: 0 ohms (op amp output)

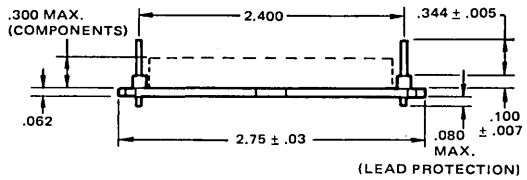
Maximum output level ≤ +6.0dB

Note: This output for transformer loss compensation.

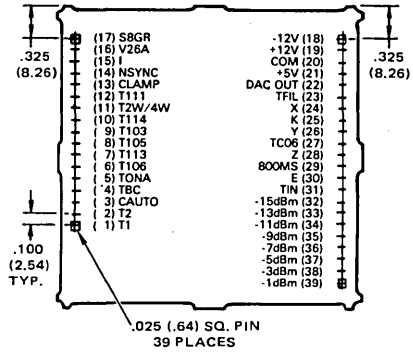
Receiver Input:

Input Impedance: 15.8K ohms ±1%
Maximum Input Level: 0.0 dBm

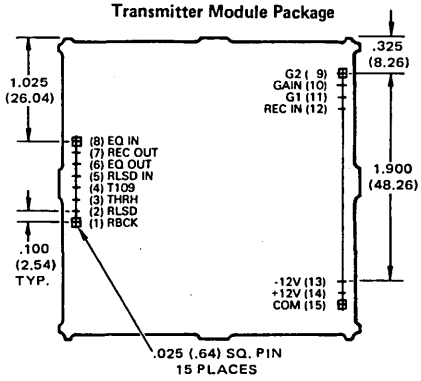
MECHANICAL SPECIFICATIONS



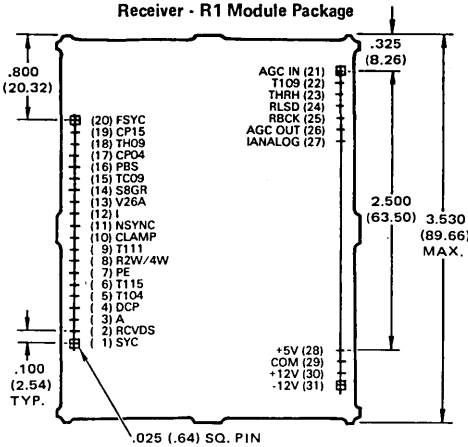
NOTE: This cross-section is common to all modules.



Transmitter Module Package



Receiver - R1 Module Package



Receiver - R2 Module Package

NOTES: 1) Dimensions in inches (millimeters).
2) Component side shown

PRINTED CIRCUIT BOARD MOUNTING OPTIONS FOR THE R24 MODULES

Three methods of mounting are commonly used. Each configuration has certain distinct advantages.

Mounting Method	Type of Connection or Connector Used	Basic Advantage
Standard Flush PCB Component Mount	Wave Soldered Into Standard PCB Eyelets	Lowest Height Profile
Above Board Low Profile Socket	Connectors (SAE Series 3000 or Methode Series 1000) These Sockets are Wave Soldered Into Standard PCB Eyelets	Plug-in Capability at Low Cost
PCB Plug-in Sockets (Bullets)	Connectors (AMP Miniature Spring Sockets.) Pin Sockets are Individually Soldered Into PCB Eyelets	Lowest Profile for Plug-in Capability

ENVIRONMENTAL SPECIFICATIONS:

Operating temperature: 0°C to 60°C
Storage temperature: -40°C to + 80°C
Relative humidity: to 95% (non-condensing)
Altitude: -200 to 10,000 feet (-61 meters to 3,049 meters)
Burn-In: 96 hours at 70°C

Order Information

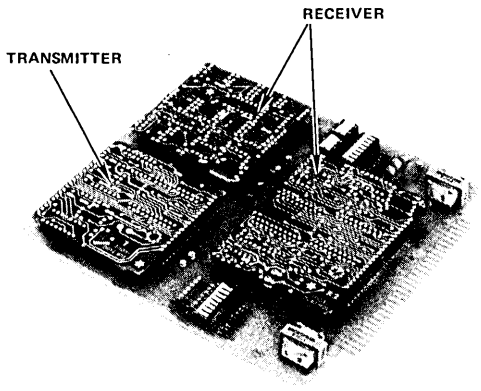
When ordering, specify products as follows:

R24 — Set of 3 modules (T, R1, R2)
R24MEB — Modem Evaluation Board

The R24 transmitter function (R24-T module) and the R24 receiver function (R24-R1, R24-R2 modules) can be purchased separately. Contact your Rockwell Sales office or Anaheim to quote specific customer requirements.

R24 MODEM EVALUATION BOARD

To facilitate evaluation and design-in of the R24 modem for new and existing equipment designs, an R24 Modem Evaluation Board (R24MEB) is available — see below. The R24MEB can be easily combined with terminal systems for real-time performance evaluation.



R24 Modem Evaluation Board (R24MEB)

The Modem Evaluation Board is equipped with a standard 31 pin edge connector, control switches, output level jumper, and interface transformers. These features allow full control of the interface circuitry. In addition, this unit can be used directly in a U.S. leased line configuration.

The R24MEB is recommended for all first-time users to assist in their evaluation. Complete documentation is supplied with each initial R24MEB.

Rockwell

MODEM PRODUCTS PRODUCT SUMMARY

R24 DC 2400 BPS Direct Connect Modem

INTRODUCTION

The Rockwell R24 DC is a high-performance, serial synchronous DPSK modem suitable for direct connection to domestic switched network or two-wire private lines. Utilizing extensively MOS/LSI Technology and High Quality Components, the Modem plus registered protective circuitry is implemented on a single 5.00" by 7.850" card. Performance and versitility are enhanced while cost and size are reduced by the on-board Rockwell PPS-4/1 One Chip Microcomputer.

The Rockwell R24 DC offers the user a complete high performance 2400 BPS Modem that is FCC registered for direct connection to the dial-up network. OEM's can easily incorporate the Single Card into their computer terminals, communication networks, PABX equipment, Data concentrators, Stand-alone box modems or any applications where reliable data communication is required.

MAXIMUM MODULE DIMENSIONS

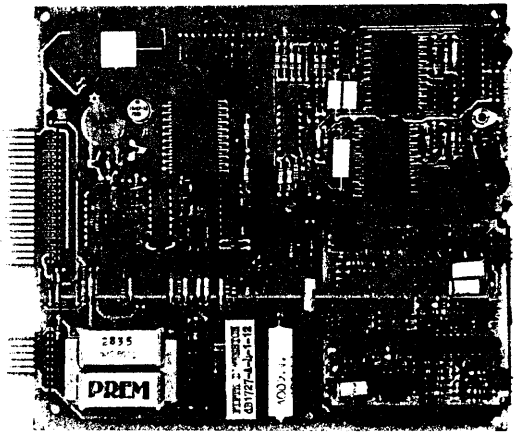
W	L	H
5.00"	7.850"	0.600"

INTERFACE CONNECTORS

DTE	TELEPHONE LINE
40 pin, 0.100" spacing 20/side	10 pin, 0.100" spacing 5/side

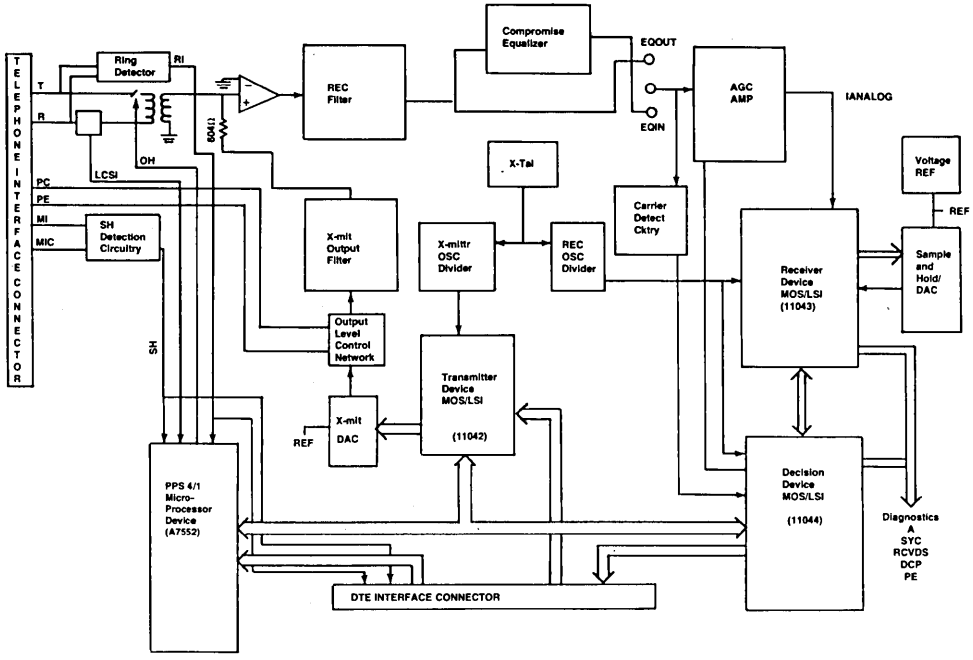
FEATURES/BENEFITS

- High Performance; Low Cost
- LSI High Density; Low Power
- Microcomputer Controlled Line Connect/Disconnect Sequence; Low Component Count
- Bell 201 B/C, CCITT V.26 Compatible
- Half Duplex (2-Wire) Operating Mode
- 2400 BPS Data Rate
- Auto or Manual Answer
- Auto or Manual Call Originate (Pulse Dialing)
- Automatic Answer Back Tone Generation upon Auto Answer
- Direct Connect to Swtiched Network
- Programmable or Permissive Connection Arrangement
- Local Analog Loopback Test Mode
- Compromise Equalizer (Strap Selectable)
- Scrambler/Descrambler Facility (Selectable)
- Line Current Sensing (Selectable)
- DTE Interface LSTTL/CMOS Compatible
- External Transmit Data Clock Tracking
- Power Requirements, ±12V, +5V
- Typical Power Consumption 3 Watts
- Diagnostic Outputs Available for Eye Pattern and Data Quality Monitor
- 15 Second Abort Timer (Selectable)



Specifications subject to change without notice
Document No. 82400 N44
April 1981

R24 DC FUNCTIONAL BLOCK DIAGRAM



POWER SUPPLIES:

+5VDC ± 5% at 102 ma (max.)
+12VDC ± 5% at 64 ma (max.)
−12VDC ± 5% at 142 ma (max.)

ENVIRONMENTAL SPECIFICATIONS

Operating temperature: 0°C to 60°C
Storage temperature: −40°C to +80°C
Relative humidity: to 95% (non-condensing)
Burn In: 96 hours at 70°C

For more information contact your local Rockwell Representative or Regional Office, or Telecom/Subsystem Marketing, Rockwell Microelectronic Devices, P.O. Box 3669, Anaheim, CA 92803. TWX 910-591-1698. Telephone: (800) 854-8099, in California (800) 422-4230.

Rockwell International

Rockwell

MODEM PRODUCTS PRODUCT SUMMARY

V96P/1 Multi-Configuration 9600 BPS Modem

INTRODUCTION

The Rockwell V96P/1 is a versatile, high-performance modem on a single printed circuit board. Having CCITT V.29 and V.27 compatibility, the V96P/1 offers the user sufficient flexibility to customize a 9600 bps modem. With minimum interface circuitry, the V96P/1 can operate on dedicated lines or on the general switched network. In addition, the V96P/1 is compatible with the Rockwell V96P and M96P products.

MARKET RESTRICTIONS

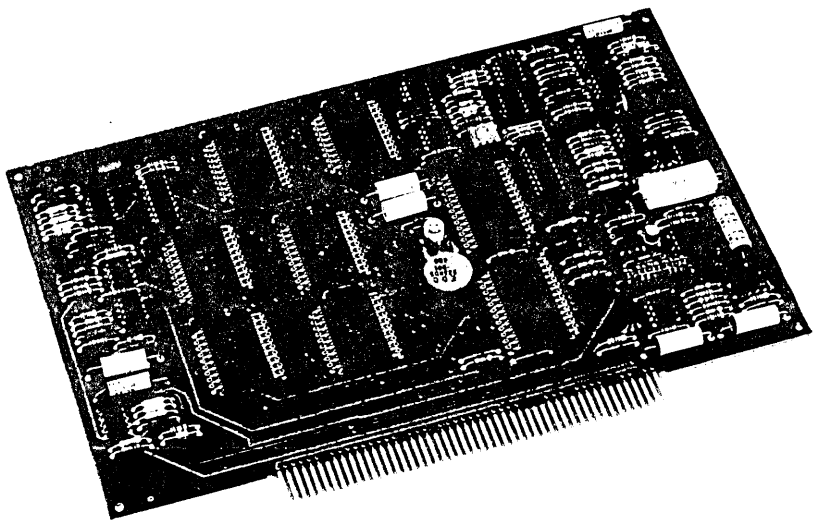
Minimum purchase must be 1000 units/year. Additional restrictions are application dependent. Please contact Rockwell for further information.

FEATURES/BENEFITS

- Maximum digital LSI signal processing
- 9600/7200/4800/2400 bps modes
- Ultimate user flexibility (CCITT V.29, V.27 ter, V.27 bis compatible, and 300 bps per CCITT T.30)
- Single printed circuit card
- Smallest full-feature modem
- High reliability
- Approaches theoretical performance limits
- Operating Modes:
  - Half duplex (2 wire)
  - Full duplex (4 wire)
- TTL-compatible
- 0 to −45 dBm dynamic AGC range
- Analog loopback test circuitry
- Automatic adaptive equalizer
- Typical power consumption 3.5 watts

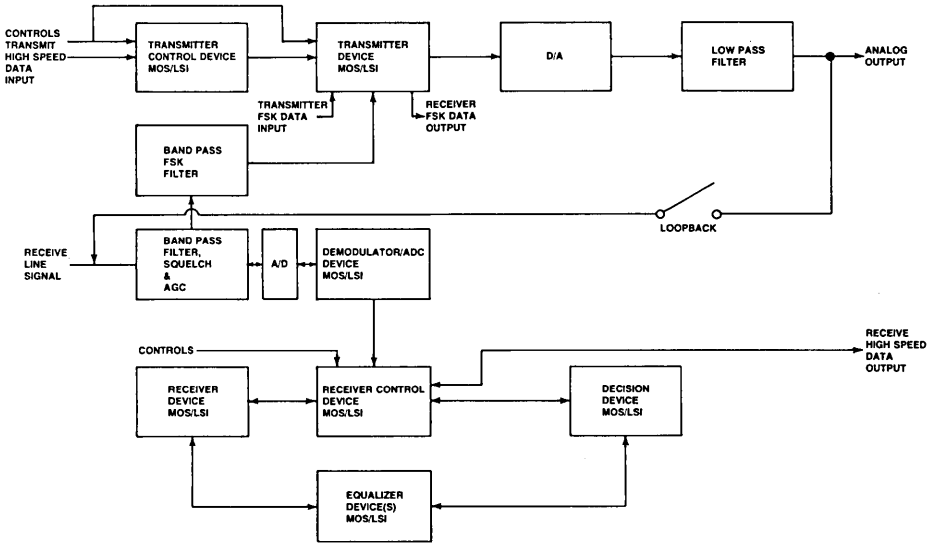
BOARD DIMENSIONS

9.188 in. (233.38 mm) × 6.288 in. (159.7 mm)



Specifications subject to change without notice
Document No. 82400 N45
April 1981

V96P/1 FUNCTIONAL DIAGRAM



POWER SUPPLIES:

+5V (± 5%) +VM, <200 ma
+12V (± 5%) +VA, <110 ma
−12V (± 5%) −V, <280 ma
(maximum currents)

ENVIRONMENTAL SPECIFICATIONS

Operating temperature: 0°C to 60°C
Humidity: Up to 90%, non-condensing, or a wet bulb temperature up to 35°C, whichever is less

For more information contact your local Rockwell Representative or Regional Office, or Telecom/Subsystem Marketing, Rockwell Microelectronic Devices, P.O. Box 3669, Anaheim, CA 92803. TWX 910-591-1698. Telephone: (800) 854-8099, in California (800) 422-4230.

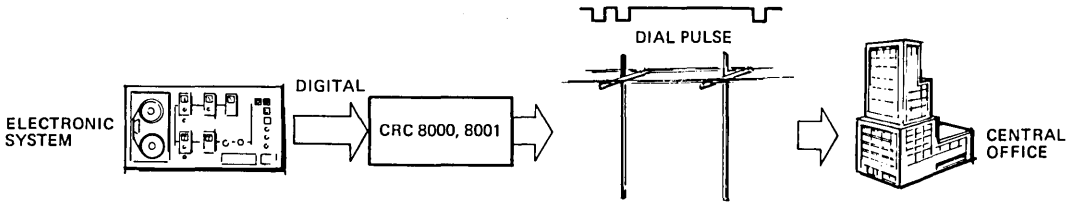
Rockwell International

TELECOM DEVICES

Rockwell International

Rockwell MOS/LSI Telecommunication Products

CRC 8000, 8001 — Binary to Dial Pulse Dialer



16 Digit First-In-First-Out (FIFO) Memory

Asynchronous Operation

10pps (2KHz Clock) Dial Pulse Operation with a Minimum 650ms Interdigit Time

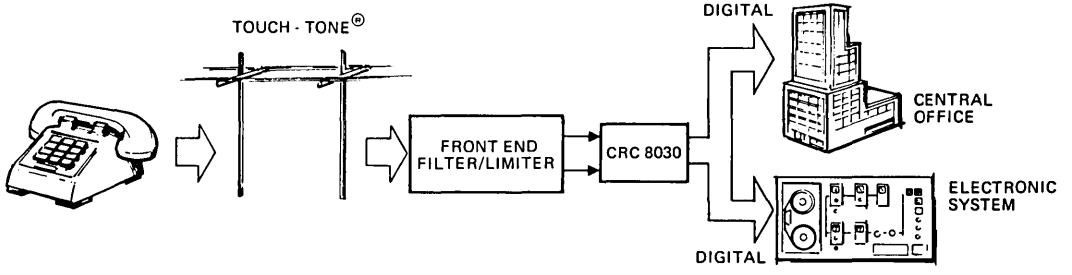
20pps (4KHz Clock) Dial Pulse Operation with a Minimum 325ms Interdigit Time

CRC 8000, TTL Input compatible

CRC 8001, MOS Input compatible

The dialer accepts binary data, stores the data in a first-in-first-out memory, and generates dial pulses at normal telephone rates. Internal timing is derived from an external 2KHz or 4KHz clock. With a 2KHz clock, a 10pps (60% break/40% make) dial pulse frequency having a minimum 650 ms interdigit time is generated. If a 4KHz clock is used, the dial pulse frequency is 20pps and the interdigit time is reduced to 325ms minimum. The memory section is necessary as the incoming data rate may be much faster than the normal dial pulse output rate. Binary codes one (1) through fifteen (15) produce the same number of dial pulses. A binary zero input produces sixteen (16) dial pulses.

CRC 8030 — Dual Tone Multi-Frequency Detector



Digital range filter detects all 16 Touch-Tone® signal combinations

Detects a tone pair in 22 ms to 39 ms

Digital logic impervious to frequency or bandwidth drift caused by time, temperature, or voltage

Automatic internal reset when no tones are present

Variable pulsewidth Strobe output provides increased talk-off protection

Binary or 2-of-8 coded outputs option

Inputs/outputs can be left floating when not used

Single or dual power supply option

On-chip oscillator – 3.579545 MHz color-burst crystal

Central-office-quality detection

Excellent talk-off protection – As little as one hit on Mitel test tape (CM 7290)

Dual-Tone Multi-Frequency (DTMF) or Touch-Tone® signaling has made telephone communication faster, more efficient and more convenient than dial pulse signaling. Touch-Tone® telephone instruments or automatic dialers generate a tone pair representing the "dialed" number and send them over the lines to a receiver which detects the tones and reliably identifies the number.

Utilizing a digital filter algorithm, the CRC 8030 provides a low-cost and high-performance solution for DTMF detection.

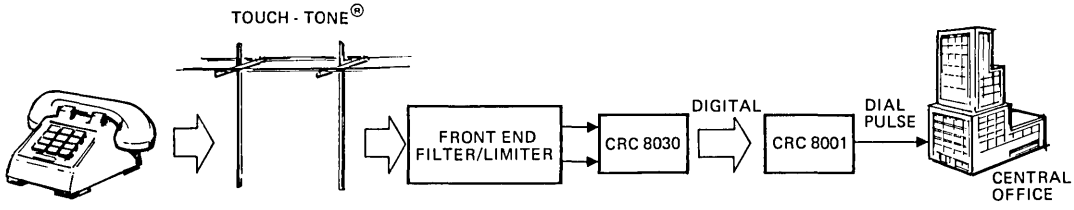
A strobe output indicates when the output data are valid.

When linked with a front-end band-split filter/limiter, the CRC 8030 implements a complete DTMF receiver.

This design approach provides the optimum technological benefits of analog and digital design techniques.

® Registered trademark of AT&T

DTMF to Dial Pulse Conversion



A DTMF to dial pulse converter can be easily implemented using the CRC 8030 and the CRC 8001.

For example, where electronic switching systems (ESS) are not available, the CRC 8030, a Dual-Tone Multi-Frequency Detector, and the CRC 8001, a Binary to Dial Pulse Dialer, can be utilized to convert Touch-Tone® signals to dial pulse signals. The CRC 8030 decodes Touch-Tone signals to their binary equivalent and the CRC 8001 converts the binary information to a train of pulses compatible with the standard telephone dial pulse signals.

MOS/LSI TELECOMMUNICATIONS DEVICES

TECHNICAL BULLETIN

Binary to Dial Pulse Dialer

CRC 8000, 8001

16 Digit First-In-First-Out (FIFO) Memory

Asynchronous Operation

10pps (2KHz Clock) Dial Pulse Operation with a Minimum 650ms Interdigit Time

20pps (4KHz Clock) Dial Pulse Operation with a Minimum 325ms Interdigit Time

TTL Compatible

General Description

The CRC 8000 and CRC 8001 are P-channel enhancement mode MOS Binary to Dial Pulse Dialer utilizing ion implant, low threshold voltage processing. The Dialer accepts binary data, stores the data in a first-in-first-out memory, and generates dial pulses at normal telephone rates. Internal timing is derived from an external 2KHz or 4KHz clock. With a 2KHz clock, a 10pps (60% break/40% make) dial pulse frequency having a minimum 650 ms interdigit time is generated. If a 4KHz clock is used, the dial pulse frequency is 20pps and the interdigit time is reduced to 325ms minimum. CRC 8000 and CRC 8001 are identical except for their input interface. CRC 8000 inputs are TTL compatible and CRC 8001 inputs are MOS compatible. The devices are available in a 16 pin dual-in-line package.

The CRC 8000 can be installed in telephone central office stations to perform binary to dial pulse conversions. In areas where electronic switching systems (ESS) are not available, the CRC 8000 and CRC 8030, a Dual-Multi-Frequency Detector, can be utilized to convert Touch-Tone® signals to dial pulse signals. The CRC 8030 decodes Touch-Tone signals to their binary equivalent and the CRC 8000 converts the binary information to a train of pulses compatible with the standard telephone dial pulse signals.

Operation

Digits, in the form of four binary inputs, are loaded asynchronously relative to the clock into a 16 digit first-in-first-out (FIFO) memory. This memory section is necessary as the incoming data rate may be much faster than the normal dial pulse output rate. Binary codes one (1) through fifteen (15) produce the same number of dial pulses. A binary zero input produces sixteen (16) dial pulses.

Dialer operation is controlled by the "Load" and "Memory Read Inhibit" inputs. A load pulse is required in order to input each digit into the FIFO. With a 2KHz clock, the maximum data entry rate is 500 digits per second.

The Memory Read Inhibit line can be used to delay the Dial Pulse Output. If the Memory Read Inhibit line is low (binary zero), the first digit entering the FIFO memory initiates the dialing sequence. The digit is transferred from the memory to a down counter that generates the appropriate number of dial pulses. Internal timing produces the proper interdigit time between pulse trains. If there is a pause in the binary data input, the circuit generates an extra length interdigit time in a manner identical to that created by a rotary dial.

A high level (binary one) Memory Read Inhibit prevents the reading of the memory thereby causing a pause. During this condition, existing data in the FIFO will be stored until Memory Read Inhibit is released (low level). When the inhibit line is changed from a low level (binary zero) to a high level (binary one), a dial pulse train in process will be completed before pausing. Additional digit data may be input to the FIFO memory as long as the 16 digit capacity is not exceeded.

The Busy output line is high when there is data in memory or dial pulses are being generated.

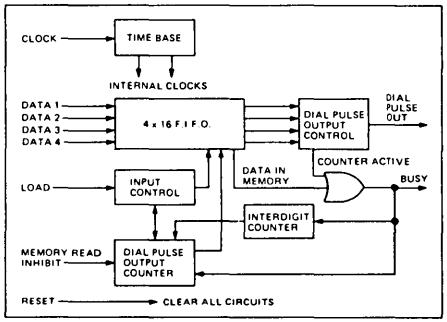
The Reset input is a "Master Reset". If the Reset input line is low, Busy is set to a low level and Dial Pulse Out is set to a high level. The outputs will remain in that state until a new digit is input to the FIFO.

Technical Characteristics

MAXIMUM RATINGS

Non-operating voltages with no damage to device

Supply Voltage V_{DD}	V_{SS} - 8.0V
Supply Voltage V_{GG}	V_{SS} - 21.0V
Positive Voltage on any pin	V_{SS} + 0.3V
Negative Voltage on any pin	V_{SS} - 20.0V
Power Dissipation at 25°C	275mw
V_{SS} = +5.0V, V_{GG} = -12.0V	
Operating Temperature Range (case)	0°C to +70°C
Storage Temperature Range (case)	-55°C to +150°C



33177-3

® AT&T Registered Trademark

CRC 8000, 8001 Binary to Dial Pulse Dialer

RECOMMENDED OPERATING CONDITIONS/ELECTRICAL CHARACTERISTICS FOR 10pps OPERATION

Unless Otherwise Noted V_{SS} = +5.0V, V_{GG} = -12.0V, V_{DD} = 0.0V, $0^oC \leq T_A \leq 70^oC$, and clock frequency = 2.0KHz ± 5%

PARAMETER		MIN	TYP	MAX	UNITS	CONDITIONS
Power Supplies						
V_{SS}	Supply Voltage	4.75	5.0	5.25	V	V_{DD} = 0.0V See Note 1
V_{GG}	Supply Voltage	-13.0	-12.0	-11.0	V	V_{DD} = 0.0V
Inputs						
$V_{IN}(0)$	Logical "0" input voltage	-1.0	0.0	0.8	V	See Note 2
$V_{IN}(1)$	Logical "1" input voltage	V_{SS}-0.7		V_{SS}+0.2	V	See Note 2
C_{IN}	Input capacitance			10	pF	$V_{IN} = V_{SS}$ - 1.0V
Input Timing						
f_c	Clock repetition rate	1.9	2.0	2.1	KHz	See Note 3
t_{pc}	Clock duty cycle	45	50	55	%	Applies to all inputs including clock
t_r	Input pulse rise time	40		500	ns	Applies to all inputs including clock
t_f	Input pulse fall time	40		500	ns	Applies to all inputs including clock
t_{LH}	Load pulse width "High"	1.9			ms	See Timing Diagram
t_{LL}	Load pulse width "Low"	0.1			ms	See Timing Diagram
t_{d1}	Data set-up time			0.5	ms	See Timing Diagram
t_{d2}	Data hold time	1.75			ms	See Timing Diagram
t_{ML}	Memory Read Inhibit stable time relative to Load			650	ms	See Note 4
t_{MDP}	Memory Read Inhibit stable time relative to Dial Pulse Out			650	ms	See Note 4
t_R	Reset pulse width	1.0			μs	

NOTES

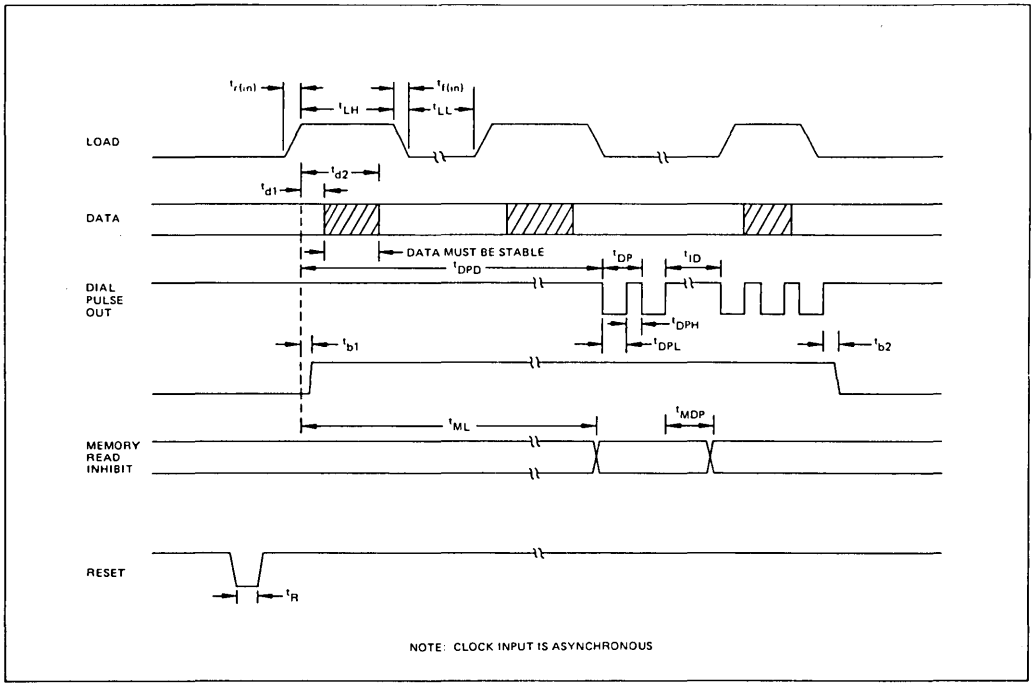
1. Other supply parameters are permissible including V_{SS} = 0.0V, V_{DD} = -6V, and V_{GG} = -12V. Input/output parameters will be adjusted accordingly.

	Min.	Typical	Max.
V_{in} (0)	-7.0	-6.0	-5.2
V_{in} (1)	-0.7	0.0	+0.2
V_{out} (0)	0.0	0.0	-5.6
V_{out} (1)	-2.6	0.0	0.0

2. All inputs of CRC 8000 have "on chip" 3200 ±30% ohm pull-up resistor to V_{SS} and are suitable for being driven by TTL. All inputs of CRC 8001 have a high impedance input (no pull-up resistor) and are suitable for interface with MOS devices.

3. For 20pps operation, a 4.0 KHz is clock required. If the clock has a 5% tolerance, the operating specification can be derived from the above table. All parameters will remain the same except for the following timing parameters which will be reduced by one half: t_{LH}, t_{LL}, t_{d2}, t_{ML}, t_{MDP}, t_{DPD}, t_{DP}, t_{DPL}, t_{DPH}, t_{ID}. Similarly, a 10 KHZ clock could be used, producing a 50pps output rate.

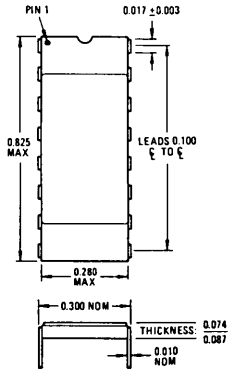
PARAMETER		MIN	TYP	MAX	UNITS	CONDITIONS
Outputs						
$V_{out}(0)$	Logical "0" output voltage			0.4	V	I_{sink} = 1.6 mA
t_f(out)	Output fall time			500	ns	90% to 10%
$V_{out}(1)$	Logical "1" output voltage	2.4			V	I_{source} = 0.1 mA
t_r(out)	Output rise time			400	ns	10% to 90%
Output Timing						
t_{DPD}	Dial Pulse Out Delay	700		900	ms	
t_{DP}	Dial Pulse Period	95	100	105	ms	See Note 3
t_{DPL}	Dial Pulse Width "Low"	57	60	63	ms	and Timing
t_{DPH}	Dial Pulse Width "High"	38	40	42	ms	Diagram
t_{ID}	Dial Pulse Interdigit Time	650	740		ms	
t_{b1}	Busy Low/High Delay			2.1	ms	
t_{b2}	Busy High/Low Delay			10	μs	
Power						
P_D	Power Dissipation		125	275	mw	



30377-6

4. To prevent a dial pulse train from being output, Memory Read Inhibit must be stable prior to initiating that pulse train. This stabilization point is specified for two cases: (1) If no pulse trains are presently in process (e.g., the device has been reset), Memory Read Inhibit must be stable 650ms after the load pulse was initiated; (2) If a pulse train is in process, to prevent the next pulse train from being output, Memory Read Inhibit must be stable 650ms after the interdigit time was initiated.

BINARY TO DIAL PULSE DIALER (CRC8000-1-3)



PIN ASSIGNMENTS

1	V_{SS}
2	BUSY
3	DATA (2)
4	N.C.
5	DATA (1)
6	DATA (4)
7	DIAL PULSE OUT
8	DATA (8)
9	V_{GG}
10	V_{DD}
11	MEMORY READ INHIBIT
12	LOAD
13	CLOCK
14	TEST OUT*
15	TEST IN**
16	RESET

*PIN 14 IS AN OUTPUT CLOCK RUNNING AT A FREQUENCY OF (PIN 13 ÷ 200)Hz. THE PERIOD IS 60% BREAK/40% MAKE.

**PIN 15 MUST BE GROUNDED (V_{DD}) DURING CIRCUIT OPERATION.

30377-7

Packaging and Ordering Information

The Binary to Dial Pulse Dialer is available in a 16-pin hermetically sealed ceramic dual-in-line package (see pin assignments and package dimension diagram). Order by type numbers.

CRC 8000-1-3 (ceramic DIP) 765-1892-001
CRC 8001-1-3 (ceramic DIP) 765-5841-001

TELECOM
DEVICES

Rockwell

MOS/LSI TELECOMMUNICATIONS DEVICES
DATA SHEET

Dual Tone Multi-Frequency Detector

Digital range filter detects all 16 Touch Tone® signal combinations

Detects a tone pair in 22 ms to 39 ms

Digital logic impervious to frequency or bandwidth drift caused by time, temperature, or voltage

Automatic internal reset when no tones are present

Variable pulsewidth Strobe output provides increased talk-off protection

Binary or 2-of-8 coded outputs option

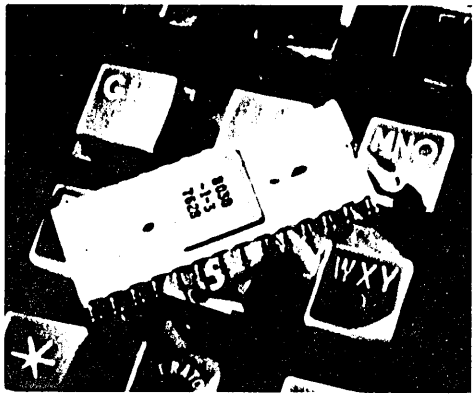
Inputs/outputs can be left floating when not used

Single or dual power supply option

On-chip oscillator — 3.579545 MHz color-burst crystal

Central-office-quality detection

Excellent talk-off protection — As little as one hit on Mitel test tape (CM 7290)



DTMF Signaling and Receivers

Dual-Tone Multi-Frequency (DTMF) or Touch-Tone® signaling has made telephone communication faster, more efficient and more convenient than dial pulse signaling. Touch-Tone® telephone instruments or automatic dialers generate a tone pair representing the "dialed" number and send them over the lines to a receiver which detects the tones and reliably identifies the number. DTMF signals are defined by a 4 x 4 audio tone matrix as illustrated in figure 1. Each digit is represented by one tone from the low-group and one tone from the high-group. These non-harmonically related frequencies protect the message against false-keying by stray signals and voice-generated tones.

A DTMF receiver must recognize the dual tones within a certain bandwidth while tolerating dial tone, noise, input amplitude variation and "twist" or amplitude differential between the two tones. In addition, the receiver has to comply with timing restrictions imposed by the DTMF generation process and meet other specific requirements of the particular application.

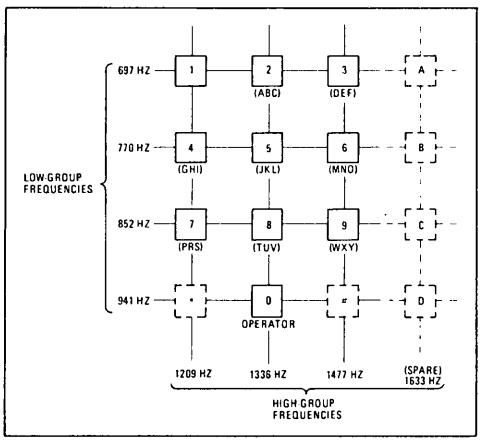


Figure 1. Touch Tone® Pad (Dual Tone Multi-Frequency Signaling)

CRC 8030 General Description

The CRC 8030 provides a low-cost and high-performance solution for DTMF detection. Utilizing a unique digital filter algorithm, the patented* CRC 8030 performs the key critical functions of a DTMF receiver. When used in conjunction with a front-end band-split filter/limiter, the CRC 8030 implements a complete DTMF receiver (figure 2). This design approach provides the optimum technological benefits of analog and digital design techniques.

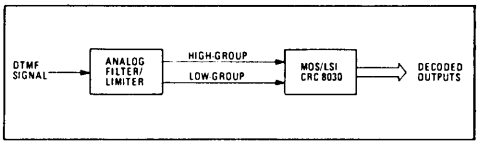


Figure 2. DTMF Receiver Utilizing CRC 8030

® Registered trademark of AT&T

*U.S. Patent No. 4016371

The exact requirements for the front-end filter/limiter vary with the particular receiver application. For example, high quality central office receivers require a more selective front-end filter. Conversely, low-noise environment keyphone systems can use a less stringent front-end filter design.

DTMF receivers historically have been implemented with all-analog filtering techniques, i.e., phase-locked loops, LC filters and active filters. Compared to a phase-locked-loop receiver, the CRC 8030 provides much superior performance. Compared to LC or active filter receivers, the CRC 8030 can be manufactured for a significantly lower cost while providing improved performance. The CRC 8030 provides the economy, performance, size and reliability benefits of digital MOS/LSI. The CRC 8030 is packaged in a 28-pin DIP.

Applications

The CRC 8030 can be applied to all systems requiring DTMF detection. This includes the traditional telephony systems: keyphone, PABX, central office, intercom and mobile radio communications. Other applications include computer signaling and control systems. Where it is necessary to interface with a dial pulse system, the CRC 8030 and the CRC 8000 (a Binary-to-Dial-Pulse Dialer) implement a DTMF-to-dial-pulse conversion system.

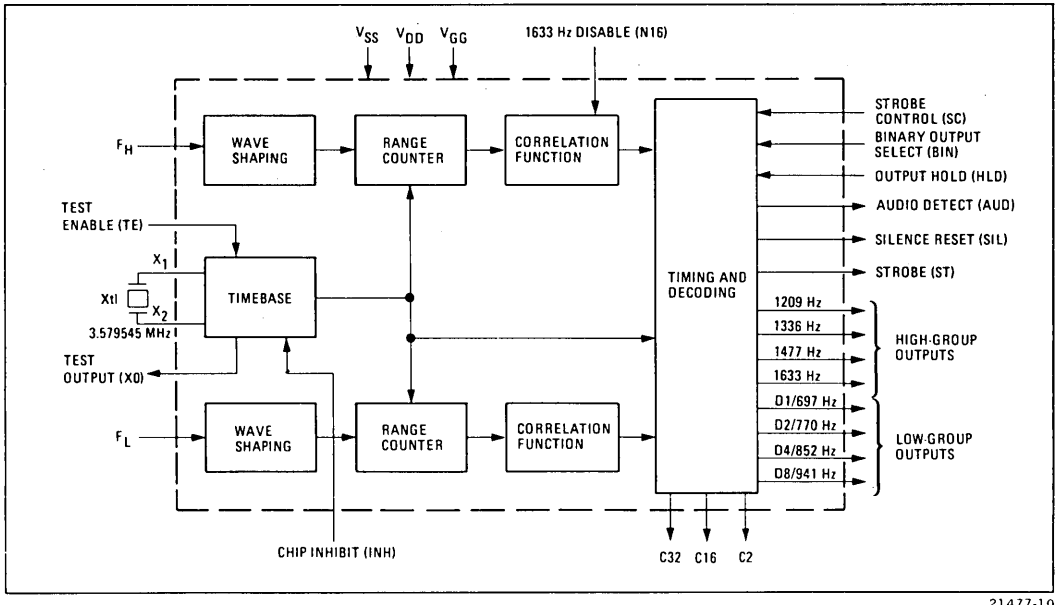
The CRC 8030 has been functionally designed to provide optimum performance for a wide variety of DTMF detection applications.

Operation

The CRC 8030 is a DTMF detector implemented with PMOS ion-implantation processing. This detector accepts group-filtered and square-shaped DTMF frequencies and converts them to binary data or 2-of-8 coded data in 22 ms to 39 ms; out-of-tolerance frequencies are rejected. The device ignores the first few pulses of the input signal in order to prevent errors in detection due to the transients from the Touch-Tone® pad. The signal is then analyzed several times by a digital range filter prior to being accepted as valid. As soon as the range filter has recognized a frequency below 1680 Hz, the Audio Detect (AUD) output is enabled. This output provides the user with a signal for controlling the limiter gain at the receiver front-end. A Strobe (ST) output indicates when the output data are valid.

Once a digit is accepted as valid, the CRC 8030 will ignore any change in tone frequency until either the high-group or low-group tone disappears for more than 10 ms. When this occurs, the device is reset internally and will be ready to accept another Touch-Tone® digit. This feature provides immunity to frequency drift that could be caused by Doppler shift. Should a frequency in either the high- or low-group disappear for less than 10 ms, the gap is bridged resulting in only one digit.

A block diagram of the CRC 8030 is shown in figure 3. The functions include timebase generation, wave shaping circuitry, range counters with correlation circuitry, and the output timing and decoding functions.



21477-10

Figure 3. CRC 8030 Block Diagram.

Technical Characteristics

Maximum Ratings: Non-operating voltages with no damage to device —

Supply Voltage V_{DD} . . . . . V_{SS} -8.0V
Supply Voltage V_{GG} . . . . . V_{SS} -21.0V
Positive Voltage on any pin . . . . . V_{SS} +0.3V
Negative Voltage on any pin . . . . . V_{SS} -20.0V

Power Dissipation ($0^{o}C \leq T_A \leq 70^{o}C$) . . . . . 200 mW
Operating Temperature Range (case) . . . 0^{o} to $+70^{o}C$*
Storage Temperature Range (case) . . $-65^{o}C$ to $+150^{o}C$

*An extended temperature range device will be available in the future.

Inputs and Outputs

The inputs and outputs are illustrated in figure 3 and are described below with a positive logic convention assumed. However, the operation is defined such that when a 2-of-8 output format is chosen, the Strobe and the low-group outputs display data with a negative logic convention. The high-group outputs always display data in a negative logic convention. Detailed timing is shown in the timing diagram, figure 4.

Inputs

Logic levels are MOS compatible. Inputs BIN, INH, HLD, SC, N16, and TE have on-chip active pull-up devices to V_{SS} with a minimum of 50 KΩ resistance; therefore, no connection is required to these pins if a high-level input is desired.

- High- and low-group DTMF signals (FL, FH) — These are the filtered and square-shaped DTMF tones. When no signal is present, both input levels should be low (most negative level).
- Binary Output Select (BIN) — If this input is low (most negative level), the decoded outputs are displayed in a binary format and Strobe (ST) pulses from a normally low state to a high state (figure 4). If this input is high or open, the decoded outputs are displayed in a 2-of-8 code and Strobe pulses from a normally high state to a low state.
- Chip Inhibit (INH) — If this input is low, the device is inhibited from decoding any DTMF tones. When decoding binary, the outputs stay low. When decoding 2-of-8, the outputs stay high. If this input is high or open, the outputs function normally. Chip Inhibit is also a master reset except for the output data registers when Output Hold is low.
- Output Hold (HLD) — If this input is low, the output data, if valid, are stored in the output registers. If the input is high or open, the outputs will function normally.
- Strobe Control (SC) — This input controls the pulsewidth of the Strobe (ST) output.

  When Strobe Control is high or open, the signal is analyzed for the full 39 ms data acquisition (t_{DA1}, Long Strobe) period. If the input tone-pair is detected within 22 ms, then the Strobe (ST) output pulsewidth is at a maximum of 17 ms. If detection takes more than 22 ms, the Strobe pulsewidth is reduced by the extra time needed for detection. If the signal is detected after the 39 ms period, no Strobe pulse will occur.

  When Strobe Control is low, the input signal is analyzed for a 33 ms period (t_{DA2}, Short Strobe). If the tone is detected within 25 ms after its inception, then the Strobe pulsewidth is 8 ms. If detection occurs after 25 ms, then the Strobe pulsewidth is reduced by the lag time. If no signal is detected within the 33 ms period, no Strobe pulse will occur.

  When a Short Strobe is selected, a higher quality input signal must be present in order to be accepted as a valid signal. Thus, voice or noise signals on the telephone line, which require a longer detection time, will be ignored by the chip. As a result, the device has a higher immunity to false-keying when Strobe Control is low.

  In either case, the tone pair may be detected, but the Strobe signal may not necessarily be generated, depending on the quality of the input tone-pair.
- 1633 Hz Disable (N16) — If this input is low, the device will not respond to the 1633 Hz tone, thus improving the talk-off rate. If this input is high or open, the device will respond to the 1633 Hz tone.
- Clock Inputs and Control (X1, X2, TE) — The CRC 8030 contains an on-chip oscillator for a 3.57954 MHz parallel resonant crystal. This crystal is connected to X1 and X2 and TE is held high or left open. As an option, an external 447.443 kHz oscillator can be used to clock the CRC 8030. In this case, X1 is the 447.443 kHz clock input, X2 is left open, and TE is held low. For some applications (e.g., using several CRC 8030 devices on a board), it is possible to drive the chip with an external 3.579545-MHz clock at pin X2, while leaving the TE pin open, and tying pin X1 to V_{SS}.

Outputs

All outputs feature open-drain devices. With a single-power supply ($V_{GG} = V_{DD}$), they will drive LPTTL, MOS or CMOS inputs. With a dual power supply, they will drive the base of a transistor. The open-drain output devices must be tied through a pull-down resistor to a negative voltage between V_{DD} and V_{GG} (when used); the value of this resistor depends upon the type of interface. Typically:

Resistor	Interface
1.5KΩ	LPTTL
10.0KΩ	MOS or CMOS
7.5KΩ	Base of a Transistor

These outputs can also drive LEDs. For more design details, consult the Collins Application Note, "CRC 8030 Telephone DTMF Receiver".

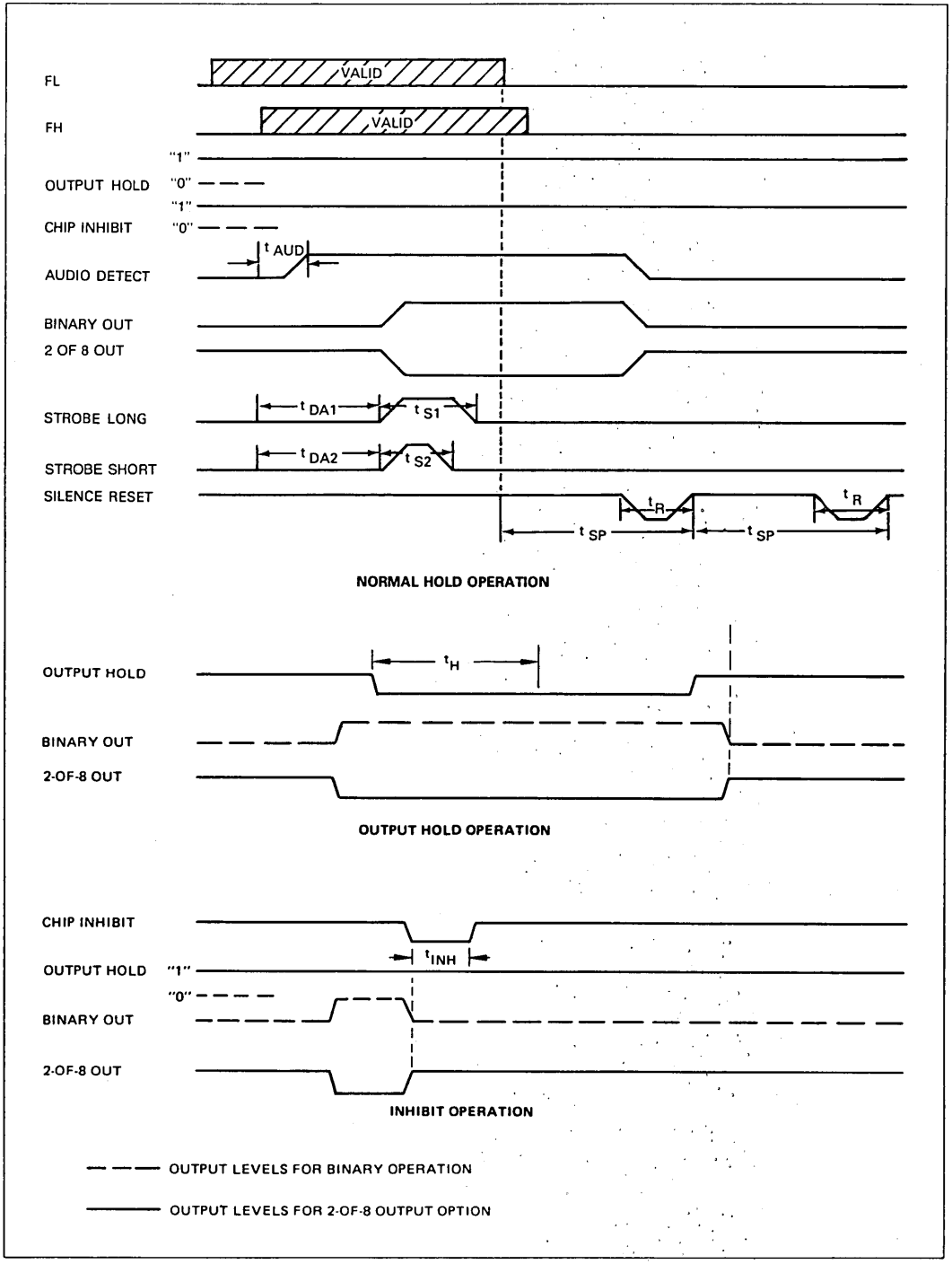
- Decoded Outputs (D1/697 Hz, D2/770 Hz, D4/852 Hz, D8/941 Hz, 1209 Hz, 1336 Hz, 1477 Hz, 1633 Hz) — These outputs display decoded information in either a binary or a 2-of-8-coded format as described below.

  When a 2-of-8 format is selected (BIN input is held high or left open), all 8 outputs are utilized. When a particular digit is decoded, the corresponding high- and low-group outputs go low (figure 1). For

RECOMMENDED OPERATING CONDITIONS/ELECTRICAL CHARACTERISTICS
Unless Otherwise Noted V_{SS} = +5.0V, V_{GG} = -8.0V, V_{DD} = 0.0V
$0^oC \leq T_A \leq 70^oC$
Positive Logic

PARAMETER		MIN.	TYP.	MAX.	UNITS	CONDITIONS
Power Supplies						
V_{SS}		+4.75	+5	+5.25	V	
V_{GG}		-13.0	-8.0	V_{DD}	V	
V_{DD}				0		
Inputs						
$V_{IN}(0)$	Logical "0" input voltage	-13.0	-8.0	V_{SS}-4.0	V	
$V_{IN}(1)$	Logical "1" input voltage	V_{SS}-0.7		V_{SS}+0.2	V	
R_{IN}	Input impedance	50			kΩ	
C_{IN}	Input capacitance			10.0	pF	$V_{IN} = V_{SS}$-1.0V
t_r & t_f	Input voltage rise or fall time			15.0	μS	Voltage swing 10% to 90% of final level
Input Timing						
F_1	Clock Crystal Frequency		3.579545		MHz	±0.005%
F_2	Optional Clock Frequency		447.443		KHz	±0.005%
DC	Clock duty cycle	45	50	55	%	Optional Clock
t_r	Input clock pulse rise time	40		200	ns	10% to 90% of final level } Optional Clock
t_f	Input clock pulse fall time	40		200	ns	90% to 10% of final level } Optional Clock
Detected Frequencies Low Group			697		Hz	
			770		Hz	
			852		Hz	
			941		Hz	Bandwidth range:
Detected Frequencies High Group			1209		Hz	−1.9 to −3.2%
			1336		Hz	+2.0 to +3.3%
			1477		Hz	
			1633		Hz	
IDC	Input signal (FL or FH) duty cycle	30	50	70	%	
Outputs*						
$V_{OUT}(0)$	Logical "0" output voltage					$V_{GG} + R_L I_{sink}$
t_f(OUT)	Output fall time					$2.2\ R_L\ C_L$
$V_{OUT}(1)$	Logical "1" output voltage	V_{SS}-0.4			V	I_{SOURCE} = 2.0 mA
t_r(OUT)	Output rise time			4	μS	10% to 90% of final level (with 30 pF load)
Output Timing						
t_{SP}	Silence Period	9.4	10	10.6	ms	
t_R	Silence Pulsewidth	1.0	1.1	1.2	ms	
t_{DA1}	Data Acquisition Time Option 1	22		39	ms	
t_{DA2}	Data Acquisition Time Option 2	25		33	ms	
t_{AUD}	Audio Detection Time	1.5	5	8	ms	
t_H	Output Hold Set-up Time	10			μS	
t_{INH}	Chip Inhibit Pulsewidth	2			μS	
C_2	Clock		2		kHz	
C_{16}	Clock		16		kHz	±0.1 %
C_{32}	Clock		32		kHz	
t_{S1}	Strobe Pulsewidth Option 1	0		17	ms	
t_{S2}	Strobe Pulsewidth Option 2	0		8	ms	
Power						
P_{D1}	Power Dissipation (Dual Power Supply)			200	mW	V_{SS} = 5.25V; V_{GG} = -13V
P_{D2}	Power Dissipation (Single Power Supply)			180	mW	V_{SS} = 5.25V; $V_{GG} = V_{DD}$ = 0V

*For a full description of the output buffer capabilities, refer to the CRC 8030 Application Note.



21477-12

Figure 4. Timing Diagram

Touch-Tone® Matrix: Binary Outputs																
	1209				1336				1477				1633			
	D1	D2	D4	D8	D1	D2	D4	D8	D1	D2	D4	D8	D1	D2	D4	D8
697	1	0	0	0	0	1	0	0	1	1	0	0	1	0	1	1
770	0	0	1	0	1	0	1	0	0	1	1	0	0	1	1	1
852	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1
941	1	1	0	1	0	1	0	1	0	0	1	1	0	0	0	0

21477-13

Outputs (continued)

example, for digit 1, D1/697 Hz and 1209 Hz outputs will go low when detected. All other outputs remain high.

When the binary format is selected (BIN input is held low), the high-group outputs operate as described above. The low-group outputs (D1/697 Hz, D2/770 Hz, D4/852 Hz and D8/941 Hz) provide the binary coded information. These binary outputs are normally low and go high when a tone is detected. The outputs are defined by the above matrix:

- Strobe (ST) — This output indicates when the output data are valid. Validity is defined as detection within 39 ms or 33 ms depending upon the level of Strobe Control. For a description of the operation, refer to the inputs BIN and SC and figure 4.
- Silence Reset (SIL) — This output pulses to a low level when silence is detected. This occurs 9 ms after the interruption of a signal on either high- or low-group inputs. This output can be used to reset any external logic or to exercise the Output Hold option. The chip will reset itself after the Silence Reset output returns to a high level. Silence reset pulses at 10 ms intervals until a signal is present on either F_L or F_H.
- Audio Detect (AUD) — Audio is defined as energy carried by any frequency lower than 1680 Hz. AUD remains low when both FL and FH are low; AUD will go high if either FL or FH is toggling and will return to a low level as soon as Silence Reset returns from a low to a high level. This output may be used to control the admissible level in the Front-End circuitry (off-chip) or to give advance notice of a tone-pair.
- Test Output (X0) — When using the 3.579545 MHz crystal on-chip oscillator, X0 will display a 447.443 kHz clock. If the 447.443 kHz external oscillator option is utilized, X0 will display a 55.930 kHz clock. The X0 output frequency will be the X1 input frequency divided by 8.
- Clock Outputs (C2, C16, C32) — These outputs will generate 2 kHz, 16 kHz and 32 kHz clocks, respectively.

DTMF Receiver Design

The CRC 8030, in conjunction with a front-end analog filter/limiter, implements a complete DTMF receiver. Figure 2 illustrates this design. With this approach, a central-office-quality receiver with the following specification can be implemented:

- Input Dynamic Range . . . . . -26 dBm to +6 dBm
- Twist . . . . . -8 dB to +4 dB
- Valid Tone Tolerance . . . . . ±1.5%
- Invalid Tone Reject Limit . . . . . ±3.5%
- Tone Burst (minimum) . . . 40 ms ON, 11 ms OFF at 12 bursts per second

Inasmuch as the front-end filter is an essential part of the total receiver, its characteristics have a major impact on the performance of the system. For example, for high-quality central-office receivers, a more selective front-end filter is required. Conversely, low-noise environment keyphone systems will operate with a less stringent front-end filter design. In view of the differences in specifications for DTMF receivers, the front-end design must be tailored for the particular application. Several manufacturers have off-the-shelf hybrid products which meet these filtering requirements. For more details concerning these design considerations, refer to the Collins "Application Note — CRC 8030 Telephone DTMF Receiver".

For specialized applications, the CRC 8030 has several mask programmable features. The parameters that can be programmed include the bandwidth, detection time, strobe time, silence time, and output decode format. Contact Collins Applications Engineering for details.

Packaging and Ordering Information

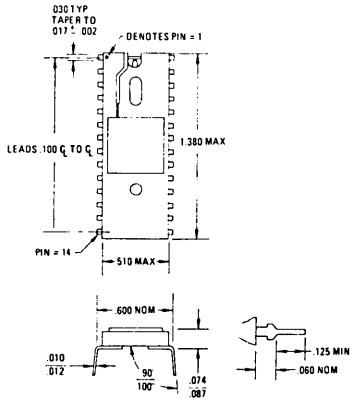
The DTMF Detector is available in a 28-pin, hermetically sealed ceramic dual-in-line package and in a 28-lead ceramic chip carrier (see pin assignments and package dimension diagrams). Order by type number.

CRC 8030-1-3 (ceramic DIP) 765-5795-001
CRC 8030-4-3 (ceramic carrier) . . . 765-5795-003

For further information on Rockwell MOS/LSI Standard Products, call your local Rockwell Sales office or:

MOS/LSI Marketing
Rockwell International
Microelectronic Devices
3310 Miraloma Avenue
Anaheim, California 92803
Telephone (714) 632-2558
TWX 910-591-1698

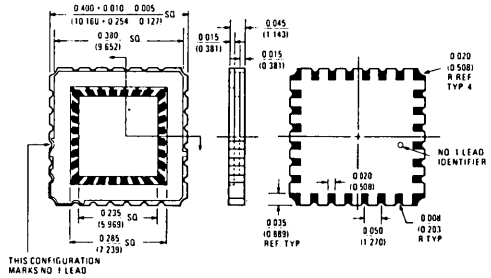
DTMF DETECTOR (CRC 8030-1-3)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{SS}	15	1209 HZ
2	1633 HZ	16	HLD
3	SIL	17	SC
4	INH	18	V_{DD}
5	C2	19	D4/852 HZ
6	C16	20	D8/941 HZ
7	C32	21	ST
8	X2	22	D2/770 HZ
9	V_{GG}	23	BIN
10	X1	24	FL
11	TE	25	FH
12	X0	26	D1/697 HZ
13	AUD	27	1477 HZ
14	1336 HZ	28	N16

21477-14

DTMF DETECTOR (CRC 8030-4-3)



PINS ARE READ COUNTERCLOCKWISE

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{SS}	15	1209 HZ
2	1633 HZ	16	HLD
3	SIL	17	SC
4	INH	18	V_{DD}
5	C2	19	D4/852 HZ
6	C16	20	D8/941 HZ
7	C32	21	ST
8	X2	22	D2/770 HZ
9	V_{GG}	23	BIN
10	X1	24	FL
11	TE	25	FH
12	X0	26	D1/697 HZ
13	AUD	27	1477 HZ
14	1336 HZ	28	N16

21477-15

NOTE: Collins MOS/LSI Products is now a part of Microelectronic Devices, Rockwell International.

TELECOM
DEVICES

DOCUMENT NO. R8040D
REV. 1, AUGUST 1979

PART NUMBER
R8040

Rockwell

MOS/LSI TELECOMMUNICATIONS DEVICES
DATA SHEET

T-1 TRI-PORT MEMORY

OVERVIEW

The Tri-Port Memory circuit is designed to function as an assembly point and temporary storage area for 8-bit T-1 data. It provides 64 8-bit locations of on-chip random access memory which can be accessed via external addresses or internal sequential addressing.

TRI-PORT MEMORY OPERATION

The Tri-Port Memory device accepts 8-bit parallel input data on lines A through H. This data is stored in an internal memory location that is selected by either random address lines R01 through R32 or by the device's Sequential Address Counter. Write Select signal WSEL determines the source of the address; in the logic 0 state, WSEL selects the random address, in the logic 1 state, WSEL selects the internal sequential address.

The state of Write Enable signal $\overline{WE}$ determines whether or not the data on lines A through H will be written into memory. Data will only be written into memory when $\overline{WE}$ goes low (to a logic 0 state) and the address inputs have stabilized.

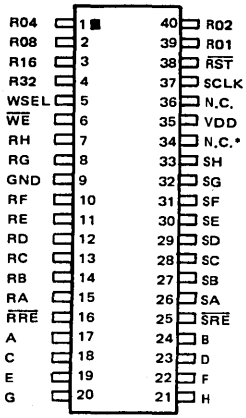
The on-chip, six-bit Sequential Address Counter is a binary counter that increments on each positive transition of Sequential Clock (SCLK). When the Counter attains binary 111111, the next positive transition on SCLK will clear it to binary 000000. The Counter will also be cleared unconditionally if Reset signal $\overline{RST}$ has been set to logic 0 when the positive transition of SCLK occurs.

The Sequential Read Enable signal, $\overline{SRE}$, enables sequentially-addressed read operations. If $\overline{SRE}$ is logic 0, the sequential accessed data outputs (SA through SH) will become valid within 430 ns after the next positive transition on SCLK. If $\overline{SRE}$ is logic 1, and 350 ns have elapsed since the positive transition of SCLK, the sequential accessed data outputs will become valid 80 ns after the negative transition of $\overline{SRE}$. The Sequential Read Data will cease to be valid within 100 ns after the positive transition of $\overline{SRE}$, or within 340 ns after the negative transition of $\overline{WE}$ (in the case of a same-location read/write cycle), or within 430 ns after the next positive transition of SCLK.

The Random Read Enable signal, $\overline{RRE}$, enables random-accessed read operations. If $\overline{RRE}$ is logic 0, the random accessed data outputs (RA through RH) will become valid within 380 ns after the random address lines have stabilized. If $\overline{RRE}$ is logic 1, and 300 ns have elapsed since the random address lines have stabilized, the random accessed data outputs will become valid 80 ns after the negative transition of $\overline{RRE}$. The random accessed data outputs cease to be valid after a positive transition of $\overline{RRE}$, or within 340 ns after the negative transition of $\overline{WE}$ (in the case of a same-location read/write cycle) or within 380 ns after the random address input lines change.

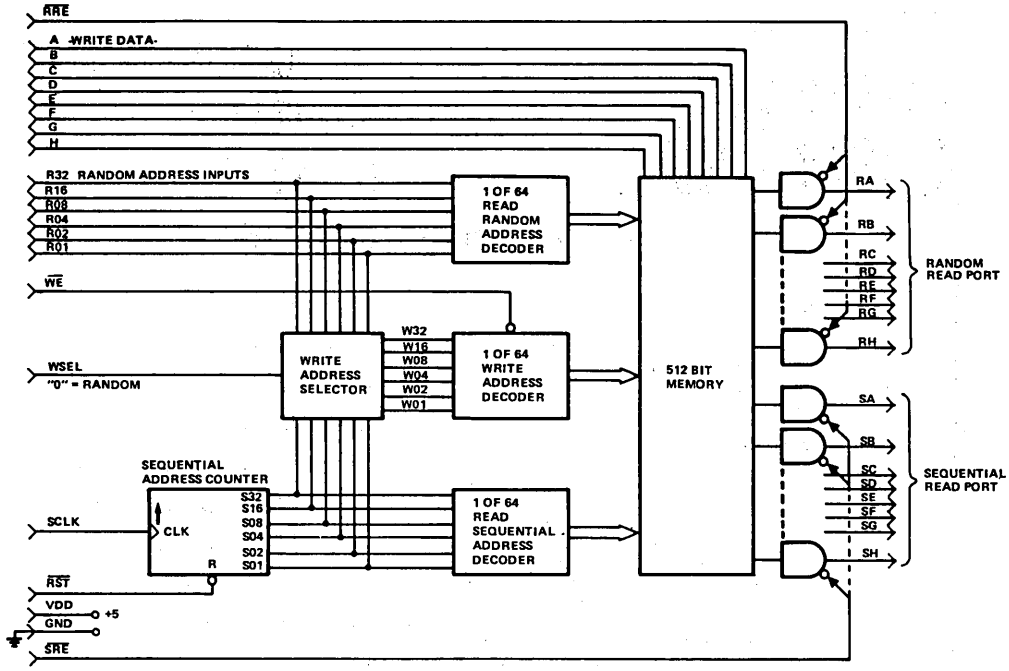
FEATURES

- 64 x 8 bit static memory
- Single +5V supply
- Two totally independent read ports
- Multiple Read access time <430 ns (worst case)
- Selectable random- or sequential-address Write operation
- On-chip sequential address counter
- Tri-state drivers, for chip-selectable bus operation
- 40-pin plastic dual in-line package
- LSTTL Schottky-compatible (12K Ω pullup, to drive CMOS)



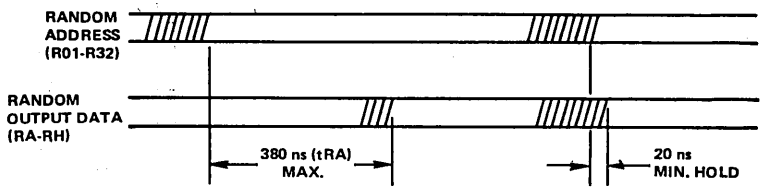
*PIN 34 HAS AN OUTPUT SIGNAL APPLICABLE ONLY TO ROCKWELL TESTING. MAKE NO CONNECTION TO THIS PIN.

Pin Configuration

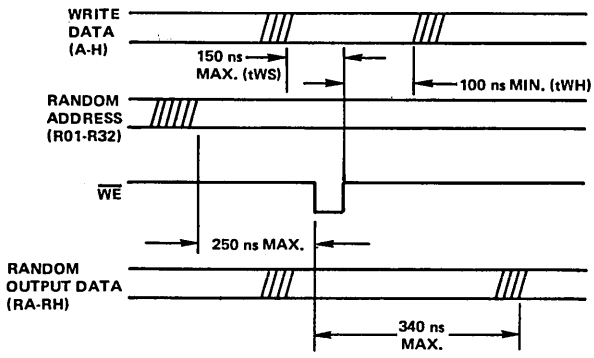


Tri-Port Memory Block Diagram

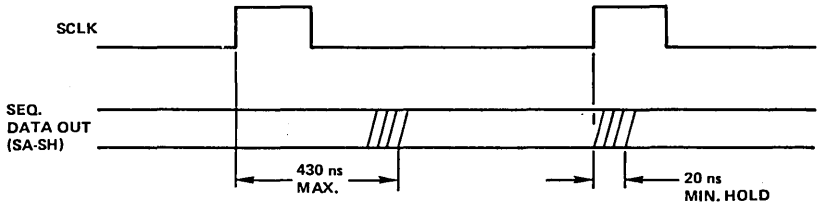
RANDOM READ



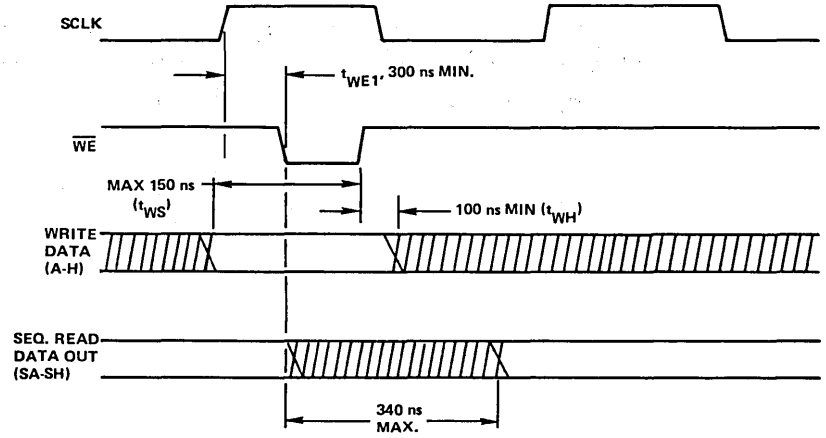
RANDOM WRITE



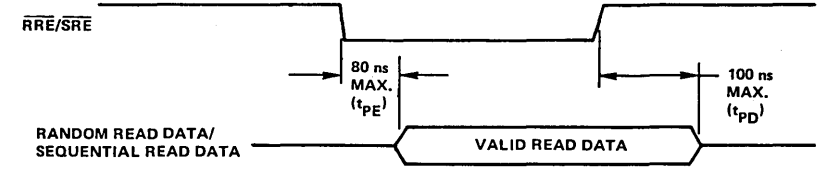
SEQUENTIAL READ



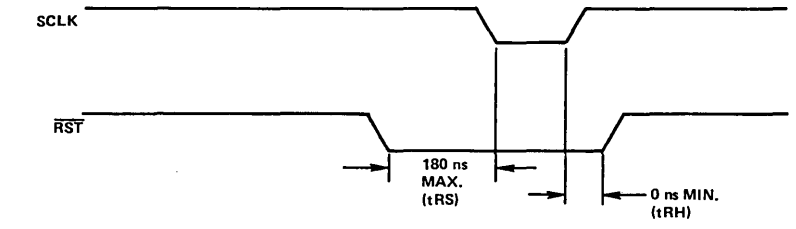
SEQUENTIAL WRITE



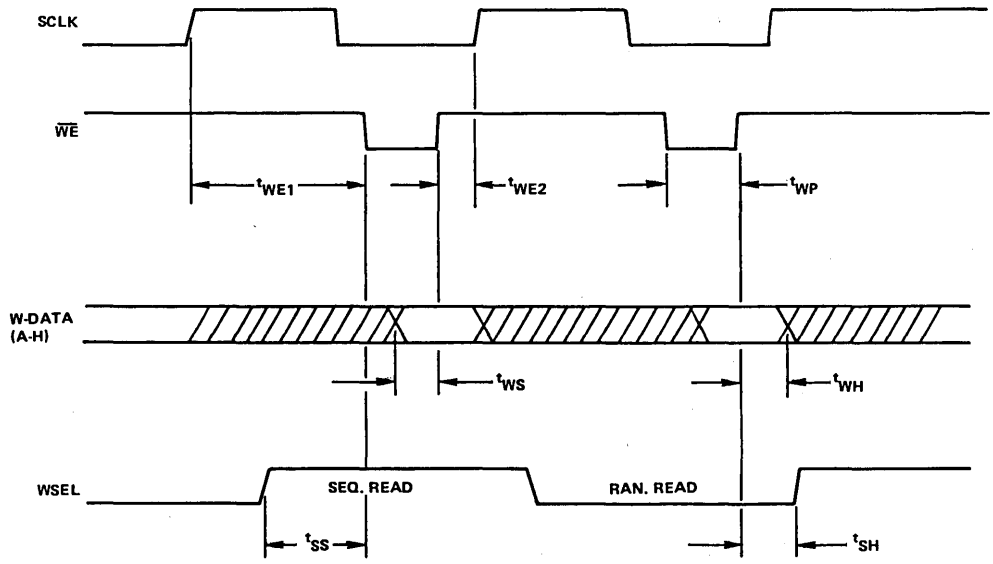
READ PORT ENABLES (t_{PE}/t_{PD})



SEQUENTIAL COUNTER RESET



WRITE ENABLE AND WRITE SELECT TIMING



Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Random Read Access Time	t_{RA}			380	ns
Sequential Read Access Time	t_{SA}			430	ns
Random Read Address Setup Time	t_{AS}			380	ns
Read Port Disable (to Hi Z)	t_{PD}			100	ns
Read Port Enable	t_{PE}			80	ns
$\overline{WE}$ Pulse Width	t_{WP}	170	300		ns
$\overline{WE}$ Pulse Delay	t_{WE1}	300			ns
$\overline{WE}$ Pulse Setup	t_{WE2}			0	ns
SCLK Pulse Width	t_{SP}	220	325		ns
SCLK Frequency	f		1.544		MHz
Write Data Setup Time	t_{WS}			150	ns
Write Data Hold Time	t_{WH}	100			ns
Write Select Setup Time	t_{SS}			280	ns
Write Select Hold Time	t_{SH}	0			ns
$\overline{RST}$ Setup Time	t_{RS}			180	ns
$\overline{RST}$ Hold Time	t_{RH}	0			ns

SPECIFICATIONS

Maximum Ratings

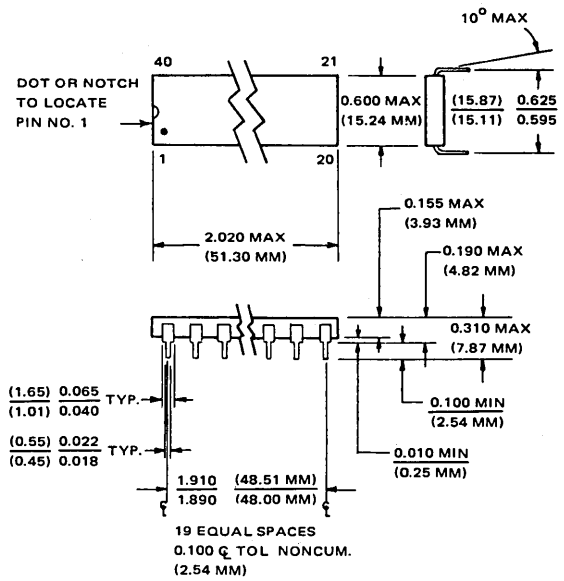
Rating	Symbol	Voltage	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature Range	T_{OP}	0 to 70	^{o}C
Storage Temperature Range	T_{STG}	-55 to +150	^{o}C

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

Electrical Characteristics

(V_{DD}= +5V ±5%, V_{SS}= 0V T_A=25°C)

Characteristic	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0		V
Input Logic "0" Voltage	V_{IL}		0.8	V
Output Logic "1" Voltage	V_{OH}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	-100		µA
Output Sink Current	I_{OL}	400		µA
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation (at 25°C)	P_{DSS}		300	mW



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

Packaging Diagram

SPECIFICATIONS

Maximum Ratings

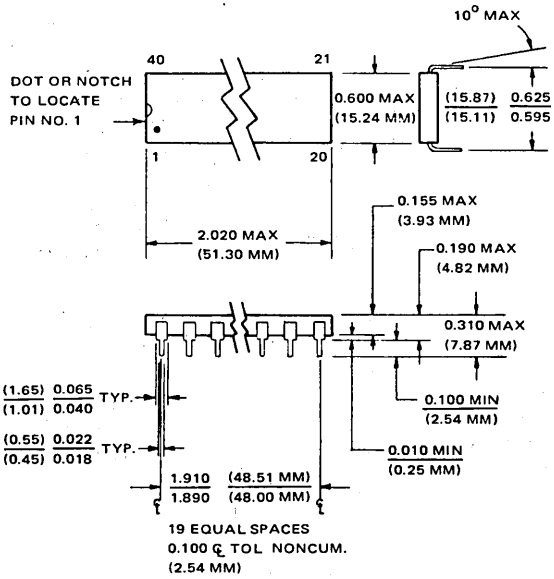
Rating	Symbol	Voltage	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature Range	T_{OP}	0 to 70	^{o}C
Storage Temperature Range	T_{STG}	-55 to +150	^{o}C

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

Electrical Characteristics

(V_{DD} = +5V ±5%, V_{SS} = 0V T_A=25°C)

Characteristic	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0		V
Input Logic "0" Voltage	V_{IL}		0.8	V
Output Logic "1" Voltage	V_{OH}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	-100		µA
Output Sink Current	I_{OL}	400		µA
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation (at 25°C)	P_{DSS}		300	mW



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

Packaging Diagram

DOCUMENT NO. R8050D
APRIL 1979

PART NUMBER
R8050

Rockwell

MOS/LSI TELECOMMUNICATIONS DEVICES
DATA SHEET

T-1 SERIAL TRANSMITTER

GENERAL DESCRIPTION

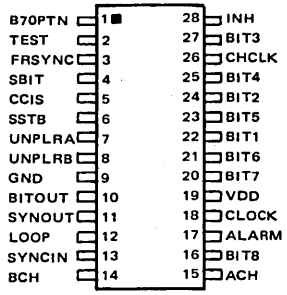
The Rockwell T-1 Serial Transmitter formats data to be serially transmitted according to T-1 D2 or T-1 D3 specifications, inserting framing and signalling bits along with 24 channels of 8-bit channel data. The T-1 Serial Transmitter also provides for alarm reporting via the Bit 2 inhibit method or, with minimal external logic, via the multiframe alignment signal (F_S) modification.

Figure 1 is a functional block diagram of the T-1 Serial Transmitter. The Mod 193 counter is driven by the clock at 1.544 MHz and is either synchronized to the driving system by input signal SYNCIN or provides synchronization via output signal SYNOUT. Input signal FRSYNC applies synchronization to a Mod 12 counter, which identifies the frame of the 12-frame multiframe being processed.

The input data register latches data during each bit period, when the 8th bit of a channel sample is being transmitted. The data selector outputs the proper sequence of bits, as controlled by a bit count and frame count.

The zero channel monitor function causes Bit 8 or Bit 7 (as selected by B7OPTN) to be transmitted as a "one" if the channel data sample is all "zeros" for any frame except signalling frame (Frame 6 or 12). Input INH provides a means to inhibit the zero channel monitor function.

Two types of transmit formats are provided, a binary output and a paired unipolar output. The unipolar pair provides a means to externally create a single bipolar output with minimal logic.



Pin Configuration

FEATURES

- Single 5V supply, low power Schottky TTL compatible
- Accepts 8 bits of parallel data as input
- Generates output as 193 bit serial data stream in T-1, D2 or T-1, D3 data format
- Provides a channel and frame timing signal.
- Provides alternate control for alarm reporting and signalling
- Provides automatic bit insertion for all zero channel samples.

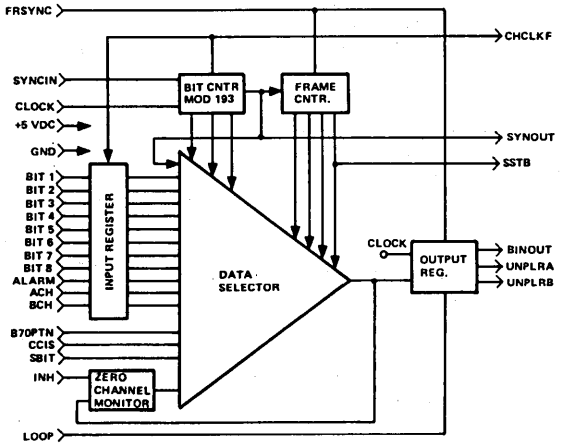


Figure 1. T-1 Serial Transmitter

T-1 SERIAL TRANSMITTER

TELECOM DEVICES

Specifications subject to change without notice

T-1 Transmitter Inputs

Any input ≤0.8V = logic 0, low. Any input ≥2.0V = logic 1, high. The transition from a low level to a high level is called a rising edge, while the converse is defined as a falling edge.

FRSYNC: Frame Synchronization

Frame sync allows the user to force the frame counter to the frame count of 1. (The first frame of a possible 12.) When high, FRSYNC directly sets the frame count to be frame 1. If FRSYNC does not return to zero before the rising edge of CLOCK, BINOUT, UNPLRA are transmitted high and UNPLRB is transmitted low. Refer to Figure 6 and Figure 7.

SYNCIN: Synchronization Input

Provides a means to directly reset the Mod 193 bit counter to a bit position corresponding to the first bit of channel 1. The high level causes the reset. The first bit of channel 1 will be transmitted following the release of SYNCIN.

TEST: Rockwell Device Test Input

Used only for Rockwell device testing. **Keep this input grounded.**

CLOCK: T-1 Clock

Maximum frequency = 1.6 MHz
Minimum pulse width = 275 ns
The T-1 bit period is bounded by the rising edges of this input.

INH: Inhibit Zero Channel Monitor

If INH is high, the zero channel monitor function is disabled, and Bits 7 and 8 are transmitted per corresponding inputs received. See Table 1.

For any frame except a signalling frame (Frame 6 or 12) Bit 8 or Bit 7 as selected by B7OPTN will be transmitted as a "one" if the channel input data is "zero" and INH is low.

BITS 1-8: Parallel Channel Data Inputs

Bit 1, the sign bit, will be serially transmitted first, followed by Bits 2 through 8. The falling edge of CHCLKF indicates input channel data has been clocked into the input register and always occurs during the transmission of the final bit (Bit 8) of each channel data sample.

ACH: "A" Channel Highway Signalling

ACH allows the user to transmit a one bit of signalling per channel as Bit 8 of each channel data sample in Frame 6 only. ACH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

BCH: "B" Channel Highway Signalling

BCH allows the user to transmit a one bit of signalling per channel as Bit 8 of each channel data sample in Frame 12 only. BCH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

S-BIT: Multiframe Signalling Bit

SBIT, in conjunction with CCIS, provides an alternate way to control the multiframe signalling bit (F_S) transmission. The S-Bit input is transmitted as the multiframe signalling bit (F_S) if CCIS is held high. Refer to Table 2.

ALARM: Local Alarm

Used for reporting alarm conditions. If the ALARM signal is high, Bit 2 (the most-significant bit) of every channel data sample of every frame is transmitted as a zero. This is commonly called remote alarm signalling. ALARM is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

LOOP: Loop Strap

Provided to aid testing of user applications. When enabled to a high level, LOOP forces the unipolar outputs to transmit alternating ones and zeros, regardless of input conditions. Refer to Figure 3.

CCIS: Common Channel Interoffice Signalling Strap

Provides optional control for transmitting an alternate multiframe (even-numbered frames) signalling pattern via the S-Bit input. Automatically programmed S-Bit (F_S) transmission following Table 2 is achieved by holding CCIS at a low level.

B7OPTN: Bit 7 Option

Provides Bit 7 as an alternate bit position for "one" stuffing, as programmed by the zero channel monitor function. Refer to Table 1.

VSS, VDD: Ground and Power

VDD = +5 ±0.5 Vdc
VSS = Ground, 0 Vdc

T-1 Transmitter Outputs

Low power TTL Schottky compatible. "1" ≥2.4 Vdc, "0" ≤0.4 Vdc, C_L, 25 pf.

SSTB: 4 kHz Signalling Channel Strobe

SSTB is the least-significant bit of the frame counter. Unless it is directly set by FRSYNC, SSTB will go high as each framing bit (F_T) is serially transmitted, and will return low as each multiframe alignment signal (F_S) is transmitted. Refer to Figure 2.

SYNOUT: Channel Sync Output

SYNOUT provides a means to synchronize to the internal bit counter (Mod 193). SYNOUT is high for one bit time, beginning just prior to the first data bit of a frame being serially transmitted. Refer to Figure 8.

CHCLKF: Channel Clock False

The falling edge of CHCLKF, occurring as Bit 8 of any channel is being serially transmitted, indicates input data has been clocked into the input register. With the exception of an extra bit period extending the low level duration at frame bit time, CHCLKF is a divide-by-eight of CLOCK. Refer to Figure 2.

BINOUT: Serial Data Output, Binary Formatted

BINOUT is the binary formatted serial conversion of the parallel input data. The programmed format of BINOUT follows Table 1 and 2.

BINOUT is synchronously transmitted as a high level if FRSYNC remains during the rising edge of CLOCK. Refer to Figure 6 and 7.

UNPLRA, UNPLRB: T-1 Serial Data Unipolar Outputs

Two paired unipolar outputs are provided for the purpose of creating a single serial data output transmission in bipolar format. The unipolar output register toggles for each "one" bit to be serially transmitted. UNPLRA and UNPLRB are transmitted as complements for "one" data bits and as low levels for "zero" data bits. See Figure 3.

The input signal loop, if high, forces the unipolar outputs to toggle every bit time, regardless of input data.

FRSYNC perturbs the current bits being transmitted by UNPLRA and UNPLRB. If FRSYNC remains high during the rising edge of CLOCK, UNPLRA will be transmitted as a high level and UNPLRB will be low. Refer to Figures 6 and 7.

Table 1. Serial Output Data Processing for Channel Sample Data (Not F_T or F_S)

BINOUT representing the serial data out will be a "1" if the below equations are true.

SERIAL DATA BIT TO BE TRANSMITTED (NEXT BINOUT)	FRAME = 6 OR FRAME = 12 AND CCIS = 0	CCIS = 1 AND ANY FRAME (2)
1st	Bit 1 = 1 (1)	Bit 1 = 1
2nd	B2 = 1 (see equation below)	B2 = 1
3rd	Bit 3 = 1	Bit 3 = 1
4th	Bit 4 = 1	Bit 4 = 1
5th	Bit 5 = 1	Bit 5 = 1
6th	Bit 6 = 1	Bit 6 = 1
7th	Bit 7 or B7X = 1	B7 = 1
8th	Bit 8 or B8X = 1	Sig = 1

(1) Terms Bit 1 thru Bit 8, ACH, BCH and ALARM are the clocked data from the parallel data input register. All other terms are either complex equation terms or unstored device inputs.

(2) If CCIS = 1 the T-1 transmitter can not uniquely identify Frame 6 or Frame 12.

$B2 = BIT2 \cdot \overline{ALARM}$

$B7 = BIT7 + \overline{SIG} \cdot \overline{BIT1} \cdot \overline{B2} \cdot \overline{BIT3} \cdot \overline{BIT4} \cdot \overline{BIT5} \cdot \overline{BIT6} \cdot \overline{INH}$

$Sig = ACH \cdot FRAME = 6 + BCH \cdot FRAME = 12$

$B7X = B7OPTN \cdot \overline{BIT1} \cdot \overline{B2} \cdot \overline{BIT3} \cdot \overline{BIT4} \cdot \overline{BIT5} \cdot \overline{BIT6} \cdot \overline{INH} \cdot \overline{BIT8}$

$B8X = \overline{B7OPTN} \cdot \overline{BIT1} \cdot \overline{B2} \cdot \overline{BIT3} \cdot \overline{BIT4} \cdot \overline{BIT5} \cdot \overline{BIT6} \cdot \overline{INH} \cdot \overline{BIT7}$

Table 2. Serial Output Data Processing for Framing Bits F_T, F_S

CURRENT FRAME NUMBER	REPRESENTED BIT	BINOUT BECOMES A "1" IF: (UNLESS STATED OTHERWISE)
1	F_S	SBIT and CCIS = 1
2	F_T	"0"
3	F_S	SBIT and CCIS = 1
4	F_T	"1"
5	F_S	SBIT = 1 or CCIS = 0
6	F_T	"0"
7	F_S	SBIT = 1 or CCIS = 0
8	F_T	"1"
9	F_S	SBIT = 1 or CCIS = 0
10	F_T	"0"
11	F_S	SBIT and CCIS = 1
12	F_T	"1"

F_T = Framing Bit

F_S = Multiframing Alignment Bit

NOTE: F_T Bit insertion is automatic and no optional control is provided.

Table 3. Input Timing

		MIN	MAX	UNITS
t_{1S}	Buffered Data Setup Time	450		ns
t_{1H}	Buffered Data Hold Time	0		ns
t_{2S}	Control Input Setup Time	400		ns
t_{2H}	Control Input Hold Time	20		ns
t_{3S}	Asynchronous Control Input Setup Time	350		ns
t_{3H}	Asynchronous Control Input Hold Time	20		ns
t_{4S}	SYNCIN Setup Time	200		ns
t_{4H}	SYNCIN Hold Time	20		ns
	SYNCIN Pulse Width	100		ns
t_{5S}	Frame Sync Setup Time (Return to Zero)	250		ns
t_{5H}	Frame Sync Hold Time (Return to Zero)	20		ns
	Frame Sync Pulse Width	200		ns
t_{5S}	Frame Sync Setup Time (Non-Return to Zero)	525		ns
t_{5H}	Frame Sync Hold Time (Non-Return to Zero)	20		ns

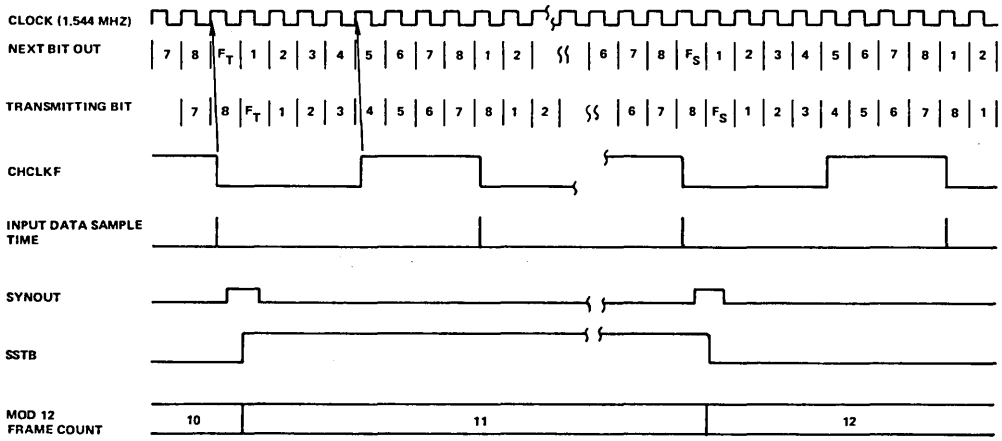


Figure 2. T-1 Transmitter Output Signal Relationship

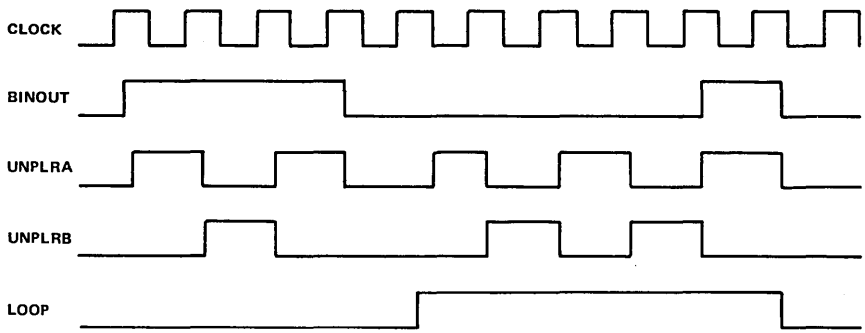


Figure 3. T-1 Transmitter Binary, Unipolar Format

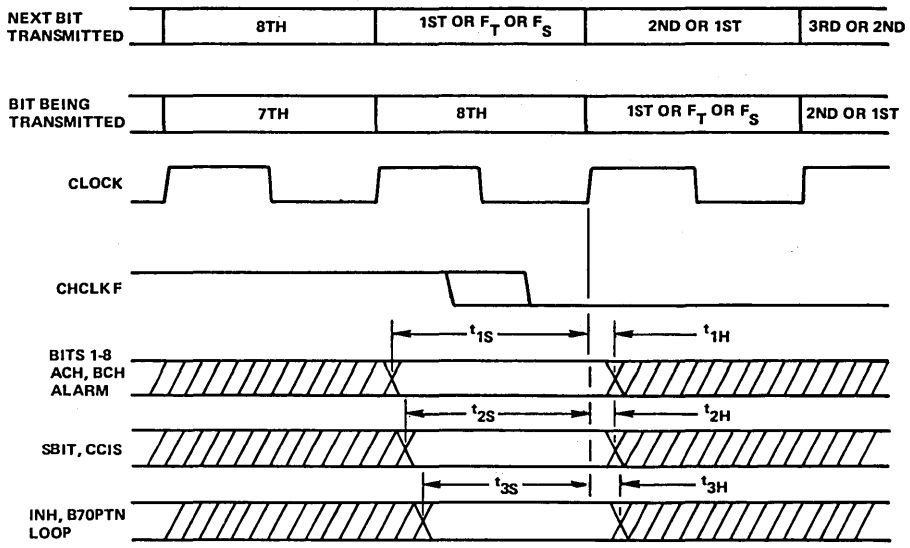


Figure 4. Input Timing Relationships

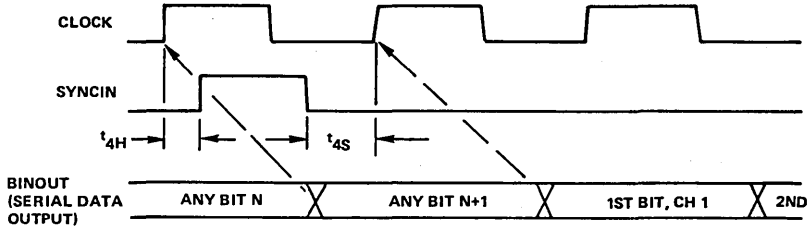


Figure 5. SYNCIN Timing Relationship

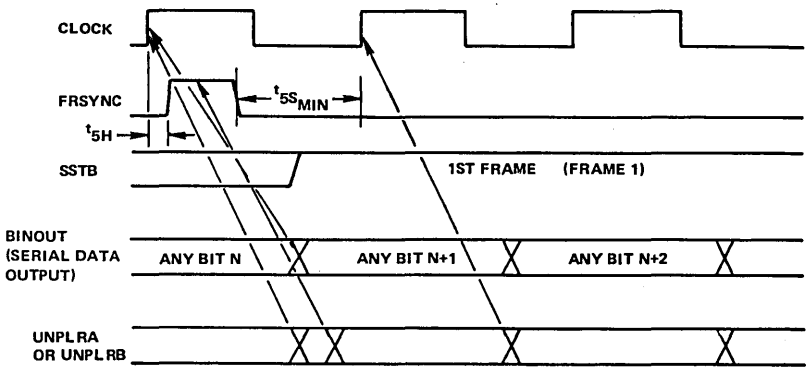


Figure 6. Return to Zero Frame Sync Application

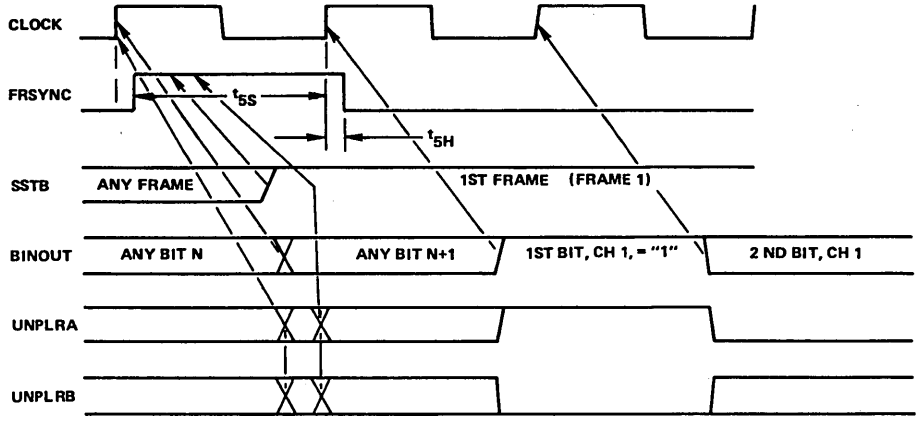


Figure 7. Non-Return to Zero Frame Sync Application

Table 4. Output Propagation Delay, Worst Case
(Measured from Rising Edge of Clock
Unless, Stated Otherwise)

OUTPUT	MAX DELAY	UNIT
SSTB	500	ns
SYNOUT	500	ns
Ref from Falling Edge of Clock		
CHCLKF	500	ns
BINOUT	500	ns
UNPLRA	500	ns
UNPLRB	500	ns

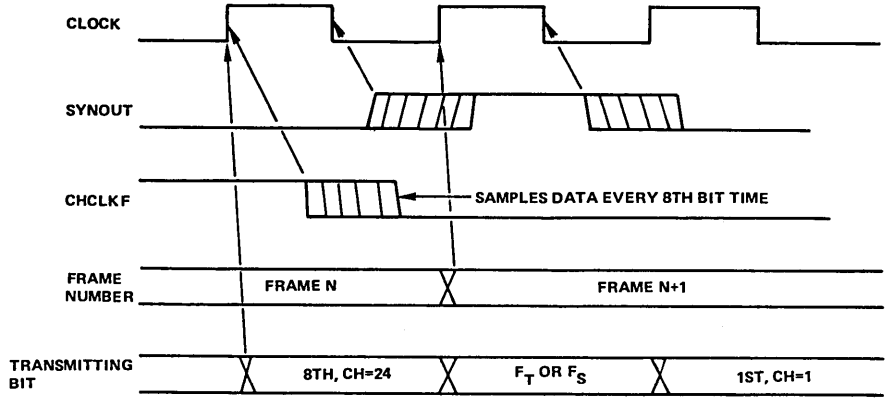


Figure 8. SYNOUT Signal Relationship

SPECIFICATIONS

Maximum Ratings

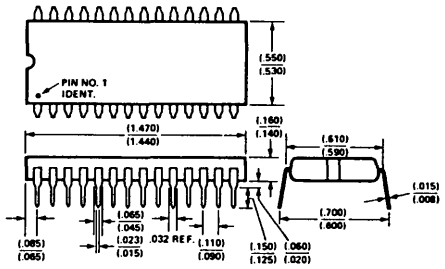
Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.5 to +5.5	Vdc
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics

(V_{DD} = 5.0 ±5%)

Characteristic	Symbol	Min	Max	Unit
Logical "1" Input Voltage	V_{OH}	2.0	V_{DD} + 0.3	V
Logical "0" Input Voltage	V_{IL}	-0.3	0.8	V
Logical "1" Output Voltage	V_{OH}	2.4	–	V
Logical "0" Output Voltage	V_{OL}	–	0.4	V
Output Source Current	I_{OH}	-100	–	μA
Output Sink Current	I_{OL}	400	–	μA
Capacitance Load	C	–	25	pF
Input Capacitance (any input)	C_{IN}	–	5	pF
Clock Frequency		–	1.6	MHz
Power Dissipation	P_D	–	250	mw



Packaging Diagram

Rockwell

MOS/LSI TELECOMMUNICATIONS DEVICES
DATA SHEET

T-1 SERIAL RECEIVER

DESCRIPTION

The Rockwell T-1 Receiver processes serial unipolar data of a T-1,D2 or T-1,D3 line from which data and a 1.544 MHz clock have been extracted.

Frame synchronization is accomplished by locating the frame bit (F_T) alternating every 386 bits. Loss of frame sync is indicated if a frame bit error occurs within two to four F-Bit frames since the previous frame bit error.

A loss of carrier is indicated if 31 consecutive bit times yield "zeros" at the input. Carrier loss is reset and frame sync search begins when a "one" reappears at the TDATA input.

Signaling bits, which occur 193 bit positions after a framing bit, are monitored to detect signaling frames. The signaling frame output, SIGFR, identifies the present frame as a signaling frame, and the S-Bit output at that time identifies which signaling frame is being processed.

Remote alarm reporting is detected by monitoring the second received bit of every channel sample of every frame. An alarm is indicated if 255 consecutive Bit 2 zeros are received.

Channel data bits are output by an eight-bit parallel register. The rising edge of the signal called channel clock (CHCLK) indicates the extraction of new output channel data.

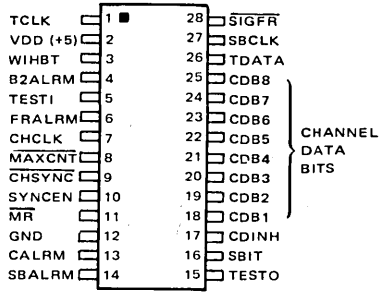
Several signals developed from a MOD 386 counter are provided to aid in the external processing and storage of channel data. Signals are provided to increment counters, synchronize counters, strobe data into memories, etc.

The Rockwell T-1 Receiver chip operates on a single 5 volt supply and directly interfaces to the low power TTL Schottky logic family. The Receiver is packaged in a 28 pin dual in-line (DIP).

Timing relationships are given in figures 3 through 5.

FEATURES

- Synchronizes serial T-1, D2 or T-1, D3 signals in less than 5 ms.
- Extracts 8-bit parallel channel data
- Provides timing signals to capture and synchronize channel and frame information
- Monitors and detects
  - Errors in signaling bit pattern
  - Loss of frame sync
  - Loss of carrier
  - Remote alarm reporting
- Single 5V supply
- LSTTL Schottky compatible



Pin Configuration

ORDERING INFORMATION

The T-1 Serial Receiver is available in two versions. With the standard commercial version, R8060, data will be stable within 900 ns after the bit clock. With the selected version, R8060A, data will be available within 600 ns after the bit clock.

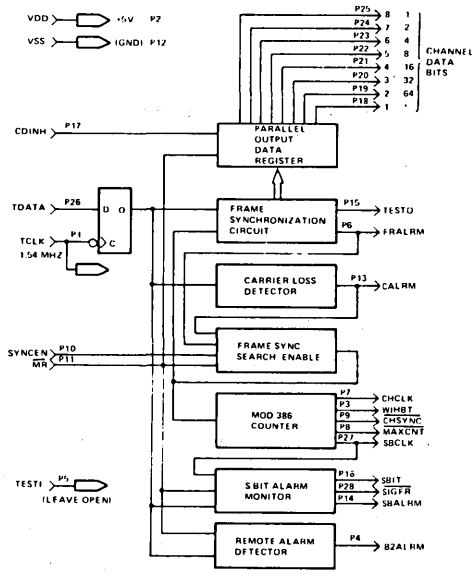


Figure 1. R8060 Block Diagram

Specifications subject to change without notice
Document No. R8060D
Rev. 2, May 1981

T-1 RECEIVER INPUTS

Any input ≤0.8V = LOGIC 0, LOW, ZERO. Any input ≥2.0V = LOGIC 1, HIGH, ONE. A transition from a low level to a high level is called a rising edge, while the converse is true for the falling edge.

TDATA: UNIPOLAR T-1-D2, T-1-D3 SERIAL DATA INPUT

Unipolar T-1 Data is clocked in on the falling edge of TCLK. Thereafter, TDATA is processed on the rising edge of TCLK. TDATA must be stable 100 ns before and remain stable 100 ns after the falling edge of TCLK.

TCLK: T-1 CLOCK

Typical clock frequency is 1.544 MHz. Maximum clock frequency is 1.85 MHz. The T-1 bit period is bounded by the rising edges of TCLK.

SYNCEN: FRAME SYNCHRONIZATION ENABLE

Provides a means to disable the automatic resync search initiated by a FRAME ALARM condition. If the SYNCEN signal is low, the synchronization function is inhibited and remains inhibited until SYNCEN transitions high. SYNCEN must be stable 200 ns before the rising edge of FRALRM, in order to inhibit the synchronization function.

MR: MASTER RESET

Master Reset, when low, performs an initialization clear of the T-1 Receiver; SBALRM and CALRM are reset to low levels while FRALRM, CHCLK, WIHBT and CHSYNC are set to high levels. Frame synchronization search begins on the rising edge of $\overline{MR}$ provided that SYNCEN signal has been high for 200 ns. Minimum pulse width is one T-1 clock period.

CDINH: CHANNEL DATA INHIBIT

Provides a means to disable channel data bit outputs. When at a high level, CDINH forces channel data Bits 1 through 7 high. Bit 8, the least significant channel data bit, is not controlled by CDINH.

TESTI: ROCKWELL DEVICE TEST INPUT

Used only for Rockwell device testing, no connection to TESTI is required for normal operation.

VSS, VDD: GROUND AND POWER

VDD = +5.0 ± 0.25 VDC
VSS = Ground, 0 VDC

T-1 RECEIVER OUTPUTS

Low Power TTL Schottky – compatible
"1" ≥ 2.4 Vdc; "0" ≤ 0.4 Vdc
CMOS – 12 KΩ pullup to VDD required.

CDB (1-8): CHANNEL DATA BIT 1 THROUGH 8

Bit 1 is the sign bit, Bit 2 is the most significant bit and Bit 8 is the least significant bit. If CDINH is low, new parallel channel data becomes valid within 200 ns after the rising edge of CHCLK and remains valid until the next rising edge of CHCLK. If CDINH is high, channel data Bits 1 through 7 are forced to a high level. Bit 8, the least significant bit, is not controlled by CDINH. Channel data Bits 1 through 7 are enabled or disabled within 300 ns (R8060) or 150 ns (R8060A) by CDINH. Refer to Figures 3 through 5.

CHCLK – CHANNEL CLOCK

The rising edge of CHCLK indicates a change of parallel output channel data. CHCLK is four TCLKS high then four TCLKS low except for when an "F" or "S" bit is received. Then CHCLK stretches to five TCLKS high and four TCLKS low. Refer to Figures 3 and 4.

$\overline{CHSYNC}$: CHANNEL SYNC

Channel Sync occurs one time in a 24 channel period, making it suitable for synchronizing external counters to the T-1 Frame rate. $\overline{CHSYNC}$ goes low one TCLK period before the falling edge of CHCLK at channel 24 date sample time. $\overline{CHSYNC}$ returns high 1 TCLK period after the next rising edge of CHCLK. Refer to Figures 3 through 5.

TESTO: ROCKWELL DEVICE TEST OUTPUT

Designed to aid in Rockwell device testing. No connection required for normal operation.

WIHBT: WRITE INHIBIT

WIHBT covers the parallel channel data transition period. WIHBT is suitable for clocking or strobing channel data into external memories. WIHBT is high for two TCLK periods, beginning one TCLK period before the rising edge of CHCLK. Refer to Figures 3 and 4.

$\overline{MAXCNT}$: MAXIMUM COUNT OF 386 MODULUS

$\overline{MAXCNT}$ is low for one TCLK period, marking the completion of a two-frame period corresponding to the expected receipt of an F-bit at the TDATA input. Refer to Figures 4 and 5.

SBCLK: S-BIT CLOCK

SBCLK will be high during the S-Bit frame and low during the F-bit frame. The transitions will occur within 300 ns after the rising edge of TCLK as channel 24 data is being transferred to the parallel channel outputs. Refer to Figures 3 through 5.

S-BIT: SIGNALING BIT OUTPUT

The S-Bit output monitors the previous S-Bit received which occurred two frames before the receipt of the current S-Bit. An S-Bit output transition occurs one TCLK period after the rising edge of SBCLK.

During a signaling frame (SIGFR is low), frame 6 or "A" highway signaling is identified by S-Bit output being low. If S-Bit is high during a signaling frame, frame 12 or "B" highway signaling is identified. Refer to Figures 3 through 5.

$\overline{SIGFR}$: SIGNALING FRAME

$\overline{SIGFR}$ identifies frame 6 or 12 when low. If the sequence of five consecutive received S-Bits is either 0111X or 1X001 (left to right, as received), $\overline{SIGFR}$ shall go low after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time. $\overline{SIGFR}$ returns high one frame later (193 bits). Refer to Figures 3 through 5.

SBALRM: S-BIT ALARM

SBALRM goes high if the sequence of five S-Bits received contains four consecutive ones (01111), and remains high until three consecutive "zero" bits are preceded and followed by a "one" S-Bit (10001). The actual transition of SBALRM output occurs after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time.

B2ALRM: BIT 2 ALARM

B2ALRM goes high, detecting a remote alarm condition, if 255 consecutive channel data samples are received with Bit 2 low. B2ALRM returns low upon the receipt of any channel sample with Bit 2 high.

CALRM: CARRIER LOSS ALARM

A carrier loss is detected and CALRM is set high if 31 consecutive low level TDATA bits are received. CALRM is reset low, FRALRM is set high and frame sync search begins when the first TDATA high level is received.

FRALRM: FRAME ERROR ALARM

FRALRM detects an out-of-frame condition. FRALRM goes high if:

A) The framing synchronization function is in progress.
B) Within 250 ns after the falling edge of MR.
C) An F-Bit is received which is not the inverse of the last F-Bit and the same condition also occurred two or three or four F-Bit frames earlier.
D) Within 250 ns after the falling edge of CALRM, (CALRM being reset by high level TDATA bit).

FRALRM goes low upon completion of the synchronization function or within 250 ns after the rising edge of CALRM. (Carrier loss condition during frame synchronization function).

OUTPUT CLOCK SIGNALS DURING FRAME SYNCHRONIZATION FUNCTION

Following the Declaration of Frame Sync loss (FRALRM goes high). output signals will continue normally for a two-frame period with the exception of CHSYNC, which has the above mentioned second frame sync pulse inhibited. Following the two-frame period CHCLK, CHSYNC, and WIHBT are held high until frame sync has been located, as indicated by the falling edge of FRALRM. With typical data patterns, frame synchronization takes less than five milliseconds. See Figure 2.

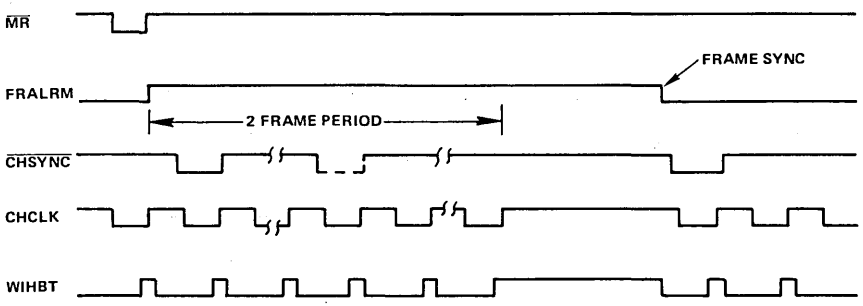


Figure 2. Signal Relationship During Frame Alarm and Search for Resynchronization

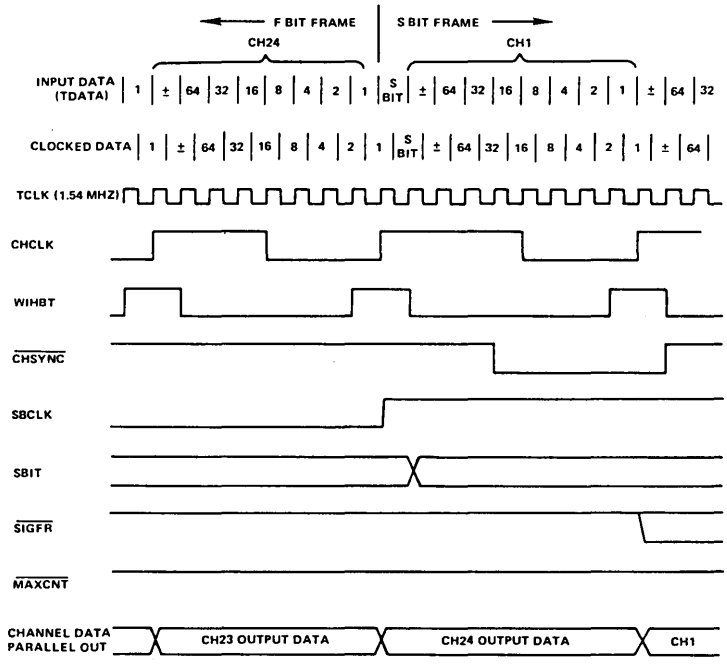


Figure 3. Signal Relationships at Beginning of F_S Frame (S-BIT)

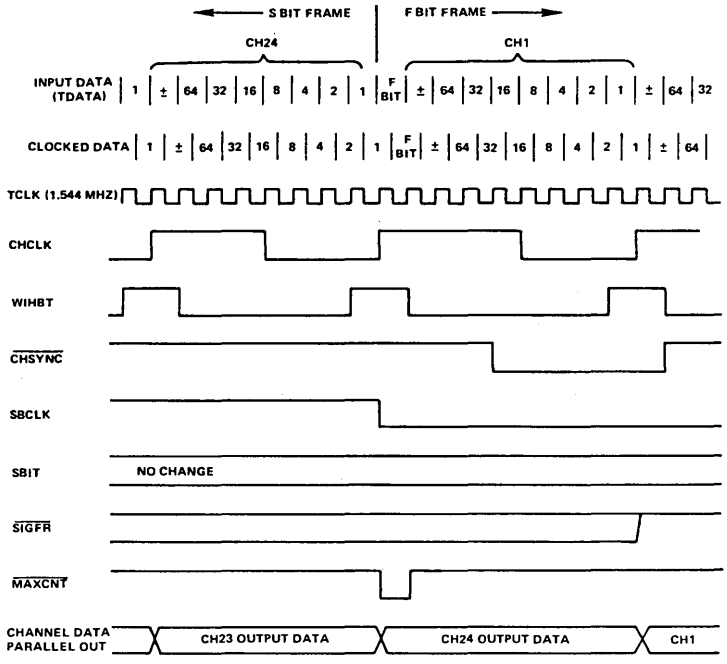
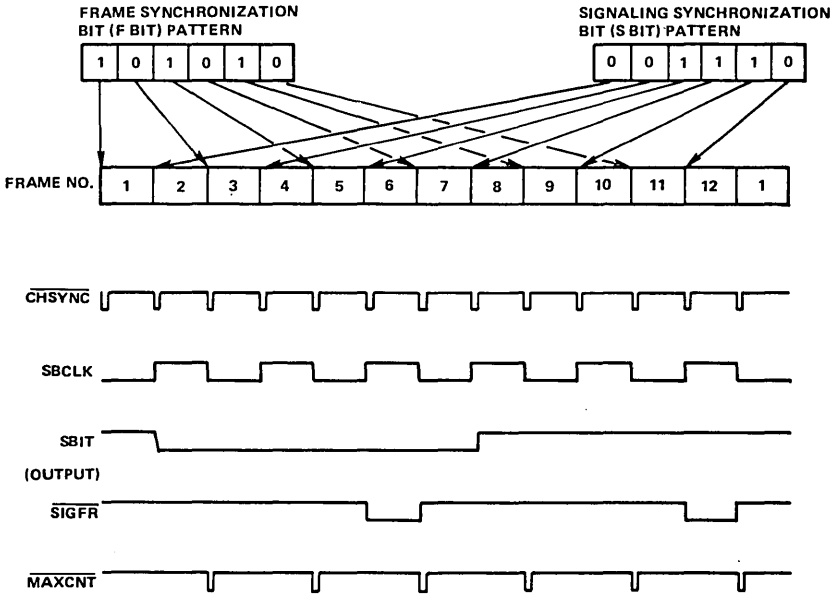


Figure 4. Signal Relationships at Beginning of F_T Frame (F-BIT)



FRAME = 24 TIME SLOTS = 193 BITS = 125μS
TIME SLOT = 5.18μS ONE BIT = 648 NS
MULTIFRAME = 12 FRAMES = 1.5 MS.

F BIT (F_T) FRAME ALIGNMENT SIGNAL
(ODD-NUMBERED FRAMES)

FRAME	FIRST BIT
1	1
3	0
5	1
7	0
9	1
11	0

S BIT (F_S) MULTIFRAME ALIGNMENT SIGNAL
(EVEN-NUMBERED FRAMES)

FRAME	FIRST BIT
2	0
4	0
6	1
8	1
10	1
12	0

Figure 5. Multiframe Signal Relationships

Table 1. Output Propagation Delay Worst Case, From Rising Edge to TCLK

OUTPUT	MAX DELAY (NS)
CHCLK	300
$\overline{\text{CHSYNC}}$	300
WIHBT	300
$\overline{\text{MAXCNT}}$	300
SBCLK	300
SBIT	400
$\overline{\text{SIGFR}}$	475
SBALRM	475
B2ALRM	450
CALRM	300
FRALRM	900 (R8060) 600 (R8060A)
CDB (1-8)	400

SPECIFICATIONS

Maximum Ratings

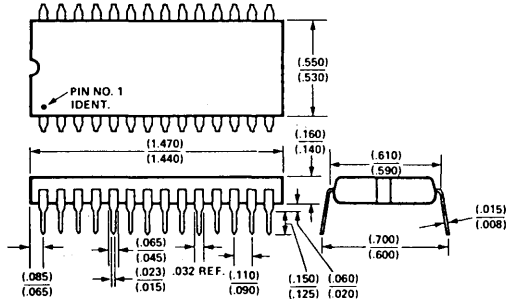
Rating	Symbol	Voltage	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature Range	T_{OP}	0 to 70	^{o}C
Storage Temperature Range	T_{STG}	-55 to +150	^{o}C

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

Electrical Characteristics

(V_{DD} = +5V ±5%, T_A = 25°C)

Characteristic	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Logic "0" Voltage	V_{IL}	-0.3	0.8	V
Output Logic "1" Voltage	V_{OH}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	-100		μA
Output Sink Current	I_{OL}	400		μA
Clock Frequency	T_{CLK}		1.85	MHz
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation	P_{DSS}		550	mW

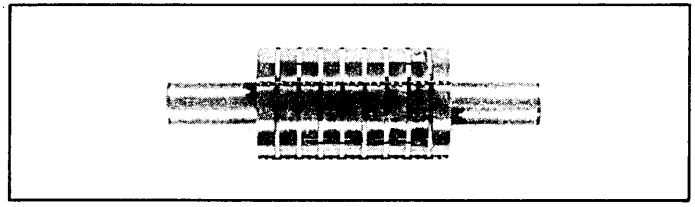


Packaging Diagram

FILTER PRODUCTS

FILTER
PRODUCTS

Rockwell-Collins Disc-Wire Mechanical Filters



Rockwell

FILTER PRODUCTS

Table of Contents

Rockwell-Collins Disc-Wire Mechanical Filters

1.0 Introduction

Disc-wire mechanical filters consist of metal disc resonators that are coupled together by wires. As shown in figure 1A, three basic elements comprise the filter structure: (1) magnetostrictive or piezoelectric transducers, used for converting electrical signals into mechanical vibrations; (2) high Q, mechanically resonant discs; and (3) disc coupling wires.

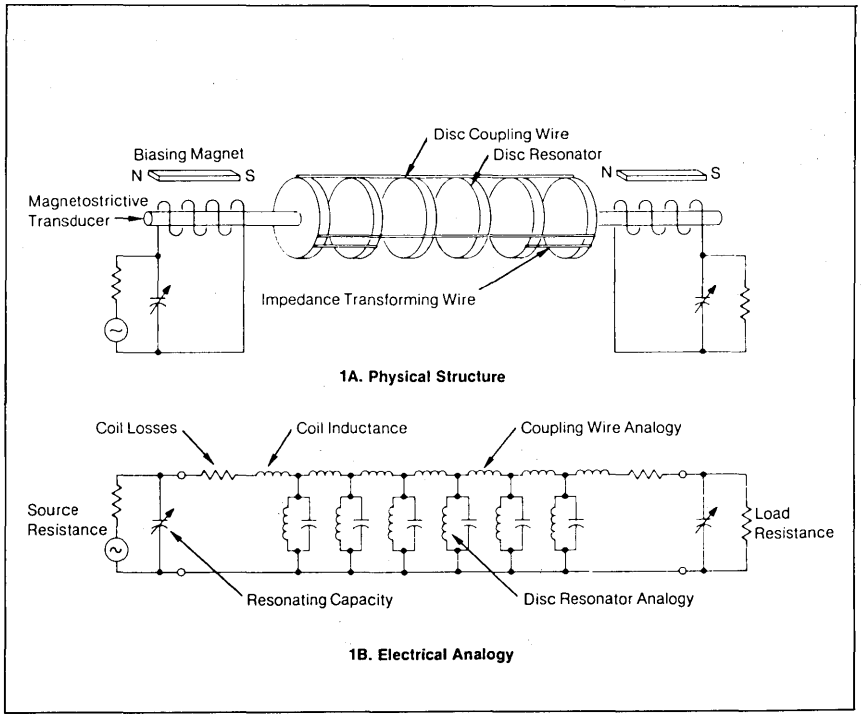


Figure 1. Disc-Wire Mechanical Filter Analogy

1.1 Filters Using Magnetostrictive Transducers

When an electrical signal is applied to the input coil of a magnetostrictive transducer (figure 1A), an alternating magnetic field is produced. This field then passes through the magnetostrictive rod that is attached to the first disc. When properly biased, the rod will vibrate at the frequency of the impressed signal. This is due to dimensional changes of magnetostrictive material that occur when being subjected to a magnetic field. The vibrating rod drives the first disc which, by means of the connecting coupling wires, drives the next disc. Each successive disc is then driven by the preceding disc until the signal reaches the output transducer. Strains developed in the output magnetostrictive rod produce an alternating magnetic field which, in turn, induces a voltage across the output coil.

1.2 Filters Using Piezoelectric Transducers

These filters operate in a manner similar to those described above, but a piezoelectric rod is used instead of the coil, biasing magnet and magnetostrictive rod shown in figure 1A. The coil inductance and resonating capacitance shown in figure 1B are replaced by the transducer static capacitance and resonating inductance, respectively. When a voltage is applied across the input piezoelectric transducer, an alternating electric field is produced, causing it to vibrate. The vibrations are transmitted through the disc-wire assembly in the same manner as described in paragraph 1.1, and are converted to a voltage at the filter output. In addition to converting energy from one form to another, the transducers also reflect the source and load resistances into the mechanical circuit. The reflected impedances provide a termination for the filter.

2.0 DESIGN CONSIDERATIONS

The disc resonators are made from a specially processed nickel-iron-chromium-titanium alloy. The constant-modulus characteristic of this material minimizes frequency shifts with changes in temperature. Figure 1B shows that the filter center frequency is determined by the disc resonator frequencies.

Several considerations are important in choosing the physical configurations of disc resonators and the mechanical coupling for a particular filter.

2.1 Disc Resonators

It must first be determined which mode of vibration is to be used. The two modes of vibration that are generally used in Rockwell-Collins filters are both flexure modes. The discs flex symmetrically about their center, similar to the vibration of a drum head. Both vibration modes use a nodal circle, or circles, which are not coincident with the edge of the disc. A mode with a single-nodal circle is generally used at frequencies of 200 kHz or lower, whereas a mode with 2-nodal circles is used up to 500 kHz. Figure 2 represents a mode with 2-nodal circles. The frequency of a disc resonator is directly proportional to thickness and inversely proportional to the square of the diameter.

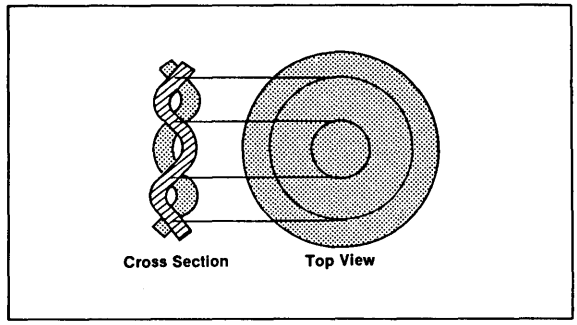


Figure 2. Vibration Mode Using 2-Nodal Circles

Other normal modes of vibration occur near the frequency region of interest, most of them having nodal diameters. The primary reason for attaching transducers at the centers of the first and last discs in a filter is to suppress these vibrations. Figure 3 illustrates four basic configurations of transducers used for this purpose.

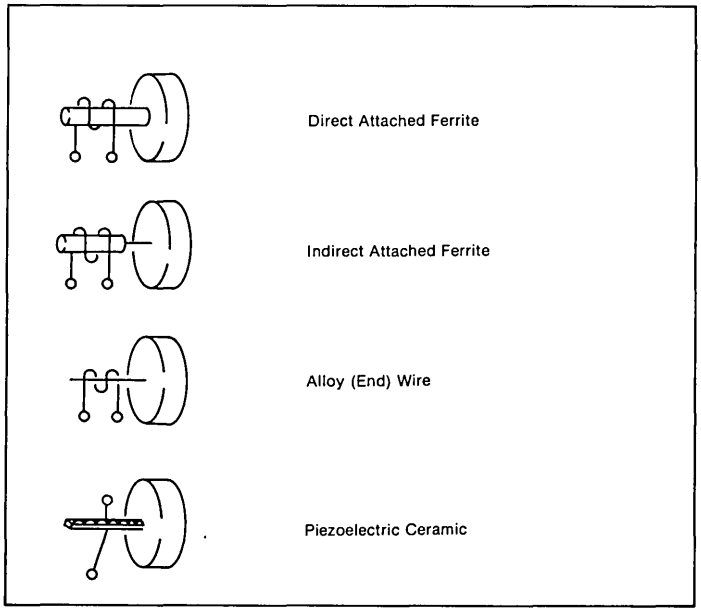


Figure 3. Transducer Configurations

2.2 Mechanical Coupling

The coupling inductors shown in figure 1B represent the wires which couple the disc resonators together and also act as their physical support. Varying the mechanical coupling between the discs, in effect making the coupling wires larger or smaller, varies the filter bandwidth. Since the bandwidth varies as a function of the approximate total cross-sectional area of the coupling wires, it can be increased either by using larger diameter wires or a greater number of coupling wires. It should also be noted that the physical structure becomes weaker as the filter bandwidth is reduced, assuming a fixed coupling wire configuration is used. This is one of the reasons why disc-wire filters are built using three basic coupling wire configurations. See figure 4.

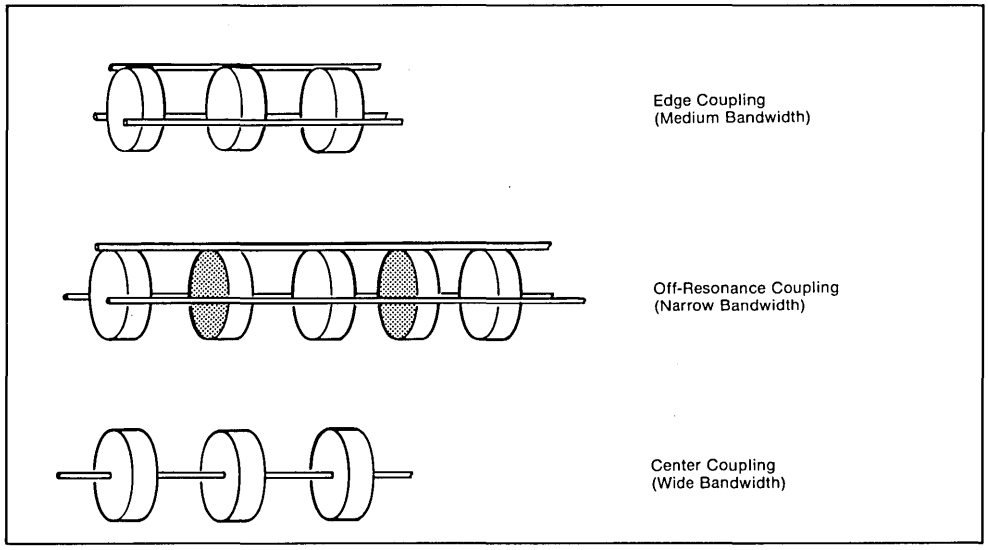


Figure 4. Disc Coupling Techniques.

Notably the least obvious of the three configurations shown in figure 4 is "off-resonance coupling", used in narrow bandwidth filters. In this scheme each alternate disc, shown shaded, is tuned so that its resonant frequency is higher than the filter passband region. Since the off-resonance disc is a shunt tank circuit, in the bandpass region in the filter (below the resonant frequency of the disc), it appears as a shunt inductance. This results in a "tee" of coupling inductors between the shaded discs. The net result produces a narrow bandwidth filter with coupling wires significantly larger in diameter than could be used without the "off resonance" discs.

3.0 Practical Design Limits

An analysis of all design considerations outlined in Section 2.0, results in definition of a set of design limits. The center frequency vs percent bandwidth is plotted in figure 5. The horizontal axis is filter center frequency and the vertical axis is filter bandwidth expressed as a percentage of center frequency. Practical limits within which mechanical filters can be built are represented in figure 5 as the shaded area. Special filters outside of these limits have been built, however, they are very costly.

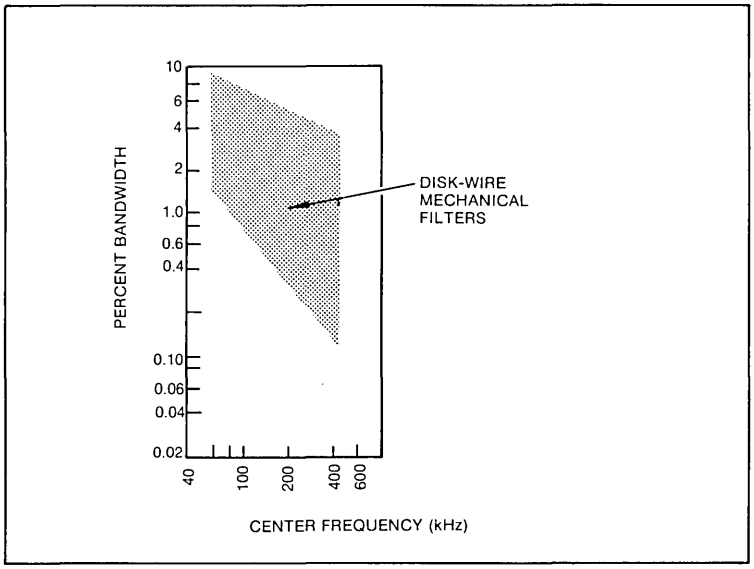


Figure 5. Center Frequency vs Bandwidth.

Most disc-wire filters approximate a 0.1 dB Chebyshev characteristic and exhibit a monotonic response. However, by bridging one or more discs with a coupling wire of proper dimension, it is possible to achieve a cancellation of signals at the output of the mechanical filter. This results in attenuation poles either in the upper or in the lower filter stopbands, or in both. Filters using these attenuation poles provide steeper skirt selectivity with fewer disc resonators than filters without the poles. This is important in applications where differential or absolute delays in the passband are of concern. See figure 6 for an attenuation comparison for filters having different numbers of disc resonators.

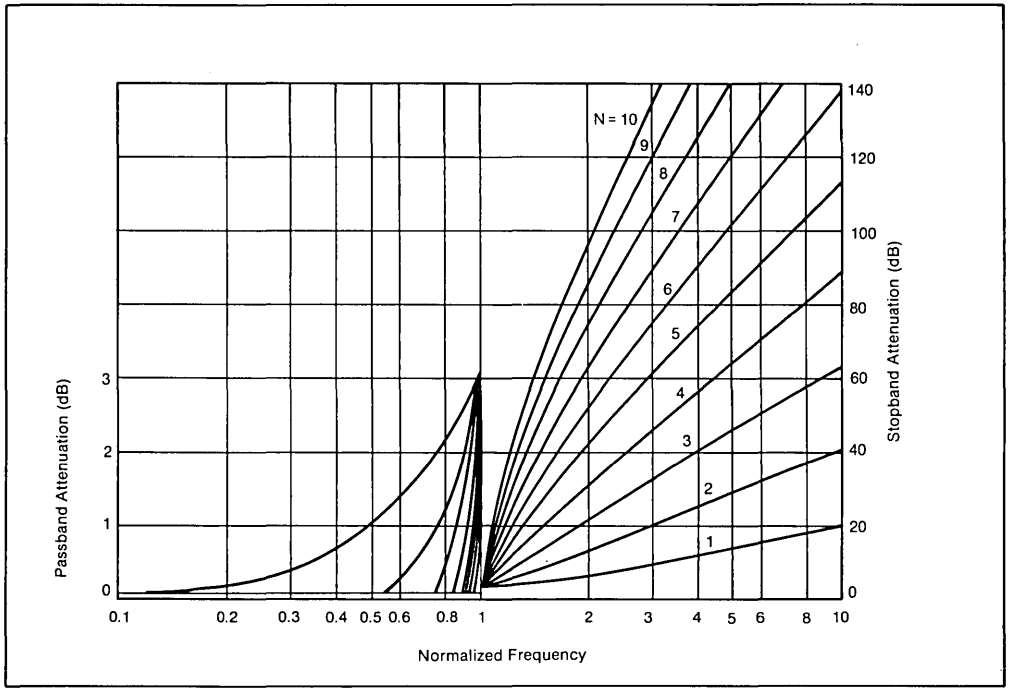


Figure 6. Attenuation Characteristics for Chebyshev Filter with 0.1 dB Ripple.

4.0 Enclosure Styles

Enclosure styles and outline dimensions for six different packages are shown in figure 7. Case styles "YA", "V" and "Y" are hermetically-sealed metal cases and are therefore the most expensive. These cases are recommended for stringent military applications, particularly where high humidity environments exist. The other styles shown in figure 7 are plastic cases that are suitable for most commercial applications but have also been used successfully in certain military applications. Case style "HS" is the least expensive and can be used in many applications for filters in the frequency range of 450-500 kHz. Whereas in most plastic enclosures the base is bonded to the cover with epoxy, the "HS" enclosure uses heat-staking. With this method no attempt is made to effect a moisture seal. However, this enclosure is suitable for many commercial environments, as the filter itself is not permanently changed by moisture.

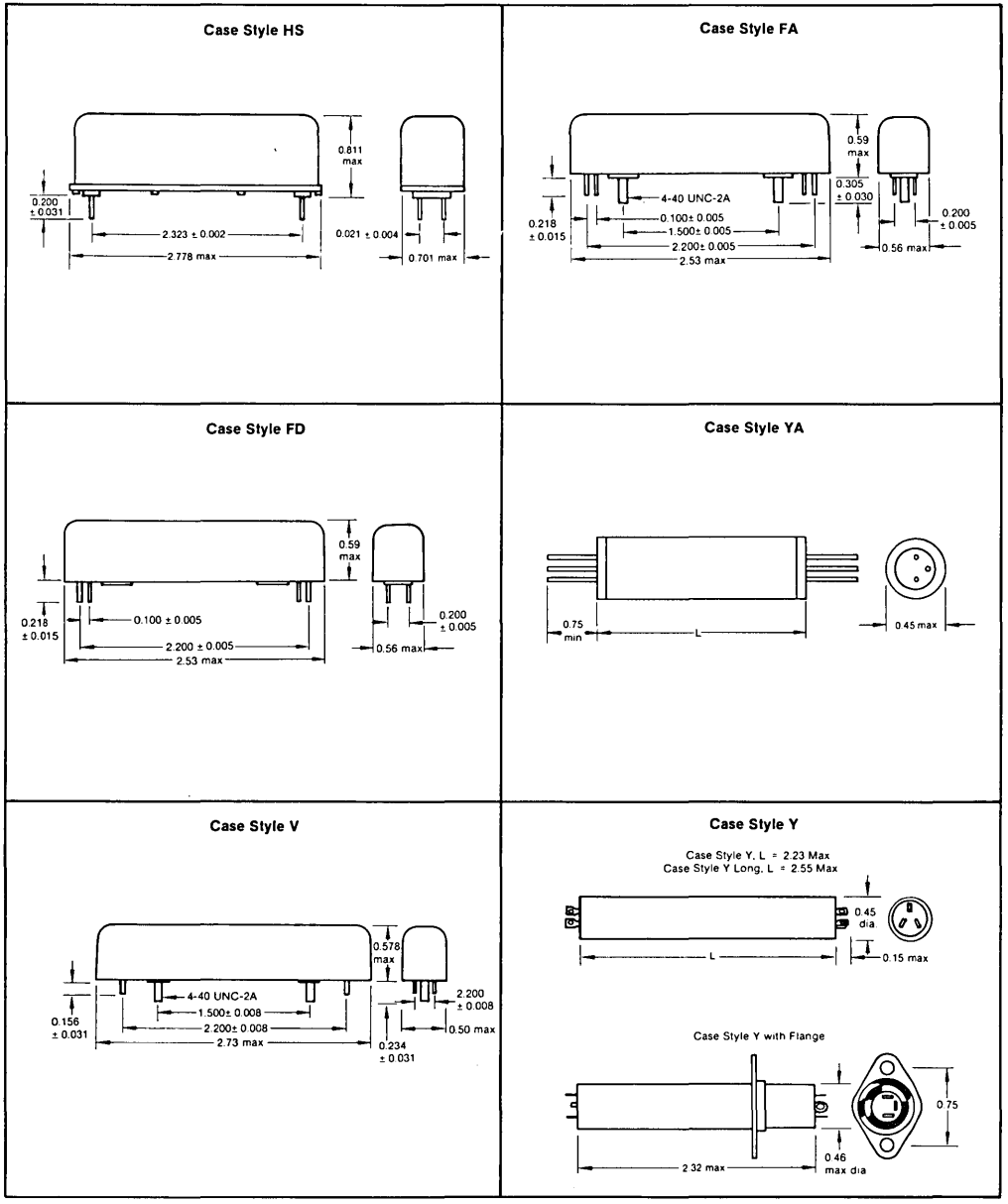


Figure 7. Disc-Wire Mechanical Filter Case Styles.

5.0 Application Guidelines

Rockwell-Collins disc-wire mechanical filters use two basic types of transducers: magnetostrictive and piezoelectric. Magnetostrictive transducers are further divided into two types: wire and ferrite. The type of transducer incorporated into the filter determines the application technique to be followed.

5.1 Magnetostrictive Transducers

Magnetostrictive wire and ferrite transducers require that the input and output transducer coils be capacitively resonated. The care required to resonate the coils depends on the filter type itself, the desired response variation (passband ripple) level, and the loss through the filter. Many mechanical filters, in various applications, can be resonated by a standard fixed-type capacitor (e.g., DM10). The value of this capacitor depends on the particular filter type and on the external/stray capacitance imposed on the filter by the application circuit. As the performance requirements for the filter become more stringent, greater care must be exercised in resonating the transducer coils. For example, if a mechanical filter is used in the receiver section of a CB transceiver, the nominal value of resonating capacitance defined in the filter specification will provide satisfactory results. However, if the filter is used in a single sideband radio that requires a low value of response variation in the passband and more precise frequency response characteristics, it is advisable to use variable capacitors to peak the filter during the equipment design stage. When the capacitance value for that specific filter type and application circuit has been determined, equivalent fixed capacitors may be substituted in production equipment. In applications where ultimate filter performance is required such as the very low ripple value required in voice multiplexing and telecommunications systems, it is advisable to use variable capacitors for tuning the production equipment. In all applications, the transducer coils must be properly resonated to ensure minimum response variation in the passband and to minimize loss through the filter.

To determine the capacitance required for resonance in a particular filter circuit, a simple method is to set the filter signal input at the center frequency of the filter. Then adjust the capacitors to obtain maximum output amplitude from the filter. In most applications no further tuning is required. However, if the absolute minimum value of response variation in the passband is required, further adjustment may be necessary. In this case, sweep the frequency of the input signal across the passband of the filter and, simultaneously, adjust the capacitors to obtain minimum ripple. The capacitance variation from the fixed value should not be large; however, it generally does result in lower ripple values.

In addition to resonating the transducer coils, the circuit must provide the proper source and load resistance values, as in other filter types. Filters which have wire transducers are essentially self-terminated and require a very high value of terminating resistance with the transducer coils parallel-resonated.A very low value of terminating resistance is required when the transducer coils are series-resonated. Thus, for parallel-resonant operation, the terminating resistance can be 100K ohms or greater and for series-resonant operation it can be 100 ohms or less. In many applications, these limiting resistance values can be changed to 50K ohms and 200 ohms, respectively; however, for values of resistance in between, a capacity divider is required.

Filters having ferrite transducers also need to be terminated with the specified resistance values defined in the filter specifications. If a filter cannot be terminated with these specific resistance values, a capacitance divider network should be used. For example, let us assume that a mechanical filter with ferrite transducers is designed for parallel-resonant operation. The capacitance value is determined to be 130 pF and the terminating resistance is 20K ohms; however, it is more convenient for the designer to provide a terminating resistance of 10K ohms. For the specified termination (20K ohms) see figure 8 and for the alternate configuration (10K ohms), see figure 9.

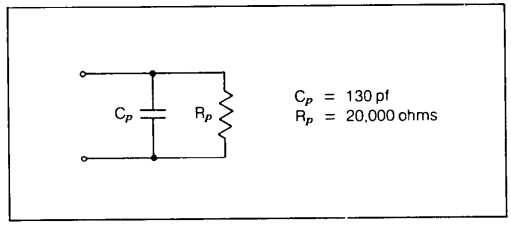


Figure 8. Specified Termination (20K ohms).

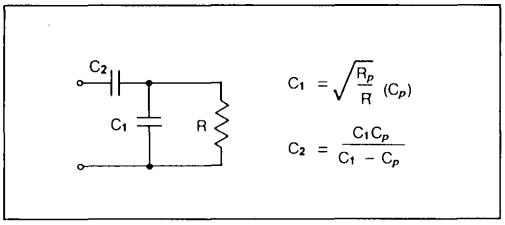


Figure 9. Alternate Configuration (10K ohms)

In the example chosen:

$$C_1 = \sqrt{\frac{20{,}000}{10{,}000}}\ (130) = 184\ \text{pf}$$

$$C_2 = \frac{(184)\ (130)}{184 - 130} = 443\ \text{pf}$$

If operation at a much lower impedance level is required, the designer can convert the terminating circuitry to series-resonate the coil. Assume again, that the filter is designed for parallel-resonant operation with 130 pf capacitance and a terminating resistance of 20K ohms. The conversions shown in figure 10 are satisfactory at a single frequency to convert either from parallel-to-series or series-to-parallel operation when only one terminating resistance condition is known. Note that the capacitive-reactance must be used in the calculation, not the capacitance value in picofarads.

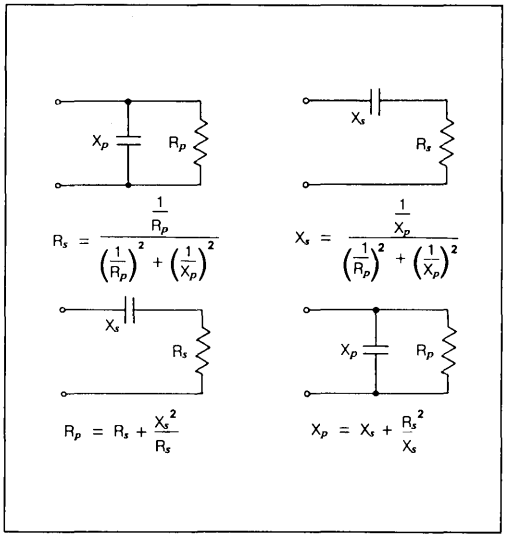


Figure 10. Parallel-to-Series and Series-to-Parallel Conversions.

In the example, let us assume an operating frequency of 455 kHz. The reactance of 130 pf at 455 kHz is:

$$\frac{1}{2\pi(455{,}000)(130 \times 10^{-12})} = 2700 \text{ ohms}$$

then:

$$R_S = \frac{\frac{1}{20{,}000}}{\left(\frac{1}{20{,}000}\right)^2 + \left(\frac{1}{2700}\right)^2} = 359 \text{ ohms}$$

$$X_S = \frac{\frac{1}{2700}}{\left(\frac{1}{20{,}000}\right)^2 + \left(\frac{1}{2700}\right)^2} = 2650 \text{ ohms}$$

and:

$$C_S = \frac{1}{2\pi(455{,}000)(2650)} = 132 \text{ pf}$$

Therefore, the equivalent series circuit at 455 kHz is a resistance of 359 ohms in series with a capacitance of 132 pf.

The preceding examples used parallel tuning, series tuning, and a capacitance divider and a terminating resistance somewhat less than the 20K ohms required for parallel tuning. In the following example, let us assume that a terminating resistance significantly closer to 359 ohms (determined above) is required for series tuning. In this range of terminating resistances, it is advantageous to use a capacitance divider, as shown in figure 11.

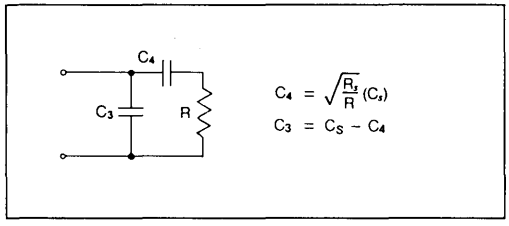


Figure 11. Capacitance Divider.

Refer to figure 11 and assume a desired value of 1K ohm for R. Knowing from the previous calculation R_S is 359 ohms and C_S is 132 pf.

Then:

$$C_4 = \sqrt{\frac{359}{1000}}(132) = 79 \text{ pf}$$

$$C_3 = 132 - 79 = 53 \text{ pf}$$

All examples shown use approximations and neglect stray capacitances. This may require some adjustments of values in the final application circuit. However, this is a simple, easy-to-use approach which provides the circuit designer with a good starting point when choosing his design. It is also apparent that some choice of approach exists in the middle range of terminating resistances between the limiting values of 20K ohms and 359 ohms.

5.2 Piezoelectric Transducers

Filters using piezoelectric ceramic transducers are generally tuned internally and need to be terminated with a specific resistance that is normally shunted by a specific capacitance. These filters can be tuned internally so that no external capacitance is required. However, since stray capacitances are always present in external circuits, the filters are designed to "see" some convenient value of capacitance which is defined in the filter specifications.

Application circuits should not be designed with signal levels so high that a slight increase in signal level input changes the bandpass characteristics of the filter. The specification for the filter defines a maximum input level. In general, levels of -20 to -10 dBm are acceptable. Permanent damage to the filter is not likely to occur unless levels are considerably higher. However, some deterioration of the response characteristics may occur when the filter is "overdriven". In terms of small signals, satisfactory operation is obtained with input levels as low as -100 dBm.

5.3 Application Conclusion

Most mechanical filters are capable of providing stopband rejection greater than 90 dB. To take full advantage of this capability, reasonable care in physical layout must be taken and good design practices must be observed. For example, physical separation and/or shielding between input and output must be provided. Do not allow leakage paths around the filter. If stopband levels are not greater than 90 dB, the problem most likely exists in the external circuit and not in the filter.

All preceding comments are intended as basic guidelines. Design experience and experimentation with mechanical filters will provide the designer with acceptable deviations for specific applications.

Figure 12 shows a generalized application using mechanical filters in transistor amplifiers and figure 13 shows an application for use in a balanced modulator. These circuits are not intended to be limiting; they are supplied only as starting point information for the designer.

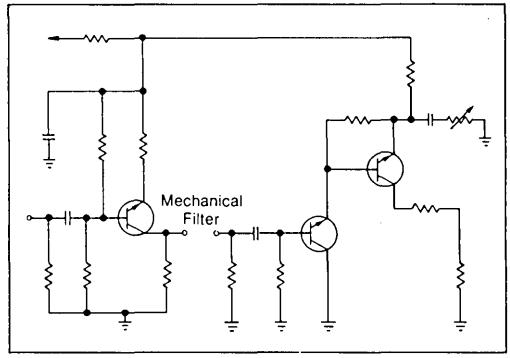


Figure 12. Transistor Amplifier Circuit

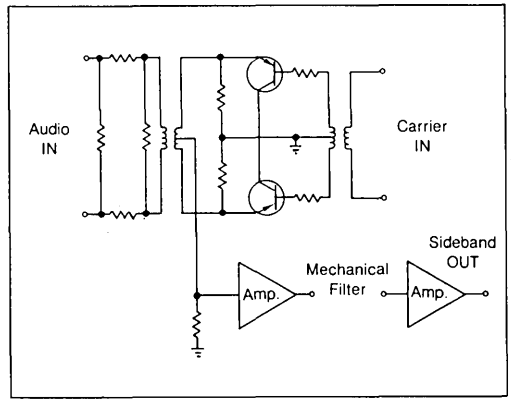


Figure 13. Balanced Modulator Circuit.

6.0 Disc-Wire Filter Characteristics

This section describes the effects of terminating circuits, group-delay response, dynamic range and power level, intermodulation distortion, spurious responses, stability and aging.

6.1 Effects of Terminating Circuits

The methods of achieving proper terminations for disc-wire filters were discussed in Section 5. This paragraph shows the effects when filters are not properly terminated. Improper terminations affect most operating characteristics of any high-performance bandpass filter. In a majority of applications, the most noticeable effects are increases in passband ripple and changes in insertion loss. Generally, the more selective the filter, the more noticeable the effects of improper termination.The performance of a multi-section filter having steep skirt selectivity will be degraded more by improper termination than will a filter having fewer sections and less steep skirt selectivity. To illustrate effects of improper terminations for typical filters, a nine-disc-resonator design with a 3 dB bandwidth of 3 kHz is presented here. Figure 6 shows that a filter (N = 9) with these characteristics has a shape factor of approximately 1.6 to 1, where shape factor is defined as the ratio of filter bandwidth at 60 dB to filter bandwidth at 3 dB.

As indicated in Section 5, all disc-wire filters must be terminated with an equivalent combination of resistance and capacitive reactance. In the following example, assume a typical filter requiring a termination of 10K ohms shunted by 160 pf. Furthermore, assume a "perfect" filter where every electrical and mechanical parameter meets exactly the nominal values specified, plus or minus zero tolerance. This filter, when properly terminated, has a 0.1 dB passband ripple that is evenly distributed across the passband. The effect of increasing or decreasing the external shunt capacity by 10 percent (16 pf), thereby increasing the passband ripple to approximately 1.0 dB (from 0.1 dB), is shown in figure 14.

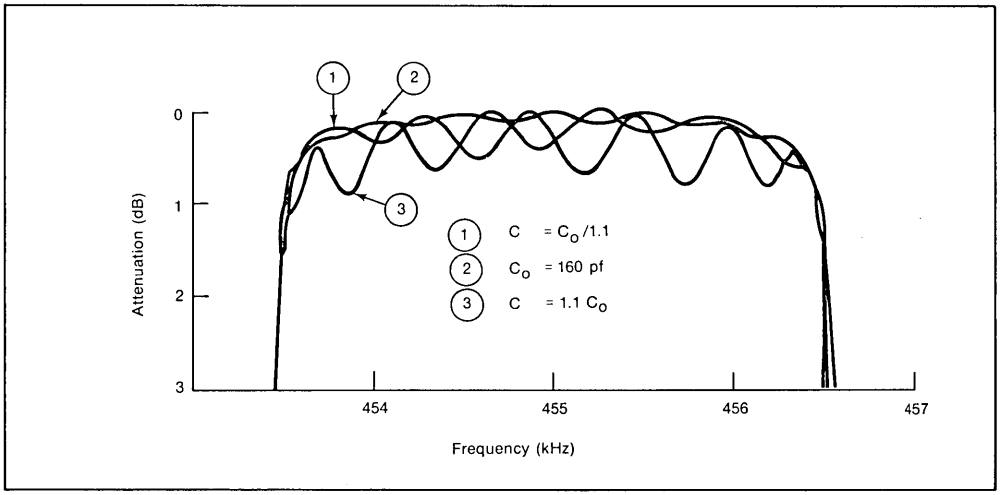


Figure 14. Effect of Terminating Capacitance on Passband Ripple.

When changing the shunt capacitors back to their correct value of 160 pf, and changing the terminating resistors by plus 100 or minus 50 percent, the passband ripple increases from 0.1 dB to 2.0 dB. This is shown in figure 15.

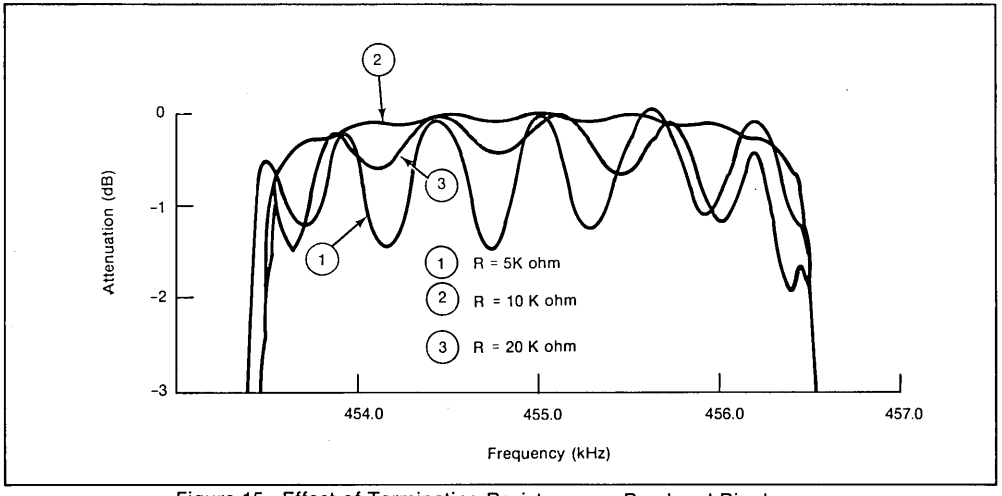


Figure 15. Effect of Terminating Resistance on Passband Ripple.

In practicality, there are almost no perfect filters. Even when ideally terminated, a filter will have a passband ripple value in the order of 1.5 dB as compared with a value of 0.1 dB. As a result, it is usually necessary to hold termination tolerances to ± 5 percent for resistance and ± 2 percent for capacitance.

6.2 Group-Delay Response

The approximate group (envelope) delay for a mechanical filter can be determined from figure 16 and from the following equations. Note that the curves shown in figure 16 are normalized to 3 dB; $F_N = 1.0$ at the 3 dB point.

$$\text{Group-Delay (Sec.) at Center Frequency} = \frac{NGD}{\pi BW_{3dB}}$$

NGD = Normalized group-delay from figure 16.

BW_{3dB} = 3 dB Bandwidth (in Hz)

Example 1:

The group-delay for a 9-pole, 0.1 dB Chebyshev filter which has a 3 kHz bandwidth is:

N	=	9
BW_{3dB}	=	3,000 Hz
NGD from fig. 16 at f_o	=	7.9 sec
Group-delay at $f_o = \frac{7.9}{3000\pi}$	=	0.0008382 sec = 838.2 μsec

To approximate group-delay at any frequency inside the 3 dB point, use the following equations:

F_x	=	Frequency in Hz from 3 dB point
F_N	=	$(0.5\ BW_{3dB} - F_x)/0.5\ BW_{3dB}$
Group-delay (sec) at F_N	=	$\frac{NGD}{\pi BW_{3dB}}$

Example 2:

In this example, let us determine the delay at 500 Hz inside the 3 dB point:

N	=	9
BW_{3dB}	=	3000 Hz
F_x	=	500 Hz
F_N	=	(1500 - 500)/1500 = 0.66
NGD from fig. 16 at (F_N = 0.66)	=	10 sec
Group-delay at X = $\frac{10}{\pi\ 3000}$	=	0.001061 sec = 1061 μsec

The differential delay of both examples above (center 2 kHz of the passband) is 1061 - 838 = 223 μsec, assuming that f_o was the minimum delay in the passband. The curves shown in figure 16 are idealized. Some variations from these curves exist in all filters.

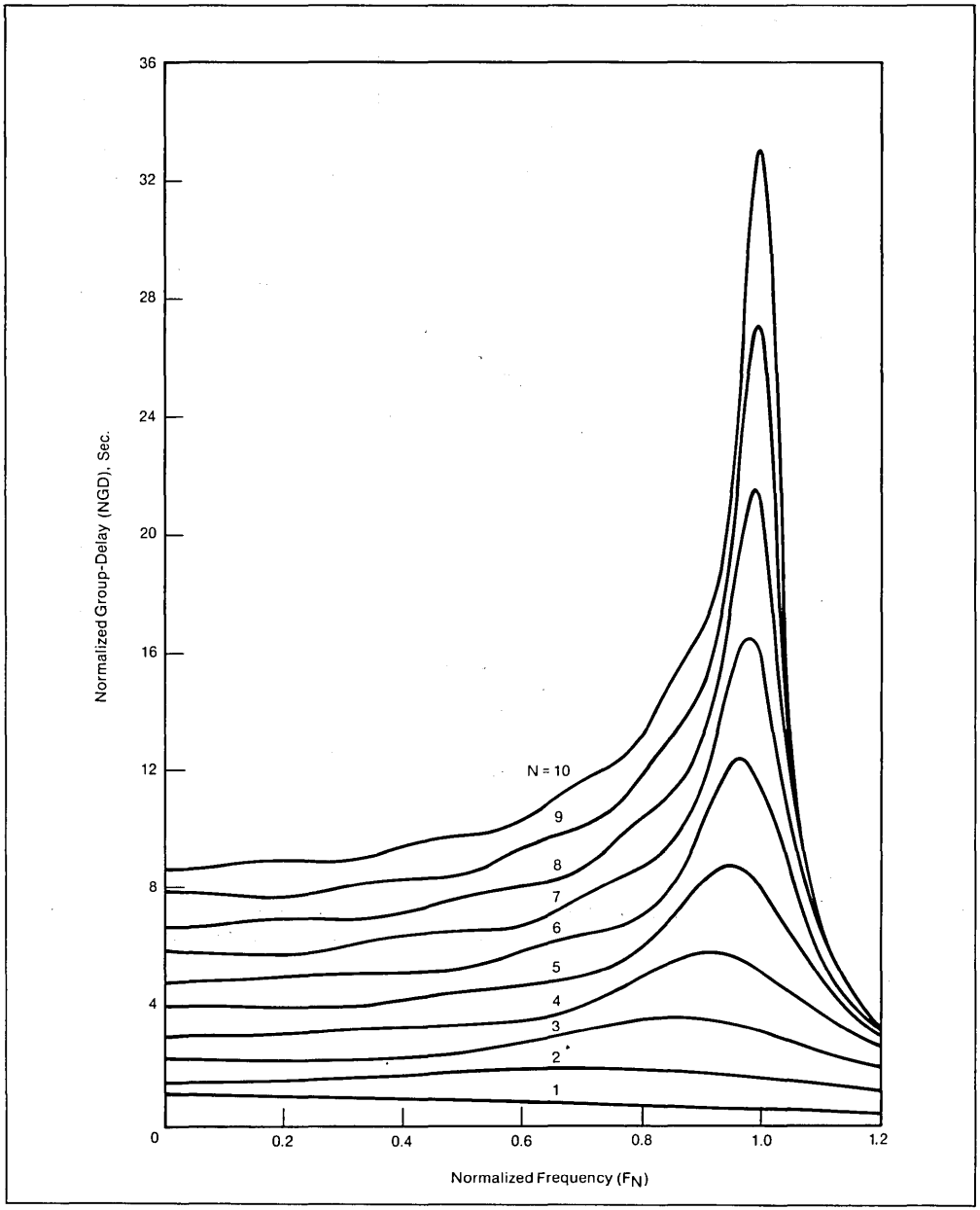


Figure 16. Group-Delay Characteristics for a Chebyshev Filter with 0.1 dB Ripple.

6.3 Dynamic Range and Power Level

There is no practical lower limit on the dynamic range since essentially no internally-generated noise exists. However, where vibration conditions exist, the microphonic electrical output from the filter is dependent on the vibration frequency and on the filter type. A typical output is in the order of -70 dB below a 100 percent, 1V rms modulated output signal at a vibration level of 5 g's betwen 0 and 500 Hz vibration frequencies.

The upper limit of the dynamic range is the linearity of the output signal. This, again, depends on the type of filter. A 3V rms input signal is a typical limit, although signals as high as 10V rms can be specified in some designs before appreciable non-linearities appear. See figure 17.

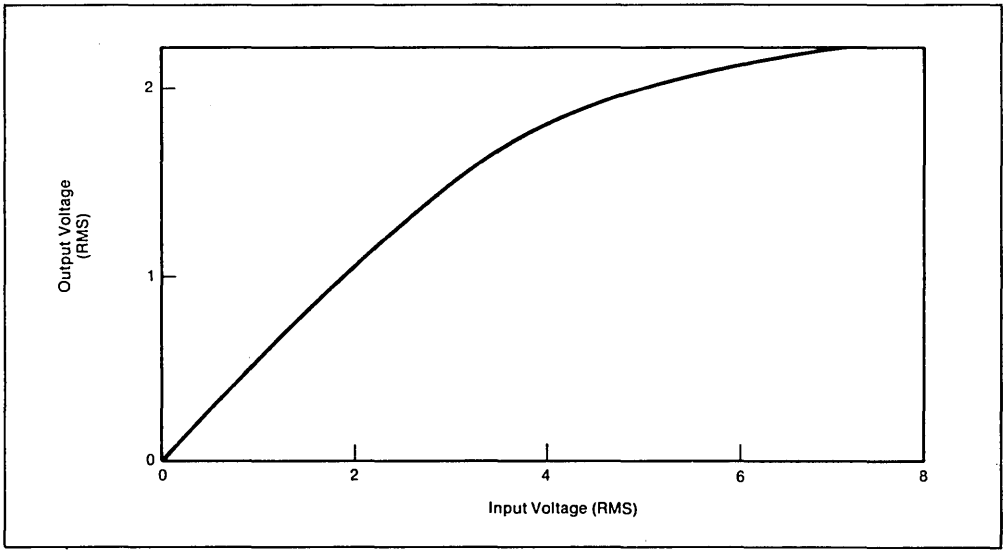


Figure 17. Voltage Linearity.

6.4 Intermodulation Distortion

Intermodulation distortion in a mechanical filter is the result of non-linearities in the electro-mechanical transducers. Therefore, intermodulation distortion is dependent on the type of transducer used and on the specific transducer design. Figure 18 shows curves of third-order intermodulation products as a function of signal level and transducer design.

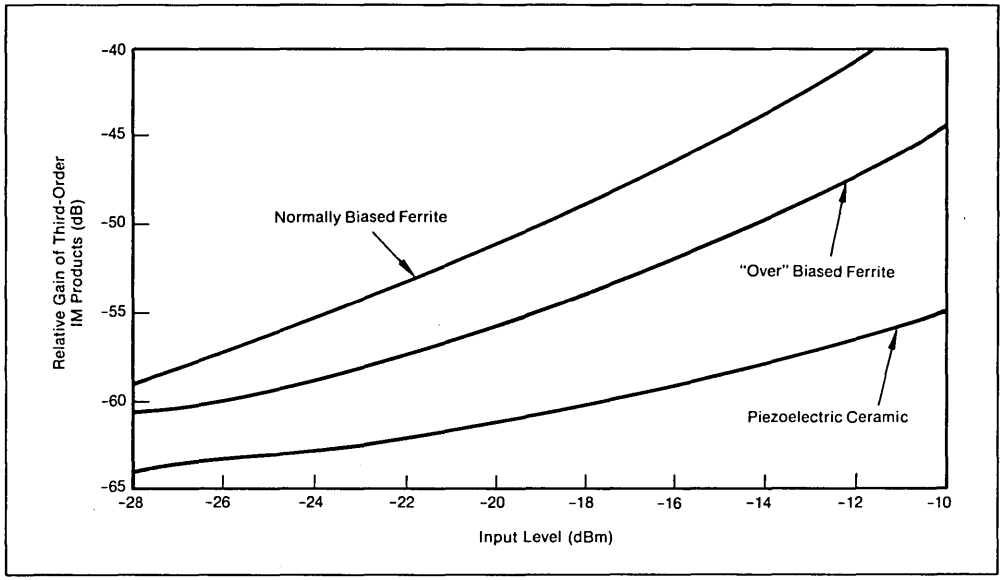


Figure 18. Third-Order Intermodulation Products

The intermodulation distortion test circuit is shown in figure 19. Generator F_3 and the short-circuit that bypasses the mechanical filter are used as a reference level. Generators F_1 and F_2 are set at frequencies in the stopband of the filter which result in F_3 falling within the passband of the filter, as shown in figure 20. To obtain accurate results, isolation between generators F_1 and F_2, and proper signal levels are of the utmost importance.

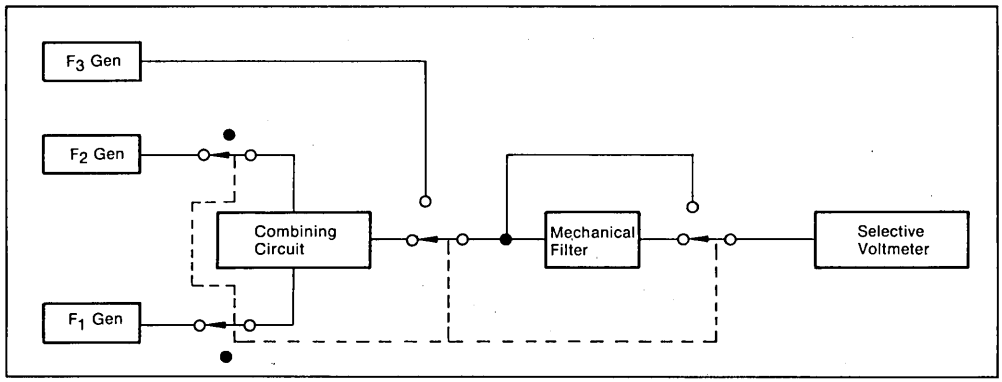


Figure 19. Filter Intermodulation Distortion Test Circuit.

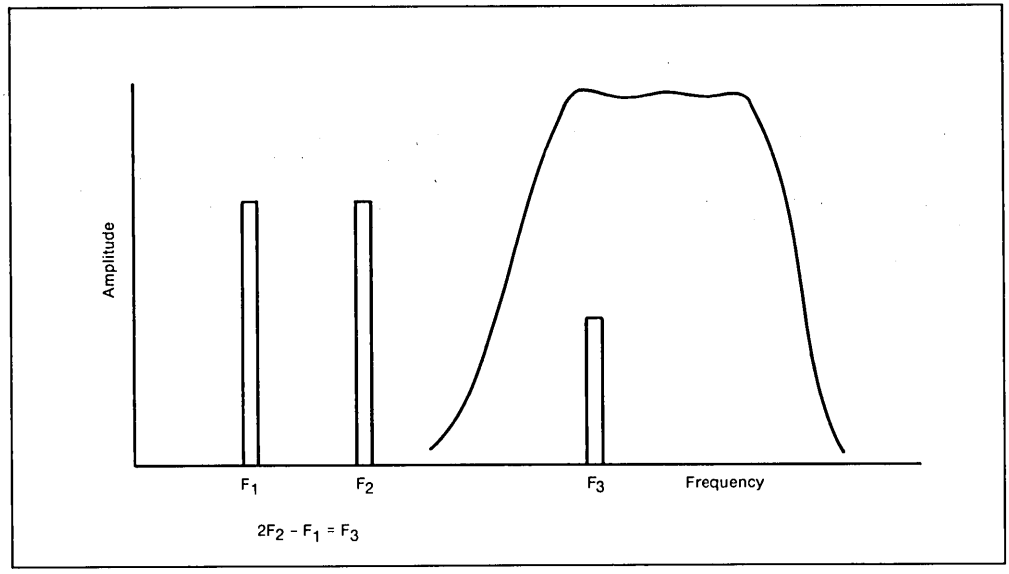


Figure 20. Third-Order Intermodulation Distortion Product.

6.5 Spurious Responses

Disc-wire filters do not have the resonant frequency overtones (nearly exact multiples) commonly found in quartz crystals. Mechanical filters do not have adjacent flexure and radial modes which appear in some filters as spurious responses.

With some exceptions, in mechanical filters the adjacent spurious modes are suppressed more than 60 dB below the passband reference level. Filters in the 5 to 10 kHz bandwidth range have spurious responses that exceed 60 dB. Filters in the 40 to 50 kHz bandwidth range may have spurious reversals in the transition bands or in the skirts of the filter response. Figure 21 compares spurious responses between filters with wire transducers, filters with ferrite transducers and center-coupled wideband filters.

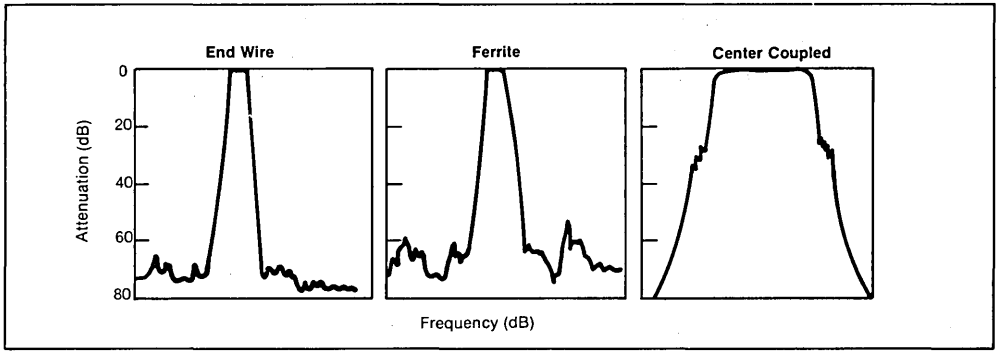


Figure 21. Comparison of Spurious Responses

6.6 Filter-to-Filter Variations

Paragraph 6.1 made the statement that "there are almost no perfect filters". Figure 22 below shows plots of 18 production filters superimposed on top of each other. This particular filter type was designed as a lower sideband filter for a 455 kHz carrier frequency. It can be seen that there are slight variations from filter to filter. It is also obvious that the specification on the skirt of the filter on the carrier side of the passband is tighter than the specification on the other skirt of the response. As a consequence, there is less filter to filter variation on that skirt.

In general, mechanical filter specifications are written conservatively, and the average filter is well inside the specified limits. Figure 23 clearly illustrates this point. It shows four histograms of selected parameters on a large (10,000 unit) sample of filters built for commercial application. The consistency of performance is an outcome of good process controls.

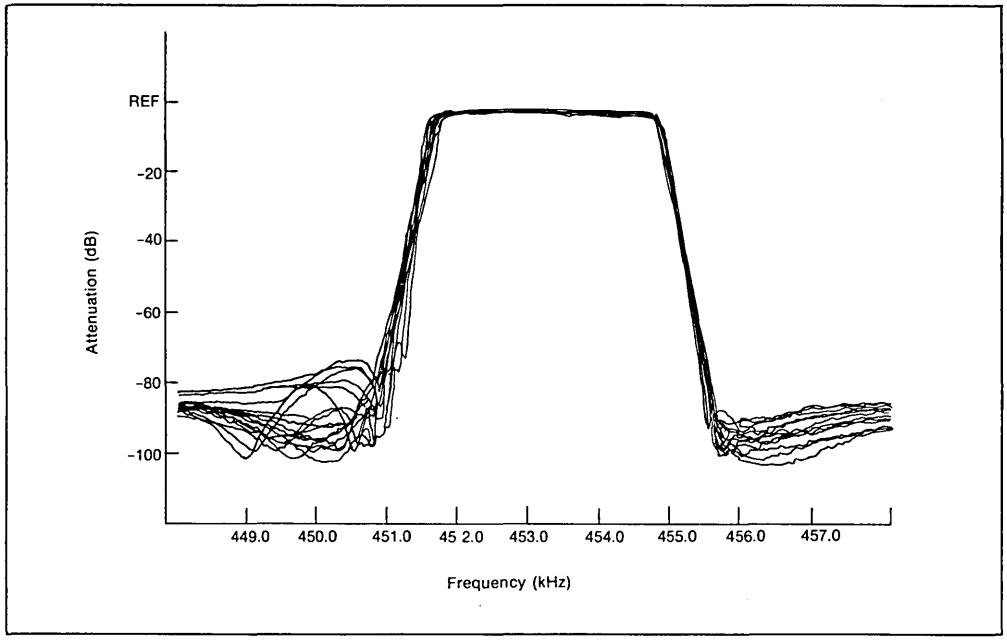


Figure 22. Filter-To-Filter Variations

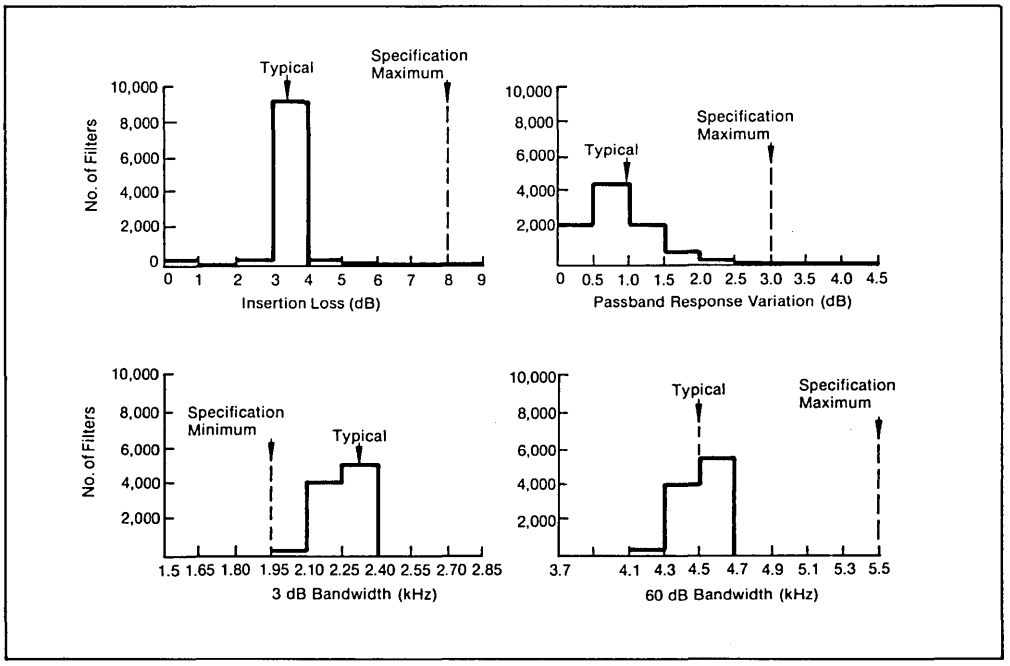


Figure 23. Typical Production Results.

6.7 Stability

The stability of disc-wire mechanical filters depends on the characteristics of the discs themselves. Collins disc-wire mechanical filters use an iron-nickel-chromium-titanium alloy (Ni-Span C) as the disc material. The titanium in the material allows the alloy to be heat-treatable. This means that the parabolic resonant frequency vs temperature curve can be shifted along the temperature axis to meet a precise filter specification. Figure 24 shows the frequency shift characteristics of a typical disc resonator at 455 kHz. To approximate the frequency shift at other frequencies, simply scale by the ratio of the new frequency to 455 kHz.

Example:

$$\Delta f_{fo(kHz)} = \Delta f_{455\ kHz} \times \frac{f_o(kHz)}{455} \quad \text{(for 2-nodal circles)}$$

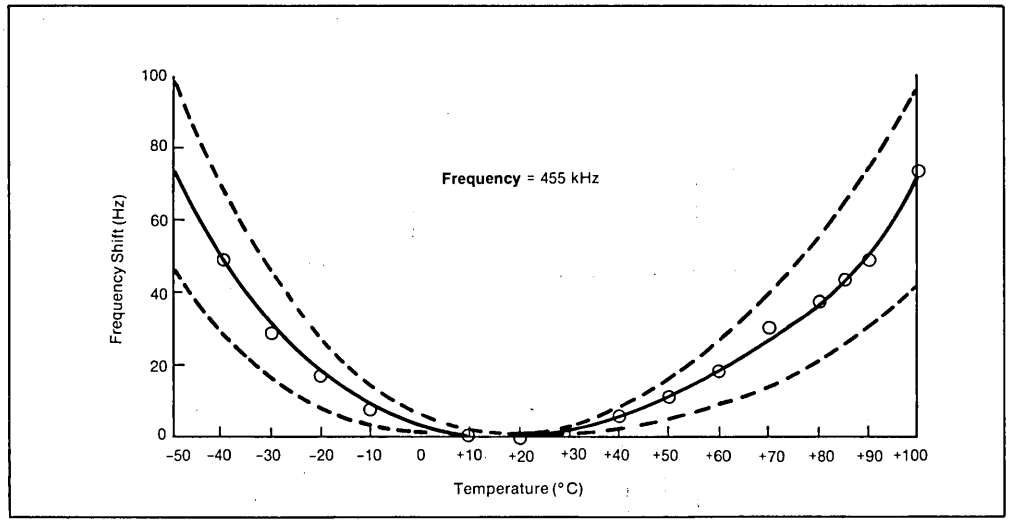


Figure 24. Disc Resonator Frequency Shift Characteristics

The one-sigma limits resulting from a variation in the heat treatment process are shown in figure 24 as dotted lines. Where single-nodal circles are used (normally below 200 kHz), the frequency shift equation must be multiplied by 1.5.

6.8 Aging

Frequency stability of mechanical filters with age is directly related to the resonator mode and to the characteristics of the material. A good estimate of center frequency shift, with age, is 50 ppm over a 20-year period or a 25 Hz shift of a 500 kHz center frequency.

The curves in figure 25 show the effect of accelerated aging at the 10 dB points of a typical 500 kHz filter having a bandwidth of 3 kHz.

Accelerated aging was accomplished by subjecting the filter to temperature cycles for 9 hours at 25° C and for 15 hours at 90° C. The cycles were repeated daily for a period of eight months.

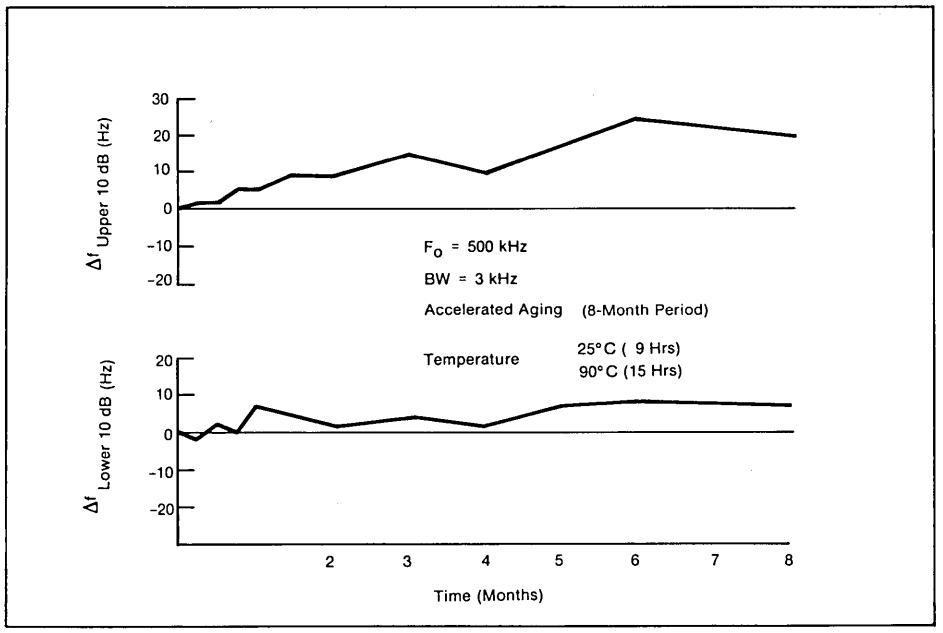


Figure 25. Effects of Accelerated Aging.

6.9 Reliability

Disc-wire mechanical filters are, by design, very reliable components. A collection of field service data is shown below:

Field Data: 277,000 Units
2.5 Years
374 Failures

$$\text{MTBF} = \frac{277{,}000 \times 2.5 \times 365 \times 24}{374}$$

$$= 1.622 \times 10^{7} \text{ Hours}$$

$$= 61.6 \times 10^{-9} \text{ (61.6 FIT)}$$

7.0 ENVIRONMENTAL EFFECTS

This section describes the environmental effects on disc-wire mechanical filters due to temperature, shock and vibration.

7.1 Temperature Effects on Center Frequency, Bandwidth, Loss and Ripple

Disc-wire filter designers use design techniques with compensating factors. These factors minimize center frequency shift and bandwidth of the filter with a change in temperature. Table 1 compares the variations of f_o and BW_{3dB} obtained from 10 single sideband filters at 450 kHz. All values shown are in Hz.

	f_o at 25°C	Δf_o at -40°C	Δf_o at +85°C	BW_{3dB} at 25°C	ΔBW_{3dB} at -40°C	ΔBW_{3dB} at +85°C
Average	451742	+48	+46	3037	-1.3	-9.4
Minimum Value	451681	+39	+37	2871	-23	-26
Maximum Value	451803	+56	+59	3138	+13	+2

Table 1. Variations of f_o and BW_{3dB} vs Temperature.

Table 2 shows effects of temperature change on a number of parameters for a sample of upper sideband filters designed for a 455 kHz carrier frequency. This filter was designed for a commercial application, so that the operating temperature range was not as great as the filter referenced in Table 1. The Table 1 filter is used in a military application.

	+25°C	-30°C to +50°C		Maximum Δ from 25°C
Parameter	Average Value	Minimum Value	Maximum Value	
Response Variation in dB	0.88	0.4	2.1	1.22
Insertion Loss in dB	2.7	2.4	4.1	1.40
3 dB Bandwidth in Hz	2152	2070	2230	82
60 dB Bandwidth in Hz	4342	4210	4480	138
Frequency in kHz of Low Side 3 dB Point	455.392	455.350	455.450	58
Frequency in kHz of High Side 3 dB Point	457.541	457.450	457.640	99
Frequency in kHz of Low Side 60 dB Point	454.305	454.170	454.400	135
Frequency in kHz of High Side 60 dB Point	458.624	458.480	458.770	146

Table 2. Temperature Variations.

A typical variation of insertion loss with temperature is ±1.0 dB over a temperature range of -10°C to +70°C. Changes in passband ripple, due to changes in temperature, depend mainly on the transducer design. Filters using piezoelectric transducers use internal components designed to optimize the response and therefore display better characteristics over temperature changes. A typical change in ripple over a temperature range of -40°C to +85°C is less than 1 dB. Most filters using ferrite or wire transducers have twice the amount of ripple of their actual room temperature values, over this same temperature range.

Temperature variations in center frequency, bandwidth, loss and ripple are temporary. The filter is restored to its original operating condition when the temperature is restored to +25°C without measurable hysteresis.

7.2 Shock

To prevent damage from shock, the mechanical filter structure uses an internal resilient rubber shock mount. This shock mount enables the average SSB filter to withstand greater than 50 G, 11 msec shocks without changing the filter response. Many mechanical filters can withstand 75 G's of shock before permanent damage occurs. See figure 26 for a comparison of shock level versus filter bandwidth. Note that filters using off-resonant discs have narrow bandwidths, and filters using the mini-single-nodal circle have wide bandwidths.

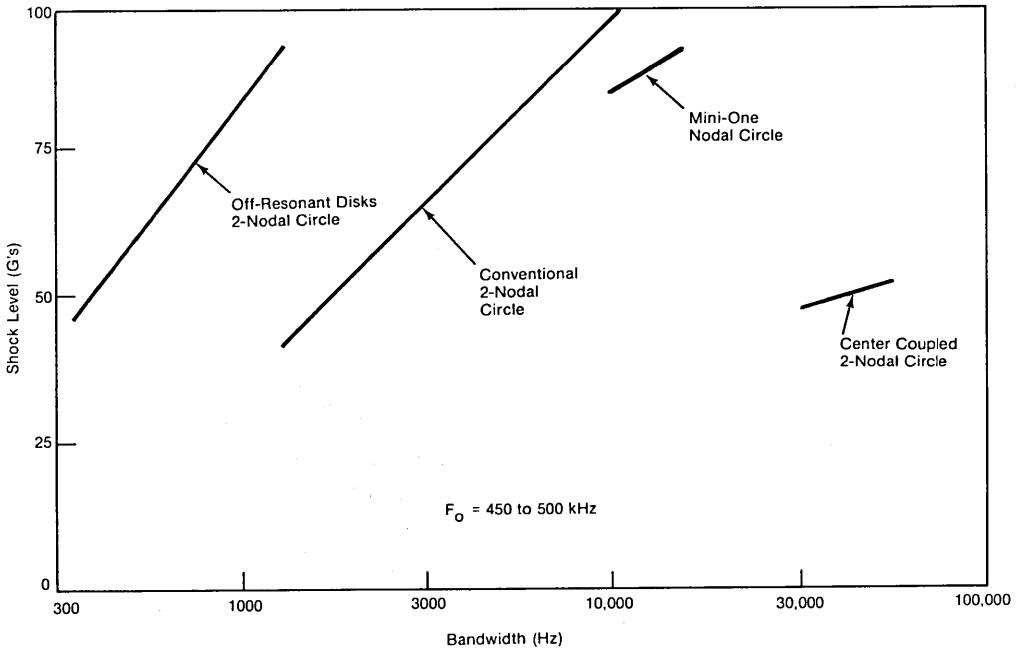


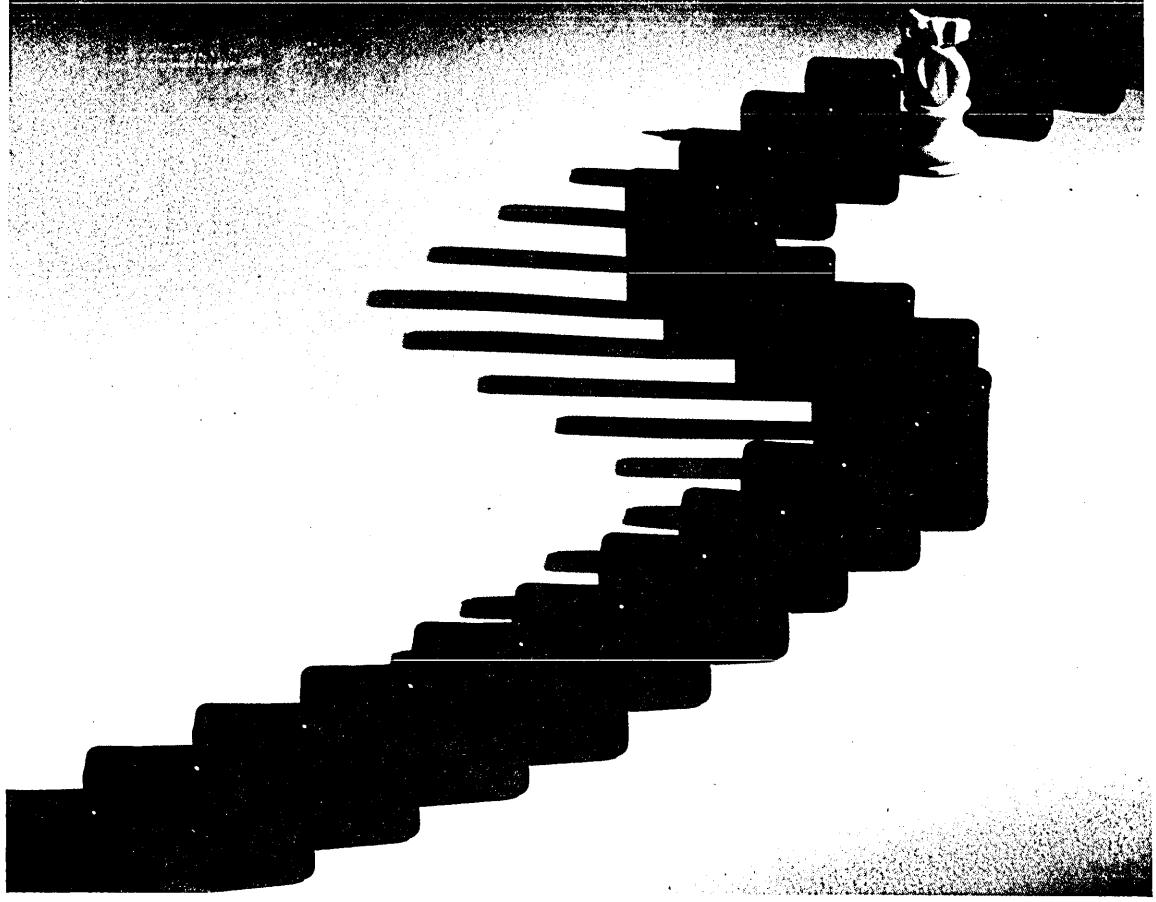
Figure 26. Shock Level vs Filter Bandwidth.

7.3 Vibration

The internal shock mount that so effectively isolates the filter from shock is also excellent for suppressing vibration. All Collins disc-wire mechanical filters exceed MIL-STD-202, Method 201.

Collins Low Frequency Mechanical Filters

Rockwell



FILTER PRODUCTS

Collins Low Frequency Mechanical Filters

Rockwell

Table of Contents

Collins Low Frequency Mechanical Filters

1.0 Introduction to Low Frequency Mechanical Filters

The low frequency mechanical filter consists of two metal alloy bars bonded to piezoelectric ceramic transducers and coupled mechanically with wires which also act as the supporting structure. See figure 1. The bars are made out of a constant modulus nickel-iron alloy whose temperature coefficient is adjusted by heat treatment to help compensate for the high positive temperature coefficient of the ceramic. The composite resonators operate in the flexure mode with wires coupling the bars torsionally. Figure 2 shows the equivalent circuit of the filter.

1.1 Practical Design Limits

The mechanical filter may be designed as a Chebyshev, Butterworth, TBT, Linear Phase or Bessel filter in either a 2, 3 or 4 pole (resonator) configuration. The Chebyshev (equal passband ripple) designs are available with ripple values ranging from .01 to 1.5 dB. Typical response curves for these designs are available in standard filter handbooks.[1]

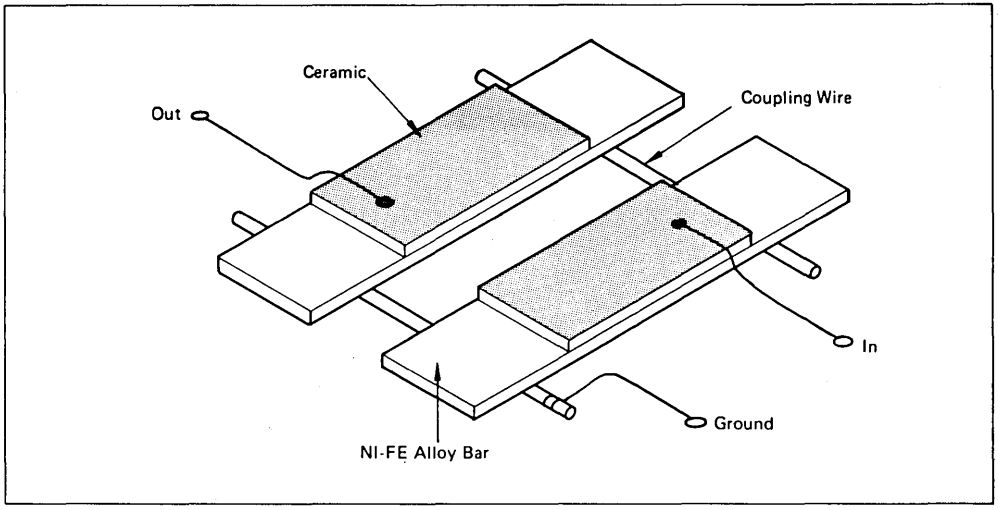


Figure 1. Low Frequency Mechanical Filter

[1] G. Hansell, Filter Design and Evaluation, Van Nostrand Reinhold Company, 1969.
Howard W. Sams, Reference Data for Radio Engineers, 1968.
A. Zverev, Handbook of Filter Synthesis, John Wiley and Sons, Inc., 1967.

The practical design limits for low frequency mechanical filters are illustrated in figure 3. The fractional bandwidth (BW_{3dB}/F_o) varies from .2% to 1.5% over a center frequency (F_o) range of 3.5 to 70 kHz. The fractional bandwidth is further influenced by the environmental restrictions (shock and vibration) and the type of design, such as Chebyshev or Bessel.

Typically, Chebyshev designs having fractional bandwidths between .2% and 1.5% can be achieved for shock levels to 100 G's and vibration levels to 10 G's.

An attenuation comparison for .25 dB ripple Chebyshev filters is presented in figure 4 and a linear phase equiripple (.5° error) design in figure 5.

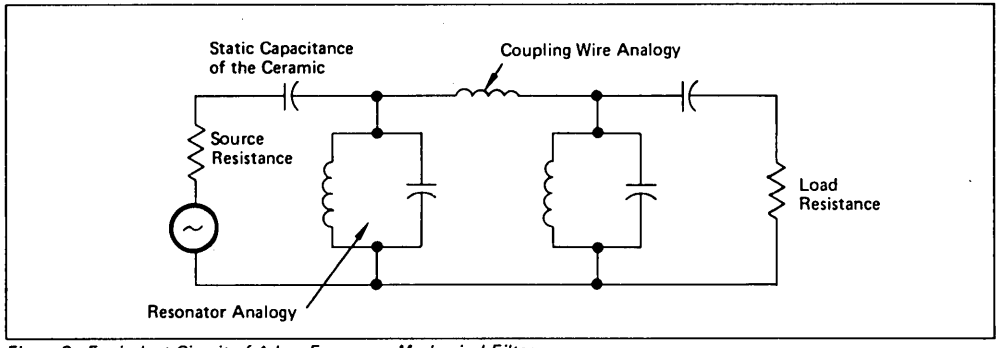


Figure 2. Equivalent Circuit of A low Frequency Mechanical Filter

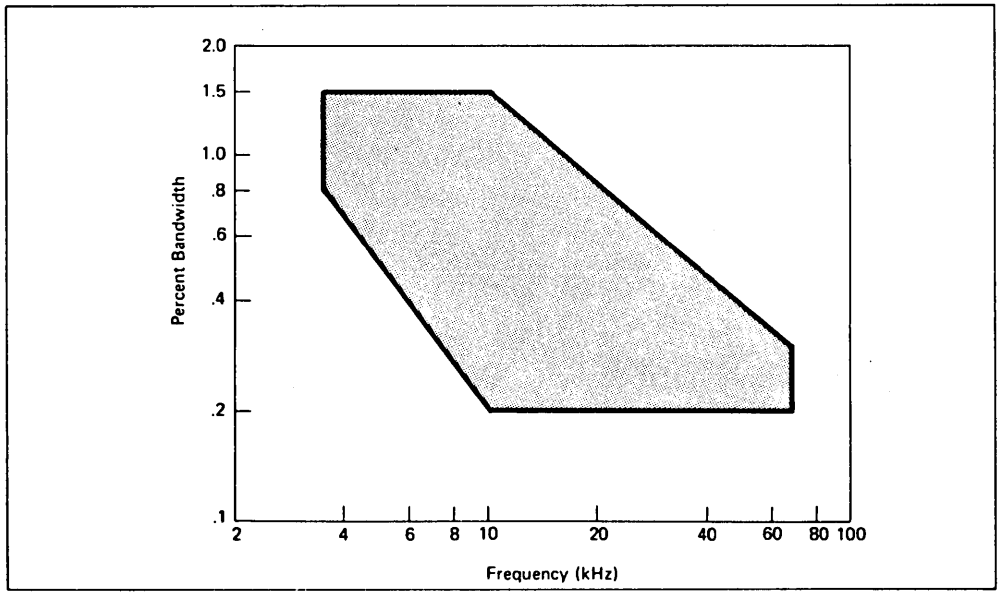


Figure 3. Practical Design Limits of Low Frequency Mechanical Filters

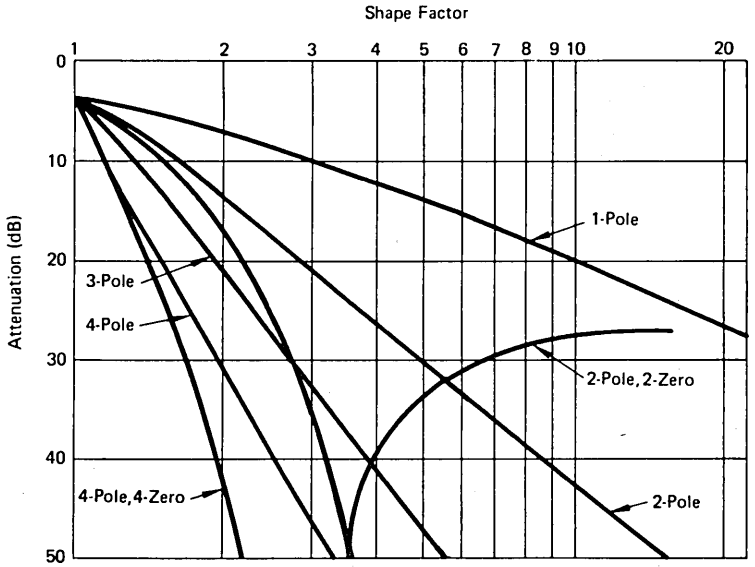


Figure 4. Attenuation Comparison for .25 dB Ripple Filters

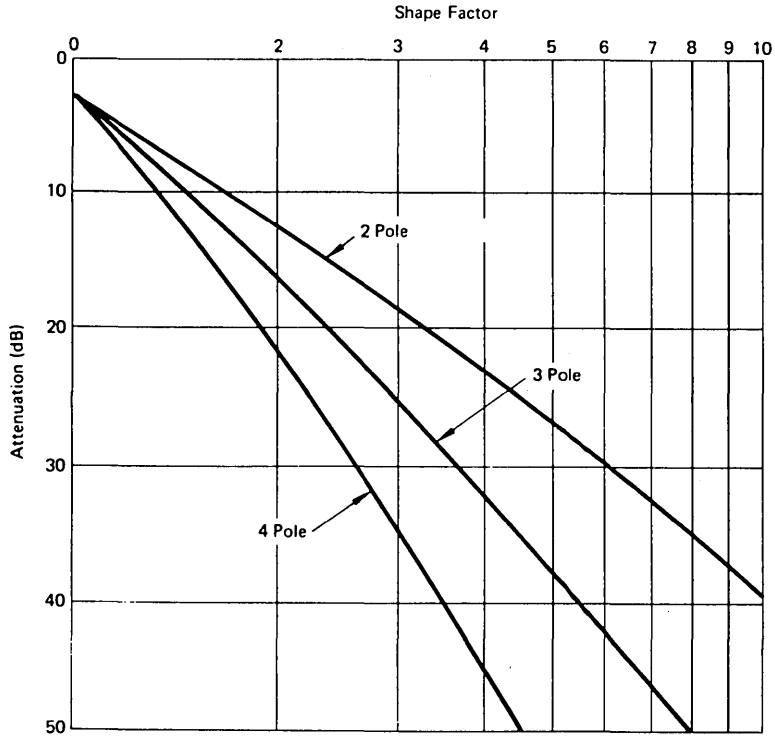


Figure 5. Attenuation Comparison for Linear Phase Equiripple (.5° Error) Filters

The Chebyshev designs are primarily for tone selectors while the linear phase designs are used where phase or FSK modulation is transmitted. The linear phase designs have 0 dB ripple and a low ringing impulse response (4% ringing for a 2-Pole). Typical mechanical filter specifications are tabulated in table 1. The values are interrelated (and therefore not independent) and are a function of the type of design, i.e. a very narrow filter would probably not have a high level shock specification.

Table 1. Mechanical Filter Specifications and Characteristics

Specifications	Minimum	Typical	Maximum
Center Frequency (F_o)	3.5 kHz		70 kHz
Fractional Bandwidth $\frac{BW_{3\ dB}}{F_o}$	0.2%		1.5%
Number of Poles (Resonators)	1		4
Characteristics	**Minimum**	**Typical**	**Maximum**
Insertion Loss	1 dB	3.5 dB	10 dB
Terminating Resistance	2 KΩ	20 KΩ	50 KΩ
Temperature Coefficient of F_o	± 3 PPM/°C	± 10 PPM/°C	± 25 PPM/°C
Temperature Coefficient of $BW_{3\ dB}$		500 PPM/°C	
Passband Ripple	0 dB	0.2 dB	1.5 dB
Vibration (10 Hz to 2000 Hz)	1G	10 G's	15 G's
Shock	15 G's	100 G's	1500 G's
Differential Phase Vs. Input Level (−70 to −10 dBm)	0.5°	0.5°	2°
Volume	0.5 IN^3	0.5 IN^3	1.0 IN^3

1.2 Enclosure Styles

There are four enclosures currently available with low frequency mechanical filters. Three of the enclosures (PA, FS, and LC) are plastic, the fourth (FP) is a hermetically-sealed metal case. It is recommended that the 'LC' case be used whenever possible as it is significantly lower in cost.

Case style 'PA' is a plastic version of the 'FP' enclosure. It is normally not available except under special circumstances.

The 'FS' enclosure is used only on 2-Pole filters which have a 'fail-safe' requirement, i.e. the input can at no time short circuit to the output. This type of filter is normally found in railway systems, people carriers and automated rapid-transit trains. The enclosure is rated for a −20° C to +95° C environment and is not hermetically-sealed.

The 'LC' case is made of plastic and is ultrasonically sealed. It is rated for a −55° C to +95° C environment. Filters in these enclosures have been tested with two consecutive cycles of Mil-Std 202, method 106 for a total time of 20 days at 90% humidity. During the 20 day period filters are thermally-cycled from −10° C to +65° C and intermittently vibrated at 9 G's. This test is designed to evaluate the resistance of component parts to tropical environments. Although the cases and the filters withstood this environment, they may not be able to withstand extremely long period environments because of the permeability of the plastic case. However, if the user provides an additional moisture barrier such as 'post-coat', filters in this enclosure will pass a more rigorous environment.

The alternative enclosure for tropical or high altitude service is the 'FP' case style. This is a cold-welded metal enclosure with glass to metal terminal seals. The filters in this package are rated for a −55° C to +95° C environment and guaranteed to meet the moisture resistance test. A disadvantage is that they are several times more expensive than the 'LC' enclosure.

1.3 Application Circuits

The following constraints are suggested limitations on the application circuit. Although these values may be exceeded without damage to the part, the filter will operate in a non-linear portion of its spectrum or will not meet the specifications.

Signal input level (across the terminals):	1 Vrms
DC voltage across the terminals:	50 VDC
Source and load termination:	$\pm$ 5%
Stray capacitance across the input/output terminals to ground:	50 pf Max

The application circuits of figure 7 demonstrate the use of bridging capacitors (C_1, C_2) which are used to convert a monotonic response to an elliptic function response. Bridging the filter with a capacitor between the input and output terminals provides the attenuation poles (transmission zeros) shown in figure 4. This capacitor is typically about 30 pf in value. Although there is a substantial improvement in the filter's shape factor (the ratio of the bandwidth, at a specified attenuation level to the 3 dB bandwidth) the disadvantage with this technique is that the attenuation level in the stopband of the filter decreases as the bridging capacitance is increased. See figure 4 for an illustration of a 2 Pole – 2 Zero design.

A method used for realizing greater performance from a mechanical filter and still maintain a high stopband attenuation level is to cascade two or more units. This method results in an addition of the attenuation levels of each filter at any specific frequency.

The cascading is accomplished by using an active network to prevent interaction between the filters. The network could be either a transistor buffer amplifier or an Op-Amp. See figure 7.

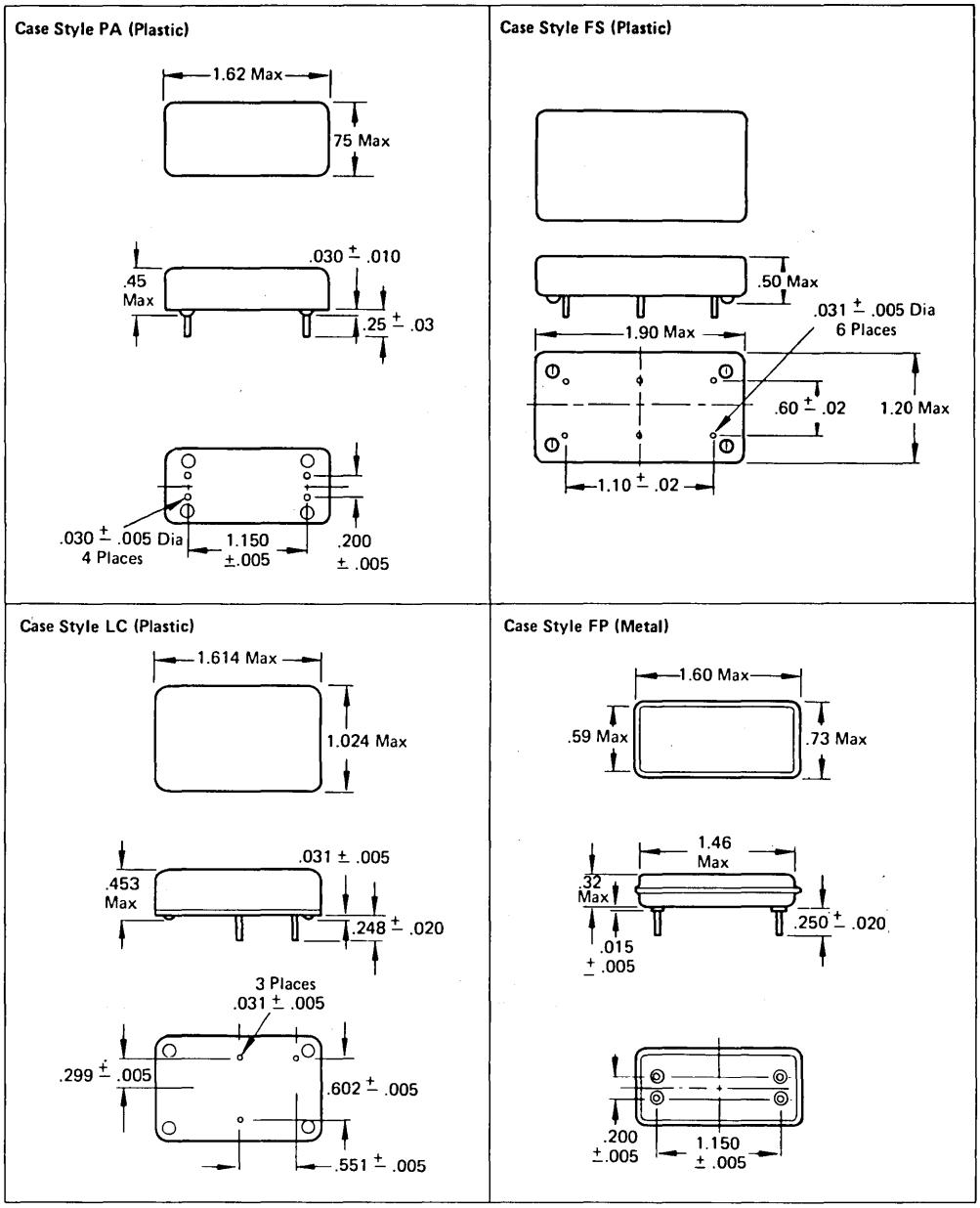


Figure 6. Low Frequency Narrowband Mechanical Filter Flatpack Dimensions

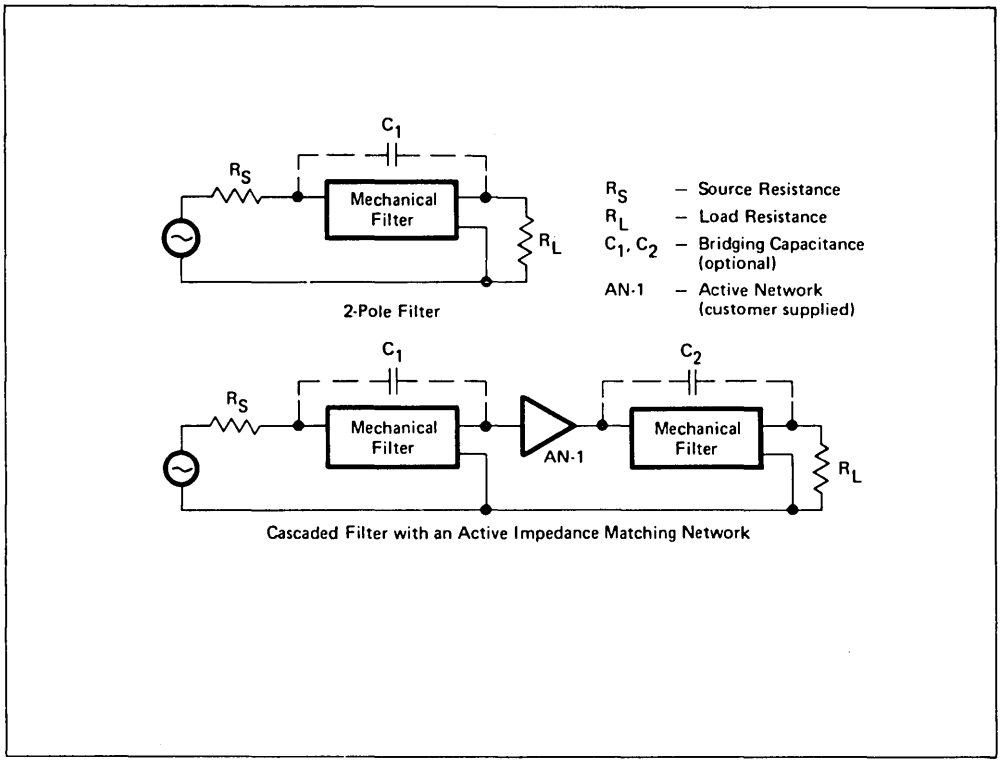


Figure 7. Low Frequency Mechanical Filter Circuit Configurations

1.4 Applications for Low Frequency Mechanical Filters

Small size and low cost make the filters ideally suited for Omega navigation, selective calling systems, telephone multiplex, telemetry, centralized control systems, Sonar, mobile radio and FSK telegraph applications.

Low frequency mechanical filters can also be used to delay a signal by a specific amount. The delay of the filter is inversely proportional to the bandwidth of the filter and directly proportional to the number of poles, therefore, the delay can be accurately controlled. See section 2.5 for additional information.

2.0 Characteristics of Low Frequency Mechanical Filters

2.1 Center Frequency Vs. Termination

In normal applications of low frequency mechanical filters, the resistive terminations (R_S and R_L) shown in figure 7, should not deviate more than $\pm$ 5% from the specified values. That is, the terminations affect the actual center frequency to some extent. For example, if a filter with a nominal center frequency of 10 kHz and a 50 Hz bandwidth has both its source and load resistances increased by 5% above the specified values, the filter center frequency($\frac{F3H + F3L}{2}$) will increase by .5 Hz. If R_S and R_L are changed (from the specified value) in opposite directions, small changes (2% to 3%) are off-setting, and there is no center frequency shift. For large variations (in opposite directions) in R_S and R_L, the effects are not completely offset, and the insertion loss and passband ripple of the filter will increase.

Stray capacitance between the input/output terminals and ground should not exceed 50 pf. Additional capacitance beyond this value will cause changes in insertion loss and center frequency. An increase to 150 pf will result in a .5 dB change in loss and a 75 ppm change in center frequency in the above example.

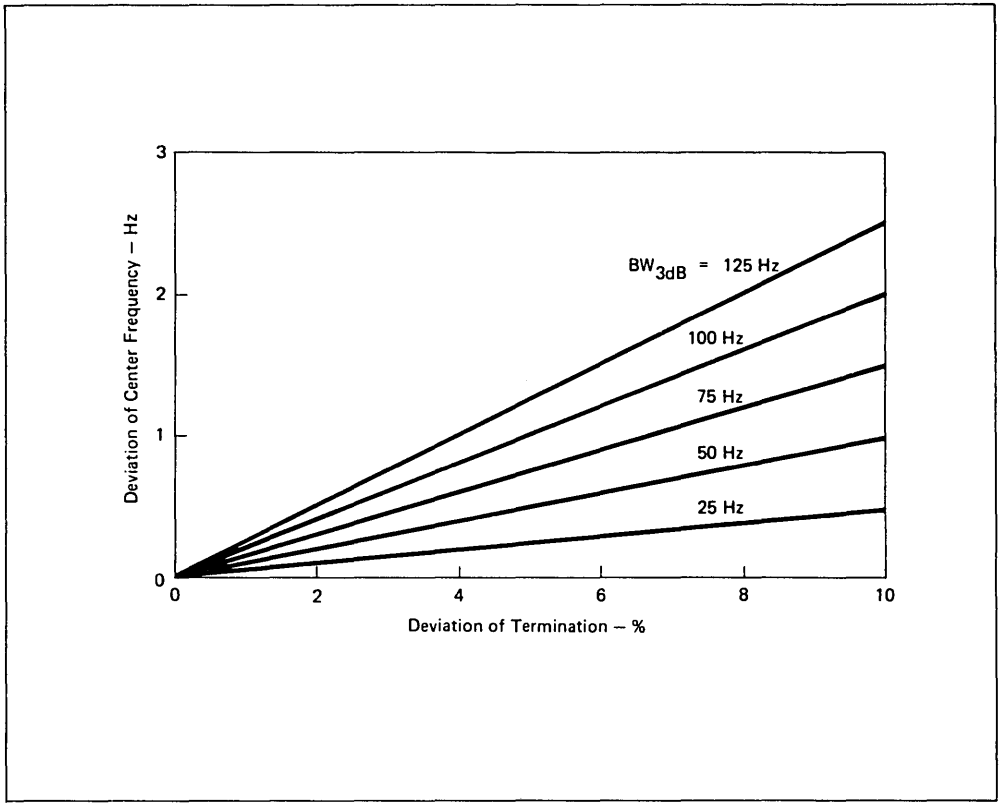


Figure 8. Variation of Filter Center Frequency with Resistive Termination

2.2 Center Frequency Vs. Input Voltage Level

Low frequency mechanical filters remain very linear with drive level up to 0.5 v, at which point they rapidly become non-linear. See figure 9. The shift in the center frequency at a ten volt level is enough to move some filters out of specification. Also, along with the non-linear effects, excessive drive level causes time dependent changes in the ceramic material. These changes cause the center frequency of the filter to be lower after being driven at a high voltage level. Once the drive level is reduced the filter response begins to return to its original frequency.

2.3 Differential Phase Vs. Input Voltage Level

The differential phase at the center frequency of a linear-phase equiripple (.5° error) filter is 0.5 degree over an input level variation of 60 dB, namely −10 dBm to −70 dBm. The change in phase is due to a center frequency shift caused by the nonlinearity of the input transducer.

2.4 Input to Output Level Linearity

The linearity of the output signal level to the input level at the filter center frequency is 0.1 dB over an input voltage range of 60 dB (−10 dBm to −70 dBm).

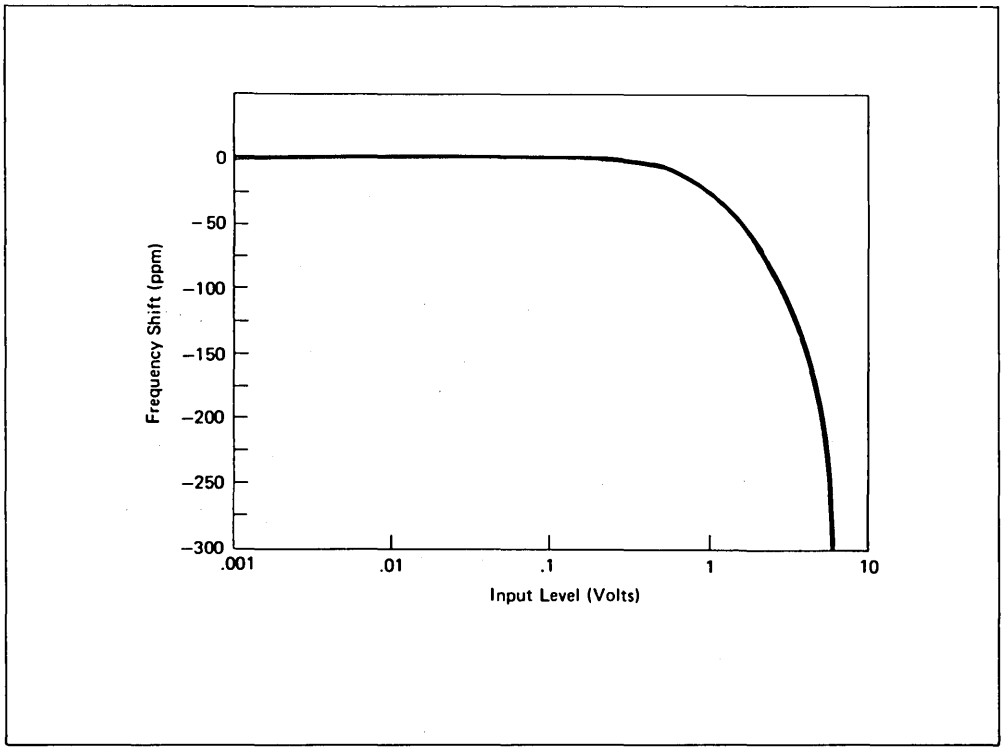


Figure 9. Variation in Center Frequency with Input Voltage Level

2.5 Group Delay Response

The approximate group (envelope) delay for a mechanical filter can be determined from figures 10, 11, 12 and 13 as well as the following equation.

$$\text{Group delay (sec) at center frequency} = \frac{NGD}{\pi \, BW_{3\,dB}}$$

NGD = Normalized Group Delay from figures 10, 11, 12, or 13

$BW_{3\,dB}$ = 3 dB Bandwidth (in Hz)

Example:

The group delay for a 2 Pole .1 dB Chebyshev filter which has a 40 Hz bandwidth is

N = 2

$BW_{3\,dB}$ = 40 Hz

NGD from figure 12 = 1.4 sec

$$\text{Group delay} = \frac{1.4}{\pi \, 40} = .011 \text{ sec} = 11 \text{ msec}$$

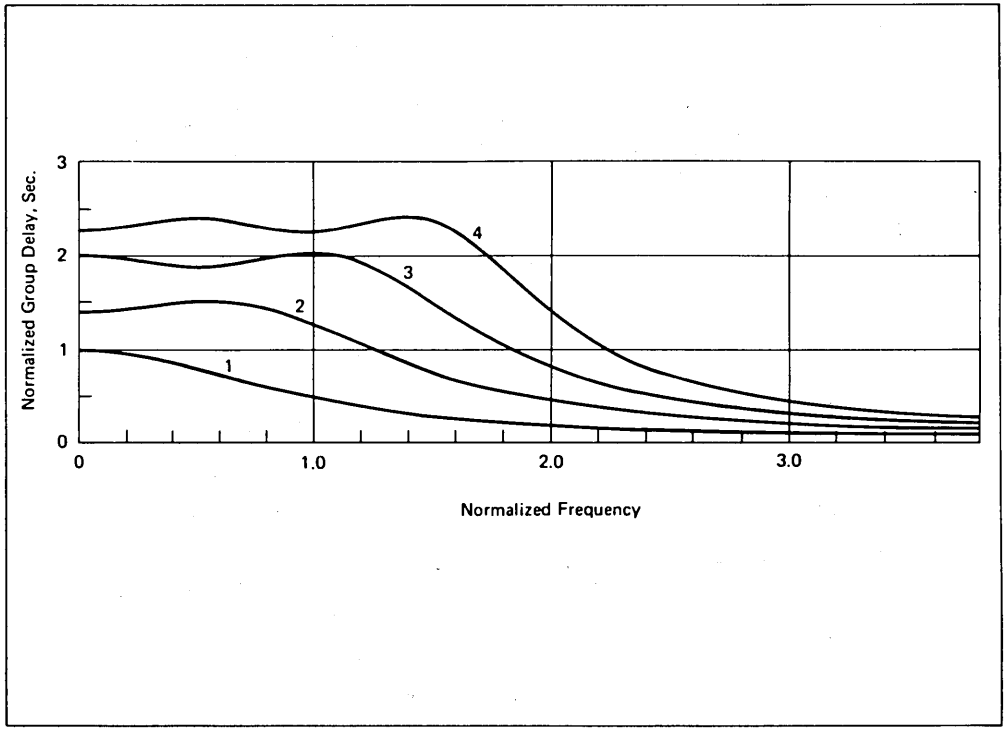


Figure 10. Group-Delay Characteristics for Linear Phase (Phase Error = .5°) Filter

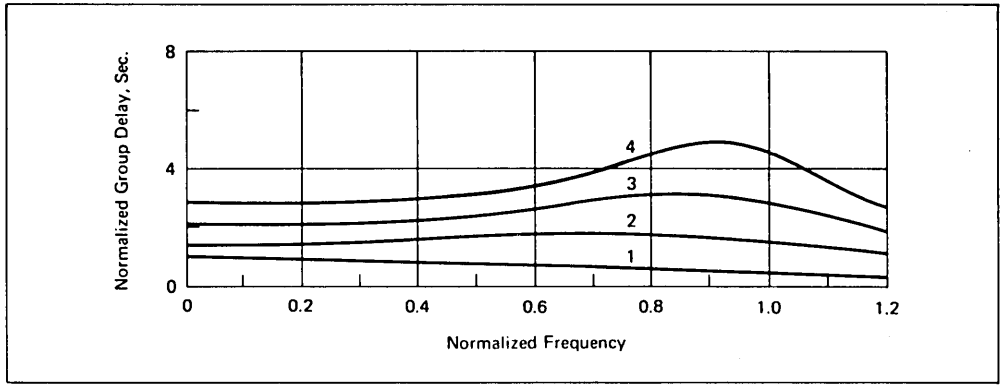


Figure 11. Group-Delay Characteristics for Chebyshev Filter with 0.01 dB Ripple

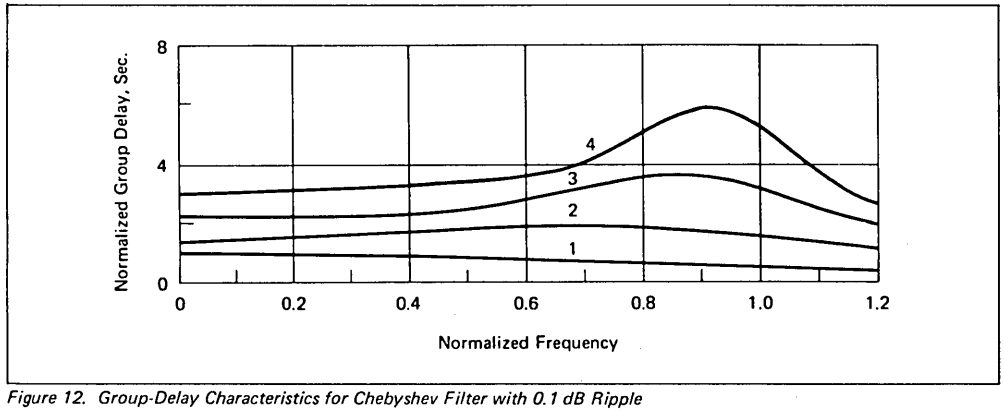


Figure 12. Group-Delay Characteristics for Chebyshev Filter with 0.1 dB Ripple

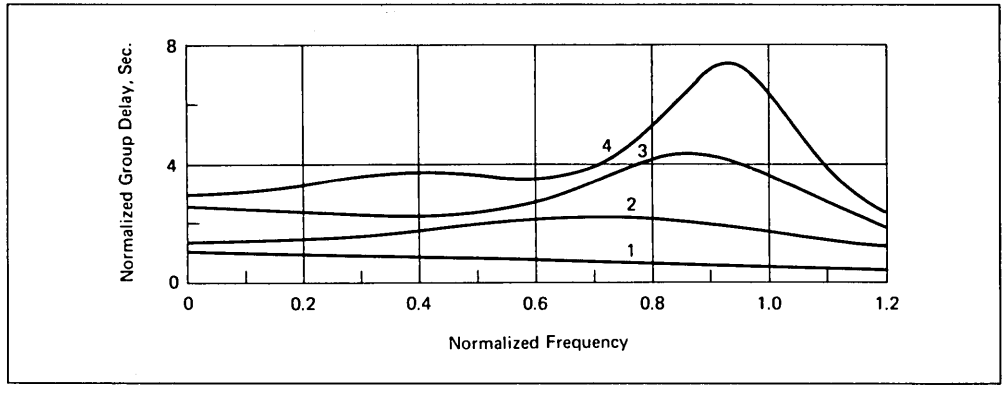
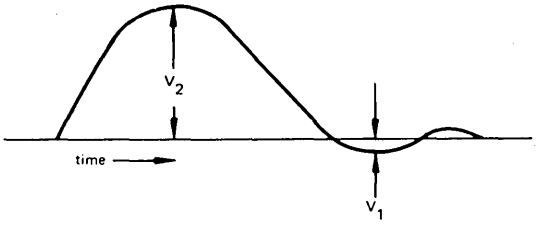


Figure 13. Group-Delay Characteristics for Chebyshev Filter with 0.5 dB Ripple

2.6 Impulse Response

Figures 14 thru 17 can be used to approximate the impulse response ringing value of a mechanical filter. A definition of ringing is the ratio of V_1/V_2 in percent.



For example:

A two-pole mechanical filter designed as a linear-phase filter has an impulse response ringing value of 4%.

N = 2

V_1 = .02 from figure 14

V_2 = .48 from figure 14

$$\text{Impulse response ringing} = \frac{V_1}{V_2} \times 100 = \frac{.02}{.48} \times 100 = 4.1\%$$

A three-pole .5 dB Chebyshev design has an impulse response of 21%.

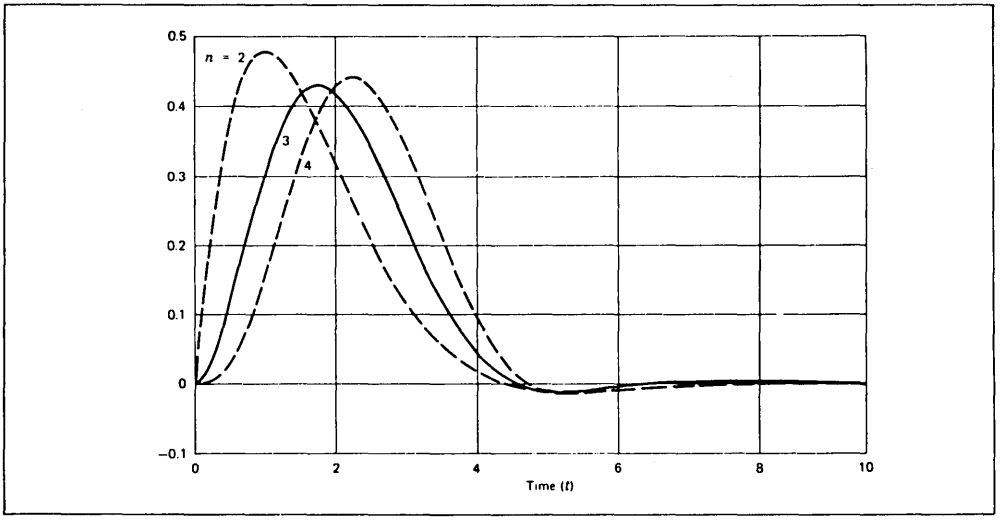


Figure 14. Impulse Response for Linear Phase (Phase Error = .5°) Filters

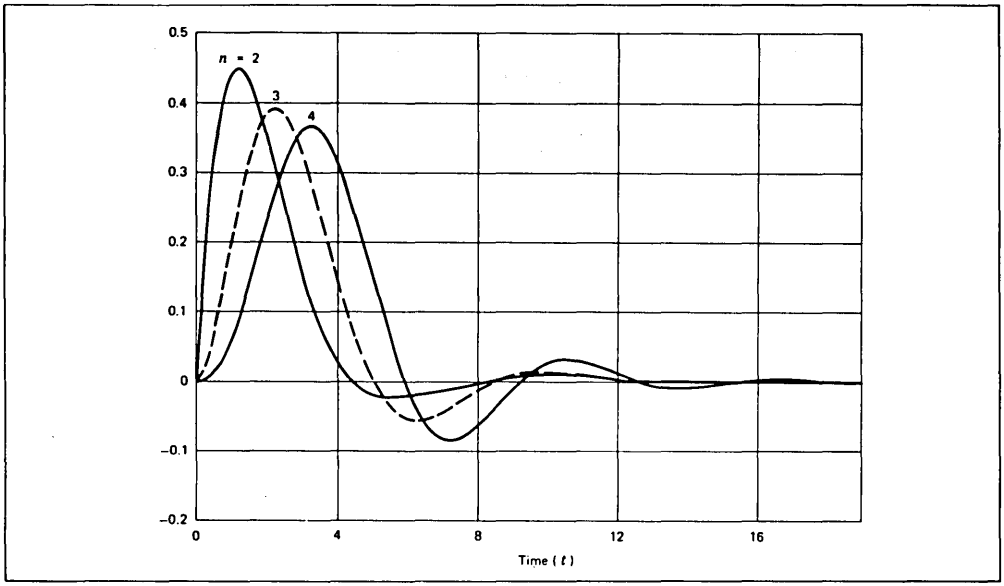


Figure 15. Impulse Response for Chebyshev Filters with 0.01 dB Ripple

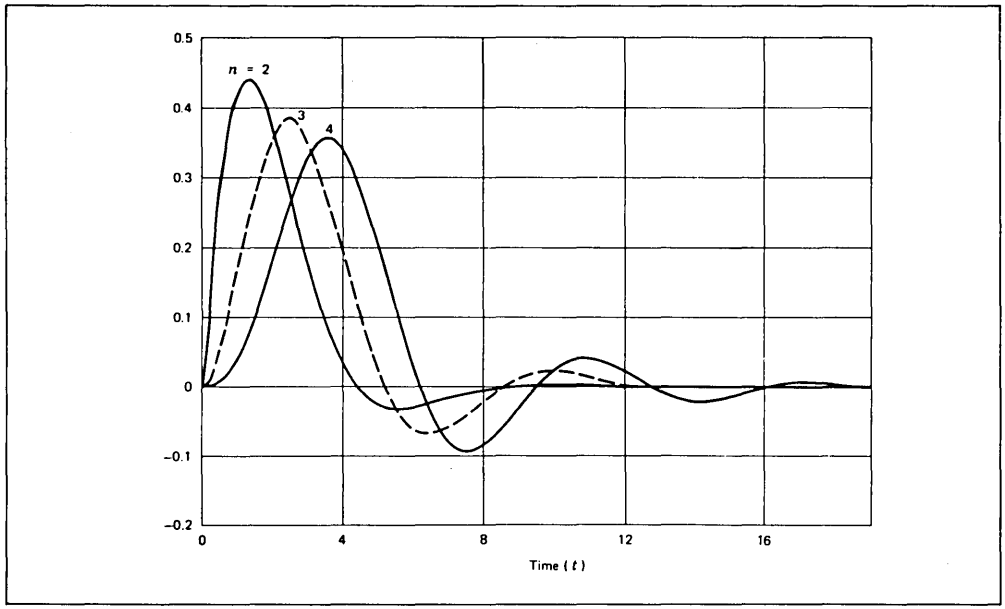


Figure 16. Impulse Response for Chebyshev Filters with 0.1 dB Ripple

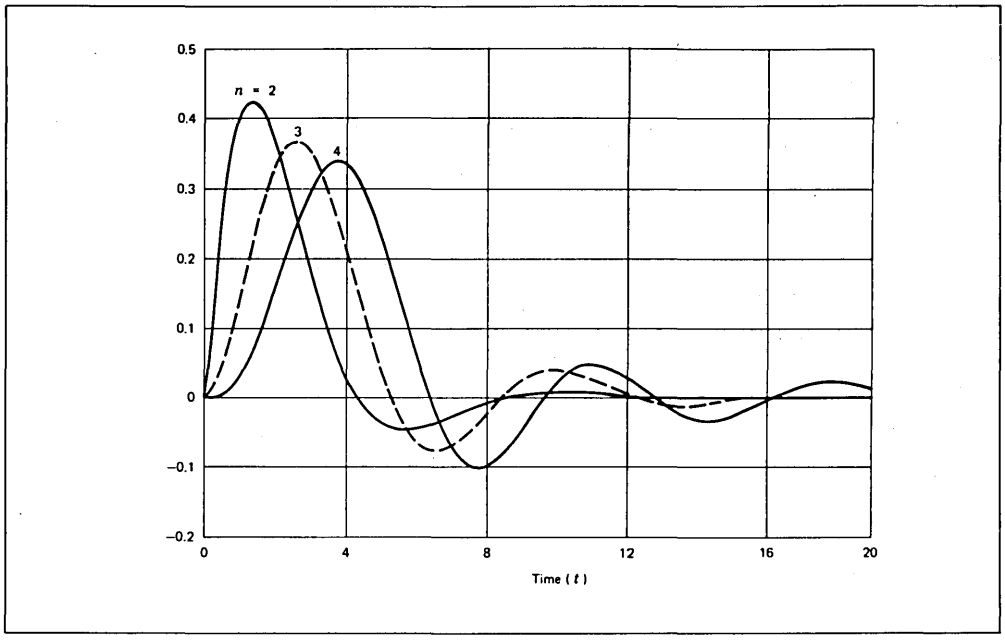


Figure 17. Impulse Response for Chebyshev Filters with 0.5 dB Ripple

2.7 Spurious Responses

Mechanical filters have resonant frequency overtones very similar to those found in quartz crystals. These overtones occur at multiples of the fundamental; the multiples are 2.4, 4.8, 7.6, 10.6, etc.

As an example, a mechanical filter designed for Omega navigation system applications at 10.2 kHz will have spurious responses (frequency overtones) at 24.5, 49, 77.5 and 108 kHz.

These overtones are inherent to the flexure mode of vibration used in the design of low-frequency mechanical filters. They cannot be suppressed without compromising the filter design. The odd-numbered modes, 2.4 and 7.6, are normally 50 dB below the fundamental. Suppression of these occurs because of the transducer coupling method utilized to drive the fundamental mode. The even-numbered overtones, 4.8, 10.6, have levels approximately 15 dB below the fundamental. These modes cannot be suppressed internally, however, a low-pass filter can be used to reject these higher frequency modes. Another alternative is the use of a bandpass "roofing" filter. See figure 22. The 'roofing' filter will reject both the low frequency microphonic and the high frequency spurious responses. It should be placed after the mechanical filter i.e., the incoming signal should go through the mechanical filter first, then through the 'roofing' filter. In this way, the microphonic responses are rejected as well as the spurious responses. The 'roofing' filter should be compatible with the mechanical filter; it should not affect its passband response.

2.8 Aging

Aging is defined herein as the change of center frequency with time. Since insertion loss and bandwidth do not change an appreciable amount, they will not be considered.

The low frequency mechanical filter has four components and processes which are likely to contribute to aging problems: the nickel-iron alloy bar, the ceramic transducer, the solder bond between the bar and transducer and the welds that connect the coupling wires to the bars. When heat treated properly, the nickel-iron alloy bar is very stable. Because its mass is much greater than any of the other components, the stability of the bar helps to compensate for the instability of the ceramic and solder bond.

Since the aging characteristics of low frequency mechanical filters are dependent on the ratio of the ceramic transducer mass to the nickel-iron alloy bar mass, the rate of aging for various types of filters is not only dependent on the center frequency, but perhaps, to a greater extent, on the design bandwidth of the filter. The narrower the bandwidth, the smaller the ceramic transducer need be. This means that the narrower bandwidth filters will age, as a percentage of their center frequency, less than wider bandwidth filters at the same frequency.

The aging rate of a mechanical filter is predictable and always in the positive direction. The aging (Δ f) of a filter can be computed using the following equation, where t is the time in days, BW is the 3 dB bandwidth in Hertz and t_o is 10 days, the time required to manufacture a mechanical filter.

$$\Delta f = .02\ BW\ (\text{Log}\ \frac{t}{to})$$

For example: A 12 kHz filter which is 50 Hz wide at 3 dB after 5 years will have aged:

$$\Delta f = .02\ (50)\ \text{Log}\ \frac{5(365)}{10} = 2.26\ \text{Hz}$$

2.9 Reliability

The MTBF (mean time between failures) is 3×10^7 hours. This is based on field data which was accumulated over a period of several years.

3.0 Environmental Effects

3.1 Temperature Effect on Center Frequency, Loss and Bandwidth

Design techniques for low frequency mechanical filters utilize compensating factors which minimize the shift of the filter center frequency with a change in temperature.

The center frequency shift vs. temperature is normally compensated to a tolerance of $\pm$ 10 ppm/°C over a temperature range of −20°C to +65°C. The tolerance can be as high as $\pm$ 25 ppm/°C for the largest fractional bandwidth filters. The filters may be used over larger temperature ranges, such as −55°C to +95°C without any physical damage or permanent effect on the frequency response characteristics.

The variation of insertion loss with temperature is typically $\pm$ 1 dB (with a maximum variation of $\pm$ 1.5 dB) over a temperature range of −20°C to +65°C. The narrower the filter bandwidth the smaller the insertion loss variation.

Bandwidth normally changes very little with temperature in absolute terms. A typical variation for a filter with a 100 Hz bandwidth would be 1.5 Hz over a temperature range of +25°C to +65°C. This is a bandwidth shift of +375 ppm/°C.

The variations in center frequency, loss and bandwidth due to temperature change are temporary in nature; the filter will return to its original condition when the temperature is restored to +25°C.

3.2 Shock

A resilient rubber shock mount is used to isolate the mechanical filter structure from shock forces which could cause damage. This mount allows the average filter to withstand 100 G, 6msec, shocks without a change in the filter response. Certain mechanical filters can withstand 1500 G's of shock before permanent damage occurs.

3.3 Vibration

The internal shock mount, that so effectively isolates the filter from shock, also does an excellent job against vibration forces. The average filter will safely withstand a constant 10 G vibration level between 10 to 2000 Hz. At approximately 15 G's the elastic limit is reached causing the filter to become permanently damaged.

Often it is not only important that a filter survive a specific vibration level, but it is also important that it retains the proper response characteristics during the vibration. While the attenuation response shows little change, there is some variation of phase and some microphonic effects during vibration. These are important characteristics in applications like Omega navigation systems.

The variation of phase of an Omega filter as a function of vibration frequency is shown in figure 18. It will be noticed that there is a peak deviation point around 400 Hz. The reason for the peak is that the entire filter structure has a resonance at this point. This structural resonance also has an effect on the microphonic noise level.

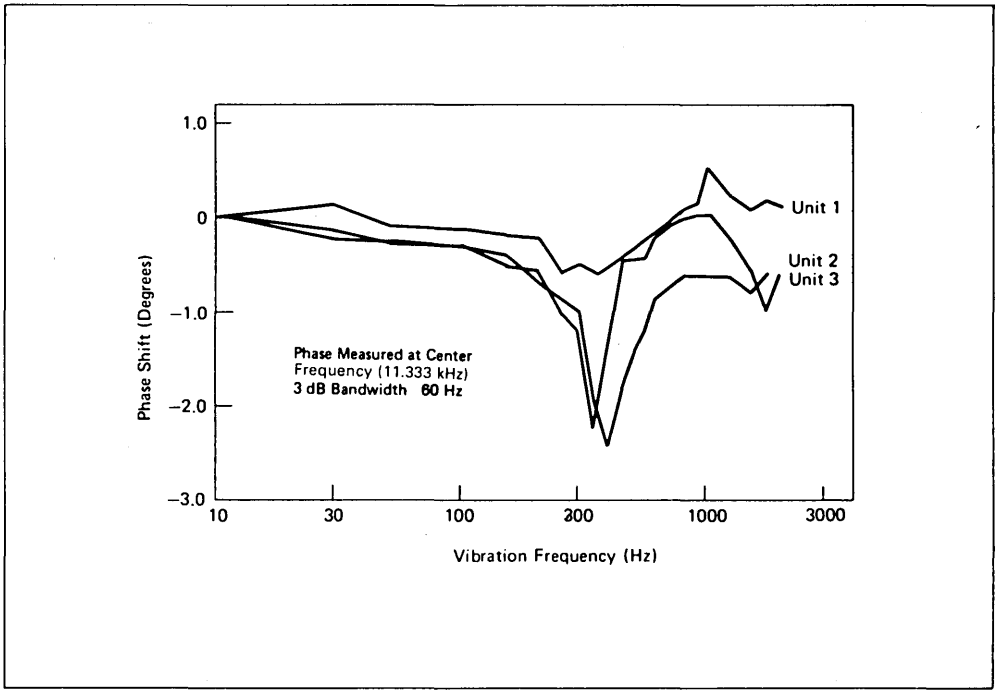


Figure 18. Variation in Phase with External Vibration (10 G Level)

Figure 19 illustrates the levels of microphonic responses of a 100 Hz bandwidth Omega filter. These levels were measured while the filter was vibrated at a constant 5 G level over the frequency range of 50 to 4000 Hz. The maximum output occurred at 525 Hz at a level of −50 dBv.

In applications where these levels are intolerable, special structural designs can be incorporated into the equipment in order to dampen the vibrations around 500 Hz. Methods such as mounting the filter near a brace or an equipment corner, using a low-Q rubber or elastomer as an external filter mount and other vibration suppression techniques will help in limiting the phase shift and amplitude response microphonics.

A successful technique for attenuation of the low frequency microphonic responses is the use of a highpass filter network. These filters are placed in the signal path between the mechanical filter and the detector. Figures 20, 21 and 22 illustrate 3 types of filters which may be used to reduce microphonic responses. They differ in the type and number of components required. The improvement in microphonic amplitude response as a result of using these filters is presented in figures 23 through 26.

The filter circuit of figure 20 will attenuate the microphonic level by approximately 15 dB. It is a single section consisting of 1 reactive component, however, it will not attenuate any spurious frequencies above the filter passband.

The high-pass circuit of figure 21 consists of 3 reactive components and will attenuate only frequencies below 9 kHz. This LC circuit provides 60 dB of rejection at microphonic frequencies.

A "roofing" bandpass filter may be used to attenuate both the spurious modes at high frequencies and the microphonic signals at low frequencies. One circuit which may be used appears in figure 22. The complexity of this circuit is a function of how much attenuation is required by the user, i.e., additional sections provide greater attenuation.

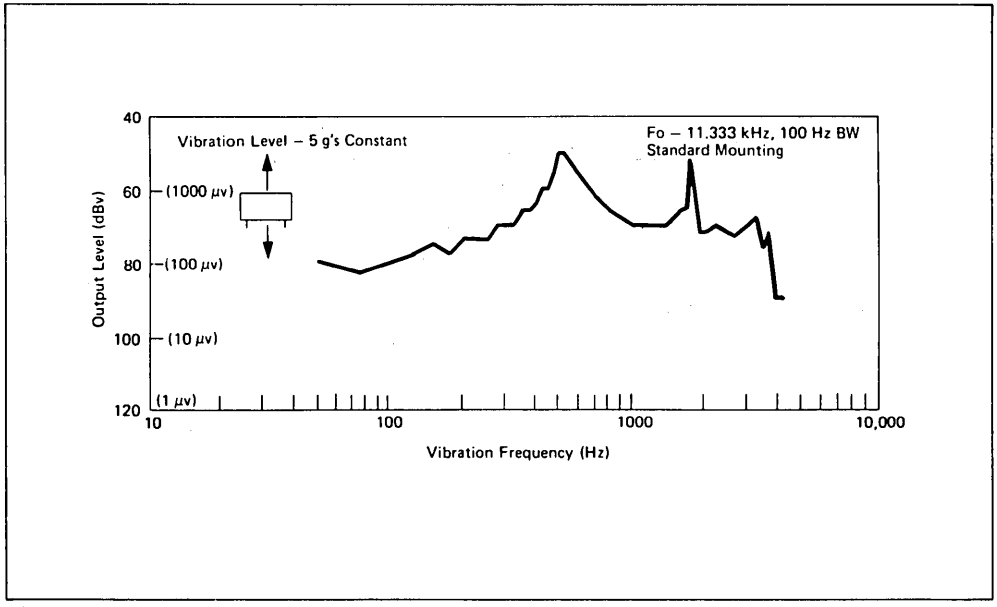


Figure 19. Omega Filter Microphonic Response

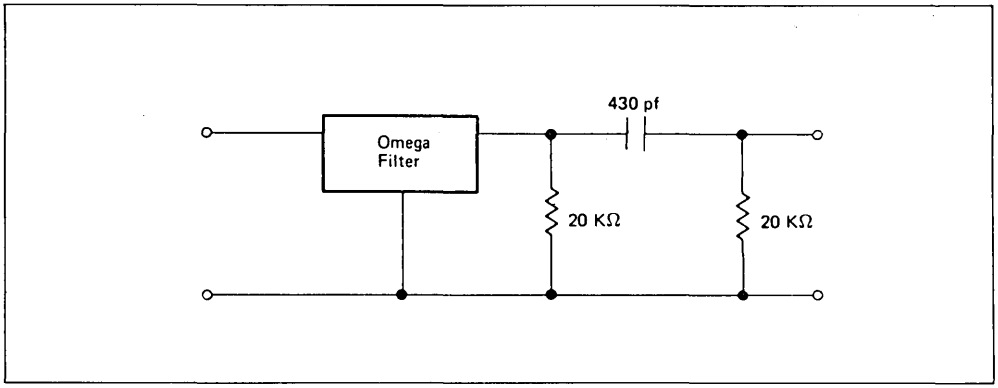


Figure 20. RC High-Pass Filter

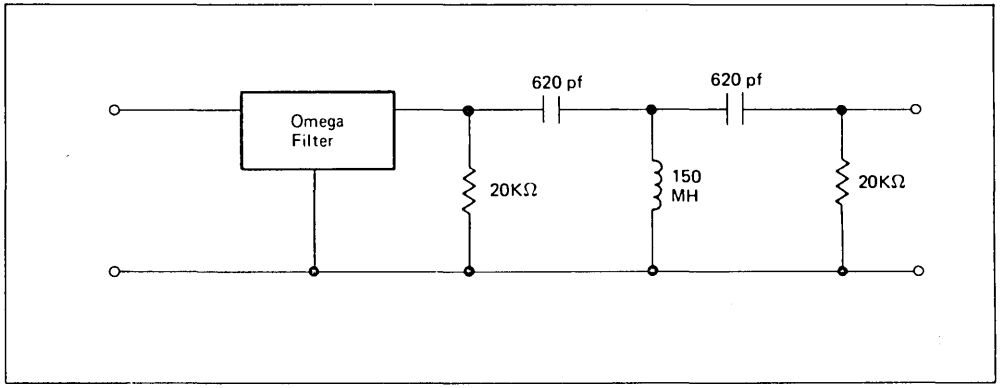


Figure 21. LC High-Pass Filter

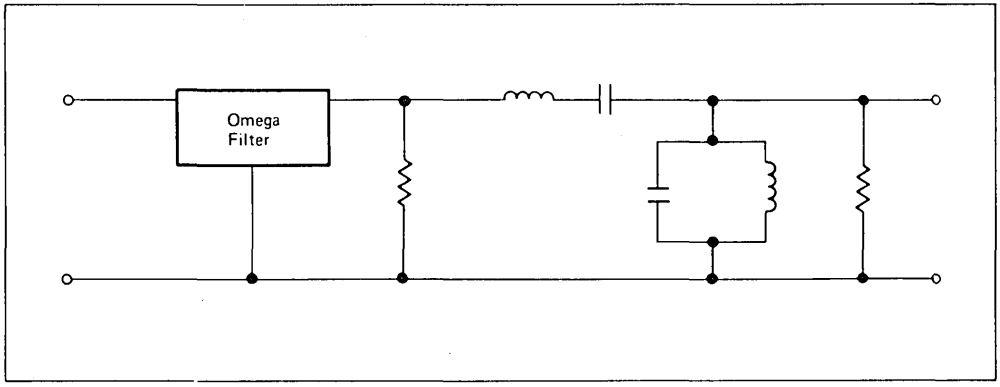


Figure 22. Bandpass Filter

3.4 Moisture Resistance

The four available low-frequency mechanical filter enclosures have been tested to MIL-STD-202, method 106. This strenuous test is used to evaluate materials which are subjected to high humidity tropical environments.

The test consists of ten days at 90–95% humidity with the temperature being cycled from −10°C to +65°C. At the end of each 24 hr. cycle, the filter enclosures are vibrated at a 9 G level.

Two enclosures, 'LC' and 'FP', passed the test without a change in the filter response or the enclosure. Although the all-plastic 'LC' enclosure passed the test, it should receive additional moisture protection, such as "post coat", if the filter is to be subjected to this type of environment for a long period of time. The additional moisture barrier is necessary because most plastics are permeable to moisture, therefore, there would be an eventual effect on the filter response. No precautions need to be taken with the all-metal 'FP' enclosure.

The plastic 'PA' and 'FS' enclosures were also subjected to the above moisture test. On these, the epoxy seal around the cases showed signs of degradation and cracking. Moisture apparently enters the filters through the damaged seal, however, the filter response was unchanged and the filters functioned normally. It is not recommended that these enclosures be used in tropical environments because of the possibility of seal failure.

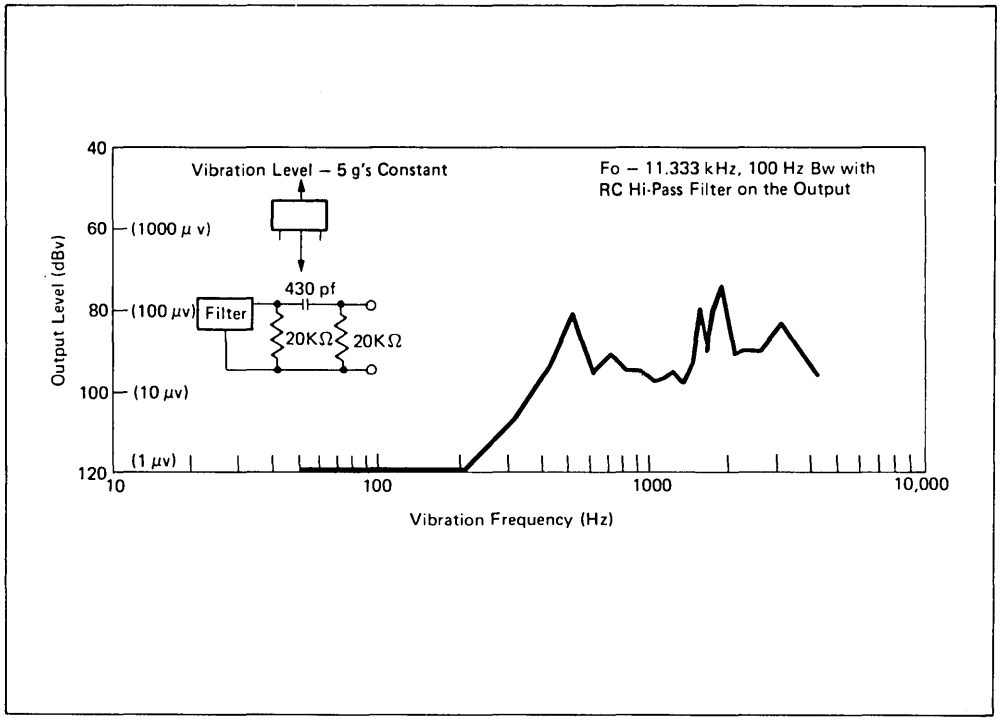


Figure 23. Omega Filter Microphonic Response

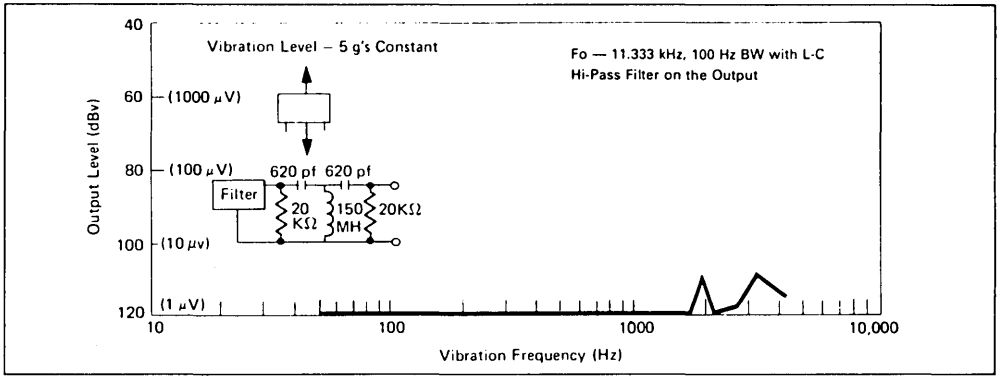


Figure 24. Omega Filter Microphonic Response

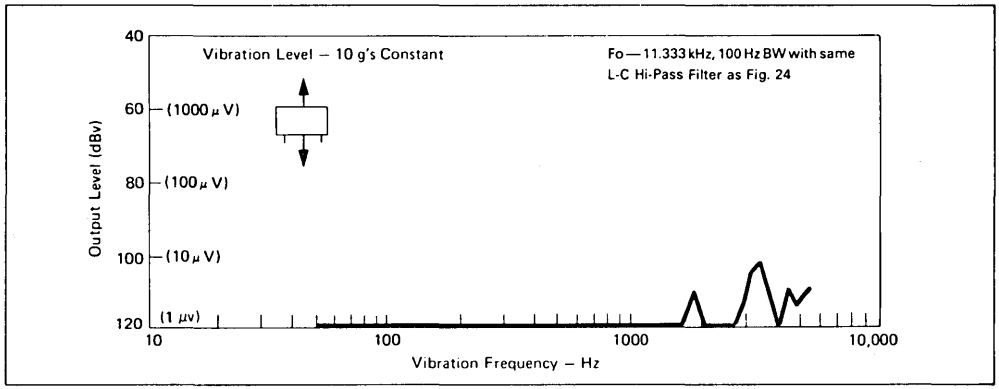


Figure 25. Omega Filter Microphonic Response

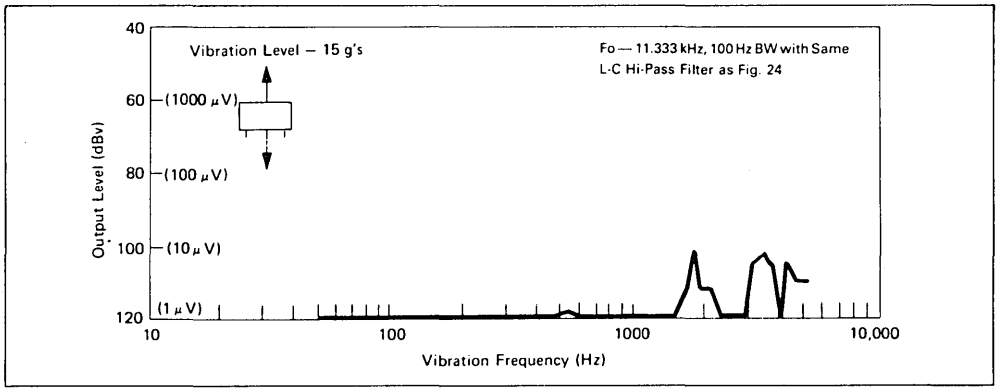


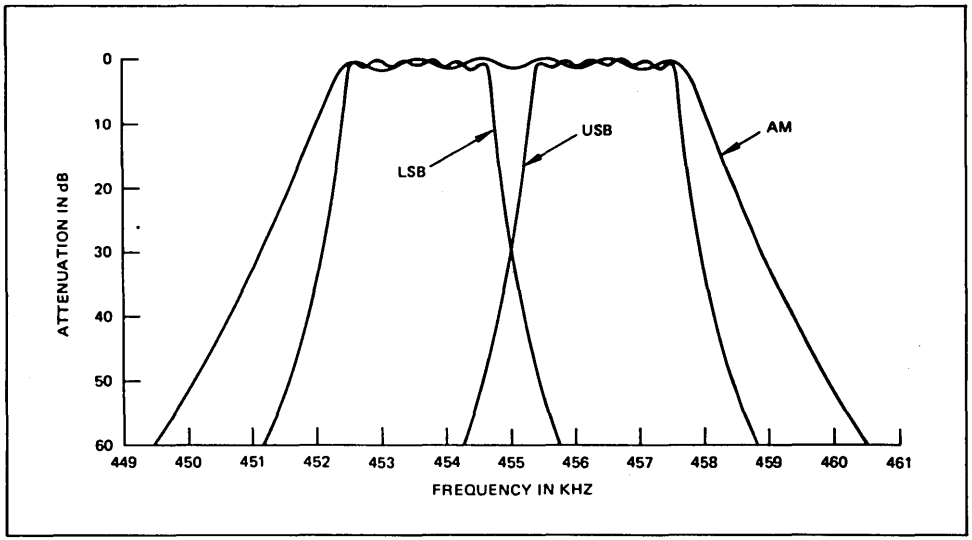
Figure 26. Omega Filter Microphonic Response

DOCUMENT NO. FD-05
FEBRUARY 1980

Rockwell

FILTER PRODUCTS DATA SHEET

COLLINS USB-LSB-AM MECHANICAL FILTERS



Rockwell-Collins Filter Products offers a complete set of mechanical filters for the communication radio service. Either upper or lower sideband filters plus a super-selective AM filter are available. The unique design features of the original upper sideband filter are incorporated into all three of these filters. You get the inherent stability with time and environmental change of all Rockwell-Collins Mechanical Filters, along with low volume prices. Here is a very cost-effective package for the ultimate SSB and AM radio.

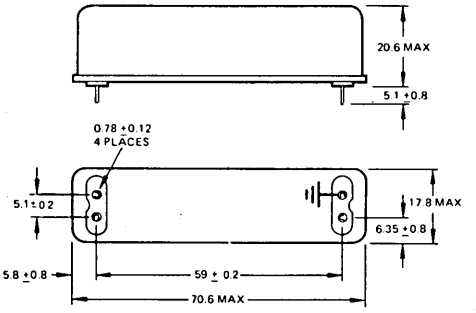
These filters incorporate quality features that have made Collins Mechanical Filters famous. The disk resonators are made from specially processed Ni-Span "C", so that filter frequency shift with change in temperature is minimized. For example, over the temperature range of -30°C to +50°C a typical value of total frequency shift for the carrier side 3 dB point of a sideband filter would be 45 Hz. Custom-made ferrite transducers keep the insertion loss low. Normal welded construction is used for the filter assembly. The result is a trio of filters that are very stable with time and/or temperature and have the high performance characteristics needed for minimum interference operations.

The curves shown here illustrate the typical response characteristics of the three filters. Even with the exceptional selectivity and stability of these fine filters, they are competitively priced in volume. Contact your local Rockwell Sales Representative and find out how little it costs to use the best.

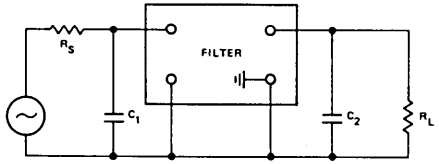
COLLINS USB-LSB-AM MECHANICAL FILTERS

Specifications subject to change without notice

DIMENSIONS (mm)



FILTER TEST CIRCUIT



FOR SIDEBAND FILTERS:
R_S = R_L = 2700 OHMS
FOR AM FILTER:
R_S = R_L = 12,000 OHMS
FOR ALL THREE FILTERS:
C_1 = C_2 = 360 pf

The filters were designed with the input balanced and the output unbalanced, so that the radio designer can operate them in a balanced modulator circuit (or any other balanced circuit). Either end may be used as input (or output) but only one end is balanced. Both ends of the sideband filters should be terminated with 2700 ohms resistance, with the filter terminals shunted by 360 pf of capacitance. The AM filter should be terminated with 12,000 ohms resistance and 360 pf of capacitance.

Part Numbers are: 526-9897-010, USB
526-9939-010, LSB
526-9920-010, AM

FURTHER INFORMATION

For technical information on Rockwell filter products or to discuss a filter to your specifications, contact

Rockwell International
Filter Products
4311 Jamboree Road
Newport Beach, CA 92660

Phone 714/833-4632 or contact your local Rockwell Representative.

TYPICAL PERFORMANCE CHARACTERISTICS:

Parameter	Filter Type	Min.	Typ.	Max.	Units
3 dB Bandwidth	USB/LSB	1,950	2,200		Hz
	AM	5,000	5,500		Hz
60 dB Bandwidth	USB/LSB		4,500	5,500	Hz
	AM		11,000	13,000	Hz
Insertion Loss	USB/LSB		3.5	8	dB
	AM		8	12	dB
Passband Response Variation	USB/LSB		1	3	dB
	AM		2.5	3.5	dB

DOCUMENT NO. FD-06
MARCH 1980

Rockwell

FILTER PRODUCTS DATA SHEET

F455FD SERIES LOW-COST MECHANICAL FILTERS

Rockwell-Collins' low cost F455FD-series of Mechanical Filters takes full advantage of advances in manufacturing techniques to realize superior performance at a modest price for manufacturers of SSB, AM and CW communications equipment. An additional saving in cost is achieved by writing worst-case limit specification requirements which are suitable for the intended applications, and then over-designing the filters to minimize costly inspection and test procedures. As an example, actual insertion loss values are typically 5 or 6 dB, while the specified maximum is 10 dB. Actual 60 dB to 3 dB bandwidth ratios are typically 2 to 1 while the specified maximum ratios range from 2.3-to-1 to 3.3-to-1. Actual response variation values are typically 1 to 1.5 dB, while the specified maximum is 3 dB.

RECOMMENDED OPERATING PARAMETERS

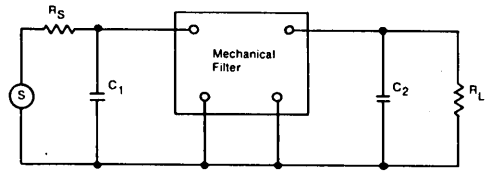
All seven of the filters in the F455FD-series are designed to operate with 2,000-ohm source and load resistances, and need to be parallel-tuned with a fixed capacitance, the value of which can vary ±5% from nominal with negligible effect on the filter performance. This makes for easy and inexpensive assembly in production radios. The signal input voltage should not exceed 2 volts RMS.

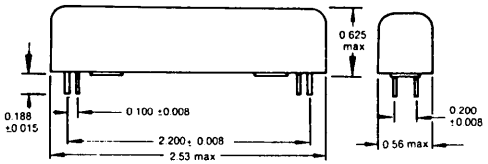
A common ground connection and effective shielding between the input and the output must be used to obtain full advantage of the Mechanical Filter's selectivity.

The filters are normally used inter-stage. Used in an IF stage of a receiver, or the modulator stage in an exciter, the filter eliminates the need for additional selectivity components, and permits simplified circuit design and production tuning procedures.

ELECTRICAL CHARACTERISTICS

Part and Type Numbers	Minimum 3 dB BW @ 25°C (kHz)	Minimum 4 dB BW OTR (kHz)	Maximum 60 dB BW @ 25°C (kHz)	Maximum 60 dB BW OTR (kHz)	C_1, C_2 Res Cap ±5% (pf)
526-9689-010 F455FD-04	0.375	0.375	3.5	4.0	350
526-9690-010 F455FD	1.2	1.2	8.7	9.5	350
526-9691-010 F455FD-19	1.9	1.9	5.4	5.9	330
526-9692-010 F455FD-25	2.5	2.5	6.5	7.0	510
526-9693-010 F455FD-29	2.9	2.9	7.0	8.0	510
526-9694-010 F455FD-38	3.8	3.8	9.0	10.0	1000
526-9695-010 F455FD-58	5.8	5.8	14.0	15.0	1100





Termination circuits should be designed to eliminate DC currents and voltages from the filter. Satisfactory results may be obtained with current up to 2 ma DC, but in no case to exceed 3 ma DC. DC voltage should not exceed 100 volts DC.

ENVIRONMENTAL SPECIFICATIONS

Shock. . . . . .MIL-STD-202, Method 202
Vibration. . . . . .MIL-STD-202, Method 201
Operating Temperature Range (OTR) . . . . . -10°C to +60°C

COMMON CHARACTERISTICS:

Maximum Ripple Voltage
@ 25°C. . . . . .3.0 dB
Operating Temperature Range (OTR) . . . . . .4.0 dB

Maximum Insertion Loss
@ 25°C. . . . . .10.0 dB
Operating Temperature Range (OTR) . . . . . .12.0 dB

Minimum 60 dB Stop Band Range . . . . . 445 kHz to F60L
F60H to 465 kHz

R_S and R_L, ±5% 2,000Ω

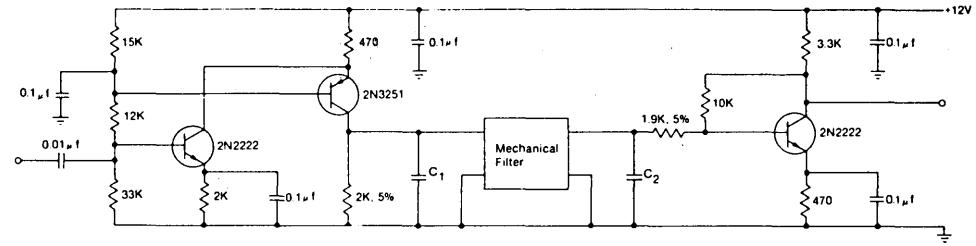
F455FD SERIES LOW-COST MECHANICAL FILTERS

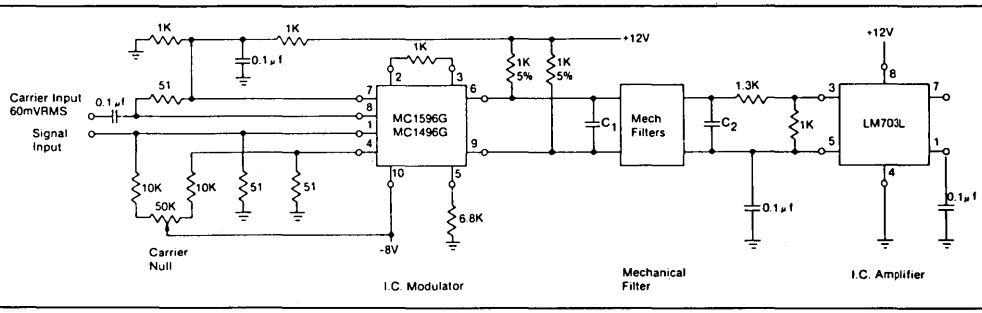
FILTER PRODUCTS

Specifications subject to change without notice

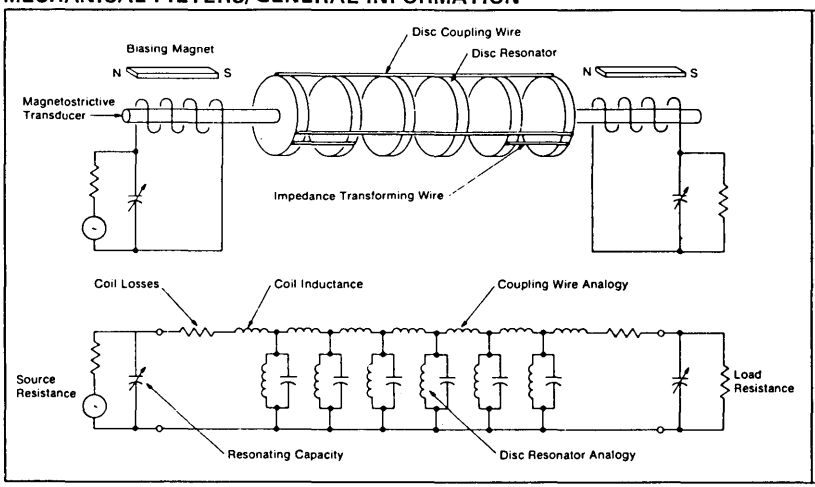
APPLICATION EXAMPLES

Transistor Amplifier





MECHANICAL FILTERS/GENERAL INFORMATION



The Rockwell-Collins Mechanical Filter is a mechanically resonant device which receives an electrical signal, converts this signal into mechanical vibrations, rejects unwanted frequencies within the mechanical structure, and then converts the mechanical vibration back into electrical energy. The filter consists of three basic elements: (1) transducers which convert electrical signals into mechanical vibrations, (2) high Q mechanically resonant metal discs, and (3) disc coupling wires. The multi-element filter shown in the diagram illustrates how the center frequency is determined by the discs. Each disc is represented by a parallel resonant circuit.

Applications for the wide range of standard filters include single sideband, high performance transmitting and receiving equipment, multiplexing equipment, missile guidance systems, precision navigation equipment, spectrum analyzers, FM communications receivers, CB transceivers, and others.

FURTHER INFORMATION

For technical information on Rockwell filter products or to discuss a filter to your specifications, contact

Rockwell International
Filter Products
4311 Jamboree Road
Newport Beach, CA 92660

Phone 714/833-4632 or contact your local Rockwell Representative.

Disc-Wire Mechanical Filters
Standard Products and Specifications

Cntr. Freq. (kHz)	Part Number	Typical P/B (kHz/dB)	Typical Stopband (kHz/dB)	Source & Load K ohms	Res Cap. (pf)	Func-tion	Case Style
256	526-9700-010	3.6/1.0	8.4/600	5.0	350	LSB	Spec
300	526-9311-000	2.95/2.5	5.2/60	100.0	110	LSB	L Spec
300	526-9312-000	2.95/2.5	5.2/60	100.0	110	USB	L Spec
450	526-9963-010	0.320/3.0	1.2/60	5.0	180	CW	HS
450	526-9963-020	0.650/3.0	2.1/60	5.0	270	CW	HS
450	526-9963-030	1.2/3.0	3.1/60	5.0	110	BP	HS
450	526-9963-040	3.4/3.0	6.0/60	5.0	360	BP	HS
450	526-9963-060	6.8/3.0	1.5/60	5.0	750	BP	HS
450	526-9643-010	6.0/6.0	23.0/60	20.0	30	BP	V
450	526-9643-030	6.75/6.0	23.0/60	20.0	30	BP	V
450	526-9776-010	8.0/6.0	31.0/60	20.0	30	BP	V
450	526-9901-010	2.35/6.0	4.0/60	20.0	30	USB	V
450	526-9902-010	2.35/6.0	4.0/60	20.0	30	LSB	V
450	526-9955-010	2.8/3.0	4.6/60	5.0	30	USB	FD
450	526-9956-010	2.8/3.0	4.6/60	5.0	30	LSB	FD
450	526-9923-010	2.8/3.0	4.5/60	5.0	30	USB	FD
450	526-9924-010	2.8/3.0	4.5/60	5.0	30	LSB	FD
450	526-9678-010	3.35/2.0	4.75/60	20.0	30	USB	V
450	526-9679-010	3.35/2.0	4.75/60	20.0	30	LSB	V
450	526-9936-010	6.1/3.0	8.7/50.0	2.0	30	LSB	FA
450	526-9937-010	6.1/3.0	8.7/50.0	2.0	30	USB	FA
455	526-9764-010	0.2/3.0	2.4/60	5.0	50	CW	V
455	526-9689-010	0.525/3.0	3.5/60	2.0	350	CW	FD
455	526-9494-000	0.5/6.0	3.0/60	100.0	130	CW	FA
455	526-9521-000	0.5/6.0	3.0/60	100.0	130	CW	Y
455	526-9765-010	0.5/3.0	3.5/60	5.0	200	CW	V
455	526-9446-000	0.90/6.0	4.0/60	100.0	130	CW	FA
455	526-9770-010	1.175/3.0	6.0/60	5.0	100	BP	V
455	526-9690-010	1.35/3.0	8.0/60	2.0	350	BP	FD
455	526-9495-000	1.50/6.0	3.5/60	100.0	130	BP	FA
455	526-9691-010	2.05/3.0	5.4/60	2.0	330	BP	FD
455	526-9337-000	2.1/6.0	5.3/60	100.0	130	BP	Y
455	526-9427-000	2.1/6.0	5.3/60	100.0	130	BP	FA
455	526-9766-010	2.25/3.0	6.3/60	5.0	130	BP	V
455	526-9860-010	2.8/3.0	11.75/70	2.0	1500	BP	V
455	526-9692-010	2.8/3.0	6.5/60	2.0	510	BP	FD
455	526-9904-010	2.65/3.0	7.0/60	2.0	510	BP	V
455	526-9500-000	2.3/3.0	6.2/60	100.0	130	BP	FA
455	526-9693-010	3.05/3.0	7.0/60	2.0	510	BP	FD
455	526-9772-010	3.0/3.0	9.0/60	5.0	50	BP	V
455	526-9496-000	3.1/6.0	6.5/60	100.0	130	BP	FA
455	526-9338-000	3.1/6.0	6.5/60	100.0	130	BP	Y
455	526-9694-010	3.95/3.0	9.0/60	2.0	1000	BP	FD
455	526-9339-000	4.0/6.0	8.5/60	100.0	130	BP	Y
455	526-9639-010	4.0/6.0	8.5/60	0.750	130	BP	Y
455	526-9767-010	4.0/3.0	12.0/60	5.0	470	BP	V
455	526-9497-000	4.0/6.0	8.5/60	100.0	130	BP	FA
455	526-9920-010	5.5/3.0	13.0/60	12.0	360	BP	HS
455	526-9930-010	5.8/4.0	12.0/63	3.0	820	BP	YA
455	526-9695-010	5.95/3.0	14.0/60	2.0	1100	BP	FD
455	526-9498-000	6.0/6.0	12.6/60	100.0	130	BP	FA
455	526-9522-001	6.0/3.5	25.0/60	100.0	130	BP	FA
455	526-9340-000	6.0/6.0	12.6/60	100.0	130	BP	Y
455	526-9773-010	6.0/3.0	18.0/60	5.0	750	BP	V
455	526-9341-000	8.0/6.0	18.5/60	100.0	130	BP	Y
455	526-9768-010	8.0/3.0	24.0/60	5.0	680	BP	V
455	526-9774-010	12.0/3.0	36.0/60	5.0	—	BP	V
455	526-9667-010	15.0/6.0	30.0/60	0.500	See Spec	BP	T
455	526-9343-000	16.0/6.0	27.5/60	100.0	130	BP	Y
455	526-9769-010	16.0/3.0	30.0/60	5.0	1100	BP	V

Cntr. Freq. (kHz)	Part Number	Typical P/B (kHz/dB)	Typical Stopband (kHz/dB)	Source & Load K ohms	Res. Cap. (pf)	Func-tion	Case Style
455	526-9605-010	1.85/3.0	5.0/60	100.0	130.0	USB	FA
455	526-9606-010	1.85/3.0	5.0/60	100.0	130.0	LSB	FA
455	526-9897-010	2.1/3.0	6.25/60	2.7	360	USB	HS
455	526-9939-010	2.1/3.0	6.25/60	2.7	360	LSB	HS
455	526-9967-010	2.3/3.0	4.8/60	1.0	30	USB	YA
455	526-9870-010	2.4/3.0	5.35/60	2.0	680	USB	V
455	526-9724-010	2.65/6.0	4.3/60	2.0	700	USB	FA
455	526-9640-010	2.8/3.0	7.5/60	0.750	130	LSB	Y
455	526-9641-010	2.8/3.0	7.5/60	0.750	130	USB	Y
455	526-9958-010	3.15/3.0	4.9/60	5.0	270	LSB	HS
455	526-9959-010	3.15/3.0	4.9/60	5.0	270	USB	HS
455	526-9364-000	3.0/3.0	6.0/60	100.0	130	USB	Y Long
455	526-9365-000	3.0/3.0	6.0/60	100.0	130	LSB	Y Long
455	526-9903-010	3.2/1.5	4.9/40	2.0	30	LSB	FD
455	526-9698-010	3.3/3.0	4.8/40	2.0	30	USB	FD
455	526-9699-010	3.0/3.0	4.8/40	2.0	30	LSB	FD
455	526-9899-010	3.0/3.0	4.9/60	2.0	30	LSB	V
455	526-9900-010	3.0/3.0	4.9/60	2.0	30	USB	V
455	526-9892-010	3.3/3.0	4.75/60	2.0	30	USB	V
455	526-9783-010	6.3/3.0	8.7/50	2.0	30	LSB	V
455	526-9784-010	6.3/3.0	8.7/50	2.0	30	USB	V
500	526-9588-010	0.8/3.0	3.0/60	S=1.0 L=0.330	See Spec	CS	Y Flange
500	526-9719-010	1.15/3.0	5.6/60	2.0	30	BP	V
500	526-9717-010	3.3/3.0	7.0/60	2.0	30.0	BP	V
500	526-9717-020	3.3/3.0	7.0/60	2.0	30.0	BP	FD
500	526-9378-000	6.4/3.0	13.2/60	100.0	120.0	BP	Y
500	526-9718-010	6.3/3.0	13.0/60	2.0	30.0	BP	V
500	526-9646-010	8.3/3.0	20.0/40	1.0	51	BP	V
500	526-9663-010	1.8/2.0	5.38/60	20.0	160	USB	Y Long
500	526-9664-010	1.8/2.0	5.38/60	20.0	160	LSB	Y Long
500	526-9663-020	2.3/3.0	4.30/60	20.0	160	USB	FD
500	526-9906-010	2.34/6.0	4.6/60	3.0	180	LSB	FD
500	526-9906-020	2.34/6.0	4.6/60	3.0	180	LSB	YA
500	526-9414-000	2.7/3.0	6.1/60	100.0	120	USB	Y
500	526-9415-000	2.7/3.0	6.1/60	100.0	120	LSB	Y
500	526-9616-010	2.7/3.5	6.1/60	100.0	120	LSB	V
500	526-9376-000	3.0/3.0	5.8/60	100.0	105	LSB	Y
500	526-9377-000	3.0/3.0	5.8/60	100.0	105	USB	Y
500	526-9873-010	2.85/3.0	6.5/60	20.0	100	USB	YA
500	526-9874-010	2.85/3.0	6.5/60	20.0	100	LSB	YA
500	526-9927-010	3.3/3.0	6.5/60	20.0	100	USB	Y
500	526-9928-010	3.3/3.0	6.5/60	20.0	100	LBS	Y
500	526-9644-010	3.35/3.0	5.9/50	1.0	20	USB	V
500	526-9645-010	3.35/3.0	5.9/50	1.0	20	LSB	V
500	526-9968-010	4.6/3.0	6.75/50	1.0	20	USB	V
500	526-9711-010	6.3/3.0	10.5/50	1.0	30	LSB	V
500	526-9712-010	6.3/3.0	10.5/50	1.0	30	USB	V

FURTHER INFORMATION

For technical information on Rockwell filter products or to discuss a filter to your specifications, contact

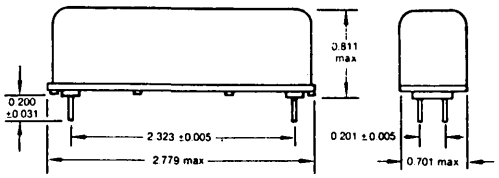
Rockwell International
Filter Products
4311 Jamboree Road
Newport Beach, CA 92660

or phone 714/833-4324 or 714/833-4544. To order, phone 714/833-4632 or contact your local Rockwell Representative.

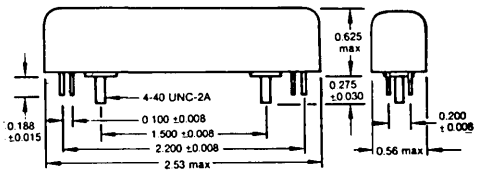
DOCUMENT NO. F-02
REV. 1, FEBRUARY 1980

Disc-Wire Mechanical Filters Case Styles

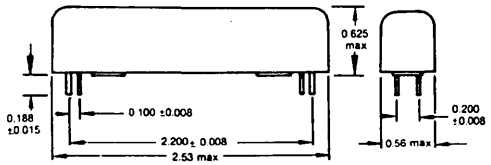
Case Style HS



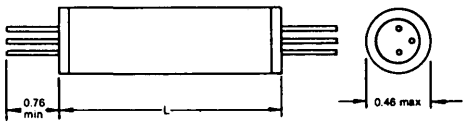
Case Style FA



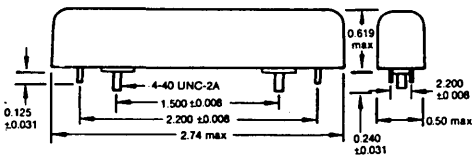
Case Style FD



Case Style YA

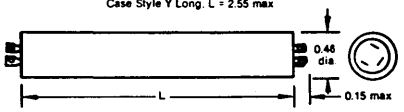


Case Style V

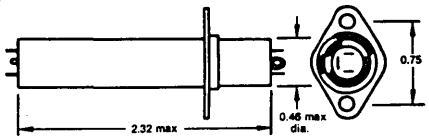


Case Style Y

Case Style Y, L = 2.23 max
Case Style Y Long, L = 2.55 max



Case Style Y with Flange

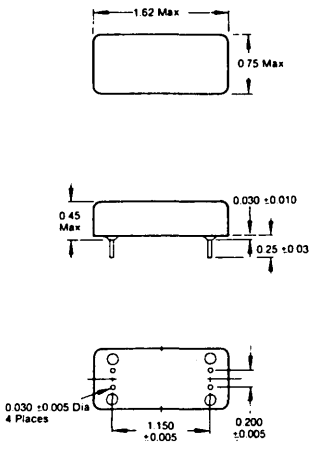


Low Frequency Narrowband Mechanical Filters
Standard Products and Specifications

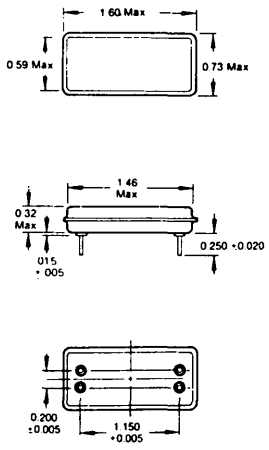
Center Frequency (kHz)	Part Number	Nom Passband Width (Hz/dB)	Max. Stopband Width (Hz/dB)	Max. Ripple 25°C (dB)	Nom IL dB 25°C	Number of Resonators	Source and Load (K ohms)	O.T.R. (°C)	Case Style
3.821	526-9714-010	52/3	204/23	1	2.5	2	33	+10/70	PA
3.821	526-9918-010	52/3	204/23	1	2.5	2	33	+10/70	LC
3.840	526-9886-010	45/3	163/20	1	2.5	2	33	+10/70	PA
5.182	526-9799-010	25/3	110/25	1	2.5	2	33	0/55	PA
5.182	526-9875-010	25/3	110/25	1	2.5	2	33	0/55	FS
5.328	526-9752-010	45/3	540/30	0.5	2.5	2	9.2	-20/85	FP
5.598	526-9801-010	25/3	110/25	1	2.5	2	30	0/55	PA
5.598	526-9876-010	25/3	110/25	1	2.5	2	30	0/55	FS
5.840	526-9803-010	25/3	110/25	1	2.5	2	27	0/55	PA
5.840	526-9877-010	25/3	110/25	1	2.5	2	27	0/55	FS
5.920	526-9753-010	45/3	540/30	0.5	2.5	2	9.2	-20/85	FP
6.362	526-9754-010	45/3	540/30	0.5	2.5	2	9.2	-20/85	FP
6.622	526-9805-010	25/3	110/25	1	2.5	2	30	0/55	
6.622	526-9878-010	25/3	110/25	1	2.5	2	30	0/55	FS
7.774	526-9800-010	25/3	110/25	1	2.5	2	30	0/55	PA
7.774	526-9879-010	25/3	110/25	1	2.5	2	30	0/55	FS
7.992	526-9755-010	45/3	540/30	0.5	2.5	2	9.2	-20/85	FP
8.398	526-9802-010	25/3	110/25	1	2.5	2	30	0/55	PA
8.398	526-9880-010	25/3	110/25	1	2.5	2	30	0/55	FS
8.761	526-9804-010	25/3	110/25	1	2.5	2	30	0/55	PA
8.761	526-9881-010	25/3	110/25	1	2.5	2	30	0/55	FS
8.880	526-9756-010	45/3	540/30	0.5	2.5	2	9.2	-20/85	FP
9.934	526-9806-010	25/3	110/25	1	2.5	2	20	0/55	PA
9.934	526-9882-010	25/3	110/25	1	2.5	2	20	0/55	FS
10.200	526-9775-010	8/3	100/40	0.5	7.0	2	18	0/60	FP
10.200	526-9965-010	9/3	400/60	0.5	7.0	2	30	-40/85	LC
10.200	526-9727-010	23/3	172/30	0.5	2.5	2	20	+10/40	FP
10.200	526-9964-010	25/3	400/60	0.5	2.5	2	30	-40/85	FP
10.200	526-9780-010	40/3	350/30	0.5	2.5	2	20	+10/40	FP
10.200	526-9861-010	70/3	420/25	0.5	2.5	2	20	-55/90	FP
10.200	526-9935-010	50/3	420/25	0.5	2.5	2	20	-20/90	LC
10.200	526-9946-010	100/3	660/30	0.5	3.5	2	20	0/60	LC
10.200	526-9916-010	120/3	800/30	0.5	3.5	2	20	-55/85	FP
11.333	526-9965-020	9/3	400/60	0.5	7.0	2	30	-40/85	LC
11.333	526-9727-040	22/3	172/30	0.5	2.5	2	20	+10/40	FP
11.333	526-9964-020	25/3	400/40	0.5	2.5	2	30	-40/85	FP
11.333	526-9727-030	46/3	344/30	0.5	2.5	2	20	+10/40	FP
11.333	526-9935-020	50/3	420/25	0.5	2.5	2	20	-20/90	LC
11.333	526-9861-020	70/3	420/25	0.5	2.5	2	20	-55/90	FP
11.333	526-9916-020	120/3	800/30	0.5	3.5	2	20	-55/85	FP
13.600	526-9965-030	9/3	400/60	0.5	7.0	2	30	-40/85	LC
13.600	526-9964-030	25/3	400/40	0.5	2.5	2	30	-40/85	FP
13.600	526-9950-030	25/3	240/50	0.5	2.5	3	20	-20/65	LC
13.600	526-9727-020	28/3	210/30	0.5	2.5	2	20	+10/40	FP
13.600	526-9861-030	70/3	420/25	0.5	2.5	2	20	-55/90	FP
13.600	526-9935-030	50/3	420/25	0.5	2.5	2	20	-20/90	LC
13.600	526-9916-030	120/3	800/3	0.5	3.5	2	20	-55/85	FP
16.000	526-9830-010	35/3	260/30	0.5	3.5	2	18	0/55	FP
17.000	526-9915-010	35/3	260/30	0.5	3.5	2	18	0/50	FP
25.000	526-9761-010	600/3	4000/25	1.0	3.5	2	5.6	0/60	FP
30.525	526-9763-010	400/3	4500/40	0.5	3.5	2	9.2	-10/50	FP
31.250	526-9762-010	600/3	4000/25	1.5	3.5	2	3.3	0/60	FP
39.250	526-9826-010	750/3	6000/30	2.0	3.5	2	8.2	0/60	FP

Low Frequency Narrowband Mechanical Filters Case Styles

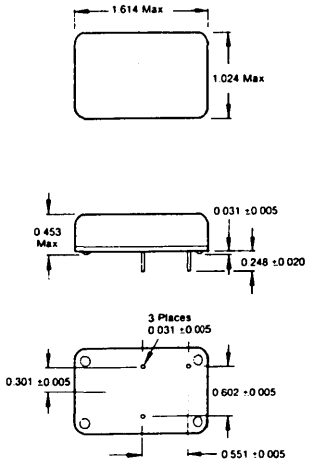
Case Style PA (Plastic)



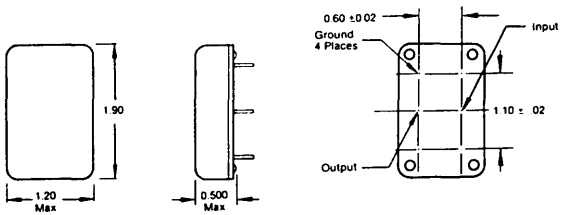
Case Style FP (Metal)



Case Style LC (Plastic)



Case Style FS



FURTHER INFORMATION

For technical information on Rockwell filter products or to discuss a filter to your specifications, contact

Rockwell International
Filter Products
4311 Jamboree Road
Newport Beach, CA 92660

or phone 714/833-4324 or 714/833-4544. To order, phone 714/833-4632 or contact your local Rockwell Representative.

FILTER
PRODUCTS

Notes

Notes

Notes

Notes

ELECTRONIC DEVICES DIVISION REGIONAL ROCKWELL SALES OFFICES

HOME OFFICE

Electronic Devices Division
Rockwell International
3310 Miraloma Avenue
P.O. Box 3669
Anaheim, California 92803
(714) 632-3729
TWX: 910 591-1698

UNITED STATES

Electronic Devices Division
Rockwell International
1842 Reynolds
Irvine, California 92626
(714) 632-3710
DDD (714) 545-6227

Electronic Devices Division
Rockwell International
921 Bowser Road
Richardson, Texas 75080
(214) 996-6500
Telex: 73-307

Electronic Devices Division
Rockwell International
10700 West Higgins Rd., Suite 102
Rosemont, Illinois 60018
(312) 297-8862
TWX: 910 233-0179 (RI MED ROSM)

Electronic Devices Division
Rockwell International
5001B Greentree
Executive Campus, Rt. 73
Marlton, New Jersey 08053
(609) 596-0090
TWX: 710 940-1377

EUROPE

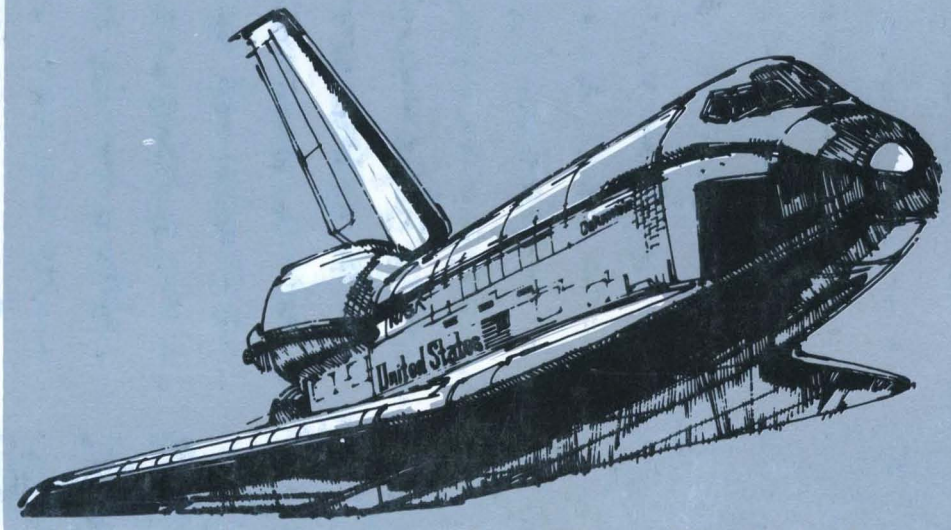
Electronic Devices Division
Rockwell International GmbH
Fraunhoferstrasse 11
D-8033 Munchen-Martinsried
Germany
(089) 859-9575
Telex: 0521/2650

Electronic Devices Division
Rockwell International
Heathrow House, Bath Rd.
Cranford, Hounslow,
Middlesex, England
(01) 759-9911
Telex: 851-25463

FAR EAST

Electronic Devices Division
Rockwell International Overseas Corp.
Itohpia Hirakawa-cho Bldg.
7-6, 2-chome, Hirakawa-cho
Chiyoda-ku, Tokyo 102, Japan
(03) 265-8806
Telex: J22198

YOUR LOCAL REPRESENTATIVE



A heritage of unsurpassed quality and technical excellence

Electronic Devices Division
3310 Miraloma Avenue
P.O. Box 3669
Anaheim, CA 92803

Toll Free (800) 854-8099
in California (800) 422-4230

Rockwell International

Document No. 1
Rev. 2, June 1981